65 W auxiliary power supply using CoolSET™ ICE502LD

EVAL_65WT1_FF_502LD

About this document

Scope and purpose

This document demonstrates high-input-voltage 65 W DC link auxiliary power supply designs using Infineon's CoolSET™ ICE502LD switching controller and CoolSiC™ IMWF170R1K0M1 1700 V MOSFET in TO-247 package in a single-switch flyback topology. The document can support designers targeting three-phase converters that include solar inverters, energy storage, EV chargers, UPS, and motor drives.

The evaluation board is designed to showcase the performance of the CoolSET™ ICE502LD switching controller.

Intended audience

This document is intended for design engineers of auxiliary power supply designs in three-phase converters with Infineon's CoolSET™ ICE502LD PWM Fixed Frequency (FF) Gen5 Pro controller and CoolSiC™ 1700 V MOSFET.

Keypoints

- Demonstrates design of a 65 W high-voltage auxiliary power supply using ICE502LD controller and CoolSiC™ MOSFET
- Explains implementation of single-switch flyback topology with secondary-side regulation and optional primary-side control
- Describes key features such as selectable gate voltage, frequency foldback, jittering, and active burst mode for efficiency and EMI reduction
- Provides comprehensive protection strategies including line overvoltage, VCC OVP/UVLO, overload, and thermal safeguards
- Presents test results on efficiency, regulation, thermal performance, and dynamic response for three-phase converter applications

About this product family

CoolSET™ product family

Infineon's CoolSET™ integrated power stages in a fixed-frequency switching scheme offers increased robustness and outstanding performance. This family offers superior energy efficiency, comprehensive protective features, and reduced system costs, and is ideally suited for auxiliary power supply applications in a wide variety of potential applications such as:

- SMPS
- Renewables
- Server
- Telecom
- Home appliances

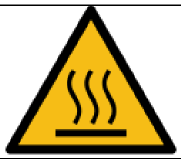
Table of contents

Table of contents

Safety precautions

Note: Please note the following warnings regarding the hazards associated with development systems.

Table 1 Safety Precautions

	**Warning:** *The DC link potential of this board is up to 1000 VDC. When measuring voltage waveforms by oscilloscope, high voltage differential probes must be used. Failure to do so may result in personal injury or death.*
	**Warning**: *The evaluation or reference board contains DC bus capacitors which take time to discharge after removal of the main supply. Before working on the drive system, wait five minutes for capacitors to discharge to safe voltage levels. Failure to do so may result in personal injury or death. Darkened display LEDs are not an indication that capacitors have discharged to safe voltage levels.*
	**Warning:** *Remove or disconnect power from the drive before you disconnect or reconnect wires, or perform maintenance work. Wait five minutes after removing power to discharge the bus capacitors. Do not attempt to service the drive until the bus capacitors have discharged to zero. Failure to do so may result in personal injury or death.*
	**Caution:** *The heat sink and device surfaces of the evaluation or reference board may become hot during testing. Hence, necessary precautions are required while handling the board. Failure to comply may cause injury.*
	**Caution:** *Only personnel familiar with the drive, power electronics and associated machinery should plan, install, commission and subsequently service the system. Failure to comply may result in personal injury and/or equipment damage.*
	**Caution:** *The evaluation or reference board contains parts and assemblies sensitive to electrostatic discharge (ESD). Electrostatic control precautions are required when installing, testing, servicing or repairing the assembly. Component damage may result if ESD control procedures are not followed. If you are not familiar with electrostatic control procedures, refer to the applicable ESD protection handbooks and guidelines.*
	**Caution:** *A drive that is incorrectly applied or installed can lead to component damage or reduction in product lifetime. Wiring or application errors such as undersizing the motor, supplying an incorrect or inadequate AC supply, or excessive ambient temperatures may result in system malfunction.*
	**Caution:** *The evaluation or reference board is shipped with packing materials that need to be removed prior to installation. Failure to remove all packing materials that are unnecessary for system installation may result in overheating or abnormal operating conditions.*

1 Introduction

The EVAL_65WT1_FF_502LD evaluation board was developed to support customers designing auxiliary power supplies for three-phase converters using CoolSET™ ICE502LD PWM Fixed Frequency Gen5 Pro controller and CoolSiC™ 1700 V MOSFET in a single-switch flyback topology. The board has triple outputs (+12 V, +5 V, and -12 V) with up to 65 W output power working in a wide input voltage range from 200 V_{DC} to 1000 V_{DC}. Its potential applications are three-phase systems having a high input voltage DC link. This application note contains an overview of the evaluation board's operation, product information, and technical details with measurement results. This information can help customers during their design-in phase, and for reuse of the board for their own specific requirements.

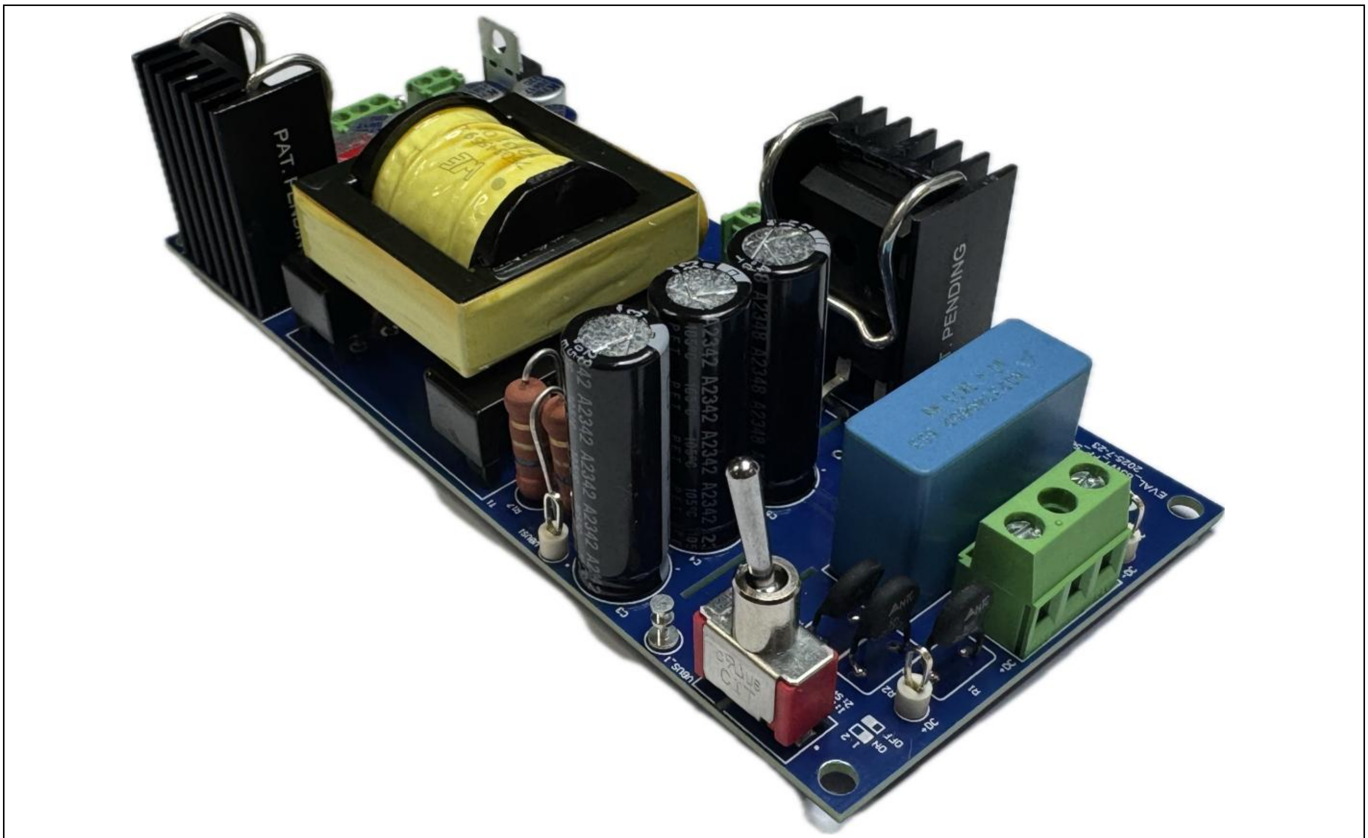


Figure 1 EVAL_65WT1_FF_502LD evaluation board

2 EVAL_65WT1_FF_502LD evaluation board overview

2.1 Board features

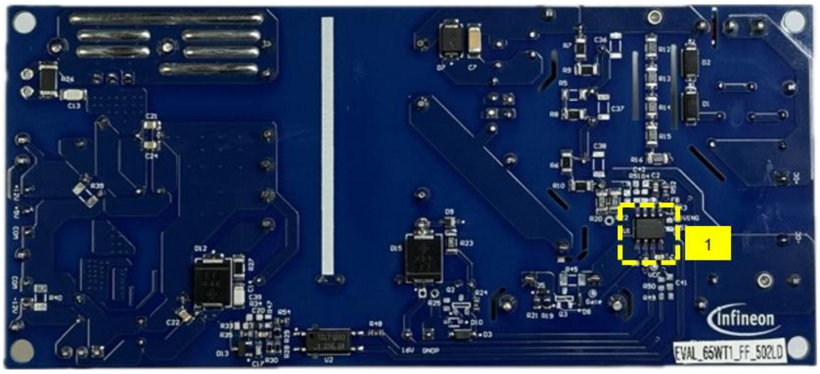
Key features of the controller ICE502LD used in the evaluation board are:

- Externally selectable gate voltage of 10 V, 15 V, and 18 V
- Fast startup through cascode configuration
- Integrated error amplifier to implement primary side control, if required
- Frequency reduction for improved light-load efficiency
- Comprehensive protection including line overvoltage protection

2.2 Board details

1. Input voltage connector
2. CoolSiC™ 1700V MOSFET
3. Output voltage −12 V connector
4. Output voltage +12 V, +5 V connector

Figure 2 Board top side



1. CoolSET™ ICE502LD PWM Fixed Frequency Gen5 Pro controller

Figure 3 Board bottom side

2.3 EVAL_65WT1_FF_502LD technical specifications

The EVAL_65WT1_FF_502LD evaluation board is intended to support customers designing an auxiliary power supply for three-phase converters using the Infineon's CoolSET™ ICE502LD PWM Fixed Frequency Gen5 Pro controller and CoolSiC™ 1700 V MOSFET. Potential applications include solar inverters, energy storage, EV chargers, UPS, and motor drives. Table 2 lists the key specifications of the board.

Table 2 EVAL_65WT1_FF_502LD evaluation board specifications

Input voltage	200 V_{DC} to 1000 V_{DC}
Output power	65 W
Topology	Single-switch flyback
Output voltages and currents	+12 V/4.2 A, –12 V/0.42 A, +5 V/2 A
Switching frequency	65 kHz with frequency foldback for lighter loads
Efficiency at full load	>80%
Regulation	Secondary-side regulated control
PWM gate voltage	15 V
Protections	All as mentioned in the datasheet with line OVP set to 1050 V
Transformer	ETD34, $L_{primary}$ = 380 µH, 40:5:5:6
Isolation	Reinforced, 6 kV
Form-factor case size (L x W x H)	134 mm x 60 mm x 32 mm

2.4 Wiring

Input and output wiring		Ensure that there is no loose wire connections. Recommendation is not to use too exposed wire for input connection to prevent accidental shorting.
S1 Switch ON		Bypass the NTCs R1, R2, R3 and diodes D1 and D2 for efficiency measurement. Ensure not to apply reverse polarity at the input.
S1 Switch OFF		In case of non-efficiency related measurements, keep the switch in the off state to protect the board under accidental reverse polarity input connection.
WARNING: DO NOT CHANGE THE POSITION OF THE SWITCH IN RUNNING CONDITION. ENSURE THAT THE INPUT IS DISCONNECTED AND INPUT BULK CAPACITOR IS COMPLETELY DISCHARGED BEFORE CHANGING THE SWITCH STATE.		

Figure 4 Wiring diagram

2.5 Schematic

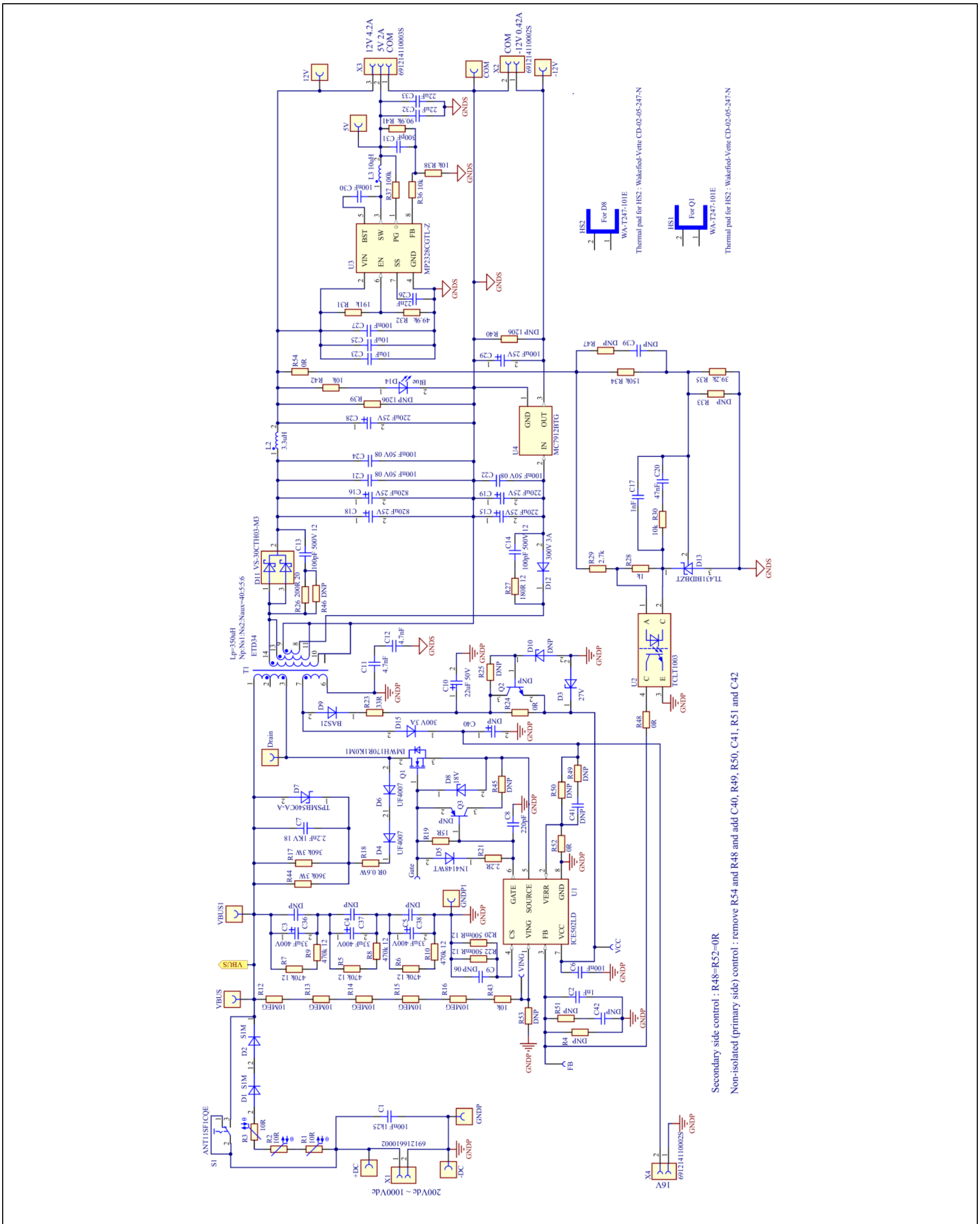


Figure 5 Schematic

2.6 PCB Layout

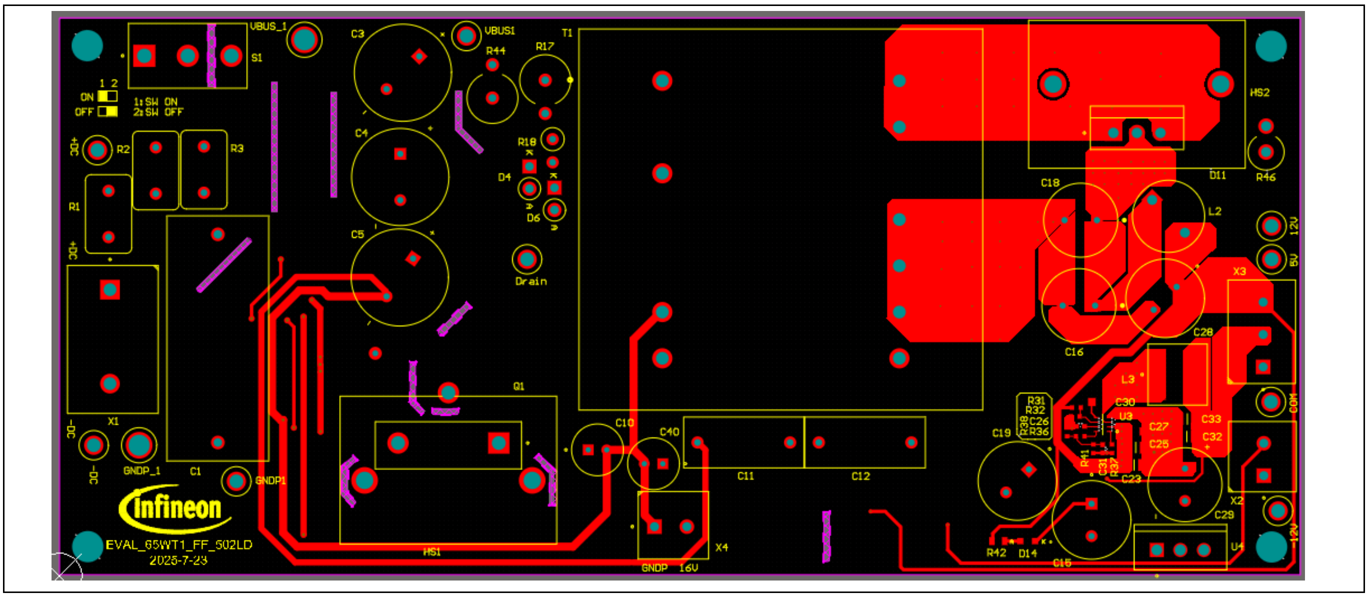


Figure 6 **Top side**

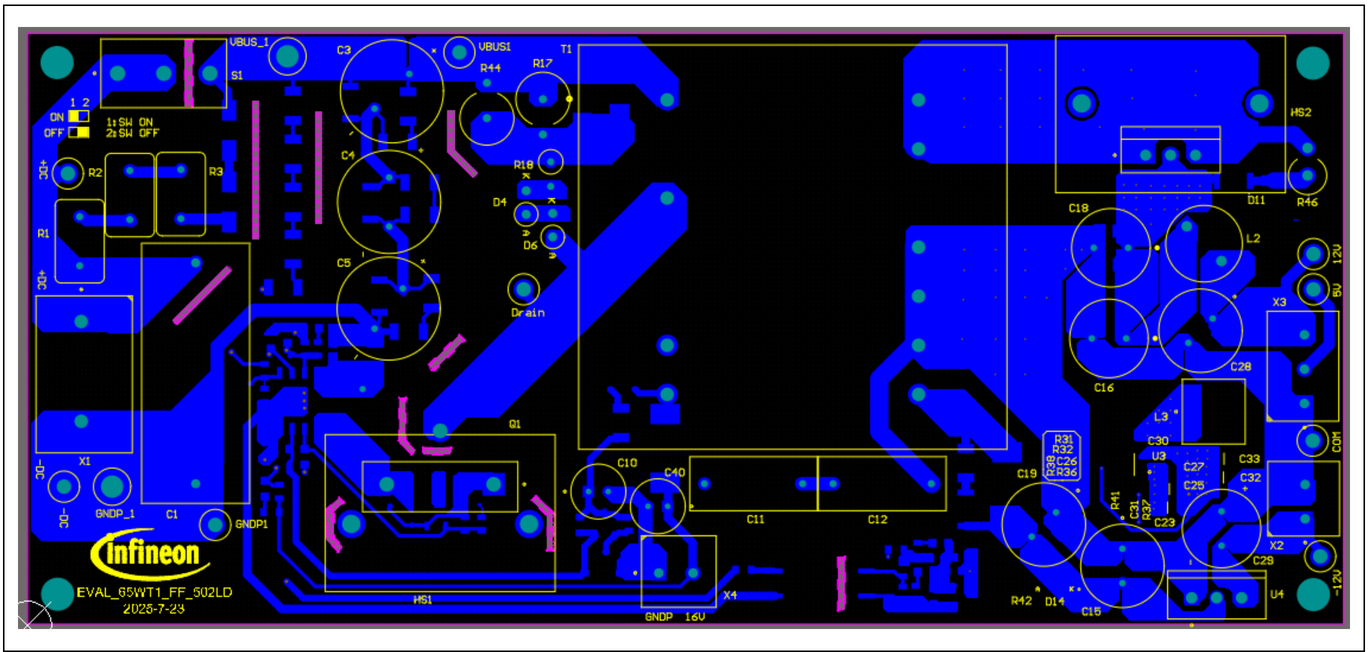


Figure 7 **Bottom side**

2.7 Bill of Material

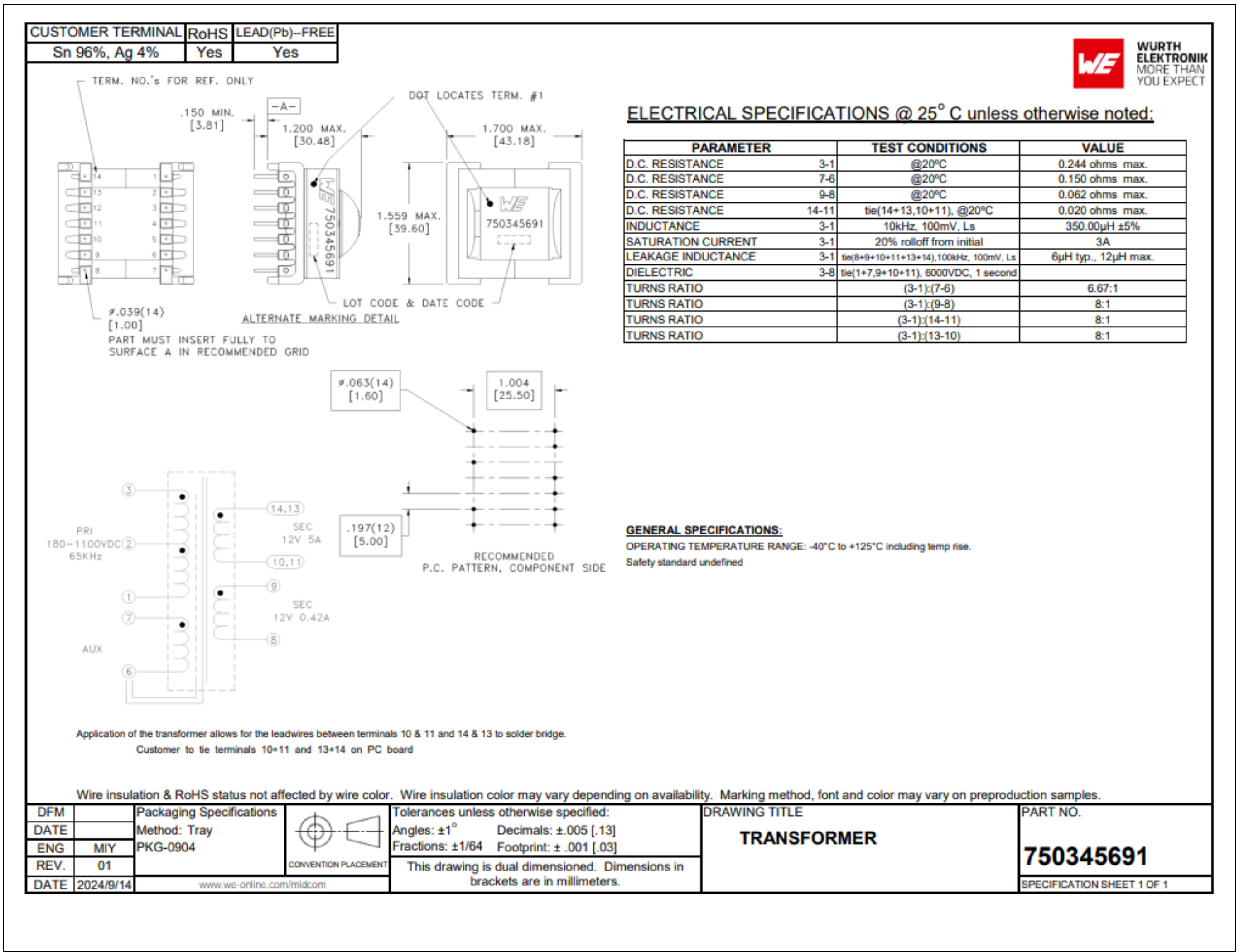
Table 3 Bill of materials

Item	Designator	Quantity	Value	Package	Manufacturer	Manufacturer order number
1	C1	1	100nF 1k25	–	–	B32653A7104J
2	C10	1	22uF 50V	–	–	50PX22MEFC5X11
3	C11, C12	2	4.7nF	–	–	VY1472M51Y5VQ63V0
4	C13, C14	2	100pF 500V 12	1206	–	CC1206JRNPOBBN101
5	C15, C19, C28	3	220uF 25V	–	–	A750KS227M1EEAE015
6	C16, C18	2	820uF 25V	–	–	RPF0816821M025K
7	C17	1	1nF	0603	–	GRM1885C1H102JA01
8	C2	1	1nF	0603	–	GRM188R71C102KA01
9	C20	1	47nF	0603	–	GRM188R71E473KA01
10	C21, C22, C24	3	100nF 50V 08	0805	–	C0805C104J5RAC
11	C23, C25	2	10uF	0805	–	GRM219R61E106KA12
12	C26	1	22nF	0402	–	GRM155R61C223KA01
13	C27, C30	2	100nF	0603	–	C0603C104J3RAC
14	C29	1	100uF 25V	–	–	A750KK107M1EAAE040
15	C3, C4, C5	3	33uF 400V	–	–	400BXW33MEFR10x30
16	C31	1	300pF	0402	–	GRM1555C1E301JA01
17	C32, C33	2	22uF	0805	–	GRM21BR61C226ME44
18	C36, C37, C38	3	DNP	–	–	–
19	C39	1	DNP	–	–	–
20	C40	1	DNP	–	–	–
21	C41	1	DNP	–	–	–
22	C42	1	DNP	–	–	–
23	C6	1	100nF	0603	–	06035C104K4Z2A
24	C7	1	2.2nF 1KV 18	1808	–	1808AC222KAT1A
25	C8	1	220pF	0603	–	GRM1885C1H221GA01
26	C9	1	DNP	–	–	–
27	D1, D2	2	S1M	–	–	S1M-13-F
28	D10	1	DNP	–	–	–
29	D11	1	VS-30CTH03-M3	–	–	VS-30CTH03-M3
30	D12, D15	2	300V 3A	–	–	ES3F-E3/57T
31	D13	1	TL431BIDBZT	–	–	TL431BIDBZT
32	D14	1	Blue	–	Würth Elektronik	150060RS75003

Item	Designator	Quantity	Value	Package	Manufacturer	Manufacturer order number
33	D3	1	27V Zener	–	–	BZT52C27W
34	D4, D6	2	UF4007	–	–	UF4007-E3/54
35	D5	1	1N4148WT	–	–	1N4148WT-7
36	D7	1	TPSMB540CA-A	–	–	TPSMB540CA-A
37	D8	1	18V	–	–	SZMM5Z18VT1G
38	D9	1	BAS21	–	–	BAS21-03W or BAS21HT1G
39	HS1, HS2	2	WA-T247-101E	–	–	WA-T247-101E
40	L2	1	3.3uH	–	–	RLB9012-3R3ML
41	L3	1	10uH	–	–	MPL-AL6060-100
42	Q1	1	IMWH170R1K0M1	–	Infineon Technologies	IMWH170R1K0M1
43	Q2	1	DNP	–	–	–
44	Q3	1	DNP	–	–	–
45	R1, R2, R3	3	10R	–	–	B57153S0100M000
46	R12, R13, R14, R15, R16	5	10MEG	–	–	MCHVR06FTFV1005
47	R17, R44	2	360k 3W	–	–	RR03J360KTB
48	R18	1	0R 0.6W	–	–	MBB02070Z0000ZCT00
49	R19	1	15R	0603	–	CRCW060315R0FK
50	R20, R22	2	500mR 12	1206	–	RL1206FR-070R5L
51	R21	1	2.2R	0603	–	CRCW06032R20FK
52	R23	1	33R	1206	–	AC1206JR-0733RL
53	R24, R48	2	0R	0603	–	RC0603JR-070RL
54	R25	1	DNP	–	–	–
55	R26	1	200R 20	2010	–	CRCW2010200RFK
56	R27	1	180R 12	1206	–	CRCW1206180RFK
57	R28	1	1k	0603	–	CRCW06031K00FK
58	R29	1	2.7k	0603	–	CRCW06032K70FK
59	R30, R42, R43	3	10k	0603	–	CRCW060310K0FKEA
60	R31	1	191k	0402	–	CRCW0402191KFK
61	R32	1	49.9k	0402	–	CRCW040249K9FK
62	R33	1	DNP	–	–	–
63	R34	1	150k	0603	–	CRCW0603150KFK
64	R35	1	39.2k	0603	–	RN73C1J39K2BTDF
65	R36, R38	2	10k	0402	–	CRCW040210K0FK
66	R37	1	100k	0402	–	CRCW0402100KFK

Item	Designator	Quantity	Value	Package	Manufacturer	Manufacturer order number
67	R39, R40	2	DNP 1206	1206	–	DNP
68	R4, R47	2	DNP	–	–	-
69	R41	1	90.9k	0402	–	CRCW040290K9FK
70	R45	1	DNP	–	–	–
71	R46	1	DNP	–	–	–
72	R49	1	DNP	–	–	–
73	R5, R6, R7, R8, R9, R10	6	470k 12	1206	–	CRCW1206470KFKEA
74	R50	1	DNP	–	–	–
75	R51, R53	2	DNP	–	–	–
76	R52	1	0 R	0603	–	CRCW06030000Z0EA
77	R54	1	0R	0603	–	AC0603JR-070RL
78	S1	1	ANT11SF1CQE	–	–	ANT11SF1CQE
79	T1	1	ETD34	–	Würth Elektronik	750345961 Rev01
80	U1	1	ICE502LD	–	Infineon Technologies	ICE502LD
81	U2	1	TCLT1003	–	–	TCLT1003
82	U3	1	MP2328CGTL-Z	–	–	MP2328CGTL-Z
83	U4	1	MC7912BTG	–	–	MC7912BTG
84	X1	1	691216610002	–	Würth Elektronik	691216610002
85	X2, X4	2	691214110002S	–	Würth Elektronik	691214110002S
86	X3	1	691214110003S	–	Würth Elektronik	691214110003S
87	-12V, +DC, 5V, 12V, COM, -DC, Drain, GNDP1, VBUS1	9	5012	–	–	5012
88	VBUS_1, GNDP_1	2	1502-2	–	–	1502-2
89	Thermal pad for D11, Q1	2	TO220/TO247 Thermal pad	–	–	CD-02-05-247-N
90	Thermal grease for HS1 and HS2	thin layer	Thermal grease	–	–	S606 or equivalent

2.8 Transformer construction



PARAMETER		TEST CONDITIONS	VALUE
D.C. RESISTANCE	3-1	@20ºC	0.244 ohms max.
D.C. RESISTANCE	7-6	@20ºC	0.150 ohms max.
D.C. RESISTANCE	9-8	@20ºC	0.062 ohms max.
D.C. RESISTANCE	14-11	tie(14+13,10+11), @20ºC	0.020 ohms max.
INDUCTANCE	3-1	10kHz, 100mV, Ls	350.00µH ±5%
SATURATION CURRENT	3-1	20% rolloff from initial	3A
LEAKAGE INDUCTANCE	3-1	tie(8+9+10+11+13+14),100kHz, 100mV, Ls	6µH typ., 12µH max.
DIELECTRIC	3-8	tie(1+7,9+10+11), 6000VDC, 1 second	
TURNS RATIO		(3-1):(7-6)	6.67:1
TURNS RATIO		(3-1):(9-8)	8:1
TURNS RATIO		(3-1):(14-11)	8:1
TURNS RATIO		(3-1):(13-10)	8:1

Figure 8 Transformer datasheet

Table 4 Transformer specifications

Manufacturer and part number	Wurth 750345691
Core size	ETD 34
Core material	DMR95
Bobbin	14 pin ETD34 Horizontal
Primary inductance	350 µH
Leakage inductance	< 10 µH
Turns ratio (Primary: +12 Vout secondary: –12 Vout secondary: auxiliary)	40:5:5:6

3 Circuit description

3.1 Startup

Startup is implemented using the cascode method. When a sufficient line voltage is applied, a pull-up resistor at the VING pin (R12, R13, R14, R15, R16, and R43) from the system bus provides a current to turn on the external CoolSiC™ device (Q1). Q1 is operated in linear mode to charge the VCC capacitor until the VCC voltage reaches V_{VCC_ON}.

Soft start commences after V_{VCC_ON}. The soft start implemented in ICE502LD is a digital time-based function. The preset soft-start time is 12 ms with four steps. If not limited by other functions, the peak voltage on the CS pin will increase in increments from 0.3 V to 0.8 V (V_{CS_N}). The VCC voltage is supplied by the auxiliary winding of the transformer. VCC short-to-GND protection is implemented during the startup time.

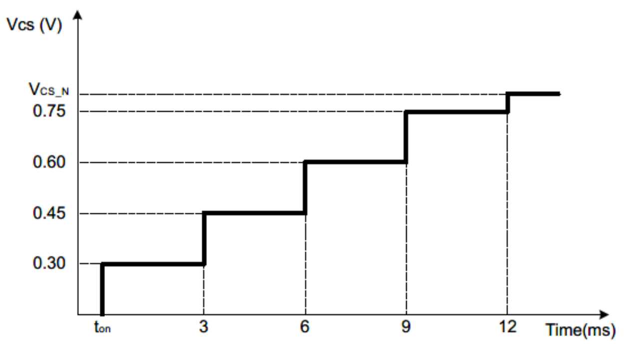


Figure 9 Soft-start phase

If LOVP is not required and should be disabled, the VING pin can be connected to ground. In that case, startup can be done via a pull-up resistor from the DC bus to the Gate pin of the controller as shown in the schematic (Figure 10).

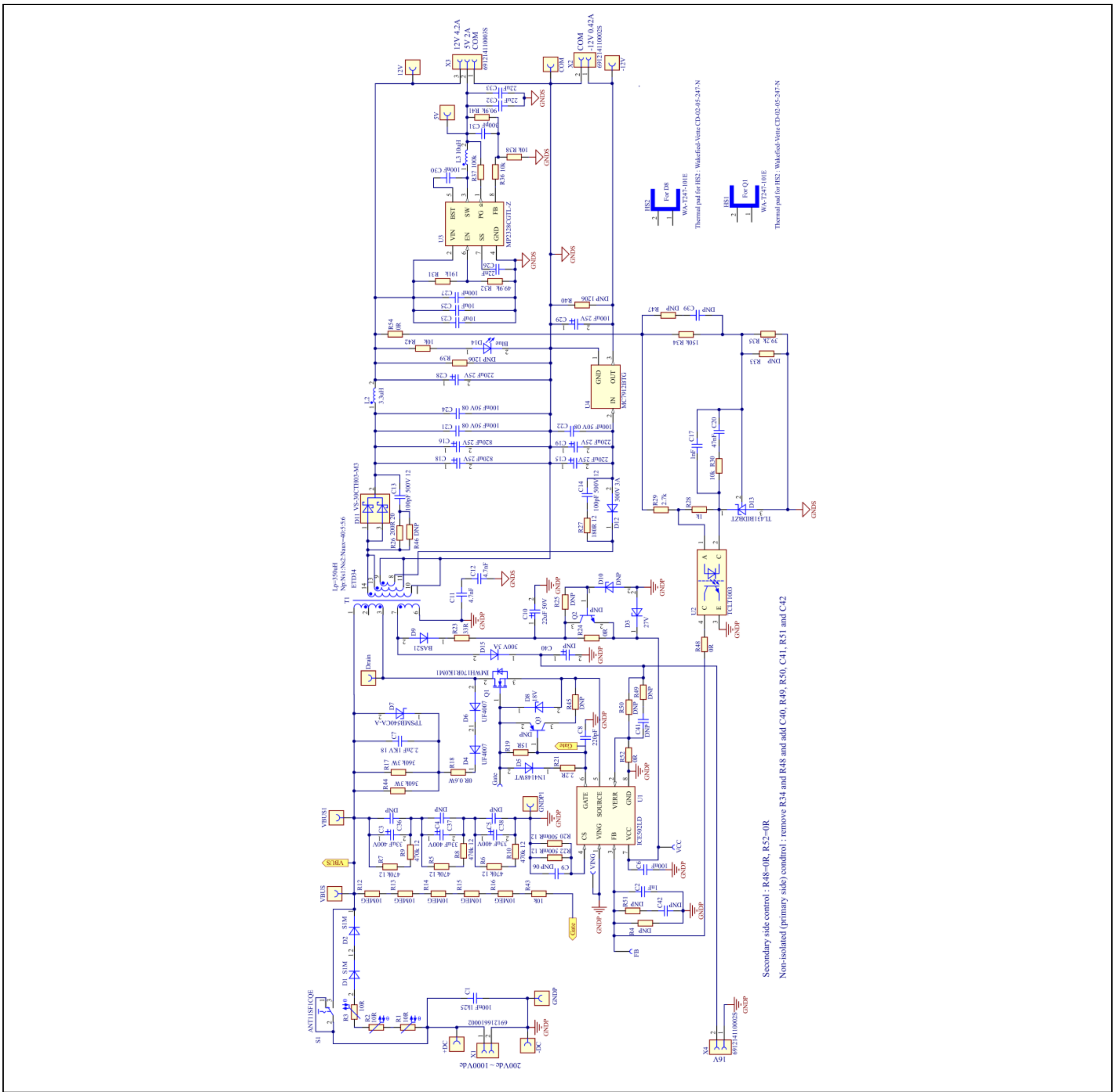


Figure 10 Secondary-side regulated isolated flyback design with line OVP disabled

3.2 Selectable gate drive voltage

One of the unique features of ICE502LD is that it allows selectable gate voltage to drive a variety of switches (both Si and CoolSiC™). The gate voltage can be selected by changing the RSEL at the FB pin. There are three configuration options for different V_{GATE} gate drive voltages. Table 5 shows the control logic for the selection of gate voltage with RSEL.

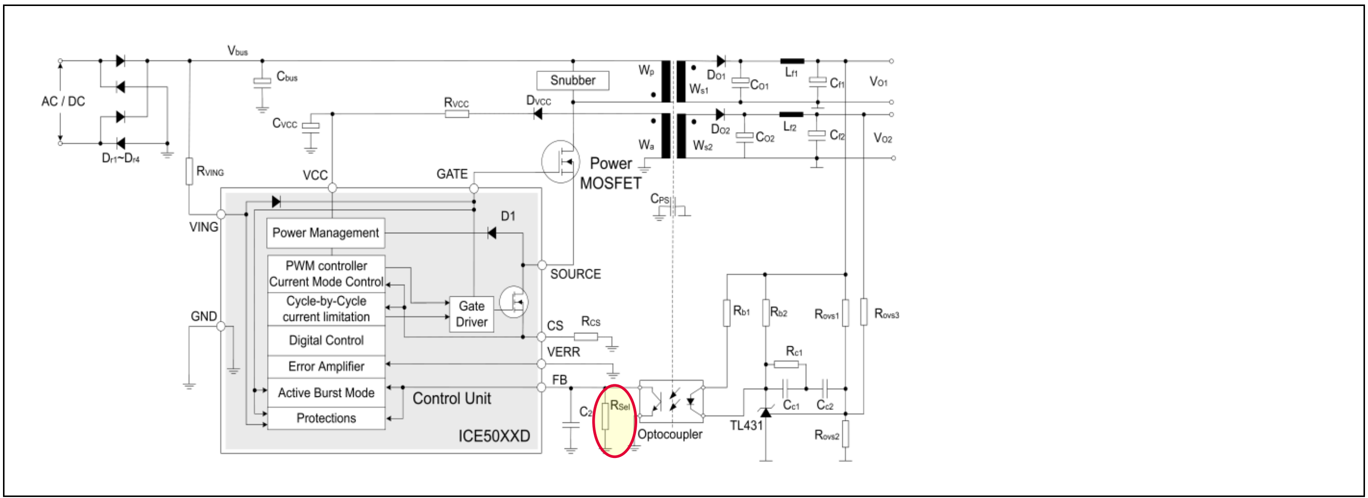


Figure 11 RSEL for selecting gate drive voltage

Table 5 Gate drive voltage selection

Option	RSEL	V_{GATE}
1	300 kΩ ~ 502 kΩ	10 V
2	721 kΩ ~ 797 kΩ	18 V
3	> 1.14 MΩ or open	15 V

3.3 Frequency reduction control

ICE502LD uses a peak current mode control scheme. When operating at maximum power, the switching frequency is f_{OCX} (65 kHz for ICE502LD). As the load reduces, the feedback voltage also reduces. In order to improve the efficiency for light loads, a frequency foldback scheme is introduced. The frequency keeps reducing as the load becomes lighter until it reaches the minimum switching frequency f_{OSCX_MIN}. If the load is reduced further, the controller enters active burst mode (ABM) where the switching frequency is clamped to f_{OCX_ABM} and V_{CS} is limited by V_{CS_B}. The controller is capable of supporting continuous conduction mode (CCM) at low-line, heavy load conditions to improve efficiency. Figure 12 shows the frequency reduction curve.

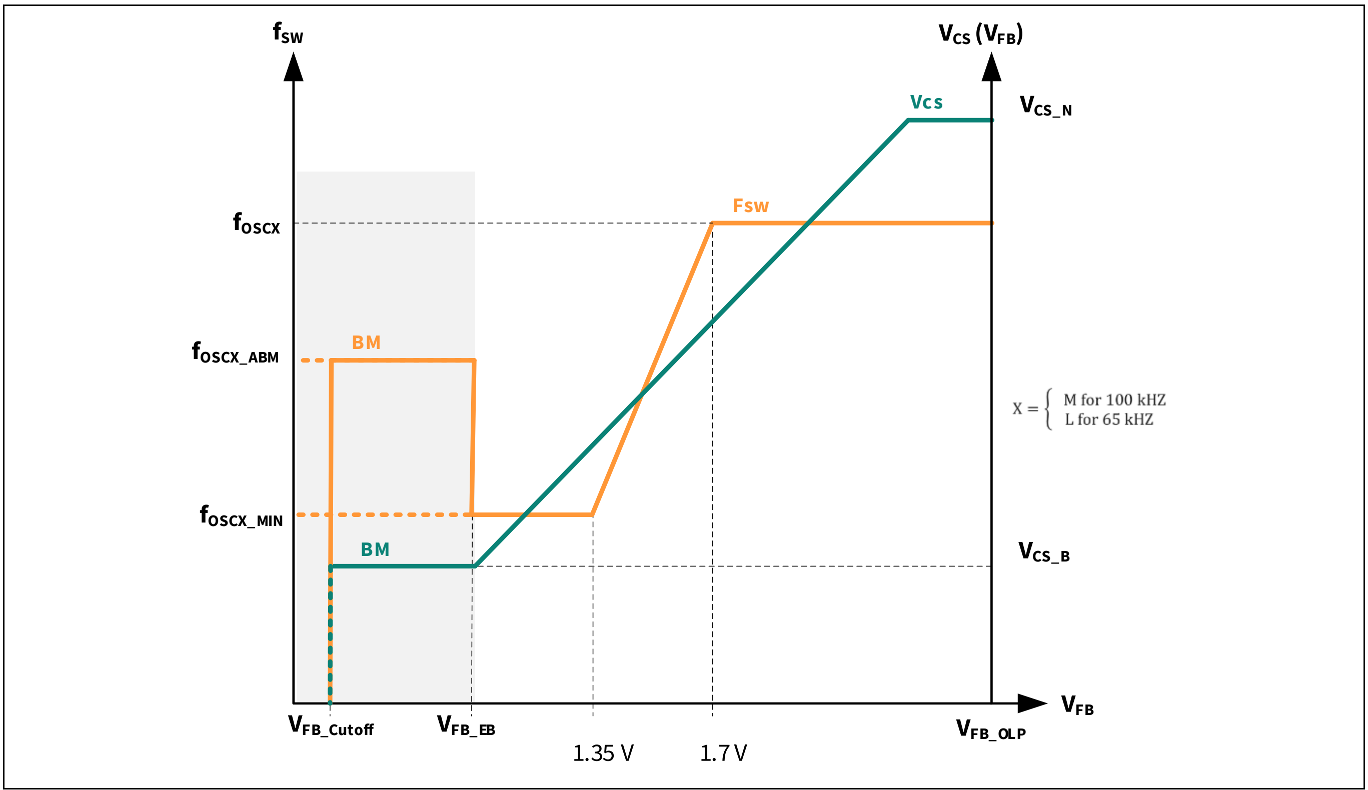


Figure 12 **Frequency reduction curve**

3.4 Frequency jittering

ICE502LD has a frequency jittering feature to reduce the EMI noise. The jitter frequency is internally set at 65 kHz (±4 kHz) and the jitter period is 4 ms.

3.5 RCD clamper circuit

A clamper network (R17, R44, C7, D4, D6, and D7) dissipates the energy of the leakage inductance and suppresses the ringing on the SMPS transformer.

3.6 Output stage

There are three outputs on the secondary side: +12 V, +5 V and –12 V. The +5 V output is derived from the +12 V supply using a DC-DC converter(MP2328CGTL-Z). The output capacitors selected must have an internal resistance (ESR) as low as possible to minimize the output voltage ripple caused by the triangular current.

3.7 Feedback loop

This evaluation board is designed for secondary-side regulation. For feedback (FB), the output is sensed by the voltage divider (R34 and R35) and compared to the D13 (TL431) internal reference voltage. The capacitors and resistor (C17, C20, and R30) form the compensation network. The output voltage of D9 (TL431) is converted to the current signal via the optocoupler U2 and two resistors R28 and R29 for regulation control.

If you are interested in designing using primary-side regulation instead, the evaluation board also has provisions to implement this configuration. Follow the instructions given in the Section 2.5

3.8 Active burst mode (ABM)

As mentioned in Section 0 and shown in Figure 12, under light-load conditions, the SMPS enters active burst mode (ABM) operation. At this stage, the controller is always active but keeps V_{VCC} above the switch-off threshold.

To enter ABM operation, two conditions apply:

- The FB voltage must be lower than the threshold of V_{FB_EB}
- A certain blanking time (t_{FB_BEB}) is required

Once both conditions are fulfilled, the ABM flip-flop is set and the controller enters ABM operation. This dual condition determines entering ABM operation and prevents mis-triggering of ABM so that the controller enters ABM operation only when the output power is really low.

During ABM, the maximum current sense (CS) voltage is reduced from V_{CS_B} to reduce the conduction loss and audible noise. The FB voltage changes like a sawtooth between $V_{FB\_Bon\_ISO}$ and $V_{FB\_Boff\_ISO}$. In the event of a heavy load jump, the controller exits ABM immediately when V_{FB} exceeds, V_{FB_LB} and transitions to maximum switching frequency and peak current limit (V_{CS_N}) to allow output voltage to recover quickly.

3.9 Line overvoltage protection

The CoolSET™ PWM FF Gen5 Pro product family implements line overvoltage protection and startup using the dual functionality of the VING pin. The current flowing into the VING pin (I_{VING}) is compared against a fixed reference (I_{VING_LOVP}). When I_{VING} is greater than I_{VING_LOVP}, line overvoltage protection is triggered. To avoid any noise coupling into the VING pin, ensure that the R_{VING} ladder is outside the switching power loop and no capacitor is connected from the VING pin to ground.

4 Protection features

ICE502LD provides comprehensive protection features to ensure the system is operating safely, including the following:

- Line overvoltage protection (LOVP)
- VCC overvoltage protection
- VCC undervoltage protection
- Overload protection
- Overtemperature protection for controller junction
- VCC short-to-GND protection

When these faults are detected, the system will enter protection mode. Once the fault is removed, the system resumes normal operation. The following table lists the protections and failure conditions.

Table 6 Protection behavior

Protection function	Protection trigger condition	Protection mode
Line overvoltage protection	$I_{VING} > I_{VING\_LOVP}$	Non-switch auto-restart
VCC overvoltage	$V_{VCC} > V_{VCC\_OVP}$	Extended cycle skip auto-restart
VCC undervoltage protection	$V_{VCC} < V_{VCCOFF}$	Auto-restart
Overload or open-loop protection	$V_{FB} > V_{FB\_OLP}$ and lasts for $t_{FB\_OLP\_B}$	Extended cycle skip auto-restart
Overtemperature protection	T_J > 140°C (40°C hysteresis)	Non-switch auto-restart
VCC short-to-GND protection (V_{VCC} = 0 V, R_{VING} = 20 MΩ and V_{DRAIN} = 90 V)	$V_{VCC} < V_{CC\_SCP}$	Cannot start up and I_{VCC} is limited to $I_{VCC\_Charge1}$

5 Test results

5.1 Efficiency

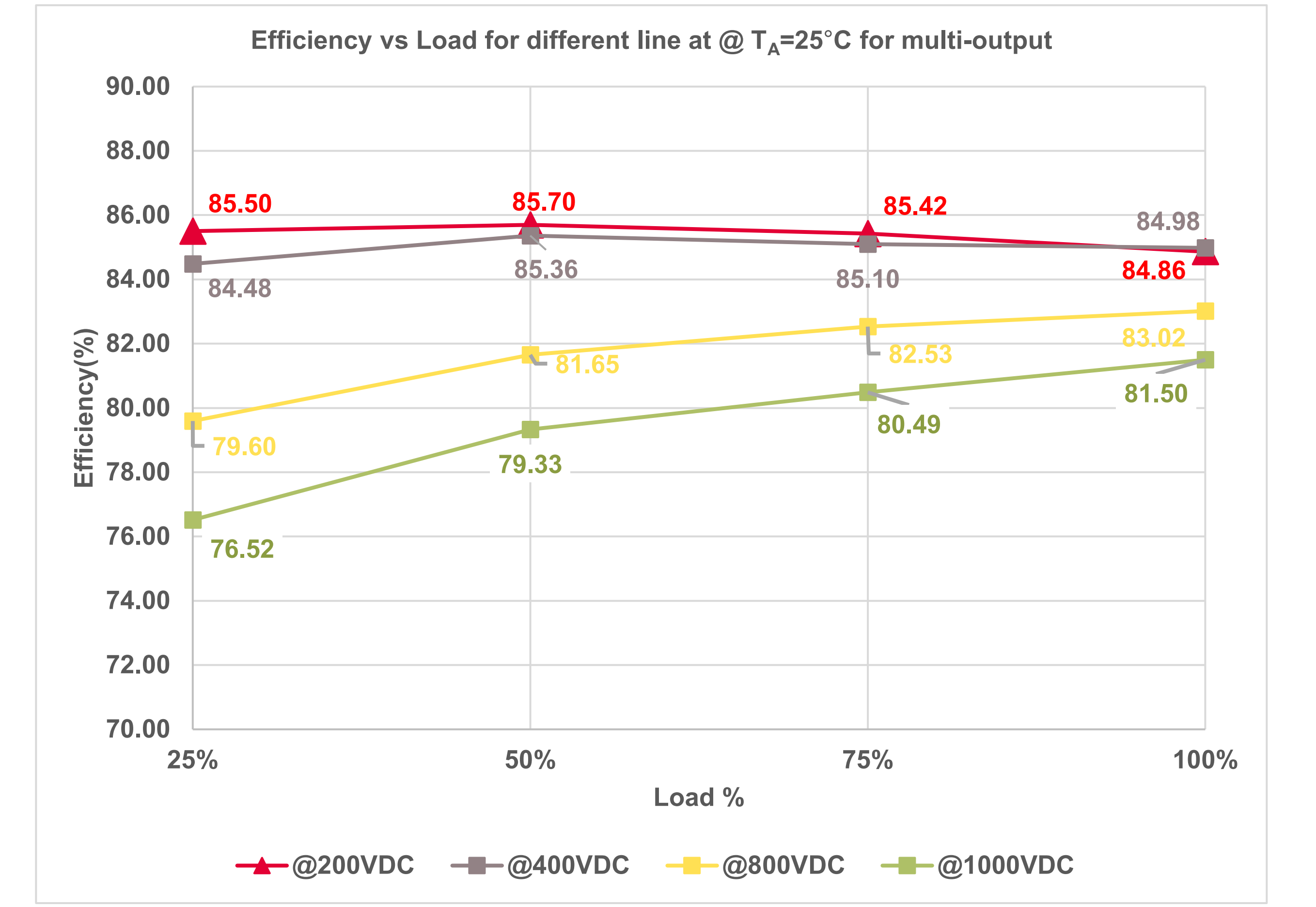


Figure 13 **Efficiency vs. load for different input voltages**

5.2 Load and line regulation

The graphs show the load and line regulation of the evaluation board. The load regulation shows the variation in output voltage with varying loads for different line conditions. Similarly, the line regulation shows the variation in output voltage with varying line voltages for different percentages of loading.

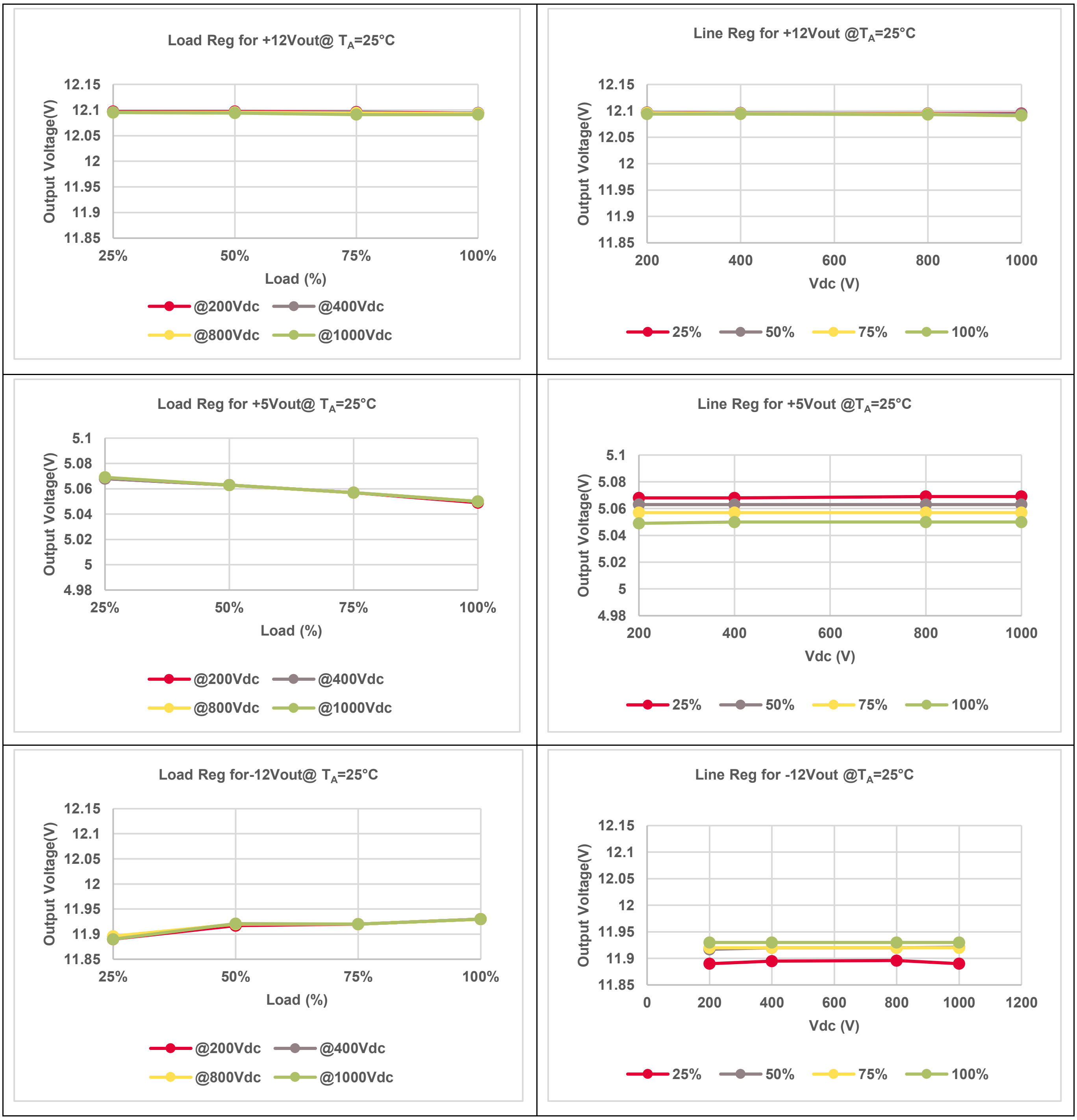


Figure 14 Load and line regulation

5.3 Thermal measurement

The thermal testing of the open-frame reference board is done using an infrared thermography camera (FLIR-T62101) at an ambient temperature of 25°C. The measurements are taken after one hour running at full load.

Table 7 Component thermals

No.	Major component	At 200 V_{DC}/full load (°C)	At 1000 V_{DC}/full load (°C)
1	CoolSiC™ IMWH170R1K0M1 (Q1) device	45	83
2	CoolSiC™ device heatsink (HS1)	47	87
3	Transformer core	68.4	86
4	Transformer winding	74	90
5	Output diode (D8)	93.8	95
6	Diode heatsink (HS2)	97	98
7	ICE502LD (U1)	53	65
8	RCD diode (D3,D5)	62.6	62.9
9	TVS diode (D6)	58	68
10	Snubber resistor (R23)	58	63

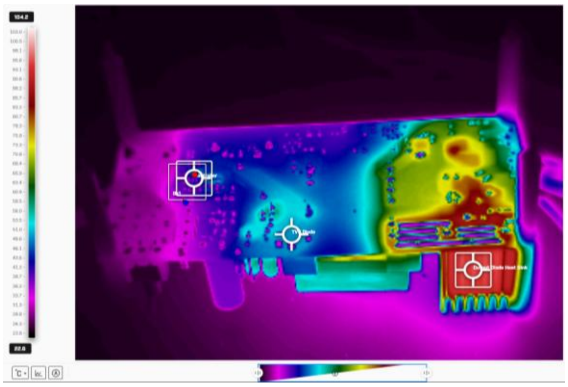
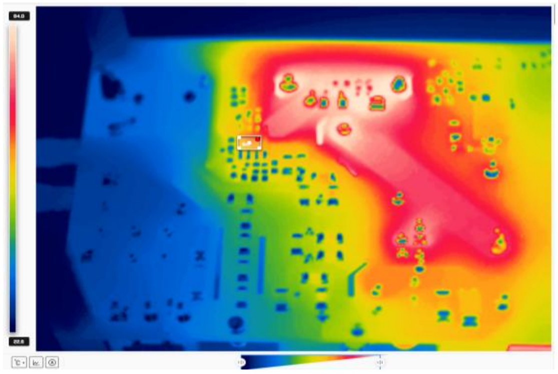
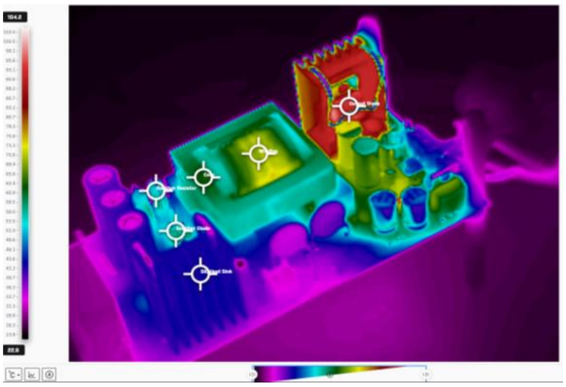
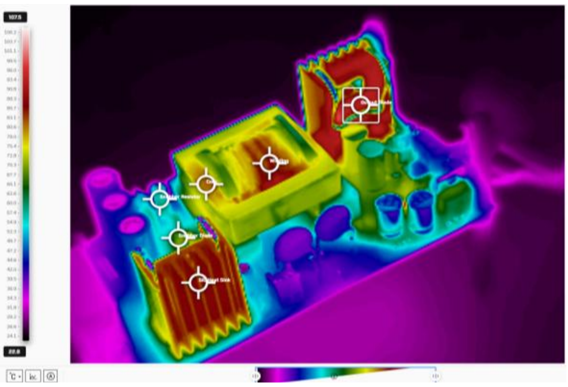
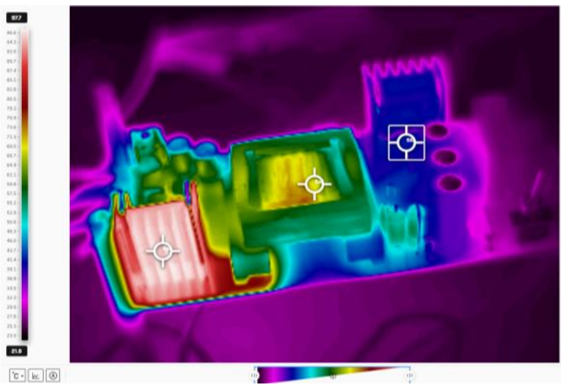
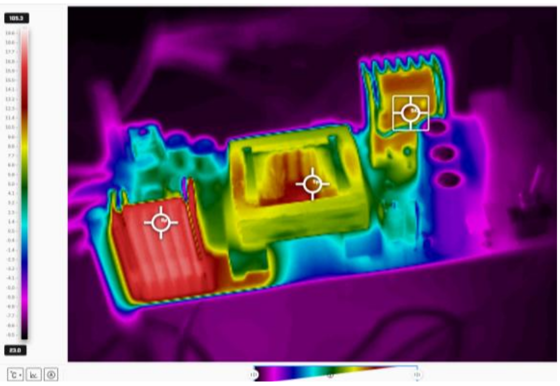
200 V_{DC} full load and 25°C ambient	1000 V_{DC} full load and 25°C ambient
 **Bottom side**	 **Bottom side**
 **Top side**	 **Top side**
 **Top side**	 **Top side**

Figure 15 Thermal images

6 Waveforms and scope plots

6.1 Startup at low/high DC line input voltage with maximum load

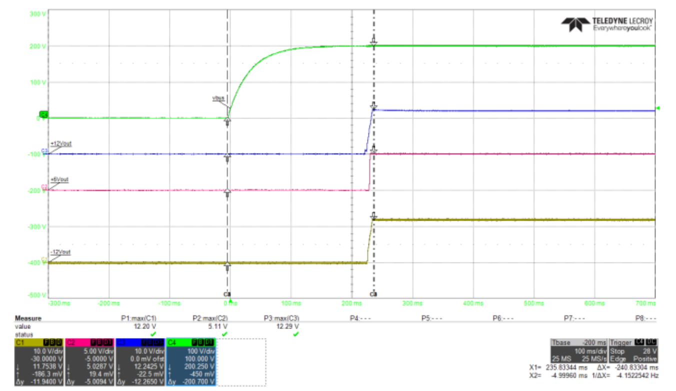
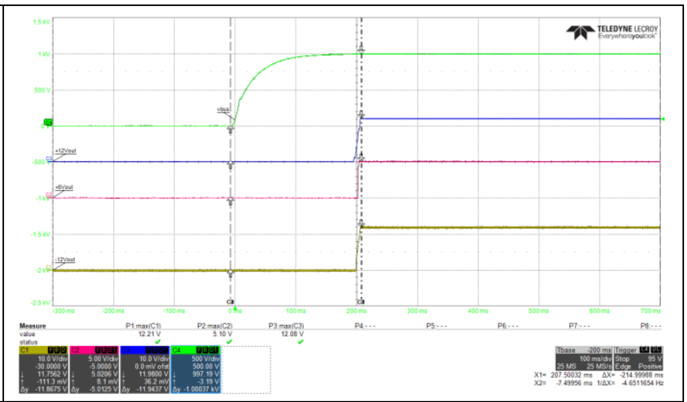
	
C1:-12 Vout C2:+5 Vout C3:+12 Vout C4:DC Bus	**C1:-12 Vout C2:+5 Vout C3:+12 Vout C4:DC Bus**
Startup time at 200 V_{DC} and maximum load ≈ 240 ms	Startup time at 1000 V_{DC} and maximum load ≈ 214 ms

Figure 16 Startup

6.2 Soft start

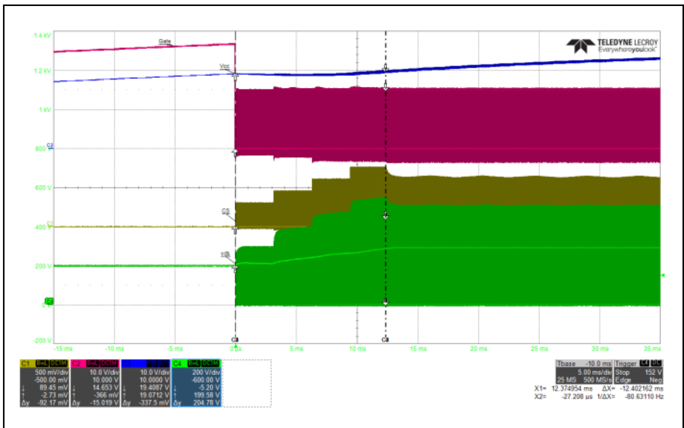
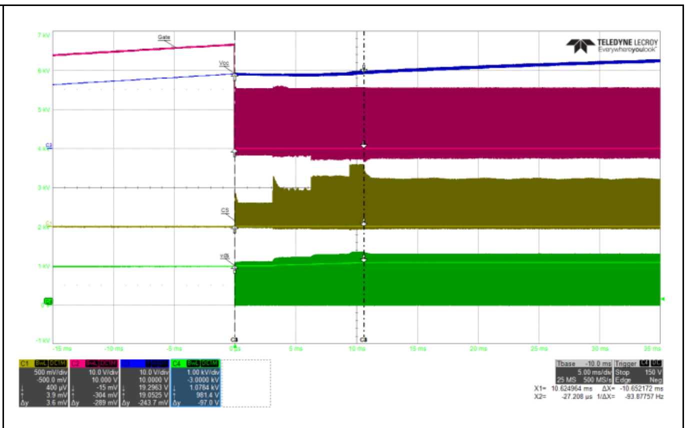
	
C1:CS C2:GATE C3:VCC C4:V_{DS}	**C1:CS C2:GATE C3:VCC C4:V_{DS}**
Soft-start time at 200 V_{DC} and maximum load ≈ 12 ms	Soft-start time at 1000 V_{DC} and maximum load ≈12 ms

Figure 17 Soft start

6.3 Steady-state switching

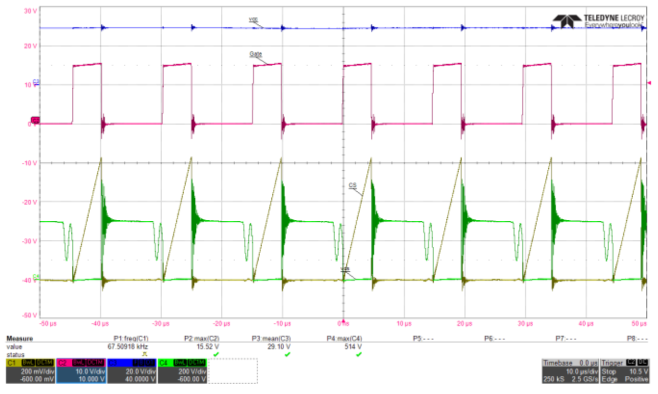
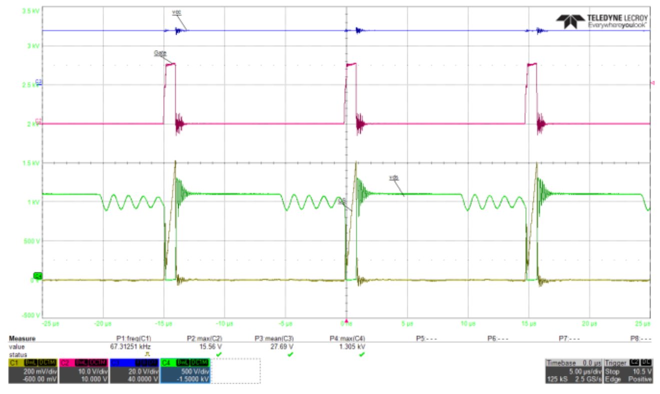
	
C1:CS C2:GATE C3:VCC C4:V_{DS}	**C1:CS C2:GATE C3:VCC C4:V_{DS}**
At 200 V_{DC}, full load	At 1000 V_{DC}, full load
Target gate voltage is set to 15 V	

Figure 18 Steady-state switching

6.4 Steady-state switching stress

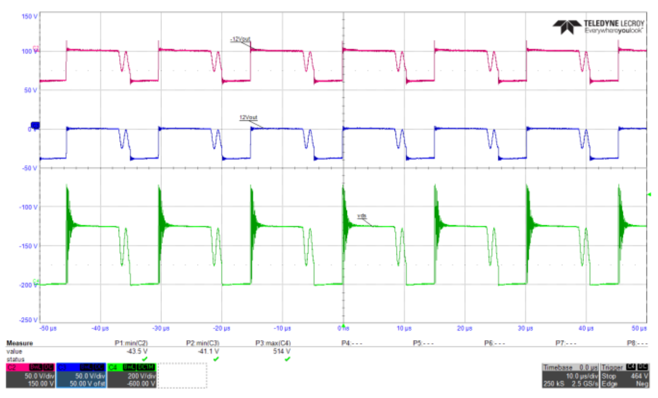
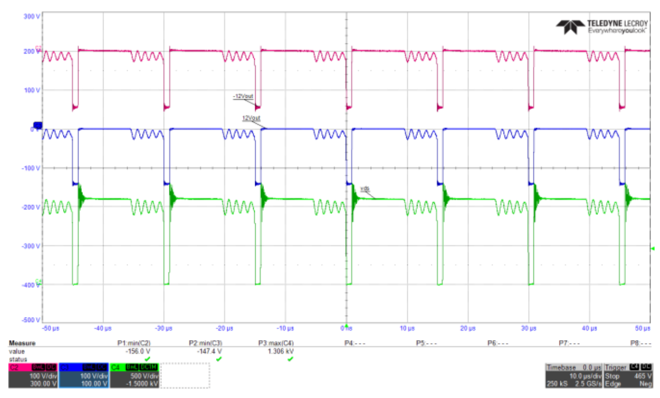
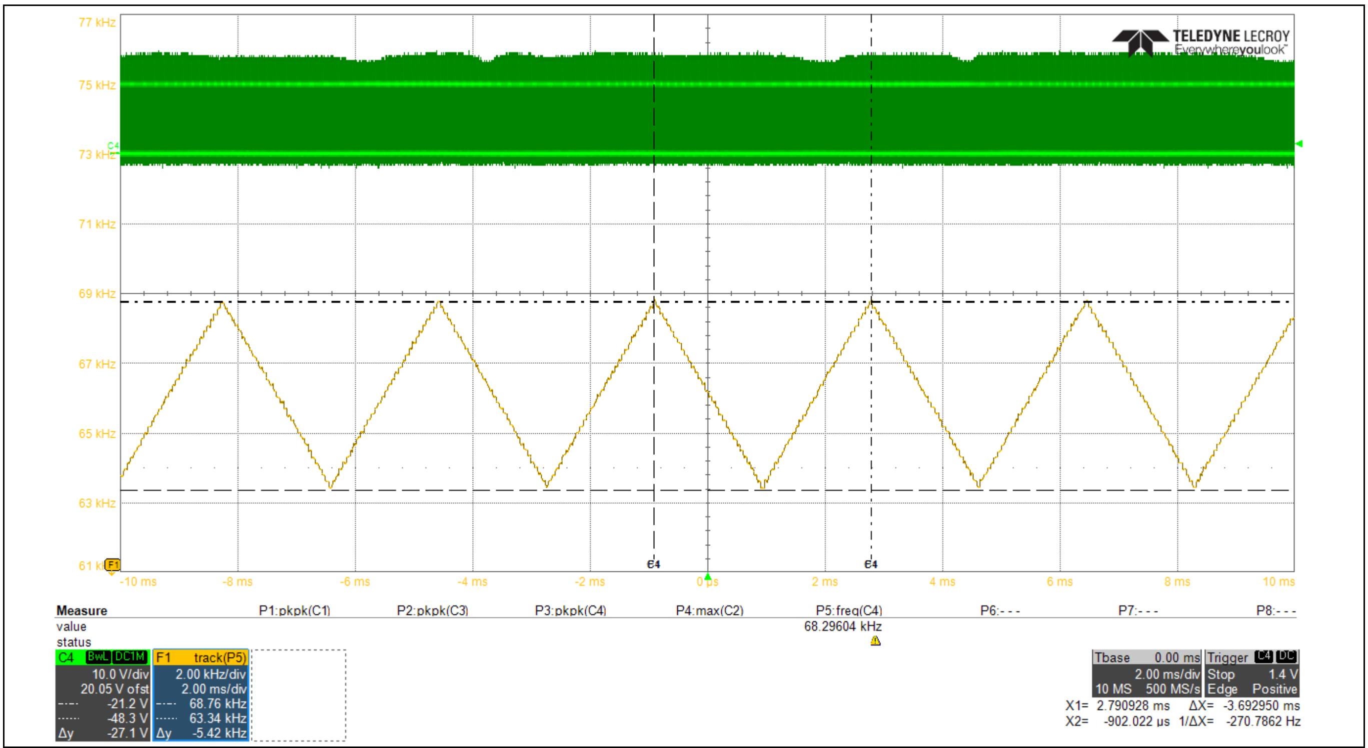
	
C2:D12 (–12 V diode) C3:D11(+12 V diode) C4:V_{DS}	**C2:D12 (–12 V diode) C3:D11 (+12 V diode) C4:V_{DS}**
At 200 V_{DC}, full load	At 1000 V_{DC}, full load
V_{DS_MAX} = 514 V, PIV_{D12_MAX} = 43.5 V, PIV_{D11_MAX} = 41.1 V	V_{DS_MAX} = 1306 V, PIV_{D12_MAX} = 156 V, PIV_{D11_MAX} = 147 V

Figure 19 Steady-state switching stress

6.5 Frequency jittering



C4:Gate F1:Frequency track of gate voltage

Frequency jittering at 200 V_{DC} and maximum load is ~63 kHz to ~69 kHz at 3.7 ms period

Figure 20 Frequency jittering

6.6 Load transient response (dynamic load from 10% to 100%)

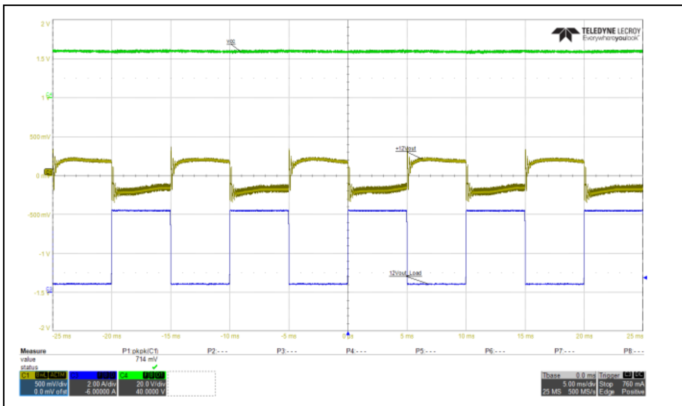
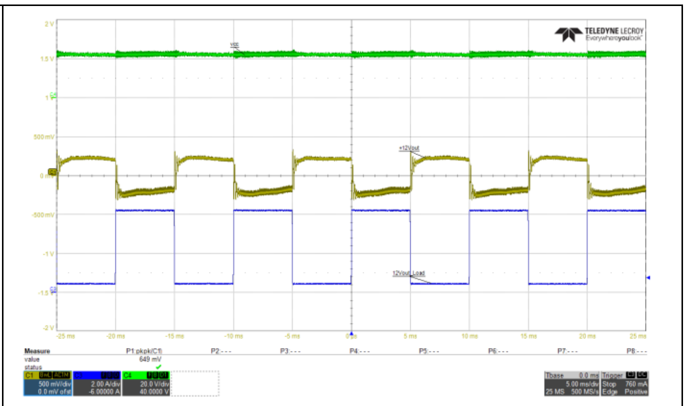
	
C1:+12 Vout C3:+12 Vout Load C4:VCC	**C1:+12 Vout C3:+12 Vout Load C4:VCC**
At 200 V_{DC}, all loads except +12 Vout fixed to 5%	At 1000 V_{DC}, all loads except +12 Vout fixed to 5%
12 $V_{pk\_pk} \approx$ 714 mV (5.9%) (load change from 10% to 100%, 100 Hz, 0.4 A/µs slew rate) Probe terminal end with decoupling capacitor of 0.1 µF (ceramic) and 10 µF (electrolytic), 20 MHz filter	12 $V_{pk\_pk} \approx$ 649 mV (5.4%) (load change from 10% to 100%, 100 Hz, 0.4 A/µs slew rate) Probe terminal end with decoupling capacitor of 0.1 µF (ceramic) and 10 µF (electrolytic), 20 MHz filter

Figure 21 Dynamic load response

6.7 Output ripple voltage at maximum load

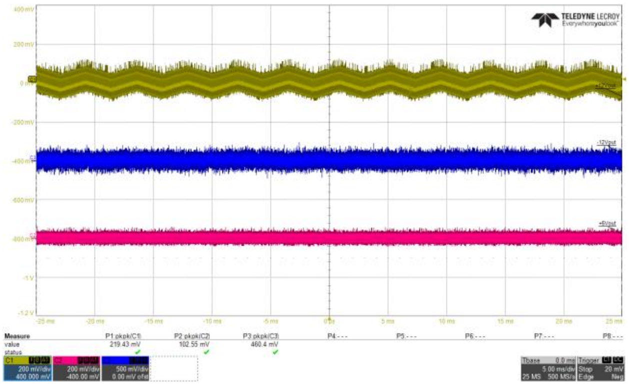
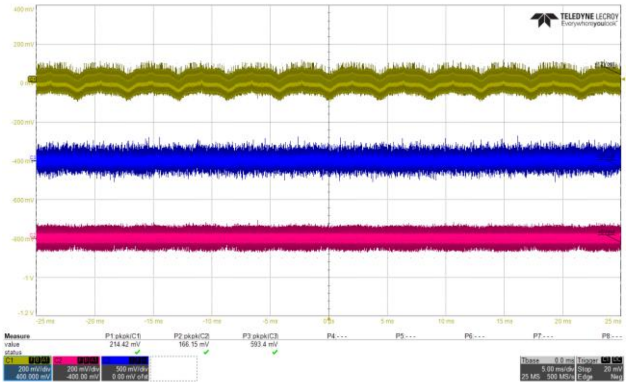
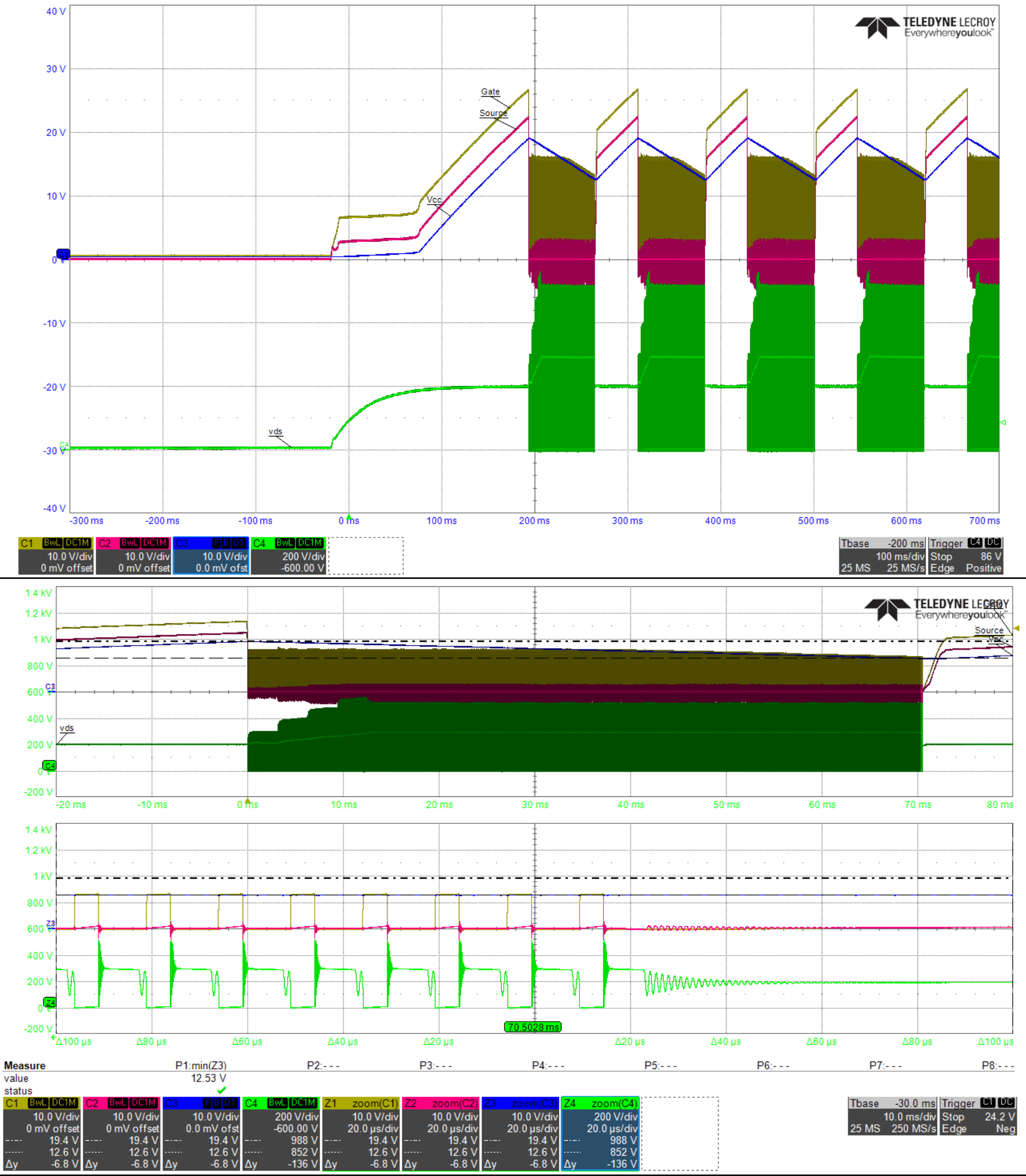
	
C1: +12 Vout (AC) C2:+5 Vout (AC) C3:-12 Vout (AC)	**C1: +12 Vout (AC) C2:+5 Vout (AC) C3:-12 Vout (AC)**
At 200 V_{DC}, full load	At 1000 V_{DC}, full load
+12 $V_{ripple\_pk\_pk}$ at 200 V_{DC} ≈ 220 mV -12 $V_{ripple\_pk\_pk}$ at 200 V_{DC} ≈ 460 mV +5 $V_{ripple\_pk\_pk}$ at 200 V_{DC} ≈ 102 mV Probe terminal end with decoupling capacitor of 0.1 µF (ceramic) and 10 µF (electrolytic), 20 MHz filter	+12 $V_{ripple\_pk\_pk}$ at 200 V_{DC} ≈ 214 mV -12 $V_{ripple\_pk\_pk}$ at 200 V_{DC} ≈ 594 mV +5 $V_{ripple\_pk\_pk}$ at 200 V_{DC} ≈ 166 mV Probe terminal end with decoupling capacitor of 0.1 µF (ceramic) and 10 µF (electrolytic), 20 MHz filter

Figure 22 Output ripple at maximum load

6.8 VCC UVLO protection

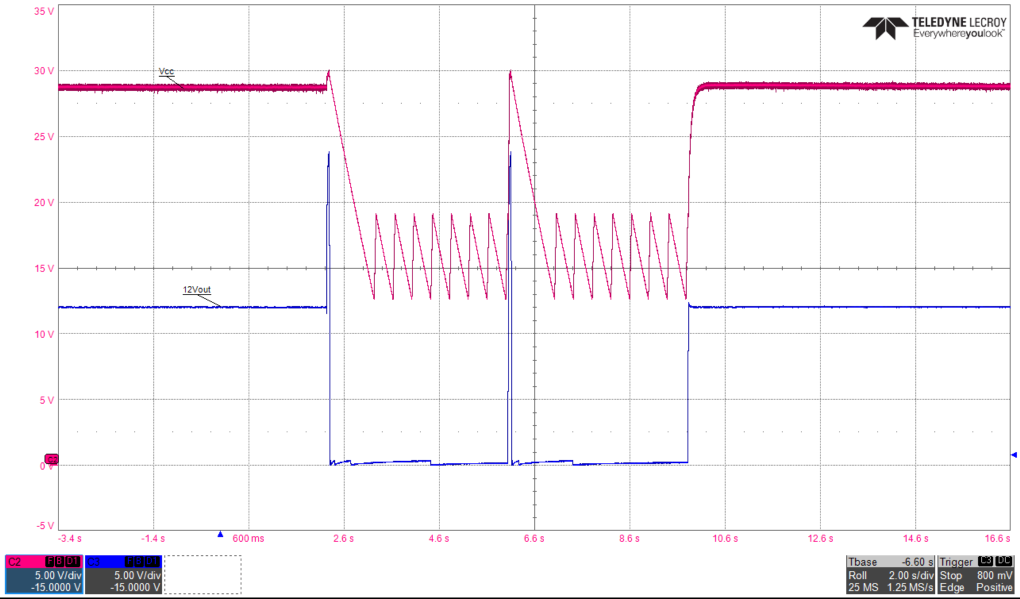


C1:Gate C2:Source C3:VCC C4:V_{DS}

Condition to enter VCC undervoltage protection (UVLO): VCC < 12.5 V
(Remove R23 and power on the system with full load at 200 V_{DC}). Part enters auto-restart

Figure 23 **VCC UVLO protection**

6.9 VCC OVP protection entry and recovery



C2:VCC C3:+12 Vout

Condition to enter V_{VCC} overvoltage protection (OVP): $V_{VCC} > 30.5$ V

In the above scope-shot, short R35 while the system is operating at 200 V_{DC} and 0.5 A load). The open loop causes the VCC to overshoot and hit V_{VCC} OVP threshold. The controller enters extended cycle skip auto-restart. Output recovers after fault is removed

Figure 24 VCC OVP protection entry and recovery

6.10 Entering active burst mode (ABM)

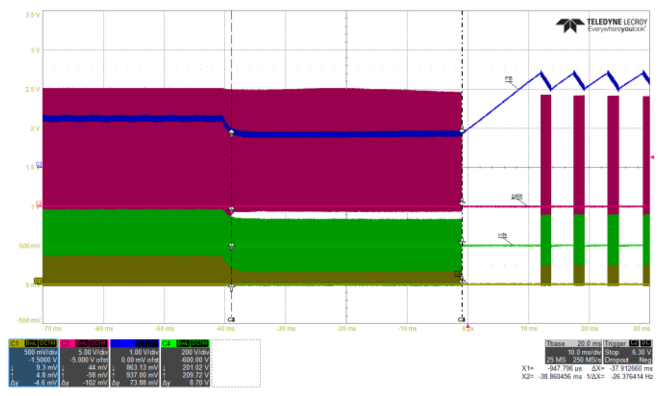
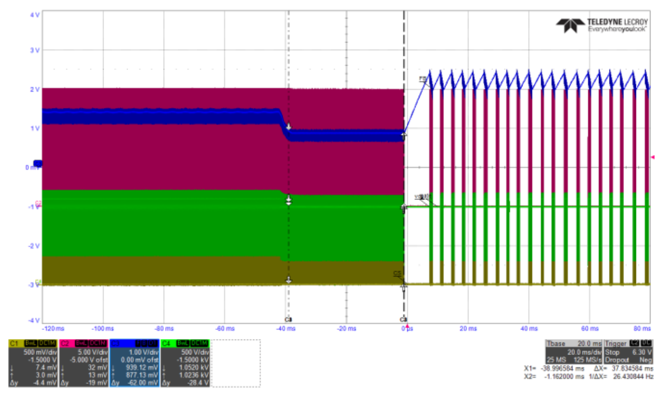
	
C1:CS C2:Gate C3:V_{FB} C4:V_{DS}	**C1:CS C2:Gate C3:V_{FB} C4:V_{DS}**
At 200 V_{DC}, 5% load at other outputs, 700 mA to 100 mA at 12 Vout	At 1000 V_{DC}, 5% load at other outputs, 1200 mA to 200 mA at 12 Vout
Condition to enter ABM level: $V_{FB} < V_{FB\_EB}$ and $t_{blanking} = t_{FB\_BEB}$	Condition to enter ABM level: $V_{FB} < V_{FB\_EB}$ and $t_{blanking} = t_{FB\_BEB}$

Figure 25 Entering active burst mode (ABM)

6.11 During active burst mode (ABM)

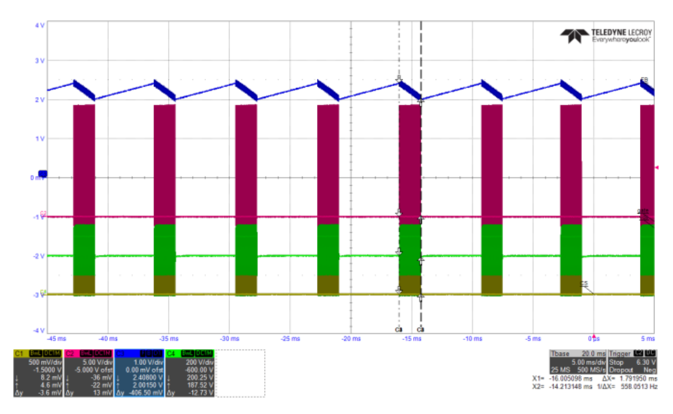
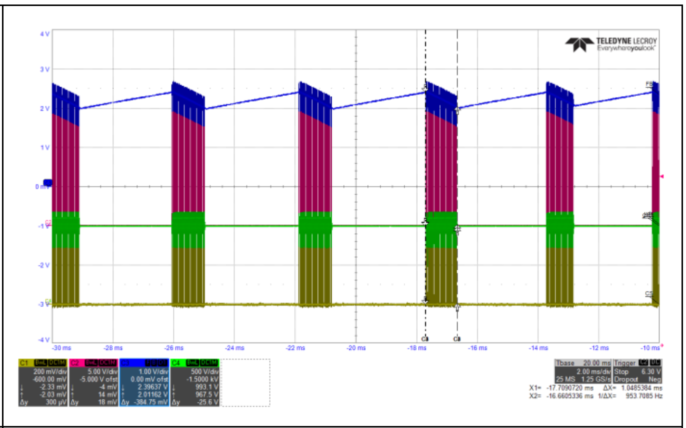
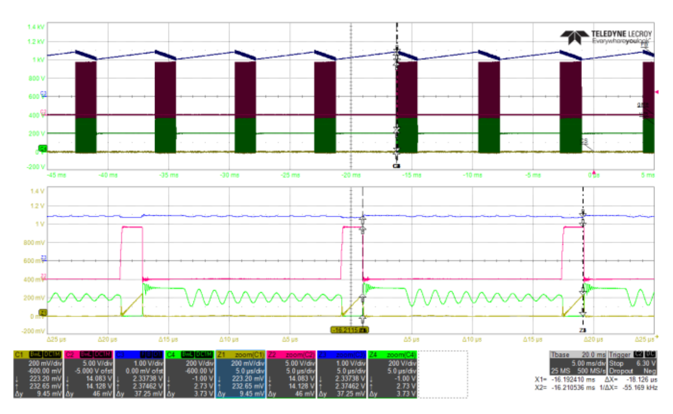
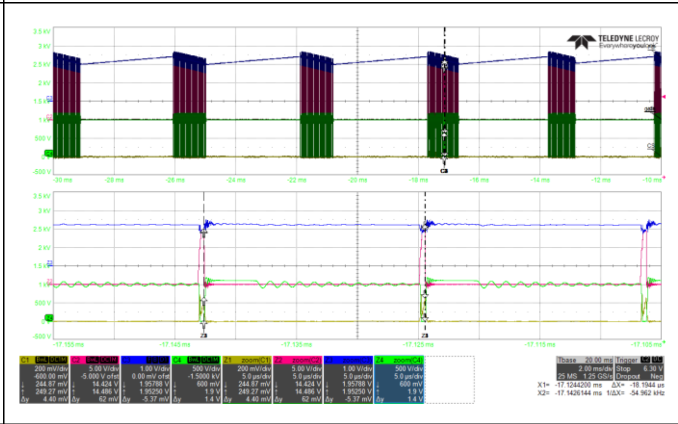
	
	
C1:CS C2:Gate C3:V_{FB} C4:V_{DS}	**C1:CS C2:Gate C3:V_{FB} C4:V_{DS}**
At 200 V_{DC}, 3% load at all outputs	At 1000 V_{DC}, 5% load at all outputs
During ABM level: $V_{FB\_Bon\_ISO}$ = 2.35 V, $V_{FB\_BOff\_ISO}$ = 2.0 V, V_{CS_BP} = 0.22 V	During ABM level: $V_{FB\_Bon\_ISO}$ = 2.35 V, $V_{FB\_BOff\_ISO}$ = 2.0 V, V_{CS_BP} = 0.22 V

Figure 26 During active burst mode (ABM)

6.12 Leaving active burst mode (ABM)

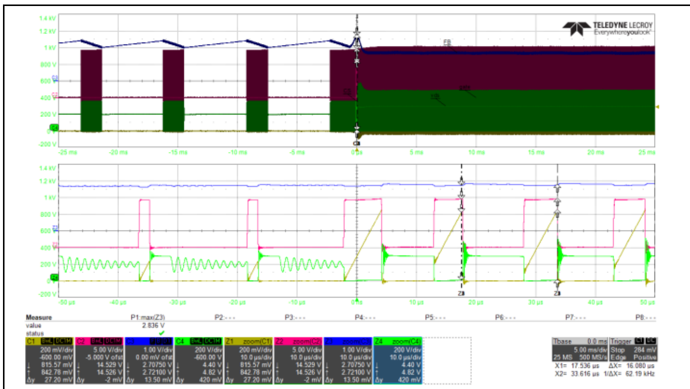
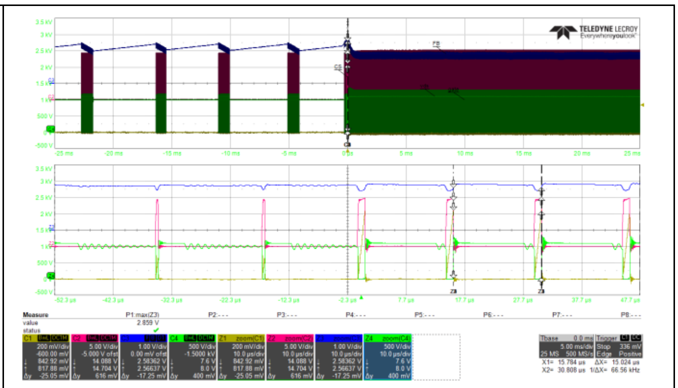
	
C1:CS C2:Gate C3:V_{FB} C4:V_{DS}	**C1:CS C2:Gate C3:V_{FB} C4:V_{DS}**
Condition to leave ABM level: V_{FB} > 2.73 V (Load change from 10% load to full load at 200 V_{DC})	Condition to leave ABM level: V_{FB} > 2.73 V (Load change from 10% load to full load at 1000 V_{DC})

Figure 27 Leaving active burst mode (ABM)

6.13 Overload protection entry and recovery

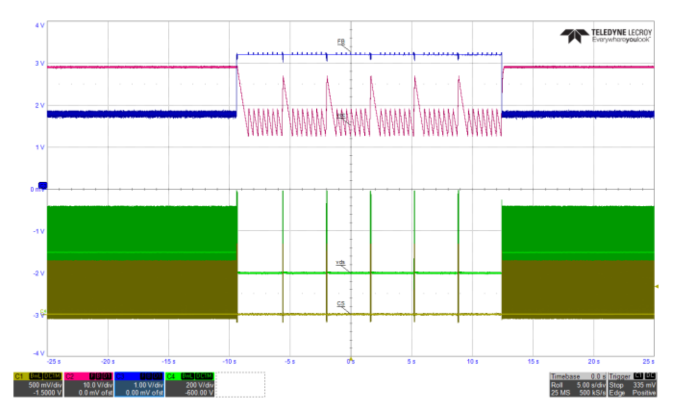
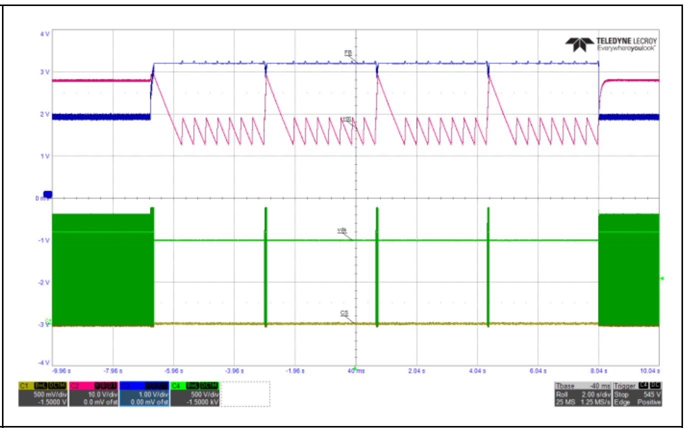
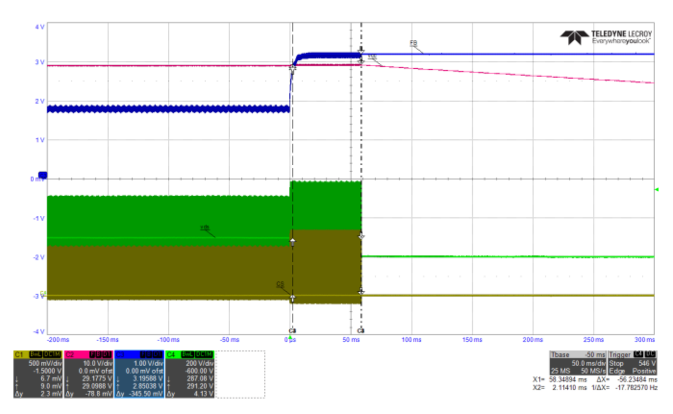
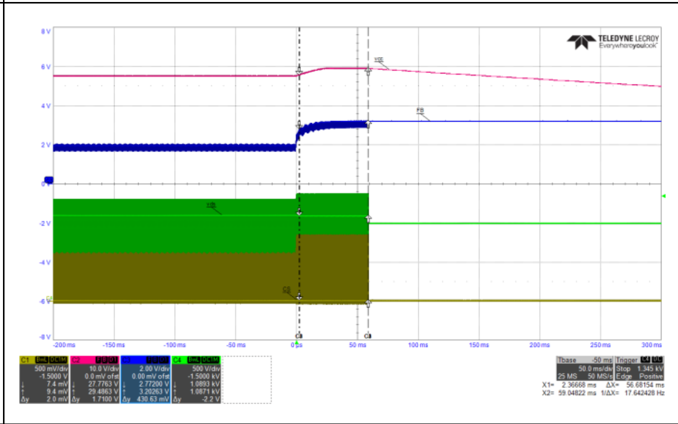
	
	
C1:CS C2:VCC C3:V_{FB} C4:V_{DS}	**C1:CS C2:VCC C3:V_{FB} C4:V_{DS}**
Output short-circuit at 200 V_{DC}, full load and recovery. $t_{blanking}$ = 56 ms, enter extended cycle skip auto-restart protection	Output short-circuit at 1000 V_{DC}, full load and recovery. $t_{blanking}$ = 56 ms, enter extended cycle skip auto-restart protection

Figure 28 Overload protection entry and recovery

6.14 Overtemperature protection entry and recovery

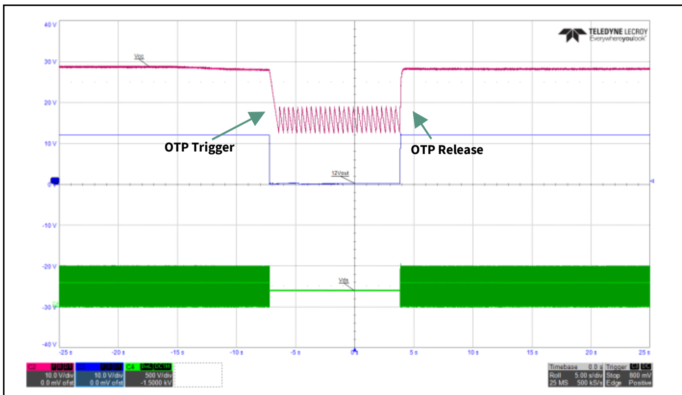
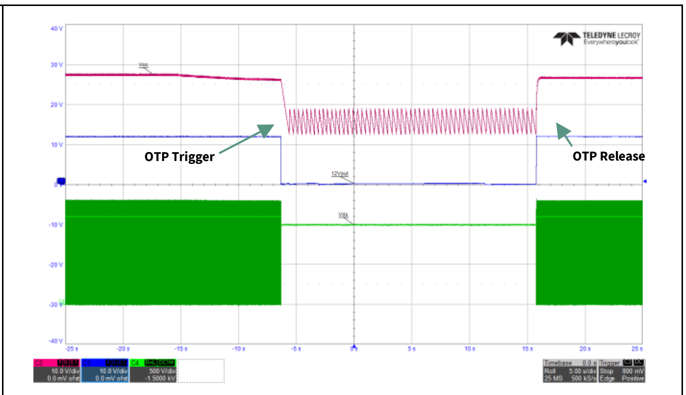
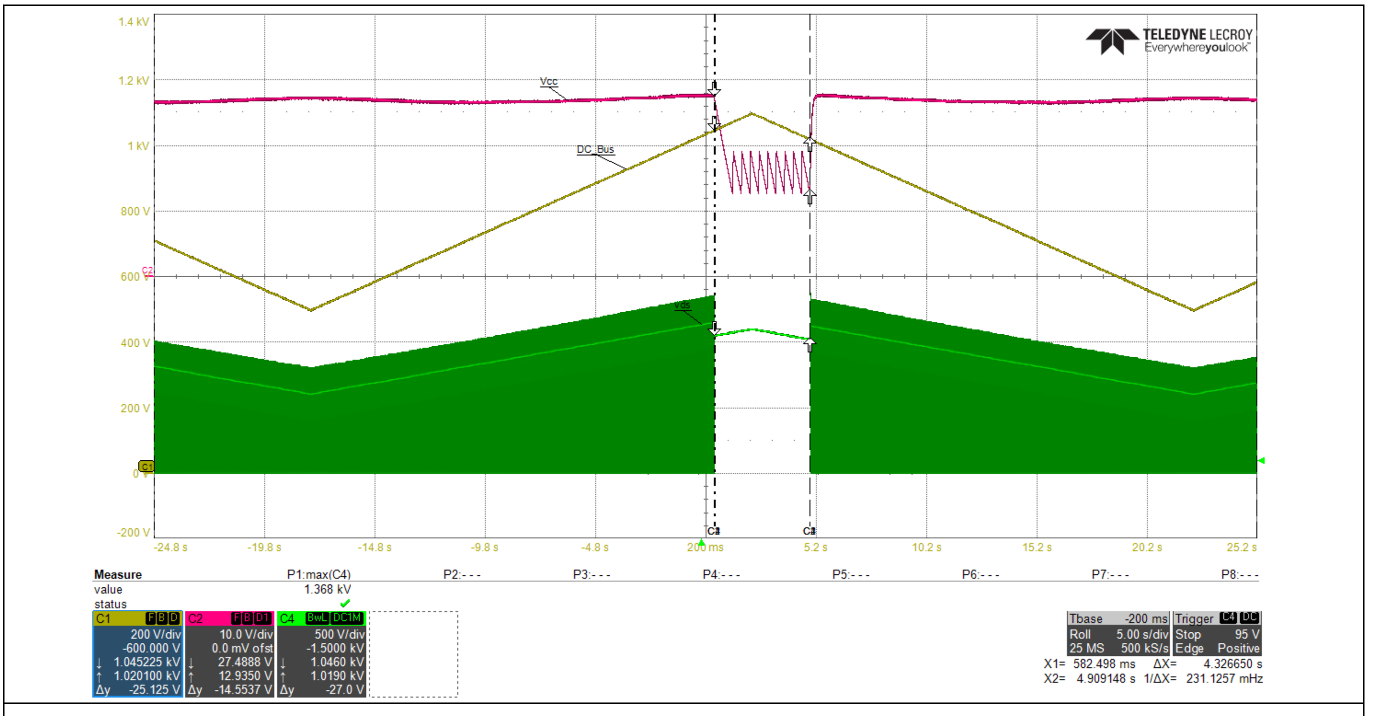
	
C2:VCC C3:+12 Vout C4:V_{DS}	**C2:VCC C3:+12 Vout C4:V_{DS}**
Vin = 200 V_{DC}, full load. Overtemperature protection tested by using hot air gun to heat the controller	Vin = 1000 V_{DC}, full load. Overtemperature protection tested by using hot air gun to heat the controller

Figure 29 Overtemperature protection entry and recovery

6.15 Line overvoltage protection entry and recovery



C1:DC Bus C2:VCC C4:V_{DS}

Tested with full load. Perform line sweep-up and sweep-down from 500 V_{DC} to 1100 V_{DC}. Line OVP triggers at 1050 V_{DC} and recovers at 1020 V_{DC}

Figure 30 Line overvoltage protection entry and recovery

7 Related resources

Developer community

For a wider discussion with peers from industry to trade ideas regarding Infineon products, we welcome you to actively participate on the Infineon Developer Community.

Technical support

Have technical queries? Consult experts from Infineon to get a fast turn-around by raising a request on the Technical Support page or a local sales representative.

References

[1] Infineon Technologies AG: *CoolSET™ PWM FF Gen5 Pro datasheet*; Available upon request

[2] Infineon Technologies AG: *CoolSET™ PWM FF Gen5 Pro flyback design guide*; Available upon request

[3] Infineon Technologies AG: *CoolSET™ PWM FF Gen5 Pro calculation tool for flyback*; Available upon request

Revision history

Document revision	Date	Description of changes
1.0	2025-12-15	Initial release

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