AN093446 2EP1xxR transformer driver IC design guide for isolated power supplies

2EP130R

About this document

Scope and purpose

This application note extends the functional and application description that is given in the 2EP1xxR family datasheet [1]. It also describes the possible topologies for the transformer and rectification with use cases.

Intended audience

This application note is intended for electrical design engineers developing a new isolated power supply solution for gate driver ICs and other ICs requiring a local isolated voltage supply.

Keypoints

- Peak rectification, voltage doubler, and bridge rectification topologies
- Transformer winding configuration
- Output power and losses
- Typical application use case calculation examples

About this product family

Product family

The 2EP1xxR is a full-bridge transformer driver family providing up to 13 W at its outputs for an open-loop isolated supply. It is optimized to supply gate drivers for a variety of switches such as TRENCHSTOP™ IGBTs, OptiMOS™ MOSFETs, CoolMOS™ super-junction MOSFETs, CoolGaN™ high electron mobility transistors, and CoolSiC™ MOSFETs together with EiceDRIVER™ gate driver ICs, and other similar products.

Target applications

- Energy storage solutions and PV inverter
- Fast EV charger
- Motor drive inverter
- Solid state circuit breaker

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1 Introduction

The 2EP1xxR is a full-bridge transformer driver family providing up to 13 W at its outputs for an open-loop isolated supply. It is optimized to supply gate drivers for a variety of switches such as TRENCHSTOP™ IGBTs, OptiMOS™ MOSFETs, CoolMOS™ super-junction MOSFETs, CoolGaN™ high electron mobility transistors, and CoolSiC™ MOSFETs together with EiceDRIVER™ gate driver ICs, and other similar products.

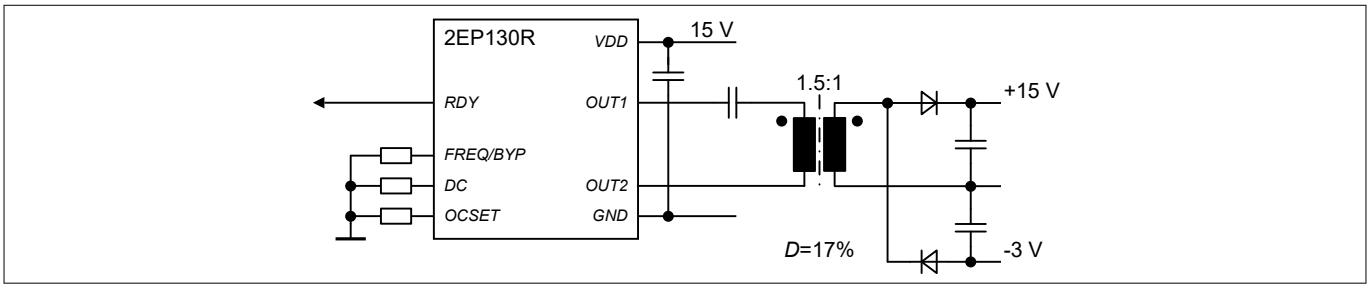


Figure 1 Schematic example for 2EP130R

The 2EP1xxR family offers the following product variants:

- 2EP100R and 2EP101R are optimized for low-component count designs for IGBT and SiC MOSFET gate driver supplies
- 2EP110R allows a fine duty-cycle adjustment to adapt the output voltage ratio to the application requirements of SiC and GaN power switches
- 2EP130R is optimized for highly flexible designs to adapt to different application requirements. It provides:
  - 5-step overcurrent protection
  - 41 selectable switching frequencies or synchronization to an external PWM for transformer adaptation
  - 41 selectable duty-cycle options to adjust the output supply voltage

All 2EP1xxR family variants provide several safety functions to secure safe device operation, such as:

- UVLO monitoring
- Overtemperature protection
- Short circuit protection for the outputs
- Average overcurrent protection
- Soft start
- Ready output

The 2EP1xxR family is available in the thermally enhanced package, PG-TSSOP-8, with a fine pitch of 0.65 mm.

Table 1 Product variants

Part number	Frequency	Duty cycle *D*	Power capability at 15 V	Marking
2EP100R	65 kHz, 103 kHz	33%, 50%	up to 6 W	2EP100R
2EP101R	50 kHz, 65 kHz	12%, 17%	2 W .. 4 W	2EP101R
2EP110R	50 kHz, 65 kHz	10% .. 50%	up to 6 W	2EP110R
2EP130R	50 kHz .. 695 kHz	10% .. 50%	up to 6 W	2EP130R

2 Topologies

The 2EP1xxR transformer driver ICs support various topologies in terms of transformer configuration and output voltage rectification. The actual selection of these options depend on required output power, output voltages, and layout limitations of the individual application.

2.1 Rectification

The 2EP1xxR requires the transformer for isolation and voltage adaption using PWM switch patterns for power transmission. The output voltage after the transformer is a pulsed AC voltage and requires rectification. Therefore, there are multiple rectification circuit options available for use with the 2EP1xxR.

Peak rectification (PR)

The peak rectification is one of the simplest circuit options, requiring the least amount of rectification diodes, and takes full advantage of the adjustable duty cycle of the 2EP1xxR resulting in positive and negative output voltages with adjustable ratio.

The details of this rectification topology in combination with the 2EP1xxR is described in Chapter 2.1.1.

Voltage doubler (VD)

The voltage doubler circuit is best suited for half-bridge gate driver supplies requiring a 2:1 ratio between positive and negative output voltage. This circuit is mainly used in drives applications using IGBTs.

The details of this rectification topology in combination with the 2EP1xxR is described in Chapter 2.1.2.

Bridge or full-wave rectification (BR)

The bridge rectification is best suited for singe output voltages resulting in the least amount of ripple current. This rectification topology is useful for isolated sensor supplies or in applications with additional post regulation to provide the actual output voltage.

The details of this rectification topology in combination with the 2EP100R is described in Chapter 2.1.3

2.1.1 Theory of the 2EP1xxR using peak rectification topology

This section describes the theory behind the full-bridge power stage of 2EP1xxR and the peak rectification topology to provide two isolated output voltages.

The diagrams in this section only show one output winding at the transformer. However, each single transformer output winding supports a positive and a negative output voltage. The ratio between the positive voltage and negative voltage is defined by the duty cycle.

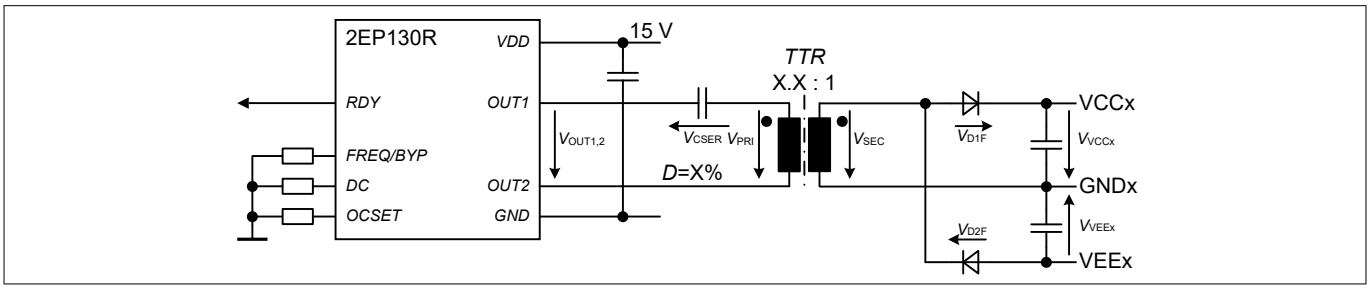


Figure 2 Simplified schematic of 2EP130R using peak rectification topology

The voltage arrows indicate the polarity of the corresponding symbol for use in the equations provided later. V_{PRI} and V_{SEC} represent the transformer voltages, V_{DxF} the individual diode forward voltages, V_{CSER} the voltage across the primary series capacitor, and V_{VCCx}, V_{VEEx} the output voltage.

The following sections describe how to determine the output voltages of a peak rectification according to:

- The applied input voltage to 2EP
- The applied duty cycle by chopping the input voltage

- The level-shift (offset) of the series capacitor
- The transformer turns ratio

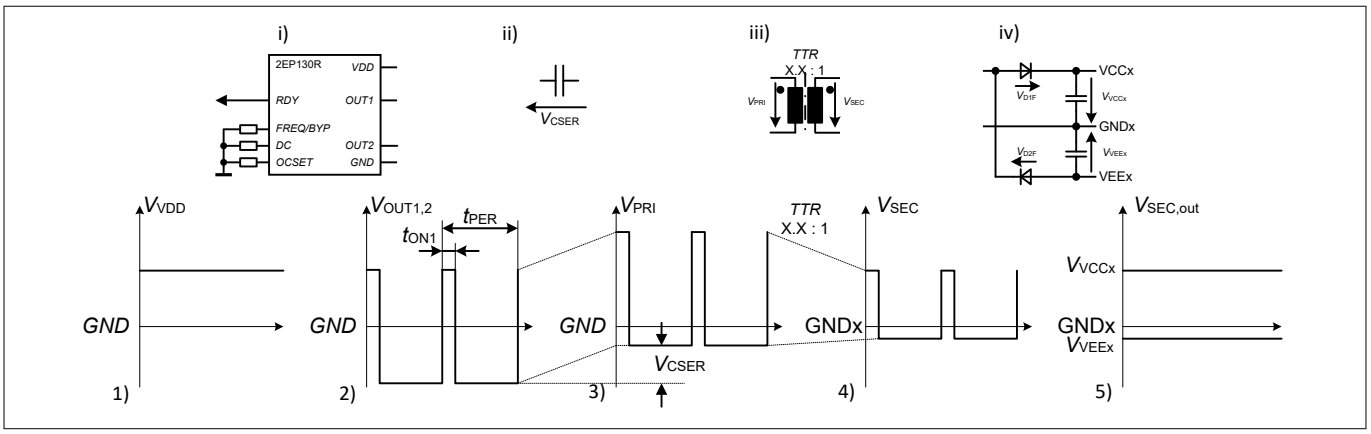


Figure 3 DC offset voltage and influence of transformer turns ratio output voltage

The figure shows the idealized voltage wave forms at each step (1-5) and the involved components at the intermediate step (i-iv). The input supply voltage V_{VDD} (1) is applied to 2EP130R (i). It provides the output voltage $V_{OUT1,2}$ (2) to the series capacitor (ii). This results in the shifted input voltage V_{PRI} (3) for the transformer (iii). The transformer scales the input voltage to the secondary side as V_{SEC} (4). The last step is peak current rectification (iv) and its output voltages (5).

Full-bridge transformer driver – 2EP130R

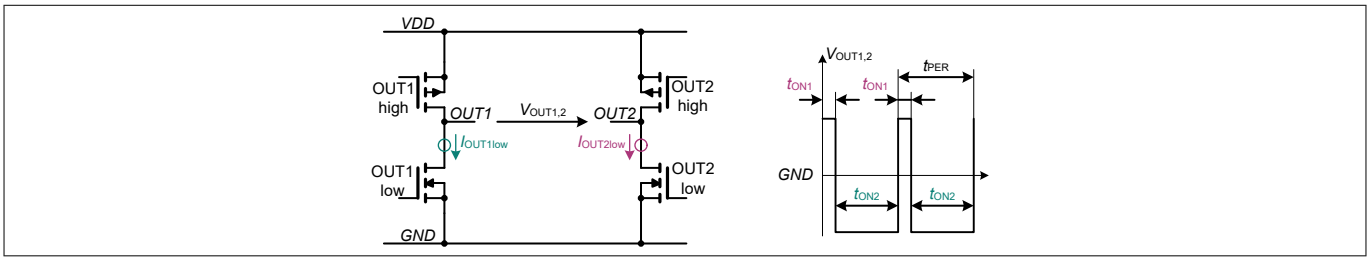


Figure 4 Current path mapping to individual segments of the switching period

This diagram shows the mapping of the individual current paths to the timing diagram of the outputs:

- Current during t_{ON1} flows through the *OUT1* high-side and the *OUT2* low-side switch
- Current during t_{ON2} flows through the *OUT2* high-side and the *OUT1* low-side switch

The duration of t_{ON1} together with the time period, t_{PER}, defines the duty cycle $D = \frac{t_{ON1}}{t_{PER}}$

2EP130R chops the applied supply voltage, V_{VDD}, according to the configured switching frequency and duty cycle (*D*). The output of *OUT1* is switched between *VDD* and *GND*. The same is valid for *OUT2*. However, its switching pattern is inverted. This results in twice the amplitude of V_{VDD} across the outputs $V_{OUT1,2}$ or with a *GND* reference:

$$V_{OUT1,2} = \pm V_{VDD}$$

The duty cycle is calculated as: $D = \frac{t_{ON1}}{t_{PER}}$ with the on duration of output 1, t_{ON1}, and the period time, t_{PER}, of the switching frequency. The duty cycle for *OUT2* always complements that of *OUT1*. The duty cycle always refers to *OUT1*.

Series capacitor – C_{SER}

The series capacitor creates an offset derived from the duty cycle. The DC offset voltage, V_{CSER}, is therefore an integral component for calculating output voltages. The capacitor voltage level during steady state operation is calculated as:

$$V_{CSER} = V_{VDD}\left(1 - \frac{2 \cdot D}{100\,\%}\right)$$

The offset voltage V_{CSER} varies between 80% of the V_{VDD} at 10% and 0% of the V_{VDD} at 50% duty cycle. Since 2EP130R only allows duty cycles between 10% to 50%, the resulting offset voltage is positive according to its indicated polarity. Any waveform with a duty cycle not equal to 50% has a DC offset voltage component. The series capacitor, basically, removes the direct component from the chopped supply voltage. Due to this, the series capacitor converts the symmetric peak voltages, $V_{OUT1,2}$, into asymmetric peak voltages:

$$V_{PRI} = \pm V_{VDD} + V_{CSER}$$

The primary transformer voltage alternates between (+V_{VDD}+V_{CSER}) and (-V_{VDD}+V_{CSER}) due to the full-bridge output stage of 2EP130R and the aforementioned offset voltage stored within V_{CSER}.

Transformer, transformer turns ratio (*TTR*), and transformer saturation

The transformer transforms the primary input voltage, V_{PRI}, according to the transformer turns ratio (*TTR*) to the secondary side. The secondary transformer voltage, V_{SEC}, is calculated as:

$$V_{SEC} = \frac{V_{PRI}}{TTR} = \pm \frac{V_{VDD}}{TTR} + \frac{V_{CSER}}{TTR}$$

The aforementioned V_{CSER} offset voltage ensures an equal voltage × time product of both polarities for the primary winding. This equal voltage×time product prevents the transformer from saturating, even when driven with asymmetric peak voltages.

Peak current rectification

Due to the diodes in the peak rectification circuit, individual current paths must be considered separately. The matching voltage polarity of the secondary transformer voltage should be taken into account when calculating the expected output capacitor voltages.

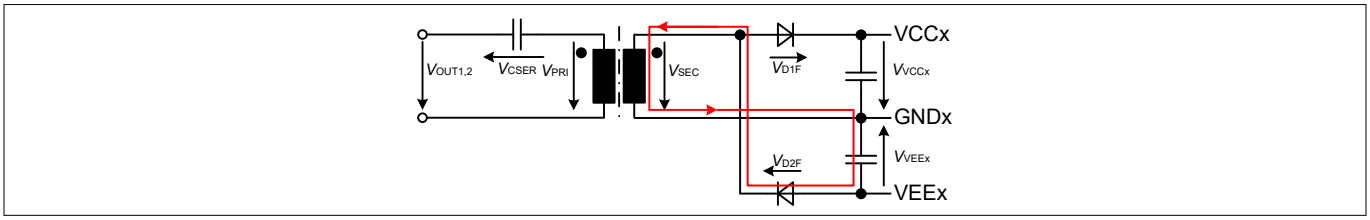


Figure 5 Current path of the negative voltage rail

The current path to charge the negative voltage rail requires V_{SEC} to be in reverse polarity to the indicated arrow. The current charges the negative output voltage capacitor and closes the circuit via the diode, D2, in forward direction resulting in the V_{D2F} voltage drop.

The negative output voltage then results in: $V_{VEEx} = V_{SEC(neg)} + V_{D2F}$

As the secondary transformer voltage is negative at that half-wave, the resulting output voltage is also negative, but reduced by the diode forward voltage.

The positive output voltage behaves similar to the negative output voltage.

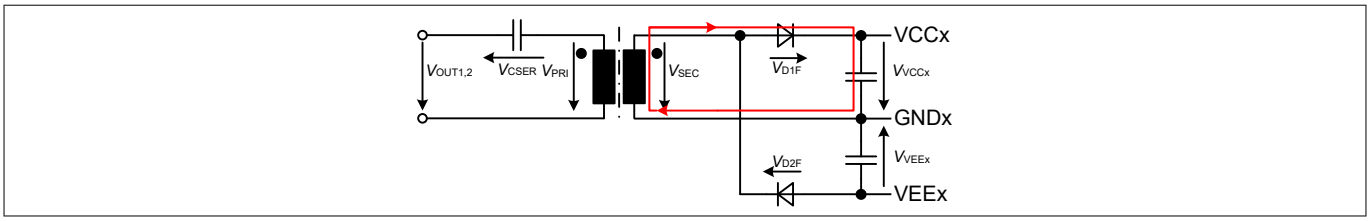


Figure 6 Current path of the positive voltage rail

The current path to charge the positive voltage rail requires V_{SEC} to be in the indicated polarity (positive half-wave). The current charges the positive output voltage capacitor and closes the circuit via the diode, D1, in forward direction resulting in the V_{D1F} voltage drop.

The positive output voltage then results in: $V_{VCCx} = V_{SEC(pos)} - V_{D1F}$

Both output voltages can be written as:

Assumption 1: All forward voltages are equal:

$$V_F = V_{D1F} = V_{D2F}$$

Assumption 2: Amplitudes of both the positive and negative half-waves experience the same offset:

$$V_{SEC} = \pm \frac{V_{VDD}}{TTR} + \frac{V_{CSER}}{TTR}$$

Positive output voltage:

$$V_{VCCx} = \left(\frac{V_{VDD}}{TTR} + \frac{V_{CSER}}{TTR} - V_F \right)$$

Negative output voltage:

$$V_{VEEx} = -\left(\frac{V_{VDD}}{TTR} - \frac{V_{CSER}}{TTR} - V_F \right)$$

(1)

***Note**: Equal load at positive and negative voltage rails results in asymmetric currents for positive and negative half waves. This can result in unequal output voltage drops for positive and negative output voltages. The actual output voltages may differ slightly from the ones calculated using the equations given in this section. When designing a peak rectifier circuit with dual output rails, the same winding polarity should be used for both rails.*

Inserting the series capacitor voltage V_{CSER} equation into the output voltage equations results in:

Positive output voltage:

$$V_{CCx} = \frac{2 \cdot V_{VDD}}{TTR}(1 - D) - V_F$$

Negative output voltage:

$$V_{EEx} = \frac{2 \cdot V_{VDD}}{TTR}(-D) + V_F$$

(2)

2.1.2 Theory of the 2EP1xxR using the voltage doubler topology

This section describes the theory behind the full-bridge power stage of 2EP1xxR together with the voltage doubler topology to provide two isolated output voltages. Each transformer output winding supports a positive

and a negative output voltage. The positive output voltage has double the voltage level compared to the negative output voltage.

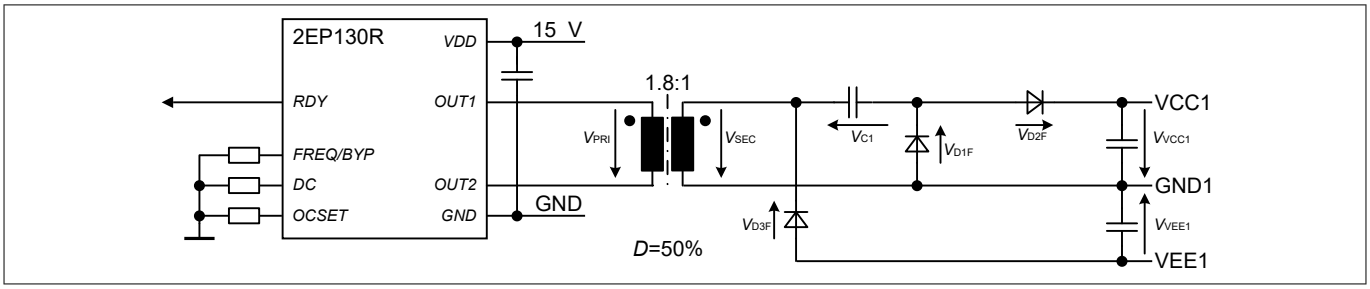


Figure 7 Simplified schematic of 2EP130R using voltage doubler topology

The voltage arrows indicate the polarity of the corresponding symbol used in the equations provided later. V_{PRI} and V_{SEC} represent the transformer voltages, V_{DxF} the individual diode forward voltages, V_{C1} the voltage of the voltage doubler capacitor (flying capacitor), and V_{VCC1}, V_{VEE1} the output voltage of one of the rails.

The following sections describe how to determine the output voltages of a voltage doubler topology connected to 2EP130R.

Full-bridge transformer driver 2EP130R

For output rectification using the voltage doubler topology, the configured duty cycle needs to be at 50%. 2EP130R chops the applied supply voltage, V_{VDD}, according to the configured switching frequency. The output of *OUT1* is switched between *VDD* and *GND*. The same is valid for *OUT2*. However, its switching pattern is inverted. This results in twice the amplitude of V_{VDD} across the outputs $V_{OUT1,2}$. In the schematic shown above, this voltage is referred to as the primary transformer voltage, V_{PRI}.

$$V_{PRI} = \pm V_{VDD}$$

Transformer, transformer turn ratio (*TTR*), and transformer saturation

The transformer transforms the primary input voltage, V_{PRI}, to the secondary side voltage based on the transformer turn ratio (*TTR*). The secondary transformer voltage V_{SEC} is calculated as:

$$V_{SEC} = \frac{V_{PRI}}{TTR} = \pm \frac{V_{VDD}}{TTR}$$

If the output voltages are loaded asymmetrically or the input duty cycle is not exactly at 50%, the transformer could drift into saturation. The EVAL-2EP130R-VD evaluation board [2] includes a series capacitor between *OUT1* and the primary winding. To simplify, this component is not shown nor considered in the calculations given in this section. This capacitor ensures an equal voltage × time product for primary winding. The equal voltage × time product prevents the transformer from saturating, even when driven with asymmetric loads.

Voltage doubler current rectification

Due to the diodes in the voltage doubler circuit, individual current paths must be considered separately. The matching voltage polarity of the secondary transformer voltage must be applied only when calculating the expected output capacitor voltages.

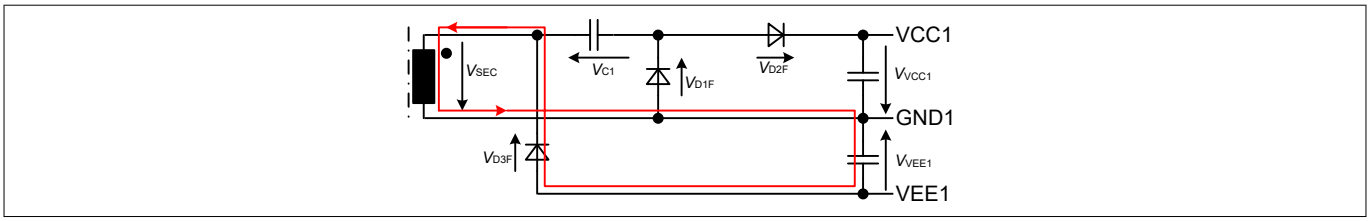


Figure 8 Current path of the negative voltage rail

The current path to charge the negative voltage rail requires V_{SEC} to be in reverse polarity. The current charges the negative output voltage capacitor. The current then closes the circuit via diode D3 in the forward direction resulting in V_{D3F} voltage drop.

The negative output voltage results in: $V_{VEE1} = V_{SEC(neg)} + V_{D3F}$

Since the secondary transformer voltage is negative at that half wave, the resulting output voltage is also negative but lowered by the diode's forward voltage.

The positive output voltage requires a two-step approach for the full output voltage. In the first step, the flying capacitor is charged. In the second step, this pre-charged capacitor boosts the voltage for a positive output rail.

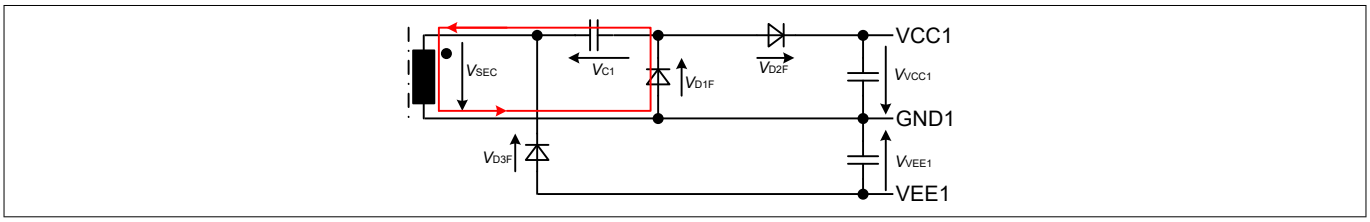


Figure 9 Current path to charge the bootstrap capacitor of the positive voltage rail

The current path to charge the flying capacitor requires V_{SEC} to be in reverse polarity. The direction of current is the same as that for the negative output voltage. Therefore, the current during the negative half wave of the secondary winding is doubled compared to the positive half wave. The current flows through the diode, D1, resulting in V_{D1F} voltage drop. It then charges the flying capacitor before closing the circuit.

The flying capacitor, therefore, has a positive voltage that results in: $V_{C1} = -V_{SEC(neg)} - V_{D1F}$

As the secondary transformer voltage is negative at that half wave, the resulting flying capacitor voltage, according to the indicated polarity, is positive but reduced by the diode's forward voltage.

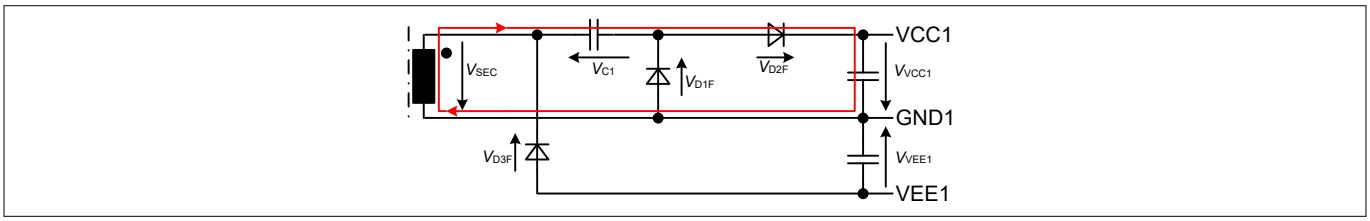


Figure 10 Current path of the positive voltage rail via the bootstrap capacitor

The current path to finally charge the positive output voltage capacitor requires V_{SEC} to be in the indicated polarity (positive half wave). It has, therefore, the same polarity as the flying capacitor voltage, V_{C1}. The resulting current will pass through D2 resulting in a V_{D2F} voltage drop. It then charges the positive output voltage capacitor before closing the circuit.

The positive output voltage results in: $V_{VCC1} = V_{SEC(pos)} + V_{C1} - V_{D2F}$

Both output voltages can then be written as:

Assumption 1: All diode forward voltages are equal

$$V_F = V_{D1F} = V_{D2F} = V_{D3F}$$

Assumption 2: Amplitudes of positive and negative half wave are equal

$$|V_{SEC}| = V_{SEC(pos)} = -V_{SEC(neg)} = \frac{V_{VDD}}{TTR}$$

positive output voltage

$$V_{CC1} = 2 \cdot \left(\frac{V_{VDD}}{TTR} - V_F\right) \quad (3)$$

negative output voltage

$$V_{EE1} = -\left(\frac{V_{VDD}}{TTR} - V_F\right)$$

***Note**: A single rail voltage doubler output has asymmetric current during positive and negative half waves. To compensate for this, when designing a voltage doubler circuit with dual output rails different winding polarities must be used for the two rails.*

2.1.3 Theory of the 2EP100R using bridge rectification topology

This section describes the theory behind the full-bridge power stage of 2EP100R and the bridge or full-wave rectification topology to provide one isolated output voltage. Each transformer output winding supports a single output voltage. This description is also compatible with all other 2EP1xxR product variants.

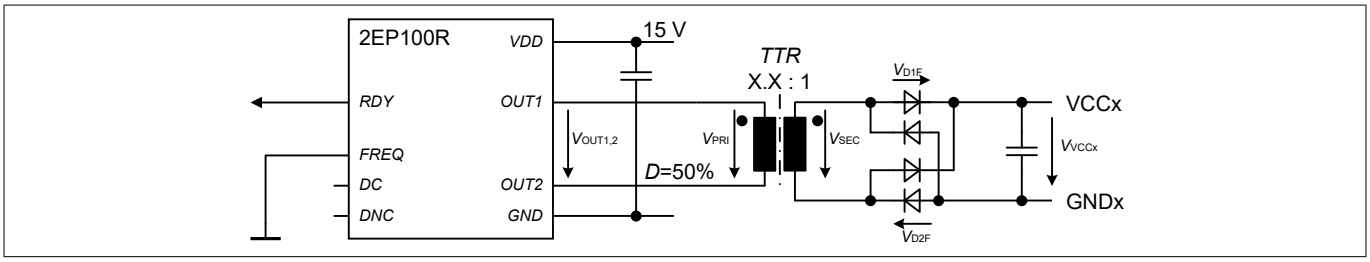


Figure 11 Simplified schematic of 2EP100R using bridge rectification topology

The voltage arrows indicate the polarity of the corresponding symbol for use in the equations provided later. V_{PRI} and V_{SEC} represent the transformer voltages, V_{DxF} the individual diode forward voltages, and V_{VCCx} the output voltage.

The following sections describe how to determine the output voltages of a bridge rectification according to:

- The applied input voltage to 2EP
- The transformer turn ratio
- The bridge rectification

Full-bridge transformer driver – 2EP100R

2EP100R chops the applied supply voltage, V_{VDD}, according to the configured switching frequency. For this rectification topology, the duty cycle (*D*) needs to be selected with 50%. The output of *OUT1* is switched between *VDD* and *GND*. The same is valid for *OUT2*. However, its switching pattern is inverted. This results in twice the amplitude of V_{VDD} across the outputs $V_{OUT1,2}$ or with a *GND* reference:

$$V_{OUT1,2} = \pm V_{VDD}$$

Transformer, transformer turn ratio (*TTR*), and transformer saturation

The transformer transforms the primary input voltage, V_{PRI}, according to the transformer turn ratio (*TTR*) to the secondary side. The secondary transformer voltage, V_{SEC}, is calculated as:

$$V_{SEC} = \frac{V_{PRI}}{TTR} = \pm \frac{V_{VDD}}{TTR}$$

This topology does not require a series capacitor for offset compensation since the output load in bridge rectification is expected to be symmetrical for 50% duty cycle. The voltage × time product is equal and prevents the transformer from saturating. The voltage × time still plays a role in selecting the minimum switching frequency of the 2EP100R to avoid saturation during the 50% pulse-pause cycle.

Bridge rectification

Due to the diodes in the peak rectification circuit, individual current paths must be considered separately. The matching voltage polarity of the secondary transformer voltage should be taken into account when calculating the expected output capacitor voltages.

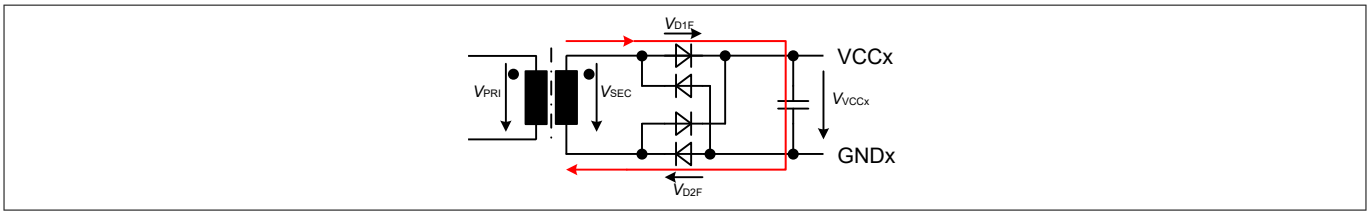


Figure 12 Current path via D1 and D2

V_{SEC} can be of either polarity to charge the output voltage rail. During a positive half-wave, the current path closes the circuit via the diode D1 and D2. This results in a voltage drop of both diodes V_{D1F} and V_{D2F} reducing the output voltage V_{VCCx}.

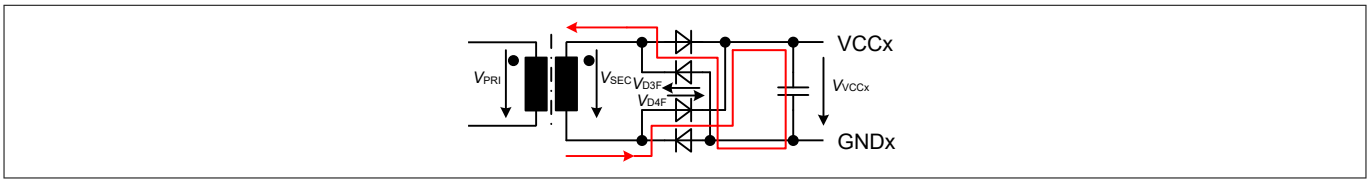


Figure 13 Current path via D3 and D4

During a negative half-wave, the current path closes the circuit via the diode D3 and D4. This results in a voltage drop of both diodes V_{D3F} and V_{D4F} reducing the output voltage V_{VCCx}.

Since both half-waves have two diodes in their circuit path, the output voltage then results in:
$V_{VCCx} = V_{SEC} - 2 \cdot V_{DxF}$
Inserting the transformer ratio into the calculation the equation results in:

$$V_{CCx} = \frac{V_{VDD}}{TTR} - 2 \cdot V_F \quad (4)$$

2.2 Transformer

Apart from the mentioned rectification topologies the 2EP1xxR can operate with, the 2EP1xxR also supports various transformer configuration options. The transformer is always required for isolation and voltage adaptation. The transformer transfer ratio has been discussed in the individual rectification sections, here the focus is on isolation and configuration options.

Transformer insulation ratings

Transformer manufacturers specify their insulation test voltages as RMS voltage, for example V_{ISO} = 5000 V (rms). This rating is mainly derived from the wires and their insulation used in the construction of the transformer. For creating an insulated power supply for gate driver ICs in a high voltage converter/inverter application, the resulting working voltage due to physical dimensions of the transformer become important. Sometimes such a value is not mentioned in the manufacturers datasheet of the transformer and needs to be

requested separately. Some manufacturers provide the working voltage for different insulation requirements like basic or reinforced insulation.

Which value then applies to the customer application depends on the overall operating conditions as well as the circuit partitioning. A transformer selection requires careful consideration of many insulation related parameters. Any open questions should therefore always be discussed with the transformer manufacturer. The 2EP1xxR itself is a non-isolated product and is also not part of the application insulation concept.

Transformer winding configuration options

Details about the electrical characteristics to dimension the transformer for its application are described in the application section of the 2EP1xxR product datasheet. This section describes the options of various output winding configuration as well as the number of parallel input windings the 2EP1xxR can support:

- One single-output winding transformer
- Two or more single-output winding transformers in parallel
- One dual-output winding transformer
- Two or more dual-output winding transformers in parallel
- Dual-output winding transformers for special application uses

The input supply voltage, transformer ratio, duty cycle, and the resulting output voltages using any rectification method in these topologies are only examples. Different output voltages can be achieved using the calculation methods and limitations described in the rectification topologies sections.

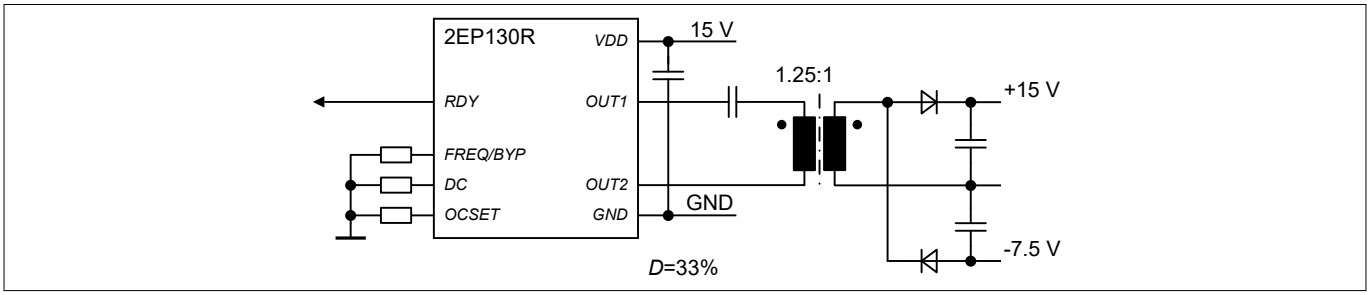


Figure 14 2EP130R with a single-output winding transformer

The single-output winding topology allows for the highest output power per channel.

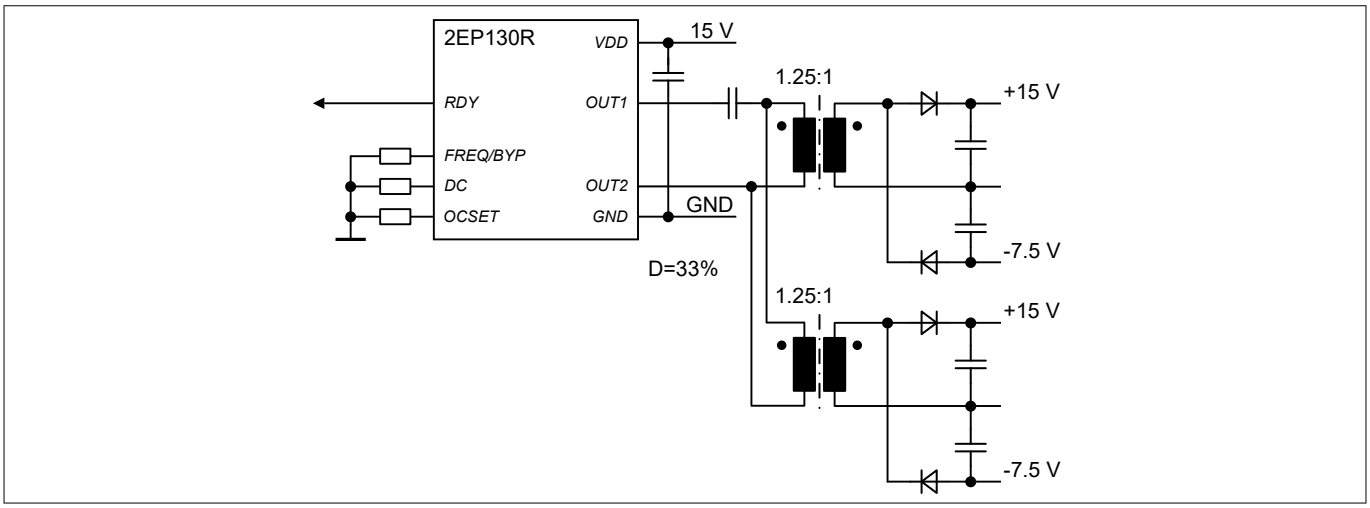


Figure 15 2EP130R with two single-output winding transformers

The topology with two single-output winding transformers shares its maximum output power with two channels. Due to individual transformers, the circuit routing can be optimized for the application.

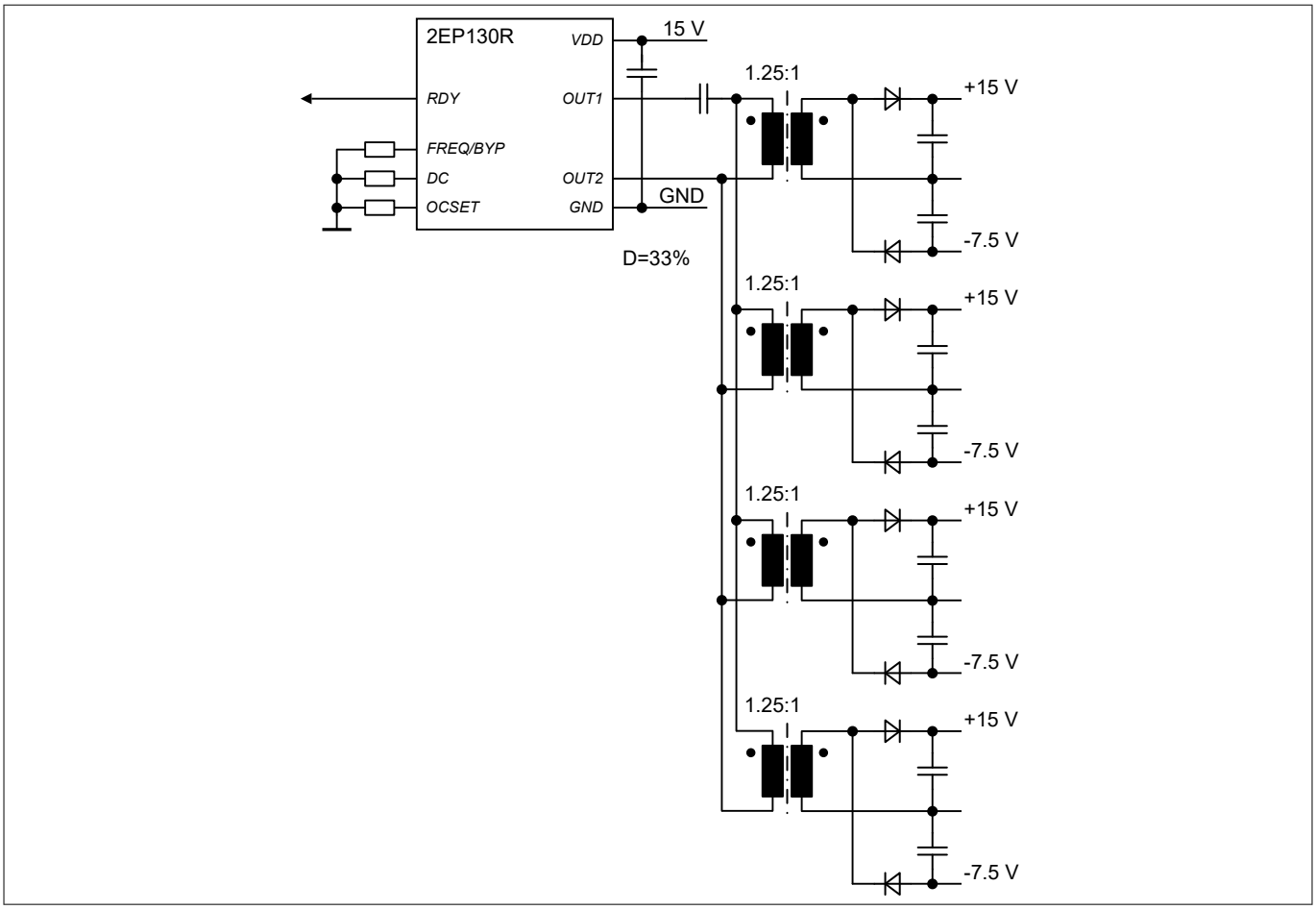


Figure 16 2EP130R with four single-output winding transformers

Adding more single-output winding transformers in parallel further reduces the maximum available output power per channel. The circuit can be optimized for symmetrical switching loads like in the primary and secondary sides of a dual active-bridge topology.

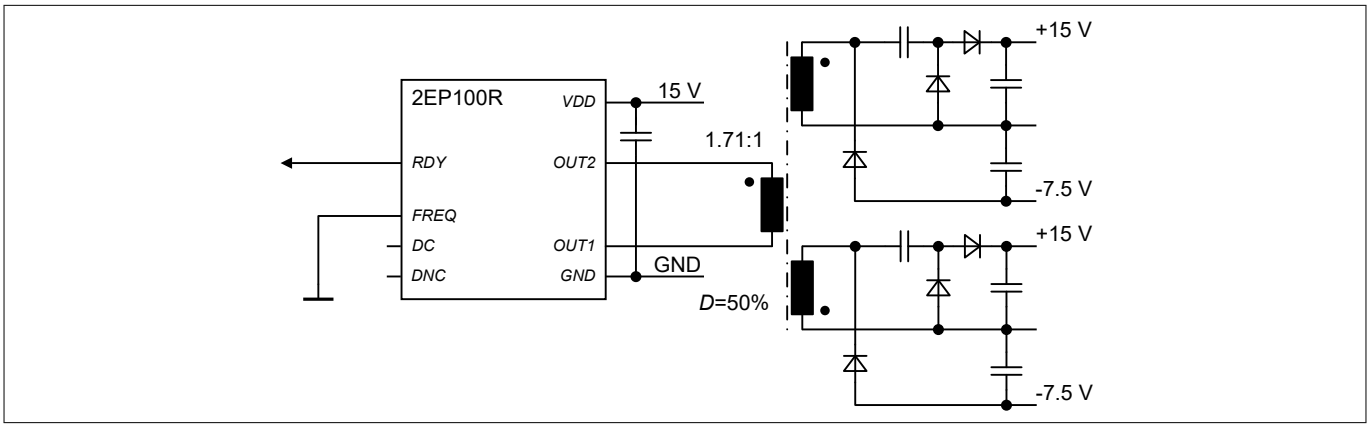


Figure 17 2EP130R with a dual-output winding transformer

The topology with a dual-output winding transformer offers a space saving circuit for all half-bridge based power topologies. Dual-output transformers with their shared magnetic core allow topologies like the voltage doubler rectification where a change of winding polarity at the outputs will turn an asymmetric load into a symmetric one.

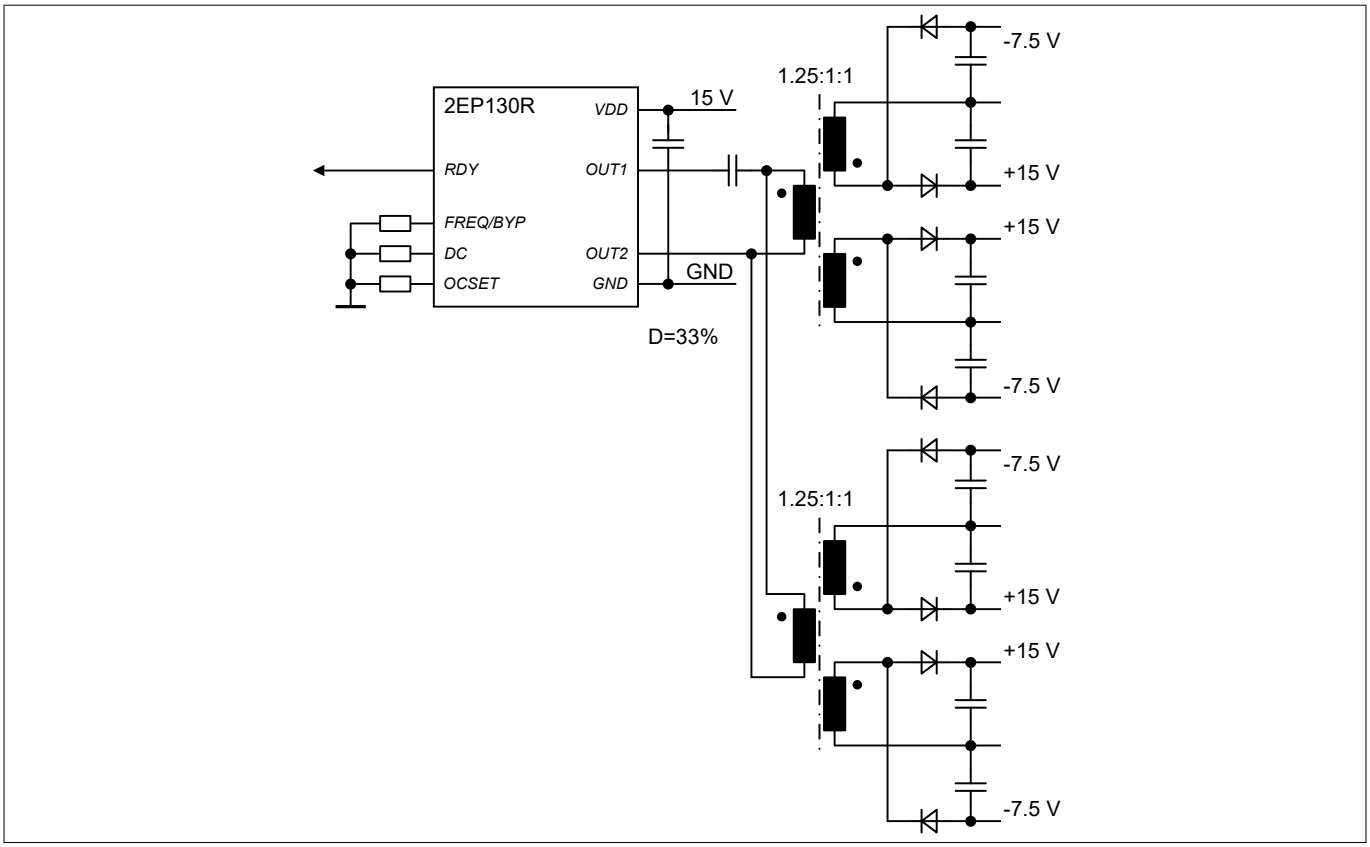


Figure 18 2EP130R with two dual-output winding transformers

The topology with two or more dual-output winding transformer offers a space saving circuit for all half-bridge based power topologies. The maximum output power per channel gets further reduced by the amount of transformers added.

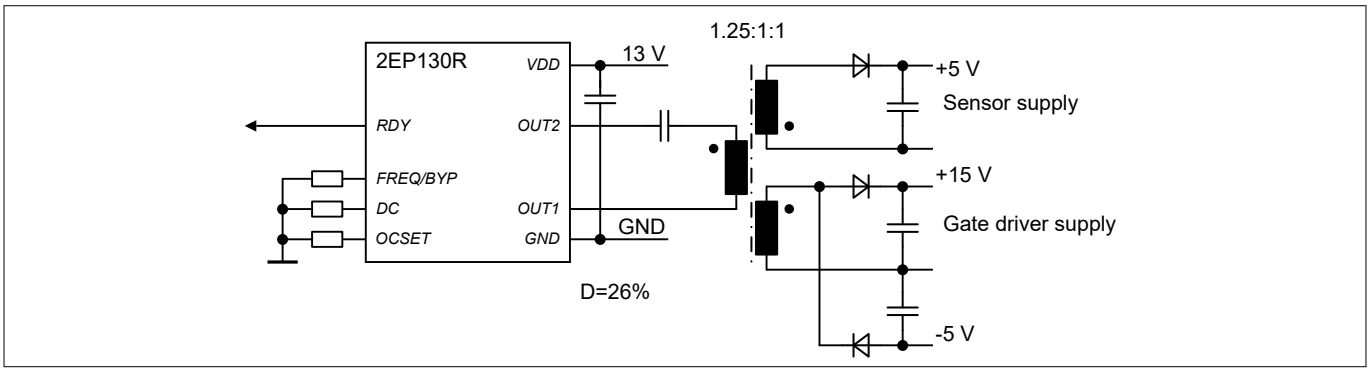


Figure 19 2EP130R with dual-output winding transformer for gate driver and sensor supply

The dual-output winding transformer can also be used for other loads needing an isolated supply. For example, a sensor supply using the same supply voltage amplitude as the negative rail of the gate driver supply portion. By rearranging the rectification circuit a formerly negative voltage can become a positive voltage for an independently isolated output winding. Take note of the winding and diode polarity. An excessive asymmetric load can have an impact on the output voltage ratio and should be evaluated at all operating conditions.

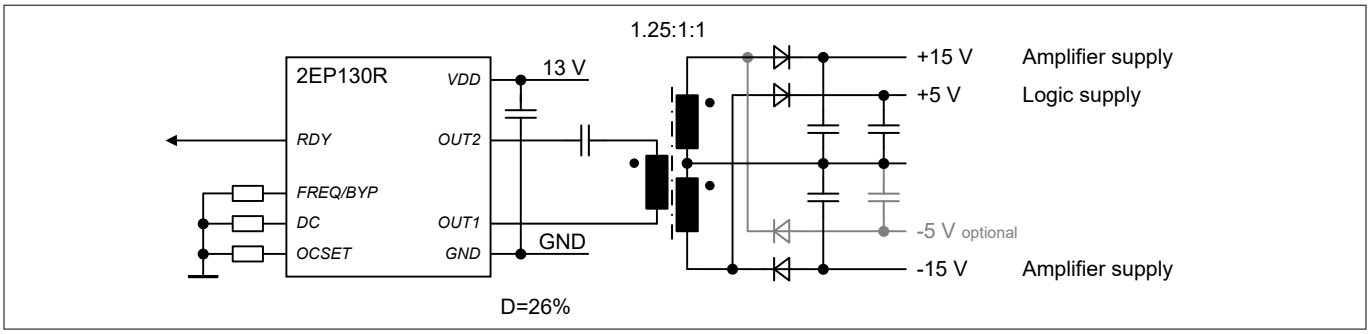


Figure 20 **2EP130R with dual-output winding transformer for differential amplifiers and sensor supply**

Using an interleaved peak rectification approach at a dual-output winding transformer can achieve two pairs of bi-polar supply voltages with adjustable ratio. As seen in this example, the upper output winding generates the positive 15 V and optionally the negative 5 V while the lower output winding generates the negative 15 V and the positive 5 V.

2.3 Output load

It is important to determine the maximum reachable output power for a given operating condition to estimate if the circuit design can work in the final application. This section provides some guidance on how to calculate such estimation values and apply them in an application.

2.3.1 2EP output power estimation

Estimation of the maximum output power available at the pins *OUT1* and *OUT2* requires the following parameters and use the values in brackets as an example value:

- Configured duty cycle of the 2EP: *D* (14%)
- Input voltage of the 2EP: V_{VDD} (15 V)
- Configured average overcurrent set: *OCSET* (5)
- Individual overcurrent threshold values for *OUT1* and *OUT2*: $I_{OCthr,x,1}$, $I_{OCthr,x,2}$

The *OCSET* parameter for the product variants 2EP100R, 2EP101R, and 2EP110R is fixed to 4. This parameter is adjustable for the 2EP130R from 1 to 5. Extracting the actual overcurrent threshold values for *OUT1* high and *OUT2* high from its datasheet table requires both the configured duty cycle and the *OCSET* parameter. Unless the duty cycle is set for close to 50%, the average overcurrent threshold differ between *OUT1* and *OUT2*:

Table 2 **Individual overcurrent thresholds depending on the configured duty cycle, *D*, and overcurrent setting level, *OCSET***

OCSET	**Ranges of duty cycle *D***					
	10% - 14%		**15% - 35%**		**36% - 50%**	
	***OUT1* high *OUT2* low**	***OUT2* high *OUT1* low**	***OUT1* high *OUT2* low**	***OUT2* high *OUT1* low**	***OUT1* high *OUT2* low**	***OUT2* high *OUT1* low**
1	$I_{OCthr,3}$	$I_{OCthr,0}$	$I_{OCthr,2}$	$I_{OCthr,0}$	$I_{OCthr,1}$	$I_{OCthr,1}$
2	$I_{OCthr,4}$	$I_{OCthr,0}$	$I_{OCthr,3}$	$I_{OCthr,1}$	$I_{OCthr,2}$	$I_{OCthr,2}$
3	$I_{OCthr,5}$	$I_{OCthr,1}$	$I_{OCthr,4}$	$I_{OCthr,2}$	$I_{OCthr,3}$	$I_{OCthr,3}$
4	$I_{OCthr,6}$	$I_{OCthr,2}$	$I_{OCthr,5}$	$I_{OCthr,3}$	$I_{OCthr,4}$	$I_{OCthr,4}$
5	$I_{OCthr,7}$	$I_{OCthr,3}$	$I_{OCthr,6}$	$I_{OCthr,4}$	$I_{OCthr,5}$	$I_{OCthr,5}$

Looking at the output stage and the current path of the 2EP, explains the meaning of *OUT1* high/*OUT2* low and *OUT2* high/*OUT1* low.

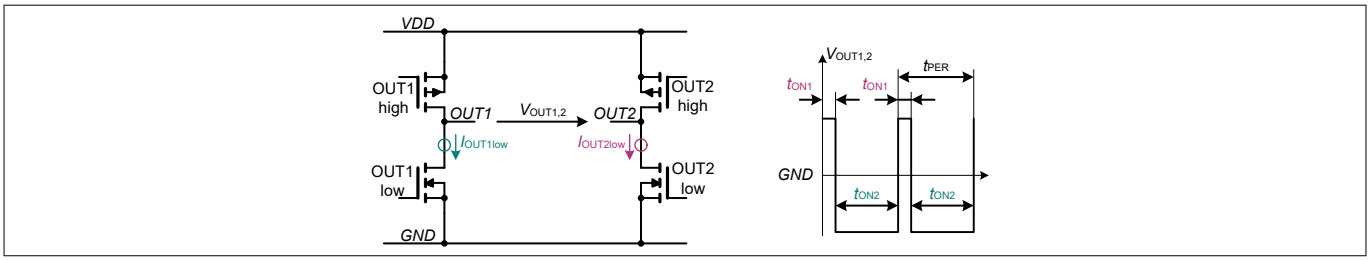


Figure 21 Current path mapping to individual segments of the switching period

This diagram shows the mapping of the individual current paths to the timing diagram of the outputs:

- Current during t_{ON1} flows through the *OUT1* high-side and the *OUT2* low-side switch
- Current during t_{ON2} flows through the *OUT2* high-side and the *OUT1* low-side switch

The duration of t_{ON1} together with the time period, t_{PER}, defines the duty cycle $D = \frac{t_{ON1}}{t_{PER}}$

For example: A *OCSET* = 4 with *D* = 14% gives us: $I_{OCthr,x,1} = I_{OCthr,7}$ and $I_{OCthr,x,2} = I_{OCthr,3}$.

These two current values would be the shutoff point of the 2EP average overcurrent protection and it is recommended to continue with the minimum threshold value as given in the datasheet. For example: $I_{OCthr,7,min}$ = 2900 mA and $I_{OCthr,3,min}$ = 200 mA.

The next step scales the two extracted average overcurrent threshold values according to their active duty cycle time:

$$\begin{aligned} &OUT1: \\ &I_{avg1} = D \cdot I_{OCthr,x,1} \\ &OUT2: \\ &I_{avg2} = (1-D) \cdot I_{OCthr,x,1} \end{aligned} \tag{5}$$

For this example, the minimum average overcurrent limit will be: I_{avg1} = 406 mA and I_{avg2} = 172 mA

Keeping in mind, that the average operational current should always be the same for both outputs. Take the minimum of both values to calculate the maximum achievable power:

$$P_{out} = 2 \cdot V_{VDD} \cdot \mathrm{MIN}\left(I_{avg1}, I_{avg2}\right) \tag{6}$$

For this example, the expected output power at the 2EP output pins results in P_{out} = 5.16 W.

I_{avg1} is not always smaller than I_{avg2}, this becomes clear when assuming a duty cycle of *D* = 15%. It does not look like a major change, but it results in different threshold values ($I_{OCthr,x,1} = I_{OCthr,6}$ and $I_{OCthr,x,2} = I_{OCthr,4}$) and therefore the scaled average values (I_{avg1} = 195 mA and I_{avg2} = 297.5 mA).

Using this calculation, allows the 2EP to deliver up to 13 W at its outputs for a duty cycle of *D* = 50%, supply voltage V_{VDD} = 20 V, and *OCSET* = 5.

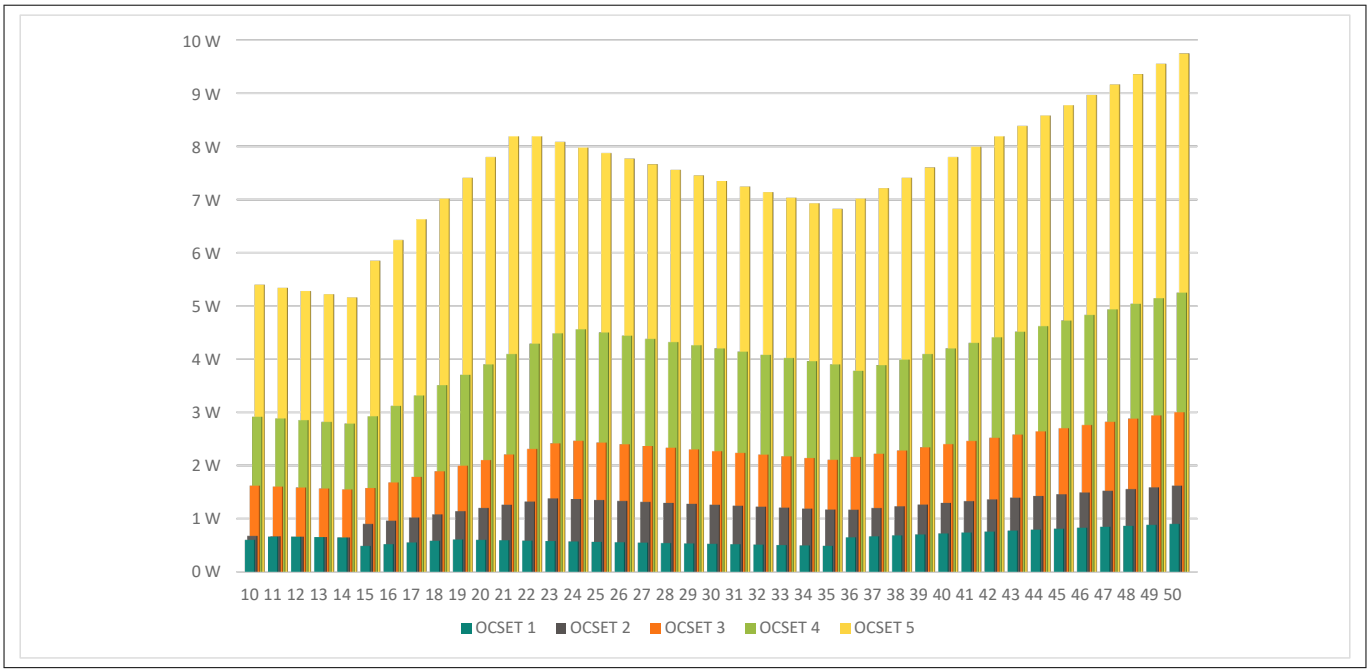


Figure 22 2EP output power over duty cycle at V_{VDD} = 15 V

The figure shows the maximum output power at the 2EP output pins calculated from the minimum overcurrent threshold values at a supply voltage of 15 V for all of the 5 *OCSET* options.

2.3.2 Circuit loss estimation

The output power at the 2EP output pins does not translate one-to-one into the available output power for the application. Thermal behavior and circuit losses will reduce and limit the usable power and need to be taken into account. These include:

- Thermal limitation of the 2EP
- Transformer losses including core (hysteresis and eddy current) and winding resistance
- Rectification component losses

The following subsections discuss some of these considerations.

Thermal limitation of the 2EP

The 2EP utilizes a MOSFET based full-bridge output stage to drive the external transformer and it also requires some internal operational current to operate. These electrical losses will increase the junction temperature and need to be dissipated to avoid an overtemperature shutdown. Use the following parameters for a simply loss estimation:

- Input supply voltage V_{VDD}
- No load supply current I_{VDD}
- Output stage average currents $I_{avg,x}$

The losses then consists of:

- Static IC operational losses: $P_{D,IC} = V_{VDD} \cdot I_{VDD}$
- Static IC switching losses: $P_{D,SS} = \left(I_{avg,1}^2 + I_{avg,2}^2\right) \cdot \left(R_{ON,H} + R_{ON,L}\right)$
- Dynamic IC switching losses: $P_{D,DS} = 2 \cdot \left(E_{ON} + E_{OFF}\right) \cdot f_{SW}$

The dynamic switching losses of the 2EP are not attainable through calculation and play also only a minor role for frequencies below 360 kHz. Here it is sufficient to add a 5% adder to the switching losses to have the total losses for thermal estimation: $P_{D,tot} = P_{D,IC} + 1.05 \cdot P_{D,SS}$

The expected junction temperature of the 2EP calculates as: $T_J = T_A + R_{th,JA} \cdot P_{D,tot}$ with T_A the worst case ambient temperature in the application and $R_{th,JA}$ the thermal resistance from the product datasheet. The

selected operating conditions will not limit the operation of the 2EP as long as the junction temperature T_J stays below the absolute maximum rating of the product. Exceeding it will result in thermal shutdown and interruption of the application operation. Note that heat dissipation from nearby components will increase the effective R_{th} of the IC compared to the datasheet value. The transformer is one of these components often neglected.

Transformer losses

The transformer losses can be split into core losses and copper losses (also known as winding or load losses).

Core losses contributed by the main inductance (also known as primary or magnetizing inductance) are composed of two components: hysteresis losses and eddy current losses. These contribute as no-load core losses. Hysteresis losses occur due to the energy required to magnetize and demagnetize the core material as the magnetic field changes. Eddy current losses, on the other hand, are caused by the currents that flow in the core material itself due to the changing magnetic field, and these can be significant in cores made of conductive materials. These losses are strongly depending on the transformer construction and cannot be described in more detail here.

The copper losses can be calculated from the AC winding resistance times the RMS winding current squared $P_{copper} = I_{RMS}^2 \cdot R_{AC}$. The actual current shape depends on the load and the leakage inductance. The leakage inductance contributes to the overall series impedance of the transformer and affects the current flow. To sum-up: it is not sufficient to simply assume the average DC current but evaluate the AC behavior influenced by the leakage inductance as well. Since the average currents used above for the thermal limitation of the 2EP are not useful here, the behavior of the transformer would need to be evaluated in the target application using a no-load and nominal load test.

Component losses of rectification

The losses due to the rectification method consists of the forward voltage drop during recharge of the output capacitors and the reverse recovery energy or reverse current of the diode during switched polarities of the transformer output voltage.

The forward voltage loses of the diodes can be estimated by multiplying the nominal forward voltage V_{DF} and the average output current $I_{avg,out}$ divided by the individual duty cycle D during the on-phase of the diode. The calculated result will probably be higher than the actual losses. That is based on the current shape during recharge and the varying forward voltage of the diode at different currents. $P_{D,on} = \frac{I_{avg,out}}{D} \cdot V_{DF}$. The amount of diodes to consider depend on the implemented rectification method.

The losses due to reverse recovery or reverse current are defined by the diode characteristics like reverse recovery time, reverse recovery charge, the overall reverse voltage in the application, and the reverse current. For a first estimation of losses this contribution could be neglected.

Summary

The output voltage in an ideal switch/transformer/rectification setup where losses are neglected can be easily calculated. However a real setup using the 2EP open-loop transformer driver IC, an off-the-shelf transformer, and rectifier diodes will always impact the output voltage at output load changes.

3 Use cases

The following use cases explain how to calculate and select components for an isolated power supply using the 2EP1xxR transformer driver IC in a given application. The steps are usually the same for all applications or functional blocks and are summarized here.

The calculation methods used in the following examples are described in the application section of the 2EP1xxR product datasheet.

Collect functional block and application requirements

- For gate driver supplies:
  - Required gate voltage to drive the power switch
  - Power switch total gate charge at selected gate voltage, load current, and application blocking voltage
  - Expected switching frequency of power switch
  - Expected idle load per channel (gate driver IC quiescent current, LED indicators, and others)
- For other supplies:
  - Required output voltage
  - expected load current at that output voltage
- Number of output channels required
- Define available input voltage

Derive rectification topology and partitioning

- Select rectification method which fulfills the output voltage requirements (unipolar, bipolar with specific positive to negative voltage ratio)
- Select the duty cycle parameter according to the rectification method and voltage ratio
- Select number of 2EP circuits based on output power requirements including estimated losses, input voltage, and duty cycle

Derive transformer requirements

- Calculate the turn ratio according to rectification method, required output voltages, and available input voltage
- Calculate the minimum voltage × time product from input voltage, 2EP switching frequency, and duty cycle to avoid transformer saturation
- Estimate a maximum winding resistance to limit the resistive transformer losses and output voltage drop
- Estimate a minimum main inductance to limit the magnetizing currents
- Estimate a leakage inductance according to expected load condition and EMI requirements

Cross check assumptions and calculations

- After component selection, re-calculate parameters with the actual known component values
- Evaluate usability for given functional block and application requirements

Selection of additional components

- Calculate the values of output capacitors to limit the output voltage ripple
- Calculate the value of the series capacitor for the peak rectification topology

3.1 Motor drive inverter

This use case describes the steps to determine the partitioning and component selection for a typical isolated power supply of the gate driver ICs in a motor drive inverter.

Motor drive inverter requirements for isolated gate driver supply

This example uses data from the EasyPACK™ FS100R12W2T7_B11 IGBT module.

- Required gate voltage to drive the power switch: Bipolar V_{CC} = +15 V and V_{EE} = -7.5 V
- Power switch total gate charge at selected gate voltage, load current, and application blocking voltage: Q_G = 1.4 µC
- Expected switching frequency of power switch: f_{sw} = 16 kHz
- Expected idle load per gate driver IC: P_{IC} = 2 mA × 22.5 V;
- Number of output channels: $n_{channels}$ = 6
- Available input voltage for gate supply: V_{DD} = 15 V

Rectification topology and partitioning

- Rectification method: Peak rectification
- Duty cycle for 2:1 output voltage ratio: D = 33%
- Number of required 2EP transformer driver ICs
  - Total required application output power: P_{APP} = 6 × 22.5 V × (2 mA + 1.4 µC × 16 kHz); P_{APP} = 3.3 W
  - Assuming overall circuit losses of 30% the transformer drivers would need to provide: $P_{OUT,2EP}$ = 4.3 W
  - A 2EP100R can provide 33% duty cycle but only offers OCSET=4, its power limit is approximately $P_{2EP100R,33\%,max}$ = 4.02 W. If the losses of the circuit components are lower than 21% then a single 2EP100R would be able to drive the 6 required output channels
  - A 2EP130R can be configured to an OCSET level of 5 achieving a much higher power limit: $P_{2EP130R,33\%,max}$ = 7.03 W. This type can drive these 6 channels easily
  - Summary: a single 2EP130R can be used and with careful evaluation a 2EP100R might still be able to provide enough power
- Partitioning: one 2EP driving one or more transformer primary sides to achieve 6 independent output voltages

Derive transformer requirements

- Turn ratio
  - Calculated assuming a 0.4 V diode forward voltage: $TTR_{(calc)}$ = 1.288 : 1 (primary to secondary)
  - Selected ratio should be a bit lower to get higher output voltages that can compensate the open-loop voltage drop: $TTR_{(sel)}$ = 1.25 : 1
- Transformer minimum voltage×time product (bipolar):
  - For $f_{SW,2EP}$ = 65 kHz: $Vt_{bipolar}$ = 2 × 15 V × 0.33×(1-0.33) / 65 kHz; $Vt_{bipolar}$ = 102 Vµs
  - For $f_{SW,2EP}$ = 103 kHz: $Vt_{bipolar}$ = 2 × 15 V × 0.33×(1-0.33) / 103 kHz; $Vt_{bipolar}$ = 64.4 Vµs
- Estimate a maximum winding resistance to limit the resistive transformer losses and output voltage drop:
  - For dV = 0.1 V drop: $R_{pri+sec,max}$ = 0.1 V × 22.5 V / (4.3 W × 2); $R_{pri+sec,max}$ = 0.27 Ω
  - For dV = 0.2 V drop: $R_{pri+sec,max}$ = 0.2 V × 22.5 V / (4.3 W × 2); $R_{pri+sec,max}$ = 0.54 Ω
- Estimate a minimum main inductance to limit the magnetizing currents to $I_{Lmain,pp}$ = 100 mA
  - For $f_{SW,2EP}$ = 65 kHz: $L_{main,min}$ = 2 × 15 V × 0.33×(1-0.33) / (65 kHz × 100 mA); $L_{main,min}$ = 1.02 mH
  - For $f_{SW,2EP}$ = 103 kHz: $L_{main,min}$ = 2 × 15 V × 0.33×(1-0.33) / (103 kHz × 100 mA); $L_{main,min}$ = 0.644 mH
- The leakage inductance needs to be selected according to expected load condition and EMI requirements between 0.1 µH and 2 µH
  - Lower leakage inductance limits voltage drop at higher loads but increases EMI
  - Higher leakage inductance recommended for low-load application use cases

Cross check assumptions and calculations

- Selected 2EP variant and parameter: 2EP130R, OCSET=5, duty cycle 33%, $f_{SW,2EP}$ = 103 kHz
- Selected transformer partitioning: 3 × dual output transformer in parallel
- Resulting output voltages: $V_{CC,calc}$ = 15.68 V; $V_{EE,calc}$ = -7.52 V
- Transformer requirements: $Vt_{bipolar}$ = 64.4 Vµs; $L_{main,min}$ = 0.644 mH
- Winding resistance for selected partitioning:
  - Primary: 3 windings in parallel: $R_{pri,max}$ = 3/2 × 0.27 Ω; $R_{pri,max}$ = 0.4 Ω
  - Secondary: 6 windings in parallel: $R_{sec,max}$ = 6/2 × 0.27 Ω; $R_{sec,max}$ = 0.8 Ω
- Note: These calculations use a lot of simplifications. It is strongly recommended to verify these parameters in a lab test

3.2 Fast EV charger

This use case describes the steps to determine the partitioning and component selection for a typical isolated power supply of the gate driver ICs in a DAB of an EV charger circuit.

DAB requirements for isolated gate driver supply

This example uses data from the EasyPACK™ F4-8MXTR12C2M2_H11 CoolSiC™ MOSFET M2 .XT fourpack module.

- Required gate voltage to drive the power switch: Bipolar V_{CC} = +18 V and V_{EE} = -2.2 V
- Power switch total gate charge at selected gate voltage, load current, and application blocking voltage: Q_G = 240 nC
- Expected switching frequency of power switch: f_{sw} = 49 kHz
- Expected idle load per gate driver IC: P_{IC} = 2 mA × 20.2 V;
- Number of output channels: $n_{channels}$ = 4 (or 8)
- Available input voltage for gate supply: V_{DD} = 15 V

Rectification topology and partitioning

- Rectification method: Peak rectification
- Duty cycle for 8.2:1 output voltage ratio: D = 12%
- Number of required 2EP transformer driver ICs
  - Total required application output power: P_{APP} = 4 × 20.2 V × (2 mA + 240 nC × 49 kHz); P_{APP} = 1.15 W
  - Assuming overall circuit losses of 30% the transformer drivers would need to provide: $P_{OUT,2EP}$ = 1.5 W
  - A 2EP101R can provide 12% duty cycle with OCSET=4, its power limit is approximately $P_{2EP101R,12\%,max}$ = 2.85 W
  - A 2EP130R can be configured to an OCSET level of 5 achieving a much higher power limit: $P_{2EP130R,12\%,max}$ = 5.28 W. This type can drive 8 channels easily
  - Summary: Both 2EP101R and 2EP130R can be used to provide enough power for at least 4 channels
- Partitioning: one 2EP driving one or more transformer primary sides to achieve 4 independent output voltages

Derive transformer requirements

- Turn ratio
  - Calculated assuming a 0.4 V diode forward voltage: $TTR_{(calc)}$ = 1.429 : 1 (primary to secondary)
  - Selected ratio should be a bit lower to get higher output voltages that can compensate the open-loop voltage drop: $TTR_{(sel)}$ = 1.4 : 1
- Transformer minimum voltage×time product (bipolar):
  - For $f_{SW,2EP}$ = 50 kHz: $Vt_{bipolar}$ = 2 × 15 V × 0.12×(1-0.12) / 50 kHz; $Vt_{bipolar}$ = 63.4 Vµs
  - For $f_{SW,2EP}$ = 65 kHz: $Vt_{bipolar}$ = 2 × 15 V × 0.12×(1-0.12) / 65 kHz; $Vt_{bipolar}$ = 48.8 Vµs

- Estimate a maximum winding resistance to limit the resistive transformer losses and output voltage drop:
  - For dV = 0.05 V drop: $R_{pri+sec,max}$ = 0.05 V × 20.2 V / (1.5 W × 2); $R_{pri+sec,max}$ = 0.31 Ω
  - For dV = 0.1 V drop: $R_{pri+sec,max}$ = 0.1 V × 20.2 V / (1.5 W × 2); $R_{pri+sec,max}$ = 0.62 Ω
- Estimate a minimum main inductance to limit the magnetizing currents to $I_{Lmain,pp}$ = 100 mA
  - For $f_{SW,2EP}$ = 50 kHz: $L_{main,min}$ = 2 × 15 V × 0.12×(1-0.12) / (50 kHz × 100 mA); $L_{main,min}$ = 0.634 mH
  - For $f_{SW,2EP}$ = 65 kHz: $L_{main,min}$ = 2 × 15 V × 0.12×(1-0.12) / (65 kHz × 100 mA); $L_{main,min}$ = 0.487 mH
- The leakage inductance needs to be selected according to expected load condition and EMI requirements between 0.1 µH and 2 µH
  - Lower leakage inductance limits voltage drop at higher loads but increases EMI
  - Higher leakage inductance recommended for low-load application use cases

Cross check assumptions and calculations

- Selected 2EP variant and parameter: 2EP130R, OCSET=4, duty cycle 12%, $f_{SW,2EP}$ = 65 kHz
- Selected transformer partitioning: 2 × dual output transformer in parallel
- Resulting output voltages: $V_{CC,calc}$ = 18.46 V; $V_{EE,calc}$ = -2.17 V
- Transformer requirements: $Vt_{bipolar}$ = 48.8 Vµs; $L_{main,min}$ = 0.487 mH
- Winding resistance for selected partitioning:
  - Primary: 2 windings in parallel: $R_{pri,max}$ = 2/2 × 0.31 Ω; $R_{pri,max}$ = 0.31 Ω
  - Secondary: 4 windings in parallel: $R_{sec,max}$ = 4/2 × 0.31 Ω; $R_{sec,max}$ = 0.62 Ω
- Note: These calculations use a lot of simplifications. It is strongly recommended to verify these parameters in a lab test

3.3 PV inverter

This use case describes the steps to determine the partitioning and component selection for a typical isolated power supply of the gate driver ICs in an inverter stage of a PV inverter circuit.

Inverter requirements for isolated gate driver supply

This example uses data from the F4-8MXTR12C2M2_H11 EasyDUAL™ 2B CoolSiC™ MOSFET half-bridge module.

- Required gate voltage to drive the power switch with short circuit rating: Bipolar V_{CC} = +15 V and V_{EE} = -5 V
- Power switch total gate charge at selected gate voltage, load current, and application blocking voltage: Q_G = 300 nC
- Expected switching frequency of power switch: f_{sw} = 48 kHz
- Expected idle load per gate driver IC: P_{IC} = 2 mA × 20 V;
- Number of output channels: $n_{channels}$ = 2 (or 6)
- Available input voltage for gate supply: V_{DD} = 15 V

Rectification topology and partitioning

- Rectification method: Peak rectification
- Duty cycle for 3:1 output voltage ratio: D = 25%
- Number of required 2EP transformer driver ICs
  - Total required application output power: P_{APP} = 6 × 20 V × (2 mA + 300 nC × 48 kHz); P_{APP} = 1.97 W
  - Assuming overall circuit losses of 30% the transformer drivers would need to provide: $P_{OUT,2EP}$ = 2.6 W
  - A 2EP110R can provide adjustable duty cycle with OCSET=4, its power limit is approximately $P_{2EP110R,25\%,max}$ = 4.5 W

  - A 2EP130R can be configured to an OCSET level of 5 achieving a much higher power limit: $P_{2EP130R,25\%,max}$ = 7.8 W
  - Summary: Both 2EP110R and 2EP130R can be used to provide enough power for all 6 channels
- Partitioning: one 2EP driving one or more transformer primary sides to achieve 6 independent output voltages

Derive transformer requirements

- Turn ratio
  - Calculated assuming a 0.4 V diode forward voltage: $TTR_{(calc)}$ = 1.442 : 1 (primary to secondary)
  - Selected ratio should be a bit lower to get higher output voltages that can compensate the open-loop voltage drop: $TTR_{(sel)}$ = 1.4 : 1
- Transformer minimum voltage×time product (bipolar):
  - For $f_{SW,2EP}$ = 50 kHz: $Vt_{bipolar}$ = 2 × 15 V × 0.25×(1-0.25) / 50 kHz; $Vt_{bipolar}$ = 112.5 Vµs
  - For $f_{SW,2EP}$ = 65 kHz: $Vt_{bipolar}$ = 2 × 15 V × 0.25×(1-0.25) / 65 kHz; $Vt_{bipolar}$ = 86.54 Vµs
- Estimate a maximum winding resistance to limit the resistive transformer losses and output voltage drop:
  - For dV = 0.05 V drop: $R_{pri+sec,max}$ = 0.05 V × 20 V / (2.6 W × 2); $R_{pri+sec,max}$ = 0.181 Ω
  - For dV = 0.1 V drop: $R_{pri+sec,max}$ = 0.1 V × 20 V / (2.6 W × 2); $R_{pri+sec,max}$ = 0.363 Ω
- Estimate a minimum main inductance to limit the magnetizing currents to $I_{Lmain,pp}$ = 100 mA
  - For $f_{SW,2EP}$ = 50 kHz: $L_{main,min}$ = 2 × 15 V × 0.25×(1-0.25) / (50 kHz × 100 mA); $L_{main,min}$ = 1.125 mH
  - For $f_{SW,2EP}$ = 65 kHz: $L_{main,min}$ = 2 × 15 V × 0.25×(1-0.25) / (65 kHz × 100 mA); $L_{main,min}$ = 0.866 mH
- The leakage inductance needs to be selected according to expected load condition and EMI requirements between 0.1 µH and 2 µH
  - Lower leakage inductance limits voltage drop at higher loads but increases EMI
  - Higher leakage inductance recommended for low-load application use cases

Cross check assumptions and calculations

- Selected 2EP variant and parameter: 2EP130R, OCSET=4, duty cycle 25%, $f_{SW,2EP}$ = 65 kHz
- Selected transformer partitioning: 3 × dual output transformer in parallel
- Resulting output voltages: $V_{CC,calc}$ = 15.67 V; $V_{EE,calc}$ = -4.96 V; In case the +15 V limit for the short circuit rating is more important, that value can be lowered by increasing the duty cycle by one or two percent points
- Transformer requirements: $Vt_{bipolar}$ = 86.54 Vµs; $L_{main,min}$ = 0.866 mH
- Winding resistance for selected partitioning:
  - Primary: 3 windings in parallel: $R_{pri,max}$ = 3/2 × 0.36 Ω; $R_{pri,max}$ = 0.54 Ω
  - Secondary: 6 windings in parallel: $R_{sec,max}$ = 6/2 × 0.36 Ω; $R_{sec,max}$ = 1.08 Ω
- Note: These calculations use a lot of simplifications. It is strongly recommended to verify these parameters in a lab test

3.4 Solid state circuit breaker

This use case describes the steps to determine the partitioning and component selection for a typical isolated power supply of the gate driver ICs and controller of a solid state circuit breaker.

SSCB requirements for isolated gate driver supply and controller

This example uses data from the IMDQ75R007M2H CoolSiC™ MOSFET 750 V G2 in Q-DPAK top-side cooled package as well as the XENSIV™ TLI5570-AE24E1-E0001 high precision coreless current sensor.

- Required gate voltage to drive the power switch: V_{CC} = +18 V
- Required supply voltage for the controller and sensors: V_{Sensor} = 3.3 V

- Power switch total gate charge at selected gate voltage, load current, and application blocking voltage: Q_G = 360 nC
- Expected idle load current for power switches since those are mostly statically on or off: I_{VCC} = 10 mA
- Expected idle load for sensor and controller: I_{Sensor} = 10 mA
- Available input voltage for supply: V_{DD} = 14 V

Rectification topology and partitioning

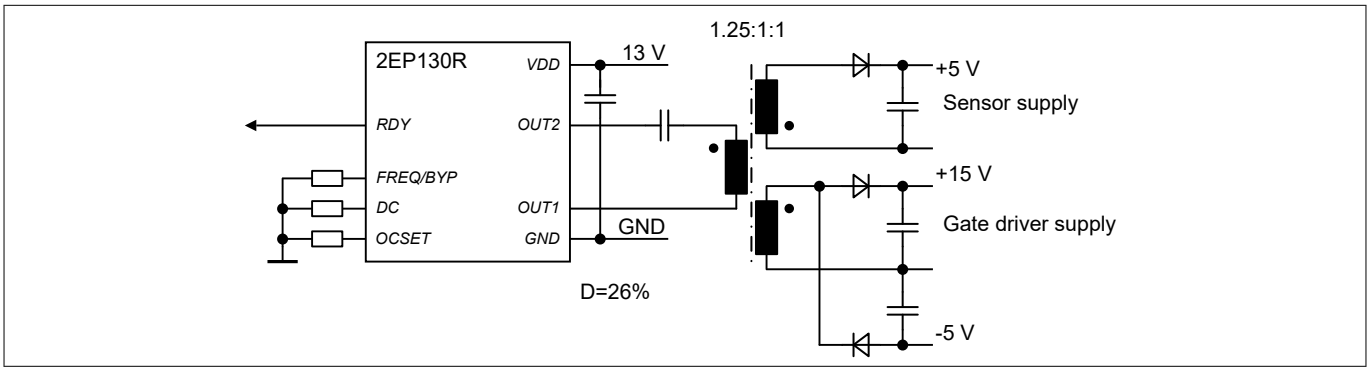


Figure 23 Topology for gate driver and sensor supply (example)

In this solid state circuit breaker example, the gate driver uses unipolar supply, so the negative supply portion here can be removed. The required voltage ratio is also different, which results in a changed duty cycle requirement.

- Rectification method: Peak rectification with dual output transformer and asymmetric rectification
- Duty cycle for 5.5:1 output voltage ratio: D = 17%
- The supply current consists of mostly idle current and therefore the 2EP power capabilities are more than enough
  - Total required application output power: P_{APP} = 18 V × 10 mA + 3.3 V × 10 mA; P_{APP} = 0.22 W
  - Assuming overall circuit losses of 30% the transformer driver would need to provide: $P_{OUT,2EP}$ = 0.28 W
  - A 2EP101R can provide 17% duty cycle with OCSET=4, its power limit is approximately $P_{2EP101R,17\%,max}$ = 3.1 W
  - A 2EP110R can provide adjustable duty cycle with OCSET=4, its power limit is also: $P_{2EP110R,17\%,max}$ = 3.1 W
  - Summary: 2EP101R, 2EP110R, and 2EP130R can be used to provide enough power for the solid state circuit breaker supply
- Partitioning: one 2EP driving one dual output transformer to achieve 2 independent output voltages

Derive transformer requirements

- Turn ratio
  - Calculated assuming a 0.4 V diode forward voltage: $TTR_{(calc)}$ = 1.267 : 1 (primary to secondary)
  - Selected ratio should be a bit lower to get higher output voltages that can compensate the open-loop voltage drop: $TTR_{(sel)}$ = 1.25 : 1
- Transformer minimum voltage×time product (bipolar):
  - For $f_{SW,2EP}$ = 50 kHz: $Vt_{bipolar}$ = 2 × 14 V × 0.17×(1-0.17) / 50 kHz; $Vt_{bipolar}$ = 79.02 Vµs
  - For $f_{SW,2EP}$ = 65 kHz: $Vt_{bipolar}$ = 2 × 14 V × 0.17×(1-0.17) / 65 kHz; $Vt_{bipolar}$ = 60.78 Vµs
- Estimate a maximum winding resistance to limit the resistive transformer losses and output voltage drop:
  - For dV = 0.05 V drop: $R_{pri+sec,max}$ = 0.05 V × 21.3 V / (0.28 W × 2); $R_{pri+sec,max}$ = 1.75 Ω
  - For dV = 0.1 V drop: $R_{pri+sec,max}$ = 0.1 V × 21.3 V / (0.28 W × 2); $R_{pri+sec,max}$ = 3.5 Ω

- Estimate a minimum main inductance to limit the magnetizing currents to $I_{Lmain,pp}$ = 100 mA
  - For $f_{SW,2EP}$ = 50 kHz: $L_{main,min}$ = 2 × 14 V × 0.17×(1-0.17) / (50 kHz × 100 mA); $L_{main,min}$ = 0.79 mH
  - For $f_{SW,2EP}$ = 65 kHz: $L_{main,min}$ = 2 × 14 V × 0.17×(1-0.17) / (65 kHz × 100 mA); $L_{main,min}$ = 0.61 mH
- The leakage inductance needs to be selected according to expected load condition and EMI requirements between 0.1 µH and 2 µH
  - Here a higher leakage inductance is recommended for this low-load application use case

Cross check assumptions and calculations

- Selected 2EP variant and parameter: 2EP101R, OCSET=4, duty cycle 17%, $f_{SW,2EP}$ = 65 kHz
- Selected transformer partitioning: 1 × dual output transformer
- Resulting output voltages: $V_{CC,calc}$ = 18.19 V; $V_{EE,calc}$ = -3.41 V;
- Transformer requirements: $Vt_{bipolar}$ = 60.78 Vµs; $L_{main,min}$ = 0.61 mH
- Winding resistance for selected partitioning:
  - Primary: 1 winding: $R_{pri,max}$ = 1/2 × 1.75 Ω; $R_{pri,max}$ = 0.87 Ω
  - Secondary: 2 windings in parallel: $R_{sec,max}$ = 2/2 × 1.75 Ω; $R_{sec,max}$ = 1.75 Ω
  - These calculated winding resistances are quite high and it is recommended to select lower ones for the transformer
- Note: These calculations use a lot of simplifications. It is strongly recommended to verify these parameters in a lab test; It might also be necessary to add a base load to the gate driver supply output to achieve a similar load current as for the 3.3 V rail to stabilize the voltage ratio

4 Related resources

- Product family website: Transformer Driver ICs
- Product datasheet: EiceDRIVER™ Power 2EP1xxR family datasheet
- Transformer specification calculator for 2EP1xxR: https://www.infineon.com/gated/infineon-transformer-specification-calculator-2ep1xxr-transformer-driver_a0ffc72e-bfdd-4f87-8cdc-c43d022157b4
- Developer community: https://www.infineon.com/part/2EP130R#community
- User guides for evaluation boards:
  - EVAL-2EP130R-PR: https://www.infineon.com/assets/row/public/documents/24/44/infineon-eval-2ep130r-pr-usermanual-en.pdf
  - EVAL-2EP130R-PR-SiC: https://www.infineon.com/assets/row/public/documents/24/44/infineon-eval-2ep130r-pr-sic-usermanual-en.pdf
  - EVAL-2EP130R-VD: https://www.infineon.com/assets/row/public/documents/24/44/infineon-eval-2ep130r-vd-usermanual-en.pdf

References

[1] Infineon Technologies AG: *EiceDRIVER™ Power 2EP1xxR family datasheet*; Available online
[2] Infineon Technologies AG: *EVAL-2EP130R-VD user guide*; Available online

Revision history

Document version	Date of release	Description of changes
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