100 W auxiliary power supply using CoolSET™ ICE502MD

EVAL_100W1_FF_502MD

About this document

Scope and purpose

This document demonstrates high-input-voltage 100 W DC link auxiliary power supply designs using Infineon's CoolSET™ ICE502MD switching controller and CoolSiC™ IMWF170R1K0M1 1700 V MOSFET in a TO-247 package in a single-switch flyback topology. The document can support designers working on three-phase converters that include solar inverters, energy storage systems, EV chargers, UPS, and motor drives.

The evaluation board is designed to showcase the performance of the CoolSET™ ICE502MD switching controller.

Intended audience

This document is intended for design engineers of auxiliary power supply designs in three-phase converters with Infineon's CoolSET™ ICE502MD PWM Fixed Frequency (FF) Gen5 Pro controller and CoolSiC™ 1700 V MOSFET.

Keypoints

- Demonstrates a 100 W auxiliary power supply design for high-voltage DC links using a single-switch flyback topology
- Explains implementation details including startup method, selectable gate voltage, frequency reduction, jittering, and protection features
- Provides test results for efficiency, thermal performance, load/line regulation, and dynamic response under varying input voltages
- Describes comprehensive protection mechanisms such as UVLO, OVP, overload, overtemperature, and line overvoltage for robust operation
- Highlights design benefits like wide input range, high efficiency, and suitability for three-phase applications including solar, EV chargers, and UPS

About this product family

Product family

Infineon's CoolSET™ integrated power stages, operating in a fixed-frequency switching scheme offers increased robustness and outstanding performance. This family offers superior energy efficiency, comprehensive protection features, and reduced system costs and is ideally suited for auxiliary power supply applications in a wide variety of potential applications such as:

- SMPS
- Renewables
- Server
- Telecom
- Home appliances

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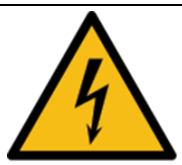
Safety precautions

Note: *Please note the following warnings regarding the hazards associated with development systems.*

Table 1 **Safety precautions**

	**Warning:** *The DC link potential of this board is up to 1000 VDC. When measuring voltage waveforms by oscilloscope, high voltage differential probes must be used. Failure to do so may result in personal injury or death.*
	**Warning**: *The evaluation or reference board contains DC bus capacitors which take time to discharge after removal of the main supply. Before working on the drive system, wait five minutes for capacitors to discharge to safe voltage levels. Failure to do so may result in personal injury or death. Darkened display LEDs are not an indication that capacitors have discharged to safe voltage levels.*
	**Warning:** *Remove or disconnect power from the drive before you disconnect or reconnect wires, or perform maintenance work. Wait five minutes after removing power to discharge the bus capacitors. Do not attempt to service the drive until the bus capacitors have discharged to zero. Failure to do so may result in personal injury or death.*
	**Caution:** *The heat sink and device surfaces of the evaluation or reference board may become hot during testing. Hence, necessary precautions are required while handling the board. Failure to comply may cause injury.*
	**Caution:** *Only personnel familiar with the drive, power electronics and associated machinery should plan, install, commission, and subsequently service the system. Failure to comply may result in personal injury and/or equipment damage.*
	**Caution:** *The evaluation or reference board contains parts and assemblies sensitive to electrostatic discharge (ESD). Electrostatic control precautions are required when installing, testing, servicing or repairing the assembly. Component damage may result if ESD control procedures are not followed. If you are not familiar with electrostatic control procedures, refer to the applicable ESD protection handbooks and guidelines.*
	**Caution:** *A drive that is incorrectly applied or installed can lead to component damage or reduction in product lifetime. Wiring or application errors such as undersizing the motor, supplying an incorrect or inadequate AC supply, or excessive ambient temperatures may result in system malfunction.*
	**Caution:** *The evaluation or reference board is shipped with packing materials that need to be removed prior to installation. Failure to remove all packing materials that are unnecessary for system installation may result in overheating or abnormal operating conditions.*

1 Introduction

The EVAL_100W1_FF_502MD evaluation board is developed to support customers designing auxiliary power supplies for three-phase converters using CoolSET™ ICE502MD PWM Fixed Frequency Gen5 Pro controller and CoolSiC™ 1700 V MOSFET in a single-switch flyback topology. The board has a single output of +24 V with up to 100 W output power working in a wide input voltage range from 200 V_{DC} to 1000 V_{DC}. Its potential applications are three-phase systems having a high input voltage DC link. This application note contains an overview of the evaluation board's operation, product information, and technical details with measurement results. This information can help customers during their design-in phase, and for reuse of the board for their own specific requirements.

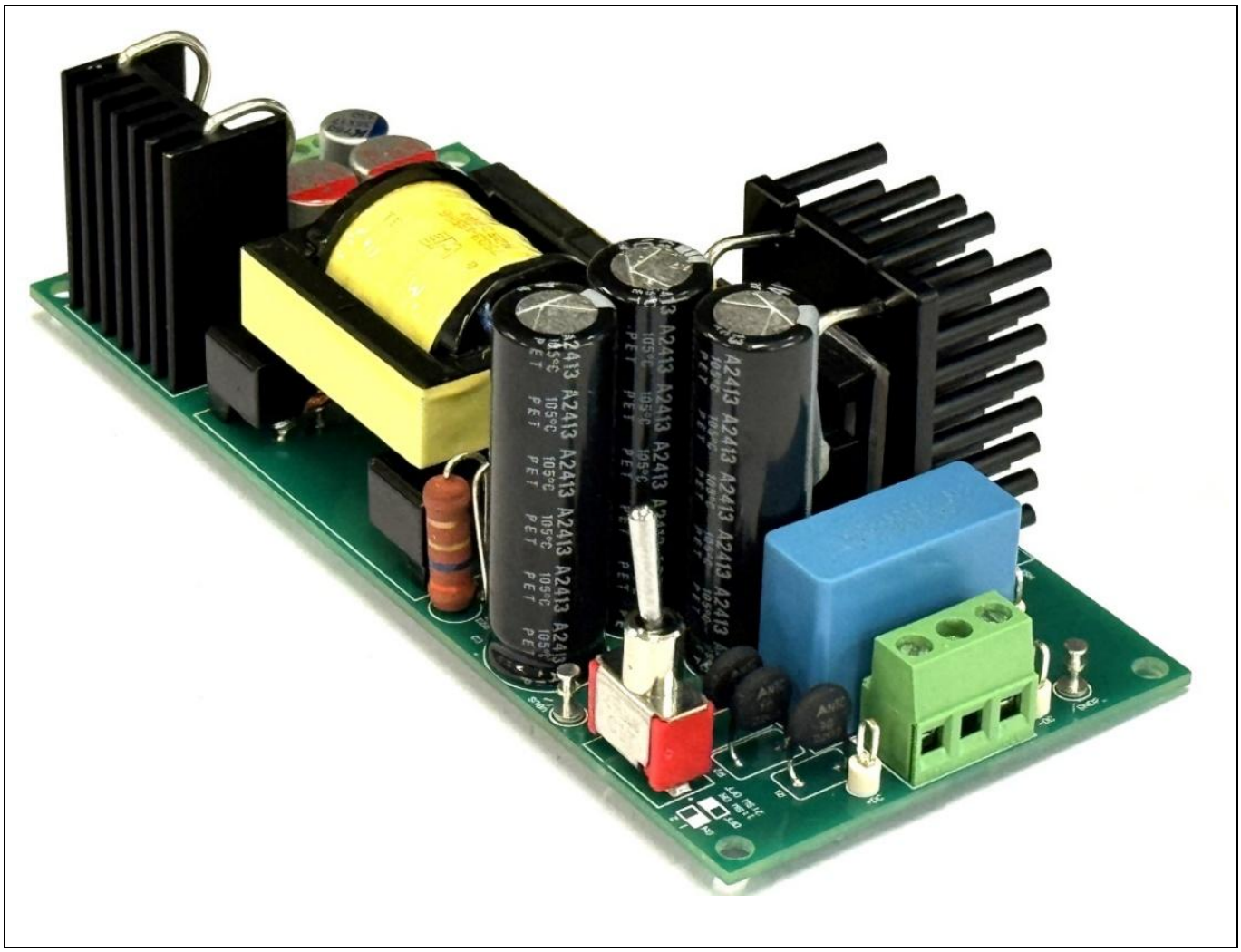


Figure 1 Isometric view of EVAL_100W1_FF_502MD evaluation board

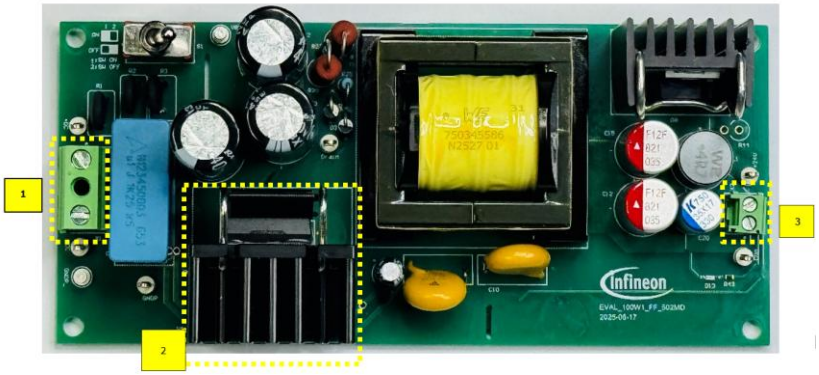
2 Evaluation board overview

2.1 Board features

The key features of the controller ICE502MD used in the evaluation board are:

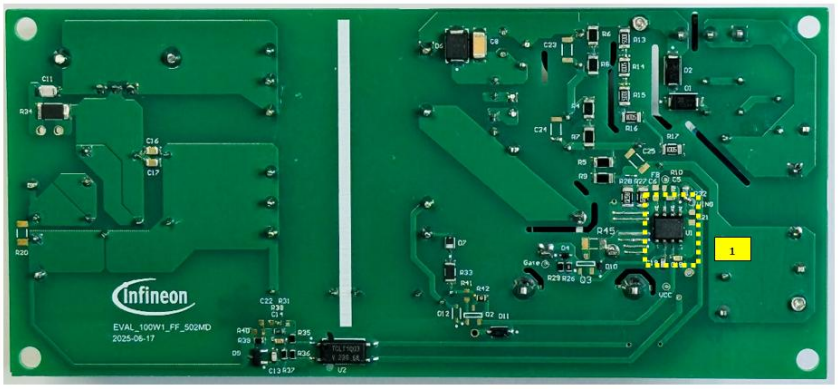
- Externally selectable gate voltage of 10 V, 15 V, and 18 V
- Fast start-up through cascode configuration
- Integrated error amplifier to implement primary side control, if required
- Frequency reduction for improved light load efficiency
- Comprehensive protection including line over-voltage protection

2.2 Board details



1. Input voltage connector
2. CoolSiC™ 1700 V MOSFET
3. Output voltage +24 V connector

Figure 2 Board top side



1. CoolSET™ ICE502MD PWM Fixed Frequency Gen5 Pro controller

Figure 3 Board bottom side

2.3 EVAL_100W1_FF_502MD technical specifications

The EVAL_100W1_FF_502MD evaluation board is intended to support customers designing an auxiliary power supply for three-phase converters using Infineon's CoolSET™ ICE502MD PWM Fixed Frequency Gen5 Pro controller and CoolSiC™ 1700 V MOSFET. Potential applications include solar inverters, energy storage, EV chargers, UPS, and motor drives. Table 2 lists the key specifications of the board.

Table 2 EVAL_100W1_FF_502MD evaluation board specifications

Input voltage	200 V_{DC} to 1000 V_{DC}
Output power	100 W
Topology	Single switch flyback
Output voltage	24 V
Output current	4.2 A
Switching frequency	100 kHz with frequency foldback for lighter loads
Efficiency at full load	>85%
Regulation	Secondary side regulated control
PWM gate voltage	15 V
Protections	All as mentioned in the datasheet with line OVP set to 1050 V
Isolation	Reinforced, 3 kV
Form factor case size (L x W x H)	134 mm x 60 mm x 40 mm

2.4 Wiring and switch S1 polarity

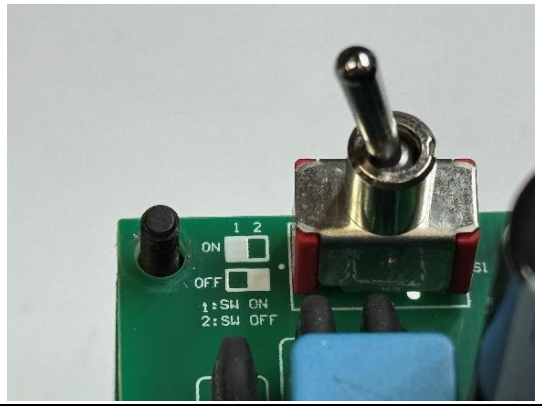
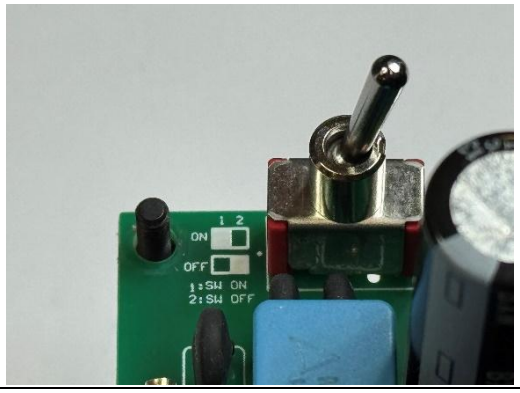
Input and output wiring		Ensure that there is no loose wire connections. Recommendation is not to use too exposed wire for input connection to prevent accidental shorting.
S1 Switch ON		Bypass the NTCs R1, R2, R3, and diodes D1 and D2 for efficiency measurement. Ensure not to apply reverse polarity at the input.
S1 Switch OFF		In case of non-efficiency related measurements, keep the switch in the off state to protect the board under accidental reverse polarity input connection.
WARNING: DO NOT CHANGE THE POSITION OF THE SWITCH IN RUNNING CONDITION. ENSURE THAT THE INPUT IS DISCONNECTED AND INPUT BULK CAPACITOR IS COMPLETELY DISCHARGED BEFORE CHANGING THE SWITCH STATE.		

Figure 4 Wiring diagram

2.5 Schematic

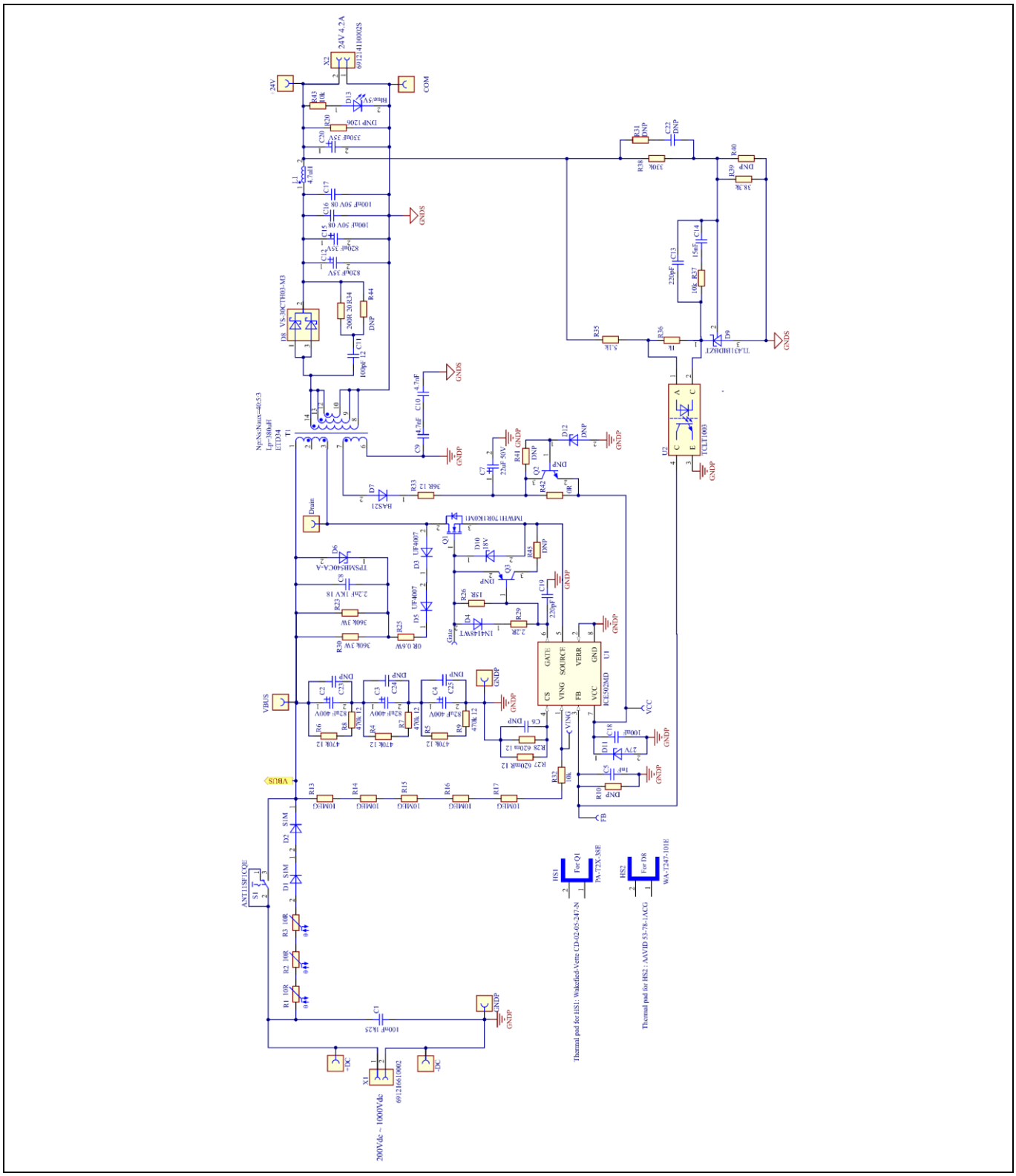


Figure 5 Schematic

2.6 PCB layout

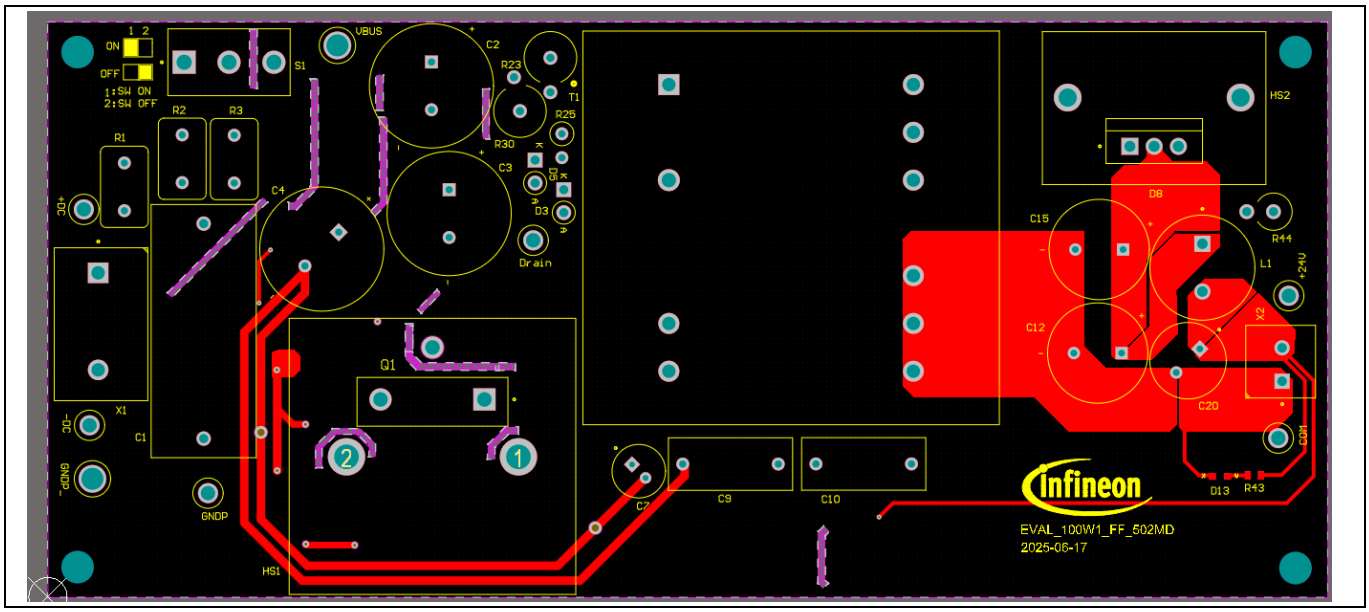


Figure 6 Top view

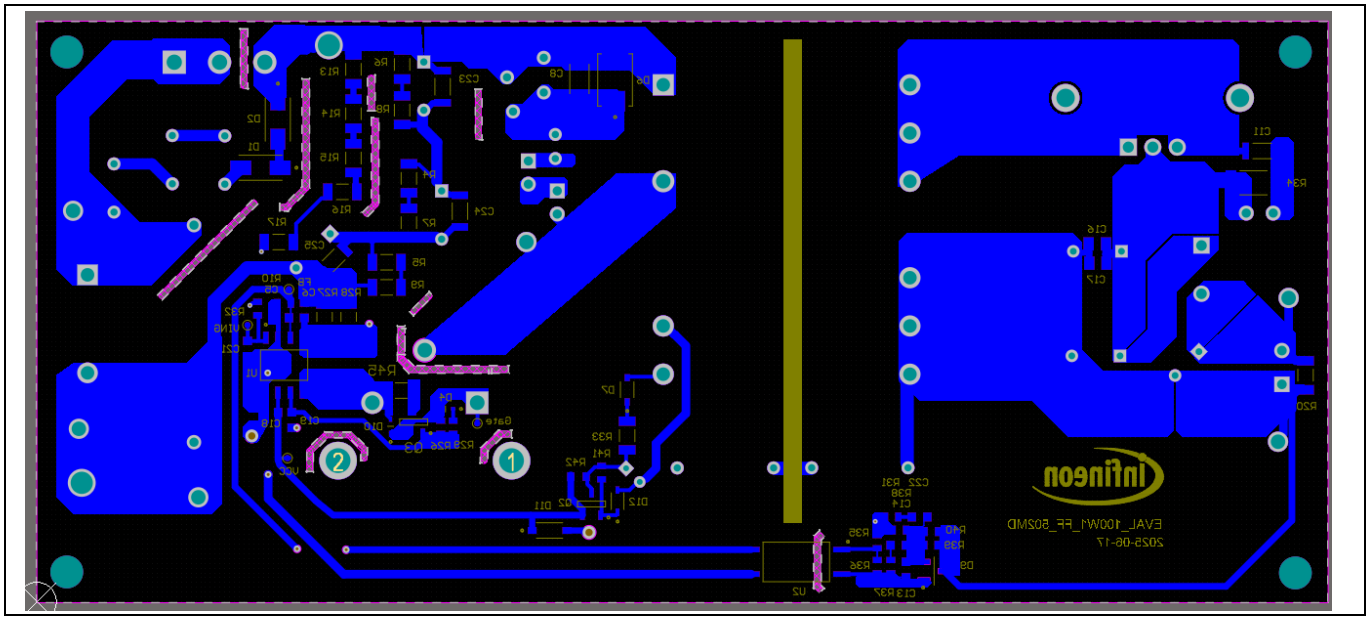


Figure 7 Bottom view

2.7 Bill of materials

Table 3 Bill of materials

Item	Designator	Quantity	Value	Package	Manufacturer	Manufacturer order number
1	C1	1	100 nF 1 k25	-	-	B32653A7104J
2	C11	1	100 pF 1 kV	1206	-	GRM31A5C3A101JW01
3	C12, C15	2	820 µF 35 V	-	-	RPF1018821M035K
4	C13, C19	2	220 pF	0603	-	GRM1885C1H221GA01
5	C14	1	15 nF	0603	-	GRM188R71H153JA01
6	C16, C17	2	100 nF 50 V	0805		C0805C104J5RAC
7	C18	1	100 nF 50 V	0603	-	06035C104K4Z2A
8	C2, C3, C4	3	82 µF 400 V	-	-	400BXW82MEFR12.5X40
9	C20	1	330 µF 35 V	-	-	A750KW337M1VAAE020
10	C21	1	DNP	-	-	-
11	C22	1	DNP	-	-	-
12	C23, C24, C25	3	DNP	-	-	-
13	C5	1	1 nF	0603	-	GRM188R71C102KA01
14	C6	1	DNP	-	-	-
15	C7	1	22 µF 50 V	-	-	50PX22MEFC5X11
16	C8	1	2.2 nF 1 kV	1808	-	1808AC222KAT1A
17	C9, C10	2	4.7 nF 1.5 kV	-	-	VY1472M51Y5VQ63V0
18	D1, D2	2	S1M	-	-	S1M-13-F
19	D10	1	18 V zener	-	-	SZMM5Z18VT1G
20	D11	1	27 V zener	-	-	BZT52C27W
21	D12	1	DNP	-	-	-
22	D13	1	Red/5 V LED	-	Würth Elektronik	150060RS75003
23	D3, D5	2	UF4007	-	-	UF4007-E3/54
24	D4	1	1N4148WT	-	-	1N4148WT-7
25	D6	1	TPSMB540CA-A	-	-	TPSMB540CA-A
26	D7	1	BAS21	-	Infineon Technologies	BAS21-03W or BAS21HT1G

Evaluation board overview

Item	Designator	Quantity	Value	Package	Manufacturer	Manufacturer order number
27	D8	1	VS-30CTH03-M3	-	-	VS-30CTH03-M3
28	D9	1	TL431BIDBZT	-	-	TL431BIDBZT
29	HS1	1	PA-T2X-38E	-	-	PA-T2X-38E
30	HS2	1	WA-T247-101E	-	-	WA-T247-101E
31	L1	1	4.7 µH	-	Würth Elektronik	7447471047
32	Q1	1	IMWH170R1K0M1	-	Infineon Technologies	IMWH170R1K0M1
33	Q2	1	DNP	-	-	-
34	Q3	1	DNP	-	-	-
35	R1, R2, R3	3	10R	-	-	B57153S0100M000
36	R10, R31	2	DNP	-	-	-
37	R13, R14, R15, R16, R17	5	10MEG	1206	-	MCHVR06FTFV1005
38	R20	1	DNP	-	-	-
39	R23, R30	2	360k 3 W	-	-	RR03J360KTB
40	R25	1	0R 0.6 W	-	-	MBB02070Z0000ZCT00
41	R26	1	15R	0603	-	CRCW060315R0FK
42	R27	1	620mR	1206	-	CSR1206FTR620
43	R28	1	620mR	1206	-	CSR1206FTR620
44	R29	1	2.2R	0603	-	CRCW06032R20FK
45	R32, R37, R43	3	10k	0603	-	CRCW060310K0FKEA
46	R33	1	36R	1206	-	CRCW120636R0FK
47	R34	1	200R	2010	-	CRCW2010200RFK
48	R35	1	5.1k	0603	-	CRCW06035K10FK
49	R36	1	1k	0603	-	CRCW06031K00FK
50	R38	1	330k	0603	-	CRCW0603330KFK
51	R39	1	38.3k	0603	-	CRCW060338K3FK
52	R4, R5, R6, R7, R8, R9	6	470k	1206	-	CRCW1206470KFKEA
53	R40	1	DNP	-	-	-
54	R41	1	DNP	-	-	-
55	R42	1	0R	-	-	RC0603JR-070RL

Evaluation board overview

Item	Designator	Quantity	Value	Package	Manufacturer	Manufacturer order number
56	R44	1	DNP	-	-	-
57	R45	1	DNP	-	-	-
58	S1	1	ANT11SF1CQE	-	-	ANT11SF1CQE
59	T1	1	ETD34	-	Würth Electronik	750345586 R01
60	U1	1	ICE502MD	-	Infineon Technologies	ICE502MD
61	U2	1	TCLT1003	-	-	TCLT1003
62	X1	1	691216610002	-	Würth Elektronik	691216610002
63	X2	1	691214110002S	-	Würth Elektronik	691214110002S
64	+24V, +DC, COM, -DC, Drain, GNDP	6	5012	-	-	5012
65	VBUS	1	1502-2	-	-	1502-2
66	GNDP_	1	1502-2	-	-	1502-2
67	Thermal pad for D8	1	TO220 Thermal pad	-	-	53-78-1ACG
68	Thermal pad for Q1	1	TO247 Thermal pad	-	-	CD-02-05-247-N
69	Thermal grease for HS1 and HS2	thin layer	Thermal grease	-	-	S606 or equivalent

2.8 Transformer construction

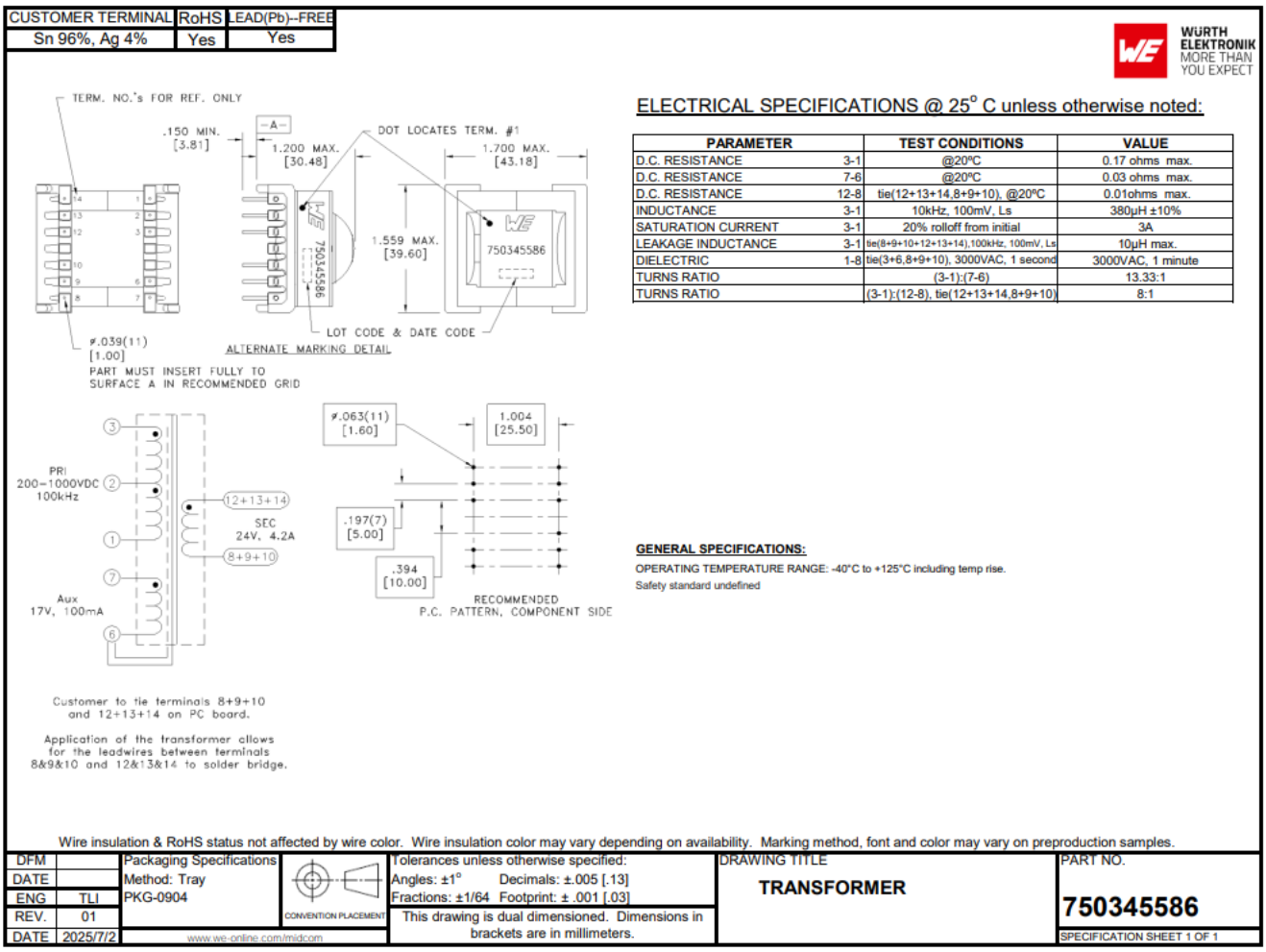


Figure 8 Transformer datasheet

Table 4 Transformer specifications

Manufacturer and part number	Wurth 750345586
Core size	ETD 34
Core material	DMR95
Bobbin	14 pin ETD34 Horizontal
Primary inductance	380 µH
Leakage inductance	< 10 µH
Turns ratio (Primary: +24 Vout secondary: auxiliary)	40:5:3

3 Circuit description

3.1 Startup

Startup is implemented using the cascode method. When a sufficient line voltage is applied, a pull-up resistor at the VING pin (R13, R14, R15, R16, R17 and R32) from the system bus provides a current to turn on the external CoolSiC™ device (Q1). Q1 is operated in linear mode to charge the VCC capacitor until the VCC voltage reaches V_{VCC_ON}.

Soft-start commences after V_{VCC_ON}. The soft start implemented in ICE502MD is a digital time-based function. The preset soft-start time is 12 ms with four steps. If not limited by other functions, the peak voltage on the CS pin will increase in increments from 0.3 V to 0.8 V (V_{CS_N}). The VCC voltage is supplied by the auxiliary winding of the transformer. VCC short-to-GND protection is implemented during startup.

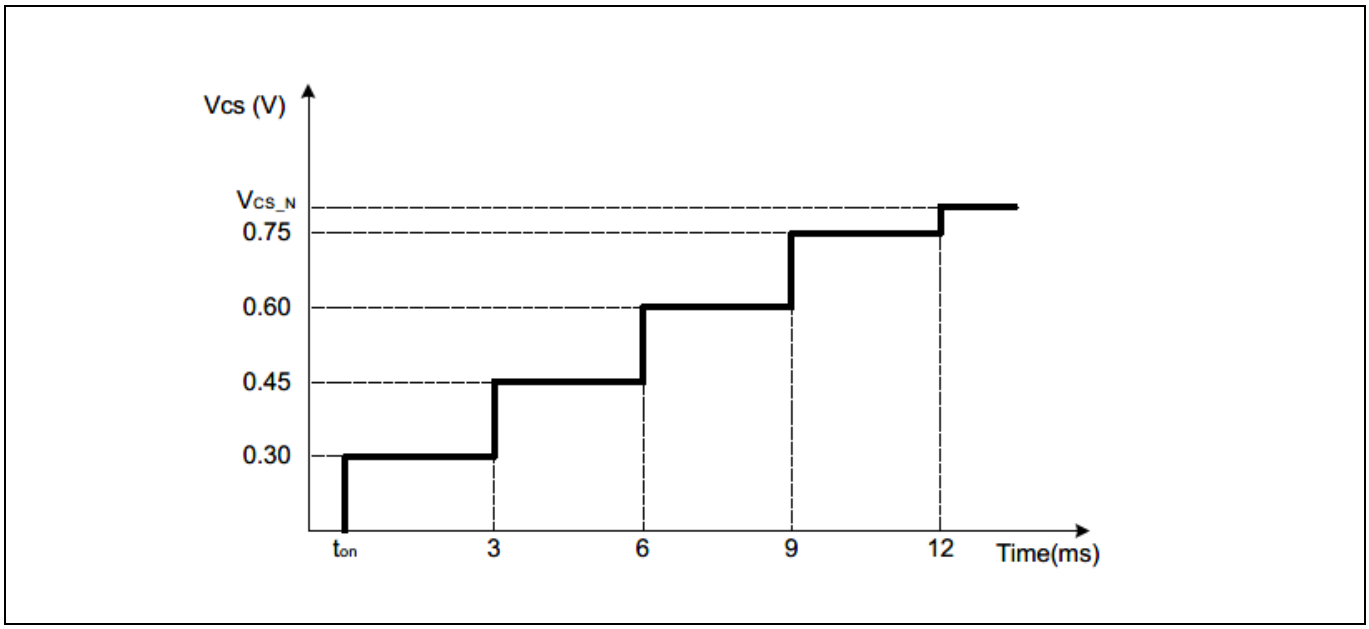


Figure 9 Soft-start phase

If LOVP is not required and should be disabled, the VING pin can be connected to ground. Startup can then be achieved via a pull-up resistor from the DC bus to the Gate pin of the controller, as shown in Figure 10.

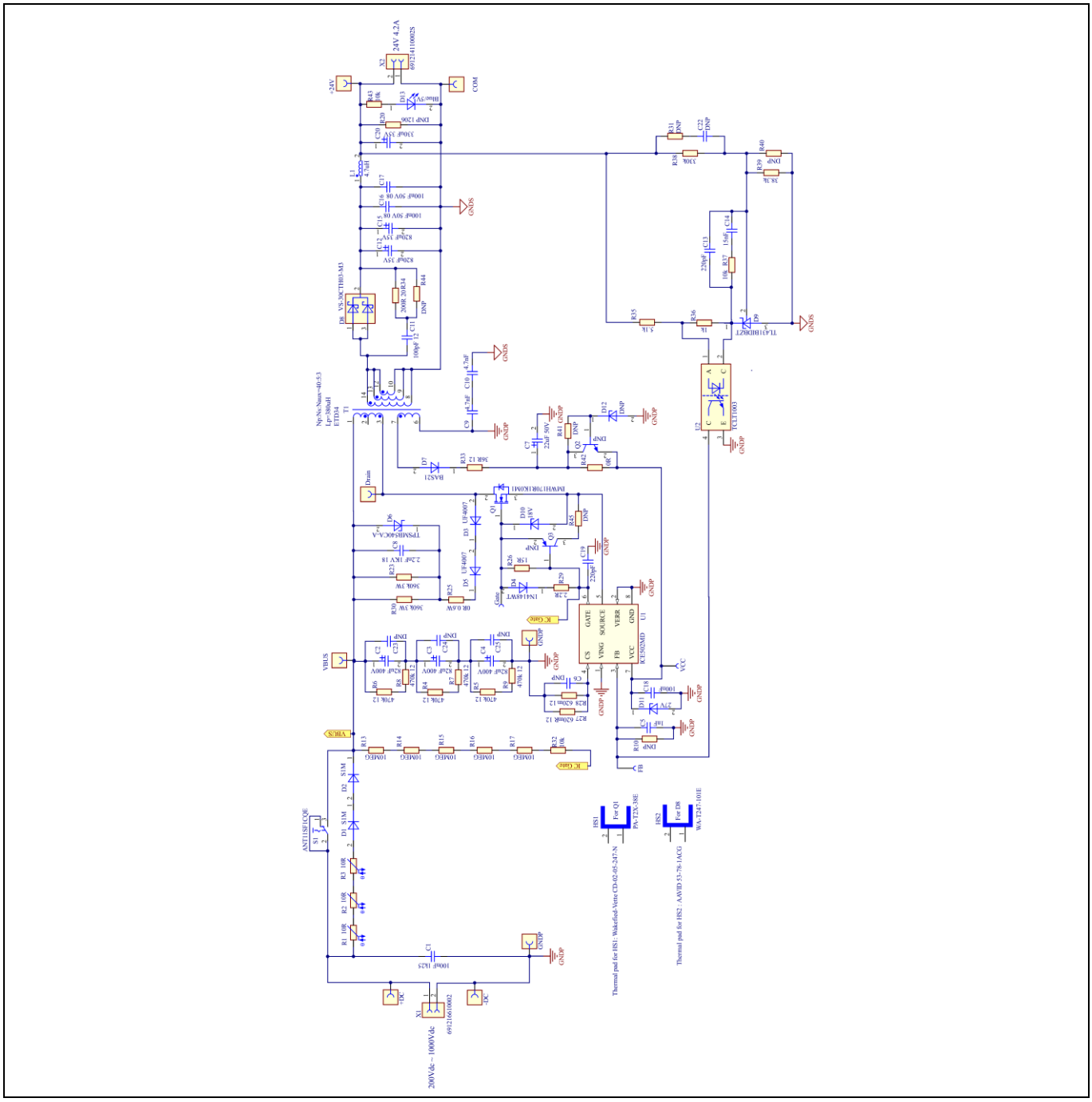


Figure 10 Secondary-side regulated isolated flyback design with line OVP disabled

3.2 ICE502MD selectable gate drive voltage

One of the unique features of ICE502MD is that it allows selectable gate voltage to drive a variety of switches (both Si and CoolSiC™). The gate voltage can be selected by changing the RSEL at the FB pin. There are three configuration options for different V_{GATE} gate drive voltages. Table 5 shows the control logic for selecting the gate voltage using RSEL.

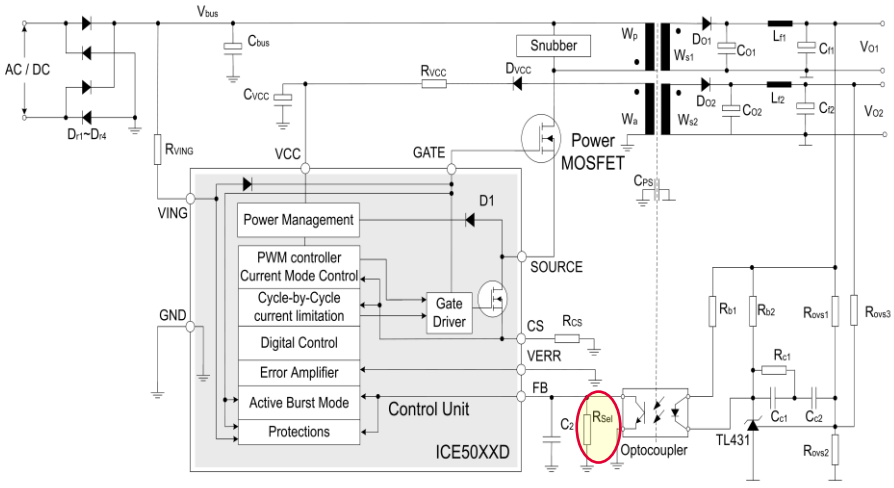


Figure 11 RSEL for selecting gate drive voltage

Table 5 Gate voltage selection

Option	RSEL	V_{GATE}
1	300 kΩ ~ 502 kΩ	10 V
2	721 kΩ ~ 797 kΩ	18 V
3	> 1.14 MΩ or open	15 V

3.3 Frequency foldback

ICE502MD uses a peak current-mode control scheme. When operating at maximum power, the switching frequency is f_{OCX} (100 kHz for ICE502MD). As the load reduces, the feedback voltage also reduces. To improve the efficiency at light loads, a frequency foldback scheme is introduced. The frequency keeps reducing as the load becomes lighter until it reaches the minimum switching frequency f_{OSCX_MIN}. If the load is reduced further, the controller enters active burst mode (ABM), where the switching frequency is clamped to f_{OCX_ABM} and the V_{CS} is limited by V_{CS_B}. The controller supports continuous conduction mode (CCM) under low line, heavy-load conditions to improve efficiency. Figure 12 shows the frequency reduction curve.

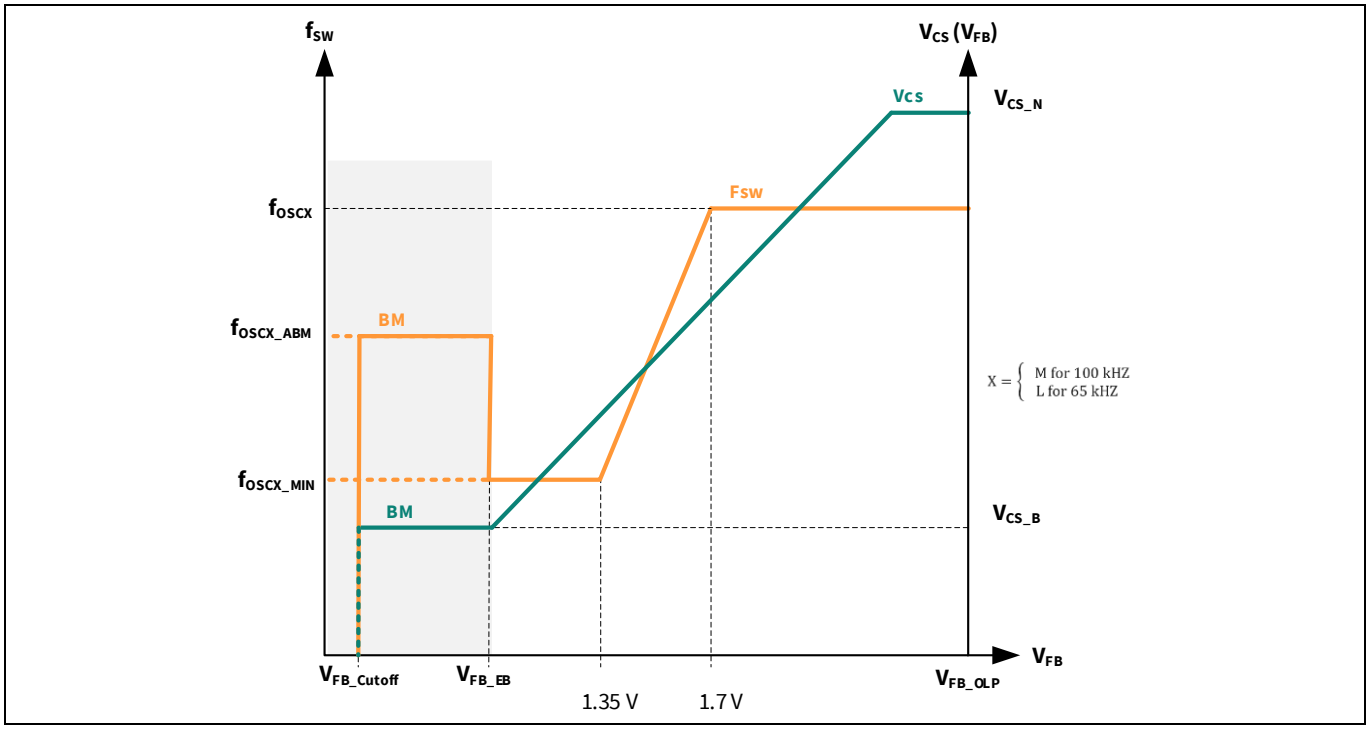


Figure 12 Frequency reduction curve

3.4 Frequency jittering

ICE502MD includes a frequency jittering feature to reduce the EMI noise. The jitter frequency is internally set to 100 kHz (±4 kHz) and the jitter period is 4 ms.

3.5 RCD clamper circuit

A clamper network (R30, R23, C8, D5, D3, and D6) dissipates the energy of the leakage inductance and suppress the ringing on the SMPS transformer.

3.6 Output stage

There is a single output on the secondary side, 24 V. The power is coupled out via the ultra-fast diode (D8). The output capacitors (C12 and C15) provide energy buffering followed by the L-C filters (L1-C20) to reduce the output ripple. The selected output capacitors must have an internal resistance (ESR) as low as possible to minimize the output voltage ripple caused by the triangular current.

3.7 Feedback loop

For feedback (FB), the output is sensed by the voltage divider (R38 and R39) and compared with the internal reference voltage D9 (TL431). The capacitors and resistor (C13, R37, and C14) form the compensation network. The output voltage of D9 (TL431) is converted into a current signal via the optocoupler U2 and two resistors (R35 and R36) for regulation control.

3.8 Active burst mode (ABM)

As mentioned in Section 3.3 and shown in Figure 12, under light-load conditions, the SMPS enters active burst mode (ABM) operation. At this stage, the controller is always active but keeps V_{VCC} above the switch-off threshold.

To enter ABM operation, two conditions must be met:

- The FB voltage must be lower than the V_{FB_EB} threshold
- A blanking time (t_{FB_BEB}) is required

Once both conditions are met, the ABM flip-flop is set, and the controller enters ABM operation. This dual condition requirement ensures proper entry into ABM operation and prevents mis-triggering, so the controller enters ABM operation only when the output power is low.

During ABM, the maximum current sense (CS) voltage is reduced to V_{CS_B} to minimize conduction loss and audible noise. The FB voltage varies in a sawtooth pattern between $V_{FB\_Bon\_ISO}$ and $V_{FB\_Boff\_ISO}$. In the event of a heavy-load jump, the controller exits ABM immediately when V_{FB} exceeds V_{FB_LB} and transitions to the maximum switching frequency and peak current limit (V_{CS_N}) to allow the output voltage to recover quickly.

3.9 Line over-voltage protection

The “CoolSET™ PWM Gen5 FF Pro” product family implements line over-voltage protection and start-up using the dual functionality of the VING pin. The current flowing into the VING pin (I_{VING}) is compared against a fixed reference I_{VING_LOVP}. When I_{VING} is greater than I_{VING_LOVP}, line overvoltage protection is triggered. To avoid any noise coupling into the VING pin, ensure that the R_{VING} ladder is placed outside the switching power loop and that no capacitor is connected from the VING pin to ground.

4 Protection features

ICE502MD provides comprehensive protection features to ensure the system is operating safely, including the following:

- Line overvoltage protection (LOVP)
- VCC overvoltage protection
- VCC undervoltage protection
- Overload protection
- Overtemperature protection for controller junction
- VCC short-to-GND protection

When these faults are detected, the system enters protection mode. Once the fault is cleared, the system resumes normal operation. The following table lists the protections and failure conditions.

Table 6 Protection behavior

Protection function	Protection trigger condition	Protection mode
Line overvoltage protection	$I_{VING} > I_{VING\_LOVP}$	Non-switch auto-restart
VCC overvoltage	$V_{VCC} > V_{VCC\_OVP}$	Extended cycle skip auto-restart
VCC undervoltage protection	$V_{VCC} < V_{VCCOFF}$	Auto-restart
Overload or open-loop protection	$V_{FB} > V_{FB\_OLP}$ and lasts for $t_{FB\_OLP\_B}$	Extended cycle skip auto-restart
Overtemperature protection	$T_J > 140°C$ (40°C hysteresis)	Non-switch auto-restart
VCC short-to-GND protection (V_{VCC} = 0 V, R_{VING} = 20 MΩ and V_{DRAIN} = 90 V)	$V_{VCC} < V_{CC\_SCP}$	Cannot start up and I_{VCC} is limited to $I_{VCC\_Charge1}$

5 Test results

5.1 Efficiency

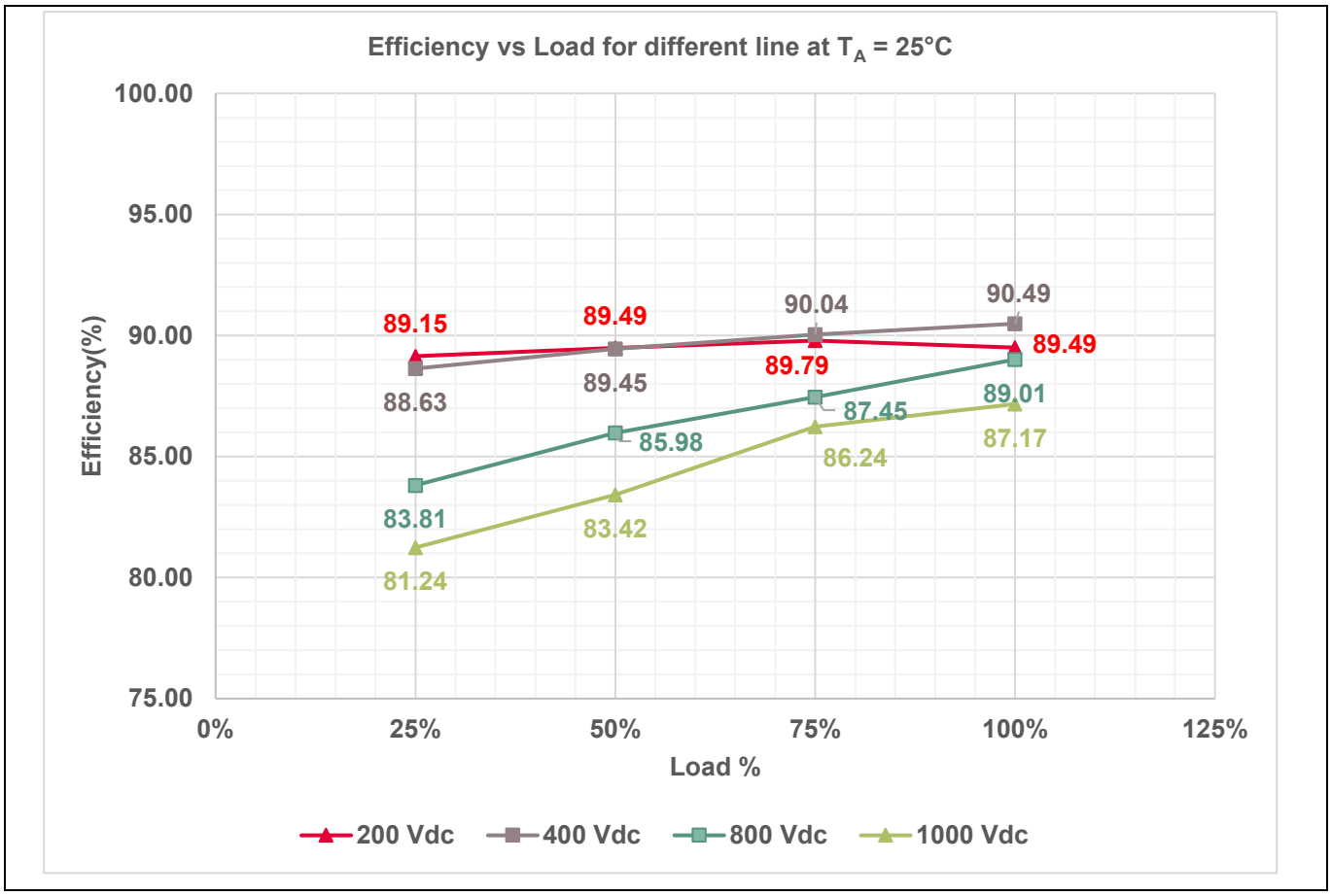


Figure 13 Efficiency vs. load for different input voltages

5.2 Line regulation

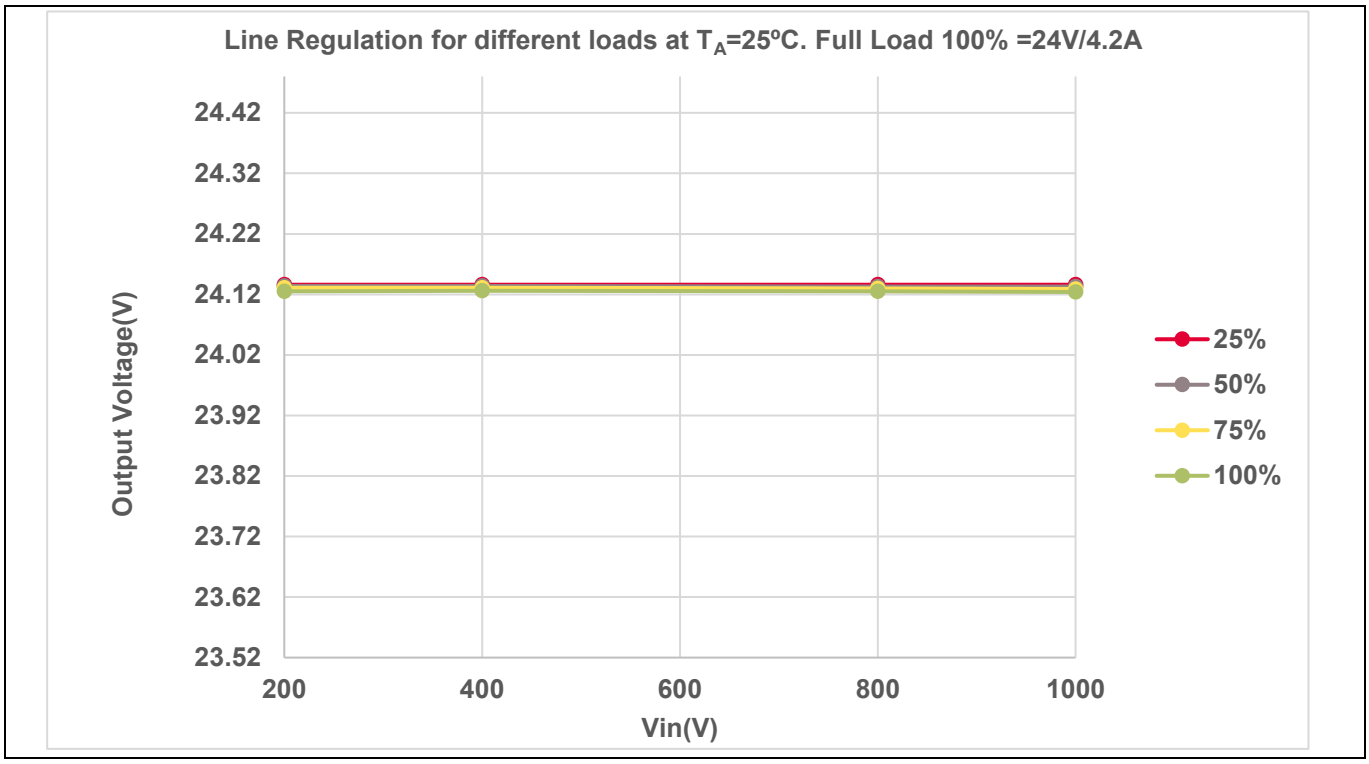


Figure 14 Line regulation for different loads

5.3 Load regulation

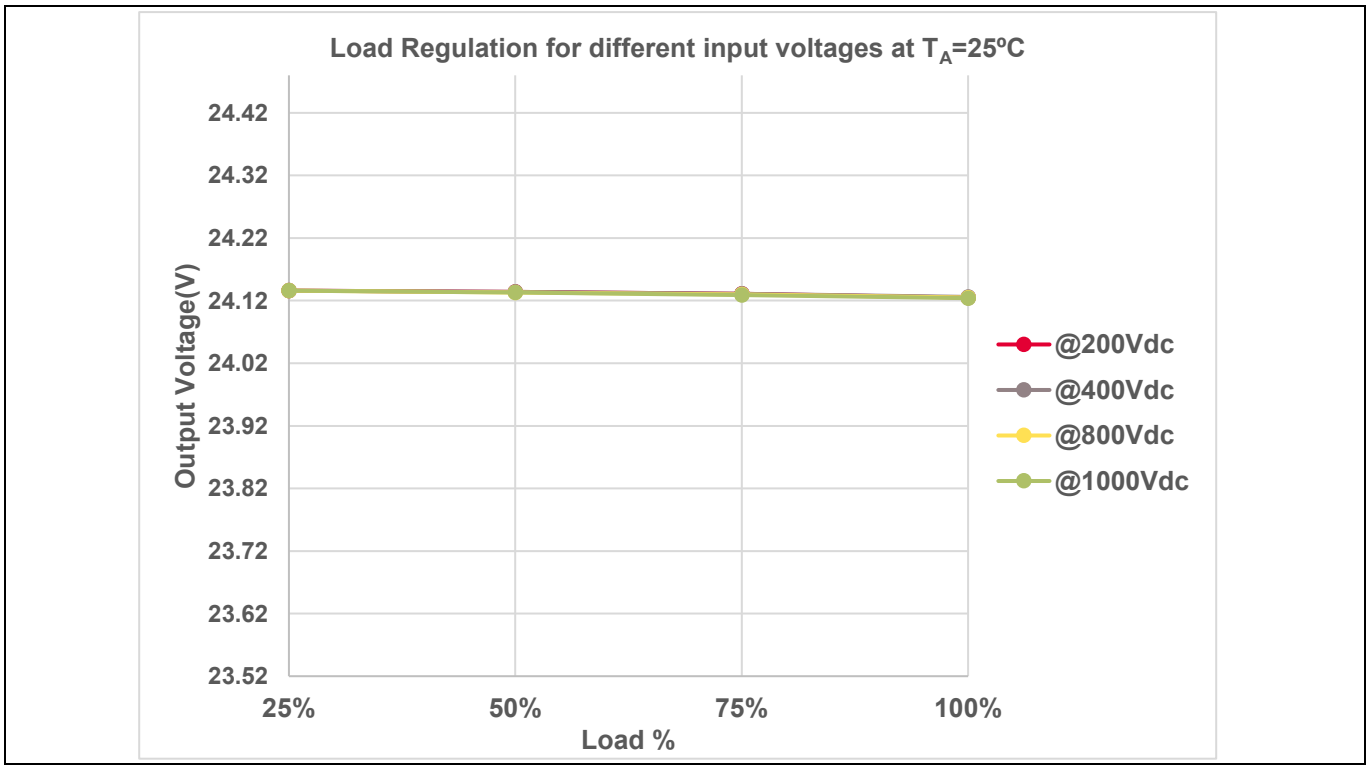


Figure 15 Load regulation for different input voltages

5.4 Thermal measurement

The thermal testing of the open-frame reference board is done using an infrared thermography camera (FLIR-T62101) at an ambient temperature of 25°C. Measurements are taken after the board has been running at full load for one hour.

Table 7 Component thermals

No.	Major component	At 200 V_{DC}/full load (°C)	At 1000 V_{DC}/full load (°C)
1	CoolSiC™ IMWH170R1K0M1 (Q1) device	40.2	78
2	CoolSiC™ device heatsink (HS1)	40.8	74.2
3	Transformer core	52.2	74
4	Transformer winding	59.6	79
5	Output diode (D8)	86.3	92
6	Diode heatsink (HS2)	81	85.2
7	ICE502MD (U1)	52	60.3
8	RCD diode (D3, D5)	66.1	78
9	TVS diode (D6)	58	68
10	Snubber resistor (R23)	70	74

Test results

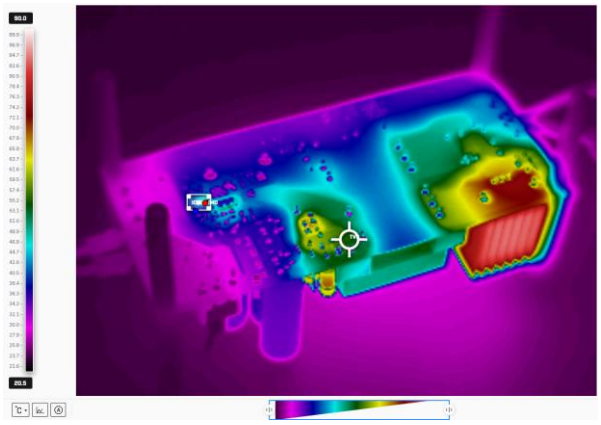
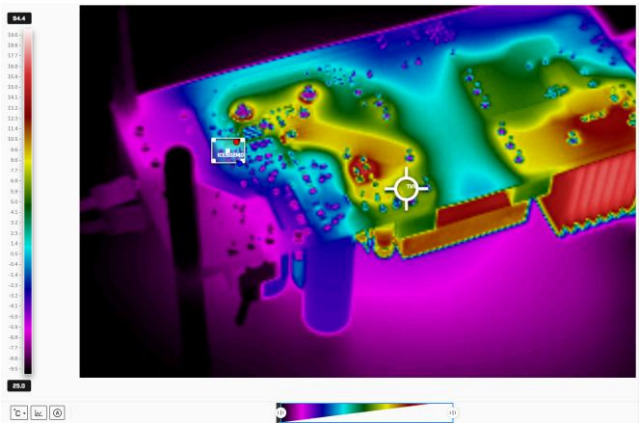
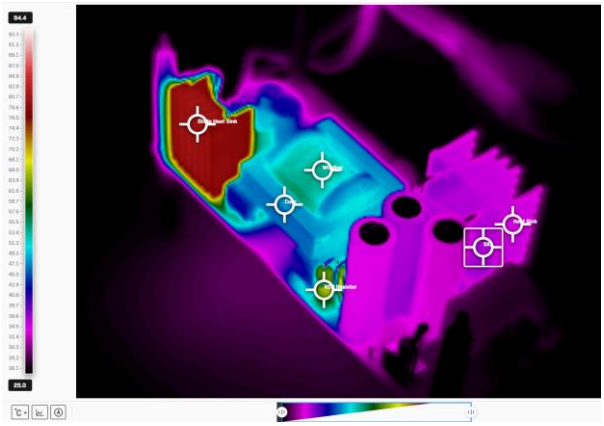
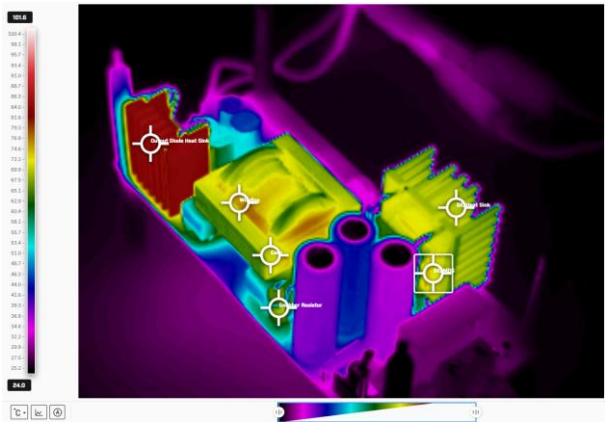
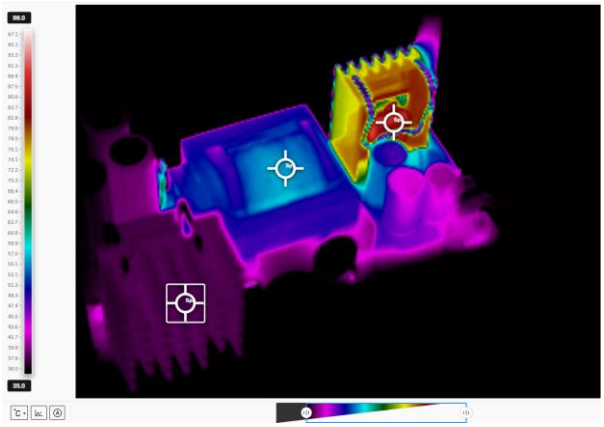
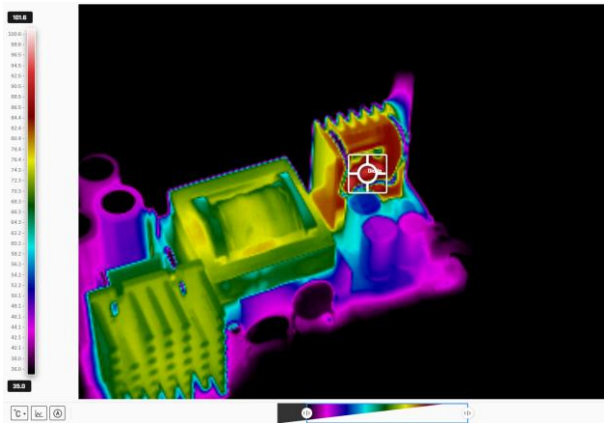
200 V_{DC} full load and 25°C ambient	1000 V_{DC} full load and 25°C ambient
 Bottom view	 Bottom view
 Top view	 Top view
 Top view	 Top view

Figure 16 Thermal images

6 Waveforms and scope plots

6.1 Startup at low/high DC line input voltage with maximum load

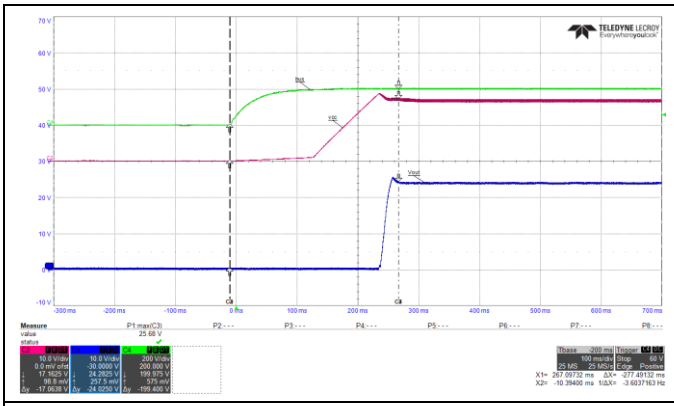
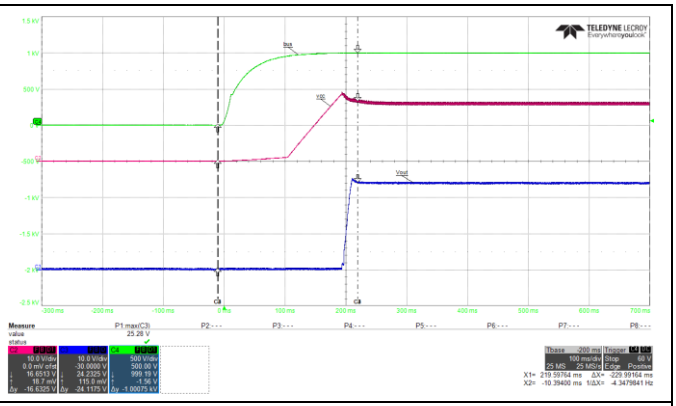
	
C2:VCC C3:24 Vout C4:DC bus	C2:VCC C3:24 Vout C4:DC bus
Startup time at 200 V_{DC} and maximum load ≈ 277 ms	Startup time at 1000 V_{DC} and maximum load ≈ 230 ms

Figure 17 Startup

6.2 Soft start

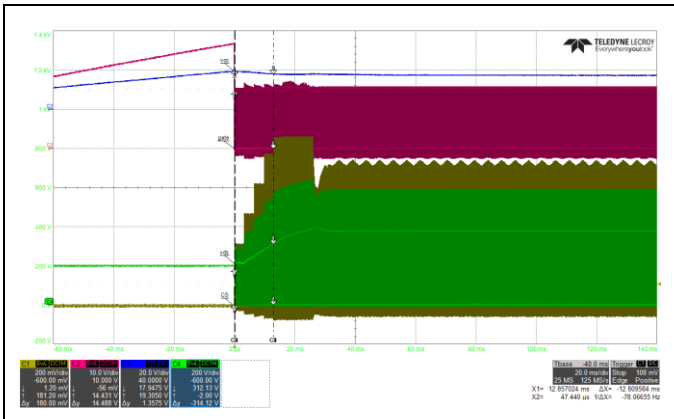
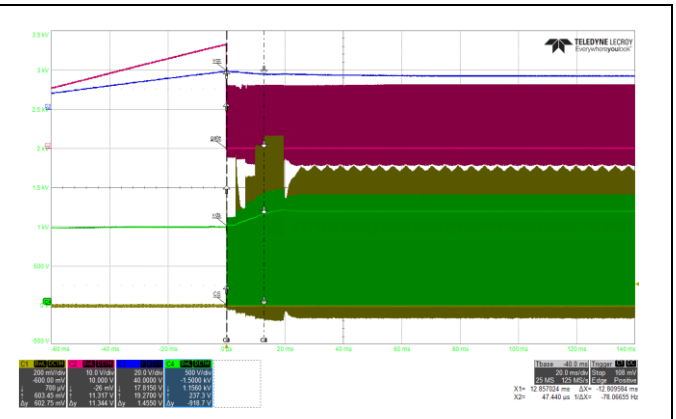
	
C1:CS C2:GATE C3:VCC C4:V_{DS}	C1:CS C2:GATE C3:VCC C4:V_{DS}
Soft-start time at 200 V_{DC} and maximum load ≈ 12 ms	Soft-start time at 1000 V_{DC} and maximum load ≈ 12 ms

Figure 18 Soft start

6.3 Steady-state switching

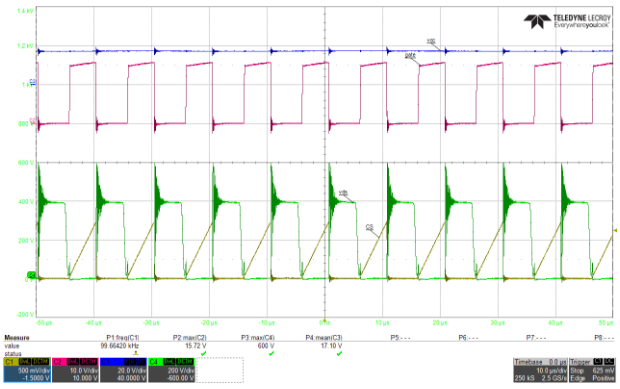
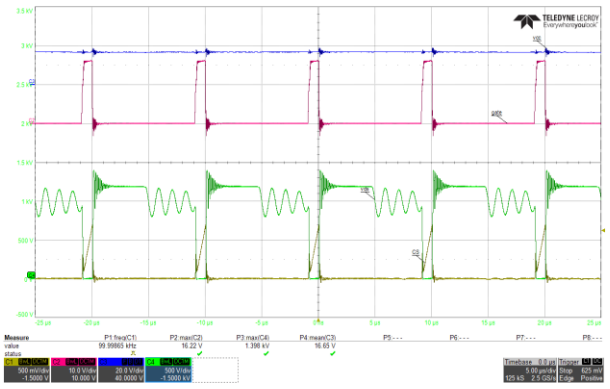
	
C1:CS C2:GATE C3:VCC C4:V_{DS}	**C1:CS C2:GATE C3:VCC C4:V_{DS}**
At 200 V_{DC}, full load	At 1000 V_{DC}, full load
Target gate voltage is set to 15 V	

Figure 19 Steady-state switching

6.4 Steady-state switching stress

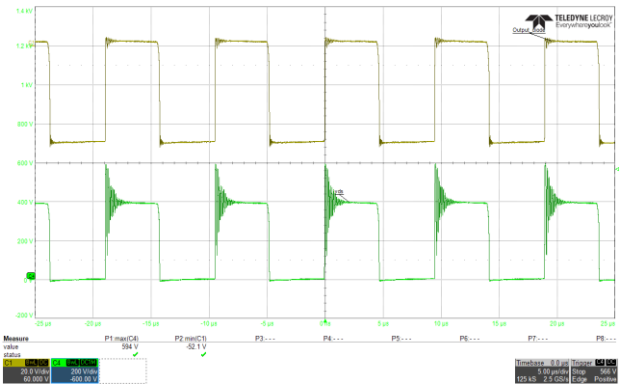
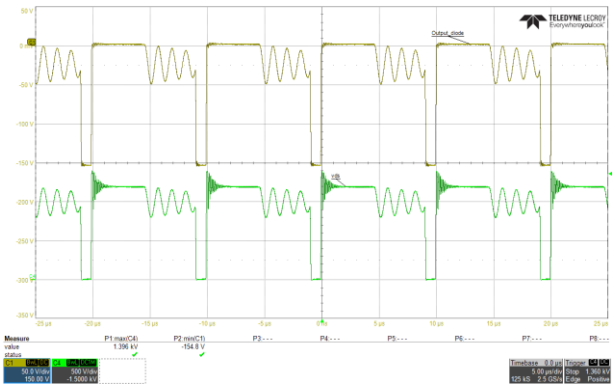
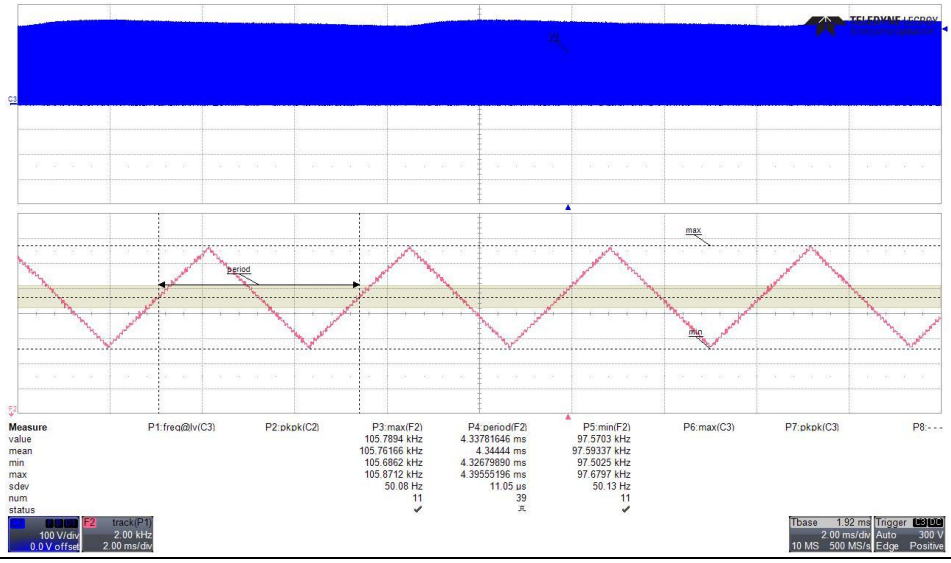
	
C1: Output diode (D8) C4:V_{DS}	**C1: Output diode (D8) C4:V_{DS}**
At 200 V_{DC}, full load	At 1000 V_{DC}, full load
V_{DS_MAX} = 594 V, PIV_{D8_MAX} = 52.1 V	V_{DS_MAX} = 1396 V, PIV_{D8_MAX} = 154.8 V

Figure 20 Steady-state switching stress

6.5 Frequency jittering

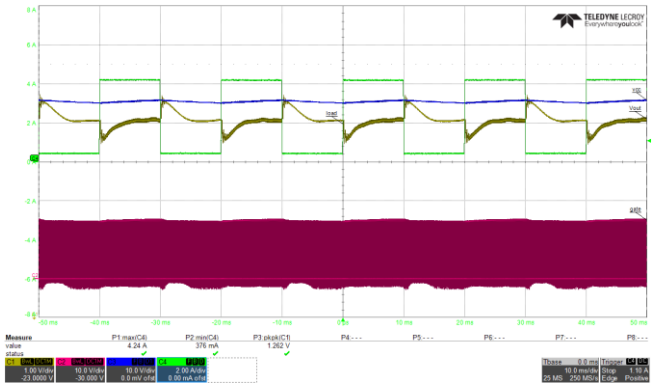


F2: Frequency trend C3:V_{DS}

Frequency jittering at 200 V_{DC} and maximum load is ≈ 97 kHz ~ 105 kHz, jitter period is ≈ 4.3 ms

Figure 21 Frequency jittering

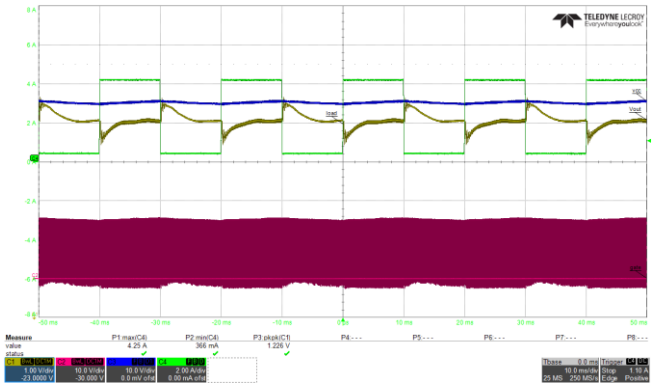
6.6 Load transient response (dynamic load from 10% to 100%)



C1:24 Vout (AC coupled) C2:GATE C3:VCC C4:Load

At 200 V_{DC}

24 V_{pk_pk} ≈ 1.26 V (5.2%)
(load change from 10% to 100%, 10 Hz, 0.4 A/µs slew rate)
Probe terminal end with a decoupling capacitor of 0.1 µF (ceramic) and 10 µF (electrolytic), along with a 20 MHz filter



C1:24 Vout (AC coupled) C2:GATE C3:VCC C4:Load

At 1000 V_{DC}

24 V_{pk_pk} ≈ 1.22 V (5.1%)
(load change from 10% to 100%, 10 Hz, 0.4 A/µs slew rate)
Probe terminal end with a decoupling capacitor of 0.1 µF (ceramic) and 10 µF (electrolytic), along with a 20 MHz filter

Figure 22 Dynamic load response

6.7 Output ripple voltage at maximum load

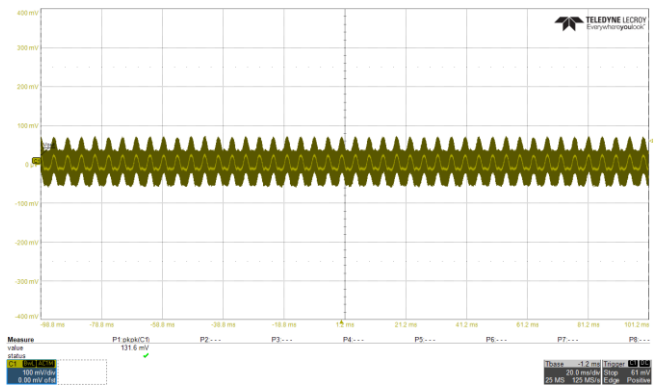
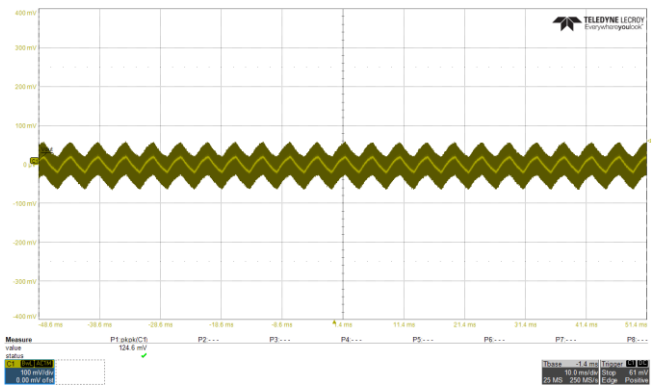
	
C1:24 Vout (AC coupled)	**C1:24 Vout (AC coupled)**
At 200 V_{DC}, full load	At 1000 V_{DC}, full load
24 $V_{ripple\_pk\_pk}$ at 200 V_{DC} ≈ 132 mV Probe terminal end with a decoupling capacitor of 0.1 µF (ceramic) and 10 µF (electrolytic), along with a 20 MHz filter	24 $V_{ripple\_pk\_pk}$ at 1000 V_{DC} ≈ 126 mV Probe terminal end with a decoupling capacitor of 0.1 µF (ceramic) and 10 µF (electrolytic), along with a 20 MHz filter

Figure 23 Output ripple at maximum load

6.8 Output ripple voltage in ABM load

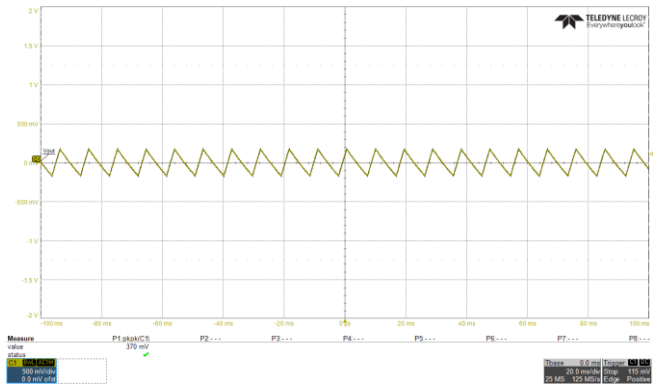
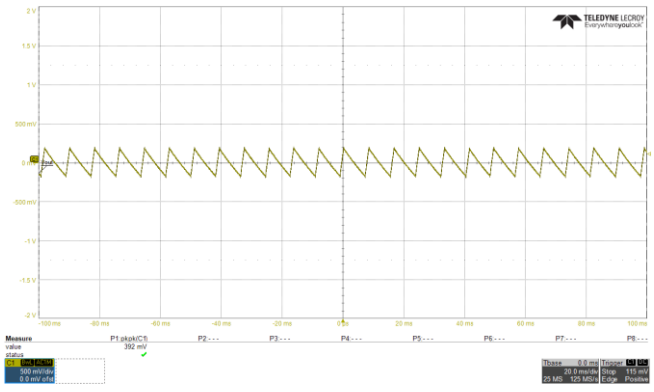
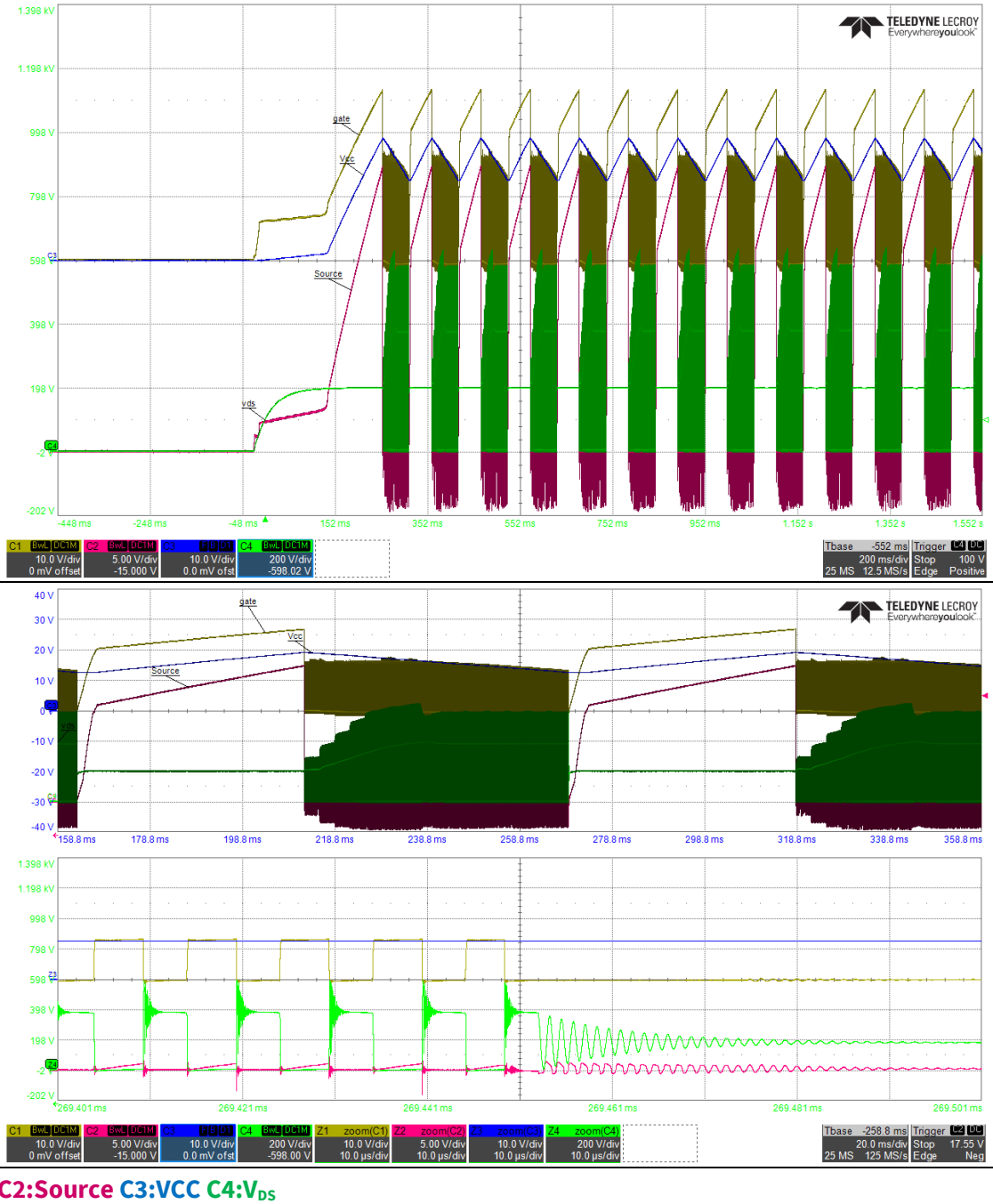
	
C1:24 Vout (AC coupled)	**C1:24 Vout (AC coupled)**
At 200 V_{DC}, 10% load	At 1000 V_{DC}, 10% load
24 $V_{ripple\_pk\_pk}$ at 200 V_{DC} ≈ 370 mV Probe terminal end with a decoupling capacitor of 0.1 µF (ceramic) and 10 µF (electrolytic), along with a 20 MHz filter	24 $V_{ripple\_pk\_pk}$ at 1000 V_{DC} ≈ 392 mV Probe terminal end with a decoupling capacitor of 0.1 µF (ceramic) and 10 µF (electrolytic), along with a 20 MHz filter

Figure 24 Output ripple at light load

6.9 VCC UVLO protection

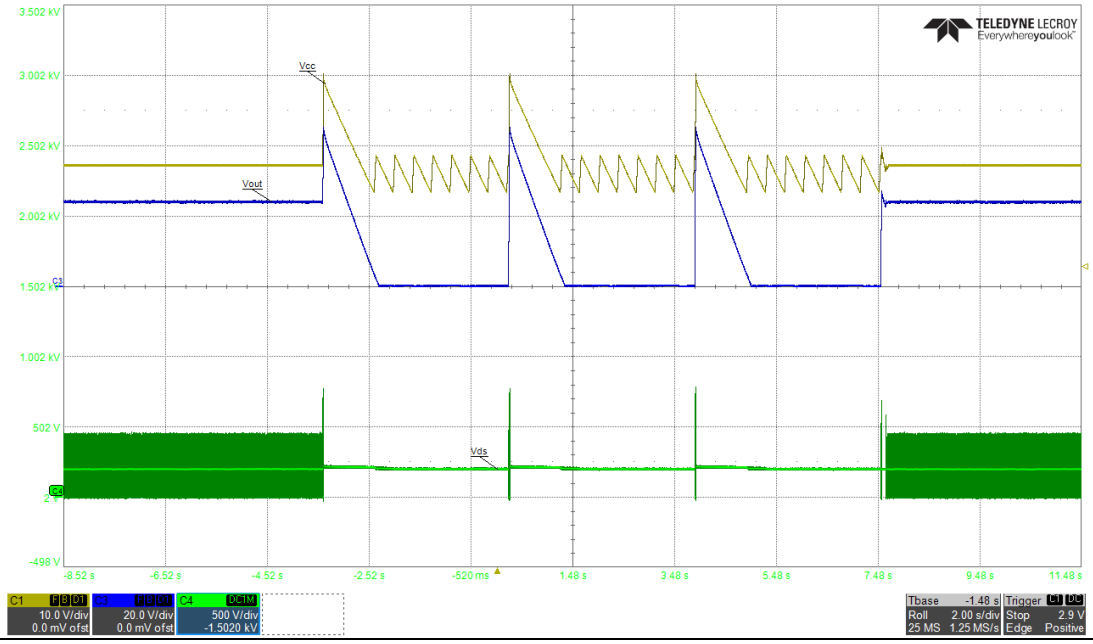


C1:Gate C2:Source C3:VCC C4:V_{DS}

Condition to enter VCC undervoltage protection (UVLO): VCC < 12.5 V
Remove R33 and power on the system at full load with 200 V_{DC}. Part enters auto-restart mode

Figure 25 VCC UVLO protection

6.10 VCC OVP protection entry and recovery



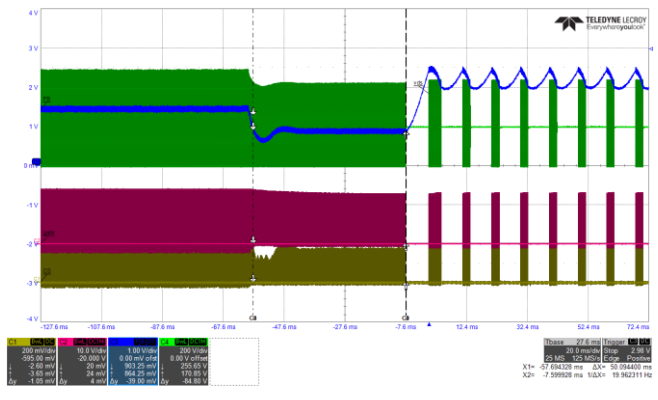
C1:VCC C3:Vout C4:V_{DS}

Condition to enter V_{VCC} overvoltage protection (OVP): V_{VCC} > 30.5 V

In the scope-shot above, short R39 while the system is operating at 200 V_{DC} and 0.5 A load. The open loop causes VCC to overshoot and reach V_{VCC} OVP threshold. The controller enters extended cycle-skip auto-restart mode. The output recovers after the fault is removed.

Figure 26 VCC OVP protection entry and recovery

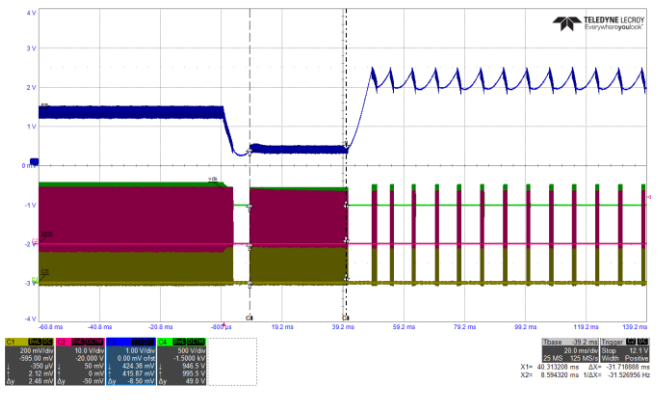
6.11 Entering active burst mode (ABM)



C1:CS C2:Gate C3:V_{FB} C4:V_{DS}

At 200 V_{DC}, 1 A to 0.1 A load

Condition to enter ABM level: V_{FB} < V_{FB_EB} and $t_{blanking}$ = t_{FB_BEB}



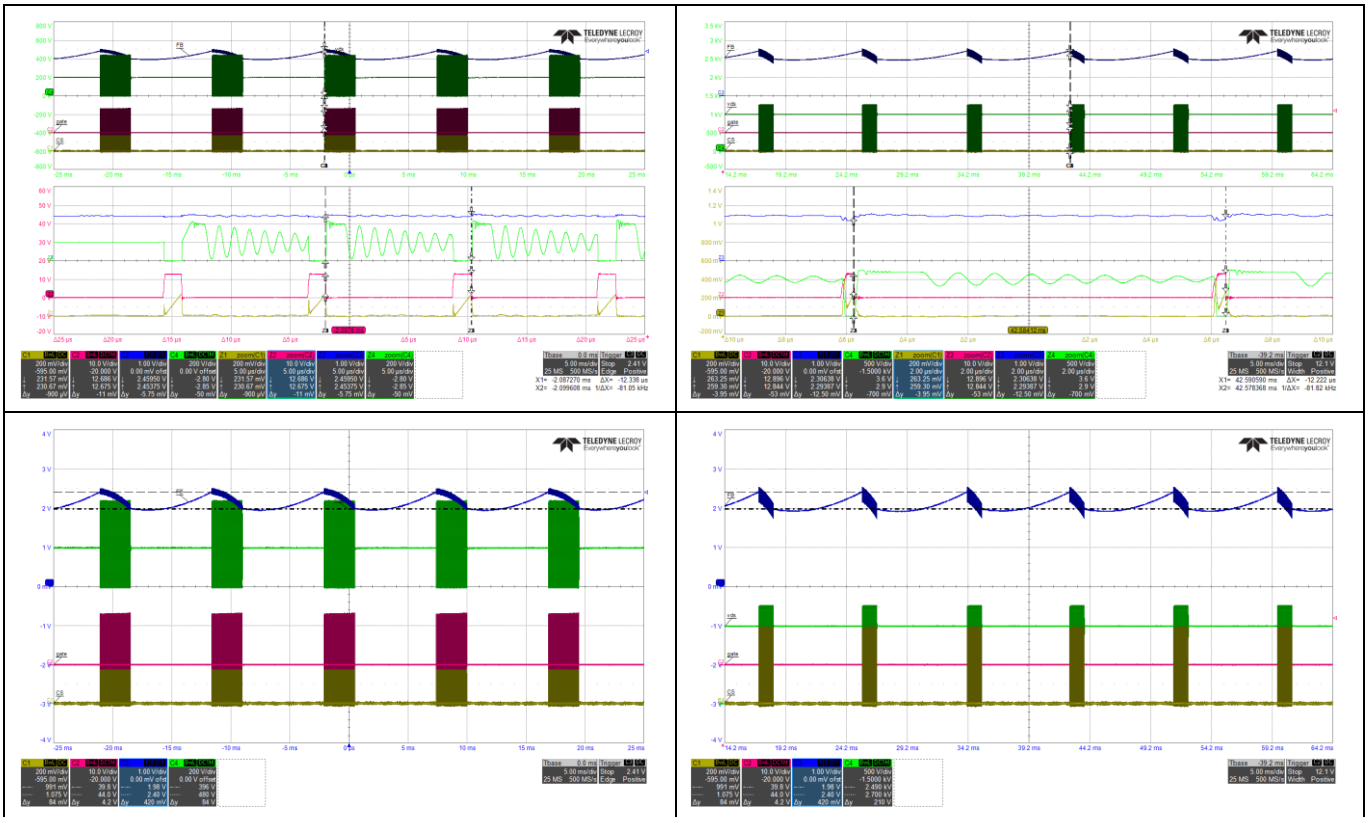
C1:CS C2:Gate C3:V_{FB} C4:V_{DS}

At 1000 V_{DC}, 1 A to 0.1 A load

Condition to enter ABM level: V_{FB} < V_{FB_EB} and $t_{blanking}$ = t_{FB_BEB}

Figure 27 Entering active burst mode (ABM)

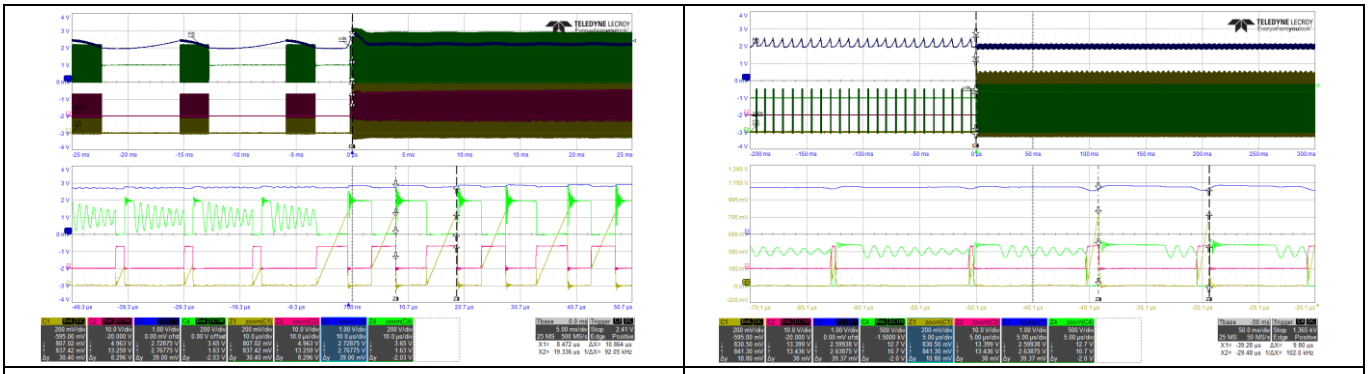
6.12 During active burst mode (ABM)



C1:CS C2:Gate C3:V_{FB} C4:V_{DS}	C1:CS C2:Gate C3:V_{FB} C4:V_{DS}
At 200 V_{DC}, 0.1 A load	At 200 V_{DC}, 0.1 A load
During ABM level: $V_{FB\_Bon\_ISO}$ = 2.35 V, $V_{FB\_BOff\_ISO}$ = 2.0 V, V_{CS_BP} = 0.22 V	During ABM level: $V_{FB\_Bon\_ISO}$ = 2.35 V, $V_{FB\_BOff\_ISO}$ = 2.0 V, V_{CS_BP} = 0.22 V

Figure 28 During active burst mode (ABM)

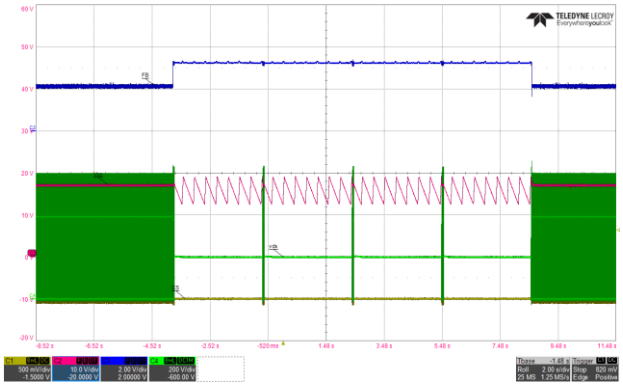
6.13 Leaving active burst mode (ABM)



C1:CS C2:Gate C3:V_{FB} C4:V_{DS}	C1:CS C2:Gate C3:V_{FB} C4:V_{DS}
Condition to leave ABM level: V_{FB} > 2.73 V (load change from 10% load to full load at 200 V_{DC})	Condition to leave ABM level: V_{FB} > 2.73 V (load change from 10% load to full load at 1000 V_{DC})

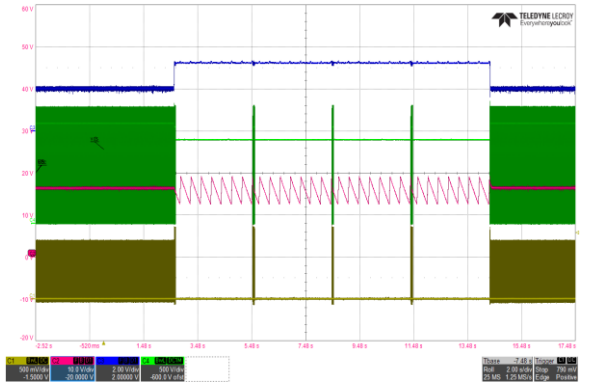
Figure 29 Leaving active burst mode (ABM)

6.14 Over-load protection entry and recovery



C1:CS C2:VCC C3:V_{FB} C4:V_{DS}

Output short-circuit at 200 V_{DC} full load, and recovery. $t_{blanking}$ = 59.6 ms. The controller enters extended cycle-skip auto-restart protection

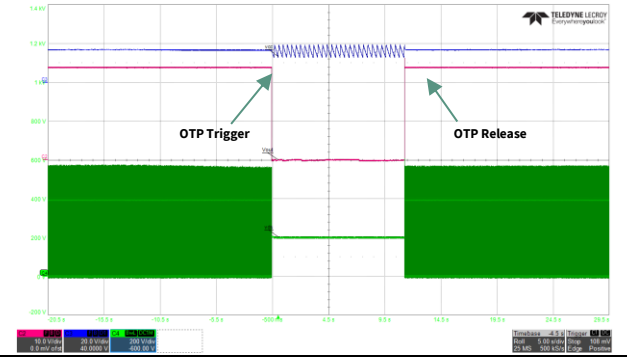


C1:CS C2:VCC C3:V_{FB} C4:V_{DS}

Output short-circuit at 1000 V_{DC}, full load and recovery. $t_{blanking}$ = 59.6 ms. The controller enters extended cycle-skip auto-restart protection

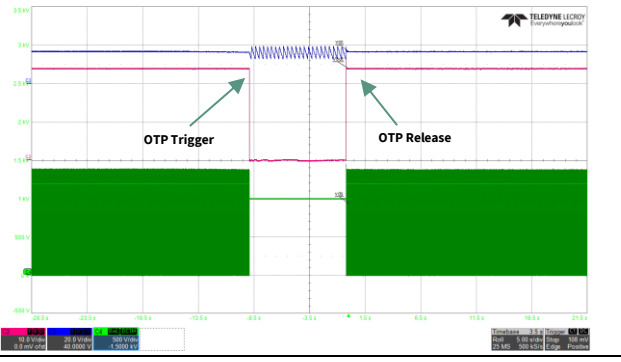
Figure 30 Over-load protection entry and recovery

6.15 Over-temperature protection entry and recovery



C2:Vout C3:VCC C4:V_{DS}

Vin = 200 V_{DC}, full load. Overtemperature protection tested by using hot air gun to heat the controller

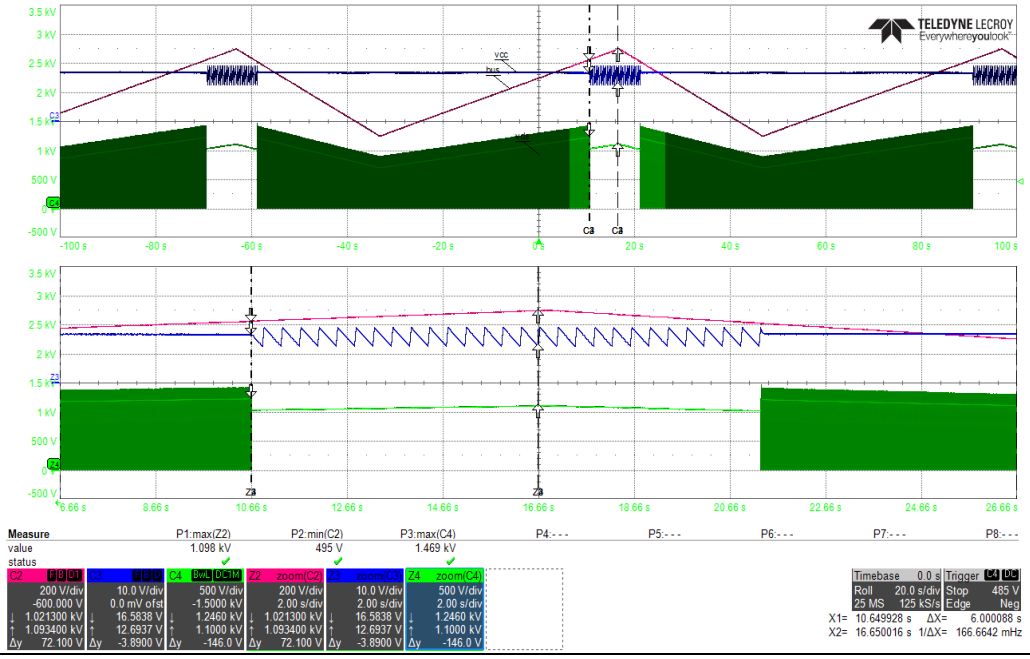


C2:Vout C3:VCC C4:V_{DS}

Vin = 1000 V_{DC}, full load. Over temperature protection tested by using hot air gun to heat the controller

Figure 31 Over-temperature protection entry and recovery

6.16 Line overvoltage protection entry and recovery



C2:DC Bus C3:VCC C4:V_{DS}

Tested with full load. Perform line sweep-up and sweep-down from 500 V_{DC} to 1100 V_{DC}. Line OVP triggers at 1020 V_{DC} and recovers at 1010 V_{DC}

Figure 32 Line overvoltage protection entry and recovery

7 Related resources

Developer community

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Technical support

Have technical queries? Consult experts from Infineon to get a fast turn-around by raising a request on the Technical Support page or a local sales representative.

References

[1] Infineon Technologies AG: *CoolSET™ PWM FF Gen5 Pro datasheet*; Available upon request

[2] Infineon Technologies AG: *CoolSET™ PWM FF Gen5 Pro flyback design guide*; Available upon request

[3] Infineon Technologies AG: *CoolSET™ PWM FF Gen5 Pro calculation tool for flyback*; Available upon request

Revision history

Document revision	Date	Description of changes
1.0	2025-12-15	Initial release

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Published by

Infineon Technologies AG

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