Dual output 60 W power supply using CoolSET™ SiP ICE186EM

REF_60WD1_ZVS_186EM

About this document

Scope and purpose

This application note describes a dual output 60 W power supply using Infineon's latest CoolSET™ System in Package (SiP) ICE186EM. The power supply is designed with a universal AC input line and two outputs (isolated +12 V/2.5 A and +24 V/1.25 A) with an optional non-isolated +15 V/0.15 A output.

Intended audience

This document is intended for power supply design, application engineers, or others who want to design efficient and reliable auxiliary power supplies.

Keypoints

- Overall high efficiency to meet energy efficiency requirements
- Simplified circuitry with high-level integration of power control and protection features
- Auto-restart protection scheme to minimize interruption to enhance end user experience
- Secondary controlled primary LDO circuit to reduce component counts
- Zero-voltage switching (ZVS) technology to boost efficiency performance

About this product family

Product family

Infineon's CoolSET™ AC-DC integrated power stages in fixed frequency and quasi-resonant switching schemes offer increased robustness and outstanding performance. This family offers superior energy efficiency, comprehensive protective features, and reduced system costs and is ideally suited for auxiliary power supply applications.

Target applications

- SMPS
- Home appliances
- Server
- Telecom

Table of contents

1 Introduction

This document describes a 12 V/2.5 A and 24 V/1.25 A power supply using Infineon's latest CoolSET™ SiP ICE186EM. This reference design demonstrates high efficiency and cost-effectiveness, made possible by the high-level integration capabilities of CoolSET™ SiP.

Table 1 lists the general system requirement for a power supply, and the corresponding Infineon solution by ICE186EM.

Table 1 General system requirement and reference design solution

S.No.	General system requirement	Reference design solution – ICE186EM
1	High efficiency to meet energy efficiency requirements	Primary zero-voltage switching and secondary optimal synchronous rectifier control
2	Simplified circuitry with high-level integration	Primary 800 V MOSFET, primary and secondary controllers, and communication integrated in a DSO-27 package
3	Minimize interruption to enhance end user experience	All protections are defined to enter auto-restart mode

Either 12 V and 24 V output can support to power the system hardware such as motor drives, fans, and compressors. Additionally, an optional non-isolated 15 V output obtained through the LDO at the primary side can be populated on the board to supply gate drive circuits. A unique feature of this reference board is its ability to switch the primary side LDO on or off via the secondary side ENS signal at any time according to the system requirement. This approach offers several benefits, including:

- Reduced circuit and component count
- Retain PCB space
- Lower system standby power consumption

By eliminating the need for extra isolation components, the reference board results in a more efficient, compact, and cost-effective solution for system designers.

2 Reference board

This document provides complete design details including power supply specifications, schematics, bill of materials, PCB layout, transformer specification, and performance data.

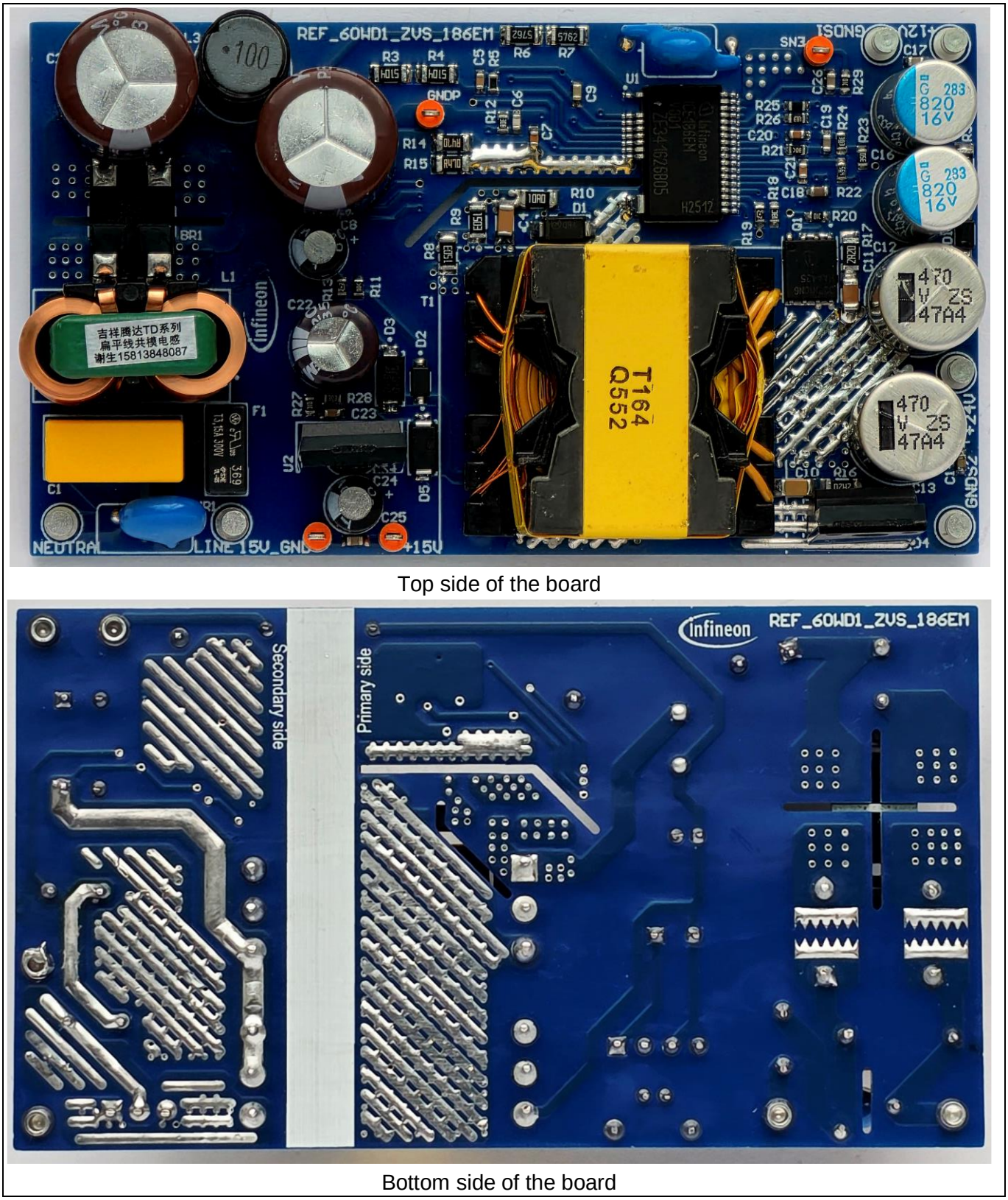


Figure 1 Reference board REF_60WD1_ZVS_186EM

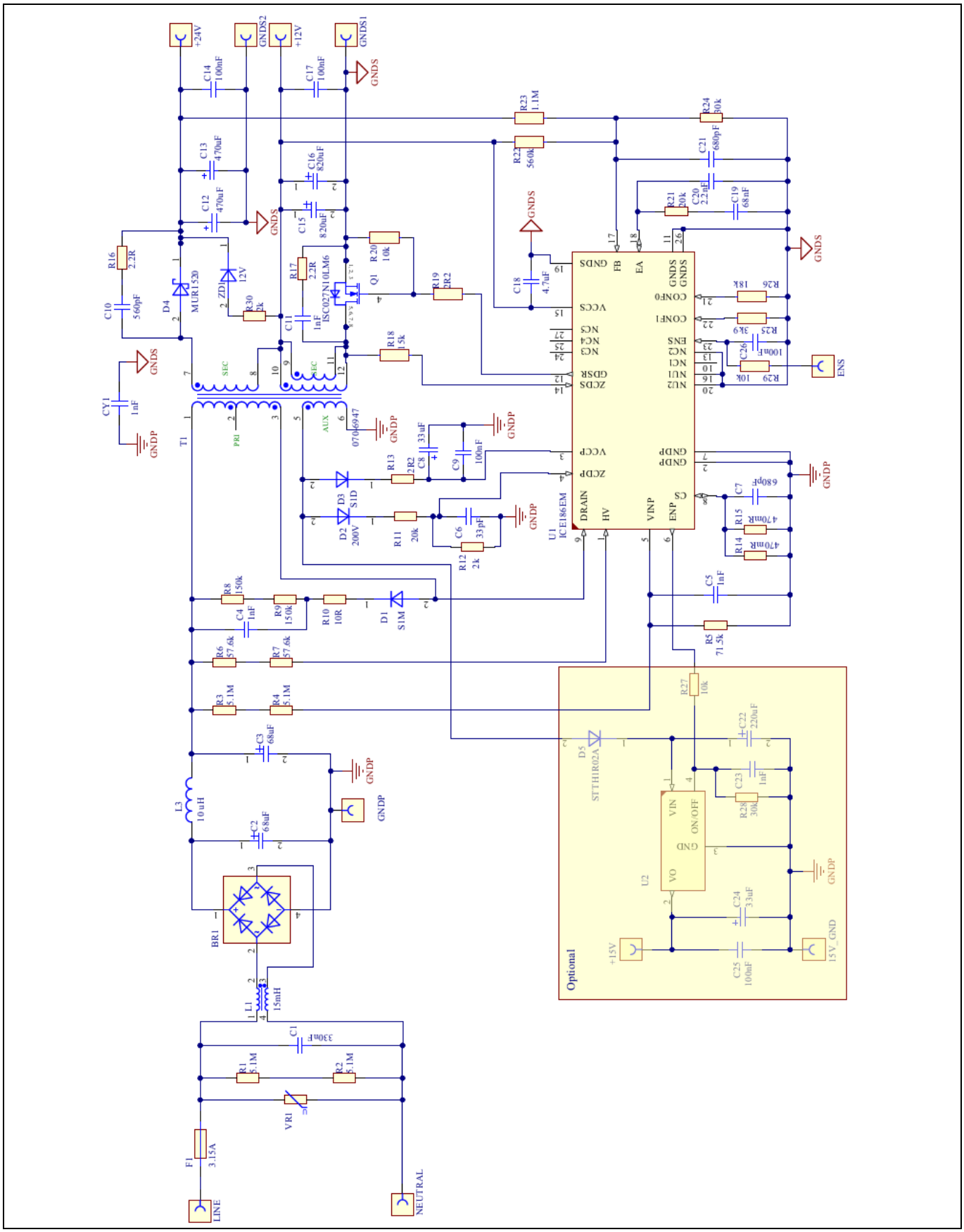
3 Power supply specifications

The following table represents the minimum acceptance performance of the design. The actual performance is listed in the Measurement data and graphs section.

Table 2 Specifications of REF_60WD1_ZVS_186EM

Description	Symbol	Min.	Typ.	Max.	Units	Comments
Input						
Voltage	V_{IN}	90	115/230	264	V AC	Two wires (no P.E.)
Frequency	f_{LINE}	47	60/50	64	Hz	–
Line overvoltage	V_{IN_OVP}	–	284	–	V AC	–
Output						
Output voltage 1	V_{OUT1}	–	12	–	V	±3 percent
Output current 1	I_{OUT1}	–	–	2.5	A	Continuous
Output voltage ripple 1	$V_{RIPPLE1}$	–	–	360	mV	Peak to peak
Output voltage 2	V_{OUT2}	–	24	–	V	±3 percent
Output current 2	I_{OUT2}	–	–	1.25	A	Continuous
Output voltage ripple 2	$V_{RIPPLE2}$	–	–	720	mV	Peak to peak
Overcurrent protection (12 V)	I_{OCP}	–	–	5.5	A	Full load at 24 V
Total output power	P_{OUT}	–	–	60	W	Continuous
Efficiency						
Maximum load efficiency	η	93	–	–	%	Measured at 230 V AC
Environmental						
Conducted EMI	–	6			dB	Margin, CISPR 22 class B
ESD	EN 61000-4-2					
Contact discharge	–	±8			kV	–
Air discharge	–	±15			kV	–
Surge immunity	EN 61000-4-5					
Differential mode	–	±2			kV	–
Common mode	–	±4			kV	–
PCB size	–	90×50×30			mm^2	L × W ×H
Ambient temperature	Ta	–	–	50	°C	Convection cooling

4 Circuit diagram



REF_60WD1_ZVS_186EM

Circuit diagram

Figure 2 Schematic of REF_60WD1_ZVS_186EM

5 Circuit description

This section briefly describes the reference design circuit by different functional blocks. For more information on design procedure and component selection for the flyback circuitry, see the design guide [1] and
IC datasheet [2].

5.1 EMI filtering and line rectification

- The input of the power supply is taken from the AC power grid, which is in the 90 V AC ~ 264 V AC range
- The F1 fuse is right at the entrance to protect the system in case of excess current entering the system circuit due to a fault
- Following is the varistor VR1, which is connected across L and N to absorb the line surge transient
- Common mode (CM) choke L1 and the X-capacitor C1 form a basic filter to reduce the EMI noise
- The bridge rectifier BR1 rectifies the AC input into DC voltage, filtered by the π filter (capacitor C2, C3, and L3)

5.2 CoolSET™ SiP power stage

The flyback converter power stage consists of:

- Power transformer
- Primary power MOSFET
- Secondary synchronous rectifier (SR) MOSFET
- Secondary output capacitors
- Filtering component if necessary

The primary side and secondary side power management are separated for isolated power supply domains (VCCP, GNDP and VCCS, GNDS). CoolSET™ SiP ICE186EM provides reinforced and safe isolated communication between primary and secondary side.

5.2.1 CoolSET™ SiP primary side

CoolSET™ SiP ICE186EM integrates a 950 V startup cell at the primary side, IC is self-starting through the startup resistors (R6 and R7) in series with this startup cell to charge the VCCP pin capacitor (C8) when AC is applied. These startup resistors (R6 and R7), together with ZCDP pin external configuration resistor R_{ZCDPL} (R12), determine brownin and brownout protections, as shown in Table 3.

Table 3 Primary side configuration options

Option	$R_{ZCDPL(min)}$; $R_{ZCDPL(max)}$	Brownin current threshold I_{HV_BI}	Brownout current threshold I_{HV_BO}	Internal shunt resistor $R_{HVshunt}$
1	[1.00 kΩ ; 1.05 kΩ]	2.00 mA	1.40 mA	0.5 kΩ
2	[1.87 kΩ ; 2.70 kΩ]	1.00 mA	0.70 mA	1.0 kΩ
3	[4.30 kΩ ; 5.00 kΩ]	0.67 mA	0.47 mA	1.5 kΩ
4	[9.20 kΩ ; 9.50 kΩ]	0.50 mA	0.35 mA	2.0 kΩ

Select option 2 with R_{ZCDPL} (R12) = 2 kΩ, then the brownin voltage can be estimated as:

Circuit description

$$V_{BI} = (R_{HV} + R_{HVshunt}) \times I_{HV\_BI} = (115\ \text{k}\Omega + 1\ \text{k}\Omega) \times 1mA = 116\ V$$

Equation 1

and the brownout voltage can be estimated as:

$$V_{BO} = (R_{HV} + R_{HVshunt}) \times I_{HV\_BO} = (115\ \text{k}\Omega + 1\ \text{k}\Omega) \times 0.7mA = 81\ V$$

Equation 2

Moreover, R11 and R12 resistors offer zero crossing detection during the soft-start period and primary-sensed output overvoltage protection at V_{OUT1}.

$$V_{OUT1\_OVP} = \left(\frac{(R_{ZCDPH} + R_{ZCDPL}) \times V_{ZCDP\_OVP\_min}}{R_{ZCDPL}} + V_{Daux)}\right) \times \frac{N_{SEC}}{N_{AUX}} - V_{Dsec}$$
$$= \left(\frac{(2\ k\Omega + 20\ k\Omega) \times 2.05V}{2\ k\Omega} + 0.3V\right) \times \frac{4}{7} - 0.1V \approx 13V$$

Equation 3

Where,

- N_{MAIN} : Number of primary turns
- N_{SEC} : Number of secondary turns
- N_{AUX}: Number of auxiliary turns
- V_{Daux} : Diode forward voltage drop at auxiliary winding
- V_{Dsec} : Voltage drop across SR MOSFET
- $V_{ZCDP\_OVP\_min}$: Minimum voltage of the output overvoltage threshold
- V_{OUT_OVP} : User-defined output overvoltage level

C6 is chosen to adjust the delay time, which starts when the drain-source voltage falls below the bus voltage until the ZCDP voltage falls to $V_{ZCDPthr}$ (typical 100 mV). Therefore, the power switch can be turned on at the valley point of the drain-source voltage. This is normally done through experimentation.

A 33 µF capacitor for C11 is applied to ensure stable system operation and enough break time for auto-restart protection. The VCCP resistor R13 is placed as noise attenuation in case of severe voltage spike coupling from transformer during surge test.

The AC line overvoltage protection is detected by sensing the bus capacitor voltage through the V_{INP} pin via the divider resistors R3, R4, and R5. Once the V_{INP} pin voltage is higher than the line overvoltage threshold V_{VINP_LOVP}, the controller enters the line overvoltage protection and releases the protection mode after the V_{INP} pin voltage is lower than V_{VINP_LOVP}.

Estimated LOVP voltage is calculated:

$$V_{BUS\_OVP} = V_{VINP\_LOVP} \times \frac{R8+R6+R7}{R8} = 2.80\ V \times \frac{71.5\ k\Omega+5100\ k\Omega+5100\ k\Omega}{71.5\ k\Omega} = 402\ V$$

Equation 4

A low-cost RCD clamp consisting of the D1 diode, R8, R9, and R10 resistors and C4 capacitor is implemented to suppress the peak drain voltage when turning off the power switch inside U1. This passive snubber helps dissipate the energy stored in the transformer leakage inductance.

5.2.2 CoolSET™ SiP secondary side

The secondary side of CoolSET™ SiP ICE186EM starts to take over the PWM control when output voltage reaches 95% of its regulation target. The ICE186EM PWM control is based on sensing the reflected voltage from the primary side via the ZCDS pin and the error amplifier output EA voltage. ICE186EM-integrated PWM and SR control ensures the timing of the SR power switch (Q2) and the primary side power switch is well-synchronized, which avoids the cross conduction of the two switches and provides reliable synchronous rectification. In addition, the current injection function via the SR power switch Q2 enables zero-voltage switching operation on the primary side.

R26 is connected to CONF0 and serves as R_{SET0}. The value of R26 is determined by the transformer turns ratio, which is a critical parameter in the design. According to Table 4, the transformer turns ratio is specified as 8. Based on this value, R26 is set as 18 kΩ.

Table 4 Resistance for R_{SET0}

Turns ratio N_{MAIN} / N_{SEC}	R_{SET0}
5	3.9 kΩ
6	6.8 kΩ
7	12.0 kΩ
8	18.0 kΩ
9	27.0 kΩ
10	39.0 kΩ

R25 is connected to CONF1 and serves as R_{SET1}, which is to preset the operation-relevant parameters. Default selection is option 1 in Table 5, R25 is set as 3.9 kΩ. There are four parameters that can be adjusted via R_{SET1} to optimize hysteretic mode performance.

By selecting different V_{EA_EHM} values, you can tune the power level of hysteretic mode; higher V_{EA_EHM} values enable higher hysteretic power. In hysteretic mode, precise control over the pulse width and timing is crucial for achieving optimal standby power. The pulse width is determined by the $V_{EA\_PWM\_HM}$ value, while the pulse starting and ending points are controlled by V_{EA_HMon} and V_{EA_HMoff}. By carefully adjusting these values, the hysteretic power can be fine-tuned to achieve the lowest standby power consumption.

Table 5 Resistance for R_{SET1}

Option	1	2	3	4	5	6
R_{SET1}	3.9 kΩ	6.8 kΩ	12.0 kΩ	18.0 kΩ	27.0 kΩ	39.0 kΩ
EA voltage threshold for entering hysteretic mode (V_{EA_EHM})	0.586 V	0.586 V	0.605 V	0.605 V	0.624 V	0.624 V
EA voltage for pulses during hysteretic mode ($V_{EA\_PWM\_HM}$)	800 mV	900 mV	900 mV	800 mV	900 mV	800 mV
EA voltage hysteretic mode on threshold (V_{EA_HMon})	1.2 V	1.2 V	1.2 V	1.25 V	1.2 V	1.25 V
EA voltage hysteretic mode off threshold (V_{EA_HMoff})	0.9 V	0.9 V	0.9 V	0.8 V	0.9 V	0.8 V

- Resistor ladder R22, R23, and R24 with a high frequency filter capacitor C21 connected to FB pin determines the output voltage
- R22 connected to 12 V output and R23 connected to 24 V output is designed to sense both outputs
- Zener diode ZD1 in series with resistor R30 prevents 24 V output from increasing too high during dynamic loading or worst cross regulation condition

A compensation network connected to EA pin consisting of C19, C20, and R21 is implemented to stabilize the output voltage regulation. This network is carefully designed to ensure that the power supply's output voltage remains stable and within the desired range. For a detailed understanding of the compensation network's calculation, see the design guide [1]. This resource provides a comprehensive explanation of the calculations.

To minimize ripple voltage, the choice of output capacitors is crucial. For C12, C13, C15, and C16, low equivalent series resistance (ESR) type capacitors are recommended. In addition, capacitors C14 and C17 are added to suppress high frequency noise.

5.3 Enable output signal

In this design, the ENP pin on the primary side is connected to the enable pin of a low dropout regulator (LDO). This connection allows the ENP pin to be fully controlled by the ENS signal from the secondary side, shown in Figure 3.

This approach offers two significant benefits:

- Eliminates the need for isolated circuitry to transfer the signal from the secondary side to the primary side, simplifying the overall design and reducing component count
- Enables the LDO output to be disabled when not required, resulting in a significant reduction in standby power loss

A straightforward relationship exists between the two signals:

- ENP logic = 1 when ENS logic = 1
- ENP logic = 0 when ENS logic = 0

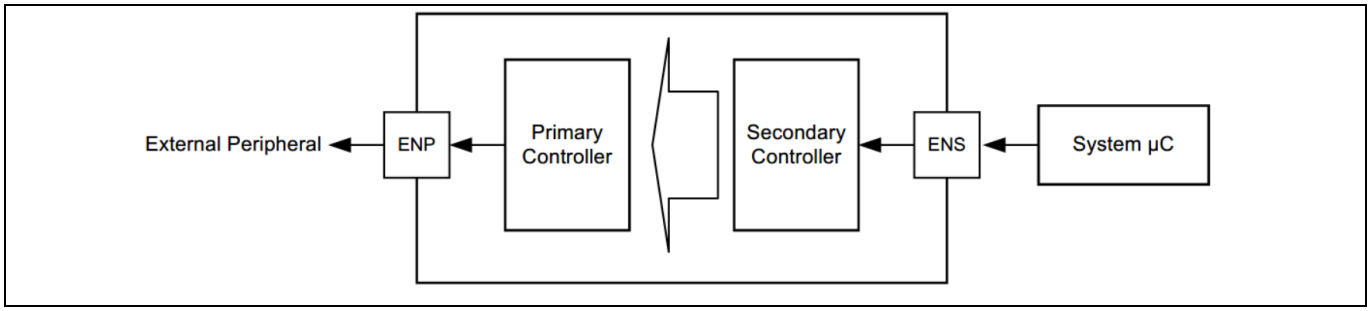


Figure 3 Enable output signal

6 PCB layout

60 W PCB layout are shown in the following figures.

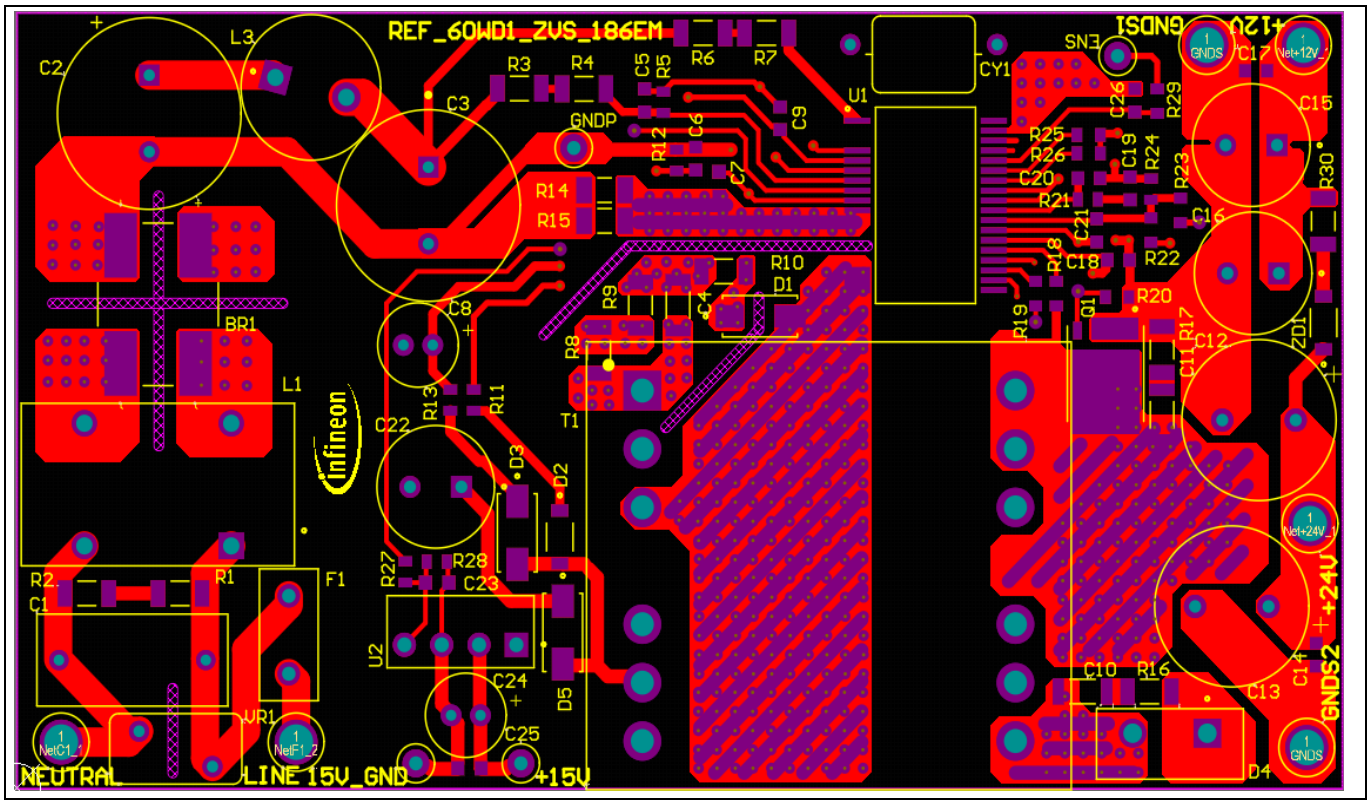


Figure 4 Top-side PCB

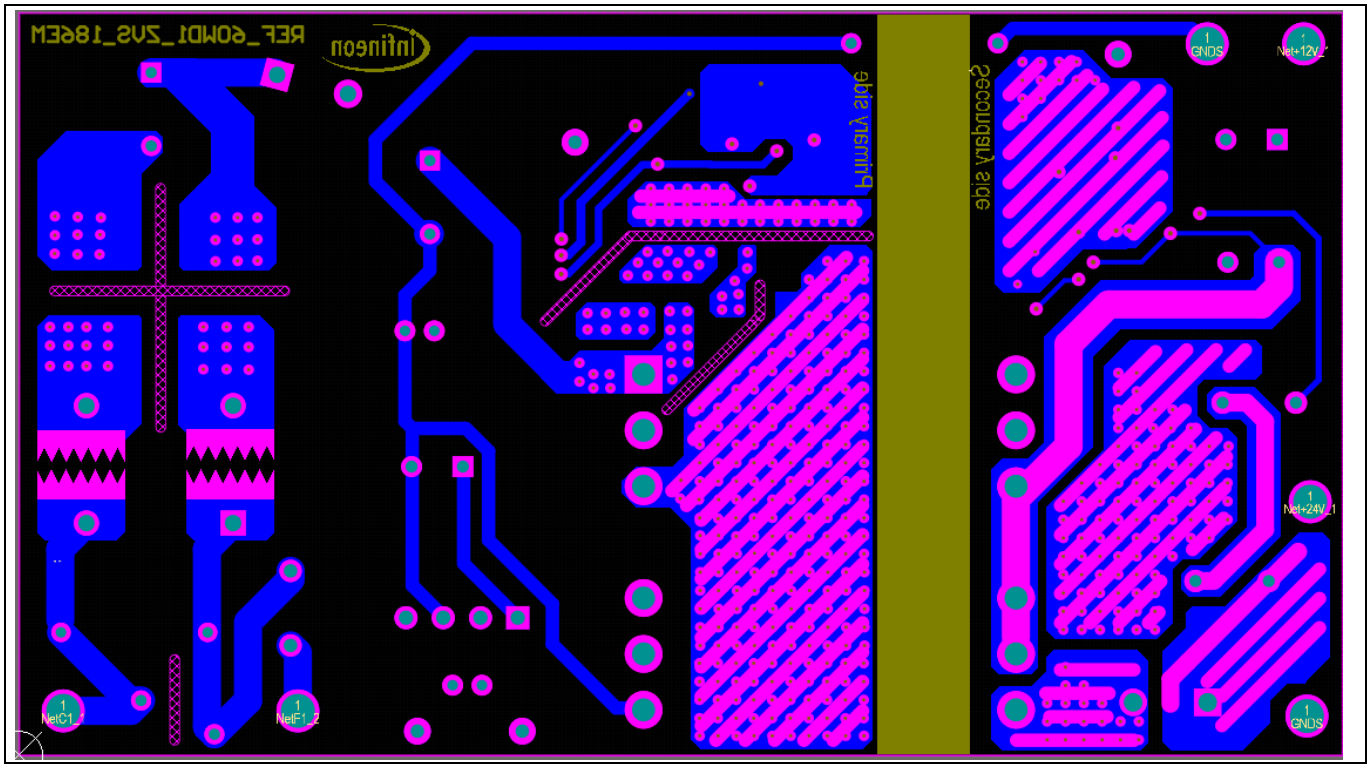


Figure 5 Bottom-side PCB

PCB layout

PCB layout is crucial to a successful design. Following are some recommendations:

1. Minimize the loop with pulse shape current or voltage, such as the loop formed by the bus voltage source, primary winding, main power switch and current sense resistor or the loop consisting of the secondary winding, output diode and output capacitor, or the loop of the V_{CC} power supply
2. **Star the ground at the bulk capacitor**: All primary grounds should be connected to the ground of the bulk capacitor separately at one point. This can reduce the switching noise entering the sensitive pins of the CoolSET™ SiP device. The primary star ground can be split into several groups:
   - Combine signal (all small signal grounds connecting to the controller GNDP pin such as the filter capacitors C5, C6, and C7) and power ground (current sense resistor R14 and R15)
   - V_{VCCP} ground includes the VCCP capacitor C8 ground and the auxiliary winding ground, pin 6 of the power transformer
   - EMI return ground includes the Y capacitor for isolated flyback application
   - DC ground from the bridge rectifier BR1
   - CoolSET™ SiP primary side GNDP pin 2 and pin 7 are recommended to jointly connected to a PCB copper plate, and then star connected to Bulk Cap Ground
3. CoolSET™ SiP secondary side GNDS pin 11, pin 19, and pin 26 are recommended to jointly connected to a PCB copper plate, and then star connected to SR MOSFET source pin
4. Place the filter capacitor (C9 and C18) close to the controller ground (GNDP and GNDS) to reduce the switching noise coupled into the controller
5. **High voltage (HV) trace clearance**: HV traces like startup and drain traces should maintain sufficient spacing to the nearby traces to avoid arcing
6. Keep a minimum of 232 mm^2 copper area at both the primary drain pin and secondary GNDS for good thermal performance of the CoolSET™ SiP

7 Bill of materials

Table 6 BOM

S.No.	Designator	Description	Manufacturer	Part number	Qty.
1	+12V, +24V, GNDS1, GNDS2, LINE, NEUTRAL	–	1502-2	Keystone Electronics Corp.	6
2	+15V, 15V_GND, ENS, GNDP	–	5003	Keystone Electronics Corp.	4
3	BR1	BRIDGE RECT 1PHASE 600 V 4 A	Z4DGP406L-HF	Comchip Technology	1
4	C1	Safety Capacitors 0.33 µF 10% 310 V AC	MX2334KQ3C20GB2000R	DGCX	1
5	C2, C3	CAP ALUM 68UF 20% 400 V RADIAL	KCMS2002G680MF	YMIN	2
6	C4	MLCC - SMD/SMT 1 kV 1 nF X7R 1206 10%	GRM31BR72H102KW01	Murata	1
7	C5, C23	MLCC - SMD/SMT 50 V 1 nF X7R 0603 10%	–	–	2
8	C6	MLCC - SMD/SMT 50 V 33 pF X7R 0603 10%	–	–	1
9	C7, C21	MLCC - SMD/SMT 50 V 680 pF X7R 0603 10%	–	–	2
10	C8, C24	CAP ALUM 33UF 20% 50 V RADIAL	ESH336M050AC3AA	KEMET	2
11	C9, C14, C17, C25, C26	MLCC - SMD/SMT 50 V 100 nF X7R 0603 10%	–	–	5
12	C10	MLCC - SMD/SMT 200 V 560 pF X7R 1206 10%	–	–	1
13	C11	MLCC - SMD/SMT 200 V 1 nF X7R 1206 10%	–	–	1
14	C12, C13	CAP ALUM HYBRID 470 µF 20% 35 V TH	EEH-AZSV471UB	Panasonic Electronic Components	2
15	C15, C16	CAP ALUM POLY 820UF 20% 16 V RADIAL	APSG160ELL821MH16S	Chemi-Con	2
16	C18	MLCC - SMD/SMT 25 V 4.7 µF X7R 0603 10%	–	–	1
17	C19	MLCC - SMD/SMT 50 V 68 nF X7R 0603 10%	–	–	1
18	C20	MLCC - SMD/SMT 50 V 2.2 nF X7R 0603 10%	–	–	1
19	C22	CAP ALUM 220UF 20% 35 V RADIAL	ESE227M035AG3AA	KEMET	1

Bill of materials

S.No.	Designator	Description	Manufacturer	Part number	Qty.
20	CY1	CAP CER 1000 PF 300/440 V AC Z5U	CS65ZU2GA102MYNKA	TDK Corporation	1
21	D1	DIODE GEN PURP 1 KV 1 A SMA	S1M	Diotec Semiconductor	1
22	D2	Diode 200 V 1 A Surface Mount SOD-123W	PMEG200G10ELRX	Nexperia	1
23	D3	DIODE GEN PURP 200 V 1 A SMA	S1D	Diotec Semiconductor	1
24	D4	DIODE STANDARD 200 V 15 A TO2202	MUR1520G	On-semi	1
25	D5	Ultrafast Diode 200 V 1.5 A SMA	STTH1R02A	ST	1
26	F1	Time Lag Fuse, 300 V, 3.15 A	36913150000	Littelfuse	1
27	L1	CMC 4 Pins, 15 mH	TD1515-15.0mH	Lucky-Tenda	1
28	L3	Radial Leaded Wire Wound Inductor WE-TI, 10 Uh	7447452100	Würth Elektronik	1
29	Q1	Power-Transistor, Optimized for high performance SMPS	ISC027N10NM6ATMA1	Infineon Technologies	1
30	R1, R2	Thick Film Resistors - SMD 1/4 watt 5.1M ohms 1206 1%	–	–	2
31	R3, R4	Thick Film Resistors - SMD 1/4 watt 5.1M ohms 1206 1%	–	–	2
32	R5	Thick Film Resistors - SMD 1/10 watt 71.5k ohms 0603 1%	–	–	1
33	R6, R7	Thick Film Resistors - SMD 1/4 watt 57.6k ohms 1206 1%	–	–	2
34	R8, R9	Thick Film Resistors - SMD 1/4 watt 150k ohms 1206 1%	–	–	2
35	R10	Thick Film Resistors - SMD 1/4 watt 10 ohms 1206 1%	–	–	1
36	R11, R21	Thick Film Resistors - SMD 1/10 watt 20k ohms 0603 1%	–	–	2

Bill of materials

S.No.	Designator	Description	Manufacturer	Part number	Qty.
37	R12	Thick Film Resistors - SMD 1/10 watt 2k ohms 0603 1%	–	–	1
38	R13, R19	Thick Film Resistors - SMD 1/10 watt 2.2 ohms 0603 1%	–	–	2
39	R14, R15	Thick Film Resistors - SMD 1/4 watt 0.47 ohms 1206 1%	–	–	2
40	R16, R17	Thick Film Resistors - SMD 1/4 watt 2.2 ohms 1206 1%	–	–	2
41	R18	Thick Film Resistors - SMD 1/10 watt 15k ohms 0603 1%	–	–	1
42	R20, R27, R29	Thick Film Resistors - SMD 1/10 watt 10k ohms 0603 1%	–	–	3
43	R22	Thick Film Resistors - SMD 1/10 watt 560k ohms 0603 1%	–	–	1
44	R23	Thick Film Resistors - SMD 1/10 watt 1.1M ohms 0603 1%	–	–	1
45	R24, R28	Thick Film Resistors - SMD 1/10 watt 30k ohms 0603 1%	–	–	2
46	R25	Thick Film Resistors - SMD 1/10 watt 3.9k ohms 0603 1%	–	–	1
47	R26	Thick Film Resistors - SMD 1/10 watt 18k ohms 0603 1%	–	–	1
48	R30	Thick Film Resistors - SMD 1/10 watt 2k ohms 1206 1%	–	–	1
49	T1	PQ26/20 12-Terminal EXT THT Vertical	–	–	1
50	U1	CoolSET™ SiP	ICE186EM	Infineon Technologies	1
51	U2	4 Terminal Low Drop Voltage Regulator	KIA78R15PI	KEC	1
52	VR1	VARISTOR 510V 1.75KA DISC 7MM	B72207S2321K 101	Epcos	1
53	ZD1	DIODE ZENER 12V 800MW DO219AB	BZD27C12P-E3-08		1

8 Transformer specification

8.1 Electrical diagram and coil build

Manufacturer and part number: Sumida (11328-T164)

Core size: PQ2620

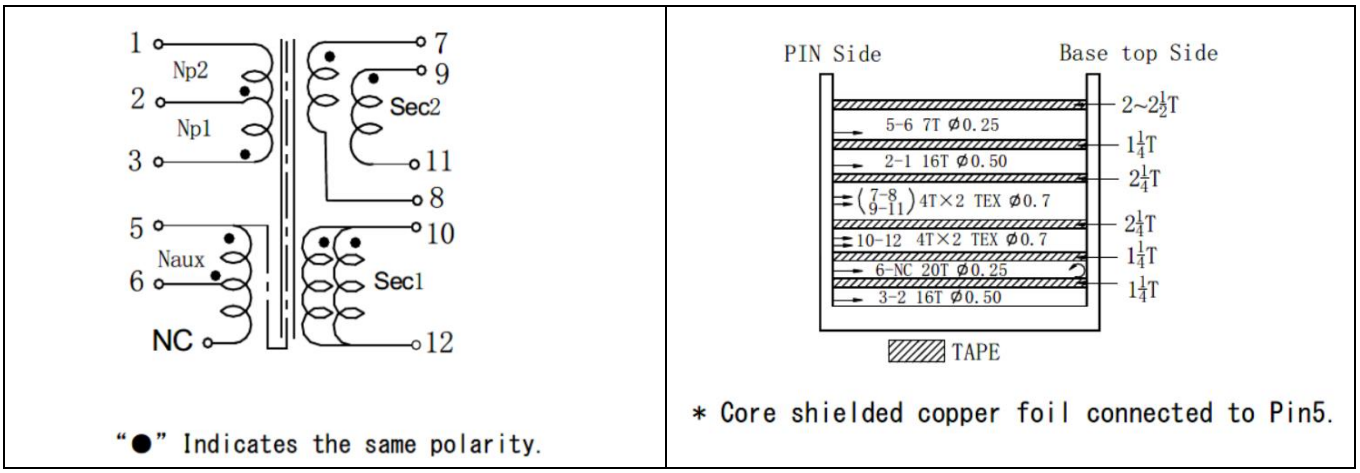


Figure 6 Electrical diagram and coil build

8.2 Electrical specifications

3.Electrical characteristics(at25℃)

Item	Specification	Measuring conditions
Inductance (3-1)	280μH±10% Within	100kHz, 0.1V (Tie 1+2, 3+4)
Leakage inductance (3-1)	5.0μH Max. (4.0μH Typ.)	100kHz, 0.1V Tie(5+6+7+8+9+10+11+12)
DCR (3-1)	222mΩ Max. (178mΩ Typ.)	
DCR (10-12)	9mΩ Max. (7.0mΩ Typ.)	
DCR (7-8) / (9-11)	19mΩ Max. (15mΩ Typ.)	
DCR (5-6)	245mΩ Max. (206mΩ Typ.)	
Turns ratio (1,3):(10,12):(7,8):(9,11):(5-6)	8:1:1:1.75 (±3%)	
Hi-pot (1,3,5,6-7,8,9,10,11,12)	AC 2500Vrms	50/60Hz, 1.0mA, 1Min

Figure 7 Electrical diagram

9 Measurement data and graphs

All performance data is measured at room temperature T_a = 25°C unless otherwise specifically mentioned.

9.1 Efficiency result

Efficiency data has been taken under +12 V and +24 V load condition. The +15 V LDO output is disabled during the test.

Table 7 Efficiency data

Input (V AC/Hz)	Load percentage	P_{IN} (W)	V_{OUT1} (V)	I_{OUT1} (A)	V_{OUT2} (V)	I_{OUT2} (A)	P_{OUT} (W)	Efficiency (%)	Average efficiency (%)
90 V AC/ 60 Hz	25%	16.620	12.185	0.625	23.760	0.319	15.19	91.38%	91.59%
	50%	32.830	12.182	1.251	23.767	0.626	30.13	91.76%	
	75%	49.050	12.175	1.878	23.772	0.934	45.05	91.85%	
	100%	65.960	12.175	2.503	23.762	1.254	60.27	91.37%	
115 V AC/ 60 Hz	25%	16.560	12.187	0.625	23.755	0.319	15.19	91.71%	92.21%
	50%	32.630	12.185	1.251	23.762	0.626	30.13	92.32%	
	75%	48.710	12.177	1.878	23.767	0.934	45.05	92.49%	
	100%	65.270	12.170	2.503	23.760	1.254	60.25	92.31%	
230 V AC/ 50 Hz	25%	16.680	12.187	0.625	23.755	0.318	15.16	90.88%	92.61%
	50%	32.490	12.182	1.251	23.752	0.626	30.12	92.69%	
	75%	48.230	12.175	1.878	23.752	0.934	45.04	93.38%	
	100%	64.430	12.170	2.503	23.745	1.254	60.23	93.48%	
264 V AC/ 50 Hz	25%	16.670	12.185	0.625	23.755	0.319	15.19	91.10%	92.67%
	50%	32.540	12.185	1.251	23.750	0.626	30.12	92.56%	
	75%	48.220	12.177	1.878	23.750	0.934	45.04	93.40%	
	100%	64.330	12.172	2.503	23.742	1.254	60.23	93.63%	

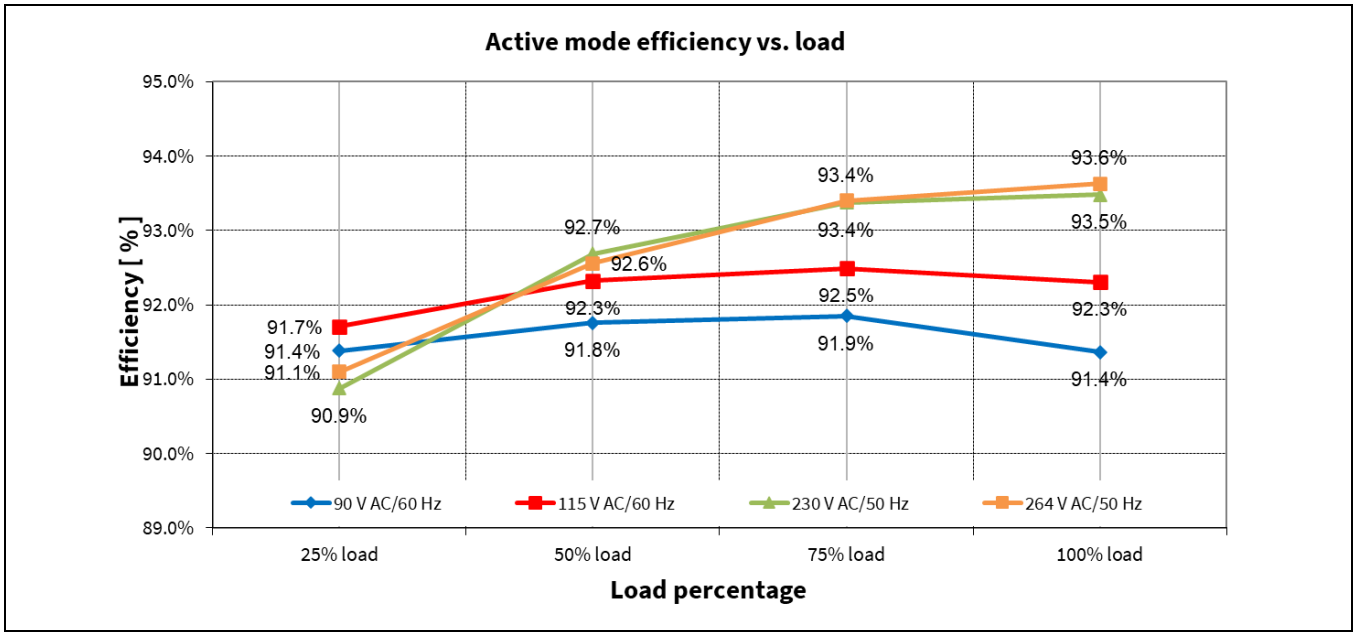


Figure 8 Efficiency vs. loading

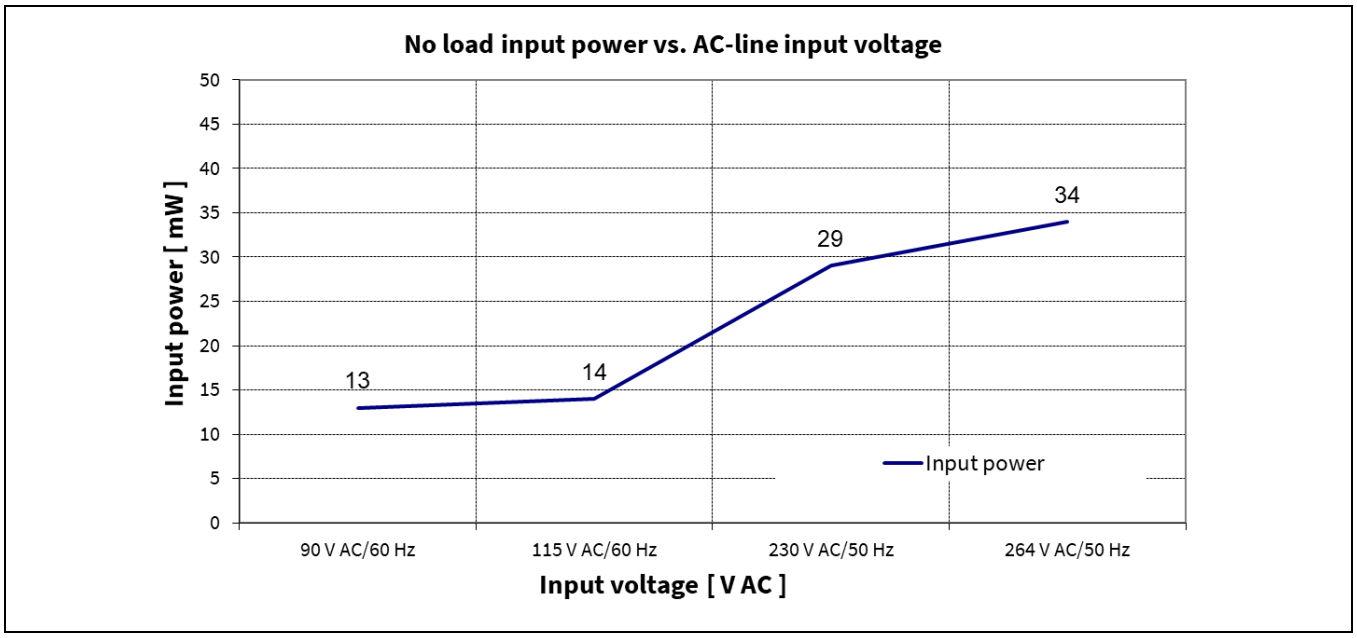


Figure 9 No load input power vs. AC-line input voltage (LDO disabled by removing D5 and X-cap discharge resistors R1 and R2 removed)

9.2 ESD immunity (EN 61000-4-2)

The reference board was subjected to ESD testing according to EN 61000-4-2 level 3 (±8 kV contact and ±15 kV air discharge). It was tested at full load (resistive load) and met criteria A (normal performance within the specification limits).

Table 8 System ESD test result

Description	ESD test	Level	Number of strikes			Test result
			V_{OUT1}	V_{OUT2}	GNDS	
230 V AC, 60 W	Contact	±8 kV	10	10	10	Pass
	Air	±15 kV	10	10	10	Pass

9.3 Surge immunity (EN 61000-4-5)

The reference board was subjected to a surge immunity test according to EN 61000-4-5 level 4 (±2 kV DM and
±4 kV CM). It was tested at full load (resistive load) and met criteria A (normal performance within the specification limits). Disable input line OVP to avoid mis triggering while testing ±4 kV CM.

Table 9 System lightning surge immunity test result

Description	Test	Level		Number of strikes				Test result
				0°	90°	180°	270°	
230 V AC, 60 W	DM	±2 kV	L ↔ N	3	3	3	3	Pass
	CM	±4 kV	L ↔ GNDS	3	3	3	3	Pass
		±4 kV	N ↔ GNDS	3	3	3	3	Pass

9.4 Conducted emissions (EN 55022 Class B)

The conducted EMI was measured by Schaffner (SMR4503) and followed the test standard of EN 55022 (CISPR 22) Class B. The reference board was tested at full load (resistive load) at input voltages of 115 V AC and 230 V AC.

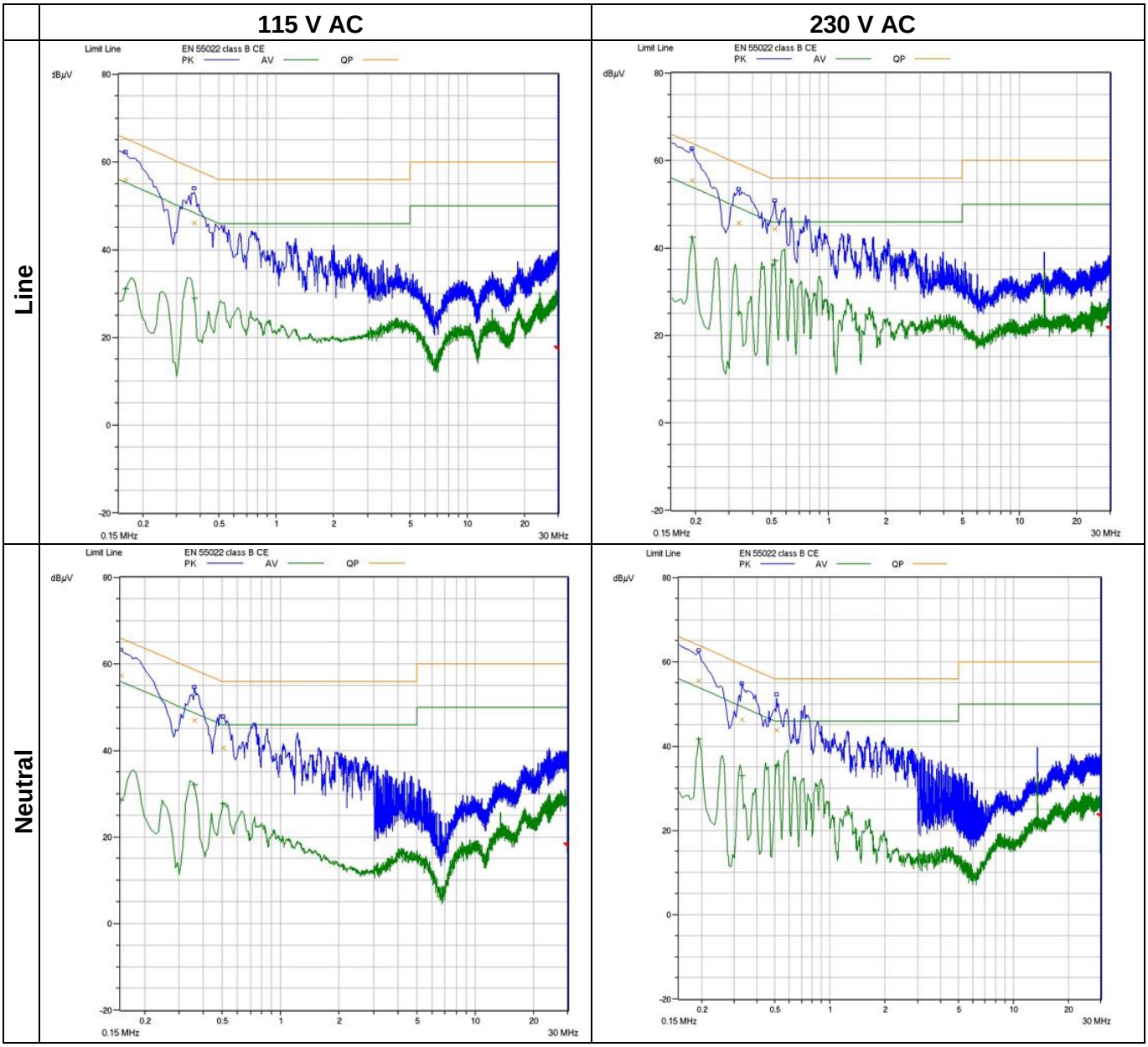


Figure 10 Conducted emissions

9.5 Thermal measurement

The thermal testing of the reference board was executed in open air without forced ventilation at an ambient temperature of 25°C. An infrared thermography camera (FLIR-T62101) was used to capture the thermal reading of critical components. The measurements were taken at the maximum load running for one hour. The tested input voltages were 90 V AC and 264 V AC.

Table 10 Component temperature at full load under T_a = 25°C

Circuit code	Major component	Input voltage 90 V AC	Input voltage 264 V AC
		Temperature (°C)	Temperature (°C)
D4	24 V rectifier diode	77.4	77.5
U1	ICE186EM	72.5	55.9
BR1	Diode bridge	70.2	40.5

Measurement data and graphs

Circuit code	Major component	Input voltage 90 V AC	Input voltage 264 V AC
		Temperature (°C)	Temperature (°C)
Q1	SR MOSFET	52.7	54.1
D1	Primary side snubber diode	66.3	53.3
T1	Transformer	67.9	71.5

90 V AC maximum load and 25°C ambient

264 V AC maximum load and 25°C ambient

Figure 11 Thermal image of REF_60WD1_ZVS_186EM

10 Waveforms and scope plots

All waveforms and scope plots were recorded with a Teledyne LeCroy oscilloscope.

10.1 Startup at full load

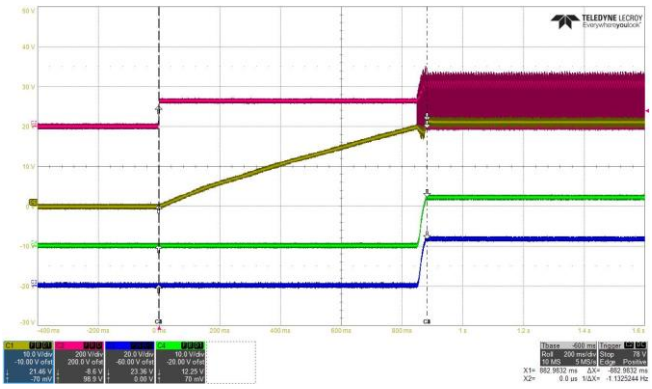
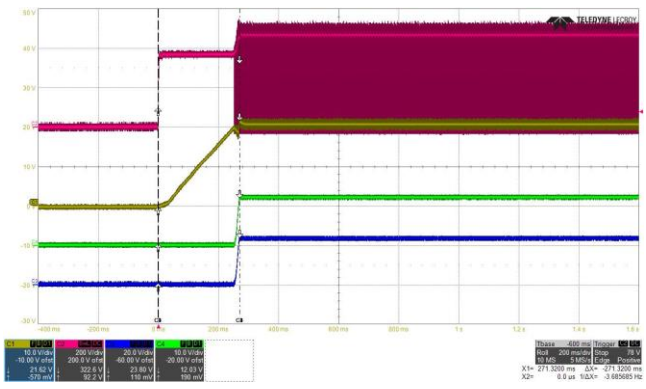
	
C1 (yellow) : VCC voltage (V_{VCC}) C2 (purple) : Drain voltage (V_{DRAIN}) C3 (blue) : +24 V output voltage C4 (green) : +12 V output voltage	C1 (yellow) : VCC voltage (V_{VCC}) C2 (purple) : Drain voltage (V_{DRAIN}) C3 (blue) : +24 V output voltage C4 (green) : +12 V output voltage
90 V AC startup time at full load is around 880 ms	264 V AC startup time at full load is around 270 ms
The board can startup as expected over 90~264V AC, output voltage smoothly rises and regulates	

Figure 12 Startup at full load

10.2 Switching waveform at full load

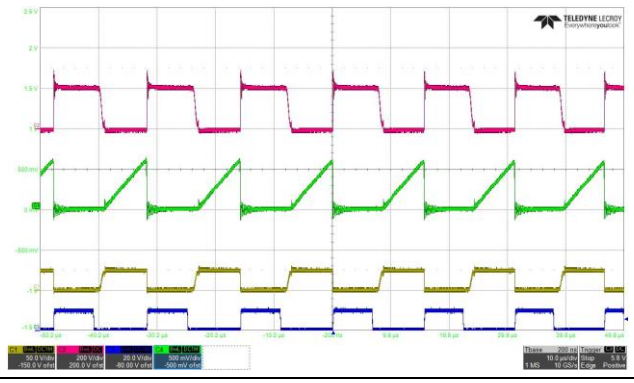
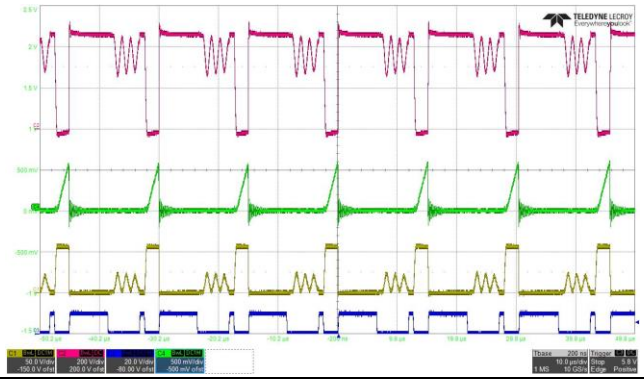
	
C1 (yellow) : SR Drain voltage (V_{SR_DRAIN}) C2 (purple) : Drain voltage (V_{DRAIN}) C3 (blue) : SR Gate voltage (V_{SR_GATE}) C4 (green) : CS voltage (V_{CS})	C1 (yellow) : SR Drain voltage (V_{SR_DRAIN}) C2 (purple) : Drain voltage (V_{DRAIN}) C3 (blue) : SR Gate voltage (V_{SR_GATE}) C4 (green) : CS voltage (V_{CS})
V_{IN} = 90 V AC, full load; the first valley is measured (QR = 1 at low line)	V_{IN} = 264 V AC, full load; the third valley is measured (QR = 3 at high line with ZVS switching)
ICE186EM operates quasi-resonant valley switching at low line and together with zero-voltage switching at high line	

Figure 13 Switching waveform at full load

10.3 Output ripple voltage at full load

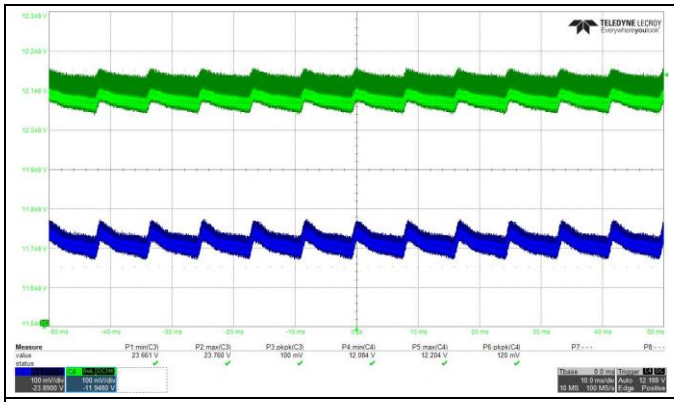
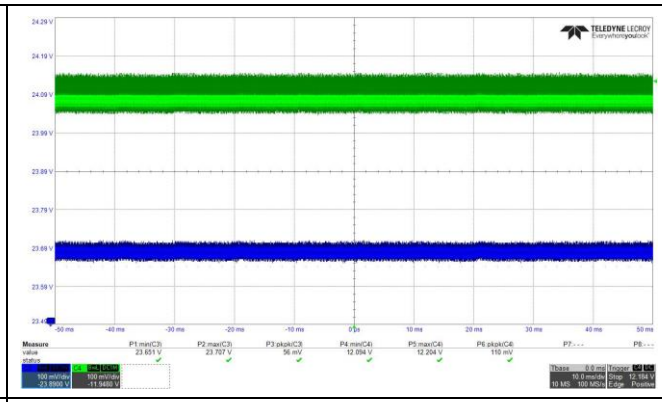
	
C2 (green) : +12 V output ripple voltage C3 (blue) : +24 V output ripple voltage	C2 (green) : +12 V output ripple voltage C3 (blue) : +24 V output ripple voltage
V_{IN} = 90 V AC V_{ripple_pkpk} for +12 V output voltage: 120 mV V_{ripple_pkpk} for +24 V output voltage: 100 mV	V_{IN} = 264 V AC V_{ripple_pkpk} for +12 V output voltage: 110 mV V_{ripple_pkpk} for +24 V output voltage: 56 mV

Figure 14 Output ripple voltage at full load (20 MHz bandwidth and 10 µF electrolytic capacitor in parallel with 0.1 µF ceramic capacitor)

10.4 Output ripple voltage at no load

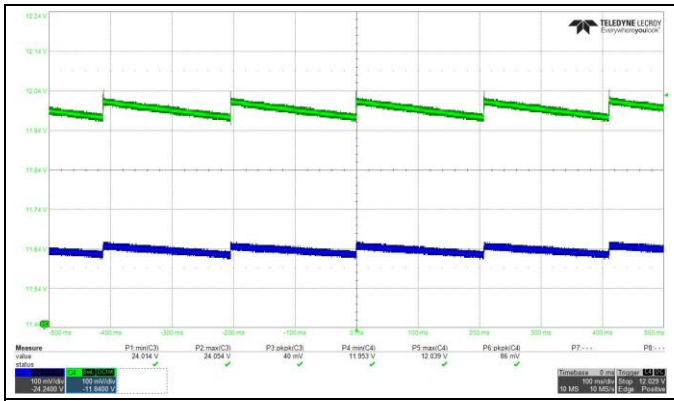
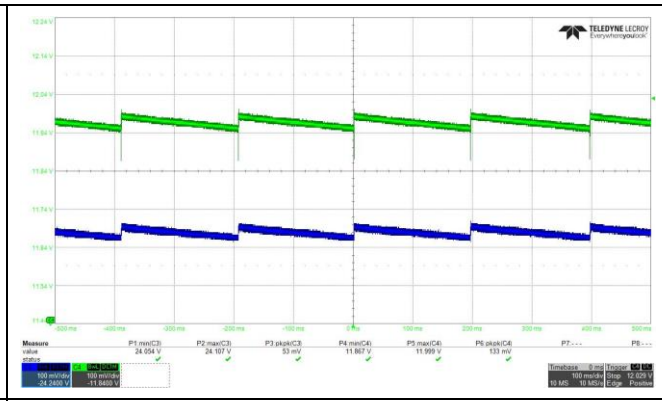
	
C2 (green) : +12 V output ripple voltage C3 (blue) : +24 V output ripple voltage	C2 (green) : +12 V output ripple voltage C3 (blue) : +24 V output ripple voltage
V_{IN} = 90 V AC V_{ripple_pkpk} for +12 V output voltage: 86 mV V_{ripple_pkpk} for +24 V output voltage: 40 mV	V_{IN} = 264 V AC V_{ripple_pkpk} for +12 V output voltage: 133 mV V_{ripple_pkpk} for +24 V output voltage: 53 mV

Figure 15 Output ripple voltage at no load (20 MHz bandwidth and 10 µF electrolytic capacitor in parallel with 0.1 µF ceramic capacitor)

10.5 Load-transient response at 12 V (full load at 24 V)

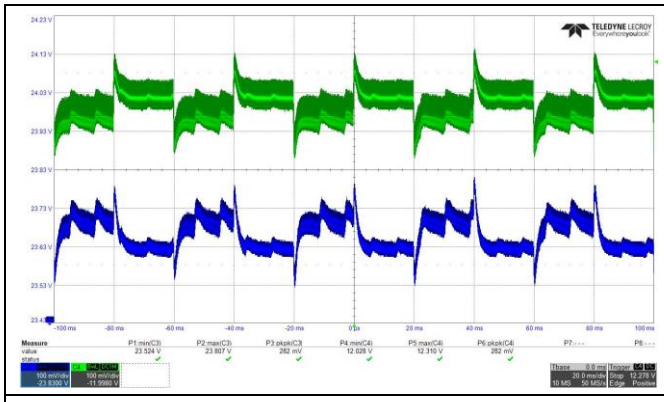
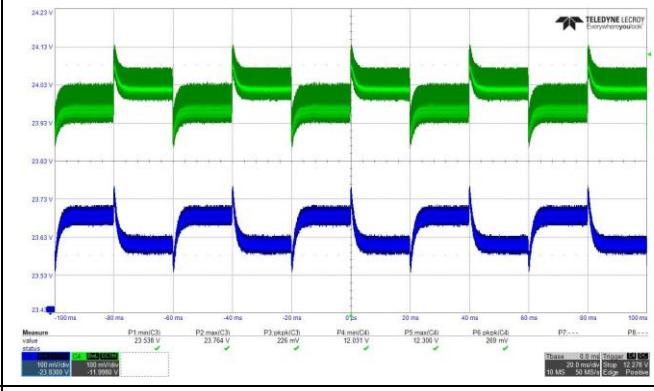
	
C2 (green) : +12 V output ripple voltage C3 (blue) : +24 V output ripple voltage	C2 (green) : +12 V output ripple voltage C3 (blue) : +24 V output ripple voltage
V_{IN} = 90 V AC V_{ripple_pkpk} for +12 V output voltage: 282 mV V_{ripple_pkpk} for +24 V output voltage: 282 mV	V_{IN} = 264 V AC V_{ripple_pkpk} for +12 V output voltage: 269 mV V_{ripple_pkpk} for +24 V output voltage: 226 mV

Figure 16 Load-transient response (+12 V output load change from 10% to 100% 0.8 A/µs slew rate, 25 Hz; 20 MHz bandwidth and 10 µF electrolytic capacitor in parallel with 0.1 µF ceramic capacitor; full load at +24 V)

10.6 Load-transient response at 12 V (10% load at 24 V)

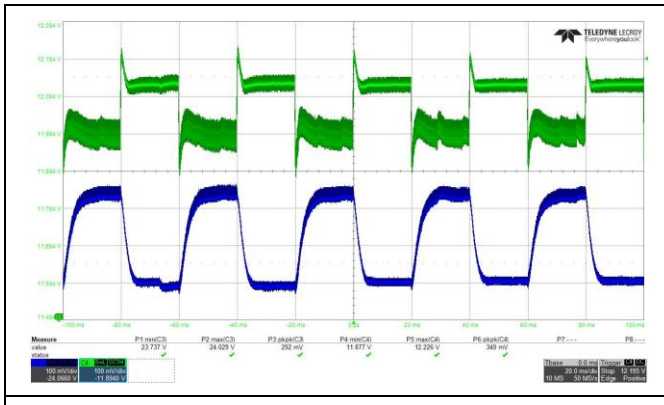
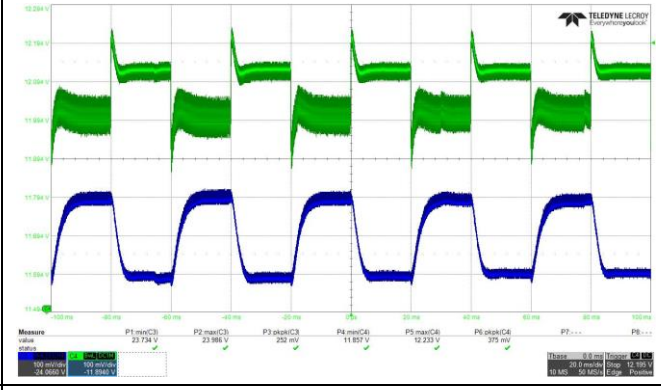
	
C2 (green) : +12 V output ripple voltage C3 (blue) : +24 V output ripple voltage	C2 (green) : +12 V output ripple voltage C3 (blue) : +24 V output ripple voltage
V_{IN} = 90 V AC V_{ripple_pkpk} for +12 V output voltage: 349 mV V_{ripple_pkpk} for +24 V output voltage: 292 mV	V_{IN} = 264 V AC V_{ripple_pkpk} for +12 V output voltage: 375 mV V_{ripple_pkpk} for +24 V output voltage: 252 mV

Figure 17 Load-transient response (+12 V output load change from 10% to 100% at 0.8 A/µs slew rate, 25 Hz; 20 MHz bandwidth and 10 µF electrolytic capacitor in parallel with 0.1 µF ceramic capacitor; 10% load at +24 V)

10.7 Load-transient response at 24 V (full load at 12 V)

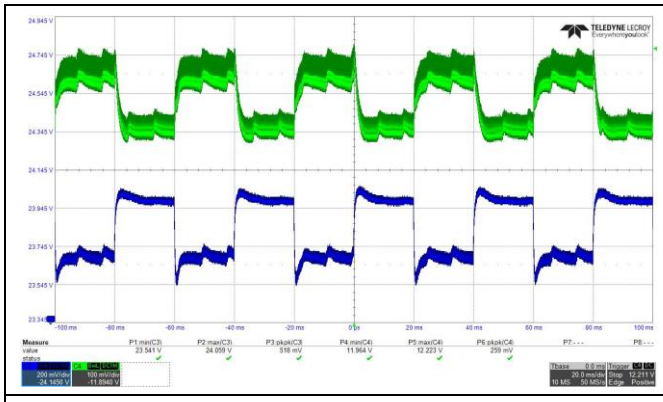
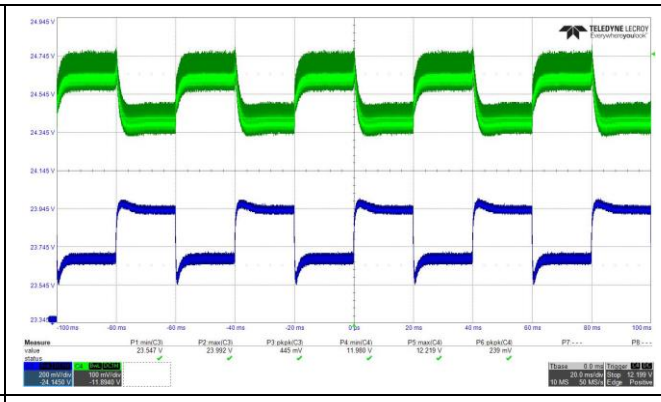
	
C2 (green) : +12 V output ripple voltage C3 (blue) : +24 V output ripple voltage	C2 (green) : +12 V output ripple voltage C3 (blue) : +24 V output ripple voltage
V_{IN} = 90 V AC V_{ripple_pkpk} for +12 V output voltage: 259 mV V_{ripple_pkpk} for +24 V output voltage: 518 mV	V_{IN} = 264 V AC V_{ripple_pkpk} for +12 V output voltage: 239 mV V_{ripple_pkpk} for +24 V output voltage: 445 mV

Figure 18 Load-transient response (+24 V output load change from 10 percent to 100 percent at 0.8 A/µs slew rate, 25 Hz; 20 MHz bandwidth and 10 µF electrolytic capacitor in parallel with 0.1 µF ceramic capacitor; full load at +12 V)

10.8 Load-transient response at 24 V (10% load at 12 V)

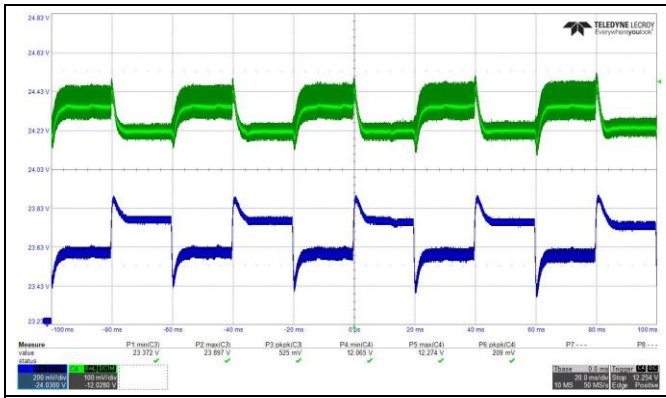
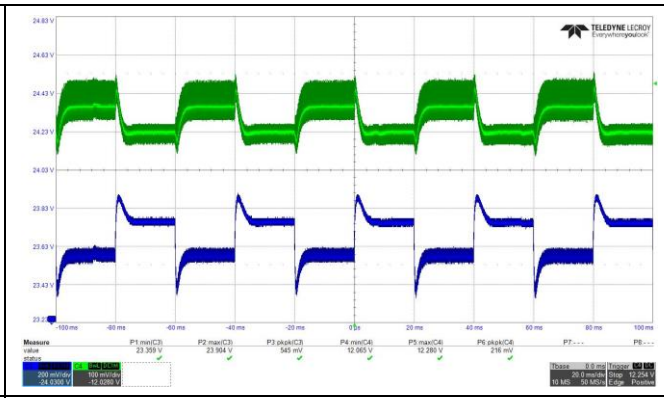
	
C2 (green) : +12 V output ripple voltage C3 (blue) : +24 V output ripple voltage	C2 (green) : +12 V output ripple voltage C3 (blue) : +24 V output ripple voltage
V_{IN} = 90 V AC V_{ripple_pkpk} for +12 V output voltage: 209 mV V_{ripple_pkpk} for +24 V output voltage: 525 mV	V_{IN} = 264 V AC V_{ripple_pkpk} for +12 V output voltage: 216 mV V_{ripple_pkpk} for +24 V output voltage: 545 mV

Figure 19 Load-transient response (+24 V output load change from 10 percent to 100 percent at 0.8 A/µs slew rate, 25 Hz; 20 MHz bandwidth and 10 µF electrolytic capacitor in parallel with 0.1 µF ceramic capacitor; 10% load at +12 V)

11 Related resources

- AC-DC integrated power stage - CoolSET™
- Power Management ICs
- REF_60W1_ZVS_186EM

References

[1] Infineon Technologies AG: Design guide – Design guide for ZVS QR flyback converter using CoolSET™ SiP; Available online

[2] Infineon Technologies AG: Datasheet – CoolSET™ SiP; Available online

[3] Infineon Technologies AG: Calculation tool: CoolSET™ SiP; Available online

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