Wide input range 720 W 48 V to 12 V regulated LLC converter using XDPP1148 digital power controller

About this document

Scope and purpose

This application note presents the design and performance of a closed-loop frequency modulated 720 W LLC converter using XDP™ XDPP1148 for 48 V to 12 V applications. The digital power controller XDPP1148 natively supports various LLC configurations, including full-bridge to full-bridge (FBFB), half-bridge center-tapped (HBCT), and phase-shift full-bridge (PSFB).

The aim of this document is to explain both basic and advanced LLC control functions provided by XDPP1148, and provide configuration examples for frequency modulation, soft-start, synchronous rectifier (SR) timing control, burst mode, and phase shift operation.

Intended audience

The intended audiences for this document are applications engineers, power supply design engineers for brick modules, telecom and server power systems.

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1 Introduction

48 V to 12 V intermediate-bus converters (IBCs) are widely used in various applications, including telecom, server, and other industrial applications. Various topologies have been investigated with the goal of increasing power density, efficiency, and optimizing cost. The IBC can be regulated, semi-regulated, or unregulated. Unregulated IBCs are also referred to as DC transformers (DCX) and are expected to have very high efficiency. The DCX can be either isolated or non-isolated, depending on the application. LLC topology has been a very suitable candidate, thanks to the ability to operate always at resonance that achieves optimal performance over the entire load range.

When regulation is required, there are a few options. The first option is to use two stages, for example, a DCX followed by a buck converter. This approach allows each stage to be optimized for the best efficiency. However, both converters have to process the full power and could incur high system cost. It is possible to configure these two converters differently, such that the DCX processes the majority of the power, and the buck converter only converts minimum power to achieve regulation. This can ensure the maximum efficiency, however, at the expense of control complexity. The second option is to just keep the same topology, but change the control from open-loop to closed-loop. For example, LLC converters can achieve closed-loop regulation using frequency modulation. Although this option may seem straightforward, it often requires redesigning the converter and configuring the controller.

This application note focuses on the closed-loop regulated LLC converter using the Infineon XDP™ XDPP1148-100B digital power controller, which has built-in support for various LLC-specific functions, such as frequency modulation, soft-start, SR adaptive timing control and burst mode operation. The Infineon evaluation board EVAL_720W_LLC_XDPP1148 consists of full-bridge LLC with full-bridge synchronous rectification. The simplified schematic diagram is shown in Figure 1. The XDPP1148 controller is located on an external Infineon evaluation board EVAL_XDPP1148_DB. All PWM and sensing signals are routed through high-speed mezzanine connectors.

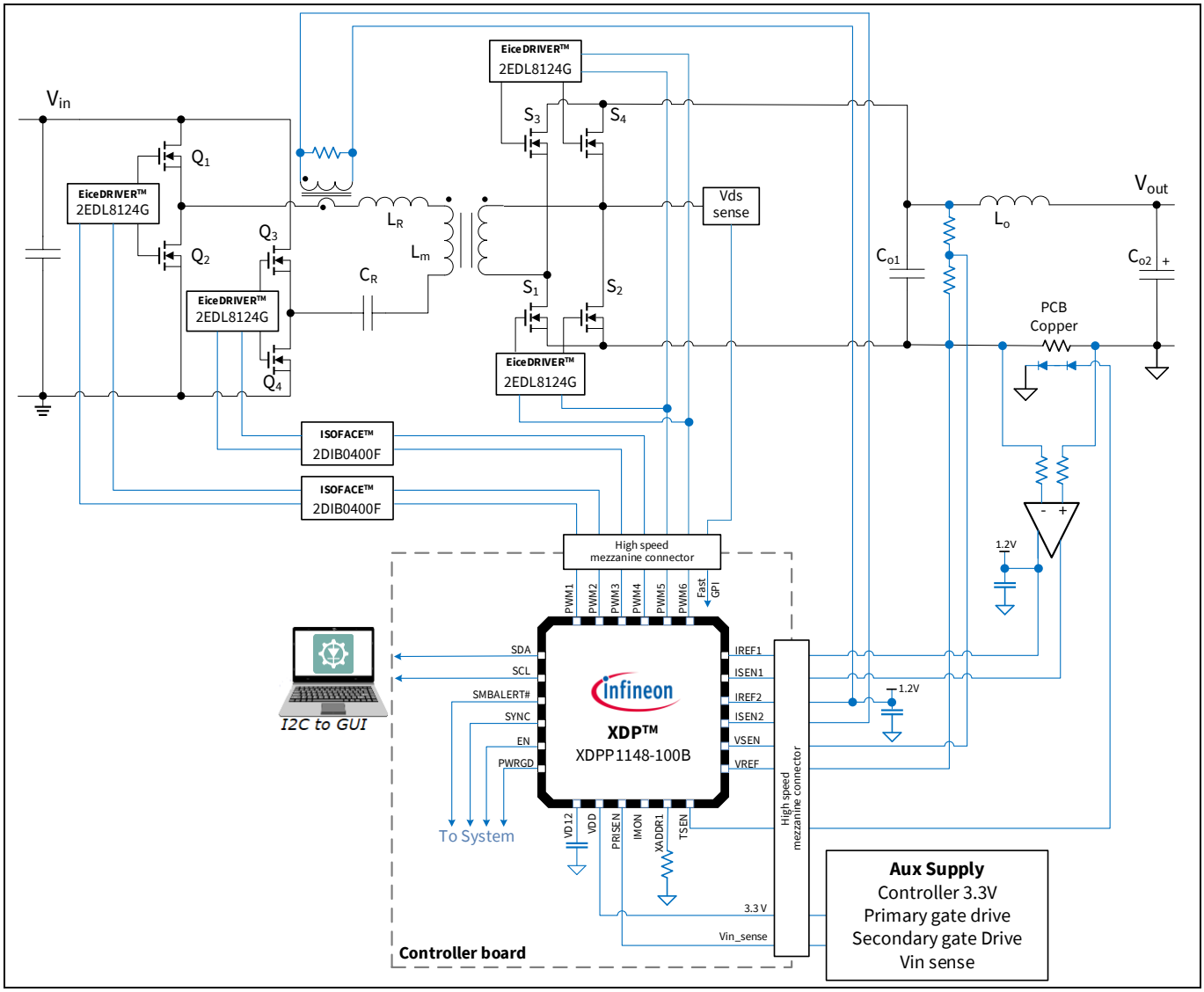


Figure 1 Simplified diagram of Infineon EVAL_720W_LLC_XDPP1148 with external controller board

1.1 Board specifications

The specifications for the Infineon EVAL_720W_LLC_XDPP1148 are given in Table 1.

Specifications are given for T_a = 25°C unless otherwise specified.

Table 1 Specifications

Parameter	Symbol	Values			Unit	Note/test condition
		Min.	Typ.	Max.		
Operating input voltage	V_{in}	44	48	60	V	–
Input current RMS value	$I_{in,RMS}$	–	16	–	A	V_{in} = 48 V, P_{out} = 720 W
Start-up voltage threshold	$V_{in(on)}$	38	–	–	V	
Minimum operating voltage after start-up	$V_{in(off)}$	–	–	36	V	–
Output voltage set-point	$V_{out,nom}$	–	12	–	V	–
Output current	I_{out}	–	–	60	A	–
Output power	P_{out}	–	–	720	W	v_{air} = 4 m/s
Efficiency	η	–	95	–	%	V_{in} = 48 V, P_{out} = 720 W
Power dissipation	P_{diss}	–	38	–	W	V_{in} = 48 V, P_{out} = 720 W
Output voltage ripple (peak-to-peak)	$V_{out,ac(pp)}$	–	25 300	–	mV	100% load, continuous switching Burst mode
Output voltage set-point tolerance	$\sigma V_{out,nom}$	-1	–	+1	%	–
Output voltage regulation (load)	$\Delta V_{out(load)}$	–	–	12	mV	V_{in} = 48 V, 0-100% of $I_{out,max}$
Output voltage regulation (line)	$\Delta V_{out(line)}$	–	–	120	mV	V_{in} = 46…60 V, I_{out} = 60 A
Dynamic load response - Output voltage deviation - Settling time	 $\Delta V_{out(tr,load)}$ $t_{tr(load)}$	–	–	 ±300 80	 mV µs	 V_{in} = 48 V, I_{out} from 0 A to 30 A at 5 A/µs
Switching frequency	f_{sw}	200	–	600	kHz	–
Airflow velocity	v_{air}	–	800 4	–	LFM m/s	–
Operating temperature (ambient)	T_a	-40	–	+50	°C	–
Functional isolation voltage	V_{iso}	–	1500	–	V	–

1.2 Resonant tank design

The target operating frequency range is 200 kHz to 600 kHz. The resonant frequency is selected to be around 300 kHz. The ratio of the magnetizing inductance and the resonant inductance needs to be low enough to get wider gain curve variation for closed loop regulation. This requirement differs from the design approach for open-loop LLC converters [1], and has an impact on both the efficiency and output power capability.

In this design, the resonant capacitance is 0.6 µF, using all NP0 capacitors. The resonant inductor is 0.42 µH, with 50 nH estimated transformer leakage inductance from the transformer, the total resonant inductance is 0.47 µH. The magnetizing inductance is 6.5 µH. The transformer turns ratio n = Np:Ns is 4.

The voltage gain curve based on this design is plotted in Figure 2, for light load (1 mA), 50% load (30 A), and full load (60 A). The normalized frequency (fs/fr) range is 0.67 to 2.0, corresponding to 200 kHz to 600 kHz.

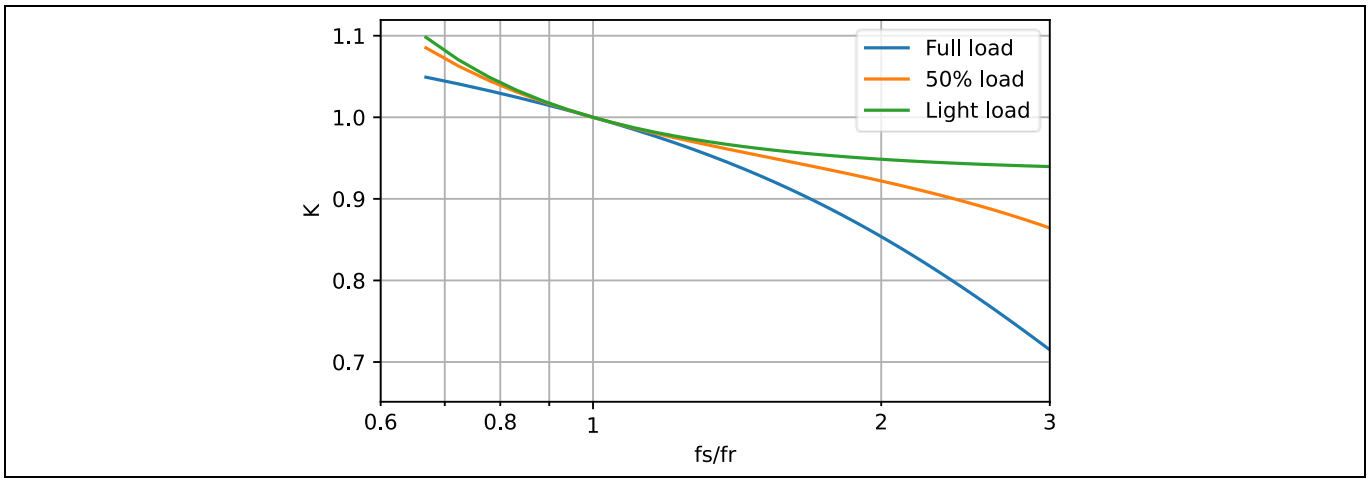


Figure 2 Voltage gain curve of the LLC converter

1.3 Schematics

The schematics of the power stage and auxiliary supply circuits are shown in Figure 3 and Figure 4. In the primary full-bridge, two OptiMOS™ 6 80 V MOSFETs (ISC031N08NM6) of 3.1 mΩ R_{DSON} are connected in parallel and driven by a single 2EDL8124G driver at each branch. In the secondary full-bridge, four OptiMOS™ 5 25 V MOSFETs (IQE006NE2LM5CG) with 0.65 mΩ R_{DSON} are used in parallel and driven by a single 2EDL8124G driver at each branch. The primary MOSFETs are controlled by 4 independent PWM signals, while the secondary MOSFETs are controlled by 2 PWM signals.

The power supply board features a range of sensing circuitry, including:

- Input and output voltage sensing
- Primary current sensing using a current transformer
- Secondary (load) current sensing via a PCB copper shunt
- Temperature sensing
- Secondary V_{DS} sensing

These sensing circuits provide critical monitoring and control functions for the power supply. All control and sensing signals are routed through the high-speed mezzanine connectors, J1 and J2.

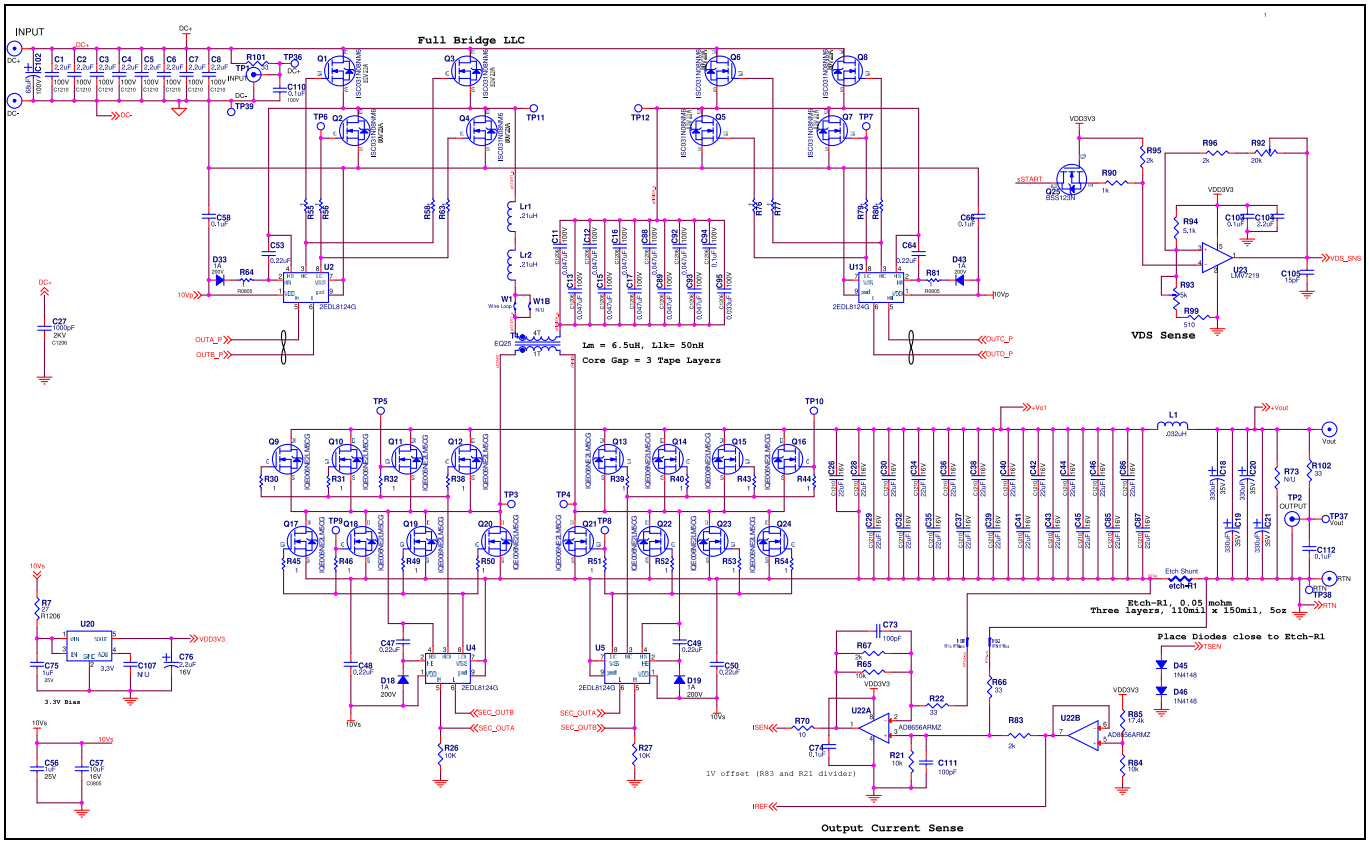


Figure 3 Power stage schematic

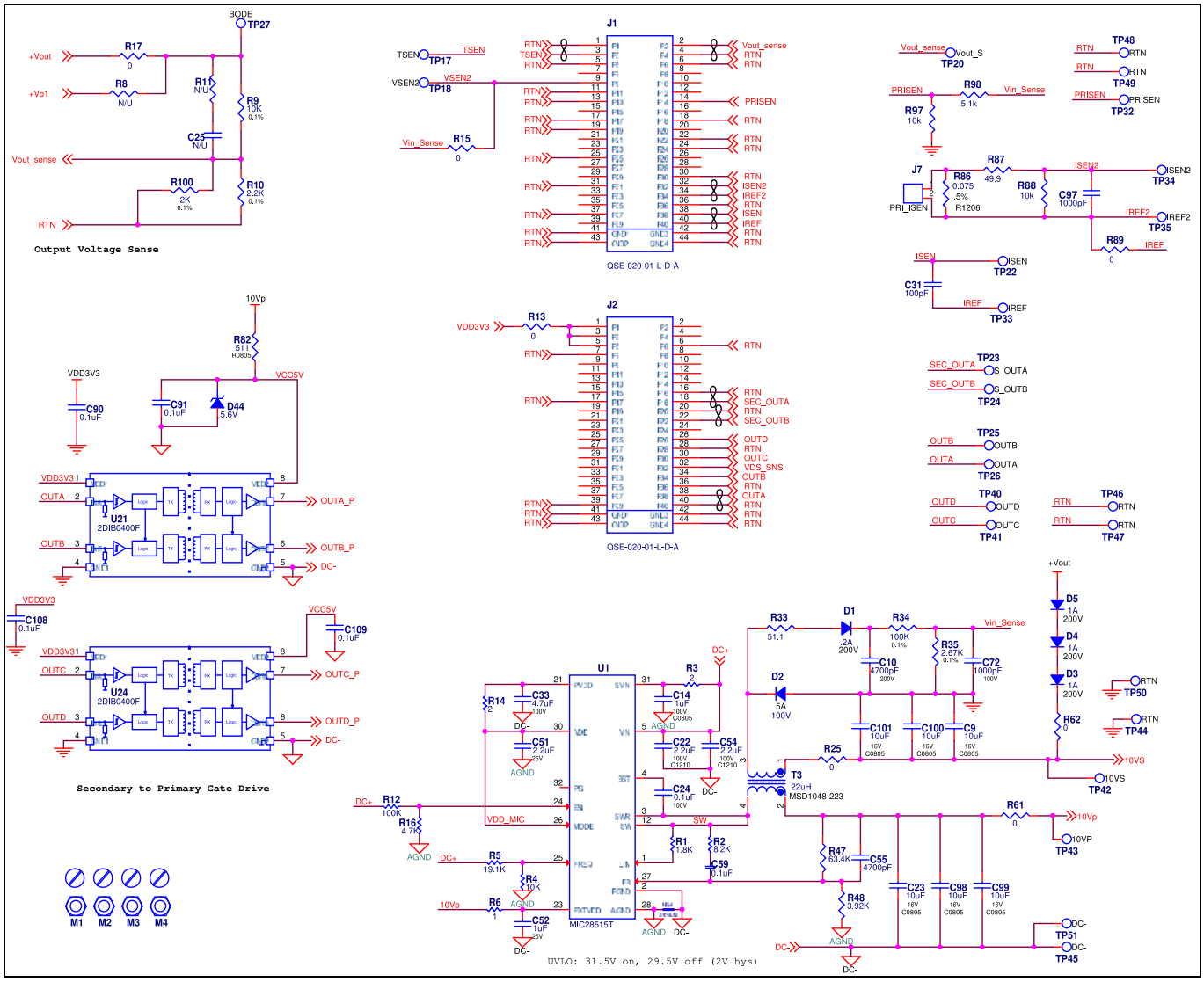


Figure 4 Auxiliary supply, isolator, and controller interface schematic

This design includes a planar transformer with Np:Ns = 4:1 turns ratio. The core geometry is an EQ25 and a plate with ferrite material ML27D. The primary winding is composed of four PCB layers in series, while the secondary winding is composed of ten PCB layers in parallel. The primary windings are interleaved with the secondary windings for minimum leakage inductance and proximity losses. A detailed description of the construction can be seen in Figure 5.

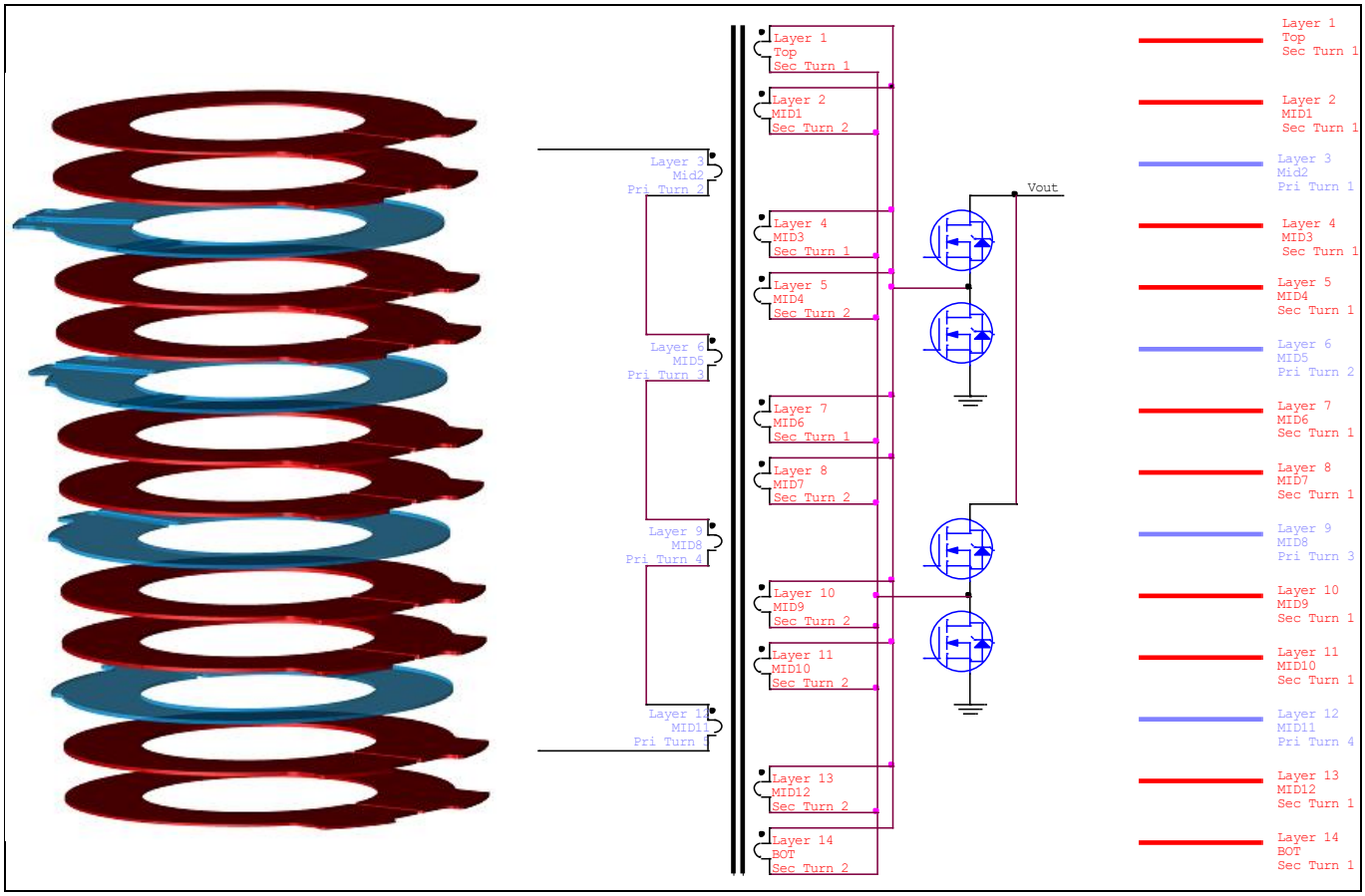


Figure 5 Planar transformer construction

2 XDPP1148 configuration

A detailed description of the configuration process for the XDPP1148 is provided in this section. Note that the XDPP1140 also supports LLC topologies, and the difference is that XDPP1140 only has one current sensing input and cannot sense both output and primary current.

2.1 Topology

For primary topology, the XDPP1148 supports LLC full-bridge, phase shift full-bridge, and half-bridge. For secondary topology, it supports full-bridge and center-tapped configurations. Only voltage mode control and trailing edge modulation are available for LLC topologies. The transformer turns ratio is defined as Ns:Np.

In this design, the primary topology is a full-bridge. Therefore, Q1 and Q4 (shown in Figure 1) are driven with the same PWM signal. Q2 and Q3 are also driven with the same PWM signal. These two PWMs are fixed at 50% duty cycle with proper dead times. When half mode is enabled (automatically by FW), this 50% duty cycle is represented as 100% duty cycle in the XDPP1148.

Table 2 Configuration for LLC topology

Register/PMBus command	Value	Comment
FW_CONFIG_REGULATION[15:12]	13	Topology select LLC FBFW
llc_mode	2	LLC closed loop mode

2.2 Current sensing

2.2.1 Primary AC current sensing

The current sense ADC in the XDPP1148 has 100 MHz sample rate and supports high frequency AC current waveform tracking. This is useful for sensing primary current in series resonant topologies such as LLC. The current estimator needs to be disabled and use 100% tracking settings. In this design, ISEN1 is used for output current sensing, and ISEN2 is used for primary current sensing.

The AC primary current can be easily scaled down using a current transformer. In this design, a 15:1 current transformer is used, as shown in Figure 6. The output of the current transformer connects to J7 (schematic in Figure 4), and into a 75 mΩ resistor (R86), converting to a voltage for the ADC.

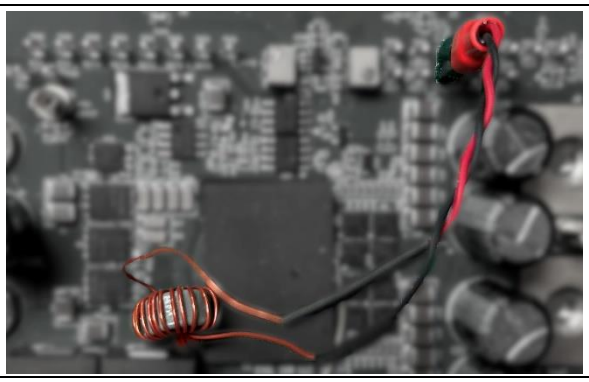


Figure 6 Primary AC current sensing transformer connected to J7

The configuration example for primary current sensing is listed in Table 3.

Table 3 Configuration for primary current sensing (ISEN2)

Register/PMBus	Value	Comment
ce1_topology	3	LLC
isp1_mode	4	Resonant primary sense
ce1_kslope_didv	0	Disable estimator
ce1_kslope_scale	0	Disable estimator
ce1_ktrack_hiz	5	100% tracking
ce1_ktrack_off	5	100% tracking
ce1_ktrack_on	5	100% tracking
ce1_pwmwin_dly	8	90ns delay between PWM signal and current sense waveform
FW_CONFIG_REGULATION[1]	1	Enable primary Isense
MFR_PHASE1_IOUT_APC	0.2056	ISEN2 current sense amps per code (APC)

2.2.2 Secondary load current sensing

The load current refers to the DC output current. The current sense shunt is typically placed after the high frequency filter capacitors and before the electrolytic capacitors. The current estimator also needs to be disabled and use 100% tracking settings. Note that even though the current estimator is disabled, the on and off mask registers still need to be set correctly. In this design, the PCB copper shunt is used, and its temperature drift should be compensated. The configuration for this design is listed in Table 4.

Table 4 Configuration for load current sensing (ISEN1)

Register/PMBus	Value	Comment
ce0_topology	3	LLC
isp0_mode	2	Load current sense
ce0_kslope_didv	0	Disable estimator
ce0_kslope_scale	0	Disable estimator
ce0_ktrack_hiz	5	100% tracking
ce0_ktrack_off	5	100% tracking
ce0_ktrack_on	5	100% tracking
ce0_on_mask0	5	PWM1 and PWM3 defines the 1st ON state of the current estimator
ce0_on_mask1	10	PWM2 and PWM4 defines the 2nd ON state of the current estimator
ce0_off_mask0	16	PWM5 defines the 1st OFF state of the current estimator
ce0_off_mask1	32	PWM6 defines the 2nd OFF state of the current estimator
ce0_pwmblank_dly	3	40ns blanking delay after rising/falling edge switching noise
FW_CONFIG_REGULATION[9]	1	Enable temperature compensation on output current sense
MFR_IOUT_APC	0.2813	ISEN1 current sense amps per code (APC)

2.3 Frequency modulation

A variable step digital ramp is used for frequency modulation. The PID output of the controller is mapped to the ramp step to control the frequency. The higher the PID output, the lower the ramp step and frequency. This inverse proportional relationship is depicted in Figure 7. The base frequency (Fmin) is set by register **pid_llc_tmax**. The minimum (Fmin_clamp) and maximum (Fmax_clamp, or Fmax in some documentations) frequencies during operation are set by registers **pid_llc_rampstep_min** and **pid_llc_rampstep_max**, respectively. The slope of line (Fgain) is set by **pid_llc_rampstep_gain**.

The internal maximum frequency (Fmin + Fgain) limits the maximum operating frequency (Fmax_clamp), as well as startup frequency (Fstart). In the case where Fmin + Fgain is larger than Fmax_clamp, which is usually true if Fstart is greater than Fmax_clamp, a non-zero PID preload value is used for smooth transition during soft start between open-loop and closed-loop operation. This is the PID value that results in the frequency of Fmax_clamp. The specifics of soft start will be explained in later sections.

The configuration for frequency modulation starts with Fmin, since all other frequencies are defined as a ratio to Fmin. Table 5 summarizes the register values for this design.

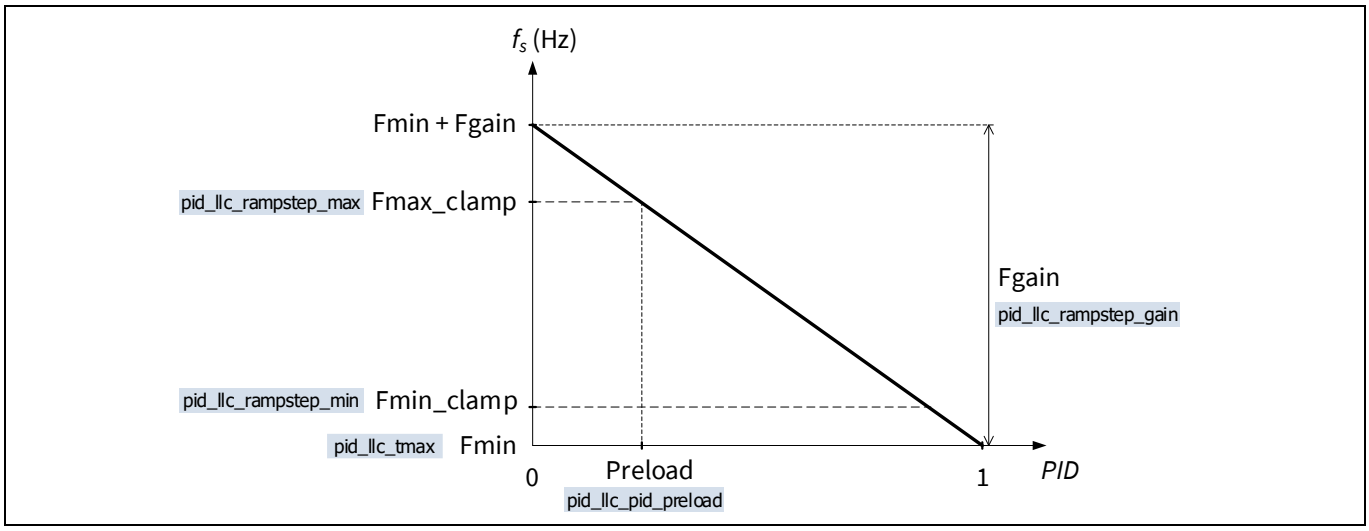


Figure 7 Frequency modulation with variable ramp

Table 5 Configuration for frequency modulation

Register	Value	Comment
pid_llc_tmax	1000	Period = 5 µs, Fmin = 200 kHz
pid_llc_rampstep_min	256	Fmin_clamp = 200 kHz
pid_llc_rampstep_gain	512	Fgain = 2.0 × 200 = 400 kHz
pid_llc_rampstep_max	704	Fmax_clamp = 2.75 × 200 = 550 kHz
pid_llc_pid_preload	0.125	Fmin + Fgain = Fmax_clamp

2.4 Frequency modulation with phase shift

For phase shift full-bridge LLC, the PWM mapping is changed so that the primary MOSFETs are driven independently with 4 PWM signals. In this way, the phase between the two half-bridges can be controlled. Figure 8 shows an example timing diagram with internal timing markers of t1 and t2 for even and odd cycles.

During normal operation, Q1 and Q3 timing are similar to the case in a standard full-bridge. After entering phase shift mode, the duty cycle is changed, indicated by t2e and t2o. Decreasing the duty cycle from 100% is equivalent to increasing the phase shift from 0 degrees. The maximum phase shift is limited by the minimum duty cycle. The extreme value of 0% duty cycle corresponds to 180-degree phase shift, which results in 0 V across the transformer and, consequently, no power delivered to the output.

The duty cycle curve can then be overlayed with the frequency modulation curve, as illustrated in Figure 9. When PID output is high, the duty cycle is at maximum (Dmax), which should be set to 100% for correct operation. As the PID output decreases beyond a transition point, the duty cycle starts to decrease, indicating an increase in phase shift. This transition point is where frequency reaches Fmax_clamp. By changing the overhead margin of frequency modulation (Fmin + Fgain – Fmax_clamp), one can change the PID output transition point. The rate of change of the duty cycle (or phase shift) is set by register **pid_llc_light_load_duty_slope** register. The minimum duty cycle (maximum phase shift) is set by **pid_llc_light_load_duty_min** register.

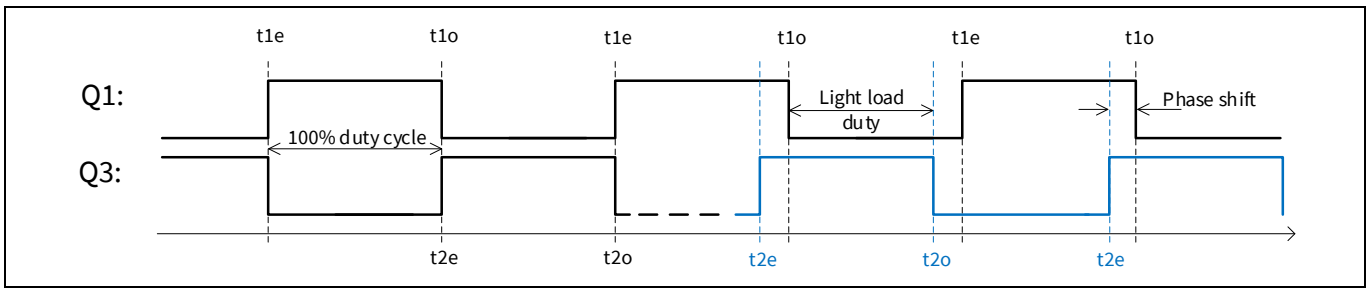


Figure 8 Example timing diagram for light load phase shift

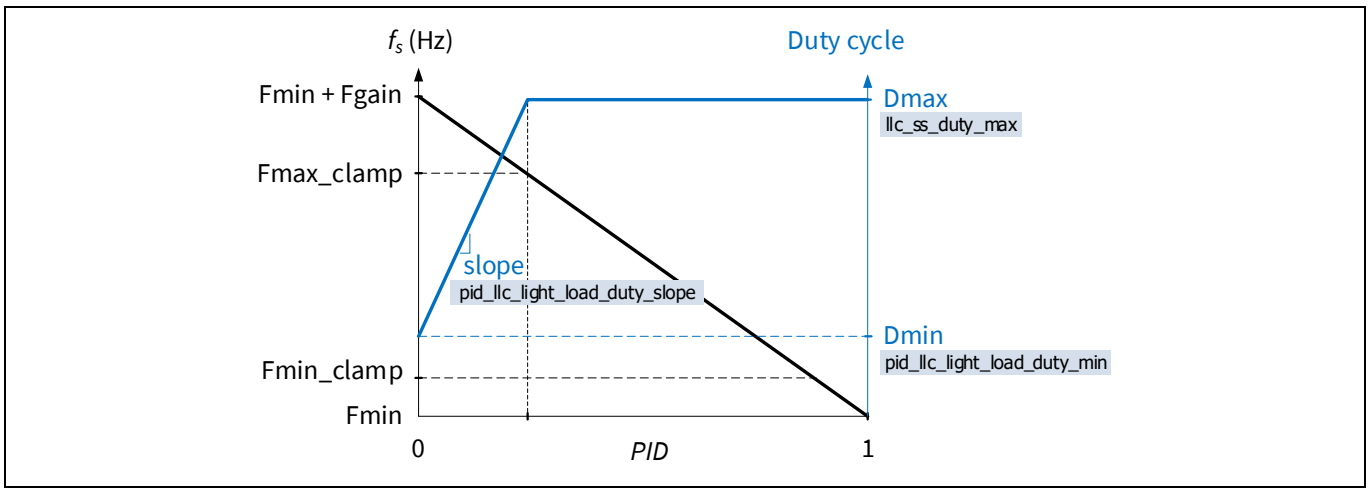


Figure 9 Frequency modulation with duty cycle reduction

This design does not use phase shift. However, since all primary MOSFETs are driven by independent PWMs, it is possible to reconfigure this board to a phase shift full-bridge LLC. As a design example, considering a frequency modulation range from 200 kHz to 600 kHz, a maximum phase shift of 108 degrees, and a PID transition point of 0.25, the register values can be computed as follows.

Fmin and Fmin_clamp are set to 200 kHz. Fmax_clamp is set to 600 kHz. The overhead margin of frequency modulation is calculated from the PID transition point (P):

$$(F_{\min} + F_{\text{gain}} - F_{\max_{\text{c}}\text{lamp}})/F_{\text{gain}} = P$$

$$F_{\text{gain}} = \frac{F_{\max_{\text{c}}\text{lamp}} - F_{\min}}{1 - P} = \frac{600\ - 200}{1 - 0.25} = 533\ \text{kHz}$$

Equation 1

According to Figure 8, 108 degrees maximum phase shift (PS_{max})corresponds to minimum duty cycle of 0.4.

$$D_{\min} = 1 - PS_{\max}/180 = 0.4$$

Equation 2

From Figure 9, the slope can be calculated from the PID transition point (P) of 0.25.

$$slope = (D_{\max} - D_{\min})/P = (1 - 0.4)/0.25 = 2.4$$

Equation 3

The configuration for this example phase shift LLC is listed in Table 6.

Table 6 Configuration example for phase shift LLC

Register	Value	Comment
pid_llc_tmax	1000	Period = 5 µs, Fmin = 200 kHz
pid_llc_rampstep_min	256	Fmin_clamp = 200 kHz
pid_llc_rampstep_gain	682	Fgain = 2.664 × 200 = 532.8 kHz
pid_llc_rampstep_max	768	Fmax_clamp = 3.0 × 200 = 600 kHz
pid_llc_light_load_duty_en	1	Enable light load phase shift
pid_llc_light_load_duty_min	1638	Dmin = 0.4
pid_llc_light_load_duty_slope	1231	slope = 2.4
pid_llc_pid_preload	16353	P = 0.25

2.5 Soft start

The XDPP1148 uses a hybrid open/closed-loop soft-start approach for LLC and similar resonant topologies. As illustrated in Figure 10, a typical soft-start sequence is outlined below:

- Open-loop duty cycle ramp, frequency fixed at Fstart
- Open-loop frequency ramp, from Fstart to Fmax_clamp
- Programmable delay before closed-loop ramp, while Vout is measured to use as starting point
- Closed-loop ramp of Vout to final target voltage

Typically, the starting frequency Fstart is greater than or equal to the maximum frequency to ensure that Vout does not exceed the target voltage during open-loop ramp. The duration of the first two steps can be programmed by changing step size and step time registers.

For phase shift topology, the duty cycle ramp is effectively the phase shift ramp. If this is not desirable, the user can configure the duty start (Dstart) to be the same as Dmax.

After the open-loop frequency ramp, PID integrator is preloaded with a value that corresponds to Fmax_clamp. This value coincides with the transition point (P) as defined in Equation 1. Meanwhile, Vout is measured and used as pre-bias voltage for the next step. This pre-bias voltage varies with load conditions applied during open-loop ramp. Therefore, the ramp time can vary depending on the load. However, the slew rate can be defined by register **vc_llc_vramp_tstep**.

In this design, duty cycle ramp is from 19.995% (Dmin) to 99.976% (Dmax). The duty step (Dstep) is 0.122%, and step time (tstep,D) is 0.5 µs. The total duty cycle ramp time (t_{DR}) can be computed as:

$$t_{DR} = \frac{D_{\max} - D_{\min}}{D_{\text{step}}} \times t_{\text{step},D} = \frac{99.976\% - 19.995\%}{0.122\%} \times 0.5\ \mu s = 328\ \mu s$$

Equation 4

For frequency ramp, Fstart = 600 kHz, Fmax = 550 kHz, step time (tstep,F) = 3 µs. the step size is fixed to 1 LSB. The frequency ramp time (t_{FR}) is calculated as:

$$t_{FR} = \frac{F_{\text{start}} - F_{\max}}{F_{\min}} \times 256 \times t_{\text{step},F} = \frac{600 - 550}{200} \times 256 \times 3\ \mu s = 192\ \mu s$$

Equation 5

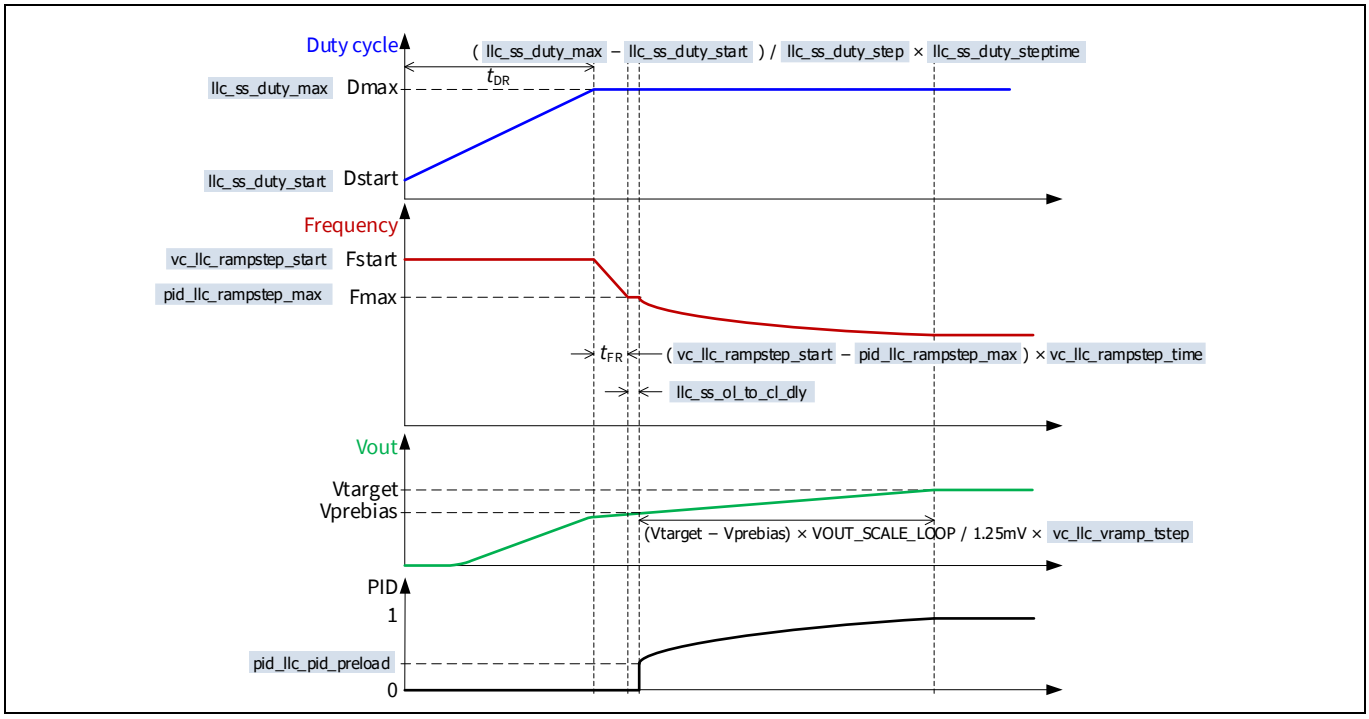


Figure 10 Soft start timing diagram

For the final closed-loop ramp, the desired voltage slew rate (dv/dt) is 5 mV/µs. The register **vc_llc_vramp_tstep** can be calculated as:

$$\text{vc\_llc\_vramp\_tstep} = \frac{62.5}{\frac{dv}{dt} \times \text{VOUT\_SCALE\_LOOP}} - 1 = \frac{62.5}{5 \times 0.0948} - 1 = 131$$

Equation 6

The configuration for soft start is shown in Table 7.

Table 7 Configuration for soft start

Register/PMBus command	Value	Comment
llc_ss_duty_max	4095	Dmax = 99.976%
llc_ss_duty_start	819	Dmin = 19.995%
llc_ss_duty_step	5	Dstep = 0.122%
llc_ss_duty_steptime	25	tstep,D = 0.5 µs
llc_ss_ol_to_cl_dly	8	5.12 µs delay
vc_llc_rampstep_start	768	Fstart = 3.0 × 200 = 600 kHz
vc_llc_rampstep_time	150	tstep,F = 3 µs
vc_llc_vramp_tstep	131	dv/dt = 5 mV/µs
VOUT_SCALE_LOOP	0.0948	–

2.6 Burst mode

For all topologies, burst mode can help improve light load efficiency. For LLC topologies with wide input voltage range, burst mode is also required for output voltage regulation. Once the switching frequency reaches Fmax, the controller enters burst mode.

Burst mode is enabled by setting the PMBus command POWER_MODE = 0x08. This mode is characterized by alternating intervals of burst ON and burst OFF periods. Upon entering burst mode, both the primary and secondary PWMs are disabled, marking the beginning of the burst OFF interval. During this interval, the output voltage gradually decreases due to the absence of energy transfer from the input to the output, resulting in a slow decline in output voltage.

The XDPP1148 controller continuously monitors the output voltage error, which is calculated as (Vtarget – Vsense). When the output voltage error exceeds the threshold defined by **pid_burst_mode_err_thr**, the burst ON interval is started. During this interval, the primary PWM is enabled, while the state of the secondary PWM is determined by the configuration of **llc_burst_sr_sel**. To maintain the tank capacitor voltage, the first and last PWM pulses of each even cycle are generated with a width that is half of the normal pulse width. To achieve precise timing, the register **llc_burst_half_pulse_dt_adj** needs to be manually set to match the primary rising edge dead-time value. For all other pulses, the duty cycle stays at 50%. The number of PWM pulses generated during each burst ON interval is defined by **pid_burst_reps**.

Upon completing the specified number of switching cycles, as defined by **pid_burst_reps**, the PWM signals are disabled, marking the end of the burst ON interval. The controller then enters the burst OFF interval, during which the output voltage is allowed to decrease. This decrease of output voltage eventually triggers the next burst ON interval, initiating a new cycle of PWM activity. This is illustrated in Figure 11.

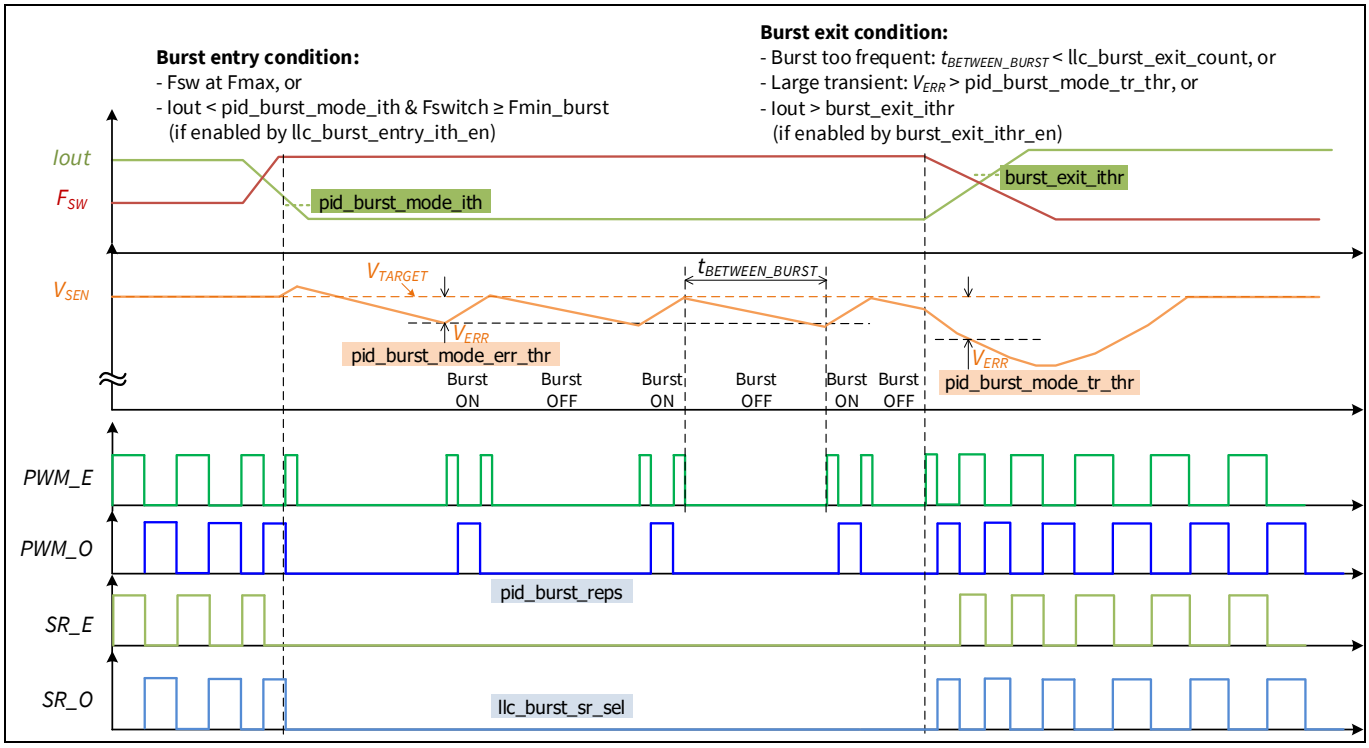


Figure 11 LLC burst mode typical waveforms

2.6.1 Burst entry and exit conditions

Burst entry condition:

- Switching frequency reaches Fmax (LLC topology only); or
- Output current is lower than threshold defined by **pid_burst_mode_ith** (enabled by setting **llc_burst_entry_ith_en** to 1) and switching frequency is above **llc_burst_ith_rampstep_min**; and
- Enough time has passed before last burst exit defined by **burst_mode_holdoff_time** (can be disabled by setting to 0)

Burst exit conditions:

- Burst OFF interval is below a threshold defined by **llc_burst_exit_count** (LLC topology only); or
- Output current is above threshold defined by **burst_exit_ithr** (recommend to disable for LLC topologies by setting **burst_exit_ithr_en** to 0); or
- Output voltage error is above a threshold defined by **pid_burst_mode_tr_thr** (LLC topology only)

As indicated in the parenthesis above, some entry and exit conditions are unique for LLC topologies. Additional consideration needs to be taken as below:

- The minimum switching frequency at which the controller is allowed to enter burst based on current threshold needs to be high enough to avoid high primary current. Typically, this frequency is at least resonant frequency.
- It is recommended to disable burst mode exit based on current threshold, because once exit, it will not enter burst again even if switching frequency reaches Fmax. This could result in output overvoltage.
- The exit condition based on output voltage error is used in case of high load transient that causes output voltage to drop quickly. Therefore, this transient threshold **pid_burst_mode_tr_thr** should be higher than the burst ON error threshold **pid_burst_mode_err_thr**.
- Small values for **pid_burst_reps** are recommended to avoid output overvoltage.

Under very light load conditions, the output voltage drops very slowly, resulting in an extended burst OFF interval. This prolonged period can cause the bootstrap capacitor for the gate driver to become excessively discharged. Consequently, the first few pulses in the next burst ON interval are utilized to charge the bootstrap capacitor, and high-side MOSFETs will remain in the off-state until the capacitor is recharged. To address this, the XDPP1148 introduces a mechanism to automatically increase the number of burst pulses based on the previous burst OFF time. For every interval defined by **burst_rep_inc_time**, the number of burst pulses is incremented by 1. The maximum increase of the number of pulses is defined by **burst_rep_inc_max**. Finally, a dedicated telemetry low pass filter index **tlm_kfp_iout_burst** is used for output current. This can be configured to a low value, therefore achieving good output current telemetry during burst mode.

2.6.2 Typical steps to configure LLC burst mode

1. Determine the maximum output voltage error Verr in burst mode. The valley of output voltage ripple is set by the register **pid_burst_mode_err_thr**, and the peak of output voltage ripple is determined by **pid_burst_reps**. For example, if the allowed minimum output voltage is 11.9 V, the error voltage Verr is 0.1 V.

$$\text{pid\_burst\_mode\_err\_thr} = V_{err} \times \text{VOUT\_SCALE\_LOOP}/1.25\,\text{mV} = 0.1\,\text{V} \times 0.1/1.25\,\text{mV} = 8$$

Equation 7

2. Determine the peak output voltage in burst mode. This is set by **pid_burst_reps**. This can be fine-tuned by simulation or lab measurement. Typically, a small value for **pid_burst_reps** yields good results. Too large value could cause too much energy being delivered to the output capacitors, resulting in overvoltage conditions. For this design, **pid_burst_reps** is set to 2 (3 burst cycles).
3. Determine the burst entry condition. If current based entry is enabled, it is also necessary to determine the minimum switching frequency for burst entry. This should be above the resonant frequency and set by **llc_burst_ith_rampstep_min**. Another burst entry condition is defined by **burst_mode_holdoff_time**. It is recommended to use 0 or other low values to avoid output overvoltage.
4. Determine the burst exit condition. For LLC topology with wide input voltage range, it is recommended to disable burst exit based on current threshold to guarantee output voltage regulation. Another burst exit condition can be triggered when a new burst is requested within a time duration defined by **llc_burst_exit_count**. This can be fine-tuned through laboratory measurement. A higher value for **llc_burst_exit_count** makes it easier to exit burst mode.
5. Configure the auto increase of burst cycles. Depending on the gate driver and MOSFET selections, this can be estimated or determined from waveform measurement. Typically, if **pid_burst_reps** is very low, for example, 0 or 1, enabling auto increase can help improve performance.

The configuration of burst mode for this design is shown in Table 8.

Table 8 Configuration for burst mode

Register/PMBus command	Value	Comment
POWER_MODE	0x08	Enable burst mode
pid_burst_mode_err_thr	8	Error voltage at VSEN. Set to 10 mV
llc_burst_entry_ith_en	0	Disable burst entry based on current
llc_burst_ith_rampstep_min	640	Minimum frequency for burst entry based on current. Set to 500 kHz
pid_burst_mode_ith	0	Burst mode entry current threshold
burst_mode_holdoff_time	0	No burst hold off time
pid_burst_reps	2	Number of cycles in each burst. Set to 3
burst_rep_inc_time	137	Auto increase of burst cycles by 1 every 701 µs
burst_rep_inc_max	3	Maximum increase to the burst cycle. Set to 3
llc_burst_exit_count	5	Exit burst if a new burst is required before this time. Set to 25 ns
burst_exit_ithr_en	0	Disable burst exit based on current threshold (Recommended for LLC)
burst_exit_ithr	0	Burst mode exit current threshold
pid_burst_mode_tr_thr	31	Transient error voltage to exit burst mode. Set to 38.75 mV
llc_burst_half_pulse_dt_adj	72	Primary PWM rising edge dead time. Set to same value defined in PWM_DEADTIME
llc_burst_sr_sel	1	During burst, SRs are on when primary PWMs are on

2.7 SR timing control

2.7.1 Fixed SR timing

In an LLC converter, the turn-off timing of SRs differs between above and below resonance operations. The XDPP1148 introduces a new timing marker, t3, which is used to define the SR PWM turn-off point. For above resonance operation, the SR is turned off simultaneously with the primary switch. For below resonance operation, the SR should be turned off when its current resonates back to 0, which ideally occurs at half resonant period. The ideal resonant period is defined by register **llc_tres**, and is used to compute t3:

$$t3 = llc\_tres/2 + llc\_tdtprim\_plus\_tiso - toff\_dly\_t3$$

Equation 8

Register **llc_tdtprim_plus_tiso** accounts for the primary dead time and isolator delay. In addition, **toff_dly_t3** defines how much earlier SR should turn off before its zero-current crossing, as shown in Figure 12. Turning off SR earlier is a popular approach to make sure that there is no circulating current.

When **sr_timing_mode** is set to 0, the XDPP1148 operates in fixed timing mode, where t3 is fixed for all below resonance conditions.

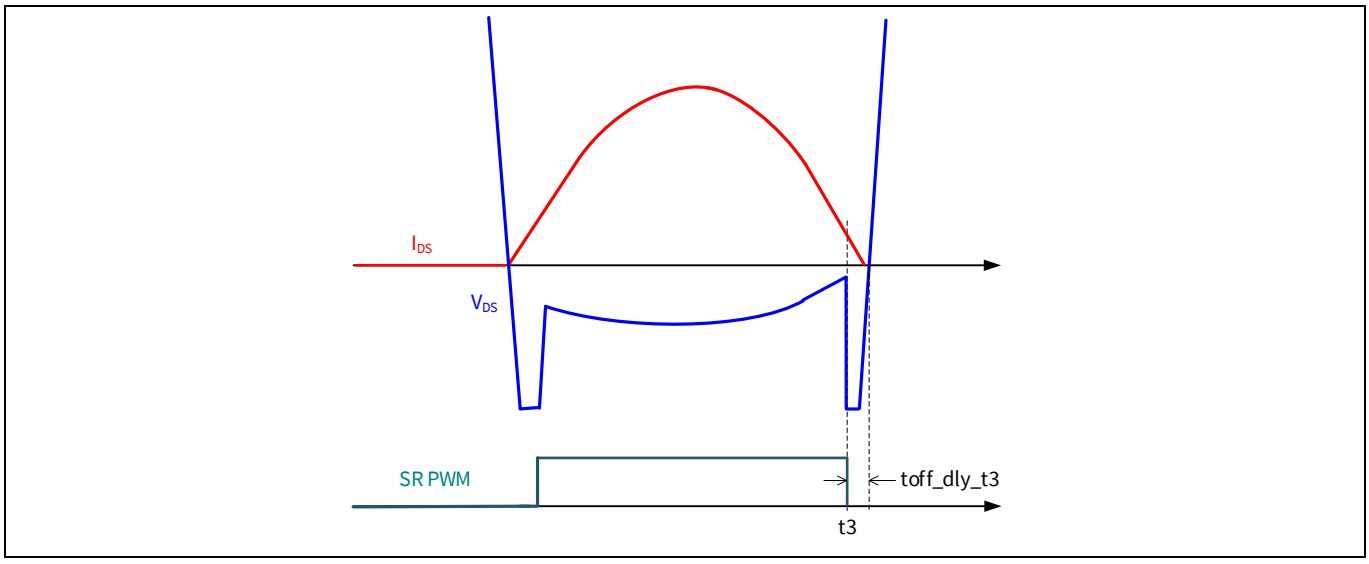


Figure 12 SR turn-off defined by t3 for below resonance

2.7.2 Adaptive SR timing

The XDPP1148 also supports adaptive SR timing. In this case, t3 is changed to:

$$t3 = llc\_tres\_auto/2 + llc\_tdtprim\_plus\_tiso - toff\_dly\_t3$$

Equation 9

Register **llc_tres_auto** is the internally adjusted resonant period according to real time V_{DS} waveform measurement, using an external V_{DS} sense circuit. Such adjustment is made continuously until optimum timing is achieved.

2.7.2.1 V_{DS} sense

An example V_{DS} sense circuit is shown in Figure 13. Using the MOSFET and the resistors R1 and R2, V_{DS} is clamped and level shifted, as shown in Figure 14. A threshold can be set by R3 and R4. Ideally, this threshold is set so that the output of the comparator (labeled as Vds_comp) has two pulses corresponding to the two MOSFET body diode conduction intervals. This signal needs to be connected to one of the fast GPI inputs of the XDPP1148. Registers **sr_timing_trig_sel** and **ext_fast_pwm_en** should then be set accordingly. A list of all available pins is given in Table 9.

Depending on which cycle (odd/even) V_{DS} sense is applied, register **sr_timing_cycle_sel** also needs to be configured.

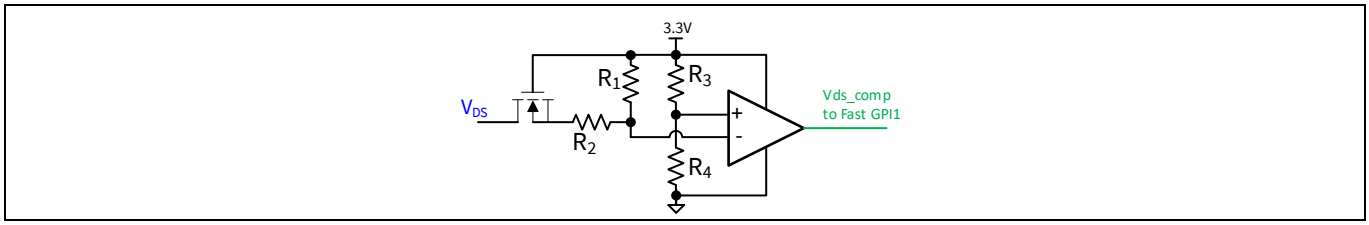


Figure 13 Example V_{DS} sense circuit

Table 9 Fast GPI input pins and register settings for V_{DS} sense

Pin name	Function	sr_timing_trig_sel	ext_fast_pwm_en
SYNC, PWM1, PWM3, PWM5	FAST_GPI1	0	1
IMON, PWM2, PWM4, PWM6	FAST_GPI2	1	2

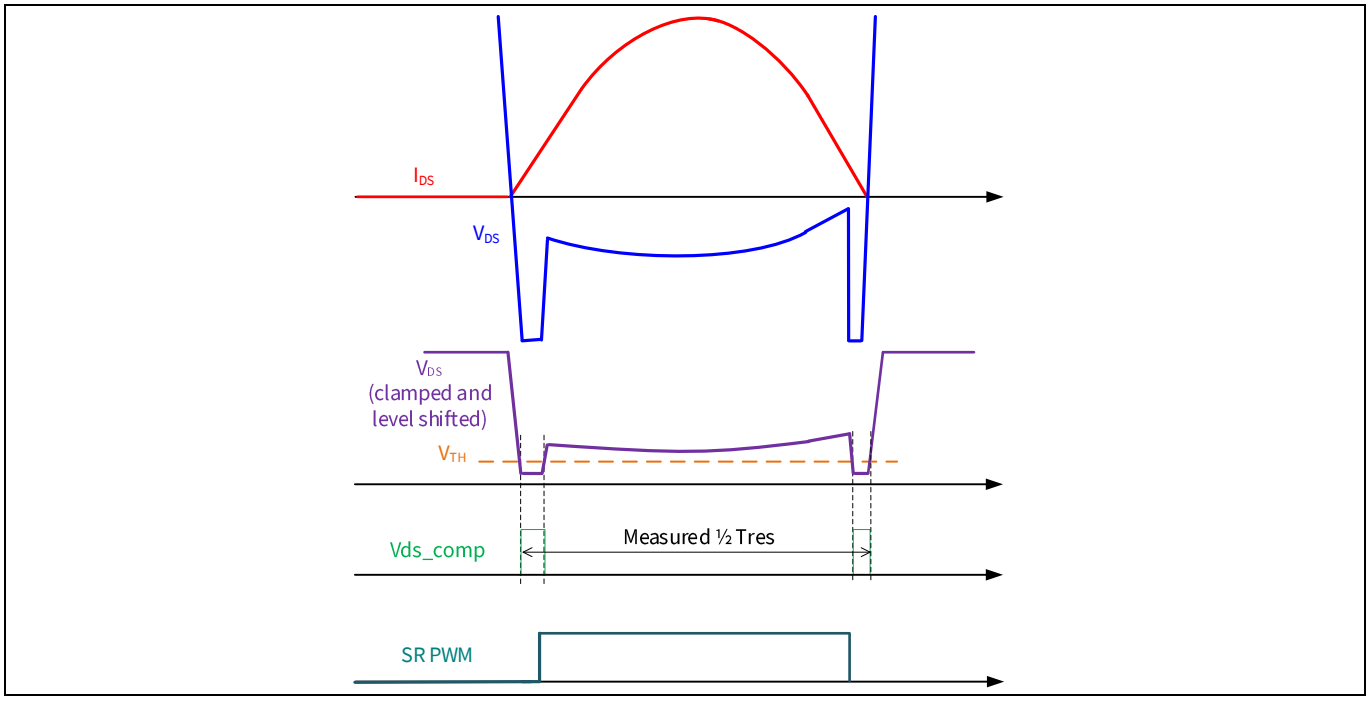


Figure 14 Ideal waveforms of external V_{DS} sense circuit

2.7.2.2 Adaptive timing modes

In XDPP1148 digital power controller, there are four basic adaptive timing modes (1 to 4), and three additional modes based on mode 2 (5 to 7). This is selected by the register **sr_timing_mode**. The measured quantity used for adaptive timing is summarized in Table 10. Relevant waveforms are also illustrated in Figure 15. The measurement result is stored in the result register, **sr_meas1** to **sr_meas4**, depending on the mode, and compared to the corresponding target.

This measurement and comparison are made every switching cycle. If the consecutive number of comparisons in the same direction exceeds a defined value (register **sr_timing_cnt_max**), the internally adjusted resonant period (**llc_tres_auto**) is incremented or decremented by 1 LSB (5 ns). Optimum timing is achieved when no adjustment is needed. That is, the measurement matches the target value.

If Vds_comp pulses are missing or have incorrect timing, measurement is canceled and no adjustment is made. This could happen due to noise near switching transitions. As illustrated in Figure 15, to achieve correct timing measurement, the rising edge of the first Vds_comp pulse must occur after t1. In addition, the falling edge of the last Vds_comp pulse must occur after t3 and before the subsequent t1. Here, t1 is the internal timing marker that indicates the beginning of each switching cycle. The rising edge of primary switch gate signal occurs after t1 with additional dead-time, isolation and gate driver delay. As shown in Figure 15, the t1 position precedes the actual switching waveform. In some cases, with long deadtimes and isolation gate driver delay, the falling edge of Vds_comp can occur after the subsequent t1. Mode 5 to 7 are designed for such cases, where additional delay of 50ns to 200ns can be applied after the subsequent t1 before canceling the measurement.

For example, when using mode 2 (or 5 to 7), the target for **sr_meas2** is ½ Tres. The Tres in adaptive SR timing is set by the **llc_tres_auto** register. According to Figure 14 and Figure 15, sr_meas2 is determined by the half resonant period of the actual circuit. The controller makes adjustment to **llc_tres_auto** until **sr_meas2** is equal to ½ Tres.

Another example is using mode 3. The target for **sr_meas3** is **toff_dly_t3**. The controller makes adjustment to **llc_tres_auto** until **sr_meas3** is equal to **toff_dly_t3**.

Table 10 SR timing modes

Mode	Description	Result register	Target
0	Fixed timing	–	–
1	t1 to first Vds_comp falling edge after t3	sr_meas1	½ Tres (llc_tres_auto) + tdtprim_plus_tiso + internal delay
2	First Vds_comp rising edge after t1 to first Vds_comp falling edge after t3	sr_meas2	½ Tres (llc_tres_auto)
3	First Vds_comp rising edge after t3 to first Vds_comp falling edge after t3	sr_meas3	toff_dly_t3
4	t3 to first Vds_comp falling edge after t3	sr_meas4	toff_dly_t3
5	Mode 2 above with additional 50ns delay applied to subsequent t1 before canceling measurement	sr_meas2	½ Tres (llc_tres_auto)
6	Mode 2 above with additional 100ns delay applied to subsequent t1 before canceling measurement	sr_meas2	½ Tres (llc_tres_auto)
7	Mode 2 above with additional 200ns delay applied to subsequent t1 before canceling measurement	sr_meas2	½ Tres (llc_tres_auto)

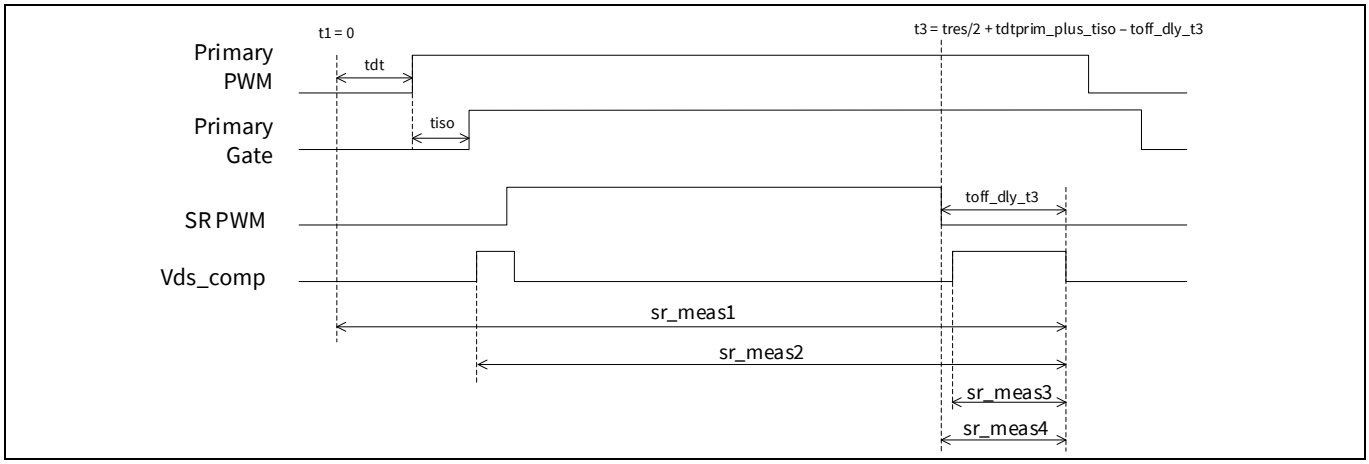


Figure 15 Adaptive SR timing measurement results

Due to switching noise and non-ideal comparator threshold settings, the Vds_comp signal can exhibit different shapes and pulse counts. Despite these variations, the critical edges for timing measurement can still be identified. For mode 1 and 2, the critical edges are the rising edge after t1, and the falling edge after t3. Notably, the presence or absence of additional pulses between these two edges does not impact the measurement. Other acceptable Vds_comp waveform examples for mode 1 and 2 are shown in Figure 16.

For mode 3 and 4, the timing measurement is based on a single pulse in the Vds_comp signal, which is defined by two critical edges: the rising edge after t3, and the falling edge also after t3. The absence of the rising edge after t1 does not affect the measurement. Therefore, it is possible to use small rising-edge dead times to minimize the body diode conduction before SR is turned on. The acceptable Vds_comp waveform example for mode 3 and 4 is shown in Figure 17.

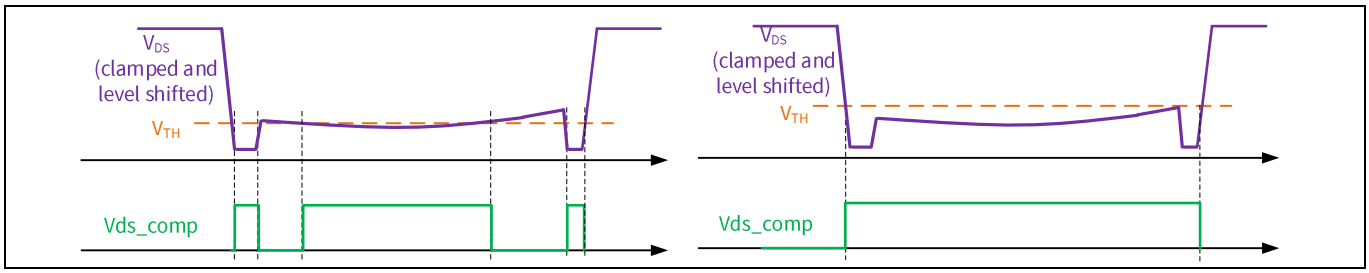


Figure 16 Other acceptable Vds_comp signals for mode 1 and 2 (5 to 7)

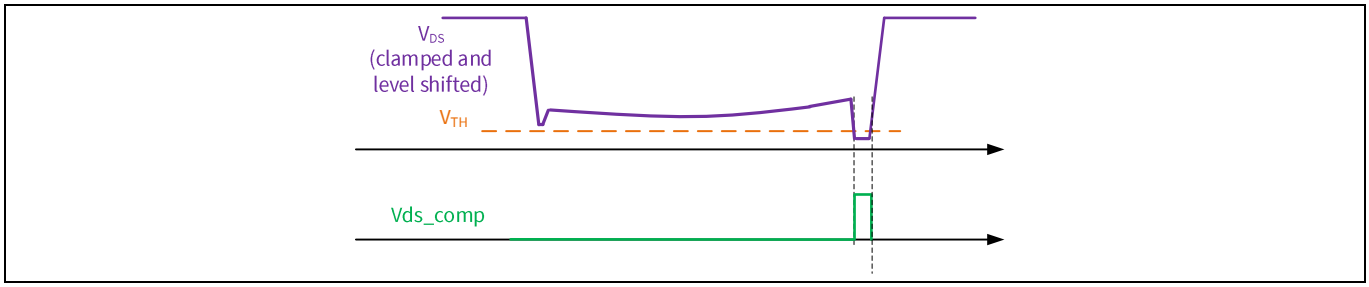


Figure 17 Other acceptable Vds_comp signal for mode 3 and 4

2.7.2.3 Adaptive timing conditions and limits

Adaptive SR timing is typically desired only for operation below resonance. To control when timing adjustments are allowed, three options are available, configured through the **llc_auto_sr_tsw_range** register. The current switching period, Tswitch, is used to determine these conditions:

Option 1: Tswitch > llc_tres_max – most restrictive condition

Adjustment is only allowed when the current switching period (Tswitch) is above the maximum defined resonant period (**llc_tres_max**). This is the most restrictive condition, ensuring that adjustments are only made when the system is operating well below resonance.

Option 2: Tswitch > max(llc_tres_auto, llc_tres)

Adjustment is allowed when current switching period (Tswitch) is above the measured resonant period (**llc_tres_auto**), but no lower than the ideal resonant period defined by **llc_tres**.

Option 3: Tswitch > llc_tres_auto – least restrictive condition

Adjustment is allowed when current switching period (Tswitch) is above the measured resonant period, but no lower than minimum resonant period defined by **llc_tres_min**.

The maximum and minimum limits for **llc_tres_auto** can be set using the **llc_tres_max** and **llc_tres_min** registers, respectively. The adjustment is also disabled during soft start, shutdown and in DE mode.

The configuration example of adaptive SR timing mode 5 is listed in Table 11.

Table 11 Configuration example for adaptive SR timing mode 5

Register	Value	Comment
llc_tdtprim_plus_tiso	96	120ns primary dead time plus the isolation delay
toff_dly_t3	14	SR turns off 70ns before zero-current crossing
sr_timing_mode	5	Mode 2 with additional 50ns delay
sr_timing_ramp_sel	0	Ramp 0
sr_timing_cycle_sel	1	Odd cycle
sr_timing_trig_sel	0	External trigger 1 (Fast GPI1)
sync_func	6	Sync pin function is FAST_GPI1
ext_fast_pwm_en	1	Fast GPI1 enabled
sr_timing_cnt_max	5	5 consecutive comparisons before adjustment
llc_tres	592	2.96µs ideal resonant period
llc_tres_max	624	3.12µs maximum resonant period
llc_tres_min	560	2.8µs minimum resonant period
llc_auto_sr_tsw_range	1	Tswitch > max(llc_tres_auto, llc_tres)

3 Experimental verification

An image of the test setup is shown in Figure 18.

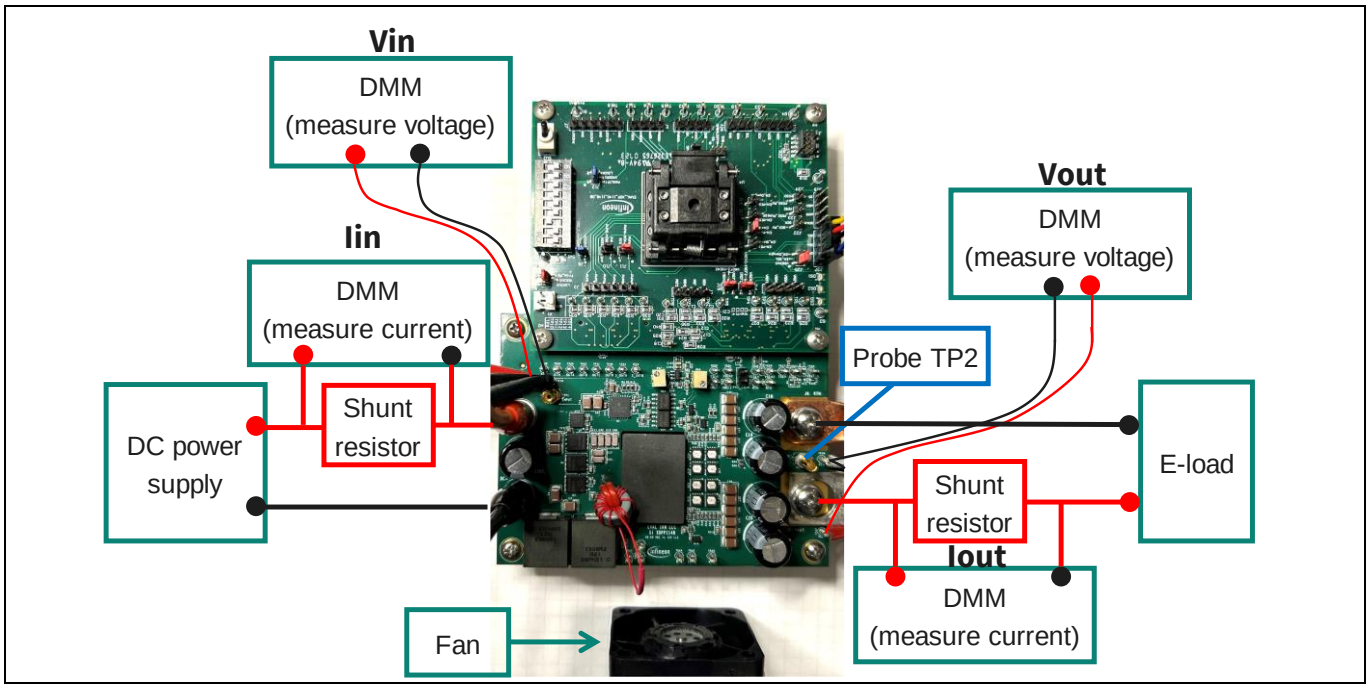


Figure 18 Test setup diagram: Evaluation board, controller board, power supply, and load connections

Necessary connections to operate the board:

- Connect the controller board to the evaluation board
- Connect the DC power supply (44 V to 60 V) to input connectors J3 (DC+) and J4 (DC-) with banana plugs
- Connect the electronic load to output connectors J5 (Vout) and J6 (RTN) with screw terminals
- A fan placed about 1 cm from the bottom edge of the board supplying about 3 m/s airflow

The following jumpers on the controller boards needs to be installed:

- J28 – select 3.3 V from power board
- J8 – provide 3.3 V to XDPP1148-100B controller
- J15 and J16 – select ISEN2 and IREF2
- J10 and J11 – select PWM5 and PWM6

Optional connections for measurement:

- Input voltage measurement DMM to TP36 (DC+) and TP39 (DC-)
- Output voltage measurement DMM to TP37 (Vout) and TP38 (RTN)
- Input and output current measurement using shut resistors
- Oscilloscope probe to probe adaptor jack TP2 for output voltage ripple measurement

3.1 Regulation and telemetry

3.1.1 Line and load regulation

Figure 19 shows the measured output voltage error. At minimum input voltage of 44 V, the converter reaches its minimum frequency at high current. Therefore, the output voltage starts to drop below 11.88 V (1% error) when the output current exceeds 30 A. When the input voltage is above approximately 52 V, at no load, the converter starts operating in burst mode. As the load current increases, the converter exits burst mode. For example, at an input voltage of 54 V, burst mode occurs for output current ranging from 0 A to 30 A. In burst mode, the output voltage error is higher than normal operation, but still remains within ±1%.

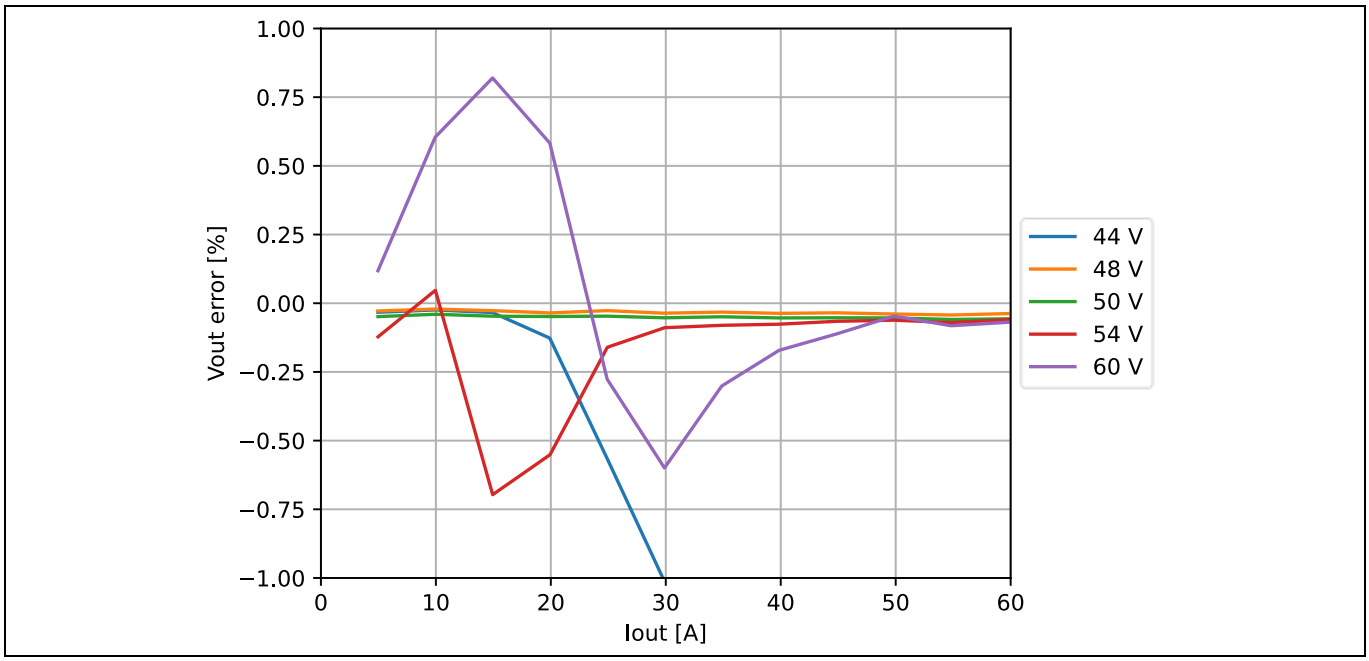


Figure 19 Line and load regulation

The boundary of the burst mode can be determined by observing the output voltage error and operation waveforms. For this design, the approximate burst mode boundary is shown in Figure 20. This can be used later to determine whether the converter is in burst mode for any given input voltage and output current combination.

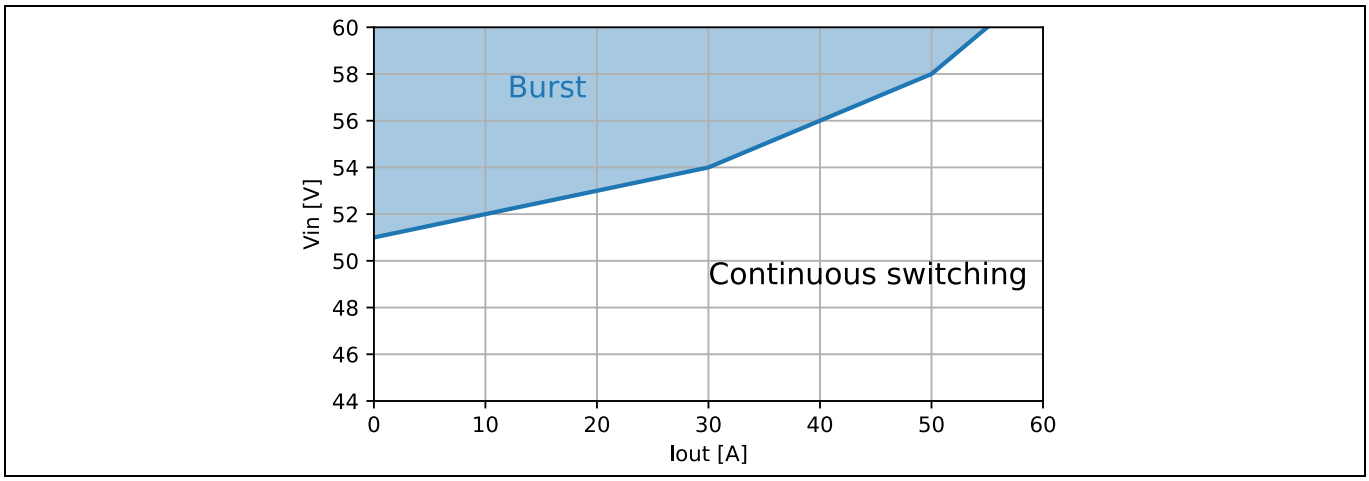


Figure 20 Approximate burst mode boundary

3.1.2 Voltage and current telemetry

Output voltage, output current, and input current telemetry results are compared to the multimeter readings at 48 V input. The errors are plotted in Figure 21, Figure 22 and Figure 23, for a load range from 0 A to 60 A. The output voltage telemetry accuracy is within 0.1%. The accuracy for current telemetry is within 1% in most conditions. The effect of temperature compensation on the output current telemetry is also shown in Figure 22, where it is evident that the error is larger at high output current without temperature compensation.

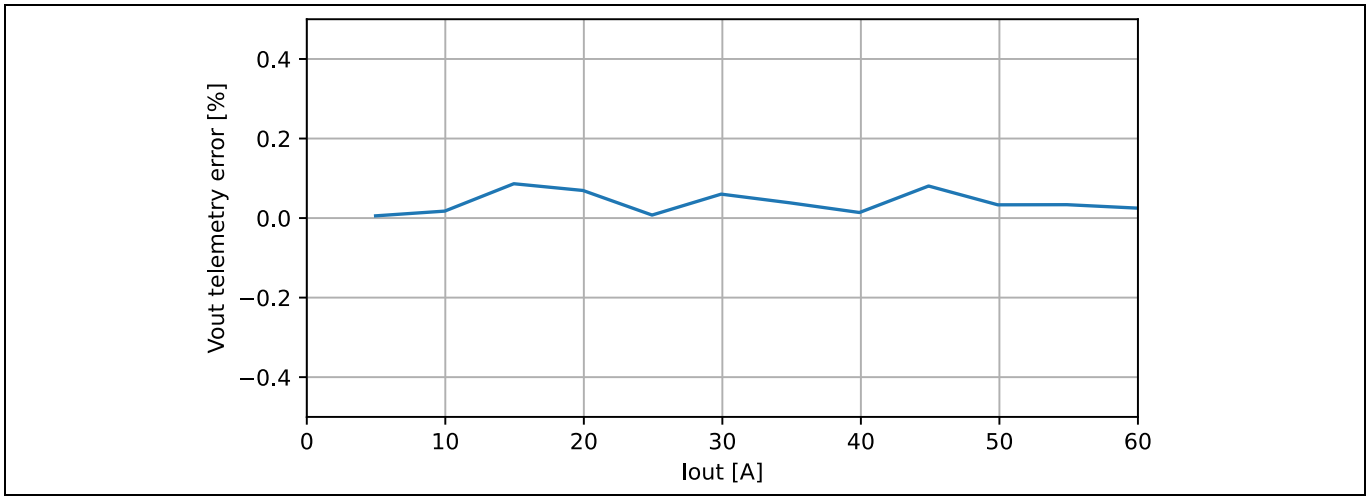


Figure 21 Output voltage telemetry accuracy at 48 V input

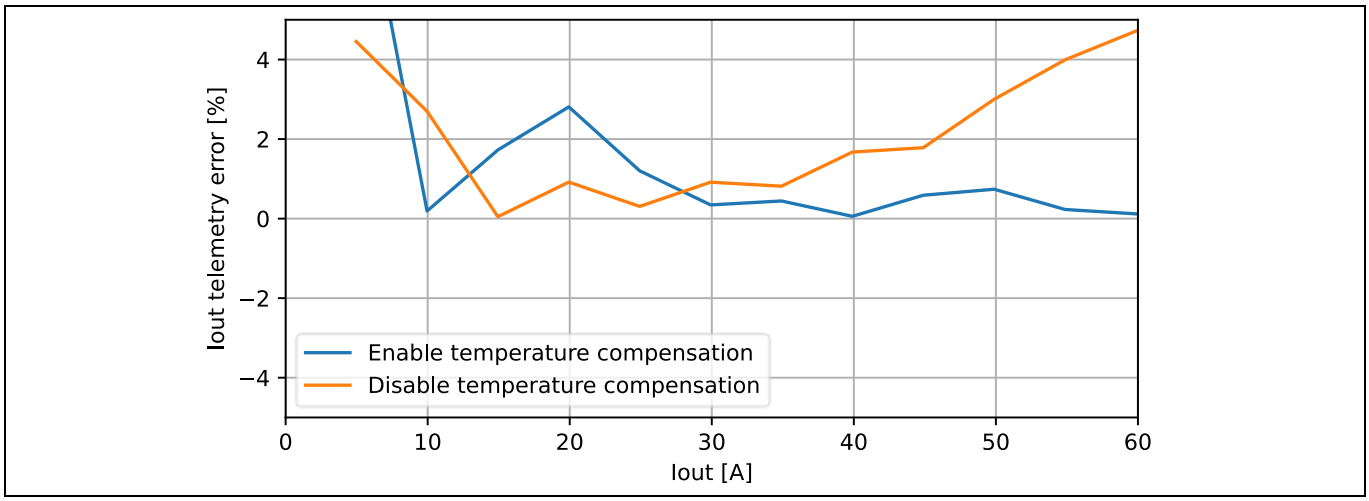


Figure 22 Output current telemetry accuracy at 48 V input

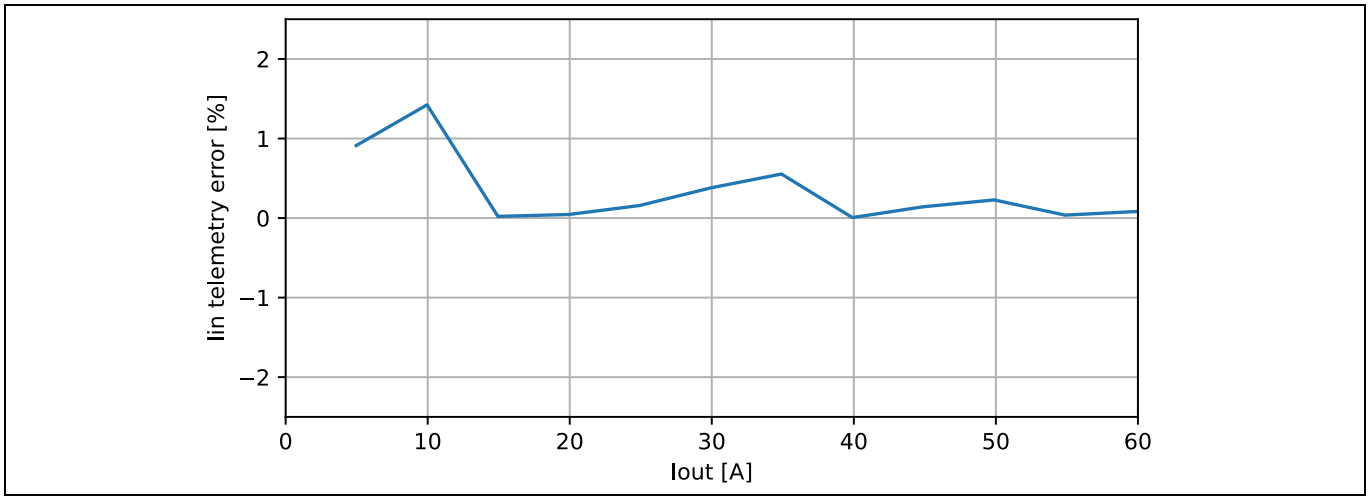


Figure 23 Input current telemetry accuracy at 48 V input

3.1.3 Efficiency

Efficiency is measured at different input voltages, regulating at 12 V output, for the output current range from 0 A to 60 A (Figure 24). The losses of the auxiliary supplies are also included. The dwell time for each measurement is 5 seconds, not thermal steady-state. For input voltages between 44 V and 50 V, the converter is operating in continuous switching mode. For 54 V and 60 V input, the converter is operating in burst mode at low current. As a result, the loss at 0 A is significantly lower for 54 V and 60 V input voltages. However, the loss increases rapidly when output current is above 10 A. This is due to above resonant operation and the secondary MOSFETs are turned off at high current.

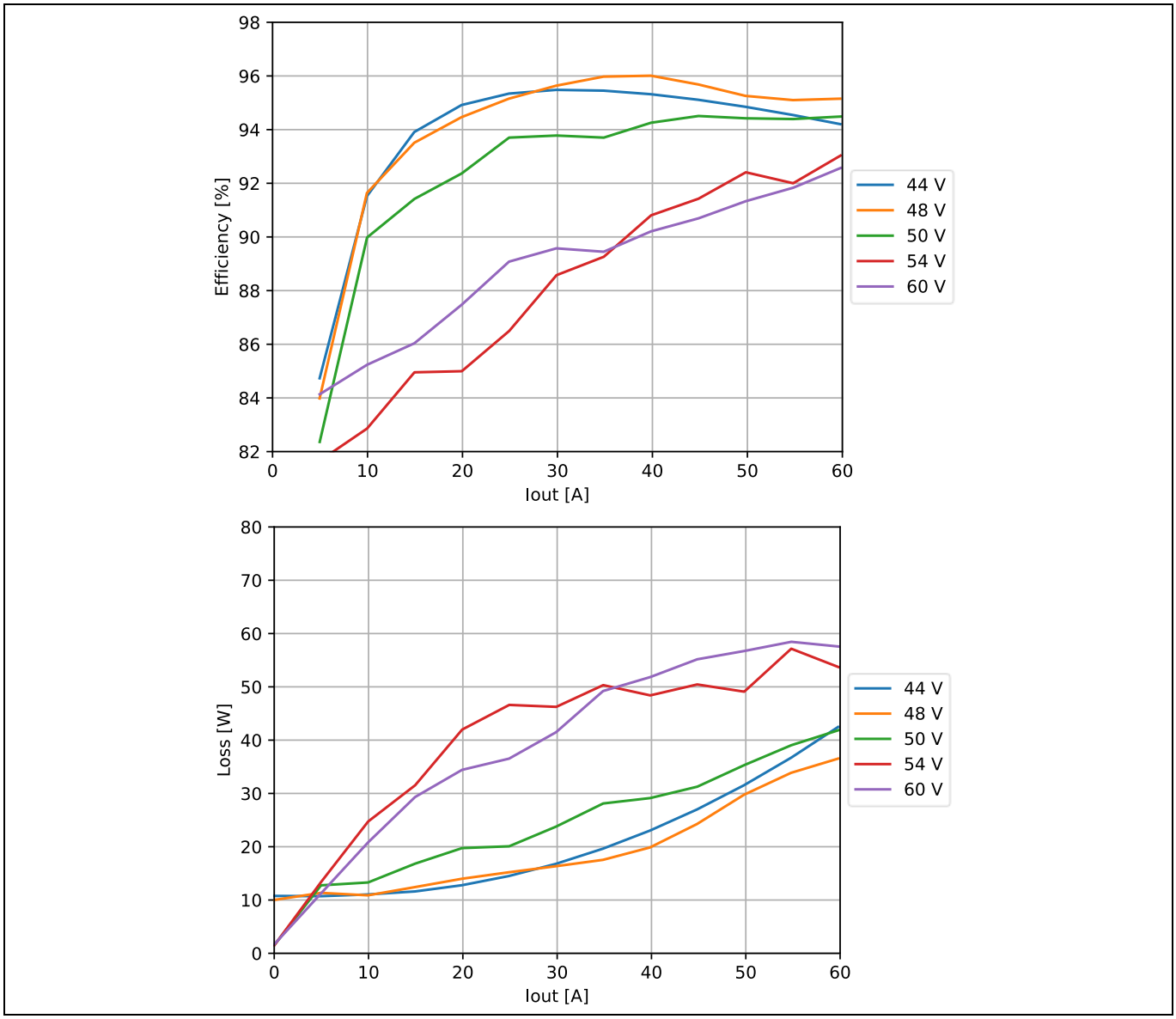


Figure 24 Measured efficiency and loss at different input voltages

3.1.4 Thermal performance

The thermal images at different input voltages and 60 A full load, with 400 LFM airflow, are shown in Figure 25, Figure 26, and Figure 27. The areas with the highest temperature are the planner PCB windings and near

secondary MOSFETs. At 48 V input, the switching frequency is closest to the resonant frequency, resulting in the lowest temperature. At 60 V input, the resonant inductors (located at the lower left corner) are also heating up.

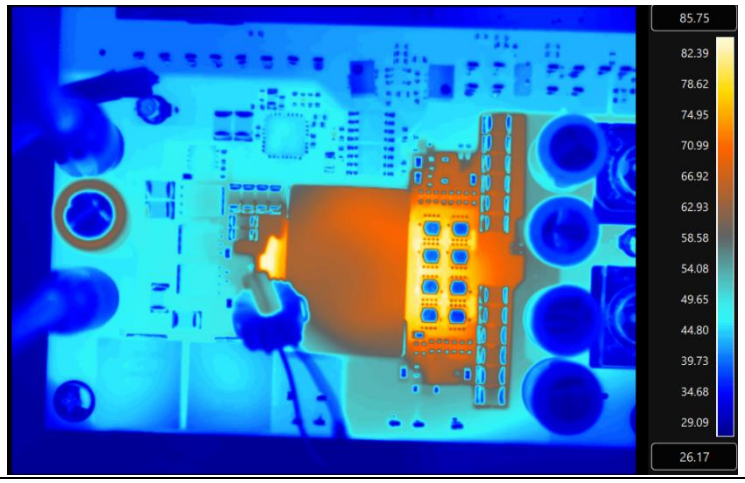


Figure 25 Thermal image for 48 V input, 60 A load

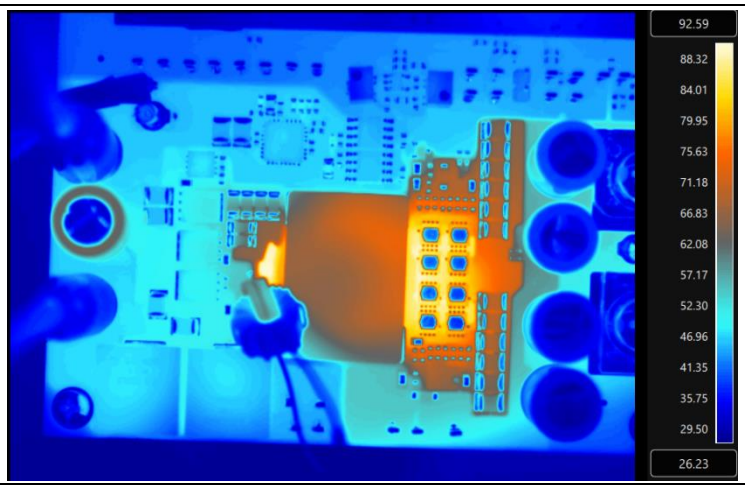


Figure 26 Thermal image for 44 V input, 60 A load

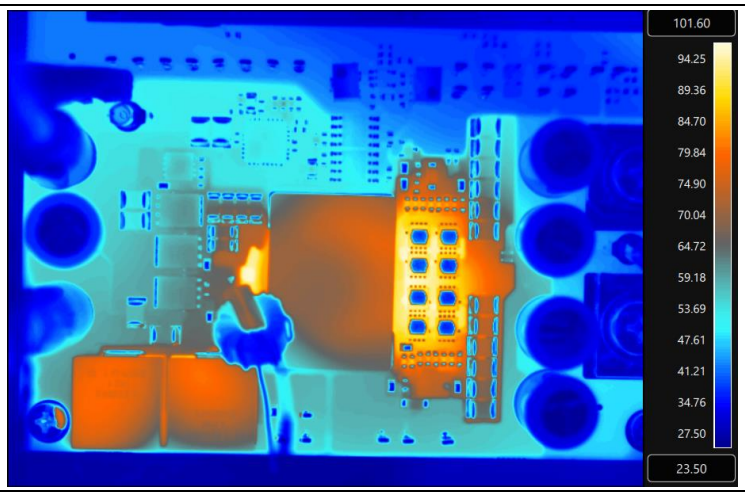


Figure 27 Thermal image for 60 V input, 60 A load

3.2 Operation waveforms

3.2.1 Steady-state waveforms

The steady-state waveforms are shown in Figure 28 at 48 V input, using SR fixed timing mode. The primary current is measured using a 15:1 current transformer.

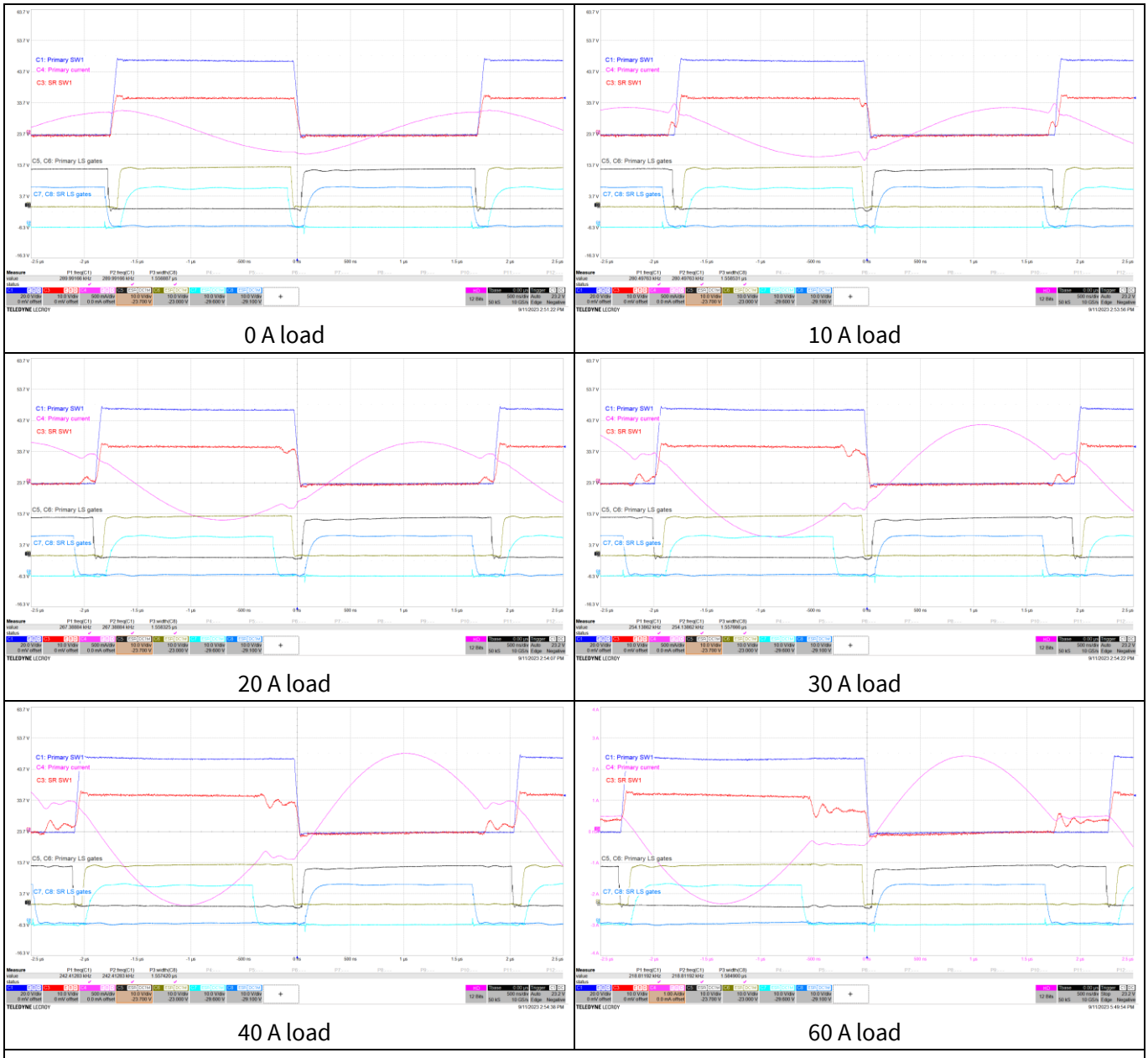
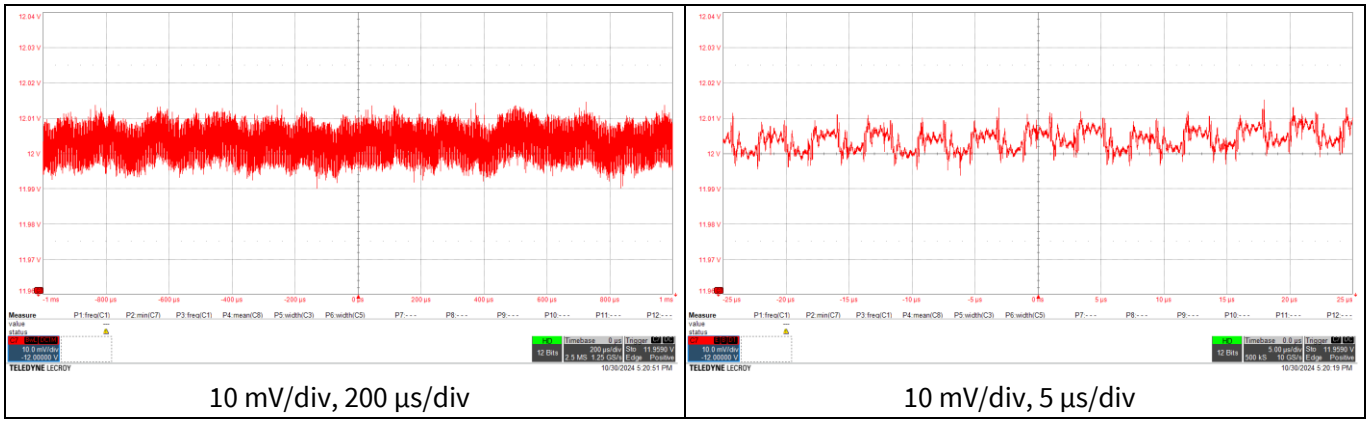


Figure 28 Steady-state waveforms at 48 V input

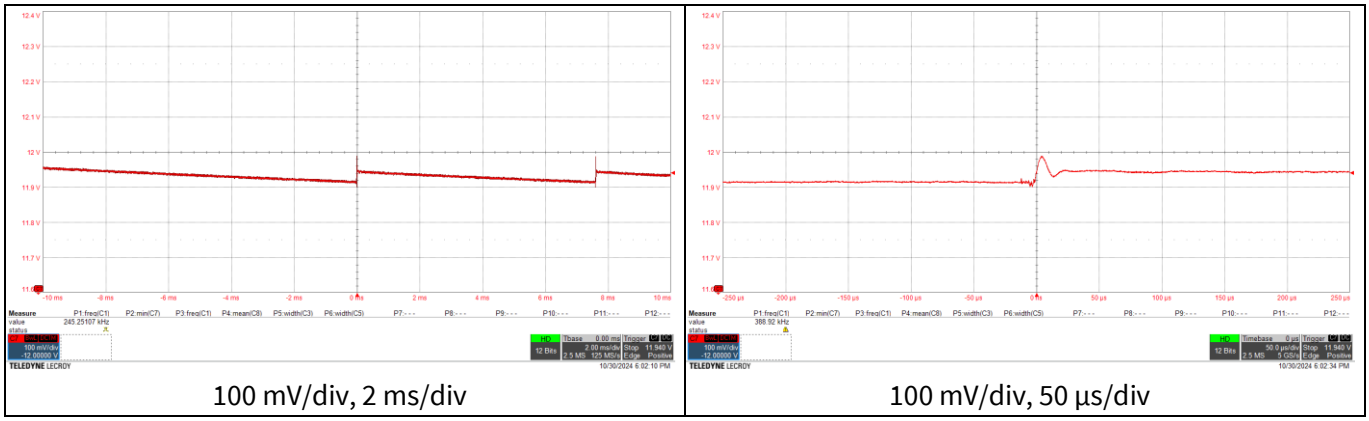
3.2.2 Output voltage ripple

The output voltage ripple was measured at the test point TP2, with 20 MHz probe bandwidth. At 48 V input, the switching frequency is close to the resonant frequency and the output voltage ripple is less than 20 mVpp, as shown in Figure 29. In burst mode, the minimum output voltage that triggers a burst on interval is 100 mV. For example, at 52 V and no load, the output voltage ripple is 100 mVpp. Depending on the input voltage and load current combination, the output voltage ripple can have different shapes, as shown in Figure 30 and Figure 31.



10 mV/div, 200 µs/div | 10 mV/div, 5 µs/div

Figure 29 Output voltage ripple at 48 V input, 60 A load (normal operation)



100 mV/div, 2 ms/div | 100 mV/div, 50 µs/div

Figure 30 Output voltage ripple at 52 V input, 0 A load (light load burst mode)

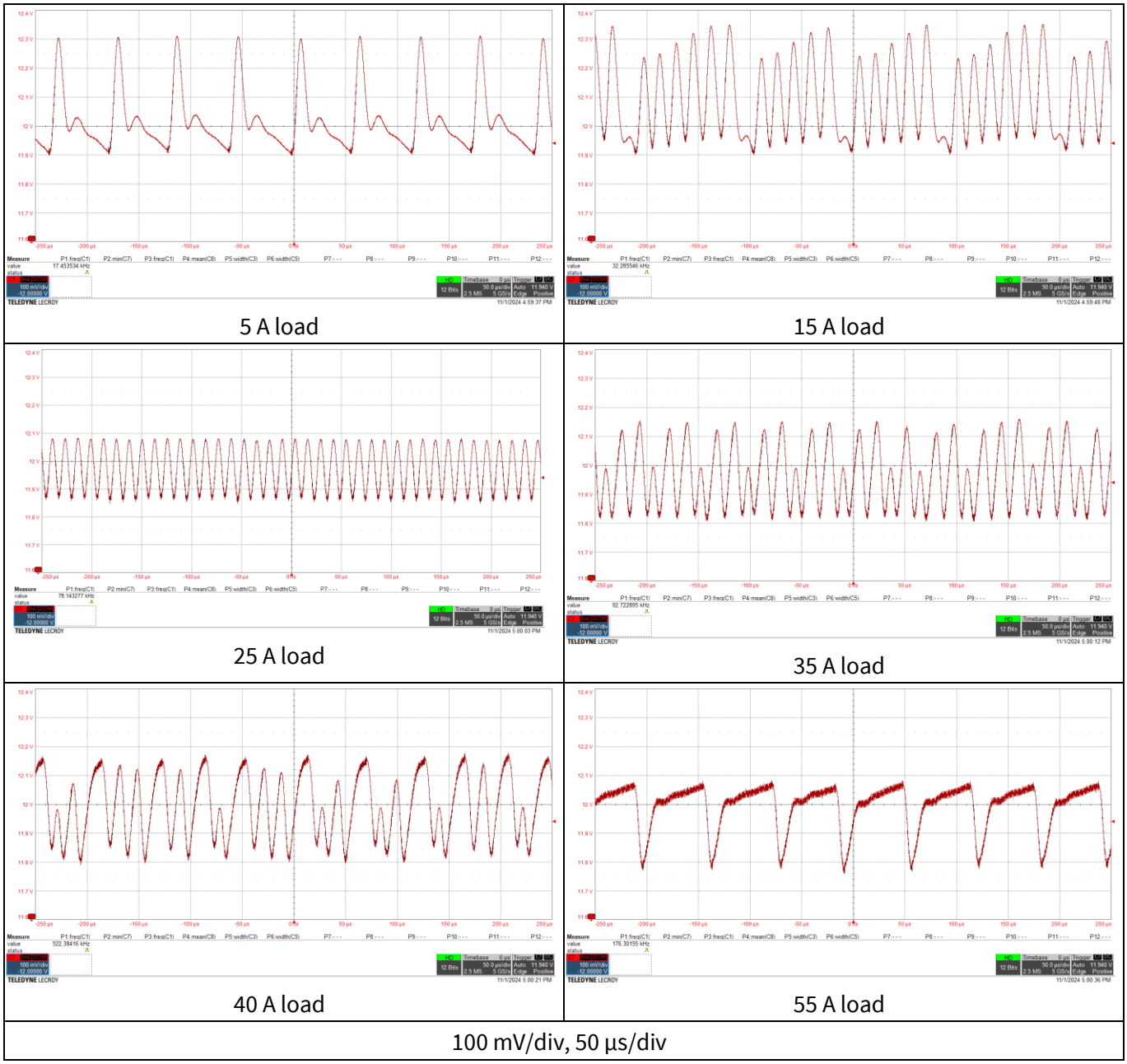


Figure 31 Output voltage ripple at 60 V input, 5 A to 55 A load (different load with burst mode)

3.2.3 Soft start

Figure 32 shows the startup waveforms captured at 48 V input, 0, 50, and 100 percent load. The pre-bias startup at 0 percent load is also shown. From the configuration given in Table 7, the duty cycle ramp time is 328 µs and the frequency ramp time is 192 µs. The final output voltage ramp slew rate is set to 5 mV/µs, which can be observed most clearly at 100% (60 A) load.

The peak primary inrush current during startup is about 1.5 times the full load primary current. With pre-bias, the peak inrush current is lower.

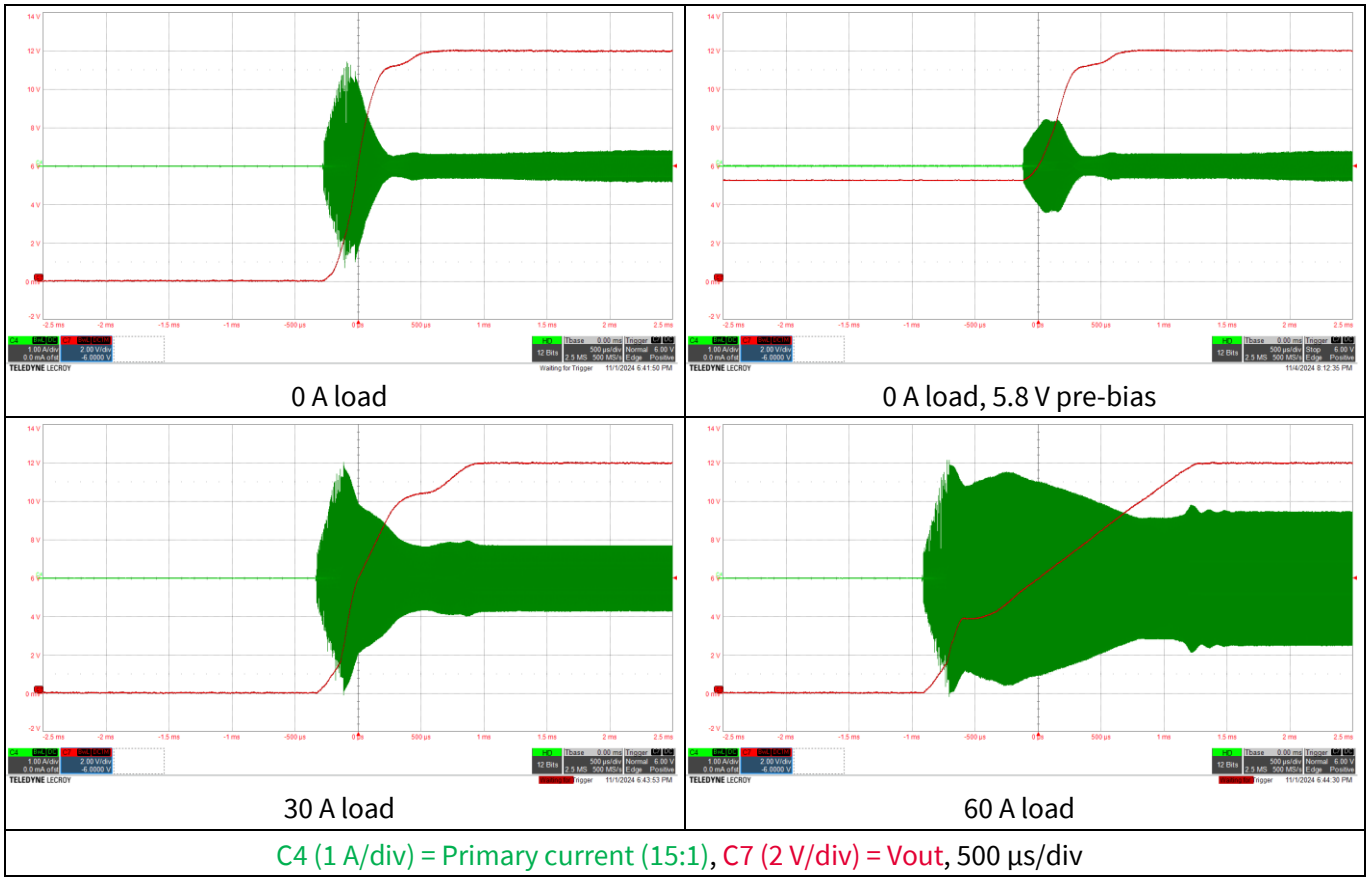


Figure 32 Startup waveforms at 48 V input

With the current configuration, at high input voltages, the converter cannot startup at no load as it cannot enter burst mode during the duty cycle ramp and frequency ramp. This can cause overvoltage at the output. If desired, it is possible to shorten or disabled frequency ramp to allow for faster burst mode entry.

The startup waveforms at 60 V input, 30 A and 50 A load are shown in Figure 33. The converter enters burst mode at the end of frequency ramp at 30 A. At 50 A, there is also a final output voltage ramp after the frequency ramp, before entering burst mode. In addition, the peak primary inrush current is about 2 times the full load current.

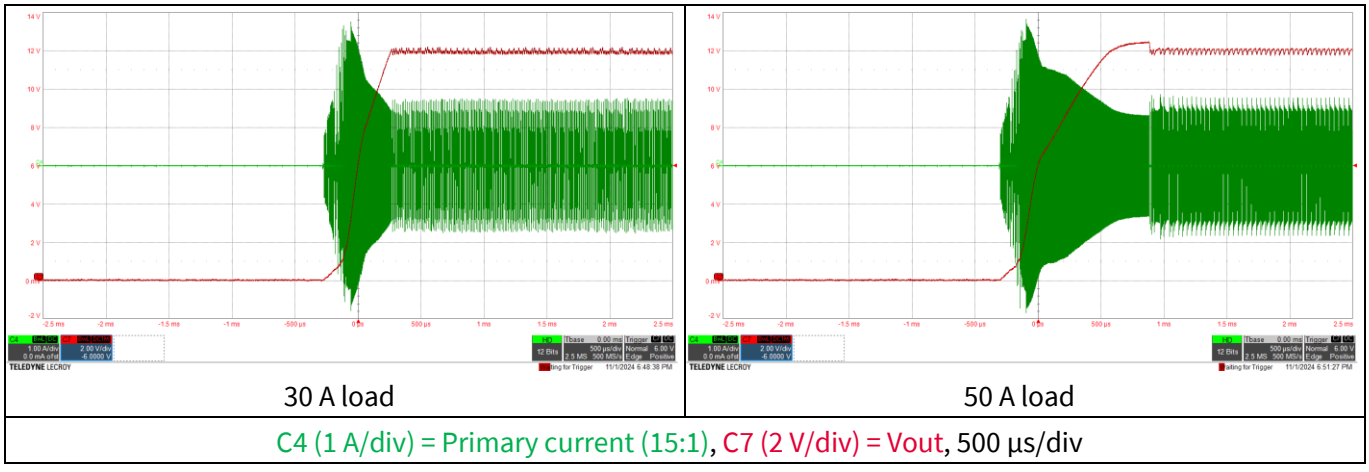
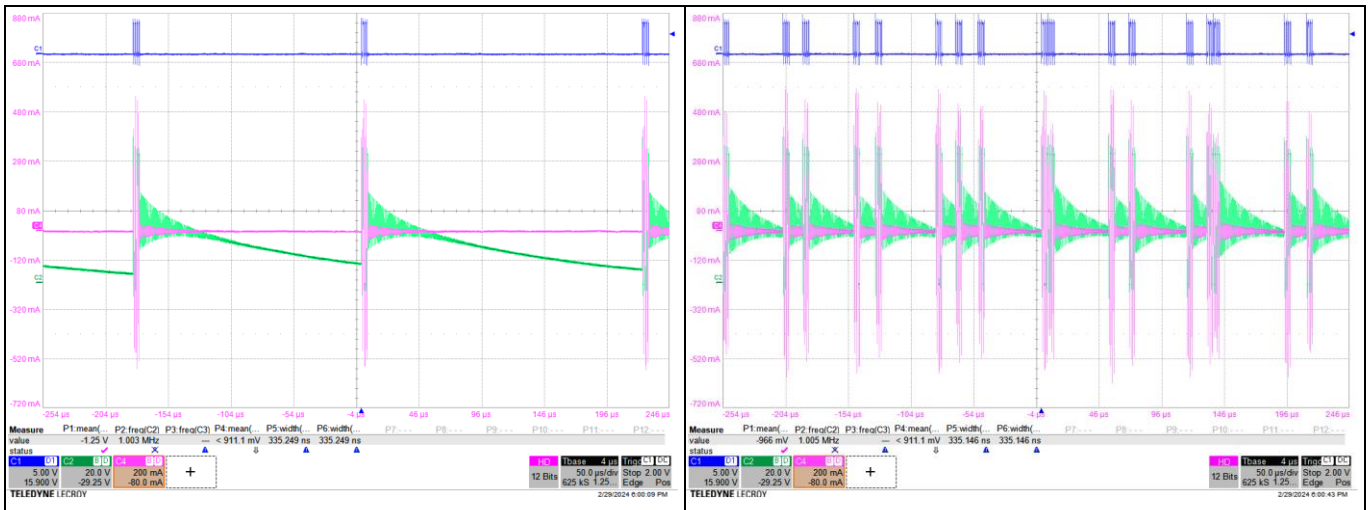


Figure 33 Startup waveforms at 60 V input

3.2.4 Burst mode

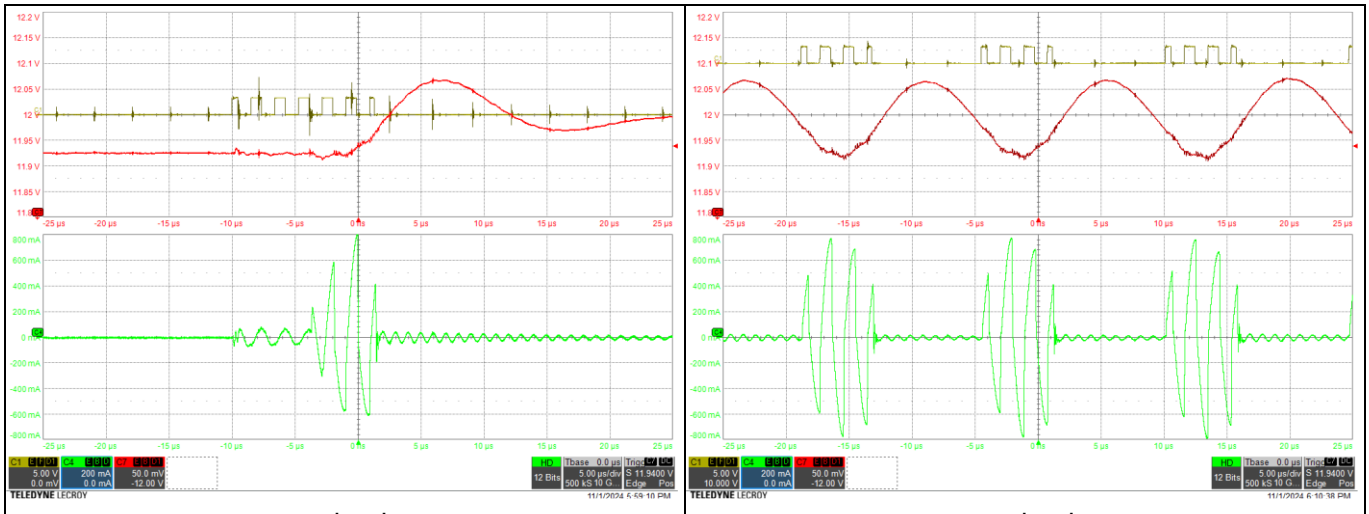
Figure 34 shows the burst mode waveforms at light load with a time scale of 50 µs. Additional details are shown in Figure 35 with a time scale of 5 µs. At 0 A load, the burst off interval is very long, causing the bootstrap capacitor to discharge. The first few pulses are used to charge the bootstrap capacitor for the high-side gate driver, and the total number of pulses are increased to 7, as defined in the configuration. At 10 A load, the burst off and burst on intervals are almost the same. A delay of around 4 µs can be observed after the start of burst pulses until output voltage starts to rise, due to the output filter inductor L1.



53 V input, 0.4 A load | 53 V input, 2.8 A load

C1 (5 V/div) = Primary PWM, C2 (20 V/div) = Primary V_{DS}, C4 (200 mA/div) = Primary current (15:1), 50 µs/div

Figure 34 Burst mode at light load



0 A load | 10 A load

C1 (5 V/div) = Primary PWM, C4 (200 mA/div) = Primary current (15:1), C7 (50 mV/div) = Vout, 5 µs/div

Figure 35 Burst mode at 54 V input

To understand different output voltage ripple shapes, Figure 36 is given for 60 V input and 20 A to 55 A load. Starting at 35 A load, the first burst-on sequence is not enough to bring up the output voltage. Therefore, a second burst sequence is started again immediately after the other. This is possible because burst mode hold off time is set to 0. As the current increases to 40 A, the controller can exist burst and stays in normal operation

for some time and enters burst again. At 55 A, this normal operation time is longer, about 50 µs between each burst mode entries.

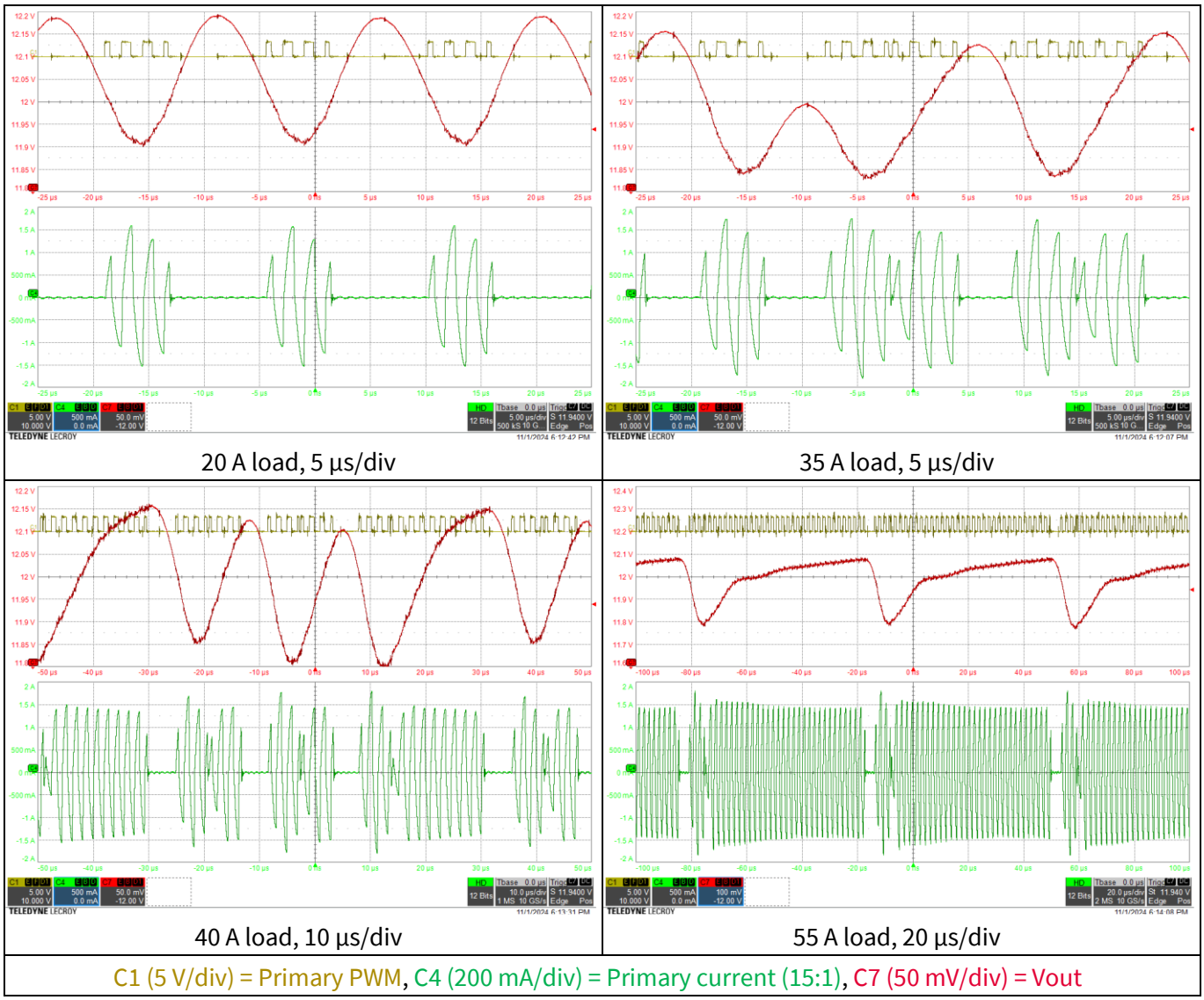


Figure 36 Burst mode at 60 V input

3.2.5 Adaptive SR timing

The external V_{DS} sense circuit shown in Figure 13 is used in this design, and the values of the resistors are adjusted to produce Vds_comp signals shown in Figure 37 and Figure 38. Since adaptive SR timing is only functioning for below resonance operation, the waveforms are captured at input voltages of 46 V and 48 V.

Figure 37 shows the results using adaptive SR timing mode 5. The target of mode 5 is the same as mode 2, which is ½Tres. The on-time of secondary V_{GS} stays about the same across the load range.

Figure 38 shows the results using timing mode 3. The target of mode 3 is toff_dly_t3, which is the pulse width of the Vds_comp signal after secondary V_{GS} transitions to low. In this case, the on-time of secondary V_{GS} varies slightly across the load range, however, the pulse width of the aforementioned Vds_comp signal stays constant.

In both timing modes, the Vds_comp signal appears to have more than 2 pulses at high load current. As expected, this does not affect the correct operation of the adaptive timing control.

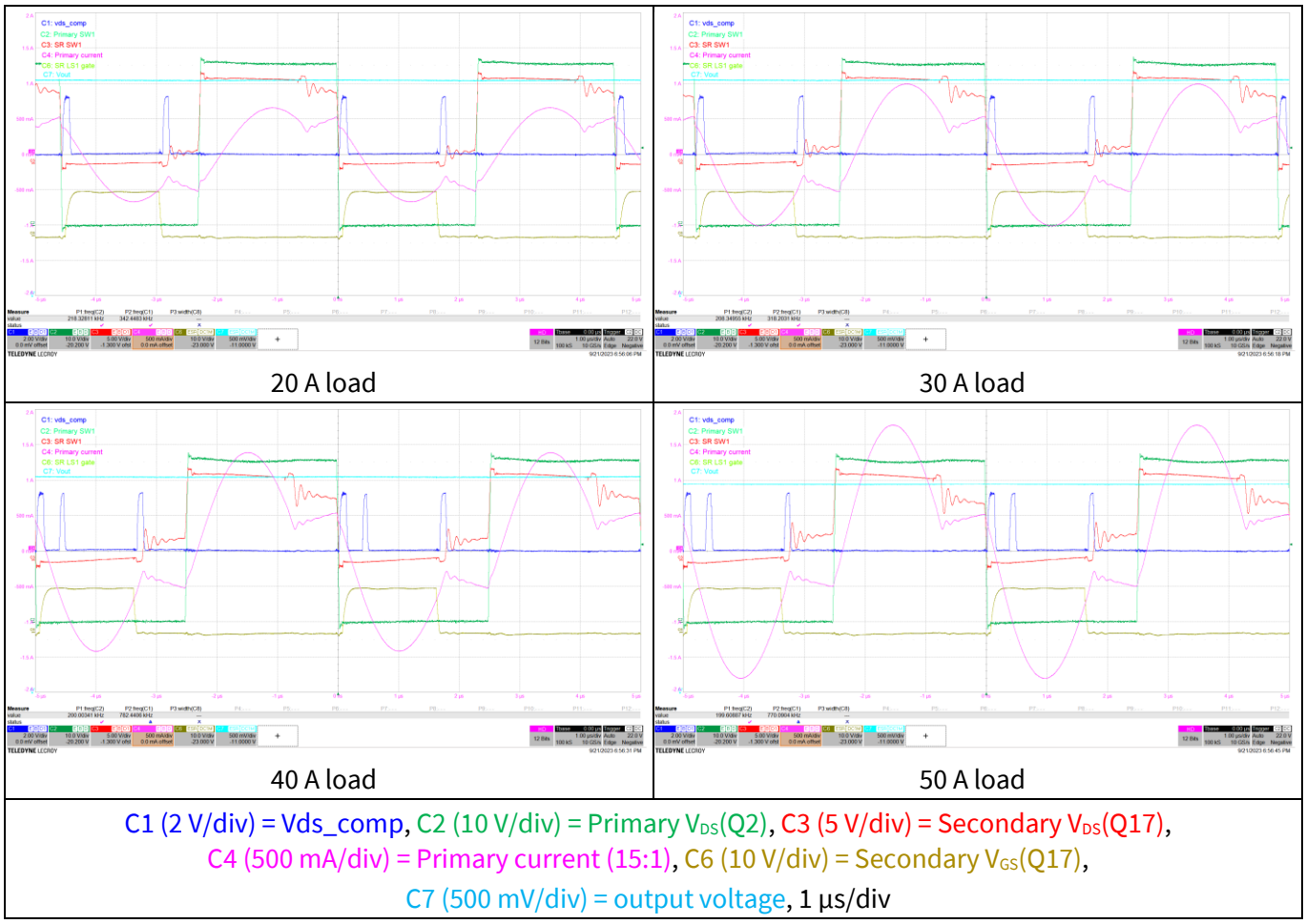
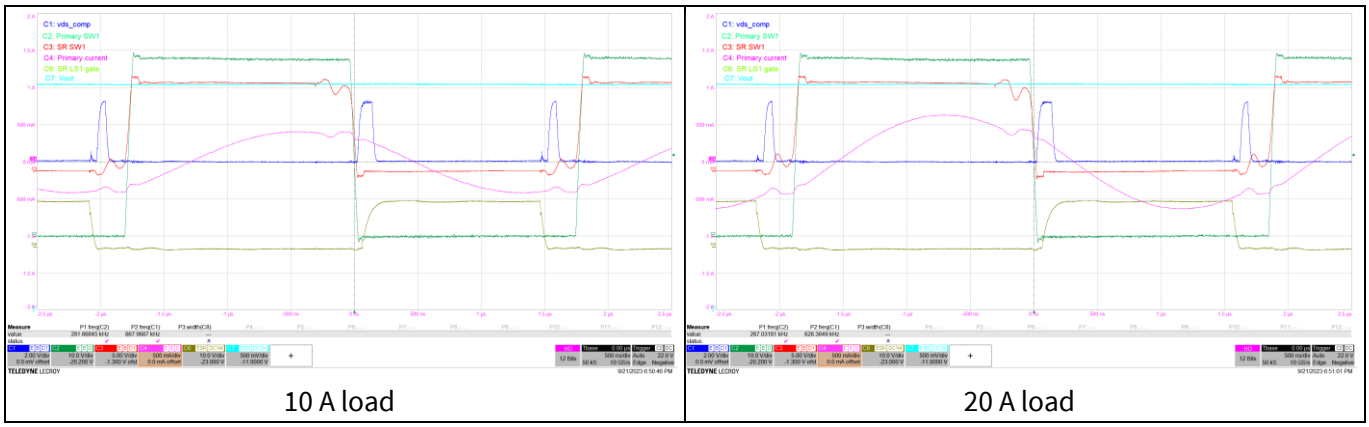


Figure 37 Waveforms using adaptive SR timing mode 5 at 46 V input



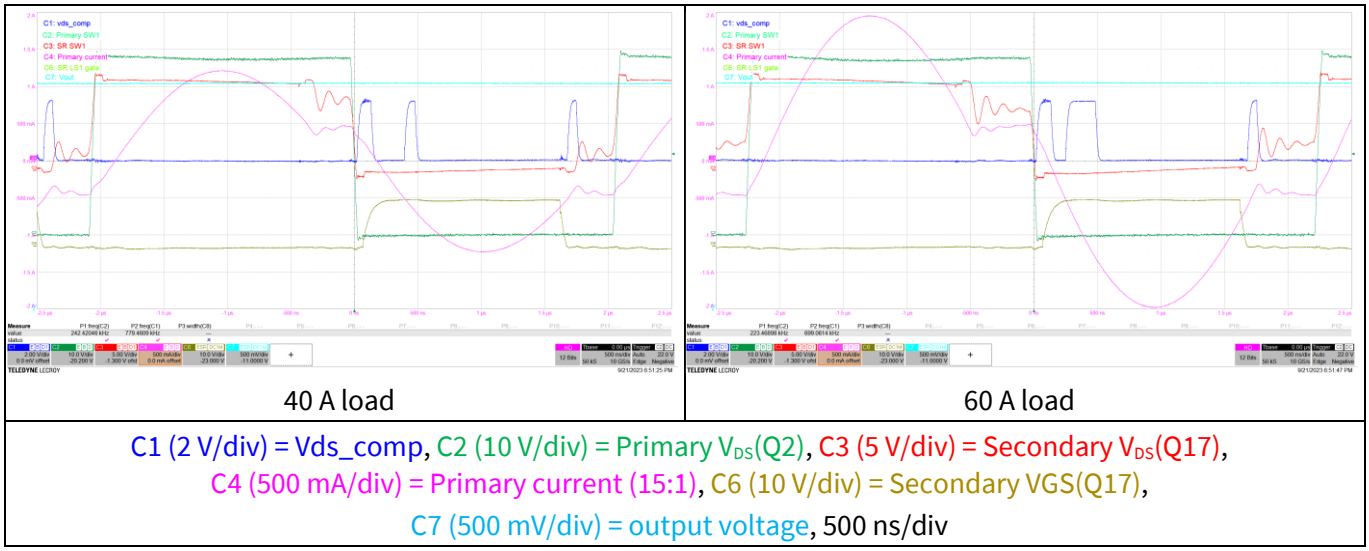
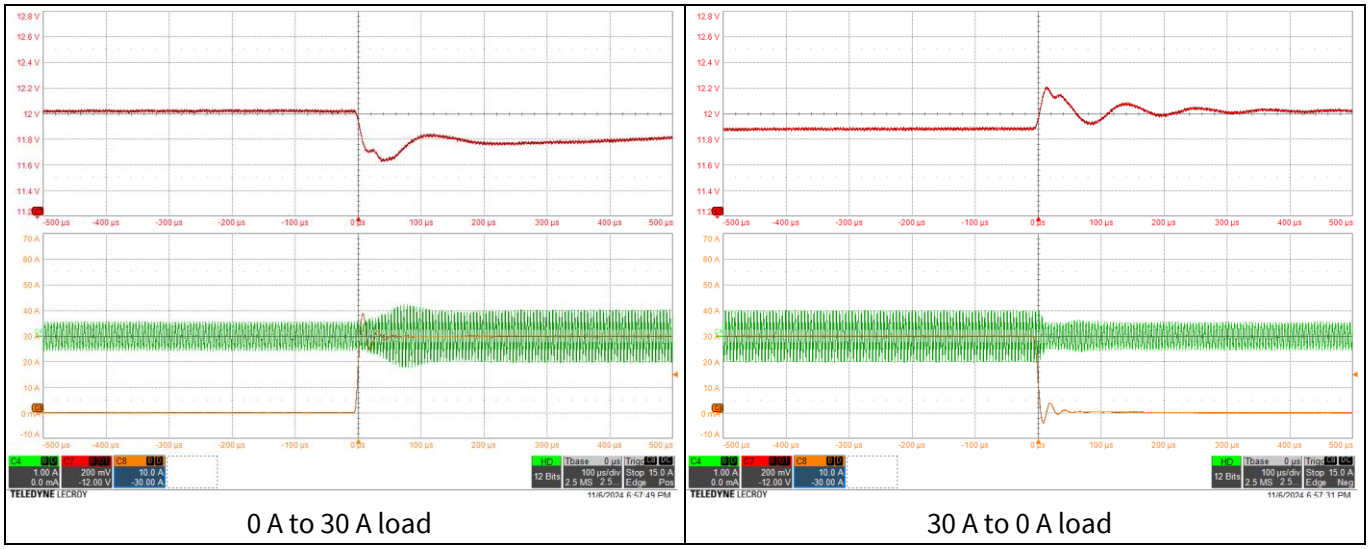
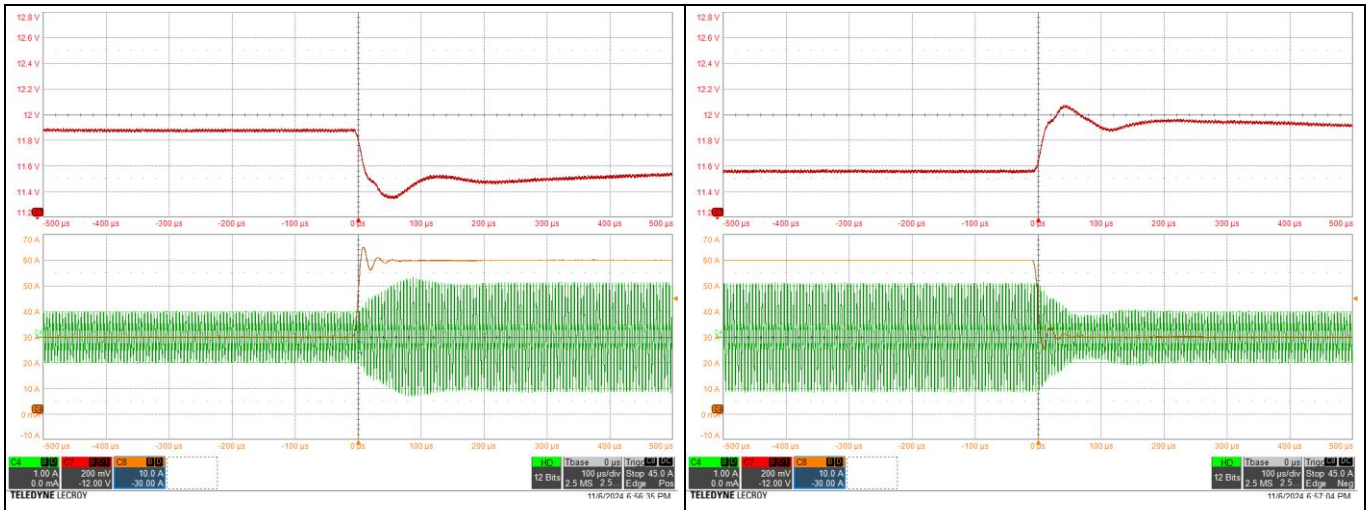


Figure 38 Waveforms using adaptive SR timing mode 3 at 48 V input

3.2.6 Load transient

Two sets of transient responses are measured: 0 A/30 A, and 30 A/60 A, at input voltages from 44 V to 60 V. The slew rate of the current is set to 5 A/µs. At low input voltage of 44 V, the converter becomes open loop when load current is above 20 A (partial regulation). The load transient response at 44 V input is shown in Figure 39. For 0 A/30 A transient, the converter is transition between closed loop and open loop. For 30 A/60 A transient, the converter remains in open loop. In all cases, the settling time is within 100 µs and the maximum output voltage error is within ±5.3%.



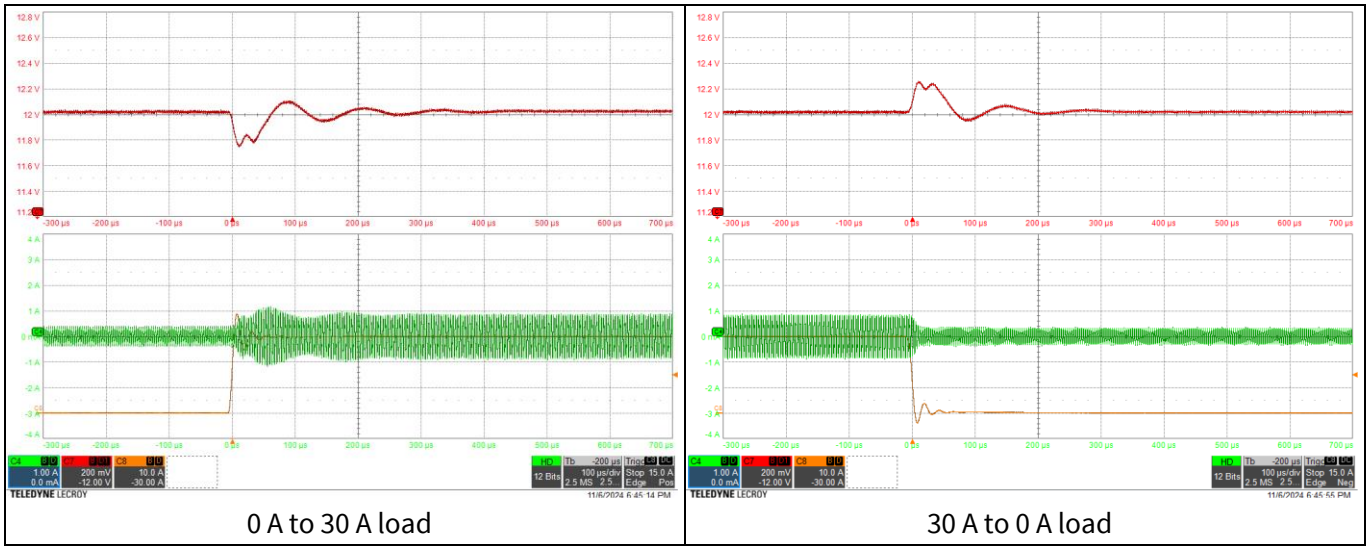


30 A to 60 A load | 60 A to 30 A load

C4 (1 A/div) = Primary current (15:1), C7 (200 mV/div) = output voltage, C8 (10 A/div) = load current, 100 µs/div

Figure 39 Load transient waveforms at 44 V input (partial regulation)

At 48 V input, the converter is in closed loop for all load conditions. The transient response waveforms are shown in Figure 40. The maximum output voltage error is within ±2.3%. The output voltage ringing is more apparent at high current, with a frequency of 9 kHz. This can be explained by the loop gain measurement shown in Figure 41. There are multiple resonances and 0 dB crossings, one of which is located near 9 kHz. Nevertheless, the system is stable according to the Nyquist plot shown in Figure 42.



0 A to 30 A load | 30 A to 0 A load

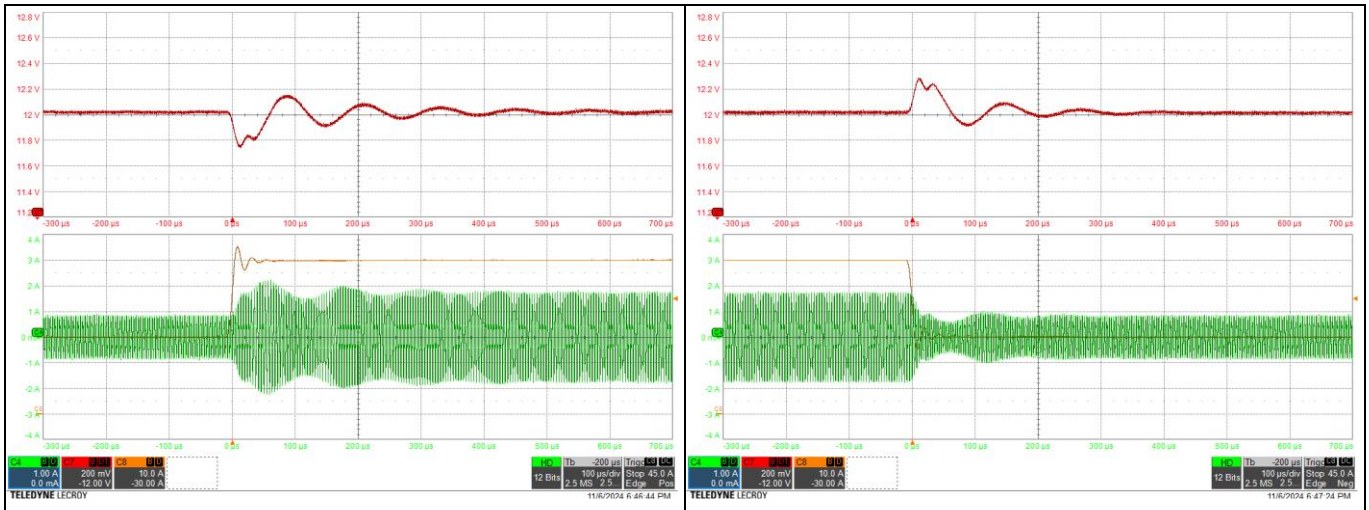


Figure 40 Load transient waveforms at 48 V input

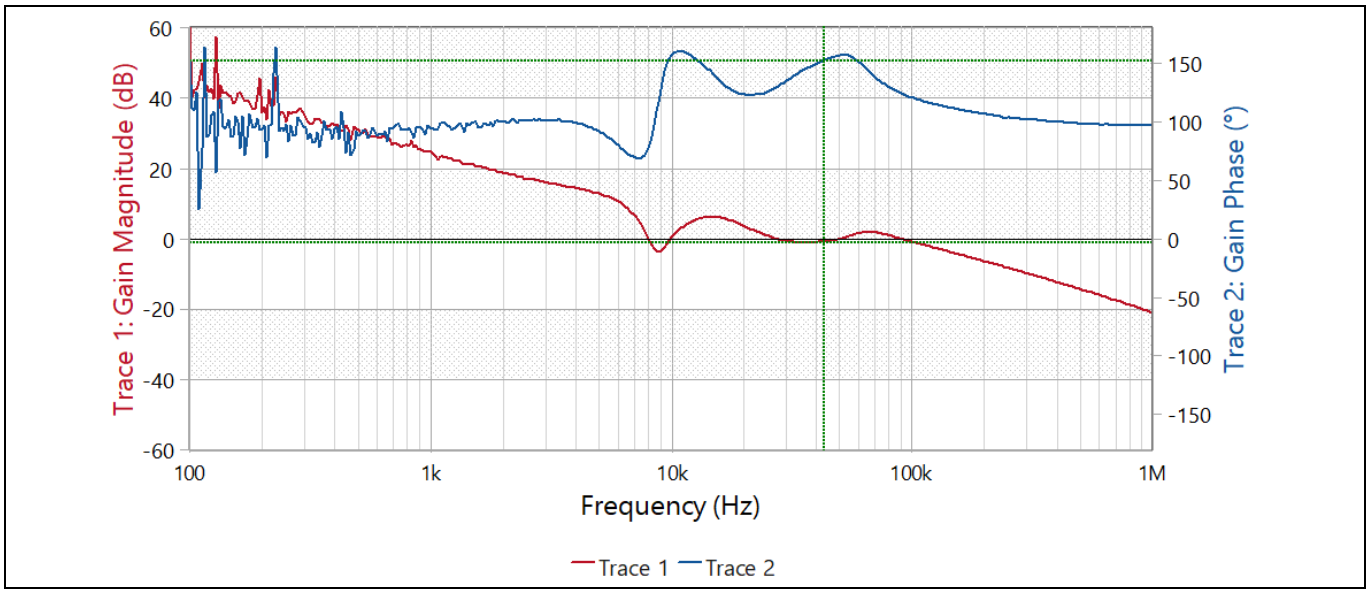


Figure 41 Measured loop gain at 48 V input, 60 A load

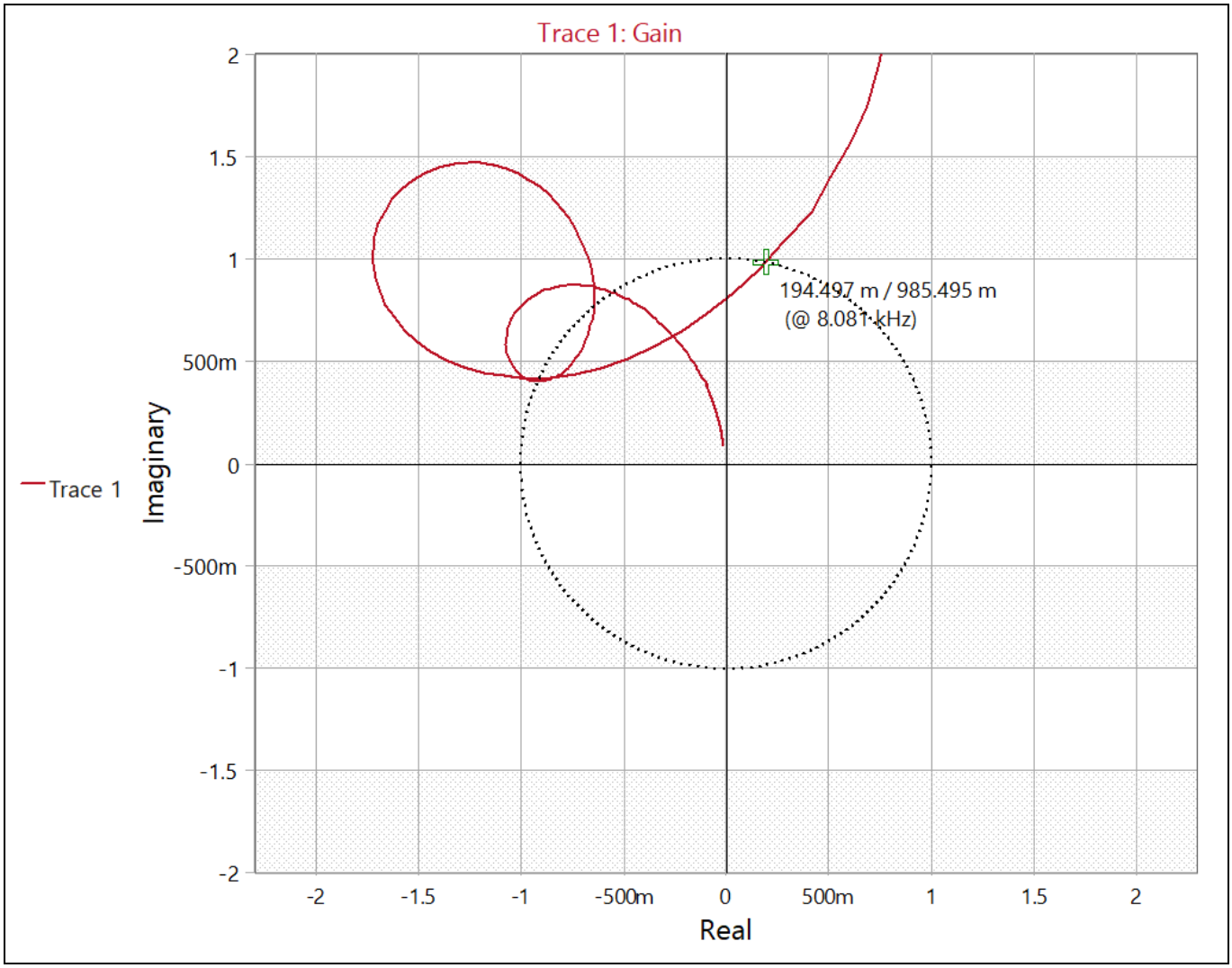
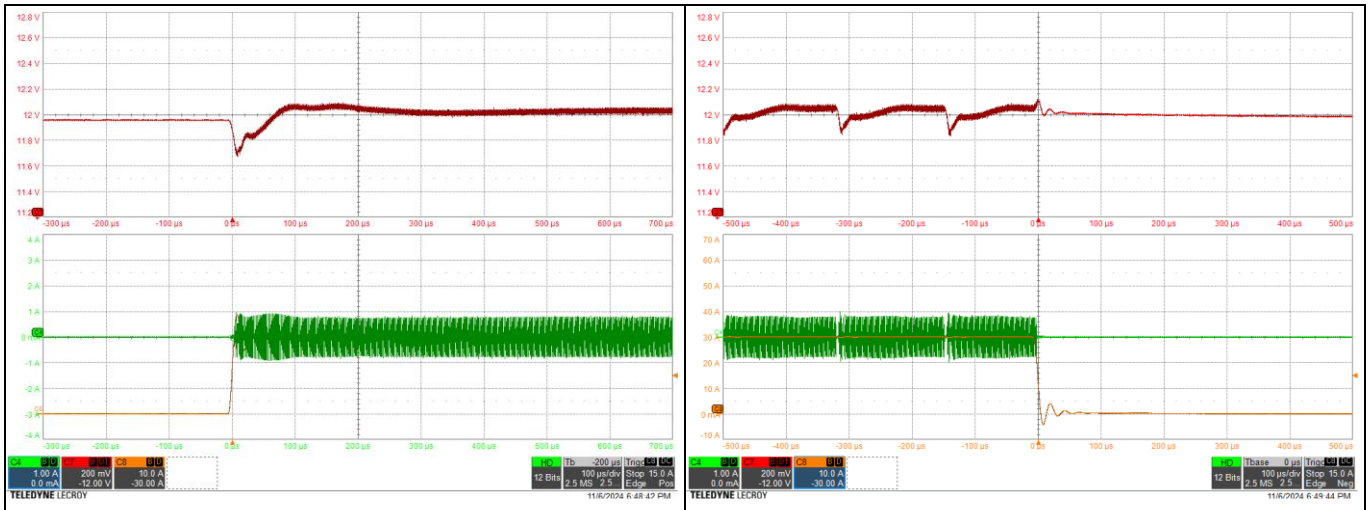


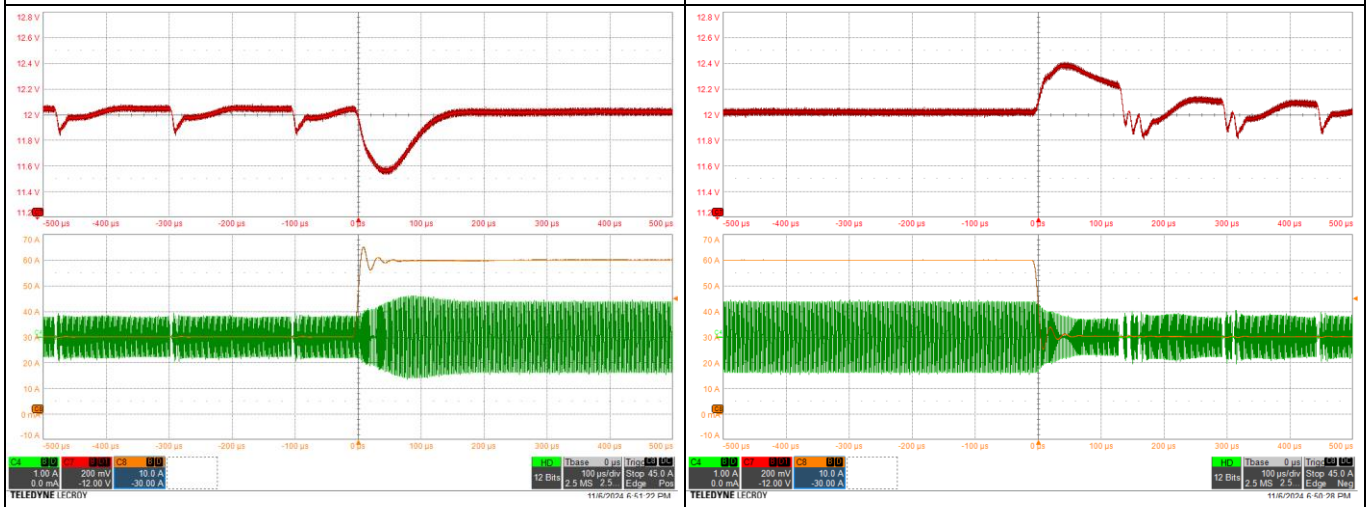
Figure 42 Nyquist plot of the loop gain at 48 V input, 60 A load

At 54 V input, from 0 A to 30 A, the converter operates in burst mode. Above 30 A, it operates in continuous switching. Figure 43 shows the transient response waveforms. All transitions settle within 150 µs and the maximum output voltage error is within ±3.5%.

Similarly, at 60 V input, the transient response waveforms are shown in Figure 44. Both settling time and error are better compared to 54 V input.



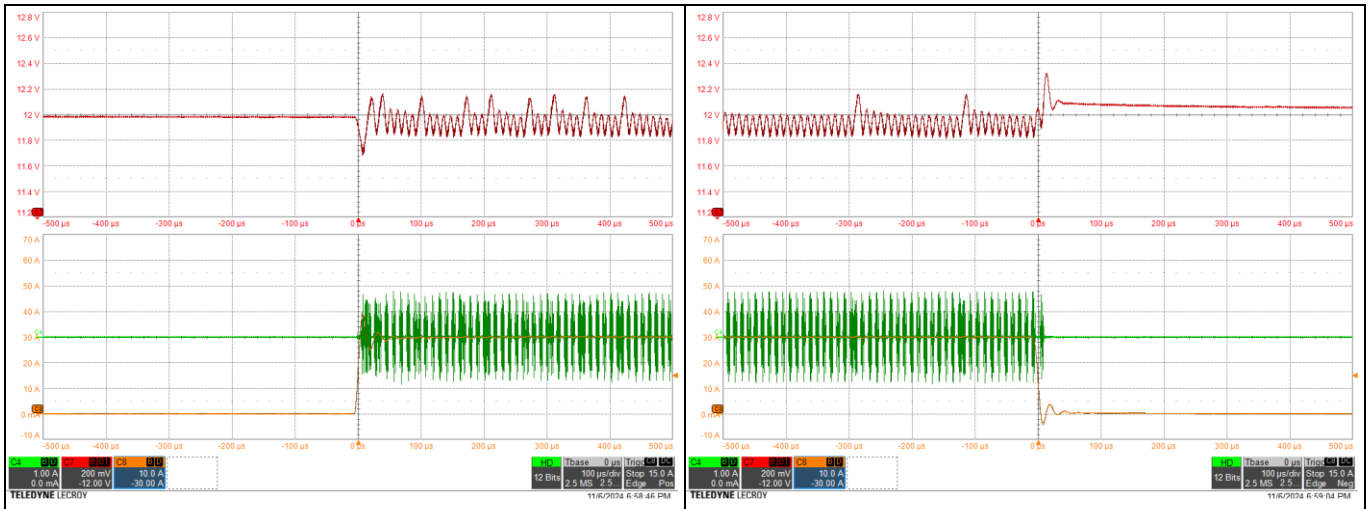
0 A to 30 A load | 30 A to 0 A load



30 A to 60 A load | 60 A to 30 A load

C4 (1 A/div) = Primary current (15:1), C7 (200 mV/div) = output voltage,
C8 (10 A/div) = load current, 100 µs/div

Figure 43 Load transient waveforms at 54 V input



0 A to 30 A load | 30 A to 0 A load

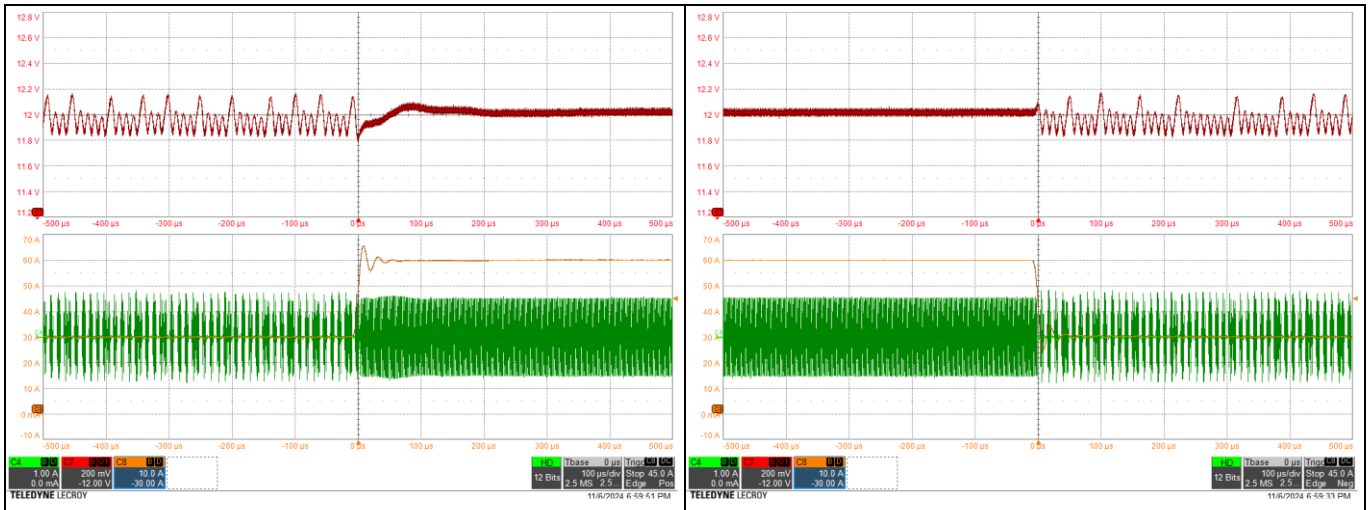


Figure 44 Load transient waveforms at 60 V input

3.2.7 Line transient

The line transient responses are highly dependent on the input voltage and load current, particularly when operating in burst mode at high input voltages. Certain combinations of input voltage and load current can lead to output overvoltage. Therefore, the acceptable input voltages range for line transient test may be limited, depending on the maximum output overshoot limit and load current. Based on the measurement from this design, the approximated regions for line transient for a given output voltage error are shown in Figure 45. In general, the output voltage error increases as the system operates further into the burst region, but decreases as the load current increases.

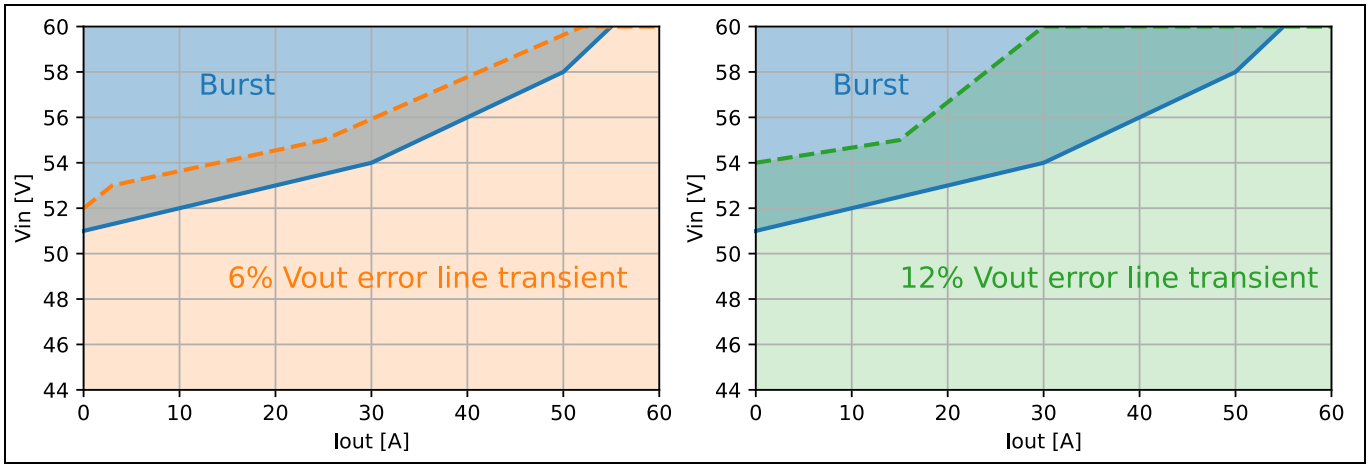
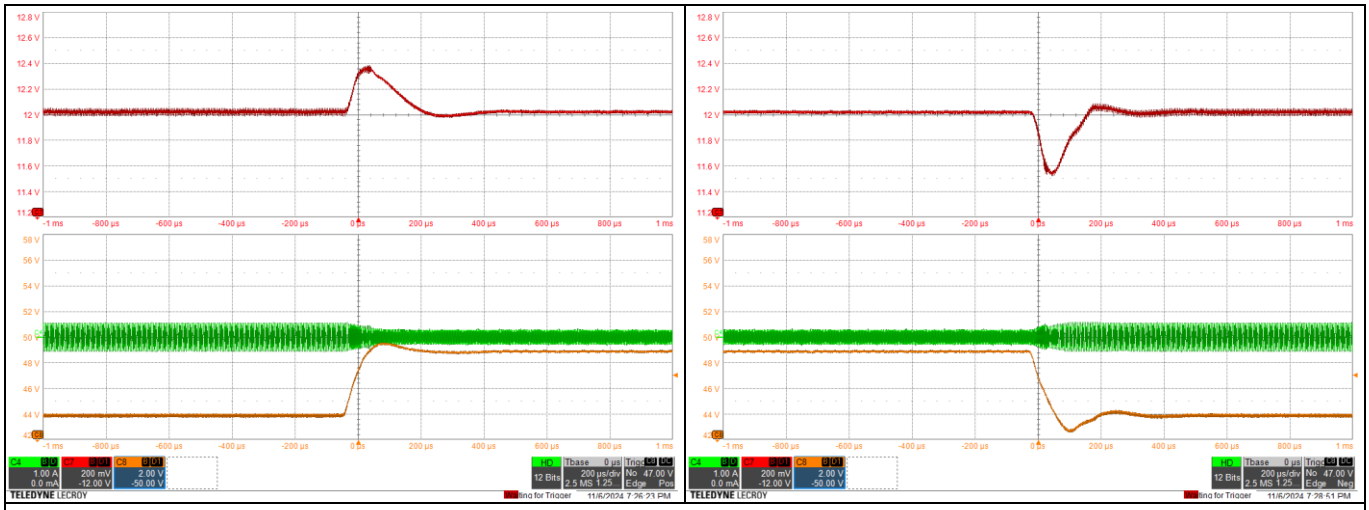


Figure 45 Allowed line transient region for 6% and 12% output voltage error

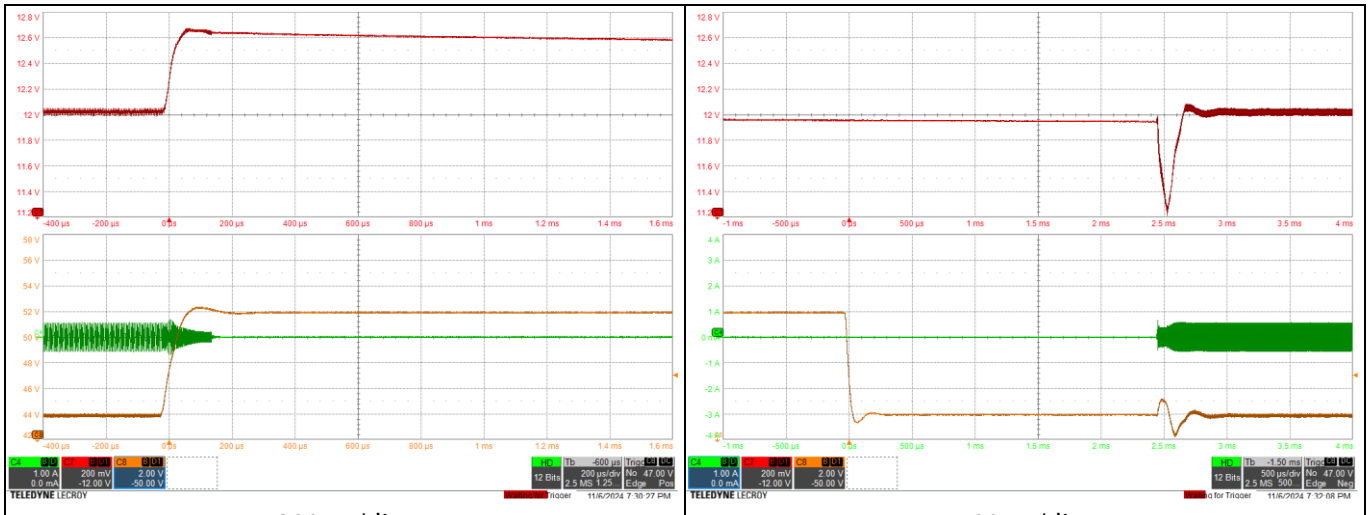
The following line transient test results are given for different combination of input voltage and output current, to demonstrate effect of the different output voltage errors. The input voltage transition slew rate is 0.2 V/µs, limited by the power supply's maximum drive capability and input capacitor.

At 0 A, the line transient responses for 44 V/49 V (continuous switching) and 44 V/52 V (into burst region) are shown in Figure 46 and Figure 47. For 44 V/49 V transient, the output voltage error is within 4%. However, for 44 V/52 V transient, the error is 6%.



C4 (1 A/div) = Primary current (15:1), C7 (200 mV/div) = output voltage,
C8 (5 V/div) = input voltage, 200 µs/div

Figure 46 Line transient response: input voltages 44 V/49 V at 0 A load current

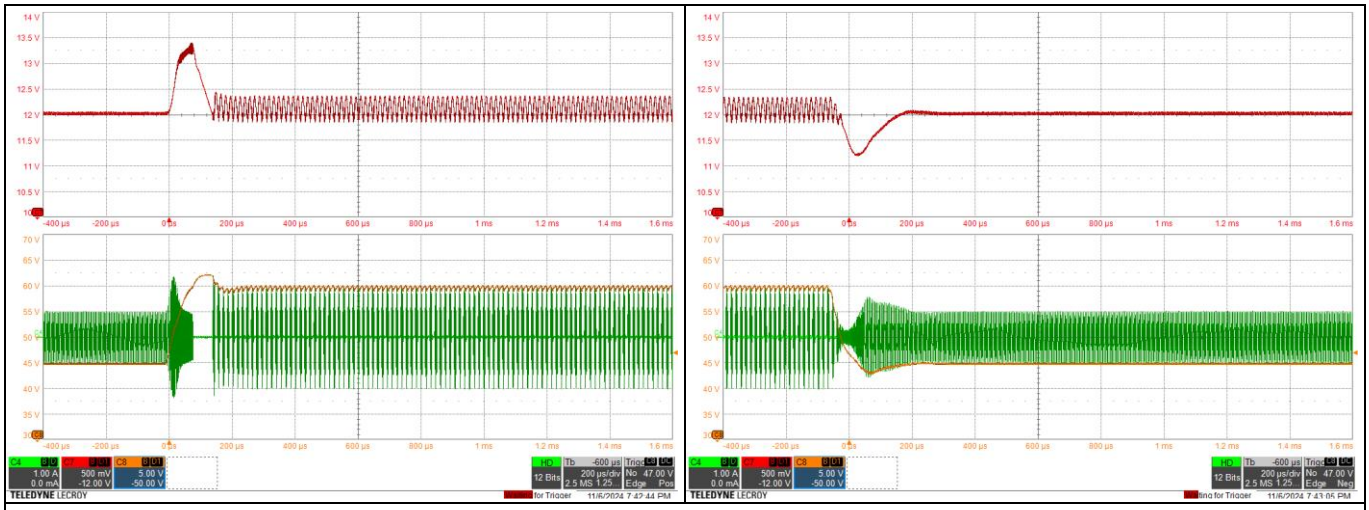


200 µs/div 500 µs/div

C4 (1 A/div) = Primary current (15:1), C7 (200 mV/div) = output voltage,
C8 (5 V/div) = input voltage

Figure 47 Line transient response: input voltages 44 V/52 V at 0 A load current

At 30 A load, the line transients for 45 V/60 V are shown in Figure 48. The output voltage overshoot is 11%.



C4 (1 A/div) = Primary current (15:1), C7 (500 mV/div) = output voltage,
C8 (5 V/div) = input voltage, 200 µs/div

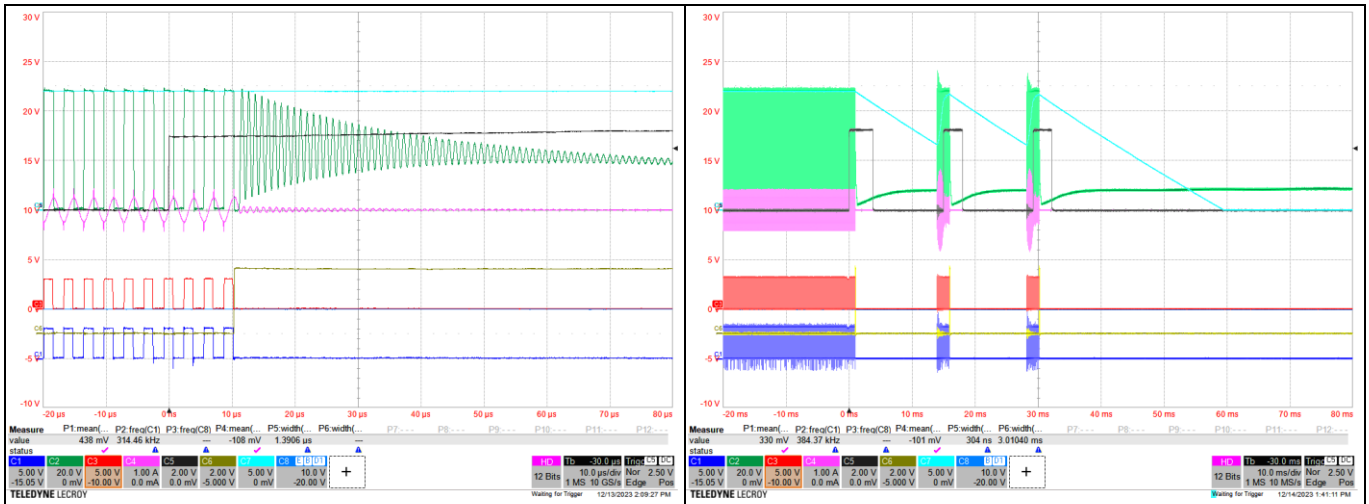
Figure 48 Line transient response: input voltages 45 V/60 V at 30 A load current

3.3 Protection

All standard protections also apply to LLC topology. For example, overvoltage protection (OVP), overcurrent protection (OCP), short-circuit protection (SCP), overtemperature protection (OTP), and so on.

3.3.1 Output OVP

Output OVP is tested at 48 V input, and is triggered by setting the PMBus command VOUT_OV_FAULT_LIMIT to 12 V. The response for no retry and retry twice are shown in Figure 49.



Shutdown, no retry, 10 µs/div | Retry twice, 10 ms/div

C1 (5 V/div) = Primary PWM, C2 (20 V/div) = Primary V_{DS}(Q2), C3 (5 V/div) = Secondary PWM,
C4 (1 A/div) = Primary current (15:1), C7 (5 V/div) = output voltage

Figure 49 Output OVP waveforms

3.3.2 Output OCP

Different responses can be configured for output OCP, as shown in Figure 50. Fast OCP is also supported, an example is shown in Figure 51.

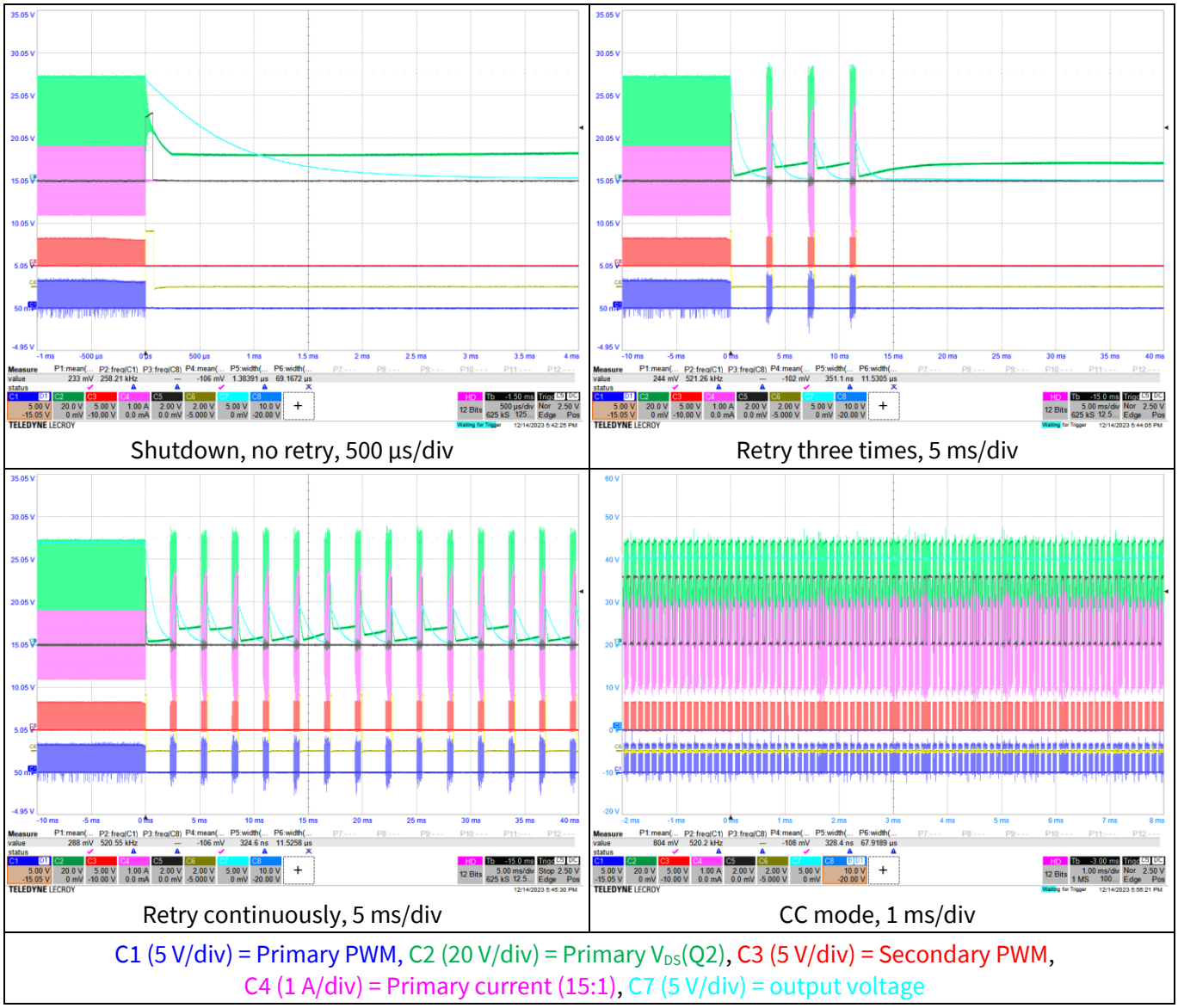
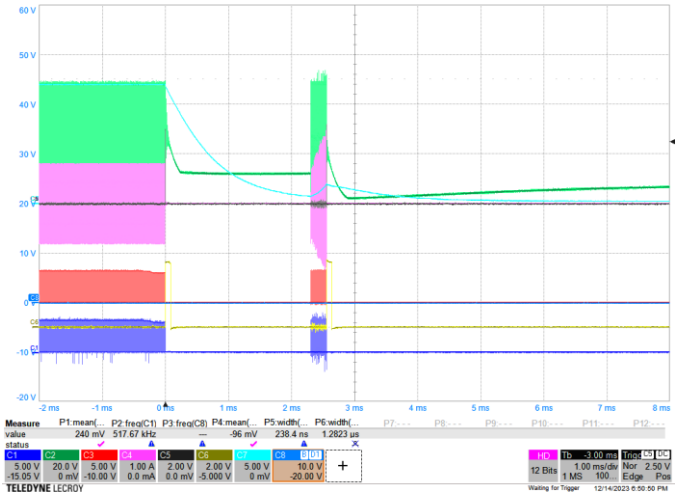


Figure 50 Output OCP waveforms



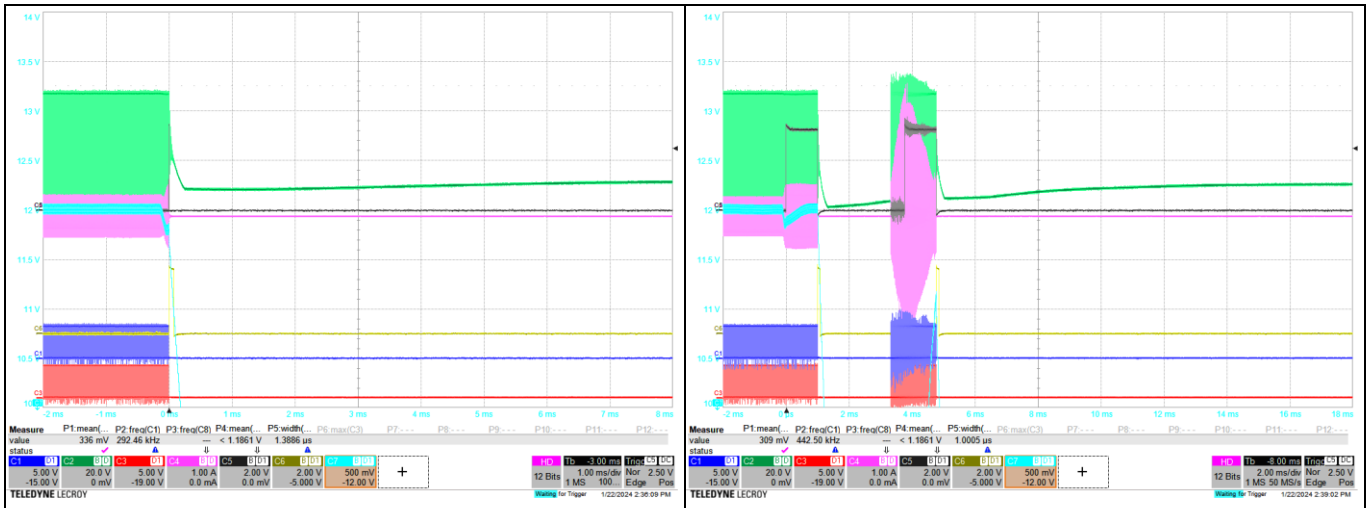
Retry once

C1 (5 V/div) = Primary PWM, C2 (20 V/div) = Primary V_{DS}(Q2), C3 (5 V/div) = Secondary PWM, C4 (1 A/div) = Primary current (15:1), C7 (5 V/div) = output voltage, 1 ms/div

Figure 51 Output fast OCP waveform

3.3.3 Input OCP

Taking advantage of the primary AC current sensing, the input OCP can be implemented. Example results are shown in Figure 52.



Shutdown, no retry, 1 ms/div

Delayed shutdown, retry once, 2 ms/div

C1 (5 V/div) = Primary PWM, C2 (20 V/div) = Primary V_{DS}(Q2), C3 (5 V/div) = Secondary PWM, C4 (1 A/div) = Primary current (15:1), C7 (5 V/div) = output voltage

Figure 52 Input OCP waveform

4 Summary

This document introduces a regulated LLC converter that supports wide input range for telecom applications. The input range is 44 V to 60 V, and the peak efficiency is 96%.

Infineon's XDP™ XDPP1148-100B is the industry's smallest digital power controller and has built-in support for LLC features, such as primary AC current sensing, frequency modulation, soft-start, SR adaptive timing control, and burst mode. The controller offers many optimized power processing blocks and pre-programmed peripherals, which enhances the performance of isolated DC-DC converters, reduces external components, and minimizes firmware development effort. It also provides accurate telemetry and PMBus interface for system communication.

The primary OptiMOS™ 6 80 V MOSFET (ISC031N08NM6) has an excellent FOM and superior switching performance. The low output capacitance reduces the required magnetizing current for ZVS operation in the LLC converter, minimizing circulating losses. The secondary OptiMOS™ 5 25 V MOSFET (IQE006NE2LM5CG) has an industry-leading $R_{DS(on)}$, significantly lowering the conduction losses of SRs in the LLC converter. The reduced form factor (PQFN 3.3 mm × 3.3 mm footprint) enables more FETs to be paralleled in the same space, which further reduces conduction losses and offers superior thermal management. Both the primary and secondary ETs are driven by Infineon's 2EDL8124G EiceDRIVER™ gate driver in VDSON-8 4 mm × 4 mm package. Infineon's 2DIB0400F ISOFACE™ dual-channel digital isolator with coreless technology provides high noise immunity and robust isolated communication to drive the primary gate drivers.

References

[1] Infineon Technologies AG: *AN234423, 1 kW 48 V to 12 V telecom quarter-brick fixed-frequency LLC with XDPP1100 digital controller*; Available online

Glossary

Definitions of acronyms, symbols and terms

Acronym, symbol or term	Definition
ADC	Analog-to-digital converter
CC	Constant current
DMM	Digital multimeter
FB	Full-bridge
FW	Firmware
LSB	Least significant bit
N_p	Transformer primary-side number of turns
N_s	Transformer secondary-side number of turns
OVP	Overvoltage protection
OCP	Overcurrent protection
PID	Proportional-integral-derivative filter
PWM	Pulse width modulation
RAM	Random-access memory
SR	Synchronous rectification/synchronous rectifier
Tres	Resonant period
TS	Telemetry sense
VMC	Voltage mode control
V_{IN}	Input voltage
V_{DS}	MOSFET drain to source voltage
V_{GS}	MOSFET gate to source voltage
V_{OUT}	Output voltage
V_{RECT}	Transformer secondary rectified voltage

Revision history

Document revision	Date	Description of changes
V 1.0	2025-04-09	Initial release

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