PCB layout guidelines for XDP™ XDP7xx-00x hot-swap applications

About this document

Scope and purpose

This application note describes the PCB layout guidelines that are critical for the Infineon XDP™ XDP7xx-00x hot-swap applications. Other PCB design guidelines can be found in references [1] and [7].

This document focuses on XDP711-001, however, the PCB layout guidelines are also applicable for Infineon's XDP710-002 and similar hot-swap controller products.

Intended audience

This document is intended for the engineers and developers working with Infineon XDP711-001, XDP710-002, or similar products of XDP™ XDP7xx series.

XDP™

XDP™ is a high-performance digital power controller designed to optimize the IC for the specific applications. They feature digital algorithms for high power efficiency and minimal standby power, digital parameter configuration for increased flexibility and lower development effort, and optimized bill of materials (BoM), making these controllers ideal for a range of applications such as:

- Telecom
- Datacenter and computing
- SMPS

Table of contents

About this document **1**
Table of contents **2**
1 Introduction **3**
1.1 XDP711-001 3
1.2 Abbreviations and acronyms 4
2 PCB layout guidelines **5**
2.1 Gate driver 5
2.2 Current sense 6
2.3 Power supply 8
2.4 Temperature sense 10
2.5 Power MOSFETs 11
3 PCB layout example **13**
4 Summary **19**
References **20**
Revision history **21**
Disclaimer **22**

1 Introduction

1.1 XDP711-001

Infineon hot-swap controllers, such as XDP711-001, are wide input voltage hot-swap controllers with programmable digital SOA control, ideal for artificial intelligence (AI) servers and telecom infrastructure [2]. Key resources of the hot-swap controllers include high-precision AFE, extensive variety of system warnings and protections, high-speed communication via PMBus® to main CPU, reset, shutdown, retry, and digital SOA control gate driver, and charge pump for a controlled turn-on and safe operation. A typical application block diagram of XDP711-001 is shown in Figure 1. See the XDP7xxx datasheets [3], [4], and [5] for more information on the pin configurations and package details, product characteristics, features, and applications.

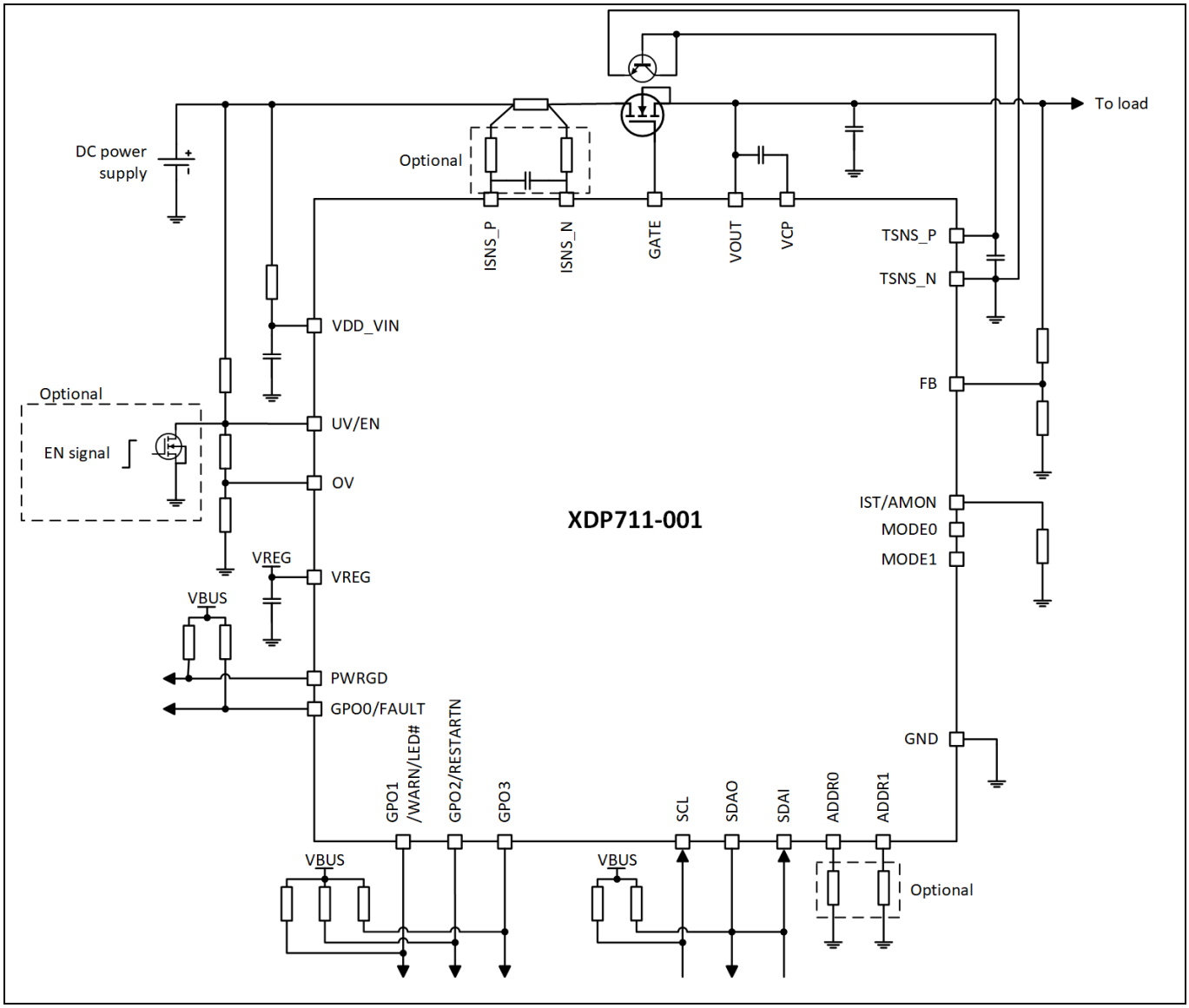

Figure 1 Application block diagram of XDP711-001

1.2 Abbreviations and acronyms

Table 1 Abbreviations and acronyms

Term	Definition
AFE	analog front-end
AI	artificial intelligence
BJT	bipolar junction transistor
CPU	central processing unit
EN	enable
GND	ground
GPO	general purpose output
IC	integrated circuit
LED	light-emitting diode
MOSFET	metal-oxide semiconductor field-effect transistor
N/U	not used, not installed
NPN	negative-positive-negative
OV	overvoltage
PCB	printed circuit board
PMBus®	Power Management Bus
PWRGD	power good
SMD	surface mounted device
UV	undervoltage

2 PCB layout guidelines

2.1 Gate driver

Figure 2 displays the schematics of the gate driver for XDP711-001. GATE is connected to the gate pins of all power MOSFETs through some resistors, while VOUT is connected to the source pins. VCP is the voltage reservoir capacitor pin for the integrated charge pump and needs to be connected to an external capacitor C2 from this pin to VOUT pin. Figure 3 shows the recommended PCB layout guidelines.

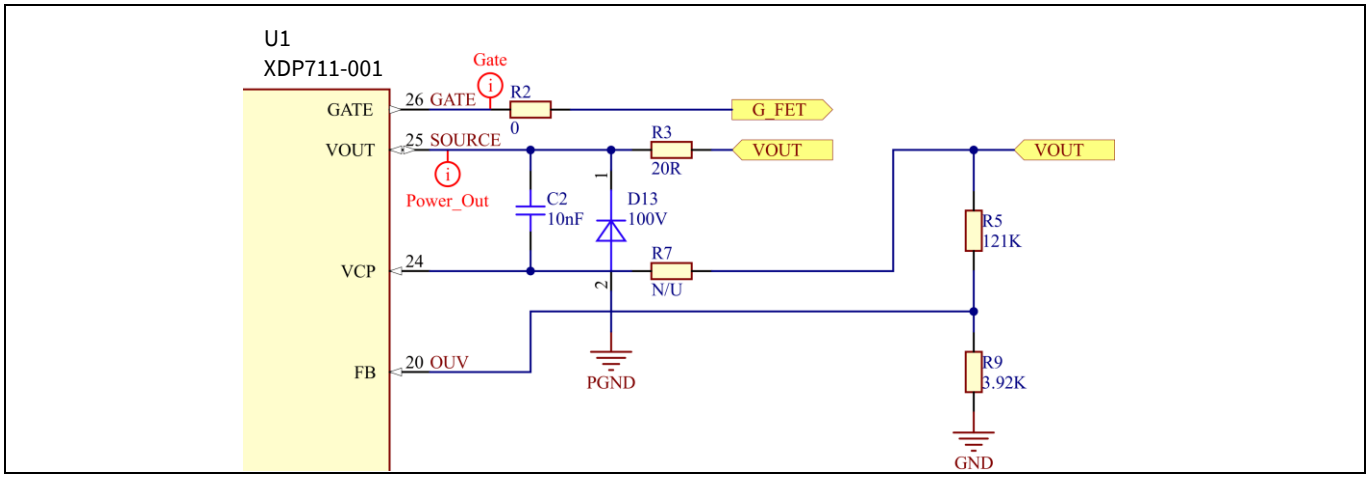

Figure 2 Schematics of gate driver for XDP711-001

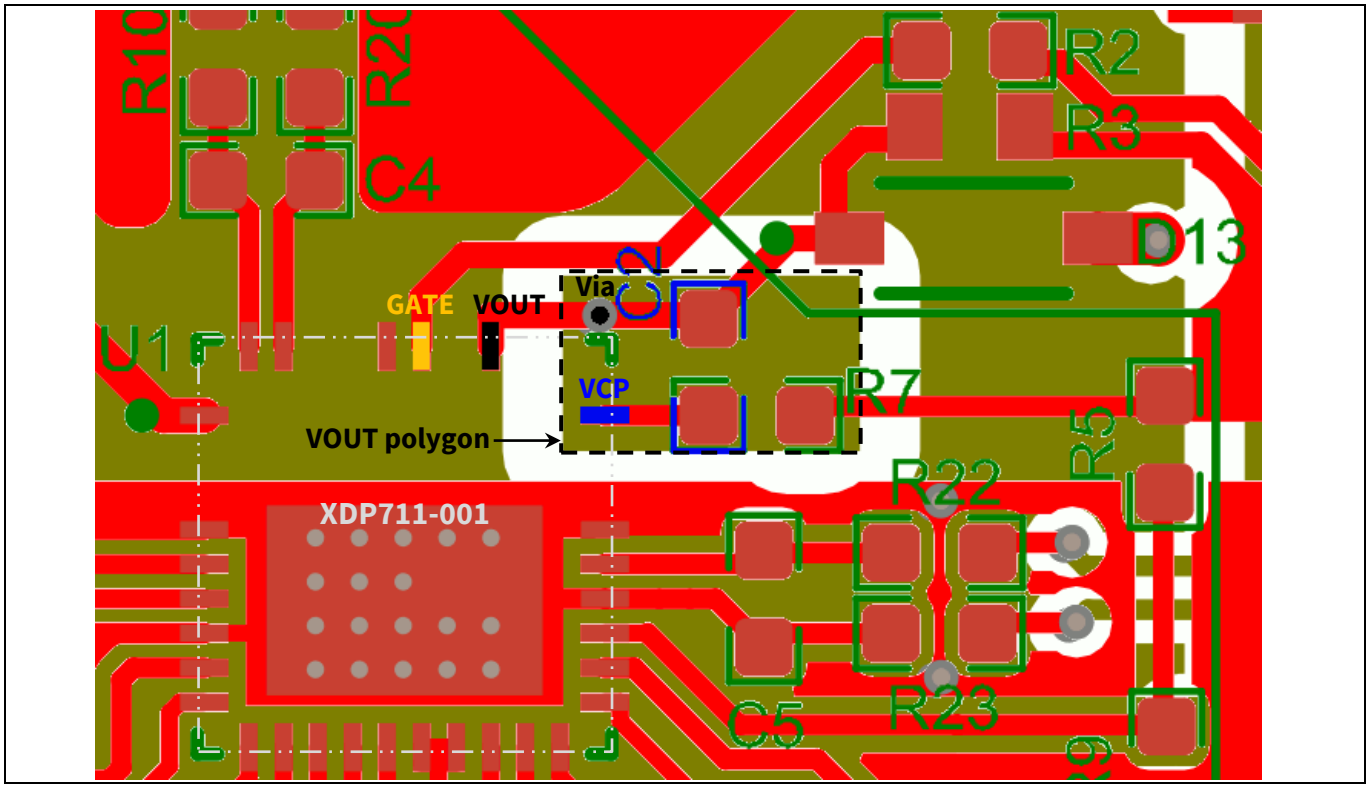

Figure 3 PCB top layer (red) on middle layer 2 (green)

The recommended PCB layout guidelines are:

1. Put the VCP capacitor C2 as close as possible to the VCP pin
2. **Important**: Put a VOUT polygon on the adjacent layer (Middle Layer 2 in this example) under the VCP pin and the VCP capacitor pad. A VOUT via (or a few vias) connects the VOUT polygon to the VOUT signal
3. Minimize the copper area of VCP pad, VCP trace, and the pad(s) connected to VCP pin. In this example, the capacitor (C2) and resistor (R7) pads of VCP signal is shared by a single pad as C2 and R7 will not be installed at the same time
4. Put traces of GATE and VOUT next to each other to minimize the gate current loop
5. Put as many GND vias as possible for the exposed pad of XDP711-001, so that the exposed pad have a solid connection to GND

2.2 Current sense

Figure 4 displays the schematics of the current sense for XDP711-001. Figure 5 shows the PCB layout following recommended layout guidelines.

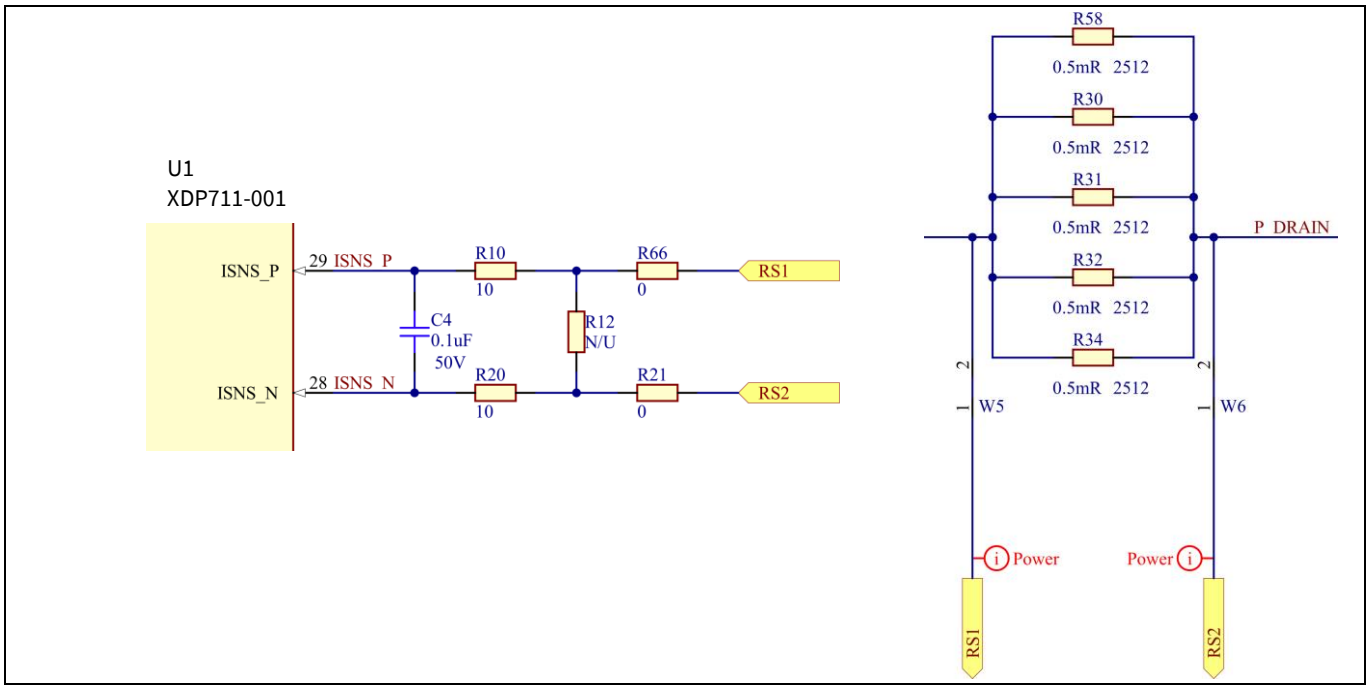

Figure 4 Schematics of current sense for XDP711-001

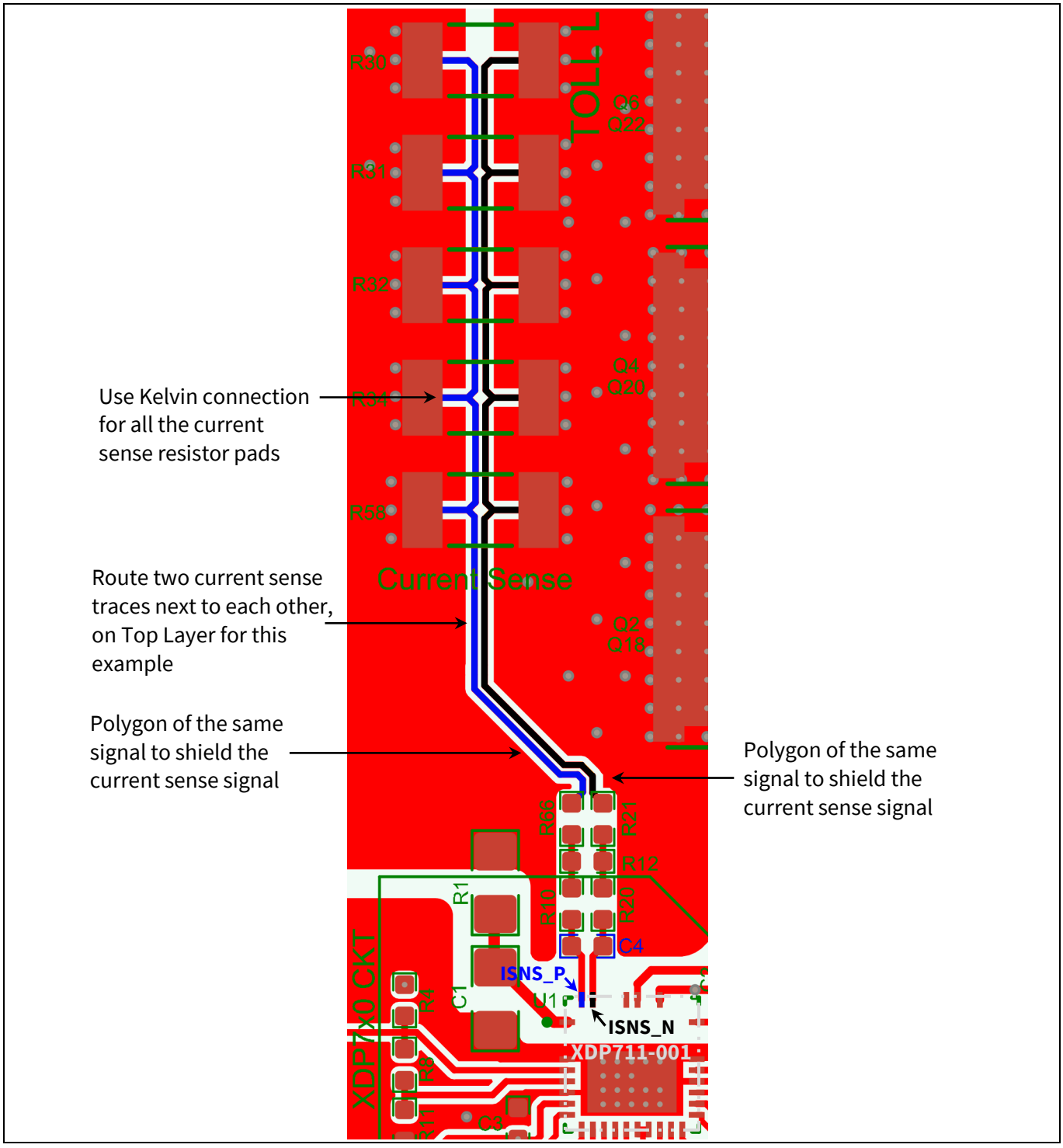

Figure 5 Current sense on the top layer

The recommended PCB layout guidelines are:

1. Use Kelvin connection for each pad of the current sense resistors. Figure 6 shows a few examples of Kelvin connection
2. Use parallel traces for the two current sense signals the ISNS_P and ISNS_N pins of XDP711-001
3. Use polygon to shield the two current sense signals
4. Put the ISNS filter capacitor (C4) near ISNS_P and ISNS_N pins of XDP711-001

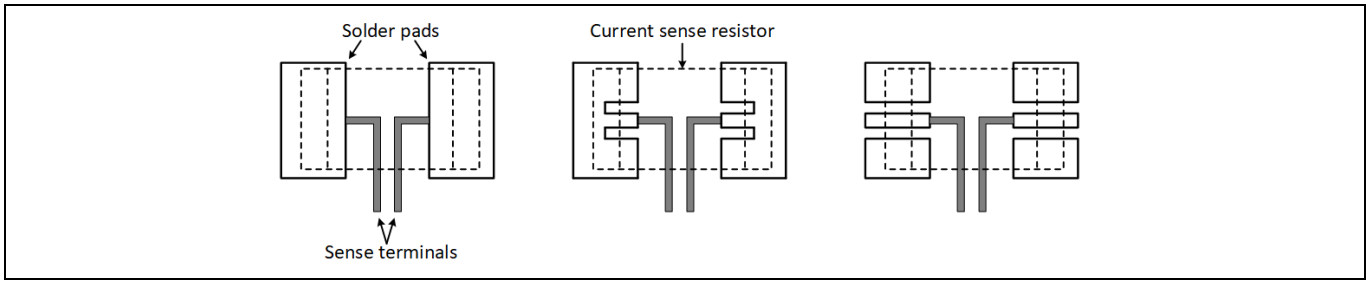

Figure 6 Examples of Kelvin connection for current sense resistor

2.3 Power supply

Figure 7 displays the schematics of the power supply decoupling for VDD_VIN and VREG pins for XDP711-001. Figure 8 shows the PCB layout following recommended layout guidelines.

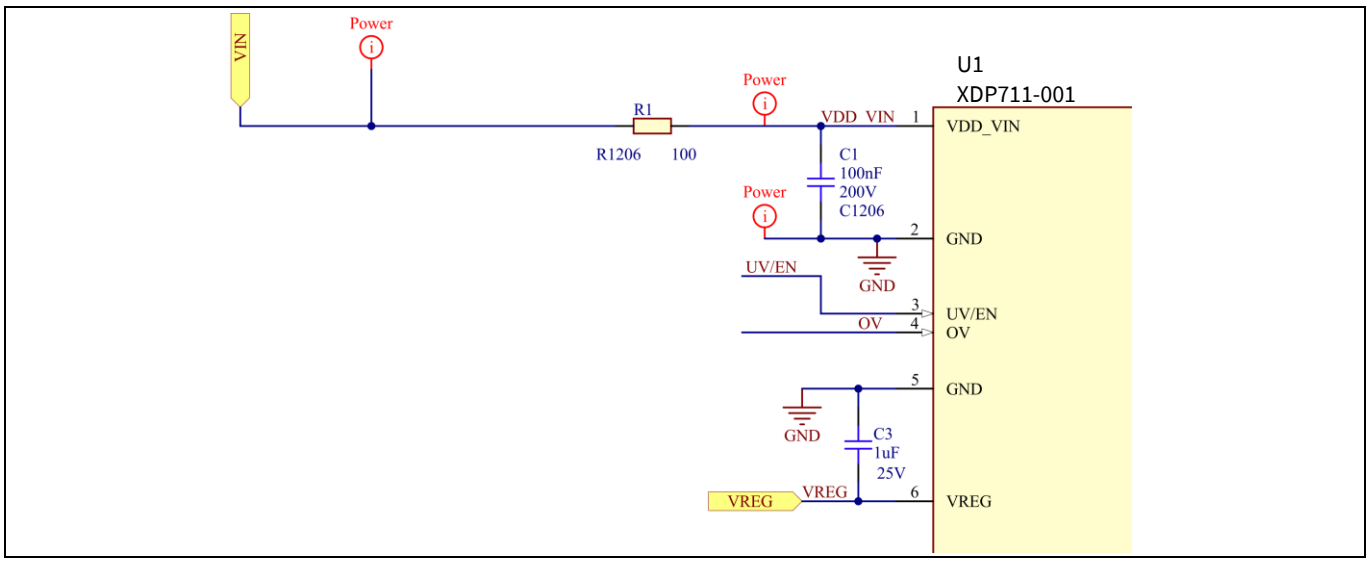

Figure 7 Schematics of power supply decoupling for XDP711-001

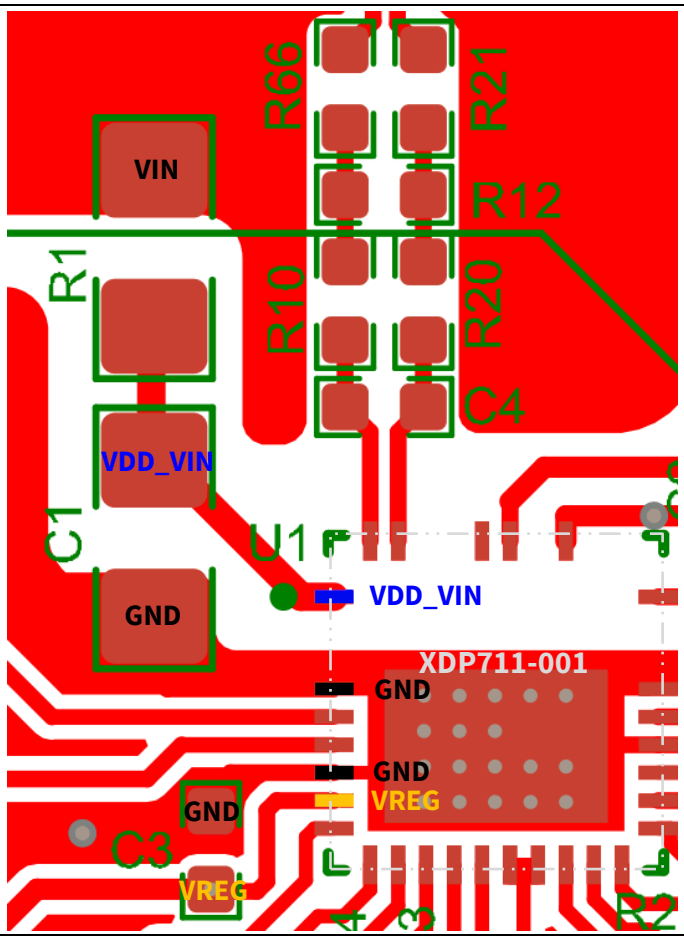

Figure 8 Power supply decoupling on top layer

The recommended PCB layout guidelines are:

1. Put the VDD_VIN decoupling capacitor (C1) near the power supply pin VDD_VIN
2. Put the VREG decoupling capacitor (C3) right next to the VREG pin
3. The GND pads of decoupling capacitors (C1 and C3) have short connections to the GND pins and the exposed pad of XDP711-001, so the GND return current loops and impedances are minimized

The maximum internal current consumption of the whole IC of XDP711-001 is 10 mA and the maximum current of VREG to supply external load is 10 mA, hence, the VDD_VIN trace doesn't need to be thick since the maximum current flowing into VDD_VIN pin is 10 mA + 10 mA = 20 mA. At I_{R1} = 20 mA, the power of the VDD_VIN filter resistor, R1 = 100 Ω, is calculated as follows:

$$P_{\mathrm{R1}} = I_{R1}^2 R1 = 0.04\,\mathrm{W}$$

Equation 1

Thus, the SMD resistor size of R1 can be 0402, but 0603 or larger is preferred considering power derating when used at temperatures above the rated ambient temperature (typically 70°C).

2.4 Temperature sense

Figure 9 displays the schematics of the temperature sense with an external NPN BJT transistor (Q1) for XDP711-001. Figure 10 shows the PCB layout following recommended layout guidelines.

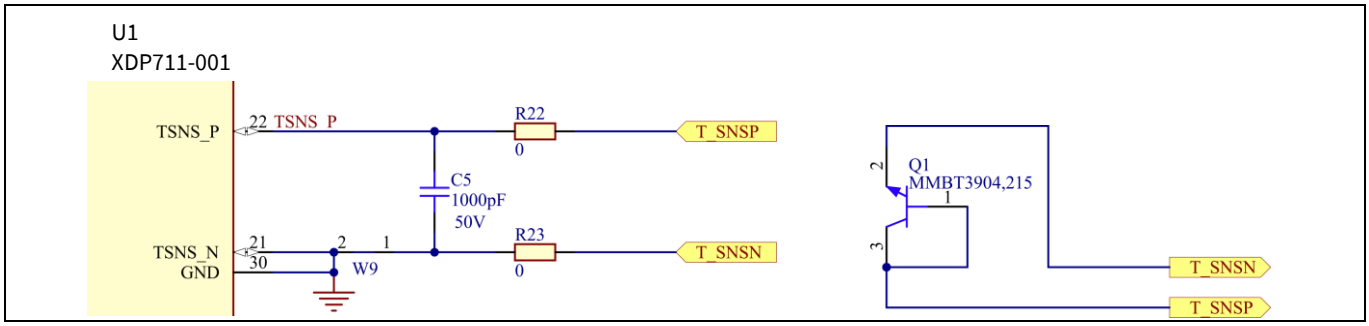

Figure 9 Schematics of temperature sense for XDP711-001

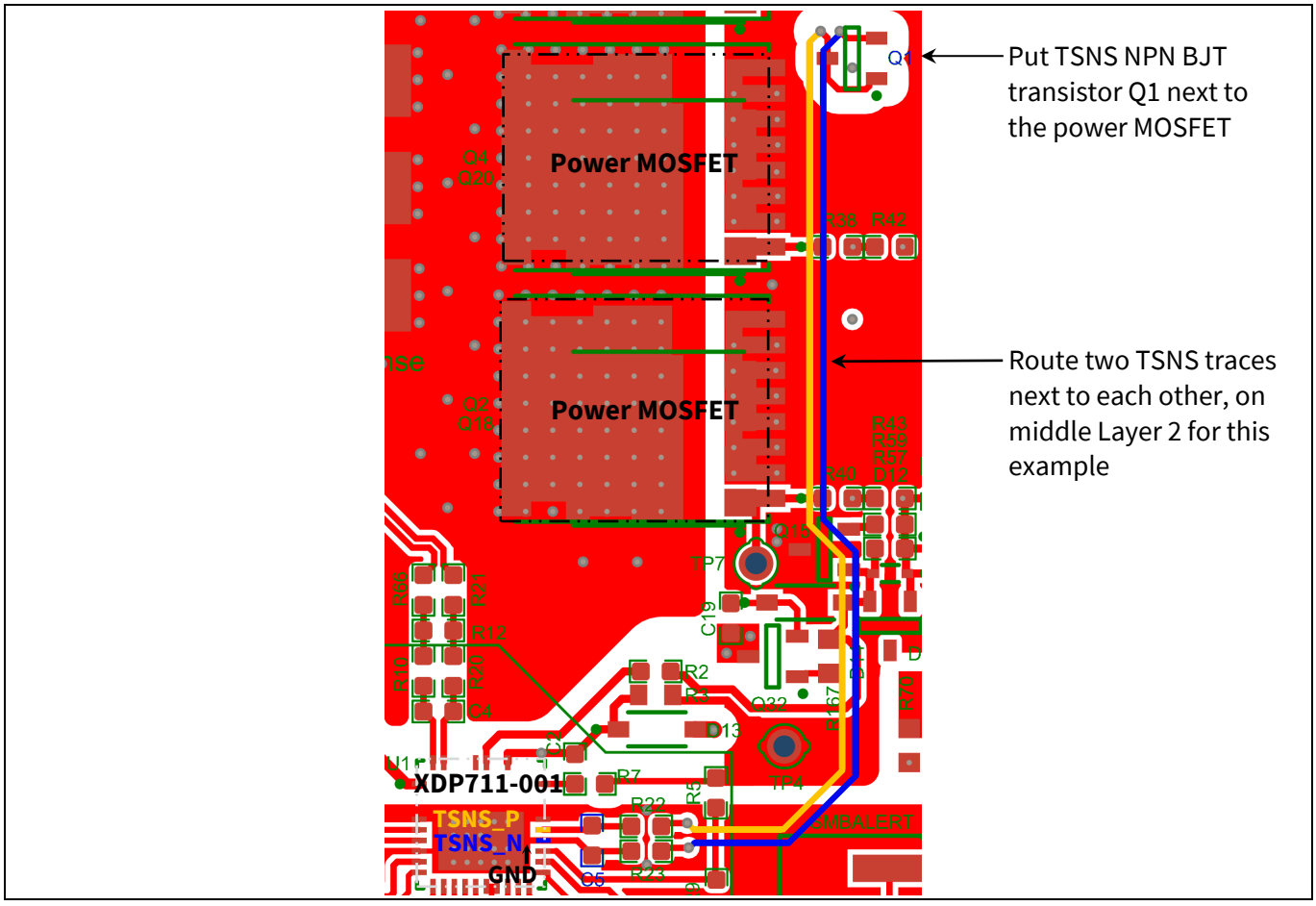

Figure 10 Top layer (red) and middle layer 2 (gold and blue TSNS traces only)

The recommended PCB layout guidelines are:

1. Put the TSNS BJT transistor (Q1) next to the power MOSFET or the point to be sensed
2. Route two TSNS traces next to each other, on the middle layer for this example
3. Put the TSNS filter capacitor (C5) near the TSNS_P and TSNS_N pins of XDP711-001
4. Connect TSNS_N pin to the exposed pad of XDP711-001 directly

2.5 Power MOSFETs

Figure 11 displays the schematics of the external power MOSFETs (using IPT017N10NM5LF2 [6] as example). Figure 12 shows the PCB layout on the top layer following the recommended layout guidelines. Some power MOSFETs and gate resistors (Rg resistors) are on the bottom layer but not shown here as the layouts are similar.

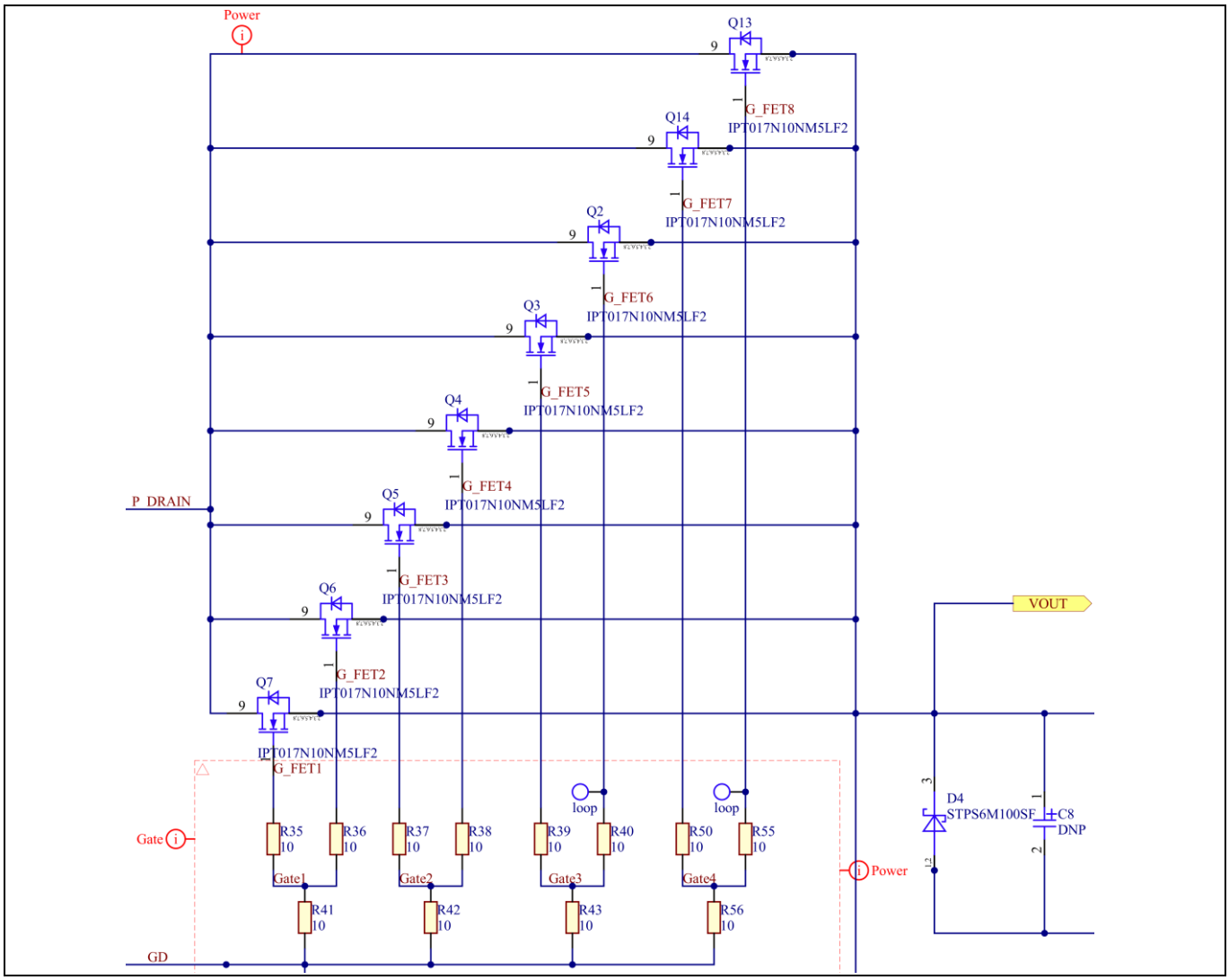

Figure 11 Schematics of power MOSFETs and gate resistors

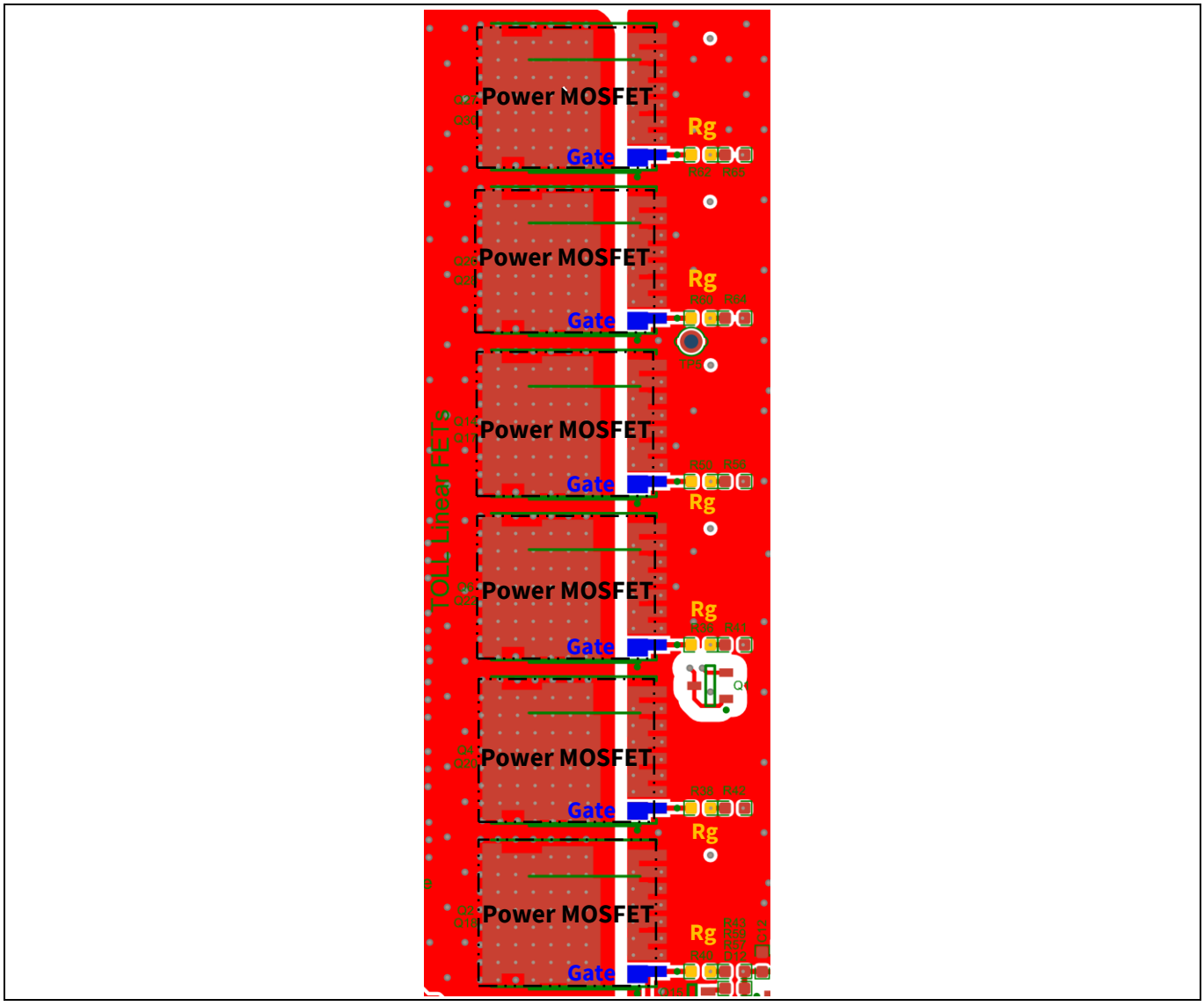

Figure 12 Power MOSFETs and Rg resistors on top layer

The recommended PCB layout guidelines are:

1. Put the Rg resistors next to the gate pins of the corresponding power MOSFETs
2. Use solid and direct connections for the drain and source of the power MOSFETs for high load current
3. Put as many vias as possible for the drain and source of the power MOSFETs for solid connections of high current paths to other PCB layers

3 PCB layout example

A PCB layout example of a 4 kW reference design for XDP711-001 or XDP710-002 hot-swap applications are shown in Figure 13 to Figure 18, where all the PCB layout guidelines in this application note have been followed.

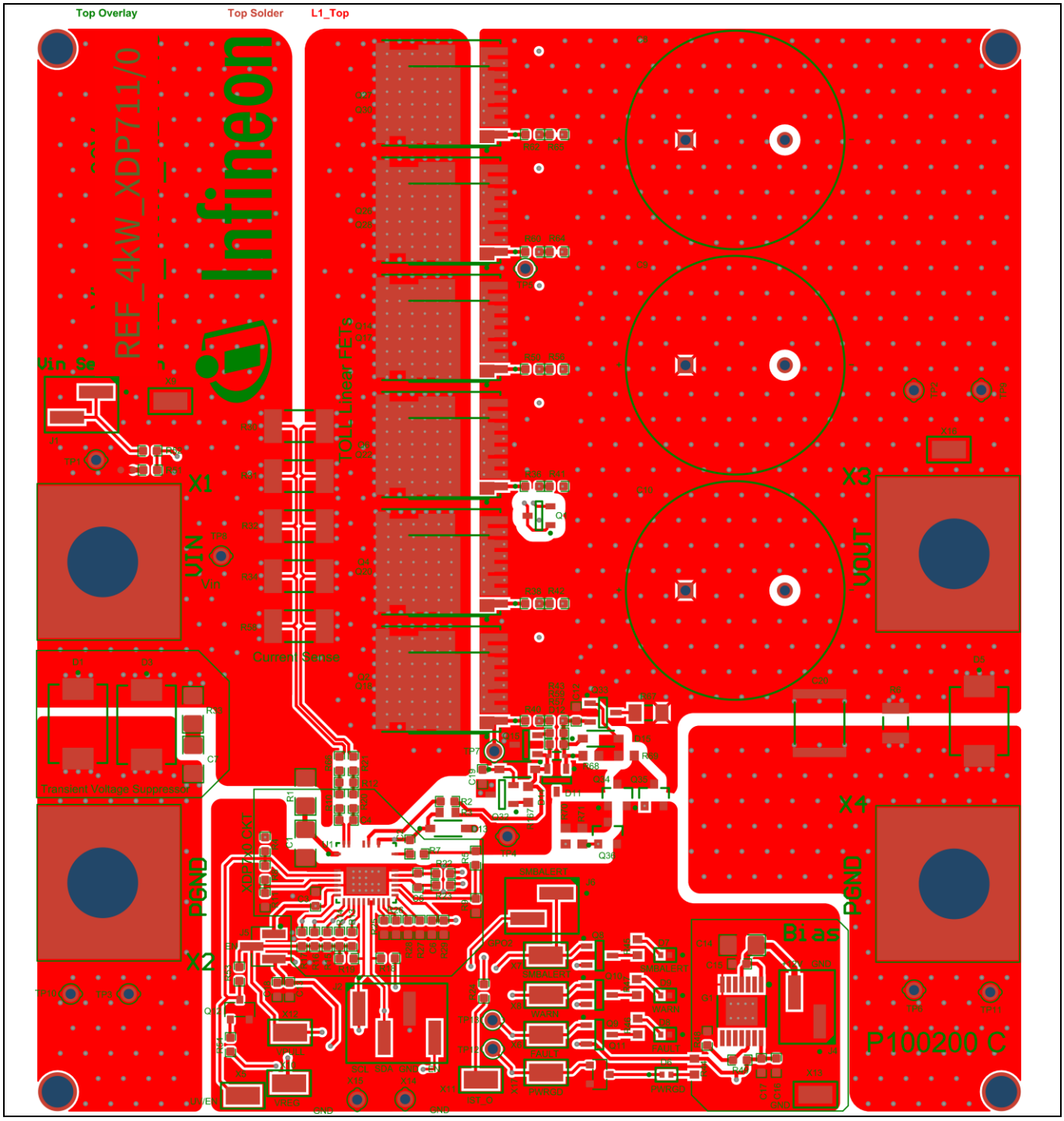

Figure 13 PCB top layer

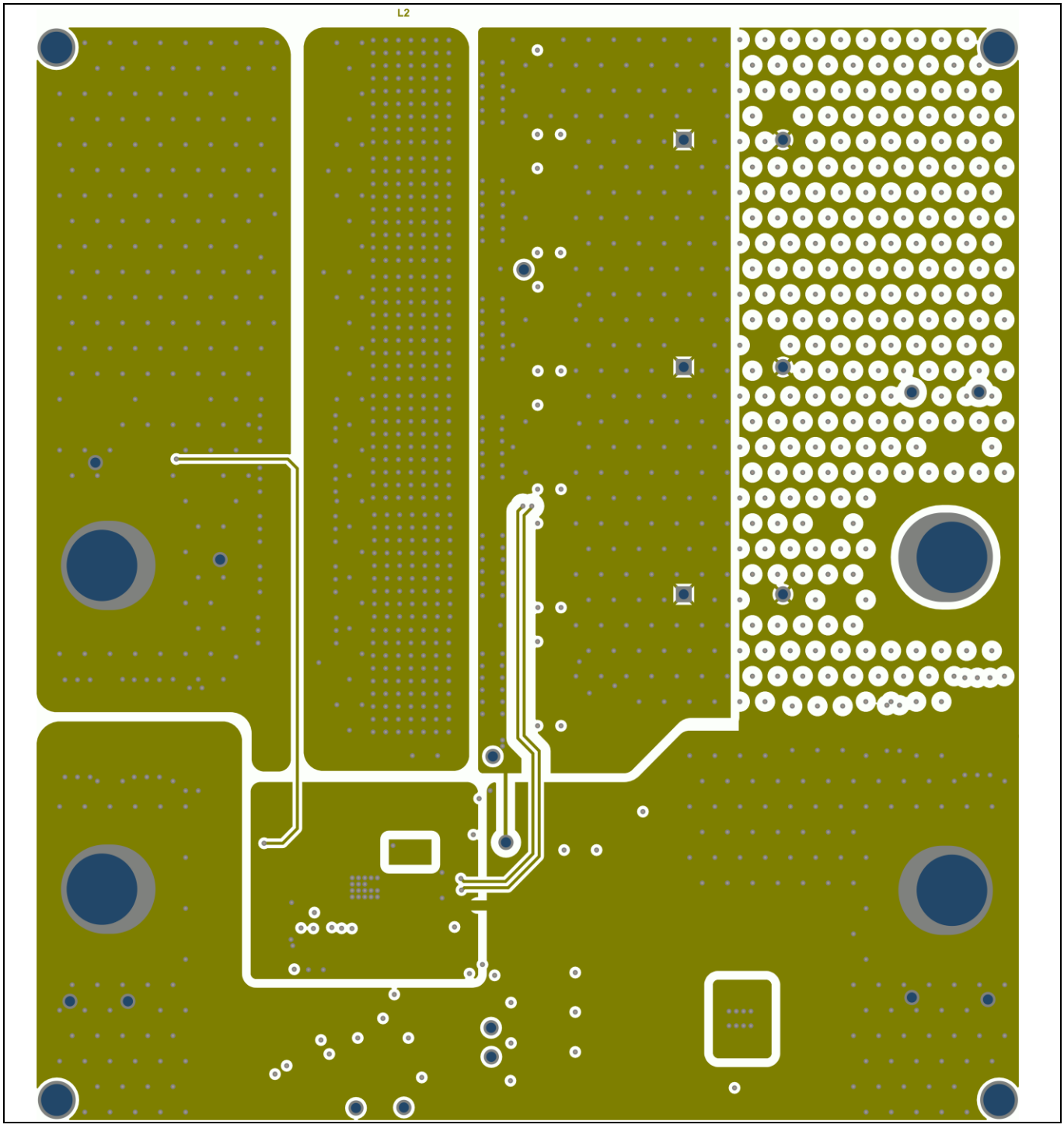

Figure 14 PCB middle layer 2

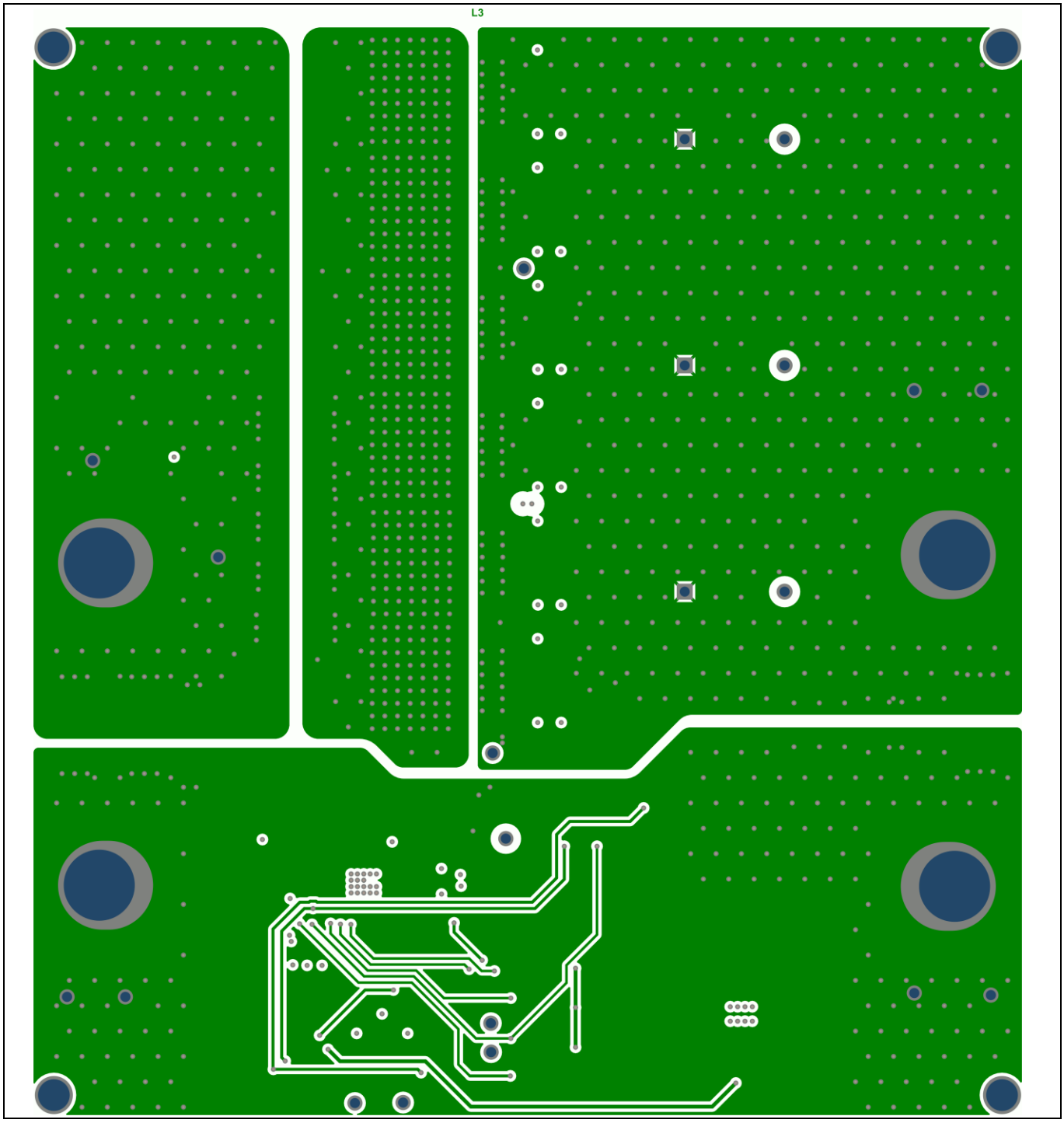

Figure 15 PCB middle layer 3

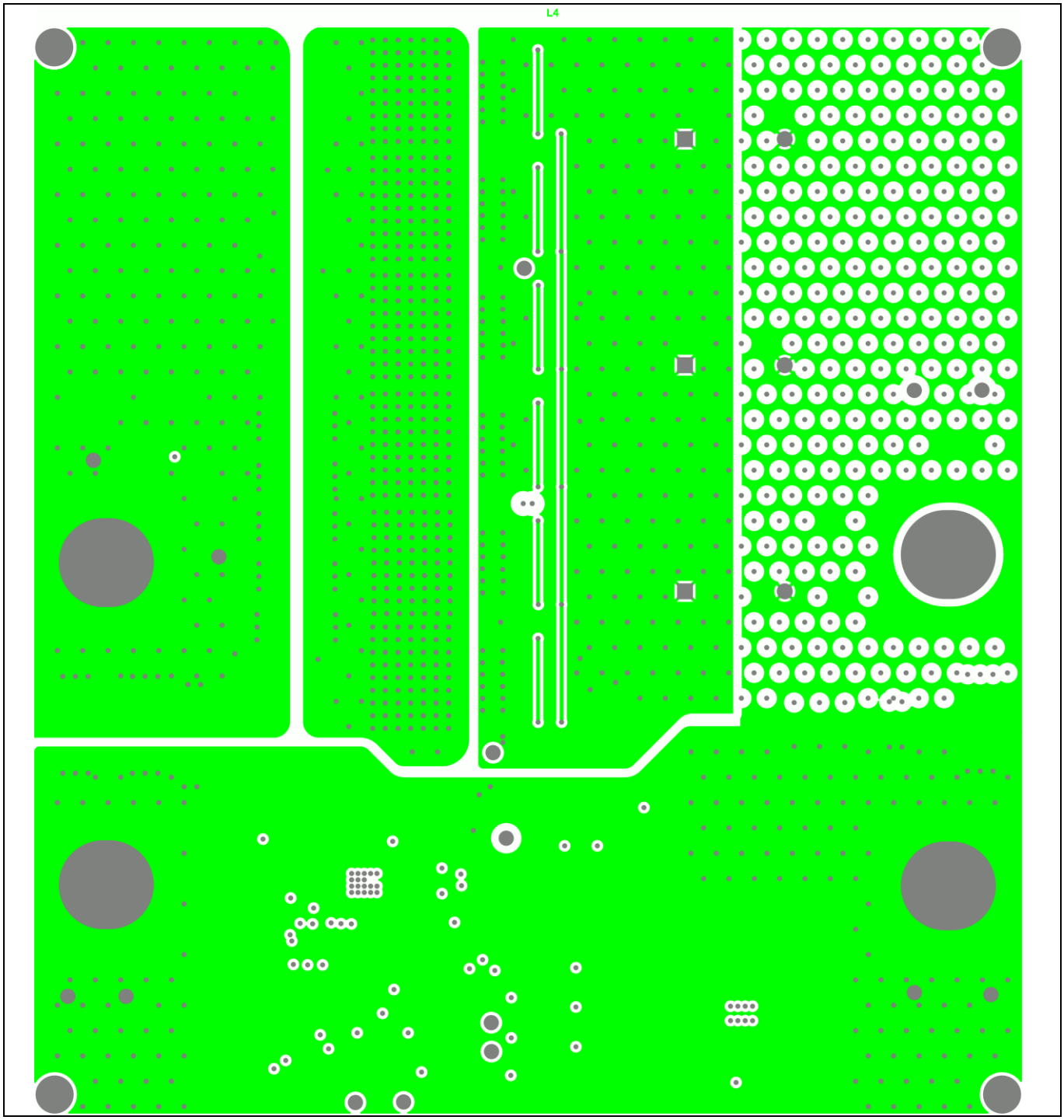

Figure 16 PCB middle layer 4

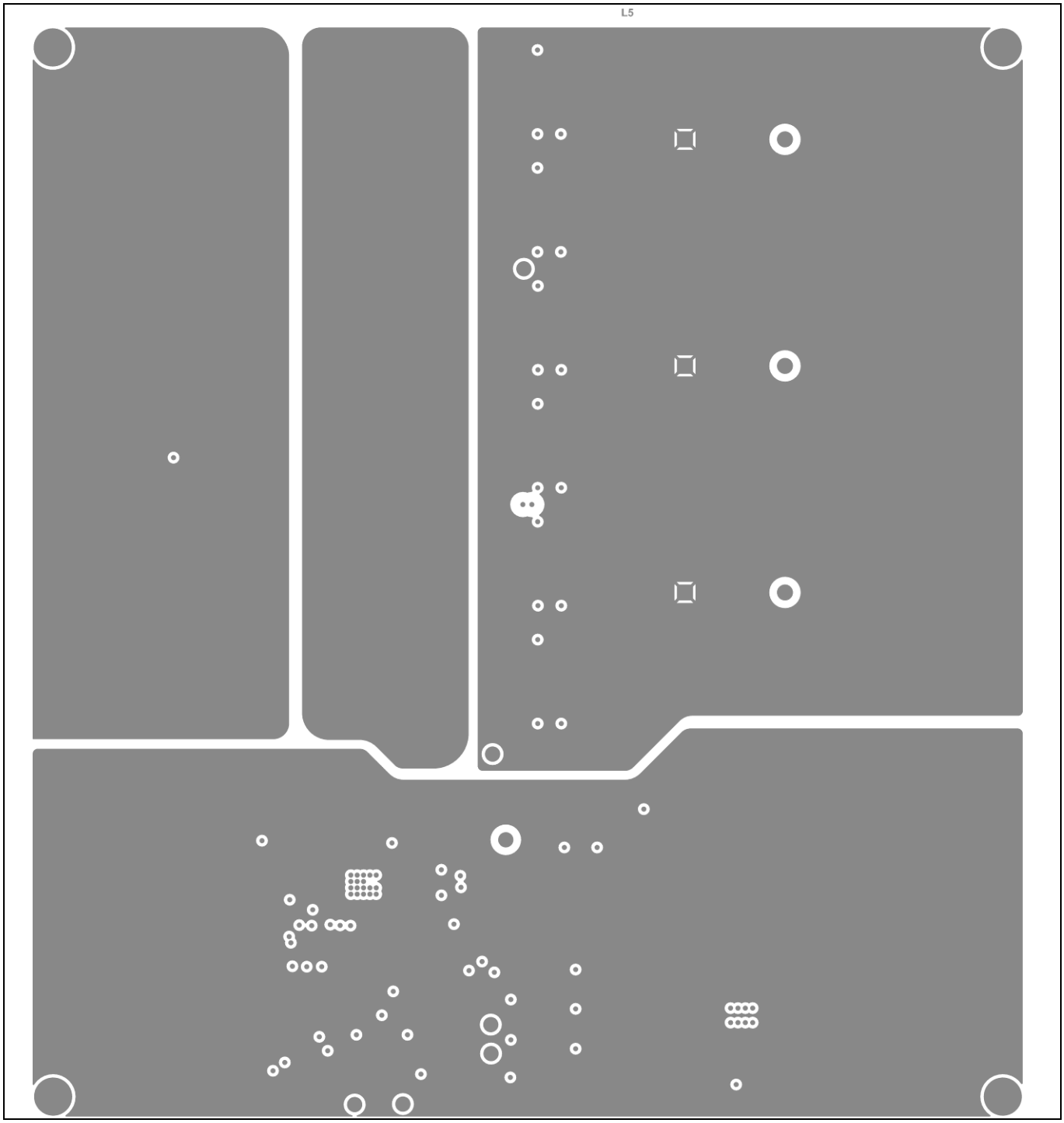

Figure 17 PCB middle layer 5

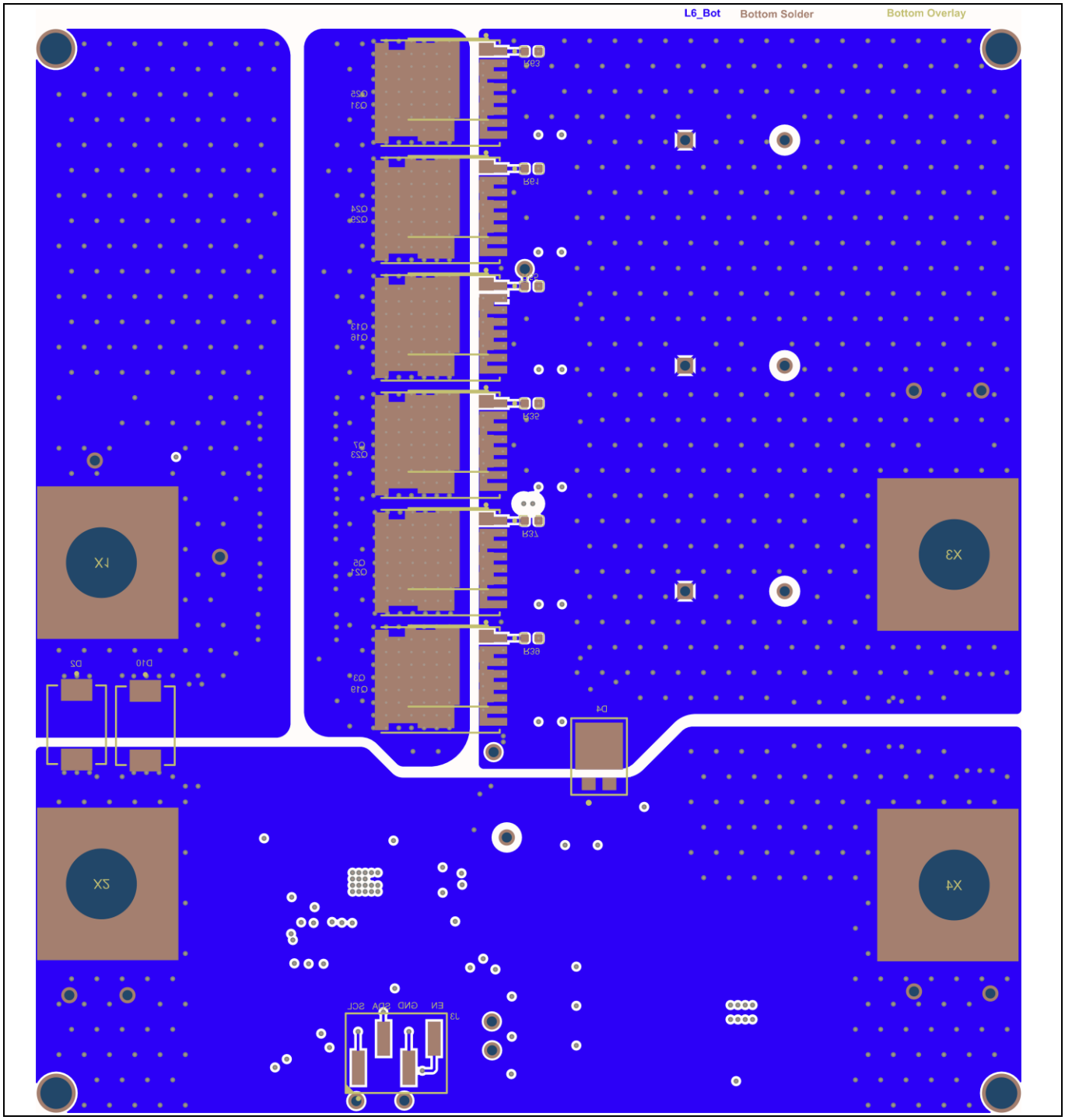

Figure 18 PCB bottom layer

4 Summary

The PCB layout is a critical part of the design for XDP7xx-00x hot-swap applications. PCB layout guidelines for the gate driver including VCP pin, current sense, power supply, temperature sense, and power MOSFETs have been listed in this application note. Short and direct connections, shielding of XDP711-001 VCP pin, Kelvin connections, differential pairs layout for current sense and temperature sense, putting Rg resistor next to the gate pin of power MOSFET, and so on, are highly important to make the XDP7xx-00x hot-swap application boards to work as expected for the first time.

References

[1] Infineon Technologies AG: *AP24026, EMC and System-ESD Design Guidelines for Board Layout*; Available online

[2] Infineon Technologies AG, AI server hot-plugging with robust hot-swap controllers; Available online

[3] Infineon Technologies AG: XDP711-001 hot-swap controller datasheet

[4] Infineon Technologies AG: *XDP710-002 hot-swap controller datasheet*; Available online

[5] Infineon Technologies AG: *XDP700-002 hot-swap controller datasheet*; Available online

[6] Infineon Technologies AG: *IPT017N10NM5LF2 datasheet*; Available online

[7] Roger Hu, PCB Design and Layout Fundamentals for EMC, July 2019

Revision history

Document revision	Date	Description of changes
V 1.0	2025-04-21	Initial release

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