Versatile controlled resistive load model for simulation circuits

For use in current limited scenarios (designed for SIMetrix[1]/SIMPLIS[2])

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About this document

Scope and purpose

It is common to be faced with the task of simulating a transient load step, a start-up/shutdown scenario or a voltage change command that provokes a high dynamic current in the system, which is limited by the control function of the voltage regulator (VR). In such a case it is not possible to use a simple piecewise linearly defined load source to model the correct behavior. Here, the problem posed will be discussed and solutions will be shown both in general and specifically for simulations with SIMetrix[1] and SIMPLIS[2].

Intended audience

Design engineers, field application engineers and developers of VR systems who need to simulate the behavior of the VR in current limited scenarios.

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1 Introduction

Transient simulations are often used to predict and analyze the response of a VR to a load transient. This is especially important for very dynamic voltage regulator applications, such as multiphase synchronous buck regulators for high currents and low voltages that require the controller to be capable of very fast and precise response to overcurrent situations, and a corresponding model to show these functions working in simulation. Infineon provides controller models for its XDPE15xxx, XDPE19xxx, XDPE1Axxx, XDPE1Bxxx and further generations of multiphase core voltage regulators.

Aside from the aforementioned specific application, the load model described in this application note is very versatile and can be used in a great variety of applications like any other voltage regulator (e.g., point-of-load (POL), telecom, chargers/adapters), and for the simulation of protection and limiting circuits (e.g., Oring, eFuse).

Using simulations for VRs, the feedback loop can be tuned, and non-linear control options can be investigated. For example, shutdown and various overcurrent scenarios require a different response than the simple voltage regulation strategy. They also need a load resembling the passive load that is mounted on the real application board rather than the very conveniently used current sink for steady-state operation and feedback loop tuning.

This application note discusses the setup of a proper resistive load with considerations for compatibility to quickly change it into a current sink.

The current sink is usually faster, more stable and supported by piecewise linear sources available in every SPICE library. However, when the VR detects a current at the sink that is too high, it will reduce power delivery by lowering the output voltage. Since the current sink is not diverting from the current it was set to sink, the output voltage of the VR drops quickly and becomes negative. Depending on the type of VR model, it might be clamped to zero by a freewheeling path or it might run away entirely in the negative direction. This should be expected, and it indicates the inadequacy of the sink load model for such a simulation scenario.

Replacing the load with a resistive model will make it possible to conduct such a simulation. Here, we need a variable resistance model that acts properly on the current slope in regular operation while scaling the resistance over output voltage so that current limiting can occur.

2 Solution

2.1 General solution

The load model has to be a controlled resistance, replicating the load resistance of a dynamic load. Usually the simulation specification is given:

- VID setpoint (voltage identification at no load)
- Loadline (voltage as a function of load current expressed as a resistance)
- Bias load (DC load)
- Load step (transient load step in magnitude and transition rate (slope))

Having a piecewise linear current source as a load sink model only considers the last two input aspects, forcing the output voltage out of regulation.

$$Vout(t) = Vout(t=0) - \frac{t \cdot (I_{sink} - I\_VR)}{C_{out}} \quad \textit{eq. 1}$$

When I_VR is current limited, V_{out} decreases at a rate given by the load sink current and the output capacitance in the model.

The real application, however, would reduce the output current as the output voltage decreases because the load is passive.

$$R_{load} = \frac{Vout(@I_{load})}{I_{load}} \quad \textit{eq. 2}$$

The average load current is equal to the current delivered by the VR.

The output voltage is dependent on the VID, the load current and the loadline.

$$Vout = VID - I_{load} \cdot LL \quad \textit{eq. 3}$$

Therefore, the target for the load resistance value can be expressed as:

$$R_{target} = \frac{VID - I_{load} \cdot LL}{I_{target}} \quad \textit{eq. 4}$$

This target resistance must be considered a physical limitation of the load, meaning that it:

- will never become negative, and
- could change the value dependent on the voltage.

For the model it will be considered to define a minimum supply voltage up to which the load follows a target current and increases in resistance when the load voltage drops below this voltage threshold. In addition, the model should support a tightly set target resistance if configured.

The calculated load resistance will be dependent on V_{out}, I_target and V_min with V_min being the aforementioned minimum supply voltage.

In general, the calculated resistance must follow the target resistance unless it is falling below the specified limit set by the constraints.

$$\mathrm{R_{calculated}} \geq \mathrm{R_{minimum}} \quad \textit{eq. 5}$$

For example, having I_{out_max} = 100 A, *LL* = 1 mV/A and *VID* = 1 V would result in *R_minimum* = (1 V-(100 A x 1 mV/A)/100 A) = 9 mΩ. Without consideration of an undershoot of 50 mV, the load current would drop to *I_load* = (0.9 V – 0.05 V)/9 mΩ = 94.4 A.

Considering all this, the calculated load resistance must take the undershoot into account.

$$\mathrm{R_{minimum}} = \frac{\mathrm{VID} - I_{out\_max} \cdot \mathrm{LL} - \mathrm{V_{US_{margin}}}}{I_{out\_max}} \quad \text{eq. 6}$$

I_{out_max} is the maximum output current that the load can draw.

V_US_margin is the undershoot margin after the transient event at which the maximum current must be supported.

If we know the load resistance description, we can think about its realization in a simulation environment.

Switching resistors in and out of the circuit introduces non-linear transitions diverting from the target solution. Going into a digital resistance implementation would add a lot of complexity without helping to give a speedy and accurate simulation. Therefore, the use of a controlled current source is a better way to describe the resistance. Instead of responding to the target current input directly, it will be controlled by the calculated target resistance (*eq. 7*) and the actual output voltage.

$$I_{load} = \frac{Vout}{\mathrm{R_{calculated}}} \quad \text{eq. 7}$$

From here one can see that this value can never become negative, as the current will proportionally be reduced to the output voltage in case the VR is limiting the current.

All that is needed to implement this resistive load model is to translate *eq. 6* and *eq. 7* into a circuit setup.

2.2 Solution for SIMetrix

In SIMetrix these equations can be combined and placed into a “Non-linear transfer function” block describing output current as a function of VID, LL, output current and target current.

$$I_{load} = \frac{Vout}{max\left(\frac{abs(Vout)}{abs(I_{target})}, R_{minimum}\right)} \quad \text{eq. 8}$$

To prevent any division-by-zero errors, the equation was implemented with a negligible added current term. Also, the calculated resistance was reduced to the positive range and a small offset was added to avoid any division-by-zero errors.

$$I_{load} = \frac{Vout}{max\left(\frac{\mathrm{abs(Vout)}}{0.001+\mathrm{abs}(I_{target})}, \mathrm{R_{minimum}}\right)} \quad \text{eq. 9}$$

For the calculation of *R_minimum* it must be ensured that this is a strictly positive value.

The load component can be set up as a three-terminal device. The load is connected between “LOAD” and “RTN”. The target current will be set external to this component using a piecewise linear voltage source to describe the current and connect to “I_target” with reference also to “RTN”.

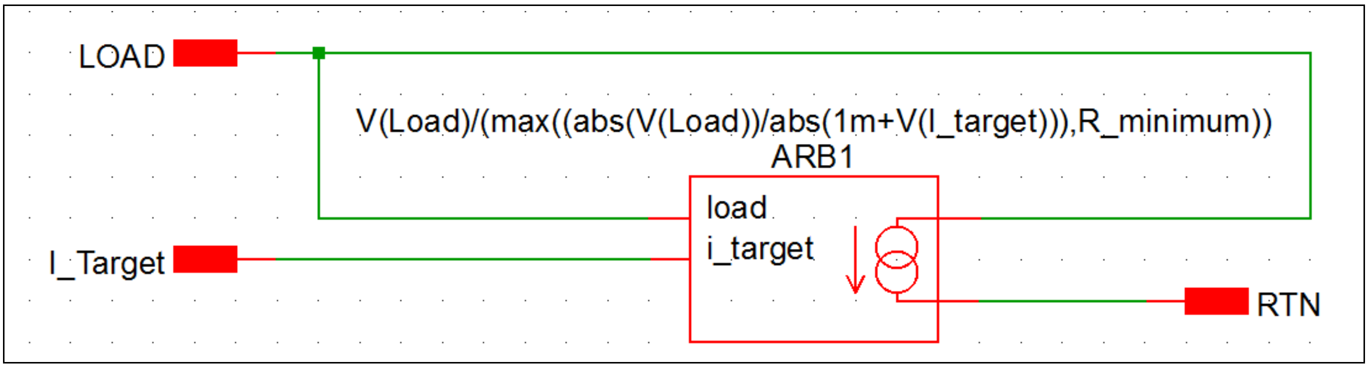

Figure 1 **Resistive load model for SIMetrix**

In a simulation that is not current limiting, it is desirable to have the ability to switch over into a simple current sink mode. This can be done by driving a voltage-controlled current source in parallel and using a parameter to select the resistive load when needed. In this example, the parameter "USE_RESISTIVE_LOAD" was introduced. If set to "1" then the resistive load defines the current; if set to "0", the current sink is used.

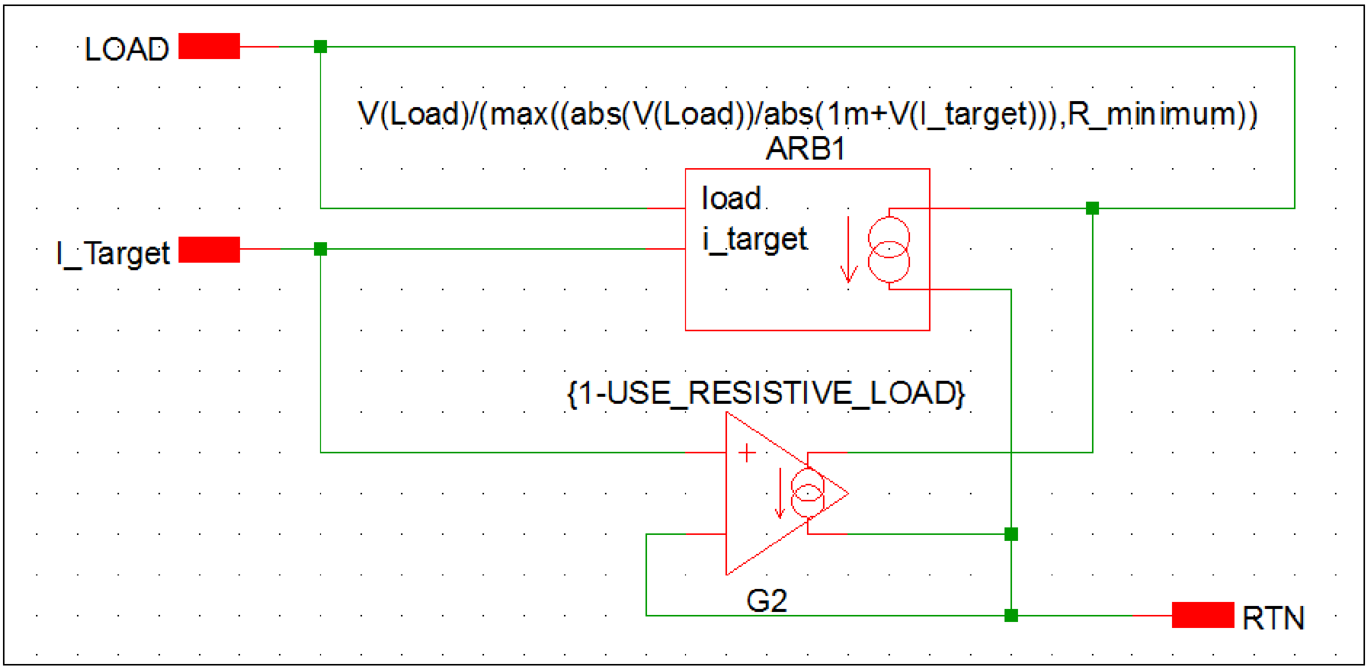

Figure 2 **Combined load model for SIMetrix**

2.3 Solution for SIMPLIS

In SIMPLIS the equations are equally valid but the implementation is more difficult. SIMPLIS does not provide such a descriptive function block and the equations have to be built as a circuit. There are two divisions of time-variant circuit parameters that need to be executed. SIMPLIS provides special components to accomplish this but these components do not work when a POP analysis has to be performed. That means that the SIMPLIS model has to be divided into two separate models from the start. One will be the resistive model that never works with POP, and the other is the current sink model that will have to be used when POP analysis is required. Both models can reside within the same component but will never be invoked at the same time in the same simulation.

Figure 3 shows the implementation of the first part, calculating the variable resistance.

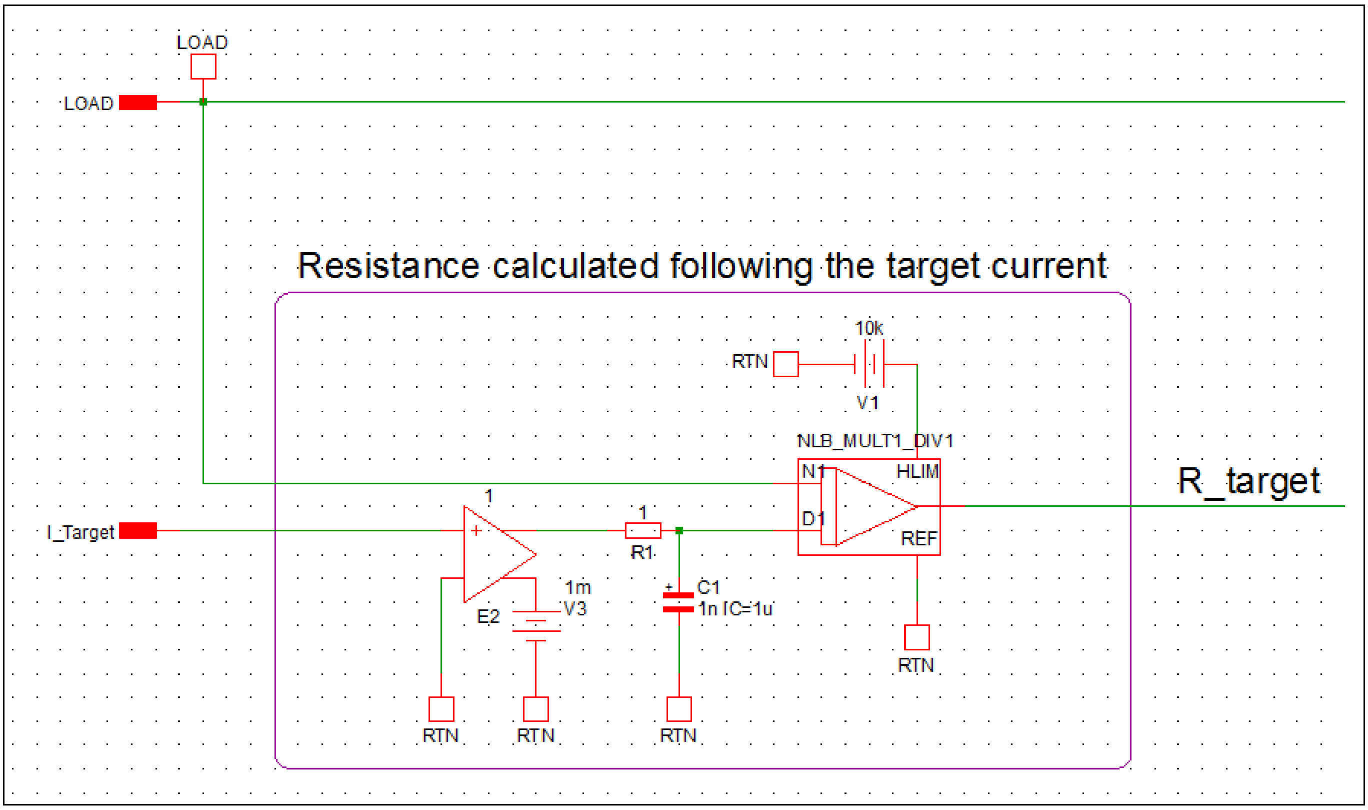

Figure 3 **Model to calculate target resistance in SIMPLIS**

The "NLB_MULT1_DIV1" component is responsible for the division. The voltage at "HLIM" sets an upper limit to the output; in this case 10 kΩ. Parameters for the divider block are set according to **Figure 4**. The small offset of 1 mA (V3) avoids a zero input to the denominator of NLB_MULTI1_DIV1.

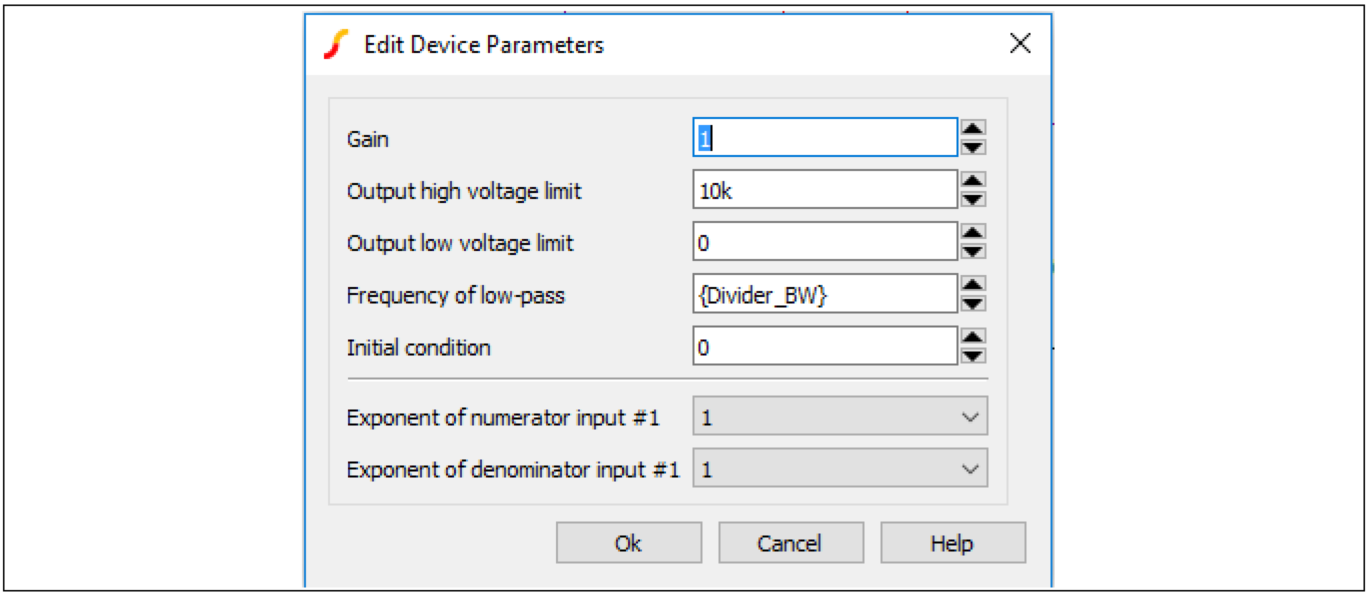

Figure 4 **Divider configuration in SIMPLIS**

The Divider_BW parameter sets the bandwidth for the divider and is a fixed parameter at the final model that can be changed if needed. The default is set to be 100 MHz. Reducing it will impact the response of the resistance calculation and hence introduce more delay into the resistive tracking. Higher-frequency values will lead to longer computation times and hence slower simulation speeds.

The low-pass filter (LPF) consisting of R1 and C1 was introduced in addition to the settings in the component itself because a rapid value change at the denominator input of the divider causes very small time constants and the simulation appears to be stuck without this filter. Its bandwidth is higher than the bandwidth in the filter block so as not to interfere with the operation.

The load current source calculation was set up by using a current limiter component and an identical divider as before, shown in **Figure 5**.

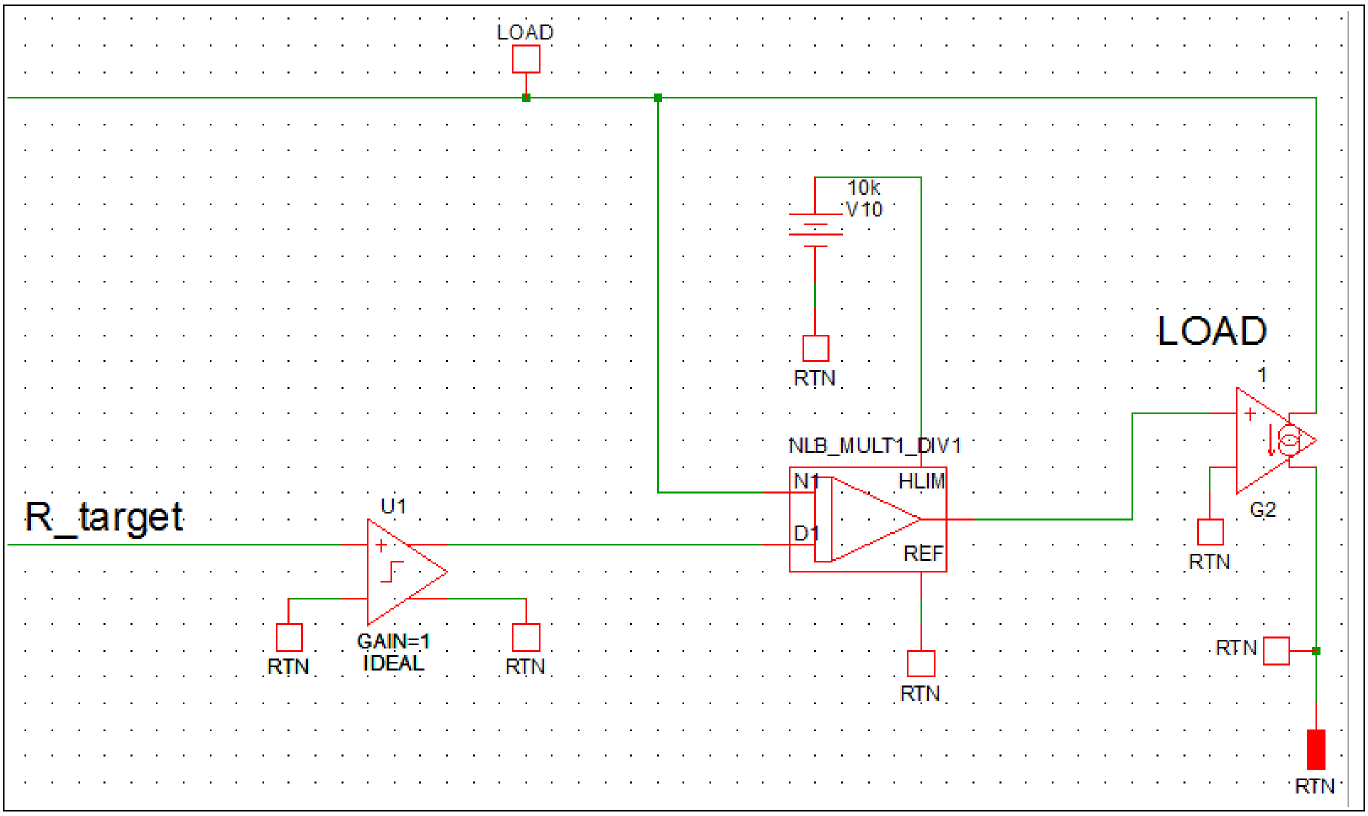

Figure 5 Resistive load source model in SIMPLIS

The voltage-controlled voltage source with limiter (U1) limits the minimum resistance to the calculated value.

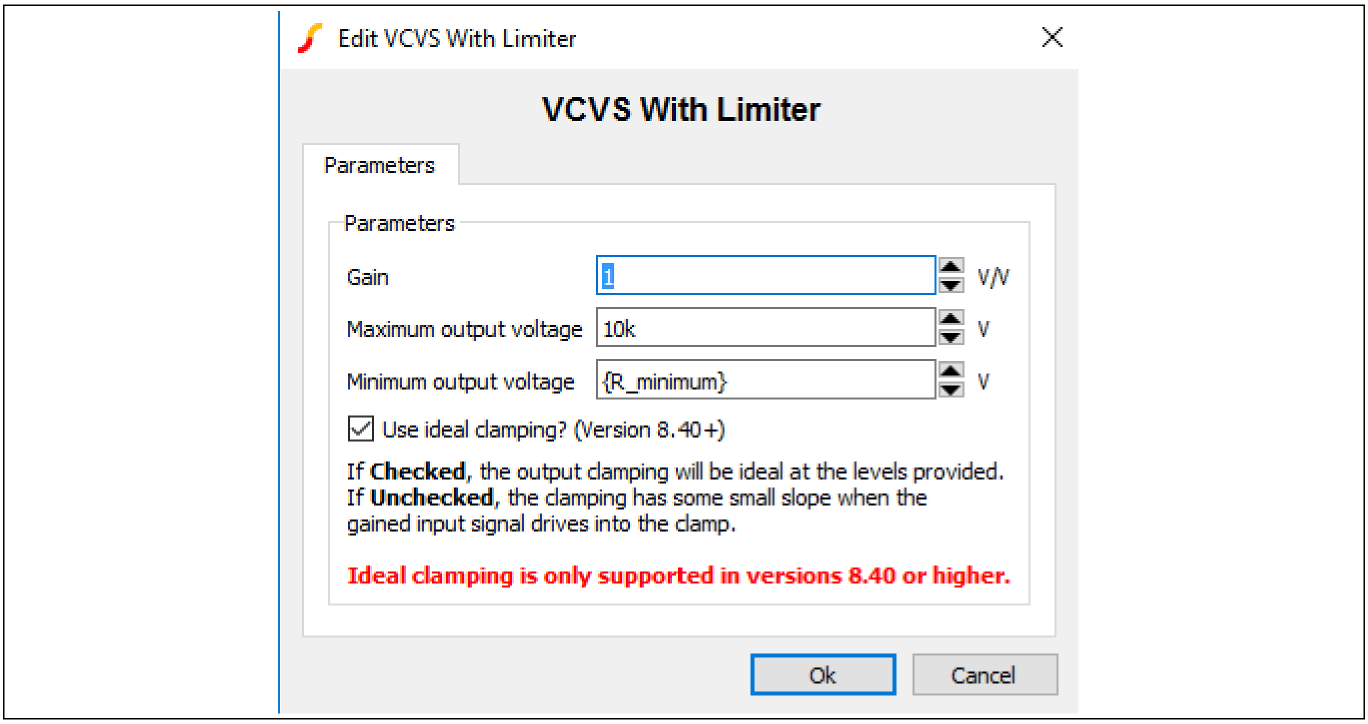

Figure 6 Resistance limiter in SIMPLIS

The recommended definition for *R_minimum* can be found in the listing for the F11 window.

F11 content

```
.if {V_min==0}
.var V_minimum={(VID - I_max*LL - V_US_margin)}
.else
.var V_minimum={V_min}
.endif
.var R_minimum ={max(1u,V_minimum/I_max)}
```

If the parameter *V_min* was set to be zero, then the resistance is calculated from the other inputs (*LL, VID, I_max and V_US_margin*). If it is non-zero, it directly defines the voltage for the maximum current given in *I_max*.

After combining these circuits, the resistive SIMPLIS load model emerges.

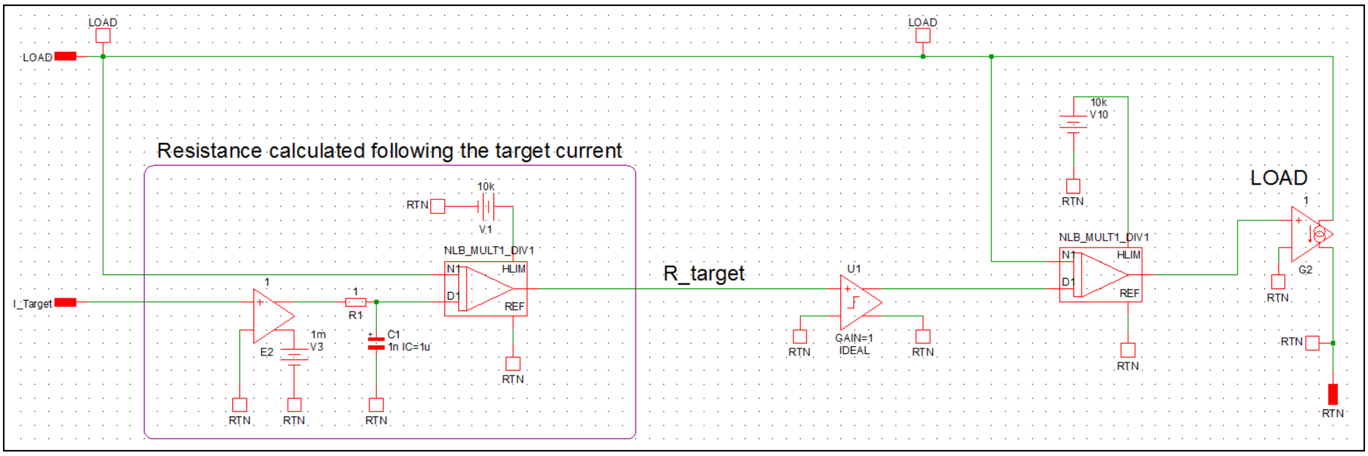

Figure 7 Resistive load model for SIMPLIS

As stated before, the conventional current source-based load model remains a non-replaceable part for some simulations in SIMPLIS and is set up in the same three-terminal component as shown in **Figure 8**.

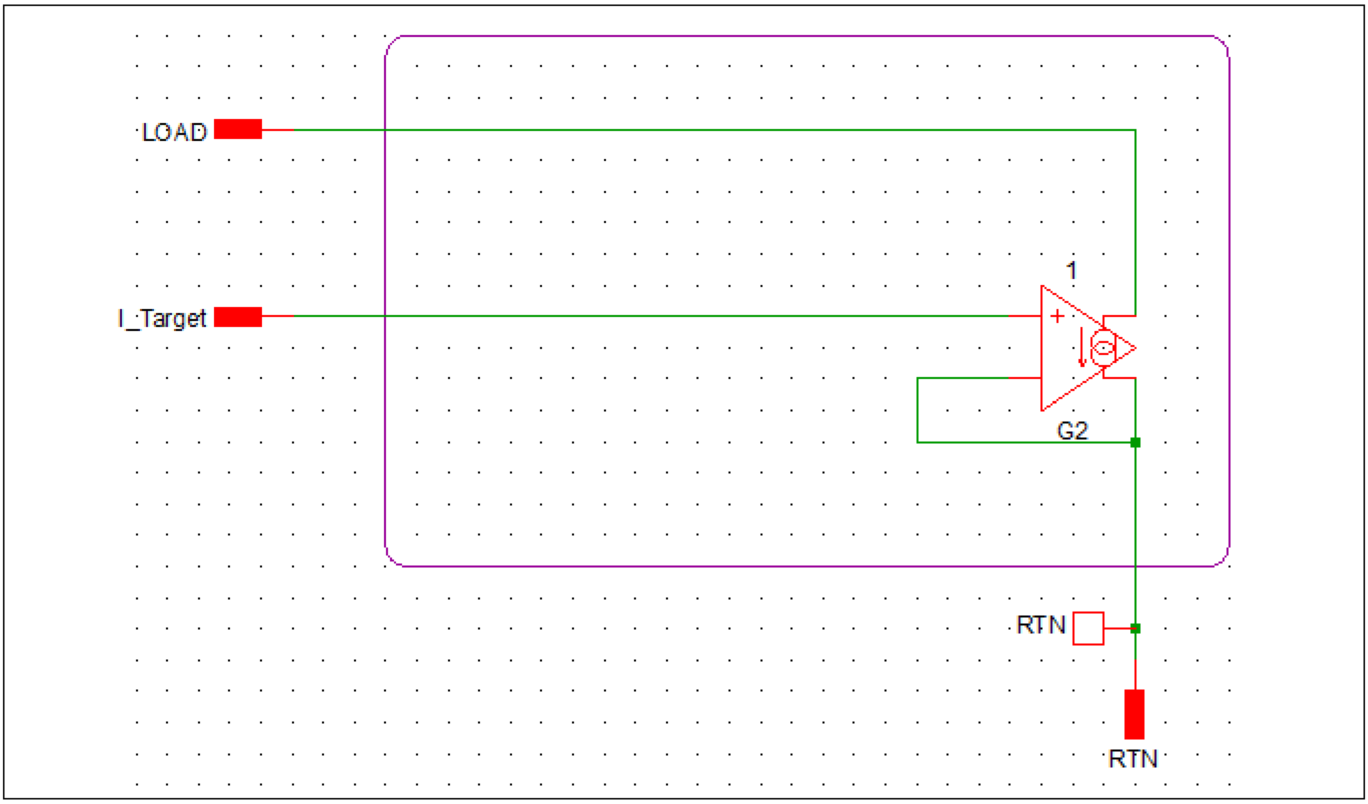

Figure 8 Current source model for SIMPLIS

Its effect is the same as using a PWL current source as a load sink directly. But this implementation allows the definition of the PWL to be made externally to this component for all load source and simulation types.

2.4 Combining all circuits into one component

A single three-terminal load component can now be defined to host the three models, as shown in **Figure 9**.

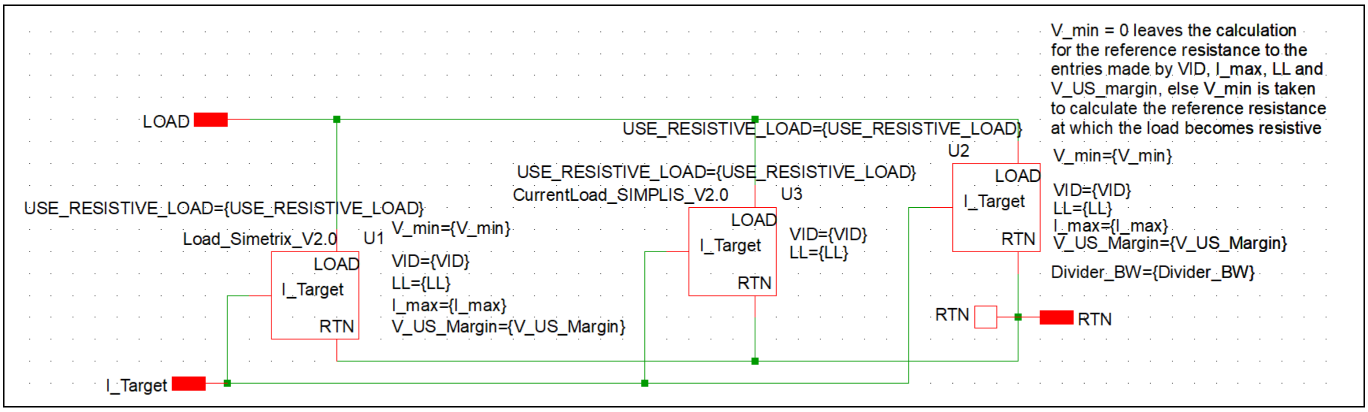

Figure 9 Load wrapper combining the different models in one component

This component can then be used as a universal load in any SIMetrix/SIMPLIS circuit. The SIMetrix model uses the "TEMPLATE" property definition while the SIMPLIS models follow the "SIMPLIS_TEMPLATE" property entry.

To determine the SIMPLIS model to be used, the parameter "USE_RESISTIVE_LOAD" is evaluated within the "SIMPLIS_TEMPLATE" entry and invokes only one of the models at a time.

Further refinements used in the component are:

- Double-clicking to toggle the switchover between the models using a script while also providing a message in the SIMetrix command shell about the model used
- Evaluation of the global system-generated variable "HAS_POP_ANALYSIS" to always use the current source as a load model when POP analysis is enabled

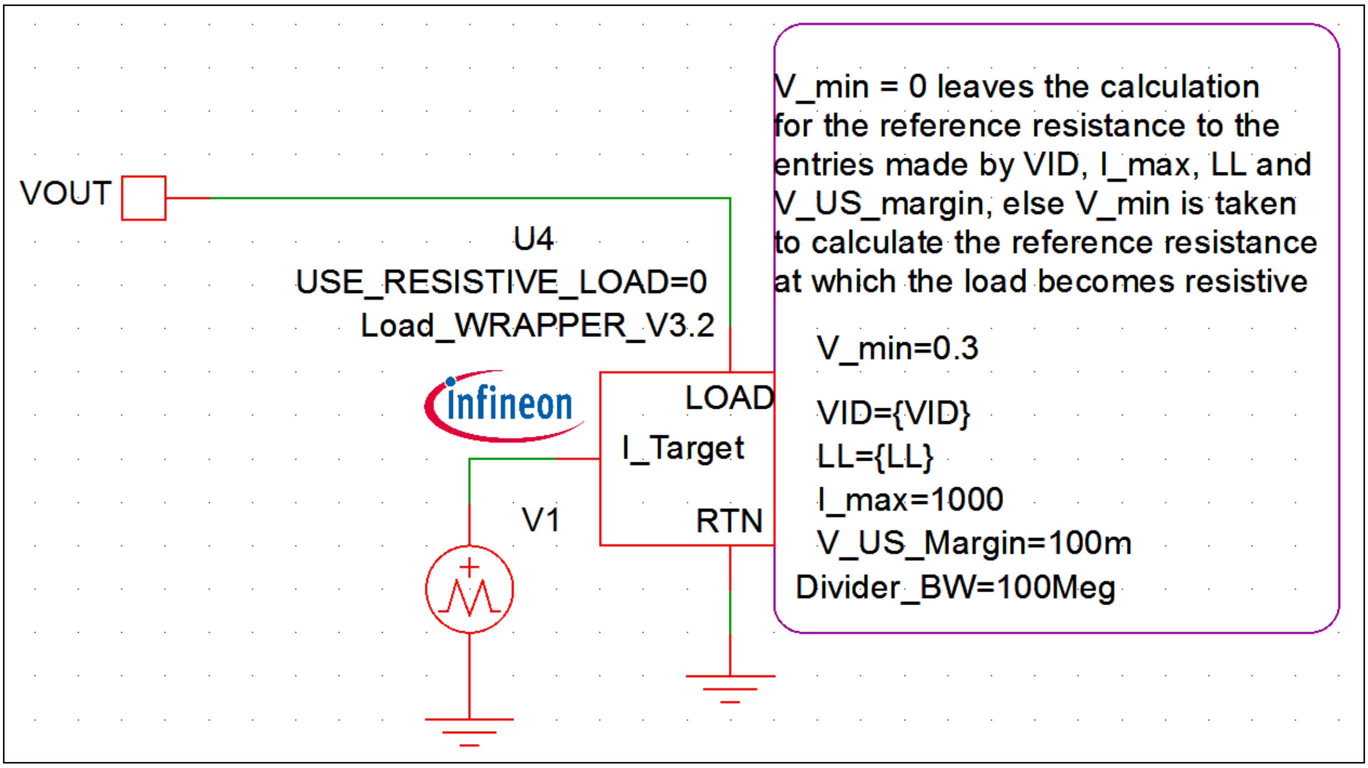

Figure 10 **Load component with all parameters and macro functionality**

In the case of **Figure 10**, the PWL current source that would normally have been used as a load directly is now substituted by a PWL voltage source for the new load model.

3 Simulation results

Figure 11 shows the simulation results on a setup observing a current step from 10 A to 1000 A followed by an output voltage (V_{out}) reduction at 70 µs simulation time.

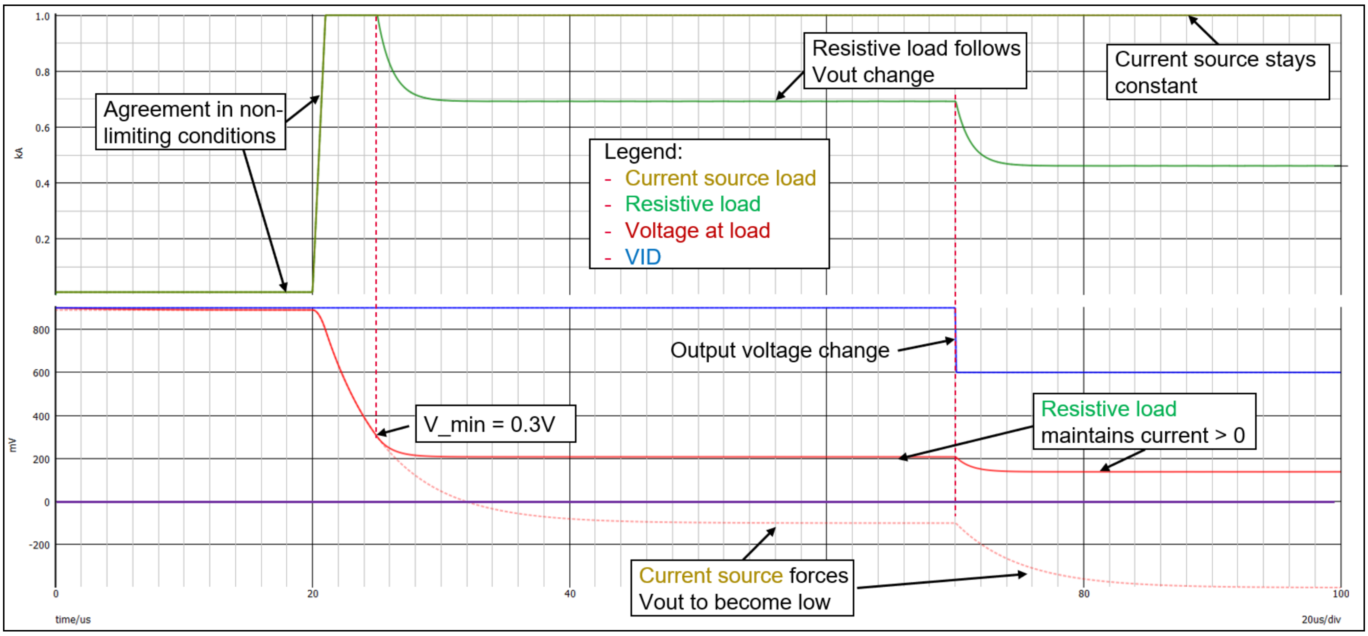

Figure 11 Simulation results comparing a current source load vs. a resistive load

Both load models agree on the waveforms during non-limited operation until the voltage is insufficient to drive the 1000 A and the current drops as a result in the resistive load model. At the 70 µs mark the output voltage is commanded to further reduce (simulating a current limit event, for example). At this point, the resistive load current drops further as V_{out} decreases.

The output voltage with the resistive load model always stays positive, while in the constant current model the output voltage drops and becomes negative.

SIMPLIS and SIMetrix runs deliver comparable results.

4 Conclusion

Despite the convenience of a current source as load there are limitations to its application. As outlined in the application note it is mandatory to use the correct load model for the targeted simulation run. In the case of investigations of output voltage changes as a result of the control loop limiting the current, the load must be set up as a resistive load to obtain reasonable simulation results.

This application note has shown how to implement the resistive load in general, as well as specifically for use in SIMetrix and SIMPLIS. For the latter, one common component can be created to work with all circuits in SIMetrix/SIMPLIS.

With this model it is now possible to simply toggle from a current sink to a resistive load on the provided simulation models for the Infineon controller families of XDPE15xxx, XDPE19xxx, XDPE1Axxx and XDPE1Bxxx voltage regulators, enabling the fastest setup for the best load option to retain maximum simulation speed. The various current limit functions can now be fully evaluated using only one model with uncompromised performance.

References

[1] SIMetrix Technologies Ltd.: *SIMetrix simulation software*; **Available online**

[2] SIMPLIS Technologies Inc.: *SIMPLIS simulation software*; **Available online**

Revision history

Document revision	Date	Description of changes
V 1.0	2023-05-11	Initial release

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