1ED324xMC12H, 1ED325xMC12H - Technical description

High voltage, isolated, two-level slew-rate control gate driver IC

1ED324xMC12H, 1ED325xMC12H

Two-level slew-rate control gate driver

About this document

Scope and purpose

This document gives an overview on the basic behavior and application related considerations of the 1ED32xx family listed in the table below. The document describes in particular the dimensioning of external components, which are used in the typical application.

Table 1 2-level slew rate control 1ED32xx family

Sales code	UVLO level	typical peak output current and configuration	Slew-rate control	Certified repetitive peak isolation voltage V_{IORM}
1ED3240MC12H	12.5 V	10 A, standard	turn-on and turn-off	VDE (reinforced): 1767 V
1ED3241MC12H	12.5 V	18 A, standard	turn-on and turn-off	VDE (reinforced): 1767 V
1ED3250MC12H	12.5 V	10 A, Miller clamp	turn-on	VDE (reinforced): 1767 V
1ED3251MC12H	12.5 V	18 A, Miller clamp	turn-on	VDE (reinforced): 1767 V

Intended audience

The intended audience include hardware design engineers of power electronic systems.

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1 Introduction

The 1ED32xx family offers two outputs *OUT* and *OUTF*. The activation of the second output *OUTF* depends on the input signals V_{IN} and $V_{/INF}$. The activation criteria of the second output can be a function of the system´s temperature or of its load status.

The 1ED32xx family is a group of galvanically isolated single channel driver ICs in a DSO-8 300 mil package. The driver ICs provide typical peak output currents up to 6 A per output. The family comprises standard output configurations and active Miller clamp output configurations with the same current rating to protect against parasitic turn on.

The input logic terminals operate safely with supply voltages of 3.3 V and 5 V. All input structures have threshold levels support 3.3 V microcontrollers. The driver IC family offers suitable output undervoltage lockout (UVLO) levels to operate various kinds of power transistors. The wide range of the output side supply voltage up to 40 V can be configured arbitrarily for positive and negative voltages as long as the absolute maximum of 40 V is not exceeded. All driver ICs have output sections with active shutdown.

Data transfer across the isolation barrier is done by the Infineon coreless transformer technology.

2 Input side

The input side contains two inputs *IN* and */INF* for the control signals and two power terminals *VCC1* and *GND1* for the reference and the supply of the input side. The output side contains the two outputs *OUT* and *OUTF* for the standard output configuration, and *OUT* and *OUTFC* for the clamp output configuration. The output side is supplied by terminals *VCC2* and *VEE2*. Both sides are described here in more detail.

2.1 Input side power supply

The supply voltage on the input side can range from V_{VCC1} = 3.3 V up to 15 V. This results in a large margin for spikes and coupling on the supply rail in non-optimal layouts with respect to the standard supply voltage of 3.3 V.

The supply voltage should be blocked by a suitable low-impedance capacitor including as well a low-impedance layout to the origins of the supply voltage. The capacitor should be placed in immediate proximity to the driver IC. This helps to stabilize the supply conditions of the IC input side and to avoid unnecessary UVLO events. This is important, because the datasheet´s specifications only apply to the operating range. The white shaded area in the figure below is the alleged supply stray inductance, which should be minimized as much as possible.

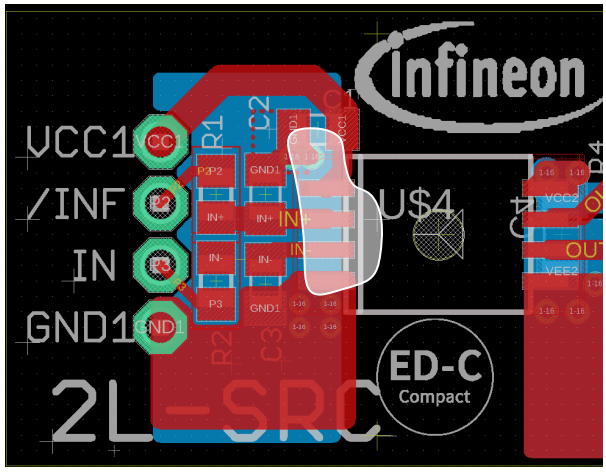

Figure 1 Correct layout for supply capacitor at terminal *VCC1*

2.2 Input terminals *IN* and */INF*

The input terminals *IN* and */INF* determine the behavior of the two output terminals *OUT* and *OUTF(C)*. While a PWM signal is connected to the IN terminal, thus determining the switching behavior of *OUT* and *OUTF(C)*, the */INF* terminal controls if only *OUT* or both *OUT* and *OUTF(C)* follow the input terminal *IN*. Since both output terminals *OUT* and *OUTF(C)* are connected to gate resistors, */INF* determines whether a single or both gate resistors are connected to an IGBT's gate.

Both input terminals contain a pull-down resistor to bias the IC into a safe mode in case the connection to the system control is interrupted. The non-inverting Schmitt trigger receives the input control signal and has CMOS-compatible trigger thresholds with minimum $V_{IN,L}$ for LOW level and maximum $V_{IN,H}$ for HIGH level. The input signal at terminal *IN* follows a positive logic, while the signal at terminal */INF* follows an active-low logic.

There is a short-pulse suppression filter after the Schmitt trigger with a filter time T_{INFLT}. All pulses that are below $T_{INFLT,min}$ will be suppressed, and pulses that are longer than $T_{INFLT,max}$ will pass the filter and be transmitted to the output side. External RC-filters with time constants of more than 10 ns, for example 1 nF and 10 Ω, have to be used to further support the integrated short pulse suppression function to filter input noise.

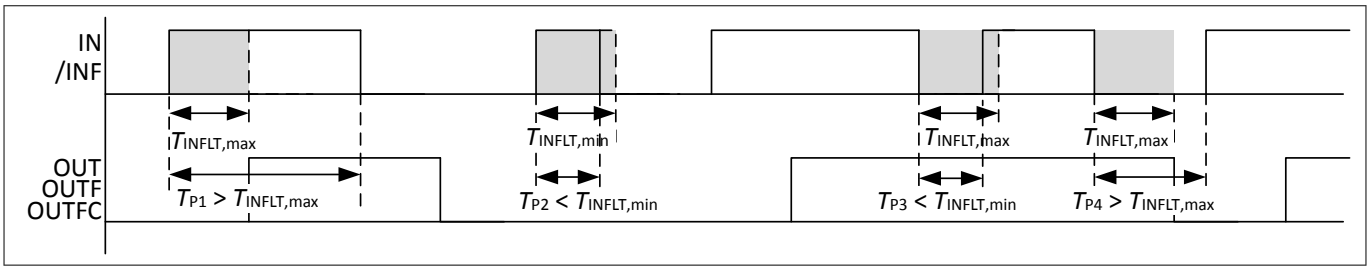

Figure 2 Timing of input signals with respect of the input filter

All changes at terminal */INF* are acknowledged, if they occur earlier than or simultaneously with a change at terminal *IN*. After a signal edge is applied at terminal *IN*, the signal at terminal */INF* has to be kept for at least $T_{/INF,hold}$ for its status to be transmitted to the output side.

2.3 Input side filtering

RC filters are a common for suppressing or reducing cross talk and parasitic coupling effects. Even best-practise layouts done by experienced engineers need external filters. However, external RC-filters are very imprecise and additionally their tolerance is asymmetric, as depicted in the figure below. This adds difficulties in the calculation of the dead time for half-bridge based power converters. The EiceDRIVER™ 1ED32xx IC family offers integrated noise filters with a symmetric tolerance and high precision. The integrated noise filters are important for reducing the external RC filter to a minimum, e.g. 10 ns, thus reducing tolerances to an absolute minimum. The performance of this combined solution is superior compared to gate driver ICs without integrated noise suppression filters.

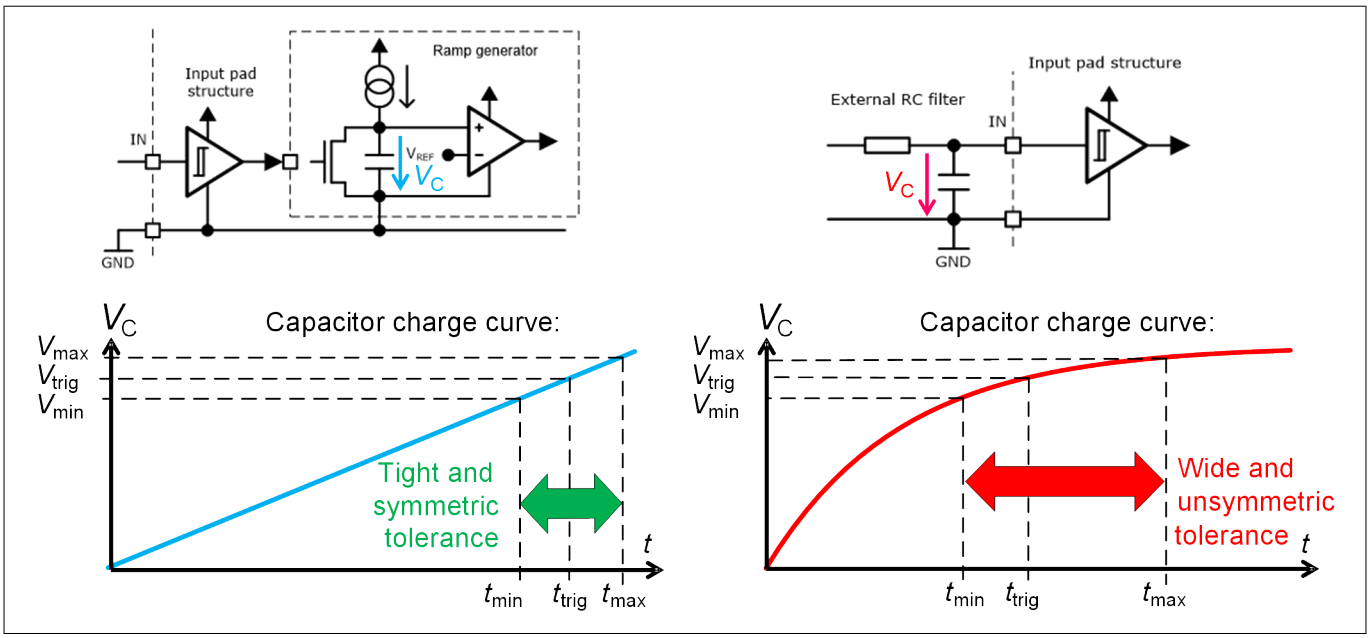

Figure 3 Tolerance of integrated filters (left) and external filters (right) for noise suppression

2.4 *IN* and */INF* timing

There is no specific timing necessary to be considered for the input control signals V_{IN} and $V_{/INF}$. Both can appear asynchronously at the terminals and will be processed as described in the datasheet. This also means that even a simultaneous change of signals at both control terminals will be processed correctly.

The only condition that has to be met is the so-called hold-time $t_{/INF,hold}$ of signal $V_{/INF}$. This timing is necessary in order to guarantee a proper synchronization of the control signals. The hold-time parameter describes a

defined period of time required to be recognized as either a valid high or low signal at terminal */INF*. In case of a simultaneous change of signals at the control terminals *IN* and */INF*, the signal at terminal */INF* has to remain at its intended level for the time $t_{/INF,hold}$. The figure below gives timing examples for the hold-time $t_{/INF,hold}$.

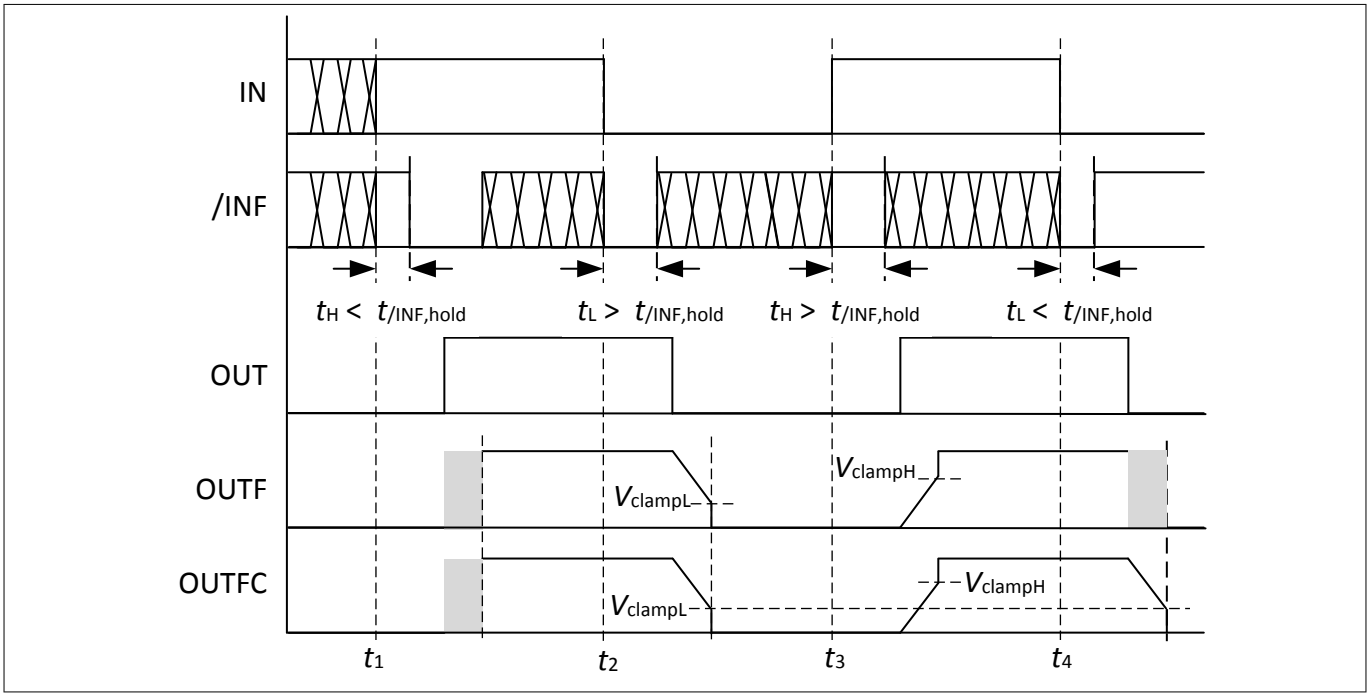

Figure 4 Timing diagram for hold-time $t_{/INF,hold}$

The period of time during which the control signal $V_{/INF}$ is at a high level after t_1 is too short for a reliable detection. The outputs *OUTF* or *OUTFC* may react according to the high signal or to the previously detected low signal. The low signal after t_2 is longer than the hold-time. The outputs act therefore as expected. This is also the case for t_3. The low signal of $V_{/INF}$ after t_4 is again too short to guarantee a determined activation at *OUTF* . The turn-off at *OUTFC* is at any rate defined, and follows the gate voltage until the latter reaches the active Miller clamp trigger level.

3 Output side

3.1 Output terminal *OUT*

The output terminal *OUT* changes its status according to the status of the input signal at terminal *IN*. A high signal at terminal *IN* determines a high signal at terminal *OUT*. A low signal determines a low signal.

The driver IC's output section at terminal *OUT* provides a rail-to-rail output. This feature allows the tight control of gate voltage during on-state and short circuit to be maintained as long as the driver’s supply is stable. The switching behavior of the power transistor is mainly controlled by the gate resistor, due to the low internal voltage drop of the IC. In turn, the low voltage drop reduces the power to be dissipated by the driver.

The active shutdown feature of terminal *OUT* ensures a safe off-state of the power transistor in case the output side is not connected to the power supply or an undervoltage lockout is in effect. The transistor's gate is clamped at terminal *OUT* to *VEE2*.

3.2 Output terminal *OUTF*

Terminal *OUTF* is the second output of those gate driver ICs, which have the standard output configuration. *OUTF* changes its status according to the status of the input signals */INF* and *IN*. It turns the power transistor on

and off in combination with the terminal *OUT*, so that depending on the status at terminal */INF*, a higher gate current is available, and the switching speed can be modified on the fly. Terminal *OUTF* is also set to clamping mode, if it is not activated for active gate operation. The clamping mode is activated when the gate voltage of the power transistor is below V_{CLAMPL} during off-state or above V_{VCC2}-V_{CLAMPH} during on-state. The clamping mode during on-state helps to achieve better short circuit clamping. The on-state clamping is activated after turn-on, as soon as the filter time of $t_{dCLAMPH}$ is elapsed. A clamping filter time $t_{dCLAMPL}$ for off-state improves the robustness of the IC's Miller clamp function.

The driver IC's output section at terminal *OUTF* provides a rail-to-rail output. This feature allows the tight control of gate voltage during on-state and short circuit to be maintained as long as the driver's supply is stable. The switching behavior of the power transistor is mainly controlled by the gate resistor, due to the low internal voltage drop of the IC. In turn, the low voltage drop reduces the power to be dissipated by the driver.

Terminal *OUTF* features the active shutdown function. This ensures a safe off-state of the power transistor in case the output side is not connected to the power supply, or the power supply of the output side collapses faster than the UVLO can react. The transistor's gate is clamped at terminal *OUTF* to *VEE2*.

The driving capability of terminal *OUTF* is the same as for terminal *OUT*. *OUTF* and *OUT* can be operated in low resistive connection (i.e. direct paralleling) only if the voltage $V_{/INF}$ at terminal */INF* is at the corresponding level at any time.

3.3 Output terminal *OUTFC*

Terminal *OUTFC* is the second output of those gate driver ICs having the Miller clamp function, i.e. the two-level slew-rate control in for turn-on only. *OUTFC* changes its status according to the status of the input signal */INF* and *IN*. It turns on the power transistor in combination with terminal *OUT*, so that depending on the status at terminal */INF*, a higher gate current is available and the switching speed can be modified for each PWM edge. Terminal *OUTFC* is not activated during the turn-off transient.

Terminal *OUTFC* is set to clamping mode also if it is not activated for active gate turn-on or turn-off . The clamping mode is activated when the gate voltage of the power transistor is below V_{CLAMPL} during off-state or above V_{VCC2}-V_{CLAMPH} during on-state. The clamping mode during on-state helps to achieve better short circuit clamping. The on-state clamping is activated after turn-on, as soon as the filter time of $t_{dCLAMPH}$ is elapsed. A clamping filter time $t_{dCLAMPL}$ for off-state improves the robustness of the IC's Miller clamp function.

The clamping capability of the output *OUTFC* during off-state of the power transistor is identical to turn-off current capability terminal *OUT*.

The driver IC's output section at terminal *OUTFC* provides a rail-to-rail output. This feature allows the tight control of gate voltage during on-state and short circuit to be maintained as long as the driver's supply is stable. The switching behavior of the power transistor is mainly controlled by the gate resistor, due to the low internal voltage drop of the IC. In turn, the low voltage drop reduces the power to be dissipated by the driver.

Terminal *OUTFC* features the active shutdown function. This ensures a safe off-state of the power transistor in case the output side is not connected to the power supply, or the power supply of the output side collapses faster than the UVLO can react. The transistor's gate is clamped at terminal *OUTFC* to *VEE2*.

The driving capability of terminal *OUTFC* is the same as for terminal *OUT*. *OUTFC* and *OUT* can be operated in low resistive connection (i.e. direct paralleling) only if the voltage $V_{/INF}$ at terminal */INF* is at the corresponding level at any time.

3.4 Gate resistor calculation guide

The 2L-SRC family offers a higher degree of freedom with respect to the dimensioning of gate resistor values. The basis of dimensioning the gate resistors is the knowledge of the switching performance of the power module as a function of gate resistor value, power transistor current and temperature. A full set of characterization measurements, which reflect the dimensioning target, e.g. of achieving a certain dv/dt, turn-off overshoot, etc., help to define the required gate resistor values for operating power transistors with the

intended performance. This section introduces the calculations for determining the values of the four gate resistances (for the turn-on and turn-off resistors) located at terminals *OUT* and *OUTF* or *OUTFC*.

3.4.1 Fully flexible gate resistance dimensioning

It is assumed here, that the target behavior of the power module is already known, which is specified by the reference values of the four gate resistors $R_{gon,slow}$, $R_{gon,fast}$, $R_{goff,slow}$, and $R_{goff,fast}$. Measurements using a double pulse setup are suitable to identify these resistors values in order to achieve the required two-level slew-rate control behavior. $R_{gon,slow}$, $R_{gon,fast}$, $R_{goff,slow}$, and $R_{goff,fast}$ are synomyms only for the resulting gate resistor with respect to the power module´s switching peformance, but do not represent values of the real application schematic, yet. Thus, they have to be transferred into related values of resistors R1, R2, R3, and R4 as it is depicted in the figure below.

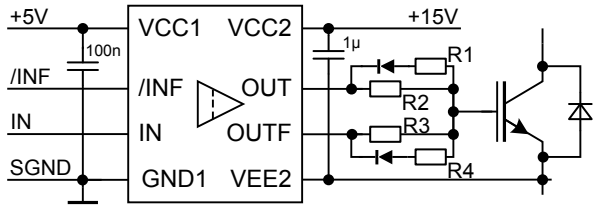

Figure 5 Typical application with turn-on and turn-off resistors at terminals *OUT* and *OUTF*

The simplest transfer is the value of resistor R2, as it is directly correlated with $R_{gon,slow}$ for the case, that only terminal *OUT* turns on the power transistor.

$$R2 = R_{\text{gon, slow}}$$

Equation 1

$R_{goff,slow}$ is the parallel circuit of R2 and R1 for the case that only terminal *OUT* is turning off the power transistor. R1 is calculated therefore with

$$R1 = \frac{R2 \cdot R_{\text{goff, slow}}}{R2 - R_{\text{goff, slow}}}$$

Equation 2

$R_{gon,fast}$ is the parallel circuit of R2 and R3 for the case that both terminal *OUT* and *OUTF* are turning on the power transistor. R3 is calculated therefore with

$$R3 = \frac{R2 \cdot R_{\text{gon, fast}}}{R2 - R_{\text{gon, fast}}}$$

Equation 3

Finally, $R_{goff,fast}$ is the parallel circuit of R1, R2, R3 and R4 for the case that both terminal *OUT* and *OUTF* are turning off the power transistor. The calculation of R4 is done by using

$$R4 = \frac{R_{\text{goff, fast}} \cdot R1 \cdot R2 \cdot R3}{R1 \cdot R2 \cdot R3 - R_{\text{goff, fast}} \cdot (R1 \cdot R2 + R1 \cdot R3 + R2 \cdot R3)}$$

Equation 4

Please note, that there is a zero in the denominator of these equation. This means, that a complete solution cannot be guaranteed.

The gate resistance calculations for those driver ICs that have terminal *OUTFC* instead of *OUTF* is identical to the equations for R1, R2 and R3. As the slew-rate control function is only for turn-on for those parts, the calculation for resistor R4 is not required.

3.4.2 OUT and OUTF share the same turn-on and turnoff gate resistor values

Limiting the number of different components is often welcome to reduce the purchasing efforts and assembly time. A wide range of different combinations of $R_{gon,slow}$, $R_{gon,fast}$, $R_{goff,slow}$, and $R_{goff,fast}$ can be achieved, as well, by using the same resistor values. Let us distinguish three cases here, and calculate $R_{gon,slow}$, $R_{gon,fast}$, $R_{goff,slow}$, and $R_{goff,fast}$ by using for example values of 20 Ω and 3.9 Ω. It is assumed, that the effect of the decoupling diodes is negligible.

The first case uses the same resistor values for R1 and R2 and the same values for R3 and R4. This results in the following gate resistance dimensioning:

R1 = R2 = 20 Ω, R3 = R4 = 3.9 Ω

$R_{gon,slow}$ = 20 Ω, $R_{gon,fast}$ = 3.26 Ω, $R_{goff,slow}$ = 10 Ω, and $R_{goff,fast}$ = 1.63 Ω

This dimensioning achieves a significant difference between fast and slow switching in general. However, there is only a moderate difference with respect to the effective values for the turn-on and the turn-off behavior.

The second case uses the same resistor values for R1 and R3 and the same values for R2 and R4. This results in the following gate resistance dimensioning:

R1 = R3 = 20 Ω, R2 = R4 = 3.9 Ω

$R_{gon,slow}$ = 20 Ω, $R_{gon,fast}$ = 10 Ω, $R_{goff,slow}$ = 3.26 Ω, and $R_{goff,fast}$ = 1.63 Ω

This dimensioning achieves a significant difference between turn-on and turn-off in general. However, there is only a moderate difference with respect to fast and slow for the turn-on and the turn-off behavior.

The third case uses the same resistor values for R1 through R4. This results in the following gate resistance dimensioning:

R1 = R2 = R3 = R4 = 20 Ω

$R_{gon,slow}$ = 20 Ω, $R_{gon,fast}$ = 10 Ω, $R_{goff,slow}$ = 10 Ω, and $R_{goff,fast}$ = 5 Ω

3.5 OUT-to-OUTF(C) matching

The matching of outputs $t_{PDOUT-OUTF}$ describes the timing precision of the transitions from high to low or vice versa at the two outputs *OUT* and *OUTF* / *OUTFC* of the EiceDRIVER™ 1ED32xx IC family. Both outputs should switch simultaneously in ideal cases. However, a tiny mismatch in unavoidable. It is nevertheless important for gate drivers which have multiple outputs operated in parallel, that there is no cross conduction from one output to another. This means that the situation in which, e.g. terminal *OUT* sources current while terminal *OUTF* is sinking current should never occur when operated simultaneously. The gate driver ICs are designed in such a way as to maximise the precision having the lowest tolerance.

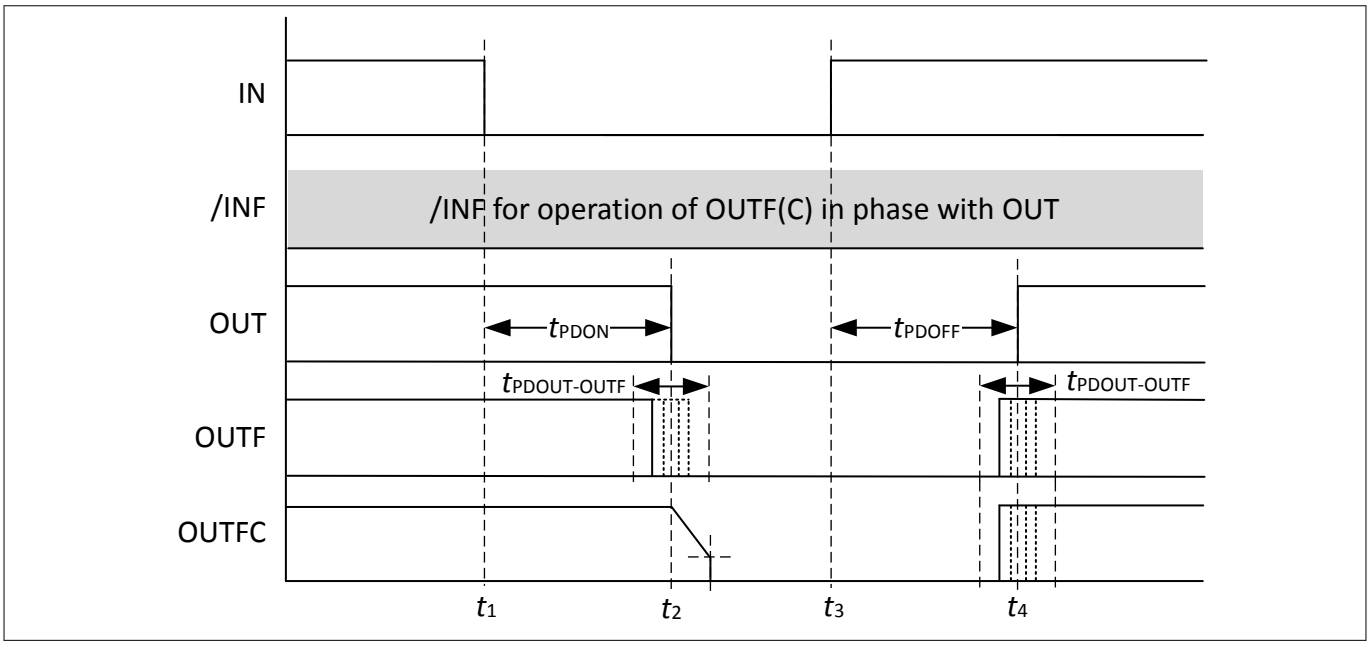

Figure 6 Definition of OUT-to-OUTF matching

3.6 Working with external booster circuits

It is possible to use the two-level slew-rate control gate driver ICs in combination with external booster circuits. However, the total output peak current of 18 A for 1ED32x1MC12H, is high enough to avoid external buffers for a wide range of applications.

It is recommended to use bipolar transistors, when designing a booster circuit, as they inherently have the ability for high impedance state, when the base current is 0. This is important when output *OUT* is operated only. The output *OUTF* or *OUTFC* have to be in a high impedance state to prevent from a short-term shoot-through of both outputs.

3 Output side

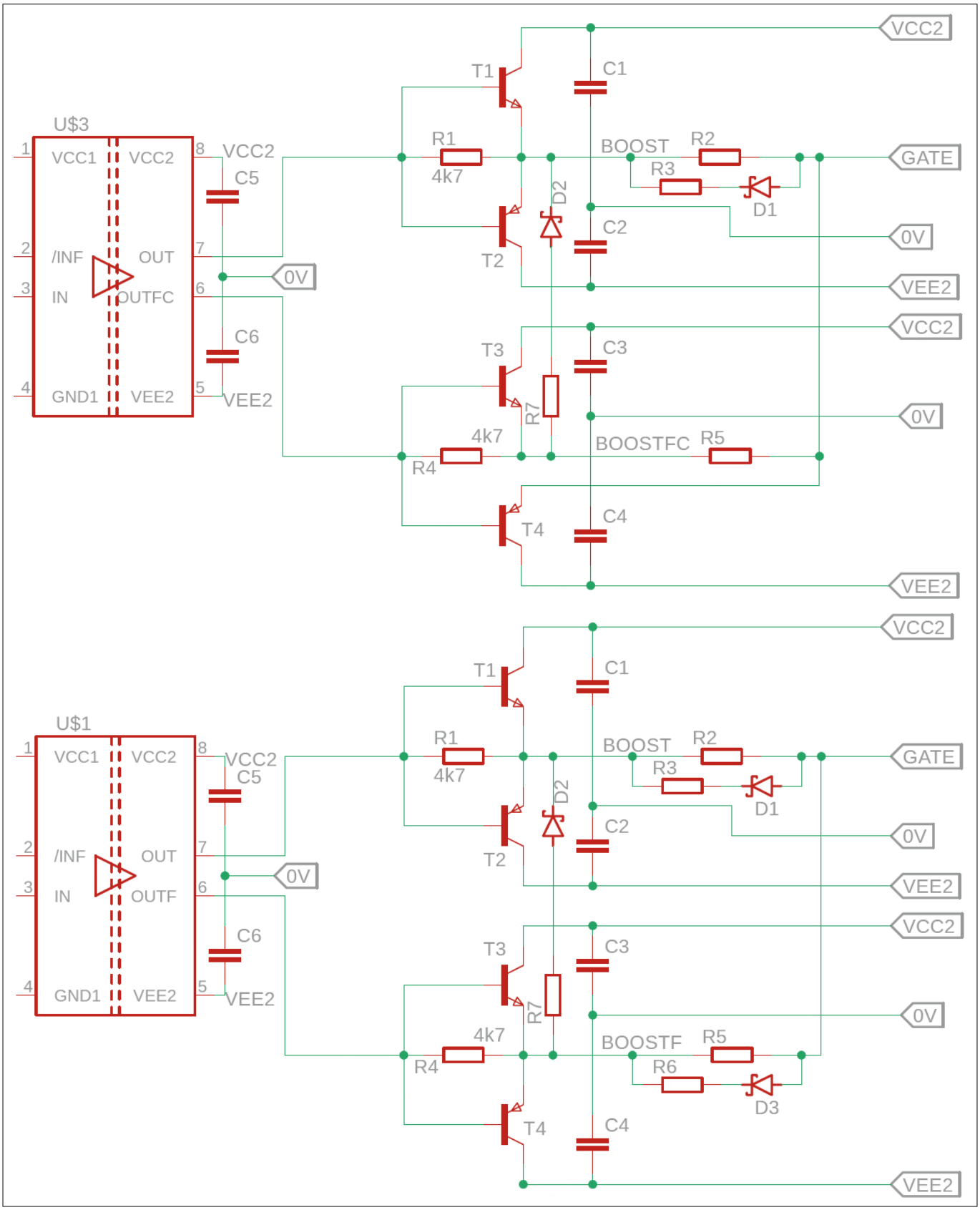

Figure 7 **Example for clamp output configuration (top) and standard configuration (bottom) driver IC in combination with an external booster**

The proposals for booster circuits are provided in the figure and do not differ very much for the two output configuration types, standard and clamp configuration. The rules for dimensioning these circuits are the same as those for other booster circuits.

Resistors R4 are necessary for providing a sense path to the terminals *OUTF* or *OUTFC* for the on-state and off-state clamping, respectively.

Resistor R7 and diode D2 avoid excessive negative base-emitter voltages at T3.

4 Input-to-output control scheme

The input-to-output control scheme defines the relationship between the input states of terminals *IN* and */INF* and the output states of terminals *OUT* and *OUTF(C)*. This scheme is defined in the table below.

Table 2 Input to output control scheme

State	*IN*	*/INF*	*OUT*	*OUTF* (1ED3240MC12H, 1ED3241MC12H)	*OUTFC* (1ED3250MC12H, 1ED3251MC12H)
1	0	0	0	0*	0*
2	0 → 1	0	0 → 1	0 → 1	0 → 1
3	0	0 → 1	0	0*	0*
4	1	0	1	1*	1*
5	1 → 0	0	1 → 0	1 → HiZ	1 → HiZ
6	1	0 → 1	1	1*	1*
7	0	1	0	0*	0*
8	0	1 → 0	0	0*	0*
9	0 → 1	1	0 → 1	0 → HiZ	0 → HiZ
10	1	1	1	1*	1*
11	1	1 → 0	1	1*	1*
12	1 → 0	1	1 → 0	1 → 0	1 → HiZ
Input UVLO↓	X	X	0	last */INF*	last */INF*
Output UVLO↓	X	X	0	last */INF*	last */INF*

*) Output is activated, when the voltage at terminal *OUTF* or *OUTFC* is higher than V_{VCC2} - V_{CLAMPH} during on-state or lower than V_{CLAMPL} during off-state.

The control scheme of the gate driver IC family inherently avoids the activation of the two outputs *OUT* or *OUTF* / *OUTFC* in active opposite status. The status of terminal */INF* can be changed pulse by pulse with a short delay with respect to a potential change of status at terminal *IN* according to the timing diagrams below.

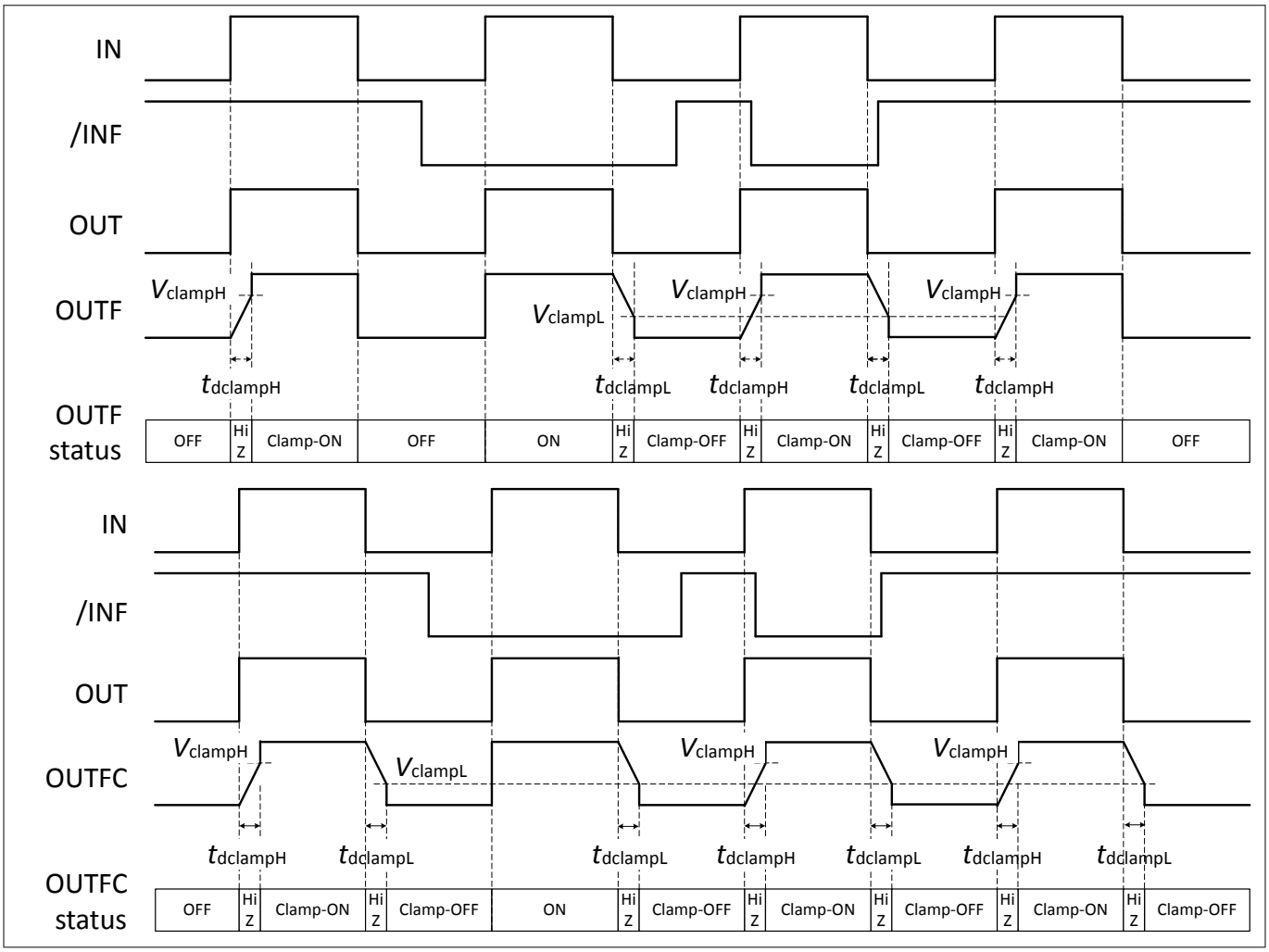

Figure 8 **Timing diagram of input and output signals for standard version (top) and clamp version (bottom)**

The timing diagrams contain two types of status changes: A sharp edge indicates the active change of the output. A slowly rising edge indicates the passive following of terminal *OUTF* or *OUTFC*, followed by the gate clamping.

It is of course possible to operate the two-level slew-rate control gate driver family with the same control signal for inputs *IN* or */INF*. This yield in the following timing diagrams.

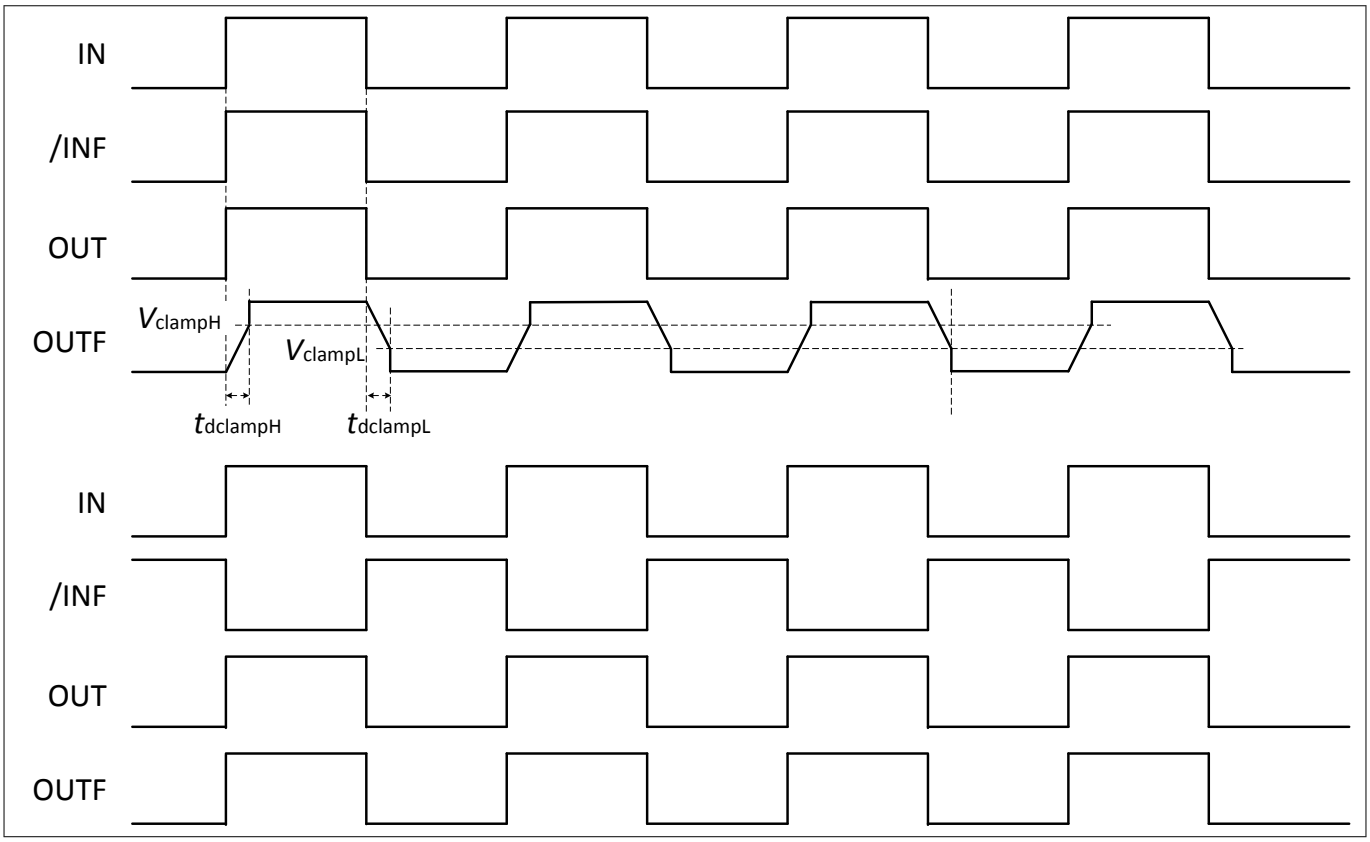

Figure 9 **Timing diagram of input and output signals for standard versions (1ED3240MC12H and 1ED3241MC12H) using similar signals for *IN* and */INF* (top: signals in phase, bottom: */INF* inverted)**

It can be seen in the top part that the output *OUTF* is never activated as long as the signals at input *IN* and */INF* are running in phase. It is the opposite in the bottom part of the figure. Here, output *OUTF* is always actively switching in parallel to output *OUT*, when signal /INF is inverted with respect to signal IN.

The clamp variants 1ED3250MC12H and 1ED3251MC12H react in principle the same as the standard version, which is shown in the top part of the previous figure. However. there is a small difference when signal /INF is inverted with respect to signal IN. This is depicted in the next figure.

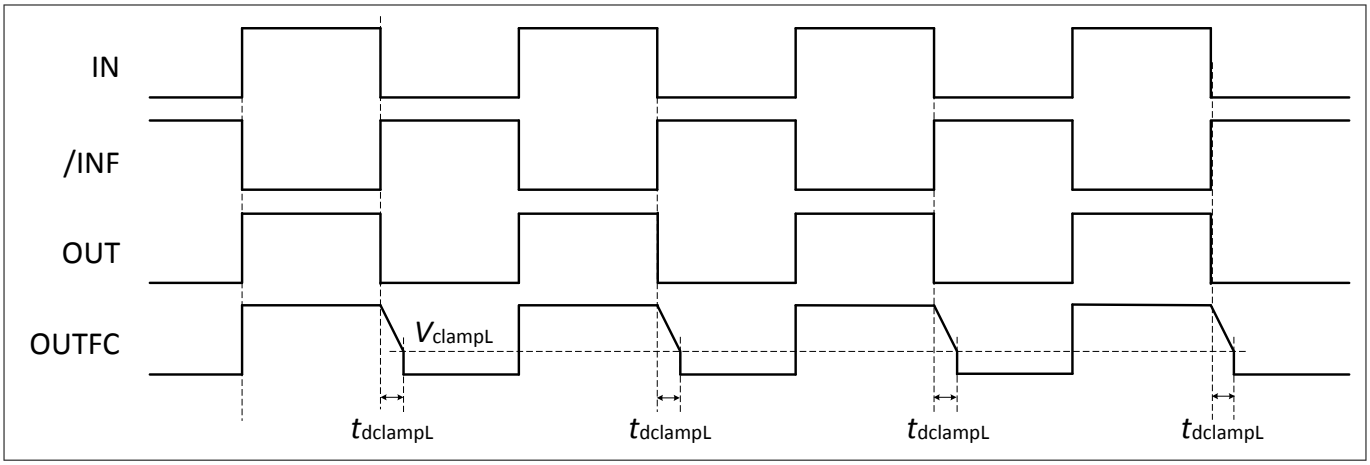

Figure 10 **Timing diagram of input and output signals for clamp versions (1ED3250MC12H and 1ED3251MC12H) using complimentary signals for *IN* and */INF* for standard and clamp variants**

Output *OUTFC* turns on actively and passively follows *OUT* during turn-off. The same behavior can be achieved by constantly applying a low signal at terminal */INF*. It is therefore a better solution to apply a pull down resistor at */INF* instead of continuously toggling the signal.

5 Application use cases

5.1 Variable speed drive

5.1.1 Application background of inverter drives

The switching speed of power transistors is crucial in drives systems. Motor windings can sustain a switching speed of slower than 5 V/ns [1]. This value is used in the motor industry as a rule of thumb. It is therefore important, that the switching speed of motor inverters stay in this range if no motor phase filters are applied. Otherwise, the high dv_{CE}/dt rates lead to reflections at the motor winding inductance resulting in overvoltage there. The effect becomes worse with longer motor cables, and degrades the winding insulation of the motor. This is given in the figure below.

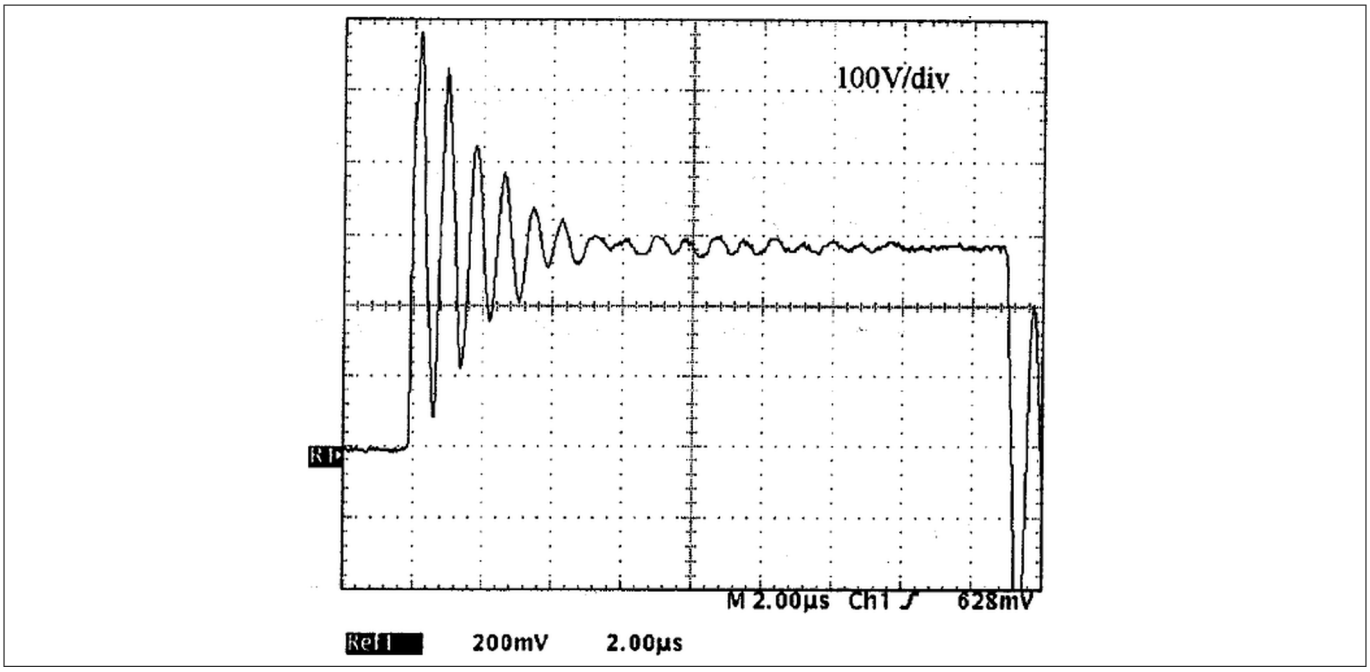

Figure 11 Motor terminal overvoltage according [2]

Furthermore, a high switching speed can lead to excessive shaft voltage. The high shaft voltage discharge through the bearings to the motor's encasement, which can degrade the bearings over time.

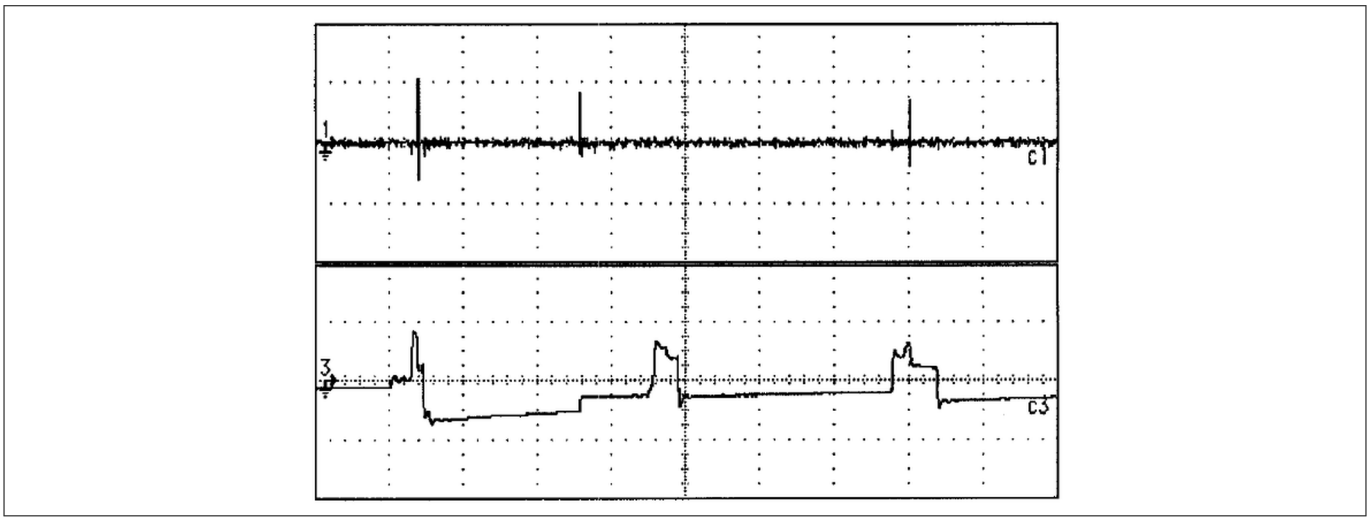

Figure 12 Shaft voltages (Ch3: 4 V/div) and bearing currents (Ch1: 50 mA/div) according [3]

5.1.2 IGBT transistor switching analysis

This section concentrates on the collector-emitter voltage slope dv_{CE}/dt ad the switching energy for turn-on and the turn-on. The figures below show these two parameters as a function of the gate resistorR_g, the junction temperature $T_J$and the collector current I_C.

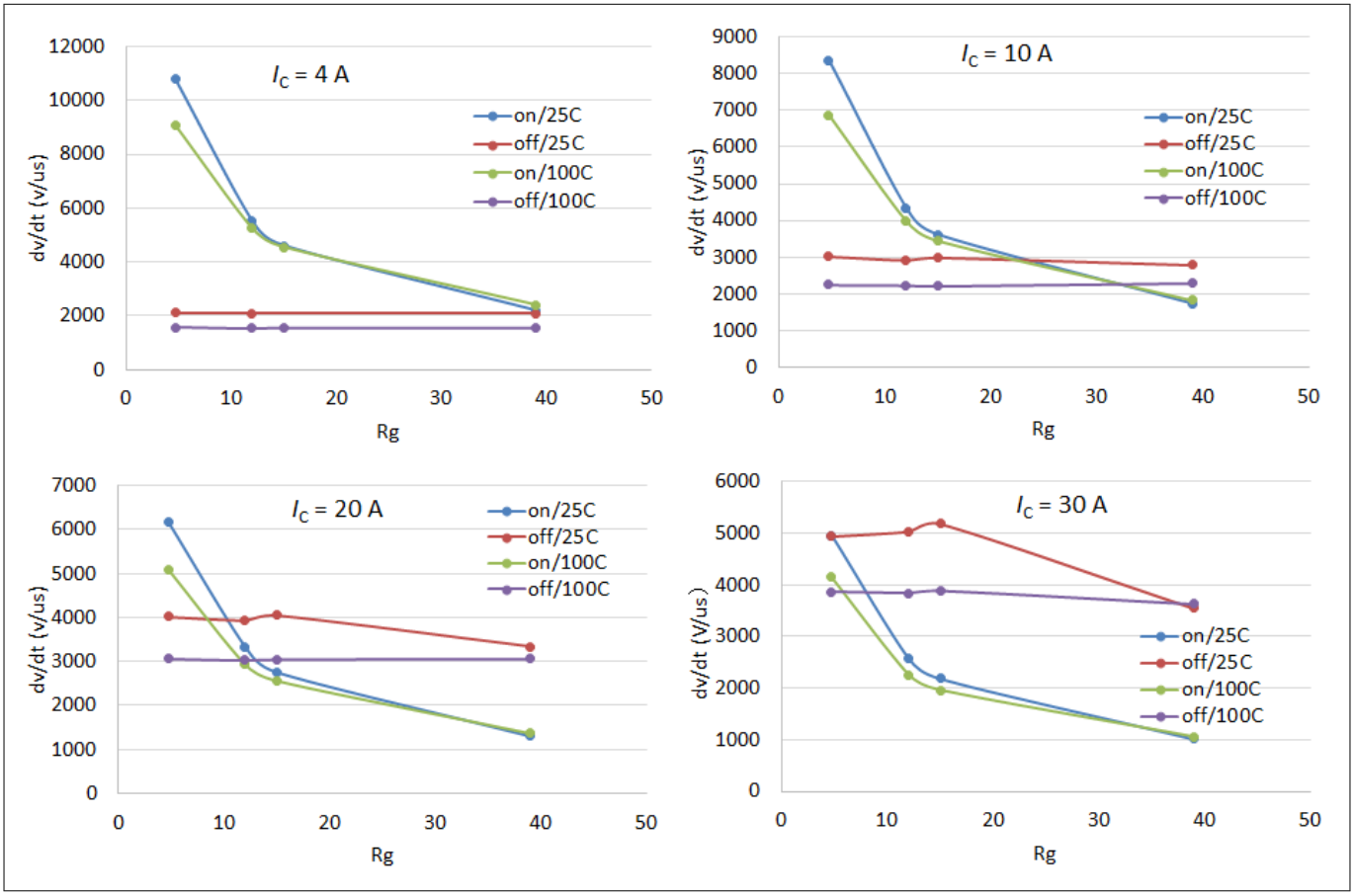

Figure 13 Collector-emitter voltage slope *dv_{CE}/dt* of FP35R12W2T7_B11

One can see that the *dv_{CE}/dt* is continuously falling with increasing collector current. The maximum *dv_{CE}/dt* at 4 A is for example highest with approximately 10 kV/µs, while it is reaching approximately 5 V/µs at 30 A. The

conventional way for the dimensioning of the turn-on gate resistor would be to select R_g = 15 Ω, which would lead to dv_{CE}/dt of close to 5 kV/µs at a collector current of 4 A.

The next figure provides the graphs for the turn-on and turn-off energy. It is obvious that the turn-off energy is flat as a function of the gate resistance, while the turn-on energy is continuously increasing. Thus, higher gate resistances will yield higher turn-on energy.

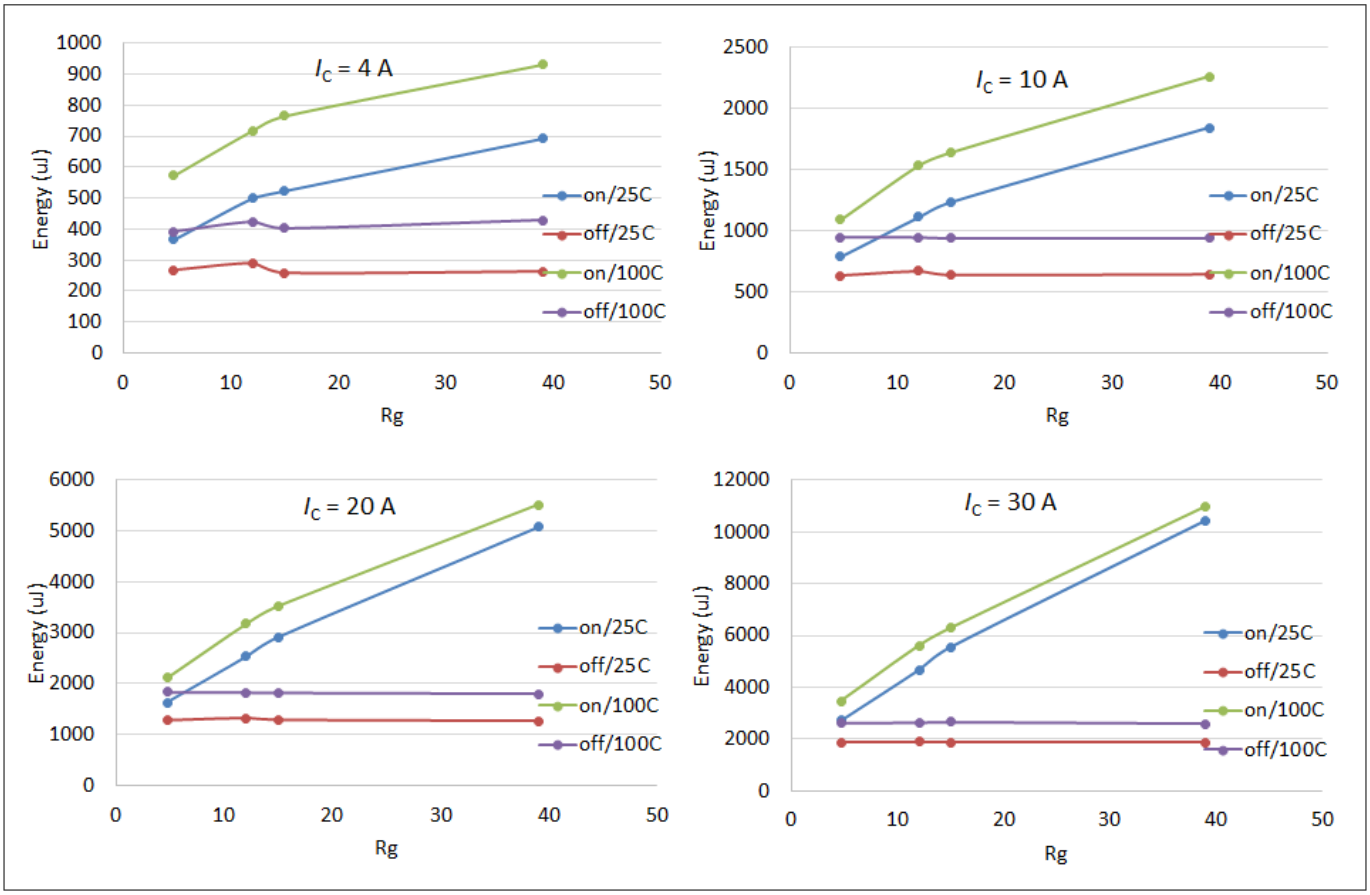

Figure 14 Turn-on energy E_{on} and E_{off} of FP35R12W2T7_B11

On one hand side, the optimum dimensioning of the turn-on gate resistance would need to be at 15 Ω for satisfying the dv/dt-requirement at low collector currents, while on the other side the gate resistance should be for example 5 Ω to satisfy the low turn-on energy requirement at higher collector current. This can be achieved with the two-level slew-rate control IC family.

The following section discusses this case in terms of the turn-on gate resistance and its changeover point.

5.1.3 System simulation for a drive system

A 3 phase drive system using an induction motor is simulated using the Plecs simulator and the above mentioned double pulse characterization results. The simulation of power losses and junction temperatures was performed with a conventional gate drive circuit using one turn-on gate resistance for turn-on and one gate resistance for turn-off. These results are compared with a gate drive using the two-level slew-rate control IC. The system model allows the value of gate resistor to be changed at any different operating point using variables such as a specific collector current, a temperature or other physical parameters. Combinations of the above-mentioned parameters are also allowed. These are the standard simulation conditions:

- DC-link voltage V_{DC} = 560 V
- sinusoidal modulation (modulation index = 0.8)
- switching frequency f_p = 8 kHz
- Motor frequency f_{mot} = 50 Hz

- Changeover current I_{chg} +/- 5 A
- Fixed heat sink temperature T_{HS} = 100 °C

To evaluate the potential efficacy of this type of two-level SRC driver, a set of reference conditions were simulated and compared with a conventional standard single fixed value of turn-on and turn-off gate resistor. The resistor values selected were R_{goff} = 5.6 Ω and a turn-on gate resistor R_{gon} = 15 Ω. The R_{gon} value limits the ddv_{CE}/dt to 5 V/ns at 4 A and 25°C.

The simulation results under this reference condition are compared in the figure below to the results using the two-level slew-rate control driver IC with a fast turn-on gate resistor R_{gfast} = 5.6 Ω and a slow turn-on gate resistor R_{gslow} = 56 Ω. The changeover point from R_{gfast} to R_{gslow} and vice versa is selected at a motor current of +/-5 A. Of course, R_{gslow} = 56 Ω is a relatively large value compared to the reference. However, very often the low load operation is critical for EMI and R_{gslow} is able to slow down current commutations at low load operation.

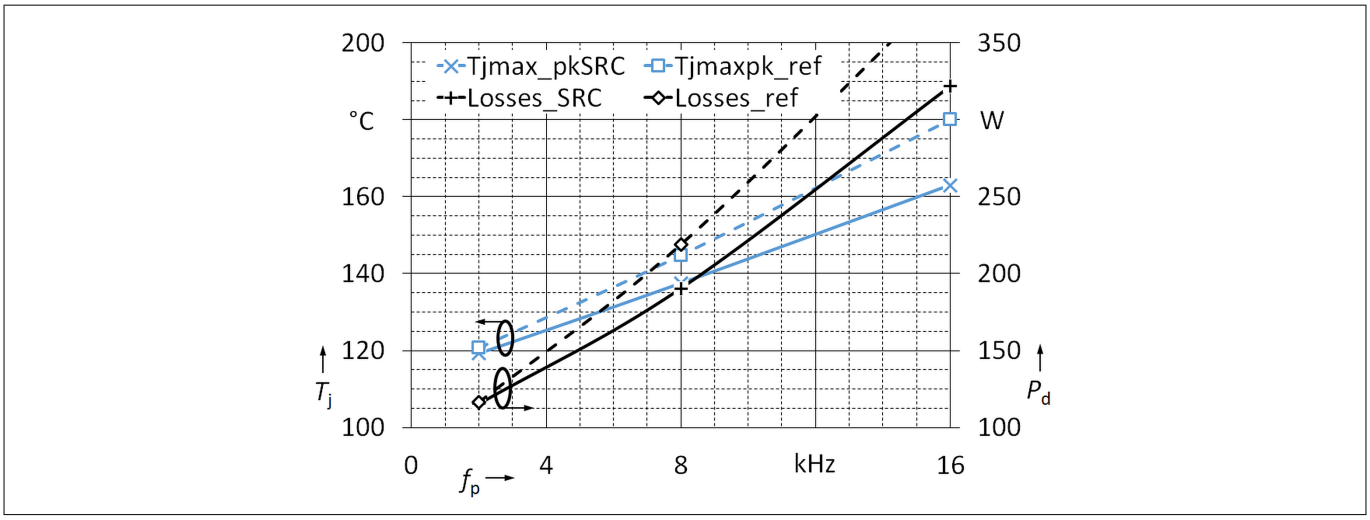

Figure 15 Inverter power loss P_d and IGBT junction temperure T_J as a function of the motor current I_{mot} (I_{chg} = +/-5 A, f_p = 8 kHz)

One can see that the selected two-level slew-rate control gate resistances have a direct influence on the simulation results. The two-level slew-rate control case uses a larger turn-on resistance, and so dissipates more power resulting in a higher peak junction temperature at low motor current amplitudes. For example, the power dissipation of the reference using R_{gon} = 15 Ω is $P_{d,ref}$ = 52 W at a collector current of I_C = 5 A, while the two level SRC gate drive dissipates $P_{d,SRC}$.= 67.4 W. However, this increase in losses only applies when operating at low current levels, where the overall losses are low, but the trade-off advantage of using the larger gate value under these conditions comes from a reduced dv_{CE}/dt level from 5 V/ns to less than 2 V/ns and the possibility of reduced EMI levels.

The real value of the proposed slew-rate control driver is visible when operating at higher motor currents, for example, above 9 A. Here, the two-level slew-rate control driver yields consistently lower losses and lower peak junction temperatures.

For example, with the reference design, the maximum output current for a temperature limit of T_J = 155°C is 26 A r.m.s., but with the two-level slew-rate control it is 30 A r.m.s., a 15% increase. This advantage can be even greater when considering comparisons at higher junction temperatures.

This paragraph compares simulation results of the reference case with possible changeover points of +/-5 A, +/-10 A and +/-15 A. The changeover point defines the ranges where R_{gslow} and R_{gfast} are active. Lower changeover points than +/-5 A are possible of course, but also jeopardize the effect of the proposed scheme, because the changeover point should not interfere with the EMI-sensitive area of low motor current commutations. The figure below depicts the simulation results for the above- mentioned changeover points at a fixed switching frequency of f_p = 8 kHz.

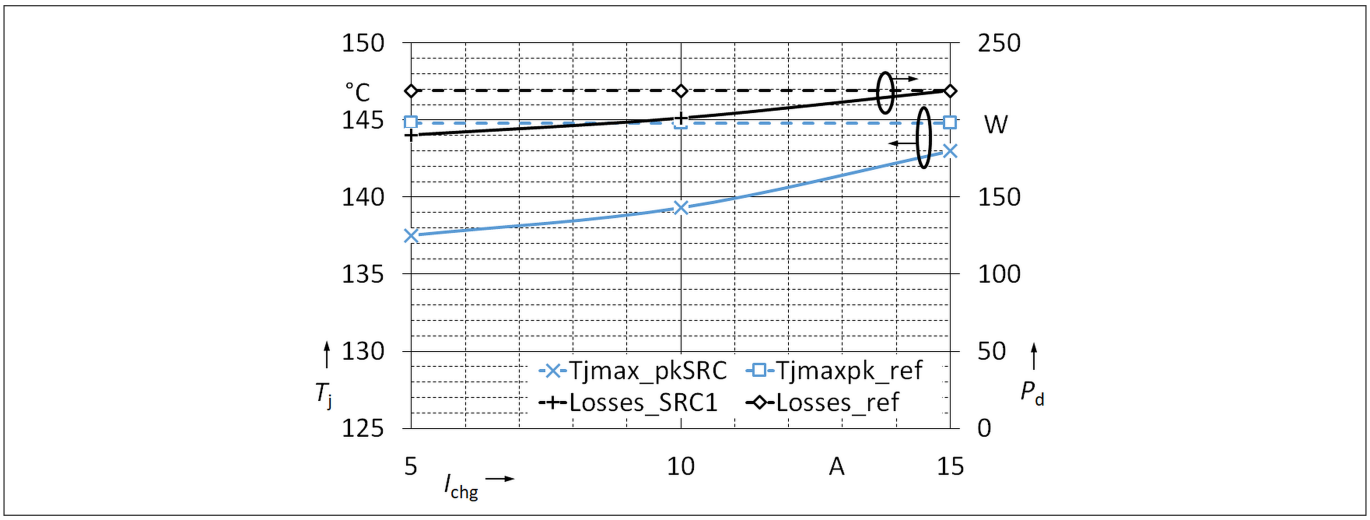

Figure 16 **Inverter power loss P_d and IGBT junction temperure T_J as a function of the changeover current I_{chg} (I_{mot} = 20 A, f_p = 8 kHz)**

The lower the changeover point value, the higher is the advantage of the proposed gate drive concept with the largest advantage at a change point at 5 A. On the other hand, a higher changeover point can allow even lower values for R_{gfast}. This can compensate for the use of R_{gfast} in a wider range of motor current.

This paragraph provides the simulation results at switching frequencies of 2 kHz, 8 kHz and 16 kHz, while the motor current is fixed to 20 A r.m.s. The switching frequency is a big leverage for using the proposed two-level slew-rate control driver. On the one hand, each and every turn-on contributes to the overall losses. Therefore, the overall losses increase with higher switching frequency for both the conventional gate drive (reference) as well as for the proposed scheme. The operating point with a motor current of I_{mot} = 20 A r.m.s., I_{chg} = +/-5 A and f_p = 2 kHz results with almost the same losses and junction temperatures. However, increasing the switching frequency leads to lower losses over the compared range of switching frequencies for the two-level slew-rate control driver.

For example, one can reach a higher switching frequency, approximately 4 kHz higher, for the same junction temperature of Tj = 160°C. This advantage can be used to reduce the ripple current portion of the motor current.

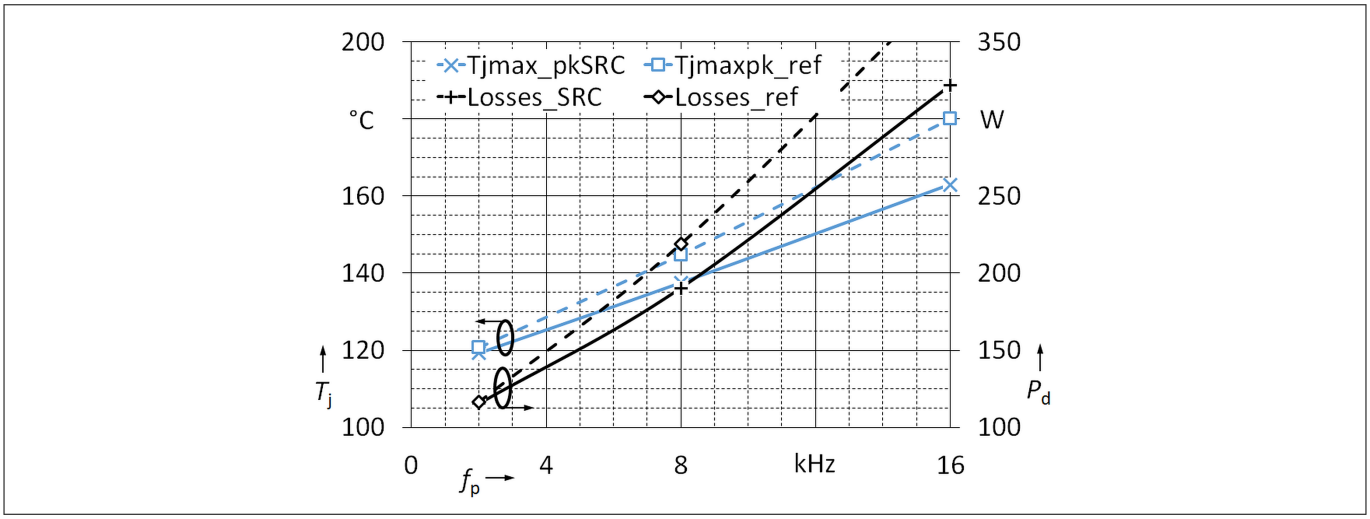

Figure 17 **Inverter power loss P_d and IGBT junction temperure T_J as a function of the switching frequency f_p (I_{mot} = 20 A, I_{chg} = +/-5A)**

5.2 PFC boost converter

5.2.1 Application background of PFC boost converters

Power factor correction (PFC) boost converters are widely used in switch-mode power supplies, as they enable compliance to IEC 61000-3-2. In such applications, dimensioning of the gate resistance is still a trade-off between turn-off voltage overshoot, EMI and switching losses. For example, PFC converters are subject to severe overload conditions when recovering from a temporary line drop under full load. The DC-link voltage continuously drops as the input power fails, but still full power is delivered to the load ($t_2 - t_1$). The DC-link voltage reduction is largest under these conditions, as it is shown in the figure below. When the input power recovers, the PFC converter has to provide the current output load, and in addition, has has to fill up the DC-link voltage again ($t_3 - t_2$).

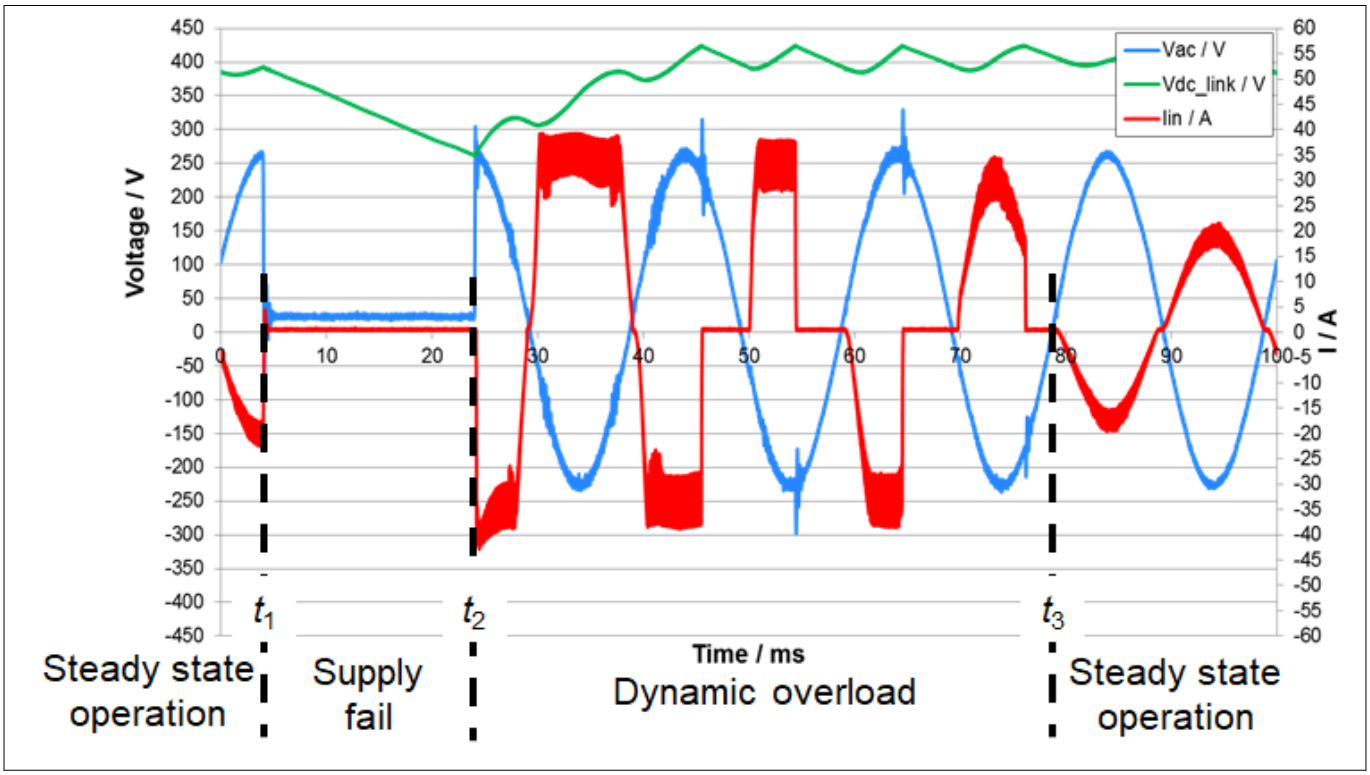

Figure 18 Input voltage (blue), input current (red) and DC-link voltage (green) at an AC input fail eventLine_fail-DC_recovery.svg

The current amplitudes during the recovery phase $t_3 - t_2$ can easily double the nominal operation value, or reach even higher values. Therefore, countermeasures like pulse-to-pulse current limitation are taken which reduce the current amplitude. This is depicted in the input current waveform (red) of the above figure. It can be seen, that the cycle-by-cycle current limitation of the PFC-control leads to a rather rectangular current waveform during the dynamic overload period.

The turn-off of modern superjunction power MOSFETs such as CoolMOS™ is very fast under these high drain current conditions with a high di_D/dt. Therefore, the drain side stray inductance generates a relatively high turn-off overshoot, which can exceed even the absolute maximum voltage rating of the MOSFET V_{DS}.

5.2.2 CoolMOS(tm) turn-off analysis

The figure below depicts the results of a characterization of IPP045R65C7 [1] under laboratory conditions using a double pulse test bench. The upper graph shows the curves for the maximum drain-source voltage *V*DS,max at turn-off, and the lower graph the results of turn-off energy. The solid lines show the results for a junction temperature of *T*J = 25°C, the dashed lines for 125°C.

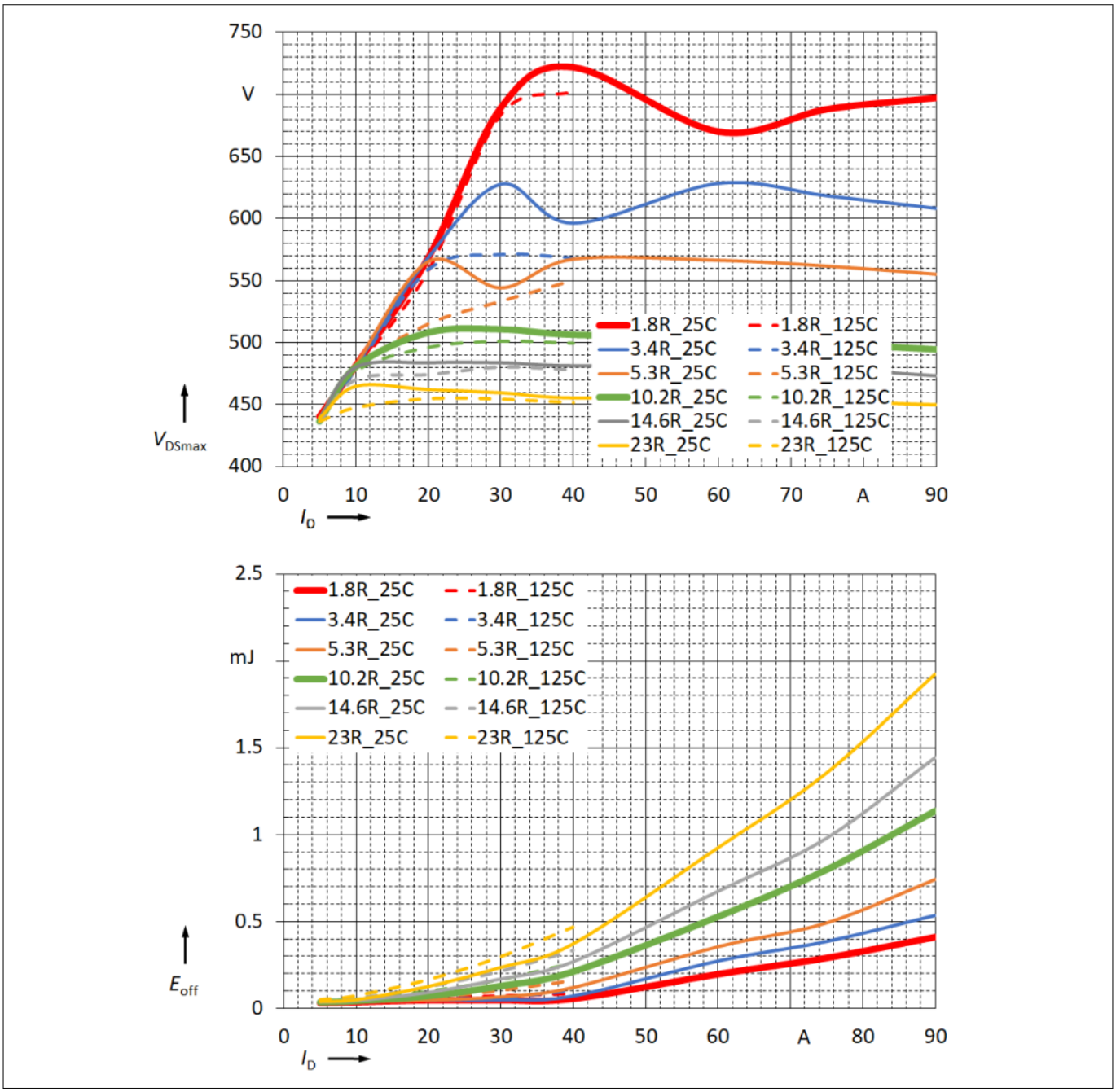

Figure 19 Maximum drain-source voltage (top) and switching energy (bottom) at turn-off

It can be seen that the favorable use of a gate resistor of R_g = 1.8 Ω (bold red line) during normal mode would result in turn-off overshoots up to 700 V during the overload conditions exceeding a drain current of I_D = 30 A. This is not acceptable for MOSFETs with a drain-source breakdown voltage of $V_{DS(br)}$ = 650 V. The acceptable voltage level would be $V_{DS(br)}$ ≈ 500 V. Such a level is achievable using a gate resistance of R_g = 10.2 Ω. However, the turn-off energy E_{off} is increasing considerably during such an operation. E_{off} is approximately 0.07 mJ for R_g = 1.5 Ω and increases to 0.12 mJ for R_g = 10.2 Ω. Thus, the PFC converter generates considerably more losses without a separate handling of overload conditions, because R_g = 10.2 Ω would be the nominal gate resistor. Since the recharge operation of the DC-link after a line fail is time limited to e.g. 50 ms, a temporarily higher turn-off energy is acceptable for the sake of a strongly reduced voltage overshoot. Furthermore, the PFC MOSFET can be operated with a much lower gate resistor during normal operation, as no trade-off with overload conditions has to be considered for dimensioning the gate resistor R_g.

Avoiding such overshoots could be possible with snubbers or soft switching techniques as well, but snubbers are always connected to additional inductors, capacitors or semiconductors, thus, adding numerous components.

5.2.3 Application verification in a PFC boost converter

The top part of the figure below depicts the PFC waveforms during a line-fail event. The PFC current control goes into current limitation mode immediately after the recovery of the line voltage. It is easy to see, that the proposed gate drive activates the 2L-SRC operation and strongly limits the voltage overshoot for about 2.5 ms after line recovery in case “1”. After that, the PFC current reaches almost zero in the middle of the picture. Then, the PFC-choke current rises and again triggers the activation of the overshoot limitation in case “2”. This proves the proper functioning over several line cycles.

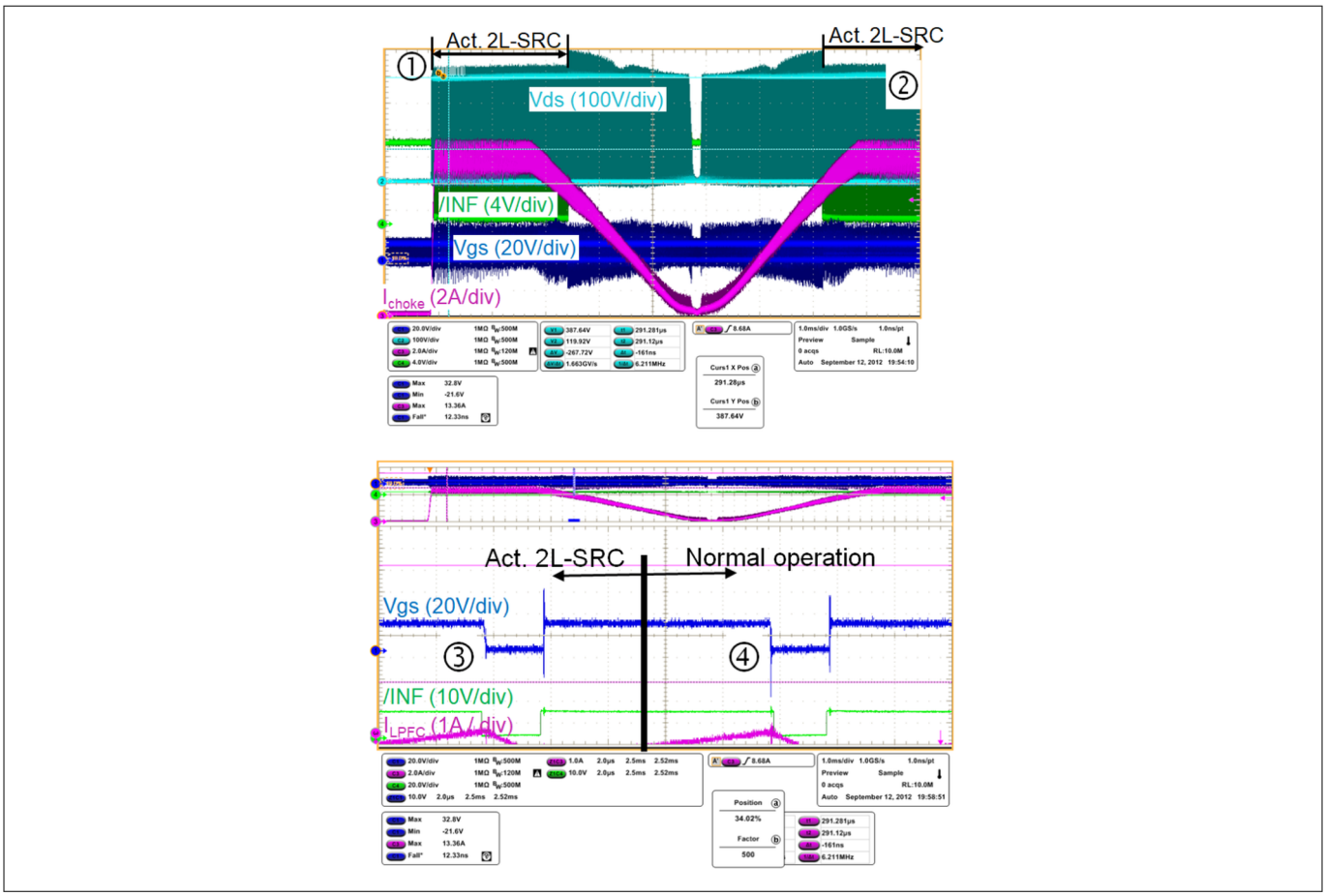

Figure 20 Measurement after line fail with AGC-signal (green), input current (purple), and gate-source voltage (blue)

The bottom section shows a zoom of the top section. Here the signal /INF shows two instances with low-level (“3”, “4”). Instance “3” is triggers the turn-off with the increased gate resistance, which results in a visible slower gate-source voltage slope. Case “4” shows the normal gate resistance using a low gate resistance, thus having a steep gate-source voltage slope. The low-level is triggered clearly by the switching noise, but it does not have an impact on that PWM period.

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Revision history

Document version	Date of release	Description of changes
		•
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Edition 2021-03-26

Published by

Infineon Technologies AG

81726 Munich, Germany

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Document reference
IFX-kmh1531224930042

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