11 kW high-efficiency high-density bidirectional three-/single-phase AC-DC PFC/inverter

About this document

Scope and purpose

This document introduces a 11kW high-efficiency high-density bidirectional three-/single-phase AC-DC power converter, i.e., REF_11KW_PFC_SIC_QD offered by Infineon. The design can be used in multiple applications, including but not limited to EV charging, onboard charger, and energy storage systems.

The REF_11KW_PFC_SIC_QD design can operate under both single-phase and three-phase AC grid with DC-side voltage around 800V. When interfacing three-phase grid, the design can convert steady state maximum power of 11 kW in both power-flow directions, i.e., either PFC mode or inverter mode, with peak efficiency of 99.15 % (PFC) and 99.122 % (inverter) with 230 V_{RMS} grid voltage. When interfacing with single-phase grid, the design can convert steady state maximum power of 7.3 kW in both power-flow directions, with peak efficiency of 98.95 % (PFC) and 98.91 % (inverter).

With the size of 243 mm x 100 mm x 40 mm (excluding cooling plate) and the power density of 11.3 kW/L, i.e., 185 W/in^3, REF_11KW_PFC_SIC_QD demonstrates a viable approach for achieving high power density and efficiency, in the combined three-/single-phase AC-DC power converter unit compared to state-of-the-art solutions. The system solution REF_11KW_PFC_SIC_QD utilizes Infineon's innovative top-side-cooling package Q-DPAK devices which enables the high-performance metrics. The design is realized by the well-proven three-level active neutral point clamped (3L-ANPC) topology with optimizations on switching loops.

This document describes the converter operation principle, hardware design as well as software design topics and a summary of the experimental results for the complete Infineon solution.

Intended audience

The document is intended for R&D engineers, hardware designers, and developers of power electronic systems.

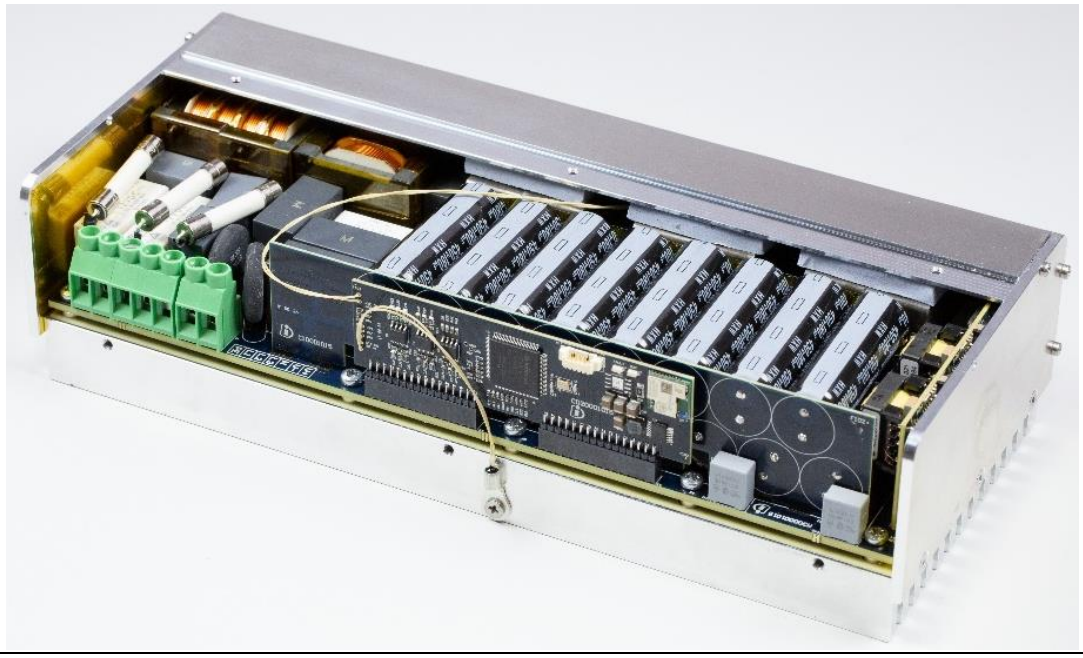

Figure 1 REF_11KW_PFC_SIC_QD

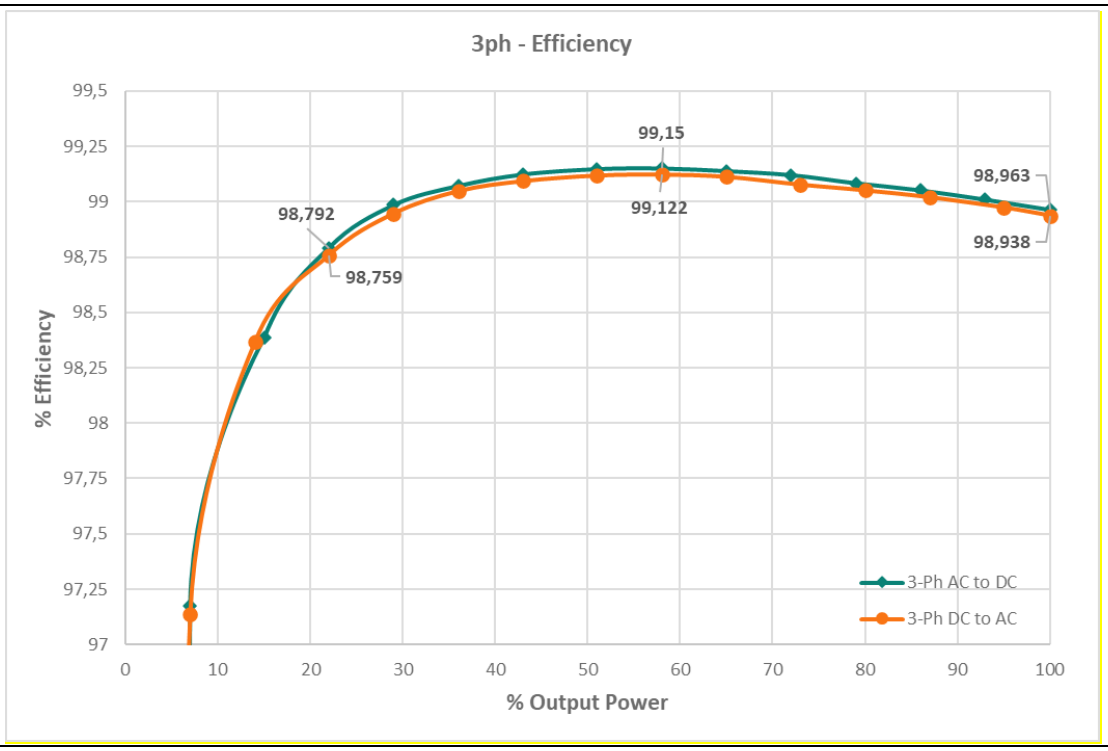

Figure 2 REF_11KW_PFC_SIC_QD measured efficiency for three-phase operation, both AC to DC (PFC mode) and DC to AC (inverter mode)

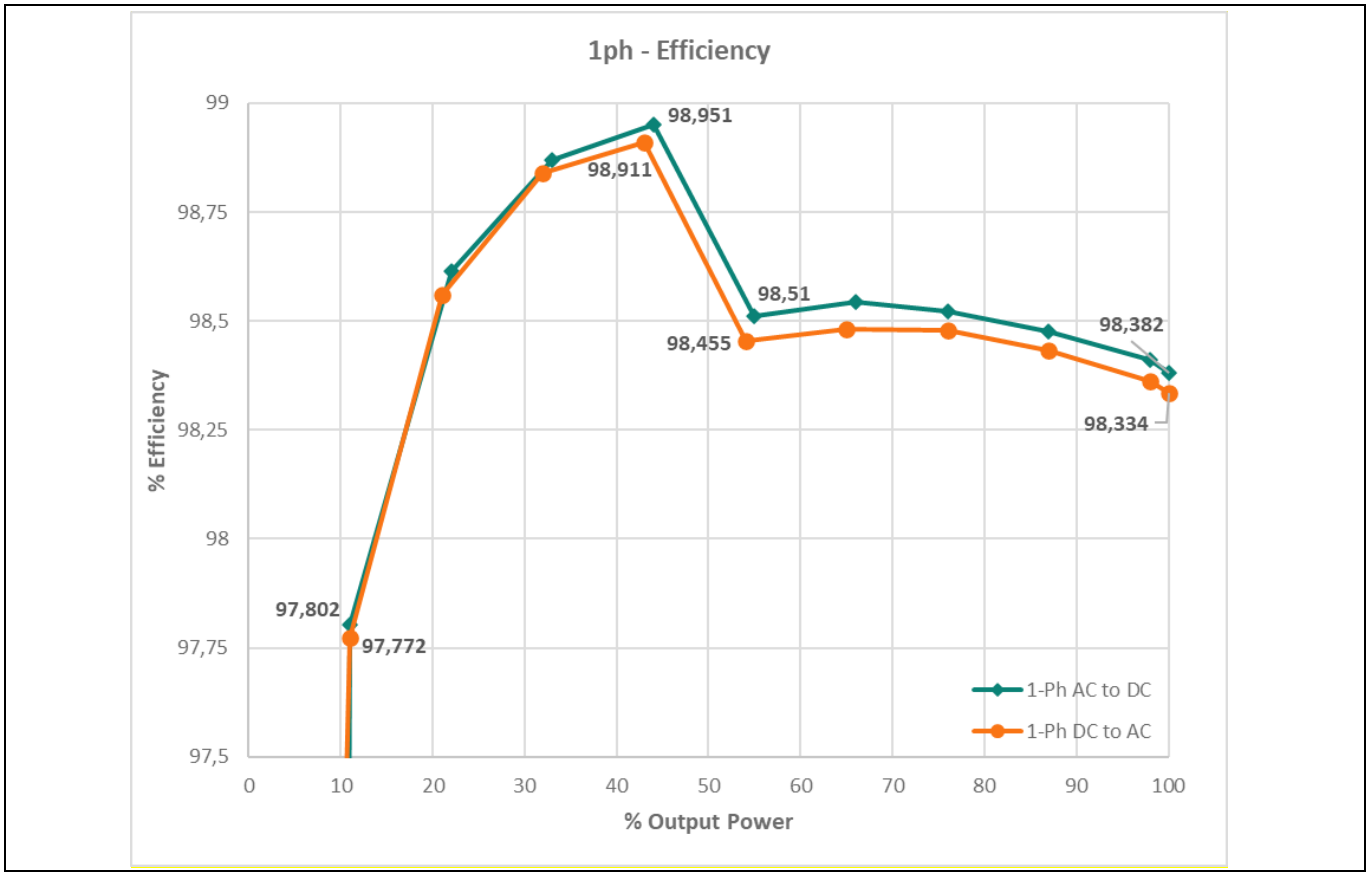

Figure 3 REF_11KW_PFC_SIC_QD measured efficiency for single-phase operation, both AC to DC (PFC mode) and DC to AC (inverter mode)

The key components from Infineon enabling REF_11KW_PFC_SIC_QD are:

- 750V CoolSiC™ Gen 2, 25 mΩ QDPAK (IMDQ75R025M2H), and EiceDRIVER™ 2EDB9259Y for the fast switching half-bridge
- 650V CoolSiC™ Gen 2, 20 mΩ QDPAK (IMDQ65R020M2H), and EiceDRIVER™ 2EDB9259Y for the single-phase power pulsation buffer
- 600 V CoolMOS™ CM8, 16 mΩ QDPAK (IPDQ60R016CM8), EiceDRIVER™ 2EDB9259Y for the line-frequency switching half-bridge
- XMC4400-F100K512 BA microcontroller for the implementation of the digital control
- XENSIV™ TLE4971-A050N5-U-E0001 high precision coreless current sensor for grid current sensing
- Quasi-resonant flyback CoolSET™ IC ICE2QR2280G for auxiliary power supply
- EiceDRIVER™ 2EDN7533R for auxiliary power supply
- OPTIREG™ switcher TLS4120D0EPV33 2.8 MHz synchronous step-down regulator for supplying the 3.3 V rail
- Medium power AF Schottky Diode BAT165
- 60 V N-Channel Small Signal MOSFET BSS138N

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1 Introduction

In the recent decade, power electronic systems have been developing towards higher efficiency and higher power density, as well as lower system cost. This application note demonstrates a viable system solution (REF_11KW_PFC_SIC_QD) for 800 VDC based three-/single-phase converters. The demonstrated system solution achieves premium power density and efficiency by introducing multi-level topology and lower voltage rating power semiconductors with better figure-of-merit into the system. The use of 600 – 750 V power semiconductors in the 800 VDC based system makes it possible to switch at a frequency of 65 kHz, reducing the size of magnetics, boosting the efficiency, and increasing the power density. The following subsection overviews the state-of-art topologies and shows the advantages of the selected topology.

1.1 Overview of feasible topologies

This section compares the four typical topology implementations for an 800 VDC bus system, focusing on practical trade-offs in efficiency, component selection, EMI performance, and implementation complexity.

Two-level half-bridge (2L-HB) topology: is the most established and widely adopted AC-DC architecture. It requires high-voltage semiconductors rated for 1200 V (e.g., Si IGBTs or SiC MOSFETs) to support the 800 VDC bus as shown in Figure 4 (a). While it offers a simple design and robust operation, it inherently exhibits high-voltage slew rates (dv/dt), leading to increased EMI, and necessitating a large PFC choke, which can limit power density. Plus, operating the 2L-HB with high frequency (e.g., 65 kHz and above) is not prefered due to the high switching losses. Nevertheless, it is still the mainstream in the market.

Three-level T-type neutral-point-clamped (3L-TNPC) topology: shown in Figure 4 (b) improves upon the 2L-HB by reducing the effective dv/dt, due to its 3-level switching nature. This enables a smaller PFC choke and better EMI behavior. The topology still requires 1200 V-rated devices, similar to the 2L-HB, but provides notable improvements in power density and system performance.

Three-level active-neutral-point-clamped (3L-ANPC) topology: Figure 4 (c) shows the classical NPC architecture by replacing two clamping diodes with actively controlled switches. This modification enhances system efficiency, provides better thermal distribution, and allows more flexible modulation strategies. A key benefit of the 3L-ANPC is that it can be implemented entirely with lower-voltage semiconductors (600 V–750 V), which are more efficient. The 3L-ANPC topology is well proven in the PV systems and multiple modulation schemes exist for this topology, with some approaches using only two high-frequency switches and four line-frequency devices — while maintaining full bidirectional operation and high efficiency.

The three-level flying-capacitor (3L-FC) topology in Figure 4 (d) uses four 600 V–750 V switches and a flying capacitor per phase leg. This architecture enables higher apparent switching frequency (via phase-shift modulation), which leads to further reduction in choke size. In practice, maintaining the flying capacitor voltage at half the DC bus voltage under all operating conditions — especially during startup, surges, or load transients — adds control complexity and may require auxiliary circuitry.

Among the various bidirectional PFC topologies for an 800 V DC bus, the 3L-ANPC stands out as the preferred choice due to its superior performance in terms of efficiency, power density, as well as the robustness. Compared to the traditional 2-Level and other 3-Level topologies, the 3L-ANPC enables the use of lower voltage-rated power devices (600 V–750 V), which significantly reduces switching losses and provides better figure-of-merits on device level. By replacing certain clamping diodes with active switches, it achieves better loss distribution and higher overall system efficiency. When combined with CoolMOS™ super-junction MOSFETs and CoolSiC™ devices, the 3L-ANPC topology delivers exceptional power density and reliability, meeting the stringent requirements of high efficiency, compactness, and robustness.

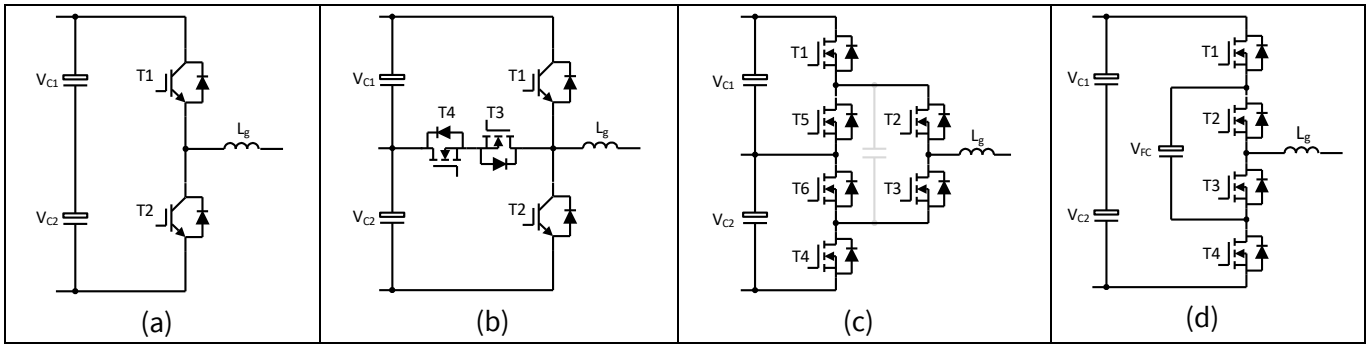


Figure 4 **Topology candidates for bidirectional AC-DC power converters featuring 800 V_{DC} bus in a single leg representation. (a) Two-level half bridge (2L-HB); (b) Three-level T-type neutral-point-clamped (3L-TNPC); (c) Three-level active-neutral-point-clamped (3L-ANPC); (d) Three-level flying-capacitor (3L-FC)**

1.2 Introduction to REF_11KW_PFC_SIC_QD

This reference design shows how to implement a three-level ANPC converter that limits the voltage stress on all the power components to only half of the DC bus voltage, allowing use of power components with better figure-of-merit. The main characteristics of the presented design are:

- Bidirectional 11 kW three-phase/7.3 kW single-phase PFC or inverter power stage using Si/SiC switches
- 600 V- rated switches in 800 V system due to three level toplogy
- Hall-based current sense (high accuracy, stray field suppression, and stability overtemperature)
- High-power/volume density due to high switching frequency (65 kHz) and high efficiency (>98.5% at full load)
- System reliability improvement by low voltage stress on the switches

This reference design is built in a compact form factor (Figure 5) with the following sub-assemblies Figure 6):

- Main board (M300001015) – comprises EMI filters, driver circuits and power stages attached to heatsink
- Bias supply card (BS200001015) – quasi-resonant flyback and ring oscillator circuits for isloated outputs
- Control card (CD300001015) – MCU, Bluetooth module, temperature measurement, and regulator IC units
- Capacitor card (C200001015) – DC bus capacitors with active voltage balancing circuitry

The reference board REF_11KW_PFC_SIC_QD bottom side is mounted on heat sink and the top side is covered by a plastic enclosure.

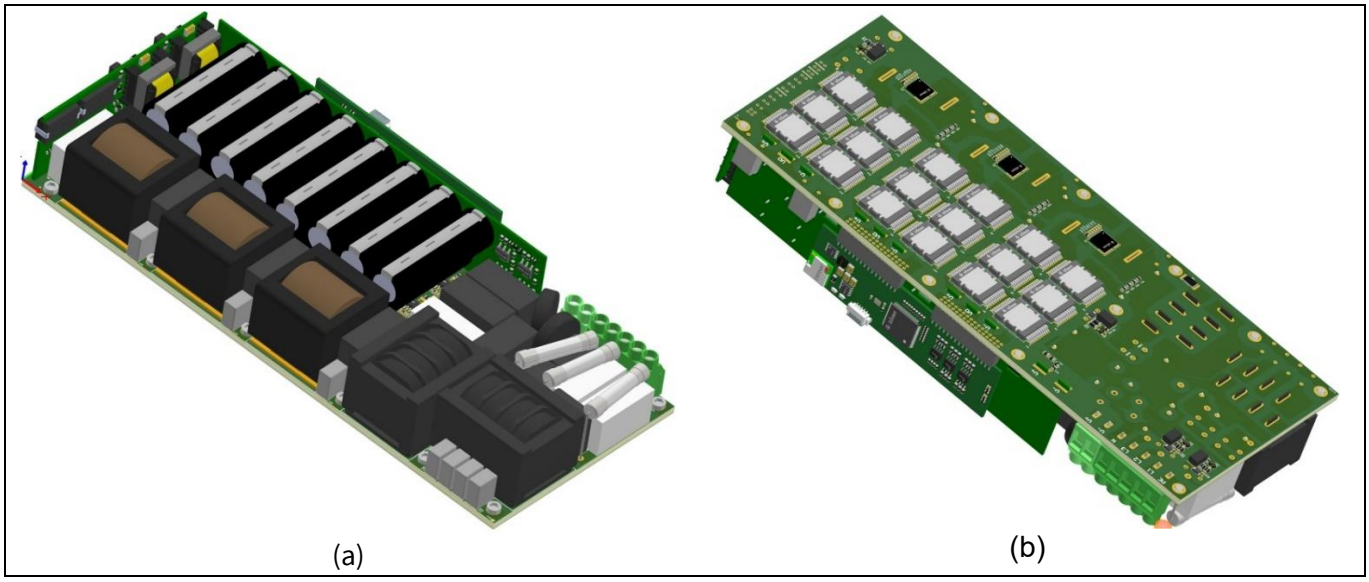
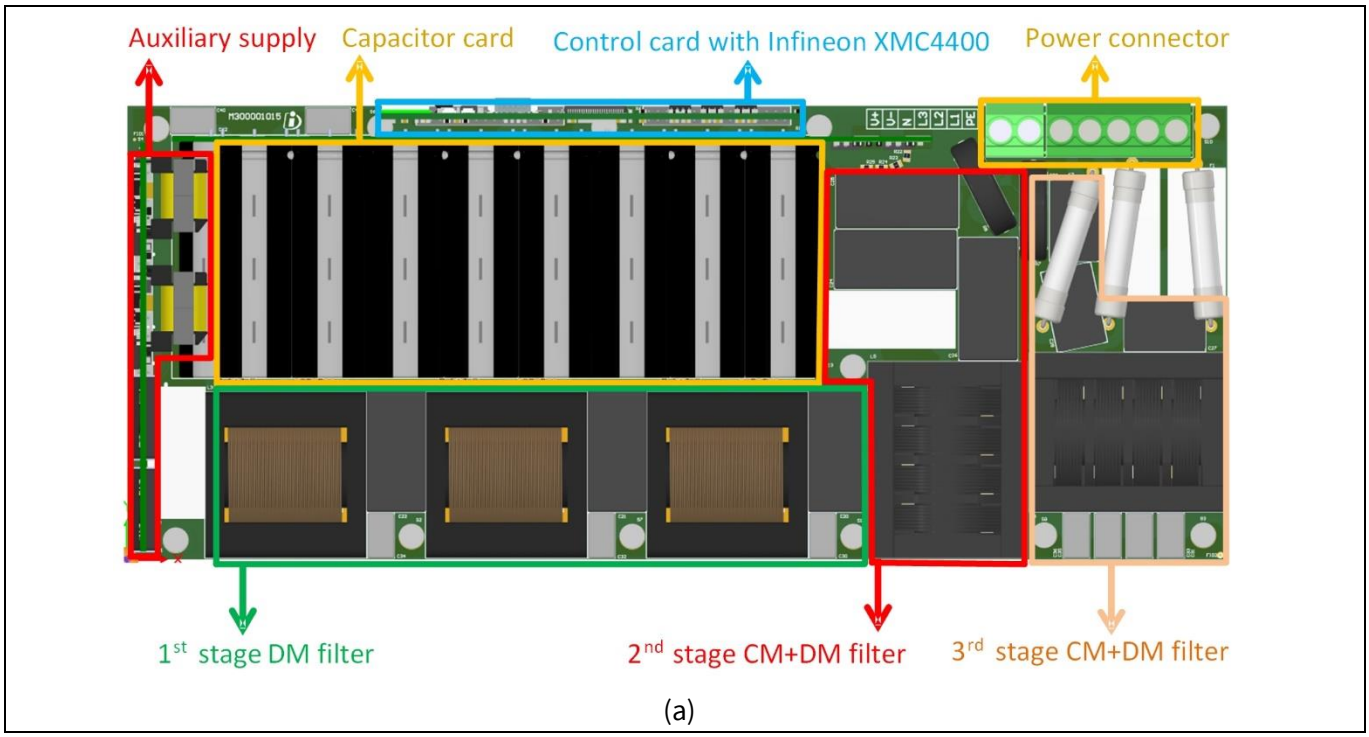


Figure 5 REF_11KW_PFC_SIC_QD captured from CAD software; (a) Top view ; (b) bottom view



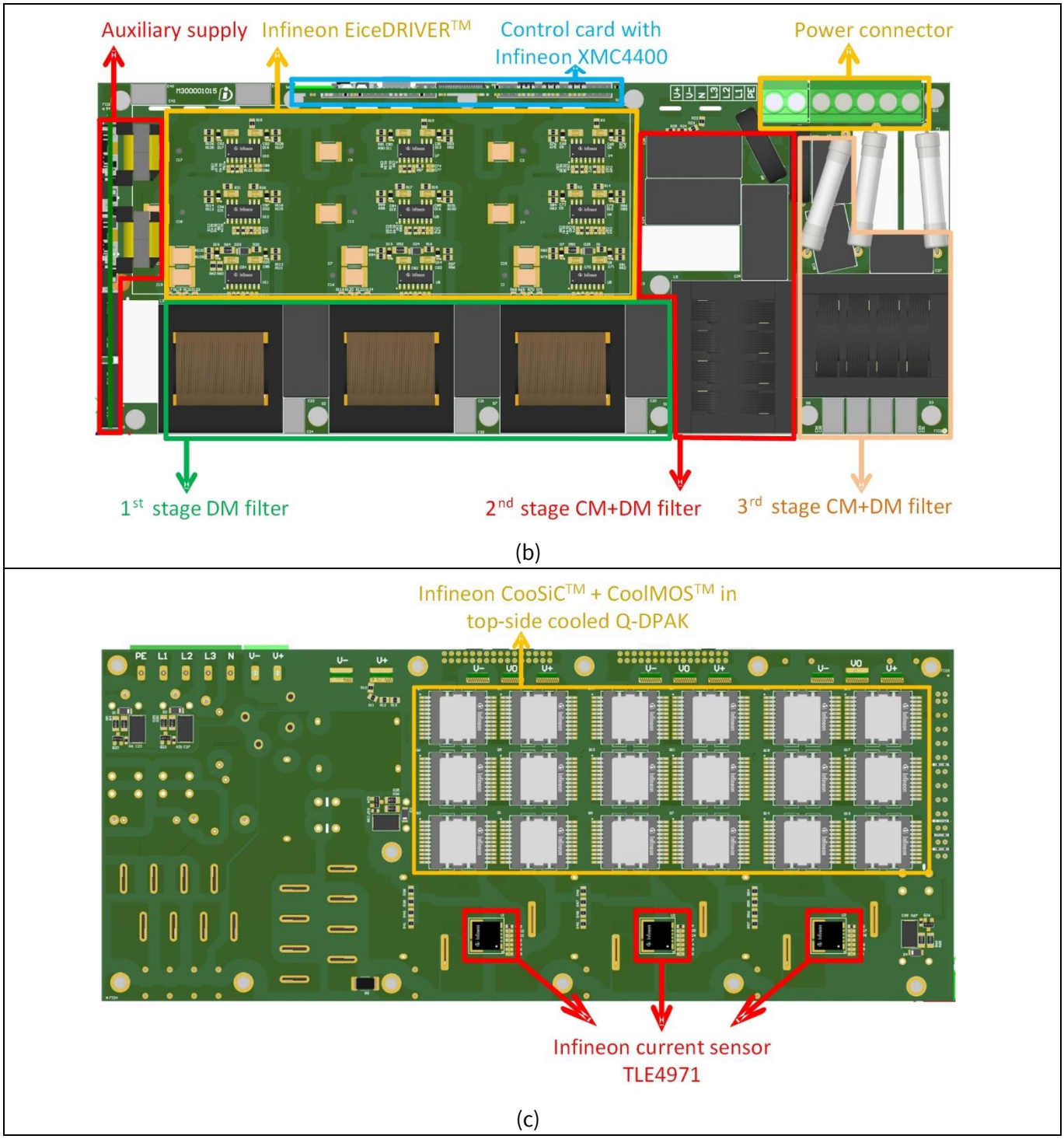


Figure 6 REF_11KW_PFC_SIC_QD captured from CAD software; (a) Top view with capacitor board assembled; (b) top view with capacitor board removed; (c) bottom view

1.3 Specifications

The specifications of the converter under tested conditions are highlighted in Table 1.

Table 1 Specification of REF_11KW_PFC_SIC_QD

Parameter	Symbol	Values			Unit	Note/Test condition
		Min.	Max.	Typ.		
3-Phase AC voltage (RMS)	V_{AC}	318	400	480	V	RMS value
1-Phase AC voltage (RMS)	V_{AC}	180	230	265	V	RMS value
AC frequency	f_{AC}	–	50	–	Hz	–
Nominal DC bulk voltage	V_{DC}	–	800	–	V	–
AC RMS current (3-phase)	I_{RMS}	–	16	–	A	per phase
AC RMS current (1-phase)	I_{RMS}	–	32	–	A	total phase current
Output power (3-phase)	P_{OUT}	–	11000	–	W	–
Output power (1-phase)	P_{OUT}	–	7300	–	W	–
Operating ambient temperature	T_{AMB}	–	25	–	°C	–
Peak to peak DC split voltage ripple	ΔV_{DC}	–	–	70	V	1-phase/3-phase maximum
Power density	–	–	11.3	–	kW/L	Without heatsink
Power factor (3-phase)	PF	0.95	–	0.999	–	Min: 10% load, Max: full-load
Power factor (1-phase)	PF	0.96	–	0.999	–	Min: 10% load, Max: full-load
Input current THD (3-phase)	iTHD	1.6	–	12	%	Min: full-load, Max:10% load
Input current THD (1-phase)	iTHD	1.4	–	15	%	Min: full-load, Max:10% load
Switching frequency	f_{SW}	–	65	–	kHz	–
Efficiency performance						
Efficiency (3-phase PFC)	η_{180V}	97.8	98.63	98.87	%	Min: 10% load, Typ: full-load, Max: half-load
	η_{230V}	98.3	98.96	99.15		
	η_{265V}	98	99.19	99.29		
Efficiency (3-phase Inverter)	η_{180V}	97.25	98.63	98.85	%	Min: 10% load, Typ: full-load, Max: half-load
	η_{230V}	97.8	98.83	99.12		
	η_{265V}	98	99.16	99.26		
Efficiency (1-phase PFC)	η_{180V}	97.5	97.95	98.66	%	Min: 10% load, Typ: full-load, Max: half-load
	η_{230V}	97.8	98.38	98.95		
	η_{265V}	97.8	98.66	99.08		
Efficiency (1-phase Inverter)	η_{180V}	97.5	97.95	98.67	%	Min: 10% load, Typ: full-load, Max: half-load
	η_{230V}	97.75	98.33	98.91		
	η_{265V}	97.5	98.6	99.03		
Protection limits						
Grid-side AC voltage per phase	V_{AC}	180	–	265	V	RMS, line-to-neutral
Grid-side over-current limit	OCL	–	–	35	A	Peak value

Parameter	Symbol	Values			Unit	Note/Test condition
		Min.	Max.	Typ.		
Split capacitor over-voltage protection	OVP	–	–	440	V	Each split capacitor
DC-side under voltage protection	UVP	510	-	750	V	Related to V_{AC}
Inverter mode DC voltage	$V_{DC,INV}$	750	–	880	V	Peak value
Heatsink temperature	$Temp_{HS}$	–	–	90	°C	@T_{AMB} = 25°C
Inductor temperature	$Temp_{Choke}$	–	–	120	°C	

2 System overview and description

REF_11KW_PFC_SIC_QD utilizes the well-proven 3L-ANPC topology. This section provides information on the operation principle of a single 3L-ANPC phase leg along with topics such as switching loop minimization and startup precharging.

Additionally, it also provides information on the two operating modes, i.e., three- and single-phase operation. For single-phase operation, an operation method to mitigate the 50 Hz DC midpoint voltage fluctuation is presented.

2.1 3L-ANPC phase leg modulation

The 3L-ANPC power stage is inherently capable of bidirectional operation. The single phase-leg representation of the three-level active neutral-point clamped (3L-ANPC) converter implemented in REF_11kW_PFC_SIC_QD is depicted in Figure 7.

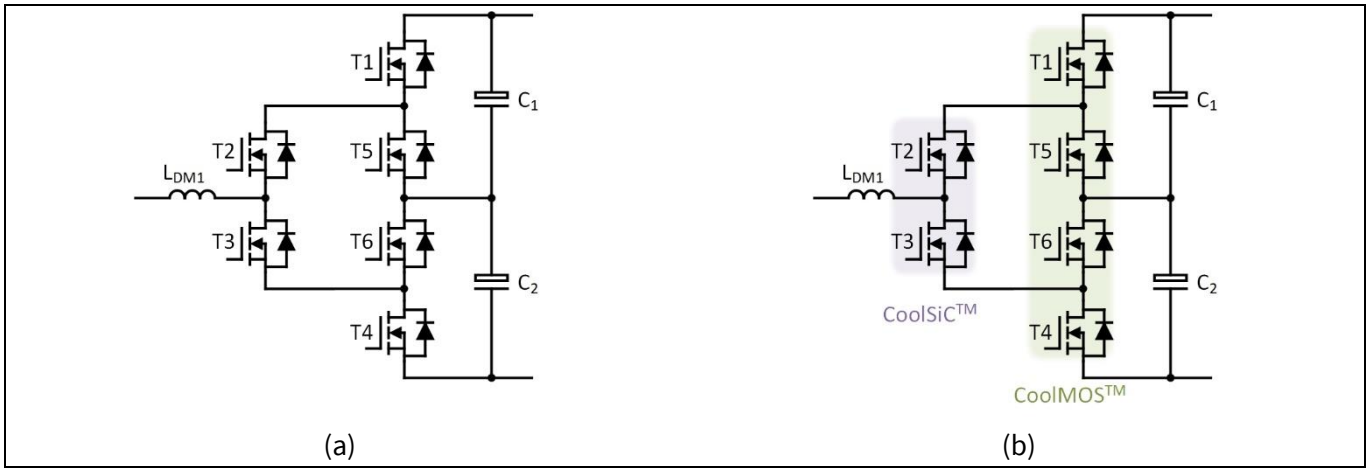
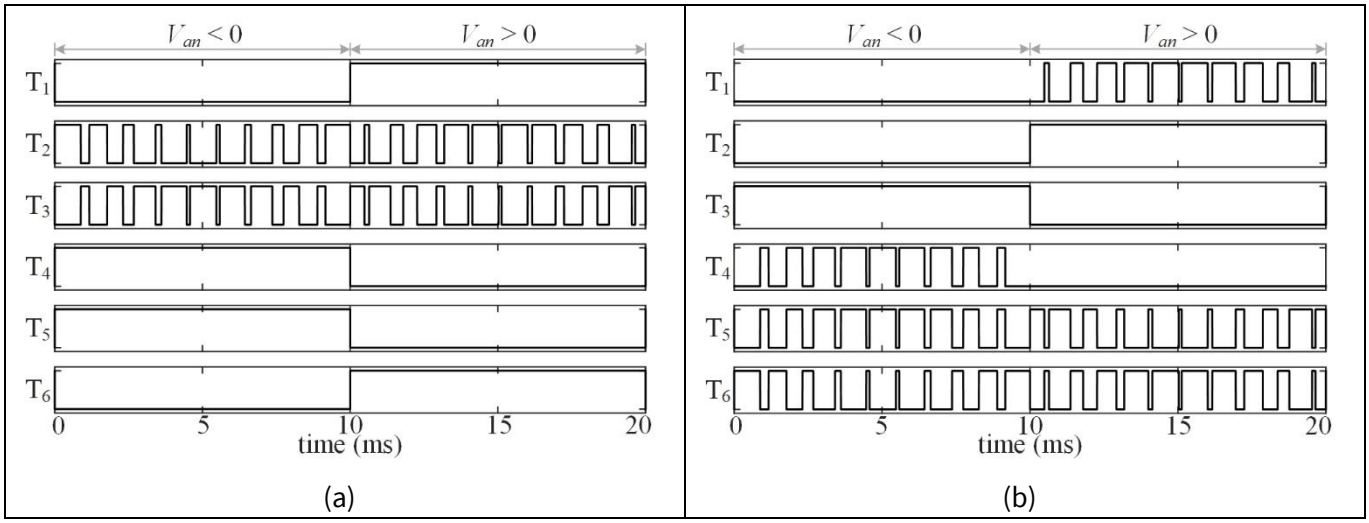


Figure 7 Circuit diagram of a single phase-leg of 3L-ANPC. (a) General drawing without assignment of CoolMOS™ and CoolSiC™; (b) Detailed drawing with assignment of CoolMOS™ and CoolSiC™ for modulation scheme I



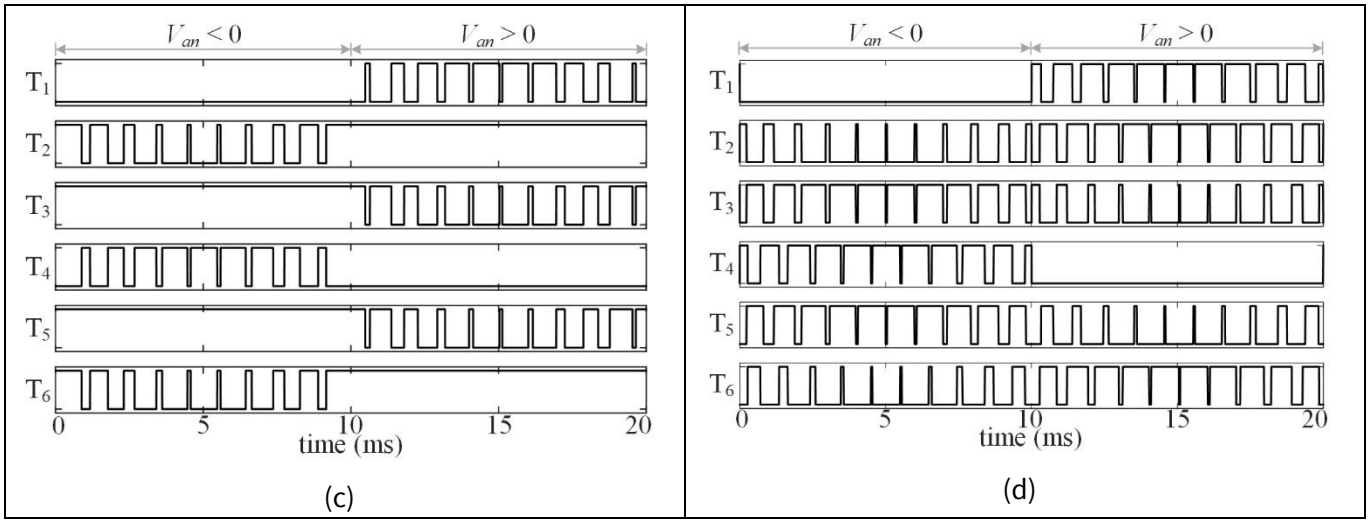


Figure 8 Modulation scheme of 3L-ANPC phase-leg. (a) Modulation scheme I; (b) Modulation scheme II; (c) Modulation scheme III; (d) Modulation scheme IV

Multiple modulation principles of 3L-ANPC converter are depicted in Figure 8 (a) and (d), which can be found in literatures [1]-[7]. These swiching patterns greatly affect the power loss distribution among the six switching devices. Particularly, the modulation scheme IV shown in Figure 8 (d) achieves the so-called switching-frequency-doubling at the swich-node, by applying the phase shift technique to the modulation carrier.

The key difference between them is the number of devices switching at high-frequency, e.g., 65 kHz, and line freuqnecy, e.g., 50 Hz. Those under line-frequency switching are implemented with Si-based power semiconductors, e.g., Si IGBT and Si super junction MOSFET, while those under high-frequency switching are implemented with wide-band-gap (WBG) power semiconductors, e.g., SiC MOSFET and GaN HEMT. Therefore, the cost and control complexity of various modulation methods differs. Considering these, this work adopts the simplest modulation pattern with the lowest number of high-frequency devices, i.e., two high-frequency-switching devices and four line-frequency switching devices.

The selected modulation scheme of one single phase-leg is illustrated in Figure 8 (a). With this scheme, the control and modulation complexity as well as the system cost of 3L-ANPC converter is minimized, compared to other schemes. The two devices T_2 and T_3 switch at high frequency, i.e., 65 kHz, which are implemented with 750 V/650 V CoolSiC™. Moreover, the four devices T_1 and T_4 – T_6 commutate at 50 Hz/60 Hz and can be implemented with Si CoolMOS™.

Since those devices bear only the conduction loss, it is very flexible for the power converter designer to scale the power level by selecting the proper R_{DSON} of the CoolMOS™. With the low R_{DSON} achievable by the CoolMOS™, the 3L-ANPC converter with the selected modulation features much lower conduction loss compared to its counterparts. Additionally, the R_{DSON} selection of CoolSiC™ T_2 and T_3 can be solely optimized based on the balance between switching and conduction losses.

Note: Assuming the DC-bus overall voltage as 800 V, all switching devices can be implemented with 600 V-750 V ratings, which provides better figure-of-merit compared with 1200 V devices.

2.1.1 Operation principle

Single phase-leg is considered as shown in Figure 9 and Figure 10 where, Figure 9 demonstrates the operation principle of single ANPC phase leg during the positive line-cycle. The line frequency CoolMOS™ T_1 and T_6

switches are kept on during the positive line cycle, whereas the other CoolMOS™ T_4 and T_5 switches are kept off. The two high-frequency CoolSiC™ T_2 and T_3 switches at 65 kHz in a complimentary way.

In the PFC mode, (i.e., the inductor current flows from the grid-side to the converter-side), when T_2 conducts, the inductor L_{DM1} current charges the upper bulk capacitor (C1) through T_1 and T_2. On the other hand, when T_3 conducts, the grid current charges the inductor L_{DM1} through T_6 and T_3.

In the inverter mode, (i.e., the inductor current flows from the converter-side to grid-side), when T_2 conducts, the upper bulk capacitor (C1) charges the inductor. On the other hand, when T_3 conducts, the inductor current gets discharged by the grid voltage.

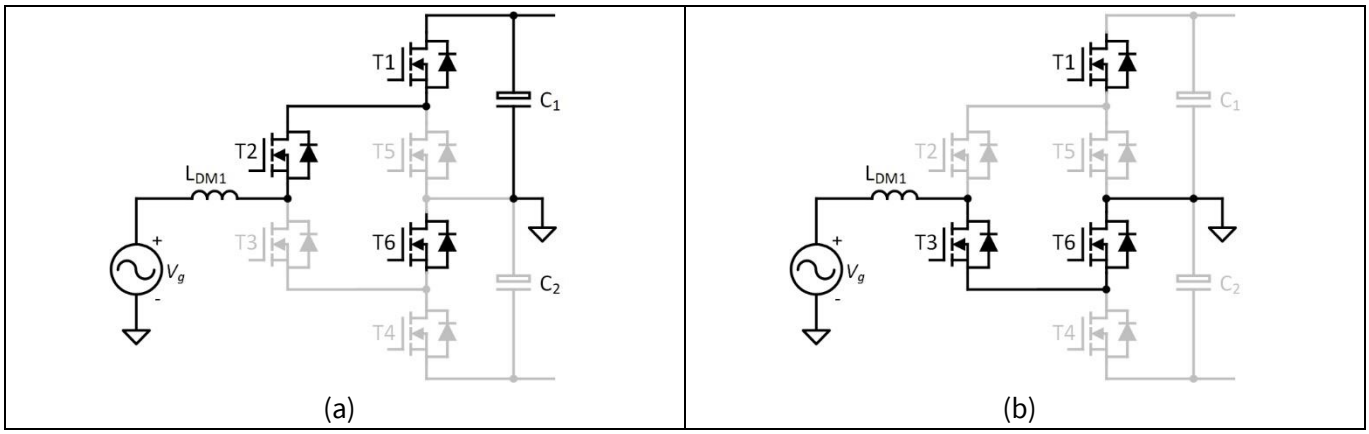


Figure 9 Operation principle of single ANPC phase leg during positive line cycle. (a) When T_2 conducts; (b) When T_3 conducts

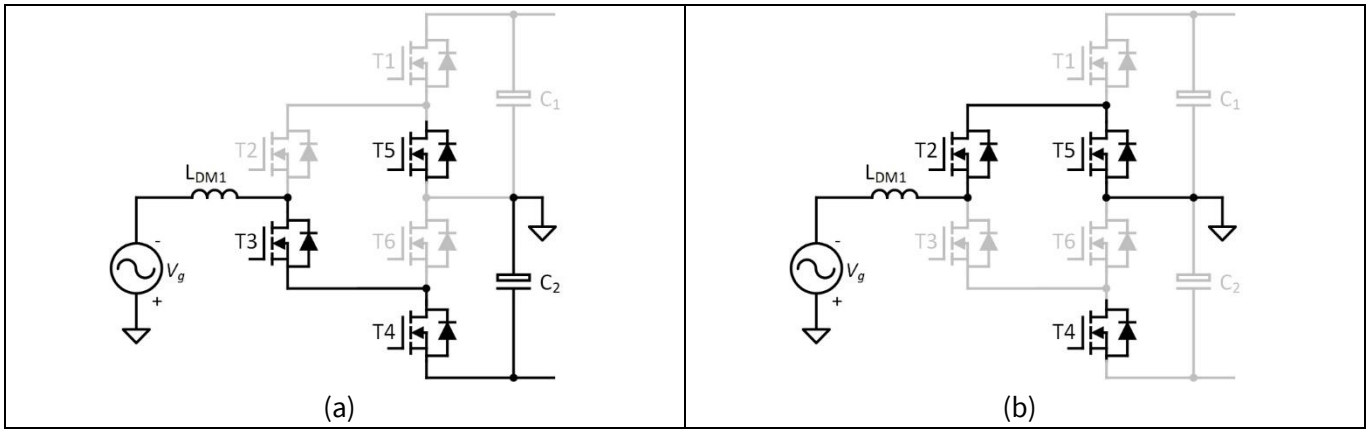


Figure 10 Operation principle of single ANPC phase leg during negative line cycle. (a) When T_3 conducts; (b) When T_2 conducts

Figure 10 demonstrates the operation principle of single ANPC phase leg during the negative line cycle. The line frequency CoolMOS™ T_4 and T_5 are kept on during the negative line cycle, whereas the other CoolMOS™ T_1 and T_6 are kept off. The two high-frequency CoolSiC™ switch at 65 kHz in a complimentary manner.

In the PFC mode, (i.e., the inductor current flows from the converter-side to the grid-side), when T_3 conducts, the inductor L_{DM1} current charges the lower bulk capacitor (C2). On the other hand, when T_2 conducts, the grid charges the inductor L_{DM1}.

In the inverter mode, (i.e., the inductor current flows from the grid-side to converter-side), when T_3 conducts, the lower bulk capacitor (C2) charges the inductor. On the other hand, when T_2 conducts, the grid inductor gets discharged by the grid voltage.

2.1.2 Decoupling capacitor to close switching loop

As mentioned, the adoped modulation method features easy implementation and lowest BOM cost compared with other ANPC modulation methods as it switches the lowest device count in high-frequency. However, one of the significant drawbacks of this method is that the switching loop is relatively long compared to the other modulation methods [7].

As shown in Figure 11 (a), the switching loop consists of switches T_2, T_3, T_4, C2, and T_5. All the device bonding inductance, the PCB trace inductance, and the ESL of capacitor contributes to the overall switching-loop inductance. This big loop inductance will induce high overshoot voltage on the high-switching-speed SiC MOSFETs. In some cases, the switching dv/dt has to be lowered in order to secure the fast-switching SiC MOSFETs. This disadvantage significantly hinders the benefit of fast-switching CoolSiC™ in the application of the aforementioned ANPC modulation method.

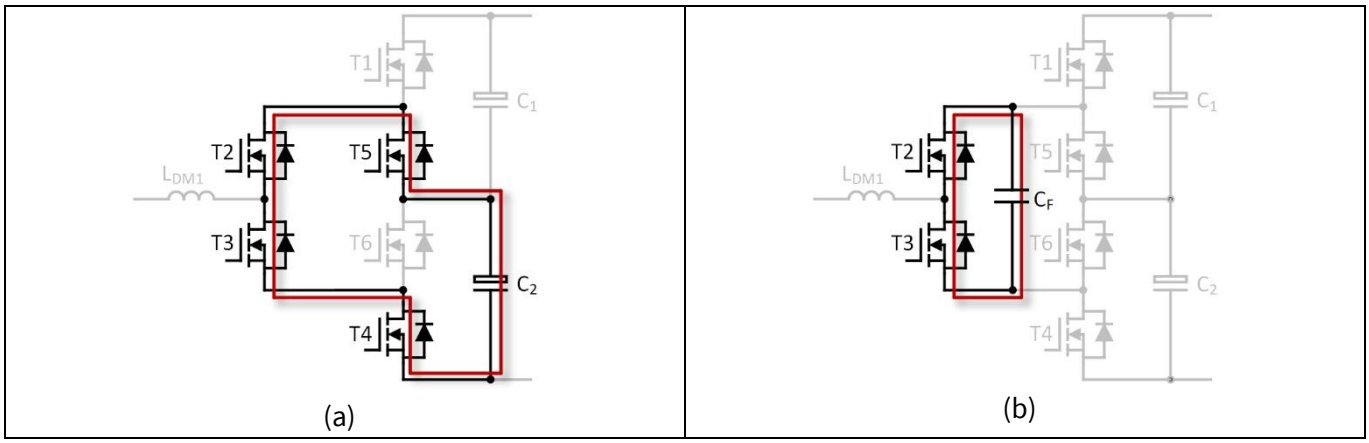


Figure 11 Commutation loop of 3L-ANPC phase leg. (a) Without a decoupling capacitor connected directly to the fast-switching leg T_2-T_3; (b) With a decoupling capacitor C_F connected directly to the fast-switching leg T_2-T_3

In reference [8], a RC series snubber circuit is added to the high-frequency switching SiC half-bridge (T_2-T_3). The RC circuit provides a low impedance for the switching-transient current. In this way, the swiching loop can be closed without switches T_4, C2, and T_5. Therefore, the fast-switching SiC MOSFETs see much less voltage overshoots. In this circuit, the resistor functions to dampen the switching oscillation, as well as to limit the current overshot caused by the switching of line-frequency MOSFETs under the condition when the two bulk voltages are not perfectly equal. However, the resistor can bring additional inductance to the loop. From the power-dense-layout perspective, the insertion of a resistor makes the switching cell no longer compact.

Therefore, in this reference design, only a single decoupling capacitor in the capacitance range of 100 nF to 200 nF (under the applied voltage level) is used across the half bridge formed by T_2 and T_3. According to experiment results, the decoupling capacitor significantly reduces the switching-loop inductance and limits the V_{DS} overshoot during switching transients. However, this small decoupling capacitor needs to be properly pre-charged during startup.

2.1.3 Pre-charging of decoupling capacitor during startup

During the PFC mode (either three phase or single phase) startup, the grid voltage naturally activates the current path through the decoupling capacitor, therefore, the decoupling capacitor can be passively charged. Figure 12 depicts the circuit diagram and simulation waveform during the passive precharge. It can be seen that, during positive line cycle, the current path containing the body diodes of T_2 and T_6, as well as the decoupling capacitor is activated, and the decoupling capacitor is clamped to the upper bulk capacitor voltage. This is verified with the simulation waveform shown in Figure 12 (b). Then, when the PWM signals are enabled, no voltage difference exists between half-bulk voltage and decoupling capacitor voltage. Therefore, the line-frequency switches T_1, T_5, T_6, and T_4 see no inrush current during switching.

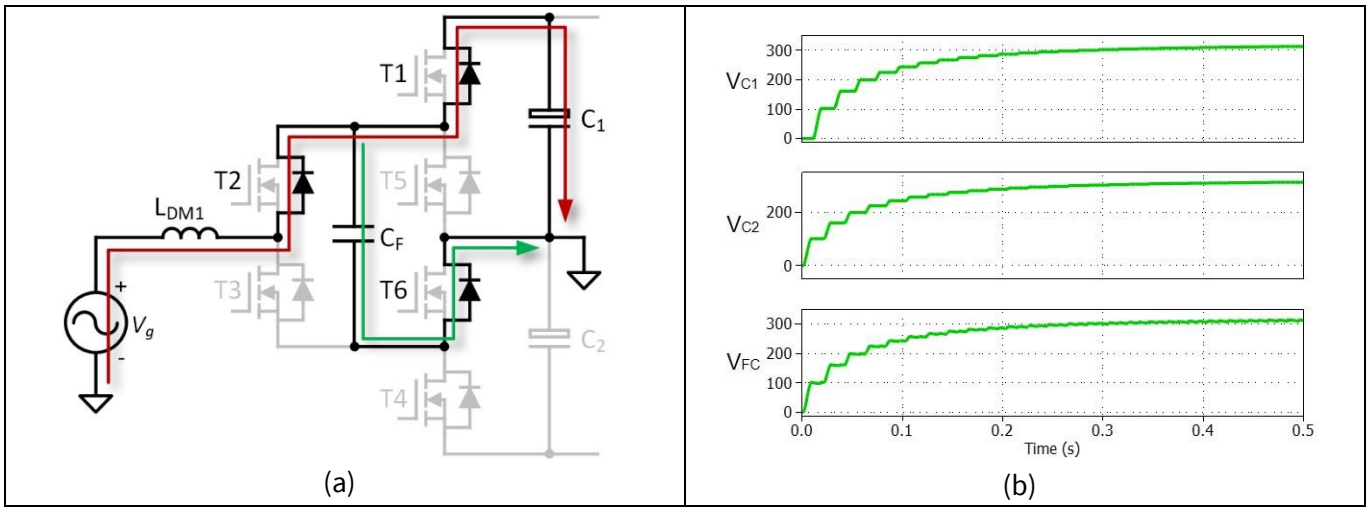


Figure 12 Passive pre-charging of the de-coupling capacitor. (a) Circuit diagram during passive precharge; (b) Simulation waveform during passive precharge

However, the grid can only charge the decoupling capacitor to the grid AC peak value. In the case that a DC source with terminal voltage is higher than two times of the grid AC peak voltage, i.e., during the inverter mode startup, high inrush current can be present when the line-frequency devices conducts due to the significant voltage difference between bulk capacitor and decoupling capacitor. Moreover, when the converter is going to operate under islanding mode, there is no voltage source present at the AC side to passively precharge the decoupling capacitor.

To handle the inverter mode (including islanding mode) startup more safely in REF_11kW_PFC_SIC_QD, an active pre-charging method is implemented. Figure 13 (a) depicts the circuit diagram during active pre-charge without grid voltage. During the process, device T_6 is kept on, while device T_1 is given short PWM pulses to its gate. In this way, the current path highlighted by the red-solid line is enabled. Figure 13 (b) and (c) present the PWM signal and V_{GS} of T_1, as well as the decoupling capacitor voltage and current in an overall and single switching cycle view, respectively.

It is concluded that the decoupling capacitor is slowly precharged to half-DC-link voltage, i.e., 400 V, and the charging current is controlled below 50 A in transient pulses to protect the power semiconductor devices. In the case scenario that the grid voltage is present, the operation of switch pair T_1-T_6 is only valid under positive line cycle, otherwise the inductor L_{DM1} current is out of regulation.

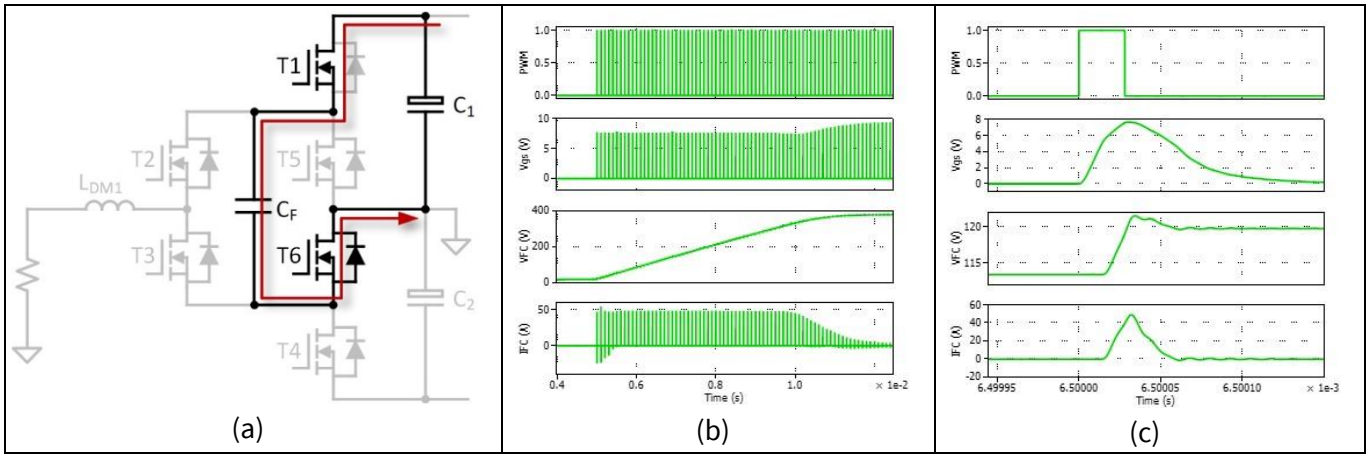


Figure 13 Active pre-charging of the decoupling capacitor. (a) Circuit diagram during active pre-charge; (b) Simulation waveform during active pre-charge; (c) Zoom-in view in one switching cycle

The device pair of T_5-T_4 can also enable the active pre-charging path in an opposite way, where T_5 is constantly ON and T_4 operates with short pulses. Additionally, the operation of device pair T_5-T_4 is only under negative line cycle if grid voltage is present.

To conclude, the active pre-charge method is only needed during the startup-phase of inverter mode operation. During operation of the converter, i.e., all devices switch according to the modulation scheme shown in Figure 13, the decoupling capacitor voltage is synchronized to either the upper or lower DC bulk voltage, therefore, no active control is required.

2.2 Three-phase configuration

Under three-phase connection, the simplified main power circuit diagram of the system solution REF_11KW_PFC_SIC_QD is demonstrated in Figure 14. The system is connected to three-phase grid without the need of connecting neutral point (N). The three-phase currents flow through three power lines, i.e., L1L1', L2L2', and L3L3'. All three phase legs of the ANPC converter are active and convert power in both AC-to-DC and DC-to-AC operation modes. The neutral power line NN' is not used for power feeding under three-phase connection. Instead, it is utilized as the return path for current ripples as well as to reduce the common-mode noise between the potential DC0 and protective earth. Only three windings of the 4-winding common-mode-choke are utilized for power transfer.

Note: In any power flow operation with REF_11KW_PFC_SIC_QD, leave the N terminal of the board unconnected during three-phase testing.

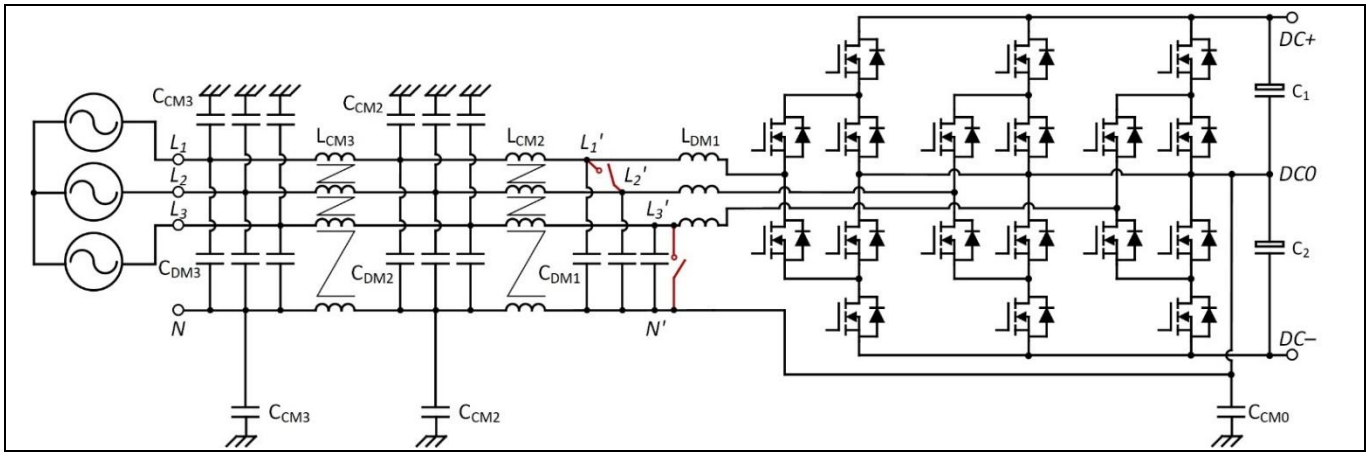


Figure 14 Simplified diagram of REF_11KW_PFC_SIC_QD in three-phase configuration

As shown in Figure 14, the two relays connected between L1'-L2' and L3'-N' are maintained open during the three-phase operation. The main purpose of these two relays is to short the two power lines L1L1' and L2L2', as well as L3L3' and NN' to maximize the utilization of copper content during single-phase operation.

2.3 Single-phase configuration

The simplified main power diagram of the system solution REF_11KW_PFC_SIC_QD under single-phase operation is depicted in Figure 15. Being different from the three-phase operation mode, the two relays connected between L1'-L2' and L3'-N' are maintained closed during the single-phase operation. At the grid side, the terminals (L1 and L2) need to be combined with a short-circuited jumper, as well as the terminals L3 and N.

Note: When intending to start the board with single phase AC supply, externally combining the terminals L1 and L2 together, as well as L3 and N together is necessary.

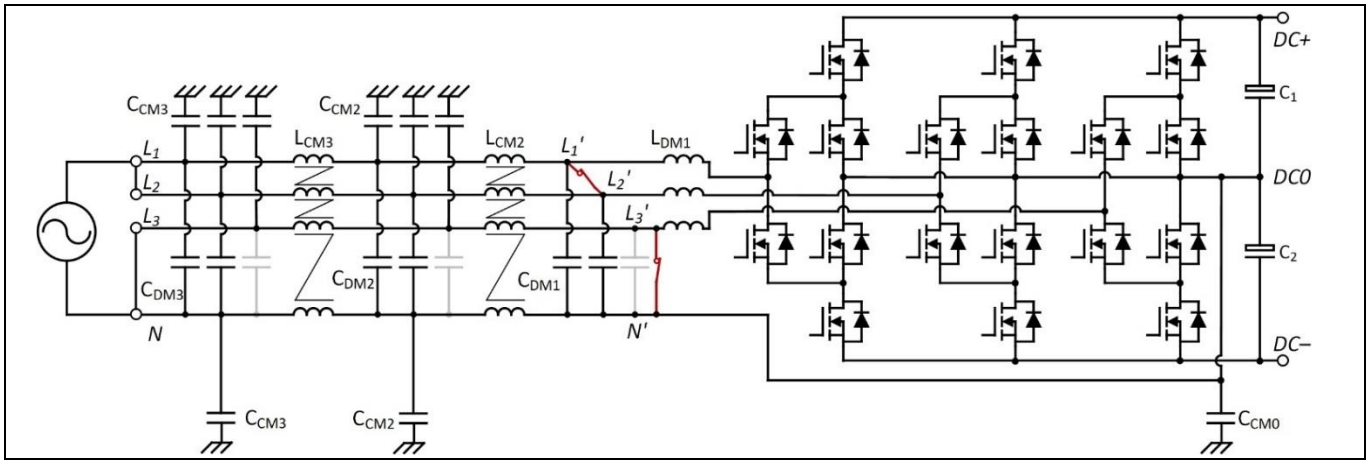


Figure 15 Simplified diagram of REF_11KW_PFC_SIC_QD in single-phase configration

Only two phase-legs (A and B) of the ANPC converter operate in an interleaved way to convert power in AC-to-DC and DC-to-AC operation modes of single-phase configuration. In this way, all four windings of the common-mode choke are utilized. Power lines L1L1' and L2L2' are used as the active line connection in combination, whereas power lines L3L3' and NN' are combined and utilized as neutral return path. This neutral path is finally connected to the mid-point of the DC-side bulk capacitor (DC0). In this way, the output DC voltage can be easily

boosted to 800 V even for single-phase operation. Therefore, no matter the how the grid-side is configured, i.e., either three-phase or single-phase input, the DC side can always maintain 800 V.

Note: Since there is only phases A and B operating to convert power, 2/3 of the three-phase power can be achieved for single-phase AC input.

However, connecting the AC neutral to the DC midpoint results in a large grid current flowing in and out of the midpoint of bulk capacitor bank. Therefore, the midpoint potential fluctuates significantly with 50 Hz content, which stresses the bulk capacitors and pentionally triggers the over/undervoltage protection of the bulk capacitors. A straightforward method to control this fluctuation is to increase the capacitance of the bulk capacitor banks. However, this would result in increased system volume and weight, which is not preferred for power converters with power density and cost constraints. Therefore, a novel operation method is created and implemented, which is explained in detail in Section 2.3.1.

Note: During hardware testing, the software is able to automatically detect whether to operate under three-phase or single-phase mode based on phase voltage measurements if the user connects AC terminals following Figure 14 and Figure 15. Hence, there is no user intervention needed for the microcontroller during the start-up phase.

2.3.1 Basic operational principle of power pulsation buffer

As explained in Section 2.3, single phase operation results in the fluctuation of DC midpoint voltage. The simulated waveforms during single phase operation is shown in Figure 16 (simulation time before 0.60 s in the figure). The two phases A and B operate in an interleaved way so that the overall input current in Figure 16 (a) has a reduced ripple at twice the switching-frequency. It can be seen in Figure 16 (b) that both the upper and lower bulk capacitors exhibit a significant voltage ripple, which contain both 50 Hz and 100 Hz harmonics. However, the overall upper and lower voltage only shows 100 Hz voltage ripple. This indicates that the 50 Hz voltage ripple on the upper and lower bulk capacitors are counter phase, which is caused by the grid current flowing in and out of the DC midpoint. This volage ripple especially at 50 Hz stresses the bulk capacitors and potentially triggers the over/undervoltage protection of capacitors.

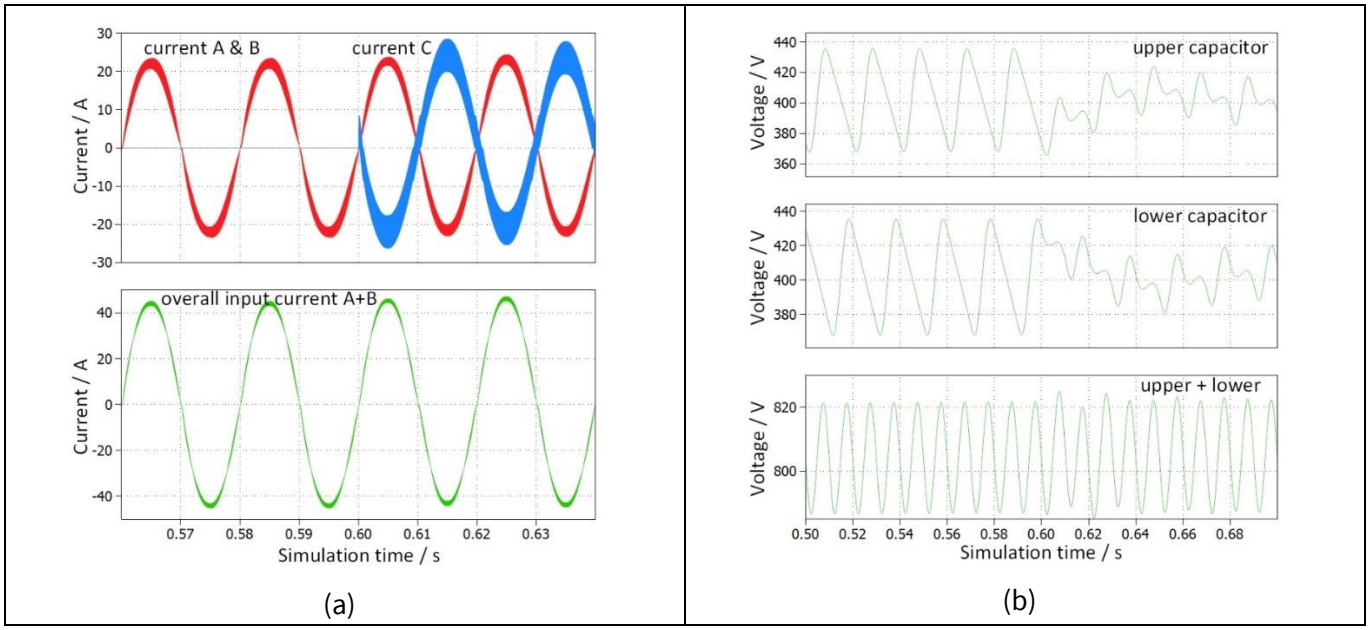


Figure 16 Simulation waveform before and after the operation of phase C as the power pulsation buffer during single-phase operation. (a) Waveforms of separate phase currents and combined input current; (b) Waveforms of separate bulk capacitor voltages and the overall bulk voltage. The capacitance of 1.5 mF for each upper and lower bulk capacitor bank is considered in the simulation

Fortunately, for single phase operation, the yet unused phase leg C of ANPC can be fully utilized to eliminate this 50 Hz voltage fluctuation. To enable this, the relay which connects L3' and N' must be closed, as it is indicated in Figure 15. Then the output of phase leg C is connected back to the DC midpoint via the first differential-mode inductor L_{DM1} and the relay L3'N'.

To highlight the operation method of phase C, the circuit diagram for phase C under single-phase operation is shown in Figure 17 (a). The basic operation principle is to turn-on/off switches T_1 and T_2, as well as T_3 and T_4 simultaneously at high switching frequency, i.e., 65 kHz in this work, and the PWM signals T_1/T_2 and T_3/T_4 are implemented in a complementary way with dead-time inserted. Unlike phase A and B, in order to operate phase C as power pulsation buffer, phase C should be implemented with all CoolSiC™ devices. The switches T_5 and T_6 are left un-modulated. Doing so, the three-level ANPC phase leg is operated the same as a two-level leg, which is depicted in Figure 17 (b).

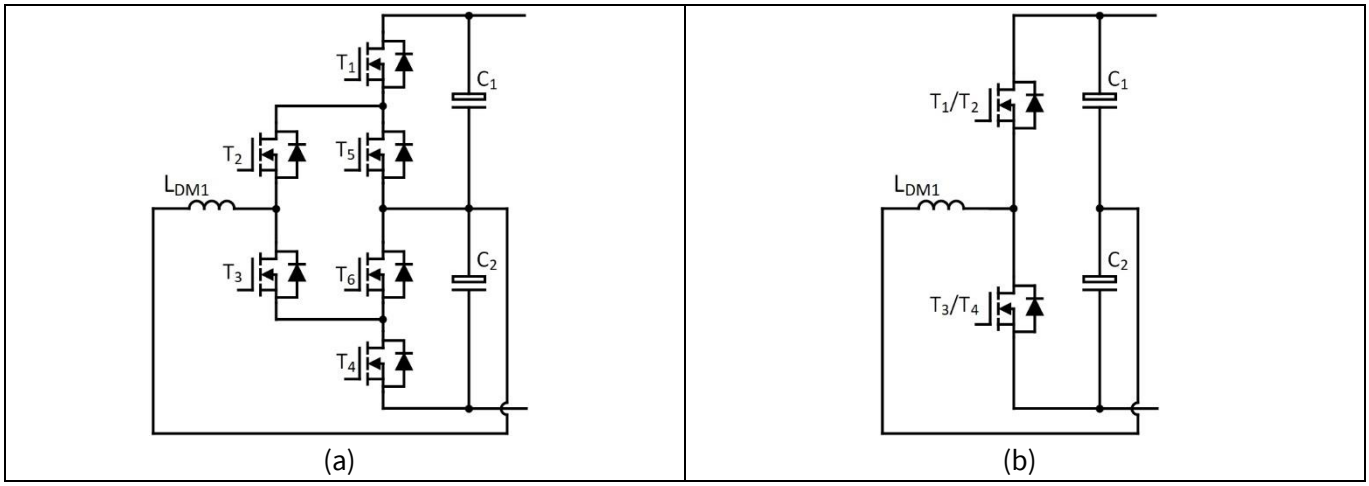


Figure 17 (a) Circuit diagram of phase leg C during single phase operation, when relay L3'N' is closed; (b) Analogy to a two-level phase leg

The simplest way of operation is to assign both device combinations T_1/T_2 and T_3/T_4 a 50% conduction duty, so that the voltage on C_1 and C_2 can be equalized, and the 50 Hz voltage fluctuation can be fully eliminated. However, the inductor (L_{DM1}) current is left uncontrolled and the MOSFETs can be damaged due to the high current. This can be managed by controlling the current on the L_{DM1} inductor in a way that the 50 Hz voltage fluctuation can also be minimized.

As shown in Figure 16 (a), after simulation time 0.6 s, the inductor L_{DM1} current of phase C is controlled to be the same magnitude but 180° out of phase to phase A/B current. As shown in Figure 16 (b), after implementing the phase C operation, i.e., after simulation time of 0.6 s, the voltage ripple on upper and lower capacitors are significantly reduced. An FFT analysis confirms that the 50 Hz ripple magnitude is reduced from 60 V peak-to-peak (before operating phase C) to 16 V peak-to-peak (after operating phase C). The 50 Hz voltage ripple can be fully eliminated if high amplitude of sinusoidal current is injected by phase C. However, the MOSFETs and inductor L_{DM1} on phase C would bear more dissipation dramatically, which is not preferred from economic perspective. Therefore, the fully elimination of 50 Hz voltage ripple is not applied.

This method is easy to implement as the current controller of phase C is assigned with the counter-phase current reference as of phase A/B. The operation of phase C does not affect the grid current waveform quality since it just enables the current to flow inside the power converter.

2.3.2 Practical modulation scheme of phase C as power pulsation buffer

In practice, assigning two switches T_1 and T_2 (or T_3 and T_4) exactly the same PWM signal might be problematic due to tolerance of gate driver propagation delay and MOSFETs turn-on delay. Overvoltage on drain-source voltage might occur and damage the MOSFETs if T_1 and T_2 (or T_3 and T_4) are not turned-on and off simultaneously. Therefore, a practical modulation scheme must be implemented to prevent device damage. Figure 18 (a) presents the modulation scheme and switching wavefoms during the transition from positive output (both T_1 and T_2 on) to negative output (both T_3 and T_4 on).

Two PWM timers are used with a designed small phase delay of 50 ns, which are noted as timer T_1/T_4 and timer T_2/T_3 in Figure 18 (a). After comparator operations in the PWM generation module in the microcontroller, PWM signals of T_1 and T_4 are generated by timer T_1/T_4 whereas, PWM signals of T_2 and T_3 are generated by timer T_2/T_3. Moreover, the dead-time between T_1 PWM and T_4 PWM should be set longer than the dead-time between T_2 PWM and T_3 PWM. The resultant switching signals follow the sequence of T_1 off – T_2 off – T_3 on – T_4 on during the transition from positive output to negative output. On the other hand, during the transition from negative output to positive output, the switching signals follow the sequence of T_4 off – T_3 off – T_2 on – T_1 on.

The equivalent circuits during transitions from positive to negative output and negative to positive output are shown in Figure 18 (b) and Figure 19 (b), respectively. It is noted that, even MOSFETs T_5 and T_6 are left unmodulated, their body diodes are utilized during the transitions. It is important to follow the switching sequence depicted in Figure 18 (a) and Figure 19 (a) in order to ensure that no overvoltage is applied to any MOSFET. The transition interval during which the switching sequence happens should also be minimized since it does not contribute to the 50 Hz voltage fluctuation reduction.

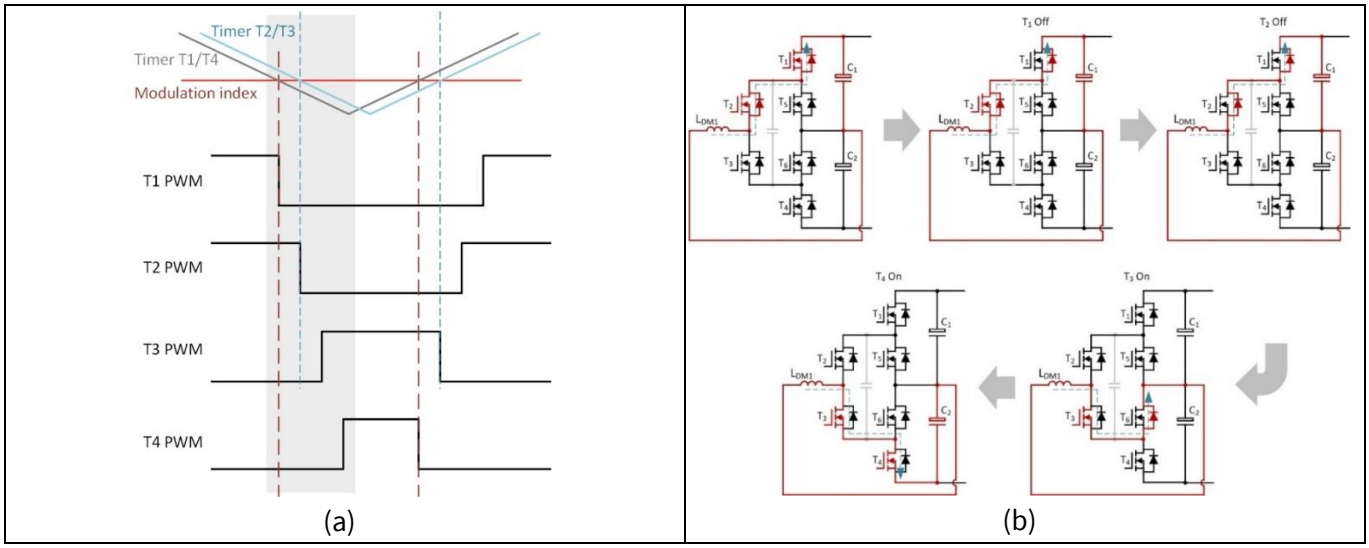


Figure 18 Assuming the inductor L_{DM1} current flows into the bridge. (a) Modulation scheme and switching waveforms during the transition from positive output to negative output; (b) Equivalent circuits during the transition from positive output to negative output

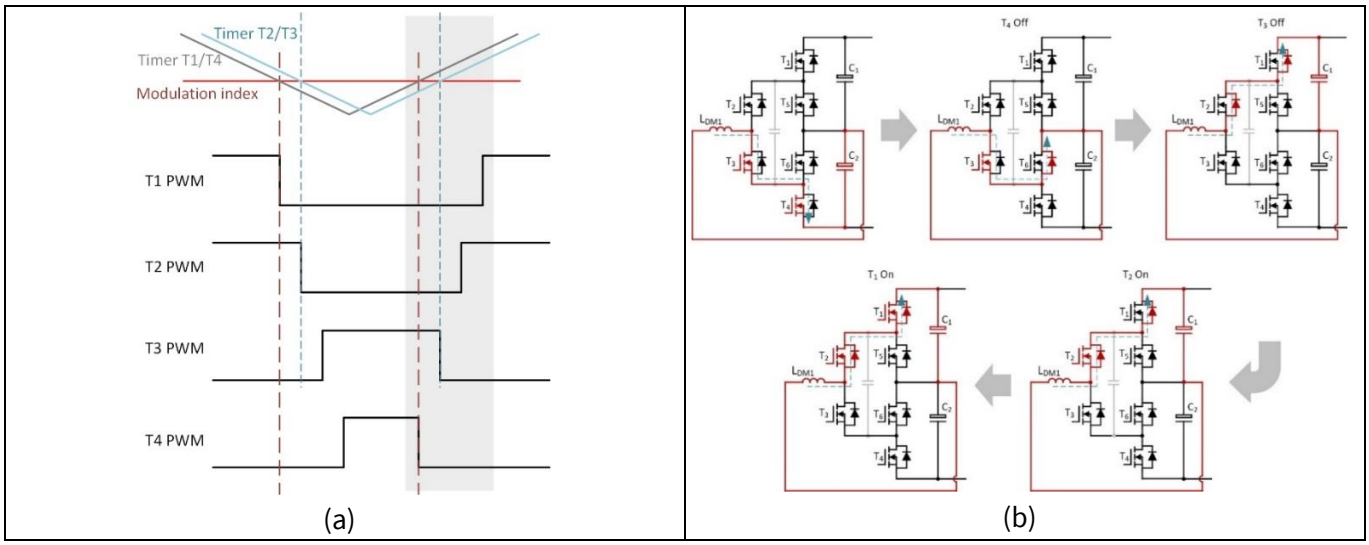


Figure 19 Assuming the inductor L_{DM1} current flows into the bridge. (a) Modulation scheme and switching waveforms during the transition from negative output to positive output; (b) Equavalent circuits during the transition from negative output to positive output

3 System hardware design

To prove the concept of combining CoolMOS™ and CoolSiC™ in a bidirectional 3L-ANPC converter, the system demonstrator REF_11KW_PFC_SIC_QD is designed with high-efficiency and high-power-density targeting EV charging, OBC, energy storage systems, and other applications.

Key system specifications are mentioned in Figure 20. The system can handle both three-phase and single-phase AC input delivering the output power of 11 kW and 7.3 kW, respectively. The output voltage is maintained as 800 VDC for both single- and three-phase inputs.

Figure 20 shows the simplified architecture of the reference design. The hardward design consists of the following parts:

- CoolMOS™ and CoolSiC™ switches are driven by the dual-channel isolated gate driver EiceDRIVER™ 2EDB9259Y. The auxiliary power supply unit is fed from DC bus, i.e., both from positive-half and negative-half DC rails
- Quasi-resonant flyback controller integrated power IC CoolSET™ ICE2QR2280G together with EiceDRIVER™ 2EDN7533R in ring oscillator concept are used to generate eleven channels of isolated 18 V bias supplies to drive all the power switches
- The CoolMOS™ and CoolSiC™ in the top-side cooling (TSC) package Q-DPAK are implemented in the prototype to demonstrate its capability to enable high power density designs
- The system efficiency at full load is boosted by 25 mΩ R_{DSON} CoolSiC™ IMDQ75R025M2H in the high-frequency leg and 16 mΩ R_{DSON} CoolMOS™ IPDQ60R016CM8 devices in low-frequency legs
- The current measurements for current loop control are realized by Infineon's XENSIV™ TLE4971 current sensors. The demonstrator is digitally controlled using Infineon microcontroller XMC4400 series. The peak efficiency can reach upto ~99.2% with the proposed solution

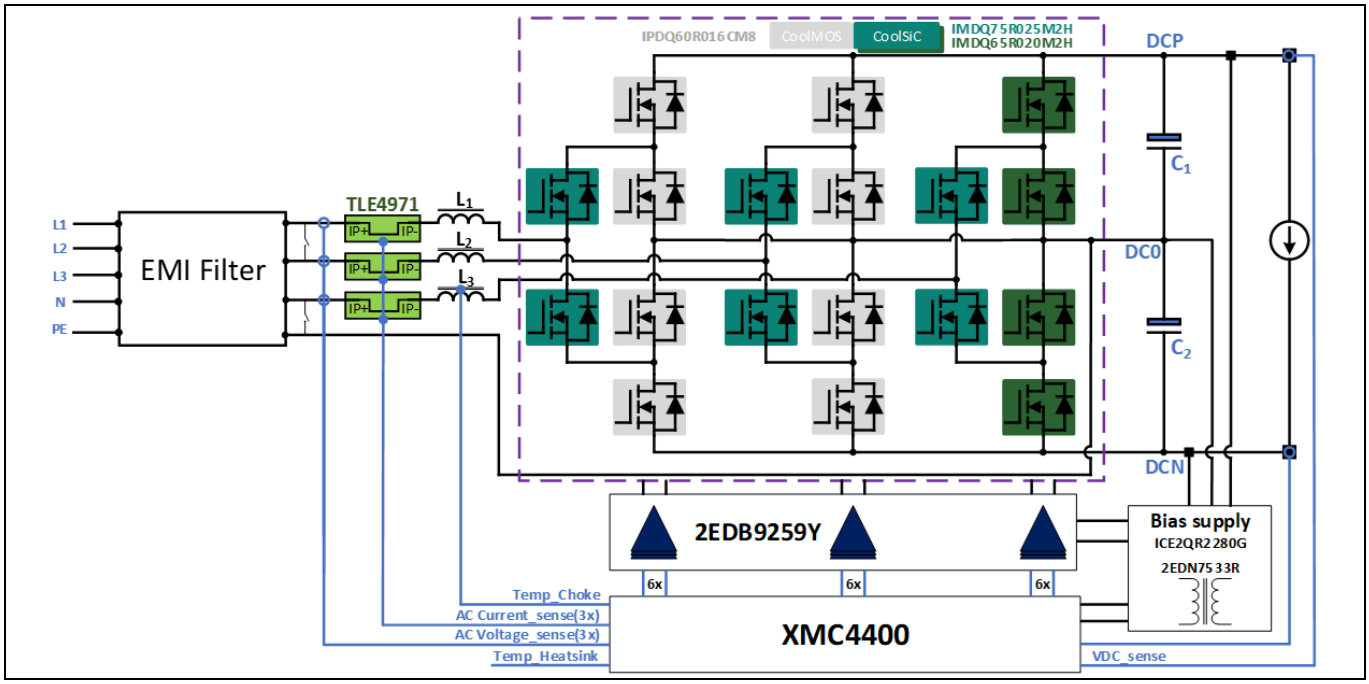


Figure 20 11 kW/800 V 3L-ANPC converter system block diagram

The functionalities implemented are soft-start, PFC, voltage regulation, overvoltage protection (OVP), undervoltage protection (UVP), overcurrent protection (OCP), and bidirectionality modes.

3.1 Auxiliary power supply

All auxiliary power supply channels are located on the daughter card labeled as “BS200001015”. Figure 21 demonstrates the overall architecture of auxiliary power supply. The loads on the auxiliary power supply include nine channels of 18 V supply for biasing all MOSFETs, one 12 V bus to power the relay coils, and one 3.3 V bus to power the MCU, current sensor, gate driver logic, operational amplifiers, and LED indicators. The schematic of the auxiliary power board is displayed in Section 7.2.2.

There are different conversion stages on the auxiliary power board. The main stage consists of two flyback converters with Infineon CoolSET™ integrated power management IC ICE2QR2280G. The two flyback converters are fed from the upper and lower DC bulk capacitors respectively, i.e., HV_DCP(+400 V)-HV_DC0(0V) and HV_DC0(0V)-HV_DCN(-400 V). As demonstrated in Figure 21, each flyback converter has three outputs and only the 13.2 V output is regulated due to its heavy loading. The rest of the two 18 V outputs are fed to bias the MOSFETs. It is to be noted from Figure 22 that the supply channels of 18V_5A/5B/5C and 18V_4A/4B/4C refer to the netlables HV_DC0(0V) and HV_DCN(-400 V) respectively, and provides driving voltage to the six MOSFETs T5A, T5B, T5C, T4A, T4B, and T4C. The rest outputs from the flyback converter feed the two gates of high-side MOSFETs T1A and T1B. Figure 23 depicts the schematic of a single primary flyback converter.

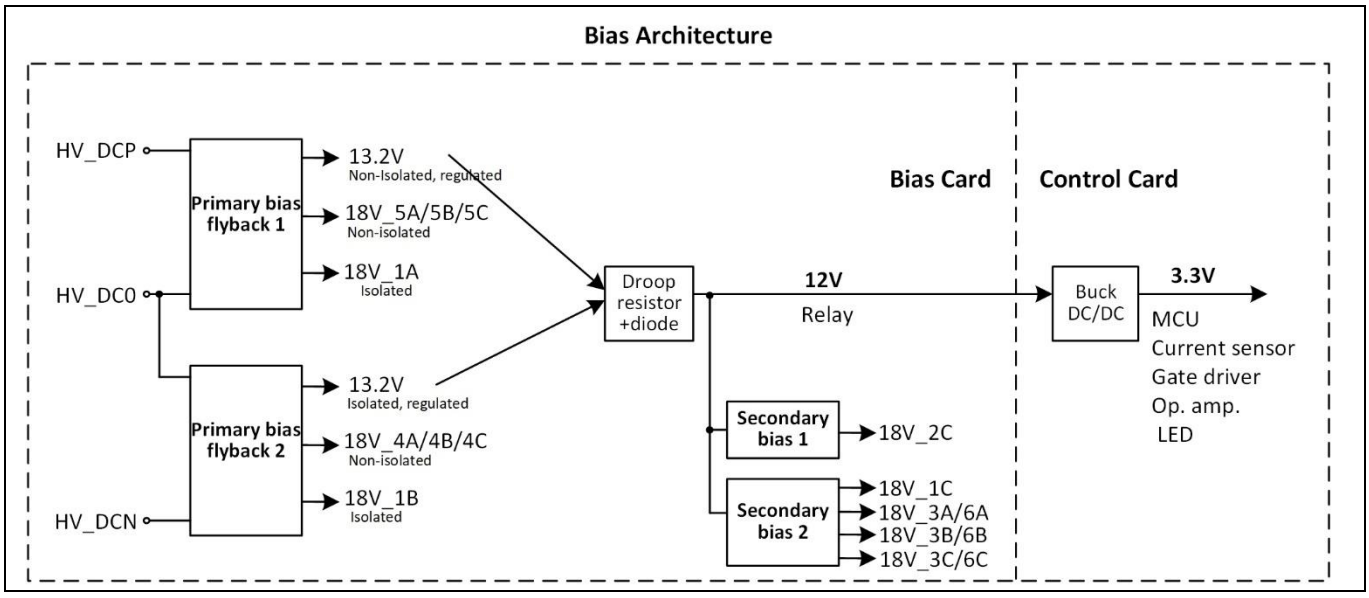


Figure 21 Overall auxiliary power supply architecture

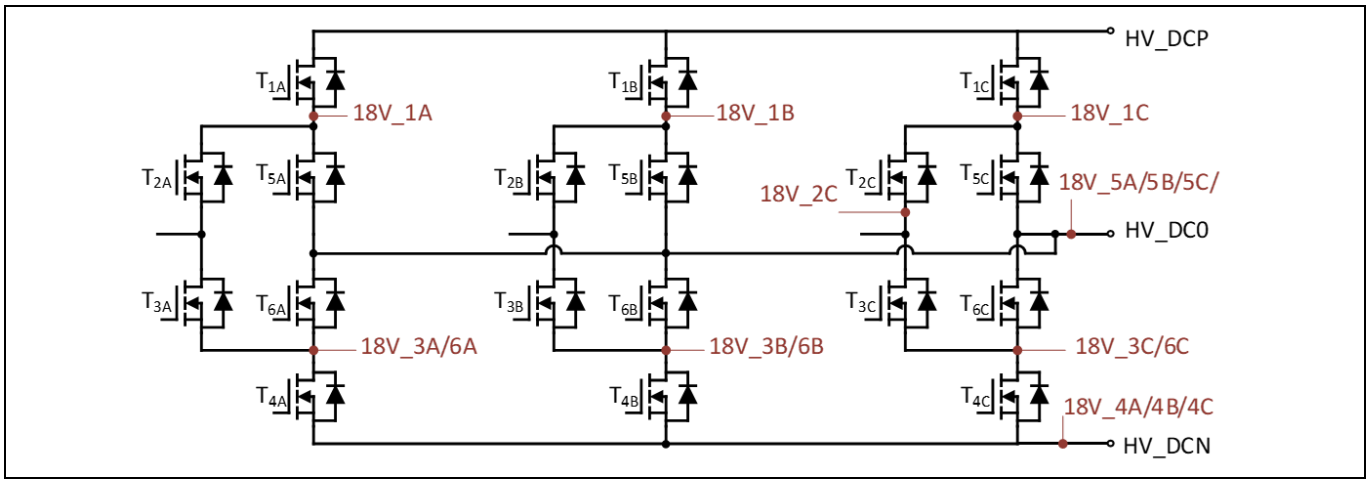


Figure 22 18 V supply scheme to bias all MOSFETs

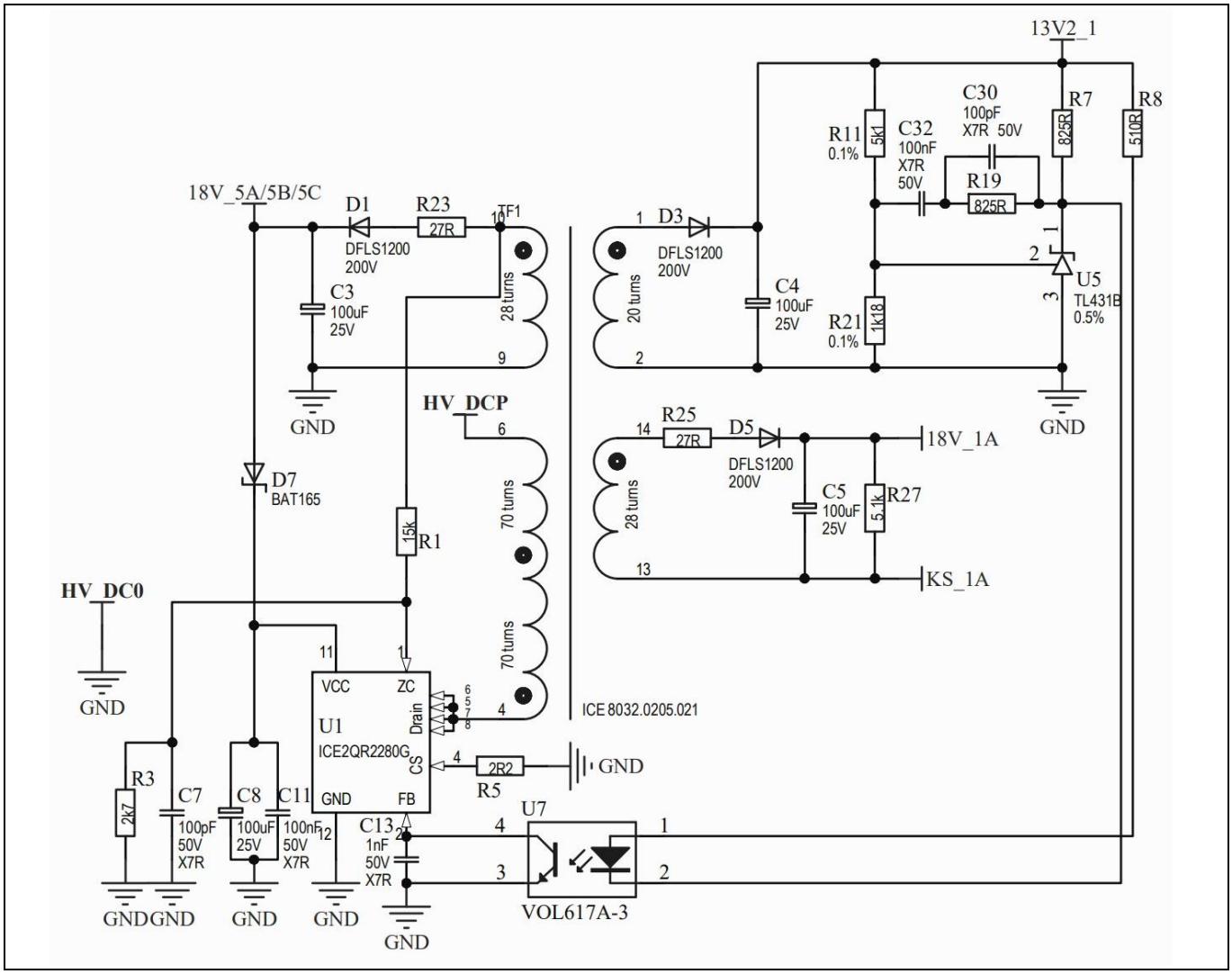


Figure 23 Single flyback converter schematic

The two 13.2 V outputs from flyback converters are then synthesized together via diode and droop resistor to form a 12 V bus. The purpose of implementing diodes and droop resistors is to equalize the output current and therefore, to support the balancing of two bulk voltages. The 12 V bus powers the relay coils and feeds the 3.3 V output switching regulator using Infineon's OPTIREG™ TLS4120D0EP V33 switching regulator. Additionally, the 12 V bus also feeds the secondary conversion stage.

The secondary conversion stage utilizes a novel ring oscillator concept with Infineon's EiceDRIVER™ 2EDN7533R, which generates the rest of the 18 V supply voltages. The planar cores are used to implement this secondary bias converter. The schematic of this secondary converter is diaplayed in Figure 24. For each phase, the MOSFETs T_3 and T_6 can share the same channel of 18 V supply due to that their source pins are tied together. The 18 V driver supply of T2A and T2B are obtained through bootstrapping circuit, which is further discussed in the following sections. Figure 25 (a) and (b) show the front- and back-side of the auxiliary power supply board, respectively. The layout of primary flyback converters and the secondary converters can be clearly identified.

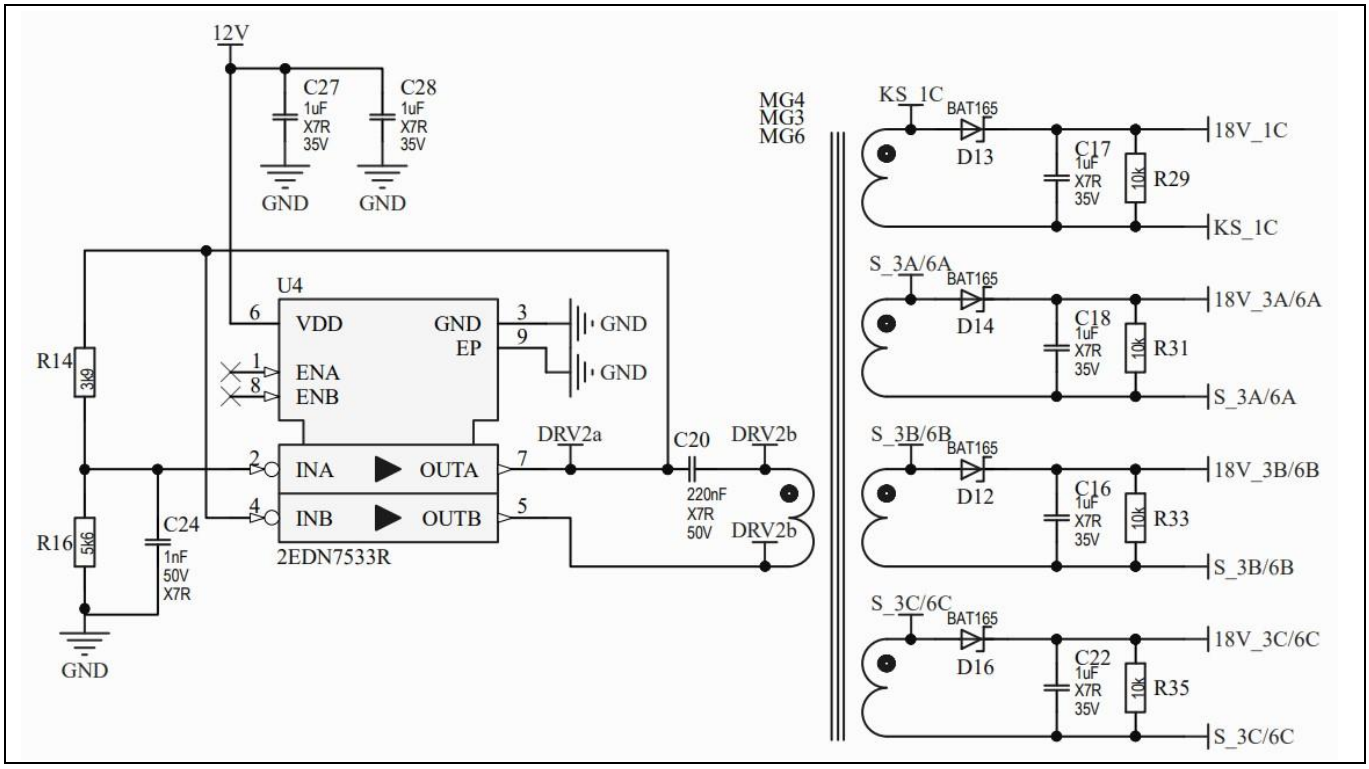
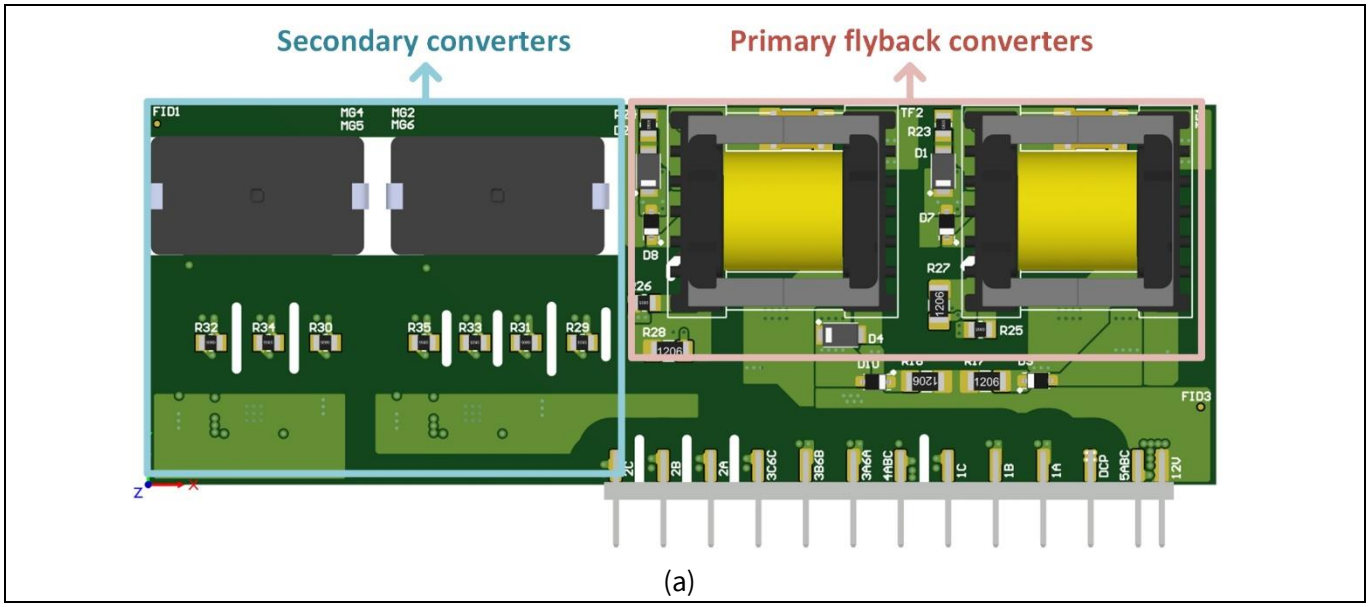


Figure 24 Secondary bias converter schematic



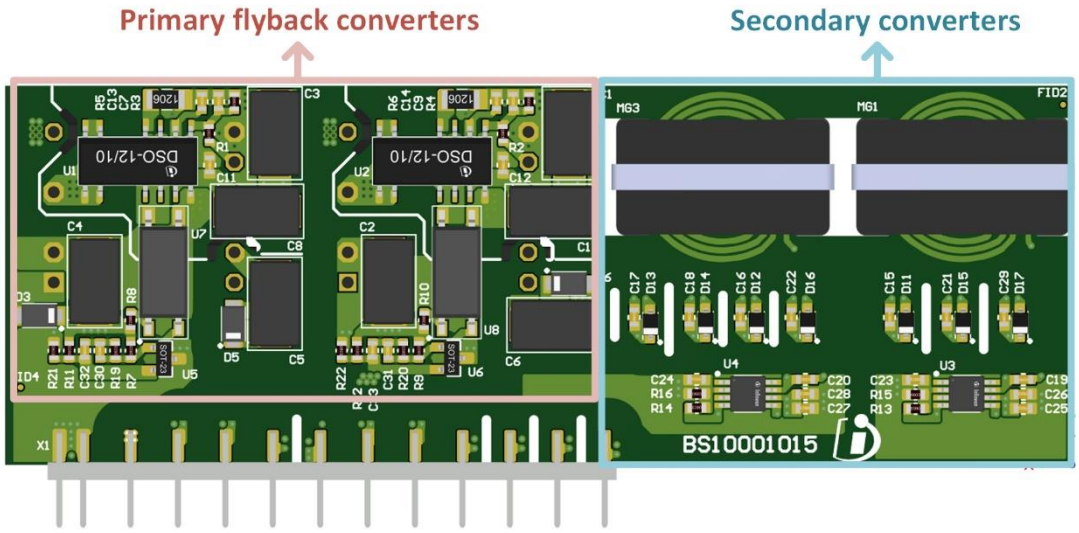


Figure 25 Pictures of the auxiliary power supply board captured from CAD design software. (a) Front side; (b) Back side

3.2 Capacitor bank voltage balancing circuit

As mentioned in Section 3.1, the two flyback converters are fed from the upper and lower DC bulk capacitor banks. Therefore, the voltage balancing of the upper and lower bulk capacitor banks can be challenging as the two flyback converters may draw unbalanced supply current from the bulk capacitors. The 3L-ANPC converter can actively balance the bulk capacitor voltages by digital control algorithm but this only functions when the ANPC phase-leg is under operation. During the startup and standby phases when the 3L-ANPC phase-legs do not operate, the voltage balancing of the upper and lower bulk capacitors cannot be guaranteed.

Therefore, in this system solution design, a circuit that does not rely on the microcontroller to balance the two bulk voltages is implemented. The schematic of the balancing circuit is displayed in Figure 26. This circuit is also known as active voltage balancer for balancing the mismatch of leakage currents in series connected electrolytic capacitors [9]. Robust high-voltage BJTs are used in cascode configuration to realize the higher gain of the circuit. The circuit also features current limiting function so that the voltage ripple (DC midpoint fluctuation) during single-phase operation would not cause additional power losses. Therefore, the designed circuit features a rejection to AC ripples and only compensates for DC voltage difference between the upper and lower bulk capacitor banks. This ensures the stable operation of the two flyback converters to supply the auxiliary power for the whole system.

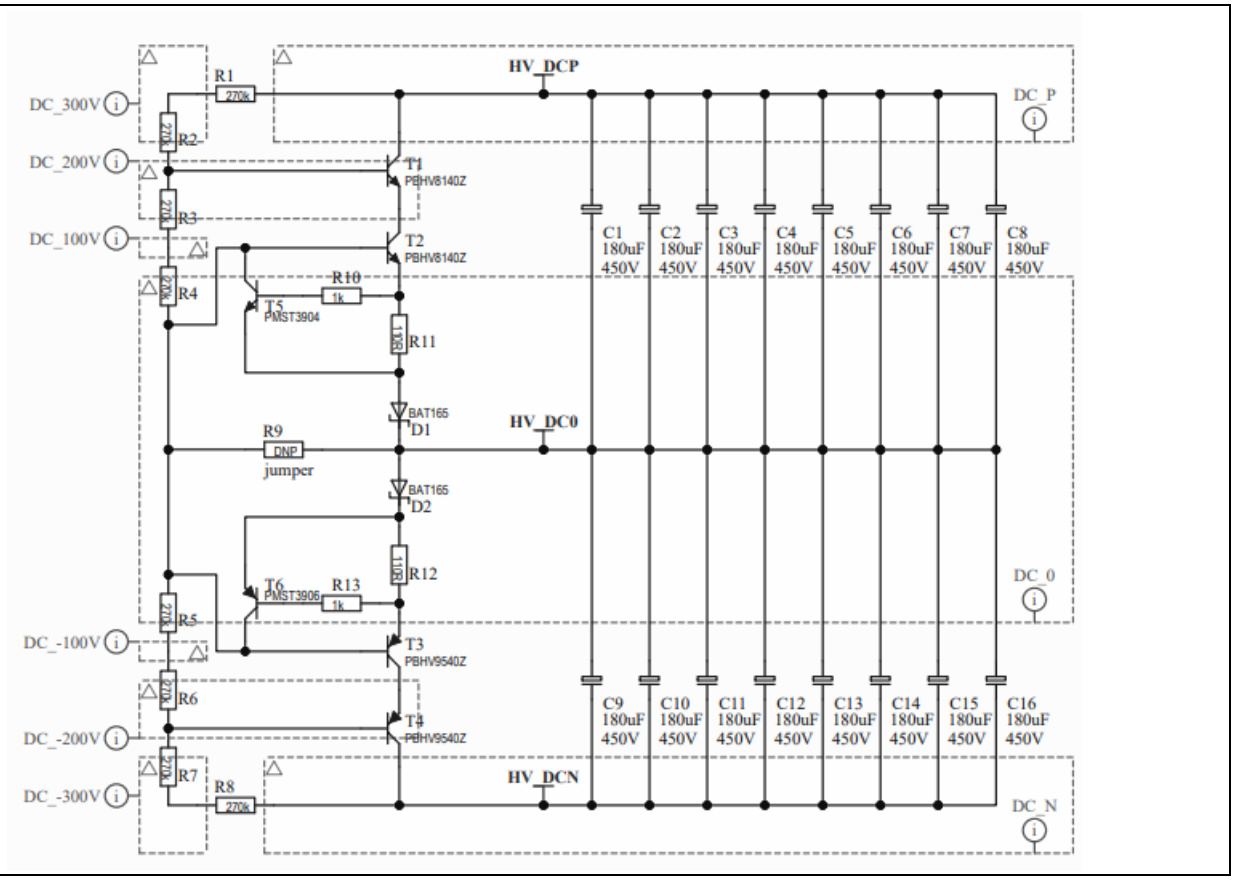


Figure 26 Bulk capacitor active voltage balancing circuit schematic

3.3 Driving configuration

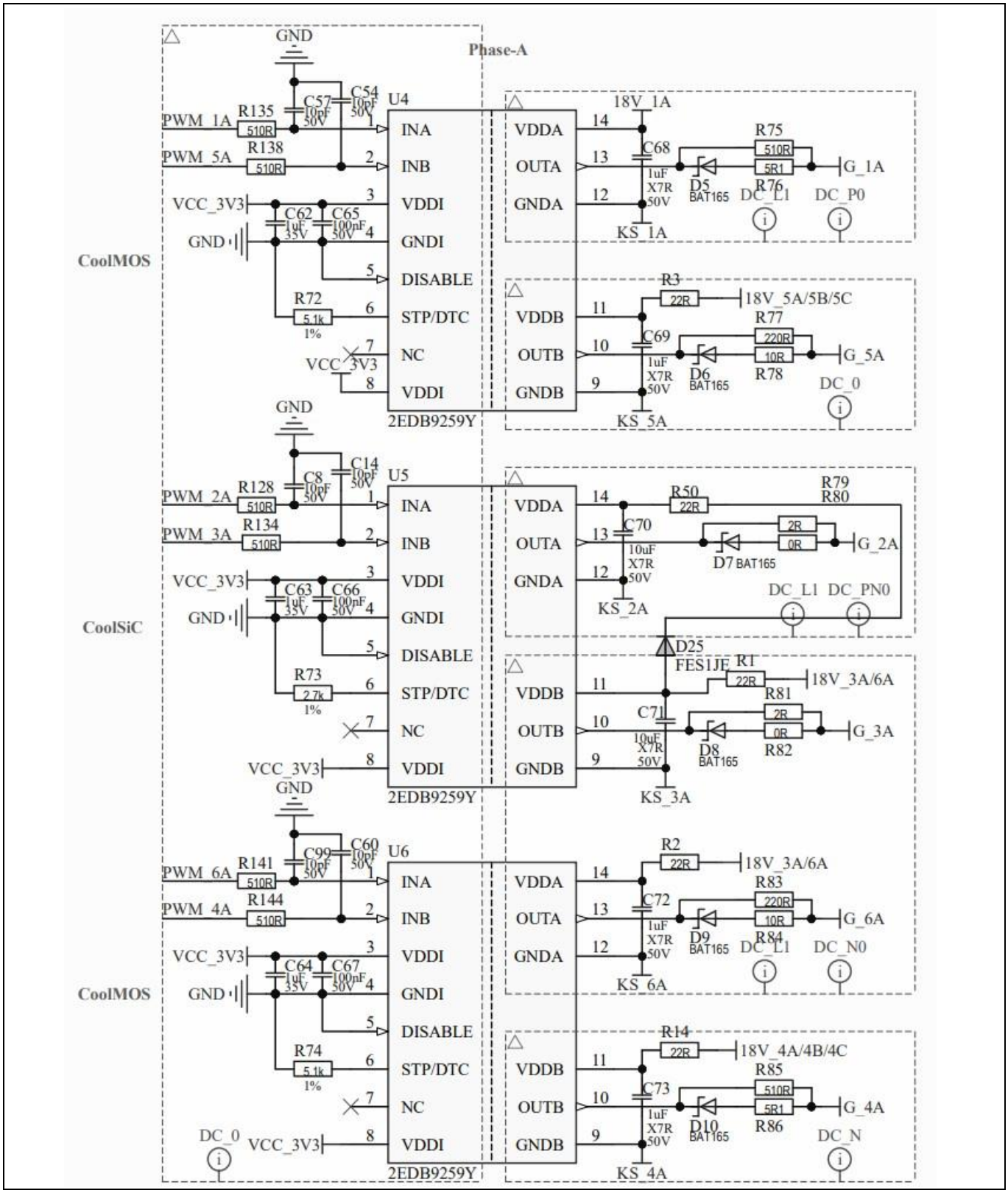


Figure 27 Gate driving scheme of one phase leg in 3L-ANPC

Figure 27 shows the gate driving stage of phase-A leg in ANPC converter topology. The dual-channel gate driver 2EDB9259Y is used to drive both CoolSiC™ and CoolMOS™ switches. As mentioned in Section 3.1, switches T1A,

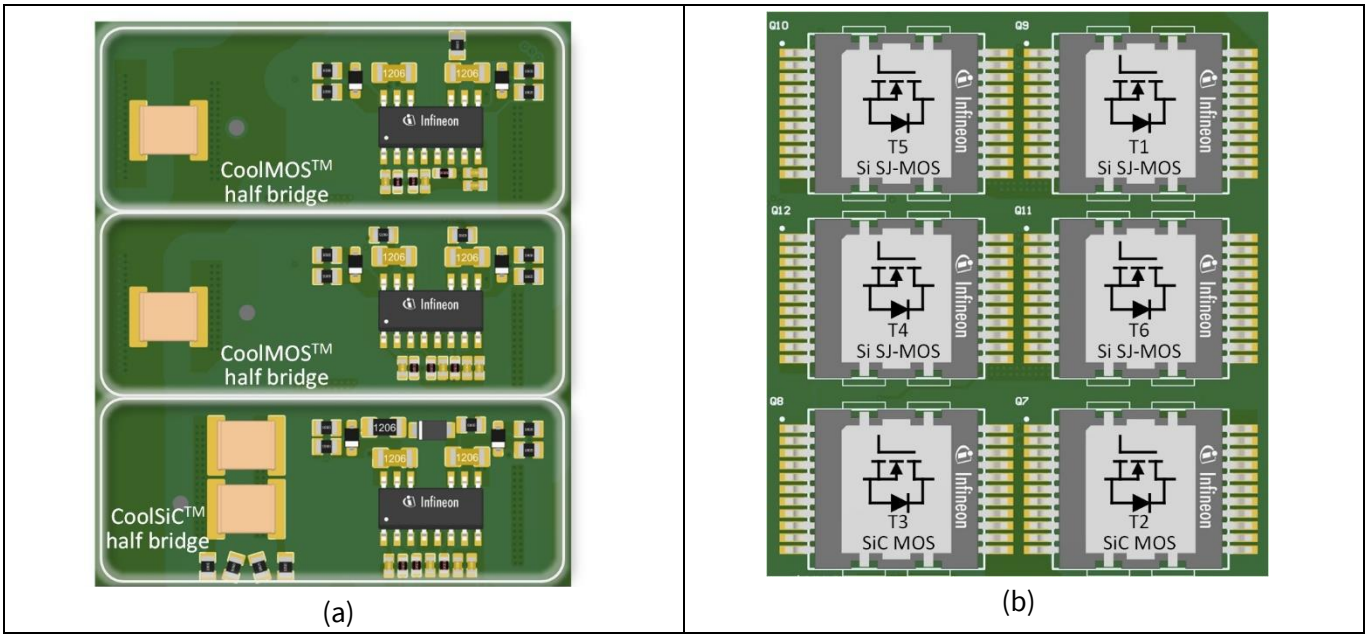
T3A, T4A, T5A, and T6A are biased by the auxliary power supply card, whereas the high-side switch T2A is biased by a bootstrap circuit (D25 and R50) from 18V_3A/6A. In this way, the switching performance of high-side switch T2A can be optimized.

With gate resistances of 2 Ω for turn-on and 0 Ω for turn off for switches T2A and T3A, high switching speeds are achieved during the commutation of those complementary SiC devices. A 2.7 kΩ pull-down resistor is connected to the STP/DTC pin of the gate driver 2EDB9259Y, which drives the fast-switching leg to configure the minium dead-time to be 27 ns. An actual dead-time of 50 ns is controlled by the XMC4400 microcontroller. Note that 22 Ω damping resistors (R1, R2, R3, and R14) are used in series with all 18 V supplies that are shared by multiple switches. Otherwise, oscillation on 18 V supply can be induced due to the Kelvin-source connection of supply voltage.

The schematic of phase-B driving stage replicates that of phase A. However, the phase-C driving-stage schematic is different than phase A/B because the high-side swtich T2C is supplied directly by the auxiliary power supply card, instead of bootstrapping. This is due to the requirement of synchronous operation of all phase legs during three-phase startup.

3.4 Switching-loop optimization

Minimizing the switching-loop inductance is crucial when designing the hard-switched bridge-leg. A single ANPC phase leg captured from the PCB CAD software is depicted in Figure 28, visualized from both the top side and bottom side of the PCB, in Figure 28 (a) and (b), respectively. To simplify and modularize the design, a single ANPC phase leg is split into three half bridges, i.e., two CoolMOS™ half-bridges and one CoolSiC™ half-bridge. All utilized MOSFETs are packed in Infineon's innovative top-side cooled package Q-DPAK. As shown in Figure 28 (b), the MOSFETs are mounted on the bottom side of the power PCB, with heatslugs facing downwards to the heatsink.

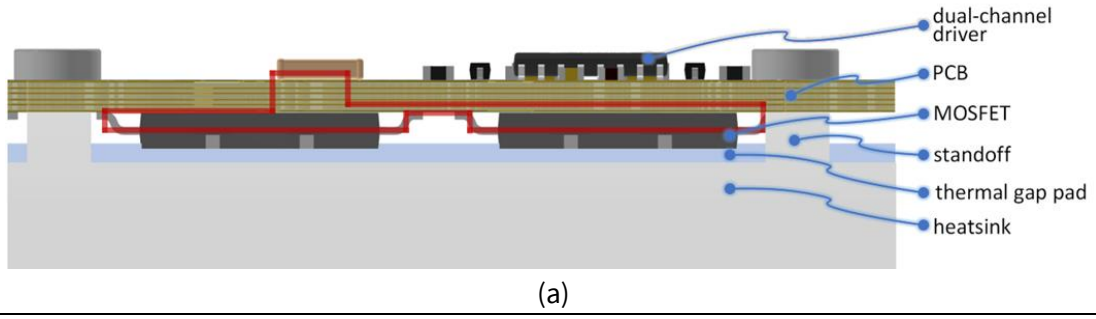


(a) (b)

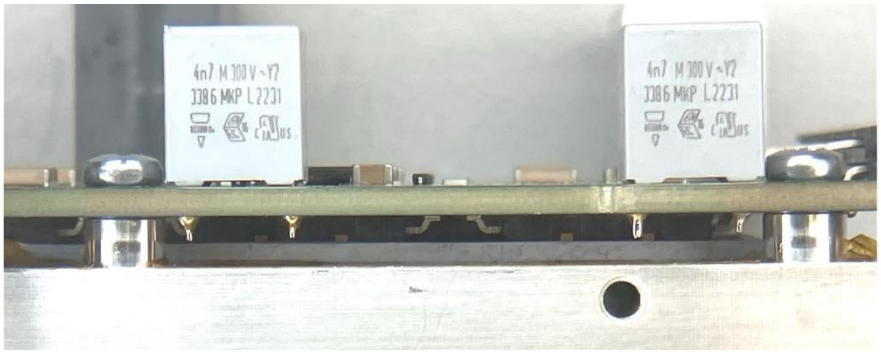
Figure 28 Phase-leg layout visualization; (a) top-side of PCB; (b) bottom-side of PCB

The top-side cooled package allows all peripheral devices, e.g., gate drive circuit, bootstrap circuit, and decoupling capacitors can be placed on top-side of the PCB, right on top of the MOSFETs. The Q-DPAK therefore, enables compact design and minimum switching area loop inductance. The switching loop in the cross-sectional view is demonstrated in Figure 29 (a), as it is highlighted in red solid line. The power loop layout is done on the bottom and second bottom layers to minimize the loop. The decoupling capacitor is connected

to the power loop by placing veritical via arrays. The total loop inductance is estimated to be ~7 nH [10] with the top-side cooled Q-DPAK and the optimized switching loop PCB design.



(a)



(b)

Figure 29 Cross-sectional view of the switching cell. (a) Captured in the PCB CAD software; (b) Real hardware in photo

3.5 Thermal design

When designing the thermal management solutions for Infineon's Q-DPAK packages, there are a variety of thermal interface materials (TIMs), including gap pads, liquid gap fillers, and phase-change materials [11]. Commercially available gap pads are typically composed of pre-cured silicone combined with ceramic powder. These materials are offered in various softness grades, such as soft and ultra-soft, and provide a thermal conductivity range typically between 2 and 10 W/(m·K) or higher. For applications with higher thermal demands, choosing a high thermal conductivity gap pad can significantly improve heat dissipation from the package.

However, thermal conductivity is not the only parameter to consider. Other important characteristics include thickness, material compressibility, and insulation level. Selecting the optimal TIM requires to balance these factors based on the application needs and design constraints.

3.5.1 Standoff height

Gap pads typically offer good high-temperature performance, but to maintain consistent thermal performance over time, they require a permanent and reliable contact force. As shown in Figure 29 (a) and (b), and 30, mechanical standoffs with defined heights are used to maintain the spacing between the PCB and heatsink, denoted as $d_{standoff}$. The final compressed thickness of the gap pad $d_{gp,contact}$ can be calculated using the following relationship:

$$d_{gp,contact} = d_{standoff} - (d_{qdpak} \pm 0.1\ mm) \quad (1)$$

where, d_{qdpak} represents the typical package thickness of the Q-DPAK (2.3 mm nominal, with a ± 0.05 mm tolerance). To ensure continuous mechanical contact between the package and gap pad, the compressed thickness must always be less than the original thickness of the gap pad:

$$d_{gp,contact} < d_{gp,origin} \quad (2)$$

$$d_{standoff} < d_{gp,origin} + (d_{qdpak} - 0.05\ mm) \quad (3)$$

For example, if the thermal gap pad has an original thickness of 1.0 mm, the standoff height should be calculated less than 3.25 mm. Considering a gap-pad compression distantce to be 0.15 mm for instance, then the final standoff height should be designed as $d_{standoff}$ = 3.1 mm. Then, the thermal resistance of the gap pad can be estimated as:

$$R_{th,gp} = d_{gp,contact} / (A_{gp} \cdot \lambda_{gp}) \quad (4)$$

$$= (d_{standoff} - (d_{qdpak} \pm 0.05mm)) / (A_{gp} \cdot \lambda_{gp}) \quad (5)$$

where, A_{gp} and λ_{gp} are the effective heat transfer area and thermal conductivity of the applied gap pad, respectively.

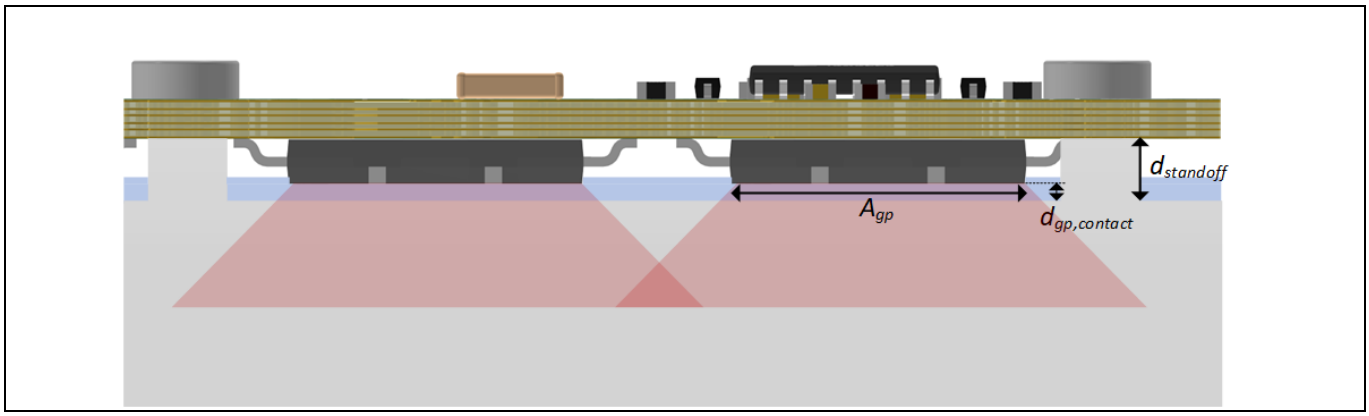


Figure 30 Cross-sectional view of the switching cell

Generally, reducing the standoff height (i.e., increasing compression distance of the gap pad) can effectively lower the thermal resistance between the package and heatsink. However, this increases mechanical stress on the PCB due to higher compression ratio of gap pad. Excessive stress can lead to PCB warpage, which in turn may cause severe issues like solder joint cracking or failure of surface-mounted components, especially multi-layer ceramic capacitors.

3.5.2 Avoiding PCB warpage

To prevent PCB warpage in the applications using top-side cooled Q-DPAK packages, three key strategies can be implemented.

The first method is to increase the thickness and to optimize the stackup of the PCB. The main board thickness of PCB used in REF_11KW_PFC_SIC_QD is ~2.5 mm. In the PCB stackup, the core layers are made of fiberglass-epoxy laminate, and they therefore provide the main structural support and substrate for the PCB. The prepreg layers, on the other hand, act mainly as adhesive and bonding layers during the lamination process. Putting more core layer in the PCB buildup helps to improve the rigidity of the PCB and prevent the PCB from warpage.

The second method is to increase the mechanical support provided to the PCB by the metallic chassis or cooling plate. This is achieved by placing additional height-defining standoffs or spacers near the Q-DPAK device, as shown in Figure 30. These standoffs help to distribute mechanical load more evenly and reduce localized stress caused by gap pad compression.

The third method involves selecting a gap pad with higher compressibility, which reduces the mechanical stress transmitted to the PCB. Figure 31 illustrates the compressibility characteristics of three different gap pad materials, expressed as thickness versus applied pressure — a common metric provided by gap pad manufacturers. Among the materials compared, Gap Pad 3 demonstrates the highest compressibility, showing the greatest reduction in thickness under the same applied pressure. This feature makes it more effective in accommodating mechanical tolerances and minimizing stress-induced deformation of the PCB.

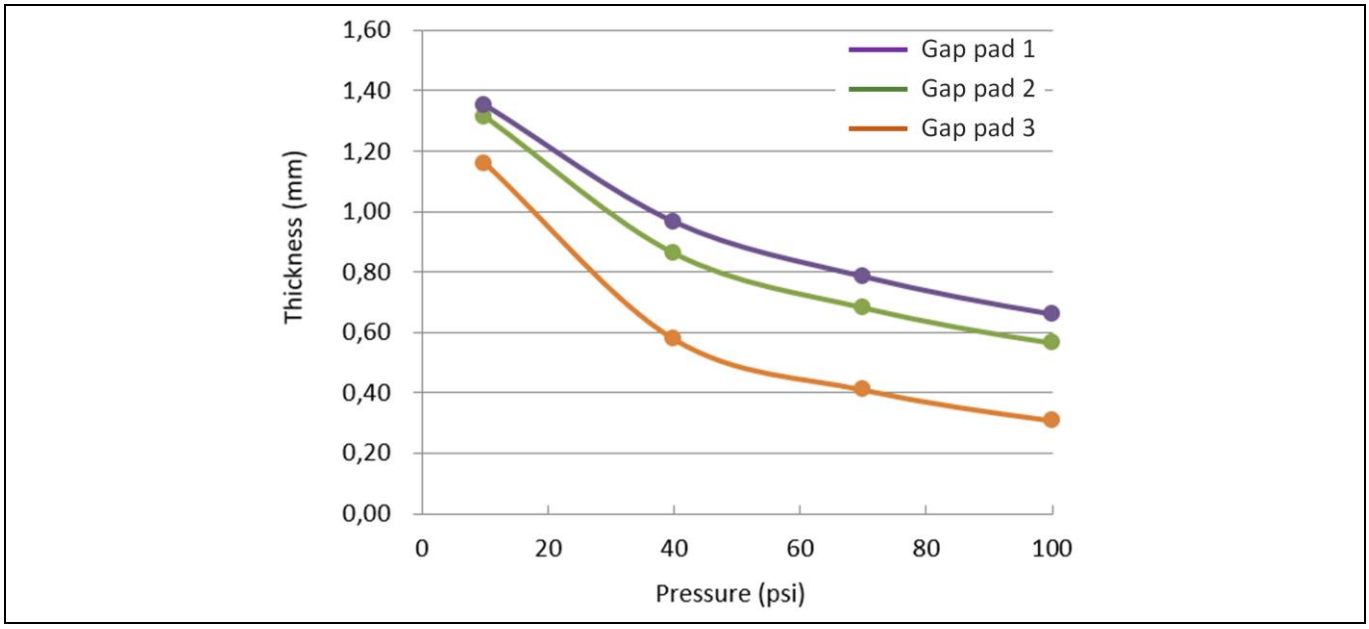


Figure 31 Thermal pad material's compressibility vs. thickness vs. pressure curve

3.5.3 Insulation requirement

In addition to thermal conduction, a secondary but equally critical function of gap pads is to provide electrical isolation between the package and the cooling structure (e.g., heatsink or metallic baseplate). This is especially important in applications where the cooling component is electrically connected to protective earth.

Depending on system-level requirements, many power converter designs must withstand high-voltage insulation levels, typically in the range of several kilovolts between active circuitry and protective earth. According to manufacturer specifications, typical dielectric breakdown strengths of commercial gap pad materials range from 5 kV/mm to 10 kV/mm.

Therefore, depending on the system insulation requirement and the selected gap pad's dielectric breakdown voltage, a minimum thickness of gap-pad layer (after pressure application) should be defined. In some cases, an additional insulation layer, such as adhesive Kapton layer, can be applied to the heatsink or chassis to reinforce electrical isolation (commonly referred to as double insulation).

Considering all these aforementioned design factors such as mechanical tolerances, PCB warpage, and insulation requirements, the typical post-compression thickness of the gap pad in practical applications generally falls within the range of 0.5 mm to 1.5 mm. With REF_11KW_PFC_SIC_QD, the standoff height of 3.1 mm is defined and the 1 mm ultra-soft gap pad FSL-BS from Denka Company Limited is used. The selected gap pad features a thermal conductivity of 3 W/m·K and a premium compressibility of 30 % at 0.1 MPa pressure. The dielectric breakdown voltage of the selected material is reported to be 10 kV/mm. Considering the full-range height tolerance of Q-DPAK, the post-compression thickness of 1 mm gap pad is in the range between 0.6 mm and 0.8 mm.

3.6 Inductor and current sense against stray field

In REF_11KW_PFC_SIC_QD, each inductor is made with one pair of HTEQ3626A high flux core from Chang Sung Corporation. Helical winding with flat wire with the dimension of 7 mm (width) × 0.4 mm (thickness), with totally 50 turns wounded, is implemented due to its better window utilization ratio. The achieved initial inductance is tested to be 330 µH, and the rated current is designed to be 16 A_{RMS}. A 3D picture of the inductor captured in CAD software is shown in Figure 32 (a).

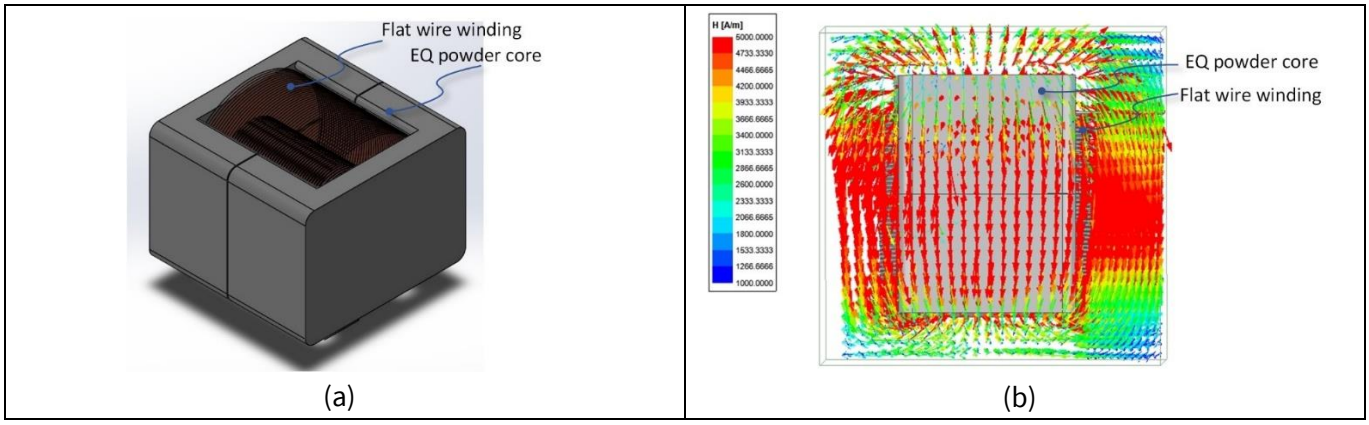


Figure 32 (a) 3D picture of the inductor captured in CAD software. (b) Simulated stray field strength in the vicinity of the inductor

The EQ-core based inductor solution helps to increase the overall power density as it occupies the least volume compared to other magnetic core shapes, e.g., toroidal etc. However, inevitable stray field can be found in the vicinity of the inductor, because the powder core material features relatively low permeability and the EQ shape increases the chance for the field to leak. Figure 32 (b) depicts the FEM simulation result of stray field surrounding the inductor. This stray field can cause interference to its neighboring components which work on magnetic priniciple, especially the Hall- and magnetoresistive-based current sensors. In theory, all Hall- and magnetoresistive-based current sensors without built-in shielding layer suffer from measurement error due to the stray field. The magnetic interference level increases sharply with higher current flowing through the inductor, and therefore, the current THD value sees significant increase with the increase of output power during the operation.

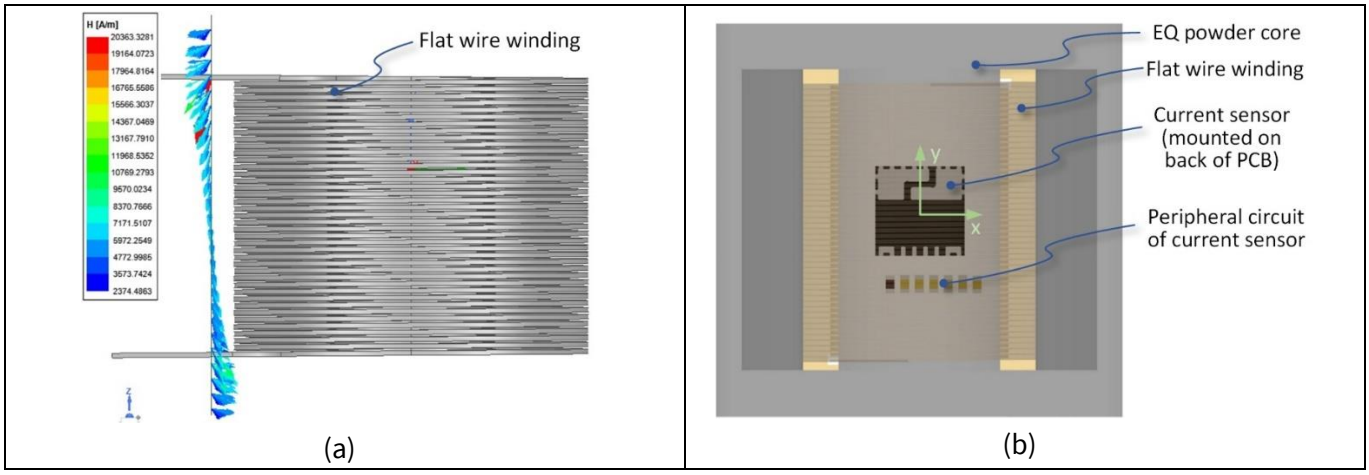


Figure 33 (a) Simulated stray field strength in the plane beneath the inductor, i.e., the PCB plane. The core is hidden for simplicity; (b) The concluded optimal position and orientation for TLE/TLI 4971 current sensor with least stray field interference, visualized from the top-side of inductor

Several methods can be applied to mitigate the stray field interference effect. First, the current sensor can be placed away from the inductor, where the stray field density is much less. This method requires more layout area on the PCB and may enlarge the switching-node area significantly if the current sensor is electrically connected between the bridge-leg and inductor. Therefore, this method may not be applicable to all designs.

The second method involves applying external field-shielding component to the current sensor. Doing so, the stray field can be bypassed before it reaches the current sensor. A slight cost would be added due to extra shielding components and the excessive effort for the assembly process.

Finally, since the current sensor typically shows immunity to a certain magnetic field direction, it can be placed in the vincinity of inductor but in a specific location and orientation that the stray field does not affect the sensor output behavior. This method does not require additional components and can be used in designs where the PCB layout needs to be compact. On the other hand, this method requires deep know-how on stray field distribution as well as current sensor behavior.

Therefore, the stray field orientation at the PCB plane (where the current sensor is assembled) is studied, which is shown in Figure 33 (a). It is known that the sensing element is sensitive to stray field in perpendicular to its sensing element. The current sensor should be placed in alignment with the center of the inductor as the perpendicular field at the center of inductor geometry is nearly zero according to Figure 33 (a). During testing, it is noticed that the orientation of current sensor also affects the stray field sensitivity. Finally, the optimal position and orientation of current sensor is concluded in Figure 33 (b), which is visualized from top-side of the inductor, and nearly no stray-field interference can be observed during testing. Rotating the current sensor by 180° still sees the optimum performance, while rotating by 90° sees more sensitive to stray field. The REF_11KW_PFC_SIC_QD finally adopts the optimal layout shown in Figure 33 (b), and the performance is verified through tested current THD is mentioned in Sections 5.3 and 5.4.

Note: *The recommended optimal orientation only applies to the tested current sensor TLE/TLI 4971 from Infineon because of the package difference and how the sensing element is mounted in the package. Extra validation needs to be conducted if another model of current sensor is used.*

In conclusion, this section provides a guideline regarding layouting and placement of Infineon's current sensor TLE/TLI 4971 with EQ-core based power inductor to achieve the lowest level of stray field interference. The concluded optimum layout to achieve the compact PCB layout is demonstrated in Figure 33 (b).

3.7 Common-mode choke with differential-mode inductance

A novel common-mode choke is used in REF_11KW_PFC_SIC_QD to further improve the power density of the design. The differential-mode inductances are integrated into the common-mode choke, and this allows the REF_11KW_PFC_SIC_QD to be implemented without dedicated differential-mode inductors.

The integration of differential-mode inductance is realized by inserting ferromagnetic material (magnetic shunt) between the adjacent windings in the common-mode choke buildup. This ferromagnetic material provides extra magnetic permeability to the leakage path and therefore, helps to increase the differential-mode inductance. Figure 34 (a) demonstrates the common-mode choke structure utilized in REF_11KW_PFC_SIC_QD. Two high-permeability ferrite cores (R10K material from DMEGC) are used, each of which is in the shape of PQ35-43A. Four sets of helical flat wires (each in the size of 6 x 0.6 mm, 8 turns) are assembled in the window area. Then, three sets of magnetic shunts with insulation are mounted in between the windings.

The geometry of the magnetic shunt is depicted in Figure 34 (b), which can be easily fitted into the core structure. The magnetic shunt is made from NO 30-16 electric steel sheet thickness of 0.3 mm. The utilized material can significantly increase the leakage path magnetic permeability and does not affect the system

efficiency through out the measurement. Multiple pieces of magnetic shunts can be stacked to increase the final differential-mode inductance. Figure 35 shows one of the finished common-mode choke prototypes. For more information on the common-mode choke design, refer to [12].

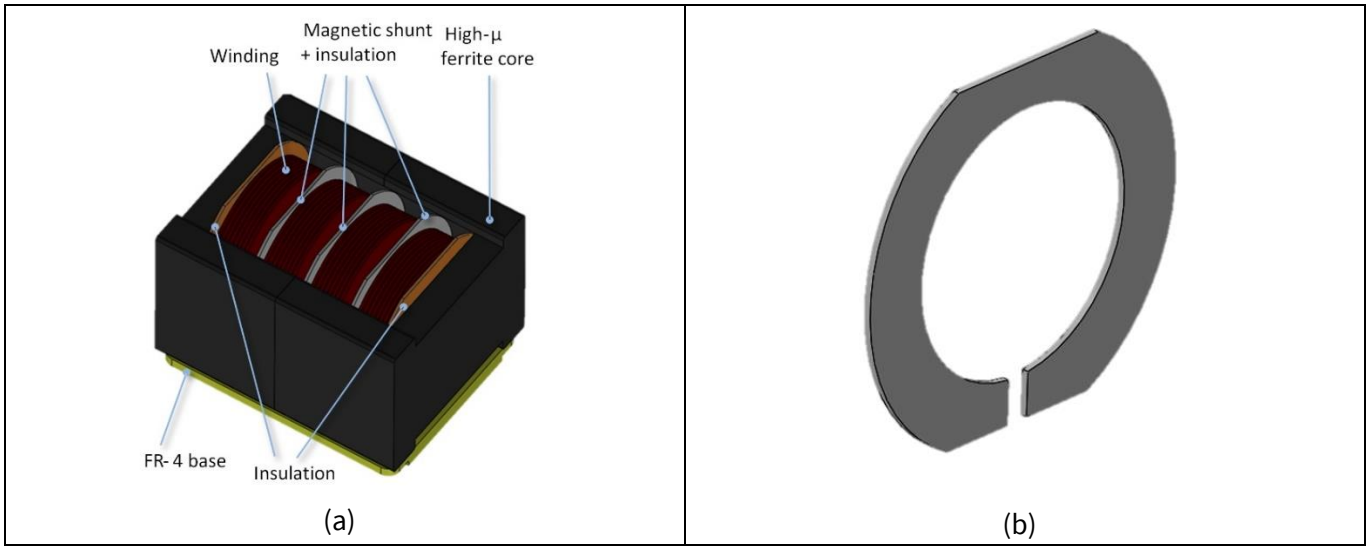


Figure 34 Common-mode choke buldup used in REF_11KW_PFC_SIC_QD. (a) The whole common-mode choke captured in 3D CAD design software; (b) Magnetic shunt in ring shape used in the common-mode choke buildup

Figure 35 Finished common-mode choke prototype

4 System software design

4.1 Three-phase control diagram

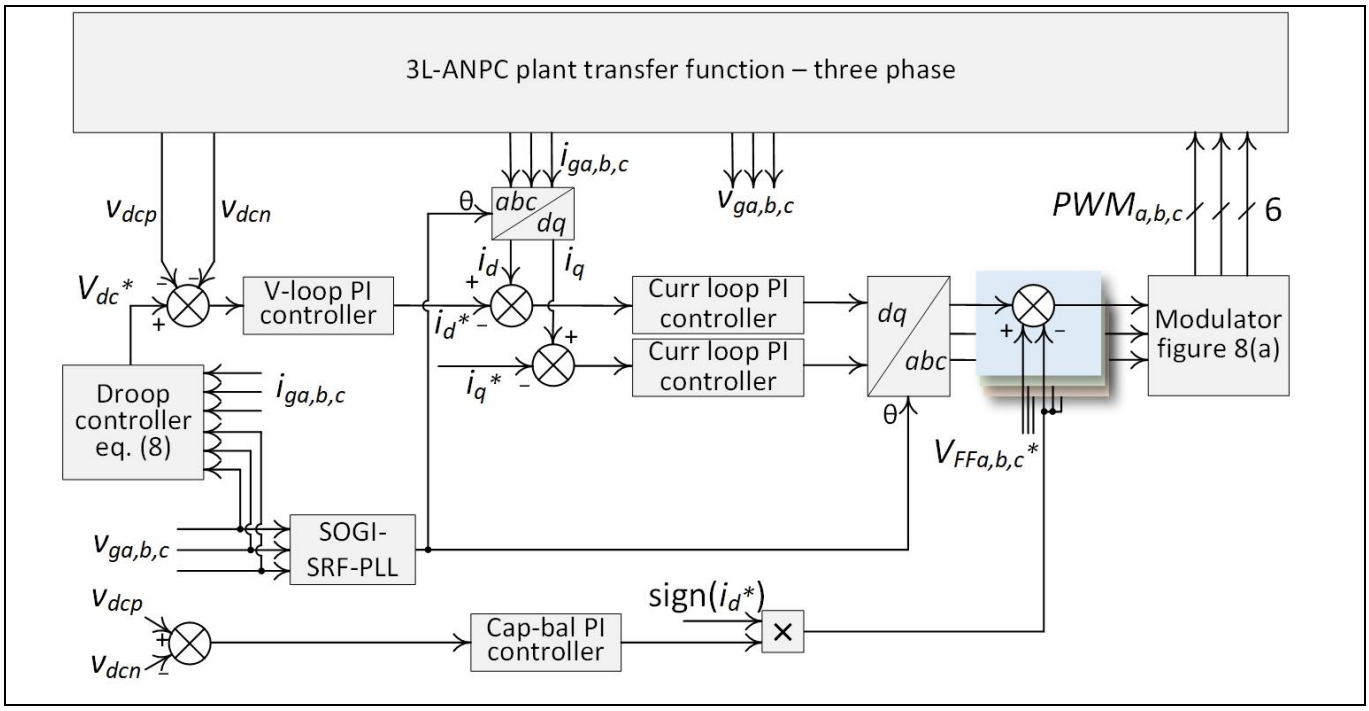


Figure 36 Three-phase control diagram

The three-phase control diagram is demonstrated in Figure 36. The two DC capacitor voltages V_{dcp} and V_{dcn} are sampled and compared with the DC volage reference V_{dc}*. The DC voltage reference V_{dc}* is given by the droop controller, which is displayed in Section 4.3. The outer voltage loop PI controller is implementd in C code to regulate the overall DC-link voltage $V_{dcp} + V_{dcn}$, which generates the d-axis current reference i_d*. Since the dc-link voltage is controlled, the converter is able to work under both PFC and inverter modes. The well-established dq current control method is utilized with two PI controllers to regulate the d- and q-axis currents [13].

The q-axis current reference i_q* is set to zero in this controller implementation. The two modulation voltages in dq axis are then transformed back to abc axis with the angle information from the three-phase second-order generalized integrator phase-locked loop (SOGI-PLL). The grid voltage feed-forward $V_{FFa,b,c}$* is used to improve the dynamic behavior of current regulation. In addition, a capacitor-voltage-balance loop is implemted to control the voltage difference of the upper and lower DC bulk voltages.

4.2 Single-phase control diagram

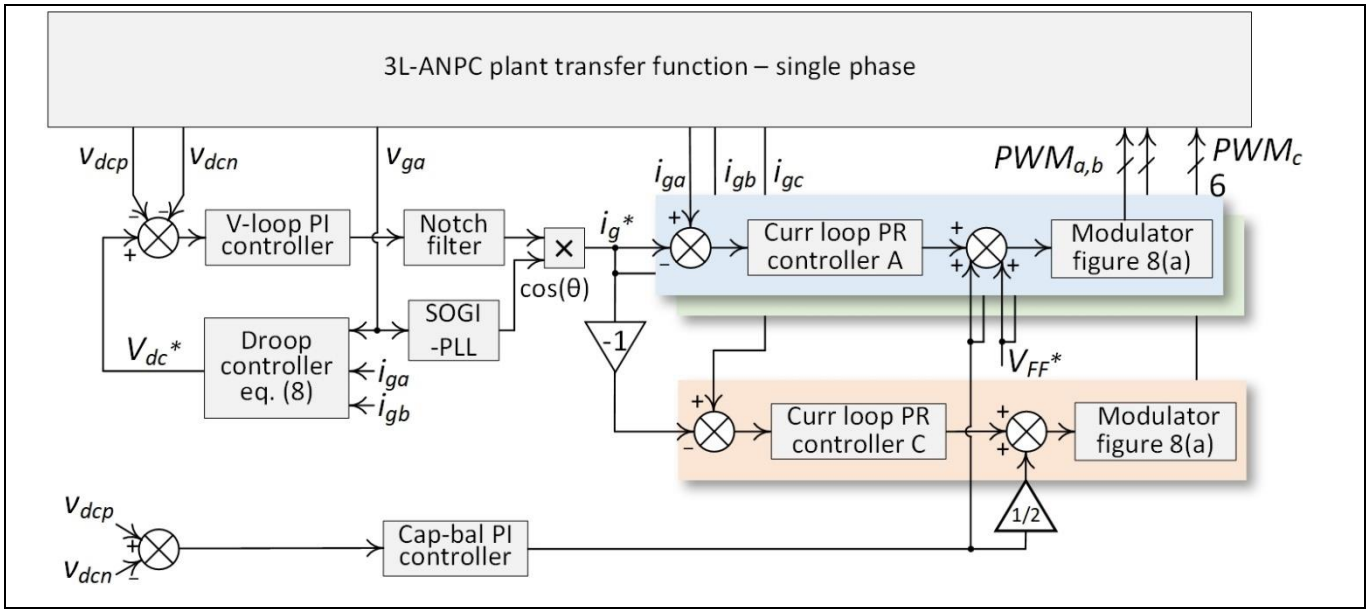


Figure 37 Single-phase control diagram

The single-phase control diagram is demonstrated in Figure 37. The DC voltage reference V_{dc}* is given by the droop controller, which is illustrated in Section 4.3. Same as the three-phase control, the overall DC-link voltage is regulated by the voltage-loop PI controller, allowing the power to flow in both directions. The notch filter is implemented in cascade to the PI controller to eliminate the double line-frequency contents appearing normally on the single-phase current reference. During operation, phase currents A and B are sampled and controlled in an interleaved manner to lower the differential mode (DM) noise. Two proportional resonant (PR) controllers are used to regulate the two single-phase currents [14]. In the end, the grid voltage feed-forward and capacitor voltage balancing contents are added to the two current regulation outputs.

Both the three-phase and single-phase control methods are implemented using Infineon's 32-bit XMC440 microcontroller in C code. And all calculations are based on fixed-point arithmetic. The 12-bit ADCs of XMC4400 are deployed to convert the three inductor currents, three grid-side voltages, two DC bulk voltages, and two temperature sense signals into digital values. All the ADC inputs are configured as single-ended mode. The three inductor currents and three grid-side voltages are configured to be sampled in a synchronous way to ensure the balanced control among three phases.

Note: The control software can self-identify whether to operate under three-phase or single-phase mode by evaluating the input voltages before start-up. The user does not need to re-configure or re-flash the software.

For both single- and three-phase control, the SOGI-PLL and current loop are executed in the frequency of 65 kHz, being the same as the switching frequency of SiC MOSFETs. The voltage loops, including the overall DC-link voltage control, the notch filter, and the DC capacitor voltage balancing control are implemented in the frequency of 6.5 kHz.

4.3 DC droop feature

To enable the bidirectional power flow and a smooth control of power flow direction, as well as power amplitude, a droop feature is implemented to the DC side voltage control. The circuit diagram of droop feature is demonstrated in Figure 38, where V_{SET} and V_{DC} denote the DC voltage reference (800 V nominal) and actual

bidirectional DC source, respectively. At the DC output/input port of REF_11KW_PFC_SIC_QD, the existing 800 V bulk capacitance presents a nominal value of 720 µF. During the bidirectional testing, directly connecting the DC terminals to the bidirectional DC source without the R_{DROOP} is not a preferred option. The capacitive current, which flows between the bulk capacitor and DC source cannot be controlled, because the amount of power is unregulated. The system will run either in steady-state PFC mode (if $V_{DC} < V_{SET}$) or steady-state inverter mode (if $V_{DC} > V_{SET}$). In the case that V_{DC} is close to V_{SET}, power flow can oscillate between the PFC mode and inverter mode.

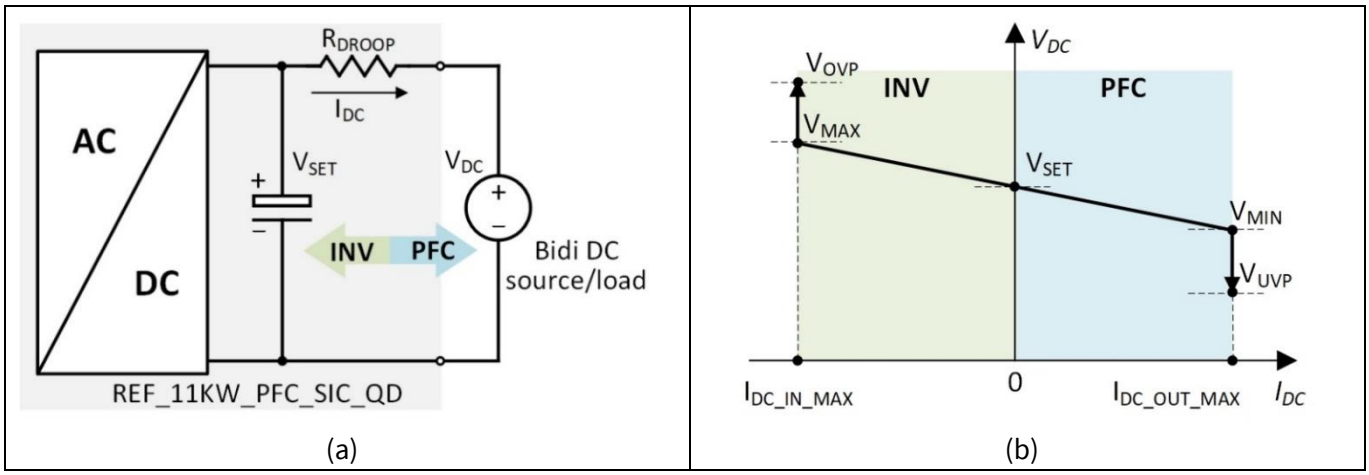


Figure 38 Droop control method. (a) Circuit diagram illustrating the droop feature at DC terminal. The resistor R_{DROOP} is a virtual resistor realized by control software; (b) Output V-I curve demonstrating the implemented droop feature

With the R_{DROOP} inserted between the bulk capacitor and DC source, the DC terminal current I_{DC} is limited by the Ohm's law:

$$I_{DC} = (V_{SET} - V_{DC}) / R_{DROOP} \quad (6)$$

With the R_{DROOP} populated, the V-I characteristic will behave as demonstrated in Figure 38 (b). By adjusing the bidirectional DC source output voltage, not only can the power flow direction be smoothly controlled, but also the power level can be precisely regulated. The R_{DROOP} value can be determined by the maximum voltage swing as well as the DC input/output current range:

$$R_{DROOP} = (V_{MAX} - V_{MIN}) / (I_{DC\_OUT\_MAX} - I_{DC\_IN\_MAX}) \quad (7)$$

Taking the three-phase operation mode for instance, the V_{MAX} and V_{MIN} are designed to be 811 V and 789 V, respectively with the center point to be V_{SET} = 800 V. The DC input/output current range are designed to be ± 13.75 A considering the power limit of ± 11 kW. Hence, the actual value of R_{DROOP} is calculated to be 0.8 Ω.

The simple way of implementing R_{DROOP} is to use a physical power resistor, but this causes additional power losses. In REF_11KW_PFC_SIC_QD, the droop resistor is realized virtually with the digital control. The XMC™ microcontroller monitors the actual input/output power from AC side P_{AC} and adjust the DC bulk voltage reference automatically following:

$$V_{dc}^* = V_{SET} - R_{DROOP}^* I_{DC} = V_{SET} - R_{DROOP}^* (P_{AC}/V_{SET}) \quad (8)$$

The detailed control diagram including the mentioned droop control are displayed in Figure 35 and Figure 36.

5 Experimental results

5.1 Setup description

This subsection introduces the experimental setup. It is recommended that all conducted testing follows the test setup introduced in this subsection. Figure 39 shows the test setup for PFC and inverter mode operations with three-phase AC feeding.

The bidirectional AC source phase terminals (A, B, C) are connected to AC terminals (L1, L2, and L3) labelled on REF_11KW_PFC_SIC_QD.

Note: The PE line between the AC source and REF_11KW_PFC_SIC_QD needs to be connected always, and the required current and voltage insulation ratings of cables are followed for safety reasons.

The DC voltage is regulated by the microcontroller following the droop rule introduced in Section 4.3, which allows the user to control both the power conversion and the power-flow direction by changing the DC source/load voltage setting.

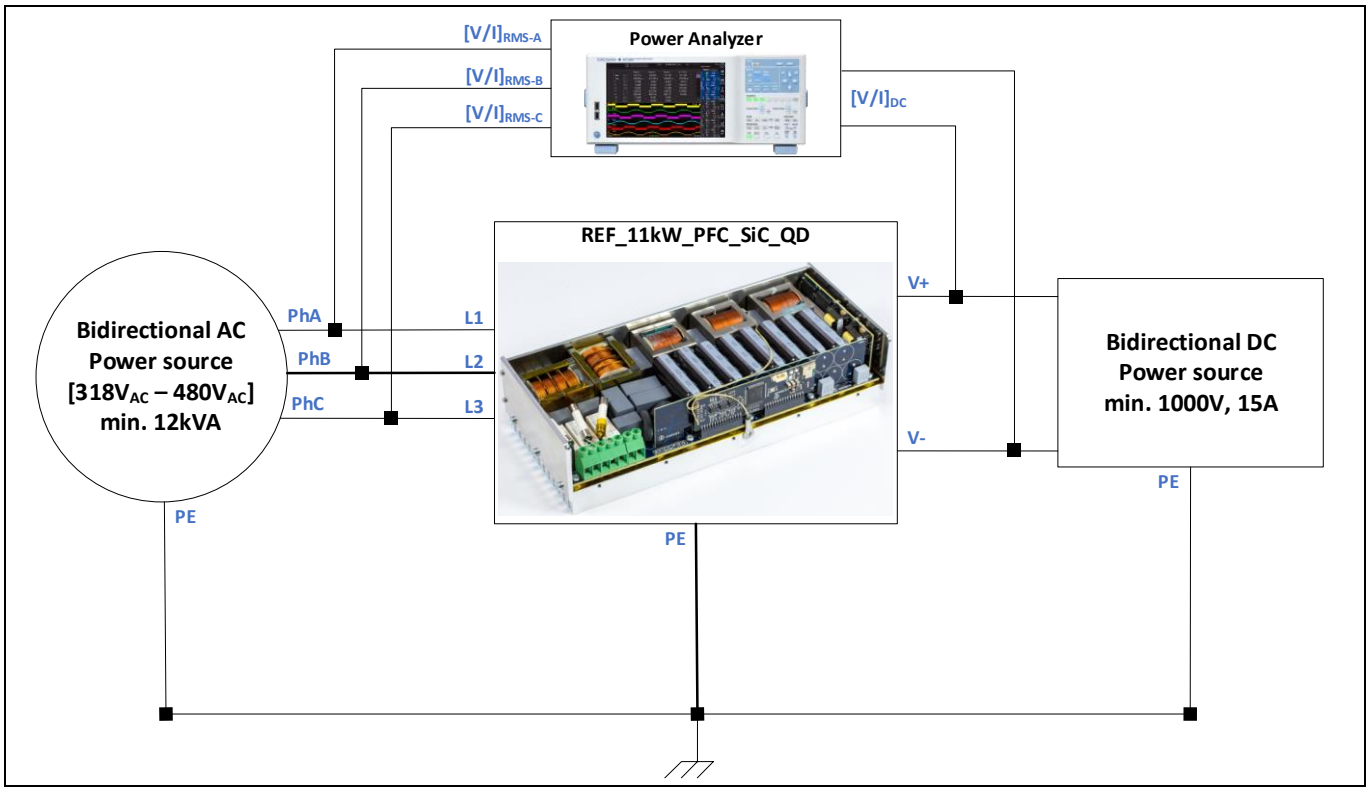


Figure 39 Test setup for three-phase operation: both PFC and inverter modes

Note: Under three-phase operation mode, REF_11KW_PFC_SIC_QD is designed with AC side three-wire connection without neutral wired. Ensure that during the three-phase operation, the neutral terminal on the board is left unconnected.

The single-phase test setup is demonstrated in Figure 40. Being different from three-phase setup, during single-phase testing, the L1 and L2 terminals of REF_11KW_PFC_SIC_QD should be combined (shorted) externally and connected to the phase terminal of the AC source. Additionally, the L3 and N terminals of REF_11KW_PFC_SIC_QD should be combined externally and connected to the neutral terminal of the AC

source. The cable connecting either phase or neutral should be at least 32 A rated to deliver 7.3 kW power in single phase.

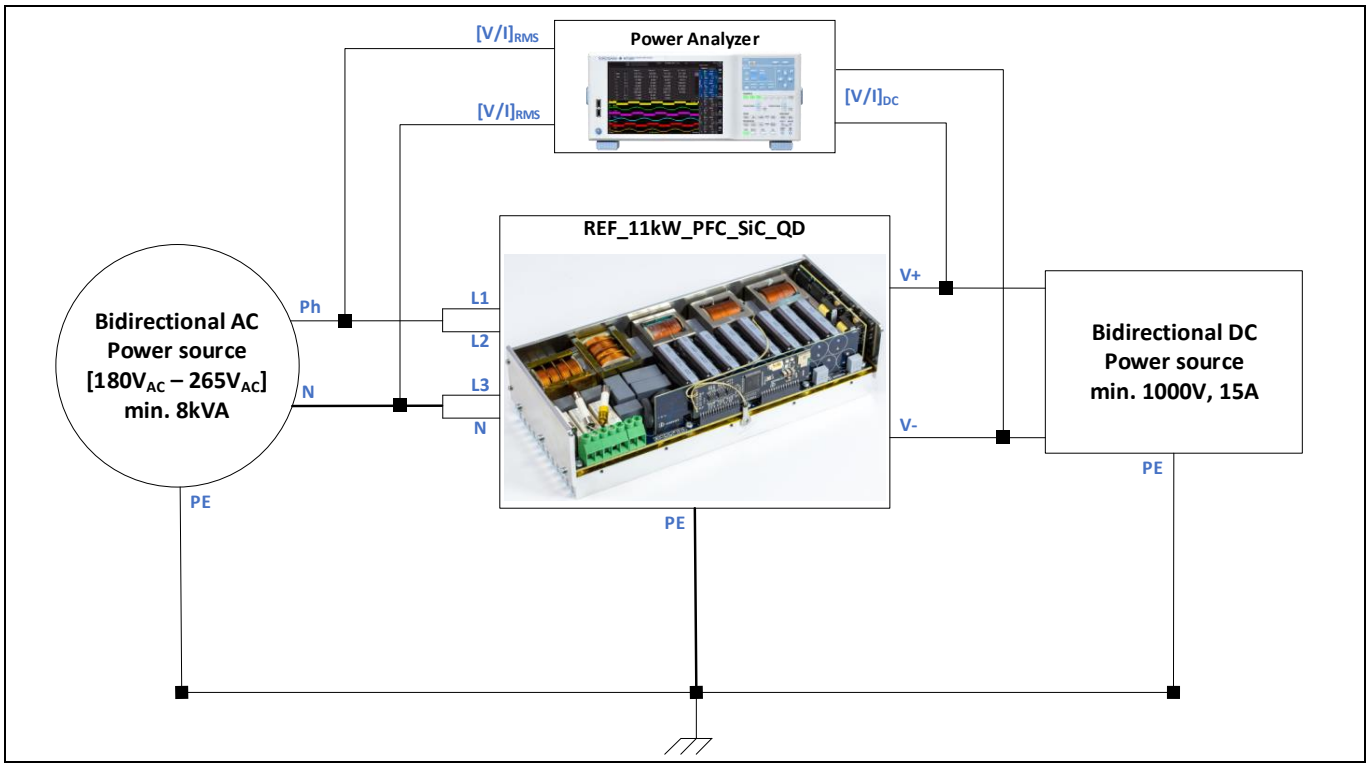


Figure 40 Test setup for one-phase operation: both PFC and inverter modes

An external fan with 500 mW power supply (<12 V) below the cold plate and four channel power quality analyzer in the setup are required to evaluate the design. In case bidirectional operation is not required, the previous setup can be simplified as follows:

- For PFC mode operation alone, bidirectional source/load can be replaced by unidirectional source/load
- For inverter mode operation alone, the same replacement can be done with an additional diode in positive rail on the DC side for safety operation
- For inverter mode operation, REF_11KW_PFC_SiC_QD should be always connected to the grid. Offline operation is not supported

5.1 Converter startup

5.1.1 AC to DC (PFC mode) startup

This subsection introduces the procedure of starting REF_11KW_PFC_SIC_QD in PFC mode. The waveform during three-phase startup is depicted in Figure 41.

Immediatley after the AC-side input voltage is applied, the bulk capacitor bank is charged via the inrush-current-limiting resistors and 3L-ANPC brige-leg as uncontrolled rectifier. The auxiliary power card starts to work when the overall bulk voltage is greater than 100 V. After being powered up, the microcontroller monitors both the AC and DC voltages and closes the input relays when both are in range. Then, the PWM signals are applied to boost both upper and lower DC bulk voltages to 400 V.

Note: The startup operation in loaded condition must be avoided as the excessive power can damage inrush-current-limiting resistors on the AC side.

Figure 41 shows the different parameters measured, which includes DC+ and DC- voltages, grid currents on all three phases (A, B, and C), grid voltage on ph-A. At an input voltage level of 230 V_{AC}, the input current peaks at 19 A from each line.

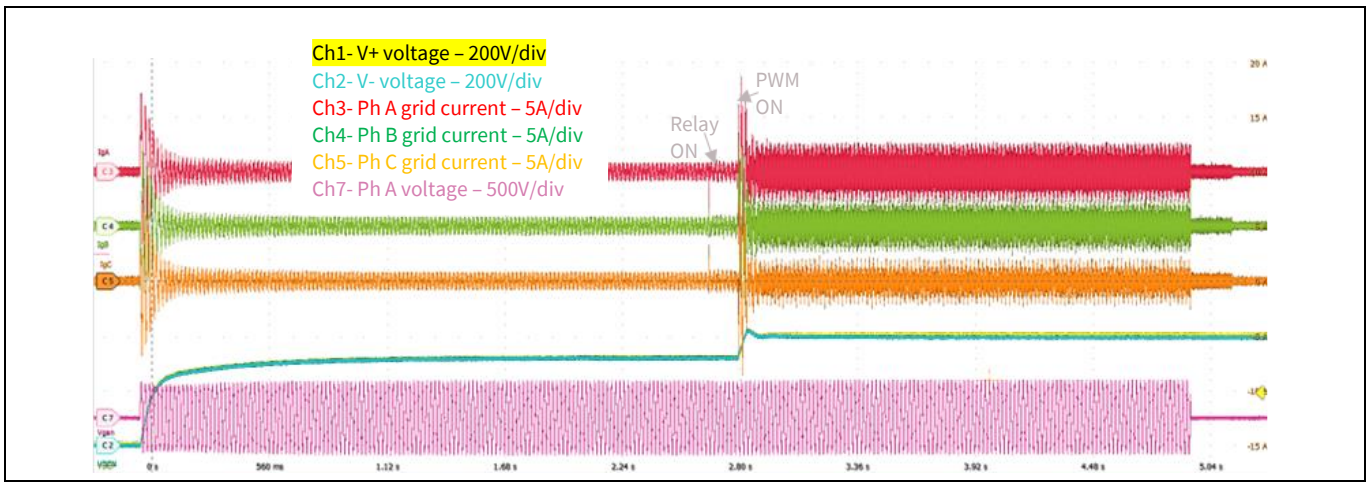


Figure 41 Waveform captured during startup under three-phase PFC mode

5.1.2 DC to AC (inverter mode) startup

REF_11KW_PFC_SIC_QD can also start up with DC-side powered before the AC grid connection, which is noted as inverter mode startup.

Being different to the PFC mode startup, a DC voltage in between 789 V and 811 V (three-phase droop range) should be applied first to the DC terminal before connecting the AC grid side, i.e., enabling the AC source output during testing. The microcontroller is initially powered up and wait for the AC grid voltage to fall into operational range. As shown in Figure 42, with the DC voltage available before 0 s, the converter starts switching after 740 ms of 230 V AC supply availability. Later, after startup, the actual operation mode (either PFC or inverter mode) is decided based on the droop curve demonstrated in Section 4.3.

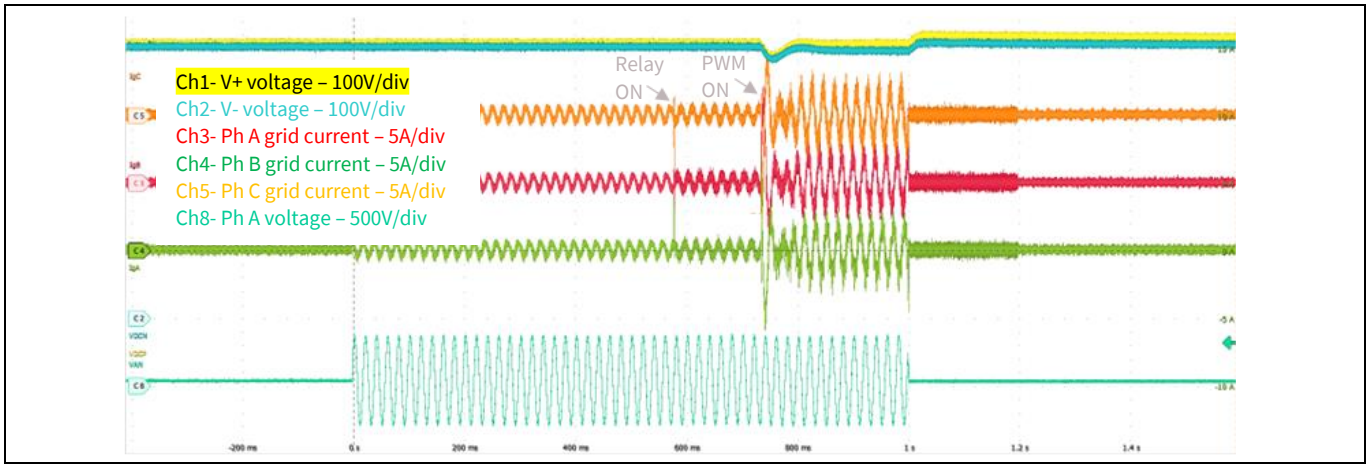


Figure 42 Waveform captured during startup under three-phase inverter mode

Note: The startup operation in single phase AC configuration is similar to that of in three-phase AC configuration.

5.2 Three-phase steady-state operation – efficiency, PF, and iTHD

5.2.1 PFC mode

The steady-state waveform captured during the three-phase PFC mode operation is shown in Figure 43, which includes the upper and lower bulk voltages, grid-side phase A, B, and C currents, and phase A voltage. It can be concluded that the three-phase current waveforms are in good shape and no significant distortion can be identified. The phase A grid-side current is in alignment with phase A voltage, which indicates a high power-factor.

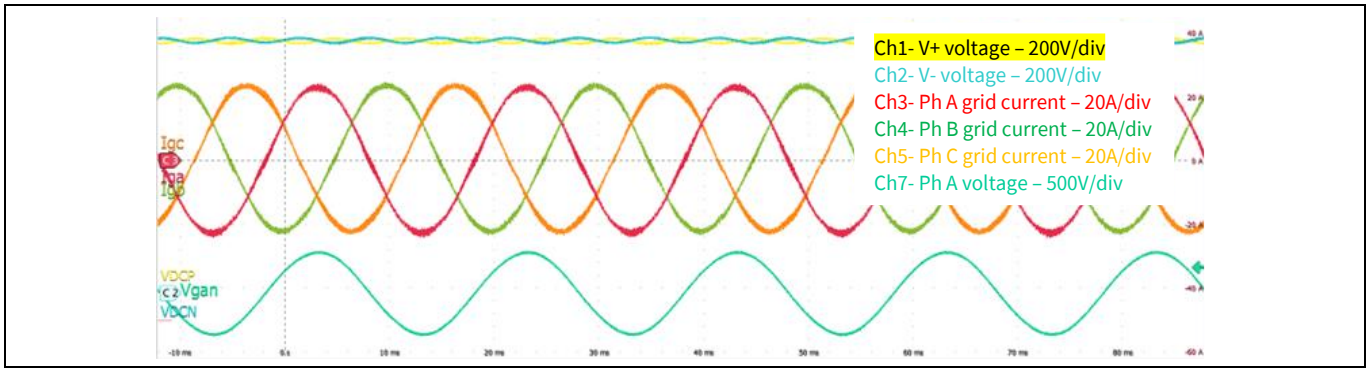


Figure 43 Three-phase PFC mode steady state operation – captured under 11 kW and nominal 230 V_{AC} (line-to-neutral voltage)

Figure 44 demonstrates the three-phase inductor-current waveforms captured during 11 kW and nominal 230 V_{AC} (line-to-neutral voltage) steady state operation. It is highlighted that the zero-crossing current sees no significant current spikes due to the refined zero-crossing control algorithm. The inductor currents are in sinusoidal shape with limited ripple current (6 A as measured peak-to-peak value).

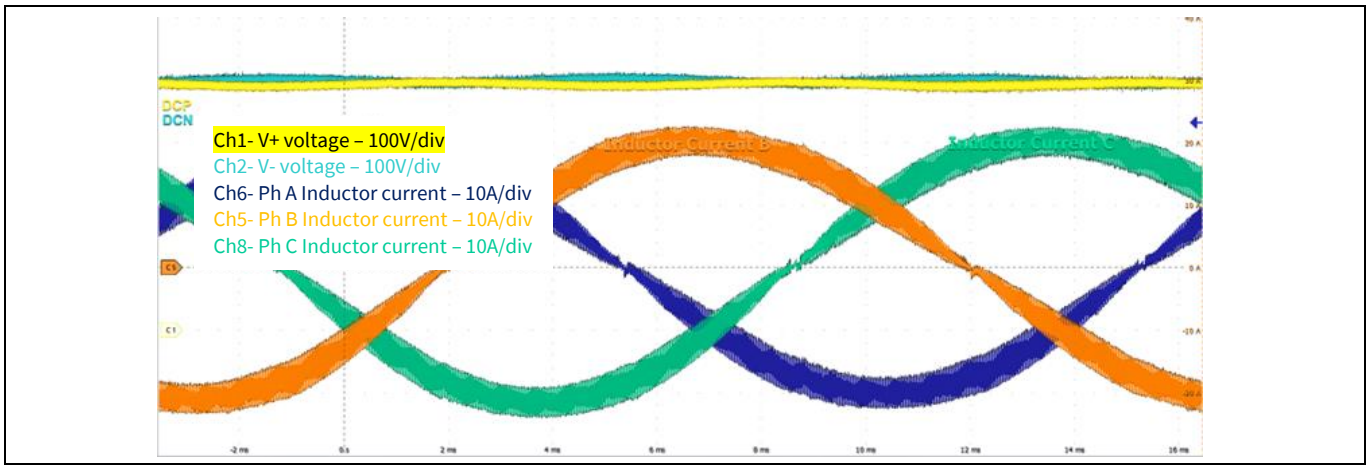


Figure 44 Inductor current waveforms under three-phase steady state operation – 11 kW and normal line 230 V_{AC} (line-to-neutral voltage)

The efficiency of REF_11KW_PFC_SIC_QD is measured following a thermal equilibrium condition of the running hardware at each loading condition. The measurements are obtained using a Yokogawa WT5000 power analyzer without line filters and at 50 Hz line voltage. Figure 45 and Figure 46 display the measured efficiency and power loss under three-phase PFC mode operation at different line-to-neutral voltages. The peak efficiencies of 99.295%, 99.15%, and 98.874% and full-load efficiencies 99.197%, 98.963%, and 98.636% are measured for the high-line, nominal, and low-line conditions, respectively. The efficiency curves feature a flat

tendency with loading greater than half-load. It is noted that no external auxiliary supply is needed for the operation except the fan, which consumes 500 mW continuous power during testing.

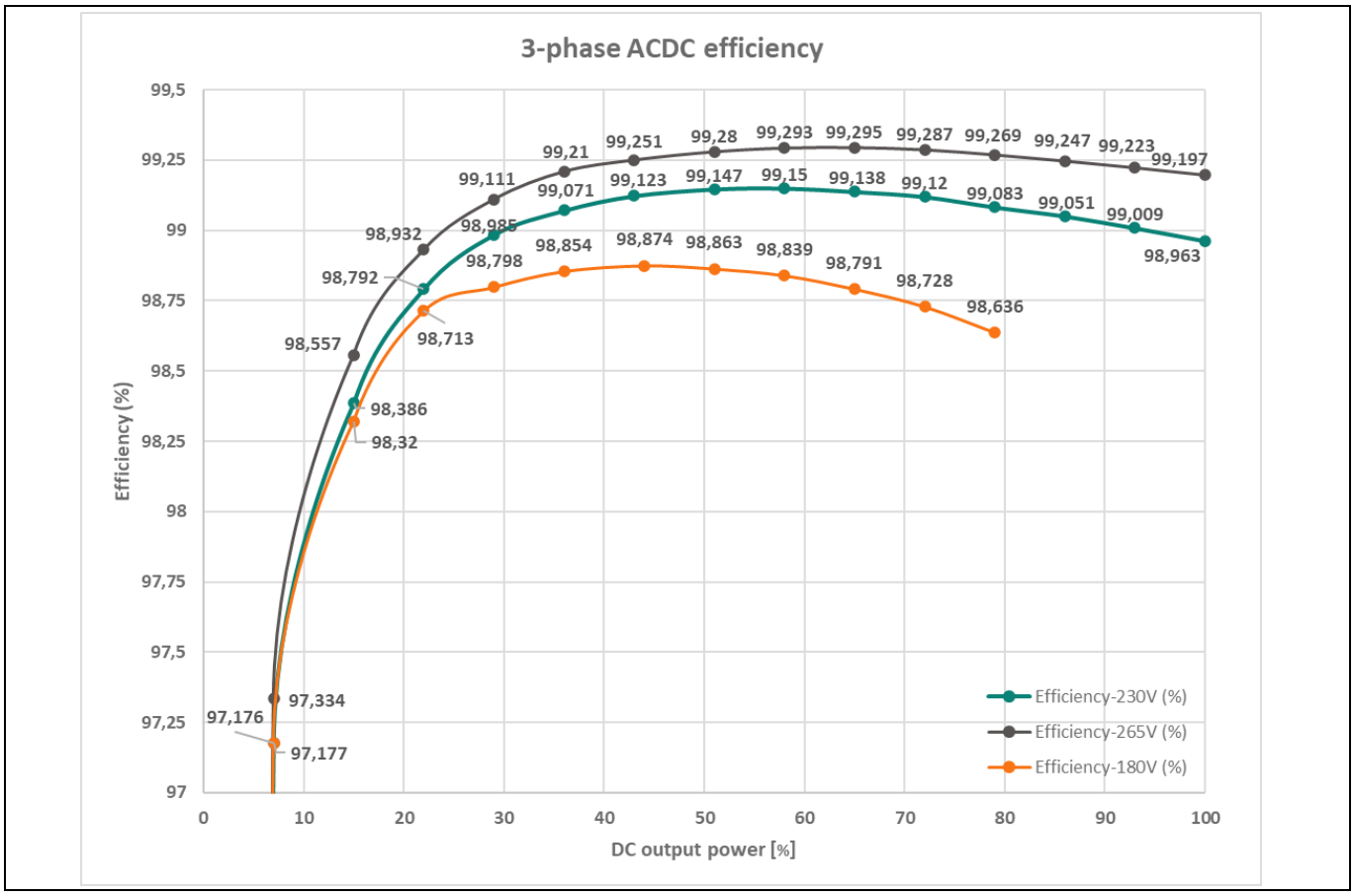


Figure 45 Measured efficiency under three-phase PFC mode at different line-to-neutral voltages (180 V_{AC}, 230 V_{AC}, and 265 V_{AC})

Figure 46 Measured power loss under three-phase PFC mode at different line-to-neutral voltages (180 V_{AC}, 230 V_{AC}, and 265 V_{AC})

Figure 47 shows an estimation of the breakdown of the power losses of the reference board at 10% to 100% of rated power for the 230 V_{AC} input. The main contributors to power losses are the winding losses of inductors, as well as the conduction and switching losses from power semiconductors.

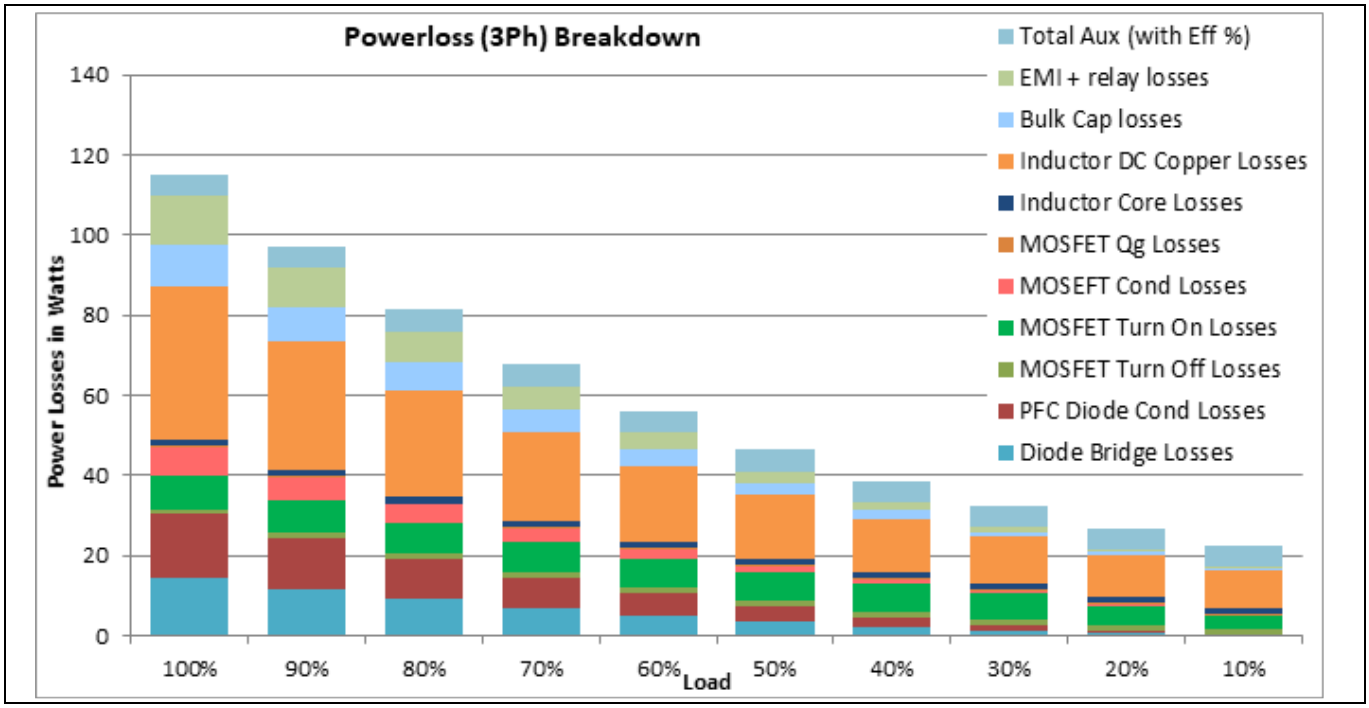


Figure 47 REF_11KW_PFC_SIC_QD power loss breakdown under three-phase PFC mode with 230 V_{AC} (line-to-neutral voltage) input

The power factor (PF) and current total harmonic distortion (iTHD) measurements are two of the major factors for evaluating the power quality performance. Figure 48 and Figure 49 summarize the measured PF and iTHD values at low-line, nominal and high-line AC grid voltages under different loading conditions. It can be observed from Figure 48 that the power factor is higher than 0.99 from 30% load to 100% load.

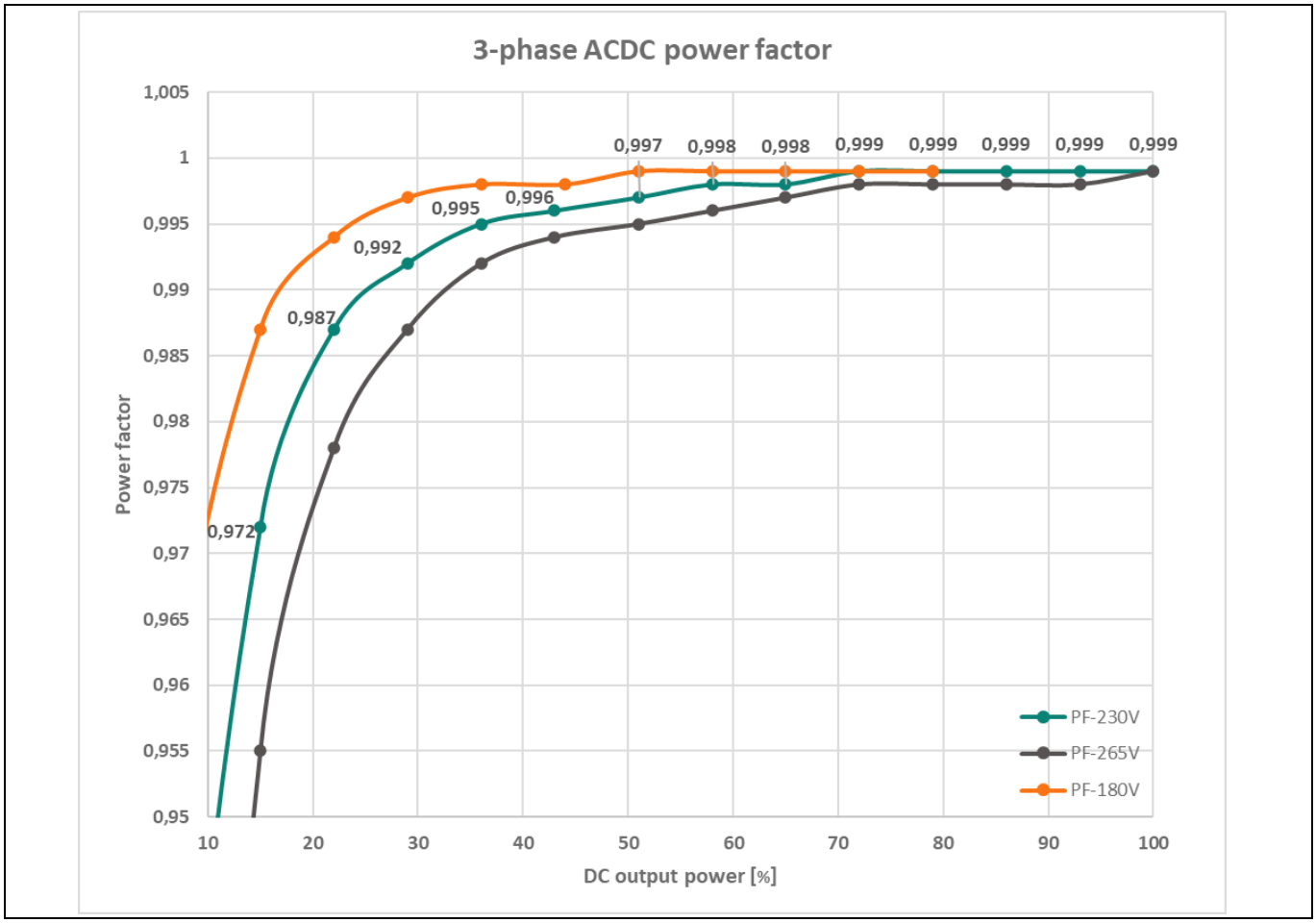


Figure 48 Measured PF under three-phase PFC mode at different line-to-neutral voltages (180 V_{AC}, 230 V_{AC}, and 265 V_{AC})

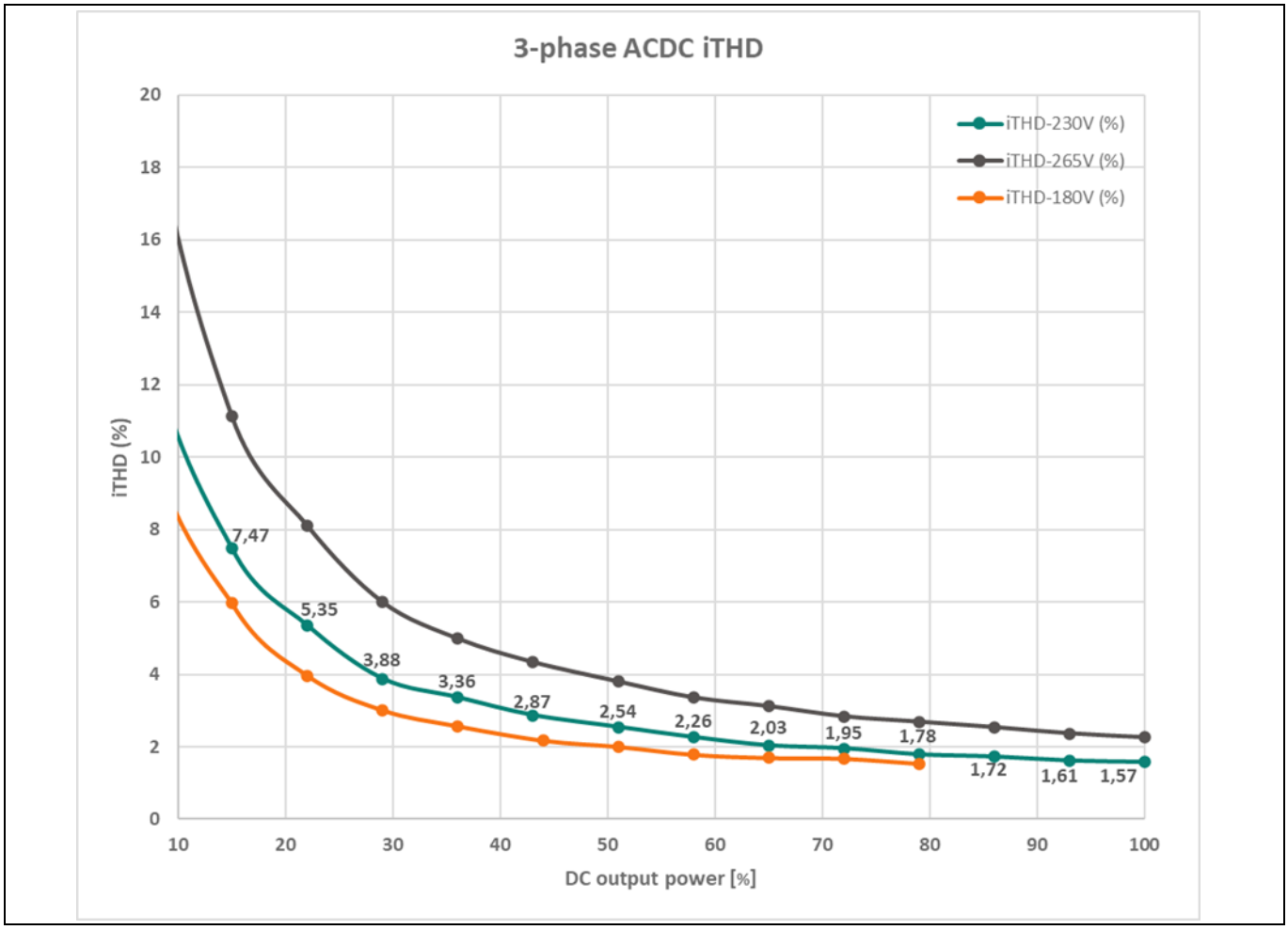


Figure 49 Measured iTHD under three-phase PFC mode at different line-to-neutral voltages (180 V_{AC}, 230 V_{AC}, and 265 V_{AC})

It can be observed from Figure 49 that the iTHD values drops significantly with the increase of loading. This is a strong indication that the current sensors are not affected by the stray-field interference. Otherwise, the iTHD increases with higher loading condition.

5.2.2 Inverter mode

The steady-state waveforms captured during three-phase inverter mode operation is shown in Figure 50, which includes the upper and lower bulk voltages, grid-side phase A, B, and C currents, and phase A voltage. It can be concluded that the three-phase current waveforms are in good shape and no significant distortion can be identified. Being different than the PFC mode operation, the phase A grid-side current is in counter-phase with phase A voltage, which indicates the inverter operation with high power-factor. In addition, no significant zero-crossing-distortion can be observed with the grid current waveform due to the refined zero-crossing control algorithm.

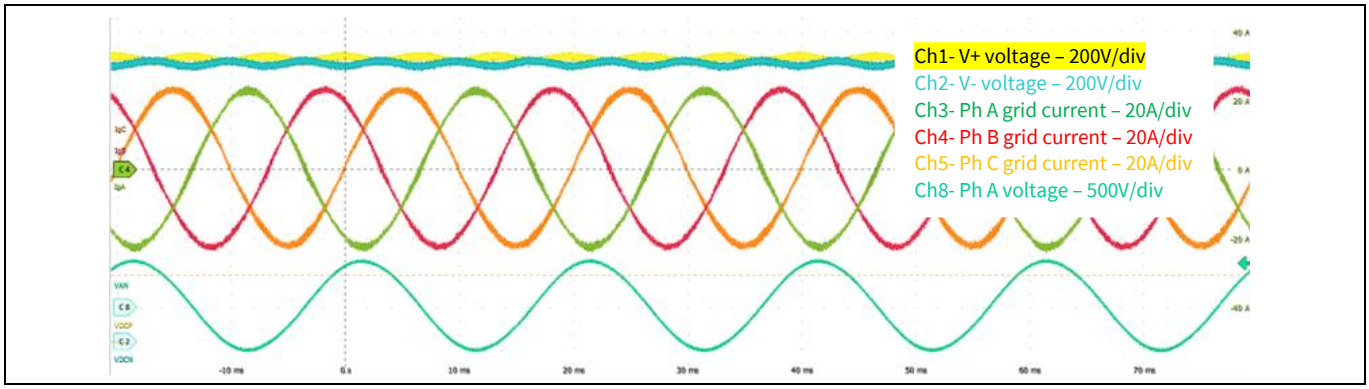


Figure 50 Three-phase inverter mode steady-state operation – captured under 11 kW and nominal 230 V_{AC} (line-to-neutral voltage)

Figure 51 and Figure 52 display the measured efficiency and power loss under three-phase inverter mode operation at different line voltages. The peak efficiencies of 99.263%, 99.122%, and 98.855% and the full-load efficiencies of 99.166%, 98.938%, and 98.632% are measured for the high-line, nominal, and low-line conditions, respectively. The efficiency curves also feature a flat tendency with loading greater than half-load. It is noted that no external auxiliary supply is needed for the operation except the fan, which consumes 500 mW continuous power during testing.

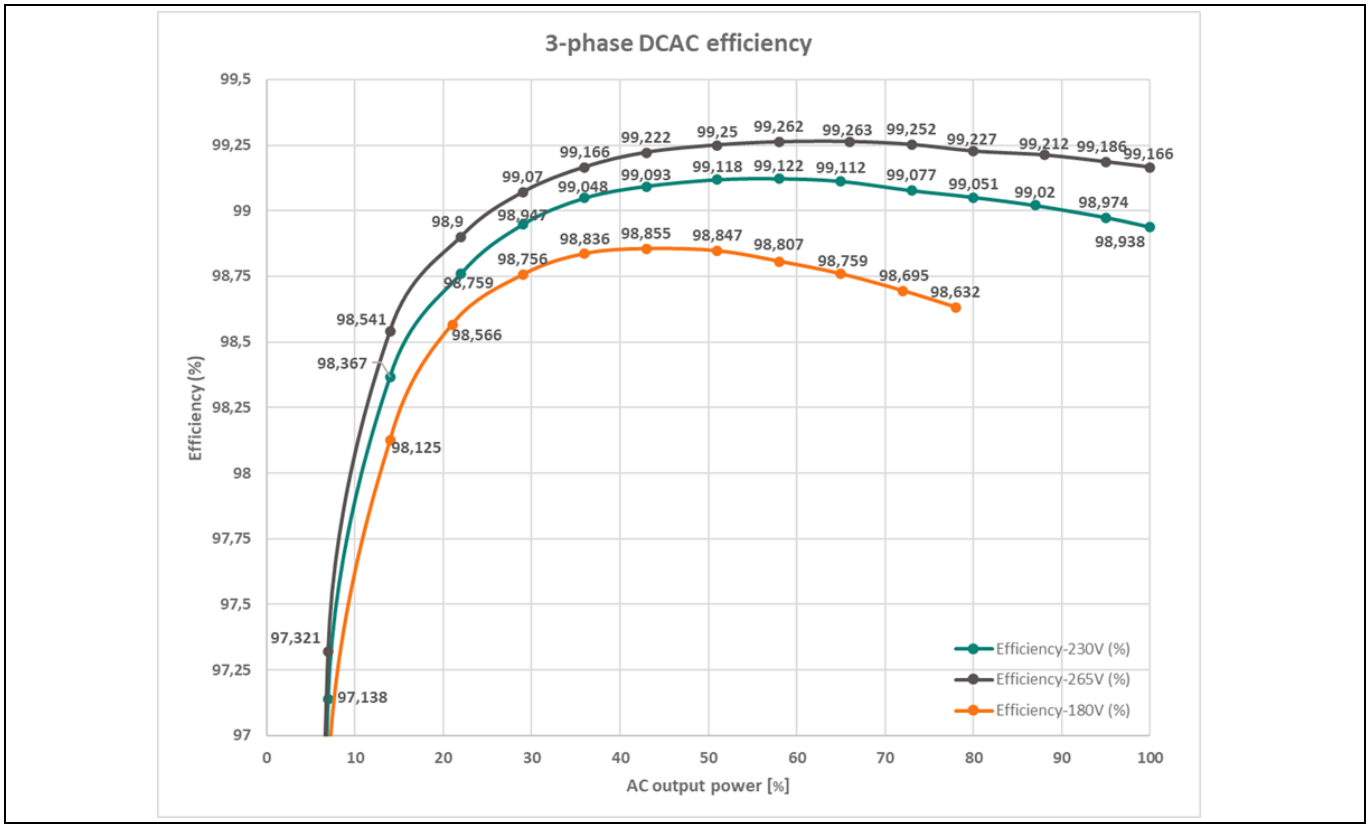


Figure 51 Measured efficiency under three-phase inverter mode at different line-to-neutral voltages (180 V_{AC}, 230 V_{AC}, and 265 V_{AC})

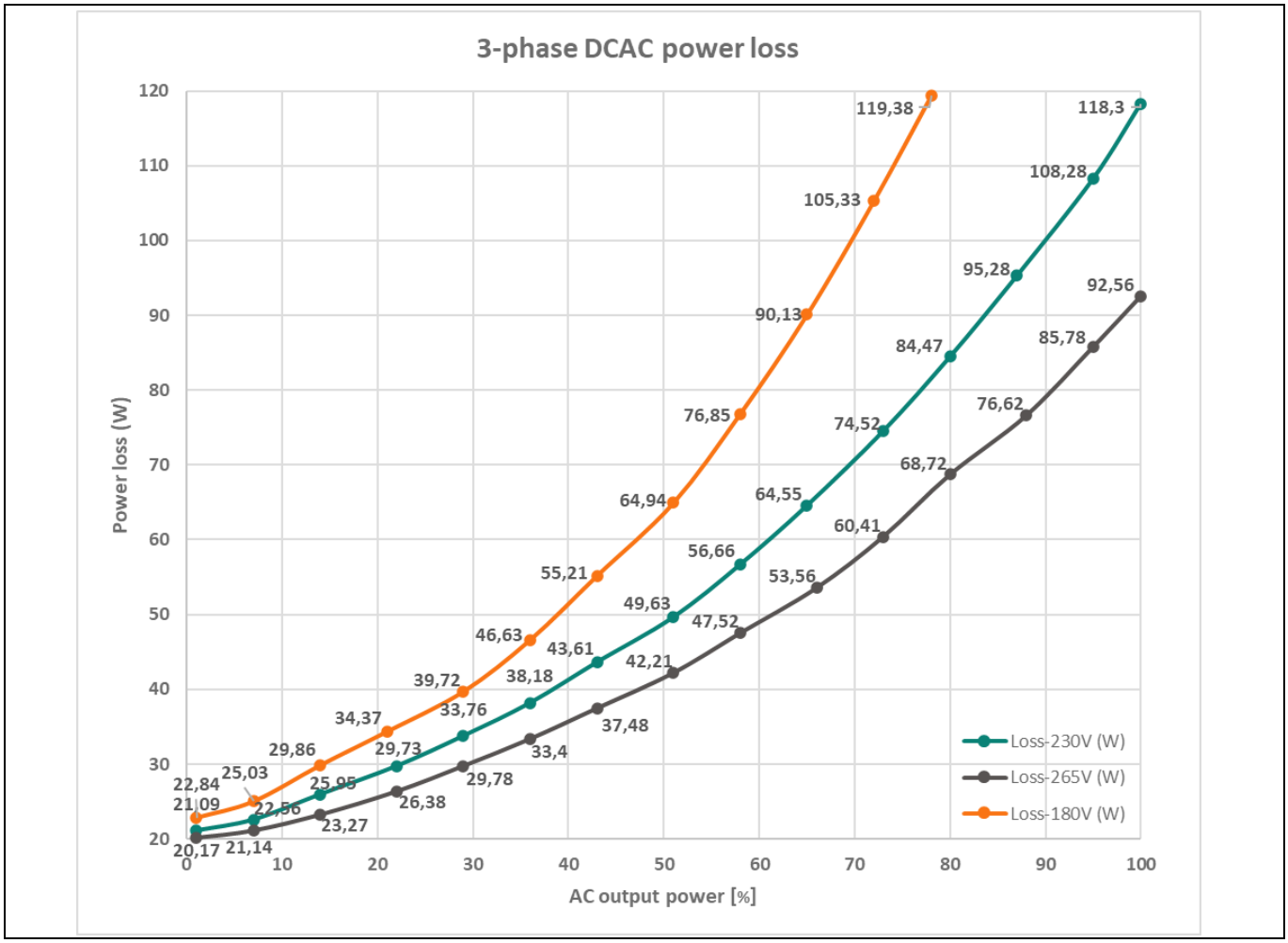


Figure 52 Measured power loss under three-phase inverter mode at different line-to-neutral voltages (180 V_{AC}, 230 V_{AC}, and 265 V_{AC})

Figure 53 and Figure 54 summarize the PF and iTHD measurements for steady-state operation under three-phase inverter mode at different AC grid voltages, 50 Hz line frequency. It can be observed that the PF value is always greater than 0.98 above 20% of rated power. Moreover, the iTHD value is less than 5% from 20% of rated power onwards and reaches significantly lower than 1.5% near the full-power operation point. Being similar to the iTHD curve measured under PFC mode, the inverter-mode iTHD drops significantly with the increase of loading, indicating a high immunity to the stray-field interference.

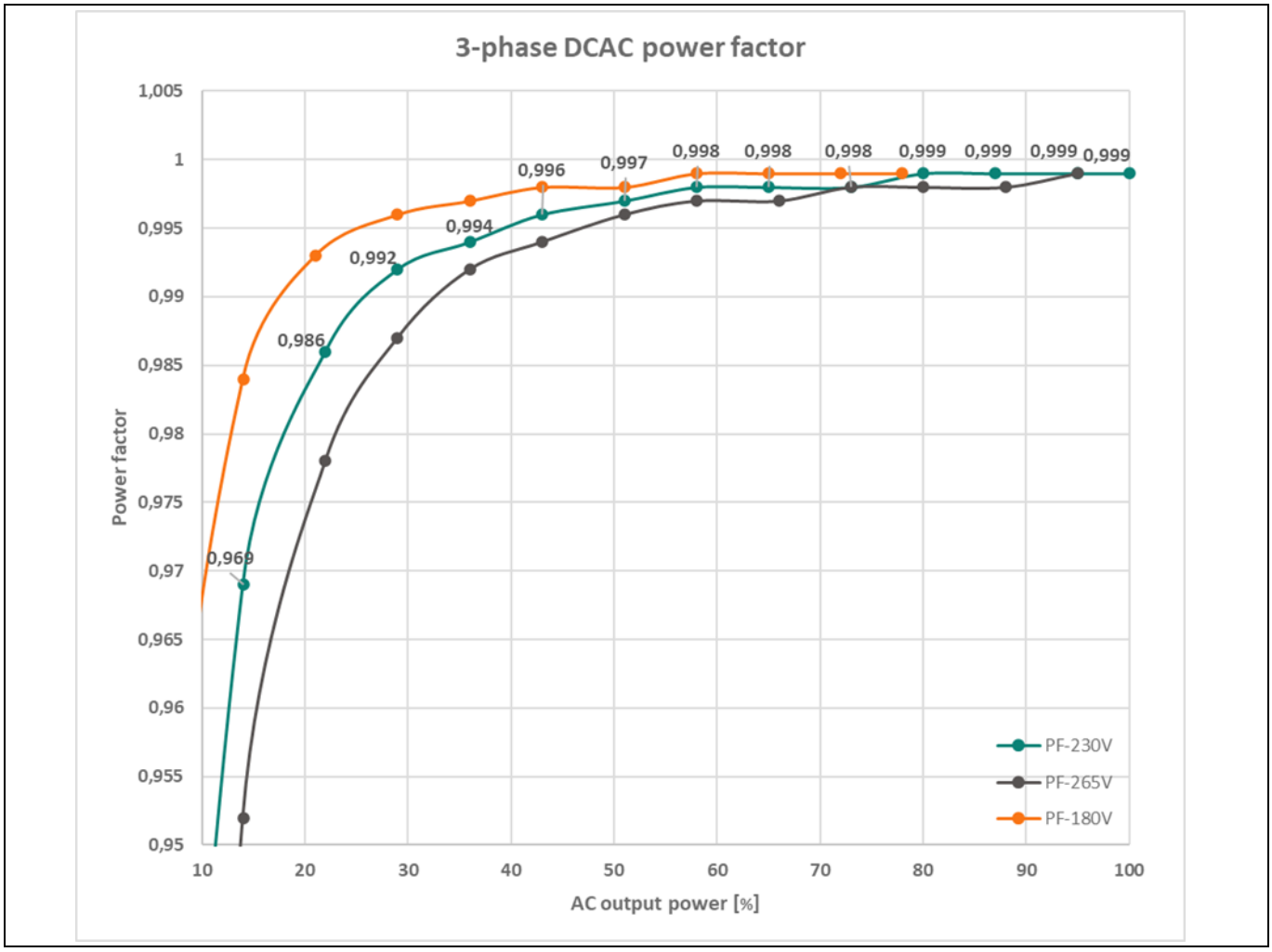


Figure 53 Measured PF under three-phase inverter mode at different line-to-neutral voltages (180 V_{AC}, 230 V_{AC}, and 265 V_{AC})

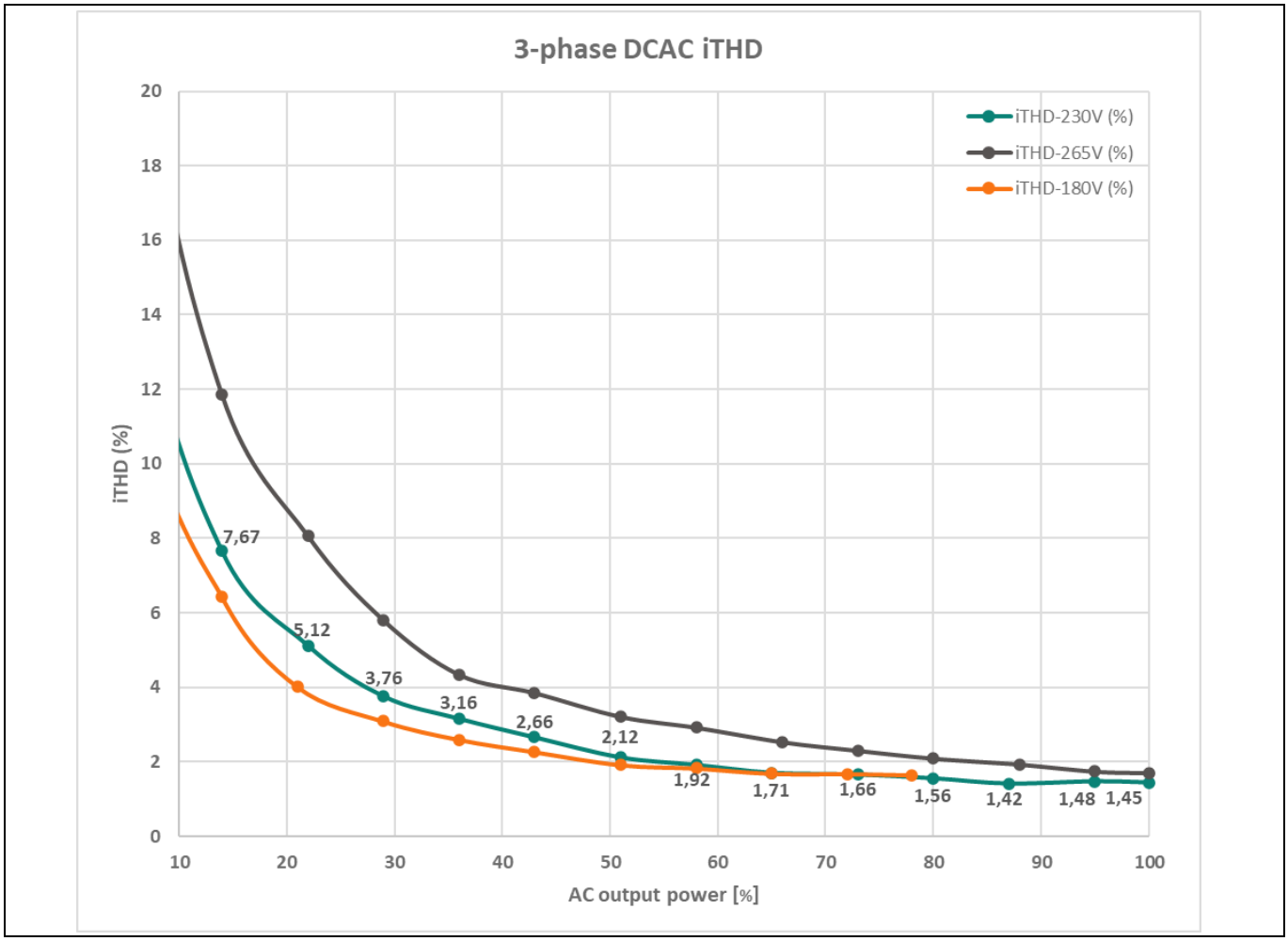


Figure 54 Measured iTHD under three-phase inverter mode at different line-to-neutral voltages (180 V_{AC}, 230 V_{AC}, and 265 V_{AC})

5.3 Single-phase steady-state operation – efficiency, PF, and iTHD

5.3.1 PFC mode

The steady-state waveform captured during single-phase PFC mode operation is shown in Figure 55, which includes the upper and lower bulk voltages, grid-side phase A and B currents, neutral line current, and phase voltage. It can be concluded that the phase A and B and neutral currents are in sinusoidal shape and no significant waveform distortion can be identified. The current is aligned with voltage, which indicates a high PF close to unity. The split bulk capacitor voltages are perfectly balanced with mean value at approximately 400 V. Each split bulk capacitor voltage features a maximum ripple of approximately 60 V peak-to-peak at rated power condition.

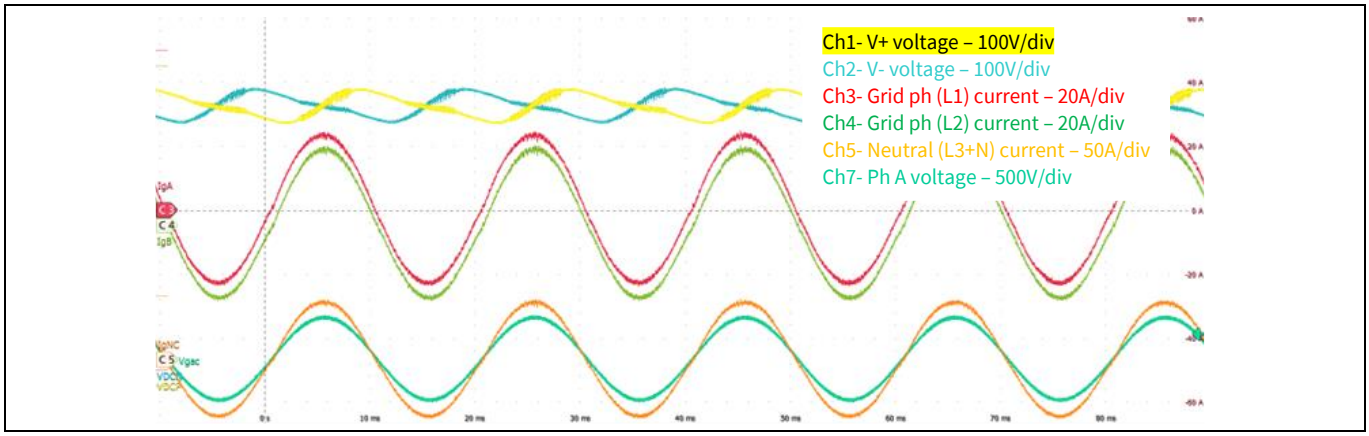


Figure 55 Single-phase PFC mode steady state operation – captured under 7.3 kW and 230 V_{AC}

Figure 56 shows the steady-state operation of REF_11KW_PFC_SIC_QD in single-phase PFC mode with phase-leg C operating as power pulsation buffer. The detailed operation principle of operating phase C as power pulsating buffer is demonstrated in Section 2.2. The phase C inductor current is sampled and presented as the green curve (Ch 4) in Figure 56. In order to lower the MOSFET switching loss and core loss, phase-leg C only works during the high-current interval, i.e., close to the current peak point. Doing so, REF_11KW_PFC_SIC_QD still features a good efficiency performance under single-phase operation. The blue curve (Ch 6) in Figure 56 denotes the gate-to-source voltage of device T_1 in phase-leg C, which confirms the applied operation region of phase-leg C.

It should also be noted that the modulation of phase-leg C starts only when the split bulk capacitor voltage ripples reach high level, which corresponds to above half-load loading condition. In this way, the efficiency performance below half-load condition is still high, where the operation of phase-leg C as power pulsation buffer is not needed and therefore not activated. It is also confirmed, from Figure 56, that operating phase-leg C under single-phase does not affect the waveform quality of the grid-side input current.

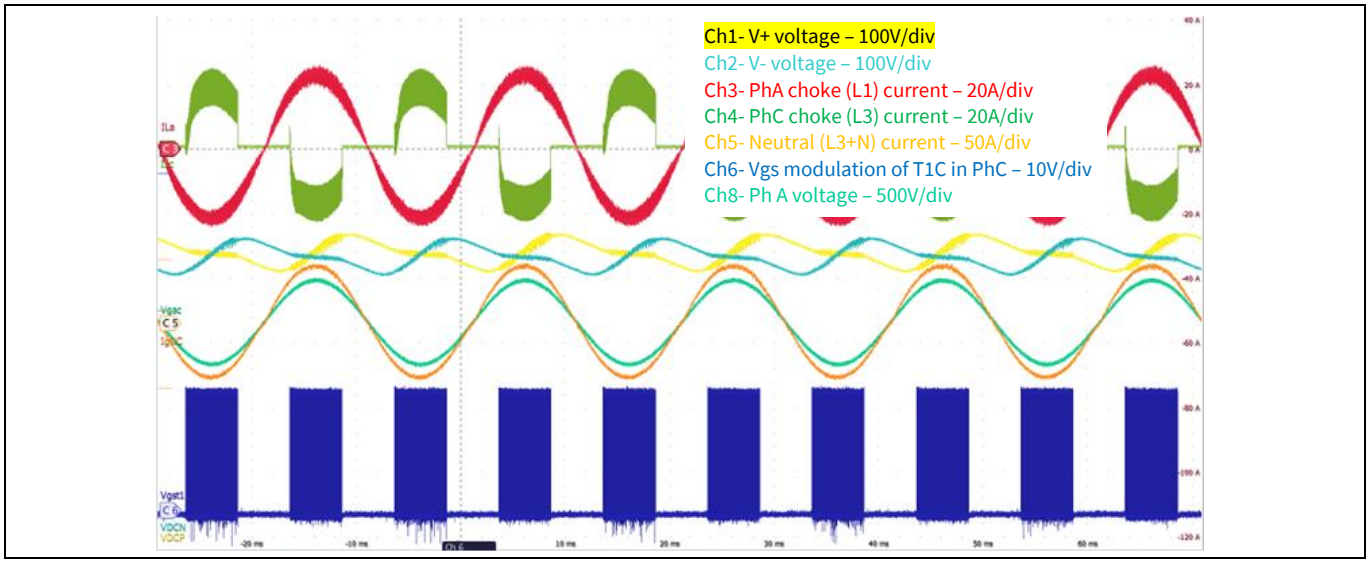


Figure 56 Single-phase PFC mode steady-state operation with phase-leg C operating as power pulsation buffer to redude the split bulk capacitor voltage ripples

Experimental results

In Figure 57 and Figure 58, the measured efficiency and power loss of REF_11KW_PFC_SIC_QD under single-phase PFC mode is shown at different AC line-to-neutral volages: 230 V_{AC}, 180 V_{AC}, and 265 V_{AC}. An external fan with power consumption of 500 mW is not included in the measurement.

For 230 V_{AC}, the efficiency peaks to 98.95% at around 50% of the rated load and reaches 98.38% at full load. While for 265 V_{AC}, the efficiency is 99.08% peaking at 50% load and 98.67% at full load. For 180 V_{AC} input, the full power is limited by the input 16 A_{RMS} current. with full-load efficiency of 97.95% and peak efficiency of 98.66%. It is observed that efficiency is reduced by approximately 0.4% after half-load condition because of the power loss contibution from phase-leg C.

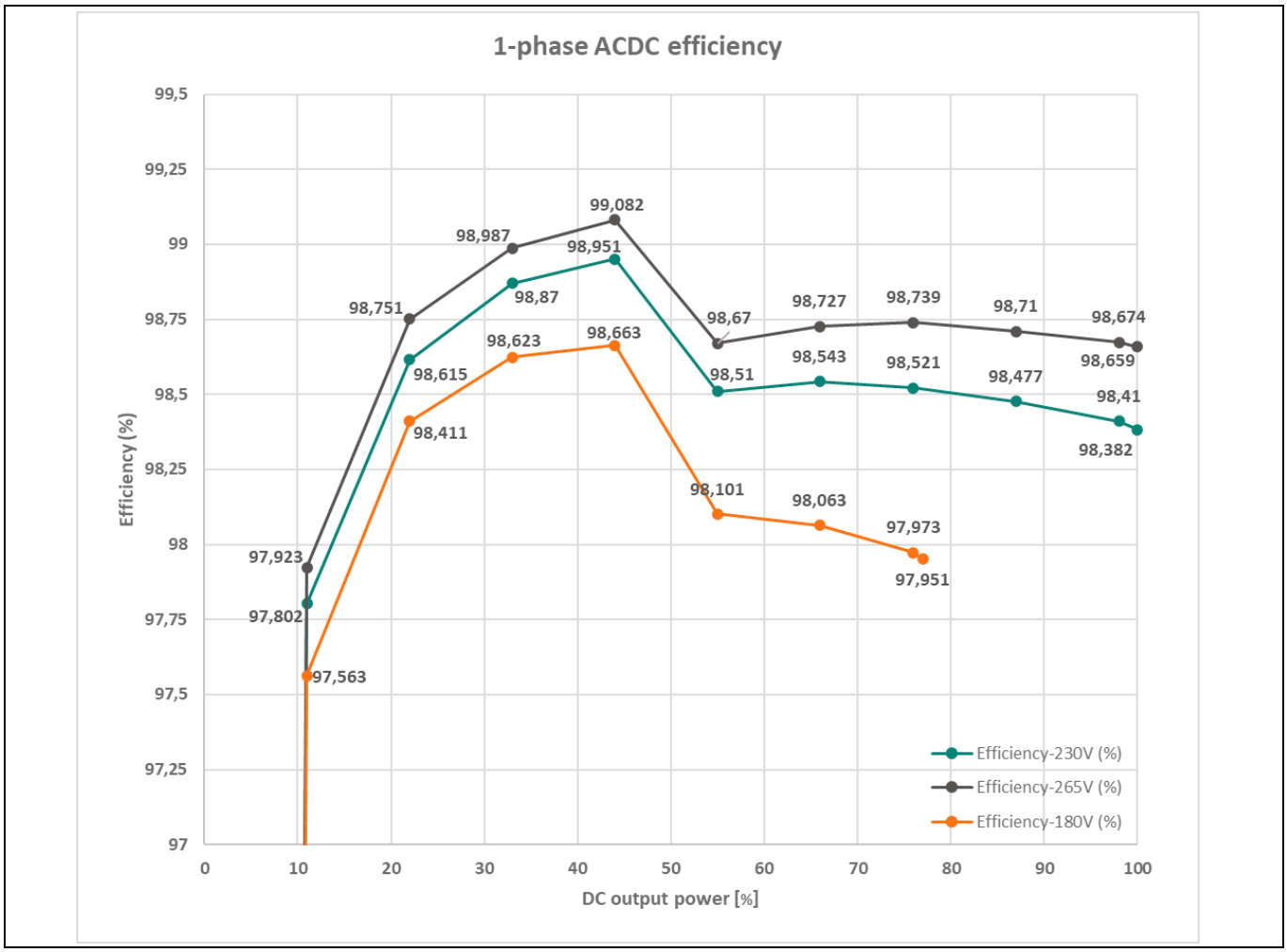


Figure 57 Measured single-phase PFC mode efficiency at different line voltages (180 V_{AC}, 230 V_{AC}, and 265 V_{AC})

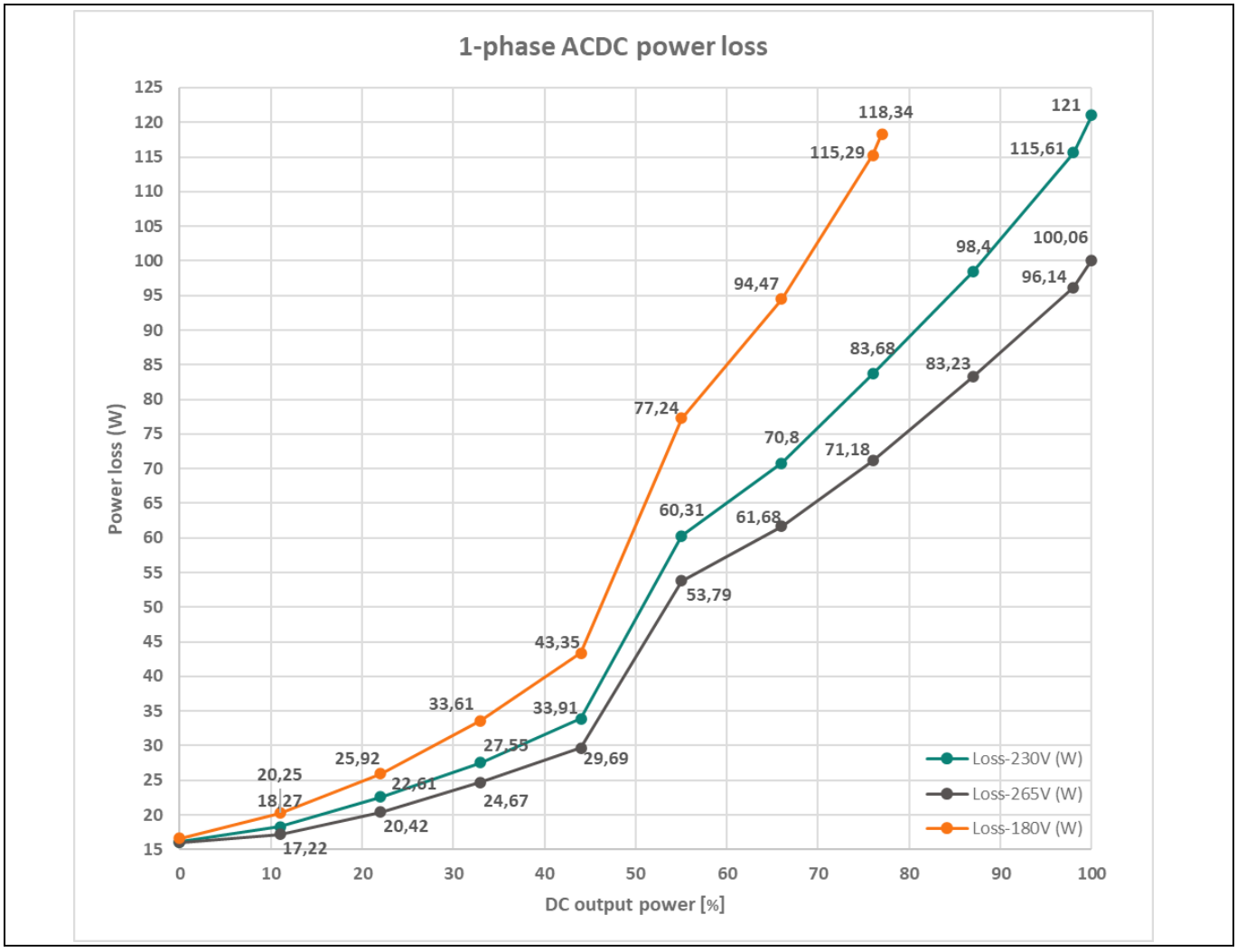


Figure 58 Measured single-phase PFC mode power loss at different line voltages (180 V_{AC}, 230 V_{AC} and 265 V_{AC})

Figure 59 and Figure 60 show the single-phase PF and iTHD measurements under PFC mode at different AC voltages, 50 Hz line frequency. Being similar to the three-phase measurements, the single-phase-PFC-mode PF is always greater than 0.98 with greater than 20% rated power. The iTHD also drop significantly with the increase of loading, and low level of iTHD is reach at heavy load conditions.

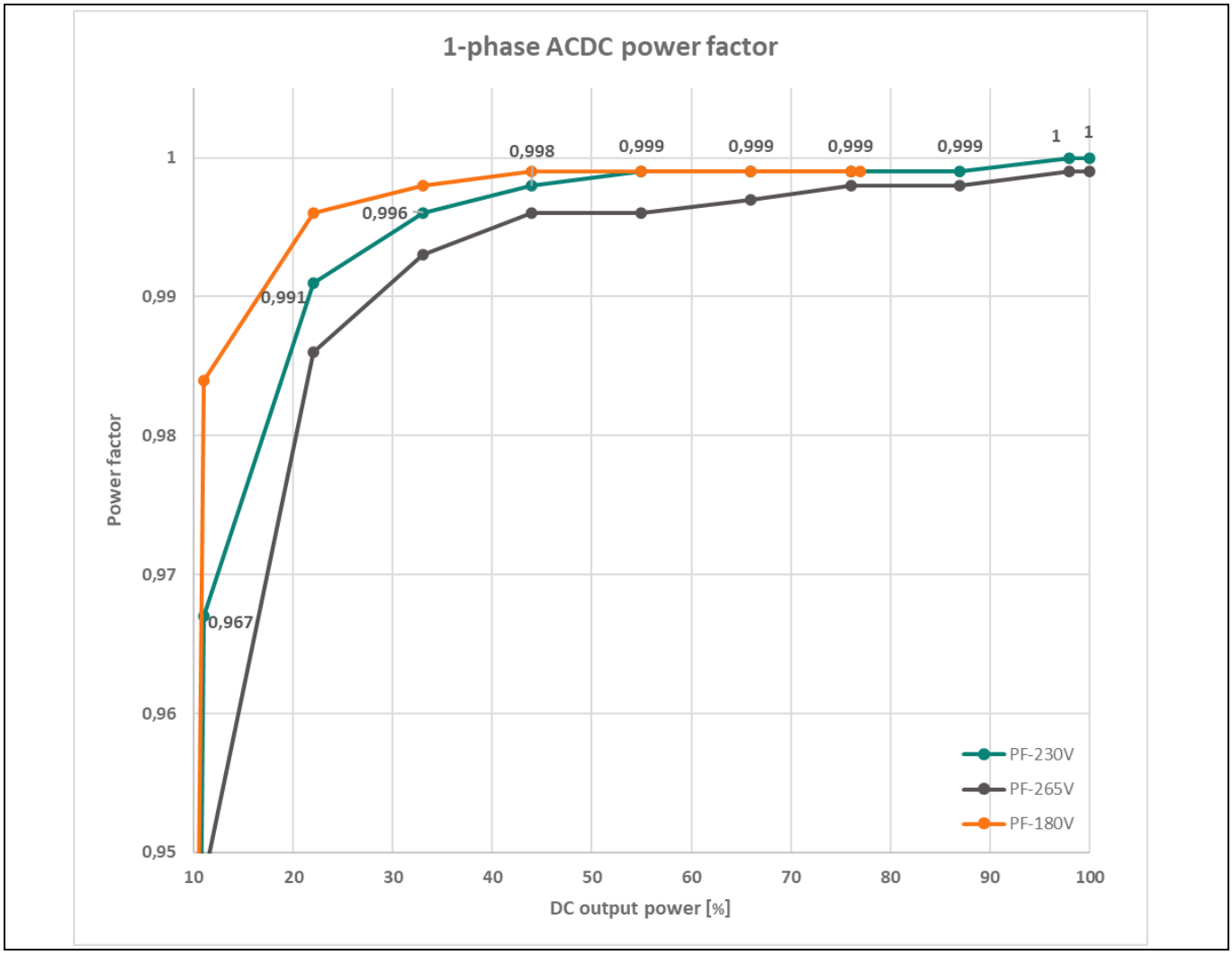


Figure 59 Measured single-phase PFC mode PF at different line voltages (180 V_{AC}, 230 V_{AC}, and 265 V_{AC})

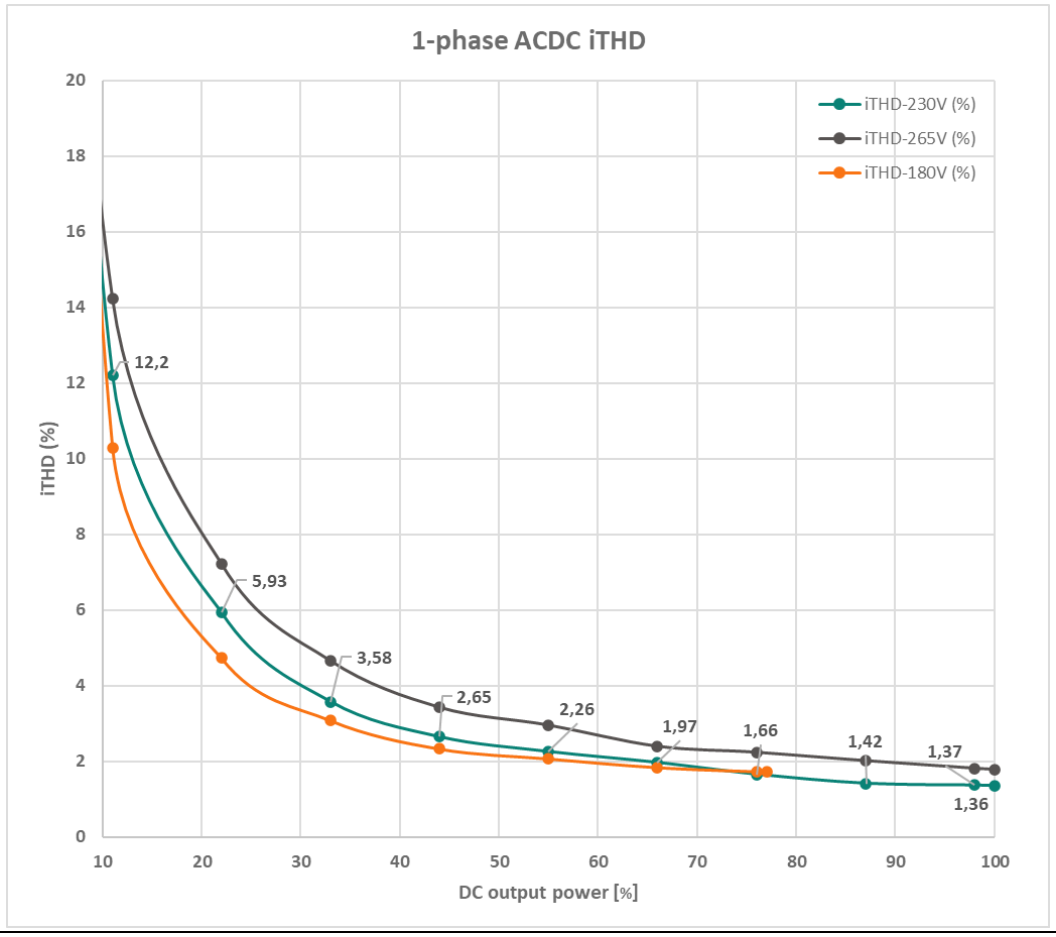


Figure 60 Measured single-phase PFC mode iTHD at different line voltages (180 V_{AC}, 230 V_{AC}, and 265 V_{AC})

5.3.2 Inverter mode

Figure 61 shows the steady-state full-load operation waveform of REF_11KW_PFC_SIC_QD under single-phase inverter mode. The waveforms of split bulk capacitor voltages show a maximum ripple of 70 V peak-to-peak with DC mean values near 400 V.

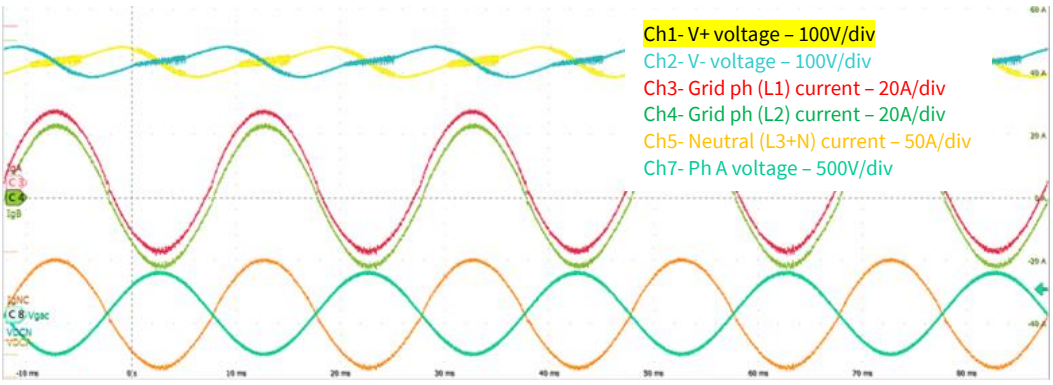


Figure 61 Single-phase inverter mode steady-state operation – captured under 7.3 kW and normal line 230 V_{AC}

Experimental results

In Figure 62 and Figure 63, the measured efficiency and power loss of REF_11KW_PFC_SIC_QD under single-phase inverter mode are shown at different AC line volages: 230 V_{AC}, 180 V_{AC}, and 265 V_{AC}. An external fan power consumption of 500 mW is not included in the measurements.

For 230 V_{AC} the efficiency peaks to 98.91% at around 50% of the rated load and is 98.33% at full load. While for 265 V_{AC}, the efficiency is 99.035% peak at 50% load and 98.61% at full load. For 180 V_{AC} input, the full power is limited by the input 16 A_{RMS} current with full-load efficiency of 97.95% and peak efficiency of 98.67%.

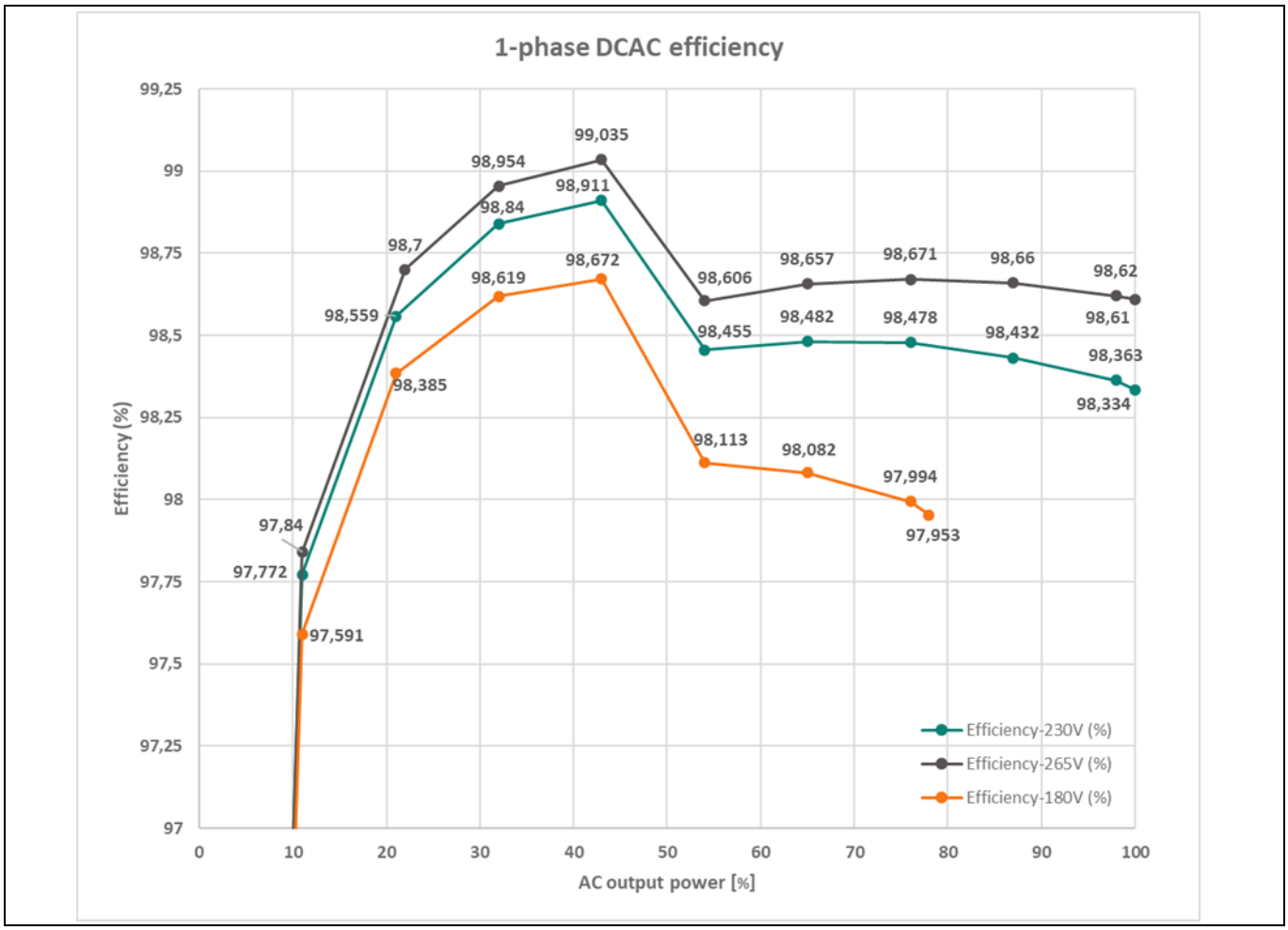


Figure 62 Measured single-phase inverter-mode efficiency at different line voltages on 1-phase AC (180 V_{AC}, 230 V_{AC}, and 265 V_{AC})

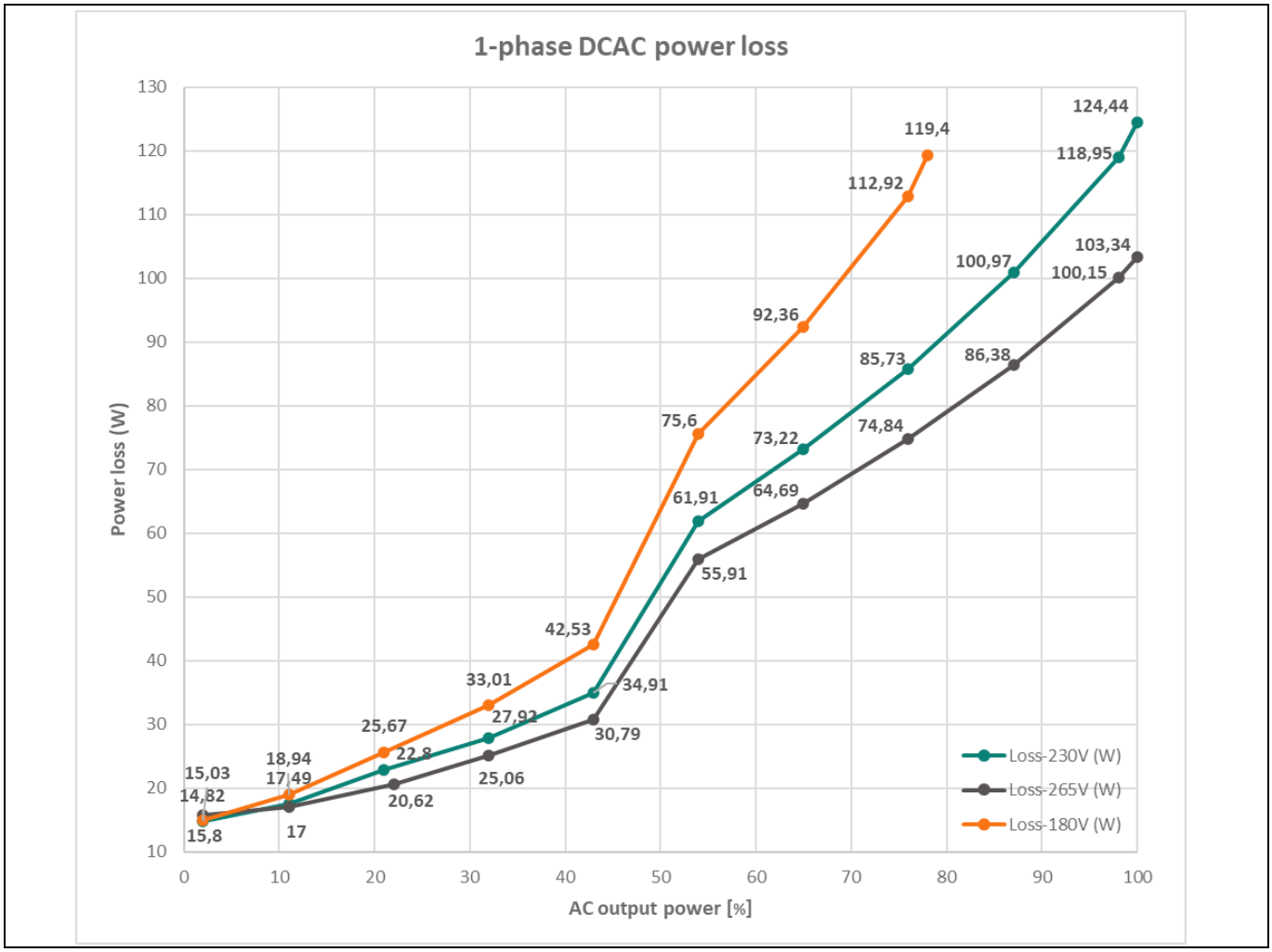


Figure 63 Measured single-phase inverter mode power loss at different line voltages (180 V_{AC}, 230 V_{AC}, and 265 V_{AC})

Figure 64 and Figure 65 show the single-phase PF and input iTHD measurements under inverter mode at different AC voltages, 50 Hz line frequency. The iTHD also drops significantly with the increase of loading, and low level of iTHD is reach at heavy load conditions.

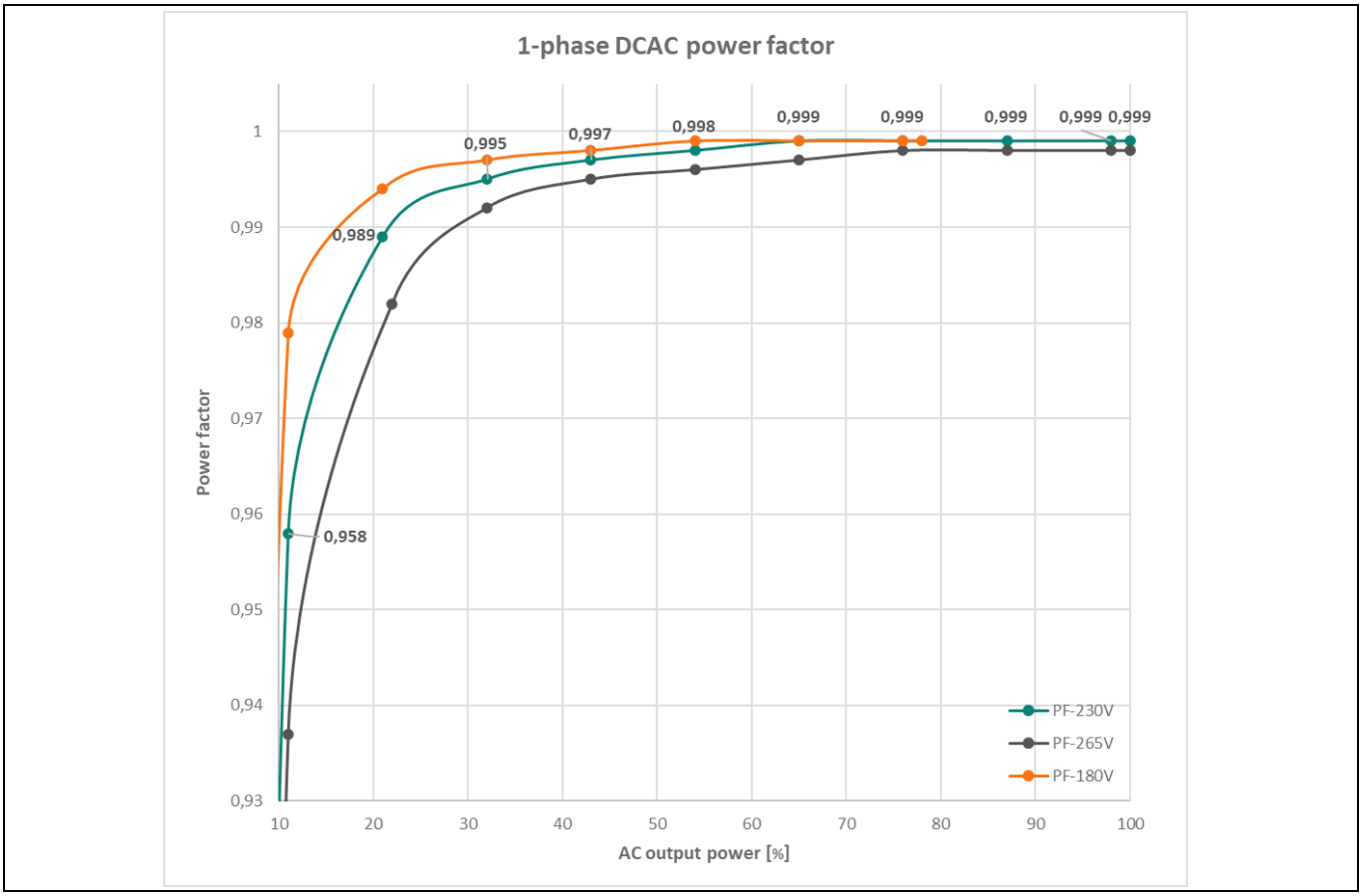


Figure 64 Measured single-phase inverter mode power factor at different line voltages (180 V_{AC}, 230 V_{AC}, and 265 V_{AC})

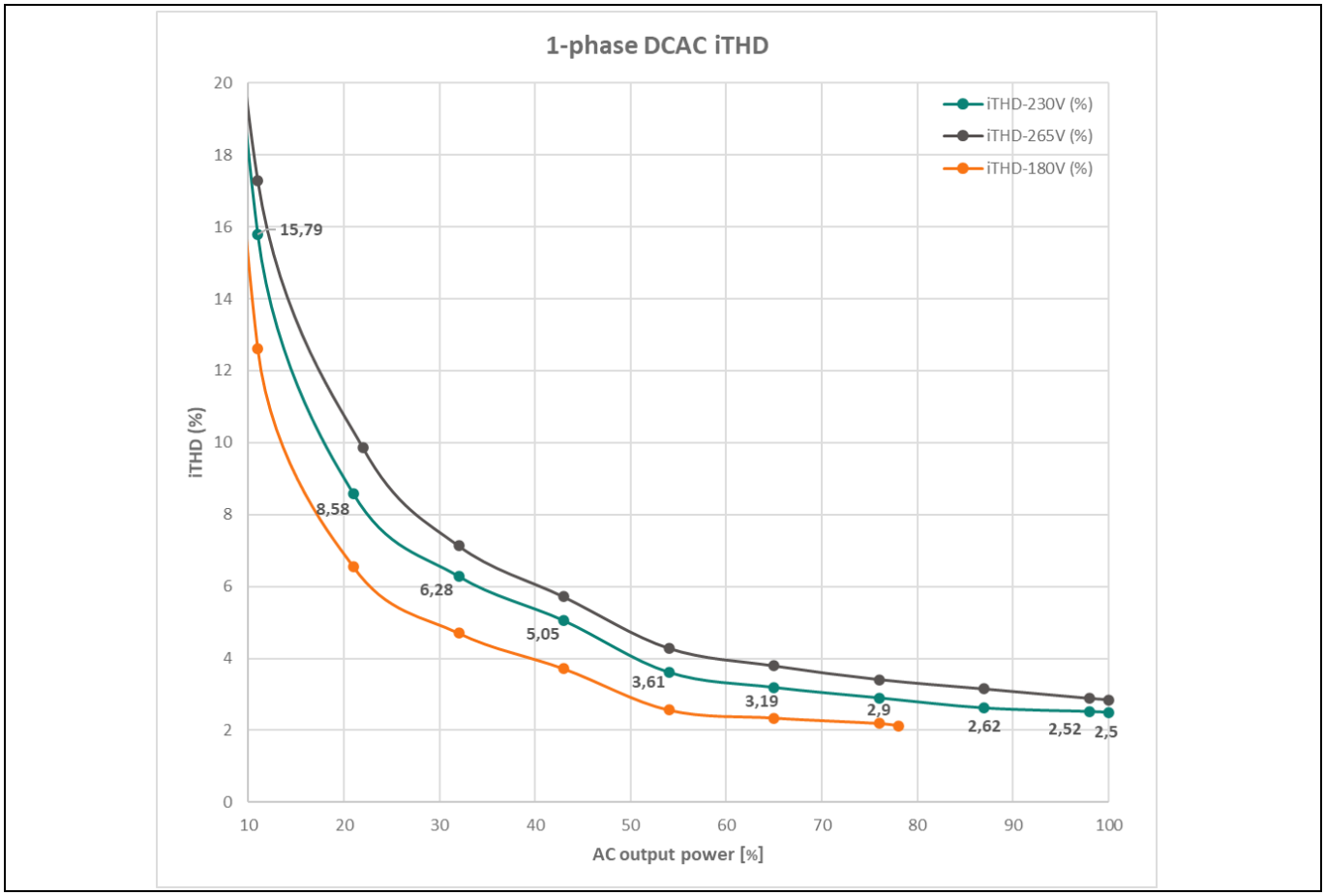


Figure 65 Measured single-phase inverter mode iTHD at different line voltages (180 V_{AC}, 230 V_{AC}, and 265 V_{AC})

5.4 Dynamic performance

5.4.1 Bidirectional power-flow transition

To fully evaluate the bidirectional capability of REF_11KW_PFC_SIC_QD, the PFC to inverter and inverter to PFC transition tests are designed and conducted.

During testing, REF_11KW_PFC_SIC_QD is connected in between bidirectional AC source and bidirectional DC supply, as it displayed in Figure 39 and Figure 40. The power flow transition can be triggered by modifying the DC supply voltage setting. The test waveforms of three-phase bidirectional transitions from PFC mode to inverter mode, as well as from inverter mode to PFC mode are shown in Figure 66 and Figure 67, respectively. The maximum time for full-power operating mode transition is less than 1.2 s, with bidirectional changeover happens in less than two full cycles of AC voltage. The grid currents maintain good quality even during the transition. Additionally, it is observed that no stability issue happens and the two split capacitor voltages are well regulated and balanced during the transition.

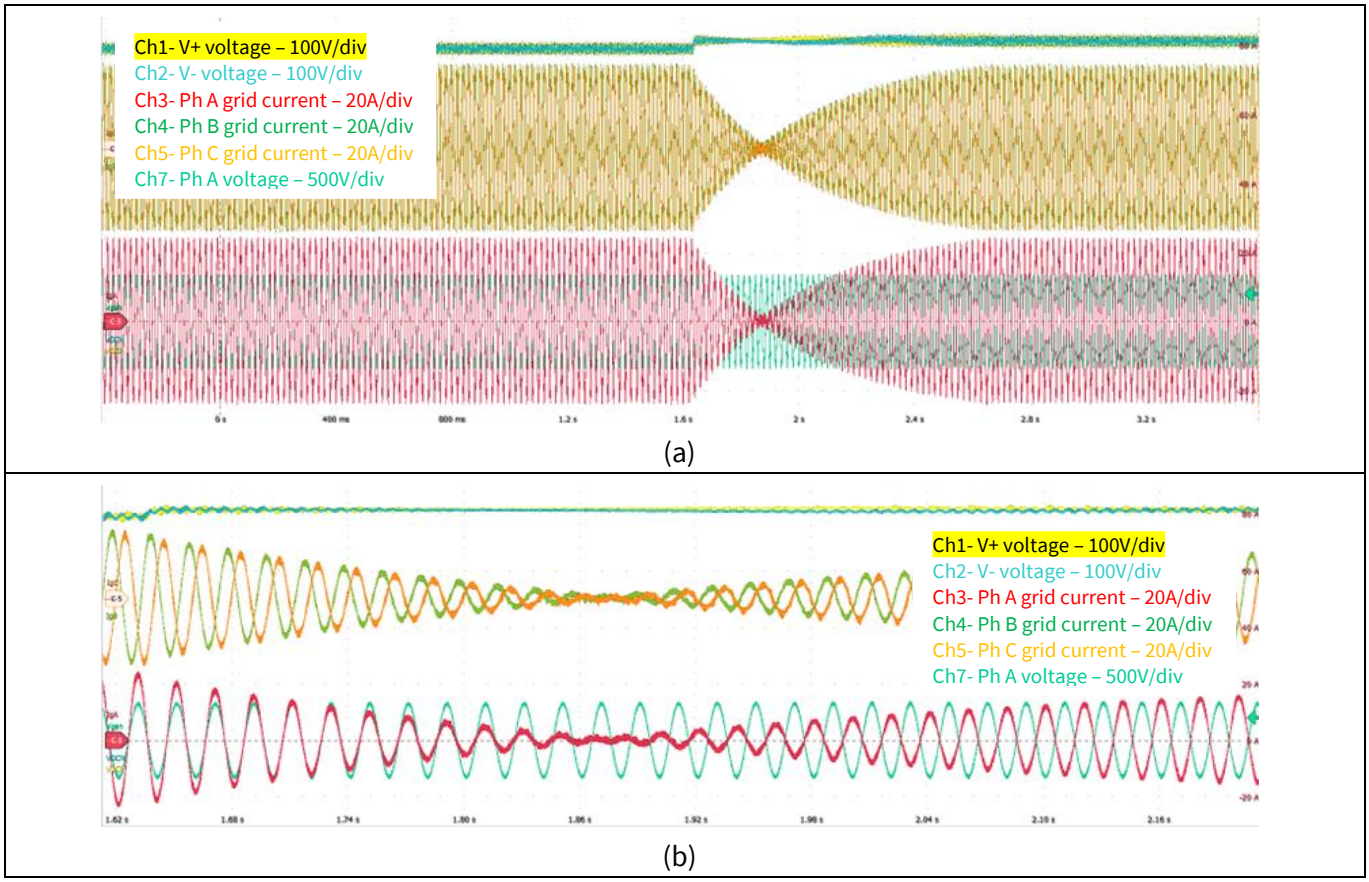
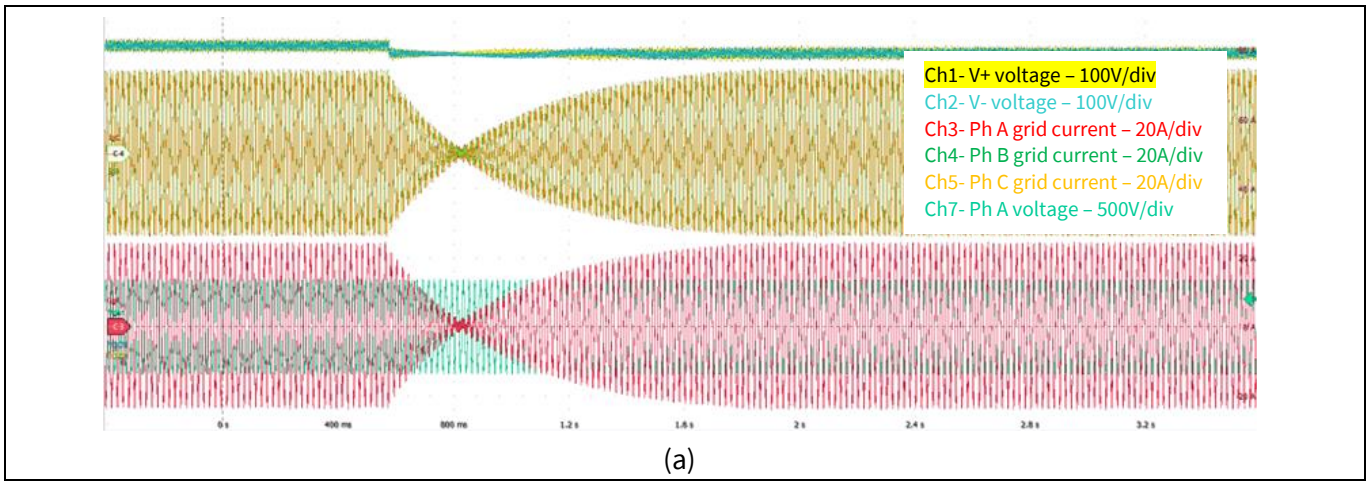
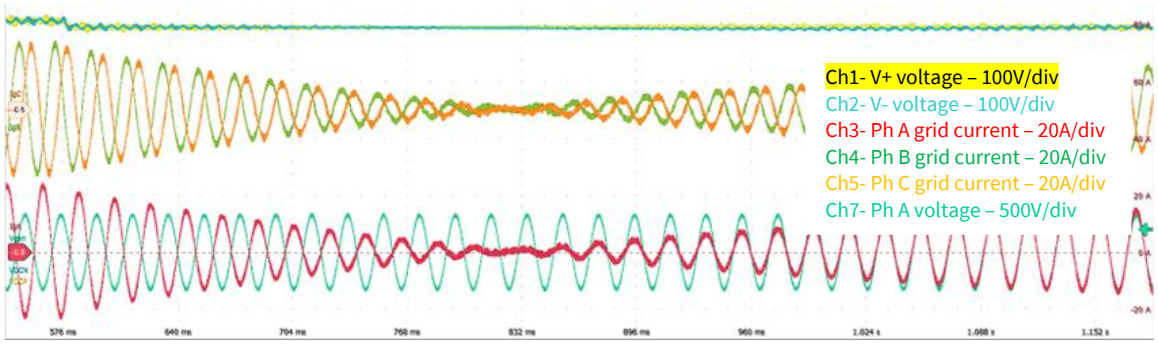


Figure 66 Three-phase bidirectional power-flow transition: full-power 11 kW PFC mode to full-power 11 kW inverter mode– under 230 V_{AC} line-to-neutral voltage. (a) Full time-scale view; (b) Zoom-in view

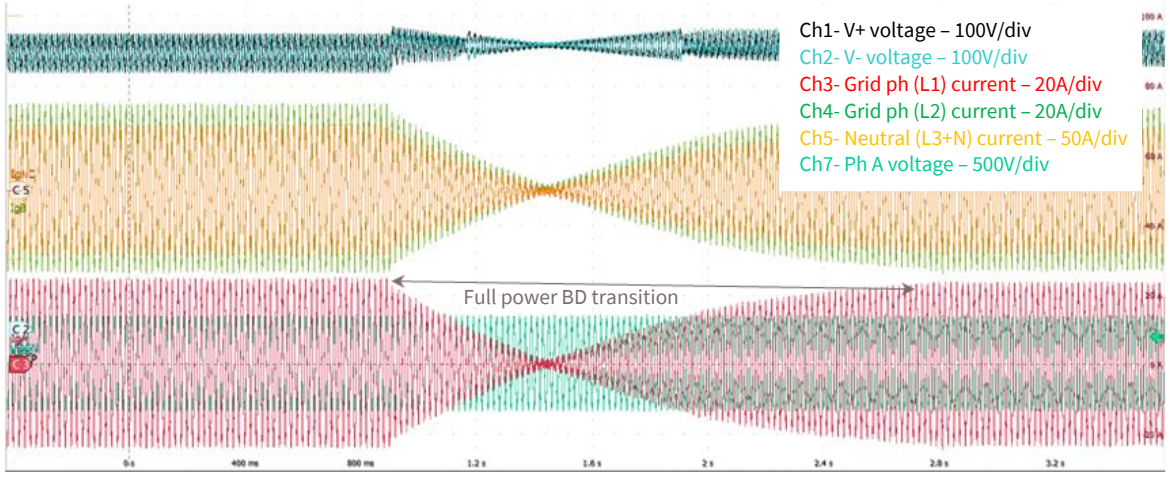




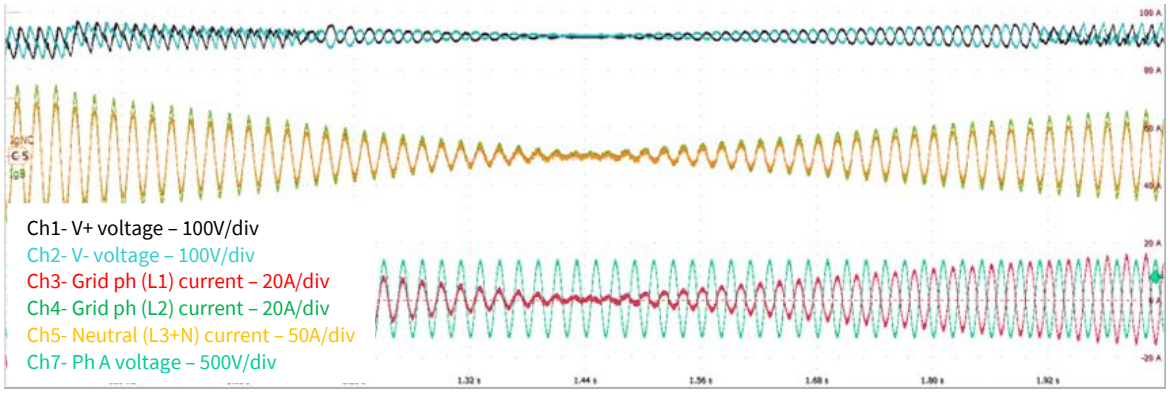
(b)

Figure 67 Three-phase bidirectional power-flow transition: full-power 11 kW inverter mode to full-power 11 kW PFC mode– under 230 V_{AC} line-to-neutral voltage. (a) Full time-scale view; (b) Zoom-in view

Moreover, the test waveforms of single-phase bidirectional transitions from PFC mode to inverter mode, as well as from inverter mode to PFC mode are shown in Figure 68 and Figure 69, respectively. The maximum time for full-power operating mode transition is less than 2 s, with bidirectional changeover happens in less than five full cycles of AC voltage. The grid currents maintain good quality even during the transition. It can also be observed that the two split capacitor voltages are well regulated and balanced during the transition. The operation of phase-leg C as power pulsation buffer is controlled independently than the grid current regulation, and it is activated and deactivated automatically based on the operational power level.

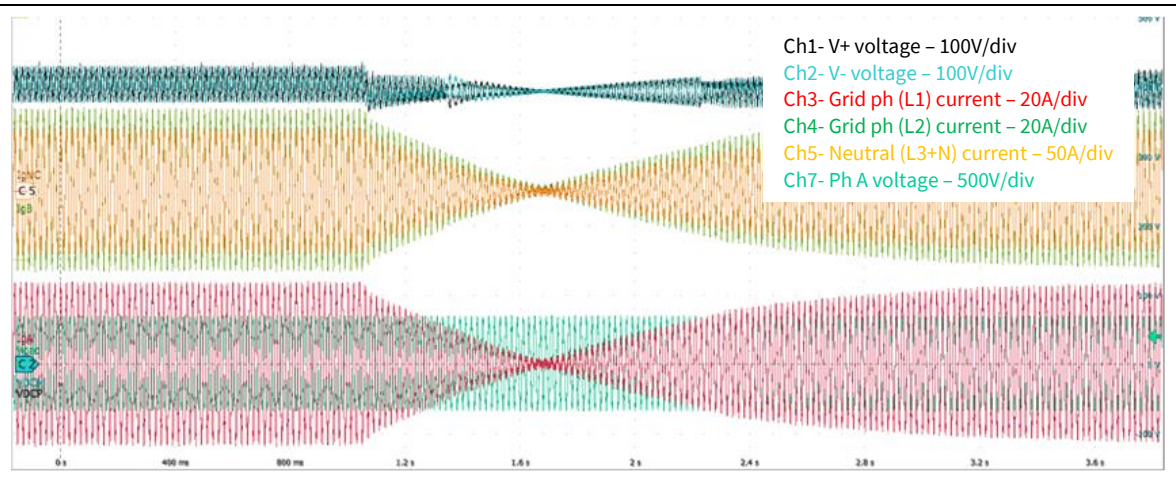


(a)

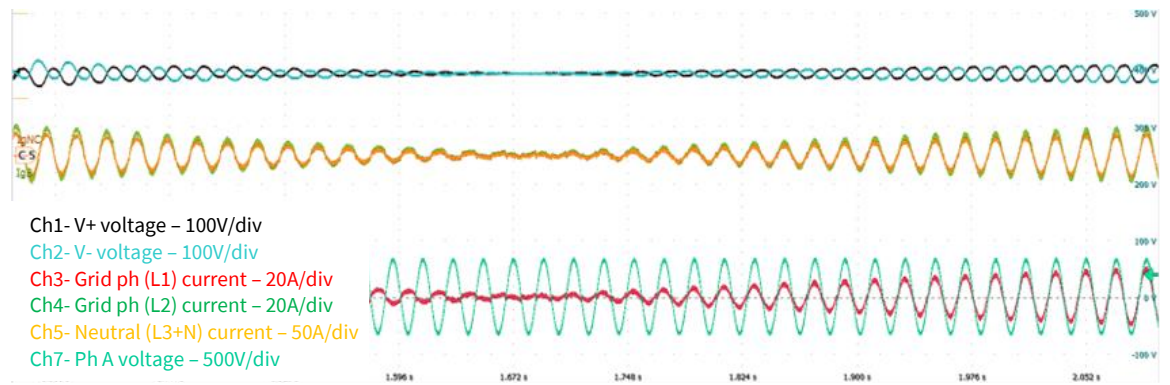


(b)

Figure 68 Single-phase bidirectional power-flow transition: full-power 7.3 kW PFC mode to full-power 7.3 kW inverter mode– under 230 V_{AC} line-to-neutral voltage. (a) Full time-scale view; (b) Zoom-in



(a)



(b)

Figure 69 Single-phase bidirectional power-flow transition: full-power 7.3 kW inverter mode to full-power 7.3 kW PFC mode under 230 V_{AC} line-to-neutral voltage. (a) Full time-scale view; (b) Zoom-in

5.4.2 Load transients

To demonstrate the control stability of REF_11KW_PFC_SIC_QD, load step tests are performed. Figure 70 (a) and Figure 70 (b) show the waveform during three-phase PFC mode load transient tests, i.e., from full load to half load and from full load to no load.

In Figure 70 (a), following the transient condition, the split bulk capacitor voltages see maximum overshoot of 30 V and fully recover to the target value within four mains cycles. In Figure 70 (b), when jumping from full load to noload, higher voltage overshoorts occurr and REF_11KW_PFC_SIC_QD switches into protection mode to prevent damage of bulk capacitors. The PWM signals are stopped and awaits the bulk capacitor voltages to fall into the control range.

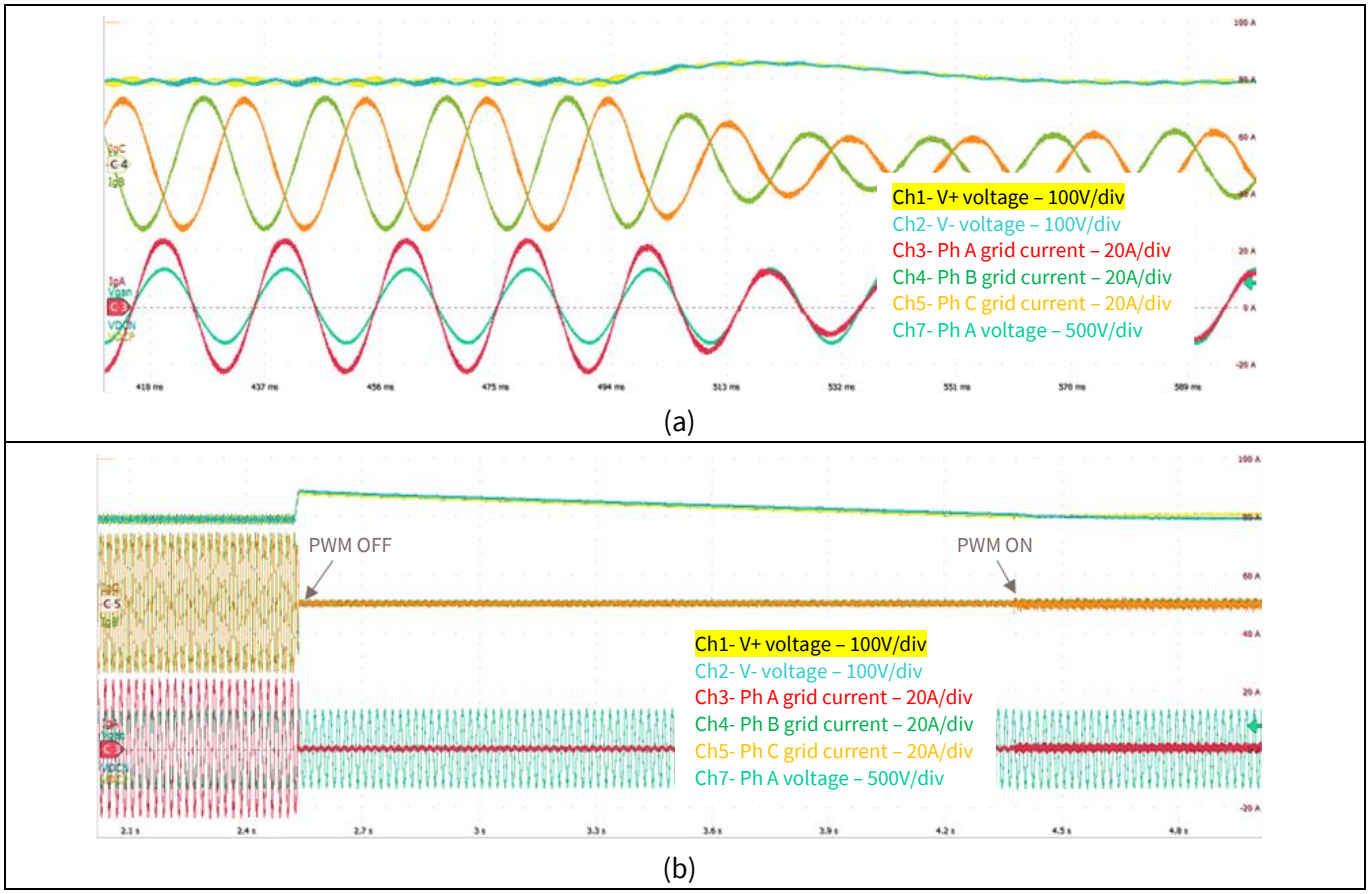


Figure 70 Three-phase PFC mode load transient. (a) Full-load 11 kW to half-load 5.5 kW; (b) Full-load 11 kW to no-load 0 kW

Figure 71 (a) and Figure 71 (b) give the three-phase PFC mode load jump test results during half- to full-load and no- to full-load conditions. It can be concluded that REF_11KW_PFC_SIC_QD can handle these conditions without signifcant output voltage deviation as well as obvious stability issue.

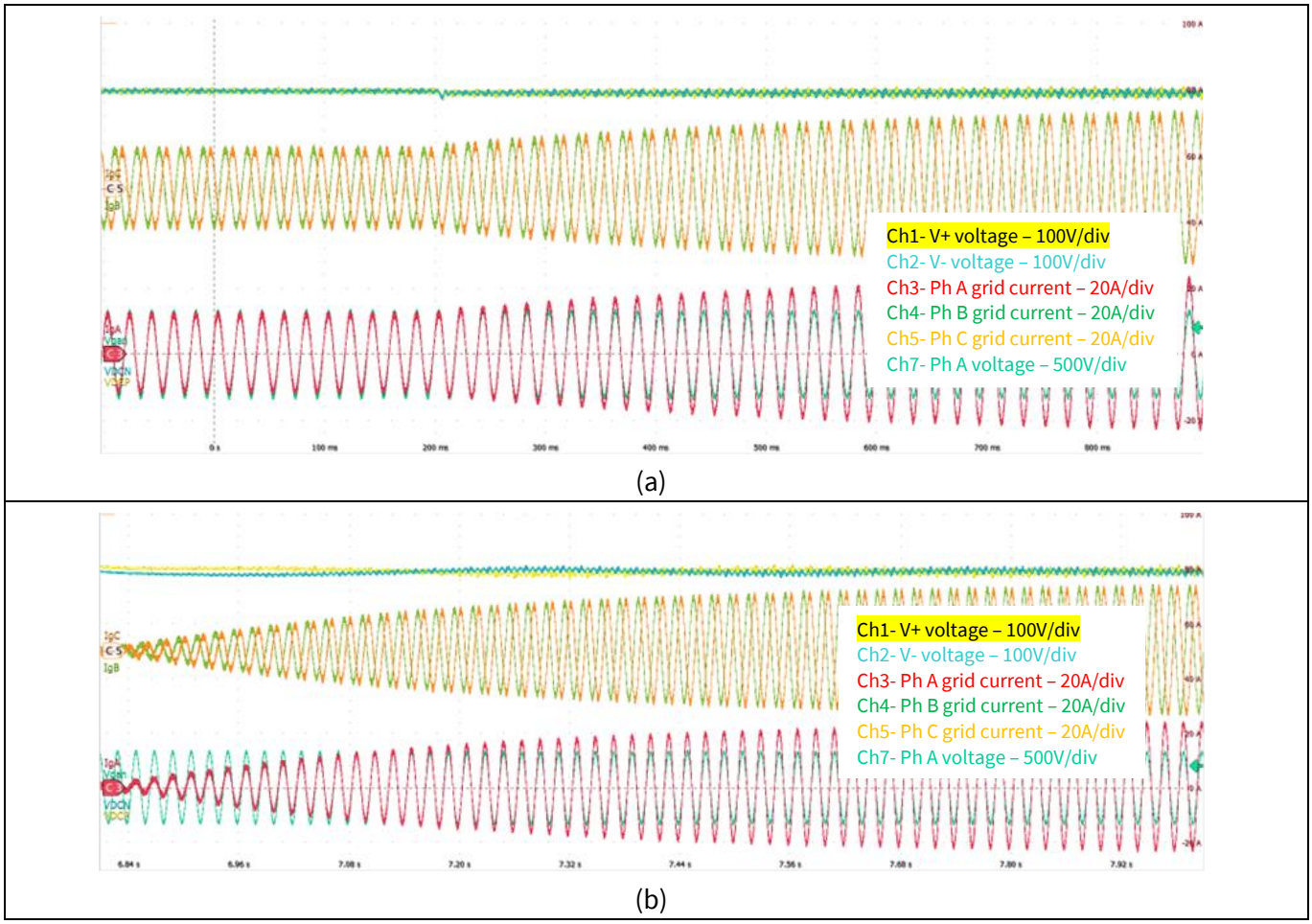


Figure 71 Three-phase PFC mode load transient. (a) Half-load 5.5 kW to full-load 11 kW; (b) No-load 0 kW to full-load 11 kW

Regarding single-phase transient performance during load jump, Figure 72 (a) and Figure 72 (b) demonstrates the transient waveforms captured during no-load to full-load and full-load to no-load transient, respectively. The load level is controlled with the bidirectional supply. In the first case in Figure 72 (a), the transition shows smooth behavior. In the second test case in Figure 72 (b), due to the sudden lost of load, the split bulk capacitor voltage rises sharply which triggers the over-voltage protection and stops the PWM signals to prevent the damage of capcitor. The PWM signals are re-activated when the split bulk capacitor voltages fall below 400 V due to self-discharge.

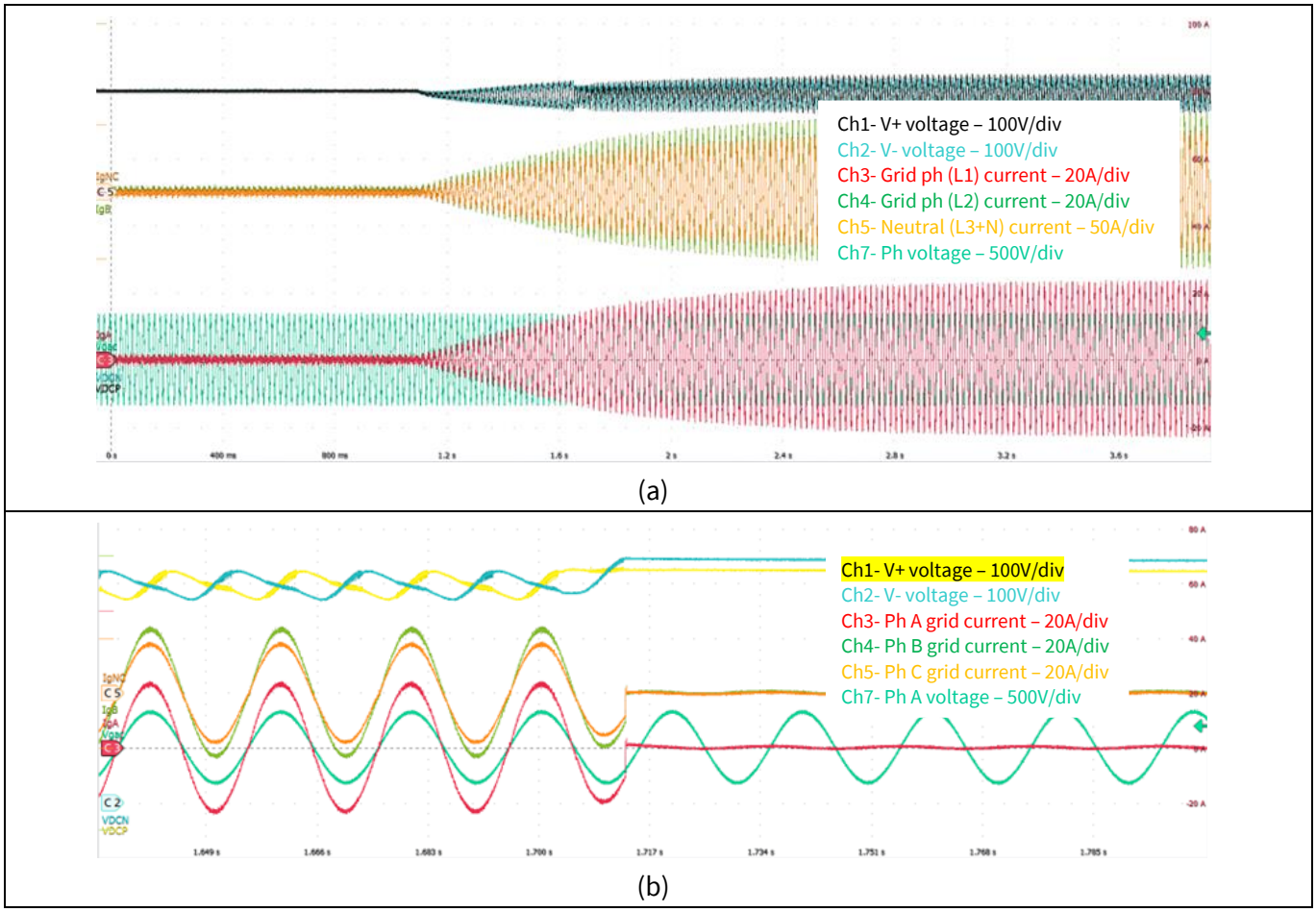


Figure 72 Single-phase PFC mode load transient. (a) No-load 0 kW to full-load 7.3 kW; (b) Full-load 7.3 kW to no-load 0 kW

These load jump tests demonstrate the ability and reliability of REF_11KW_PFC_SIC_QD to handle sudden changes in load current and maintain a well-regulated output. These smooth transitions in the current transient response corresponding to load jumps demonstrate the current loop stability of the design.

5.5 Thermal performance

The converter has been thermally characterized by operating it at full load for 30 minutes under nominal voltage of 230 V_{AC} in both three-phase and single-phase AC supply configurations. The thermal behavior is shown in Figure 73, which provides a detailed hotpsot overview of the converter such as inductors, CoolSiC™ Q-DPAK mold compound on bottom side. All temperatures are measured with thermal camera with the chassis open, under thermal equilibrium status at 24 °C ambient temperature.

Furthermore, Figure 74 shows temperatures profiles of main components (case temperature of CoolSiC™, inductor core temperature, heatsink temperature) in relation to the output power drawn from the board. J-type thermocouples are used to record these thermal measurements with the chasis closed. From the temperature profiles, REF_11KW_PFC_SIC_QD can operate at all ranges of AC input voltages specified in specifications with a maximum temperature of nearly 90°C on CoolSiC™ MOSFETs case and 100°C on Inductors, with a 500 mW fan blowing towards the back-side of heatsink.

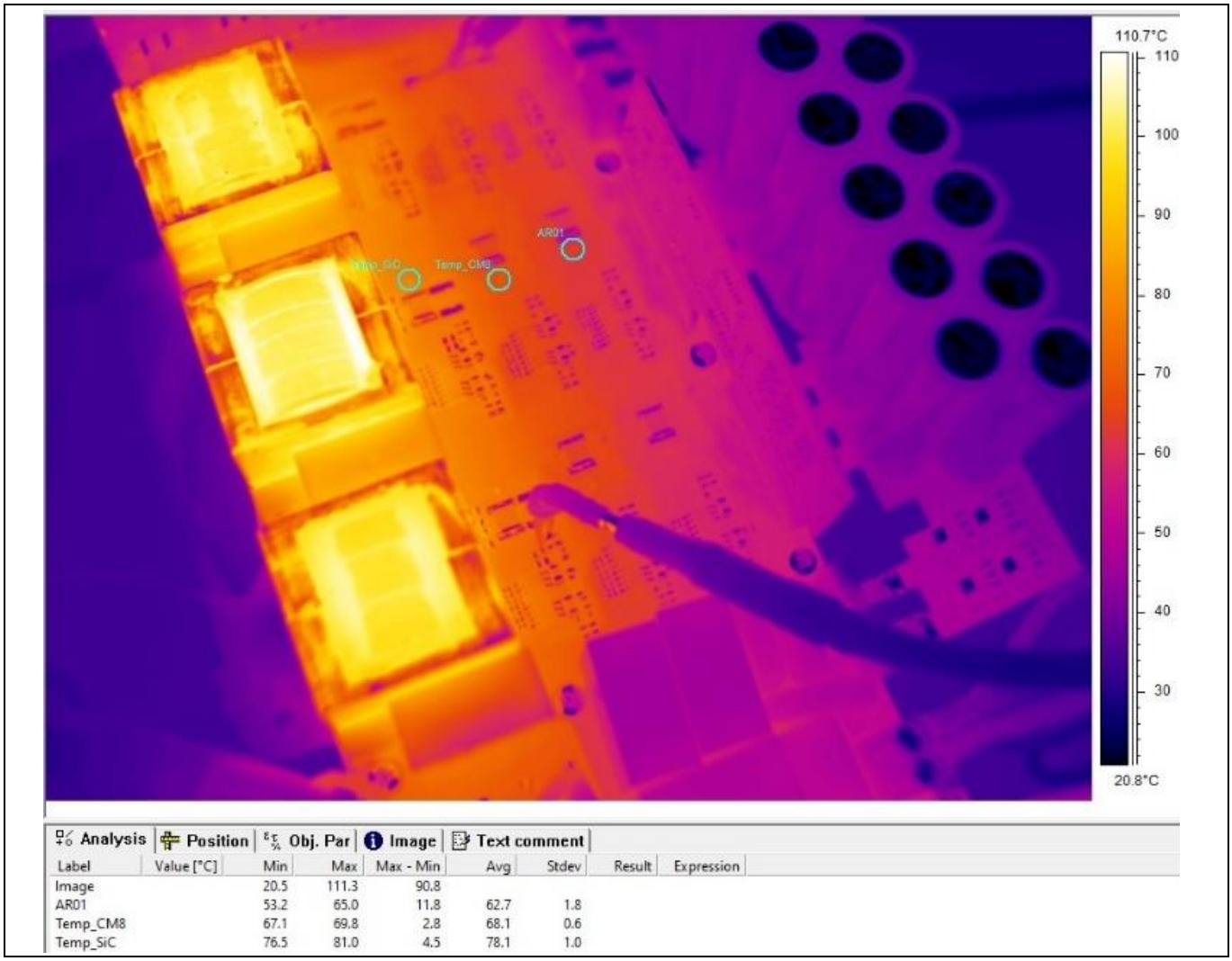


Figure 73 Thermal image captured during three-phase full power long-term testing

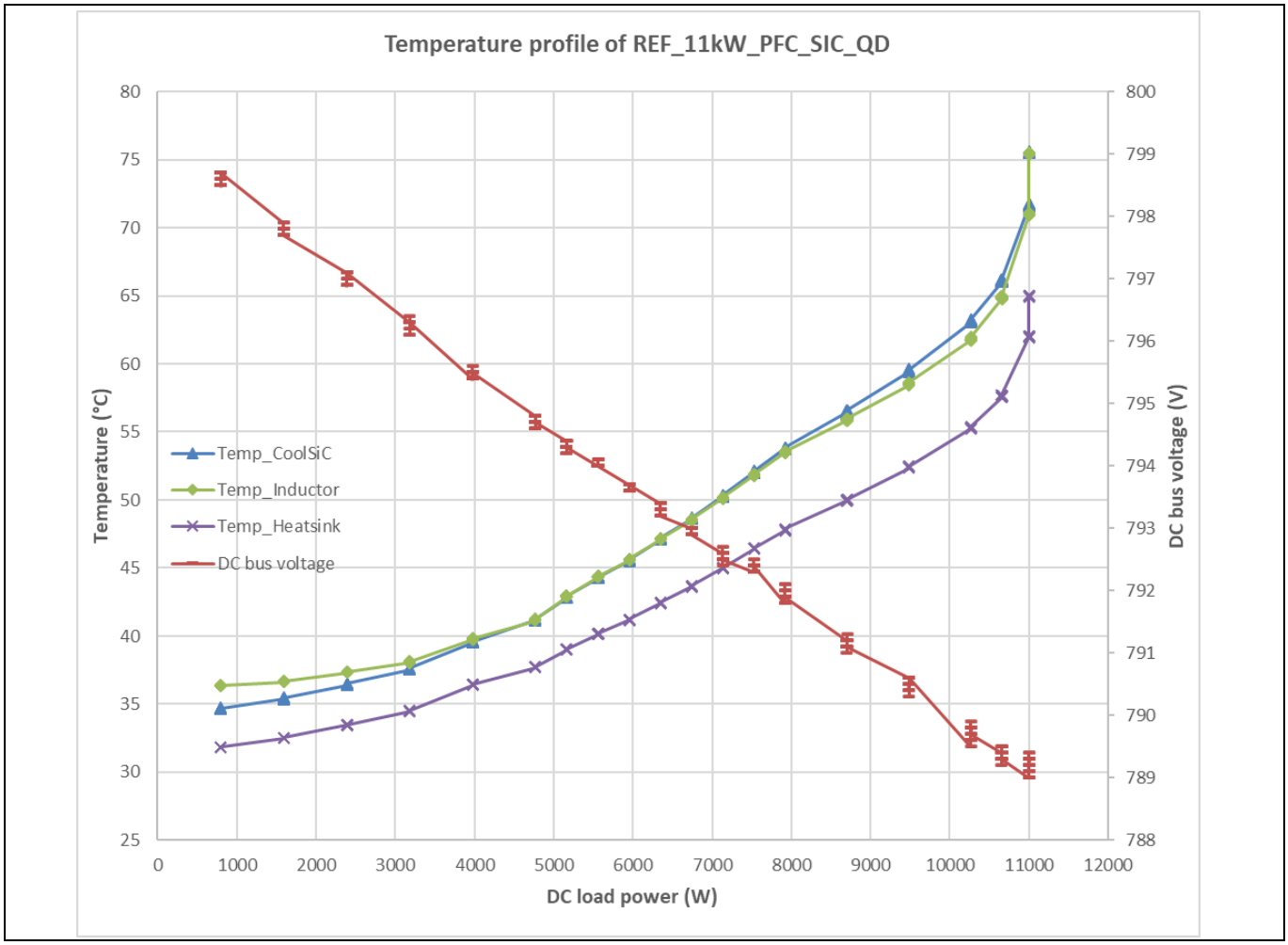


Figure 74 Temperature profile dependent on output power with the chasis closed

6 Summary

This application note provides a front-end/first-stage system solution from Infineon designed for EV-charging/OBC, and energy storage system applications.

The system incorporates three-level active neutral point clamped ACDC bidirectional converter, achieving a peak efficiency of 99.15% and 98.95% in three-phase PFC rectifier mode and inverter mode respectively. When the converter is connected to single phase AC mains, the efficiency achieved is 98.95% in PFC rectifier mode and 98.95% in inverter mode. The efficiency results are obtained with the highest form factor/power density of 11.5kW/L.

The REF_11kW_PFC_SiC_QD reference board is designed with Infineon's CoolSIC™ 750 V, CoolSIC™ 650 V and CoolMOS™ 600V power MOSFETs in QDPAK packages; EiceDRIVER™ 2EDB9259Y dual-channel isolated gate driver IC in 150mil DSO-14 package, XENSIV™ TLE4971 current sensor in 8x8 mm package and digital control through XMC4400 enable high performance within a compact form factor.

The outstanding performance shown by the steady-state tests of REF_11KW_PFC_SIC_QD is complemented by the robustness and reliability of dynamic loading operation as well as bidirectional power flow operation. These features are demonstrated by load transients and bidirectional transition events which shows the converter robust operation as well as fault toleranct capabilities.

7 Schematics

7.1 Main board

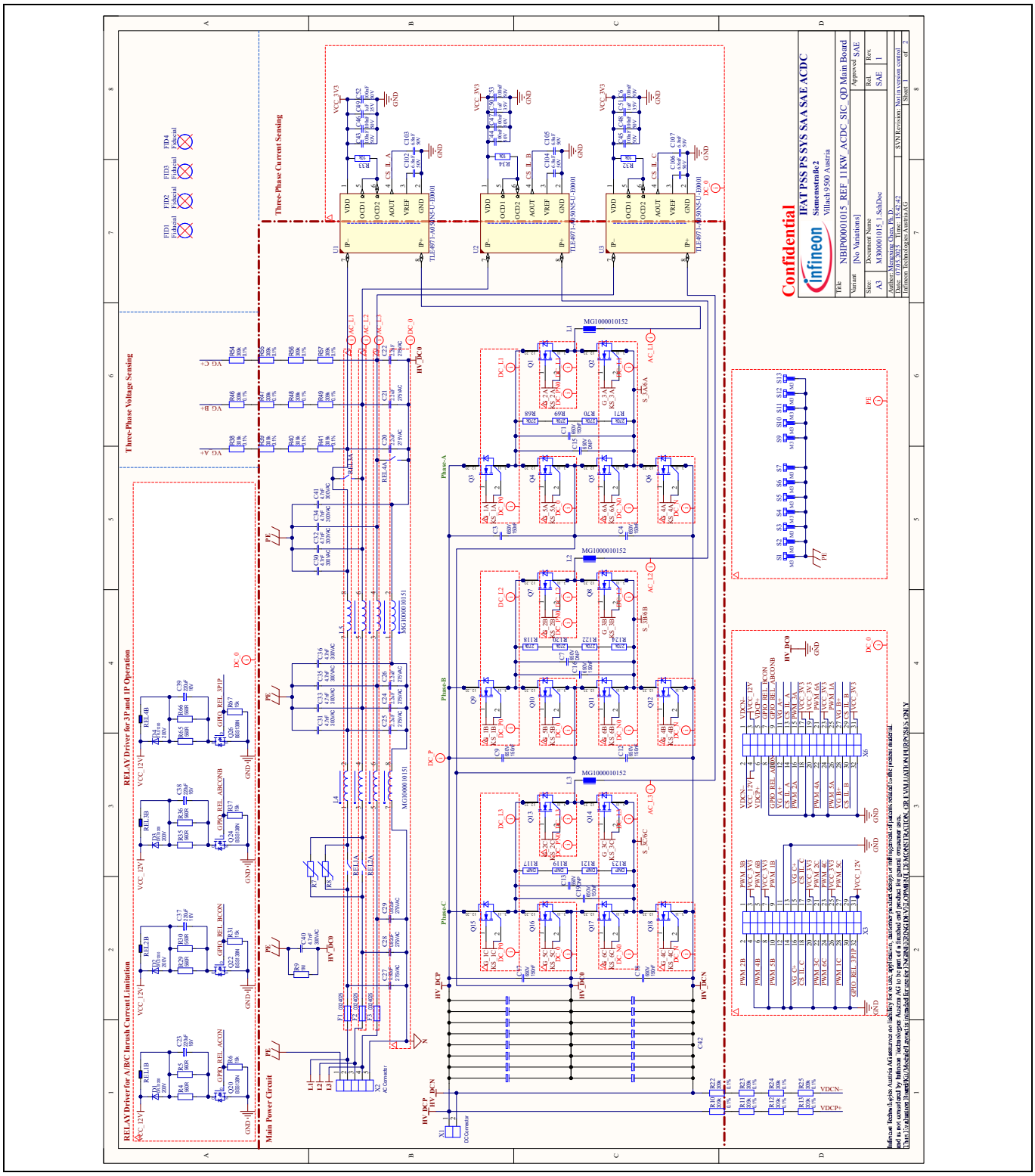


Figure 75 Power stage

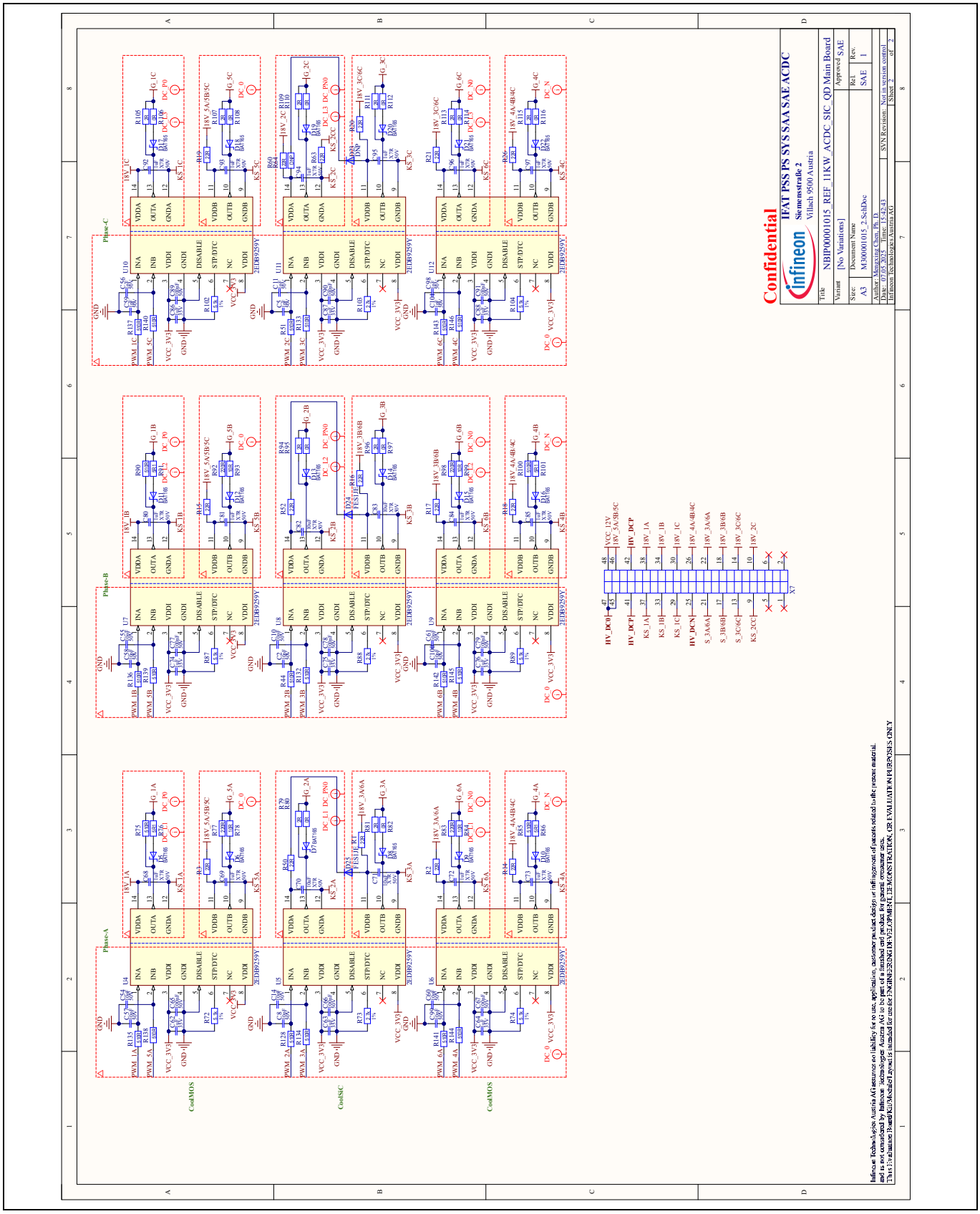


Figure 76 Gate driving

7.2 Daughter cards

7.2.1 Capacitor card

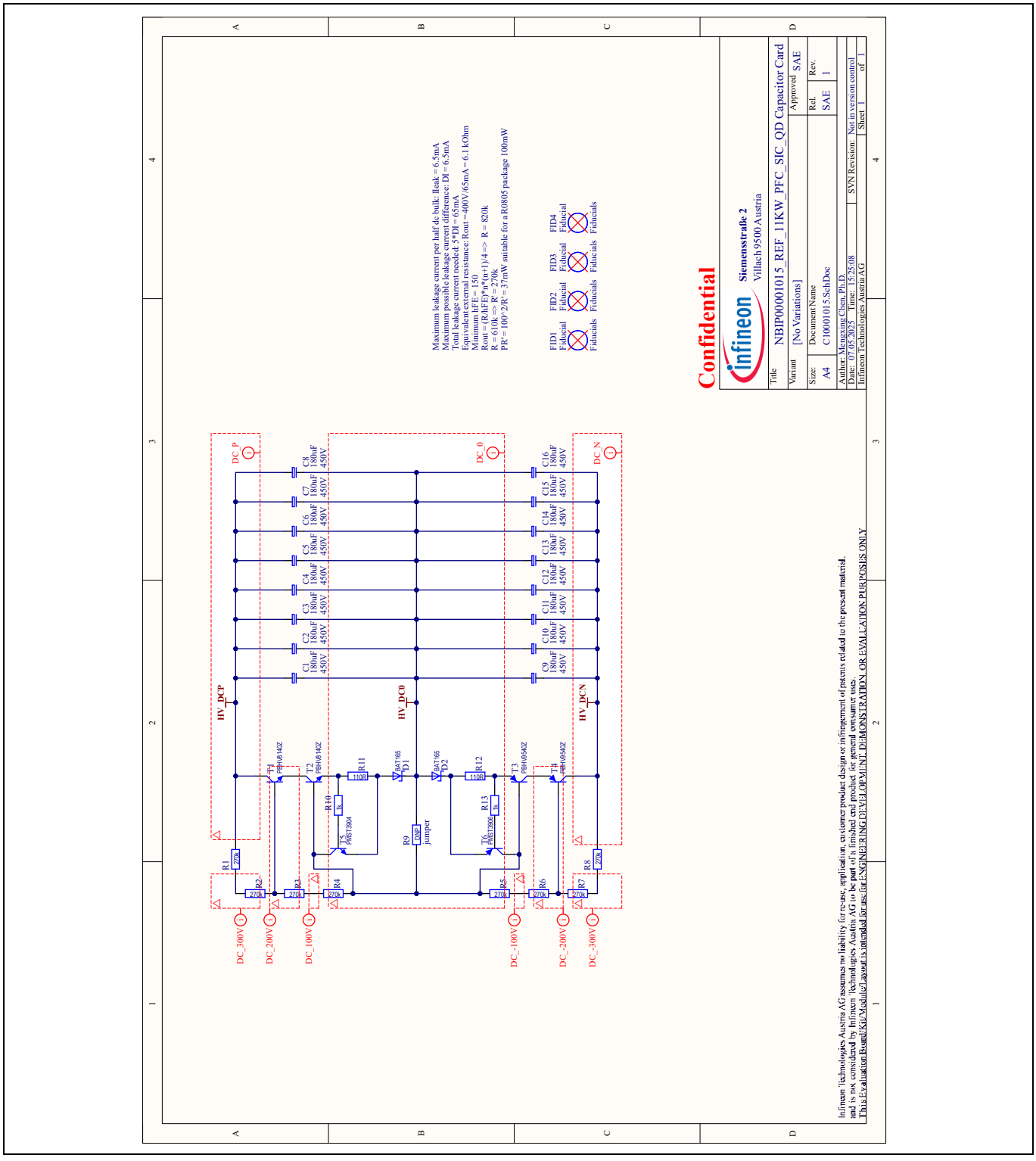


Figure 77 Capacitor board

7.2.2 Auxiliary power supply card

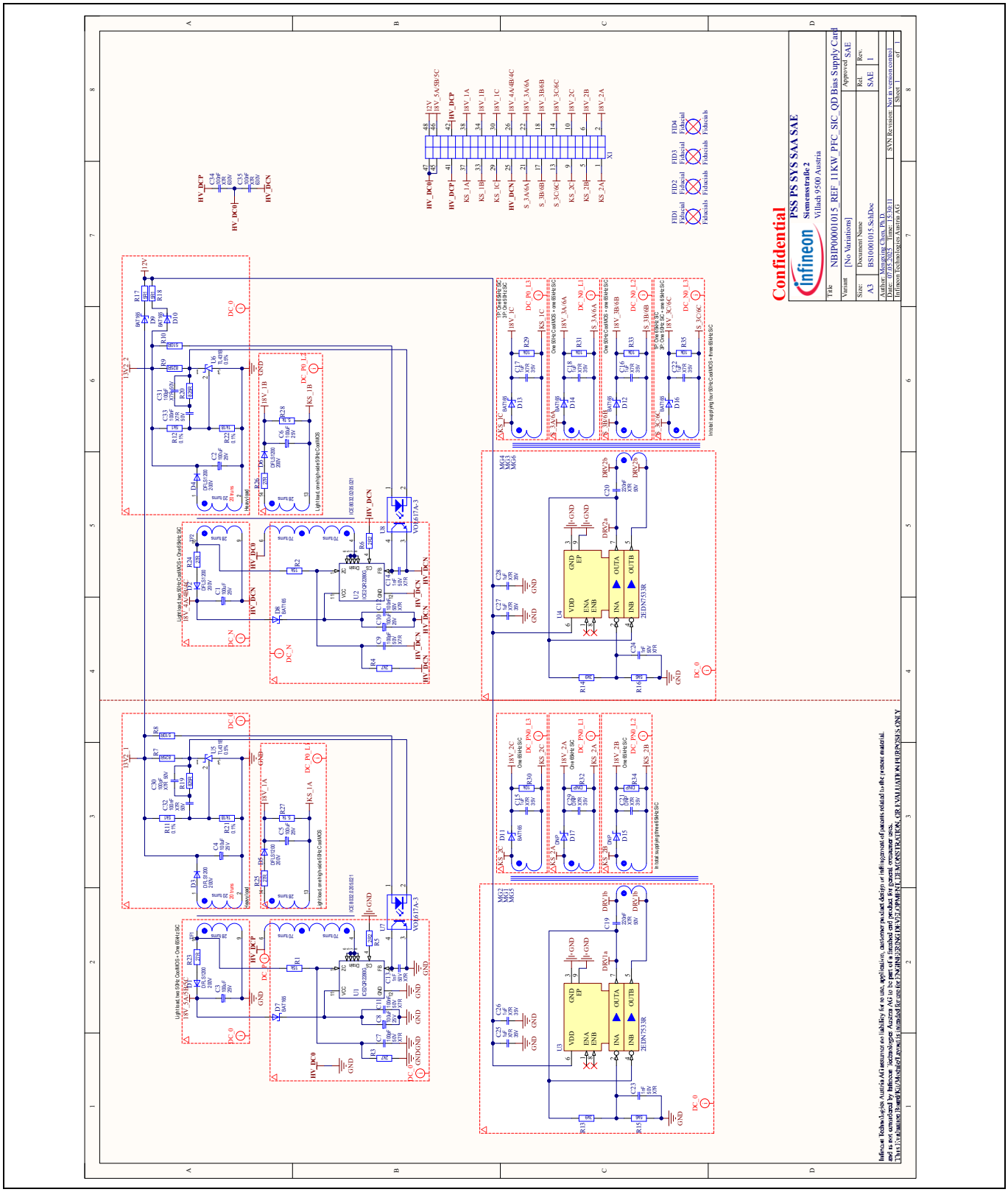


Figure 78 Auxiliary power supply card

7.2.3 Control card

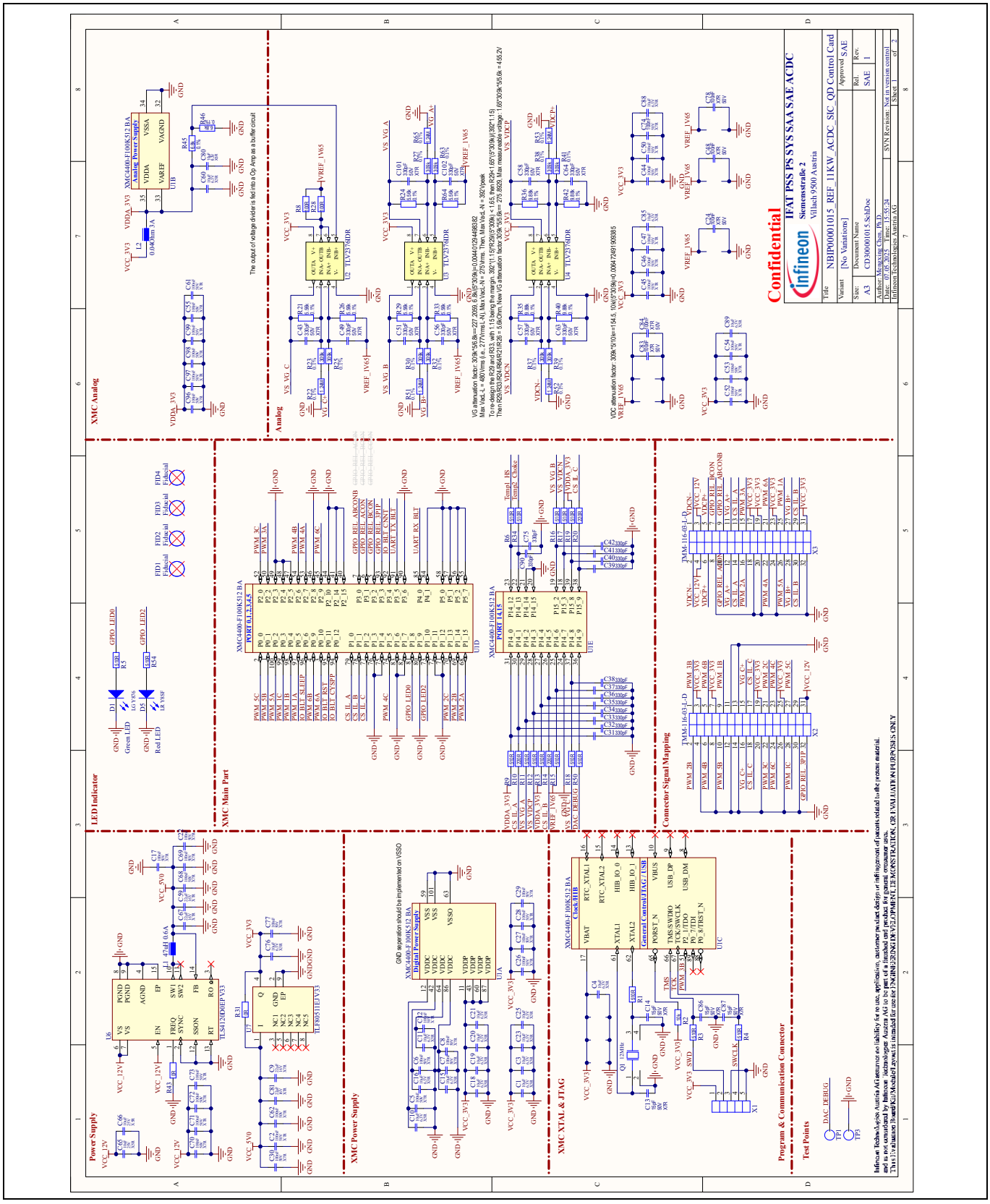


Figure 79 Control card

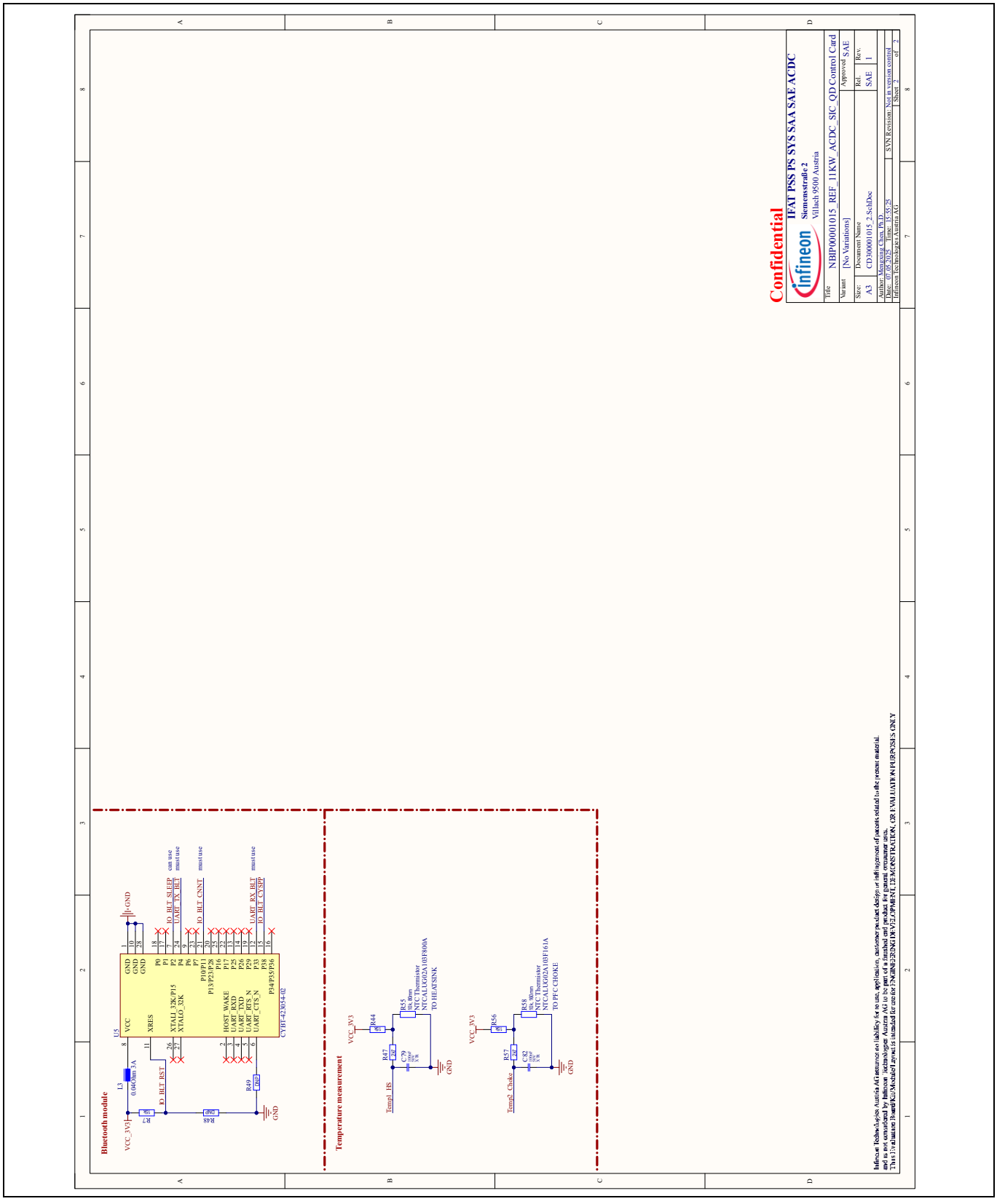


Figure 80 Control card (continued)

8 Bill of Materials

Table 2 Main board

Designator	Value	Tolerance	Voltage	Description
R28, R45, R125, R126, R130, R131	0R	1%	75V	Resistor
R80, R82, R95, R97, R110, R112	0R	1%	150V	Resistor
C27, C28, C29	0.82uF	20%	275VAC	Capacitor Foil
C49, C50, C51, C62, C63, C64, C74, C75, C76, C86, C87, C88	1uF	X7R	35V	Capacitor Unpolarized
C68, C69, C72, C73, C80, C81, C84, C85, C92, C93, C94, C95, C96, C97	1uF	X7R	50V	Capacitor Unpolarized
U4, U5, U6, U7, U8, U9, U10, U11, U12	**2EDB9259Y**	–	–	**Dual-channel isolated gate driver ICs**
R79, R81, R94, R96, R109, R111	2R	1%	150V	Resistor
C20, C21, C22, C24, C25, C26	2.2uF	20%	275VAC	Capacitor Unpolarized
R73, R88, R103	2.7k	1%	75V	Resistor
C30, C31, C32, C33, C34, C35, C36, C40, C41	4.7nF	20%	300VAC	Capacitor Unpolarized
C70, C82	4.7uF	X7R	50V	Capacitor Unpolarized
R76, R86, R91, R101, R105, R106, R107, R108, R113, R114, R115, R116	5R1	1%	150V	Resistor
R72, R74, R87, R89, R102, R104	5.1k	1%	75V	Resistor
R32, R33, R34	10k	1%	75V	Resistor
R78, R84, R93, R99	10R	1%	150V	Resistor
C71, C83	10uF	X7R	50V	Capacitor Unpolarized
R6, R31, R37, R67	15k	1%	75V	Resistor
R1, R2, R3, R14, R15, R16, R17, R18, R19, R20, R21, R26, R58, R59, R60, R61, R62, R63	22R	1%	150V	Resistor
R50, R52	27R	1%	150V	Resistor
C6, C43, C44, C45, C46, C47, C48, C52, C53, C65, C66, C67, C77, C78, C79, C89, C90, C91	100nF	X7R	50V	Capacitor Unpolarized
C2, C5, C8, C10, C11, C14, C54, C55, C56, C57, C58, C59, C60, C61, C98, C99, C100, C101	100pF	X7R	50V	Capacitor Unpolarized
C23, C37, C38, C39	100uF	20%	25V	Capacitor Polarized

Bill of Materials

Designator	Value	Tolerance	Voltage	Description
C1, C3, C4, C9, C12, C16, C17, C18, C19	150nF		650V	Capacitor Unpolarized
R77, R83, R92, R98	220R	1%	150V	Resistor
R68, R69, R70, R71, R117, R118, R119, R120, R121, R122, R123, R124	270k	1%	150V	Resistor
R10, R11, R12, R13, R22, R23, R24, R25, R38, R39, R40, R41, R46, R47, R48, R49, R54, R55, R56, R57	309k	0,10%	150V	Resistor
R75, R85, R90, R100	510R	1%	150V	Resistor
R44, R51, R128, R132, R133, R134, R135, R136, R137, R138, R139, R140, R141, R142, R143, R144, R145, R146	510R	1%	75V	Resistor
R4, R5, R29, R30, R35, R36, R65, R66	820R	1%	200V	Resistor
F1, F2, F3	32402500%	–	–	Fuse
X2	1713985	–	–	Pin Header, 5 Contacts
X1	171495500%	–	–	Pin Header, 2 Contacts
D5, D6, D7, D8, D9, D10, D11, D12, D13, D14, D15, D16, D17, D18, D19, D20, D21, D22	**BAT165**	–	**40V**	**Schottky-Diode**
Q20, Q22, Q24, Q26	**BSS138N**	–	**60V**	**MOSFET**
C42	C200001015	–	800V	16*180uF
D1, D2, D3, D4	DFLS1200	–	200V	Diode
D23	DNP	–	–	REVERSE VOLTAGE 600 Volts FORWARD CURRENT
R64	DNP	1%	150V	Resistor
C7, C13, C15	DNP	–	650V	Capacitor Unpolarized
U1, U2, U3	DNP	–	–	400 kHz, High Accuracy Current Sensor with Pin-Selectable Gains
R27, R42, R43, R53, R127, R129	DNP	1%	75V	Resistor
D24, D25	FES1JE	–	–	REVERSE VOLTAGE 600 Volts FORWARD CURRENT
REL1, REL2, REL3, REL4	G2RL-1A-E2-CV-HA DC12	–	–	Relay

Designator	Value	Tolerance	Voltage	Description
Q15, Q16, Q17, Q18	**IMDQ65R020M2H**	–	–	**N-Channel MOSFET, QDPAK**
Q1, Q2, Q7, Q8, Q13, Q14	**IMDQ75R025M2H**	–	–	**N-Channel MOSFET, QDPAK**
Q3, Q4, Q5, Q6, Q9, Q10, Q11, Q12	**IPDQ60R016CM8**	–	–	**N-Channel MOSFET, QDPAK**
S1, S2, S3, S4, S5, S6, S7, S9, S10, S11, S12, S13	M3	–	–	Screw
L4, L5	MG1000010151	–	–	CM choke 3 phase 4 winding
L1, L2, L3	MG2000010151	–	–	Inductor
R7, R8, R9	SL22 47003	25%	–	Resistor NTC
X3, X6	SQT-116-01-F-D	–	–	Pin Header, 2x16 Contacts
X7	SQT-124-01-F-D	–	–	Pin Header, 2x24 Contacts, 4mm Pitch

Table 3 Capacitor card

Designator	Value	Tolerance	Voltage	Description
R10, R13	1k	1%	150V	Resistor
R11, R12	110R	1%	150V	Resistor
C1, C2, C3, C4, C5, C6, C7, C8, C9, C10, C11, C12, C13, C14, C15, C16	180uF	20%	450V	Capacitor Polarized
R1, R2, R3, R4, R5, R6, R7, R8	270k	1%	150V	Resistor
D1, D2	**BAT165**	–	**40V**	**Schottky-Diode**
T1, T2	PBHV8140Z	–	–	NPN-Transistor
T3, T4	PBHV9540Z	–	–	PNP-Transistor
T5	PMST3904	–	–	NPN-Transistor
T6	PMST3906	–	–	PNP-Transistor

Table 4 Auxillary supply card

Designator	Value	Tolerance	Voltage	Description
R21, R22	1k18	0,10%	75V	Resistor
C13, C14, C23, C24	1nF	X7R	50V	Capacitor Unpolarized
C15, C16, C17, C18, C21, C22, C25, C26, C27, C28, C29	1uF	X7R	35V	Capacitor Unpolarized
U3, U4	**2EDN7533R**	–	–	**Driver**
R3, R4	2k7	1%	75V	Resistor

Bill of Materials

Designator	Value	Tolerance	Voltage	Description
R5, R6	2R2	1%	200V	Resistor
R13, R14	3k9	1%	75V	Resistor
R11, R12	5k1	0,10%	75V	Resistor
R15, R16	5k6	1%	75V	Resistor
R17, R18	5R1	1%	200V	Resistor
R27, R28	5.1k	1%	200V	Resistor
R29, R30, R31, R32, R33, R34, R35	10k	1%	75V	Resistor
R1, R2	15k	1%	75V	Resistor
R23, R24, R25, R26	27R	1%	75V	Resistor
C34, C35	100nF	X7R	630V	Capacitor Unpolarized
C11, C12, C32, C33	100nF	X7R	50V	Capacitor Unpolarized
C7, C9, C30, C31	100pF	X7R	50V	Capacitor Unpolarized
C1, C2, C3, C4, C5, C6, C8, C10	100uF	20%	25V	Capacitor Polarized
C19, C20	220nF	X7R	50V	Capacitor Unpolarized
R8, R10	510R	1%	75V	Resistor
R7, R9, R19, R20	825R	1%	75V	Resistor
MG5, MG6	B66453K0000X149	–	–	Magnetic cores
MG1, MG3	B66480G0000X149	–	–	Magnetic cores
D7, D8, D9, D10, D11, D12, D13, D14, D15, D16, D17	**BAT165**	–	**40V**	**Schottky-Diode**
MG2, MG4	CLM-E18/PLT18	–	–	Clamp for ER18 I18
D1, D2, D3, D4, D5, D6	DFLS1200	–	–	Diode
U1, U2	**ICE2QR2280G**	–	–	**Off-Line SMPS Quasi-Resonant PWM Controller**
TF1, TF2	ICE 8032.0205.021	–	–	Transformer
U5, U6	TL431B	0,50%	–	–
X1	TMM-124-03-T-D	–	–	Pin Header, 2x24 Contacts, 4mm Pitch
U7, U8	VOL617A-3	–	–	Integrated Circuit

Table 5 Control card

Designator	Value	Value	Voltage	Description
R31	0R	0R	75V	Resistor
R43	0R	0R	75V	Resistor
L2, L3	0.04Ohm 3A	0.04Ohm 3A	–	Ferrite beads, 3A, 0.04Ohm @ DC, 60Ohm @ 100MHz
R22, R51, R52, R53, R65	1.24M	1.24M	150V	Resistor
R47, R57	2k7	2k7	75V	Resistor
R21, R24, R26, R29, R33, R64	5.56k	5.56k	75V	Resistor
R45, R46	6.8k	6.8k	75V	Resistor
R35, R36, R40, R42	9.88k	9.88k	75V	Resistor
C1, C3, C4, C10, C11, C15, C16, C18, C19, C20, C21, C23, C25, C60, C76, C80, C85, C88, C89	10µF	10µF	6.3V	Capacitor Unpolarized
R2	10k	10k	75V	Resistor
R55	10k, 80mm	10k, 80mm	–	Resistor
R58	10k, 160mm	10k, 160mm	–	Resistor
C65, C66	10uF	10uF	25V	Capacitor Unpolarized
Q1	12MHz	12MHz	–	SMD Crystal Unit for Automotive Application, 12.000MHz
R44, R48, R49, R56	15k	15k	75V	Resistor
C13, C14, C86, C87	15pF	15pF	50V	Capacitor Unpolarized
C9, C59, C67, C81	22µF	22µF	16V	Capacitor Unpolarized
L1	47uH 0.6A	47uH 0.6A	–	WE-LQS SMD Power Inductor, size 2512, 47 uH, 0.6A
C2, C5, C6, C7, C8, C12, C17, C22, C24, C26, C27, C28, C29, C30, C44, C45, C46, C47, C48, C50, C52, C53, C54, C55, C61, C62, C68, C69, C70, C71, C72, C73, C74, C77, C78, C79, C82, C83, C84, C96, C97, C98, C99	100nF	100nF	50V	Capacitor Unpolarized
R8, R28	100R	100R	75V	Resistor
R23, R25, R27, R30, R32, R37, R38, R39, R41, R63	309k	309k	150V	Resistor

Bill of Materials

Designator	Value	Value	Voltage	Description
C31, C32, C33, C34, C35, C36, C37, C38, C39, C40, C41, C42, C43, C49, C51, C56, C57, C58, C63, C64, C75, C90, C101, C102	330pF	330pF	50V	Capacitor Unpolarized
R1, R3, R4, R5, R6, R9, R10, R11, R12, R13, R14, R15, R16, R17, R18, R19, R20, R34, R50, R54	510R	510R	75V	Resistor
U5	**CYBT-423054-02**	**CYBT-423054-02**	–	**EZ-BT WICED MODULE**
U1	**IFX_XMC4400-F100K512ABXUMA1**	**IFX_XMC4400-F100K512ABXUMA1**	–	**XMC4000 Family Microcontroller**
D1	LG Y876	LG Y876	–	LED
D5	LR Y8SF	LR Y8SF	–	LED
X1	MOLEX 53261-4005	MOLEX 53261-4005	–	Pin Header, 5 Contacts
U7	**TLF80511EJ V33**	**TLF80511EJ V33**	–	**Low Dropout Linear Fixed Voltage Regulator**
U6	**TLS4120D0EP V33**	**TLS4120D0EP V33**	–	**Synchronous Step-Down Regulator**
U2, U3, U4	TLV2376IDR	TLV2376IDR	–	Low-Noise, Low Quiescent Current, Precision Operational Amplifier
X2, X3	TMM-116-03-L-D	TMM-116-03-L-D	–	Pin Header, 2x16 Contacts

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