750 W FB-FB quarter-brick DC-DC converter for RFPA applications

-48 V to 50 V isolated digital power supply using XDPP1100

About this document

Scope and purpose

This document introduces a fully functional system solution developed by Infineon, for an isolated DC-DC converter targeting radio frequency power amplifier (RFPA) applications. The converter is made available in the form of a power module, following the industry-standard quarter-brick form factor. This converter is based on a full-bridge topology with full-bridge rectification (FB-FB), providing the required functional isolation. It can deliver up to 750 W output power while regulating +50 V output, from an input ranging from -60 V to -36 V. The converter shows high typical efficiency, up to 95.3 percent at full load at a nominal line of -48 V.

With the rollout of the fifth generation (5G) wireless communication, high-performance power supply units (PSUs) are required to support the demanding power requirements of the network equipment. High power density combined with high efficiency, fast dynamic response, flexibility to adjust output voltage, telemetry, and field upgrade capability are major features that are required besides the highest reliability. Infineon supports these needs by means of a wide portfolio of power discretes showing leading figures of merit (FOMs), other than advanced power management and driver ICs specifically targeting isolated and non-isolated DC-DC converters for telecom applications.

The reference design REF_750W_FBFB_50V includes the following parts from the Infineon product portfolio:

- The latest OptiMOS™ 6 80 V MOSFETs, 3.1 mΩ $R_{DS(on),max}$ (ISC031N08NM6) as primary-bridge switches
- OptiMOS™ 5 150 V, 11 mΩ $R_{DS(on),max}$ (BSC110N15NS5) as secondary-bridge synchronous rectifiers (SRs) and clamp MOSFETs
- EiceDRIVER™ dual-channel, functional isolated MOSFET gate driver (2EDF7275K) to drive primary FETs as well as SRs and active clamp FETs
- XDP™ integrated digital power controller with PMBus for isolated DC-DC power applications (XDPP1100) implementing advanced digital control and telemetry of the power stage

Intended audience

This application note is targeted at application engineers and designers of telecom power modules.

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1 Introduction

1.1 Background of the application

The next development stage of the mobile network is 5G. This new technology allows a significantly higher data capacity and extremely fast response times. This opens a completely new potential applications in an increasingly networked society. To support this, traditional architectures of mobile networks have changed dramatically, in both core network and radio access network (RAN).

Massive multiple input multiple output (MIMO) is one of the main enabling technologies behind 5G RAN. MIMO represents a method adopted for wireless communications using multiple antennas to transmit and receive signals. MIMO has already been exploited in 3G and 4G networks. With 5G, the concept is further developed, by using more antennas (organized in arrays) to exploit the advantages of multipath propagation. These include improved coverage (by means of advanced techniques such as beamforming, null forming and spatial multiplexing) and capacity (capability to handle traffic without compromising performance), finally translating to high user throughput.

In the first phase of the rollout, most of the cellular base stations (BTSs) will be operated at sub-6 GHz frequencies. Massive MIMO arrays at sub-6 GHz dictate the demand for small form factor, highly efficient power amplifiers (RFPAs) to be used. Form factor requirements directly translate into power density requirements. A typical way to increase output power in RPFAs is to increase the supply voltage. Silicon LDMOS technology dominated in RFPA designs for old wireless standards. The supply voltage is 28 V, which gives a good tradeoff between power and efficiency. Silicon LDMOS technology allows easy scaling to higher breakdown voltages by controlling the extension of the epitaxial drift region.

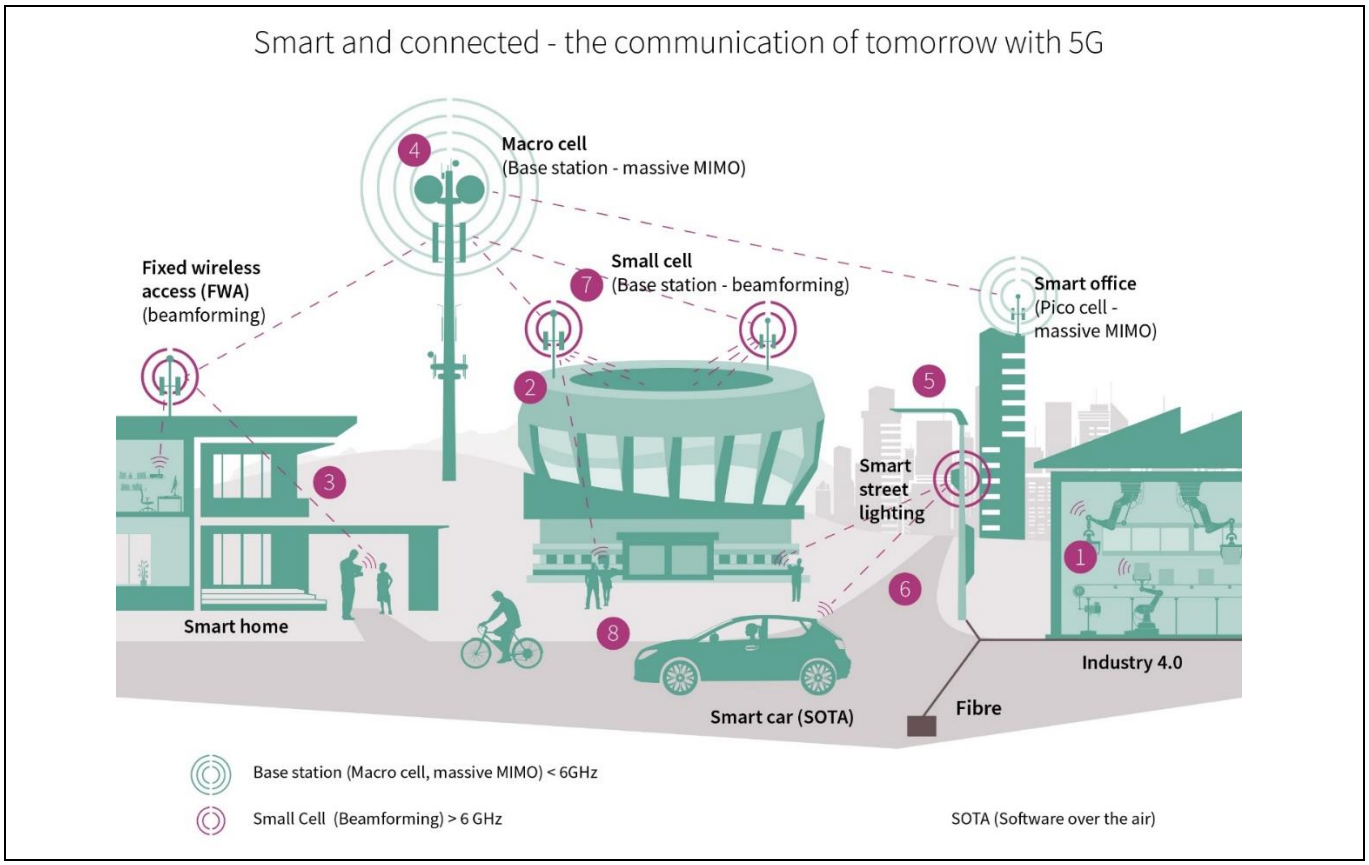


Figure 1 Possible cellular base station configurations conceived for 5G and different usage scenarios

Introduction

Silicon LDMOS solutions rated for 50 V supply enable doubling of the power density, at the expense of lower efficiency and reduced performance in terms of power gain cut-off frequency. These limit the application of 50 V silicon LDMOS RFPAs mostly to sub-GHz applications, which are not of interest for telecom radios. Furthermore, modulation schemes adopted in 5G lead to signals showing high peak-to-average power ratio (PAPR). This means that deep back-off power operation is needed to maintain linear operation of the amplifier. As a result, RFPAs will also need to be highly efficient when working far from the gain compression point.

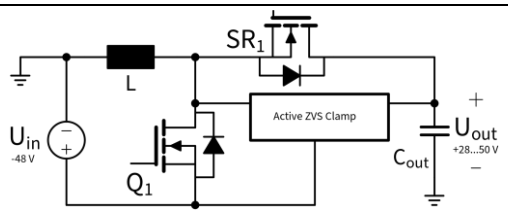
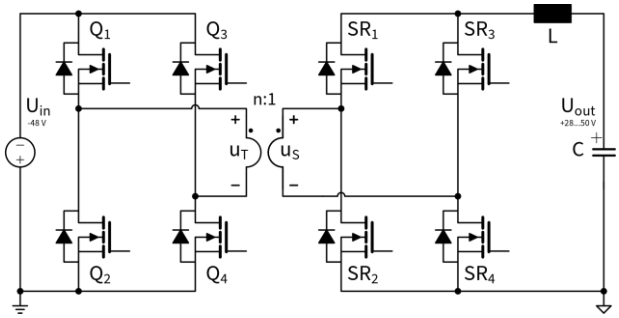
To address the demanding requirements in terms of power density and efficiency, while enabling broadband operation, GaN HEMT-based RFPAs have been affirmed as the best-in-class solution for sub-6 GHz 5G base stations. It is evident that GaN – as a compound semiconductor showing both wide-bandgap (WBG) and high electron velocity saturation (i.e., showing a high Johnson's FOM) – represents a preferred solution for high-power, high-frequency applications, solely on the basis of material properties. Wide-bandgap translates into a higher breakdown field (with the possibility to withstand higher supply voltages while retaining small geometries), while high-electron velocity saturation allows high-frequency operation. GaN HEMT-based RFPAs are typically supplied at 50 V (bringing power density benefits) and show high efficiency at higher frequencies (compared to silicon LDMOS) and high-power gain linearity.

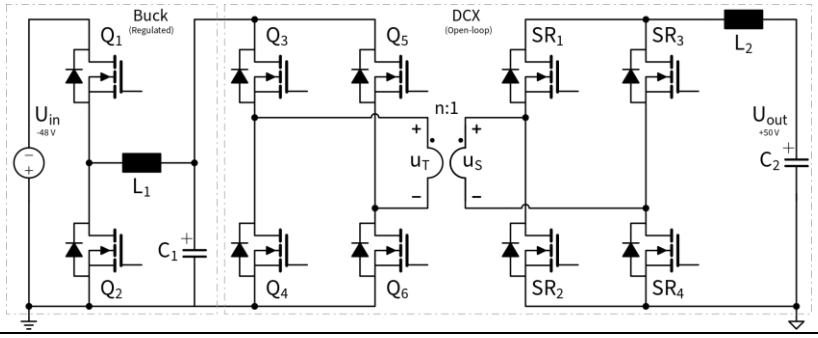
The broad adoption of GaN-based RFPAs and the strict specifications that original equipment manufacturers (OEMs) impose in terms of equipment miniaturization, in turn enforce challenging requirements on the PSU subsystem, usually embedded in the antenna itself. New solutions for DC-DC converters targeting GaN RFPAs, regulating 50 V while providing high power density and efficiency – to deal with reduced thermal budget – are needed. Major topologies aimed at RFPA applications are summarized in Table 1.

The Infineon evaluation board REF_750W_FBFB_50V aims to address the application requirements by means of a single-stage, isolated topology. The digitally controlled power supply includes advanced protections for the most reliable operation of the power module. The PMBus communication allows remote telemetry and advanced management of the PSU unit.

The Infineon evaluation board REF_750W_FBFB_50V completes the Infineon solution targeting RFPAs alongside VD_XDP_2Ph_INV_BUCK_BOOST, a non-isolated design aimed at 28 V to 56 V LDMOS and GaN RFPAs.

Table 1 Major DC-DC topologies (non-isolated, isolated) adopted in power modules aiming at RFPA applications

Topology description	Topology	Schematic diagram	Complexity (cost)
Single-stage, non-isolated	ZVS inverting buck-boost		Lowest
Single-stage, isolated **Focus of this application note**	FB-FB		Industry standard

Topology description	Topology	Schematic diagram	Complexity (cost)
Two stages, isolated	Buck + DCX		Highest

1.2 Single-stage, isolated solution: system description

This application note will focus on a system solution aimed at addressing the RFPA application requirements by means of a single-stage, isolated topology.

The main features of the Infineon evaluation board REF_750W_FBFB_50V are summarized here:

- **High power density** with 750 W output power in an industry-standard quarter-brick form factor, showing a **low profile** of 15.6 mm
- **Highly efficient** solution with typical efficiency exceeding 95.5 percent at nominal line of -48 V and full load, thanks to synergy between Infineon OptiMOS™ power MOSFETs, showing leading FOMs, and powerful Infineon EiceDRIVER™ ICs
- **Advanced digital control** thanks to Infineon's XDP™ digital power controller, ensuring **high reliability** through advanced protections (OVP, OCP, OTP, and more.) and PMBus for advanced power conversion and monitoring

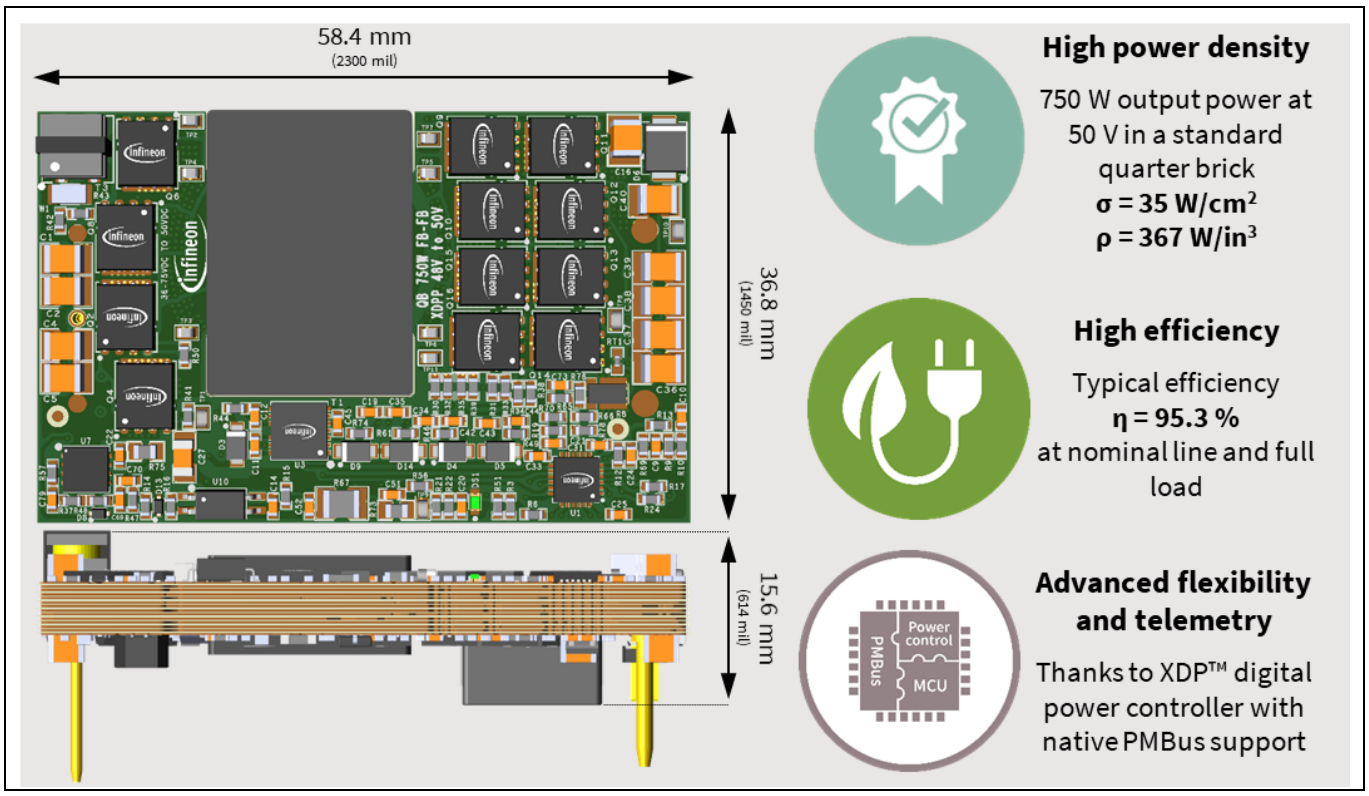


Figure 2 Main features offered by the Infineon REF_750W_FBFB_50V reference design

Introduction

The Infineon evaluation board REF_750W_FBFB_50V operates from an input voltage range of -60 to -36 V DC. The nominal output voltage is +50 V, with a maximum output current of 15 A, corresponding to a maximum output power of 750 W. The board is non-base plated, and it is intended to be operated under forced airflow of approximately 3 m/s (600 LFM). The output is galvanically isolated from the input, allowing versatile grounding configurations.

The 750 W isolated DC-DC converter consists of full-bridge topology with full-bridge synchronous rectification, switching at 140 kHz. The isolation transformer of the main power stage needs to show a step-up ratio, for the converter to be able to regulate the +50 V output rail during low-line conditions of -36 V.

The functionally isolated (coreless transformer technology) gate driver EiceDRIVER™ 2EDF7275K is used on both the primary and secondary side of the converter. This simplifies the bill of materials (BOM), by avoiding the use of digital isolators for the signals traveling across the isolation barrier. On the secondary side, the 2EDF7275K channel-to-channel functional isolation of 1.5 kV enables use of the dual-channel driver as a half-bridge driver. The 3:5 transformer ratio would not allow the choice of a junction-isolated half-bridge driver (like the EiceDRIVER™ 2EDL8024) for the SRs, because a phase voltage as high as 120 V could be expected during the high-line transient conditions.

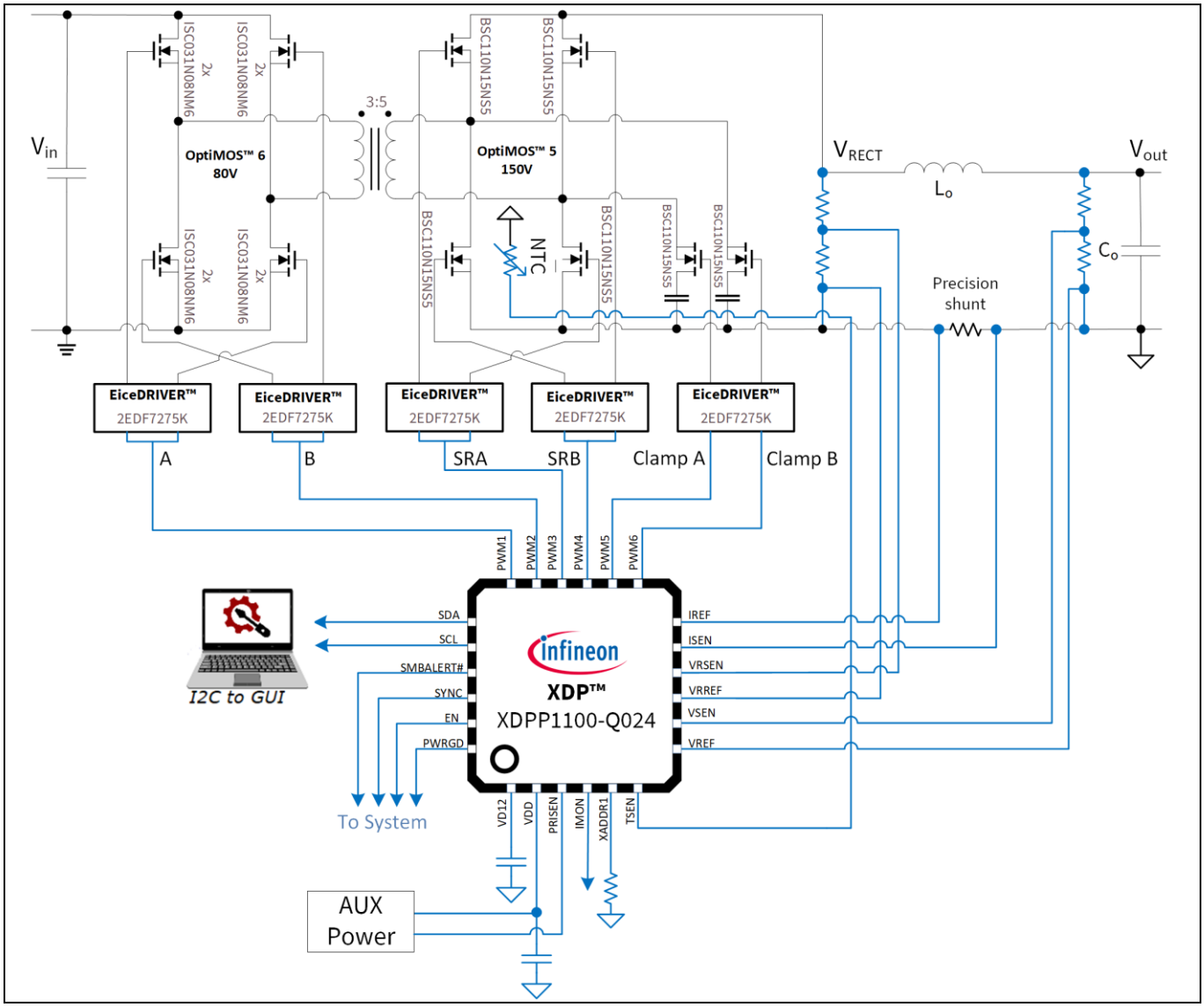


Figure 3 Block diagram of the Infineon REF_750W_FBFB_50V reference design

On the primary-side bridge, 80 V power MOSFETs in a SuperSO8 package from the latest OptiMOS™ 6 generation are used. For the secondary-side full-bridge, the 3:5 transformer step-up ratio dictates the need for 150 V rated devices, and OptiMOS™ 5 150 V serve as SRs in this application. To keep the voltage overshoot low enough to stay within the drain-source voltage rating of the SR MOSFETs, an active clamp circuit is introduced. The circuit is identified by a capacitor, to absorb the energy from the power transformer leakage inductance (as well as any other stray inductance in the power loop), properly inserted by means of an actively controlled N-channel MOSFET. The circuit is replicated for both phases of the full-wave rectifier, and the clamp switches are driven by means of an additional 2EDF7275K dual-channel isolated driver.

The control of the power stage is implemented by the Infineon XDP™ XDPP1100-Q024 digital power controller. It has analog/mixed-signal capabilities, on-chip memory, and communication peripherals. The device is specifically optimized for the control of isolated and non-isolated DC-DC converters, such as telecom brick converters. Main features include high-resolution PWM (78.125 ps), state-machine-based digital control loop, dedicated hardware (HW) peripherals (including high-performance voltage and current-sense ADCs), GUI-based system configuration for ease of use, accurate telemetry and PMBus support, and much more. It has a -40°C to 125°C operational temperature range.

The XDPP1100 supports both voltage-mode control (VMC) and peak-current-mode control (PCMC). This reference design adopts VMC. When configured to VMC, flux balancing (supported by HW) is enabled to prevent flux walkaway in the power stage transformer.

The firmware (FW) configuration and patch features are described in chapter 3.

The fully functional reference design was designed as a testing platform, with easy access to probe test points. The simplified block diagram for the board is shown in Figure 3.The full set of specifications for the board is given in the next section.

1.3 Board specification

The specifications for the Infineon REF_750W_FBFB_50V isolated quarter-brick DC-DC converter are given in Table 2.

Specifications are given for T_a = 25°C unless otherwise specified.

Table 2 Specification of the Infineon REF_750W_FBFB_50V evaluation board

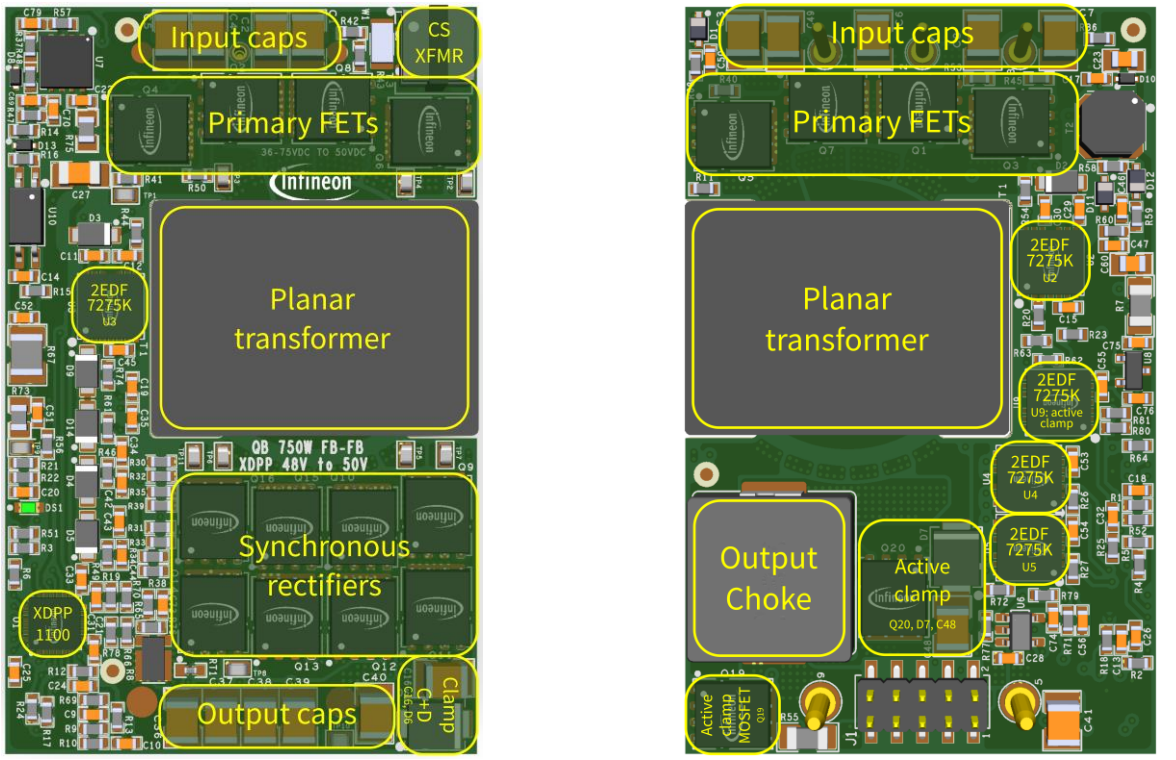
Parameter	Symbol	Values			Unit	Note/test condition
		Min.	Typ.	Max.		
Operating input voltage	V_{in}	-36	-48	-60	V	–
Input current RMS value (V_{out} = 50 V)	$I_{in,RMS}$	–	16.5 22	–	A	V_{in} = -48 V, P_{out} = 750 W V_{in} = -36 V, P_{out} = 750 W
Start-up voltage threshold	$V_{in(on)}$	-43	–	–	V	–
Minimum operating voltage after start-up	$V_{in(off)}$	–	–	-34	V	–
Output voltage set-point	$V_{out,nom}$	25	50	55	V	Adjustable setpoint
Output current	I_{out}	–	–	15	A	–
Output power	P_{out}	–	–	750	W	V_{out} = 50 V, v_{air} = 3 m/s
Efficiency (V_{out} = 50 V)	η	–	95.3	–	%	V_{in} = -48 V, P_{out} = 750 W
Power dissipation (V_{out} = 50 V)	P_{diss}	–	–	37	W	V_{in} = -48 V, P_{out} = 750 W
Output voltage ripple	$V_{out,ac}$	–	–	200	mV	Peak-to-peak, V_{out} = 50 V, $C_{out,ext}$ = 4x56 µF

Parameter	Symbol	Values			Unit	Note/test condition
		Min.	Typ.	Max.		
Output voltage set-point tolerance	$\sigma V_{out,nom}$	-1		+1	%	–
Output voltage regulation (load)	$\Delta V_{out(load)}$	–	–	100	mV	V_{in} = -48 V, 0-100% of $I_{out,max}$
Output voltage regulation (line)	$\Delta V_{out(line)}$	–	–	100	mV	V_{in} = -60…-36 V, I_{out} = 15 A
Recommended output capacitance	C_{out}	220	–	1000	µF	–
Dynamic load response -Output voltage deviation -Settling time	$\Delta V_{out(tr,load)}$ $t_{tr(load)}$	–	–	 ±500 40	 mV µs	V_{in} = -48 V, V_{out} = 50 V, 25% to 75% of $I_{out,max}$ at 2 A/µs, C_{out} = 4x56 µF
Switching frequency	f_{sw}	–	140	–	kHz	–
Airflow velocity	v_{air}	–	600 3		LFM m/s	–
Operating temperature (ambient)	T_a	-40	–	50	°C	–
Functional isolation voltage	V_{iso}	–	1500	–	V	–

1.4 Printed circuit board overview

1.4.1 PCB details

The placement of the components for the main power stage of the Infineon REF_750W_FBFB_50V isolated quarter-brick DC-DC converter is shown in Figure 4.



a) Top view b) Bottom view

Figure 4 Top and bottom views of the Infineon REF_750W_FBFB_50V Evaluation Board

The PCB follows the mechanical outline for industry-standard DOSA single-output pin, quarter-brick DC-DC converters. The board outline measures L = 58.4 mm x W = 36.8 mm (2300 mil x 1450 mil).

The PCB is made up of 14 layers. The top and bottom layers have 4 oz thickness, while the middle layers have 6 oz. thickness. The total PCB thickness is 4.72 mm (186 mil).

1.4.2 Planar transformer design

The main power stage transformer is an integral part of the PCB itself. The primary winding is made up of an effective number of turns equal to three, while the secondary winding is made up of five turns. This defines a turns ratio of 3:5. The transformer step-up ratio is needed to provide the 50 V output regulation at low-line conditions and represents a unique feature for this brick DC-DC module aimed at RFPA applications. In fact, it is typical for brick power modules to show step-down ratios of 3:1 or 4:1 (for example, the Infineon evaluation board REF_600W_FBFB_XDPP1100 – an intermediate bus converter performing 48 V to 12 V conversion – showing a turns ratio of 3:1 [1]). The step-up conversion ratio of 3:5 comes with a number of implications:

1. The PCB-integrated magnetic construction requires a higher number of layers compared to a conventional step-down DC-DC power module. Infineon's solution REF_750W_FBFB_50V comes with a PCB stackup that is 14 layers deep, with a total thickness of 4.72 mm. A core with a window height compatible with the total PCB thickness needs to be selected. A standard EQ25 core is chosen for this design.
2. The primary-referred secondary current is about 1.67 times larger than the load current. Contrary to the typical case of a step-down brick converter, a larger share of the overall copper losses is expected to affect the primary winding. To minimize these losses, in the interleaved planar construction of the transformer a larger portion of the window area is dedicated to the primary winding. Overall, the primary winding is determined by the parallel connections of three sets of windings, each of them made up of three turns. Primary winding extends to layers 1, 2, 4, 6, 7, 9, 11, 13, and 14. A complete overview of the transformer construction is shown in Figure 5.

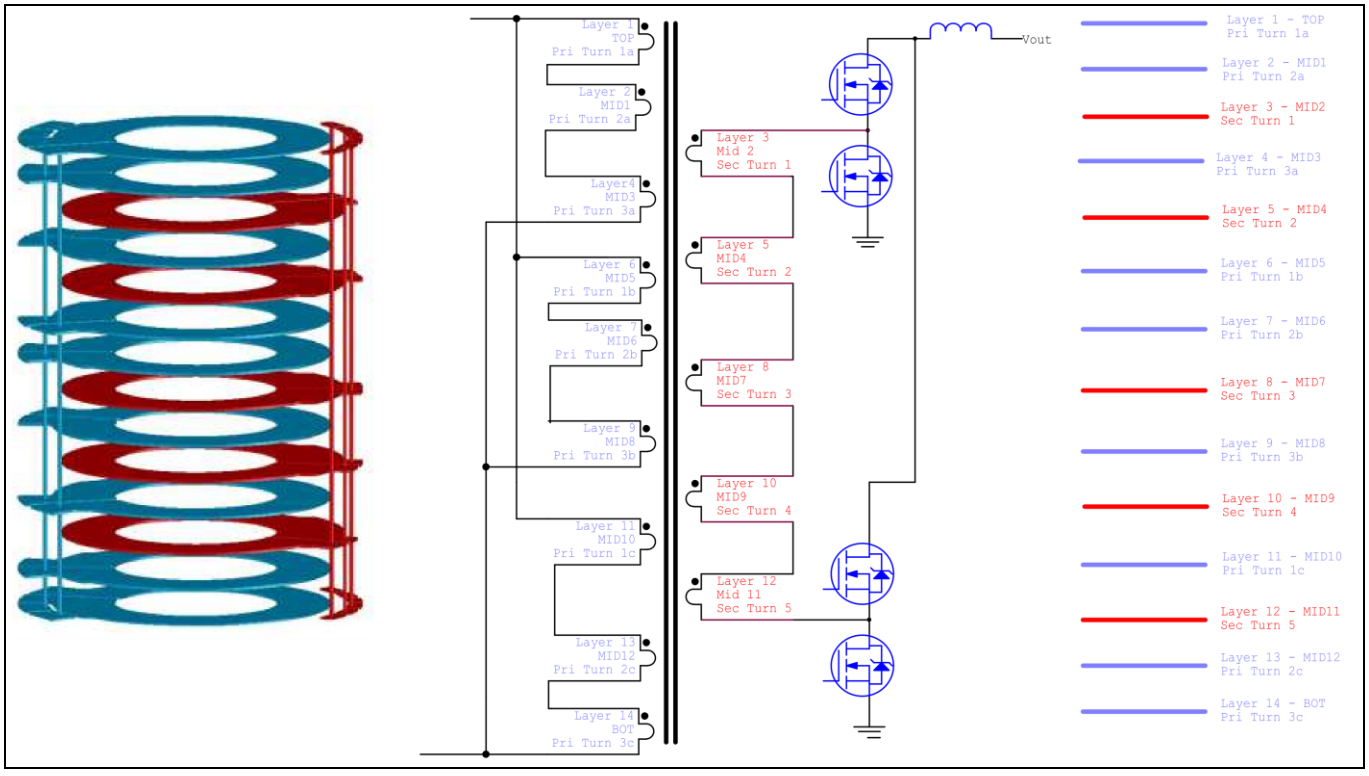
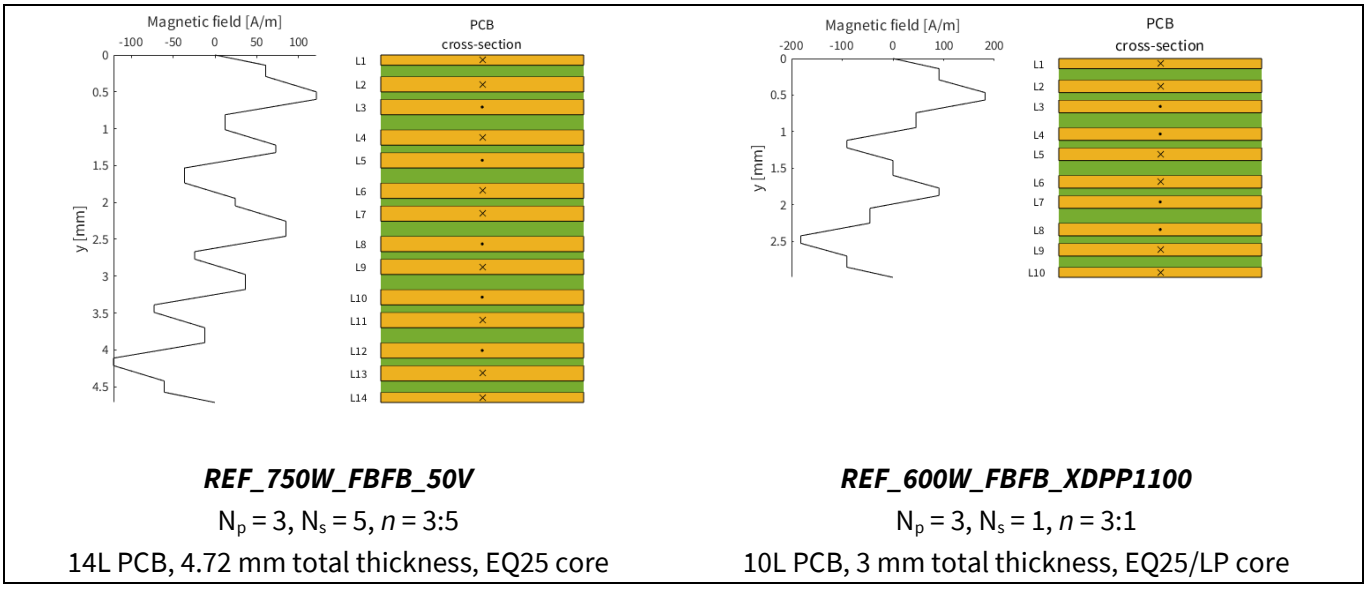


Figure 5 Planar transformer construction overview



REF_750W_FBFB_50V
N_p = 3, N_s = 5, n = 3:5
14L PCB, 4.72 mm total thickness, EQ25 core

REF_600W_FBFB_XDPP1100
N_p = 3, N_s = 1, n = 3:1
10L PCB, 3 mm total thickness, EQ25/LP core

Figure 6 Magnetomotive force (MMF) plots and scale PCB cross-sections for Infineon's REF_750W_FBFB_50V and REF_600W_FBFB_XDPP1100 reference designs

3. The overall transformer secondary-side referred leakage inductance is substantially higher compared to a transformer showing step-down conversion ratio. The comparison of the MMF plots between the Infineon reference designs REF_750W_FBFB_50V (n = 3:5) and REF_600W_FBFB_XDPP1100 (n = 3:1) for the same primary Ampere-turns (N_p = 3, I_p = 1 A) suggests a lower primary-referred leakage inductance for the 3:5 solution, as the peak value of the leakage flux is reduced thanks to the more favorable interleaving scheme adopted. A common first approximation that assumes the quasi-static AC operating regime of the transformer, enables to consider a uniform distribution of the current within each conductor cross-section. Then the magnetic field is uniform as well, resulting in a piecewise-linear MMF plot, as shown in Figure 6. The profile of the magnetic field magnitude allows, given the geometry of the core, the computation of the magnetic field energy associated with the leakage fluxes. The magnetic field energy is then associated to an overall primary-referred leakage inductance:

$$\frac{1}{2}\int_{\mathbb{R}^3} \boldsymbol{H}\cdot\boldsymbol{B}\,dV \approx \frac{1}{2\mu_0}\int_{V_{wdg}} H^2\,dV = W_m = \frac{1}{2}L_{Lk,p}I_p^2 \quad \Rightarrow \quad L_{Lk,p} = \frac{1}{I_p^2\mu_0}\int_{V_{wdg}} H^2\,dV \tag{1}$$

By evaluating the integral in equation (1) for the two different magnetic structures, it would be possible to obtain a first, rough estimation for the leakage inductances. The integral that should extend to the region of the tri-dimensional space where the magnetic field exists is carried out limited to the winding window volume V_{wdg}, since the field is negligible within the core because of the high permeability of the ferrite. The trivial solution of the integral is beyond the scope of this document, and the results of the calculations are directly reported in Table 3.

The new reference design REF_750W_FBFB_50V, aimed at RFPA, shows a primary-referred leakage inductance reduced by roughly 40 percent compared to the reference design aimed at 48 V to 12 V conversion. Still, when the overall leakage inductance is concentrated at the secondary side, the step-up ratio of 3:5 leads to a significantly higher value compared to the design showing step-down ratio:

$$L_{Lk,s} = \left(\frac{N_s}{N_p}\right)^2 L_{Lk,p} \tag{2}$$

Table 3 Estimates for transformer total leakage inductance $L_{Lk,p(s)}$ according to equations (1) and (2), primary and secondary referred

Board/reference design	XMFR ratio	Number of layers	Primary-referred leakage inductance $L_{Lk,p}$	Secondary-referred leakage inductance $L_{Lk,s}$
REF_750W_FBFB_50V	3:5	14 (4 oz. top/bottom, 6 oz. middle)	5.8 nH	16.1 nH
REF_600W_FBFB_XDPP1100	3:1	10 (4 oz. top/bottom, 5 oz. middle)	9.3 nH	1.0 nH

Since a high value of the secondary-side referred leakage inductance is heavily impacting the voltage overshoot at the synchronous rectifiers turn-off, some measures need to be taken to reduce the peak drain voltage and keep the MOSFETs operating within the SOA, or the maximum voltage allowed in compliance with the applicable regulations. See chapter 2.

4. The SR devices at the secondary side, arranged in a full-bridge configuration, need to block a voltage up to:

$$V_{s,max} = \left(\frac{N_s}{N_p}\right)|V_{in}|_{|max} = \left(\frac{5}{3}\right)60 = 100\ \text{V} \tag{3}$$

Meaning that 150 V devices need to be used to accommodate the voltage overshoot plus derating. Infineon OptiMOS™ 5 150 V, showing industry's best FOMs and in particular coming with an excellent $FOM_{rr} = R_{DS(on)} \times Q_{rr}$, is then the preferred technology for the SR MOSFETs. While the area-specific on-state resistance for OptiMOS™ 5 150 V is roughly ten times higher compared to OptiMOS™ 6 40 V devices employed in 12 V output brick converters, this is not a matter of concern for the 750 W, 50 V output reference design REF_750W_FBFB_50V, where the output current is limited to 15 A. The area-specific conduction losses for each SR MOSFET can be written:

$$P_{cond} \times (NA)\ [\text{W mm}^2] = [R_{on}A]I_{rms}^2 \tag{4}$$

With A [mm^2] being the active silicon area of each device, N the number of paralleled rectifiers and $[R_{on}A]$ the area-specific on-state resistance FOM of each technology. Considering the same total active area NA allocated for the SRs in both the conventional 12 V output (rated 600 W) and 50 V output (rated 750 W) solutions, the losses end up being roughly the same for both solutions (Table 4).

Table 4 Comparison of area-specific losses with conventional 12 V output brick converter

Board/reference design	V_{out}	$I_{out,max} \approx I_{rms}$	SRs technology	P_{cond} x (NA)
REF_600W_FBFB_XDPP1100	12 V	50 A	OptiMOS™ 6 40 V	$[R_{on}A]_{\text{OptiMOS™6 40V}}\ (50\ \text{A})^2$
REF_750W_FBFB_50V	50 V	15 A	OptiMOS™ 5 150 V	$\approx 10[R_{on}A]_{\text{OptiMOS™6 40V}}\left(\frac{50\ \text{A}}{3.\overline{3}}\right)^2$

5. The XDP™ XDPP1100 digital power controller is a versatile digital controller that can be employed in various applications, including isolated and non-isolated DC-DC converters. For isolated topologies, the IC has been conceived to support step-down type transformers by default. The controller provides flexibility through firmware, and the same hardware can also be configured to support step-up turns ratios. This can be accomplished by patching the firmware, and the details of the implementations are given in section 3.1.

1.5 Schematic files

The main power stage schematic is shown in Figure 7, while the control and bias circuit schematic is shown in Figure 8.

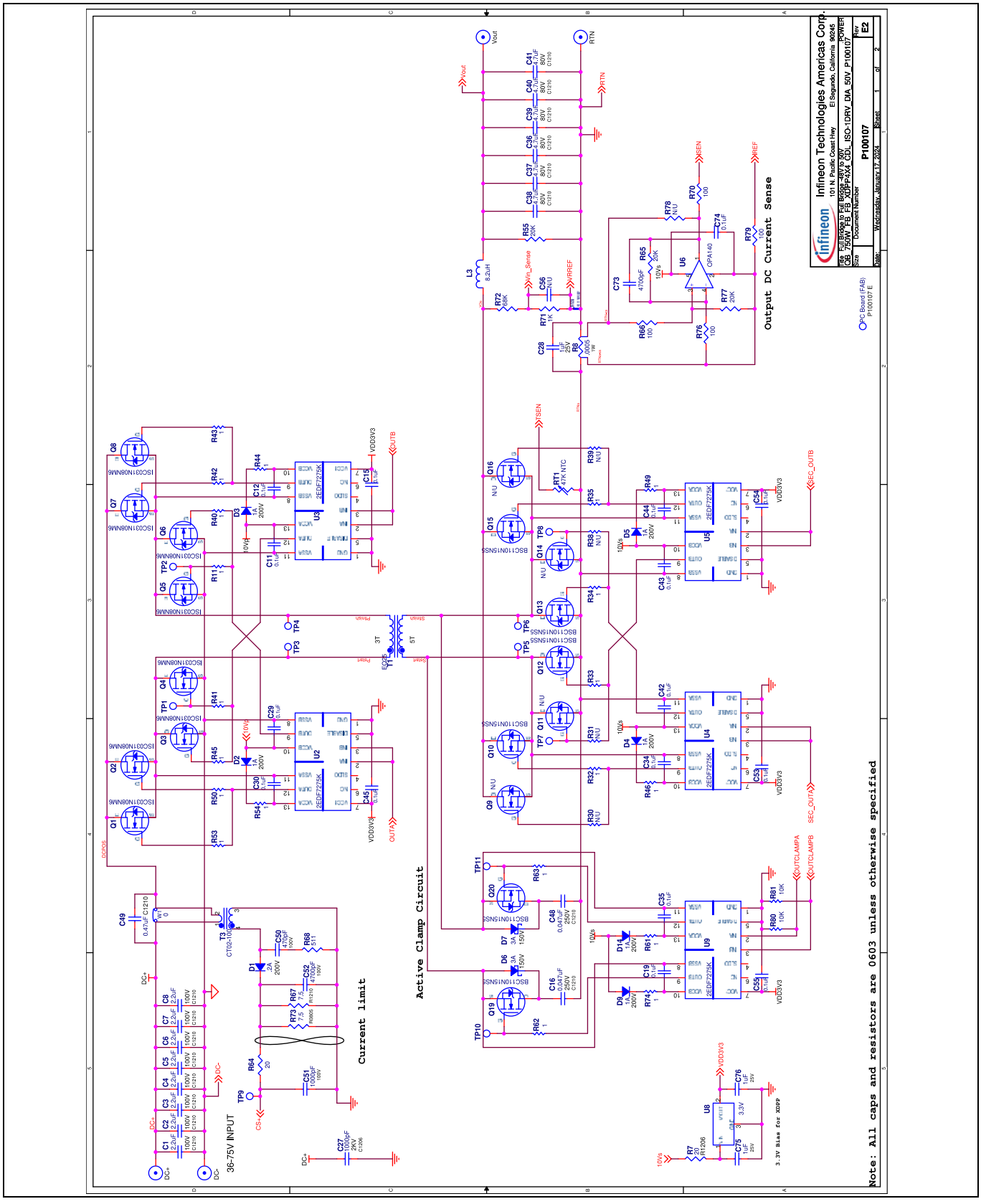


Figure 7 Power stage schematic

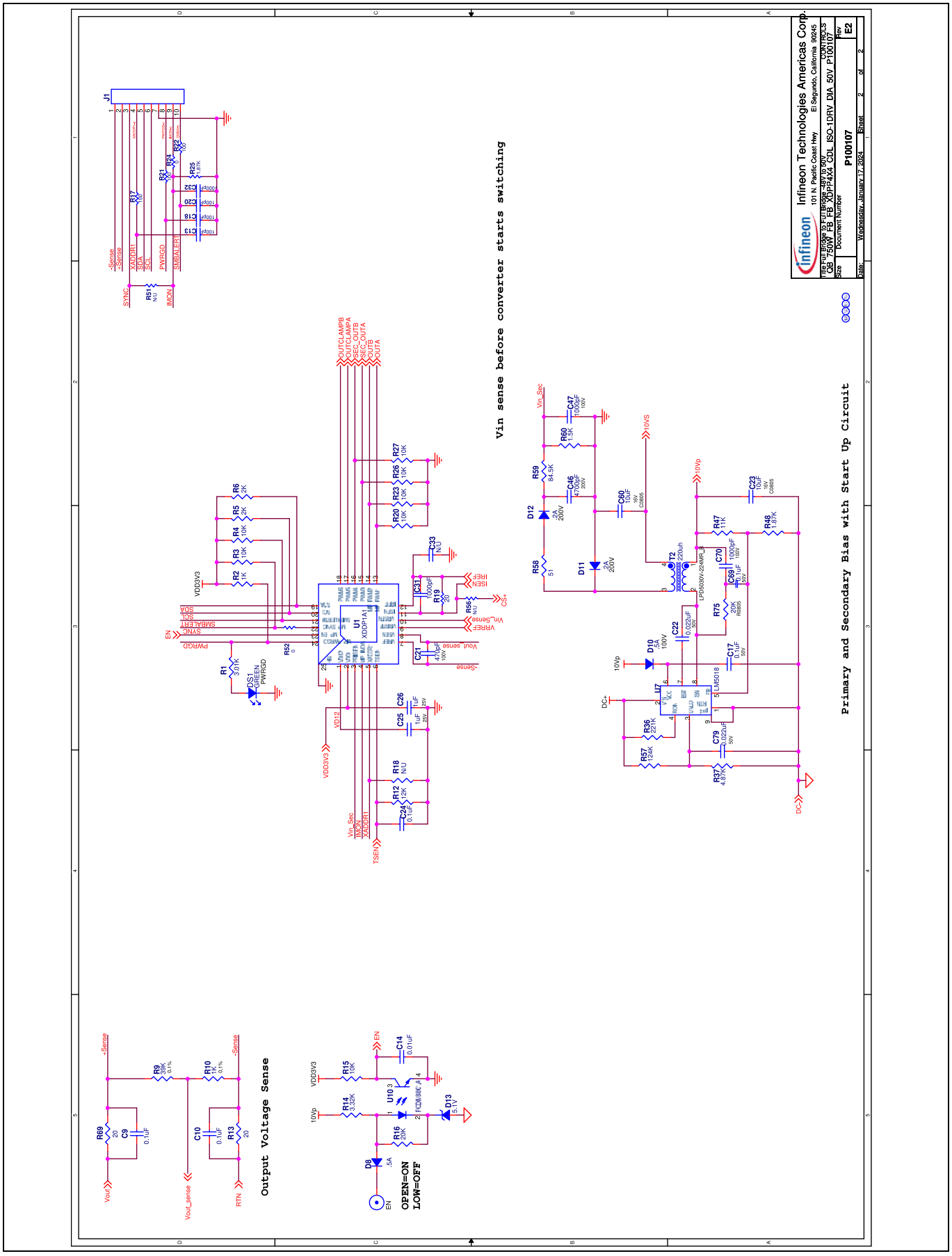


Figure 8 Control and bias circuit schematic

Introduction

The input voltage can be sensed through the auxiliary power supply secondary winding via the PRISEN pin or through the transformer secondary winding via the VRSEN pin. The XDP™ XDPP1100 digital power controller allows the user to configure V_{IN} telemetry from either source.

1.6 Test fixture board

The quarter-brick test fixture is the test platform for the quarter-brick. It provides power connection terminals and communication and debugging ports, as well as a cooling fan.

Figure 9 shows the schematic of the test fixture. It has an I²C connector for I²C and PMBus communication, and a SWD debugger port for FW debugging. The fan should be biased with an external DC power supply, in the 5 to 12 V range depending on the desired airflow. This bias is necessary to enable communication with the XDPP1100 to the USB dongle: a 3.3 V LDO regulator on the test fixture provides pull-up voltage to the SDA/SCL I²C communication bus when 5 to 12 V is applied to the external bias connector.

The switch SW1 at the primary is the enable switch to turn on the quarter-brick unit. Please note that the polarity of the enable switch can be configured by PMBus command ON_OFF_CONFIG. If EN “active low” is preferred, the user should write PMBus command ON_OFF_CONFIG and choose the polarity to be “active low”. When “active low” is selected, the on/off label on the test fixture aligns with the actual on/off status. If “active high” is selected, the on/off label shows the opposite status.

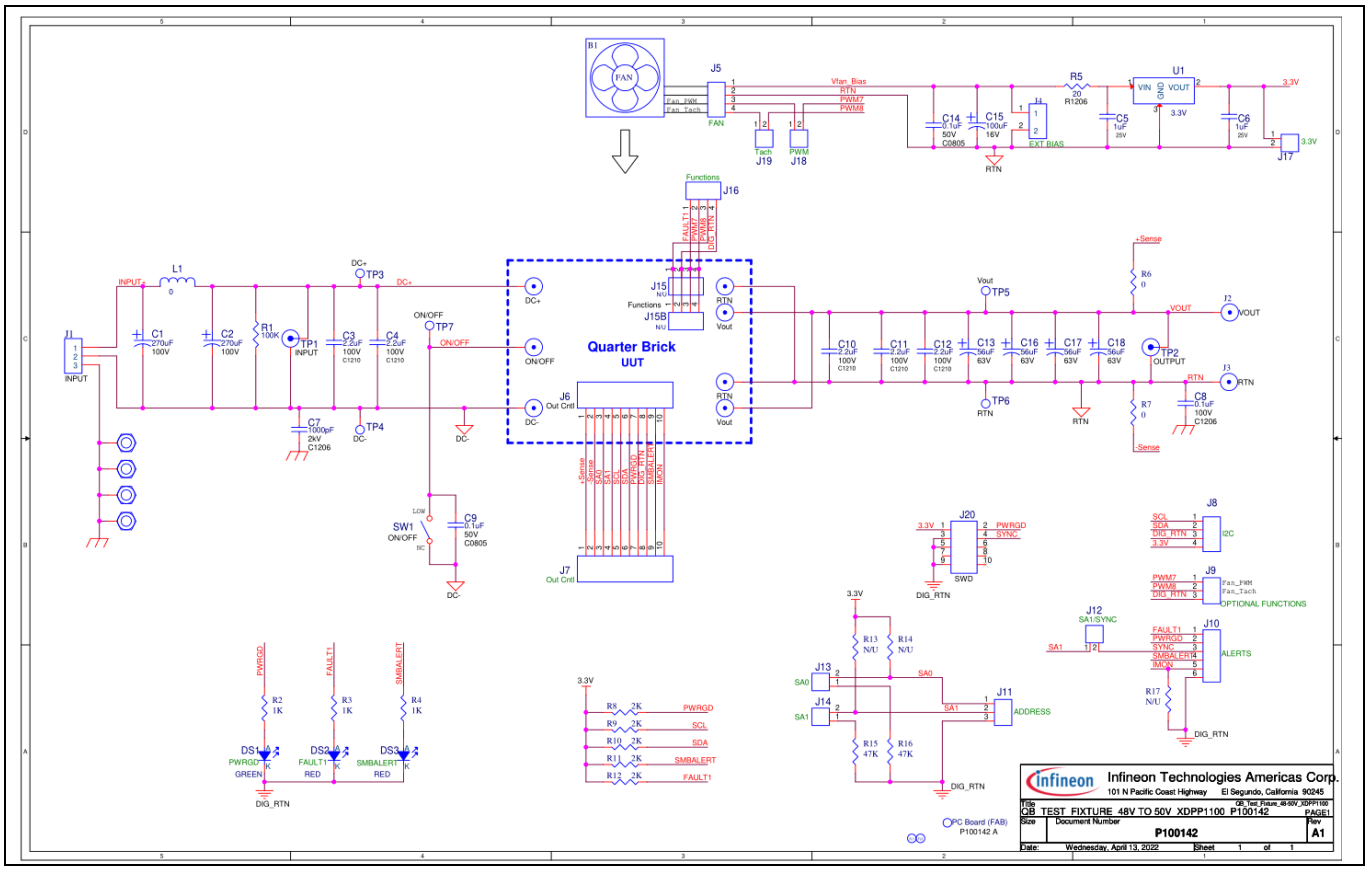


Figure 9 Test fixture board P100142 (50 V_{out}) schematic

Attention: ***The Infineon reference design REF_750W_FBFB_50V is meant to be operated only on test fixture board design no. P100142. Do not try to operate the power module on a different design, or in any design meant for 12 V output quarter-brick units!***

2 Measures to reduce the drain voltage overshoot in the synchronous rectifiers

2.1 Origin of the drain voltage overshoot

To understand the origin of the drain voltage overshoot during synchronous rectifiers turn-off, it is helpful to simplify the topology and focus only on the circuit elements that are mostly impacting on it.

The full-bridge to full-bridge topology in Table 1 can be simplified by removing the primary-side bridge, replacing it with an ideal bipolar voltage source $\pm U_{in}$. The transformer is modeled as a linear circuit consisting of an ideal transformer with a turns ratio $n = N_p:N_s$, a magnetizing inductance taking into account the finite permeability of the magnetic core, and a leakage inductance – concentrated on the primary side – modeling the imperfect flux linkage between the windings. Any primary-side power loop stray inductance (PCB and packages) can always be concentrated into the primary-side referred leakage inductance of the power transformer. CCM operation for the output inductor is assumed, and this one is considered big enough to be modeled as a constant current source I_L. The resulting simplified topology is shown in Figure 10.

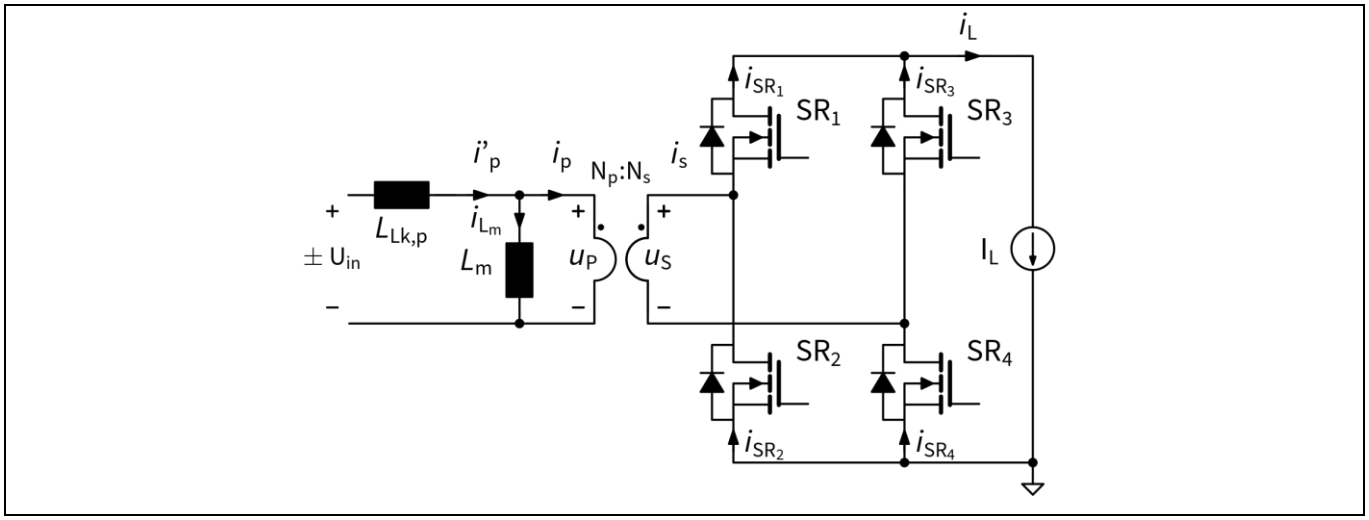


Figure 10 Simplified full-bridge to full-bridge FB-FB topology

The method summarized by equation (1) enables estimation of the sum of the leakage reactances reported overall on the primary side of the transformer, assuming that the magnetizing inductance L_m can be considered much larger compared to the primary-reflected secondary leakage inductance. The sum of the leakage reactances can be equivalently concentrated on the secondary port of the transformer. The values of the primary-side and secondary-side referred to overall transformer leakage are linked by the turns ratio squared (Figure 11).

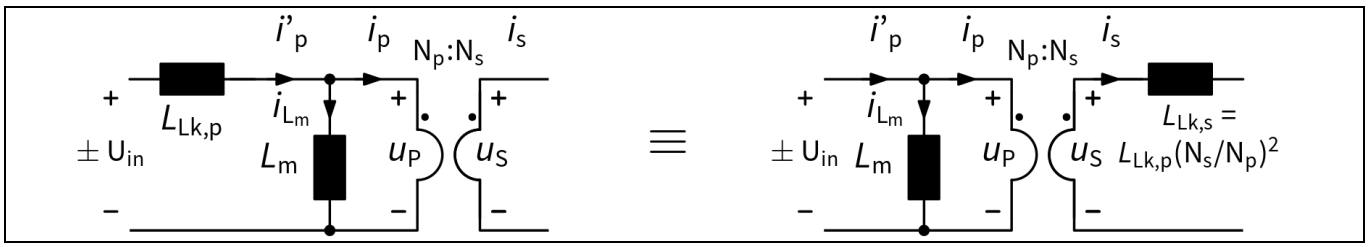


Figure 11 Equivalence of the practical transformer model showing an overall primary (left) or secondary (right) referred leakage inductance

Measures to reduce the drain voltage overshoot in the synchronous rectifiers

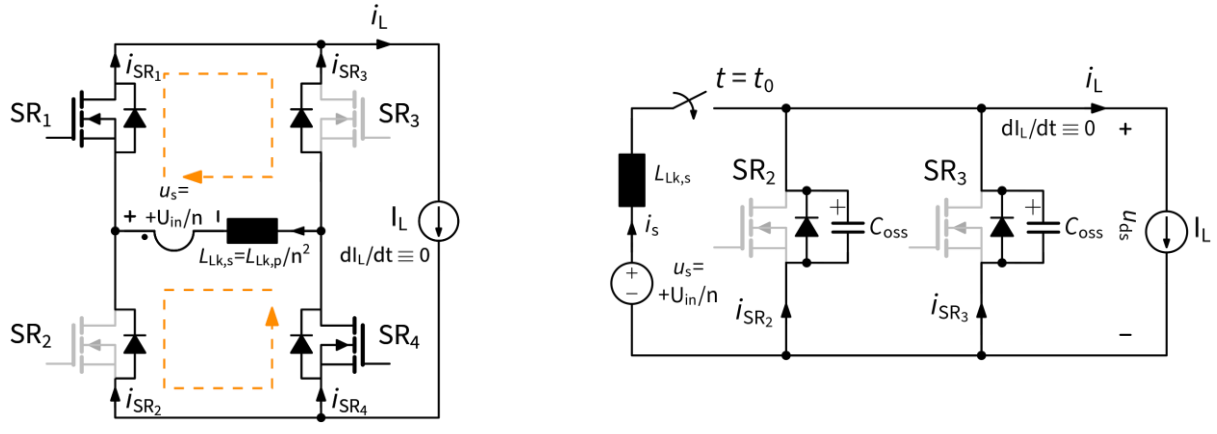
Considering a model for the transformer showing an overall secondary-side referred leakage inductance simplifies the analysis and leads to the circuit shown in Figure 12a. Here, a powering phase which sees the diagonal identified by SR_1 and SR_4 MOSFETs as the active rectification path is considered. The powering phase, starting at $t = t_0$, follows a freewheeling phase where all the primary switches are off, and all the SRs are on, sharing the load current I_L. During the freewheeling phase the transformer is effectively shorted by the SRs, and so the reflected primary voltage is zero, while the primary bridge current i'_p is zero. The primary transformer current i_p can be considered zero as well, taking the approximation of a large magnetizing inductance. By assuming this, the rectifiers only carry a portion of the load current, otherwise in the practical case of a finite magnetizing inductance L_m, they also share the non-null magnetization current ($i_p = i_{Lm}$). For the sake of clarity, the approximation for $L_m \rightarrow \infty$ is taken. For $t \geq t_0$ part of the load current carried by the body diodes of SR_2 and SR_3 starts to be transferred to the channel of the active synchronous rectifiers, SR_1 and SR_4. The di/dt on the output branch is negligible, and so the current transfer is dictated only by the two inner loops of the full-bridge, comprising the four rectifiers, the leakage inductor, and the transformer secondary (Figure 12a). In particular, the di/dt is governed by the total inner loops inductance, that according to the picture coincides with the transformer leakage inductance only, but that also includes the other stray inductances in the power loop:

$$L_{loop} = L_{Lk,s} + L_{stray} \quad \text{where} \quad L_{stray} = \Sigma(L_s + L_d) + L_{PCB} \tag{5}$$

With L_s and L_d being the source and drain package-related inductances for the power MOSFETs. According to the estimate carried out in Table 3, the contribution of $L_{Lk,s}$ is dominant among L_{stray} for the reference design REF_750W_FBFB_50V aimed at RFPA applications and again, for the sake of clarity, will be the only contribution considered. Then, assuming equal current sharing among the rectifiers, it can be shown that the current in SR_2 and SR_3 body diodes is ramped down with a rate:

$$\left|\frac{di_{1SR}}{dt}\right| = \frac{U_{in}}{2nNL_{lk,s}} \tag{6}$$

Where $n = N_p/N_s$ and N is the number of paralleled SRs for each position. From equation (6) it is evident that having a larger value for $L_{Lk,s}$ results in a current in the rectifiers ramping down at a lower rate, enabling more charge carriers to recombine and resulting in a lower value for the recovered charge Q_{rr}. Parallelization is also beneficial in this sense since the current density is reduced within each rectifier. Please note that equation (6) assumes that the primary-side MOSFETs will switch so fast they will not limit the current transfer rate.



a) Simplified circuit with secondary-side referred leakage

b) Equivalent circuit for transient analysis

Figure 12 Minimum circuits needed for the analysis of voltage overshoot in synchronous rectifiers

In Figure 12b the circuit of Figure 12a is further simplified and rearranged to perform a simple transient analysis. The complex, buck-isolated topology has been reduced to a simple circuit, which is functionally identical to a simple non-isolated buck converter.

The dead time mode of operation precedes the instant of time $t = t_0$, where the synchronous rectifiers SR_2 and SR_3 are in the off-state and their body diodes share the load current. Their drift regions are flooded by carriers sustaining the current flow. At $t = t_0$ an input voltage step is applied. The current in the rectifiers ramps down according to equation (6). The drain-source voltage is clamped by the body diode to a forward voltage drop, until the diode experiences recovery. In practice, when measuring the drain-to-source voltage with an oscilloscope, a small step in the drain-source voltage is always recorded in the waveform during the current ramp-down phase, and this is related to the stray inductances associated with the package (not shown in the equivalent circuit):

$$u_{ds} = -\underbrace{u_{sd}(i_d)}_{\substack{\text{diode forward}\\ \text{voltage}}} + (L_s + L_d)\frac{U_{in}}{2nNL_{lk,s}} \qquad t_0 \le t \le t_1 \tag{7}$$

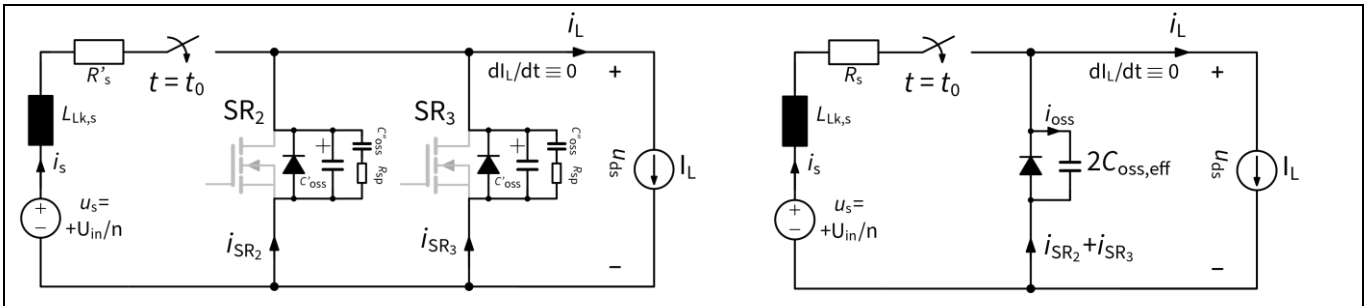
By ignoring any form of charge storage mechanism within the rectifiers, they would instantaneously turn off as soon as the current reaches zero, let's say at $t = t_1$. From this point onward, the drain-to-source voltage is no longer clamped, and it is free to rise. The drain-to-source voltage rises, overshooting the transformer secondary voltage. Let's assume, for a moment, to consider a constant, effective output capacitance for the MOSFETs. Please note that ignoring the voltage dependence of the C_{oss} is a strong assumption, given that the significant nonlinearity of the output charge characteristic in modern charge-compensated trench MOSFETs would have a severe impact on the voltage overshoot. In a latter section, this assumption will be dropped, so that the effects of the voltage-dependent output capacitance will become clearer.

By studying the forced response of the circuit in Figure 12b one would find that the voltage at the rectifiers would reach two times the transformer secondary voltage, independently of the values of $L_{Lk,s}$, C_{oss} and the load current I_L.

$$U_{ds,pk} = \max_{t \ge t_2} u_{ds}(t) = 2U_s \tag{8}$$

This outcome is the result of having neglected any damping action in the circuit and is in accordance with the theory of the non-damped series LC circuit. See section 5.1.1.

Some non-negligible damping action is always recorded in the circuit. Input capacitors' ESR, primary switches and synchronous rectifiers SR_1 and SR_4 $R_{DS(on)}$, and transformer and layout-associated AC resistance R_{ac}, can be combined into an equivalent secondary-referred series resistance R'_s. In addition, in established charge-compensated field-plate trench MOSFET technologies, including OptiMOS™ 5 150 V, an equivalent integral RC snubber can be always referred to the output port of the device [2], as shown in Figure 13a.



a) Simplified circuit including damping

b) Equivalent series RLC damped circuit for transient analysis

Figure 13 Minimum circuits including damping actions

The combination of the series resistance and the output RC snubber introduces the missing damping action that is needed to explain the experimental observations. The circuit in Figure 13a is a non-elementary series or parallel-like RLC circuit, and its analysis is complex. By applying some elementary impedance transformations (valid only at the natural oscillation frequency), and with minor approximations, the circuit in Figure 13a can be reduced to the equivalent series RLC circuit in Figure 13b.

Again the forced response of the circuit in Figure 13b can be easily obtained (see section 5.1.2), and a closed-form expression for the voltage overshoot at the rectifiers is given in equation (9):

$$U_{ds,OV}[\%] = \exp\left(\frac{-\zeta\pi}{\sqrt{1-\zeta^2}}\right) \times 100\% \tag{9}$$

Where $\zeta \triangleq R_s/(2L_{Lk,s}\omega_0)$ is the damping ratio, and $0 \leq \zeta \leq 1$.

The voltage overshoot is higher for highly underdamped circuits (high quality factor *Q*), e.g., with the higher value of the leakage inductance. In addition, the oscillations will take longer to extinguish. Drain-source voltages during rectifier turn-off are plotted in Figure 14, having swept the overall, secondary-referred loop inductance (damping ratio). Plots are produced according to equation (52), given in the Appendix.

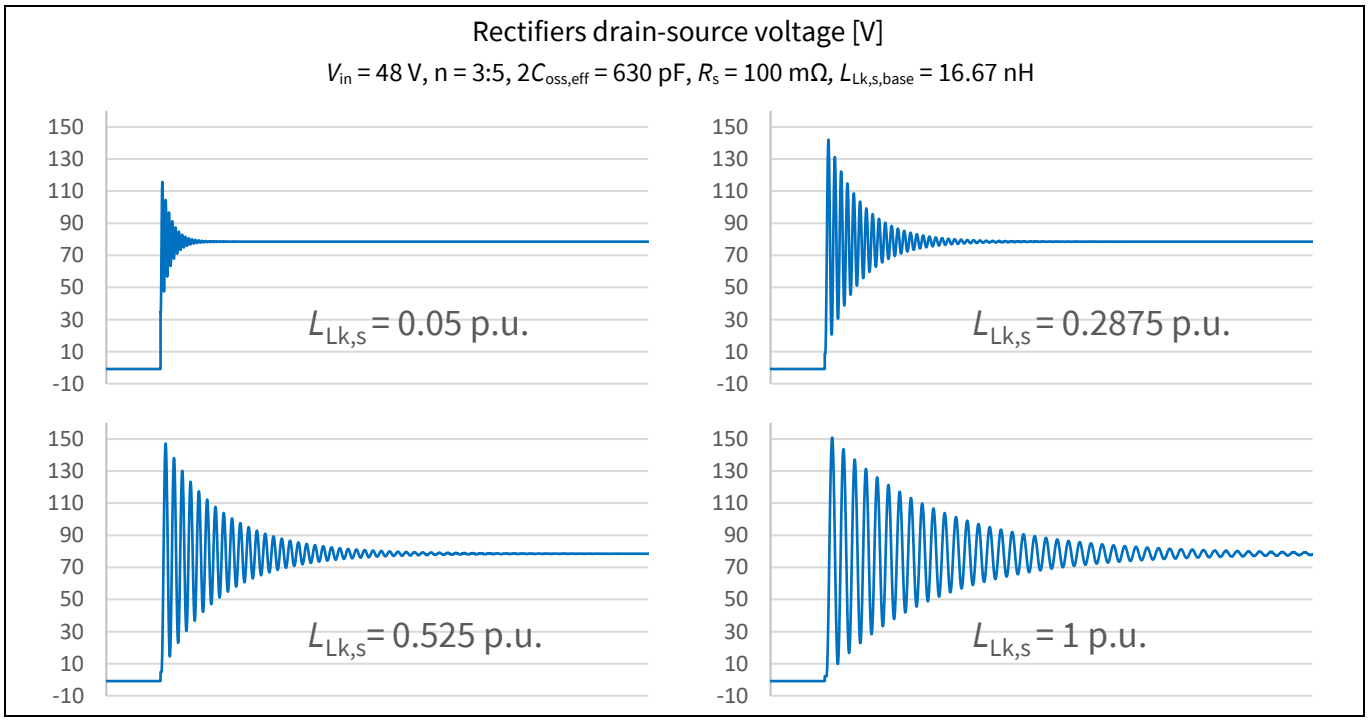
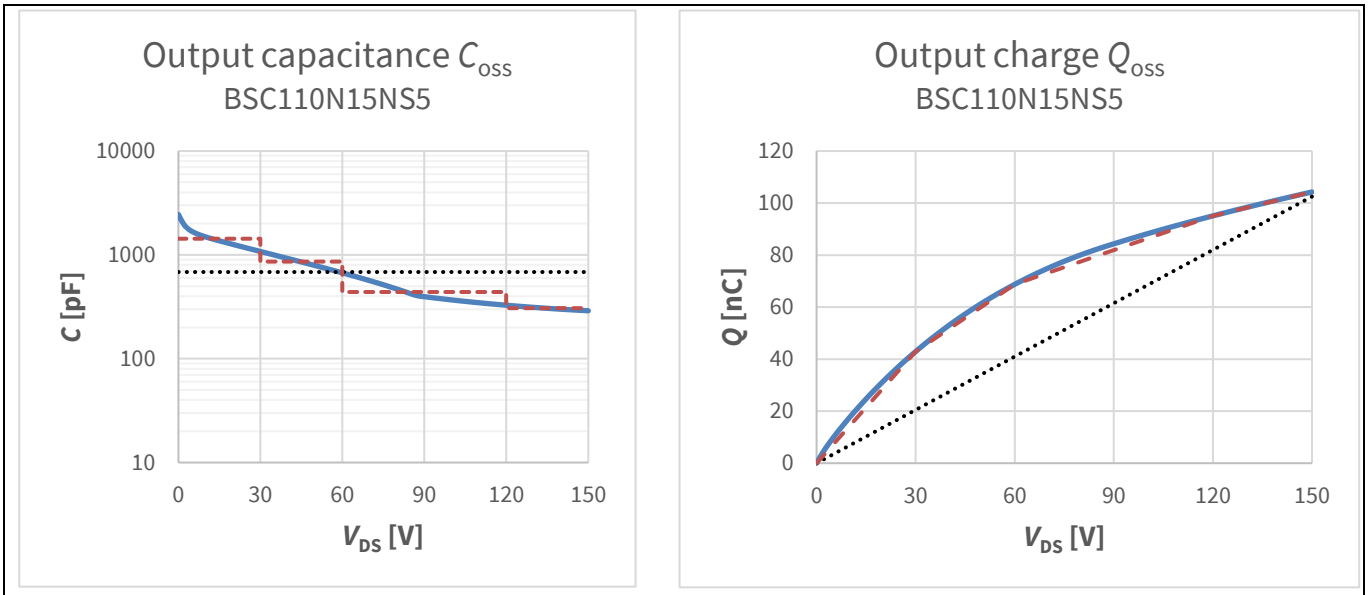


Figure 14 **Forced response plotted for the circuit in Figure 13b, having swept the inductance, resulting in different damping ratios. $L_{Lk,s}$ is given in p.u. "per unit" of the base inductance value $L_{Lk,s,base}$.**

While the result in equation (9) recovers at least the dependence on the leakage inductance and the output capacitance, the model is still inadequate to accurately describe the actual turn-off of the rectifier(s).

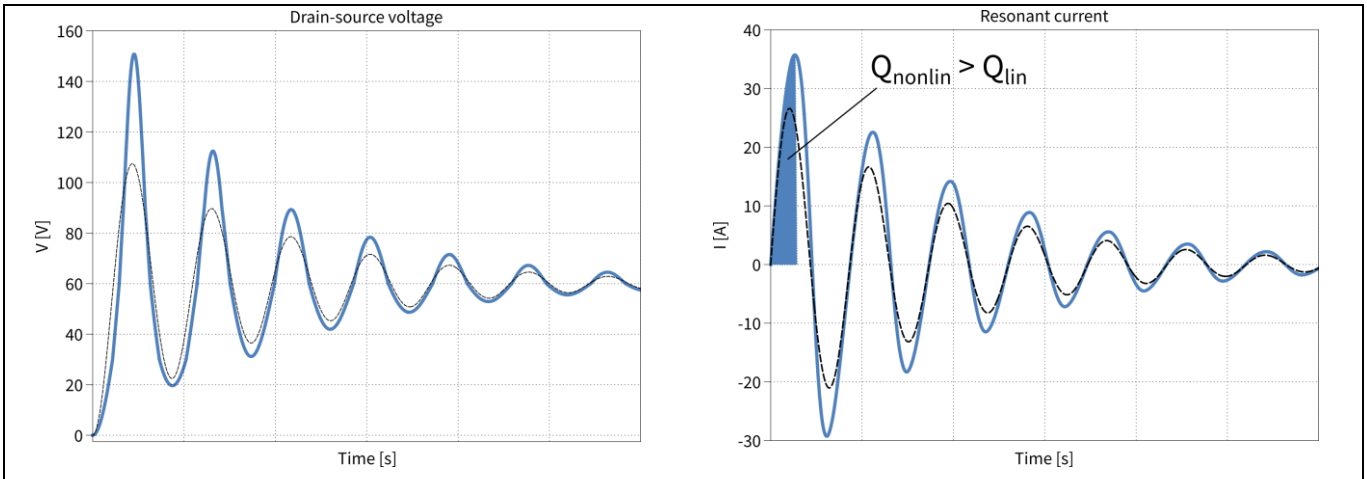
The results reported so far are in fact valid only under the assumption of a constant effective output capacitance $C_{oss,eff}$. The relation between output charge and voltage in actual devices is nonlinear, resulting in an anomalous output capacitance $C_{oss} = C_{oss}(u_{ds})$. Despite that, a constant output capacitance $C_{oss,eff}$ can always be fitted to give a response that is in partial agreement (for example, by fitting the natural oscillation frequency) with experimental results or device simulations. This was, for instance, the approach used to produce the plots in Figure 14.



Solid: Actual characteristics correspondent to nonlinear charge-voltage relationship.
Dashed: Piecewise-linear approximation for the nonlinear output charge characteristic.
Dotted: Fitted, effective constant output capacitance characteristics.

Figure 15 Output capacitance and output charge characteristics for OptiMOS™ 5 150 V BSC110N15NS5 taken as an example

In most of the cases, the impact of the actual voltage-dependent output capacitance in MOSFETs is to produce an overshoot larger than the one predicted by equation (9). In a practical MOSFET, the output capacitance decreases with increasing drain-source voltage (Figure 15). This, in the rectifiers turn-off transient, translates in a drain-source voltage waveform that rises not anymore according to a single eigenfrequency: the drain-source voltage rises more gradually at the beginning of the transient (low V_{DS}, higher C_{oss}), whereas the waveform becomes progressively steeper once the drain-source voltage increases (lower C_{oss}). Accordingly, the displacement current increases with a faster rate compared to the case of a constant capacitance. This also means that, before the current starts reverting, more charge will be transferred to the output capacitance (depletion layer) resulting in a way higher peak voltage overshoot compared to the linear case (Figure 16).



Solid: V_{DS} and resonant current waveforms according to the nonlinear output charge characteristic
Dotted: Same waveforms for an effective constant output capacitance (ω_0 fit)

Figure 16 Turn-off transient comparison for linear and nonlinear output charge characteristic

The analytical model presented in Appendix can be directly generalized to predict the overshoot also in a practical scenario, when a piecewise linear approximation is taken for the output charge characteristic (Figure 15). The same approach is pursued, for instance, by a variety of piecewise-linear simulators.

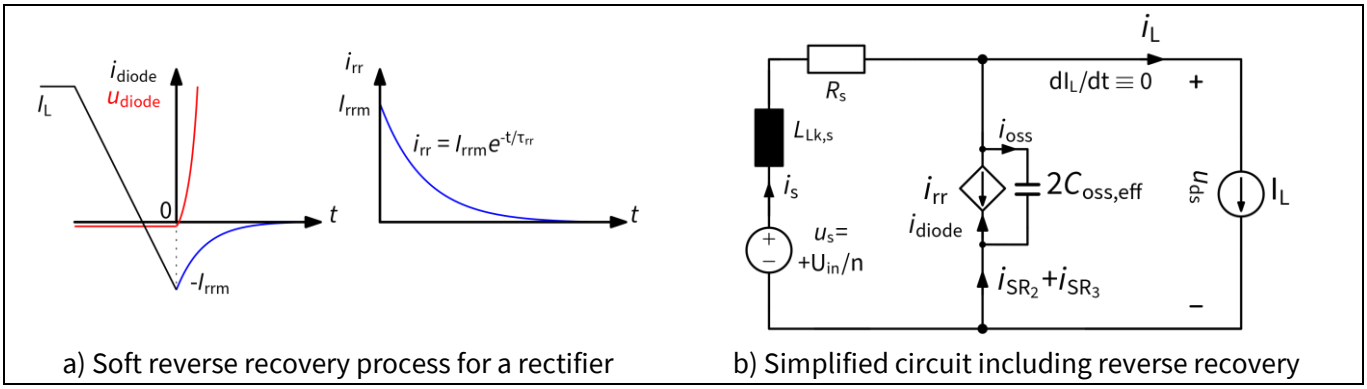
Note: *Infineon's SPICE models for OptiMOS™ Power-Transistors come with a full modeling of the MOSFETs voltage-dependent capacitances, and they must be considered the preferred tool to perform this kind of investigations.*

Although the model presented so far does not consider the effects of a load current, in its simplicity it still captures the main dependencies of the voltage overshoot on the circuit parameters. These are found to be the overall secondary-referred loop inductance (including transformer leakage and any other source of stray inductances), the output capacitance of the SR MOSFETs (with its voltage-dependent characteristic), and the power loop resistance.

Experimental results clearly show that the voltage overshoot at the rectifiers during turn-off strongly depends on the load current. Despite being modeled on the circuits just discussed; it seems from previous analysis that the voltage overshoot would be completely independent of the load. The dependence on the load current is explained by the presence of a charge storage mechanism within the rectifiers, until now ignored. During the dead time, the drift regions of the SRs are flooded with charge carriers, whose concentration is dependent on the value of the current carried by the rectifier. The higher the forward current, the greater the amount of stored charge. Charge carriers need to be removed from the drift region to create a space charge region that can support the voltage. This process, called *reverse recovery*, prevents the rectifier switching to the reverse blocking state as soon as the current crosses zero. Instead, a reverse current (whose rate is still given by equation (6)) is observed to persist until the drift region is sufficiently depleted from carriers. This happens after a time $t_a = f(I_L, di/dt, T_j)$ starting from the zero crossing, for which the reverse current reaches its peak value I_{rrm}. Then the voltage is free to rise according to the formation of a space charge region, while the remaining charge carriers are swept out by means of an exponential decaying (diffusion) current. The whole commutation process is shown in Figure 17a.

While the process is far more complex than described here [3], the modeling proposed is again sufficient and simple enough to highlight the role of the main players contributing to the drain-source voltage overshoot during rectifier turn-off. Again, the approximation for a constant, effective output capacitance for the MOSFETs is taken to keep the analysis as simple as possible.

Let's consider for simplicity $t = 0$ the instant of time for which the current in the body diode reached the peak reverse recovery current I_{rrm}. Then the diode can be replaced by a controlled current source i_{rr} and a parallel capacitance equal to an effective constant output capacitance for the MOSFET (Figure 17b).



a) Soft reverse recovery process for a rectifier b) Simplified circuit including reverse recovery

Figure 17 Reverse recovery modeling and equivalent simplified circuit for transient analysis

The initial conditions for the circuit are given by:

$$\begin{cases} u_{ds}(0) = -U_{sd,f} \approx 0 \\ i_s(0) = I_L + I_{rrm} \end{cases} \tag{10}$$

The Kirchhoff voltage law for the left-side mesh is written:

$$L_{Lk,s}\frac{d}{dt}\left[I_L + 2C_{oss,eff}\frac{du_{ds}}{dt} + i_{rr}\right] + R_s\left[I_L + 2C_{oss,eff}\frac{du_{ds}}{dt} + i_{rr}\right] + u_{ds} = U_s \tag{11}$$

Where i_{rr} is a time-varying current source modeling the soft-recovery behavior of the diode (minority-carriers diffusion current), modeled as a decaying exponential:

$$i_{rr}(t) = I_{rrm}e^{-\frac{t}{\tau_{rr}}} \tag{12}$$

The time constant τ_{rr} is closely tied to the semiconductor device physics, specifically the characteristic time for the recombination of the charge carriers under high-level injection conditions.

Using (12) in (11) results in (13), a second-order ordinary differential equation for the drain-source voltage u_{ds}:

$$2L_{Lk,s}C_{oss,eff}\frac{d^2u_{ds}}{dt^2} + 2R_sC_{oss,eff}\frac{du_{ds}}{dt} + u_{ds} = (U_s - R_sI_L) + \left(\frac{L_{Lk,s}}{\tau_{rr}} - R_s\right)I_{rrm}e^{-\frac{t}{\tau_{rr}}} \tag{13}$$

The solution of the homogeneous equation has already been found in the form (see section 5.1.2):

$$u_{ds,hom}(t) = Ae^{-\frac{R_s}{2L_{Lk,s}}t}\sin(\omega t + \Phi) \tag{14}$$

While the solution must be found in the form of a constant plus an exponential function (having the same eigenvalue as the forcing function):

$$u_{ds,part}(t) = U + U_{rr}e^{-\frac{t}{\tau_{rr}}} \tag{15}$$

By substitution of (15) into (13), and after some manipulation that includes ignoring the effect of the equivalent series resistance, one can solve the two arbitrary constants:

$$\begin{cases} U = U_s - R_sI_L \\ U_{rr} \approx \tau_{rr}I_{rrm}L_{Lk,s}\dfrac{\omega_0^2}{1+\omega_0^2\tau_{rr}} = Q_{rr}L_{Lk,s}\dfrac{\omega_0^2}{1+\omega_0^2\tau_{rr}^2} \end{cases} \tag{16}$$

Where the reverse recovery charge Q_{rr} is given by:

$$Q_{rr} = \int_0^\infty I_{rrm}e^{-\frac{t}{\tau_{rr}}}dt = \tau_{rr}I_{rrm} \tag{17}$$

The general solution is:

$$u_{ds}(t) = u_{ds,hom}(t) + u_{ds,part}(t) = Ae^{-\alpha t}\sin(\omega t + \phi) + U + U_{rr}e^{-\frac{t}{\tau_{rr}}} \tag{18}$$

The two arbitrary integration constants A and Φ are found by imposing the initial conditions:

$$\begin{cases} u_{ds}(0) = 0 \\ \dfrac{du_{ds}}{dt}(0) = \dfrac{i_{oss}(0)}{2C_{oss,eff}} = \dfrac{i_s(0) - i_{rr}(0) - I_L}{2C_{oss,eff}} = \dfrac{I_L + I_{rrm} - I_{rrm} - I_L}{2C_{oss,eff}} = 0 \end{cases} \tag{19}$$

Resulting in:

$$\begin{cases} \phi = -\tan^{-1}\left[\omega\tau_{rr}\left(1 + \dfrac{U}{U_{rr}}\right)\right] \\ A = \dfrac{U_{rr}\sqrt{1 + (\omega\tau_{rr})^2\left(1 + \dfrac{U}{U_{rr}}\right)^2}}{\omega\tau_{rr}} \approx U + U_{rr} \end{cases} \tag{20}$$

Finally, the general solution of the problem is then written:

$$u_{ds}(t) = (U_s - R_s I_L)\left[1 + e^{-\frac{R_s}{2L_{Lk,s}}t}\sin(\omega t + \phi)\right] + \underbrace{L_{Lk,s}Q_{rr}\frac{\omega_0^2}{1 + \omega_0^2\tau_{rr}^2}\left[e^{-\frac{t}{\tau_{rr}}} + e^{-\frac{R_s}{2L_{Lk,s}}t}\sin(\omega t + \phi)\right]}_{\text{Term associated with body diode reverse recovery}} \tag{21}$$

By direct comparison of equation (21) with the result already found in the Appendix (equation (52)) it shows that an additional term, in phase with the main *RLC* resonance, contributes to the drain-source voltage overshoot on the rectifiers. The additional term is directly proportional to the product of the secondary-referred loop inductance L_{Lks}, with the reverse recovery charge Q_{rr}. Since Q_{rr} is proportional to the load current I_L, the load dependence of the voltage overshoot is recovered:

$$U_{rr} \propto L_{Lk,s}Q_{rr}(I_L) \tag{22}$$

From equation (21) it is also evident that again, the higher the overall secondary-side referred loop inductance, the higher is the extra voltage overshoot expected because of the reverse recovery. This is far more complex, as a higher value for $L_{Lk,s}$ results in a lower di/dt on the rectifiers during turn-off, and this helps in reducing Q_{rr} because more charge carriers have time to recombine within the device. Despite the excellent switching performances (Q_{rr}) of OptiMOS™ 5 150 V [4], the large $L_{Lk,s}$ in Infineon REF_750W_FBFB_50V would still give an unacceptably high voltage overshoot at the drain of the rectifiers.

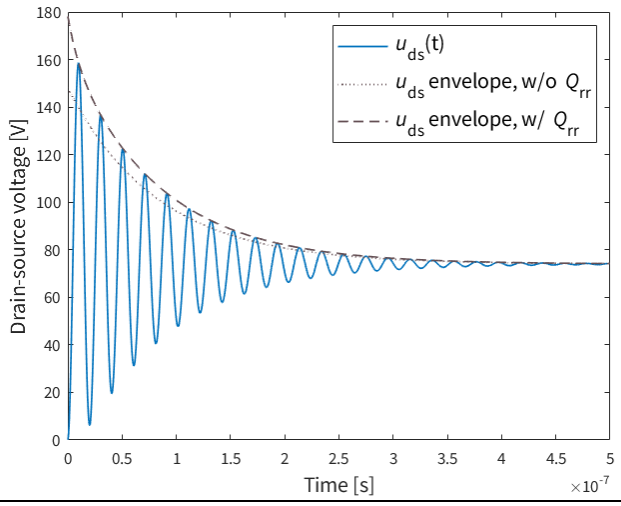
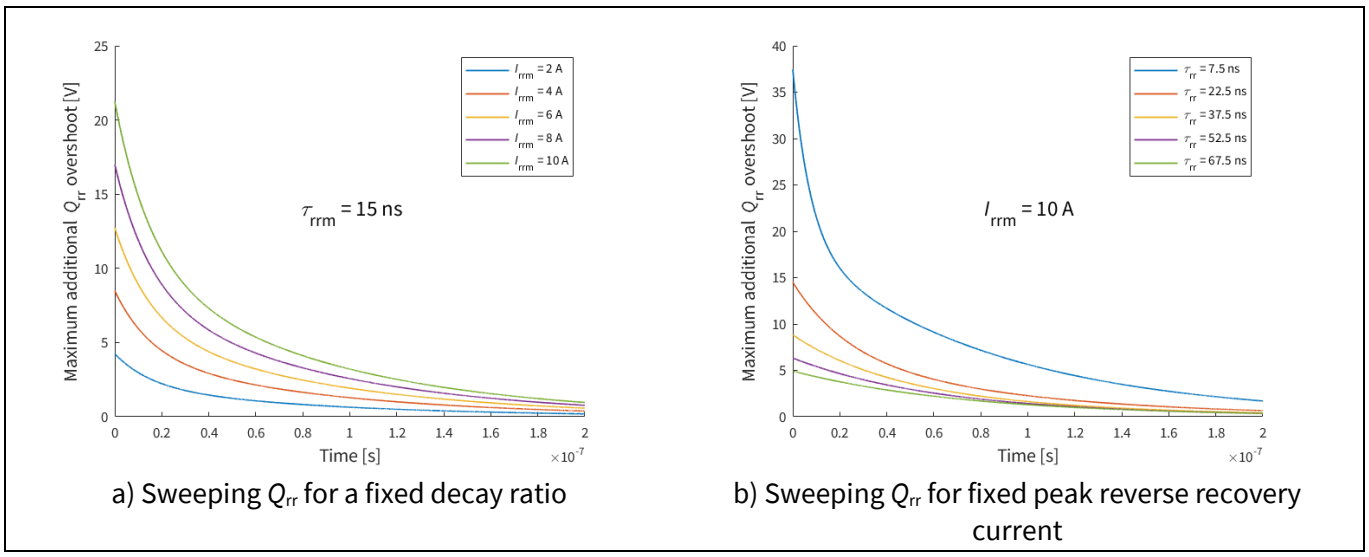


Figure 18 Drain-source voltage for the rectifier with reverse recovery in circuit in Figure 17b

The extra overshoot not only depends on Q_{rr} but also on the "softness" of the recovery (decay ratio). It would be helpful to analyze the influence of the parameters (I_{rrm} and τ_{rr}) by focusing on the upper envelope of the drain-source voltage $\widehat{u_{ds}}(t)$, having $\sup_t \sin(\omega t + \phi) = 1$:

$$\widehat{u_{ds}}(t) = (U_s - R_s I_L)\left[1 + e^{-\frac{R_S}{2L_{Lk,s}}t}\right] + L_{Lk,s} Q_{rr} \frac{\omega_0^2}{1 + \omega_0^2 \tau_{rr}^2}\left[e^{-\frac{t}{\tau_{rr}}} + e^{-\frac{R_S}{2L_{Lk,s}}t}\right] \quad (23)$$

In particular, one can focus only on the term associated with the reverse recovery of the rectifier and plot the upper limit line for the extra overshoot expected. In Figure 19a, a sweep performed on the peak reverse recovery current I_{rrm} clearly shows the extra voltage overshoot increasing with it. In Figure 19b a sweep is done on the reverse recovery current characteristic time of decay. A smaller value for τ_{rr} leads to higher di_{rr}/dt and higher voltage overshoot. The value of τ_{rr}, that is mostly dependent on the silicon technology, affects the "recovery softness factor" (RSF) as defined by JEDEC [5]. To better explain this, it is essential to distinguish between what we called until now "reverse recovery current" i_{rr} and the "*total* reverse recovery current": while the former exclusively accounts for minority charge carriers swept out from the drift region, the latter additionally includes the displacement current in the equivalent output capacitance C_{oss}, associated with the creation of a space charge region able to sustain the voltage. In Figure 20a, the total current i_s in the rectifier (Figure 17b) is plotted together with the displacement current ($-i_{oss}$) and the reverse recovery current ($-i_{rr}$). The *total* reverse recovery current is given by $i_s = -(i_{oss} + i_{rr})$.

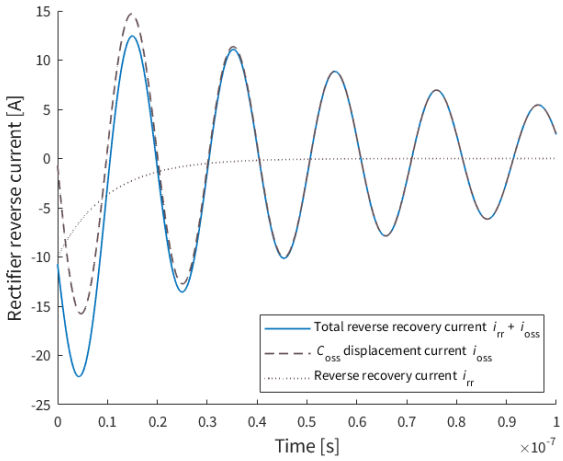


a) Sweeping Q_{rr} for a fixed decay ratio

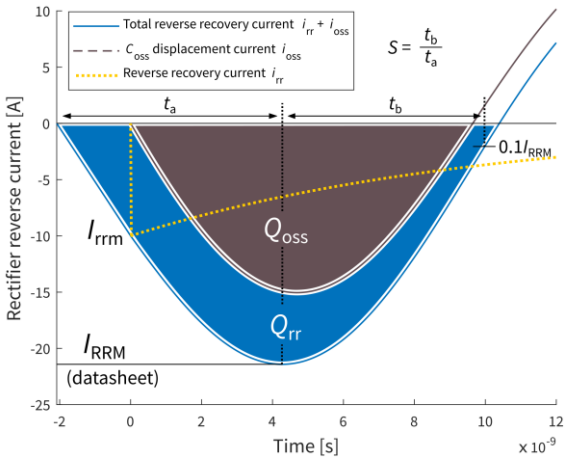
b) Sweeping Q_{rr} for fixed peak reverse recovery current

Figure 19 Extra voltage overshoot due to reverse recovery for different I_{rrm} and τ_{rr} (softness)

When it comes to characterizing the switching performances of a MOSFET operated as a synchronous rectifier, it is not possible to distinguish between displacement and reverse recovery (diffusion) currents, as it is only possible to measure the total current at the source terminal. In datasheets, when the recovered charge Q_{rr} is specified, this always includes a contribution from Q_{oss}, as it is given as the integral over time of the total current measured at the source terminal. In other words, Q_{rr} in datasheets specifies the *total* reverse recovery charge and has nothing to do with the definition given by equation (17) that only *models* the amount of minority carrier charge to be swept out from the drift region. Taking Figure 20b as an example, the value given in the datasheets for the reverse recovery charge Q_{rr} would be the sum of the brown and blue areas, i.e., $Q_{rr(datasheet)} = Q_{rr} + Q_{oss}$. Similar considerations apply for the peak reverse recovery current I_{RRM}, if specified in datasheets, as this will never correspond to the definition of I_{rrm} given in equation (12). From Figure 20b it would also now be possible to understand how τ_{rr} would affect the softness of the recovery: as a higher value for τ_{rr} would slow down the i_{rr} curve decay, and this has the effect of shifting the blue curve down, the current zero crossing will be delayed accordingly and t_b will result in a higher number.



a) Reverse recovery current plotted against the *total* reverse current in the rectifier



b) Focus on definition of charges

Figure 20 Reverse recovery current, C_{oss} displacement current and total reverse recovery current

2.2 Actively clamping the drain-source voltage in synchronous rectifiers

2.2.1 Active clamp basics

There are a variety of solutions typically adopted to keep voltage overshoot on rectifiers under control. Among them it is possible to distinguish between snubbers (made up of passive components only) and voltage clamps making use of controlled switches. Within the passive solutions, both dissipative (simple and polarized RC [6]) and resonant [7] snubbers are used. On the other hand, it is becoming common in modern DC-DC brick power modules to actively clamp the drain-source voltage at the SRs. In any buck or buck-derived topology the drain of the SR MOSFET sees a high impedance (the output filter inductor), meaning that – AC-wise – the drain terminal is left floating, enabling high-frequency oscillations to build up. The idea underlying the active clamp is to tie the drain terminal of the synchronous rectifier to a low impedance voltage source that, in practice, is realized as a large capacitor.

The basic active clamp circuit is shown in Figure 21. The clamp capacitor must be considered pre-charged at its steady-state value, which should be as close as possible to the transformer secondary voltage U_s.

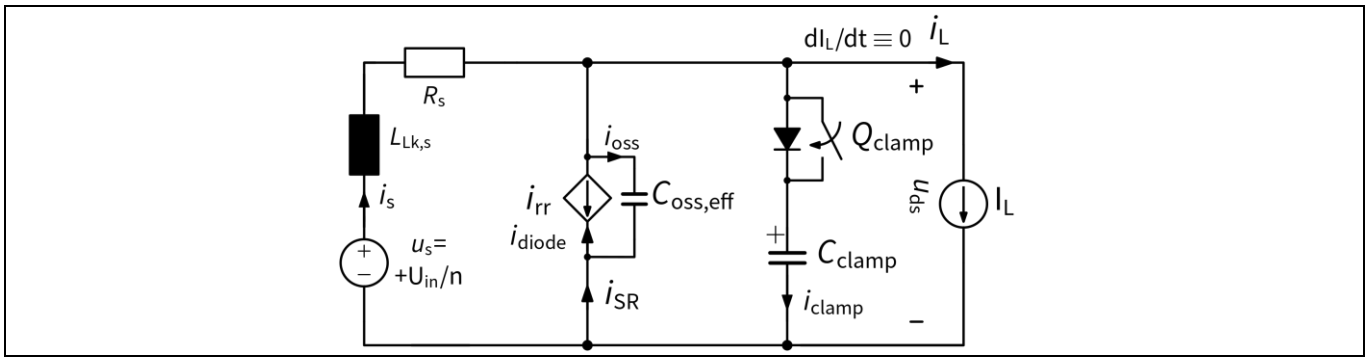


Figure 21 Simple active clamp circuit

The transient analysis starts at $t = 0$, for which $u_{ds}(0) = 0$, $i_s(0) = I_L + I_{rrm}$. The drain-source voltage rises according to equation (21), although with a slightly slowed-down transient, due to the fact that the equivalent output capacitance of the SR MOSFET now sees in parallel the series combination of the clamp capacitance and the output capacitance of Q_{clamp}:

$$C_{eq} = 2C_{oss,eff} + \frac{C_{oss,eff}(Q_{clamp})C_{clamp}}{C_{oss,eff}(Q_{clamp}) + C_{clamp}} \approx C_{oss,eff} + C_{oss,eff}(Q_{clamp}) \qquad 0 \le t \le t_1 \tag{24}$$

At a certain instant of time, say $t = t_1$, the drain-source voltage would reach the clamp capacitor voltage U_{clamp}. This can be estimated by:

$$t_1 = \frac{\sin^{-1}\left(\frac{U_{clamp}}{U + U_{rr}} - 1\right) - \phi}{\omega} \tag{25}$$

Provided that t_1 would result in less than 1/3 of $\min(\alpha, \tau_{rr})$ and where all the above quantities are defined as per equations (13)…(20). This approximation fits well for the case of the Infineon design REF_750W_FBFB_50V.

For $t > t_1$ the body diode of Q_{clamp} will result in it being forward-biased and the clamp capacitor being effectively in parallel with the synchronous rectifier output capacitance:

$$C_{tot} = C_{oss,eff} + C_{clamp} \tag{26}$$

The drain-source voltage will show a sharp change of slope and the resonance frequency will change accordingly. The drain source voltage will continue to rise according to the same law described by equation (11), now having an equivalent capacitance given by equation (26).

In the limit for an infinitely large clamp capacitor (voltage source), the peak overshoot results in being clamped exactly at the steady-state value U_{clamp}. The voltage overshoot expected for a finite value of the clamp capacitance has instead been estimated as follows. Let's assume for the sake of simplicity that the steady-state voltage for the clamp capacitor would be exactly equal to the transformer secondary voltage:

$$U_{clamp} = U_s \tag{27}$$

Then, when the drain-source voltage would equal U_{clamp}, it also happens that the total reverse recovery current in the rectifier would be equal to the peak *total* reverse recovery current. This has always to be true as, looking at the circuit in Figure 17b, the drain-source voltage can only be equal to U_s when:

$$\frac{di_s}{dt} = 0 \Leftrightarrow \frac{di_{SR}}{dt} = 0 \Leftrightarrow i_{SR} = -I_{RRM} \tag{28}$$

Where I_{RRM} stays for the peak *total* reverse recovery current, as already explained in Figure 20b. To estimate the voltage bump at the rectifiers (and at the clamp capacitor) it is then more convenient to study the transient of the circuit in Figure 22, for convenience resetting again $t = 0$. To keep the analysis straightforward, Q_{rr} is neglected this time, while its contribution can be always considered as shown in section 2.1.

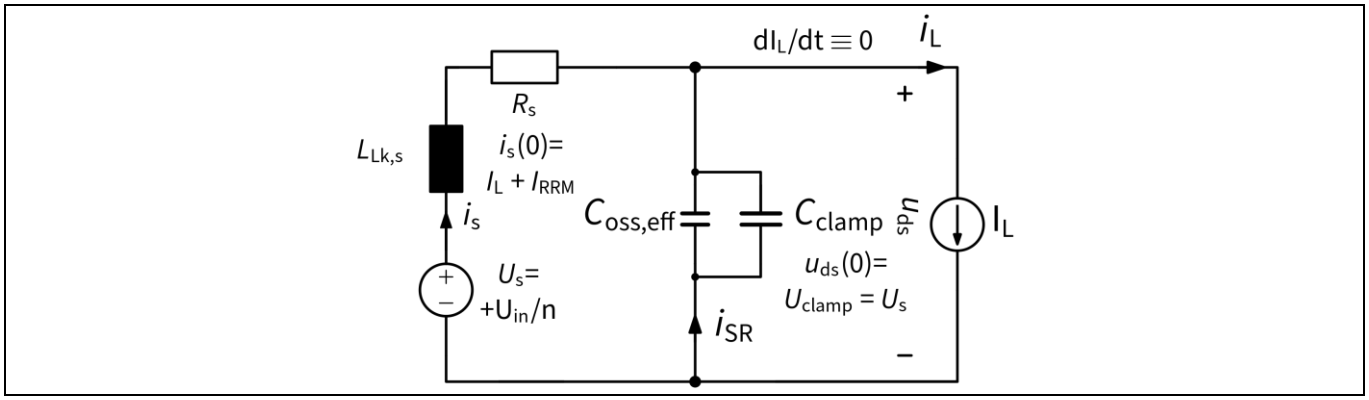


Figure 22 Simplified circuit for active clamp transient analysis

The initial conditions for the new mode of operation will be:

$$\begin{cases} u_{ds}(0) = u_{C_{oss,eff}}(0) = u_{C_{clamp}}(0) = U_{clamp} \\ i_s(0) = I_L + I_{RRM} \Rightarrow \dfrac{du_{ds}}{dt}(0) = \dfrac{I_{RRM}}{C_{tot}} \end{cases} \tag{29}$$

The drain-source voltage will evolve as described by:

$$u_{ds}(t) \approx (U_s - R_s I_L) + I_{RRM}\sqrt{\frac{L_{Lk,s}}{C_{tot}}}\, e^{-\frac{R_s}{2L_{Lk,s}}t} \sin(\omega_c t + \phi) \tag{30}$$

Where:

$$\begin{cases} \omega_c = 1/\sqrt{L_{Lk,s}C_{tot}} \\ \tan\phi \approx \phi = \dfrac{\sqrt{1-\zeta^2}}{\zeta} \dfrac{1}{1 + \dfrac{I_{RRM}}{\alpha R_s C_{tot} I_L}} \end{cases} \tag{31}$$

It is straightforward to find the peak drain-source voltage overshoot expected at the rectifier by finding the maxima of (30). Using the maxima of the envelope is in most of the cases already a reasonable estimation, and this is given by:

$$U_{ds,OV} \approx I_{RRM}\sqrt{\frac{L_{Lk,s}}{C_{tot}}} = \frac{I_{RRM}}{\sqrt{1+k}}\sqrt{\frac{L_{Lk,s}}{C_{oss,eff}}} \tag{32}$$

Being k a per-unit clamp capacitance normalized to $C_{oss,eff}$:

$$C_{clamp} = kC_{oss,eff} \tag{33}$$

This enables sizing of the clamp capacitor according to the maximum allowed overshoot at the rectifiers:

$$k = \left[\frac{I_{RRM}}{U_{ds,OV}\big|_{\max}}\sqrt{\frac{L_{Lk,s}}{C_{oss,eff}}}\right]^2 - 1 \tag{34}$$

Depending on the value of the effective output capacitance of the SR MOSFETs, clamp capacitance values 50 to 100 times greater than C_{oss} can be expected for a design such as Infineon's REF_750W_FBFB_50V.

The need for an active device to implement the clamp is evident, because as soon as the clamped drain source voltage reaches its peak, the current in the clamp capacitor will cross zero and the clamp diode will become reverse biased. A path must be provided for the current in the clamp capacitor to reverse and to guarantee the charge balance. In other words, the clamp capacitor needs to be *reset* by the resonance created with the loop inductance. This path is realized by closing Q_{clamp} sometime after the clamp diode (typically the integral body diode of Q_{clamp}) starts conducting. Typically, this is done by commanding the turn-on of Q_{clamp} after a certain dead time (where equation (25) has to be considered together with other sources of delay) with respect to the primary PWM forcing the turn-off commutation of the rectifiers. Then Q_{clamp} turns on, with ZVS taking over the diode current.

To properly reset the capacitor, the active switch clamp on-time must be selected for the current to perform at least one full resonant cycle. The switch must be turned off with the right timing: to avoid high over voltages building up across the loop inductance, the turn-off must occur when the current clamp current i_{clamp} (Figure 21) is in its positive half-cycle. To reduce the losses in the clamp, the switch on-time should be maximized (to reduce body diode conduction) and it should be turned off some time before the current zero crossing. This guard-band time should consider the tolerances in components and in PCB manufacturing that would affect the clamp resonant frequency. The minimum on-time to allow proper resetting of the capacitor while minimizing the losses in the clamp should be selected as:

$$t_{on,min}(Q_{clamp}) < \frac{5}{2}\pi\sqrt{L_{Lk,s}C_{tot}} - t_{dt,\mathrm{on}} - t_{dt,\mathrm{off}} \tag{35}$$

Where $t_{dt,on}$ and $t_{dt,off}$ are the active clamp switch turn-on and turn-off dead times.

Figure 23 shows how to obtain the expression for the minimum clamp on-time. Meanwhile, Figure 24 shows the effectiveness of the active clamp solution in keeping the voltage overshoot controlled. Figure 24 shows a strategy for which the clamp switch is kept on during the entire powering phase. Depending on the damping ratio, sometimes the on-time given in equation (35) is not sufficient to achieve the charge balance in the clamp capacitor. Whether this would be the case, more than one resonant cycle should be allowed for the reset. The recovered charge Q_{rr} from the clamp switch would be another element – neglected in this analysis – that would alter the charge balance in the clamp capacitor. Please note that the clamp resonant current is reflected on the primary side through the transformer. Although this is wanted, as the energy stored in the leakage is partially

recovered being transferred to the input capacitors, this could compromise the efficiency (larger primary current) or EMC performances of the converter.

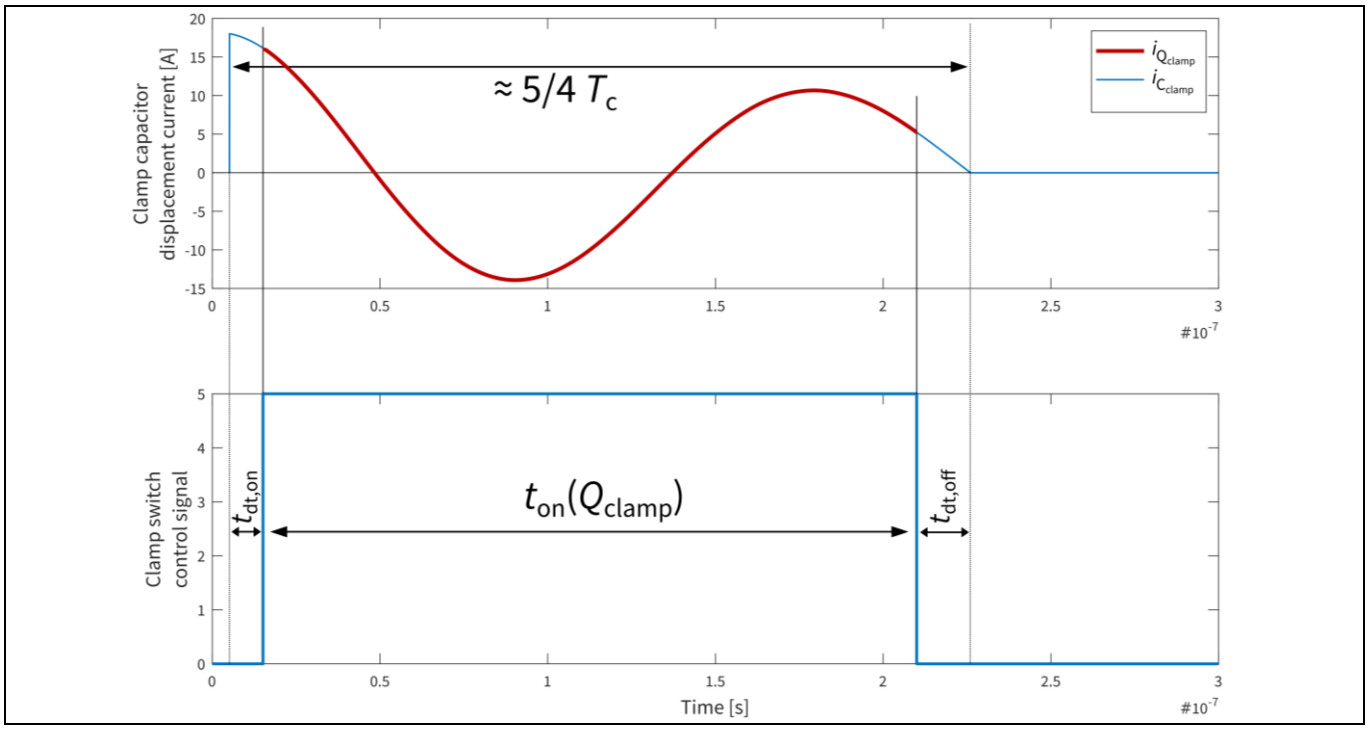


Figure 23 Minimum on-time for the clamp switch to achieve clamp capacitor reset while minimizing clamp conduction losses

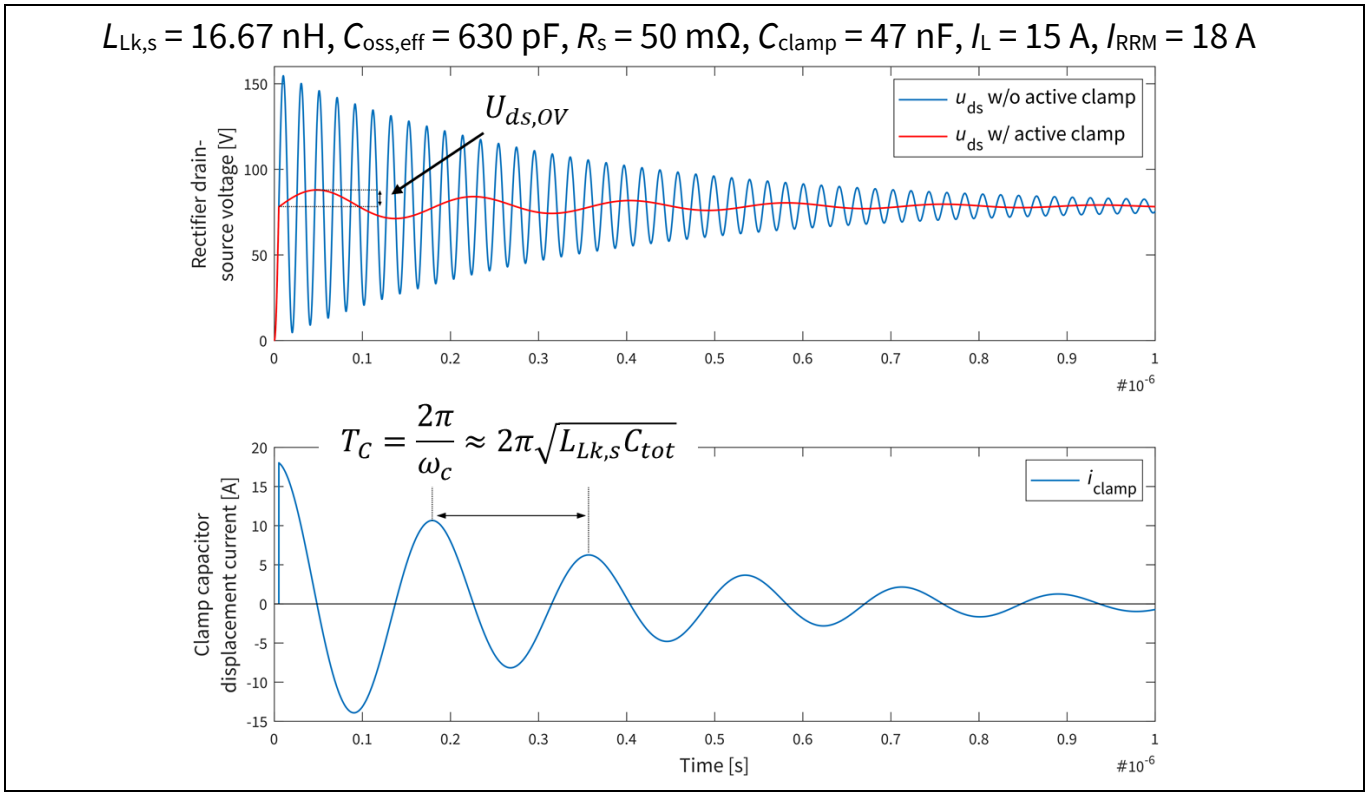


Figure 24 Effectiveness of active clamp to control voltage overshoot in SRs. This case shows a control strategy for which Q_{clamp} is kept on for the entire off-phase of the rectifier

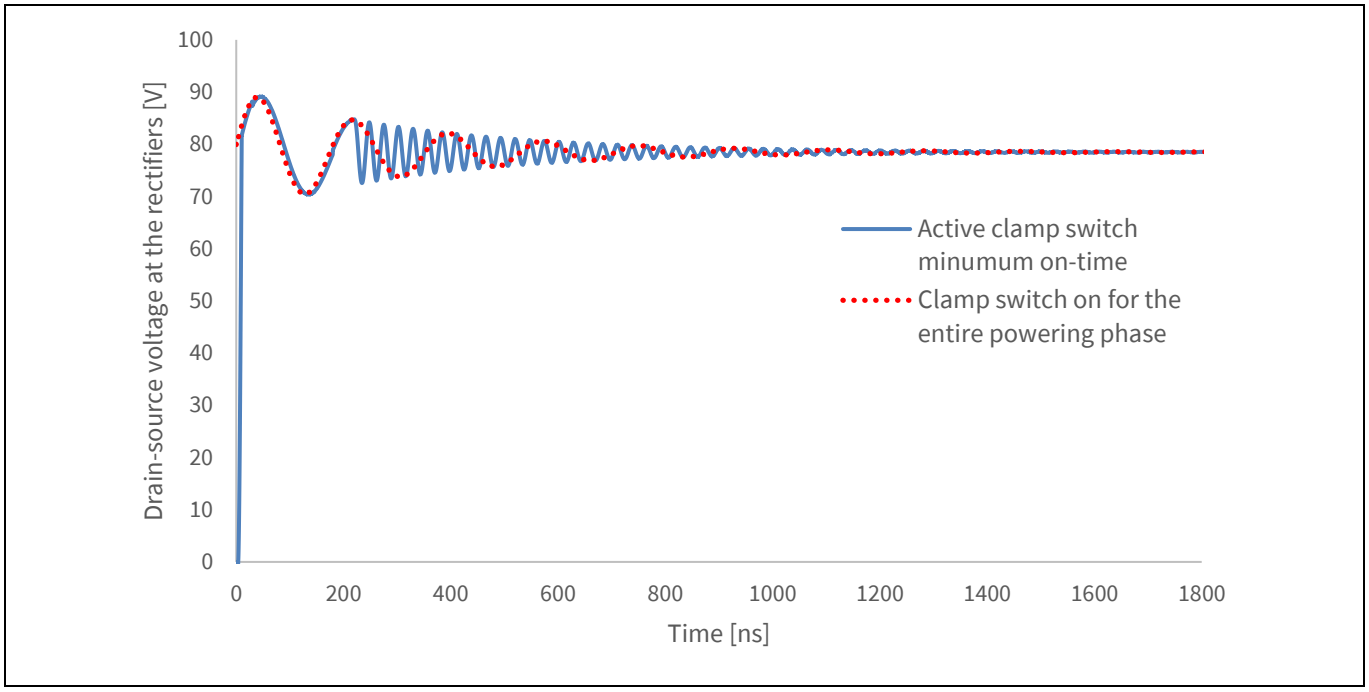


Figure 25 Simulated waveforms for two different control strategies for the active clamp switch control

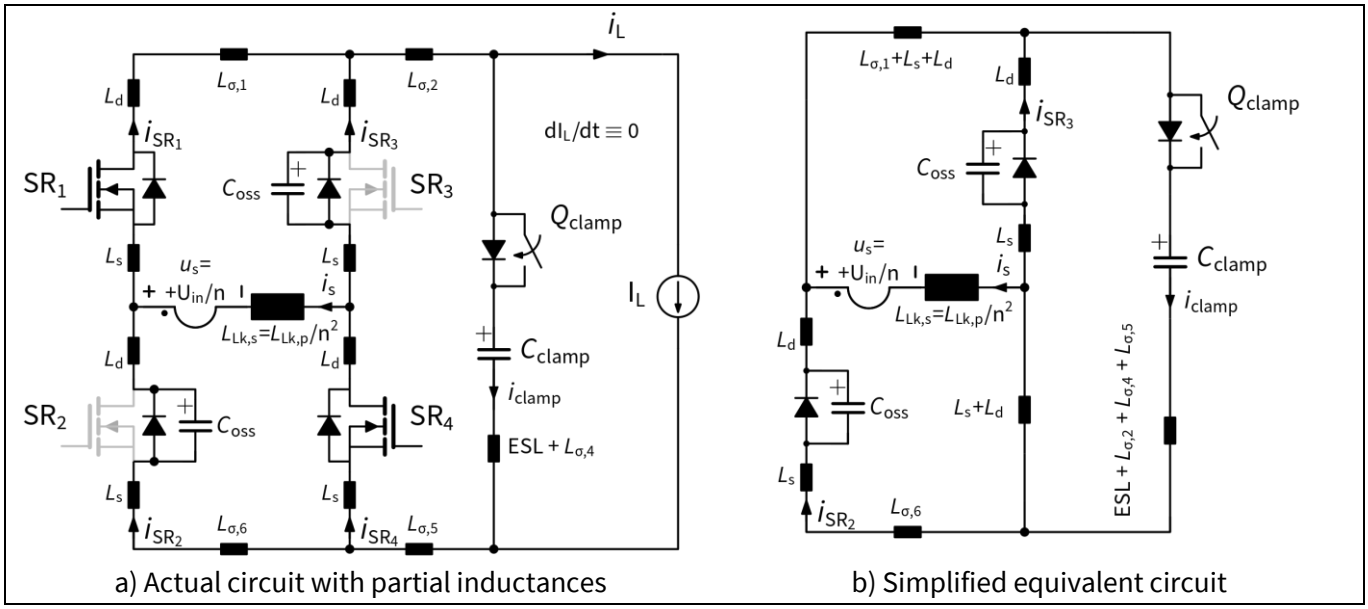
In section 3.4 different options will be given to configure the digital power controller to achieve the desired timing for the clamp, depending on the design. The Infineon reference design REF_750W_FBFB_50V adopts the solution in section 3.4.1, where the active clamp switch is kept on for the entire duration of the powering phase; i.e., the clamp switch and the primary active PWM share the same timing (apart from the necessary dead times).

2.2.2 Active clamp implementation

In practice, for the present reference design that is based on a full-bridge topology coming with a full-wave rectifier, there are different ways to implement active clamping of drain-source voltage for rectifiers. The basic implementation in Figure 21 can be traced back to the actual bridge circuit, following the steps taken from the circuit in Figure 12.

In Figure 26 the full-wave rectifier circuit including the active clamp is shown. Partial inductances related to both packages and PCBs are highlighted. These inductances will partially decouple the clamp capacitor from the drain of the rectifiers SR_2 and SR_3 that are experiencing the turn-off conditions. This will limit the effectiveness of the clamp, because high-frequency oscillatory modes will be superimposed on the waveform shown in Figure 24. The amplitude and frequency of these modes will depend on the value of the stray inductances, which should always be minimized by following best practices in PCB layout. A low-ESL clamp capacitor must also be selected in the actual implementation.

The symmetrical nature of the bridge rectifier is broken by the introduction of the clamp, as shown in Figure 26. In a practical layout, this would probably lead to an arrangement where the active clamp circuit sits closer to a bridge leg.



a) Actual circuit with partial inductances b) Simplified equivalent circuit

Figure 26 Full-wave rectifier including stray, partial inductances related to power discrete packages and PCB layout

This would again limit the effectiveness of the clamp for the leg. At the cost of almost doubling its BOM, a different clamp circuit can be dedicated to each phase node, to reinstate the symmetry of the circuit (Figure 27).

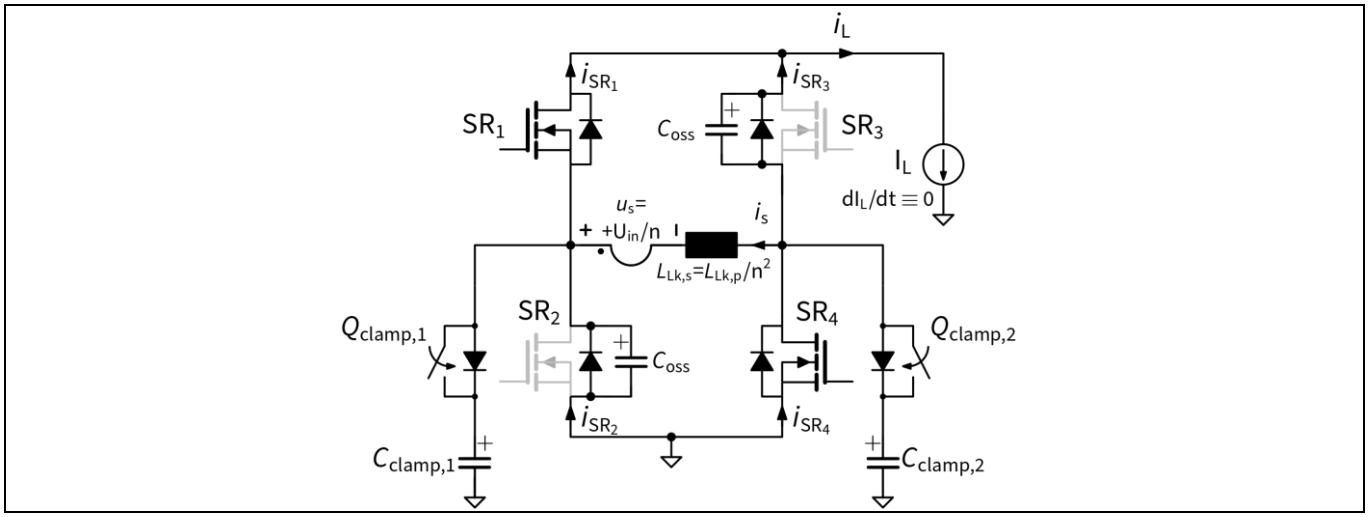


Figure 27 Full-bridge rectifier with a dedicated active clamp circuit for each phase node

When it comes to an actual realization of the clamp switches, there are two options typically adopted. In both cases, for the Infineon reference design REF_750W_FBFB_50V, the switches should be selected to block voltages as high as 150 V.

1. *P-channel MOSFET*: The advantage of using a P-channel MOSFET for the realization of Q_{clamp} comes from the possibility of using a single, dual-channel (to drive the clamp switches off both legs) low-side gate driver referred to a secondary power ground. The clamp RMS current is typically low, especially when the clamp on-time is kept at its minimum. So, the penalty in the higher area-specific on-state resistance of a P-channel MOSFET is generally not an issue, and even the smallest surface-mount packages could fit the application.

The P-channel MOSFET requires an AC-coupled gate drive scheme, as shown in Figure 28, to implement the required level shifting (C_{ls}, R_{gs}, D_{gs}) for the gate-to-source voltage. The PWM control signal needs to be complementary to the one intended for a conventional N-channel MOSFET drive.

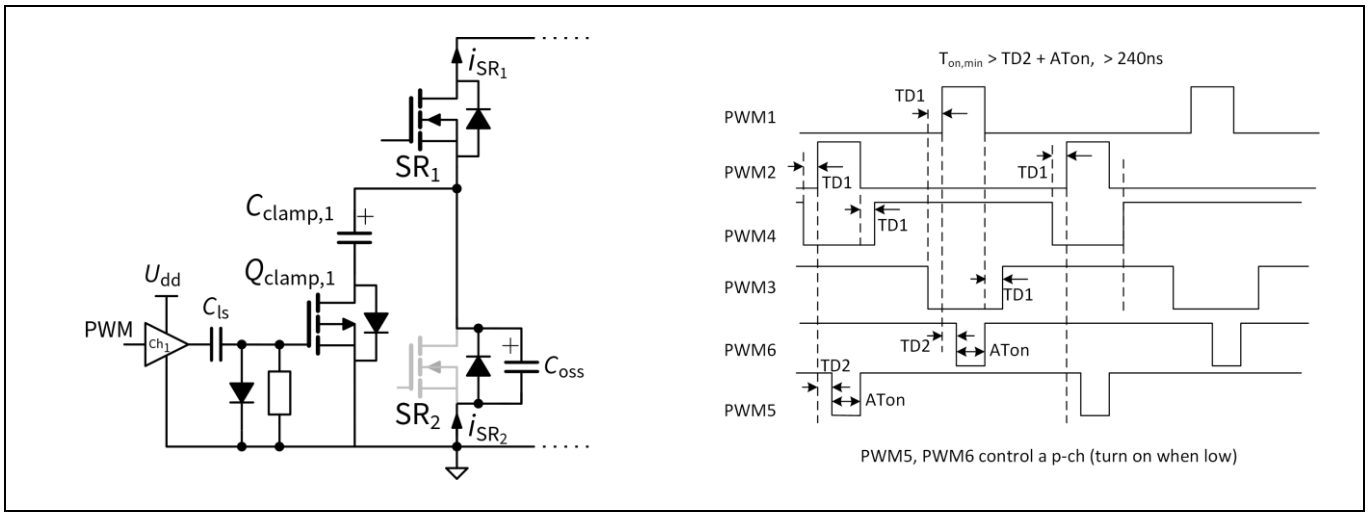


Figure 28 Active clamping implementation with P-channel MOSFET. Focus is only on one leg of the full-bridge

2. *N-channel MOSFET*: Another possible solution uses an N-channel MOSFET for the realization of Q_{clamp}. In this case, a broader portfolio of devices can be selected, especially in the 150 V voltage class. The penalty here is paid in the BOM and in the PCB real estate, as the driving requires two high-side drivers or a dual-channel isolated driver. Bootstrapping of two power supplies is also required.

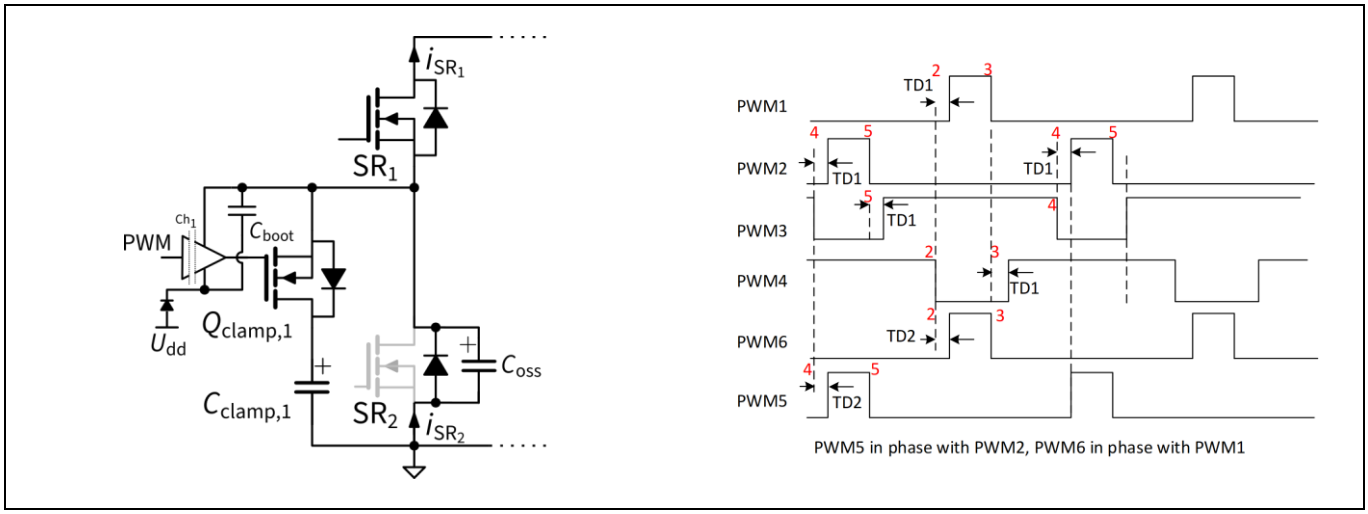


Figure 29 Active clamping implementation with N-channel MOSFET. Focus is only on one leg of the full-bridge

The solution using the N-channel MOSFET is the one chosen for the Infineon reference design REF_750W_FBFB_50V. The clamp MOSFETs are selected to be the same as the SR MOSFETs, namely OptiMOS™ 5 150 V, 11 mΩ $R_{DS(on),max}$ BSC110N15NS5.

Clamp MOSFETs are driven by the dual-channel isolated gate driver EiceDRIVER™ 2EDF7275K.

3 XDP™ XDPP1100 digital power controller configuration

3.1 Topology and transformer turns ratio

In the XDPP1100 graphical user interface (GUI) “Topology” design tool, configure the topology to full-bridge primary and full-bridge secondary, mapping the PWMs per HW connection. Please note that the XDPP1100 only supports step-down type transformers by default, i.e., the transformer turns ratio $n = N_p:N_s$ must be higher than 1. Thus in Figure 30 the transformer turns ratio is set to 1.001.

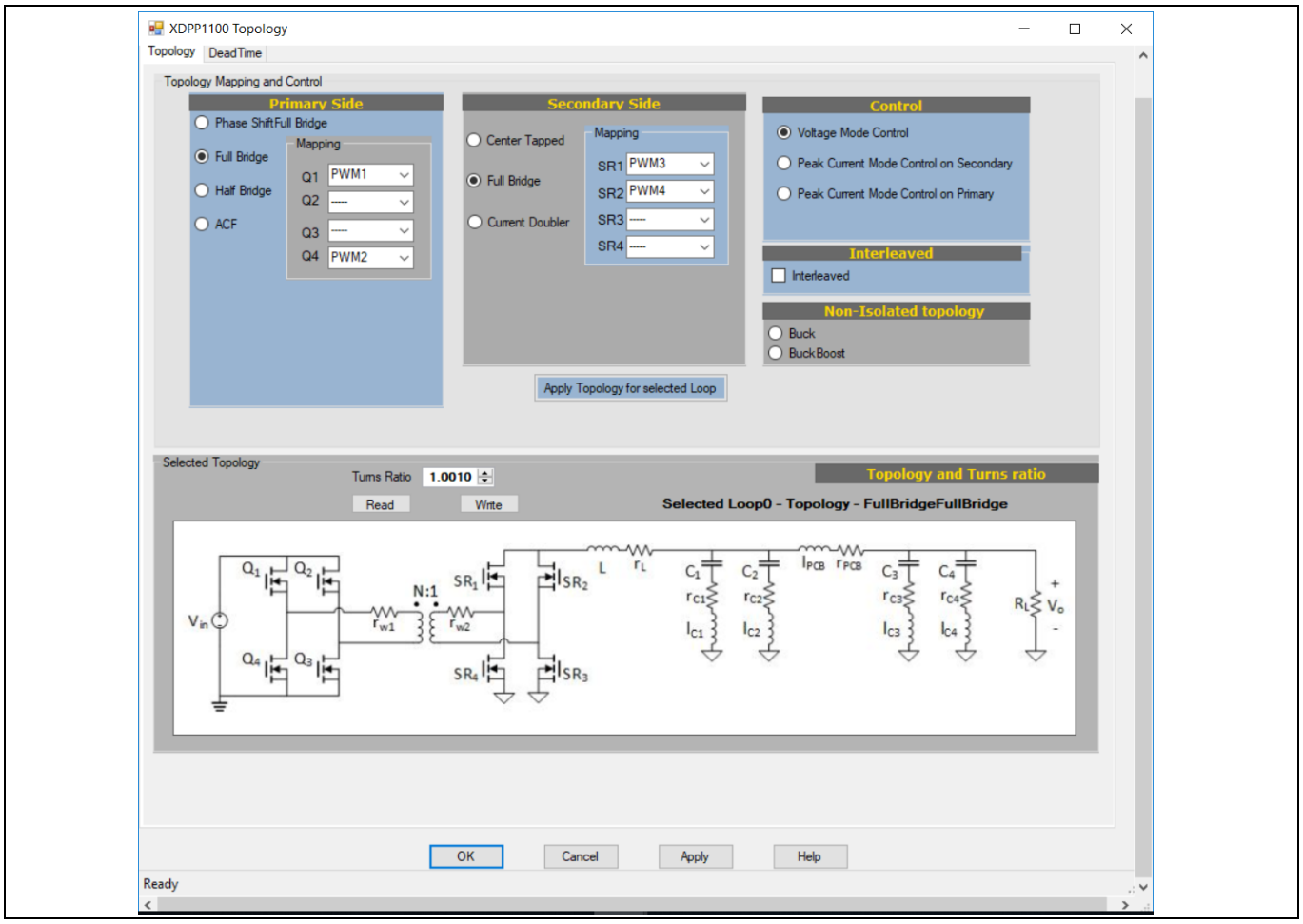


Figure 30 Full-bridge/full-bridge topology and transformer turns ratio

The transformer turns ratio configures the PMBus command MFR_TRANSFORMER_SCALE, which is defined as $N_s:N_p$ and is calculated by 1/(turns ratio). Thus MFR_TRANSFORMER_SCALE = 0.999.

Since the MFR_TRANSFORMER_SCALE is used for V_{RECT} input voltage sensing, if the value is not accurate, it affects V_{IN} telemetry and input voltage feed-forward. To support the operation with step-up ratios for the transformer, a purposely programmed FW patch introduces a parameter MFR_ADJ_TURN_RATIO, as will be shown in the following sections.

3.1.1 Input voltage (V_{IN}) telemetry by VRSEN

This board supports using either VRSEN or PRISEN for input voltage sensing. The use of VRSEN (**tlm0_vin_src_sel** = 0) shows better performance in terms of accuracy. Table 5 shows the difference between VRSEN and PRISEN. The drawback of VRSEN sensing is that it is not possible to sense the input voltage during

standby operation of the power stage. This issue can be solved by an FW patch, which uses PRISEN during the off-state and switches to VRSEN when the converter starts switching.

Table 5 VSEN/VRSEN vs. PRISEN

	ADC	Sample rate [Msps]	Resolution [mV]	Range [V]
VSEN/VRSEN/BVRSEN (VADC)	11 bit	100	1.25	0 to 2.1
PRISEN (TS ADC)	9 bit	1 (shared with other channels)	2.344	0 to 1.2

The V_{IN} telemetry block diagram is shown in Figure 31. Here, we are interested in the case **tlm0_vin_src_sel** = 0 (VRSEN with **vrs_voltage_init** applies prior to start-up). As highlighted in the block, the two key signals are **vsp1_vs_vrect_fs** and **tlm0_vin_convert_factor**.

The **vsp1_vs_vrect_fs** is the VRSEN ADC measured voltage. The **tlm0_vin_convert_factor** is determined by MFR_VRECT_SCALE and MFR_TRANSFORMER_SCALE. It is proportional to 1/(MFR_VRECT_SCALE* MFR_TRANSFORMER_SCALE). Based on this fact, increasing the MFR_VRECT_SCALE by 1.667 could compensate for the error arising from MFR_TRANSFORMER_SCALE due to the maximum value limit.

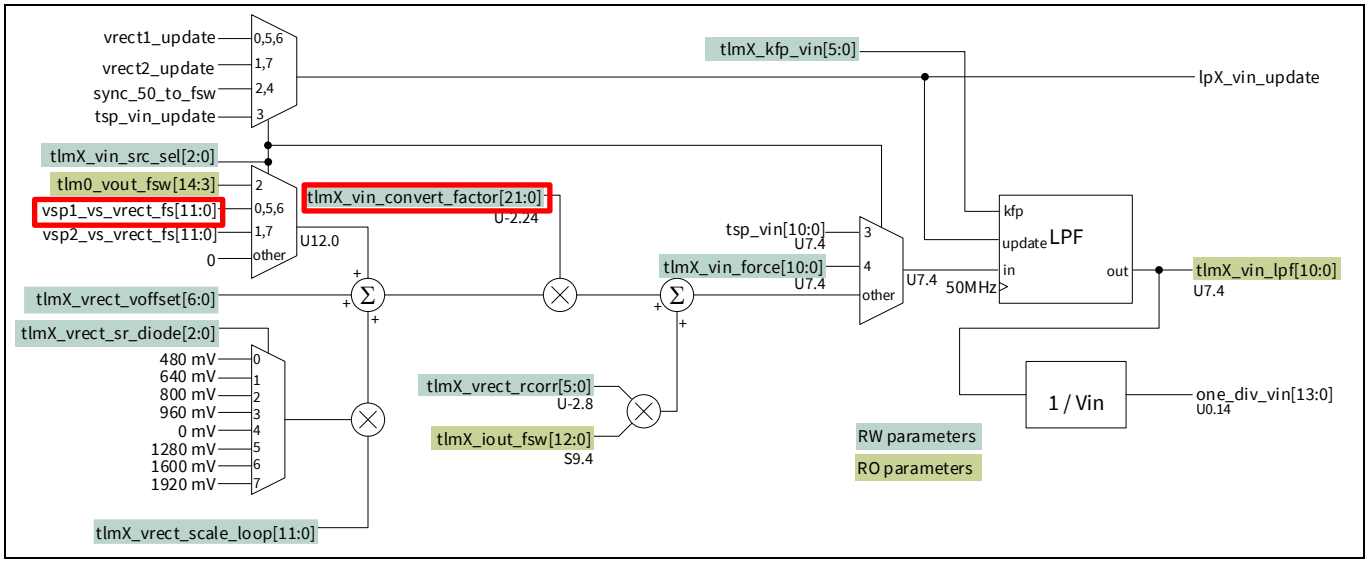


Figure 31 Input voltage telemetry block diagram

There are two options to configure the parameters:

1. The MFR_VRECT_SCALE can be calculated using the following equation. This works without FW patch:

$$\text{MFR\_VRECT\_SCALE} = 1.667 \times \frac{R71}{R71 + R72}$$

2. Keep the MFR_VRECT_SCALE matching the R71 and R72 divider ratio and use the FW patched command MFR_ADJ_TURN_RATIO to correct the error. This requires an FW patch.

$$\text{MFR\_VRECT\_SCALE} = \frac{R71}{R71 + R72}$$

$$\text{MFR\_ADJ\_TURN\_RATIO} = 1.667$$

Here, the MFR_ADJ_TURN_RATIO takes the Linear11 data format. Use the “linear format calculator” tool that comes with the GUI to calculate the value. Type in the decimal value, choose the desired exponent number,

then click the right arrow to get the hex number. MFR_ADJ_TURN_RATIO = BB56 would set the turns ratio adjustment to 1.667.

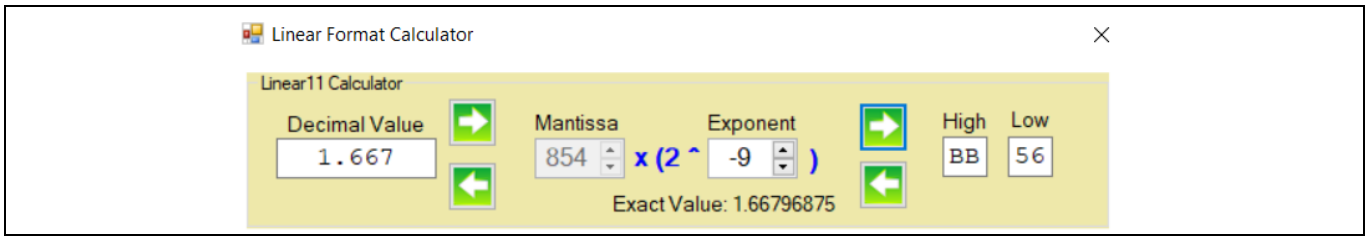


Figure 32 Linear format calculator

Both options would set the register **tlm0_vrect_scale_loop** = 100 with resistor divider ratio 0.0145.

The following registers and PMBus commands are configured for input voltage sensing by VRSEN.

Table 6 PMBus commands and registers for VRSEN

Register/command name	Value	Comments
tlm0_vin_src_sel	0	VRSEN. Input voltage is defined by vrs_init prior to start-up.
Vsp1_vrs_sel	1	Config VRSEN to V_{RECT} sense mode
vrs_cmp_wdt_thr	10	V_{RECT} comparator watchdog timeout threshold set to 100 ns
vrs_track_start_thr	35	V_{RECT} tracking start time threshold, set to 350 ns. The vrs_track_start_thr – vrs_cmp_wdt_thr must be more than 250 ns.
Vrect_div_2_sel	1	Set to 1 for bridge topology
vrs_voltage_init	59	Configure the VRS initial voltage
MFR_TRANSFORMER_SCLAE	0.999	Set transformer turns ratio to the maximum allowed value
MFR_VRECT_SCALE	0.014648	VRSEN resistor divider ratio. Please see note.
MFR_ADJ_TURN_RATIO	BB56	Set transformer turns ratio adjustment to 1.668
tlm0_vrect_rcorr	34	LSB = 3.90625 mΩ
tlm0_vrect_offset	0	

Note: This configuration is based on MFR_ADJ_TURN_RATIO = 1.667 with FW patch.

The equation of the **vrs_voltge_init** is the following:

$$\text{vrs\_voltge\_init} = V_{\text{IN,nom}} \cdot \text{MFR\_TRANSFORMER\_SCALE} \cdot \text{MFR\_VRECT\_SCALE} \,/\, 20\ \text{mV}$$

Where here the product (MFR_TRANSFORMER_SCALE * MFR_VRECT_SCALE) equals (MFR_TRANSFORMER_SCALE * MFR_VRECT_SCALE * MFR_ADJ_TURN_RATIO) with FW patch.

To improve the accuracy of the input voltage telemetry, the XDPP1100 offers HW-based compensation for VRSEN. The voltage drop on transformer DC resistance (DCR), copper trace DCR, and $R_{DS(on)}$ of SR MOSFETs can be compensated by register **tlm_vrect_rcorr**. This register defines the total equivalent DC resistance of the V_{RECT} sensing loop that reflects to primary. The V_{IN} telemetry is compensated by **tlm_vrect_rcorr** * I_{OUT}.

The voltage offset can be compensated by register **tlm_vrect_offset**. The V_{IN} telemetry is compensated by **tlm_vrect_offset**/(MFR_VRECT_SCALE *MFR_TRANSFORMER_SCALE).

3.1.2 Input voltage (V_{IN}) telemetry by PRISEN

The board has another option to sense the input voltage from the auxiliary transformer secondary winding through the resistor divider at the PRISEN pin ("Vin_Sec" in Figure 33 is connected to the PRISEN pin).

The benefit of using PRISEN instead of VRSEN for input voltage sensing is that the PRISEN is always available if the auxiliary power supply is in regulation. It is useful when the main converter is not switching and the VRSEN is not available.

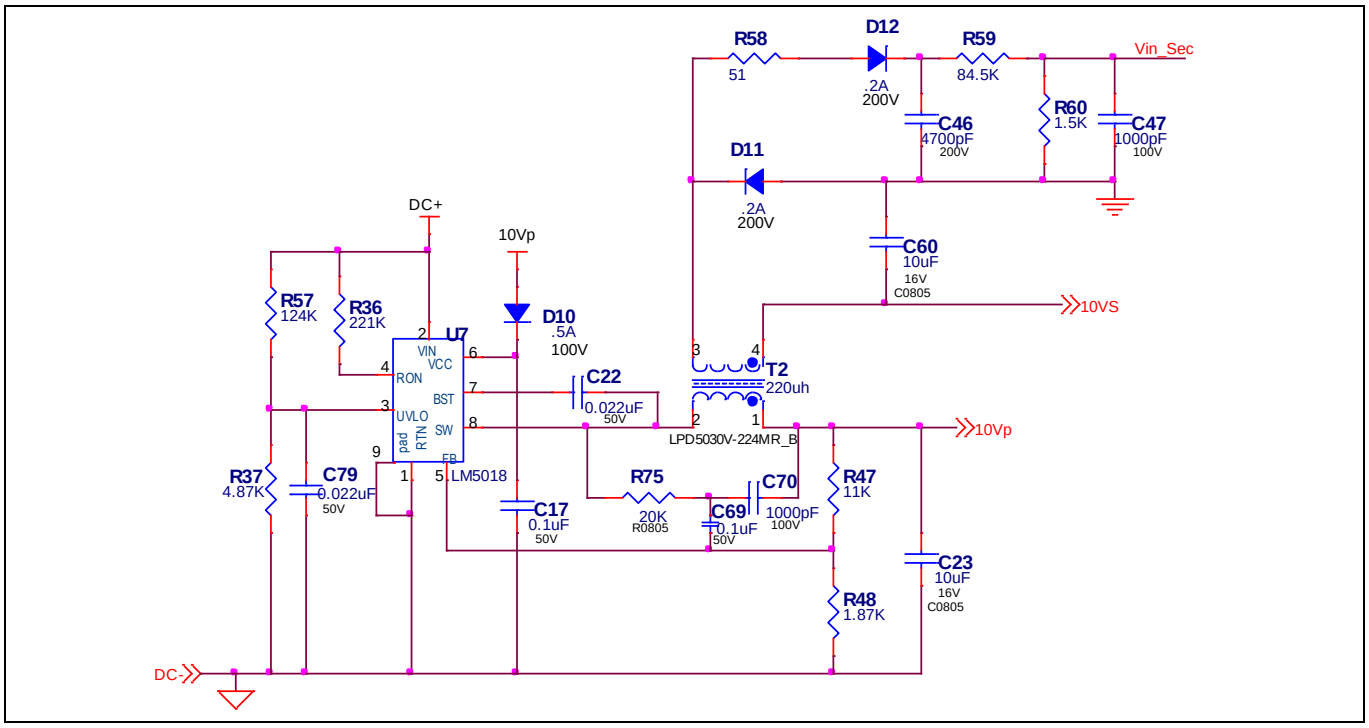


Figure 33 PRISEN input voltage sensing

The following registers are configured for input voltage sensing through PRISEN.

Table 7 PMBus commands and registers for PRISEN

Register name	Value	Comments
tlm0_vin_src_sel	3	TS ADC V_{IN}. Input voltage is sensed at PRISEN pin.
vin_pwl_slope	2207	LSB = 2^-14
vin_trim	0	V_{IN} = ADC * vin_pwl_slope * 2^-14 + vin_trim LSB = 62.5 mV

The **vin_pwl_slope** assumes a linear slope of the PRISEN signal, which is proportional to the input voltage V_{IN}. The **vin_pwl_slope** can be calculated by the following equation:

$$\text{vin\_pwl\_slope} = \frac{1.2 \times 2^5}{\text{PRISEN\_SCALE}}$$

The PRISEN resistor divider ratio is set to 1.5 / (84.5 + 1.5) = 0.0174:

$$\text{vin\_pwl\_slope} = \frac{1.2 \times 2^5}{0.0174} = 2207$$

The V_{IN} telemetry offset can be configured by **vin_trim** register.

3.1.3 Feed-forward

The XDPP1100 computes a feed-forward duty cycle based on input voltage and output voltage. The result is added to the feedback loop PID filter output to resolve the PWM duty cycle. Figure 34 shows the feed-forward block diagram.

$$\text{computed\_feed\_forward} \propto \frac{V_{\text{OUT,target}}}{V_{RECT}} = \frac{V_{\text{OUT,target}}}{\frac{V_{\text{IN}}}{n}} = \left(\frac{N_p}{N_s}\right)\frac{V_{\text{OUT,target}}}{V_{\text{IN}}}$$

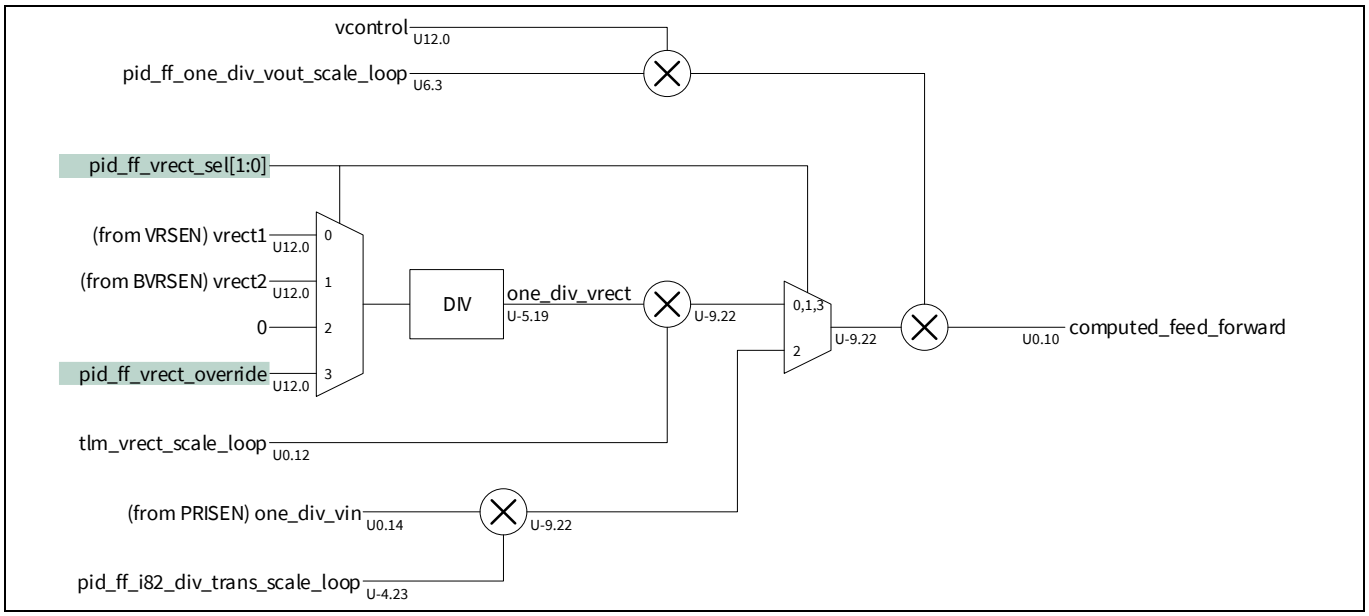


Figure 34 XDPP1100 feed-forward computation

Here there are the options to use either VRSEN or PRISEN as the input voltage source for feed-forward computation. It shows that the **tlm_vrect_scale_loop** affects the feed-forward calculation when VRSEN is selected. And the **pid_ff_i82_div_trans_scale_loop** affects the PRISEN-based feed-forward.

The **tlm0_vrect_scale_loop** is modified by a factor of 1.677 in the V_{IN} telemetry configuration to compensate the transformer scale error. Thus, the feed-forward duty-cycle will be wrong with the present configuration. To correct the error, **pid_ff_one_div_vout_scale_loop** must also update by a factor of n = 1/1.677. Because this register is not used in any other circuit, it is safe to change the value.

The **pid_ff_i82_div_trans_scale_loop** is calculated by 1/MFR_TRANSFORMER_SCALE. Due to the superior limit (0.999, see section 3.1) of MFR_TRANSFORMER_SCALE, the product (**one_div_vin** * **pid_ff_i82_div_trans_scale_loop** ≈ **one_div_vin**) needs to be scaled to match the actual $1/V_{RECT}$ value. This again can be corrected by the **pid_ff_one_div_vout_scale_loop** by a factor of n = 1/1.677.

Based on the above analysis, the feed-forward could work properly by reducing the **pid_ff_one_div_vout_scale_loop** by a factor of 1/1.677. The adjustment is implemented in the FW patch and the user just needs to configure the MFR command MFR_ADJ_TURN_RATIO to BB56.

The product **vcontrol** * **pid_ff_one_div_vout_scale_loop** is clamped to U16.0. Thus, to use the HW-based feed-forward, the maximum output voltage is limited to (2^16-1) * 1.25 mV = 81.92 V. Here 1.25 mV is the LSB of the voltage sense ADC. This limitation does not apply if using FW-computed feed-forward override.

3.1.4 PID coefficients scaling

The PID coefficients are scaled with V_{RECT} to maintain a constant loop gain despite the input voltage variations. The user can define a reference V_{RECT} voltage through the register **pid_vrect_ref**, at which the gain scale is 1.0. This coefficient scale factor is defined as follows:

$$\text{Coefficients scale factor} = \frac{V_{\text{RECT}}}{\text{pid\_vrect\_ref}}$$

The register **pid_vrect_ref** value should be set to the expected nominal V_{RECT} voltage prior to the PID coefficient optimization.

As the V_{RECT} is calculated by VRSEN/tlm0_vrect_scale_loop, and the **tlm0_vrect_scale_loop** is corrected by a factor of 1.667, we should also put 1.667 to the **pid_vrect_ref** equation.

$$\text{pid\_vrect\_ref} = \frac{48\ \text{V}}{\frac{3}{5} * 1.667 * 0.32\ \text{V}} = 150$$

3.1.5 Fast transient response (FTR) and ftr_vin_thresh configuration

In FTR mode, the controller maximizes the duty cycle when a positive load step is detected. This is obtained by reducing the switching period from the programmed T_{switch} to $2T_{on}$, where T_{on} is given below:

$$T_{on} = \left(\frac{T_{switch}}{2}\right) * \left(\frac{V_{OUT}}{V_{RECT}}\right)$$

At high V_{RECT} where the “on-time” inductor current slope is higher, it is possible to reduce T_{on} in proportion to (1 / V_{IN}). This is performed by programming a threshold value in the register **lpX_ftr_vin_thresh**, where:

- Below the threshold, the fast-transient T_{on} is based on the feed-forward duty cycle from the PID (i.e., V_{OUT} / V_{RECT}) and T_{on} is as defined in the above equation.
- Above the threshold, the fast-transient T_{on} is reduced in proportion to V_{IN} and T_{on} is as follows:

$$T_{on} = \left(\frac{T_{switch}}{2}\right) * \left(\frac{V_{OUT}}{V_{RECT}}\right) * \left(\frac{\text{lp0\_ftr\_vin\_thresh}}{V_{IN}}\right)$$

In the T_{on} equation, the product $\left(\frac{T_{switch}}{2}\right) * \left(\frac{V_{OUT}}{V_{RECT}}\right)$ should be taken as a whole unit. It represents the PWM on-time in the steady-state before entering FTR mode at the given V_{OUT} and V_{IN} (i.e., V_{RECT}). The **lp0_ftr_vin_thresh** should be set to the true V_{IN} threshold, being the input voltage telemetry already corrected in the V_{IN} telemetry configuration. For instance, if the duty cycle started reducing at 60 V input in FTR mode, set the **lp0_ftr_vin_thresh** to 60 V.

3.2 Output current (I_{OUT}) sense

The output current is sensed at the return path of the output through a precision shunt resistor. The shunt is placed before the output capacitors to sense the I_{OUT} current with ripple (inductor current). The resistance value selected is 0.5 mΩ to keep the power loss on the resistor low. A precision op-amp is placed very close to the sense resistor to amplify the signal by a gain of 200 (V/V). The amplified signal is then divided by R70 (100 Ω), R19 (20 Ω), and R79 (100 Ω) at the input of the XDPP1100 ISEN pin. Thus, the equivalent I_{OUT} sense resistor is $R_{sense,eq}$ = 0.5 (mΩ) x 200 (V/V) x 0.091 = 9.1 mΩ.

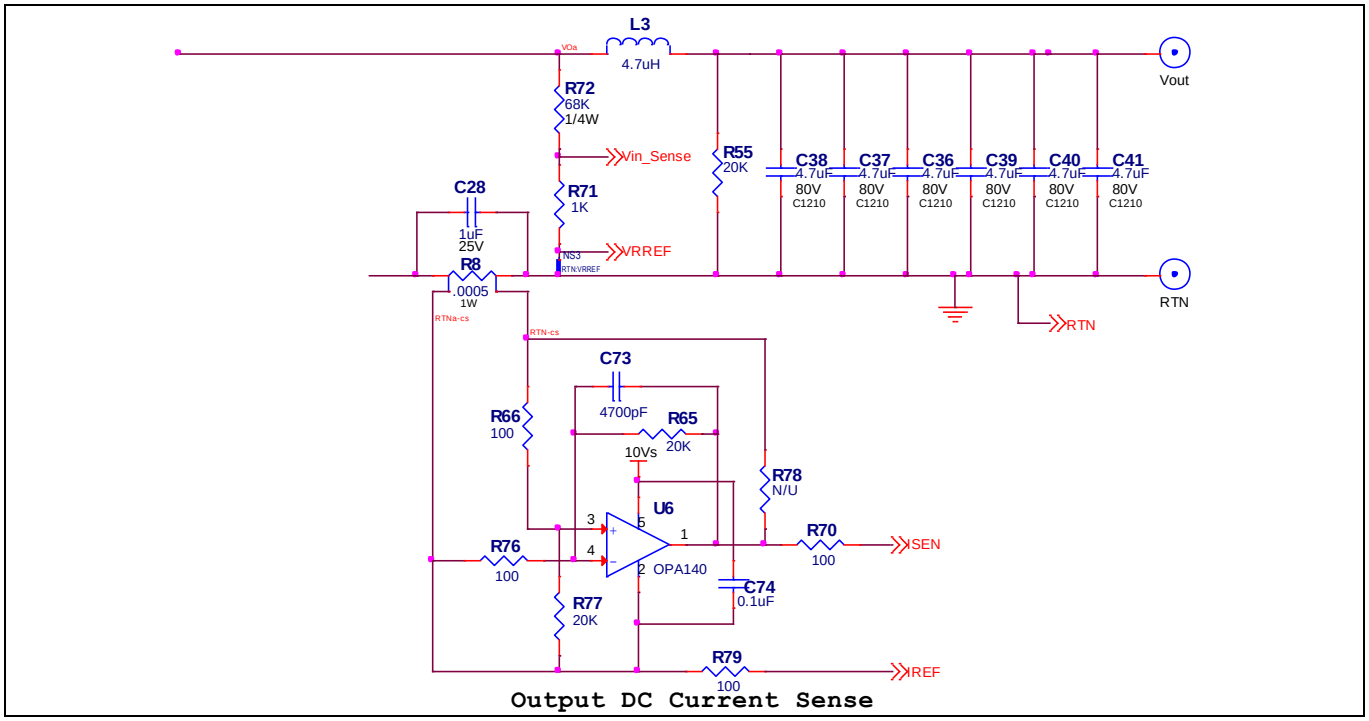


Figure 35 Output current sense

Table 8 PMBus commands and registers for I_{OUT} sense

Command/register name	Value	Comments
MFR_IOUT_APC	0.16 A	–
IOUT_CAL_OFFSET	0 A	–
isen1_gain_mode	2	Choose ISEN ADC LSB 1.45 mV
ce0_ktrack_hiz	1	Set current sense tracking gain in Hi-Z state
ce0_ktrack_off	8	Set current sense tracking gain in off-state
ce0_ktrack_on	4	Set current sense tracking gain in on-state
ce0_kslope_didv	1	Output inductor (L_{out}) current sense slope estimator setting. Set to '1' to minimize the effort of the current estimation and purely rely on ADC sensing.

The equation of MFR_IOUT_APC is:

$$\text{MFR\_IOUT\_APC} = \text{ISEN\_LSB}/R_{\text{sense,eq}}$$

The ISEN_LSB is the resolution of I_{ADC}, which is determined by the **isen1_gain_mode register**. In this demo, the ISEN_LSB is set to 1.45 mV (**isen1_gain_mode** = 2).

The secondary MFR_IOUT_APC = 1.45 mV/9.1 mΩ = 0.16 A.

The equation of **ce0_kslope_didv**:

$$\text{ce0\_kslope\_didv} = \frac{1\ (\text{V}) \cdot 10\ (\text{ns})}{L_{\text{out}}\ (\text{nH}) \cdot \text{APC}\ (\text{A})} \times 2^{13}$$

3.3 Firmware patch and configuration

The transformer turns ratio adjustment is implemented by the FW patch. This section shows how to load the patch and configure the patched command. The procedure assumes that there is no active patch in OTP or RAM, otherwise invalidating the old patch is required before storing a new patch.

3.3.1 Load patch

The “FW Patch” tool defines the OTP memory partition, as well as supports loading and managing of the FW patch and configuration.

3.3.1.1 OTP partition

Before writing the FW patch, the user should check if the OTP memory has been properly partitioned. The XDPP1100 has 64 kB OTP memory, which can be partitioned in up to 17 sections. The OTP Section 0 is used for user data such as design configuration. Sections 1 to 16 are for FW patch. The default setup partitions OTP into two sections, data takes 16 kB (0x4000 hex = 16384 dec = 16 kB), and an FW patch reserves 48 kB. The user can change the partitions according to application requirements. Clicking on “Store Trim” will save the new partition.

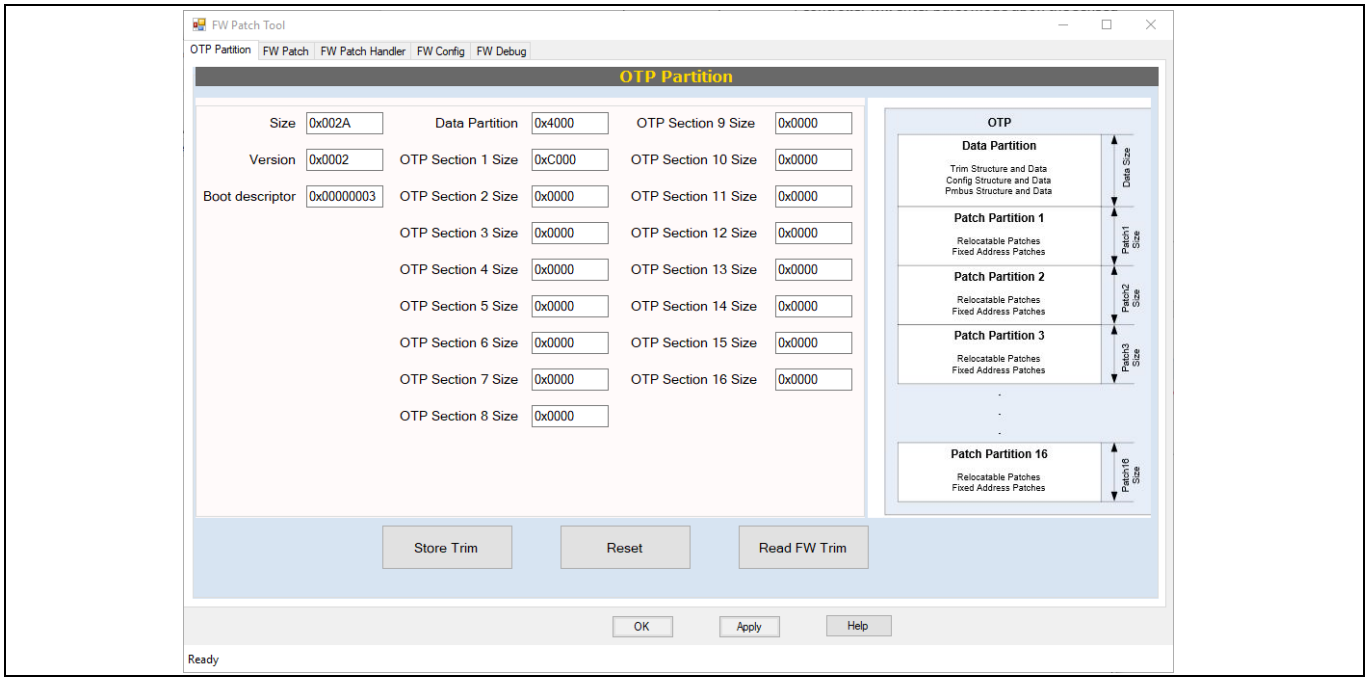


Figure 36 “OTP Partition” tool

3.3.1.2 Store FW patch

The “FW Patch” tab helps to load and store the FW patch. The patch can be stored in RAM or OTP. When debugging the patch code, storing the patch to RAM is recommended: this allows unlimited time for modification. Once the FW patch code is verified and finalized, the user can store it to OTP so the IC can execute the patch after the power cycle.

To store a patch to RAM, the size of the patch should be less than 8 kB. If larger than 8 kB, it should be broken into small modules to be verified by RAM. When all the patch modules are tested, they can be combined into one big patch and stored into OTP. The GUI will calculate the remaining size in the selected partition after storing the patch to OTP. It is recommended to disable the automatic telemetry update when storing to OTP.

3.3.1.3 FW patch handler

After loading the OTP patch, go to the “FW Patch Handler” tab. Click the “Find Active Patch” button, and the GUI should show the active patch just loaded with its address and size information.

The “Find Trim and Config” button is used to check if any register and PMBus configurations are stored in OTP.

A warning message will pop up if the user is trying to load a patch to a partition that has an active patch. Only one active patch is allowed in each OTP partition. The user can use the “Invalidate” button to deactivate the previous FW patch before loading a new patch. The PMBus config will also be invalidated when invalidating a patch, because the patch might have MFR PMBus commands, which is going to alter the number of PMBus commands and the PMBus structure. Thus, the sequence of storing the patch and configuration should be storing the patch first, then storing the configuration.

3.3.2 Load PMBus spreadsheet

To enable configuration of the patched command, go to the “MFR Commands” tab in the PMBus configuration section and load the PMBus Excel file. Each FW patch project will have its own PMBus Excel file that includes the patched commands. In the Excel file, the patched PMBus command will have column *F* “MFR” labeled “y”, and column *G* “Loop 0 support” or column *L* “Loop 1 support” also labeled “y”. Click the “Load PMBus Spread sheet” button and open the PMBus Excel file that comes with the patch. The GUI will update the command list and the patched command can be configured through the “Read/Write” buttons.

In this design, write MFR_ADJ_TURN_RATIO = BB56.

Note: *If the patch is not stored in OTP or RAM, the MFR PMBus command will show an invalid message when performing read/write operations. The patched PMBus commands are only valid with an active FW patch.*

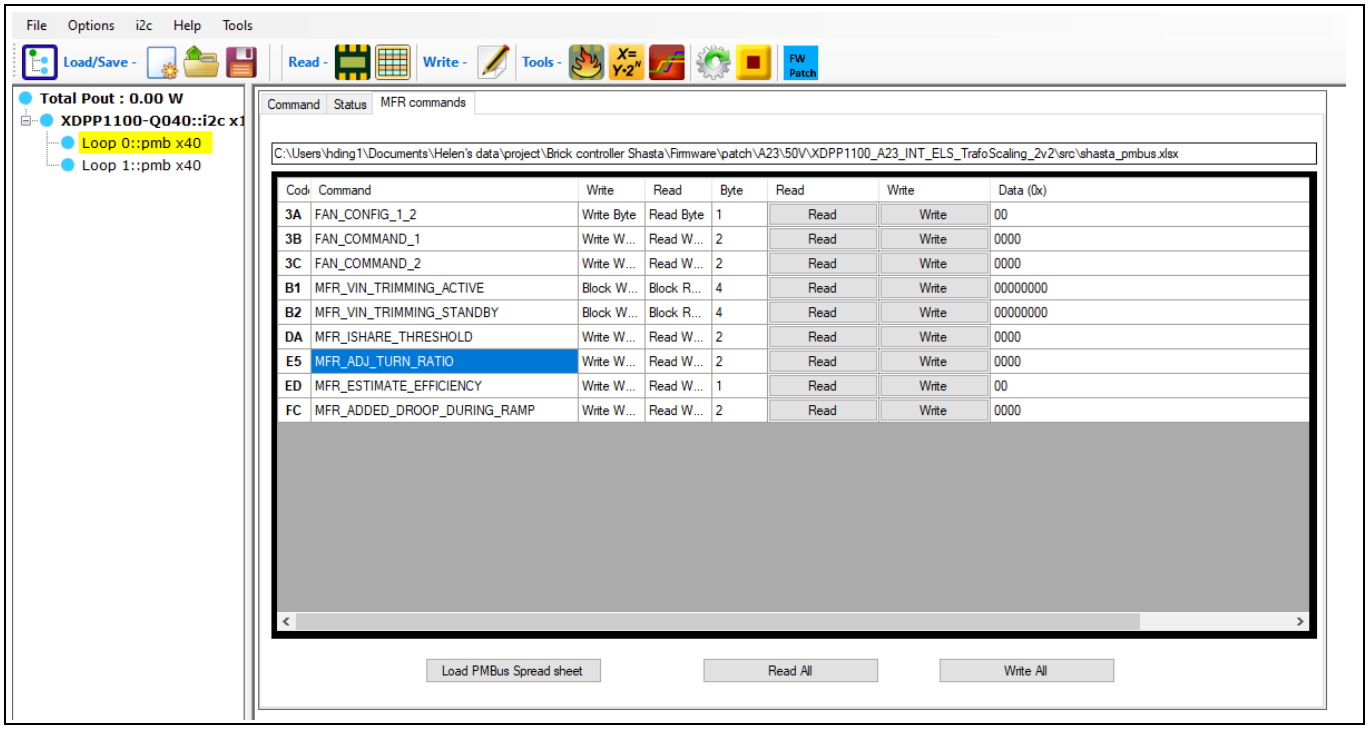


Figure 37 MFR PMBus commands

3.4 Active clamp switches PWM configuration

In this design, PWM5 and PWM6 control the active clamp switches. Each switch is assumed to be an N-channel MOSFET that provides a path between the midpoint of the secondary SR bridge and a snubber capacitor, as explained in more detail in section 2.2.2. As the active clamp circuit is not part of the standard topology, PWMs must be manually configured in the register map. This section explains how to configure these registers.

section 3.4.1 illustrates how to configure a control strategy for the active clamp switches so that they are driven in phase with the respective primary PWMs (with necessary dead time to correct the delays for the isolator and gate drivers). The XDPP1100 could also provide a narrower pulse if a different control strategy (section 2.2.1) is required. Sections 3.4.2 and 3.4.3 give instructions for creating a PWM with a user-defined pulse width.

3.4.1 Option 1 – use ramp0 (present solution)

The desired PWM output is shown in Figure 38. The register configuration is shown in Table 9.

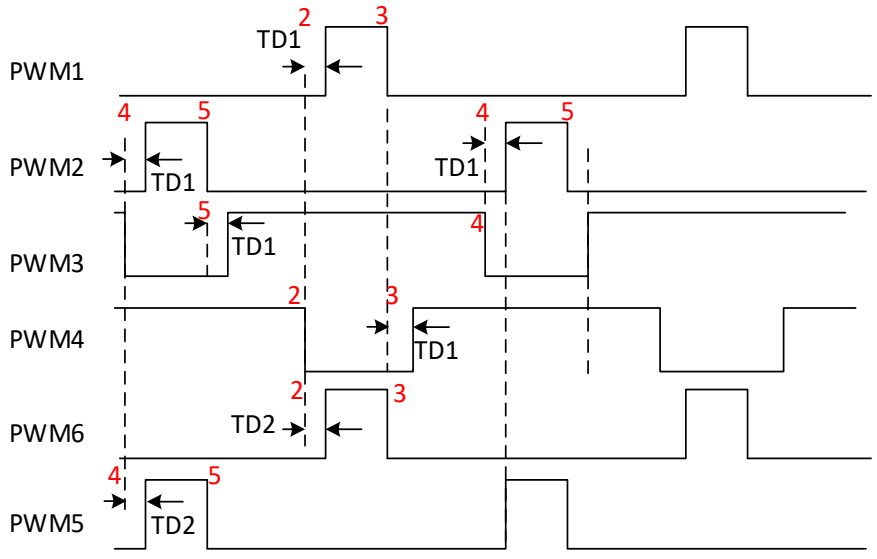


Figure 38 PWM waveforms for option 1 – clamp on for the entire duration of the powering phase

Table 9 PWM5, PWM6 configuration using ramp0

Register	Config. value	Comments
pwm5_fall_sel	5	PWM5 is low at t2 odd
pwm5_rise_sel	4	PWM5 is high at t1 odd (align with the rising edge of PWM2)
pwm6_fall_sel	3	PWM6 is low at t2 even
pwm6_rise_sel	2	PWM6 is high at t1 even (align with the rising edge of PWM1)
pwm5_loop_map	1	PWM5 is in loop0, phase1
pwm6_loop_map	1	PWM6 is in loop0, phase1
pwm5_ppen	1	Set CMOS output
pwm5_ppen	1	Set CMOS output
ramp0_min_pw_state	1	

The PMBus command FW_CONFIG_PWM should be updated to activate PWM5 and PWM6 as shown in Figure 39. This configures PWM1 and PWM2 as control PWMs, and PWM3 and PWM4 as SR output; PWM5 and PWM6 are added as control switches.

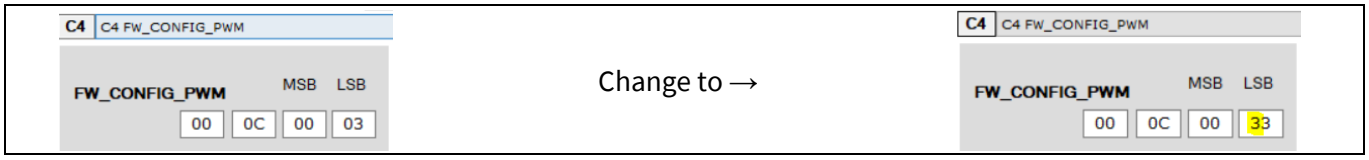


Figure 39 FW_CONFIG_PWM

Table 10 FW_CONFIG_PWM

Command	New value	Comments
FW_CONFIG_PWM	00 0C 00 33	The 00 33 means primary (control) FETs are driven by PWM1, PWM2, PWM5, PWM6 The 00 1C means SR FETs are driven by PWM3, PWM4

The dead time is configured by PMBus command PWM_DEADTIME, as shown below. Each active PWM could configure the delay of falling edge (fall time) and rising edge (rise time) independently. The dead time resolution is 1.25 ns, ranging up to 318.75 ns.

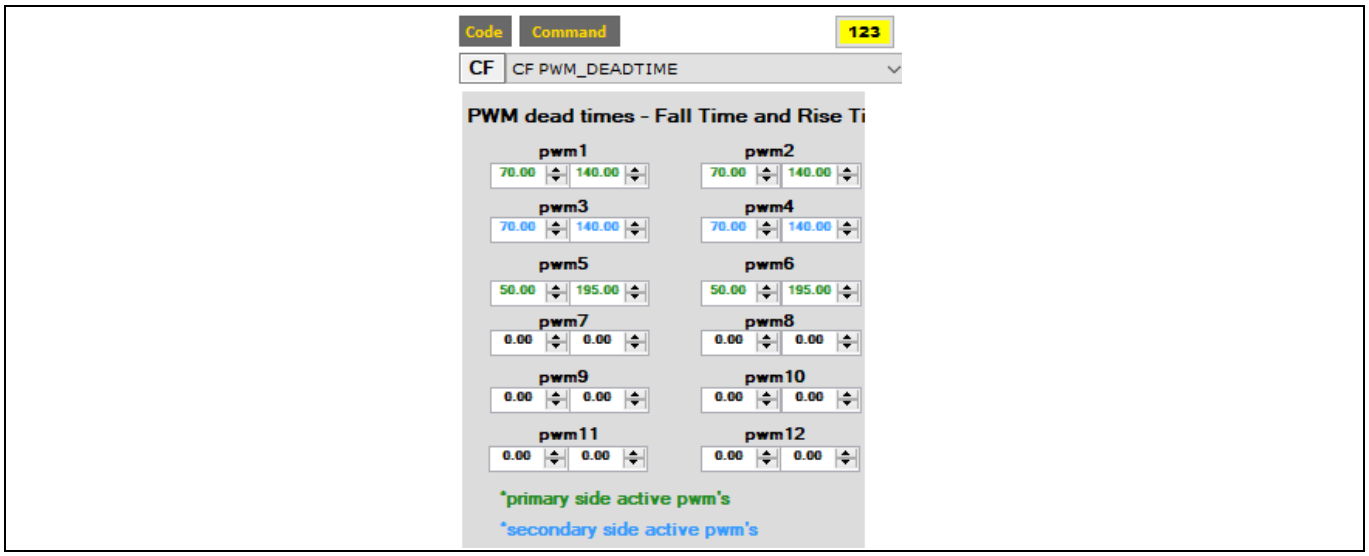


Figure 40 Dead time configuration

3.4.2 Option 2 – use ramp0

This section shows a possible configuration for control strategies that see the active clamp switches turned off before the end of the powering phase (for example, minimum clamp switch on-time as per equation (35)).

If the maximum pulse width (clamp switch on-time) is less than 318.75 ns, it is possible to use the PWM edge selection t1 and t1_delay and play with the dead time (delay) to get the desired pulse width. Please note that the **ramp0_min_pw_state** should be set to 1 to force the minimum pulse output for this application. Use the MFR_MIN_PW command to configure the minimum pulse width of the primary switch.

Table 11 PWM5, PWM6 config using ramp0

Register	Config. value	Comments
pwm5_fall_sel	6	PWM5 is low at t1 delay (5 ns after t1)
pwm5_rise_sel	4	PWM5 is high at t1 odd
pwm6_fall_sel	6	PWM6 is low at t1 delay (5 ns after t1)
pwm6_rise_sel	2	PWM6 is high at t1 even
pwm5_loop_map	1	PWM5 is in loop0, phase1
pwm6_loop_map	1	PWM6 is in loop0, phase1
pwm5_ppen	1	Set CMOS output
pwm5_ppen	1	Set CMOS output
ramp0_min_pw_state	1	

PMBus command FW_CONFIG_PWM should also be updated to activate PWM5 and PWM6 as shown in Figure 39.

The expected PWM waveform is shown below.

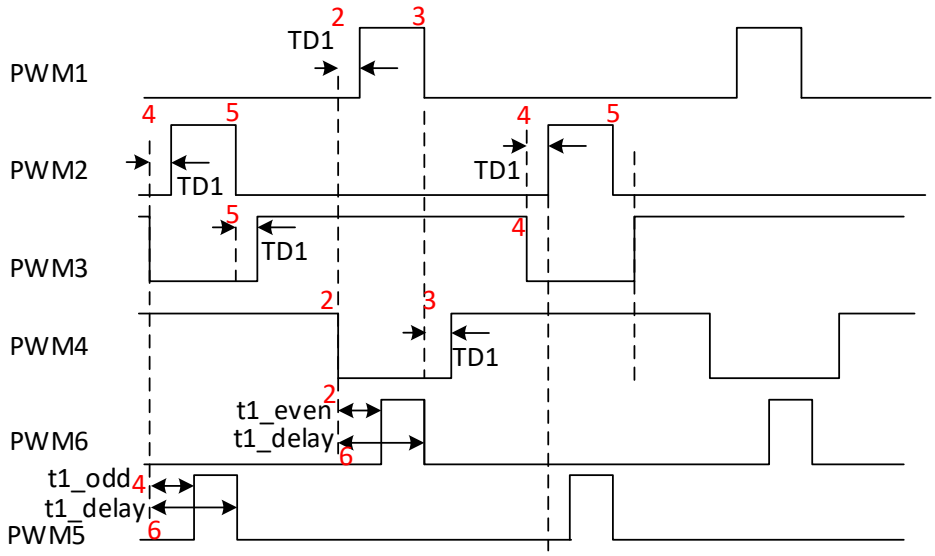


Figure 41 PWM waveform for option 2

In this case, no FW patch is required.

3.4.3 Option 3 – use ramp1

This section shows another configuration for control strategies that sees the active clamp switches turned off before the end of the powering phase. This configuration is suitable if the clamp-switch on-time needs to be longer than 318.75 ns.

Then the configuration suggested in section 3.4.2 is no longer applicable, since the delay required is outside the maximum dead time configuration range. Then we can use the second ramp (ramp1) to control PWM5, PWM6, and use the ramp1_force_t1 and ramp1_force_t2 to determine the rising edge and falling edge. It can be configured as in Table 12.

Note: Since the ramp1_force_t1 and ramp1_force_t2 are not stored in the OTP, FW control is required to apply these parameters. This is not implemented in the present project.

The highlighted register ramp1_force_t1 and ramp1_force_t2 could be modified for the desired delay. The benefit of this solution is that the pulse width of the active snubber can be set longer than 318.75 ns.

Table 12 PWM5, PWM6 configuration using ramp1

Register	Config. value	Comments
pwm5_fall_sel	5	PWM5 is low at t2 odd
pwm5_rise_sel	4	PWM5 is high at t1 odd
pwm6_fall_sel	3	PWM6 is low at t2 even
pwm6_rise_sel	2	PWM6 is high at t1 even
pwm5_loop_map	3	PWM5 is in loop0, phase2
pwm6_loop_map	3	PWM6 is in loop0, phase2
pwm5_ppen	1	Set CMOS output
pwm5_ppen	1	Set CMOS output
ramp1_sync_sel	1	Fsw1 = Fsw0
ramp1_m_flavor	2	Trailing-edge modulation
ramp1_half_mode	1	Half-mode enables bridge topology
ramp1_min_pw_state	1	Minimum pulse width is clamped to ramp1_pw_min
ramp1_dutyc_lock	1	Duty lock enabled
ramp1_phase	0	ramp0_phase = 0 and ramp1 phase is the same as ramp0
ramp1_force_t1	41	LSB 5 ns, set t1 at 205 ns
ramp1_force_t1_en	1	Ramp1 t1 force enable
ramp1_force_t2	71	LSB 5 ns, set t2 at 355 ns
ramp1_force_t2_en	1	Ramp1 t2 force enable

In addition to the register, PMBus command FW_CONFIG_PWM should also be updated to activate PWM5 and PWM6 as shown in Figure 42. This configures PWM1 and PWM2 as control PWM, PWM3 and PWM4 as SR output, and PWM5 and PWM6 are added as control switches.

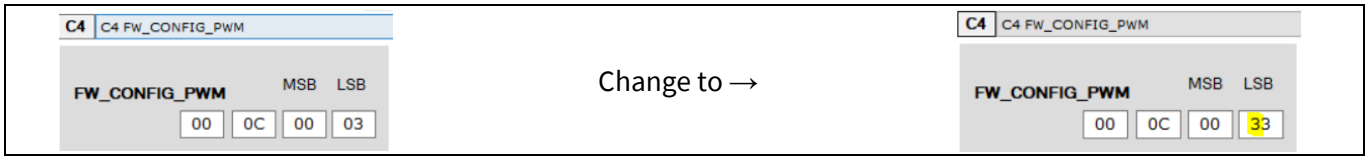


Figure 42 FW_CONFIG_PWM

The time diagram is shown below.

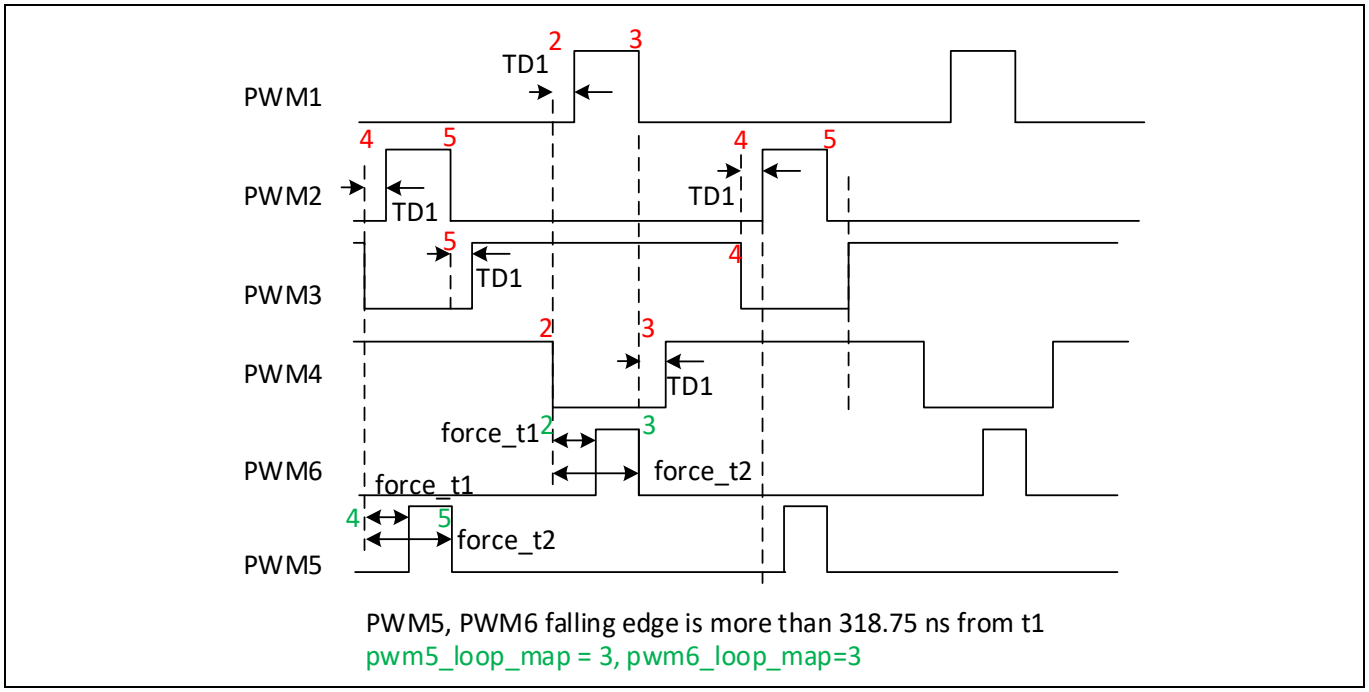


Figure 43 PWM waveforms for option 3

4 Experimental verification

4.1 Test setup

Pictures of the test setup are shown in Figure 44 and Figure 45.

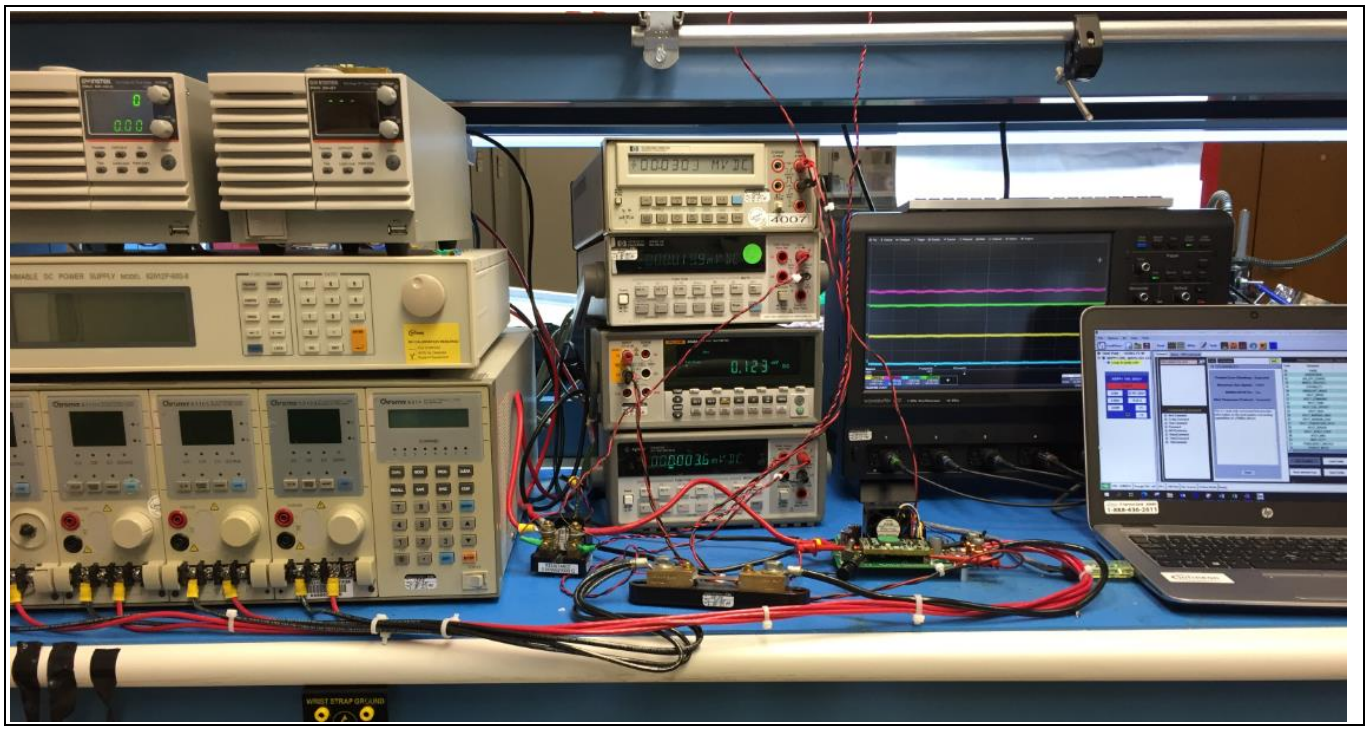


Figure 44 Test bench setup

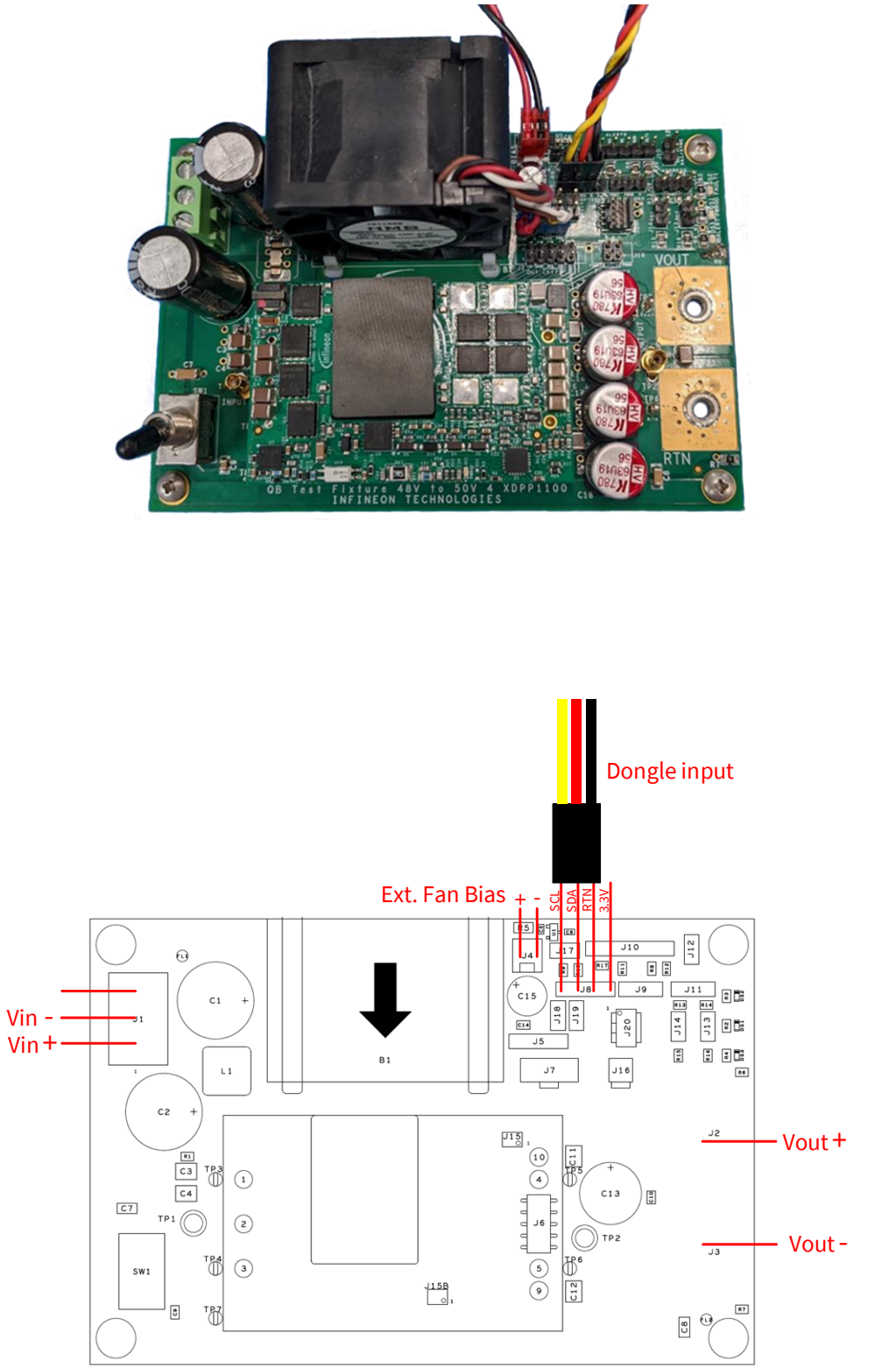


Figure 45 Overview of the brick power module, mounted on the text fixture, and main connections

Necessary connections to operate the board:

- Connect the quarter-brick to the test fixture. Make sure the input, output, and signal connector J6 on the test fixture have good contact.

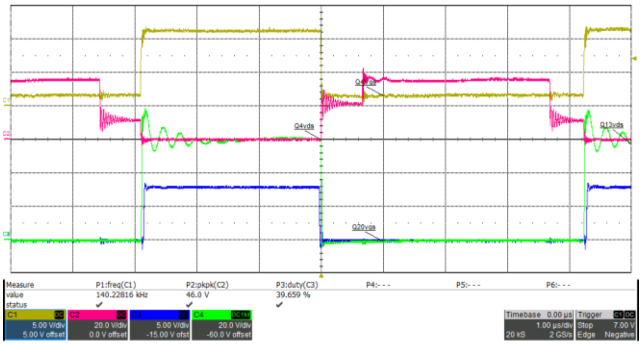
Experimental verification

- Connect the 48 V input power supply to J1.
- Connect the load to J2 and J3.
- Bias fan with 5~12 V DC power supply at J4 (EXT BIAS 7.5 V is recommended). Bias is necessary to enable communication with the XDPP1100 to the USB dongle.
- Connect the XDPP1100 USB dongle (USB007 Rev A) to J8. Find the direction by identifying the ground pin G (black wire). The blue wire of USB007 Rev A is not used and can be left floating.
- Make sure that the switch SW1 is in the off position.
- Turn on the 48 V input power supply. A minimum of 35 V is required to enable the auxiliary power supply.
- This demo board comes with a default patch and configuration stored in OTP and can be turned on once the operation command is asserted from the XDPP1100 GUI.
- To assert the operation command, open the XDPP1100 GUI and click on “Auto populate”. The auto-populate option is in the top-left corner just below the “File” option.
- Write “ON” to PMBus command “0x01 OPERATION” and turn the enable switch SW1 to the on position (sequence is not critical).

4.2 Operation waveforms

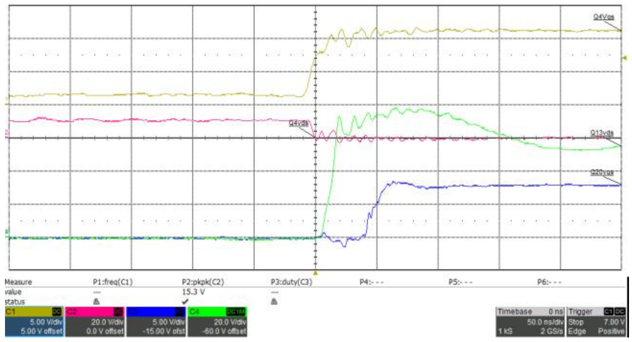
4.2.1 Steady-state operation

4.2.1.1 Switching waveforms for V_{out} = 50 V, I_{out} = 15 A



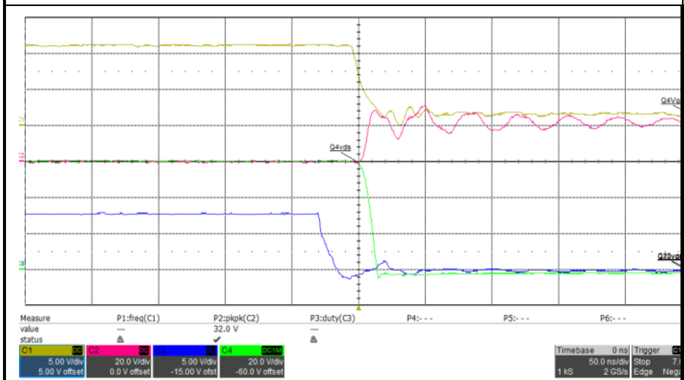
V_{in} = -36 V, horizontal scale: 1 µs/div

Ch1 (5 V/div) = Primary V_{GS} (Q4) Ch2 (20 V/div) = Primary V_{DS} (Q4)
Ch3 (5 V/div) = Active clamp V_{GS} (Q20) Ch4 (20 V/div) = Secondary V_{DS} (Q13)



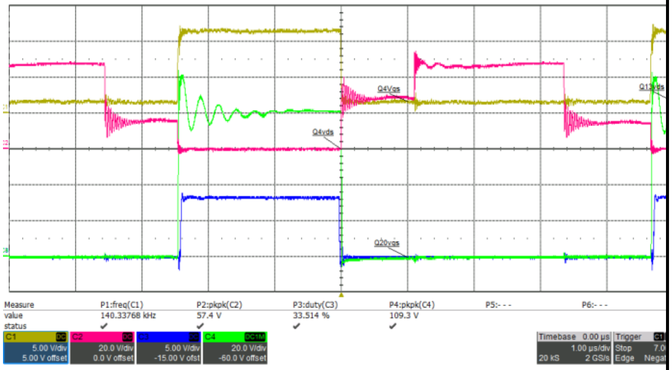
V_{in} = -36 V, horizontal scale: 50 ns/div

Ch1 (5 V/div) = Primary V_{GS} (Q4) Ch2 (20 V/div) = Primary V_{DS} (Q4)
Ch3 (5 V/div) = Active clamp V_{GS} (Q20) Ch4 (20 V/div) = Secondary V_{DS} (Q13)



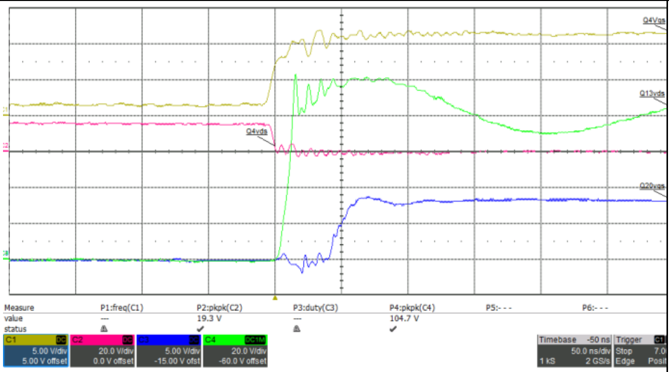
V_{in} = -36 V, horizontal scale: 1 µs/div

Ch1 (5 V/div) = Primary V_{GS} (Q4) Ch2 (20 V/div) = Primary V_{DS} (Q4)
Ch3 (5 V/div) = Active clamp V_{GS} (Q20) Ch4 (20 V/div) = Secondary V_{DS} (Q13)



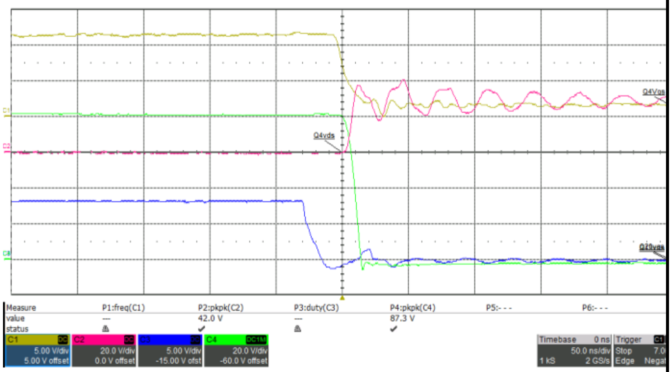
V_{in} = -48 V, horizontal scale: 50 ns/div

Ch1 (5 V/div) = Primary V_{GS} (Q4) Ch2 (20 V/div) = Primary V_{DS} (Q4)
Ch3 (5 V/div) = Active clamp V_{GS} (Q20) Ch4 (20 V/div) = Secondary V_{DS} (Q13)



V_{in} = -48 V, horizontal scale: 50 ns/div

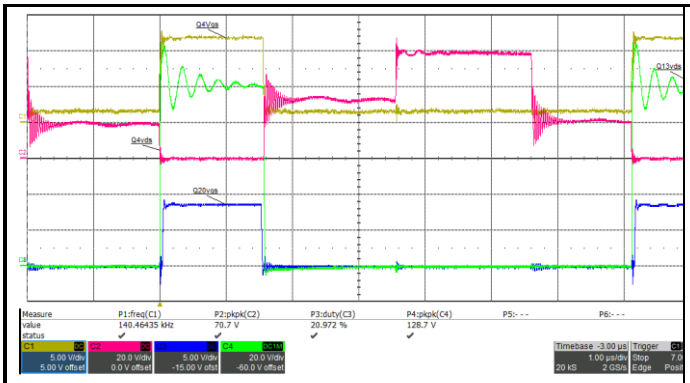
Ch1 (5 V/div) = Primary V_{GS} (Q4) Ch2 (20 V/div) = Primary V_{DS} (Q4)
Ch3 (5 V/div) = Active clamp V_{GS} (Q20) Ch4 (20 V/div) = Secondary V_{DS} (Q13)



V_{in} = -48 V, horizontal scale: 50 ns/div

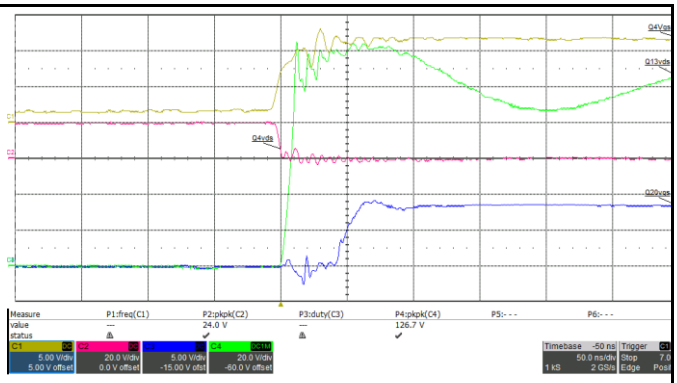
Ch1 (5 V/div) = Primary V_{GS} (Q4) Ch2 (20 V/div) = Primary V_{DS} (Q4)
Ch3 (5 V/div) = Active clamp V_{GS} (Q20) Ch4 (20 V/div) = Secondary V_{DS} (Q13)

(figure continues...)



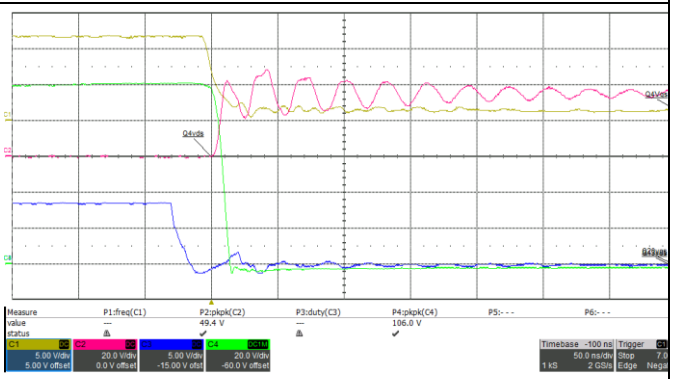
V_{in} = -60 V, horizontal scale: 1 µs/div

Ch1 (5 V/div) = Primary V_{GS} (Q4)
Ch2 (20 V/div) = Primary V_{DS} (Q4)
Ch3 (5 V/div) = Active clamp V_{GS} (Q20)
Ch4 (20 V/div) = Secondary V_{DS} (Q13)



V_{in} = -60 V, horizontal scale: 50 ns/div

Ch1 (5 V/div) = Primary V_{GS} (Q4)
Ch2 (20 V/div) = Primary V_{DS} (Q4)
Ch3 (5 V/div) = Active clamp V_{GS} (Q20)
Ch4 (20 V/div) = Secondary V_{DS} (Q13)

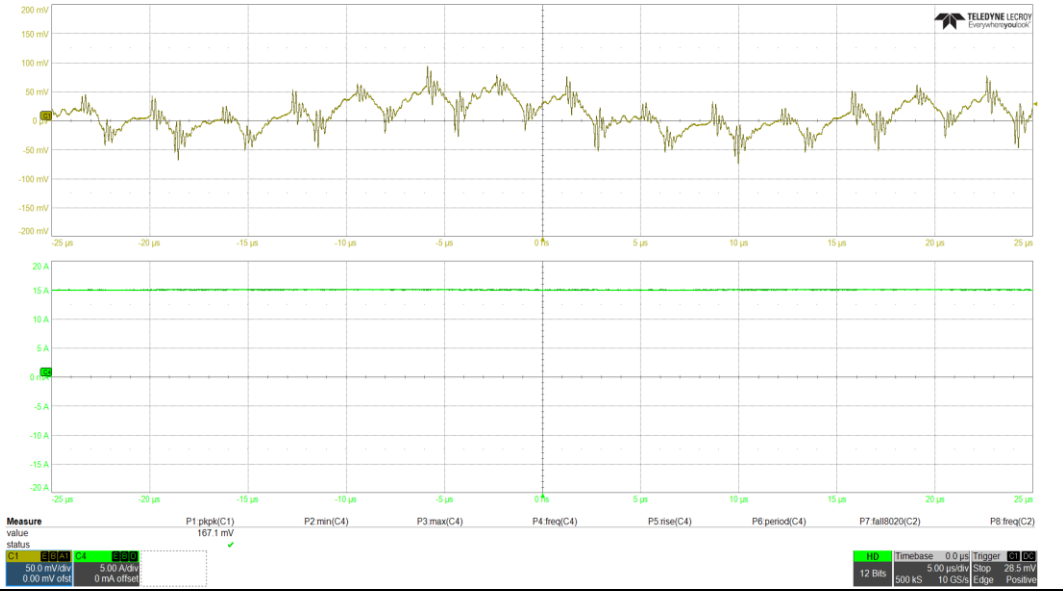


V_{in} = -60 V, horizontal scale: 50 ns/div

Ch1 (5 V/div) = Primary V_{GS} (Q4)
Ch2 (20 V/div) = Primary V_{DS} (Q4)
Ch3 (5 V/div) = Active clamp V_{GS} (Q20)
Ch4 (20 V/div) = Secondary V_{DS} (Q13)

Figure 46 Switching waveforms for V_{out} = 50 V, I_{out} = 15 A

4.2.2 Output ripple and noise



Ch.1 (50 mV/div) = Output voltage V_{out} (AC coupled)

Ch.4 (5 A/div) = Output current I_{out}

Figure 47 Output ripple and noise for V_{out} = 50 V, V_{in} = -48 V, I_{out} = 15 A

4.2.3 Start-up waveforms

4.2.3.1 Start-up waveforms for V_{out} = 50 V

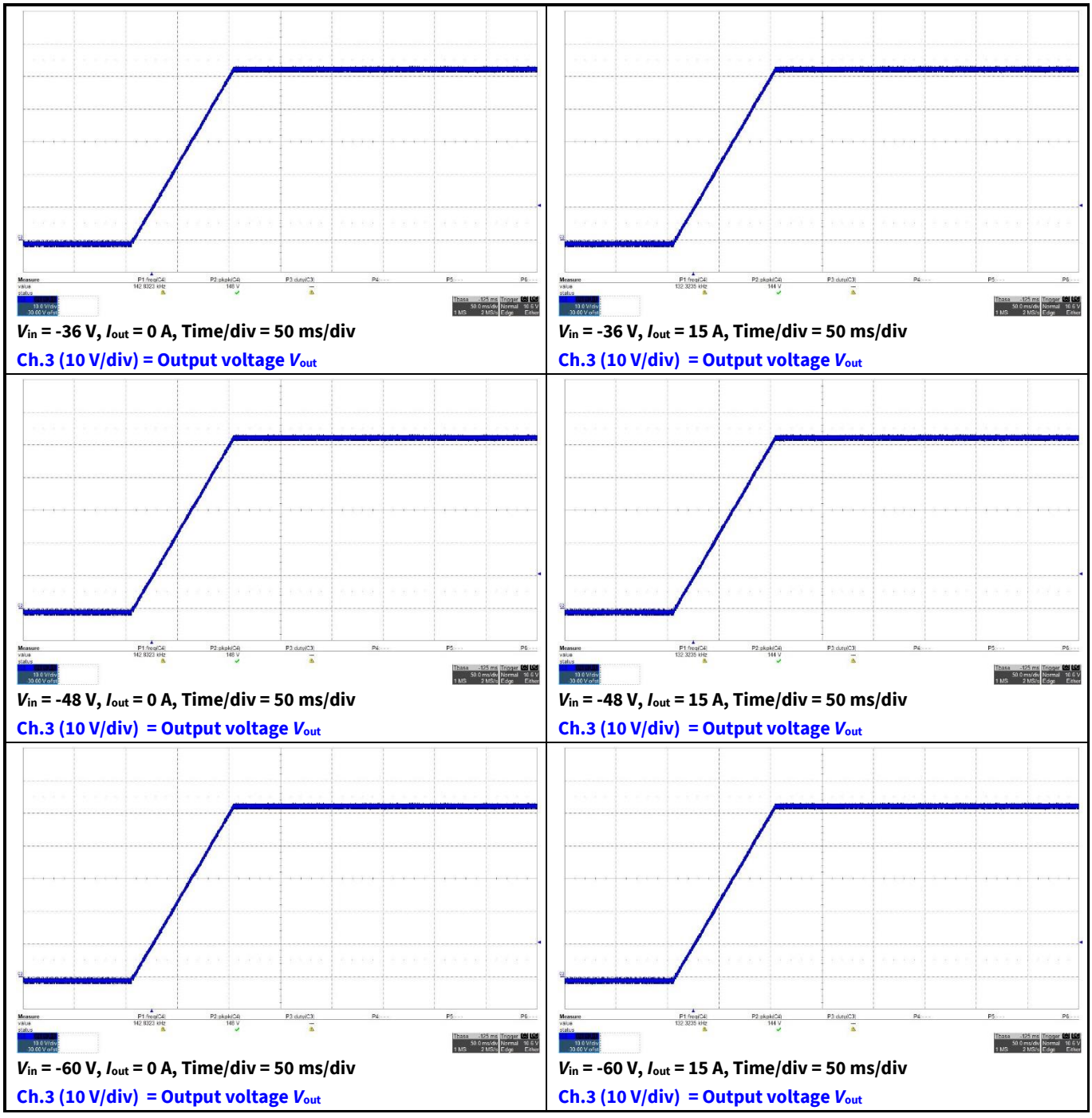
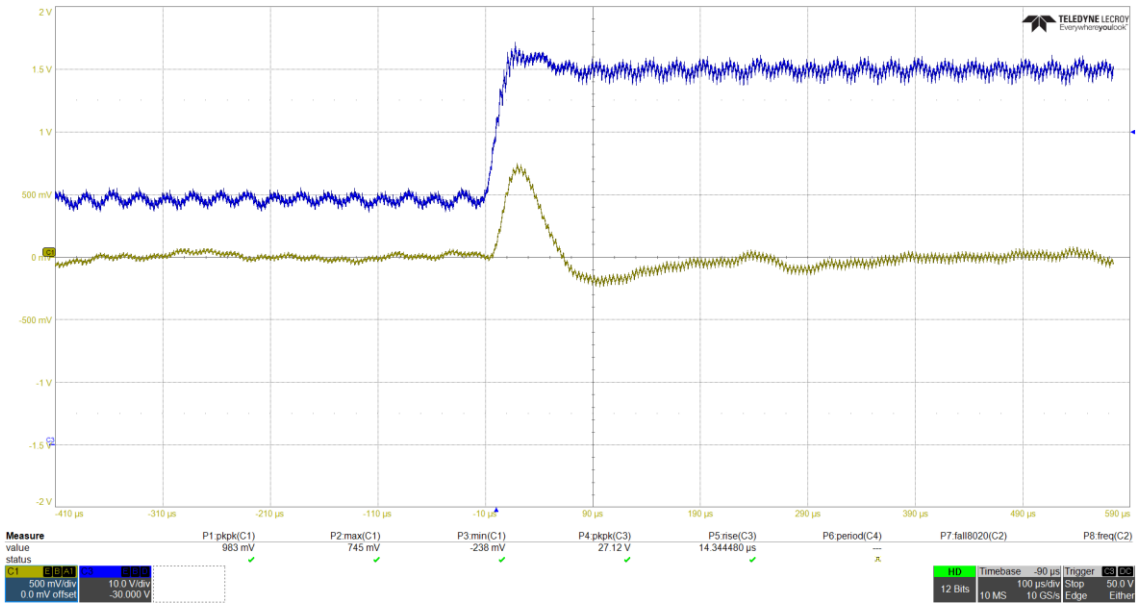


Figure 48 Start-up waveforms at V_{out} = 50 V

4.2.4 Line and load transients

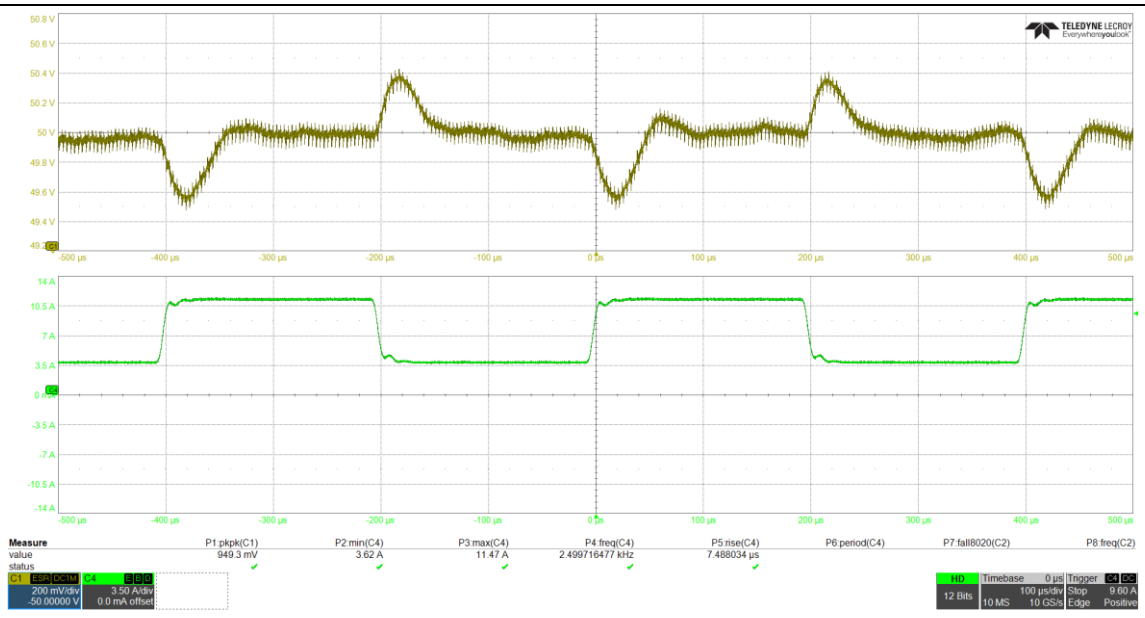
4.2.4.1 Line transients



V_{in} = -40 V to -60 V, dV_{in}/dt = 2.0 V/µs, I_{out} = 15 A
Ch.3 (10 V/div) = Input voltage V_{in}
Ch.1 (500 mV/div) = Output voltage V_{out} (AC coupled)

Figure 49 Line transient waveforms

4.2.4.2 Load transients for V_{out} = 50 V



V_{in} = -48 V, I_{out} = 3.75 / 11.25 / 3.75 A, di/dt = 2.0 A/µs
Ch.1 (500 mV/div) = Output voltage V_{out}
Ch 4 (3.5 A/div) = Output current I_{out}

Figure 50 Load transient waveforms for V_{out} = 50 V

4.3 Efficiency

Efficiencies have been captured at v_{air} = 3 m/s.

Table 13 Measured efficiency at V_{out} = 50 V

Output current	V_{in} = -36 V	V_{in} = -48 V	V_{in} = -60 V
1A	86.09%	81.14%	76.22%
3A	93.67%	91.56%	89.53%
7A	96.14%	94.51%	93.22%
11A	96.36%	95.44%	94.40%
15A	95.92%	95.33%	94.59%

Table 14 Measured efficiency at V_{out} = 55 V

Output current	V_{in} = -36 V	V_{in} = -48 V	V_{in} = -60 V
1A	85.71%	81.89%	76.53%
3A	94.07%	91.86%	89.79%
7A	96.40%	94.85%	93.49%
11A	96.45%	95.67%	94.68%
15A	96.11%	95.58%	94.84%

Table 15 Measured efficiency at V_{out} = 28 V

Output current	V_{in} = -36 V	V_{in} = -48 V	V_{in} = -60 V
1A	82.13%	77.57%	73.49%
3A	91.11%	88.85%	86.83%
7A	94.29%	92.84%	91.46%
11A	94.83%	93.90%	92.93%
15A	94.42%	93.80%	93.16%

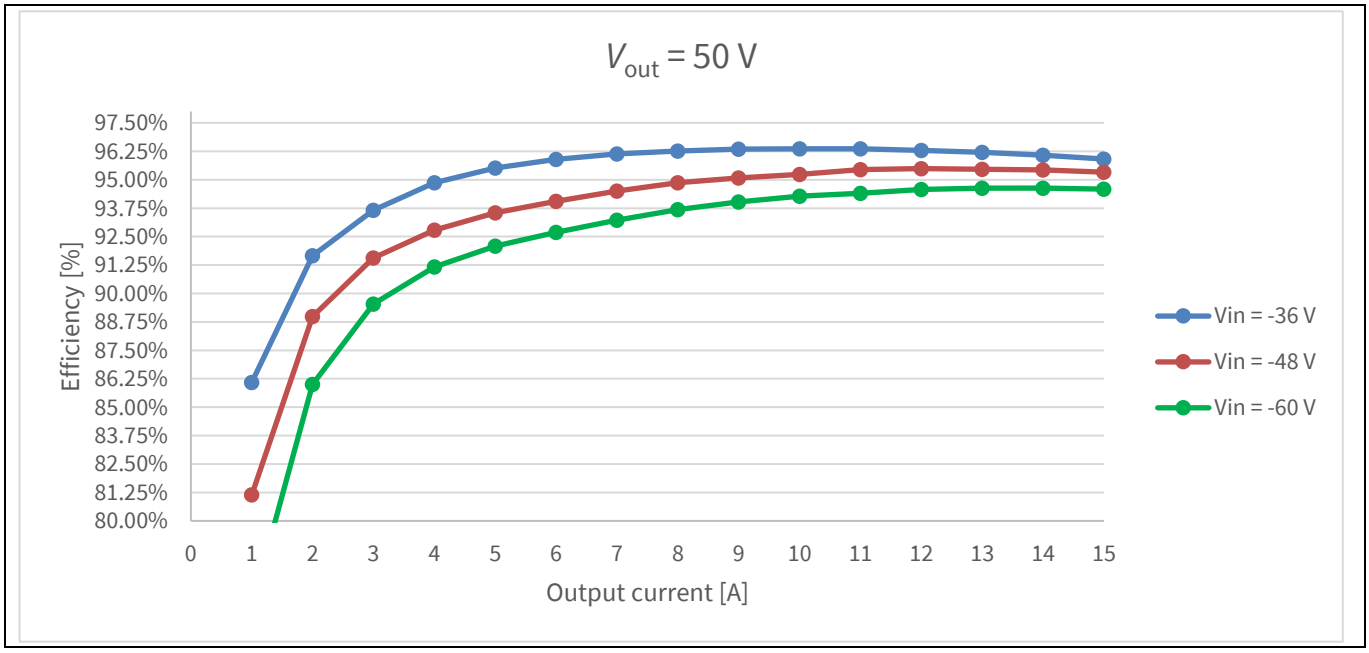


Figure 51 Efficiency curves over line and load range at V_{out} = 50 V

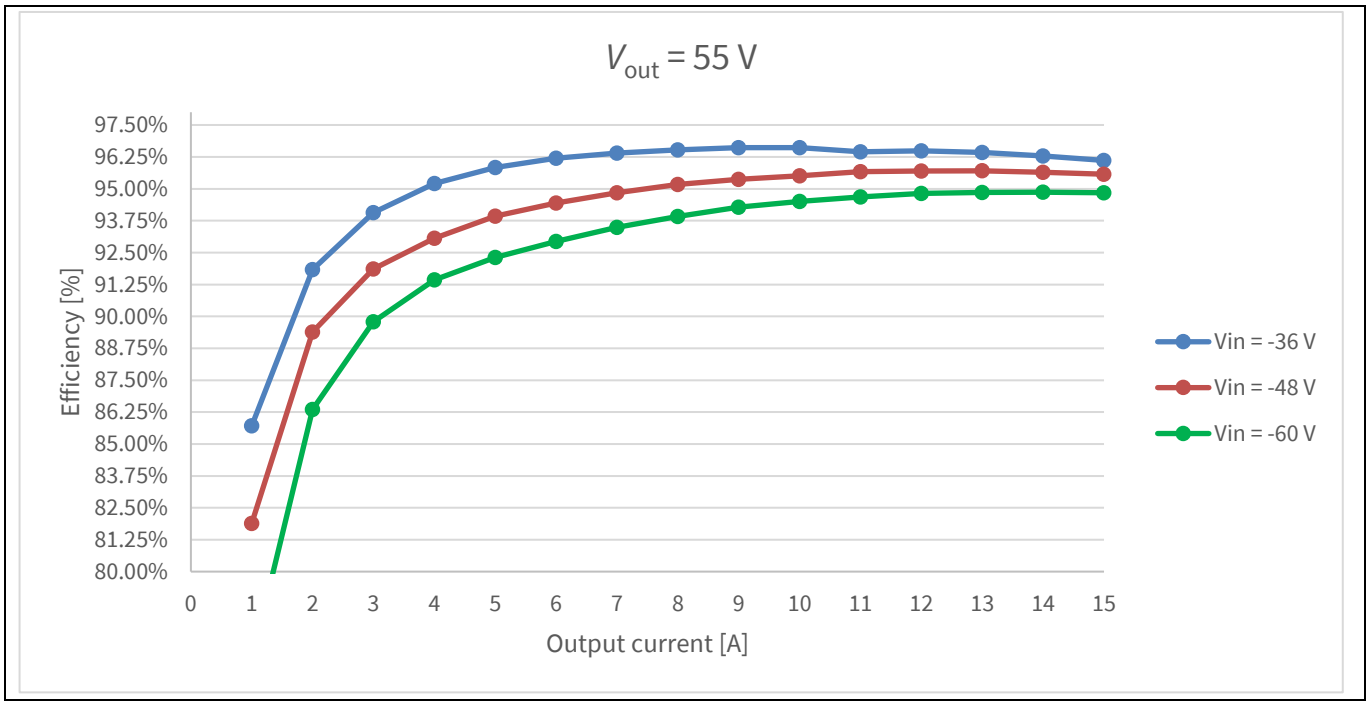


Figure 52 Efficiency curves over line and load range at V_{out} = 55 V

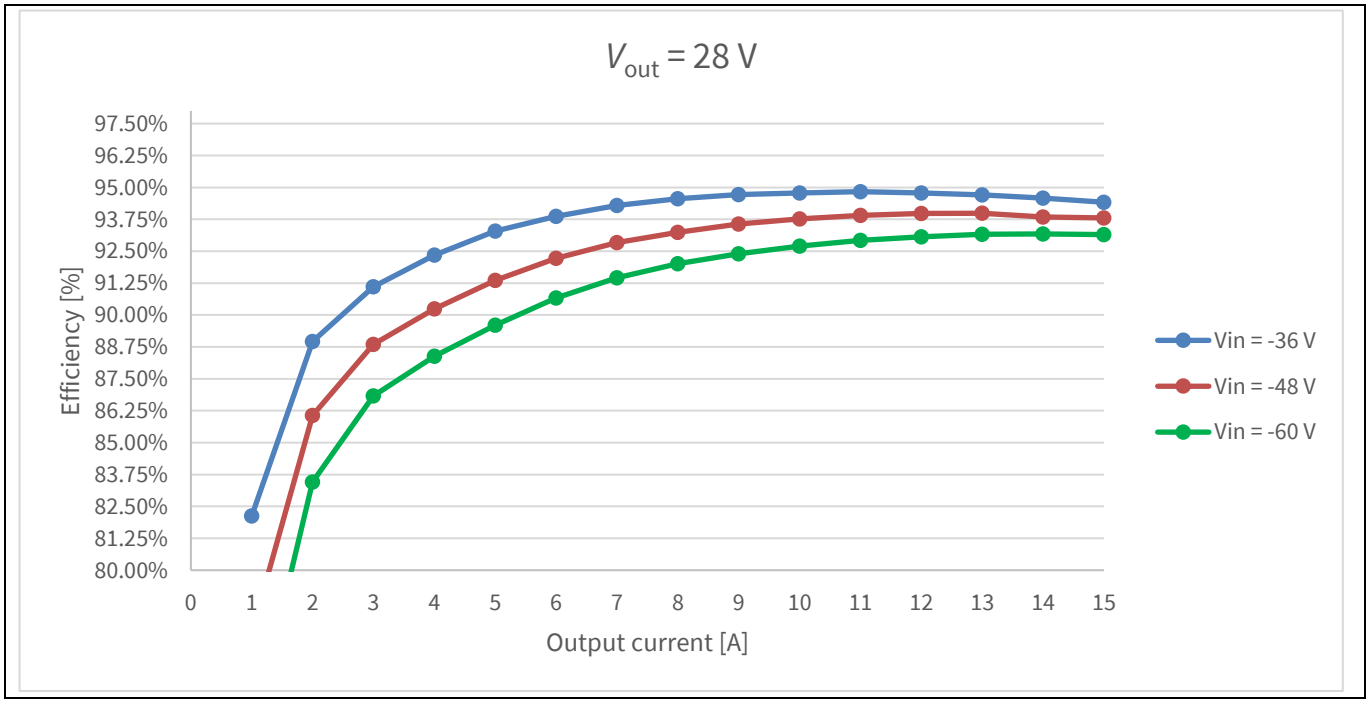


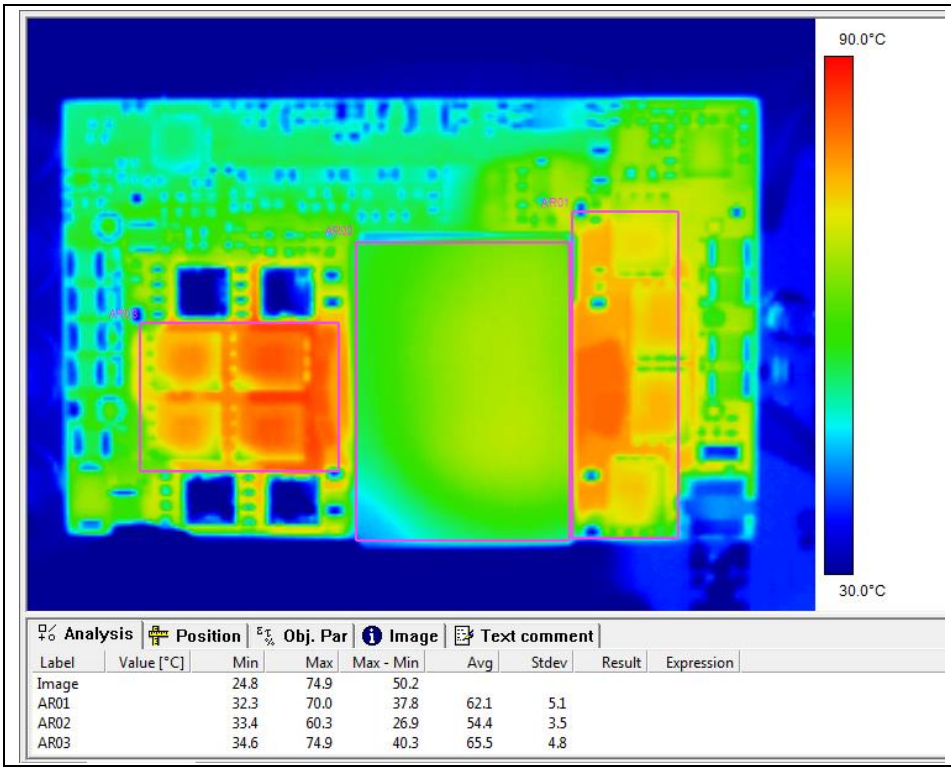
Figure 53 Efficiency curves over line and load range at V_{out} = 28 V

4.4 Thermal images

FLIR ThermoVision A20 was used to record the thermal images. Thermal images for V_{in} = -36 V, -48 V and – 60 V, while regulating V_{out} = 50 V are given in Figure 54 to Figure 56.

Experimental verification

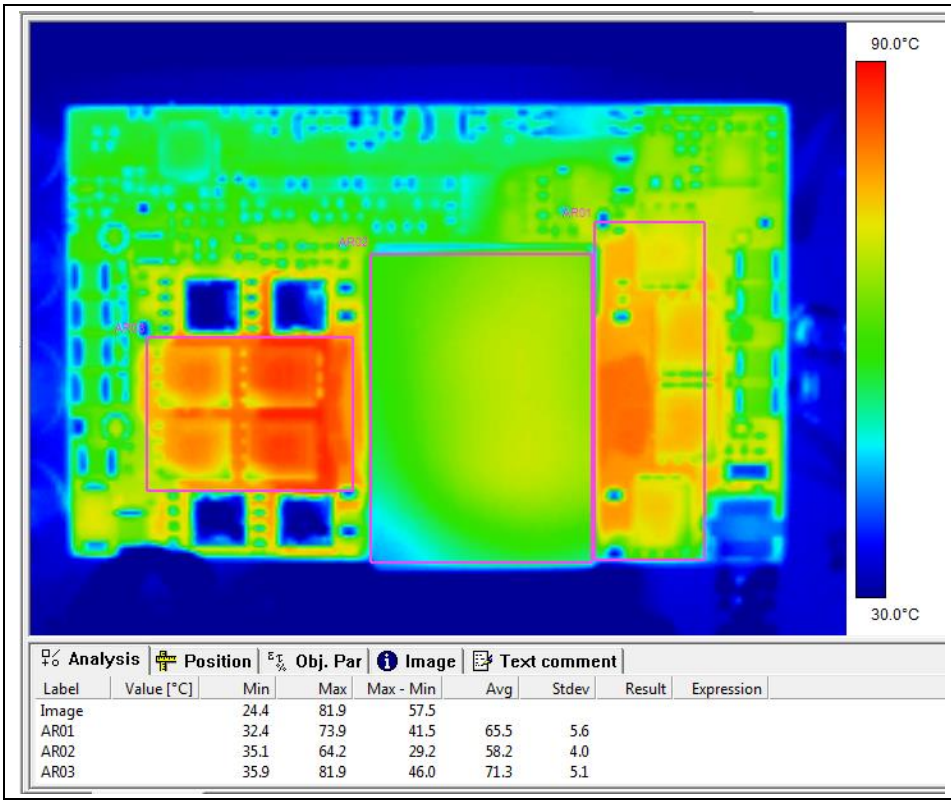
The thermal images were taken with a fan voltage of 7.5 V (airflow ~= 600 LFM).



AR01: Primary MOSFETs and transformer termination
AR02: Transformer core
AR03: SR MOSFETs

Hotspot: 74.9°C at Secondary-side transformer termination

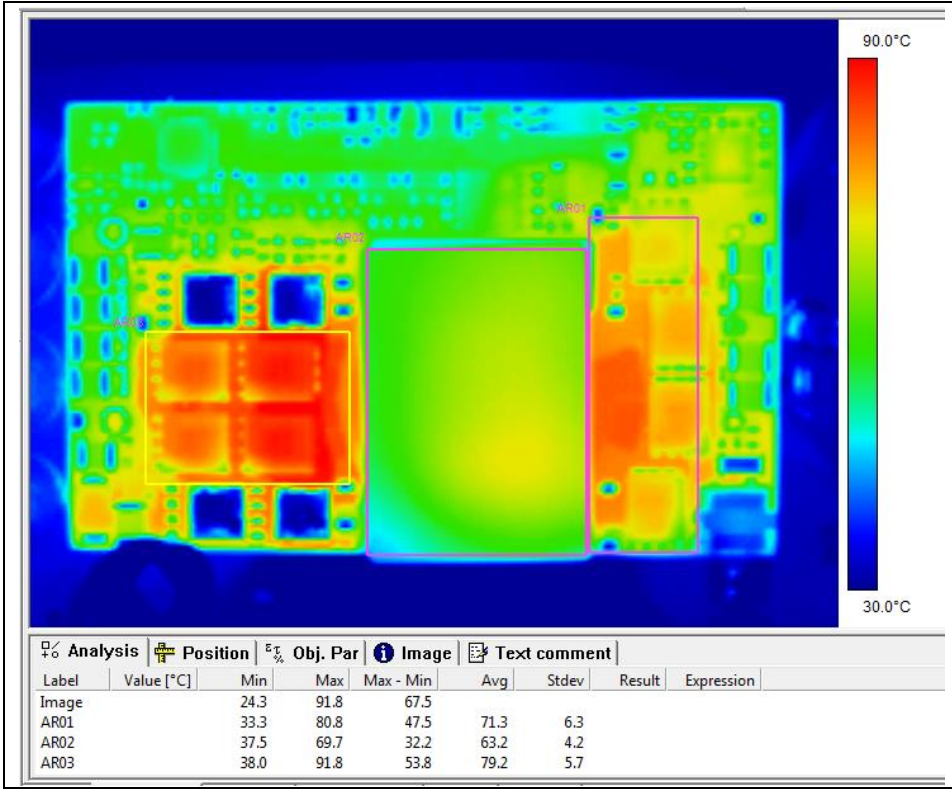
Figure 54 Thermal image for V_{in} = -36 V



AR01: Primary MOSFETs and transformer termination
AR02: Transformer core
AR03: SR MOSFETs

Hotspot: 81.9°C at secondary-side transformer termination

Figure 55 Thermal image for V_{in} = -48 V



Label	Value [°C]	Min	Max	Max - Min	Avg	Stdev	Result	Expression
Image		24.3	91.8	67.5				
AR01		33.3	80.8	47.5	71.3	6.3		
AR02		37.5	69.7	32.2	63.2	4.2		
AR03		38.0	91.8	53.8	79.2	5.7		

AR01: Primary MOSFETs and transformer termination
AR02: Transformer core
AR03: SR MOSFETs

Hotspot: 91.8°C at secondary-side transformer termination

Figure 56 Thermal image for V_{in} = -60 V

5 Appendix

5.1 (R)LC series circuit solution

Below are the step-by-step solutions for the voltage overshoot problems formulated in chapter 2.

5.1.1 Non-damped case

$$L_{Lk}\frac{d}{dt}\left[I_L + 2C_{oss}\frac{du_{ds}}{dt}\right] + u_{ds} = U_s \Leftrightarrow 2L_{Lk}C_{oss}\frac{d^2u_{ds}}{dt^2} + u_{ds} = U_s \tag{36}$$

The homogeneous equation:

$$2L_{Lk}C_{oss}\frac{d^2u_{ds}}{dt^2} + u_{ds} = 0 \tag{37}$$

Has solutions in the form:

$$u_{ds,hom}(t) = A\sin(\omega_0 t + \Phi) \tag{38}$$

Solution must be found in the form of a constant:

$$u_{ds,part}(t) = U \tag{39}$$

Resulting in:

$$u_{ds,part}(t) = U = U_s \tag{40}$$

The general solution is:

$$u_{ds}(t) = u_{ds,hom}(t) + u_{ds,part}(t) = A\sin(\omega_0 t + \Phi) + U_s \tag{41}$$

The two arbitrary integration constants *A* and *Φ* are found by imposing the initial conditions:

$$\begin{cases} u_{ds}(t_2) = 0 \\ \dfrac{du_{ds}}{dt}(t_2) = \dfrac{i_{oss}(t_2)}{C_{oss}} = 0 \end{cases} \tag{42}$$

The solution of the problem is then written:

$$u_{ds}(t) = U_s\{1 - \cos[\omega_0(t - t_2)]\} \tag{43}$$

The peak overshoot can be quantified in:

$$U_{ds,pk} = \max_{t \geq t_2} u_{ds}(t) = 2U_s \tag{44}$$

Independently of the values of L_{Lk} and C_{oss} as well as on the load current I_L.

5.1.2 Damped case

$$2L_{Lk}C_{oss}\frac{du_{ds}}{dt} + 2R_sC_{oss}\frac{du_{ds}}{dt} + u_{ds} = U_s - R_sI_L \tag{45}$$

The homogeneous equation:

$$\frac{d^2u_{ds}}{dt^2} + \frac{R_s}{L_{Lk}}\frac{du_{ds}}{dt} + \frac{1}{2L_{Lk}C_{oss}}u_{ds} = 0 \tag{46}$$

Has solutions in the form:

$$u_{ds,hom}(t) = Ae^{-\alpha t}\sin(\omega t + \Phi) \tag{47}$$

With ω being the damped oscillation frequency, related to the natural oscillation frequency by the relation:

$$\omega = \omega_0\sqrt{1-\zeta^2} \tag{48}$$

Where $\zeta \triangleq R_s/(2L_{Lk}\omega_0)$ is the damping ratio.

Solution must be found in the form of a constant:

$$u_{ds,part}(t) = U \tag{49}$$

Resulting in:

$$u_{ds,part}(t) = U = U_s - R_sI_L \tag{50}$$

The general solution is:

$$u_{ds}(t) = Ae^{-\alpha t}\sin(\omega t + \Phi) + (U_s - R_sI_L) \tag{51}$$

The two arbitrary integration constants *A* and *Φ* are found by imposing the initial conditions.

The solution of the problem is then written:

$$u_{ds}(t) = (U_s - R_sI_L)\left\{1 - e^{-\frac{R_s}{2L_{Lk}}t}\cos\left[\omega(t-t_2)\right]\right\} \tag{52}$$

The relative overshoot on top of the rectified voltage can be quantified from the undamped response in:

$$U_{ds,OV}[\%] = \exp\left(\frac{-\zeta\pi}{\sqrt{1-\zeta^2}}\right)\times 100\% \tag{53}$$

As the damping factor ζ reduces, the relative overshoot increases. For the limit of $\zeta \to 0$ the circuit reduces to the non-damped LC, and the peak overshoot is again two times the rectified voltage.

Since the damping factor ζ is inversely dependent on L_{Lk}, a large value for the leakage inductance leads to very high voltage overshoot, potentially reaching two times the rectified voltage.

5.2 Bill of materials

Qty.	Designator	Value	Rating	Footprint	Part number
8	C1,C2,C3,C4,C5,C6,C7,C8	2.2 uF	100 V X7R	C1210	C3225X7R2A225K230AM
21	C9,C10,C11,C12,C15,C17,C19,C24,C29,C30,C34,C35,C42,C43,C44,C45,C53,C54,C55,C69,C74	0.1 uF	50 V X7R	C0603	C1608X7R1H104K080AA
3	C13,C18,C20	100 pF	100 V C0G	C0603	C1608C0G2A101K080AA
1	C14	0.01 uF	50 V X7R	C0603	C1608X7R1H103K080AA
2	C16,C48	0.047 uF	250 V X7R	C1210	CGA6P3NP02E473J250AA
2	C21,C50	470 pF	100 V C0G	C0603	C1608C0G2A471K080AA
2	C22,C79	0.022 uF	50 V X7R	C0603	C1608X7R1H223K080AA
2	C23,C60	10 uF	16 V X7R	C0805	CL21B106KOQNNNE
5	C25,C26,C28,C75,C76	1 uF	25 V X7R	C0603	C1608X7R1E105K080AB
1	C27	1000 pF	2 KV X7R	C1206	C1206C102JGRACTU
5	C31,C32,C47,C51,C70	1000 pF	100 V C0G	C0603	C1608C0G2A102J080AA
2	C33,C56	N/U	50 V X7R	C0603	DNP
6	C36,C37,C38,C39,C40,C41	4.7 uF	80 V X7R	C1210	GRM32ER71K475KE14L
1	C46	4700 pF	200 V X7R	C0603	C0603C472K2RACTU
1	C49	0.47 uF	100 V X8R	C1210	C3225X8R2A474K200AB
2	C52,C73	4700 pF	100 V C0G	C0603	C1608C0G2A472K080AC
1	DS1	GREEN	LABEL	LED-smd-0603	150060GS75000
3	D1,D11,D12	.2 A	200 V	SOD323	BAS20HT1G
6	D2,D3,D4,D5,D9,D14	1 A	200 V	S-FLAT	CRH01(TE85L,Q,M)
1	D6	3 A	150 V	SMB_Flat	STPS3150UF
1	D7	3 A	150 V	SMB_Flat	STPS3150
2	D8,D10	.5 A	100 V	SOD523	BAS516,135
1	D13	5.1 V	200 mW	SOD523	MM5Z5V1T1G
1	J1	CONN10	LABEL		M22-5320505
1	L3	8.2 uH	10.5 A	L-2p-12p8x12p8mm	SRP1265A-8R2M
8	Q1,Q2,Q3,Q4,Q5,Q6,Q7,Q8	ISC031N08NM6	80V 23A	PG-TDSON-8	ISC031N08NM6 (OptiMOS™ 6 80 V)
4	Q9,Q11,Q14,Q16	BSC110N15NS5	150 V 76 A	PG-TDSON-8	BSC110N15NS5ATMA1 (DNP)
6	Q10,Q12,Q13,Q15,Q19,Q20	BSC110N15NS5	150 V 76 A	PG-TDSON-8	BSC110N15NS5ATMA1
1	RT1	47K NTC	1%	0603-0402	NCP15WB473F03RC
1	R1	3.01K	1%	R0603	ERJ-3EKF3011V
2	R2,R71	1K	1%	R0603	ERJ-3EKF1001V
9	R3,R4,R15,R20,R23,R26,R27,R80,R81	10K	1%	R0603	ERJ-3EKF1002V
2	R5,R6	2K	1%	R0603	ERJ-3EKF2001V
1	R7	20	1%	R1206	ERJ-8GEYJ200V
1	R8	0.0005	1 W 1%	R1206-4pin	RL1632T4F-0R5M-FNH
1	R9	39K	0.10%	R0603	ERJ-PB3B3902V

Qty.	Designator	Value	Rating	Footprint	Part number
1	R10	1K	0.10%	R0603	ERJ-PB3B1001V
20	R11,R32,R33,R34,R35,R40,R41,R42,R43,R44,R45,R46,R49,R50,R53,R54,R61,R62,R63,R74	1	1%	R0603	ERJ-3RQF1R0V
1	R12	12K	1%	R0603	ERJ-3EKF1202V
4	R13,R19,R64,R69	20	1%	R0603	ERJ-3EKF20R0V
1	R14	3.32K	1%	R0603	ERJ-3EKF3321V
3	R16,R65,R77	20K	1%	R0603	ERJ-3EKF2002V
7	R17,R21,R22,R66,R70,R76,R79	100	1%	R0603	ERJ-3EKF1000V
8	R18,R30,R31,R38,R39,R51,R56,R78	N/U	1%	R0603	DNP
2	R24,R52	0	1%	R0603	ERJ-3GEY0R00V
2	R25,R48	1.87K	1%	R0603	ERJ-3EKF1871V
1	R36	221K	1%	R0603	ERJ-3EKF2213V
1	R37	4.87K	1%	R0603	ERJ-3EKF4871V
1	R47	11K	1%	R0603	ERJ-3EKF1102V
1	R55	20K	1%	R1206	RC1206FR-0720KL
1	R57	124K	1%	R0603	ERJ-3EKF1243V
1	R58	51	1%	R0603	ERJ-6ENF51R0V
1	R59	84.5K	1%	R0603	ERJ-3EKF8452V
1	R60	1.5K	1%	R0603	ERJ-3EKF1501V
1	R67	7.5	1%	R1210	ERJ-14NF10R0U
1	R68	511	1%	R0603	ERJ-3EKF5110V
1	R72	68K	1%	R0603	ERJ-PA3F6802V
1	R73	7.5	1%	R0805	ERJ-6ENF10R0V
1	R75	20K	1%	R0805	ERJ-6ENF2002V
11	TP1,TP2,TP3,TP4,TP5,TP6,TP7,TP8,TP9,TP10,TP11	Smd Loop		TP-SmLoop_SMD	S2761-46R
1	T1	EQ25		XFMR_EQ25-10pin	EQ25-3F36+PLT25/18/2-3F36
1	T2	220 uH		LPD5030V	LPD5030V-224MR_B
1	T3	CT02-100		ICE-CT02	CT02-100
1	U1	XDP™ XDDP1100 digital power controller		QFN24-4x4mm	XDPP1100-Q024
5	U2,U3,U4,U5,U9	2EDF7275K		PG-TFLGA-13-1	2EDF7275KXUMA1
1	U6	OPA140		SOT23-5	OPA140AIDBVT
1	U7	LM5018		WSON-8	LM5018SD/NOPB
1	U8	3.3 V		SOT23	LT1460KCS3-3.3#TRMPBF
1	U10	FODM8801A		OPTO-MINI4	FODM8801A
1	W1	0		JUMP_SMD_5108	5108
3	1,2,3	PIN40		PIN40	3104-3-00-15-00-00-08-0
2	5,9	PIN60		PIN60	4357-0-00-15-00-00-03-0

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V 1.0	2024-01-18	Initial release
V 1.1	2024-06-06	Update product link and minor grammatical correction
V 1.2	2025-01-07	Update chapter 3.2 output current sense gain calculation

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