# 48 V to 12 V regulated convertor using XDP™ XDP710 eFuse and XDPP1100 digital controller

## 600 W DR-HSC

## About this document

### Scope and purpose

This application note details the necessary connections and operation guidelines for Infineon's demo board. The solution features a zero-voltage switching switched capacitor converter topology as a first stage, also known as ZSC converter with a fixed conversion ratio of 2:1. It is followed by a three-level flying capacitor dual phase stage that provides the 12 V regulated output.

The main Infineon components used in the 600 W digital dual-stage regulated hybrid switched capacitor convertor (DR-HSC) are as follows:

- 80 V OptiMOS™ 5: IPT012N08N5, 80 V N-channel linear FET 1.2 mΩ, TOLL (HSOF-8), eFuse
- 40 V OptiMOS™ 6: IQE013N04LM6, 40 V 1.35 mΩ, PQFN 3.3 mm x 3.3 mm source-down, ZSC FETs
- 25 V OptiMOS™ 5: 25 V 1.1 mΩ, PQFN 3.3 x 3.3 mm fused lead, 3LFC FETs
- 1EDN7550B: EiceDRIVER™ 1EDN7550B, one channel non-isolated gate-driver
- XDP710: XDP710 hot-swap controller, wide input voltage range (5.5 V to 80 V) system monitoring and protection IC
- XDPP1100: The smallest digital power controller with PMBus interface

### Intended audience

This document is intended for power engineers working on 48 V regulated DR-HSC hardware.

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# 1 Introduction

The rapidly increasing electricity consumption of modern data centers demands a continuous improvement at system and converter levels. In an attempt to reduce the conduction losses in DC bus distribution, recently, a 48 V has been proposed to replace the existing 12 V bus voltage. To adapt the existing 12 V infrastructure to 48 V, a DC-DC converter can provide the interface between the 48 V bus and the regulated 12 V rail. One of the biggest challenges in enabling artificial intelligence (AI) is designing a high-power density power architecture from 48 V bus voltage. In transformer-based converters, such as LLC and PSFB, the transformer also has a fixed core loss over the entire load range, limiting light-load and peak efficiency.

If isolation is not required, an IBC composed of a 2:1 SC divider and regulated 2-phase, 3-level buck converter including a balancing inductor (to balance the flying capacitors of the 3-level buck stage) is proposed. The DR-HSC converter is a novel two-stage approach where,

- The first stage is a zero voltage switching (ZVS) SC converter called ZSC convertor,
- The second stage is a dual-phase three-level flying capacitor (DP-3LFC) converter featuring an intrinsic flying capacitor balancing.

## 1.1 DR-HSC operating principle

The schematic of the DR-HSC is shown in Figure 1.

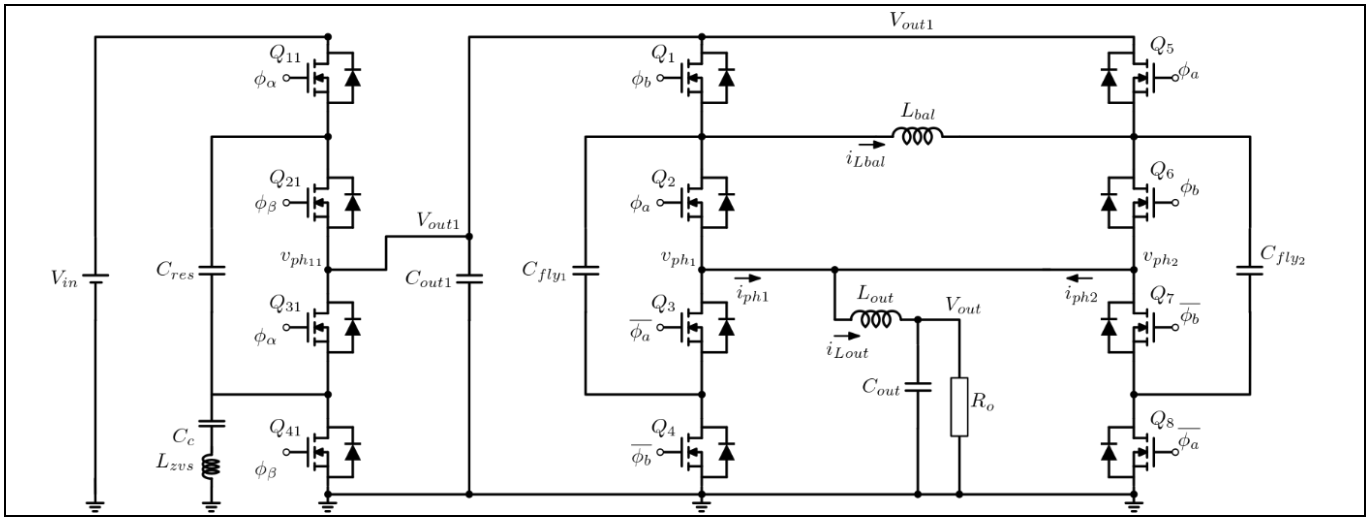



**Figure 1 Two-stage ZVS switched capacitor and three-level dual-phase buck converters with balancing inductor (DR-HSC)**

The first stage, ZSC, consists of a half-bridge multilevel structure and a resonant series LC circuit. The capacitor $C_C$ and inductor $L_{ZVS}$ are placed in series and then in parallel with $Q_{41}$ to enable ZVS operation for all switches.

The second stage, a dual-phase 3-level flying capacitor (DP-3LFC), consists of two multi-level half-bridges, two phase nodes are shorted together and the two phases are shifted by 180°. To achieve the voltage balancing of the fly capacitors, an additional balancing inductor $L_{bal}$ is added between the two positive terminals of the flying capacitor. The two phase nodes $V_{ph1}$ and $V_{ph2}$ are in phase and connected to a common output inductor $L_{out}$. DP-3LFC is controlled such that, within a part of one switching cycle $T_{sw}$, $C_{fly1}$ and $C_{fly2}$ are connected in series with the input voltage $V_{out1}$ and GND. Such a connection ensures that the voltage summation across the flying capacitors $C_{fly1}$ and $C_{fly2}$ is always the input voltage $V_{out1}$. However, by itself, the connection of the two

midpoints does not guarantee the flying capacitors balancing under all mismatch conditions, for example, strong gate driver's propagation delay mismatch. It is necessary to enforce the balancing action with an inductive component $L_{bal}$.

To analyze the DP- 3LFC waveforms at 50% duty-cycle. In this operation mode, the output inductor ripple is almost zero because of the $v_{ph1,2}(t) \simeq v_{out}(t)$. This is of paramount importance to consider since this converter is designed for a 48 V to 12 V conversion ratio, therefore such a condition is the nominal one. If low $R_{droop}$ for the first stage and low input voltage variation, the output inductor can be drastically reduced keeping low frequency operation (e.g., between 150 kHz to 250 kHz),

The main waveform for the 2:1 ZSC stage is shown in Figure 2. The main waveform for the dual-phase three-level flying capacitor buck converter DP-3LFC is shown in Figure 3.

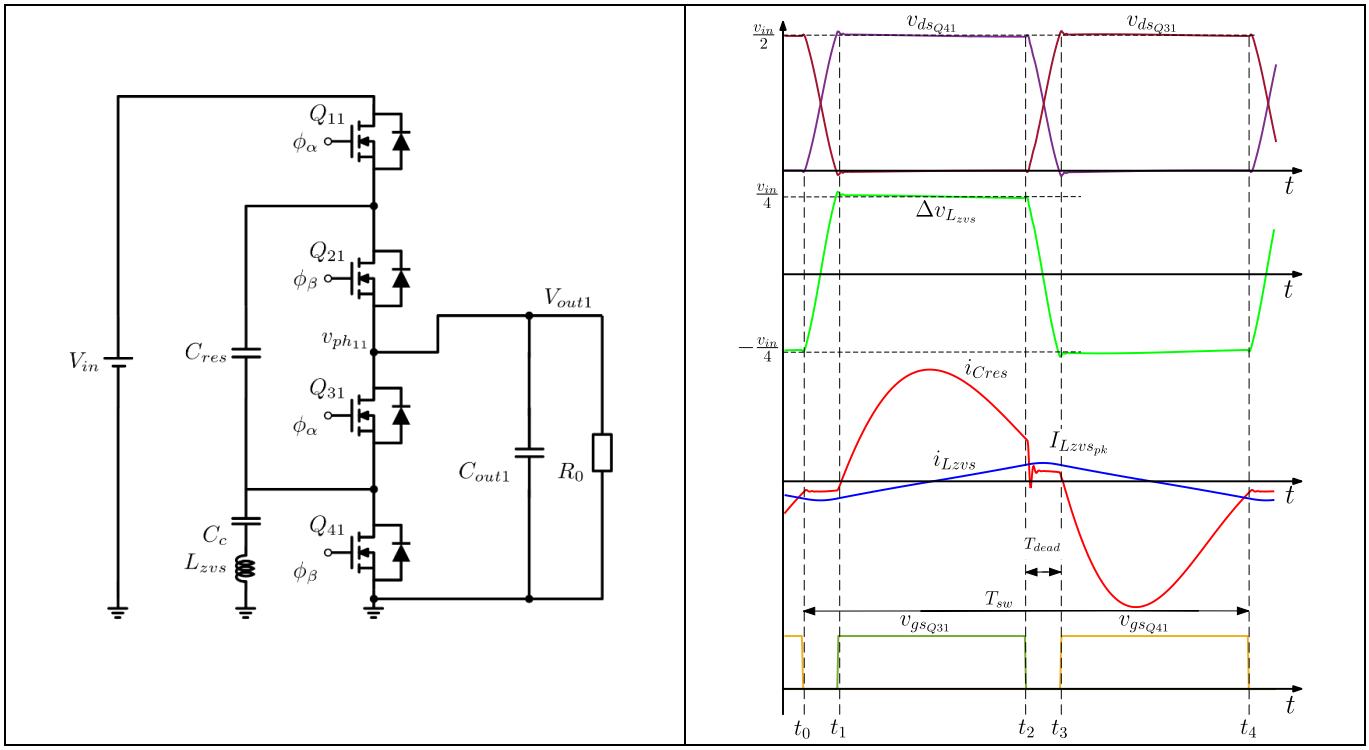



**Figure 2 ZSC convertor and main operation waveform**

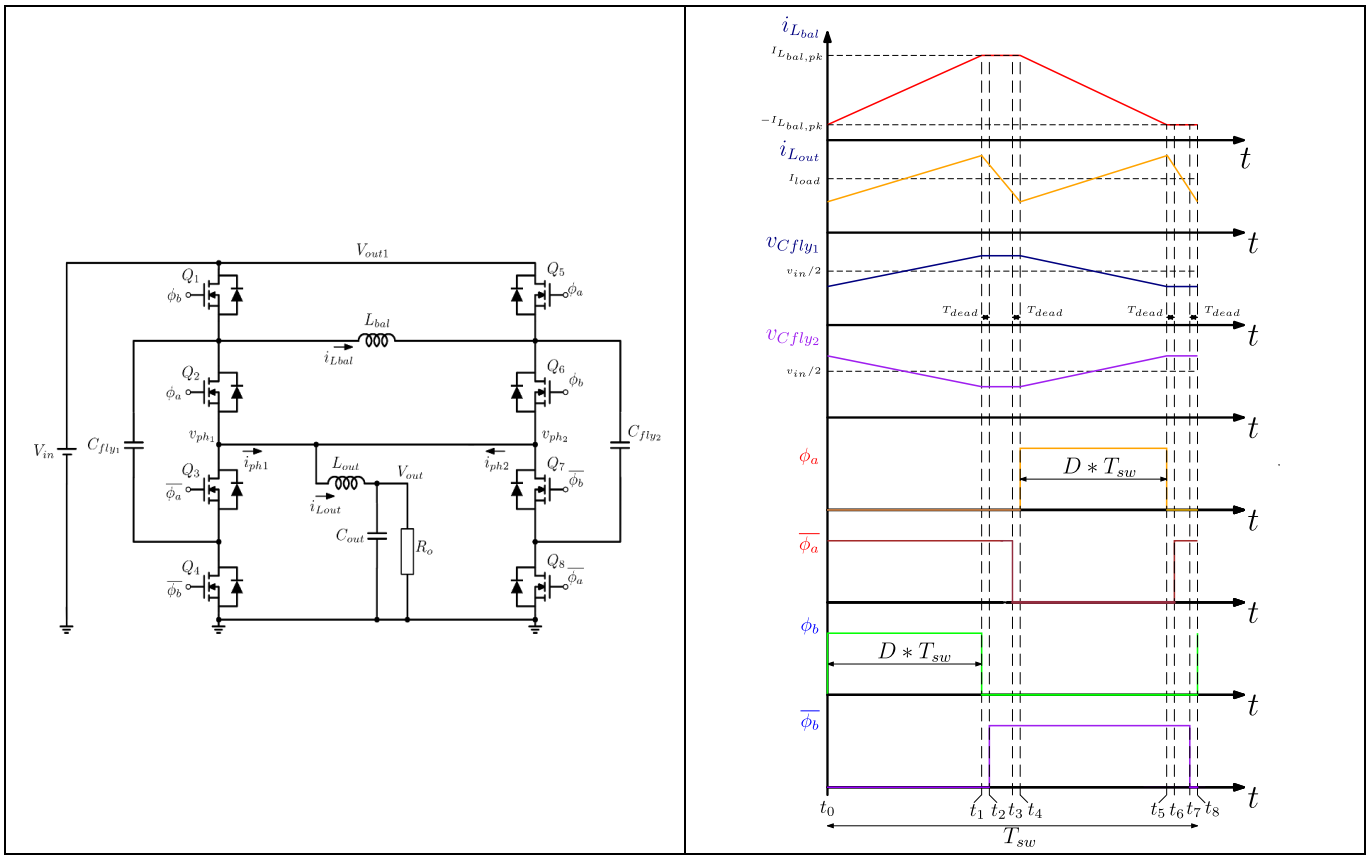



**Figure 3 DP-3LFC convertor and main operation waveform with D < 0.5**

## 1.2 DP-3LFC operational modes

The DP-3LFC converter stage is shown in Figure 3. One switching cycle $T_{sw}$ cab be split into eight subintervals. The following is for an operation cycle with duty-cycle below 50%. The eight subintervals are described as follows:

1. $t_0 - t_1$: at $t = t_0$, both the switch $Q_1$ and $Q_6$ are turned on and the flying capacitor $C_{fly1}$ is charged from the input and is connected with $Q_3$ to the node phase $V_{ph1}$ powering the output inductance, while $C_{fly2}$ is discharged powering the output inductance $L_{out}$. In this phase, the output inductance is powered with $v_{out1} - v_{C_{fly2}}$ and from $v_{C_{fly1}}$ ,respectively, from the source of $Q_6$ and the drain of $Q_3$. During this phase the balancing inductor current rises from $-I_{L_{bal,pk}}$ to $I_{L_{bal,pk}}$ with a slope of $v_{C_{fly2}}/L_{bal}$.
2. $t_1 - t_2$: at $t = t_1$, both the switch $Q_1$and $Q_6$ are turned off.
3. $t_2 - t_3$ : at $t = t_2$ after a dead-time period $T_{dead}$, the switch $Q_4$ and $Q_7$ are turned on and the output inductance is discharged with a slope of $V_{out}/L_{out}$. The two flying capacitors $C_{fly1}$ and $C_{fly2}$ are kept to stable voltage levels $v_{C_{fly1}}(t_1)$ and $v_{C_{fly2}}(t_1)$ respectively. During this phase, the $I_{L_{bal}}$ current flows between $Q_4$ and $Q_8$.
4. $t_3 - t_4$: at $t = t_3$ , both the switch $Q_3$ and $Q_8$ are turned off.
5. $t_4 - t_5$: at $t = t_4$, after a dead-time period $T_{dead}$, both the switch $Q_2$ and $Q_5$ are turned on, the flying capacitor $C_{fly2}$ now is charged from the input and is connected with $Q_7$ to the node phase $v_{ph2}$ powering the output inductance, while $C_{fly1}$ is now discharging, powering the output inductance $L_{out}$. In this phase the output inductance is powered from $v_{in} - v_{C_{fly1}}$ and from $v_{C_{fly2}}$ respectively from the source of $Q_2$ and

the drain of $Q_7$ . During this phase the balancing inductor current falls from $I_{L_{bal,pk}}$ to $-I_{L_{bal,pk}}$ with a slope of $v_{C_{fly1}}/L_{bal}$.

6. $t_5 - t_6$: at $t = t_5$, both the switch $Q_5$ and $Q_2$ are turned off.
7. $t_6 - t_7$: at $t = t_6$ after a dead-time period $T_{dead}$ , both the switch $Q_8$ and $Q_3$ are turned on. In this phase, the output inductance is discharged with a slope of $V_{out}/L_{out}$. The two flying capacitors $C_{fly1}$ and $C_{fly2}$ are kept to a stable voltage level, $v_{C_{fly1}}(t_5)$ and $v_{C_{fly2}}(t_5)$, respectively. During this phase, the $i_{L_{bal}}$ current flows between $Q_4$ and $Q_8$ keeping a stable value of $-I_{L_{bal,pk}}$ .
8. $t_7 - t_8$: at $t = t_7$ , both the switch $Q_4$ and $Q_7$ are turned off. At $t = t_8$ switch Q

From the converter operations illustrated above, it can be stated that any non-ideal behavior of the converter would be balanced by both converter symmetry and balancing inductor, without influencing the voltage loop since the mean value of $V_{ph1,2}$ is not affected.

## 1.3 Flying capacitor voltage balancing in DP-3LFC

The voltage stabilization of the flying capacitors to half of the input voltage is achieved through a capacitive and an inductive coupling between the two three-level flying capacitor phases, respectively from the phase node short and balancing inductor.

The series connection of the two flying capacitors during the subintervals $t_0 - t_1$ and $t_4 - t_5$ forces the sum of the two flying capacitors to be equal to the input voltage of the DP-3LFC stage. The main difference between subintervals $t_0 - t_1$ and $t_4 - t_5$ is that the capacitor $C_{fly2}$ is at the bottom of the series connection while in $t_4 - t_5$, $C_{fly1}$ is at the bottom of the series connection during the first interval. The voltage applied to the output inductor is equal to the voltage of the bottom capacitor ($V_{C_{fly,bottom}}$) minus the output voltage during these phases. By assuming a certain voltage deviation between $V_{C_{fly1}}$ and $V_{C_{fly2}}$ : $\Delta V = \frac{V_{C_{fly1}} - V_{C_{fly2}}}{2}$, it is possible to derive the time-dependent behavior of the re-balancing process from an initial voltage mismatch of $\Delta V_{init}$:

$$\Delta V(t) = \Delta V_{init} \cdot e^{-t/\tau}$$

**Equation 1**

Where, the time-constant $\tau$ of the balancing depends on various system parameters and can be described with sufficient accuracy by the following equation:

$$\tau \simeq \frac{f_{sw}}{f_{res}} \frac{\sqrt{L_{out} C_{fly}}}{2R_{cond}} \frac{1}{D_{adj}}$$

**Equation 2**

Where, the resistance $R_{cond}$ is the lumped resistance of the conduction path of the bottom capacitor to the output, while $f_{res} = \frac{1}{2\pi\sqrt{L_{out}\, C_{fly}}}$ is the resonant frequency and adjusted duty-cycle is:

$$D_{adj} = \begin{cases} 2 \cdot D & D < 0.5 \\ 2 \cdot (1 - D) & D \geq 0.5 \end{cases}$$

**Equation 3**

However, the capacitive charge distribution cannot keep the flying capacitors voltage stabilized during all the non-ideal mechanisms (e.g., strong driving delay imbalance). Therefore, to improve flying capacitor voltage balancing, an inductive component is required between the two 3LFC phases. The $Q_4$ is controlled by $\overline{\phi_b}$, whereas $Q_8$ is controlled by $\overline{\phi_a}$, having the output inductor valley current always positive, and considering the flux balancing of the balancing inductor $L_{bal}$, the following equation is valid:

$$\frac{T_{on_{\phi a}}}{T_{on_{\phi_b}}} = \frac{V_{Cfly2}}{V_{Cfly1} - DCR_{L_{bal}} * I_{bal,dc}}$$

**Equation 4**

Where $DCR_{L_{bal}}$ is the DC resistance of the balancing inductor. From Equation 4 it follows that the average voltage of $V_{C_{fly2}}$ equals to $V_{C_{fly1}}$, therefore $V_{C_{fly1}} = V_{C_{fly2}} = \frac{V_{in}}{2}$ when there is not a strong difference between $T_{on_{\overline{\phi a}}}$ and $T_{on_{\overline{\phi_b}}}$

When an unbalance is applied between the two phases of the 3LFC-DP converter, a DC current is built into the balancing inductor. Figure 4 shows the equivalent model of the DC current within the balancing inductor.

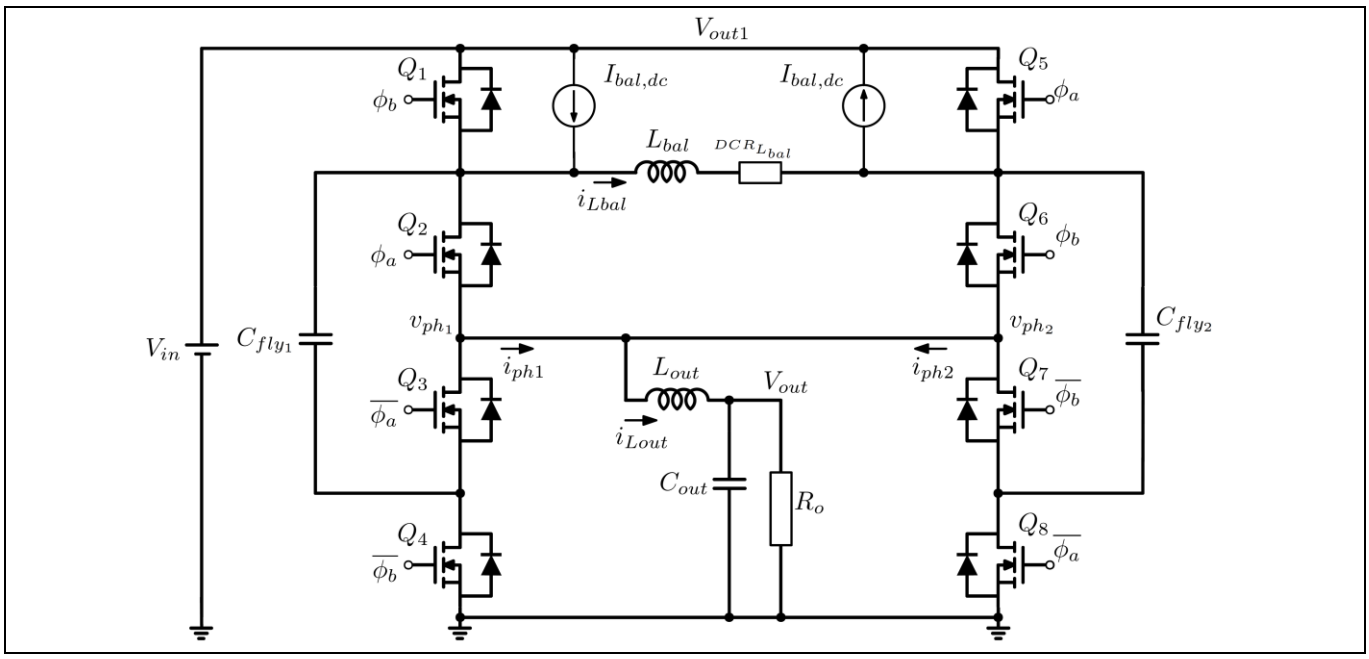



**Figure 4 Three-level dual-phase buck converters with equivalent balancing model**

If $T_{on_{\phi a}} < T_{on_{\phi_b}}$, considering the converter is running and operating with positive valley current on the output inductor, the voltage of the flying capacitors will slightly drift from $\frac{V_{in}}{2}$, as shown in Equation 4. Balancing

inductor compensation would seek to discharge the $C_{fly1}$ , when connected to $V_{in}$ , discharging it when connected to ground potential, achieving the voltage balancing point as can be demonstrated with the following equation:

$$Q_{ina} = Q_{inb}$$

**Equation 5**

where $Q_{inb}$ and $Q_{ina}$ are respectively the net charges and discharges in the flying capacitor $C_{fly1}$ ,can be expressed as:

$$Q_{inb} = \int_0^{T_{on_{\phi_b}}} \left( \frac{V_{in} - V_{C_{fly1}}}{2L_{out}} t + \frac{I_{out}}{2} - \frac{I_{bal,dc}}{2} \right) dt$$

**Equation 6**

$$Q_{ina} = \int_0^{T_{on_{\phi_a}}} \left( \frac{V_{C_{fly1}}}{2L_{out}} t + \frac{I_{out}}{2} - \frac{I_{bal,dc}}{2} \right) dt$$

**Equation 7**

Equation 6 and Equation 7 are derived without considering MOSFET body diode conduction, $V_{C_{fly1}}$ is the average voltage within one switching cycle across $C_{fly1}$ . By combining Equation 4, Equation 6, and Equation 7, the DC current of the balancing inductor can be calculated with the following equation.

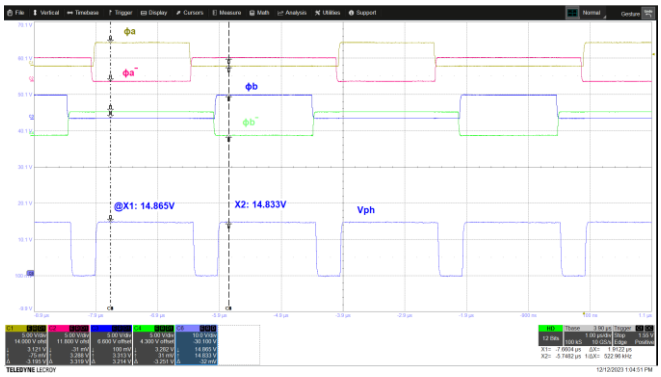
$$I_{bal,dc} = I_{out} \frac{T_{on_{\phi_b}} - T_{on_{\phi_a}}}{T_{on_{\phi_b}} + T_{on_{\phi_a}}} + 2 \frac{V_{in} T_{on_{\phi_b}}^2 - V_{Cfly1} \left( T_{on_{\phi_b}}^2 + T_{on_{\phi_a}}^2 \right)}{4L_{out} \left( T_{on_{\phi_b}} + T_{on_{\phi_a}} \right)}$$

**Equation 8**

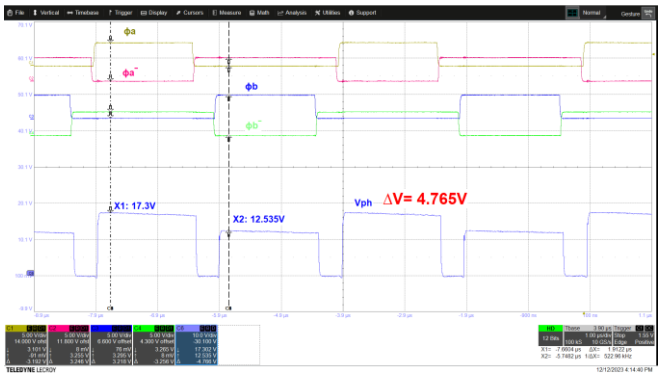
To validate the voltage balancing of the flying capacitors, the test is done with the following conditions:

- With and without the balancing inductor $L_{bal}$
- To apply a strong unbalanced between the $\phi_a$ and $\phi_b$, set the dead-time $\phi_{a_{dt}} = 20\text{ns} + \phi_{b_{dt}}$.

In the Figure 5(a), the test is done with the balancing inductor $L_{bal}$ adopted. It shows that the flying capacitors are kept at the same, the voltage results in a low ripple in the output inductor. In the Figure 5(b), the test is done without the balancing inductor $L_{bal}$. The two flying capacitors are drifting by 4.765 V from 30 V input voltage with an output current $I_{out}$ of 25 A.




(a) Vin = 60 V, Iout = 0 A, with the $L_{bal}$, $\phi_{a_{dt}} = 20\text{ ns} + \phi_{b_{dt}}$

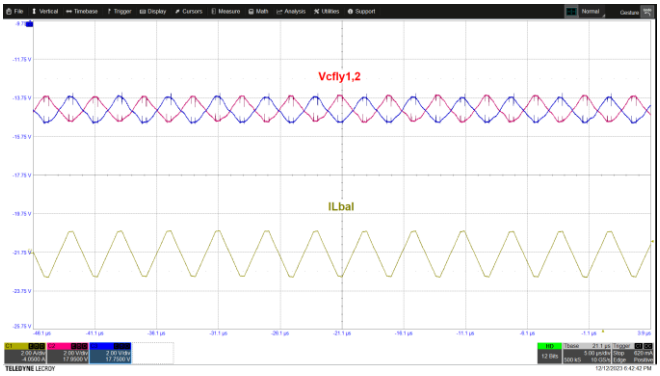



(b) Vin = 60 V, Iout = 25 A, without the $L_{bal}$ $\phi_{a_{dt}} = 20\text{ ns} + \phi_{b_{dt}}$

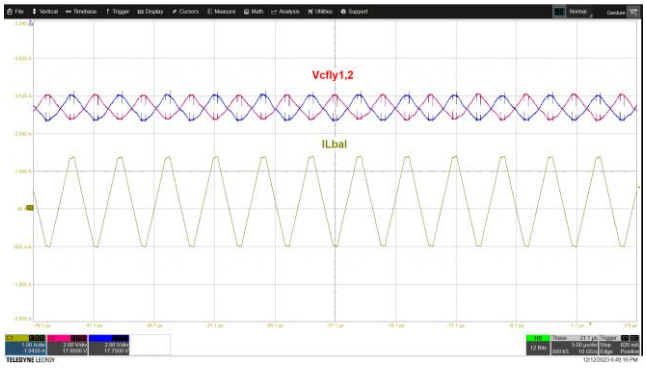
**Figure 5 Flying capacitor voltage balancing**

When the balancing inductor needs to compensate a non-ideal behavior of the 3LFC, as explained with Equation 8, a DC current is established within the balancing inductor.

The balancing inductor current has been measured, without the unbalanced applied (e.g. $\phi_{a_{dt}} = \phi_{b_{dt}}$) and with the unbalanced applied (e.g., $\phi_{a_{dt}} = 20\text{ ns} + \phi_{b_{dt}}$). A DC current of 250 mA flows between two phases throughout the balancing inductor. The maximum current built into balancing inductor is negligible with respect to the output current and therefore the balancing inductor is carrying mostly a small-sized AC current.




(a) Vin = 60 V, Iout = 50 A $\phi_{a_{dt}} = \phi_{b_{dt}}$




(b) Vin = 60 V, Iout = 50 A $\phi_{a_{dt}} = 20\text{ ns} + \phi_{b_{dt}}$

**Figure 6 Balancing inductor current**

# 2 Board information

## 2.1 Description

The 48 V regulated DR-HSC converter is Infineon's patented topology. The board is capable of power transfer from 48 V to 12 V regulated. The process of power transfer consists of the following two stages:

1. An unregulated ZVS switched capacitor converter, converting the 48 V input voltage down to 24 V $V_{mid}$ voltage.
2. A regulated dual-phase three-level flying capacitor stage, converting the 24 V $V_{mid}$ down to 12 V Vout. A hot-swap controller, XDP710, is incorporated for a safe soft-start to limit the inrush current and providing protection capabilities during operation.

## 2.2 Features

This system consists of three main blocks shown in Figure 7 and Figure 8.

- The first block is the hot-swap stage that secures the converter against the bouncing of the input voltage and guarantees a safe soft startup.
- The second block is acts as a voltage divider called a zero-voltage switching switched capacitor converter (ZSC). This stage converts the input voltage down by half with a fixed ratio at fixed switching frequency, fixed duty-cycle, and dead-time over the full load range.
- The last block is based on a regulated three-level flying capacitor dual phase converter. This stage uses voltage mode duty-cycle control algorithms to regulate the variable input voltage to a regulated 12 V rail.

The board is capable of delivering 600 W continuous power over an input voltage range from 44 V – 60 V. An auxiliary power supply to provide bias voltage for gate driver, 3.3 V and 6.5 V $V_{DD}$ during operation, with an output power higher than 300 W is required. A fan is required and should be placed next to the converter with about 100 CFM of airflow. The eFuse stage is controlled by a wide input voltage hot-swap controller XDP710, which drives a single N-channel MOSFET. In addition to a SOA controlled turn ON, the XDP710 provides continuous system health monitoring and communication to the main MCU via the PMBus interface. The ZSC and 3LFC-DF stages are driven and regulated by a digital controller, XDPP1100. XDPP1100 also controls the enable sequencing of the eFuse. The digital controls provide the utmost flexibility in design, efficiency, optimization, and customized FW capability to implement application add-on features.

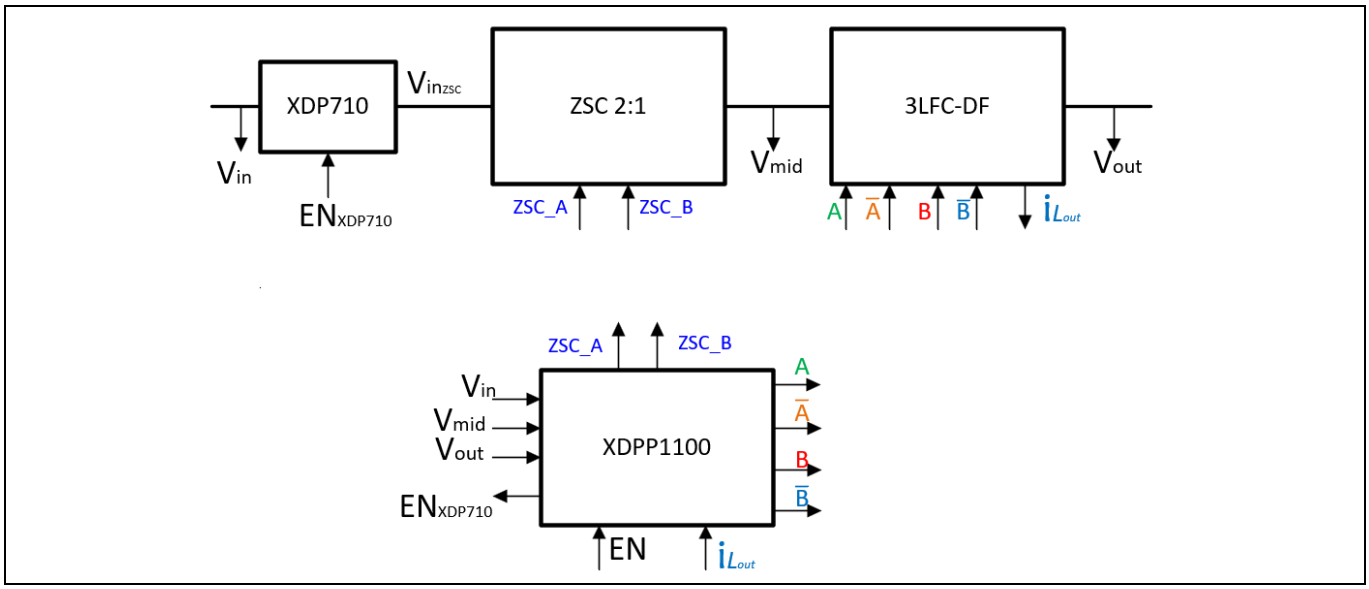



**Figure 7 Regulated 48 V to 12 V DR-HSC converter basic operation.**

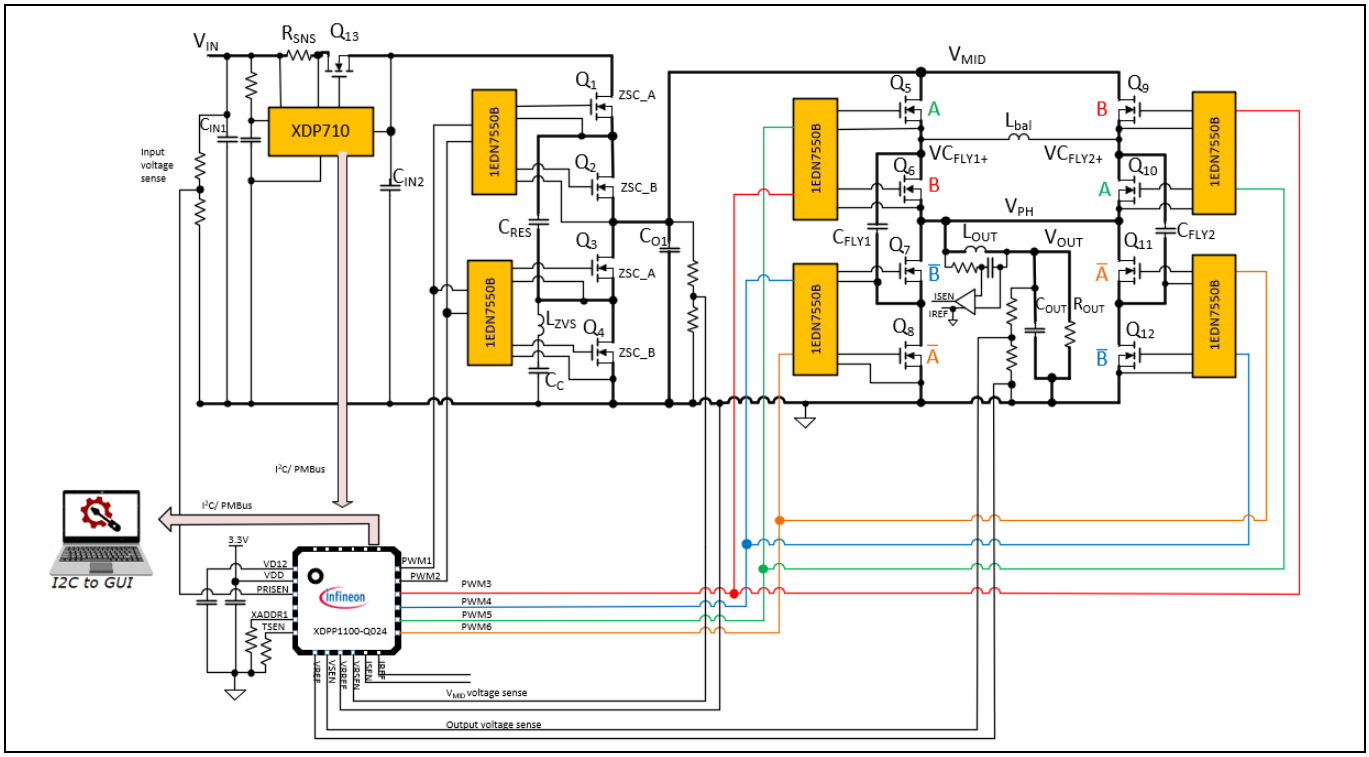



**Figure 8 DR-HSC block diagram**

## 2.3 Reference design

The reference design of the 600 W DR-HSC is shown in Figure 9. The top view is on the left and the bottom view is on the right. The 3D rendering of the PCB is shown in Figure 10. The board dimensions are $114\ \text{mm} \times 77\ \text{mm} \times 15\ \text{mm}$.

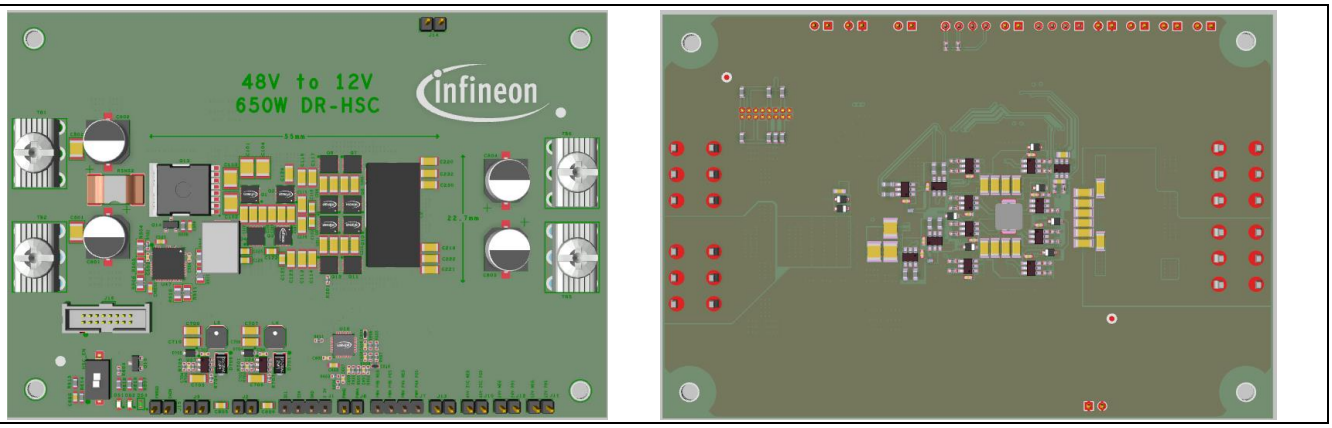



**Figure 9 Top and bottom side of the DR-HSC board**

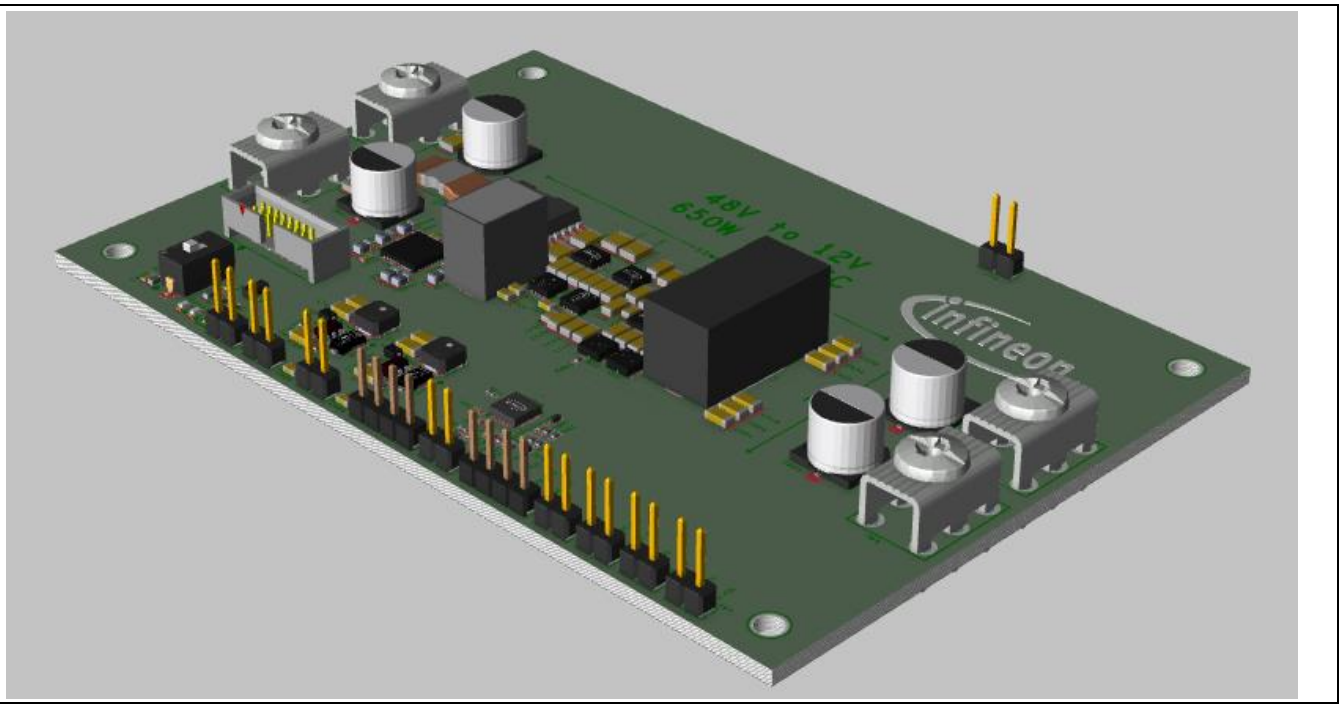



**Figure 10 3D PCB view of the DR-HSC Board**

Top and bottom views of the hardware demo board including the labeling of the main components are shown in Figure 11, Figure 12, and Figure 13.

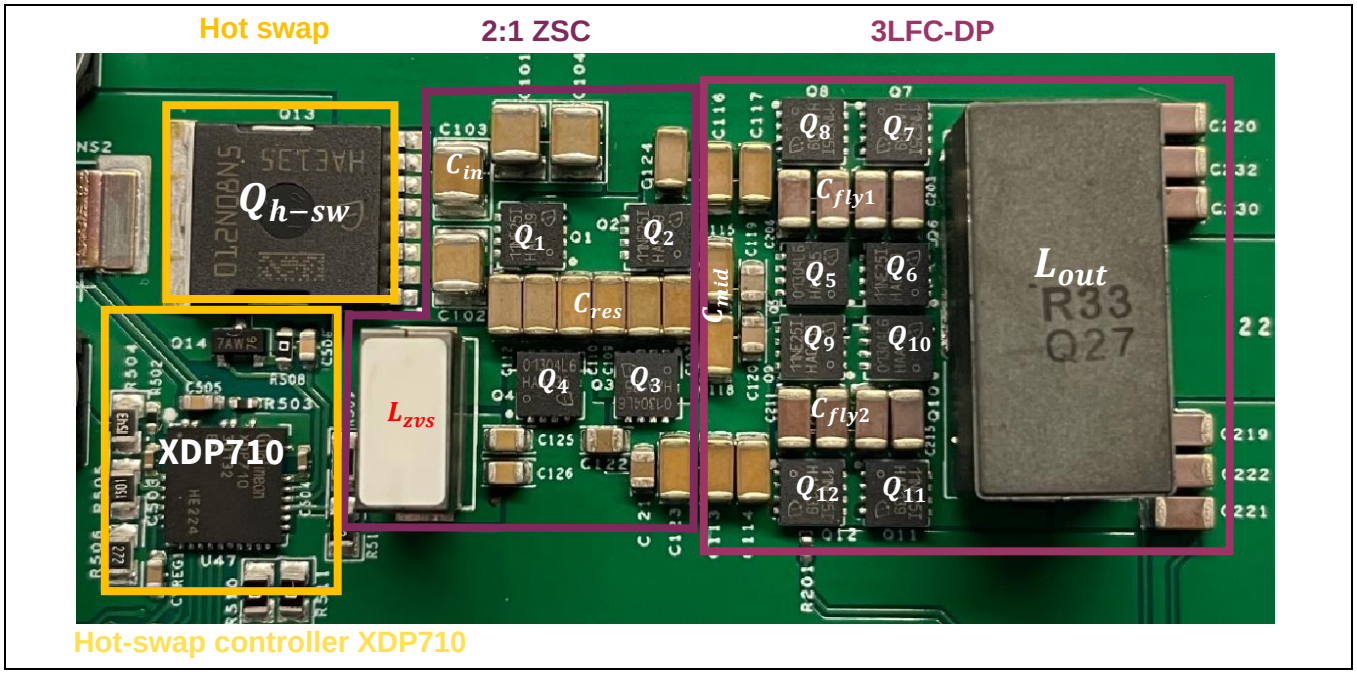



**Figure 11 Top-view of the demo board for the regulated 48 V to 12 V DR-HSC converter**

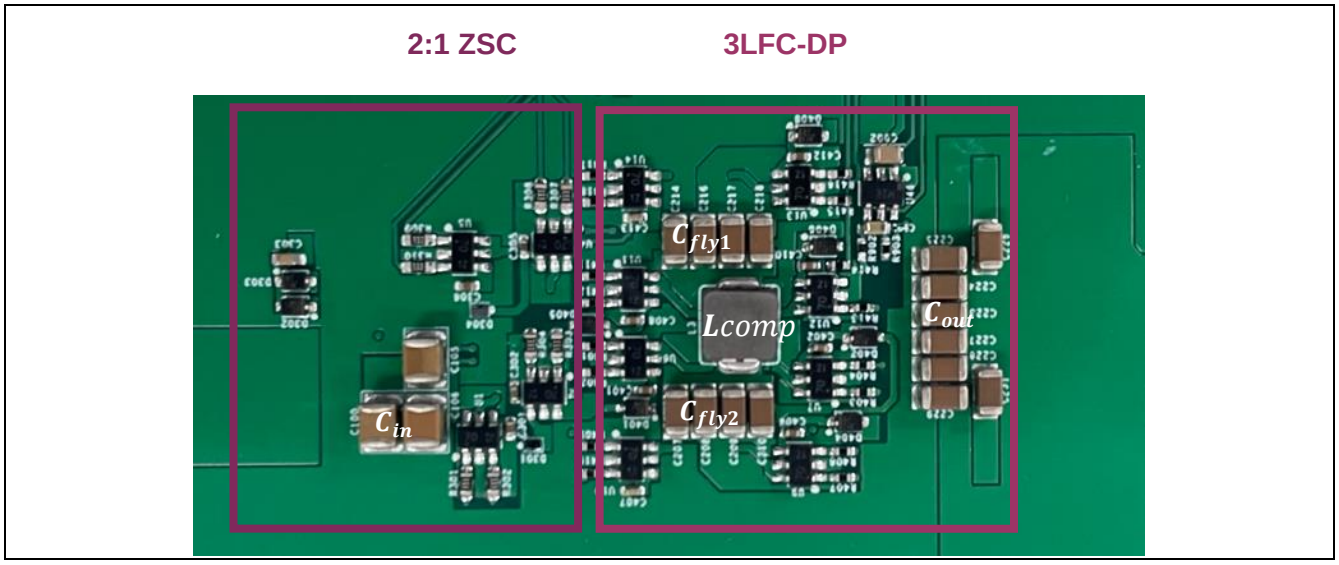



**Figure 12 Bottom-view of the demo board for the regulated 48 V to 12 V DR-HSC converter**

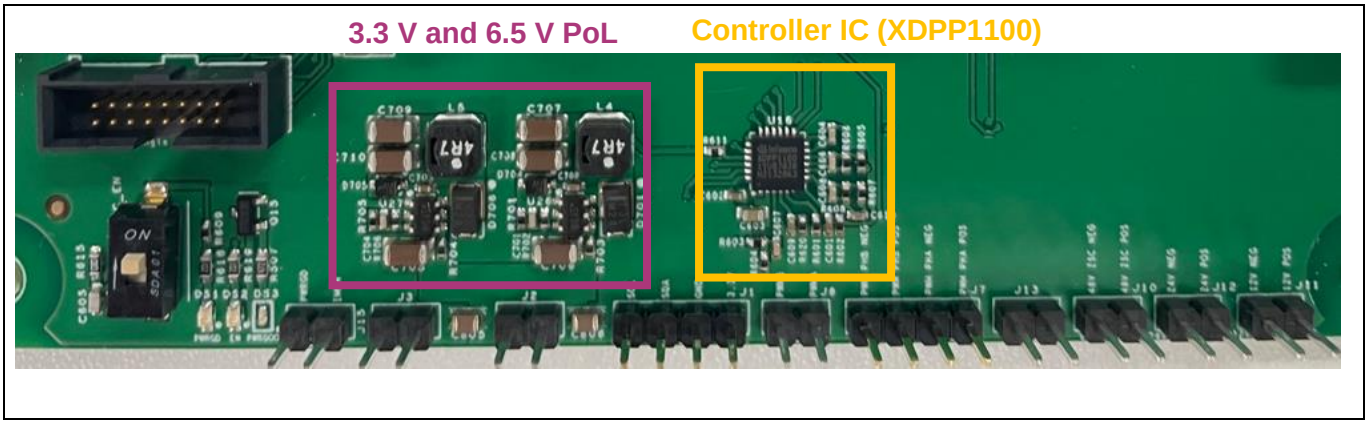



**Figure 13 Controller IC and aux power location of the hardware demonstrator**

## 2.4 Board parameters and technical data

- Input voltage range: +44 V to +60 V DC
- Minimum VIN to turn on: 44 V
- Airflow: 100 CFM (at maximum output current)
- Protection features: input and output overvoltage, overtemperature, and overcurrent

All other board parameters are summarized in Table 1.

**Table 1 Parameters and recommended operating conditions**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Input voltage range | VIN_ON | 44.0 | 48.0 | 60.0 | V |
| Output voltage | $V_{OUT}$ | 11.5 | 12.0 | 12.5 | V |
| Output power | $P_{OUT}$ | – | 600 | 650 (10 ms) | W |
| Output current | $I_{OUT}$ | – | – | 50 | A |
| ZSC switching frequency | $f_{SW}$ | – | 630 | – | kHz |
| 3LFC switching frequency | $f_{SW}$ | – | 250 | – | kHz |
| Output voltage ripple | $V_{ripple}$ | – | – | 130 | mV |

# 3 Operating instructions

## 3.1 Input/output connectors

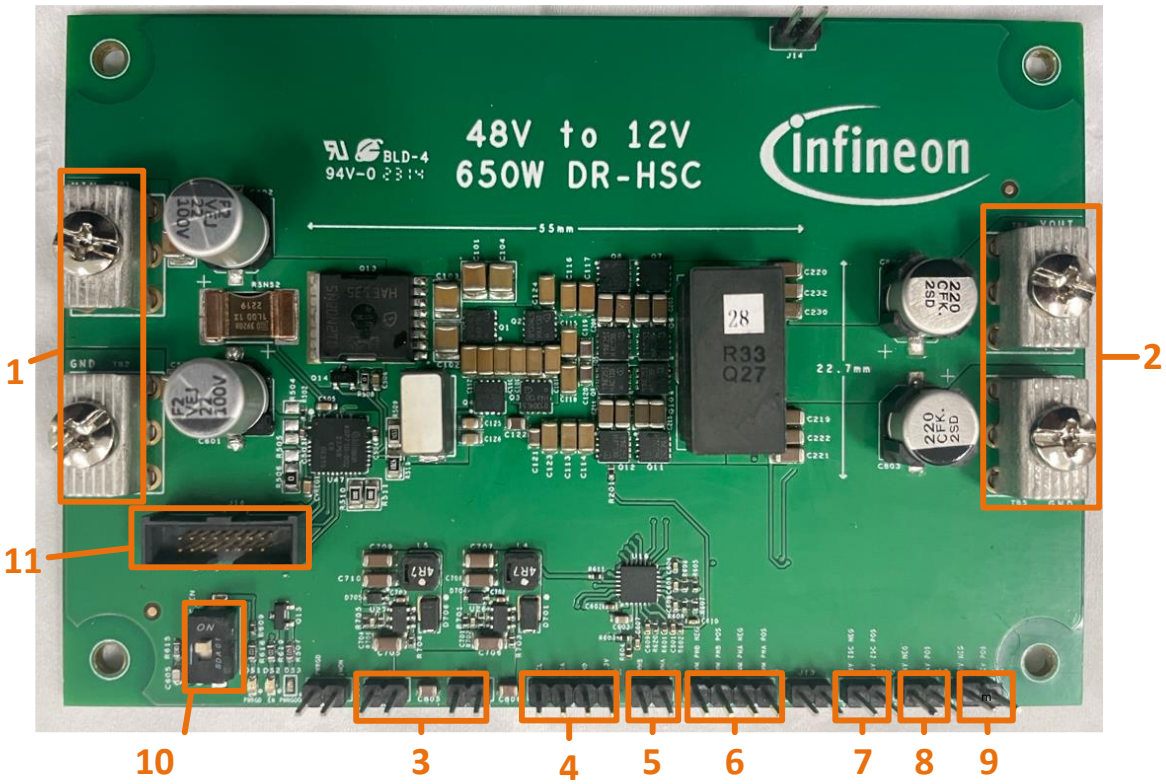



**Figure 14 DR-HSC main input and output voltage connection lugs**

1. Main input voltage connector.
2. Main output voltage connector.
3. 12 V AUX power connector. A regulated +12 V AUX supply capable of 1 A is required for all auxiliary voltage rails and soft start circuits.
4. Communication data lines to the controller XDPP1100. (SCL, SDA, GND, 3.3 V)
5. Pulse pattern signals for the ZSC stage (PWMA, PWMB)
6. Pulse pattern signals for the 3LFC-DF stage (PWM_PHB_NEG, PWM_PHB_POS, PWM_PHA_NEG, and PWM_PHA_POS) Differential positive and negative measurement point on the input (Vin).
7. Differential positive and negative measurement point on the midpoint (24 V mid).
8. Differential positive and negative measurement point on the output (12 Vout).
9. ON/OFF switch for the 3LFC-DP
10. Hot-swap controller XDP710 communication and programming connector.

## 3.2 Power sequence

1. Apply +12 V capable of 1 A at 12 V and GND (connector 3 shown in Figure 14).
2. Set the 12 V output loading current to 0 A before the 12 V output is ready.
3. Toggle the on/off switch of the converter if necessary.

4. Apply a DC voltage between 44 V and 60 V on the input lugs (Connector 1 shown in Figure 14). The converter is automatically starts up if the input voltage is in the specified window.
5. Observe that Vout rises over the test pins (Connector 9 shown in Figure 14) or directly across the Vout capacitors.
6. In case of a system shutdown, turn OFF the main DC supply voltage and wait until Vout reaches zero.

*Note: Before turning on the main DC Vin, make sure +12 V AUX is reset by turning OFF/ON the 12 V AUX power supply.*

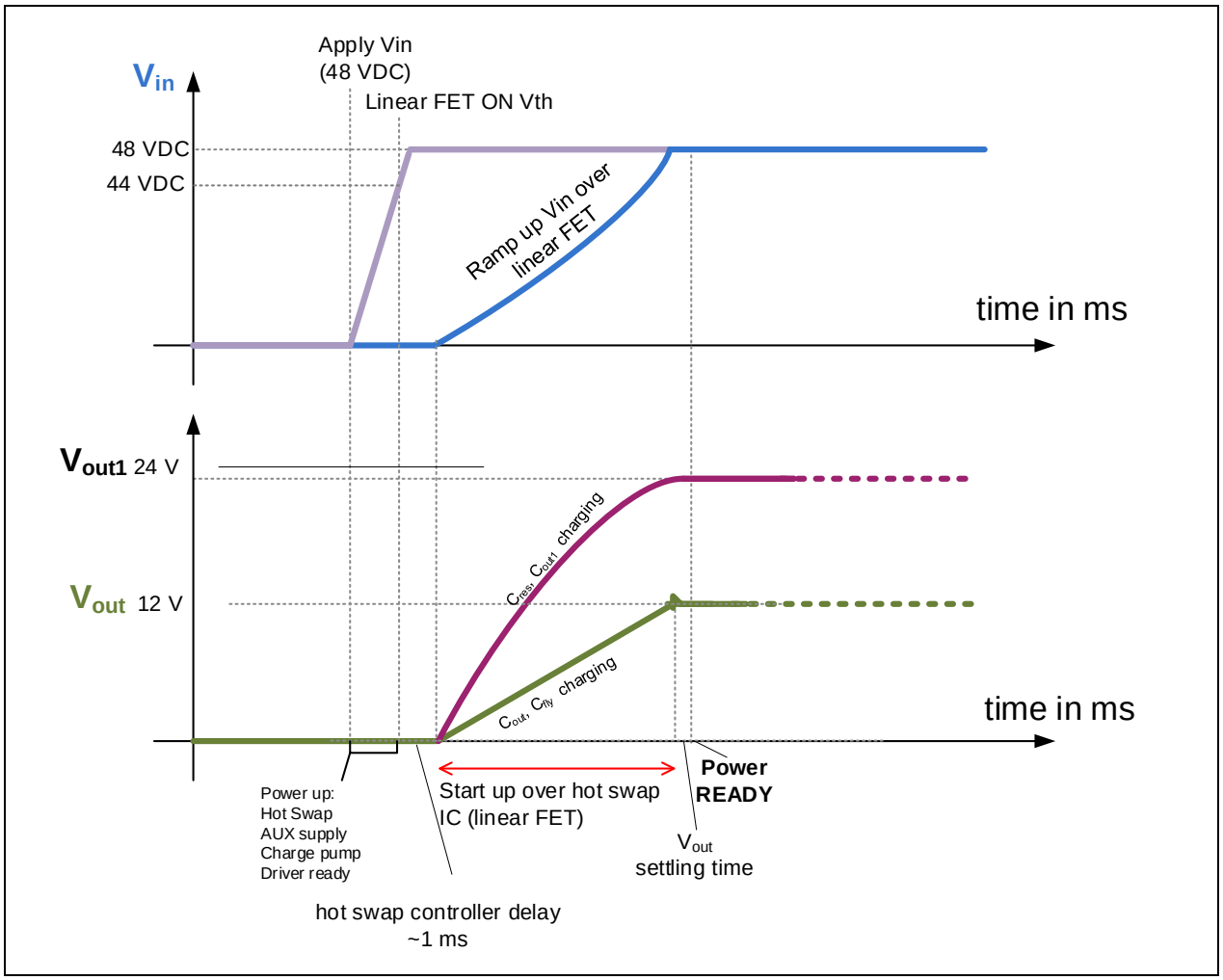



**Figure 15 DR-HSC, basic startup, and power up sequence timing diagram**

# 4 XDP710 hot-swap controller

The hot-swap controller XDP710 is capable of managing a controlled system turn ON and avoiding any inrush events by driving an external N-channel MOSFET within its safe operating area (SOA). It also incorporates an extensive variety of system protections for safety operations and generates various protection responses depending on the severity of the incident. You can use the Infineon GUI XDP designer to configure the hot-swap controller. See the XDP710 application note for more information.

In this board, an 80 V N-channel linear MOSFET IPT012N08N5 is controlled by the XDP710 hot-swap controller. The purpose of adopting the hot-swap controller is to limit the inrush current and implement the soft-start as the first stage 2:1 ZSC convertor operates in an open-loop mode. The dv/dt of the input voltage can be controlled so that the input voltage is delivered smoothly to the capacitor of the ZSC convertor. The SOA of the FET consists of a maximum allowed drain current that depends on its drain to source voltage. The more the voltage, the less current allowed through the FET. XDP710 has a closed control loop that monitors the current through the FET and its drain to source voltage. The current flow that charges the ZSC capacitor is controlled according to the FET's SOA.

# 5 XDPP1100 digital power controller

## 5.1 XDPP1100 configuration

The FW patch and optimized configuration are stored in the nonvolatile memory OTP. You can run the demo board by following the instructions in Section 3.2 without needing additional configuration. To evaluate XDPP1100, you can change configuration such as fault thresholds or response. Most of the configurations can be changed on the fly. The modified configurations are stored in the RAM and can be modified an unlimited number of times. However, once the input voltage and 3.3 V VDD are removed, the modifications will be lost and reset to the default OTP settings. To keep the new configuration, you can store the customized configuration to the OTP. See the XDPP1100 application note for more information.

This design uses XDPP1100-Q024, which is a 24-pin device and drives two loops. Therefore, the Loop1 PMBus commands are not visible if it auto-populates the device into the graphical user interface (GUI). You need to force the I2C/PMBus communication and add XDPP1100-Q040 (40-pin version) to configure the device.

To verify the design tool, perform the following steps:

1. Connect the I²C dongle to the I²C connector on the board.
2. Load the design file (*REF_600W_DR-HSC_XDPP.pcd*).
3. In the **Options** tab, check **Force i2c/PMBus OK** as shown in Figure 16.
   This step is mandatory as the device cannot be detected by using **Auto populate**.

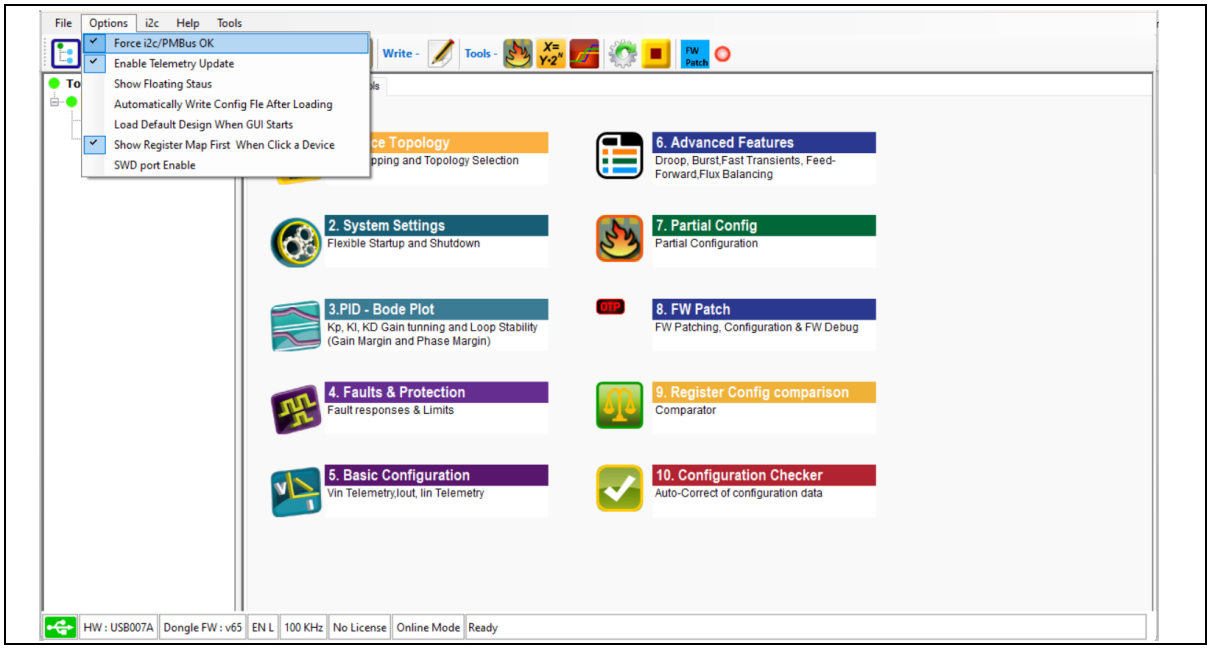



**Figure 16 Load design file through GUI and read from the device**

4. Power up the board.
   The GUI will show a pop-up window automatically after establishing communication as shown in Figure 17.

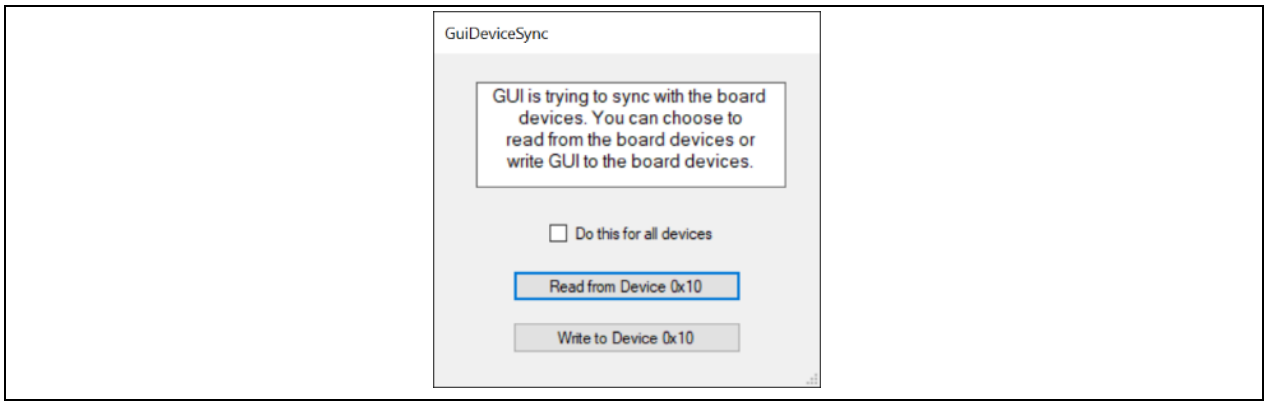



**Figure 17 Read from Device operation**

5. Click **Read from Device 0x01**.
   This will read the configuration file from XDPP1100.

## 5.2 Control loop

In the XDPP1100 GUI shown in Figure 18, use the XDPP1100-Q040 configuration for XDPP1100-Q024 to implement two digital control loops.

- Loop0: Controls the regulated 3LFC and it is closed loop with VMC control mode.
- Loop1: Controls the open-loop ZSC.

*Note: Both Loop0 and Loop1 are used to control the whole system and do not turn on/off either the ZSC stage or the 3LFC stage separately by the PMBus command "Operation".*

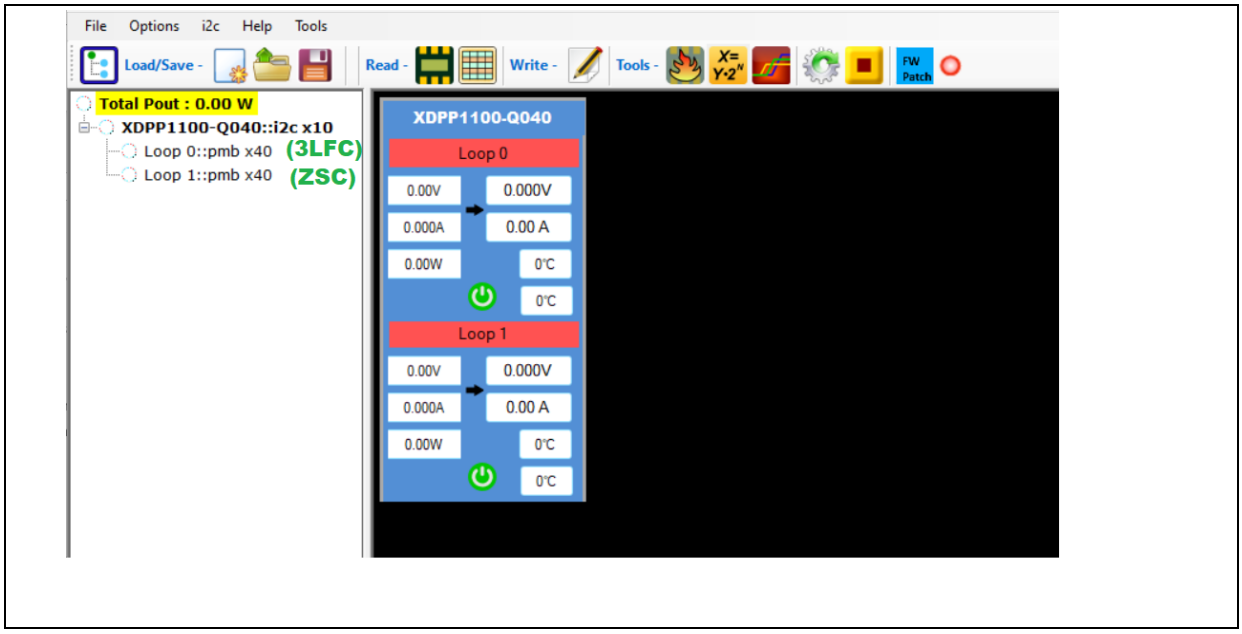



**Figure 18 XDPP1100-Q024 control loop**

## 5.3 Topology and dead-time configuration

Loop0 controls the three-level flying capacitor buck (3LFC). Loop0 is configured to half-bridge (HB) topology to drive the interleaved 3LFC as shown in Figure 18. The control loop of the 3LFC is the same as Buck, $D = V_{OUT}/V_{IN\_3LFC}$. Here the input voltage of 3LFC is the output of the 2:1 ZSC, ½ $V_{IN}$. When $V_{OUT}$ is higher than ½ $V_{IN\_3LFC}$ or ¼ $V_{IN}$, the duty-cycle is higher than 50%. The HB control loop has the same duty-cycle equation, and it could be used to control the 3LFC.

The drawback of half-bridge topology is that the max duty-cycle of HB is limited to 100%. In other words, each 3LFC phase duty-cycle is limited to 50%. When the output voltage is higher than ¼ $V_{IN}$, the 3LFC stage loses regulation. To compensate for the duty-cycle limit, the PWM falling edge dead-time is used to extend the pulse width. XDPP1100 allows a maximum of 318.75 ns dead-time. In this design, PWM3 and PWM4 falling edge dead-time is set to 298.75 ns. At the 250 kHz switching frequency, the 298.75 ns provides 7.5% duty-cycle extension. This allows for regulation at 44 V input as shown in Figure 21.

The benefit of using HB topology is the duty-cycle lock feature of the XDPP1100. The XDPP1100 could lock the odd and even duty-cycle of bridge topologies. The pulse width only adjusts at the even cycle and keeps the odd cycle the same as the even cycle. This helps to keep the voltage balancing of the two flying capacitors.

In the XDPP1100 GUI Topology design tool, configure the following parameters:

- **Loop0 3LFC**: Configure the topology to half-bridge primary and center-tapped secondary, mapping the PWMs per HW connection.

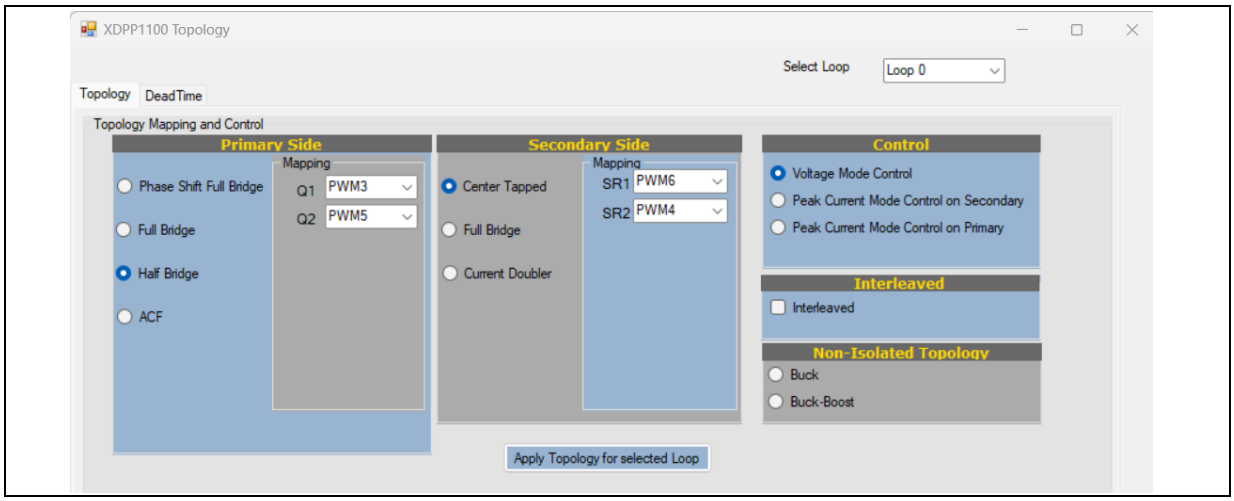



**Figure 19 3LFC topology and control mode**

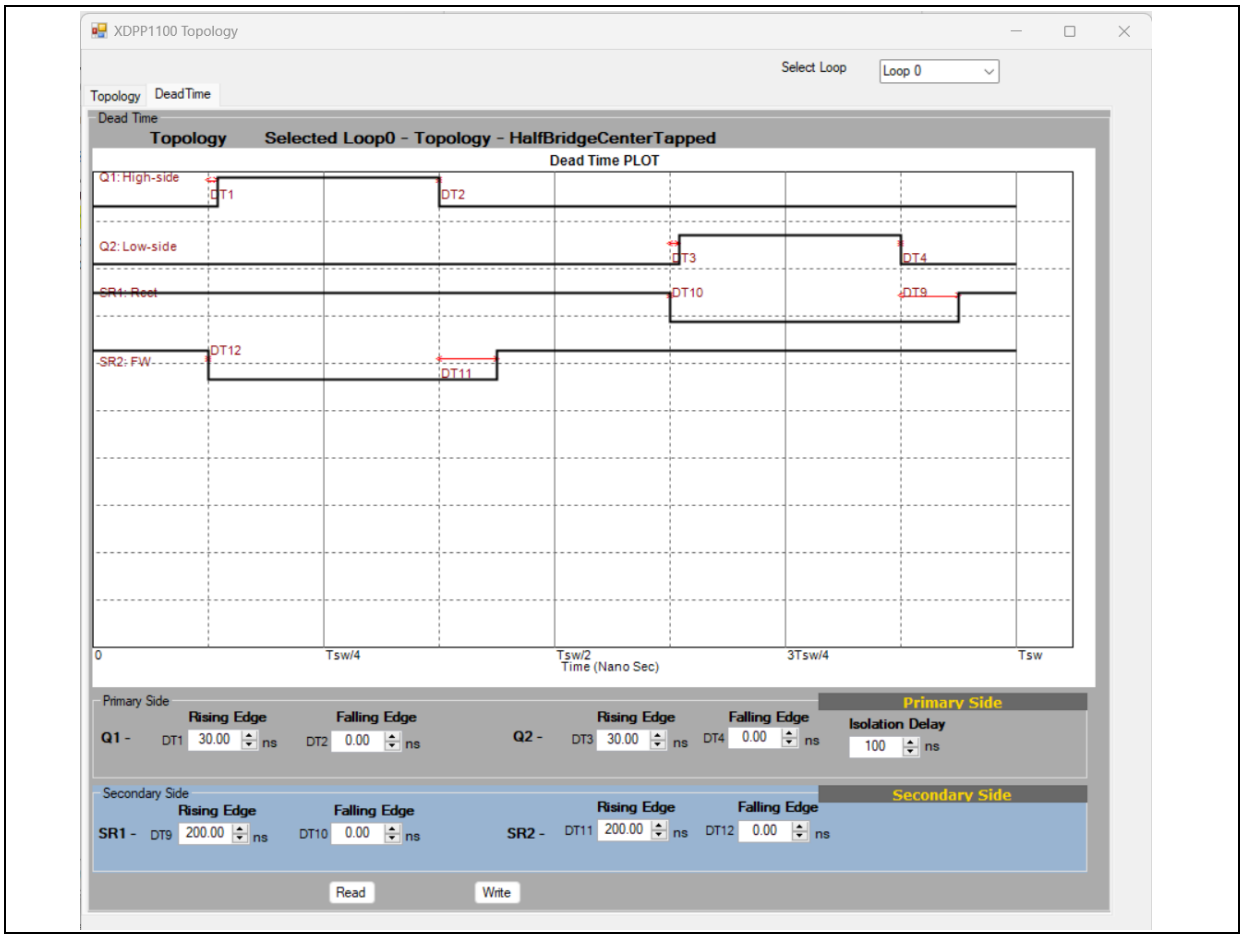



**Figure 20 3LFC dead-time and isolation delay**

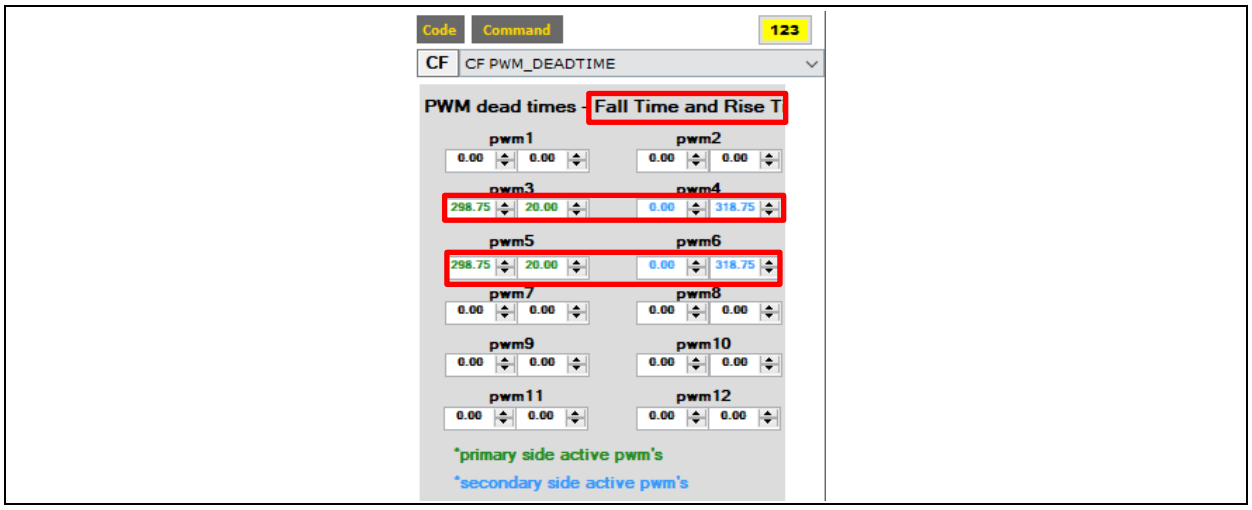



**Figure 21 3LFC dead-time configuration**

- **Loop1 ZSC**: Configure the topology to the half-bridge primary, mapping the PWMs per HW connection shown in the Figure 22.
- **ZSC dead-time configuration:** The ZSC dead-time is not implemented in the command 0xCF PWM_DEADTIME shown in the Figure 23. However, it is implemented by using the MFR command 0xED

which defines the max duty-cycle. In this design, the value of the 0xED (max duty-cycle) is 0xF170 in the PMBus spreadsheet and the max duty-cycle is 92%. The dead-time can be calculated as given in the following equation:

$$dt = \frac{1}{F_{sw}} \times \frac{1-Max\ duty\ cycle}{2} = \frac{1}{630kHz} * \frac{1-0.92}{2} \approx 64ns$$

**Equation 9**

where, the $F_{sw}$ is the ZSC switching frequency, the max duty cycle is 92%.

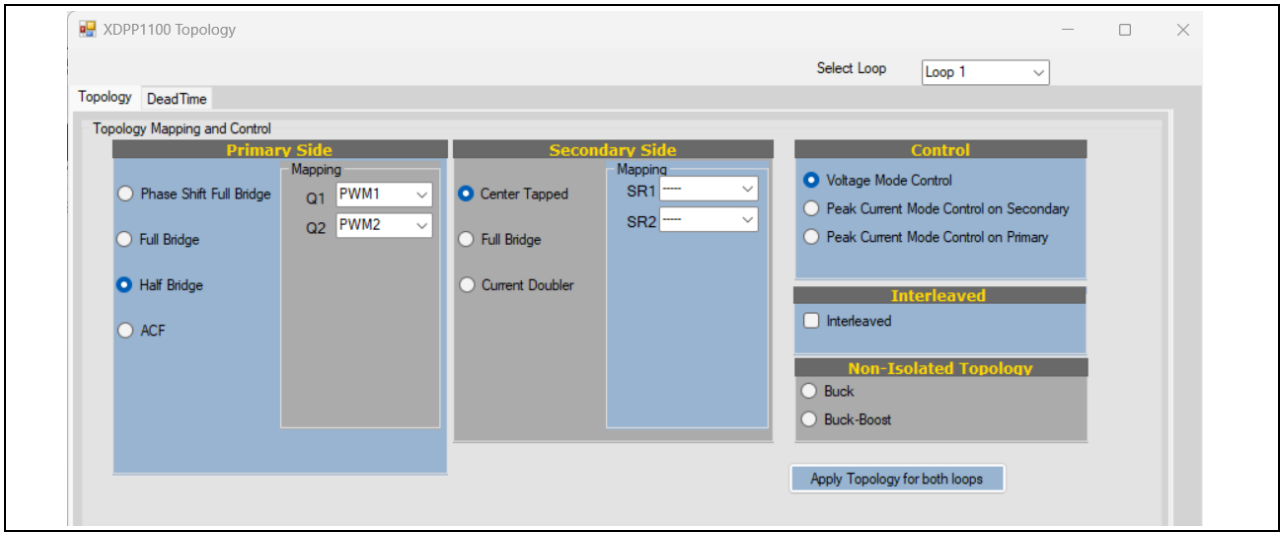



**Figure 22 ZSC topology and PWM mapping**

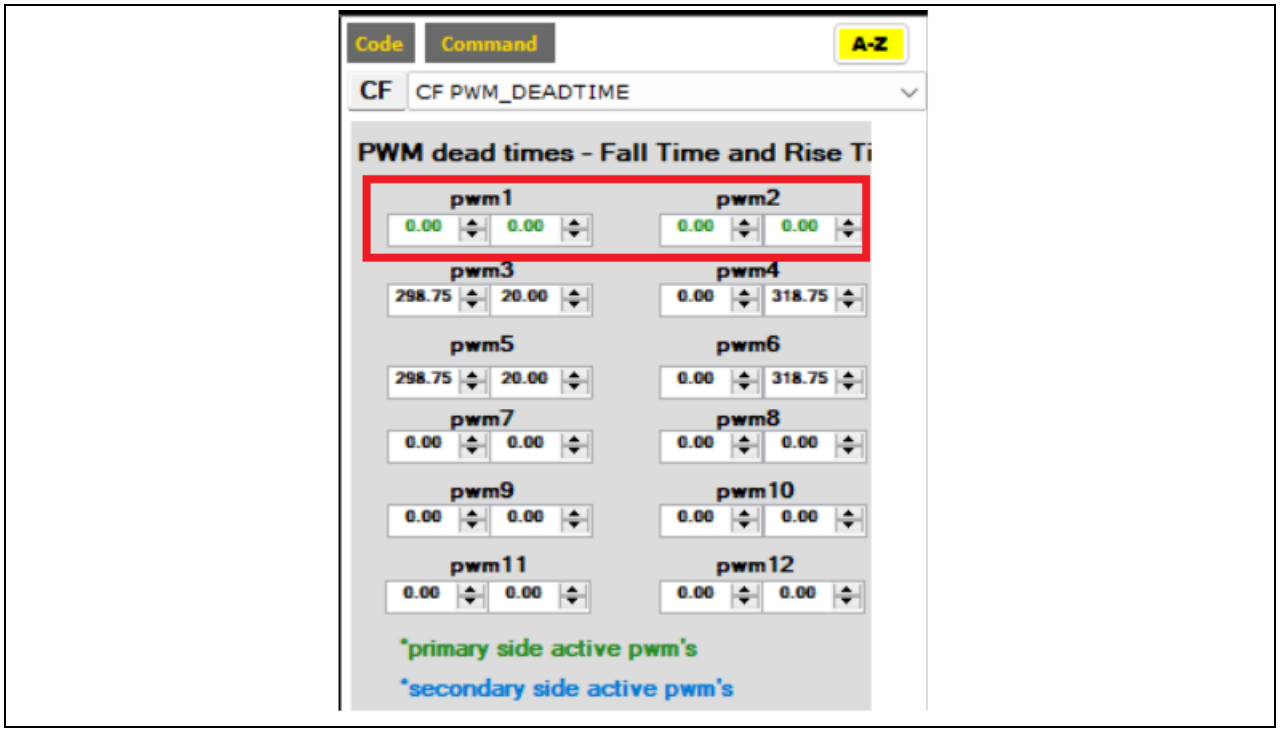



**Figure 23 ZSC dead-time**

## 5.4 PMBus configuration

The key PMBus commands are listed in Table 2 and Table 3.

**Table 2 Basic PMBus configuration for Loop0 (3LFC)**

| Command | Name | Data | Meaning |
|---|---|---|---|
| 00 | PAGE | 0x00 | Page 0 |
| 01 | OPERATION | 0x01 | On |
| 02 | ON_OFF_CONFIG | 0x1F | Respond to operation and EN pin, EN polarity active high |
| 20 | VOUT_MODE | 0x18 | –8 |
| 21 | VOUT_COMMAND | 0x0C00 | 12,000 V |
| 24 | VOUT_MAX | 0x0F00 | 15,000 V |
| 27 | VOUT_TRANSITION_RATE | 0xE810 | 2,000 mV/µs |
| 29 | VOUT_SCALE_LOOP | – | 0.13043 |
| 32 | MAX_DUTY | 0xF190 | 100.00 percent |
| 33 | FREQUENCY_SWITCH | 0x087D | 250 kHz |
| 34 | POWER_MODE | 0x03 | 0x03 |
| 61 | TON_RISE | F050 | 25.000 ms |
| CD | MFR_VRECT_SCALE | – | 0.128906 |
| EA | MFR_IOUT_APC | – | 0.353516 A |

**Table 3 Basic PMBus configuration for Loop1 (ZSC)**

| Command | Name | Data | Meaning |
|---|---|---|---|
| 00 | PAGE | 0x01 | Page 1 |
| 01 | OPERATION | 0x01 | On |
| 02 | ON_OFF_CONFIG | 0x1A | Respond to operation on/off only |
| 20 | VOUT_MODE | 0x18 | –8 |
| 21 | VOUT_COMMAND | 0x1800 | 24,000 V |
| 27 | VOUT_TRANSITION_RATE | 0xE810 | 2,000 mV/µs |
| 32 | MAX_DUTY | 0xF190 | 100.00 percent |
| 33 | FREQUENCY_SWITCH | 0x093B | 630 kHz |
| 34 | POWER_MODE | 0x03 | 0x03 |

## 5.5 Input voltage sense

The XDPP1100 uses PRISEN ADC to sense the input voltage through the resistor-divider R603, R604. The input voltage is calculated based on the sensed PRISEN voltage. The PRISEN input voltage sensing is configured by register vin_pwl_slope and vin_trim shown in Figure 24.

The vin_pwl_slope can be calculated by the following equation:

$$vin\_pwl\_slope = \frac{\Delta Vin \times 1.2 \times 2^5}{\Delta VPRISEN}$$

**Equation 10**

The $\Delta V_{PRISEN}$ /$\Delta V_{IN}$ is the resistor scale of the PRISEN resistor-divider (R603, R604). To utilize the full input voltage range of TS ADC (1.2 V), it is recommended to set the scale of $V_{IN}$ resistor divider by:

$$\frac{1.2V}{Vin\_max}$$

**Equation 11**

For example, for maximum 95 V input the $V_{IN}$ resistor-divider ratio is set to 1.2 V/95 V = 0.0126 V/V. To get this ratio, select R603 = 180 kΩ, R604 = 3.3 kΩ; the actual divider ratio is 0.018003.

$$vin\_pwl\_slope = \frac{1.2 \times 2^5}{0.018003} = 2133$$

**Equation 12**

The vin_trim configures the offset of the input voltage that is sensed by PRISEN.

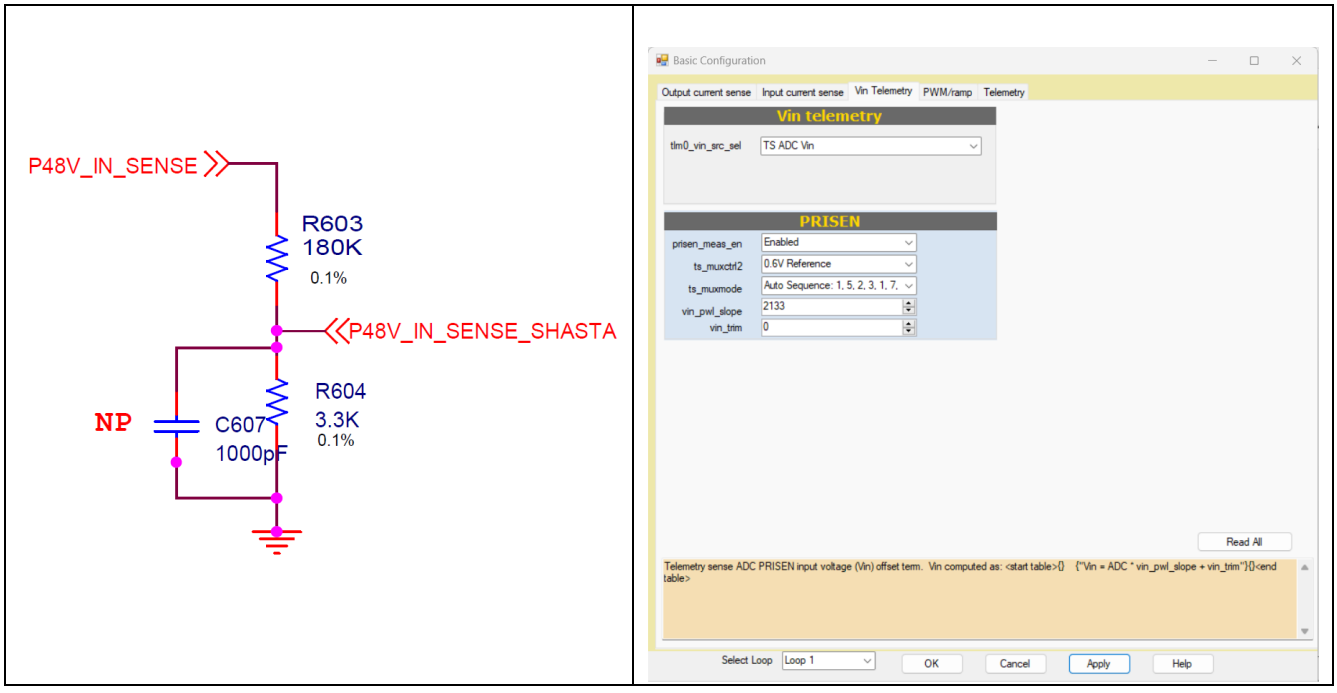



**Figure 24 Input voltage sensing by PRISEN pin**

## 5.6 $V_{mid}$ voltage sense

The XDPP1100 uses VRSEN/VRREF ADC to sense the middle point voltage ($V_{mid}$) through the resistor-divider R605, R606 shown in the Figure 25. The voltage is calculated based on the sensed VRSEN voltage. This is the 3LFC input voltage shown in the Loop0 of the GUI.

When configuring the Loop0, the MFR_VRECT_SCALE must be set to 2× of the resistor divider value, because in half-bridge topology, the FW calculates input of loop0 ($V_{IN\_3LFC}$) based on the following equation:

$$VRSEN * 2 / (MFR\_VRECT\_SCALE * MFR\_TRANSFORMER\_SCALE)$$

**Equation 13**

Setting MFR_VRECT_SCALE to 2× could cancel the factor of 2 in the equation.

The pid_vrect_ref should be set to 12 V /0.32 V = 38

0xCD MFR_VRECT_SCALE in Loop0 is calculated based on $V_{rect}$ resistor-divider R605, R606.

$$MFR\_VRECT\_SCALE = \frac{4.7\ k\Omega}{(68\ k\Omega + 4.7\ k\Omega)} \times 2 = 0.1293$$

**Equation 14**

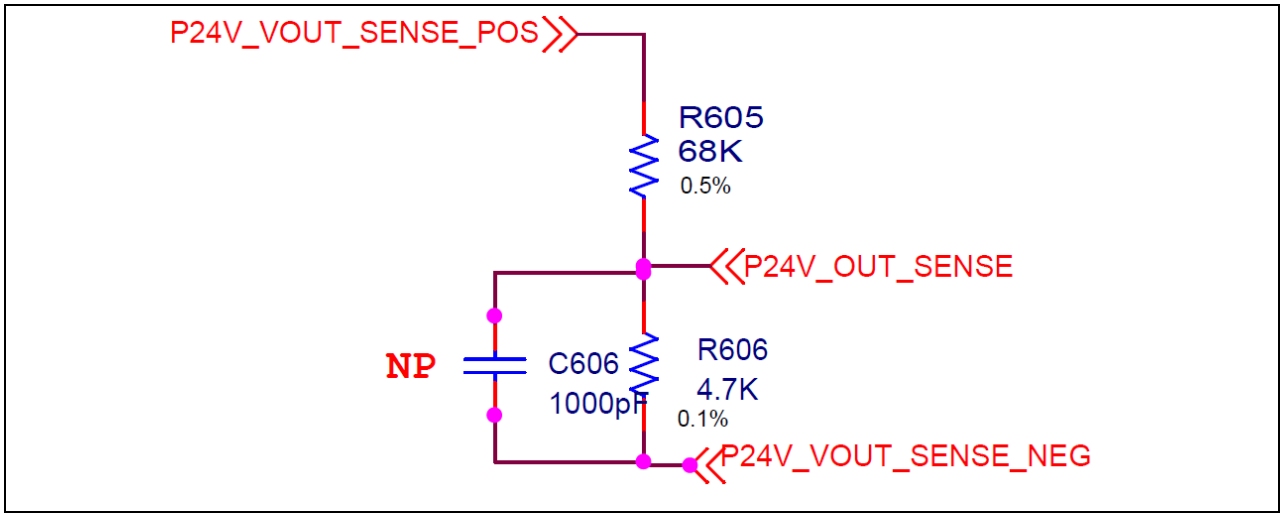



**Figure 25 Vmid voltage sensing circuit**

## 5.7 Output voltage sense

The output voltage is sensed at the VSEN pin through resistor-divider R607, R608 shown in the Figure 26. The set-point of VSEN is recommended to be set equal or higher than 1.2 V for the highest accuracy. This board sets the divider ratio to 0.1304 to get 1.56 V at the VSEN pin. the PMBus Command in Loop0 0x29 VOUT_SCALE_LOOP is 0.1304.

$$VOUT\_SCALE\_LOOP = \frac{R608}{R607+R608} = \frac{1.8K}{12K+1.8K} = 0.1304$$

**Equation 15**

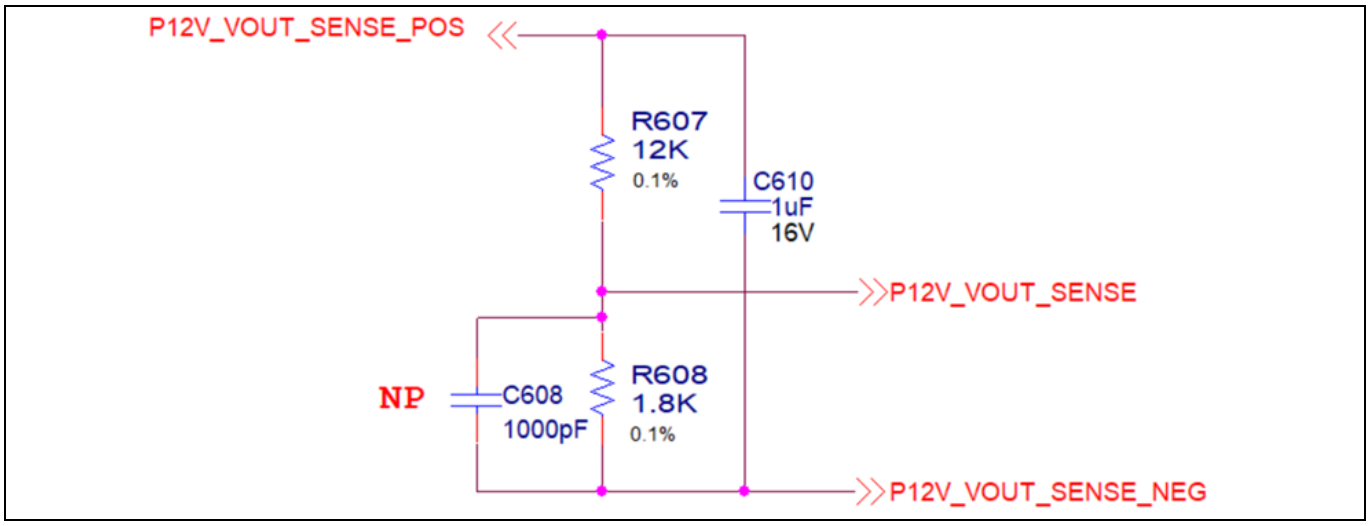



**Figure 26 Output voltage sensing circuit**

## 5.8 Firmware patch

### 5.8.1 Enable signal of the eFuse XDP710

The eFuse enable signal is controlled by pin 22 of XDPP1100, which is mapped to MP_SYNC by default. Therefore, a patch is required to modify this pin functionality, The patch is hard coded to use the MP_SYNC pin to turn on eFuse XDP710 for soft-start (e.g., signal enable for hot-swap controller).

## 5.8.2 Stage diagram

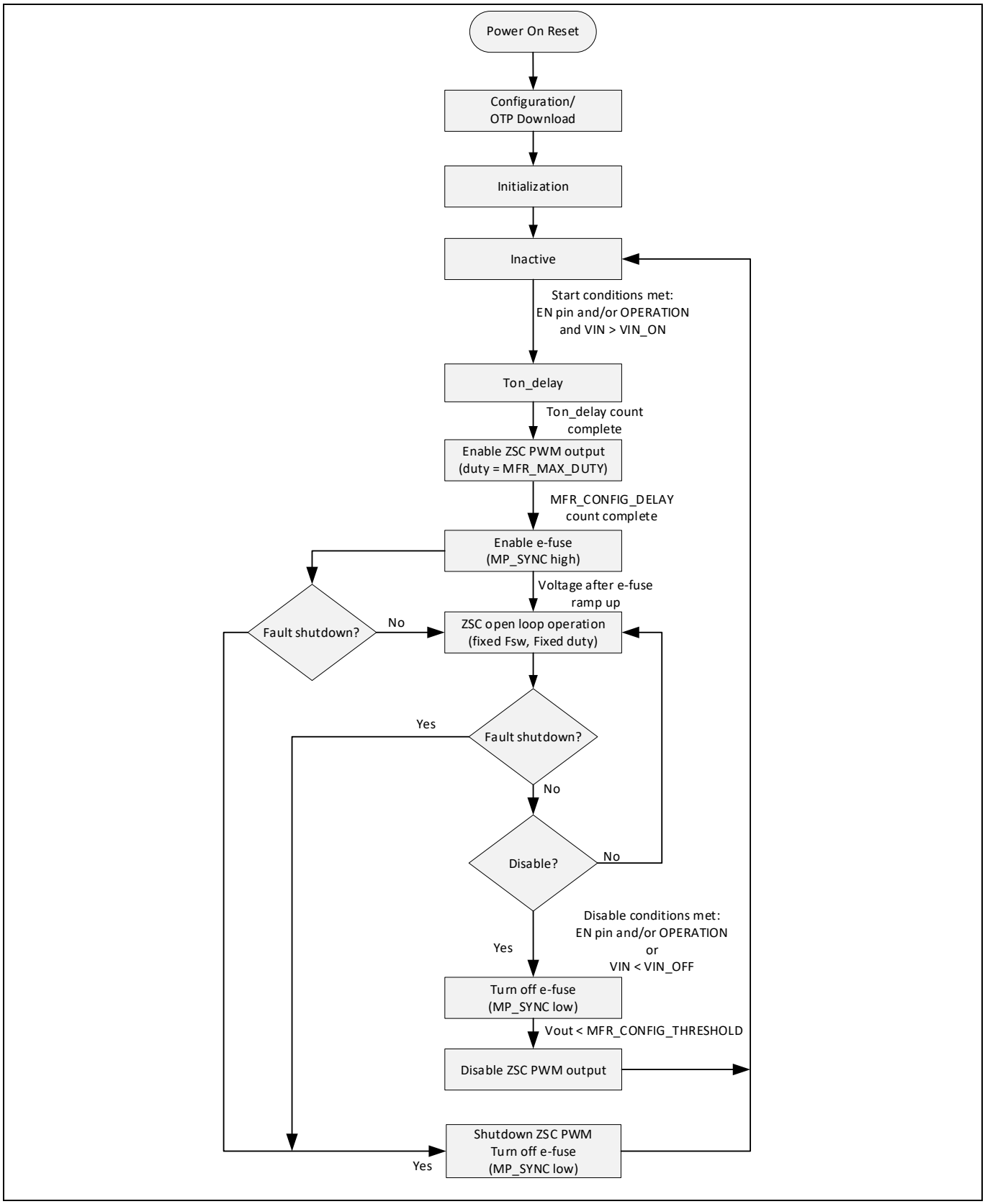



**Figure 27 ZSC (loop1) stage diagram**

Loop0 is enabled by the standard enable logic in ROM code. The VIN_ON threshold of loop0 is set very low to 3 V. The goal is to limit the inrush current in the 3LFC flying capacitor during startup. The VIN_ON threshold should be set as low as possible. However, when the input voltage applies, the Vo1 bus will be pulled up by the leakage current of the gate drivers. To prevent unexpected startup of 3LFC, e.g., without the enable converter, the VIN_ON threshold has to be set higher than the Vo1 voltage in the off state, which is around 2 V.

During shutdown, loop0 (3LFC stage) switches to the forced duty cycle except in a fault shutdown scenario. This is controlled by an FW patch to discharge the Vo1 bus voltage. The FW keeps loop0 PWMs switching and only turn off PWMs when Vout is lower than a threshold defined by MFR_CONFIG_THRESHOLD. See 5.9.4 of the configuration guide for more information.

In a fault shutdown, the PWM of both loop0 3LFC and loop1 ZSC would be pulled down immediately. The eFuse will be disabled except for undervoltage faults where soft shutdown is used.

Loop1 controls the 2:1 ZSC stage. The ZSC converter operates in open loop mode. The patch implements force duty-cycle and enable/disable eFuse functions. At startup, the ZSC stage should start switching before the eFuse XDP710 turns on. Use MFR_CONFIG_DELAY to delay the turn-on of the eFuse (see 5.9.3 for configuration guide).

### 5.8.3 Enable/disable ZSC (loop1) and eFuse

- Config MP_SYNC (EN_EFUSE) as GPIO pin. Set sync_func=1, sync_ppen=1.
- Set ramp1_force_duty (see 5.8.4, ramp1_force_duty_en=1

#### 5.8.3.1 Enable ZSC and eFuse

The following conditions need to be met to enable ZSC and eFuse.

- ON_OFF_CONFIG and the EN, OPERATION enable converter.
- Input voltage is higher than the VIN_ON threshold of loop1. Loop1 tlm1_vin_src_sel = 3, The input voltage is sensed at the PRISEN pin.
- No fault shutdown.

The EN is designed to control both loop0 and loop1 by the patch.

The following sequence must be followed for the enable sequence.

- Enable loop1 PWM output. The loop1 duty-cycle is set by ramp1_force_duty and is configured by MFR_MAX_DUTY.
- After the delay set by MFR_CONFIG_DELAY, enable eFuse by setting MP_SYNC pin high.

#### 5.8.3.2 Disable ZSC and eFuse

The following conditions need to be met for normal disable conditions.

1. ON_OFF_CONFIG and the EN, OPERATION disable converter (loop1)
2. VIN of loop1 is lower than the VIN_OFF threshold.

The following sequence must be followed for the normal disable sequence.

1. Turn off eFuse by setting MP_SYNC of the XDPP1100 pin low.
2. Keep PWM switching of both loop 0 and loop 1 until Vout of loop0 is lower than MFR_CONFIG_THRESHOLD.

The following sequence must be followed for the fault disable sequence at fault shutdown.

- Turn-off eFuse (MP_SYNC low) and shutdown all PWMs immediately.

### 5.8.4 ZSC force duty-cycle control

Set ramp1_force_duty = MFR_MAX_DUTY / (2^-8*100)

The ramp1_force_duty is updated at device power-up when loading the configuration from OTP, or when the MFR_MAX_DUTY command writes.

The ZSC frequency is defined by the FREQUENCY_SWITCH of loop1. It will be updated when FREQUENCY_SWITCH writes.

### 5.8.5 Disable VOUT_UV fault at converter enable.

Loop0 VOUT_UV fault should not trigger during soft start. The VOUT_UV fault is only activated after Vout ramps up and higher than VOUT_UV_WARN_LIMIT.

### 5.8.6 Startup sequence of DR-HSC

The main startup waveform is shown in Figure 28.

For reference, the definition of the waveforms is as follows:

- $V_{in}$: Actual input voltage before eFuse. Sensed with PRISEN ADC.
- $Vin_{\_zsc}$: Input voltage of ZSC and output voltage of eFuse FET.
- $Vout_{zsc}$ or $Vin_{3LFC-DP}$: Output voltage of ZSC which is the input voltage of 3LFC-DP, sensed with VRSEN ADC.
- $V_{out}$ : Output voltage of 3LFC-DP (output voltage of loop0). Sensed by fast ADC VSEN.
- $EN$: Digital enable of converter (connected to MP_EN GPIO[0]).
- $EN_{e-fuse}$ : Digital signal from XDPP1100 MP_SYNC pin to enable eFuse controller XDP710 startup

The following procedure describes the startup sequence.

1. Apply Vin 48 V, no load.
2. The loop1 PWM starts switching at a fixed duty cycle as described in section 5.8.4.
3. After a defined delay $EN_{delay}$ (e.g., set with MFR_CONFIG_DELAY = 0)-enabled eFuse is pulled up and the eFuse controller starts the eFuse startup procedure.
4. When the output voltage of ZSC has reached the VIN_ON threshold 3.0 V of loop0, the second stage 3LFC-DP stars switching.

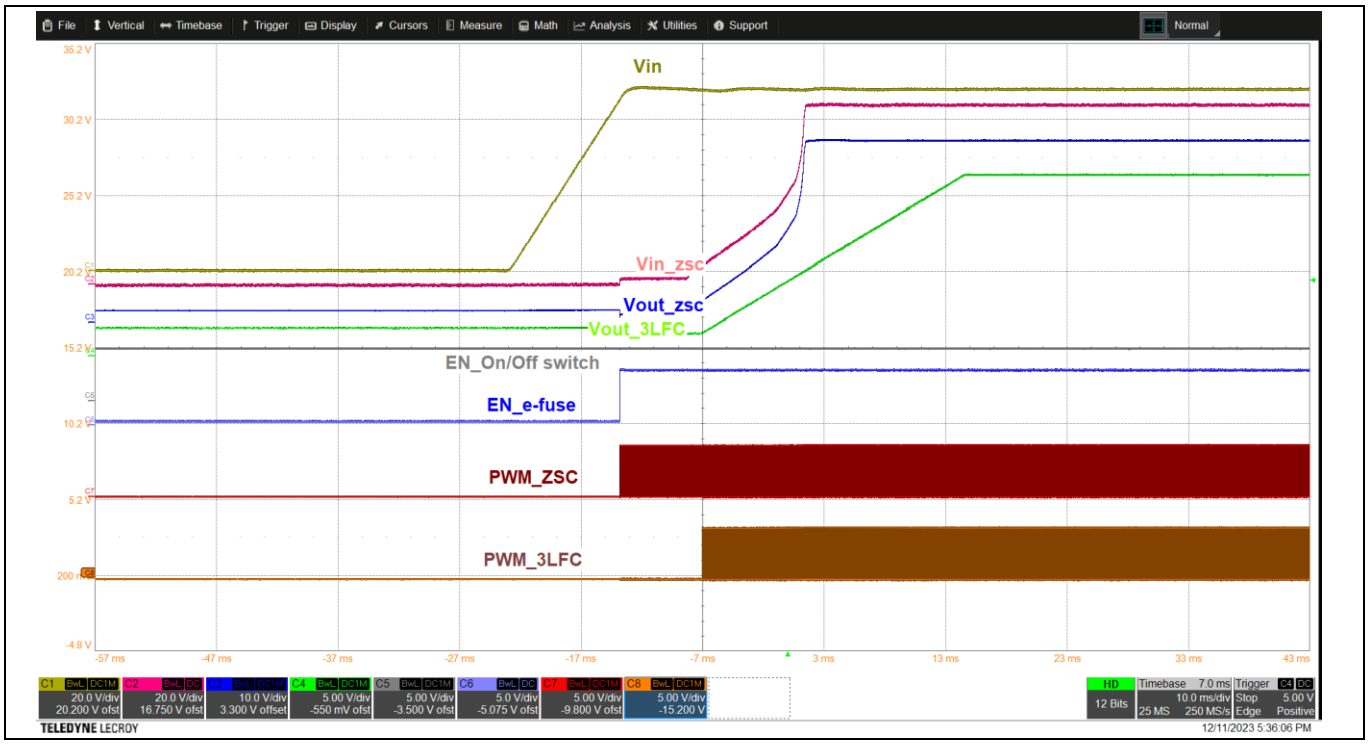



**Figure 28 Startup sequence**

## 5.8.7 Shutdown sequence of DR-HSC

Waveforms references are shown in Figure 29.

The following procedures describe the nominal shutdown sequence.

1. When the Vin voltage is below the VIN_OFF threshold defined by MFR_48V_OFF_THRESH (0xB2), the $EN_{e-fuse}$ signal goes down. The PWM of ZSC keeps switching at fixed duty-cycle as in nominal operation when the PWM of the 3LFC-DP keep switching, modulating the output voltage following shutdown ramp.
2. When the output voltage of loop0 reaches the output voltage off $V_{off}$ defined by the MFR_CONFIG_THRESHOLD(0xE5), both loops stop switching.

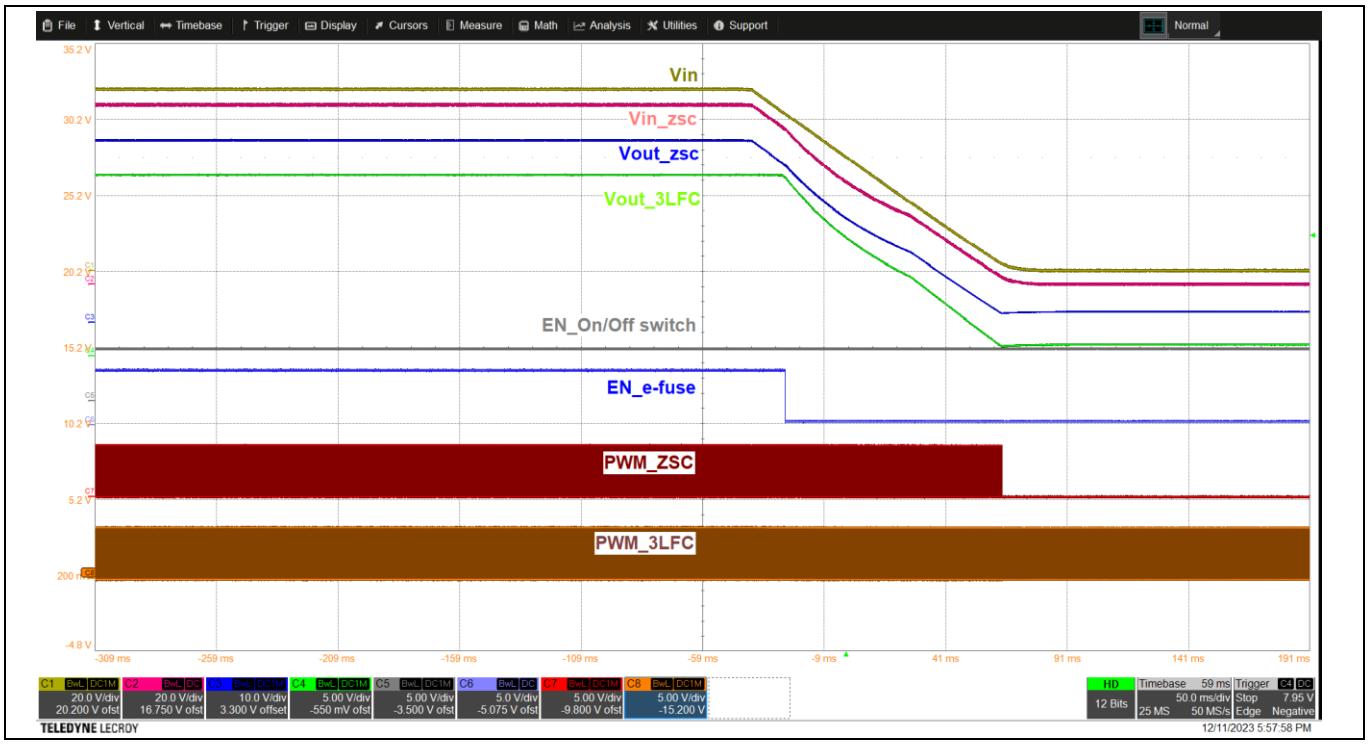



**Figure 29 Shutdown sequence**

## 5.9 MFR commands

### 5.9.1 MFR_48V_ON_THRESH

The MFR_48V_ON_THRESH sets the eFuse turn-on threshold. This command has two data bytes in the LINEAR11 data format.

**Table 4 MFR_48V_ON_THRESH**

| Command code | Command name | Write Tx | Read Tx | Bytes | Format |
|---|---|---|---|---|---|
| B1h | MFR_48V_ON_THRESH | Write word | Read word | 2 | Linear 11 |

Example: MFR_48V_ON_THRESH = 0xF0B0. Sets the turn-on threshold to 44 V.

### 5.9.2 MFR_48V_OFF_THRESH

The MFR_48V_OFF_THRESH sets the E-FUSE turn-off threshold. This command has two data bytes in the LINEAR11 data format.

**Table 5 MFR_48V_OFF_THRESH**

| Command code | Command name | Write Tx | Read Tx | Bytes | Format |
|---|---|---|---|---|---|
| B2h | MFR_48V_OFF_THRESH | Write word | Read word | 2 | Linear 11 |

Example: MFR_48V_ON_THRESH = 0xF0A8. Sets the turn-off threshold to 42 V.

### 5.9.3 MFR_CONFIG_DELAY

The MFR_CONFIG_DELAY command sets the E-FUSE turn-on delay. This command has two data bytes in the LINEAR11 data format. eFuse turn-on delay = MFR_CONFIG_DELAY * 10 µs + 20 µs.

**Table 6 MFR_CONFIG_DELAY**

| Command code | Command name | Write Tx | Read Tx | Bytes | Format |
|---|---|---|---|---|---|
| E8h | MFR_CONFIG_DELAY | Write word | Read word | 2 | Linear 11 |

Example: MFR_CONFIG_DELAY = $0xF805_H = 2.5_D$, the eFuse turn-on delay is 45 µs.

### 5.9.4 MFR_CONFIG_THRESHOLD

The MFR_CONFIG_THRESHOLD sets the ZSC PWM shutdown threshold in normal shutdown.

**Table 7 MFR_CONFIG_THRESHOLD**

| Command code | Command name | Write Tx | Read Tx | Bytes | Format |
|---|---|---|---|---|---|
| E5h | MFR_CONFIG_THRESHOLD | Write word | Read word | 2 | Linear11, Unit V |

Example: MFR_CONFIG_THRESHOLD = $0xA333_H = 0.2_D$, will set the shutdown threshold to 0.2 V. The shutdown occurs at VOUT = 0.2 V.

### 5.9.5 MFR_MAX_DUTY

The MFR_MAX_DUTY defines the max duty-cycle of the ZSC. This command has two data bytes in the LINEAR11 data format.

**Table 8 MFR_MAX_DUTY**

| Command code | Command name | Write Tx | Read Tx | Bytes | Format |
|---|---|---|---|---|---|
| EDh | MFR_MAX_DUTY | Write word | Read word | 2 | Linear 11 |

Example: MFR _MAX_DUTY = 0xF170, set the ZSC PWM maximum duty-cycle to 92%.

# 6 Regulation and telemetry

## 6.1 Line and load regulation

Line and load regulation was tested at 44 V, 48 V, and 60 V input at 0 A, 10 A, 20 A, 30 A, 40 A, and 50 A load.

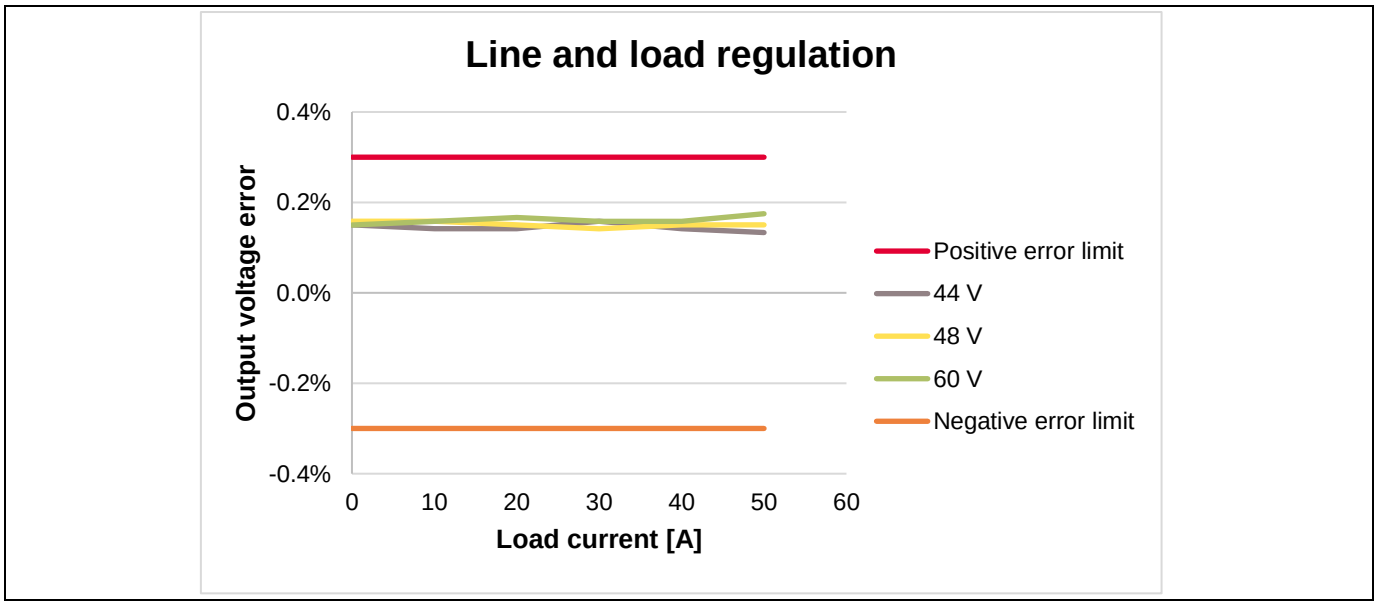



**Figure 30 Line and load regulation**

## 6.2 Input voltage telemetry

The input voltage is sensed before the eFuse. The input voltage telemetry accuracy was tested at no load, half load, and full load.

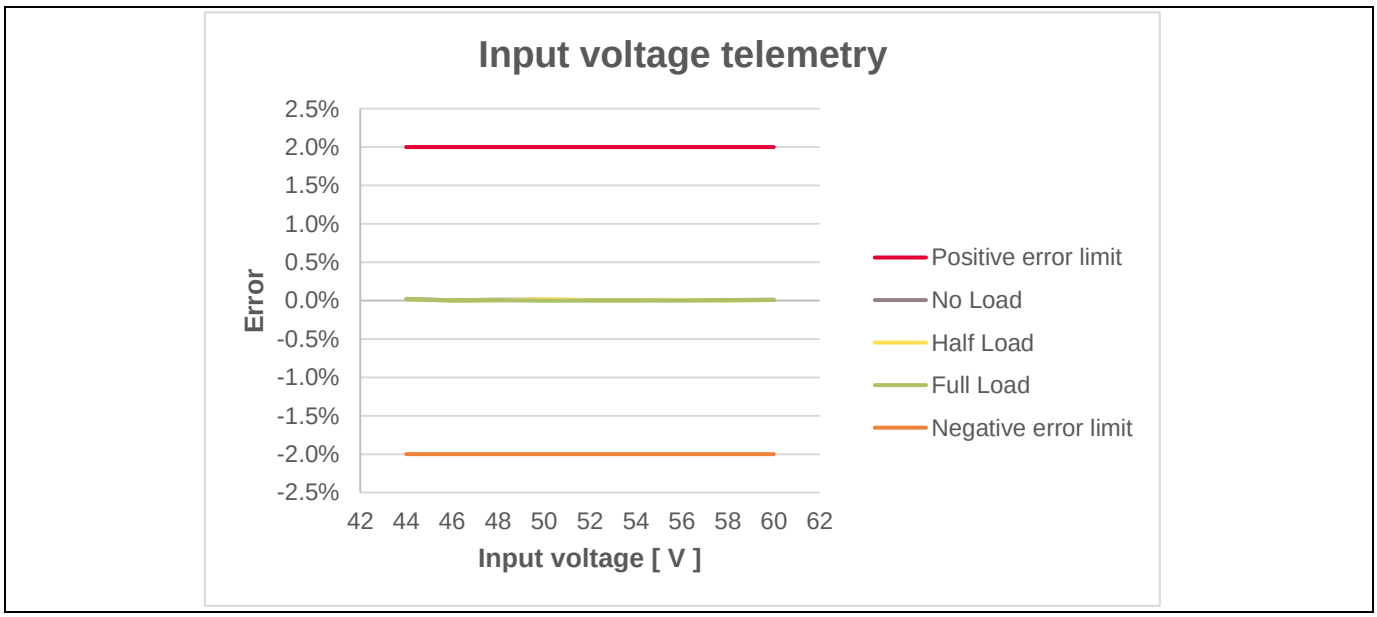



**Figure 31 Input voltage telemetry reading accuracy**

## 6.3 Output voltage telemetry

The output voltage telemetry was measured at 44 V, 48 V, and 60 V input at 0 A, 10 A, 20 A, 30 A, 40 A, and 50A load.

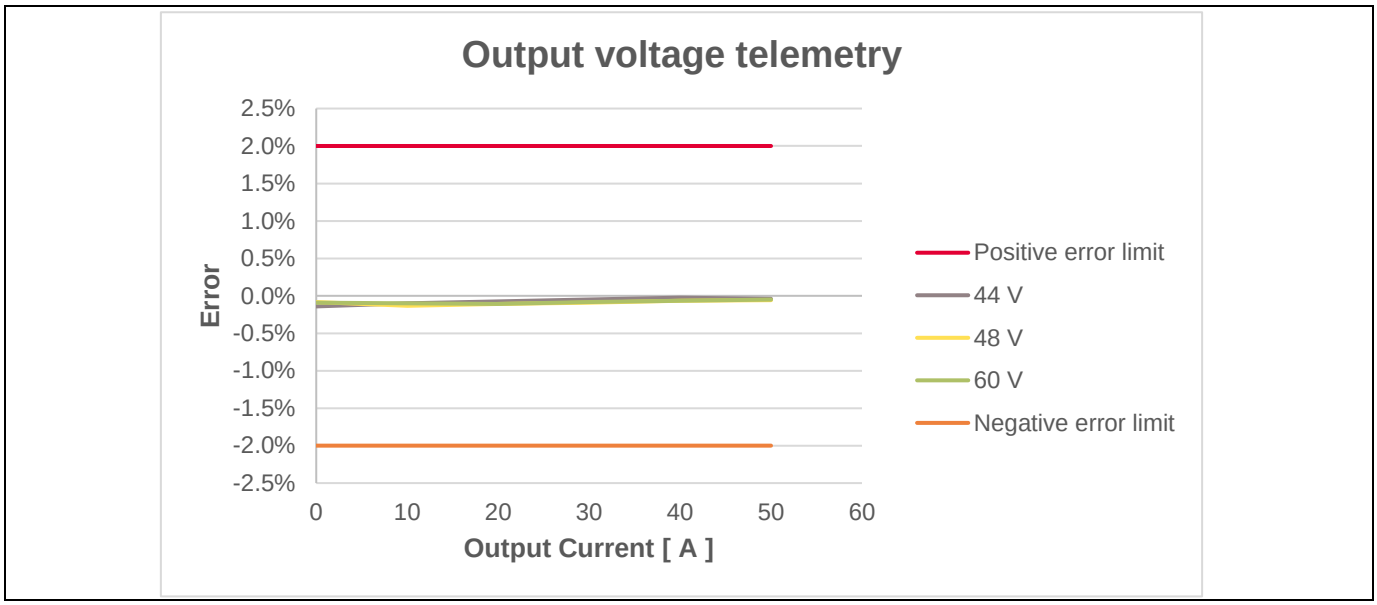



**Figure 32 Output voltage telemetry reading accuracy**

## 6.4 Output current telemetry

The output current is sensed through the DCR of the output inductor L2. Fine-tuning of the RC parameters across the inductor is needed to get accurate current sensing. At no load or light load, there is reverse current present through the inductor in a buck-derived topology. In this case, an op-amp with bidirectional sensing capability is recommended, otherwise the light load current telemetry cannot be sensed accurately. The DCR of the inductor has a positive temperature coefficient, which means resistance increases as temperature rises, so temperature compensation should be considered to achieve accurate output current sensing, which can be implemented easily with XDPP1100.

The output current telemetry was tested at 44 V, 48 V, and 60 V input. The IOUT_CAL_OFFSET is set to 9.5 A.

From the test results shown in the Figure 33, the current sensing is not accurate at light load. To improve the sensing accuracy at light load, change the op-amp U46 from ADM4073T to LMP8481 and connect 1.2 VDD of XDPP1100 to the REF pin of the LMP8481. With this change, the reverse current is sensed correctly.

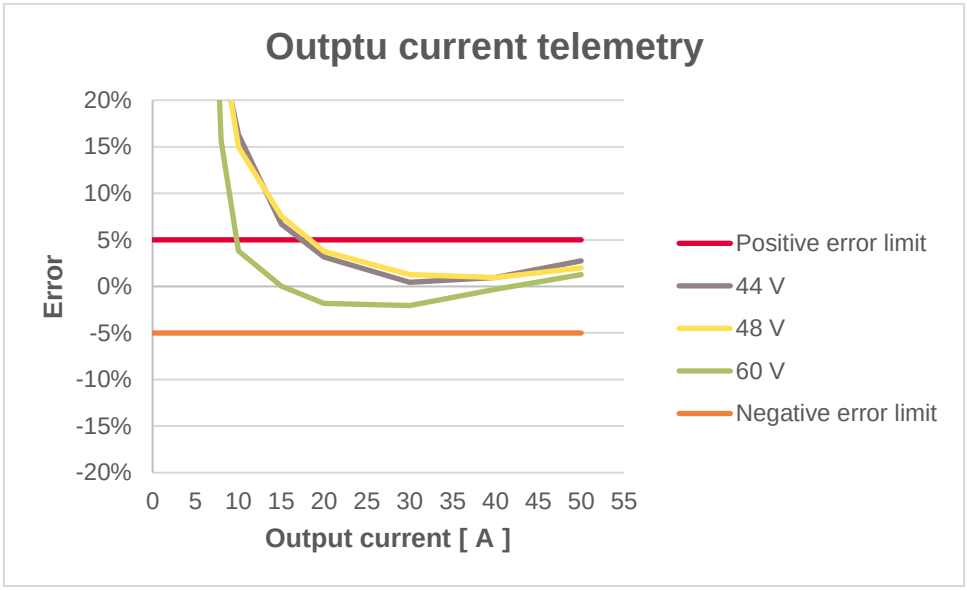



**Figure 33 Output current telemetry reading accuracy**

# 7 System performance

## 7.1 Main operation waveform

The DR-HSC board consists of an unregulated and a regulated stage.

The unregulated ZSC stage switches at around 630 kHz with 50% duty-cycle and a fixed dead-time. Since it is a soft switching topology, the main losses come from MOSFET conduction losses, PCB conduction losses, and gate driving losses.

The regulated stage compared to the ZSC stage is a hard switching topology operating at a low switching frequency of 250 kHz. One major advantage of the topology is that the inductor is facing twice the switching frequency ($f_{sw}$) and only half of the input voltage ($V_{mid}$). This allows to use a very small inductor value, without increasing the current ripple and core losses in the inductor. Another benefit is that if $V_{mid}/2$ is exactly Vout, the inductor sees no ripple current and therefore has very low core losses. That means the most efficient operation point for the converter is when $V_{in}$ = 48 V, $V_{mid}$ = 24 V, and $V_{out}$ = 12 V. Overall, the solution can achieve high power density and high efficiency, and is very flexible in how a design can be implemented.

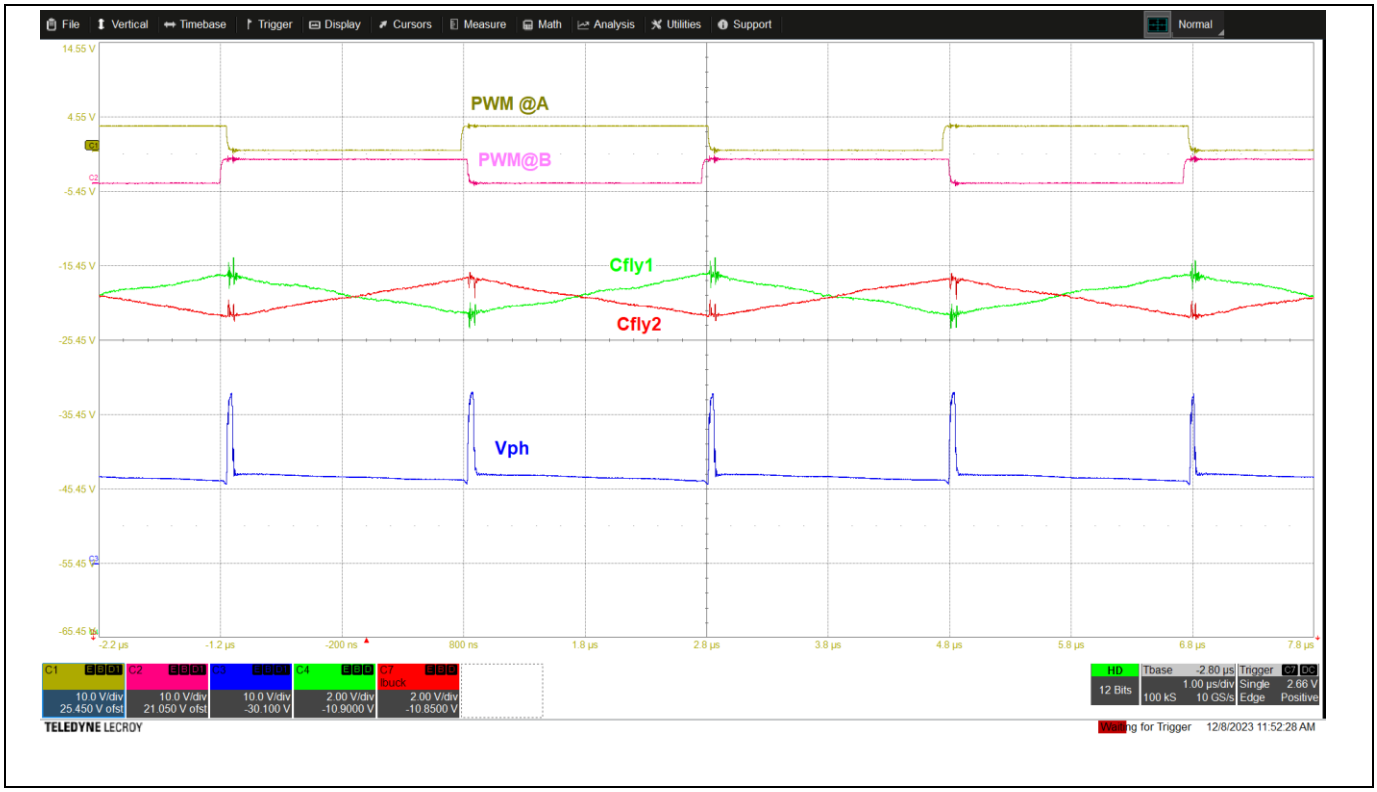
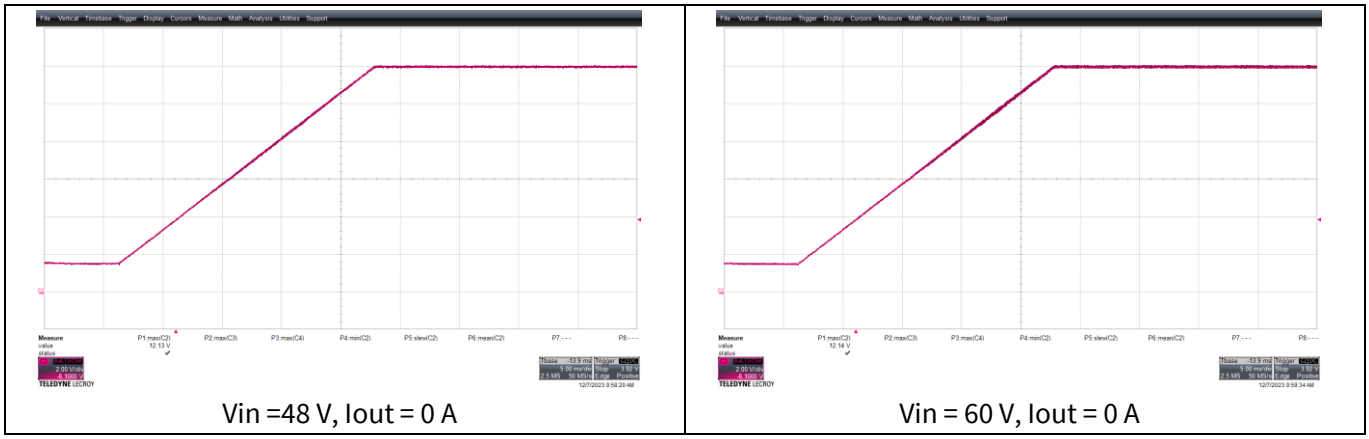



**Figure 34 3LFC-DP, basic operation waveforms showing the phase node voltage and the ripple voltage on $C_{fly1}$ and $C_{fly2}$ and according to PWM signals at $V_{in}$ = 48 V @$I_{out}$ = 40 A.**

## 7.2 Startup and shutdown

In Figure 35, startup main waveforms of the regulated 48 V to 12 V DR-HSC converter, at Vin = 48 V and 60 V, Iout = 0 A are shown.



Vin =48 V, Iout = 0 A | Vin = 60 V, Iout = 0 A

**Figure 35 Startup behavior**

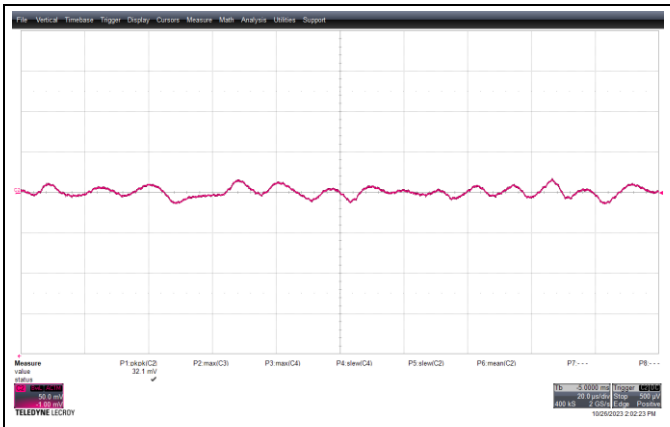
The shutdown main waveforms, from Vin 48 V, are shown in the following figure. When the VIN goes below $Vin_{min}$ ,the eFuse is turned off and the ZSC and 3LFC-DP are keep switching till Vout goes below $V_{off\_th}$ = 2 V. To make sure that $V_{mid}$ capacitors and ZSC capacitors are completely discharged to zero, the ZSC stage keeps switching after the shutdown.


**Figure 36 Shutdown behavior at Vin = 48 V, Iout = 0 A**

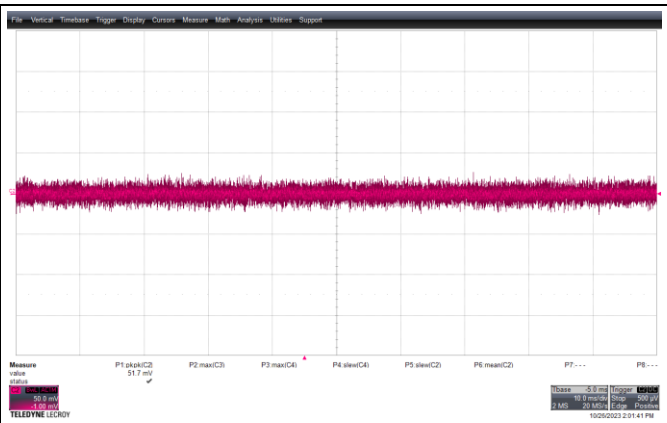
## 7.3 Output ripple and noise

The voltage ripple in steady state is less than 130 mV at different input and output current.

- **$C_{out}$** = 14 x GRM31CD71H106KE11 22 µF ceramic + 2 x EEE-FK1C221V 220 µF electrolytic
- **Vin** = 48 V, **Iout** = 0 A



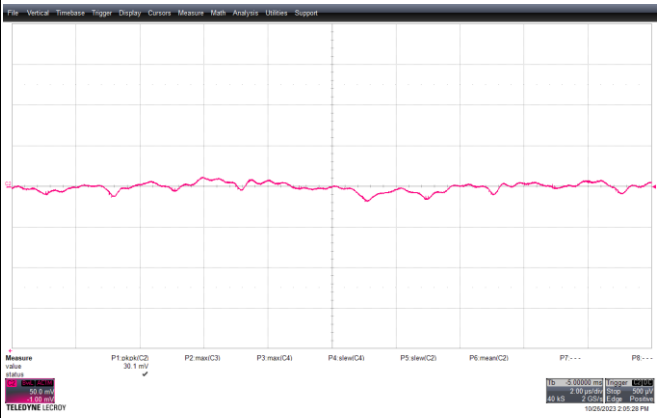
Vin = 48 V, Iout = 0 A,
Ripple = 32.1 mV, time base = 20 µs/div



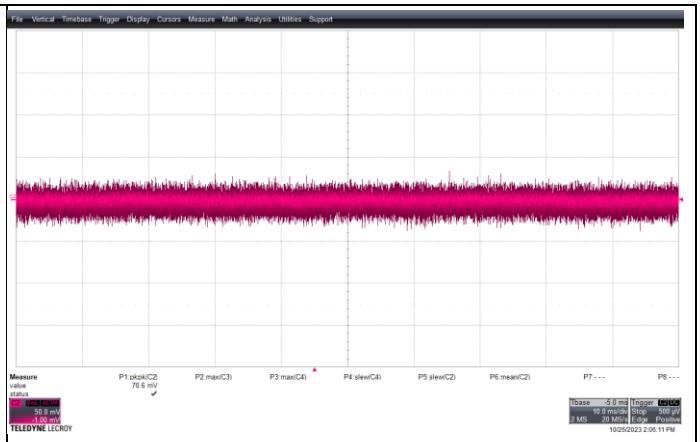
Vin = 48 V, Iout = 0 A,
Ripple = 51.7 mV, time base = 10 ms/div

**Figure 37 Output ripple at Vin =48 V, Iout = 0 A**

- **Vin** = 48 V, **Iout** = 50 A



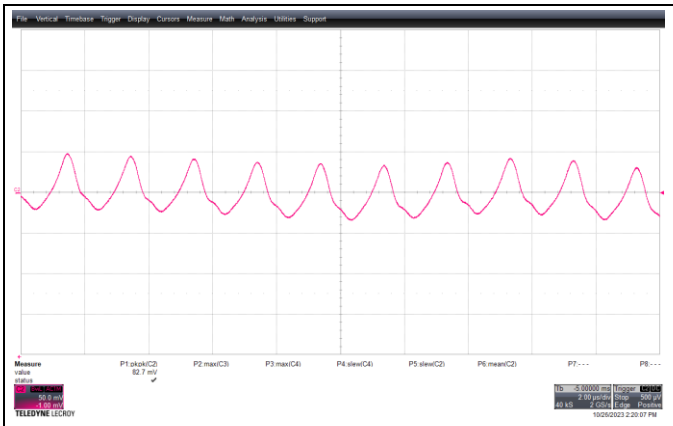
Vin =48 V, Iout = 50 A,
ripple = 30.1 mV, time base = 2 µs/div



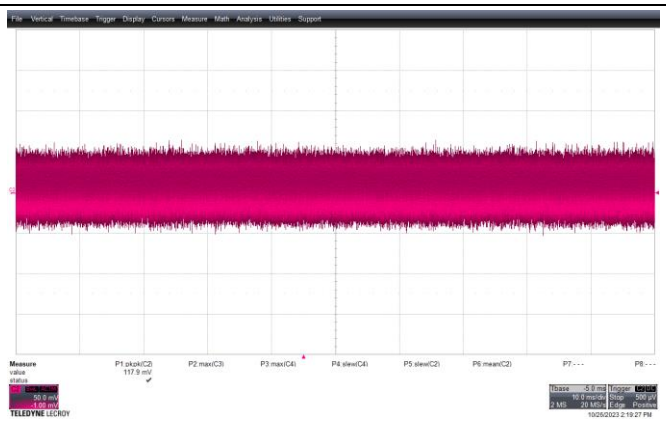
Vin =48 V, Iout = 50 A,
ripple = 70.6 mV, time base = 10 ms/div

**Figure 38 Output ripple at Vin = 48 V, Iout = 50 A**

- **Vin** = 60 V, **Iout** = 0 A



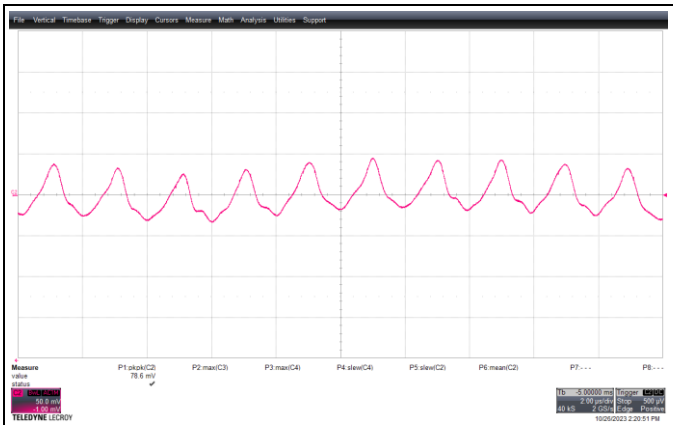
Vin = 60 V, Iout = 0 Ac,
ripple = 82.7 mV, time base = 2 µs/div



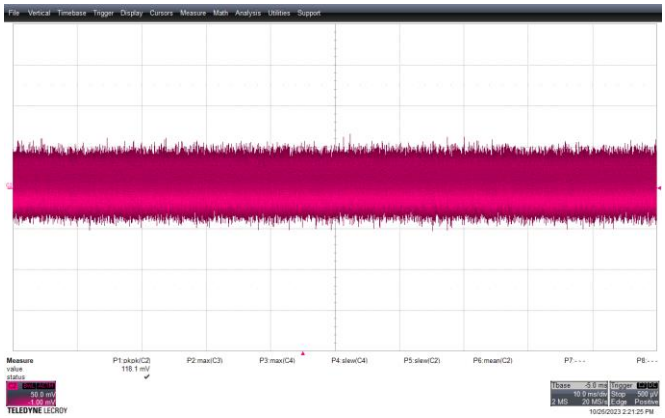
Vin = 60 V, Iout = 0 A,
Ripple = 117.9 mV, time base = 10 ms/div

**Figure 39 Output ripple at Vin = 60 V, Iout = 0 A**

- **Vin** = 60 V, **Iout** = 50 A



Vin = 60 V, Iout = 50 A
Ripple = 78.6 mV, time base = 2 µs/div



Vin = 60 V, Iout = 50 A
ripple = 118.1 mV, time base = 10 ms/div

**Figure 40 Output ripple at Vin = 60 V, 50 A**

## 7.4 Load transients

The E-load transition rate is set to 1 A/µs.

- **Vin** = 48 V
- **CH2**: 12 V output, **CH4**: output current
- Transient done from 0 A to 2 5A, the min voltage is 11.549 V, the max voltage is 12.274 V
- Transient done from 25 A to 50 A, the min voltage is 11.688 V, the max voltage is 12.308 V
- Transient done from 5 A to 45 A, the min voltage is 11.641 V, the max voltage is 12.336 V
- Transient done from 0 A to 50 A, the min voltage is 11.561 V, the max voltage is 12.343 V

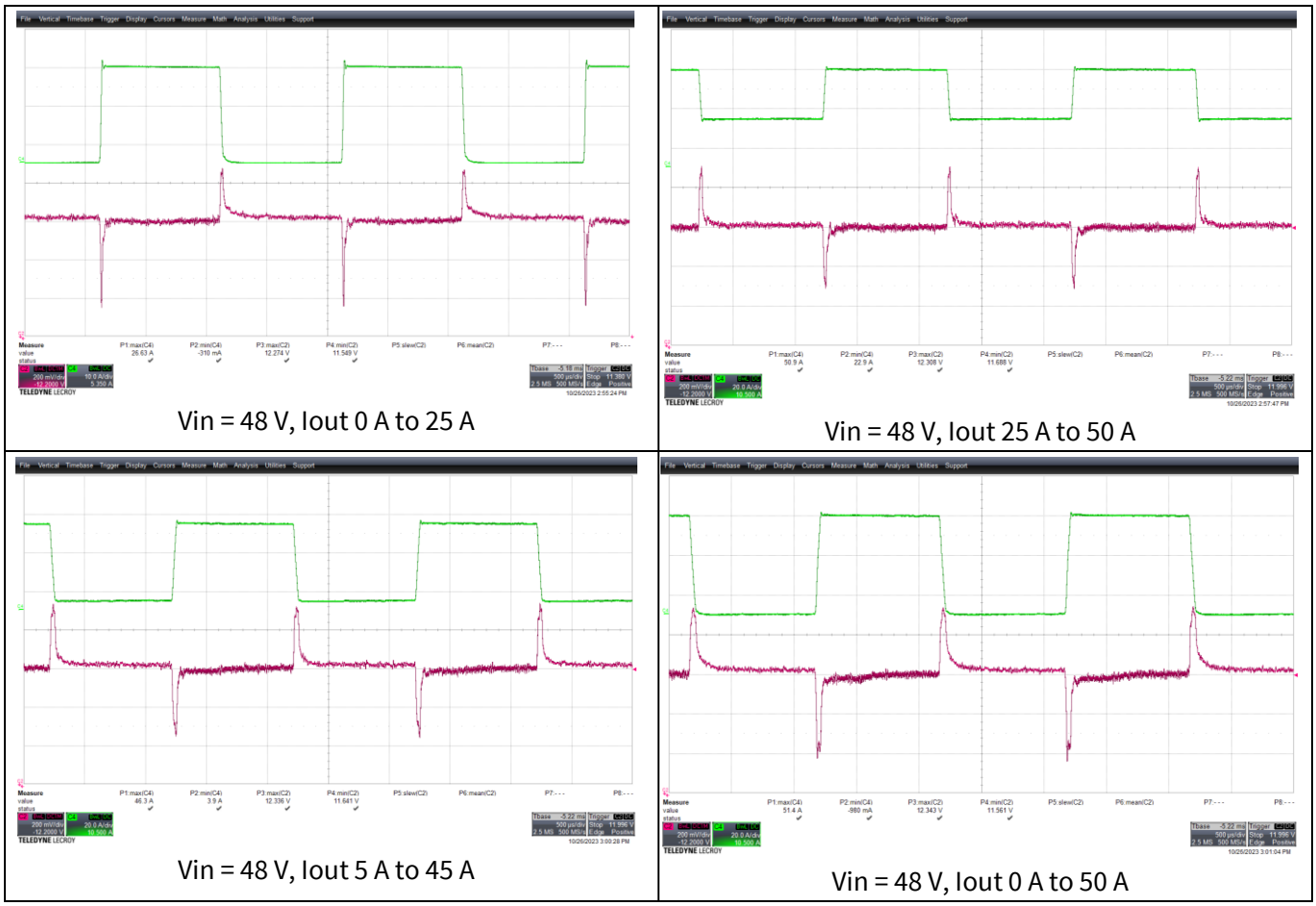
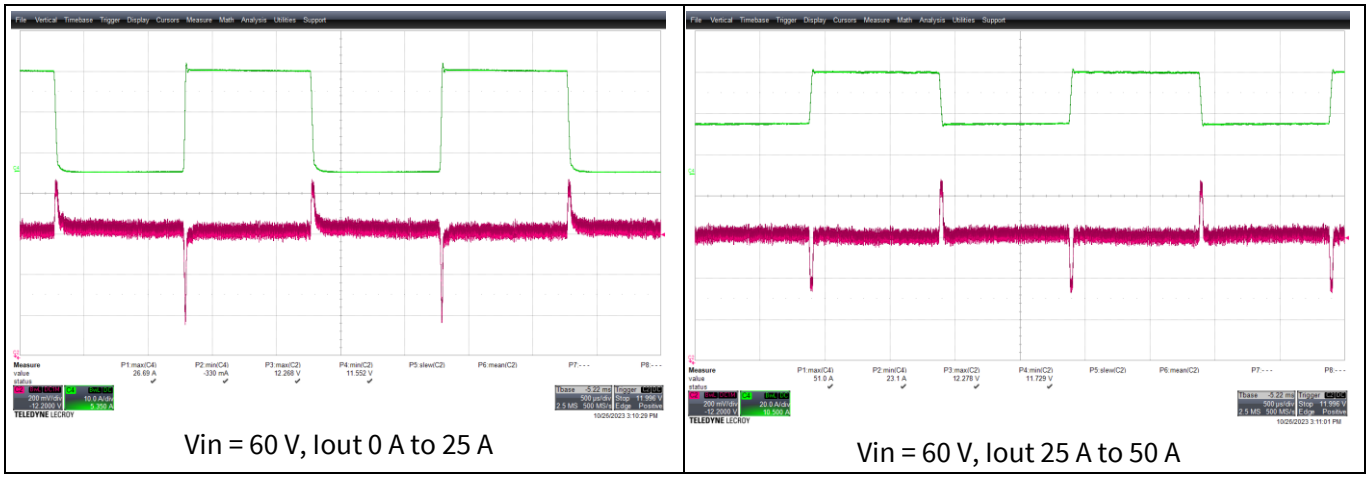



**Figure 41 Load transient at Vin = 48 V**

- **Vin** = 60 V
- **CH2**: 12 V output, **CH4**: Output current
- Transient done from 0 A to 25 A, the min voltage is 11.552 V, the max voltage is 12.268 V
- Transient done from 25 A to 50 A, the min voltage is 11.729 V, the max voltage is 12.278 V
- Transient done from 5 A to 45 A, the min voltage is 11.700 V, the max voltage is 12.285 V
- Transient done from 0 A to 50 A, the min voltage is 11.563 V, the max voltage is 12.292 V



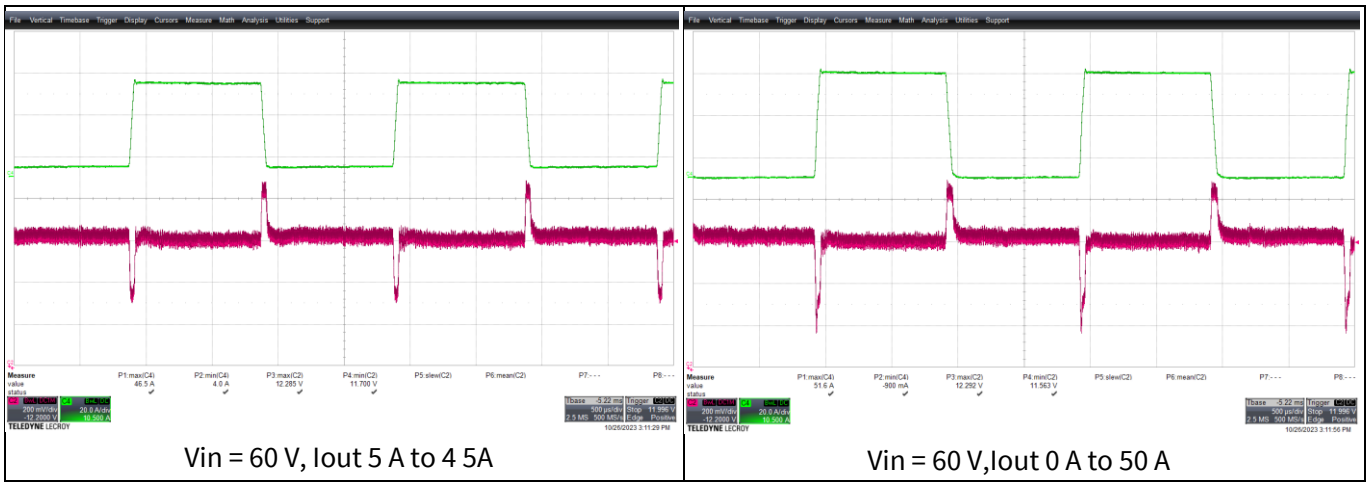



**Figure 42 Load transient at Vin = 60 V**

## 7.5 Measured efficiency

In Figure 43, the efficiency is tested at Vin = 44 V, 48 V, 54 V, and 60 V. The measured efficiency over different Vin voltages including AUX supply losses (PoL6.5 V and 3.3 V, controller IC, driver IC). Hot swap switch conduction losses are not included in the graph.

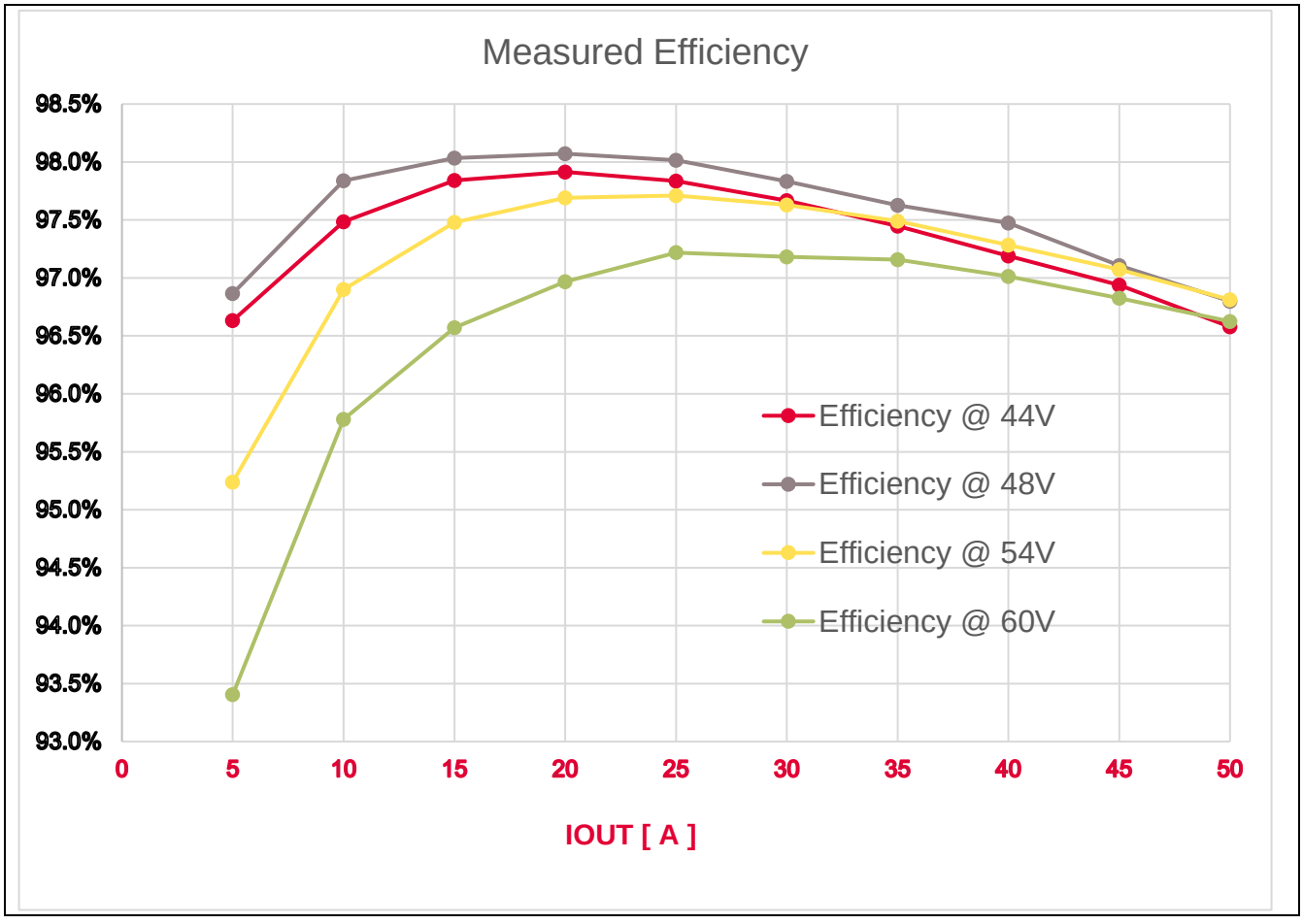



**Figure 43 Measured efficiency**

## 7.6 Thermal image

The thermal image was taken at Vin = 48 V, Iout = 50 A, the ambient temperature = 25°C with the fan cooling (airflow ~ = 100 CFM). The hot spot is 76°C, the 3LFC MOSFETs Q5, Q9 are hot spots.

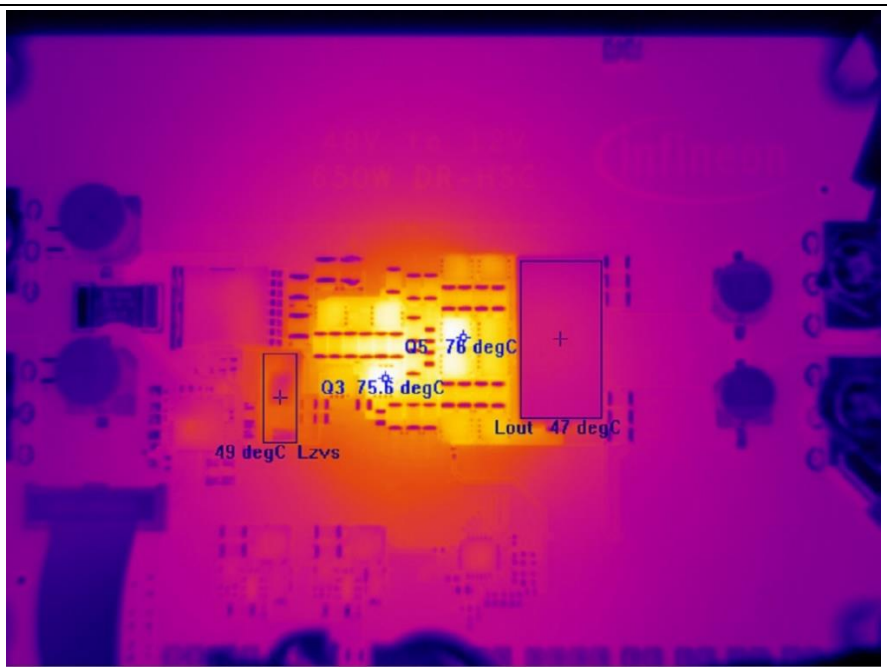



**Figure 44 Thermal performance**

# 8 Protections

In this section, the input and output fault protections are verified. The default fault thresholds and fault response of the board are listed in the following table.

**Table 9 Default fault protection configuration**

| Protection type | | Default value (PMBus configurable) | Unit |
|---|---|---|---|
| Output overvoltage Loop0 | Fault limit threshold | 14 | V |
| | Warn limit threshold | 13.5 | V |
| | Fault response | Disable and retry, no retry | – |
| Output undervoltage Loop0 | Fault limit threshold | 0 | V |
| | Warn limit threshold | 0 | V |
| | Fault response | Ignore fault | – |
| Output overcurrent Loop0 | Fault limit threshold | 60 | A |
| | Warn limit threshold | 58 | A |
| | Fault response | Shutdown and retry | – |
| Output undercurrent Loop0 | Fault limit threshold | –128 | A |
| | Fault response | Continues to operate (Constant-current) | – |
| Overtemperature Loop0 | Fault limit threshold | 125 | °C |
| | Warn limit threshold | 90 | °C |
| | Fault response | Disable and retry | – |
| Undertemperature Loop0 | Fault limit threshold | –42 | °C |
| | Warn limit threshold | –40 | °C |
| | Fault response | Ignore fault | – |
| Output overcurrent fast fault or short circuit (Loop0) | Fault limit threshold | 80 | A |
| | Fault response | Shut down and no retry | – |
| Input overvoltage Loop1 | Fault limit threshold | 66 | V |
| | Warn limit threshold | 65 | V |
| | Fault response | Ignore fault | – |
| Input undervoltage Loop1 | Fault limit threshold | 2 | V |
| | Warn limit threshold | 2.5 | V |
| | Fault response | Ignore fault | – |

The fault threshold and response can be configured by the design tool **Fault Protections**. XDPP1100 also allows the user to configure the sensitivity of the fault detection. The **Fault Configuration** tab configures the fault registers that define the consecutive fault count and the hysteresis of the fault comparator. For more information about the faults and protections can be found in the XDPP1100 application note.

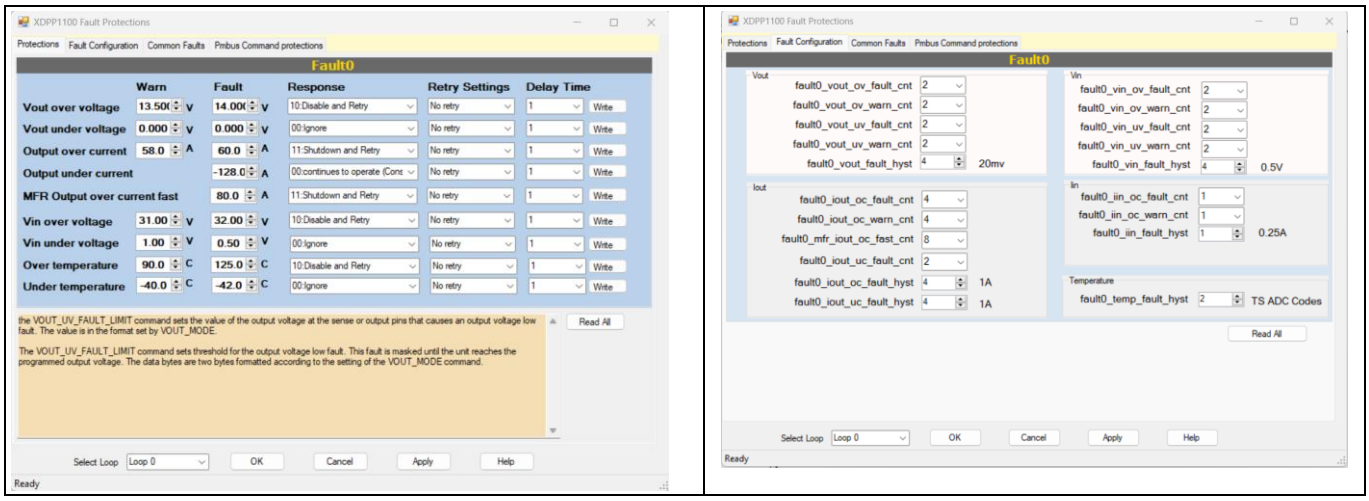



**Figure 45 Fault protections design tool**

## 8.1 Output OVP

Tested at Vin = 60 V, Iout = 0 A, the OVP is 14.03 V.

**Ch1**: 12 V output

**Ch2**: Input voltage

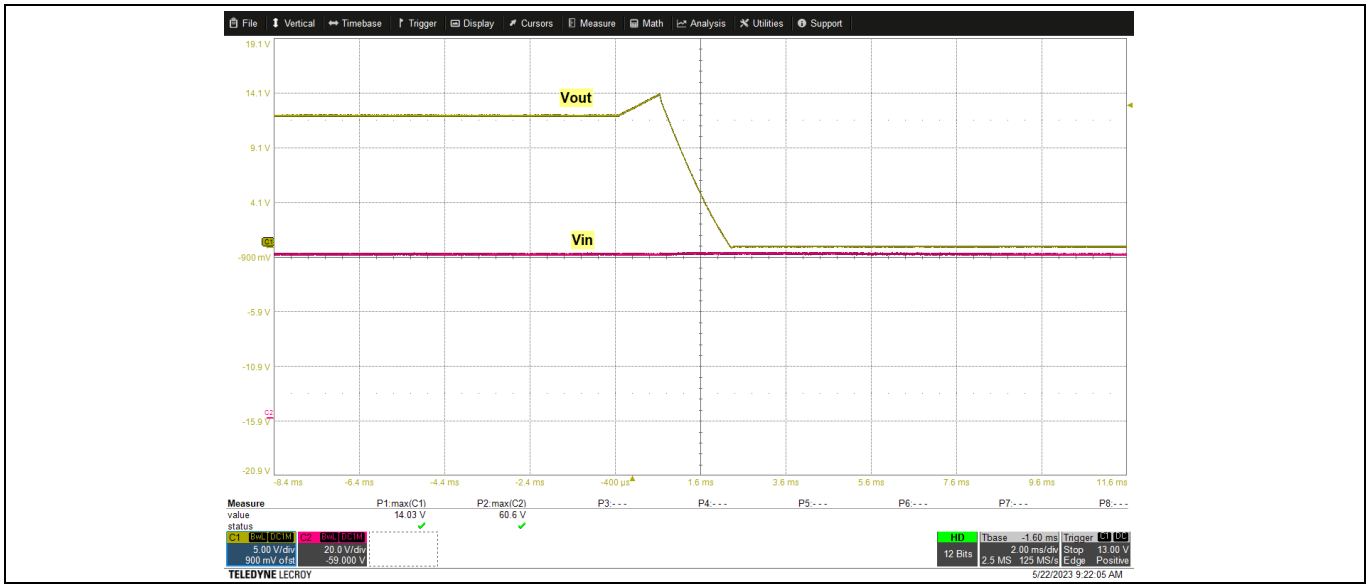



**Figure 46 Output OVP waveform at Vin = 60 V, Iout = 0 A**

## 8.2 Output OCP

Tested at Vin = 48 V, Iout = 50 A

**Ch2**: 12 V output voltage

**Ch3**: output current

**Ch4**: 3LFC PWM

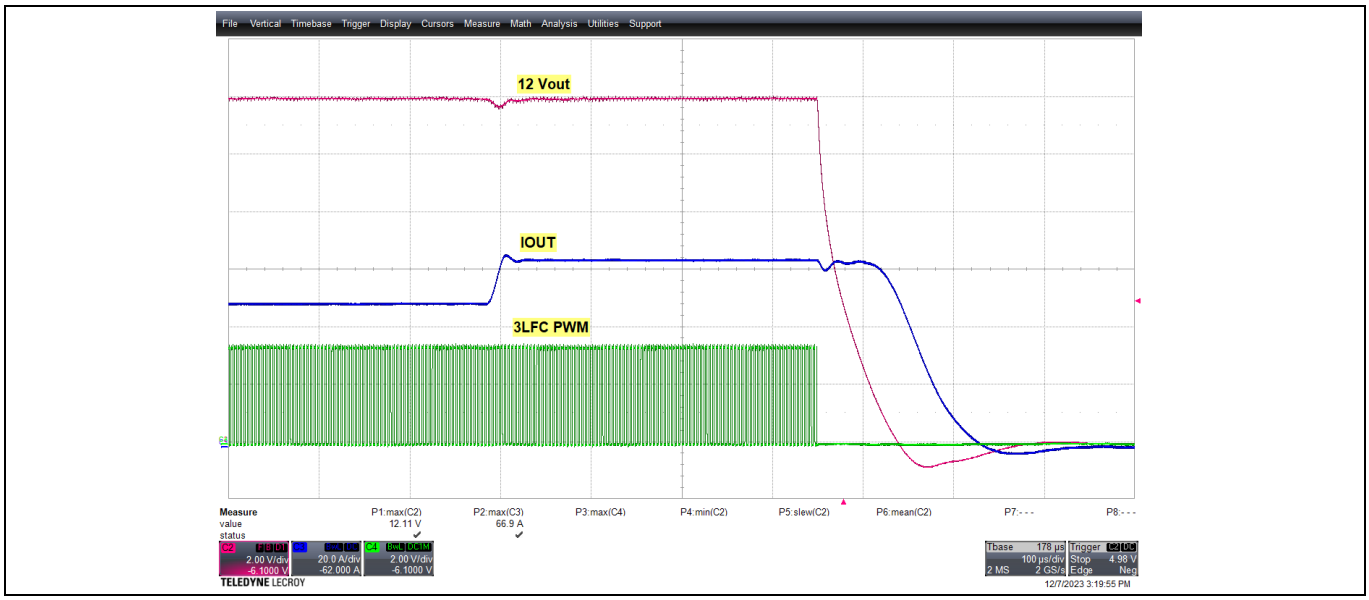



**Figure 47 Output OCP waveform at Vin = 48 V, Iout = 50 A to overcurrent**

## 8.3 Output short circuit protection

Tested at Vin = 48 V, Iout = 50 A, the output was shorted with a load bank.

**Ch1**: 12 V output voltage

**Ch3**: 3LFC PWM

**Ch4**: output current

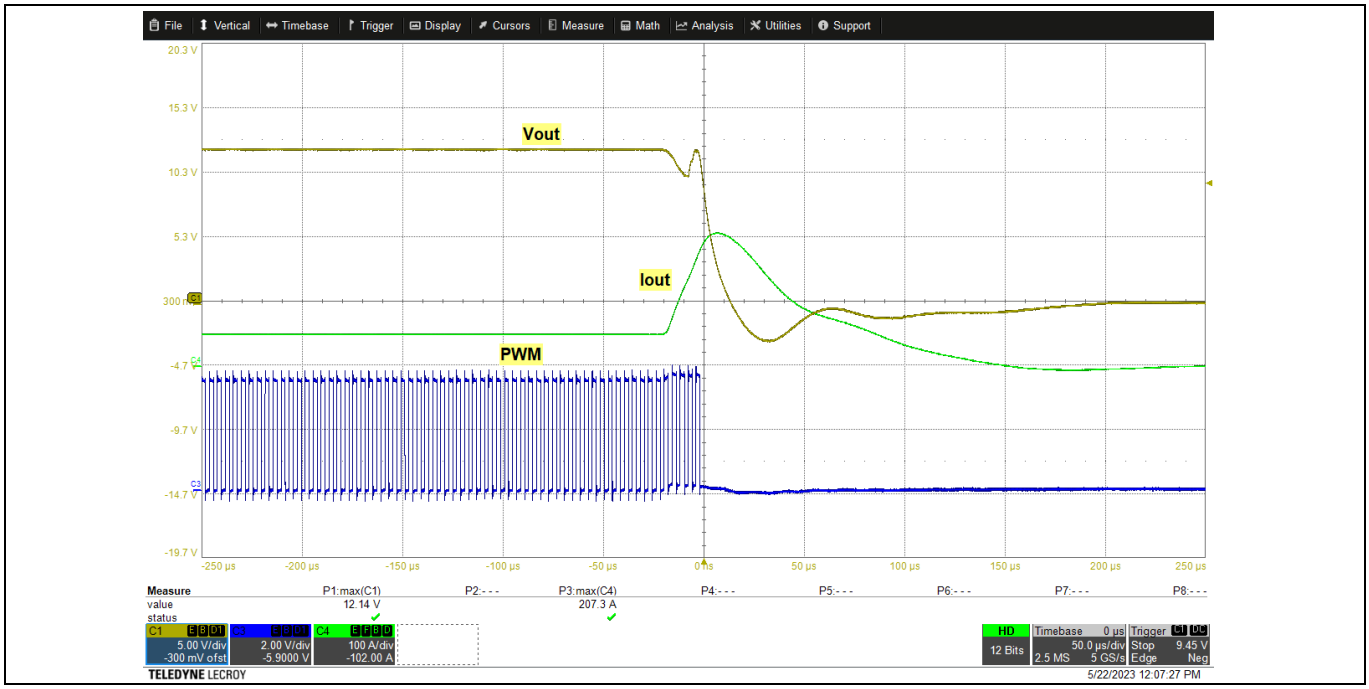



**Figure 48 Output short circuit waveform using load bank**

# 9 System design

## 9.1 Schematics

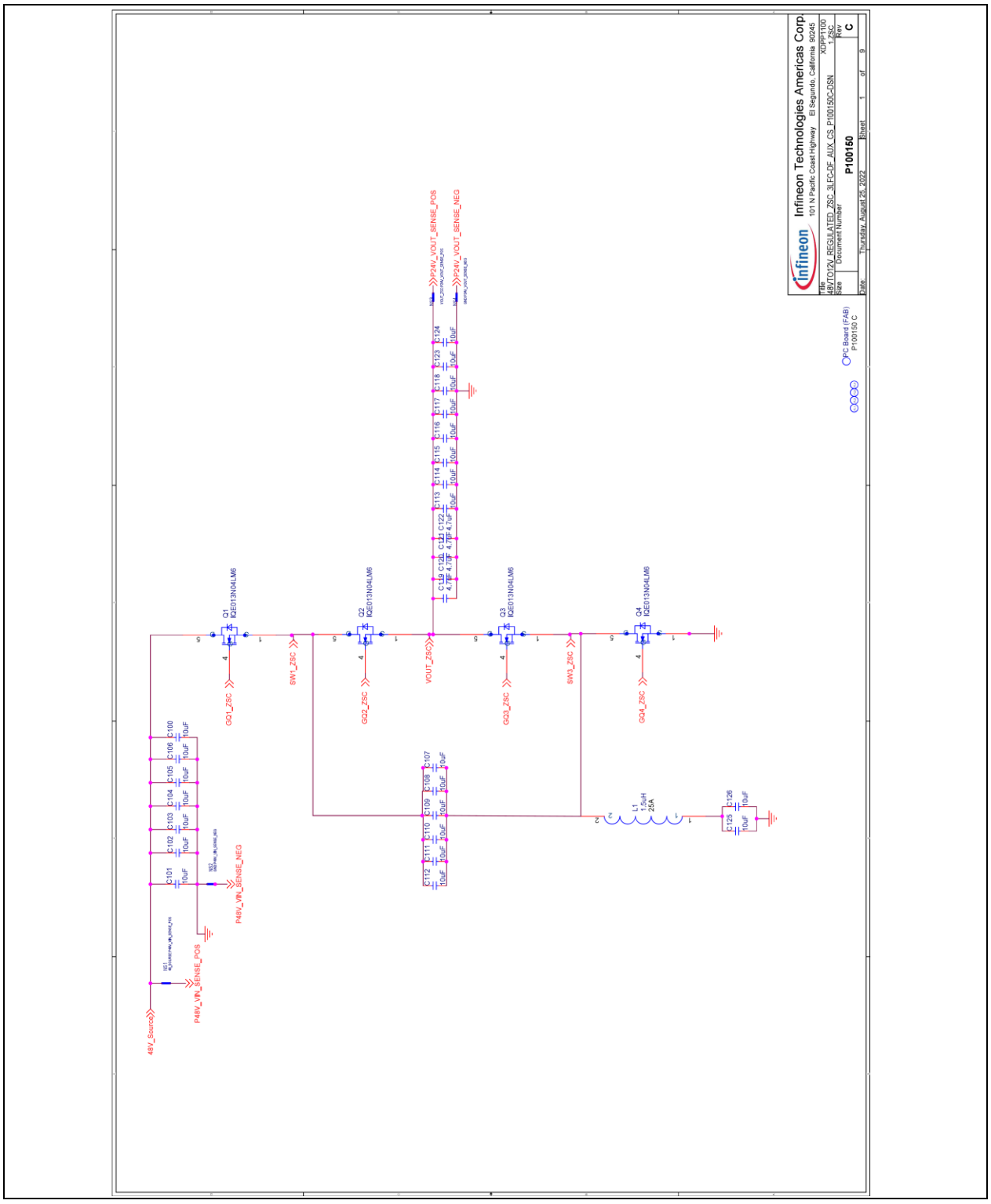



**Figure 49 DR-HSC, ZSC 2:1 main power stage**

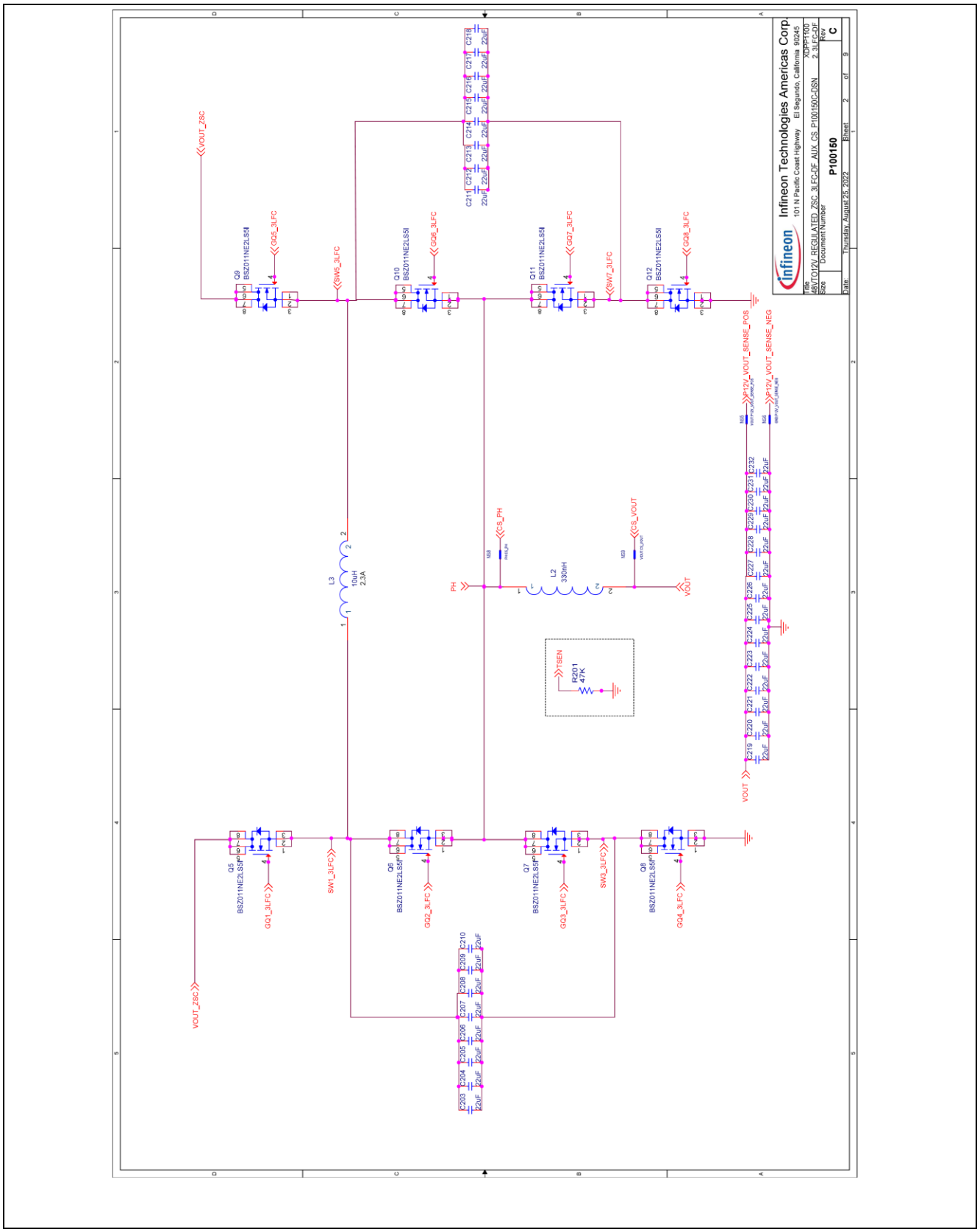



**Figure 50 DR-HSC, 3LFC-DP main power stage**

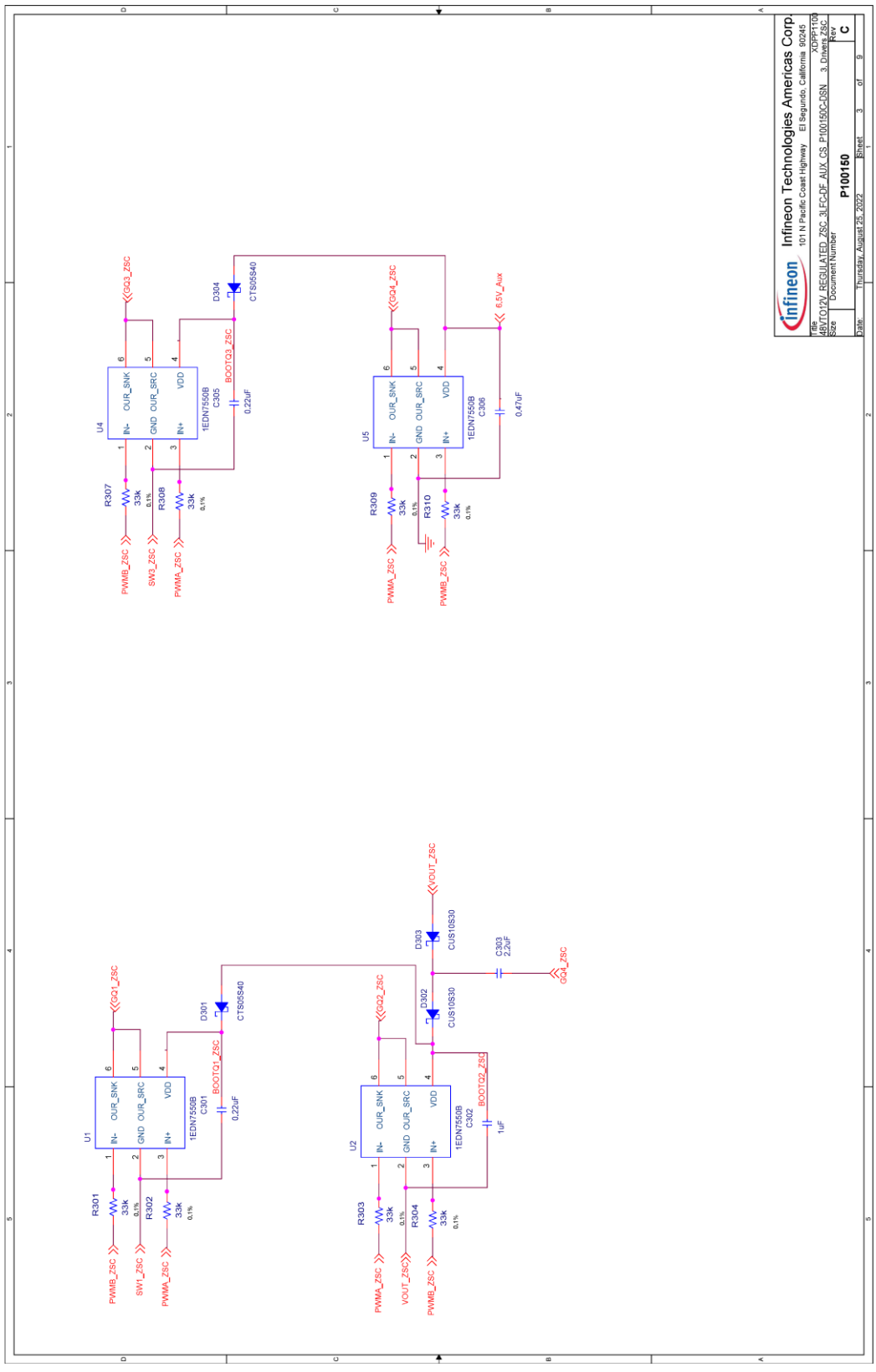



**Figure 51 DR-HSC, 2:1 ZSC driver circuit including charge pump**

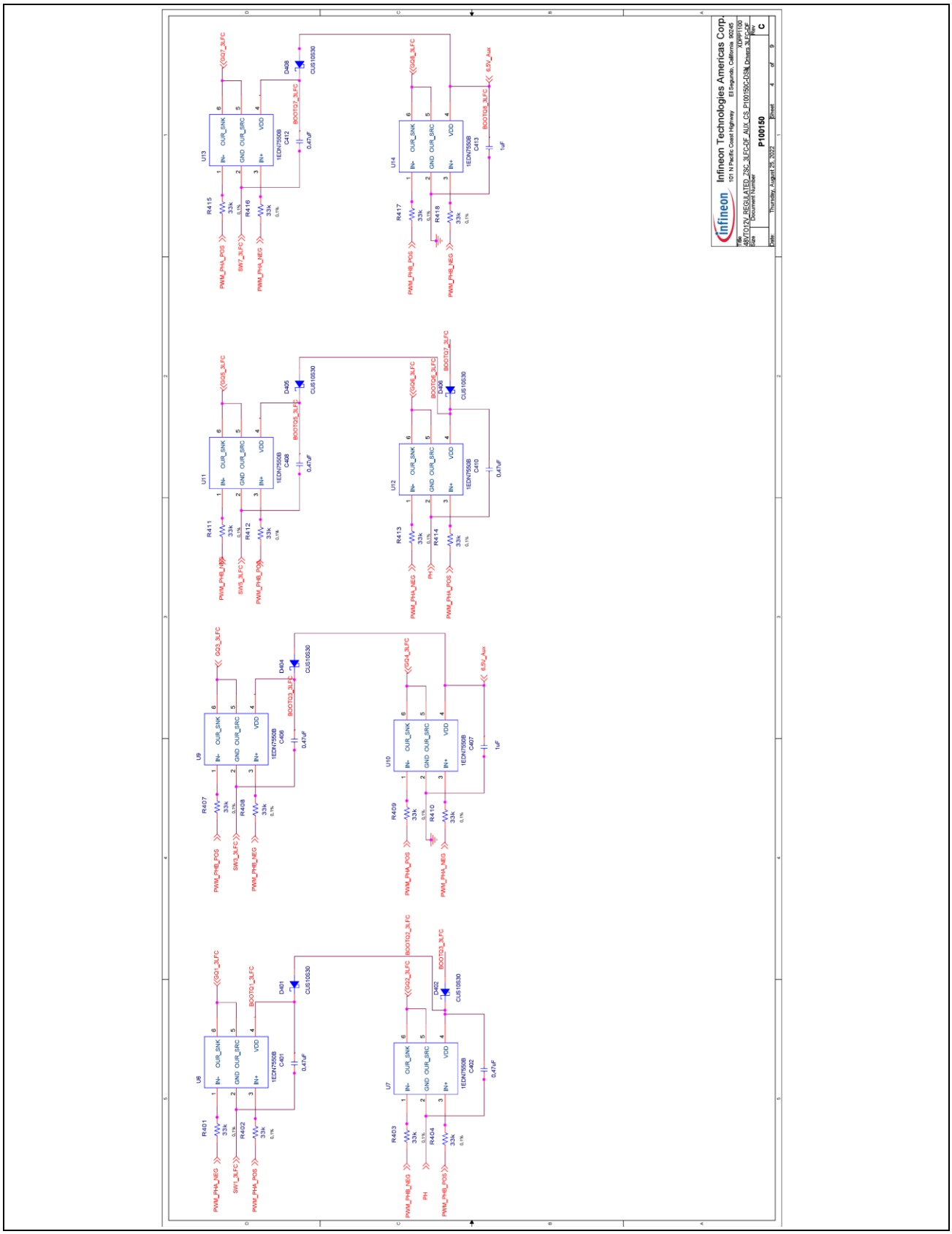


**Figure 52 DR-HSC, 3LFC-DP driver circuit**

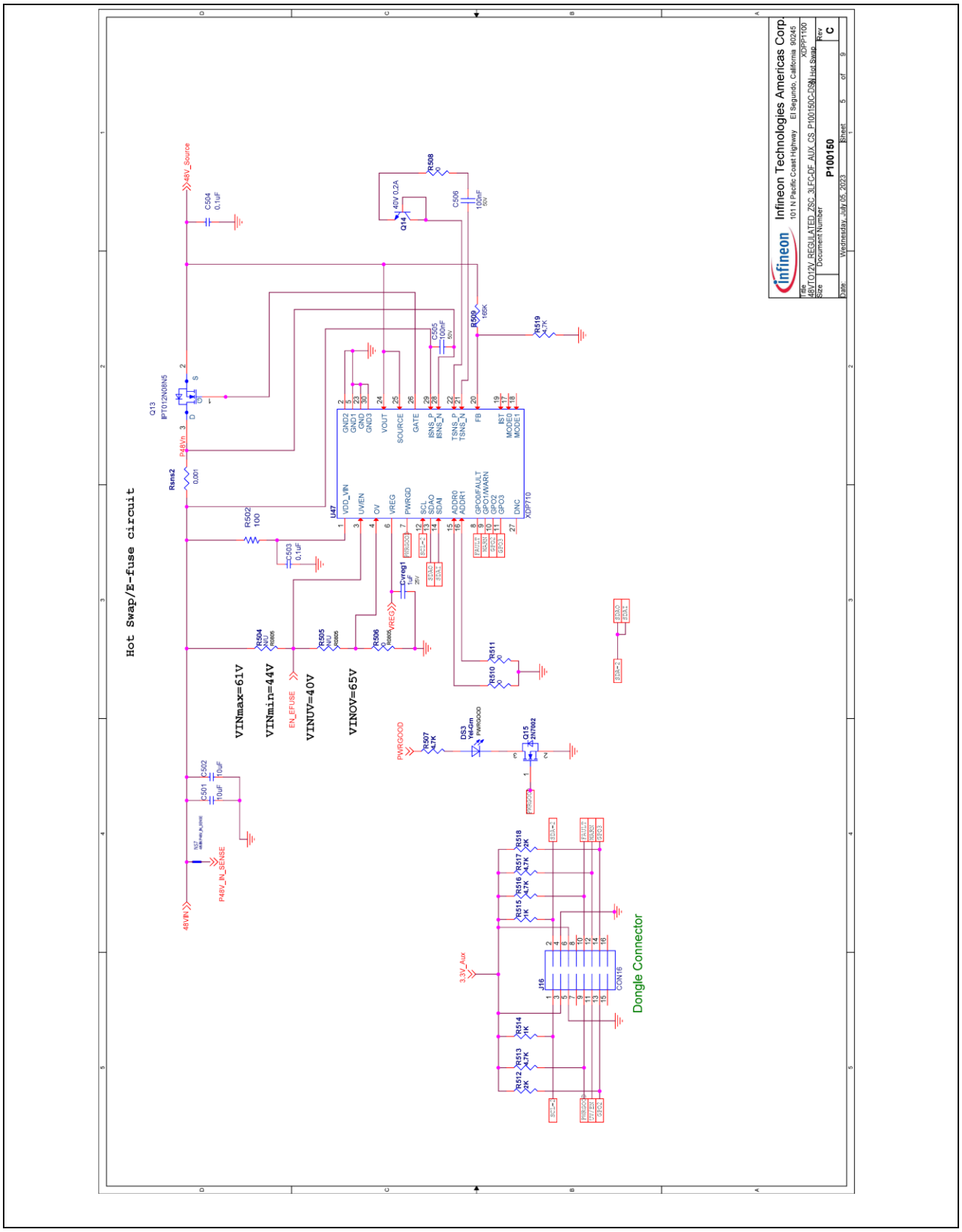



**Figure 53 DR-HSC, eFuse circuit on the 48 V input side**

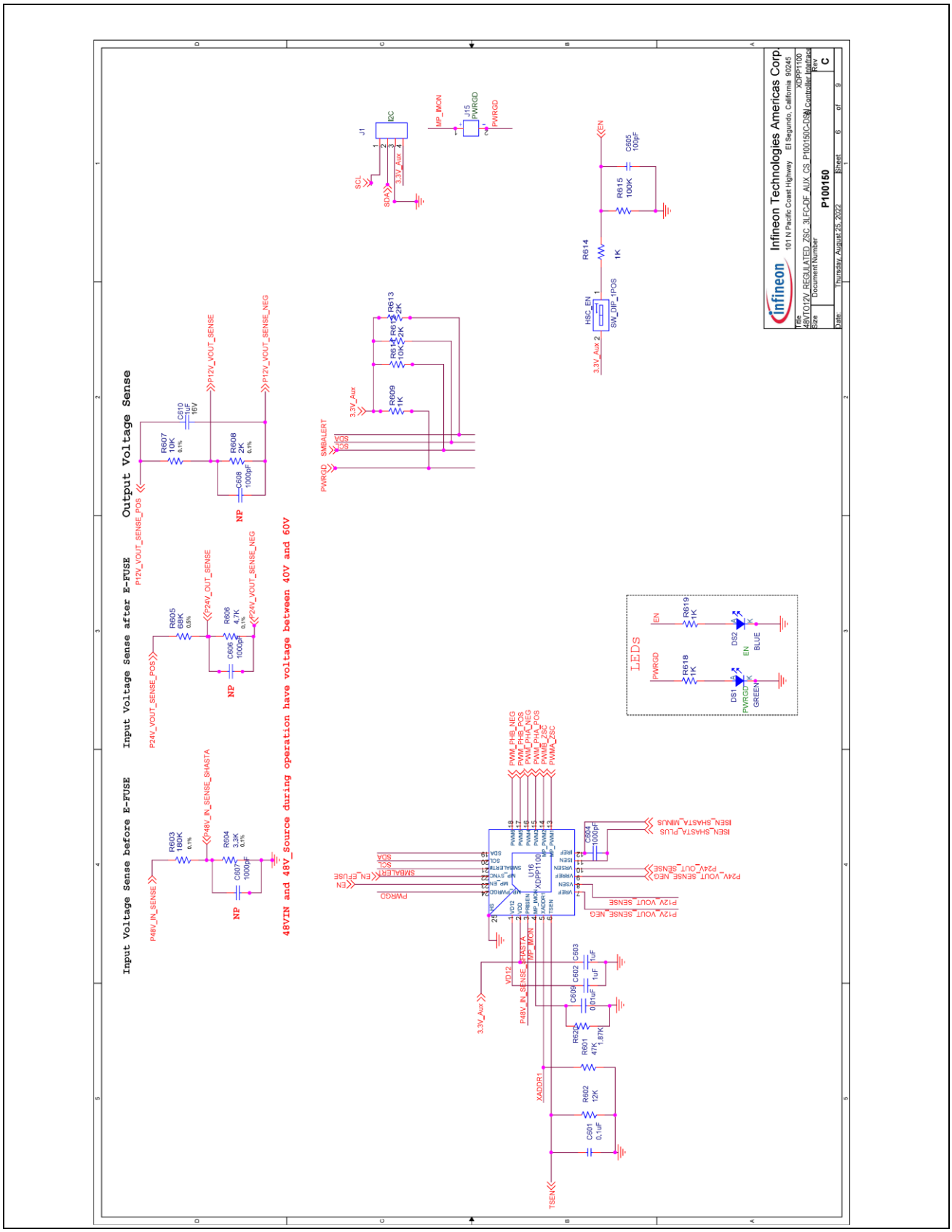



**Figure 54 DR-HSC, Main voltage sensing dividers and controller IC**

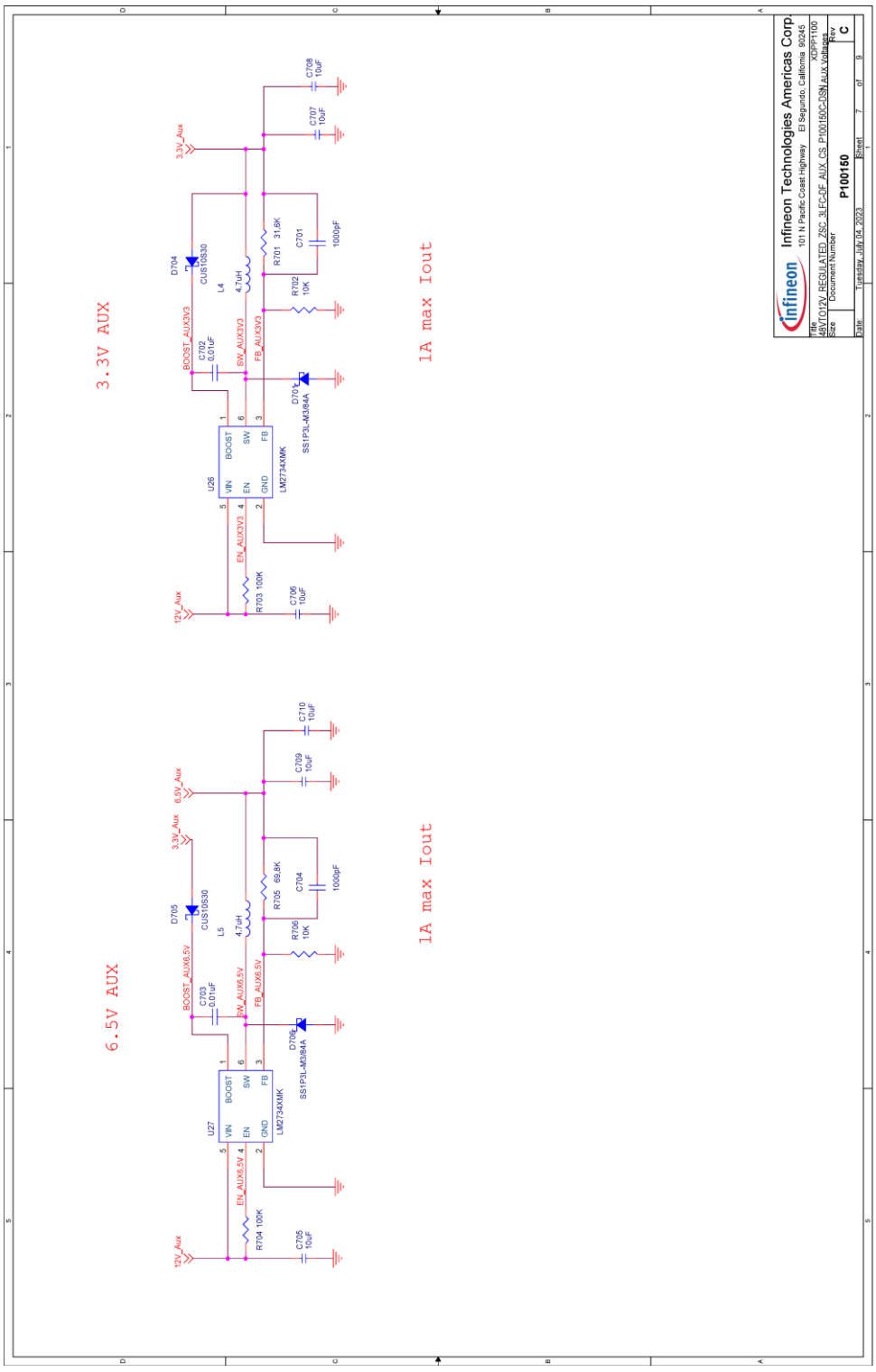



**Figure 55 DR-HSC, PoL for 3.3 V (controller) and 6.5 V (driver supply)**

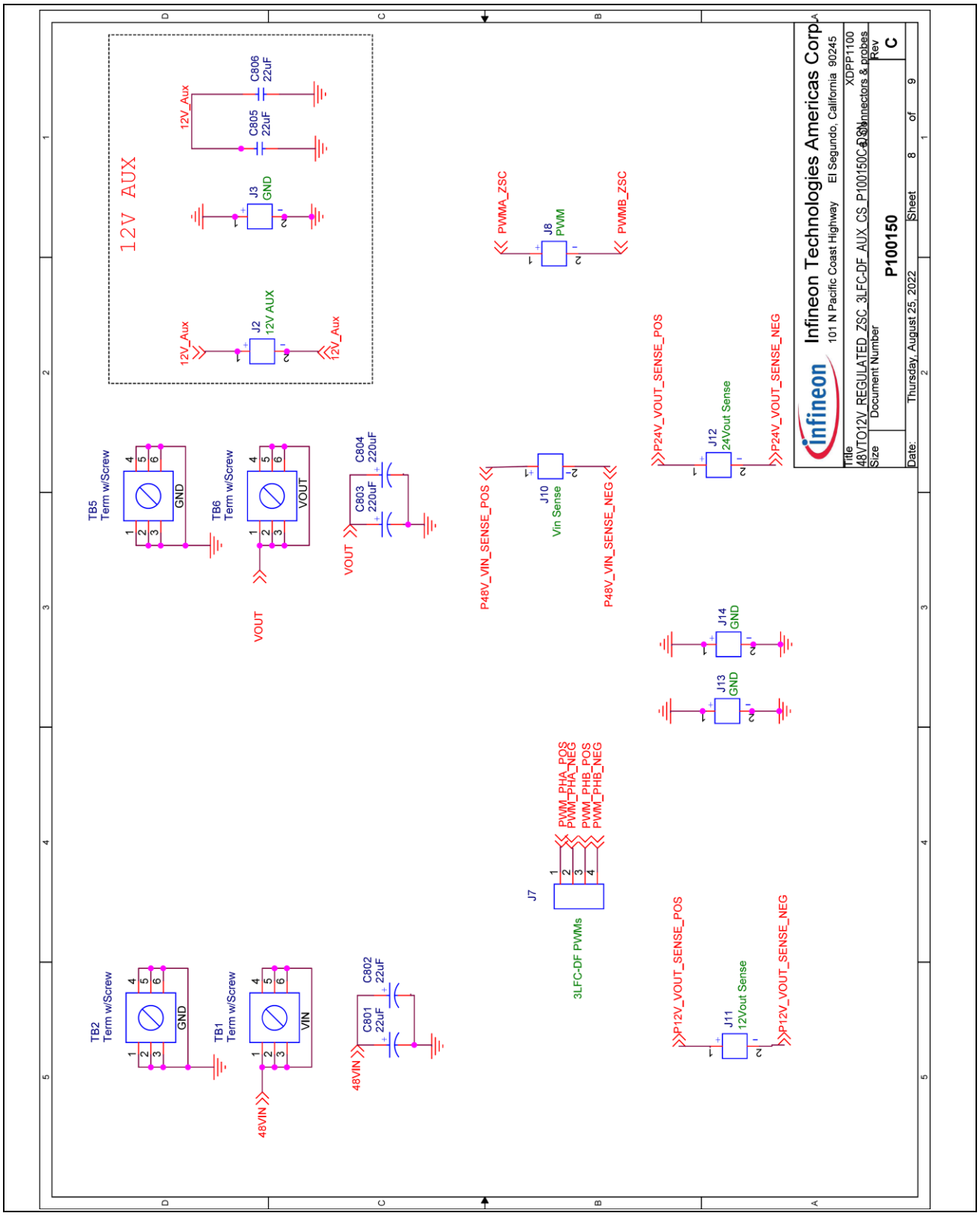



**Figure 56 DR-HSC, Main input/output connectors and test points**

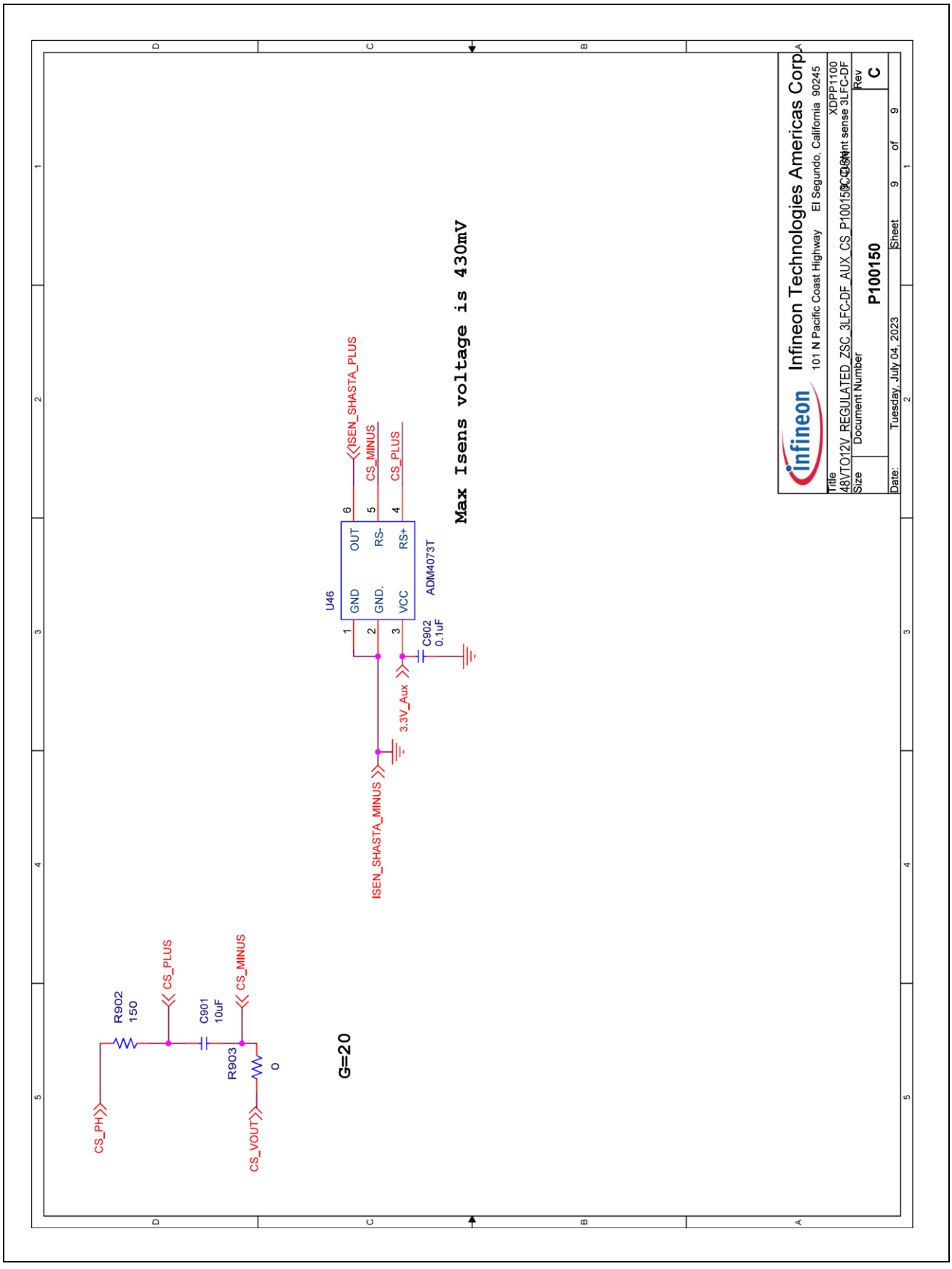



**Figure 57 DR-HSC, DCR current sensing IC**

## 9.2 Bill of materials (BoM)

The following table shows the components of the hardware demonstrator.

**Table 10 Bill of materials**

| Item | Quantity | Reference | Part | Footprint | Manufacturer | Part number |
|---|---|---|---|---|---|---|
| 1 | 9 | C100,C101, C102, C103, C104, C105, C106, C501, C502 | 10 µF | 1210 | Murata | GRM32EC72A106KE05 |
| 2 | 14 | C107,C108,C109,C110,C111,C112,C113,C114,C115,C116,C117,C118,C123,C124 | 10 µF | 1206 | Murata | GRM31CD71H106KE11 |
| 3 | 4 | C119, C120, C121, C122 | 4.7 µF | 0805 | Murata | GRM21BC81H475KE11 |
| 4 | 2 | C125,C126 | 10 µF | 0805 | Murata | GRM21BC81E106KE51 |
| 5 | 30 | C203,C204,C205,C206,C207,C208,C209,C210,C211,C212,C213,C214,C215,C216,C217,C218,C219,C220,C221,C222,C223,C224,C225,C226,C227,C228,C229,C230,C231,C232 | 22 µF | 1206 | Murata | GRM31CC81E226ME11 |
| 6 | 2 | C301,C305 | 0.22 µF | 0402 | Murata | GCM155R71C224KE02 |
| 7 | 1 | C303 | 2.2 µF | 0603 | Murata | GRM188R61H225KE11 |
| 8 | 7 | C306,C401,C402,C406,C408,C410,C412 | 0.47 µF | 0402 | Murata | GRM155C81C474KE01 |
| 9 | 4 | C302,C407,C413,C610 | 1 µF | 0402 | Murata | GRM155C81C105KE11 |
| 10 | 3 | C503,C504,C601 | 100 nF | 0402 | Murata | GRM155R62A104KE14D |
| 11 | 2 | C505,C506 | 100nF | 0603 | Murata | GRM188R71H104JA93D |
| 12 | 1 | Cvreg1 | 1 µF | 0603 | Murata | GRM188R71E105KA12D |
| 13 | 1 | C602 | 1 µF | 0402 | Murata | GRM155R61C105KA12D |
| 14 | 1 | C603 | 1 µF | 0603 | Murata | GRM188R61C105KA12 |
| 15 | 6 | C604,C606,C607,C608,C701,C704 | 1000 pF | 0402 | Murata | GRM155R71H102KA01J |
| 16 | 1 | C605 | 100 pF | 0603 | Murata | GRM1885C2A101JA01D |
| 17 | 3 | C609,C702,C703 | 0.01µF | 0402 | Murata | GRM155R71C103KA01D |
| 18 | 6 | C705,C706,C707,C708,C709,C710 | 10 µF | 1206 | TDK | CGA5L1X7R1E106M160AD |
| 19 | 2 | C801, C802 | 22 µF | smd_Fcase_cap | Chemi Con | EMVA101ADA220MHA0G |
| 20 | 2 | C803, C804 | 220 µF | smd_Fcase_cap | Panasonic | EEE-FK1C221V |

| Item | Quantity | Reference | Part | Footprint | Manufacturer | Part number |
|---|---|---|---|---|---|---|
| 21 | 2 | C805,C806 | 22 µF | 0805 | Murata | GRM21BR61E226ME44K |
| 22 | 1 | C901 | 10 µF | 0603 | Murata | GRM188R61E106KA73D |
| 23 | 1 | C902 | 0.1 µF | 0805 | Murata | GCM21BR72A104KA37L |
| 24 | 1 | DS1 | GREEN | LED-smd-0603 | Würth Elektronik | 150060GS75000 |
| 25 | 1 | DS2 | BLUE | LED-smd-0603 | Würth Elektronik | 150060BS75000 |
| 26 | 1 | DS3 | Yel-Grn | LED-SMD-SMLP13BC8T | Rohm | SML-P11MTT86R |
| 27 | 2 | D301, D304 | CTS05S40 | CTS05S40 | Toshiba | CTS05S40 |
| 28 | 10 | D302,D303,D401,D402,D404,D405,D406,D408,D704,D705 | CUS10S30 | SOD323 | Toshiba | CUS10S30 |
| 29 | 2 | D701,D706 | SS1P3L-M3/84A | DO-220AA | Vishay | SS1P3L-M3/84A |
| 30 | 1 | HSC_EN | SW_DIP_1POS | SW_1POS_GULL | C and K | SDA01H1SBD |
| 31 | 2 | J1, J7 | CON4 | conn4pin100 | Wurth | 613 004 111 21 |
| 32 | 9 | J2,J3,J8,J10,J11,J12,J13,J14,J15 | CON2 | conn2pin100 | Harwin | M20-9990246 |
| 33 | 1 | J16 | CON16 | CON-M-THT-SHF-108-01-L-D-TH | Samtec | SHF-108-01-L-D-TH |
| 34 | 1 | L1 | 1.5 µH/25 A | Lzvs_zsc | ITG | SLQ36385A-1R5L |
| 35 | 1 | L2 | 330 nH | Lout_3lfc | Sumida | CDB97D98 |
| 36 | 1 | L3 | 10 µH | IHLP-2020 | Vishay | IHLP2020BZER100M01 |
| 37 | 2 | L4,L5 | 4.7 µH | L-2p_4p1x4p1_VLCF4020T | TDK | VLCF4020T-4R7N1R2 |
| 38 | 4 | Q1, Q2, Q3, Q4 | IQE013N04LM6 | dfet_smd_033x033_h | Infineon | IQE013N04LM6ATMA1 |

| Item | Quantity | Reference | Part | Footprint | Manufacturer | Part number |
|---|---|---|---|---|---|---|
| 39 | 8 | Q5, Q6, Q7, Q8, Q9, Q10, Q11, Q12 | BSZ011NE2LS5I | pg-tsdson8 | Infineon | BSZ011NE2LS5IATMA1 |
| 40 | 1 | Q13 | IPT012N08N5 | TRANS | Infineon | IPT012N08N5ATMA1 |
| 41 | 1 | Q14 | 40V 0.2A | SOT23 | Nexperia | MMBT3904,215 |
| 42 | 1 | Q15 | 2N7002 | SOT23 | Infineon | 2N7002H6327XTSA2 |
| 43 | 1 | Rsns2 | 0.001 | R3920 | Bourns | CSS2H-3920R-1L00F |
| 44 | 2 | R201,R601 | 47K | 0402 | Yageo | RC0402FR-1347KL |
| 45 | 8 | R301,R302,R303,R304,R307,R308,R309,R31 | 33K | 0603 | Yageo | RT0603BRD0733KL |
| 46 | 16 | R401,R402,R403,R404,R407,R408,R409,R410,R411,R412,R413,R414,R415,R416,R417,R418 | 33K | 0402 | Yageo | RT0402BRD0733KL |
| 47 | 1 | R502 | 100 | 0402 | Panasonic | ERJ-2RKF1000X |
| 48 | 1 | R506 | 0 | 0805 | Panasonic | ERJ-6GEY0R00V |
| 49 | 4 | R507,R513,R516,R517 | 4.7K | 0603 | Panasonic | ERJ-3EKF4701V |
| 50 | 1 | R508 | 0 | 0603 | Panasonic | ERJ-3GEY0R00V |
| 51 | 1 | R509 | 165K | 0805 | Vishay | CRCW0805165KFKTA |
| 52 | 2 | R510,R511 | 0 | 0805 | Panasonic | ERJ-6GEY0R00V |
| 53 | 2 | R512,R518 | 2K | 0603 | Panasonic | ERJ-3EKF2001V |
| 54 | 5 | R514,R515,R614,R618,R619 | 1K | 0603 | Panasonic | ERJ-3EKF1001V |
| 55 | 1 | R519 | 4.7K | 0805 | Yageo | RC0805FR-074K7L |
| 56 | 1 | R602 | 12K | 0402 | Yageo | RMCF0402FT12K0 |
| 57 | 1 | R603 | 180K | 0402 | Yageo | RT0402FRE07180KL |
| 58 | 1 | R604 | 3.3K | 0402 | TE | CPF-A-0402B3K3E |
| 59 | 1 | R605 | 68K | 0402 | Yageo | RR0510P-683-D |
| 60 | 1 | R606 | 4.7K | 0402 | Yageo | RT0402BRD074K7L |
| 61 | 1 | R607 | 12K | 0402 | Yageo | RT0402BRD0712KL |
| 62 | 1 | R608 | 1.8K | 0402 | Yageo | RT0402BRD071K8L |
| 63 | 1 | R609 | 1K | 0402 | Rohm | ERJ-2RKF1001X |
| 64 | 3 | R611,R702,R706 | 10K | 0402 | Rohm | ERJ-2RKF1002X |
| 65 | 2 | R612,R613 | 2K | 0402 | Yageo | RT0402FRE072KL |
| 66 | 1 | R615 | 100K | 0603 | Panasonic | ERJ-3EKF1003V |
| 67 | 1 | R620 | 1.87K | 0402 | Panasonic | ERJ-2RKF1871X |
| 68 | 1 | R701 | 31.6K | 0402 | Yageo | RT0402BRD0731K6L |
| 69 | 2 | R703,R704 | 100K | 0402 | TE | CRGP0402F100K |

| Item | Quantity | Reference | Part | Footprint | Manufacturer | Part number |
|---|---|---|---|---|---|---|
| 70 | 1 | R705 | 69.8K | 0402 | Yageo | RC0402FR-0769K8L |
| 71 | 1 | R902 | 150 | 0402 | Yageo | ERJ2RKF1500X |
| 72 | 1 | R903 | 0 | 0402 | Panasonic | ERJ-2GE0R00X |
| 73 | 4 | TB1,TB2,TB5,TB6 | Term w/Screw | TB_1_0 | Keystone | 8199 |
| 74 | 12 | U1,U2,U4,U5,U6,U7,U9,U10,U11,U12,U13,U14 | 1EDN7550B | PG-SOT23-6 | Infineon | 1EDN7550B |
| 75 | 1 | U16 | XDPP1100 | qfn24-4x4mm | Infineon | XDPP1100-Q024 |
| 76 | 1 | U26,U27 | LM2734XMK | SOT23-6 | TI | LM2734XMK |
| 77 | 1 | U46 | ADM4073T | PG-SOT23-6 | Analog Devices | ADM4073TWRJZ |
| 78 | 1 | U47 | XDP710 | qfn29-6x6mm | Infineon | XDP710-002 |

## References

[1] Infineon Technologies AG: *XDP710-002 hot-swap controller datasheet;* Available online

[2] Infineon Technologies AG: *XDPP1100 datasheet;* Available online

[3] Infineon Technologies AG: *XDP™ XDPP1100, XDPP1100A reference manual;* Available online

## Revision history

| Document revision | Date | Description of changes |
|---|---|---|
| ** | 2024-04-24 | Initial release |

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**Edition 2024-04-24**

**Published by**

**Infineon Technologies AG**

**81726 Munich, Germany**



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**Email:** erratum@infineon.com

**Document reference**

**AN043252**

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