3.3 kW high-frequency and high-density PSU for server and datacenter applications

REF_3K3W_HFHD_PSU

About this document

Scope and purpose

This document introduces a complete system solution from Infineon Technologies AG for a high power density 3.3 kW power supply unit (PSU) which targets specifications for server and datacenter applications.

This document describes the converter hardware, provides a summary of the experimental results and design recommendations for the complete Infineon solution, including an innovative planar magnetic construction. The REF_3K3W_HFHD_PSU comprises a front-end AC-DC converter and a back-end isolated DC-DC converter. The AC-DC converter is an interleaved bridgeless totem pole (ILTP) stage featuring two phases that provide power factor correction (PFC) and limits total harmonic distortion (THD). The back-end DC-DC is a GaN half-bridge (HB) LLC converter with full bridge (FB) rectification, which provides safety isolation and regulates the output voltage. The PSU also features a baby-boost converter to comply with the hold-up time specifications of server applications with a reduced overall bulk capacitance, increasing the overall power density.

The measured peak efficiency of the complete PSU at 230 V_{AC} input line is 97.4 percent, not including the internal fan and the overall outer dimensions of 72 mm x 192 mm x 40 mm, yielding to 98 W/inch^3 power density.

Intended audience

The document and the related REF_3K3W_HFHD_PSU hardware are intended for R&D engineers, hardware designers, and developers of power electronic systems.

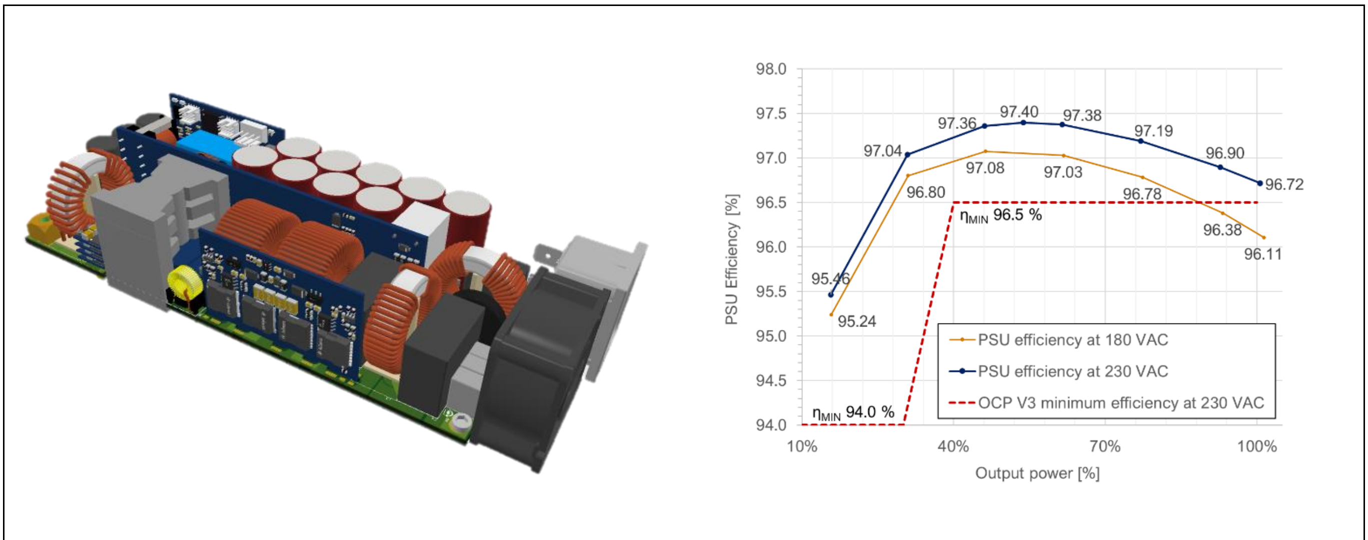


Figure 1 **3.3 kW REF_3K3W_HFHD_PSU server power supply overview and measured efficiency**

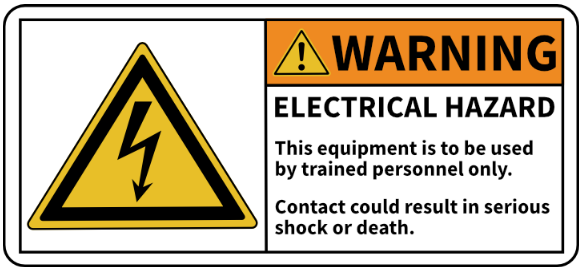
The main Infineon components used in the REF_3K3W_HFHD_PSU are:

- CoolSiC™ 650 V M1, 57 mΩ TOLL (IMT65R057M1H), and EiceDRIVER™ 2EDB9259Y for the fast legs of the totem-pole PFC converter
- CoolMOS™ 600 V CM8, 16 mΩ TOLL (IPT60R016CM8), EiceDRIVER™ 1EDN8511B, and 1EDB8275F for the slow leg of the totem-pole PFC converter and the static switch of the baby boost converter
- CoolGaN™ 650 V GIT, 35 mΩ TOLL (IGT65R035D2), EiceDRIVER™ 1EDN8550B, and 1EDB8275F for HB switches at the primary side of the LLC converter
- OptiMOS™ 80 V, 4.6 mΩ source-down (IQE046N08LM5), and EiceDRIVER™ 2EDB7259K for the synchronous rectification (SR) switches at the secondary side of the LLC converter
- CoolMOS™ 600 V G7, 80 mΩ (IPT60R080G7), CoolSiC™ 600 V diode (IDL10G65C5), and EiceDRIVER™ 1EDB8275F for the baby boost converter
- ISOFACE™ 4DIR1400H digital isolator for the primary to secondary isolation in the LLC converter
- XMC4200-Q48K256 microcontroller for the implementation of the PFC control

Table of contents

Safety information

Please read this document carefully before starting up the device.



Important notice

Evaluation boards, demonstration boards, reference boards and kits are electronic devices typically provided as an open-frame and unenclosed printed circuit board (PCB) assembly. Each board is functionally qualified by electrical engineers and strictly intended for use in development laboratory environments. Any other use and/or application is strictly prohibited. Our boards and kits are solely for qualified and professional users who have training, expertise, and knowledge of electrical safety risks in the development and application of high-voltage electrical circuits. Please note that evaluation boards, demonstration boards, reference boards and kits are provided "as is" (i.e., without warranty of any kind). Infineon is not responsible for any damage resulting from the use of its evaluation boards, demonstration boards, reference boards or kits. To make our boards as versatile as possible, and to give you (the user) opportunity for the greatest degree of customization, the virtual design data may contain different component values than those specified in the bill of materials (BOM). In this specific case, the BOM data has been used for production. Before operating the board (i.e. applying a power source), please read the application note/user guide carefully and follow the safety instructions. Please check the board for any physical damage, which may have occurred during transport. If you find damaged components or defects on the board, do not connect it to a power source. Contact your supplier for further support. If no damage or defects are found, start the board up as described in the user guide or test report. If you observe unusual operating behavior during the evaluation process, immediately shut off the power supply to the board and consult your supplier for support.

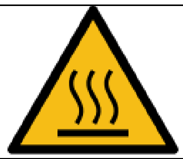
Operating instructions

Do not touch the device during operation, keep a safe distance. Do not touch the device after disconnecting the power supply, as several components may still store electrical voltage and can discharge through physical contact. Several parts, like heatsinks and transformers, may still be very hot. Allow the components to discharge and cool before touching or servicing. All work such as construction, verification, commissioning, operation, measurements, adaptations, and other work on the device (applicable national accident prevention rules must be observed) must be done by trained personnel. The electrical installation must be completed in accordance with the appropriate safety requirements.

Safety precautions

Note: *Please note the following warnings regarding the hazards associated with development systems.*

Table 1 **Safety precautions**

	**Warning:** *The evaluation or reference board contains DC bus capacitors, which take time to discharge after removal of the main supply. Before working on the converter system, wait five minutes for capacitors to discharge to safe voltage levels. Failure to do so may result in personal injury or death. Darkened display LEDs are not an indication that capacitors have discharged to safe voltage levels.*
	**Warning:** *The evaluation or reference board is connected to the AC input during testing. Hence, high-voltage differential probes must be used when measuring voltage waveforms by oscilloscope. Failure to do so may result in personal injury or death. Darkened display LEDs are not an indication that capacitors have discharged to safe voltage levels.*
	**Warning:** *Remove or disconnect power from the converter before you disconnect or reconnect wires, or perform maintenance work. Wait five minutes after removing power to discharge the bus capacitors. Do not attempt to service the drive until the bus capacitors have discharged to zero. Failure to do so may result in personal injury or death.*
	**Caution:** *The heatsink and device surfaces of the evaluation or reference board may become hot during testing. Hence, necessary precautions are required while handling the board. Failure to comply may cause injury.*
	**Caution:** *Only personnel familiar with the converter, power electronics and associated equipment should plan, install, commission, and subsequently service the system. Failure to comply may result in personal injury and/or equipment damage.*
	**Caution:** *The evaluation or reference board contains parts and assemblies sensitive to electrostatic discharge (ESD). Electrostatic control precautions are required when installing, testing, servicing or repairing the assembly. Component damage may result if ESD control procedures are not followed. If you are not familiar with electrostatic control procedures, refer to the applicable ESD protection handbooks and guidelines.*
	**Caution:** *A converter that is incorrectly applied or installed can lead to component damage or reduction in product lifetime. Wiring or application errors such as undersizing the cabling, supplying an incorrect or inadequate AC supply, or excessive ambient temperatures may result in system malfunction.*

1 Background and system functional description

1.1 Background

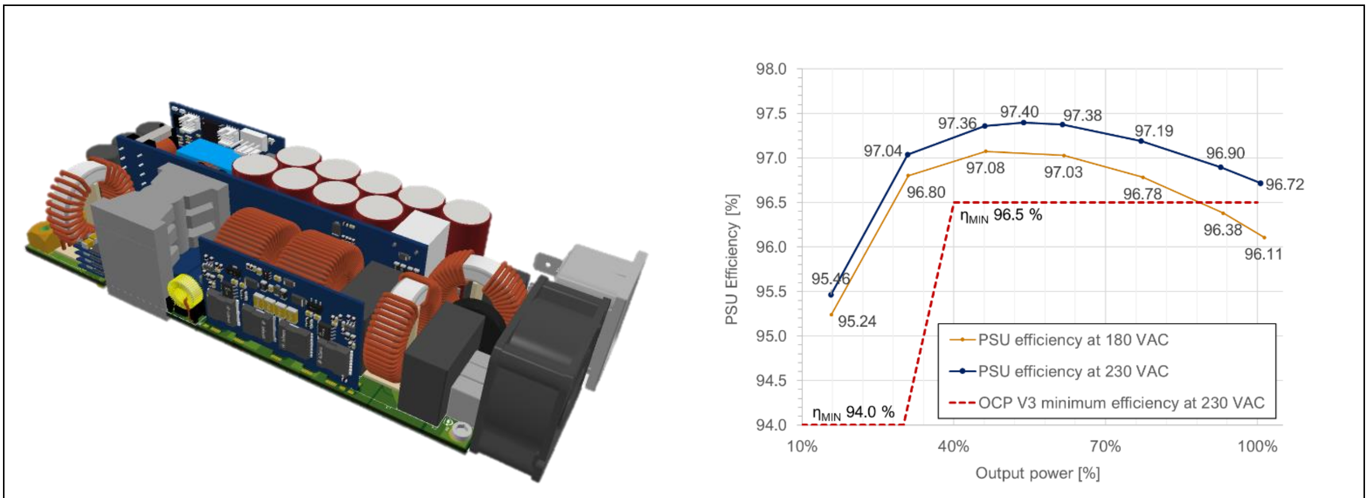
Recently, power demand at rack level in server and data centers has grown substantially to accommodate the higher computing workload in less floor space. This increase in the power demand is consistently tightening the requirements in terms of power density and efficiency in the power supplies to reduce the space occupied and also the heat dissipated.

These requirements can be observed in the OCP rectifier v3 specification for server and datacenter PSU [1]. In terms of efficiency and power density, a 97.5 percent peak efficiency at 230 V_{AC} is required, with additional requirements of a minimum power density of 32.15 W/inch^3 (1.96 W/cm^3), 520 mm × 73.5 mm × 40 mm maximum dimensions, and 20 ms hold-up time at full power. Infineon's EVAL_3KW_50V_PSU released in 2021 [2] meets all these specifications, and REF_3K3W_HFHD_PSU presented in this document showcases a possible increase of the power density with no compromise in terms of the system efficiency.

1.2 Power supply unit description

REF_3K3W_HFHD_PSU comprises a front-end AC-DC converter and a back-end isolated DC-DC converter. The AC-DC converter is an interleaved bridgeless totem-pole stage featuring two phases that provide power factor correction and limits total harmonic distortion. The back-end DC-DC is a GaN half-bridge LLC converter with full-bridge rectification. The back-end provides safety isolation and regulates the output voltage. The PSU also features a baby-boost converter to comply with the hold-up time specifications of server applications with a reduced overall bulk capacitance, increasing the overall power density.

The measured peak efficiency of the complete PSU at 230 V_{AC} input line is 97.4 percent, not including the internal fan, and overall outer dimensions of 72 mm × 192 mm × 40 mm, yielding a 98 W/inch^3 power density.



(a) (b)

Figure 2 (a) A rendering of 3.3 kW REF_3K3W_HFHD_PSU and (b) its efficiency curves

The main Infineon components used in REF_3K3W_HFHD_PSU are:

- CoolSiC™ IMT65R057M1H, 650 V M1 57 mΩ TOLL, and EiceDRIVER™ 2EDB9259Y for the fast-legs of the totem-pole PFC converter
- CoolMOS™ IPT60R016CM8, 600 V CM8 16 mΩ TOLL, EiceDRIVER™ 1EDN8511B for the slow leg of the totem-pole PFC converter, and EiceDRIVER™ 1EDB8275F for the static switch of the baby-boost converter
- CoolGaN™ IGT65R035D2 650 V GIT 35 mΩ TOLL, EiceDRIVER™ 1EDN8550B, and 1EDB8275F for HB switches at the primary side of the LLC converter
- OptiMOS™ IQE046N08LM5, 80 V 4.6 mΩ source-down, and EiceDRIVER™ 2EDB7259K for the synchronous rectification (SR)s switches at the secondary-side of the LLC converter
- CoolMOS™ IPT60R080G7, 600 V G7 80 mΩ, and CoolSiC™ IDL10G65C5, 600 V diode, and EiceDRIVER™ 1EDB8275F for the baby-boost converter
- ISOFACE™ 4DIR1400H digital isolator for the primary to secondary isolation in the LLC converter
- XMC4200-Q48K256 microcontroller for the implementation of the PFC control
- CoolSET™ ICE2QR2280G, 800 V quasi-resonant flyback controller

The evaluation board REF_3K3W_HFHD_PSU is mounted over a metallic frame and covered by a plastic enclosure to ensure proper airflow and cooling. It has dimensions of 192 mm × 72 mm × 40 mm including a fan and an AC inlet connector. For comparison, OCP v3 specifies a maximum dimension of 520 mm × 73.5 mm × 40 mm). Overall, the PSU results in a power density of 98 W/inch^3.

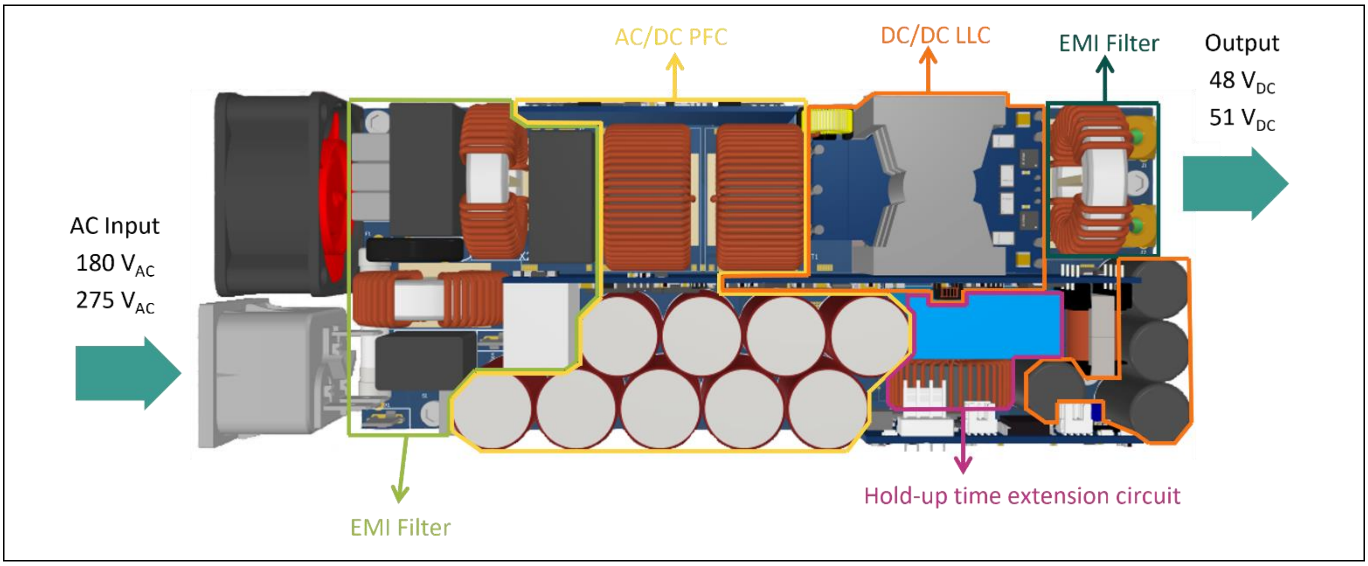


Figure 3 Overview of the REF_3K3W_HFHD_PSU

To achieve the power density target, a tri-dimensional mechanical assembly is necessary and multiple daughter boards are assembled on the main PCB as shown in Figure 4.

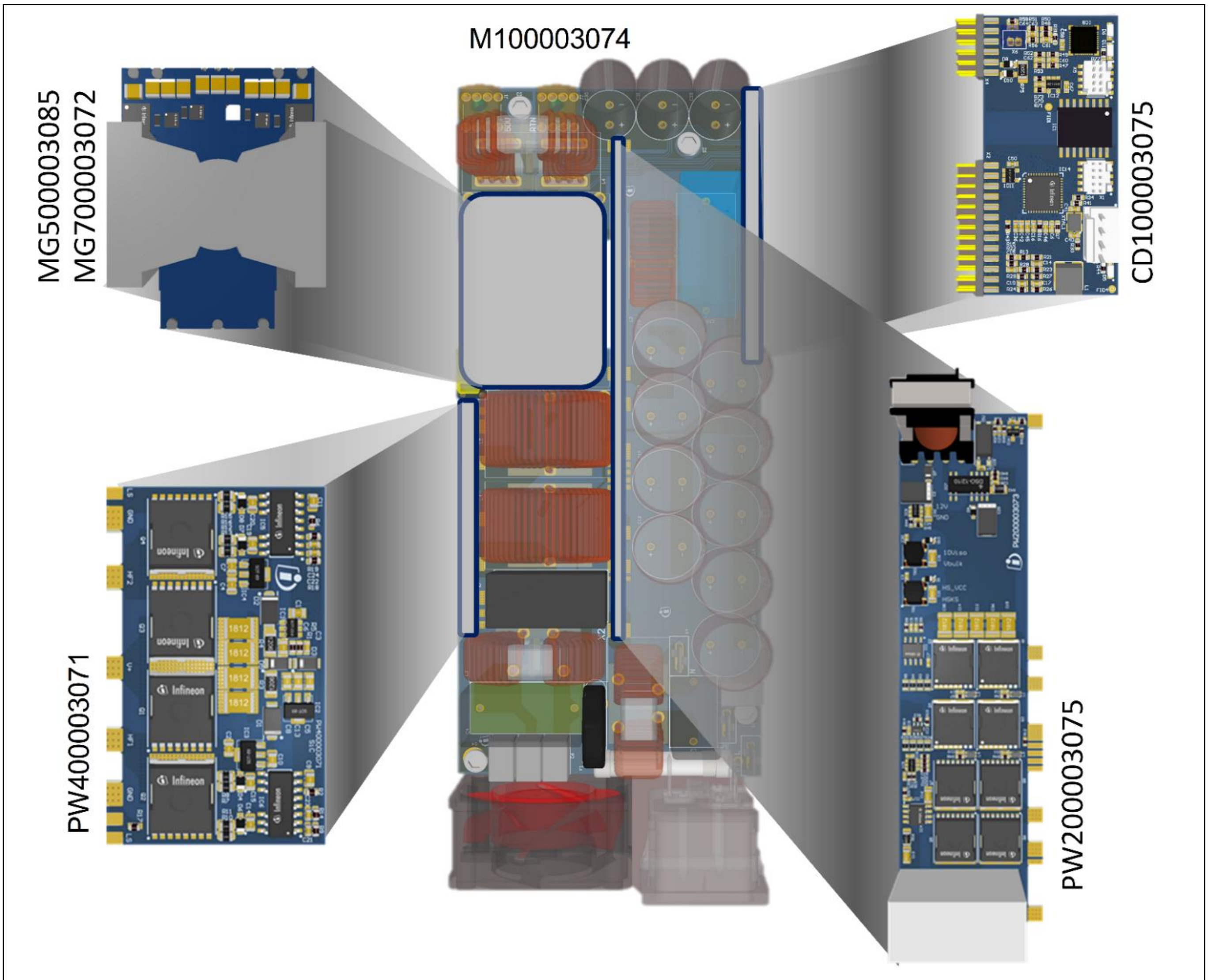


Figure 4 REF_3K3W_HFHD_PSU main board and daughter cards with their assembly

The following daughter boards are used:

- The main board (M1000003074) hosts the passive components of the input and output EMI filters, the two PFC inductor chokes, the capacitors of the intermediate bulk, and provides mechanical support and electrical connections for the daughter boards
- The ILTP-PFC high-frequency board (PW400003071) is a daughter board encompassing the two high-frequency legs of the PFC and is mounted perpendicular to the main board
- The LLC and PFC SR power card (PW200003075) is assembled in the center of the board, and hosts the PFC SR stage, the LLC primary-side, and the flyback power supply for housekeeping.
- The planar primary and secondary PCBs (MG500003085 and MG700003072) are embedded in the transformer structure for primary- and secondary-side planar windings
- The control PCBA (CD100003075) hosts the two primary- and secondary-side controllers, plus provides isolation to the UART communication channel and the PWM of the LLC HB MOSFETs. The fan airflow is sucking air out of the chassis for better thermal performances

1.3 Converter architecture

REF_3K3W_HFHD_PSU is a unidirectional PSU that comprises two stages:

- A front-end bridgeless totem-pole AC-DC converter that provides PFC and THD
- A half-bridge LLC DC-DC converter that provides safety isolation and regulated output

A simplified block diagram of the full PSU is shown in Figure 5.

The control of the totem-pole AC-DC converter is implemented with the Infineon XMC™ 4200 microcontroller with PFC, THD, voltage regulation, phase overcurrent protection (OCP1 and OCP2), overvoltage protection (OVP), undervoltage protection (UVP), undervoltage lockout (UVLO), soft-start, synchronous rectification (SR) control, adaptive dead-times, and serial communication interface towards the LLC secondary-side controller.

The control of the LLC converter is implemented with a third-party microcontroller referenced to the secondary-side ground, and features voltage-regulation functionality, burst-mode operation, output OCP, OVP, UVP, UVLO, soft-start, SR control, adaptive dead-times, and a serial communication interface. The isolation between the two controllers (UART communication and PWM signals for the primary-side HB of the LLC) is managed by means of a quad-channel digital isolator.

In the front-end AC-DC converter, the two interleaved high-frequency HB legs use in total four 57 mΩ CoolSiC™ switches driven by two EiceDRIVER™ 2EDB9259Y. The low-frequency leg uses four of 16 mΩ CoolMOS™ switches in parallel with a combination of EiceDRIVER™ 1EDB8275F and EiceDRIVER™ 1EDN8115B in a hybrid configuration.

For the LLC converter, four of 42 mΩ CoolGaN™ are used for the HB HV primary-side in conjunction with a combination of EiceDRIVER™ 1EDB8275F and EiceDRIVER™ 1EDN8550B. For the secondary-side SR, an integrated approach is followed – the SR MOSFETs are mounted on the secondary-side PCB windings and integrated on the same magnetic structure that realizes the main transformer, the resonant inductance, and the magnetizing inductance. The LLC SR stage uses 32 of 4.6 mΩ OptiMOS™ 5 power transistors, driven by eight EiceDRIVER™ 2EDB7259K. See Section 1.5.3 for more information about the integrated transformer assembly.

To ensure hold-up time specifications are met while reducing the amount of bulk capacitance of the PSU, a baby-boost converter is used to decouple the bulk voltage from the LLC input during the hold-up event. During steady-state operation, the baby-boost is bypassed by a low-ohmic 16 mΩ CoolMOS™ switch.

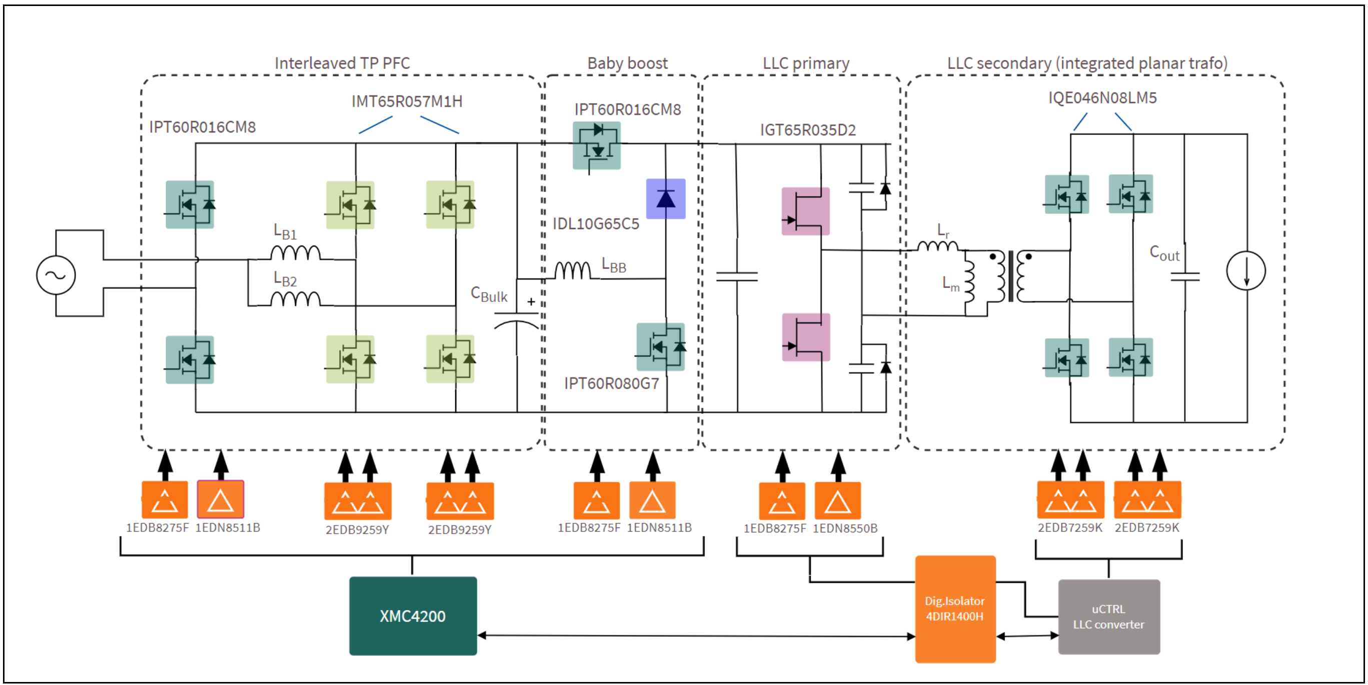


Figure 5 **Simplified schematic of the REF_3K3W_HFHD_PSU prototype**

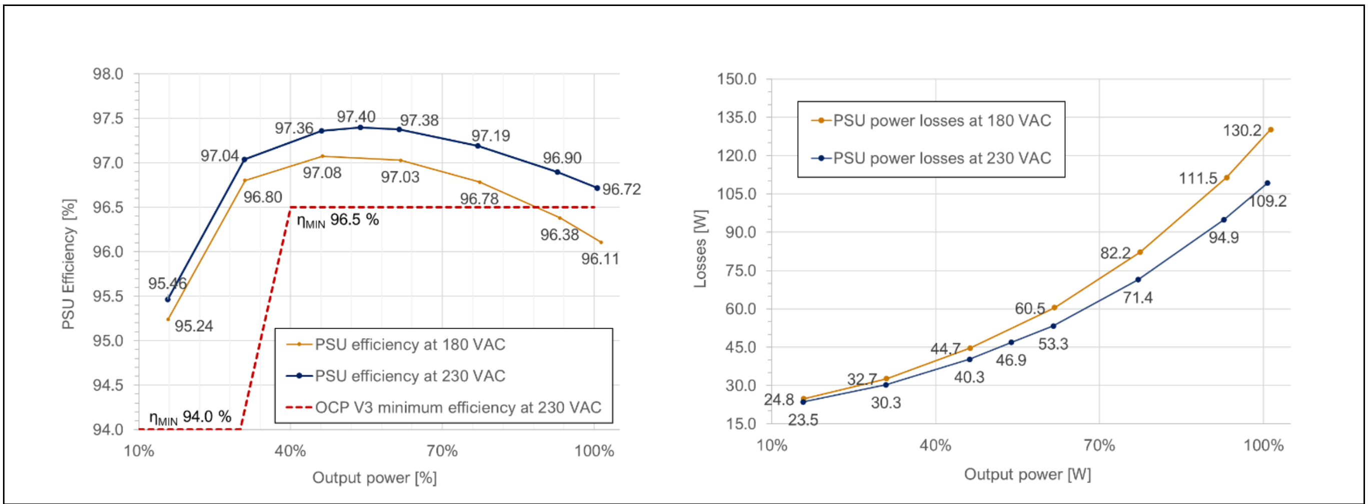


Figure 6 **Measured efficiency and power losses of REF_3K3W_HFHD_PSU vs. minimum OCP v3 targets**

The operating principle of the totem-pole PFC AC-DC and LLC DC-DC converter blocks shown in Figure 5 can be studied independently thanks to Infineon's open-frame evaluation boards EVAL_3K3W_TP_PFC_SIC and EVAL_3K3W_LLC_HB_CFD7, available to order on the Infineon website or via third-party distributors.

EVAL_3K3W_TP_PFC_SIC is a single-phase stand-alone totem-pole AC-DC converter with PFC and THD functionalities. It is an open-frame converter with an integrated internal fan. EVAL_3K3W_LLC_HB_CFD7 is a stand-alone LLC DC-DC converter with integrated probing points, easily replaceable primary-side switches, and an oversized heatsink. Like EVAL_3K3W_TP_PFC_SIC, it is an open-frame converter that allows easy evaluation. In REF_3K3W_HFHD_PSU both functional blocks slightly differ, as they have been modified to achieve the required power and efficiency targets (e.g. interleaving of the AC-DC stage, different switches/packages etc.) of the full PSU.

Note: In REF_3K3W_HFHD_PSU, the two blocks share power earth (PE) via the metallic chassis and cooling is done via piping of the airflow by means of the plastic enclosure. For electrical safety and cooling reasons, it is therefore, recommended not to operate the board without enclosure or chassis. It is the user's responsibility to ensure proper cooling and connections when operating the unit outside of the recommended operating conditions.

1.4 Bridgeless interleaved totem-pole PFC

A simplified schematic of the interleaved totem-pole PFC stage of REF_3K3W_HFHD_PSU is shown in Figure 2 while the hardware implementation of the fast SiC leg and its location within the board is shown in Figure 8. The AC inlet is followed by a two-stage input EMI filter and the NTC + relay. The AC line is connected to the two high-frequency CoolSiC™ fast-legs of the totem-pole PFC via filter-inductors (Q_{A_HS}, Q_{A_LS}, Q_{B_HS}, and Q_{B_LS} in Figure 2) and neutral to the SR leg of the converter (Q_{SR_HS} and Q_{SR_LS} in Figure 2). The two high-frequency SiC legs operate at 65 kHz switching frequency in the interleaving mode, phase shifted by 180°, whereas the two SR legs rectify the AC current according to the detected line voltage.

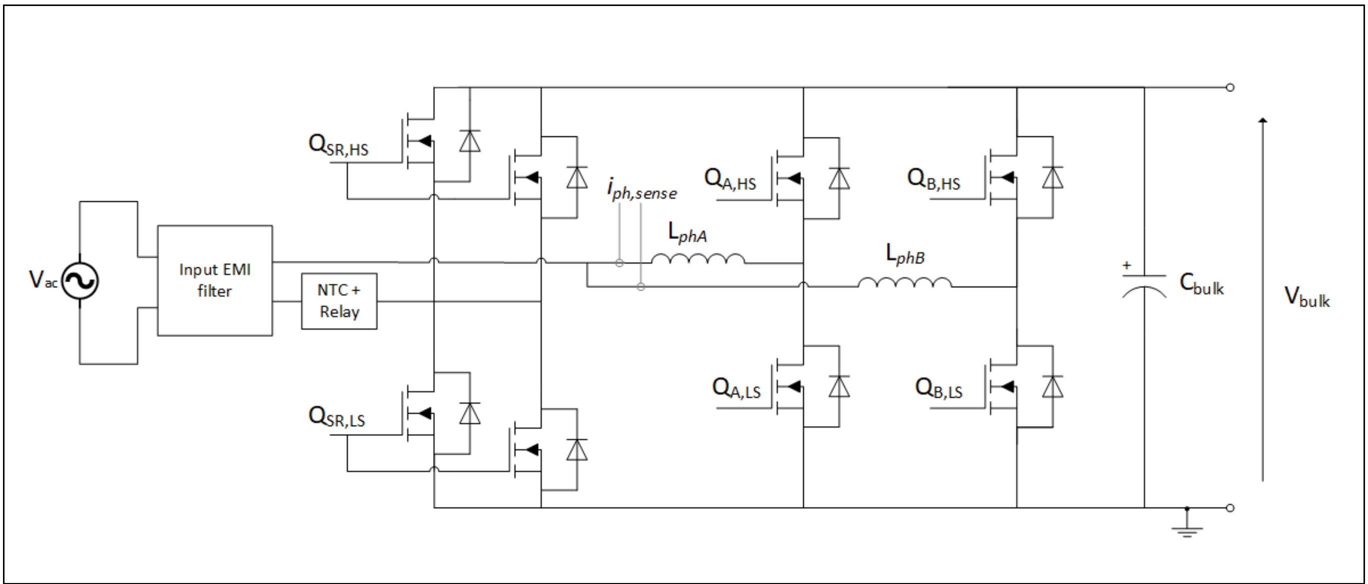


Figure 7 Simplified schematic of the totem-pole AC-DC converter in REF_3K3W_HFHD_PSU

1.4.1 Hardware implementation

The hardware implementation of the PFC is distributed among the PFC power card (PW400003071) hosting the two high-frequency MOSFETs, the LLC power card (PW200003075) hosting the synchronous rectification stage and the main board (M100003074) hosting the two PFC inductors, input line filter, and NTC. Figure 8 shows the main board and a top view of the power daughter cards and their location.

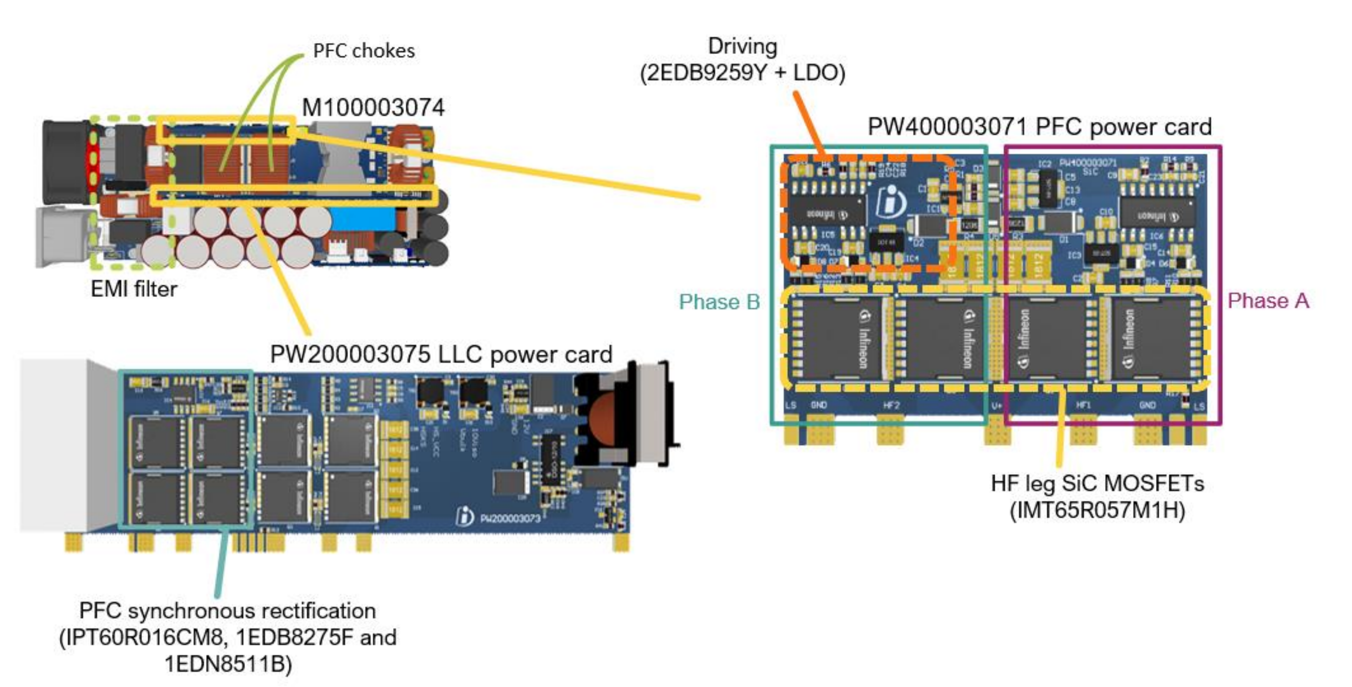


Figure 8 **Hardware implementation of the interleaved totem-pole PFC**

1.4.2 Efficiency and losses

Overall, the AC-DC PFC stage is capable of near-99 percent peak efficiency at 70 percent of the rated load, which remains above 98.8 percent up to full-load. The measured efficiency and the losses of the totem-pole PFC are shown in Figure 9 at both nominal AC line voltage (230 VAC) and at 180 VAC input.

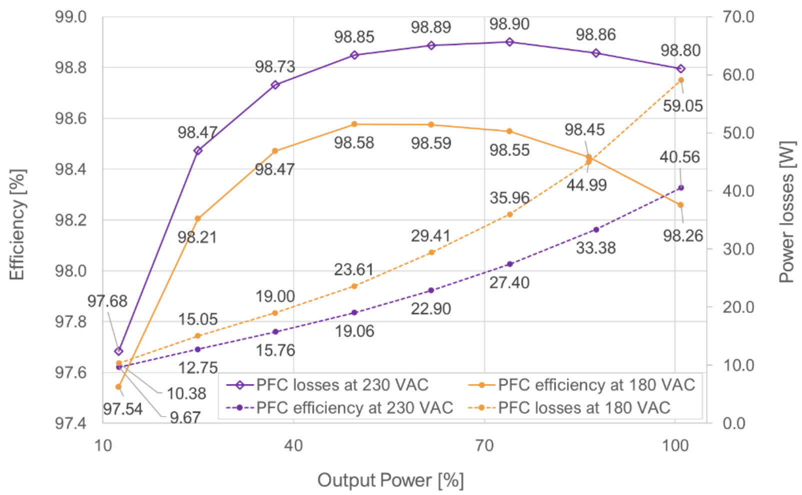


Figure 9 **Efficiency of the PFC**

Figure 10 shows an estimation of the power loss breakdown at 50 percent load for 100 percent load for a 230 V_{AC} input using a CoolSiC™ device with a 57 mΩ on-resistance. The main contributors to losses are the fast-leg boosting switches (CoolSiC™ IMZA65R057M1H) at turn-on as they are the hard-commutated MOSFETs in CCM. The low temperature-dependence of the $R_{DS(on)}$ of CoolSiC™ together with the higher maximum junction temperature T_J [1], reduce conduction loss, especially critical at 180 V_{AC} input voltage when the thermal hotspot of the PSU is the PFC fast-leg card. In this specific design, since the airflow is constrained by the very high power-density of the PSU, CoolSiC™ IMZA65R057M1H with a 57 mΩ on-resistance has been preferred in place of CoolSiC™ IMZA65R072M1H with a 72 mΩ on-resistance to maintain an adequate temperature margin during 180 V_{AC} operation at full-load.

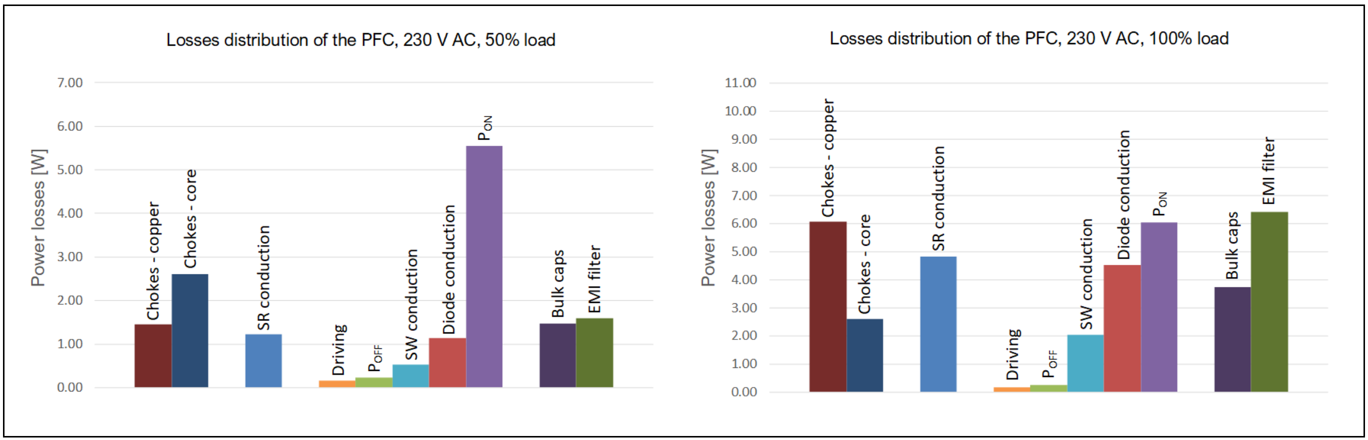


Figure 10 Power loss breakdown of the totem-pole PFC AC-DC stage with a CoolSiC™ device having a 57 mΩ on-resistance

1.4.3 Driving CoolSiC™ and CoolMOS™ in the interleaved TP PFC

To ensure correct operation of the PFC converter, proper operation of the driving stage is crucial. For CoolSiC™ devices, an 18 V_{DC}/0 V_{DC} unipolar driving voltage is used as per the driving voltage recommendations [3]. The bias supplies are initially generated via charge pumping of the flyback 12 V_{DC} output to 24 V_{DC}. The two high-side supplies are generated from the 24 V_{DC} via bootstrapping plus post-regulation, and the low-side is generated via post-regulation to 18 V_{DC}.

The main reason for using this method is that it is simple and cheap to implement. In fact, implementing the bootstrap can generate the high-side gate driver voltage supply by adding only a few components (one high-voltage diode and one resistor) from the low-side gate driver supply. As an example, the bootstrap circuit used in the ILTP PFC with Infineon CoolSiC™ MOSFETs and isolated gate drivers is shown in Figure 11.

Note: The same half-bridge stage can also be driven with a combination of a low-side non-isolated driver plus a high-side isolated gate driver IC.

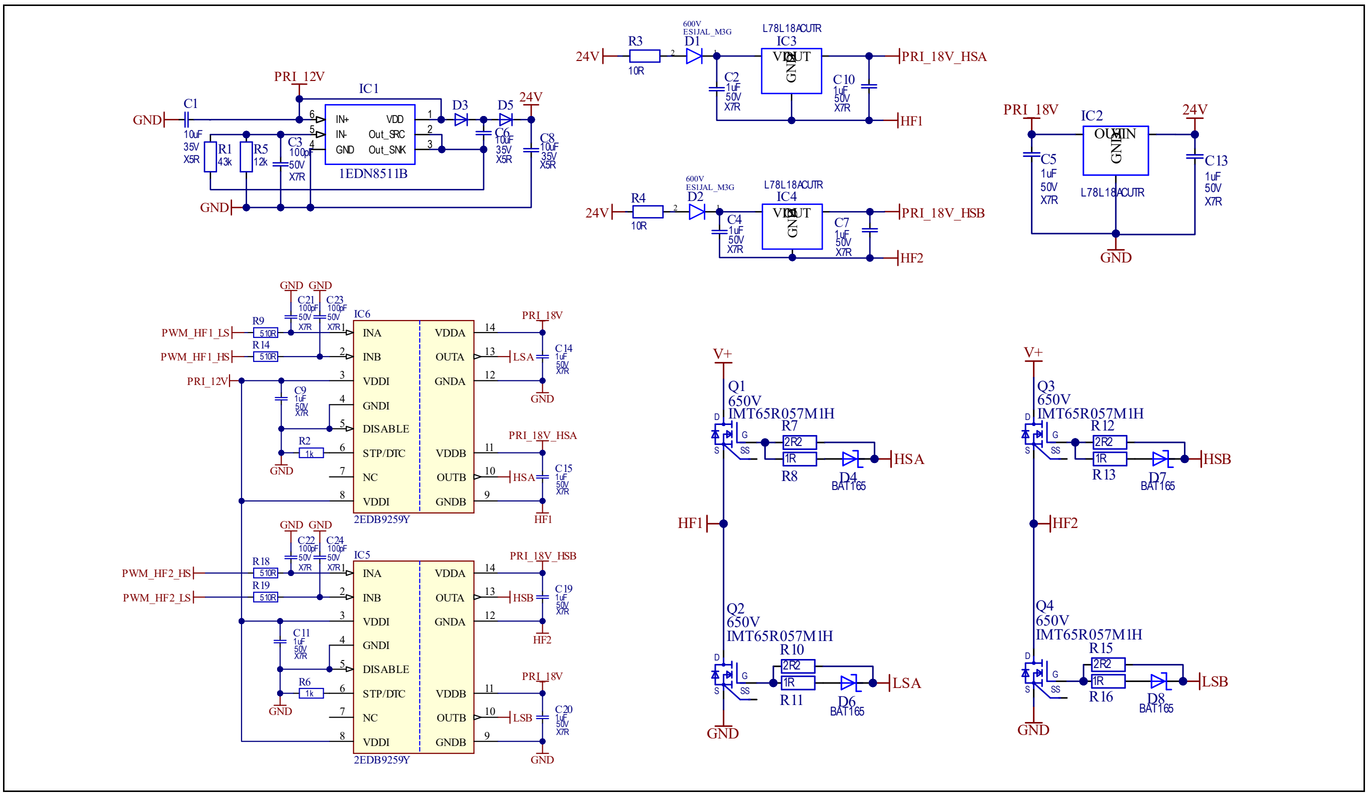


Figure 11 Driving CoolSiC™ with EiceDRIVER™ 2EDN9259Y

SiC MOSFETs are sensitive to gate voltage supply, so reducing the recommended voltage will lead to a channel-resistance increase. Using a bootstrap circuit in the PFC CCM totem-pole topology could generate a modulation of the high-side gate voltage, under some conditions (2.1). Clearly, while the high-side MOSFET device acts as a diode, the gate voltage decreases following the shape of the input AC. When the input peaks, the high-side gate has the minimum voltage and the biggest duty cycle. This leads to an increase in conduction losses in the high-side device when acting as a diode and conducting with the channel. Similarly, when the high-side is the active switch, the gate voltage increases. To overcome this cross-modulation issue, the classic bootstrap is complemented with a low-dropout regulator (LDO) post-regulation stage for the gate-driver bias-supplies. Further information about this approach is extensively discussed in 3.1 of [4].

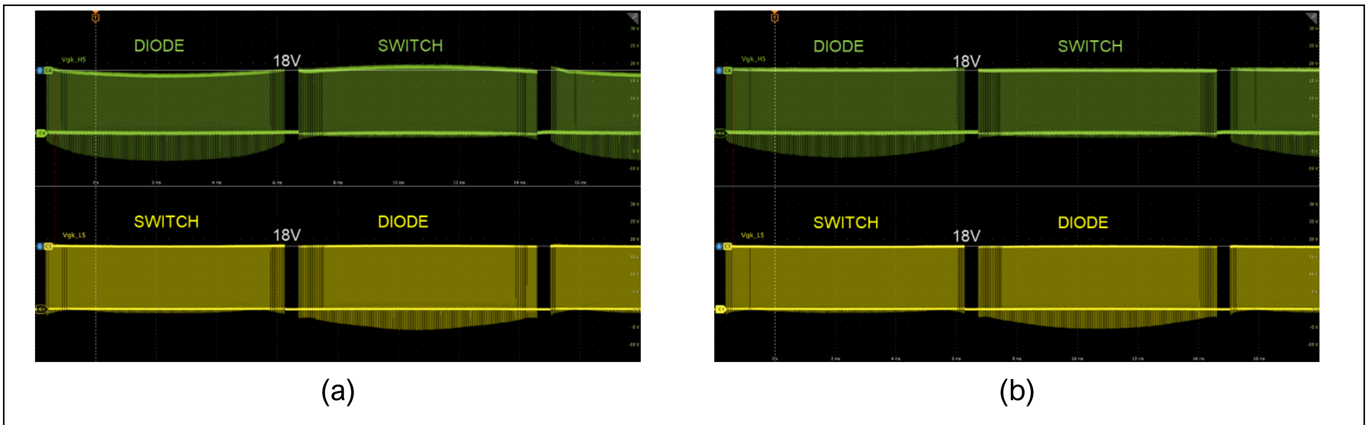


Figure 12 V_{gs} voltages of CoolSiC™ in the high-frequency leg of a totem-pole PFC: (a) Without LDO post-regulation; (b) With post-regulation

[Figure 12](#) shows waveforms with and without LDO post-regulation, with green waveforms being the high-side V_{gs}, and the yellow waveforms being the low-side V_{gs}.

The driving of the CoolMOS™ is shown in Figure 13. A hybrid driving approach with an isolated high-side and non-isolated low-side switch has been adopted [9]. Also, for the four CoolMOS™ synchronous rectification legs that are switching at 50 Hz, a bootstrap approach has been adopted to minimize costs. In this case, proper capacitor dimensioning is required to avoid discharging and breaching the UVLO threshold of the driver.

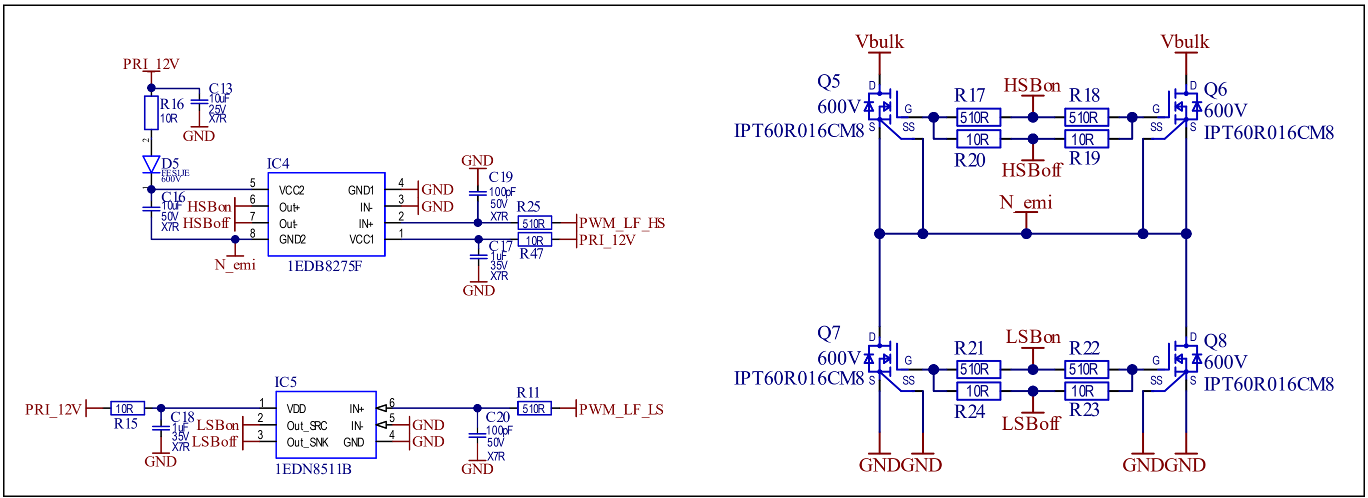


Figure 13 Driving CoolMOS™ with hybrid driving (EiceDRIVER™ 1EDB8275F along with 1EDN8511B)

1.4.4 Signal conditioning for digital control of totem-pole CCM PFC

The interleaved PFC of EF_3K3W_HFHD_PSU implements CCM average current mode control with duty and load feed-forward. Unlike the classic PFC in which the AC voltage is rectified by the diode bridge, in the bridgeless totem-pole PFC converter the inductor current is both positive and negative. In addition, isolation or common-mode rejection is required to measure the inductor current if the control ground is in place in the negative rail of the bulk voltage, as has been traditionally done in the classic PFC. A hall-effect sensor is therefore a good solution for this kind of system.

The output of the hall-effect sensor matches the ADC inputs when supplied with the same voltage – positive and negative currents are measured with the span of the ADC and a shift to half of the ADC range for zero current. The sensor has enough bandwidth to also sense the high-frequency ripple and therefore, the same signal can be used for peak-current limitation and input overcurrent protection (OCP). In case of a lower bandwidth, the hall-effect sensor typically offers an overcurrent detection signal, which could be used for the same purpose.

With respect to the bulk and the LLC input voltage, they are sensed by the PFC controller via a resistive partition as shown in blue in Figure 14 (for simplicity, only the voltage gain is reported). The AC sensing chain is shown in Figure 14 in violet. It is split into positive and negative AC sensing with respect to ground and the two resulting signals are then summed in the analog domain. Lastly, the polarity of the AC input is obtained via comparator, shown in orange.

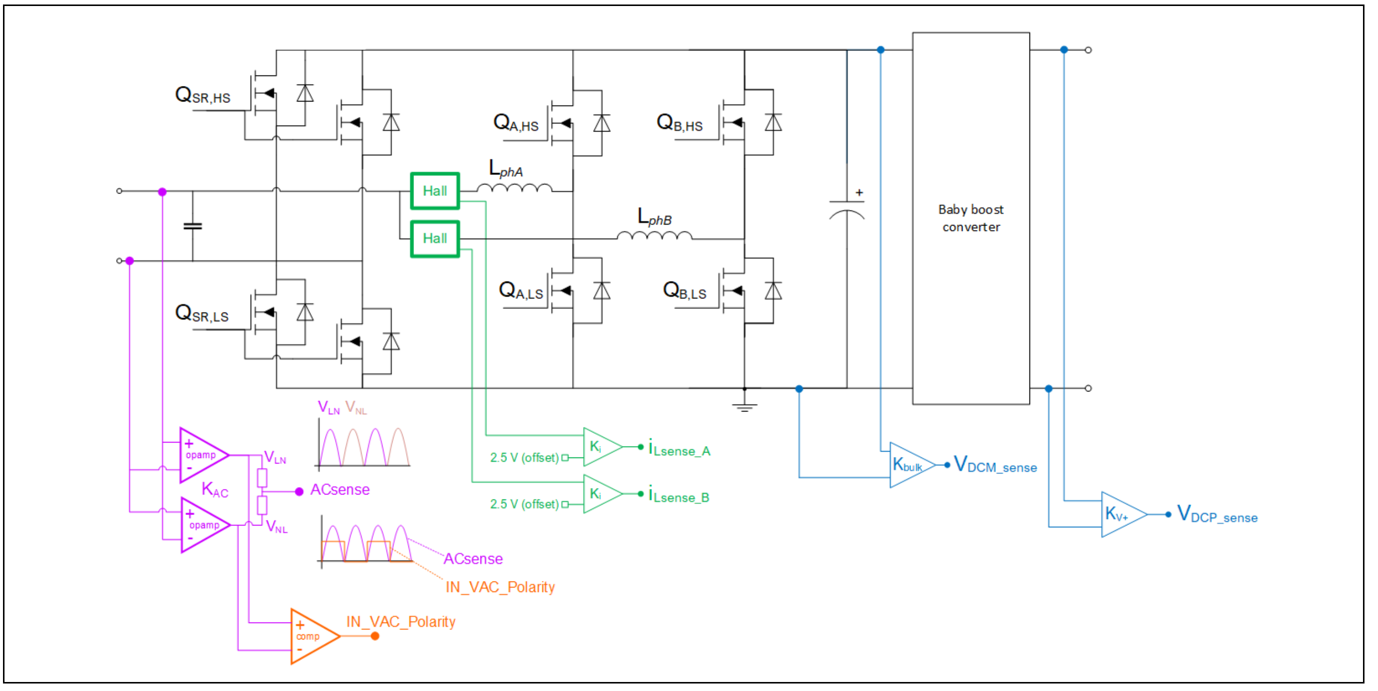


Figure 14 Sensing circuitry required to control the interleaved totem-pole PFC converter with XMC™

Since the AC voltage is used for the current reference generation in the selected average current mode structure, the current reference is a full-wave rectified sinusoidal sequence. However, the current-sense after the ADC is a sinusoidal sequence with offset at half of the ADC spam. Therefore, the ADC result from the current-sense requires that the offset be removed before being rectified according to the AC polarity signal. These two steps, together with extra gain, are implemented by software in the XMC™ controller.

Because of the low amount of bulk capacitance available in REF_3K3W_HFHD_PSU, feed-forward of the PSU load current to the PFC voltage loop was required to ensure smooth response during 10 percent to 100 percent to 10 percent, and 50 percent to 100 percent to 50 percent load jumps with 20 Hz repetition rate, as required per server and datacenter standards. Experimental results for load jump tests are discussed in Section 2.4.1.1.

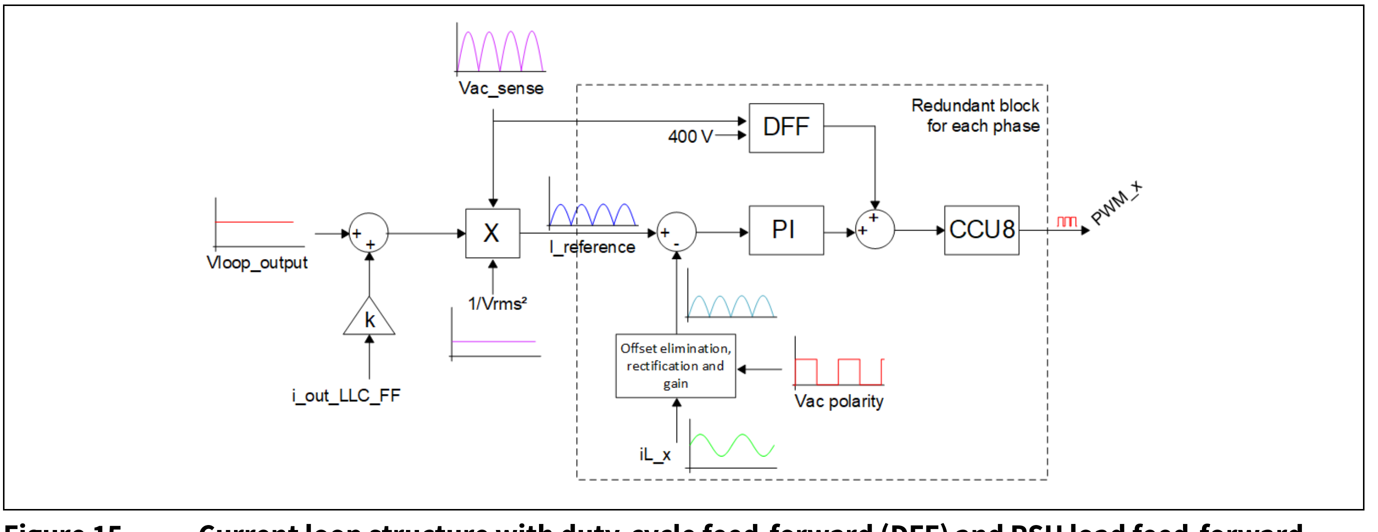


Figure 15 Current loop structure with duty-cycle feed-forward (DFF) and PSU load feed-forward

1.5 Half-bridge LLC converter

As a back-end DC-DC converter, a half-bridge LLC topology with full-bridge rectification has been selected. This conversion stage provides safety isolation and regulates the output from the 400 V bulk voltage. A simplified schematic of the chosen topology is available in Figure 16.

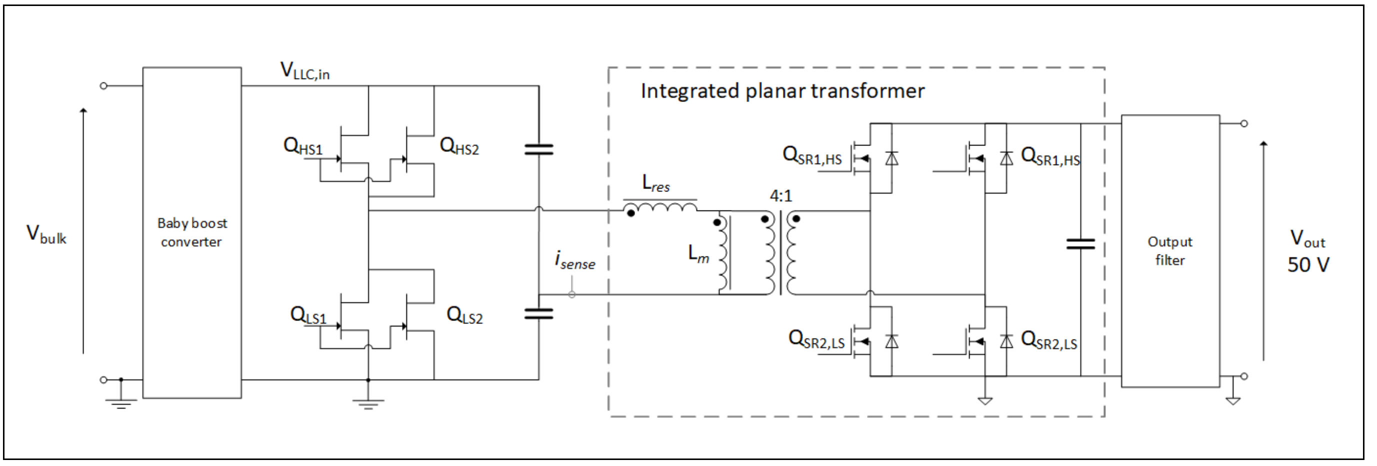


Figure 16 Simplified schematic of the LLC HB DC-DC converter in REF_3K3W_HFHD_PSU

1.5.1 Hardware implementation

The LLC DC-DC converter primary is placed on the LLC power card, which drives the integrated transformer that integrates the secondary-side synchronous rectifiers.

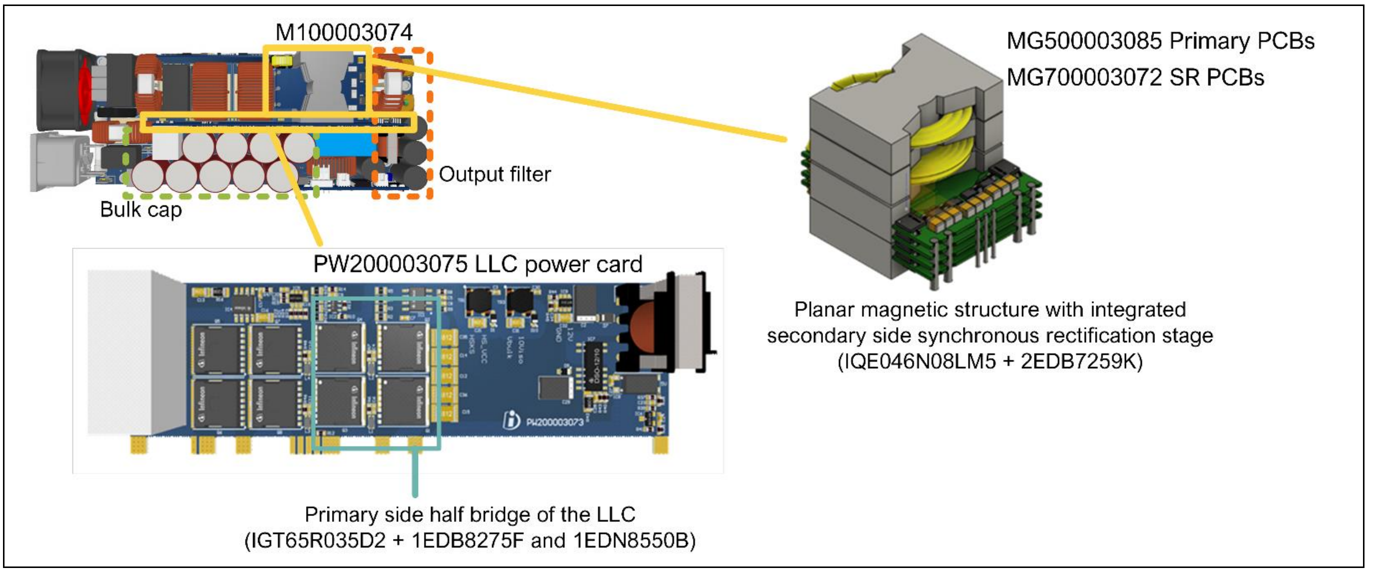


Figure 17 Primary and secondary sides of the LLC converter

1.5.2 Efficiency and losses

The measured efficiency of the half-bridge LLC converter is plotted for 400 VDC nominal input voltage in Figure 18. Efficiency is near 98.5 percent at 50 percent of the rated load and remains around 98 percent at full-load.

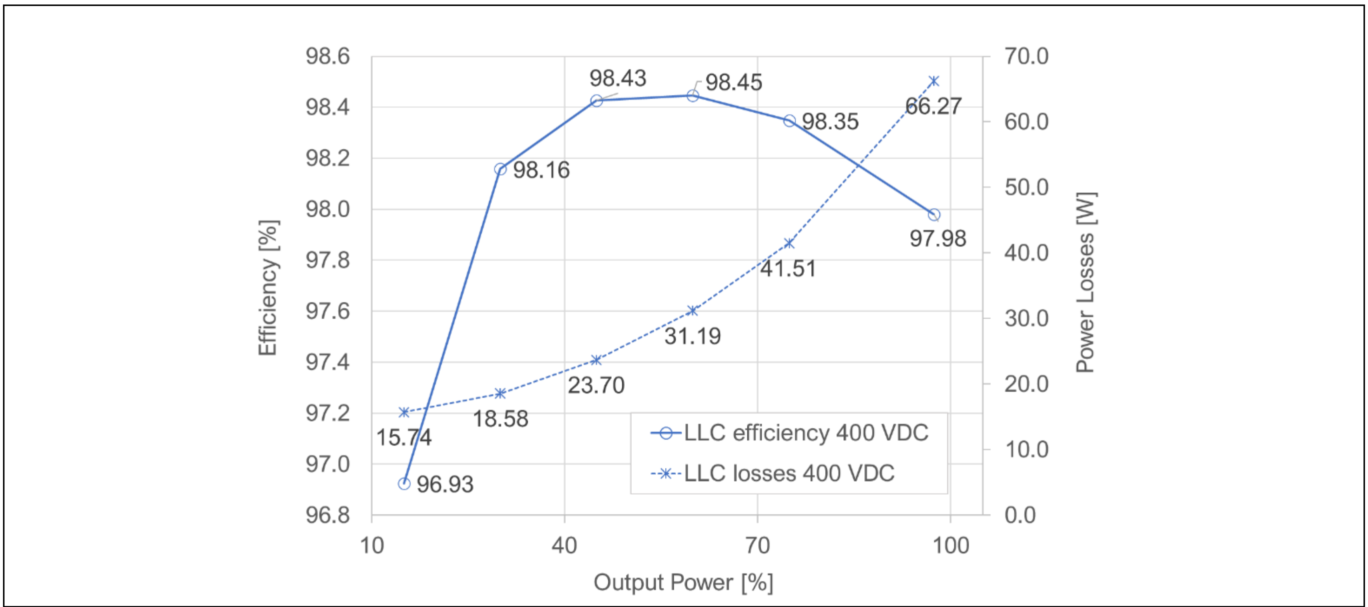


Figure 18 **Efficiency of the LLC DC-DC stage with a CoolGaN™ device having a 35 mΩ on-resistance**

Figure 19 shows an estimation of the breakdown of the power losses for the LLC converter only. The main contributors to power losses are conduction losses of the primary-side, the synchronous rectifiers, and total copper losses of the series and parallel inductance, and of the main transformer itself.

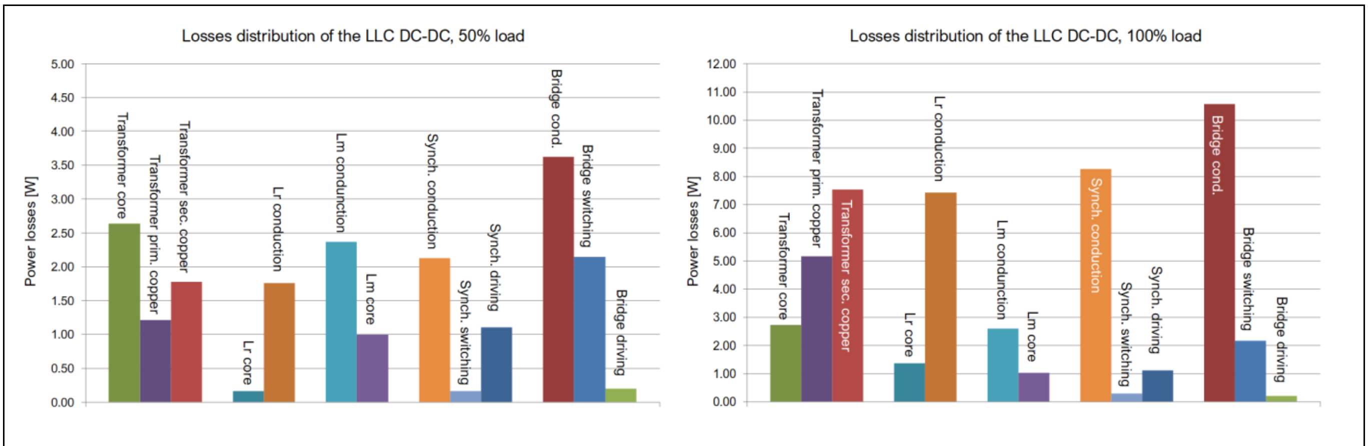


Figure 19 **Power loss breakdown for the LLC DC-DC stage with a CoolGaN™ device having a 35 mΩ on-resistance**

1.5.3 Integrated LLC half-bridge magnetics and SR

One of the advantages of the LLC topology is reusing the leakage inductance of the main transformer as the resonant inductance of the tank and the magnetizing inductance of the transformer as a parallel resonant inductor. However, this compromises the overall efficiency and therefore, the design of REF_3K3W_HFHD_PSU has series and parallel inductors integrated in the main transformer structure to minimize space. Figure 20 shows the cross section of the transformer structure.

It is important to mention that the magnetic structure presented in Figure 20 is key to this design achieving the target efficiency of 98.5 percent (LLC only), integration of the synchronous rectification stage, and the required power density.

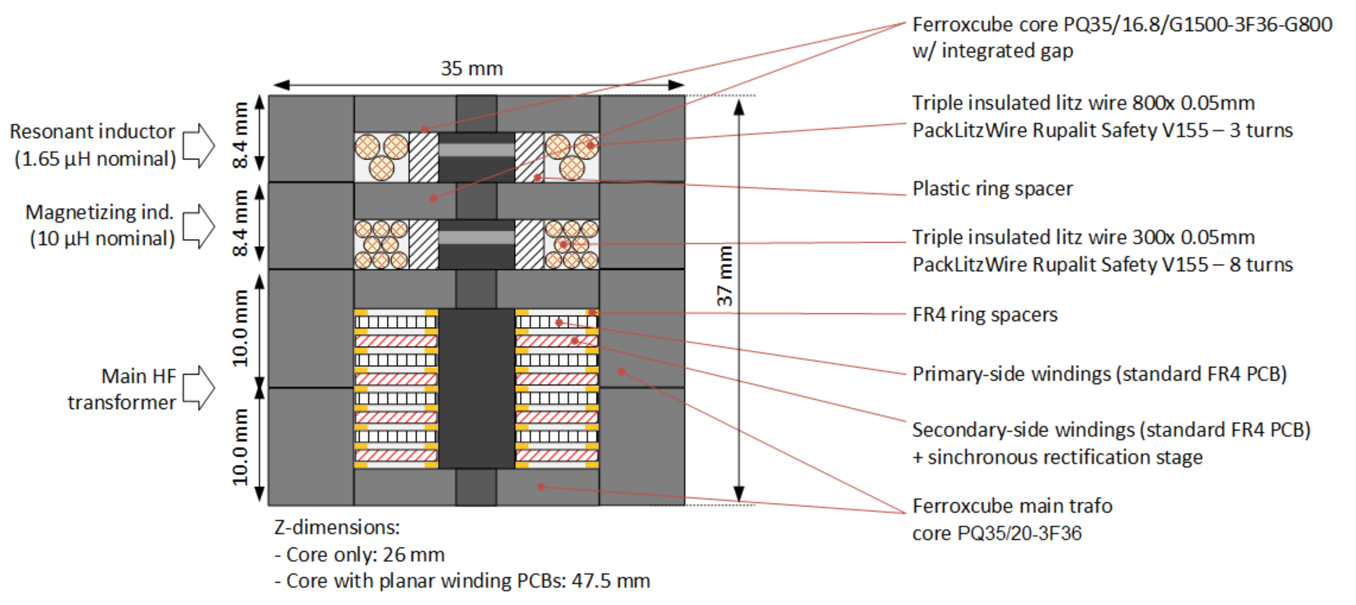


Figure 20 Integrated planar transformer assembly – cross section

The overall size of the full magnetic structure including series and parallel inductors of the LLC converter is 35 mm × 37 mm × 47.5 mm. The magnetic structure adopts two PQ35/20-3F36 cores from Ferroxcube for the main transformer, and two PQ35/16.8/G1500-3F36-G800 cores with integrated gaps from Ferroxcube for the resonant series inductor and the parallel inductor of the LLC converter. The 8:2 main transformer stack uses four primary and four secondary PCBs as shown in Figure 21 with full interleaving to reduce high-frequency copper losses. In between each PCB couple, an FR4 spacer is also inserted to increase the air gap between the windings, consequently, reduce the inter-winding capacitance for each interleaving layer, and keep it constant. It has been measured that the ring spacers between PCBs decrease the inter-winding capacitance from about 140 pF (no spacers) to about 60 pF (with FR4 spacers).

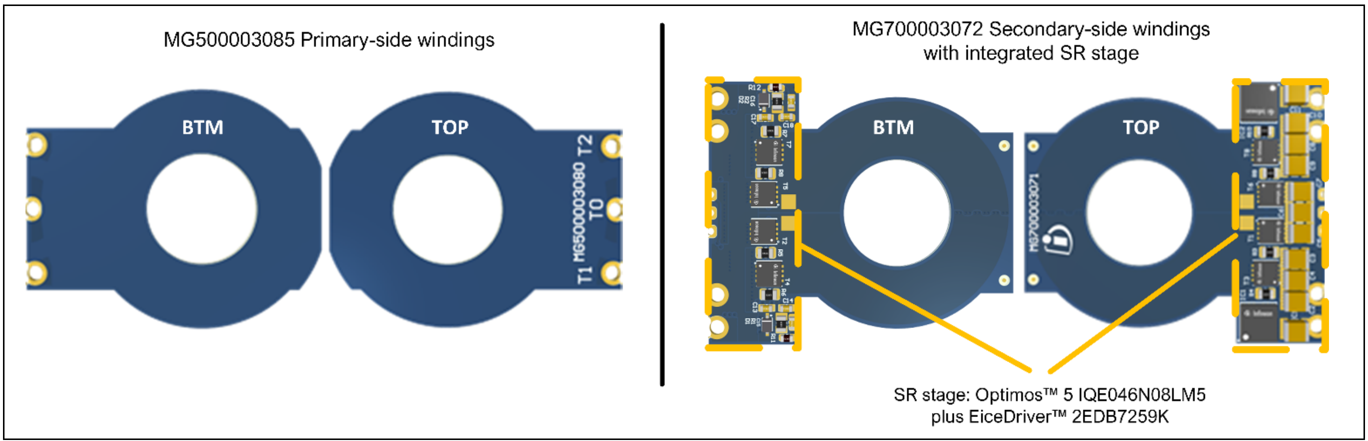


Figure 21 Primary- and secondary-side winding PCBs of the transformer in Figure 20

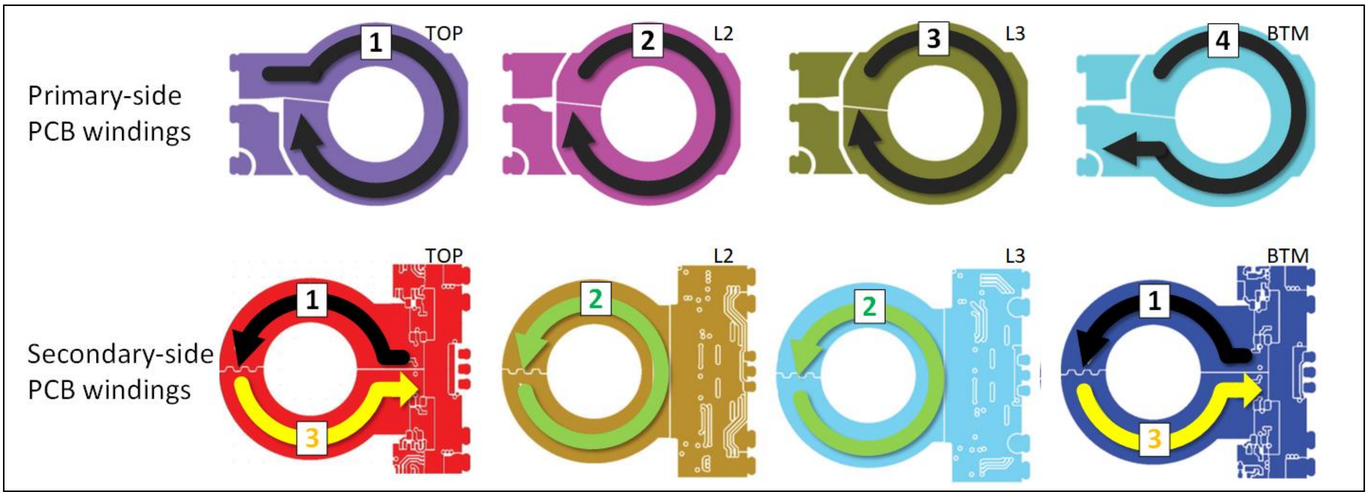


Figure 22 Arrangement of the planar windings in the main transformer

As mentioned previously, both the series and parallel inductors use cores with distributed gaps to reduce losses caused by stray magnetic fields. Litz wires are employed to reduce AC resistance and high-frequency copper losses. The series resonant inductor uses three turns of 800 strand 0.05 mm triple-insulated wire, and the parallel inductor uses eight turns of 300 strand 0.05 mm, both Rupalit Safety V155 from PackLitzWire. This results in the overall height of the full magnetic structure being only 37 mm, enabling it to fit in the 40 mm 1U maximum height limit according to the standards.

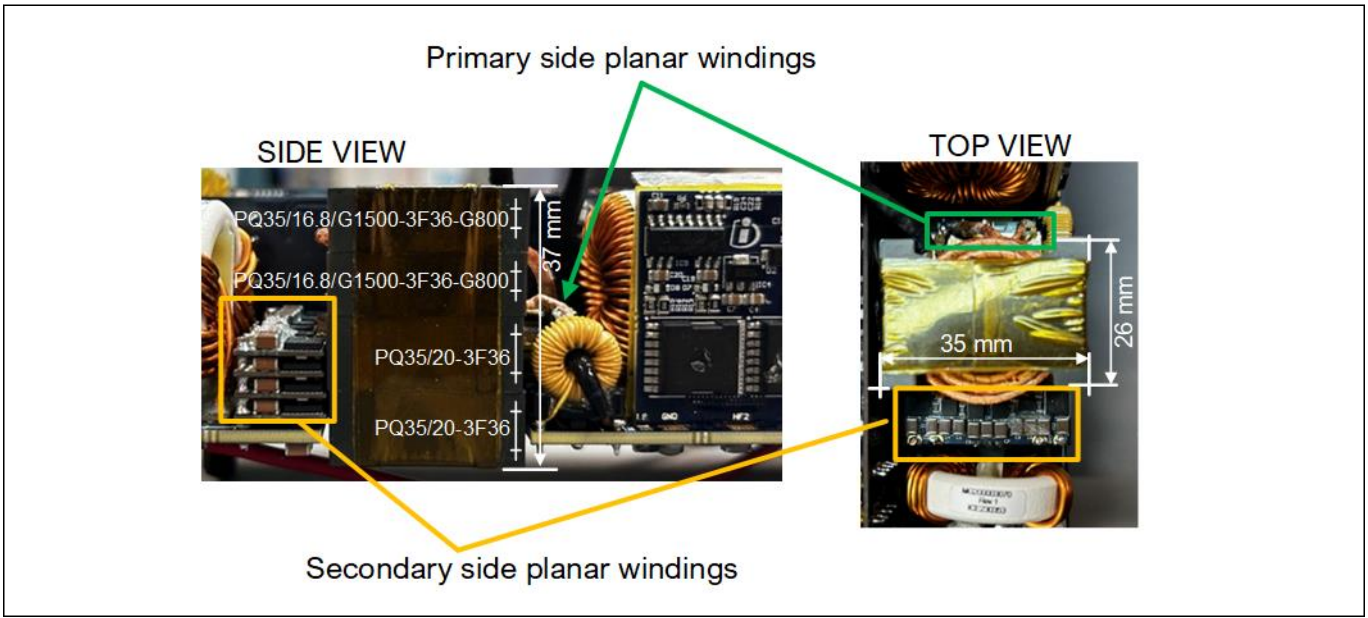


Figure 23 Integrated planar transformer assembly – picture of an assembled prototype

1.5.4 Driving CoolGaN™ and OptiMOS™ in the LLC converter

The primary-side of the LLC converter uses four CoolGaN™ GIT devices, each having a 35 mΩ on-resistance in TOLL package (CoolGaN™ IGT65R035D2), with both high and low sides having two devices in parallel. To drive the CoolGaN™ devices efficiently with paralleling, a common mode (CM) choke is suggested in series with the gate-loop in order to increase CM impedance without affecting the differential mode (DM) impedances, which could affect the driving loop. For this purpose, four CM chokes from Bourns (SRF2012-361YA) have been used, as shown in Figure 24. Further information about GaN paralleling, see [6].

The GaN HB primary leg of the LLC does not require isolation since it is already implemented with ISOFACE™ digital isolators (see Section 1.5.5) [7]. For this reason, hybrid driving is employed to ensure high CMTI, flexible placement, and a lower overall impedance due to gate-loop optimization. Further information about hybrid driving for CoolGaN™ can be found in [7]-[10].

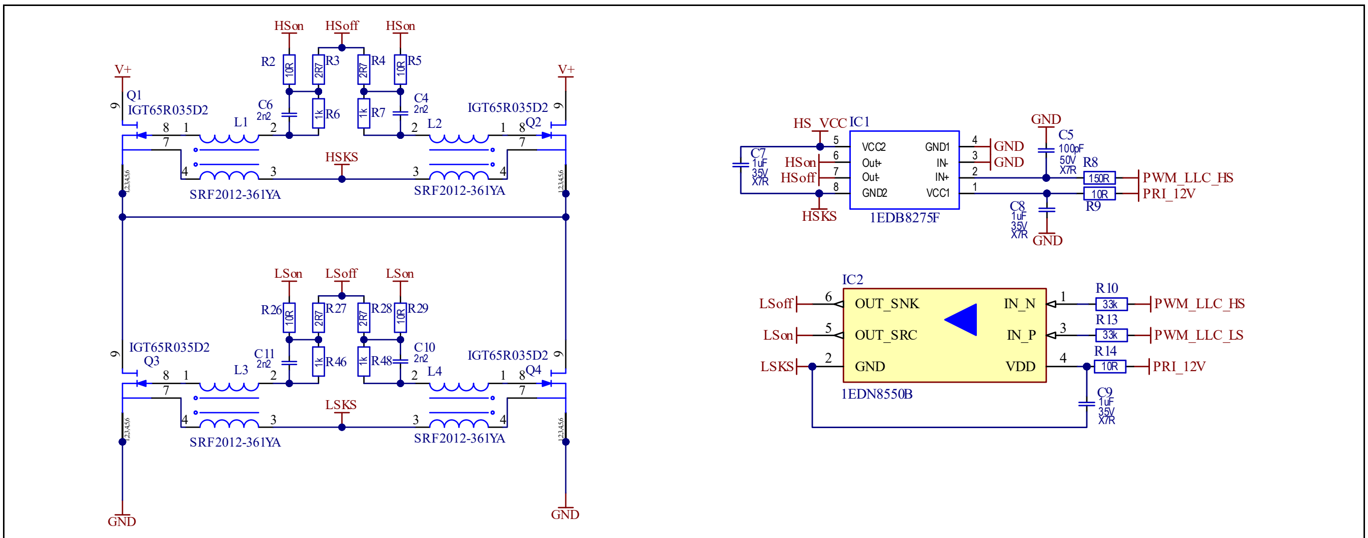


Figure 24 Driving CoolGaN™ with hybrid driving (EiceDRIVER™ 1EDB8275F with 1EDN8550B)

For the bias supply of the OptiMOS™ MOSFETs on the secondary-side, a bootstrapped solution with a 5 V_{DC} bias is used as shown in Figure 25. Because of the space constraints, EiceDRIVER™ 2EDB7275K in a 5 mm × 5 mm package is used, which exactly fits the small space available on the secondary board stacked in the transformer structure (see Figure 21).

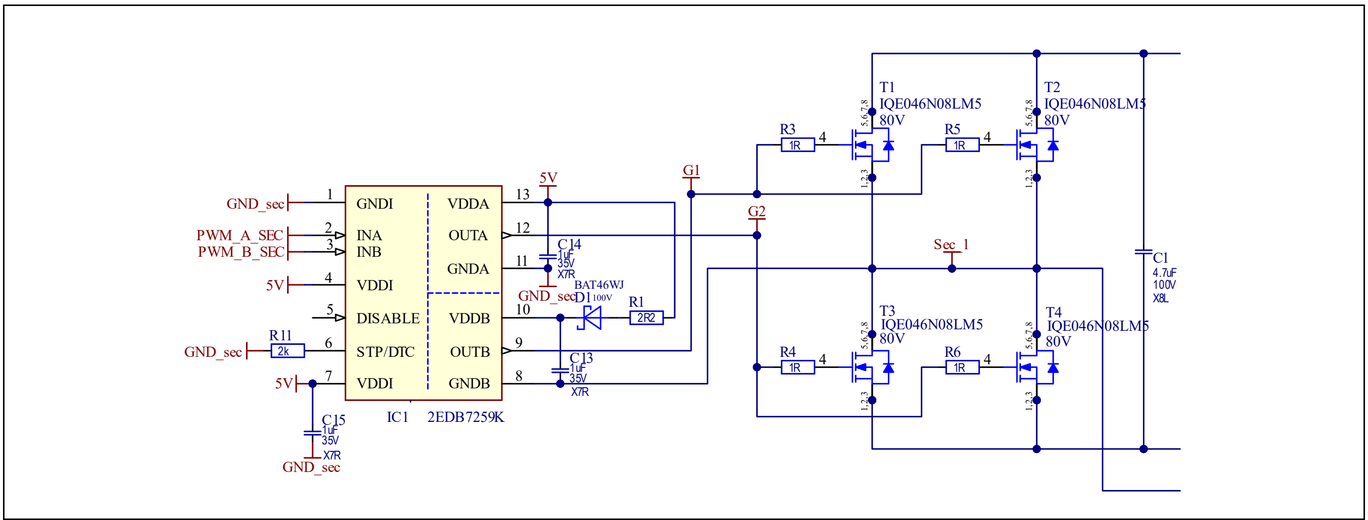


Figure 25 Driving OptiMOS™ with EiceDRIVER™ 2EDB7259K

1.5.5 Isolation partitioning

The isolation partitioning is implemented on the control board with the ISOFACE™ 4DIR1400H digital isolator. The isolator is based on the coreless transformer technology and enables robust data transmission as well as safe behavior. Each side of the digital isolator can be independently supplied with any voltage between 2.7 V_{DC} and 6.5 V_{DC}. In this case, both primary and secondary sides are supplied with 3.3 V_{DC}, as shown in the schematic (see Figure 26).

Compared to similar devices, ISOFACE™ 4DIR1400H offers a higher reliability (VISO = 5700 V_{RMS} according to UL 1577) and high CMTI >100 V/ns. Input pull-down resistors allow for a default and defined startup state of the signals, which is highly recommended when transferring PWM signals. A low propagation delay and a precise timing accuracy minimize deadtime and consequently achieve a high system efficiency. An internal deglitch-filter also detects and bypasses any glitch on the input side with a pulse duration <10 ns, preventing the transfer of unwanted noise from the primary-side to the secondary-side and vice versa.

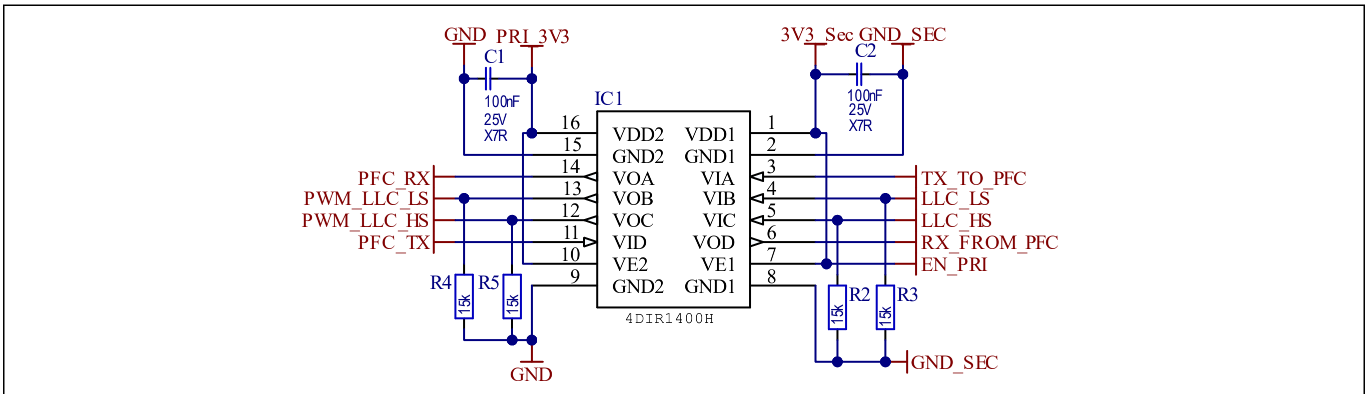


Figure 26 Isolation of the UART and PWM signals between primary and secondary on the control card via ISOFACE™ 4DIR1400H

Eventually, the improved delay performance of the ISOFACE™ 4DIR1400H compared to similar competitor parts allows for an increased timing budget to improve the safety margin or reduce deadtimes. Table 2 shows a comparison of the timing performance between ISOFACE™ 4DIRx40xH product family and equivalent competitor part. Further information about designing with Infineon ISOFACE™ digital isolators can be found in [9].

Table 1 Timing specification of ISOFACE™ 4DIRx40xH vs competitor parts

			ISOFACE™ 4DIRx40xH			Equivalent competitor part		
Symbol	**Parameter**	**Unit**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**
$t_{PD,on}$ $t_{PD,off}$	Input-to-output propagation delay	ns	22.0	26.0	33.0	50.0	75.0	100.0
$\Delta t_{PD,p\text{-}p}$	Part-to-part propagation delay mismatches	ns	–	–	3.0	–	–	–
$\Delta t_{PD,ch\text{-}ch}$	Codirectional channel-to-channel propagation delay mismatch	ns	–	–	3.0	–	–	50.0
PWD	Pulse width distortion	ns	–	–	3.5	–	–	40.0
$t_{PW,min}$	Minimum pulse width [ns]	ns	8.0	12.5	15.0	1000.0	–	–

1.6 Baby-boost stage to extend hold-up time

To have a significant improvement in the power density, a possible viable and widely accepted approach is to implement a reduction of the bulk capacitance. Indeed, under steady-state conditions, the converter can operate with a lower bulk capacitance provided that the 100 Hz ripple of the bulk voltage keeps below the maximum voltage rating of the components, the maximum RMS current can still be handled by the remaining bulk capacitors and the converter still meets the requirements in terms of load transients.

Overall, two criteria need to be satisfied: the total PFC output AC current stress must be lower than the maximum RMS current that the capacitor bank can handle, and the capacitance value must be high enough to:

- Avoid the bulk voltage to exceed the voltage rating (usually capacitors are limiting the voltage stress)
- Allow the PFC stage to operate with the required power factor and total harmonic distortion (e.g., minimum steady-state bulk voltage coming too close to the V_{AC} peak at the input)
- Supply the LLC converter for 10 ms at full output power (3.3 kW) during AC line dropout (ACLCDO)

In a standard server power supply with 3.3 kW maximum nominal output power, assuming average ($V_{bus,nom}$) and minimum bulk voltage ($V_{bus,min}$) being 410 V_{DC} and 395 V_{DC} respectively during steady-state operation at full-load, and minimum bulk voltage during LCDO ($V_{bus,LCDOmin}$) being 360 V_{DC} as in Figure 27, the minimum capacitance required to achieve the 10 ms hold-up time is $2\,P_{out,max}\,t_{HUP}/[V_{bus,min}^2 - V_{bus,LCDOmin}^2]$ which results in around 2.5 mF total capacitance.

In the case of REF_3K3W_HFHD_PSU, by allowing the $V_{bus,LDCOmin}$ to go to a voltage as low as 290 V_{DC}, the amount of capacitance required to continue providing full-load current is in the 900 µF range, which is far lower than the 2.5 mF estimated above, enabling higher power density.

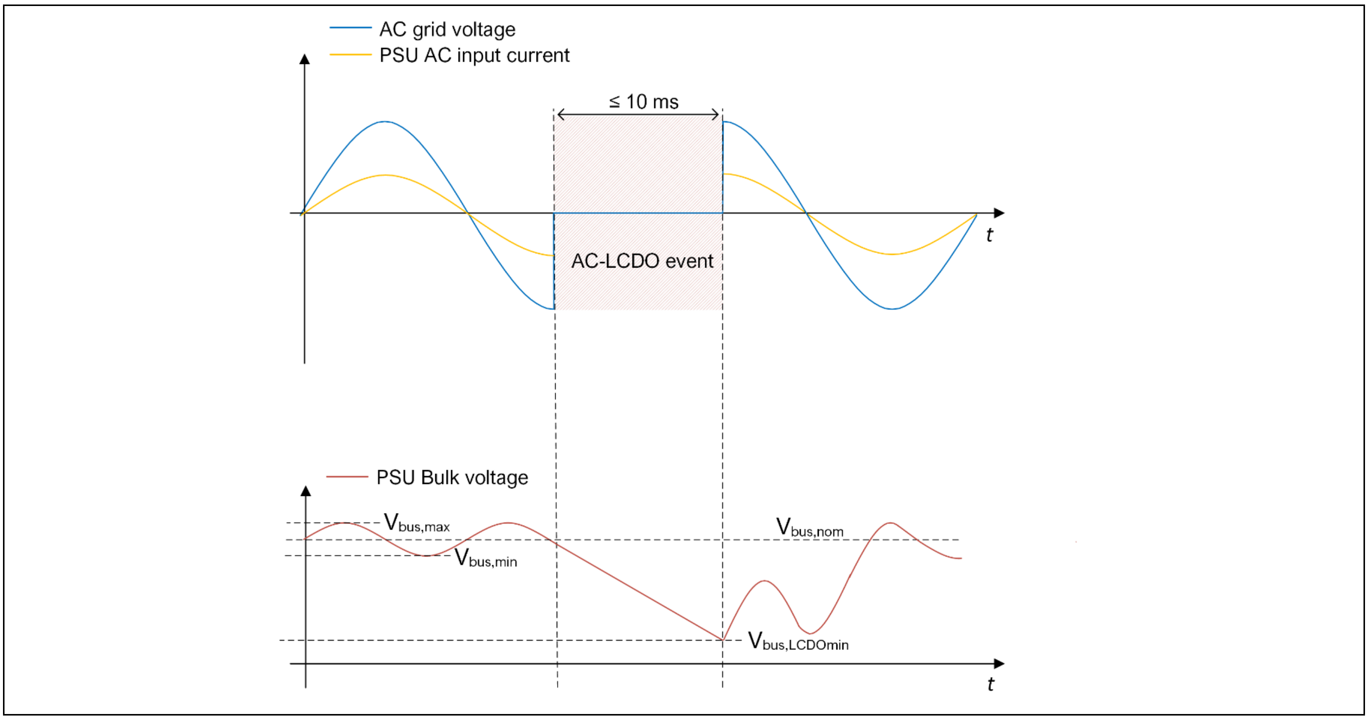


Figure 27 Simplified waveforms of the AC voltage, AC current and bulk voltage during a 10 ms LCDO event

Figure 28 shows an excerpt of a schematic of the baby-boost converter implemented in REF_3K3W_HFHD_PSU, where V_{bulk} is the bulk voltage (input of the baby-boost converter), and V+ is the input voltage of the LLC DC-DC back-end stage (output of the baby-boost converter).

During an ACLDO event, the static switch Q3 disconnects the V+ and the V_{bulk} rails, and as soon as an undervoltage is detected together with absence of grid voltage, the baby-boost starts operating to bring the V+ voltage back to the nominal value allowing a deeper discharge of the bulk cap voltage.

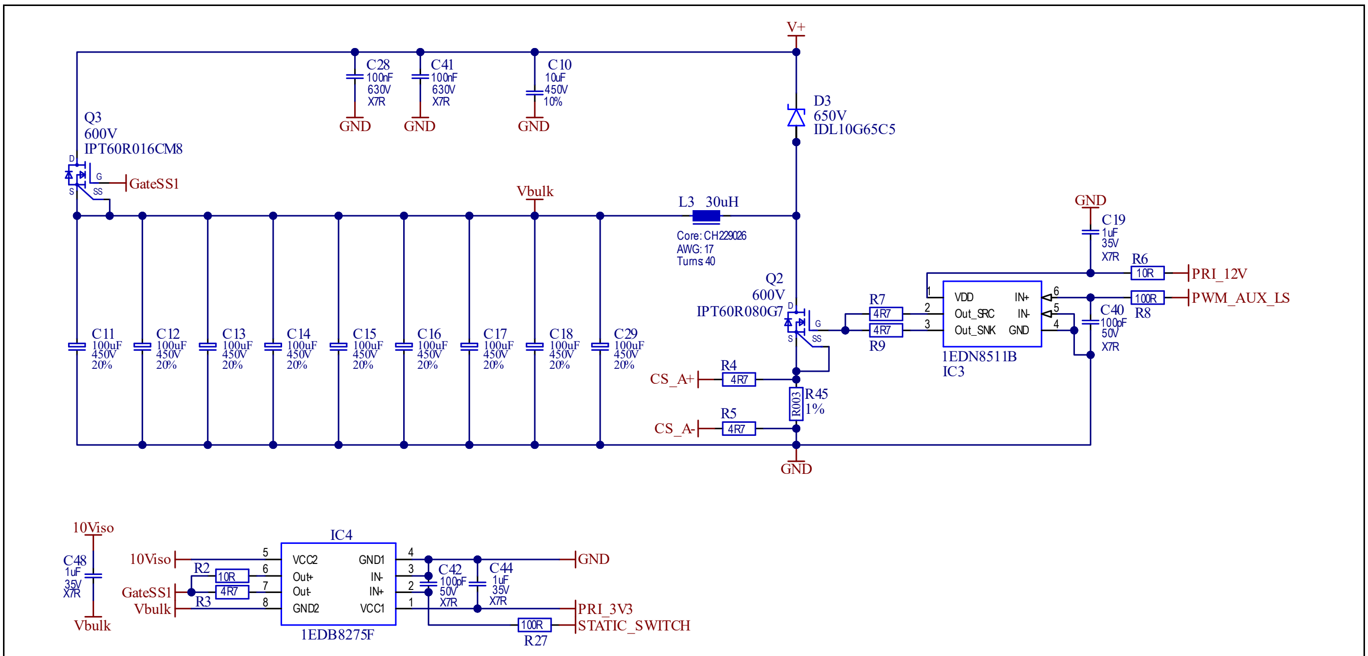


Figure 28 Schematic of the baby-boost circuity on the main board to comply with ACLDO specs

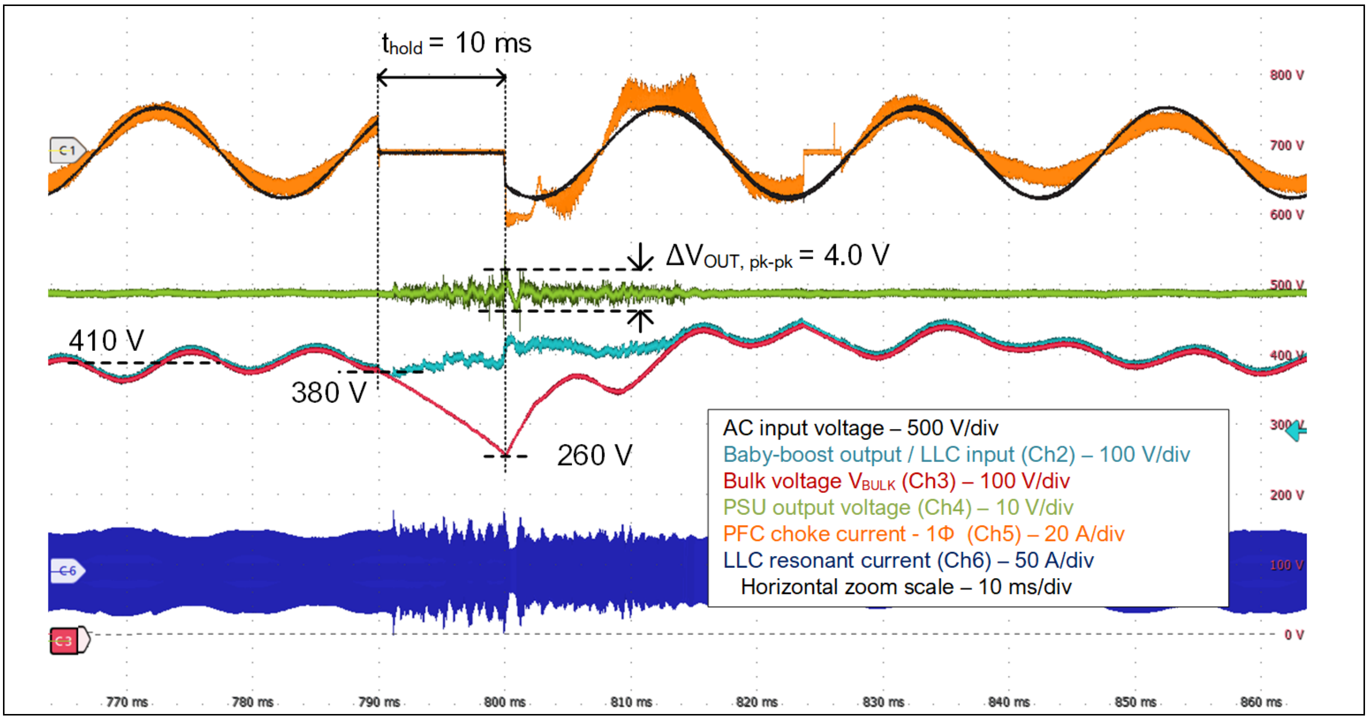


Figure 29 Baby-boost operation during ACLDO event at 100 percent load

2 Experimental results

2.1 Power supply unit specifications

This chapter presents the specifications, performance, and the behavior of the PSU for each single block, and for the overall power supply unit. Table 2 shows the required performance and specifications under several steady-state and dynamic conditions.

Table 2 Summary of specifications and test conditions for the 3300 W PSU

Test	Conditions	Specification
Input voltage V_{AC}	–	180 V_{AC} to 275 V_{AC}
Output voltage V_{DC}	Input 230 V_{AC} at 50 Hz	50 V_{DC} nominal
Output power	Input 180 V_{AC} to 275 V_{AC}	3300 W
Steady-state ripple (max.)	–	± 500 mV peak-to-peak max.
Efficiency test (full PSU)	Input 230 V_{AC} at 50 Hz 30% to 100% of full-load	97.4% peak
		96.5% min.
	Input 230 V_{AC} at 50 Hz 10% to 30% of full-load	94.0% min.
iTHD (max.)	230 V_{AC} at 50 Hz; 5-10% load	15%
	230 V_{AC} at 50 Hz; 10-30% load	10%
	230 V_{AC} at 50 Hz; 30-100% load	5%
Power factor	30% to 100% load	0.98 min.
Dynamic response (output voltage overshoot)	10% to 50% load; 20 Hz; 1 A/µs	0.5 V max.
	10% to 90% load; 20 Hz; 1 A/µs	1.0 V max.
Hold-up time	100% load	>10 ms.
Overcurrent protection (OCP)	Shut down and latch	>65 A
Overvoltage protection (OVP)	PFC bulk voltage	440 V_{DC}
Undervoltage protection (UVP)	PFC bulk voltage	330 V_{DC} in LCDO conditions
AC Line cycle dropout (LCDO)	100% load	10x [10 ms dropout, 100 ms interval]
Brown-out	AC voltage	180 V_{AC} on, 176 V_{AC} off

2.2 Steady-state performance and waveforms

2.2.1 PSU efficiency and power losses

Figure 30 shows the efficiency measurements for steady-state operation of the full PSU at different AC voltages. The efficiency measurements have been obtained with a WT3000 power analyzer with 5 kHz input and no output line filters at 50 Hz line voltage, and do not include fan power consumption.

Note: Due to production and measurement tolerances, variations of ±0.2 percent could be observed.

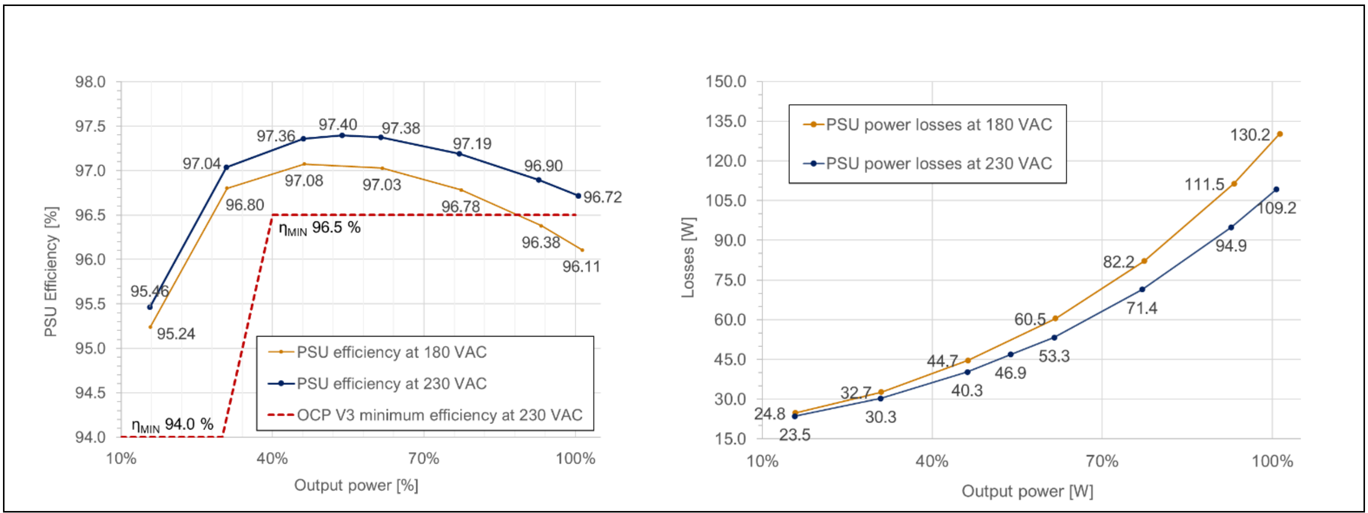


Figure 30 **Measured efficiency and power losses of REF_3K3W_HFHD_PSU (no fan) for different input line voltages at 50 Hz, with comparison to minimum OCP efficiency targets**

Figure 31 shows the efficiency measurements for steady-state operation including fan power consumption. Fan speed is not optimized for minimum power losses at the peak efficiency point.

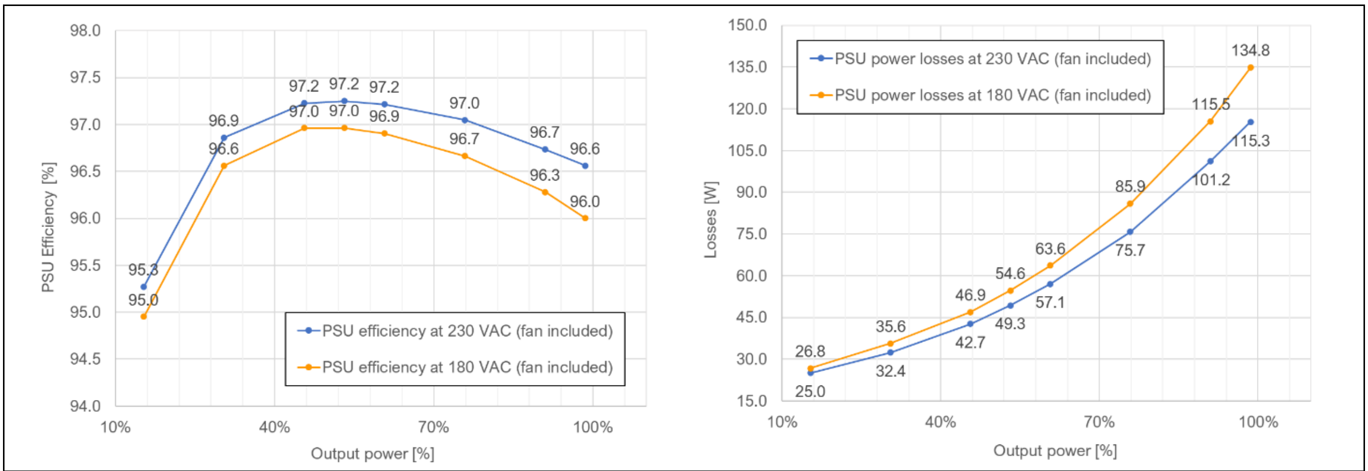


Figure 31 **Measured efficiency and power losses of REF_3K3W_HFHD_PSU (with fan) for different input line voltages at 50 Hz**

2.2.2 Output and bulk voltage ripple

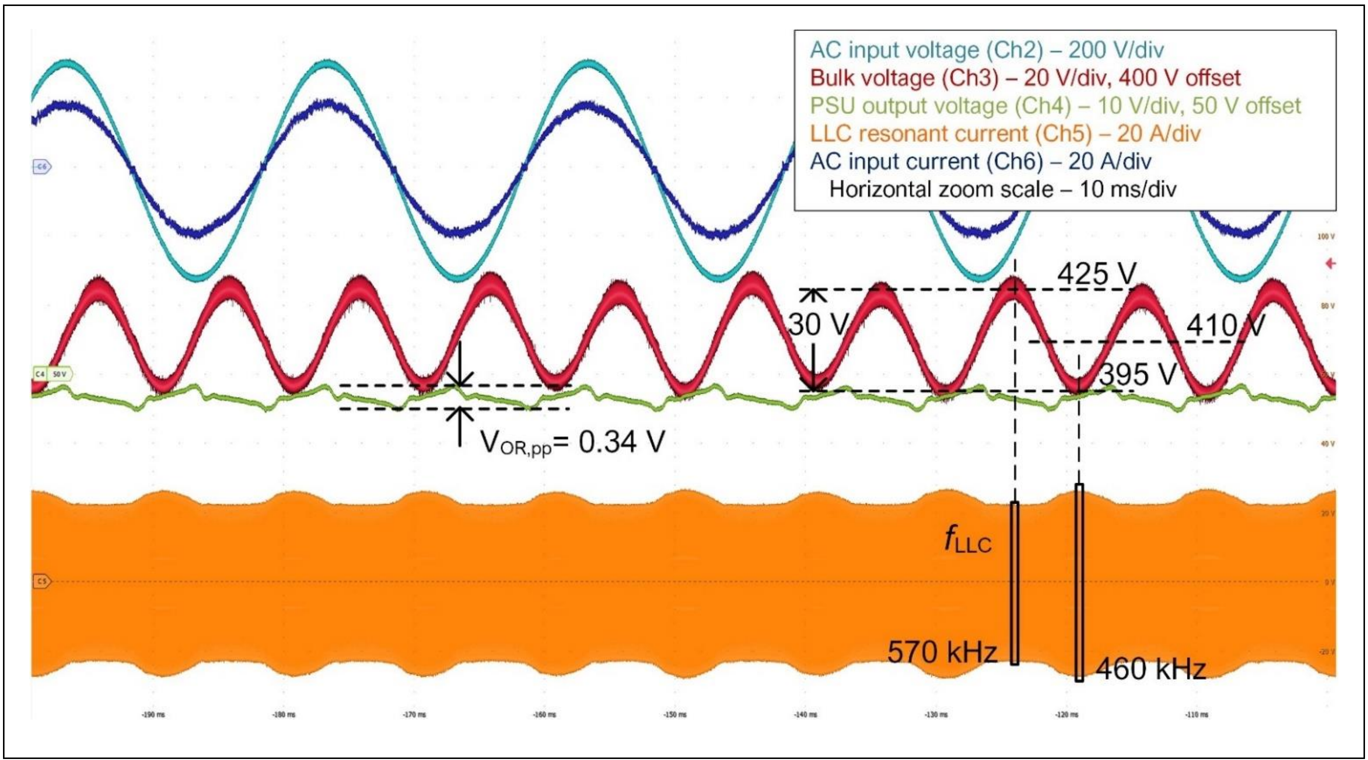


Figure 32 Output voltage ripple for 100 percent load conditions

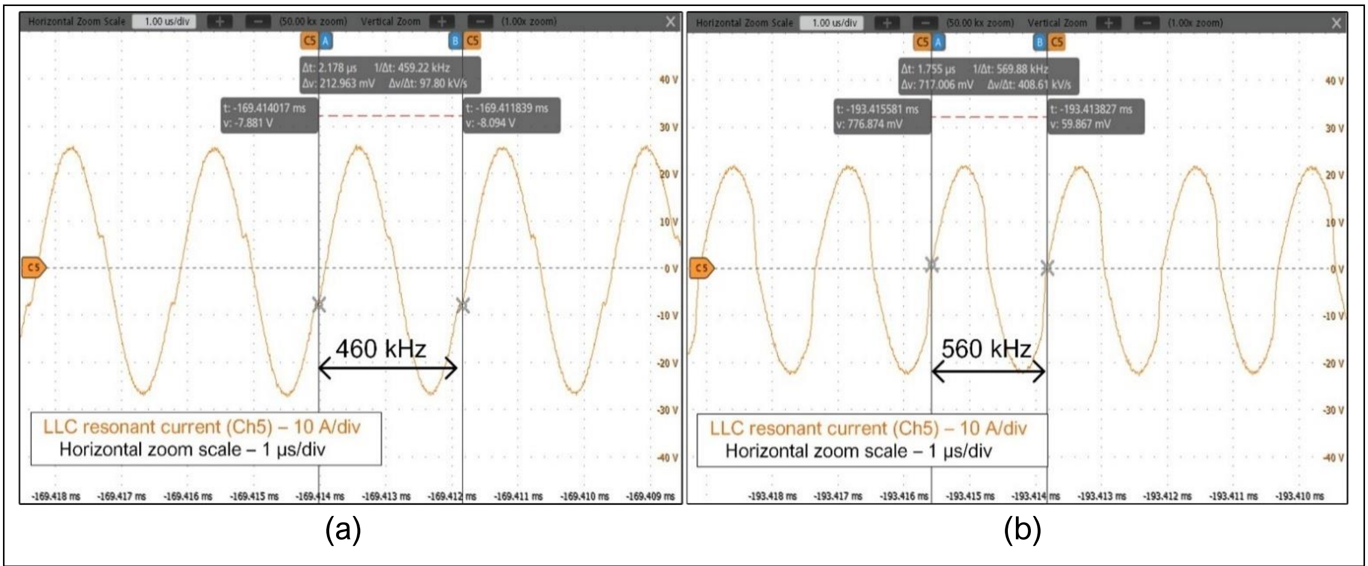


Figure 33 (a) LLC Resonant current at full-load, steady-state for maximum; (b) minimum bulk voltage

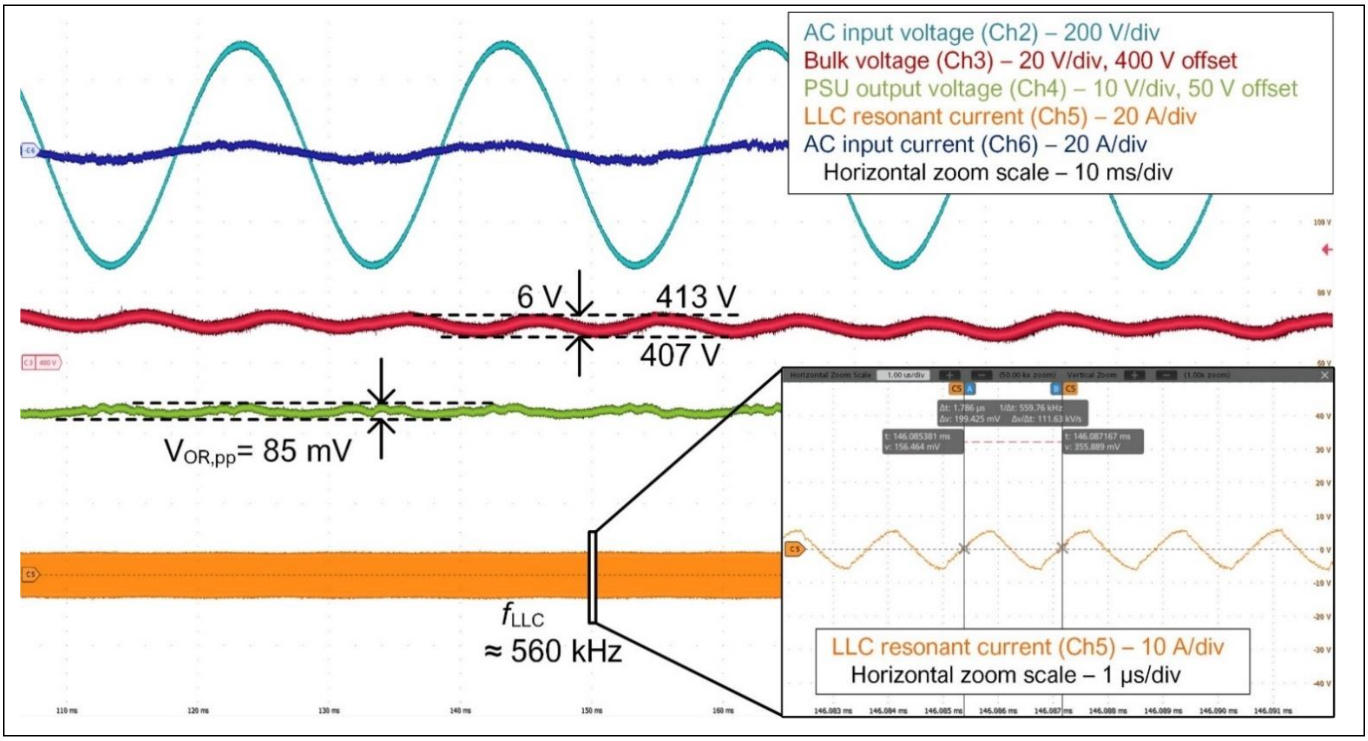


Figure 34 Output voltage ripple for 10 percent load conditions

2.2.3 PSU startup

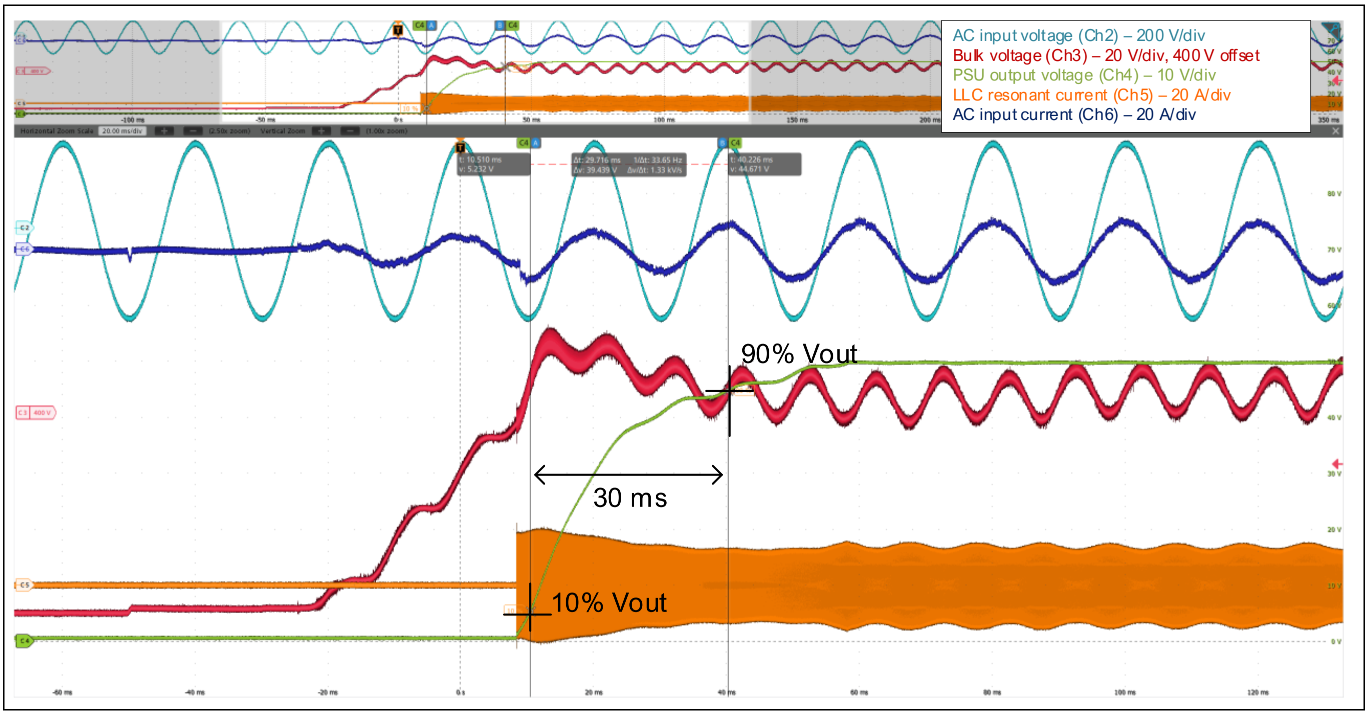


Figure 35 PSU startup at 50 percent output load

2.2.4 Interleaved totem-pole PFC

2.2.4.1 Steady-state performance of the PFC conversion stage

Figure 36 shows the efficiency measurements for steady-state operation of the PFC only at different AC voltages. The efficiency measurements have been obtained with a WT3000 power analyzer with 5 kHz input and 10 kHz output line filters at 50 Hz line voltage, and do not include fan power consumption.

Note: Due to production and measurement setup tolerance, worst case efficiency variations of ±0.2 percent maximum could be observed.

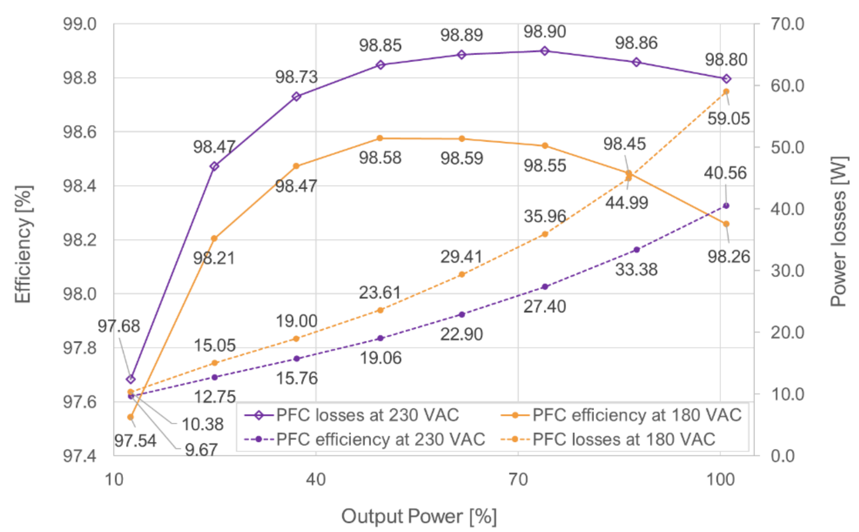


Figure 36 **Measured efficiency of the PFC stand-alone at different RMS input voltage and 50 Hz (no fan)**

Figure 37 depicts the total input current harmonic distortion (iTHD) and power factor measured at 230 VAC and 180 VAC line voltages at 50 Hz. The iTHD and PF measurements have been performed with the full PSU operating in steady state conditions.

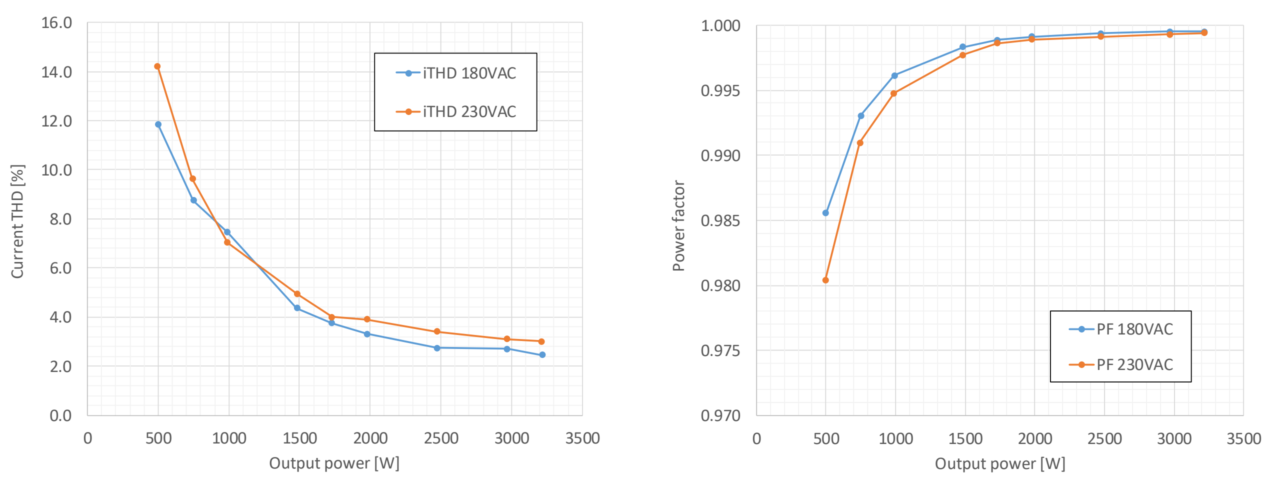


Figure 37 **(a) Measured iTHD; (b) PF at different RMS voltages for 50 Hz high-line 230 V_{AC} and 180 V_{AC} line voltage**

2.2.5 PFC waveforms and zero crossing

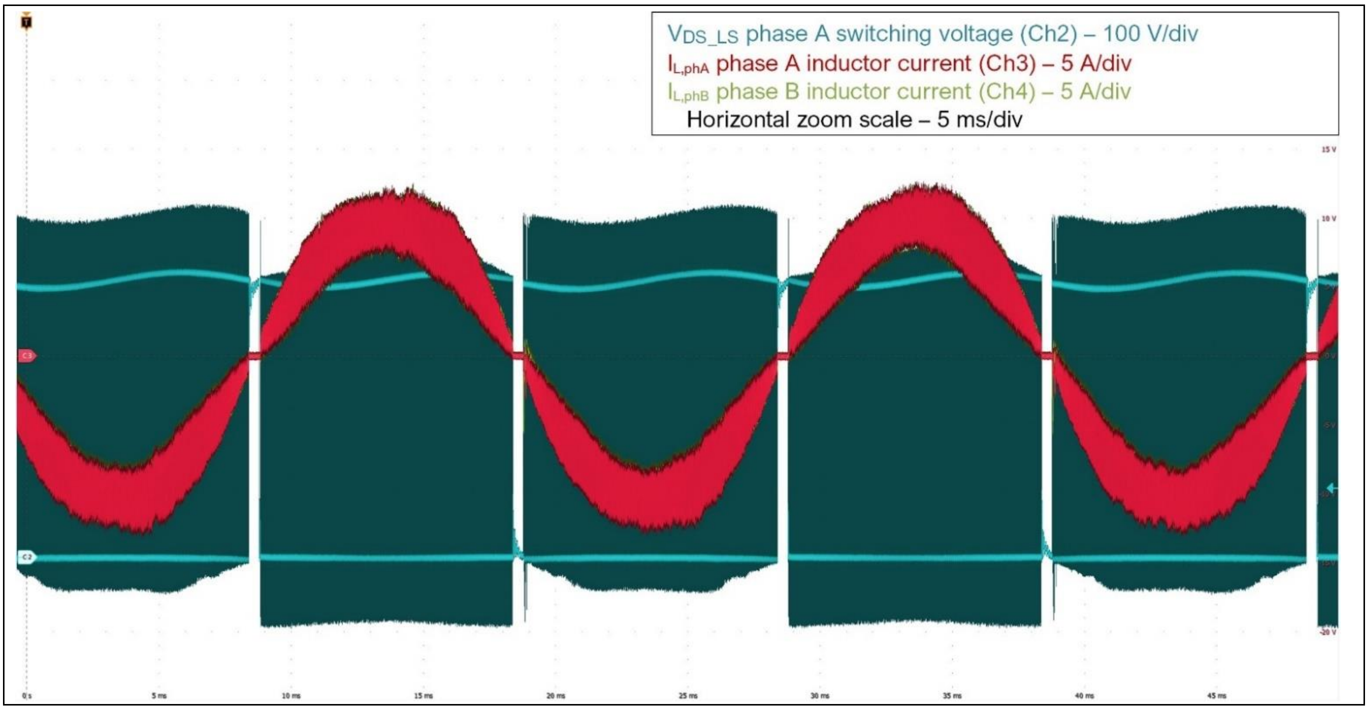


Figure 38 PFC steady-state operation at 230 V_{AC}, full-load. Current through the two inductor chokes of phases A and B, VDS_LS of phase A are shown

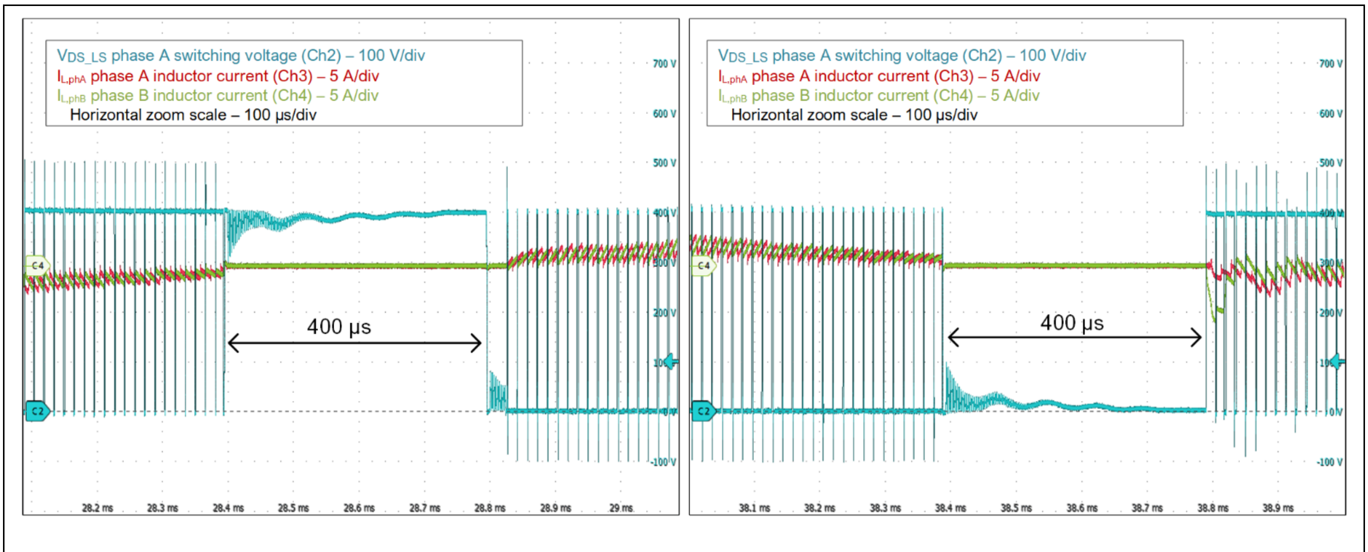


Figure 39 Detailed waveforms of zero crossings at 230 V_{AC} input voltage and at full-load

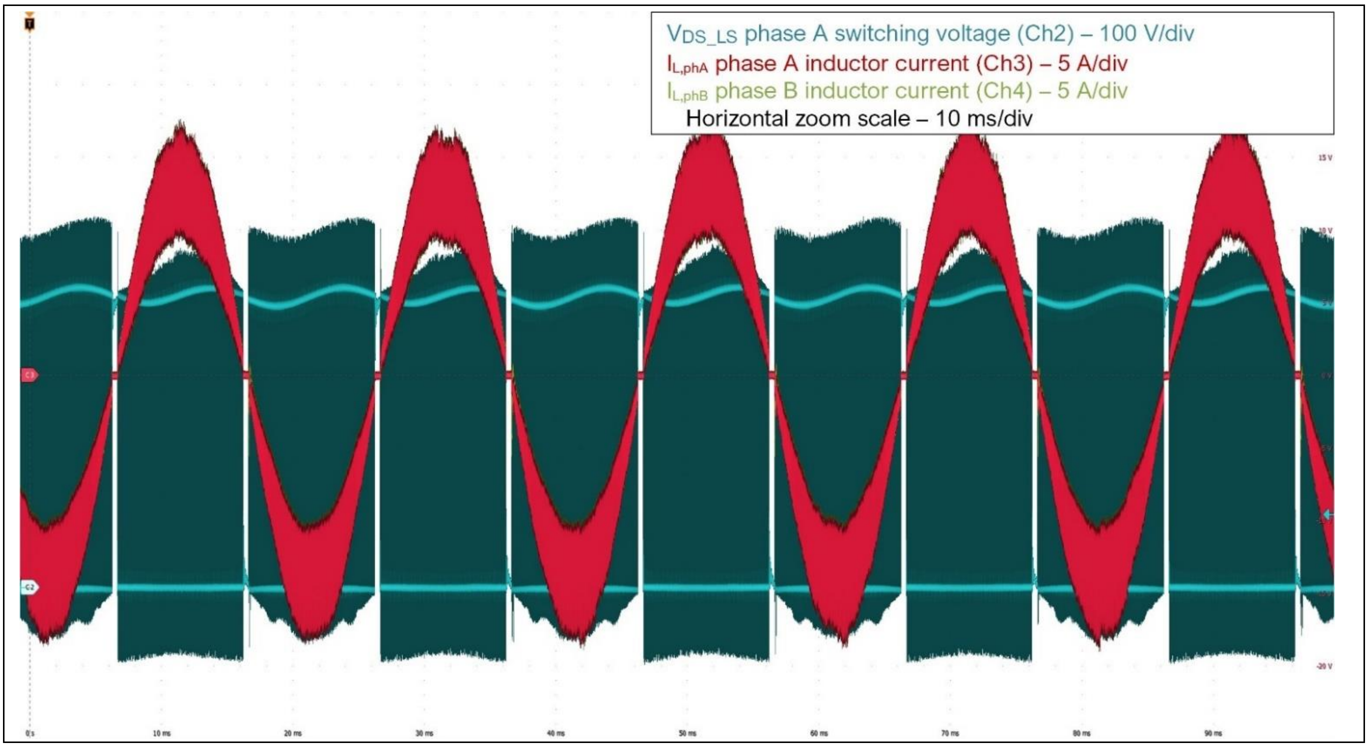


Figure 40 PFC steady-state operation at 180 V_{AC}, full-load. Current through the two inductor chokes of phases A and B, VDS_LS of phase A are shown

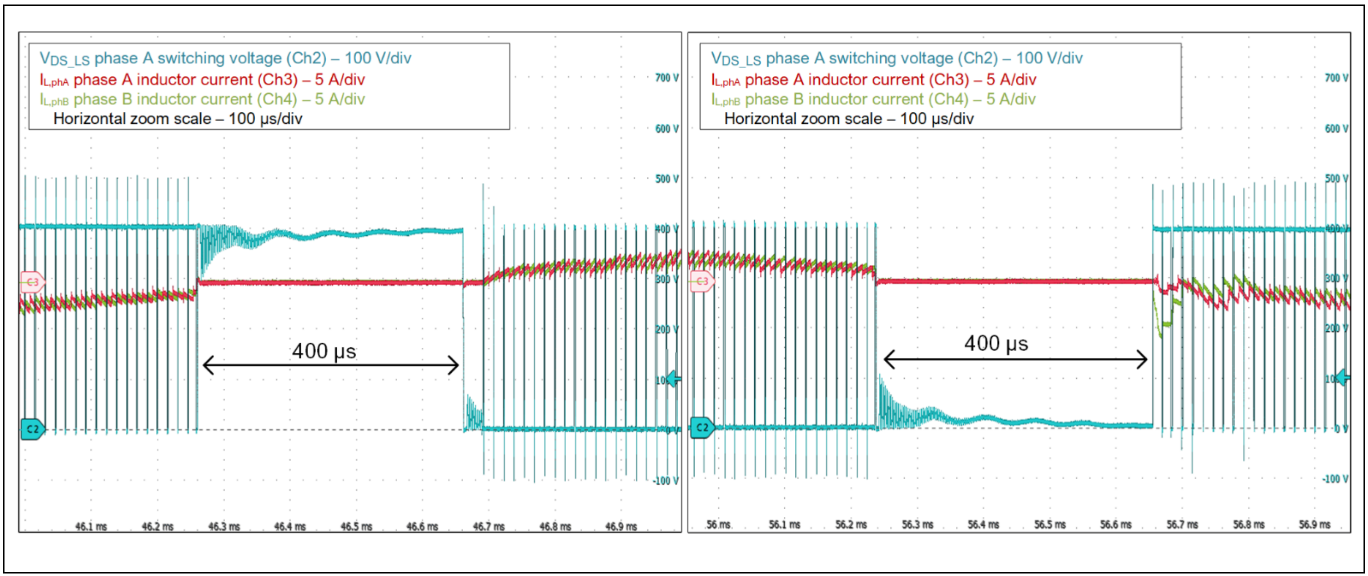


Figure 41 Detailed waveforms of zero crossings at 180 V_{AC} input voltage and at full-load

2.2.5.1 Steady-state performance comparison of CoolSiC™ devices with 57 mΩ on-resistance vs. 72 mΩ on-resistance

During the design process, PFC performances have been compared between CoolSiC™ IMT65R072M1H and IMT65R057M1H with the full PSU operating and enclosed. The main reason for performing this evaluation was the excessive temperature of the PFC fast-leg when using IMT65R072M1H. Indeed, at 180 V_{AC} line voltage the fast-leg of the ILTP-PFC becomes the hotspot of the converter due to the higher input current and the airflow direction. It has been observed that IMT65R072M1H devices were experiencing T_{CASE} of ~120°C at full-load and 180 V_{AC} input line voltage and 25°C ambient temperature. While this is acceptable when operating at ambient temperature, it does not give an adequate temperature margin when operating at the maximum ambient temperature of $T_{AMB,MAX}$ = 45°C. By using IMT65R057M1H, a total reduction of 6.3 W power dissipation at full-load, 180 V_{AC} line voltage on the HF switch only has been observed (lower conduction losses), which resulted in a significant lowering of the PFC temperature in the full-load, 180 V_{AC} line (worst-case) condition.

In Figure 42, efficiency and losses of the PFC extracted during the debugging process are reported for 230 V_{AC} and 180 V_{AC} input. At 230 V_{AC} a crossing point can be observed. This is related to the change in the $R_{DS(ON)}$ and Q_G of the MOSFETs ($R_{DS(ON)}$ at 25 °C and Q_G at 18 V_{DC} driving are 72 mΩ, 27 nC and 57 mΩ, 28 nC respectively), which shifts the peak efficiency point from near 62 percent to 75 percent. Efficiency at full-load is slightly increased at 230 V_{AC}, but no major benefit is observed when operating only at this input AC voltage. However, the use of the IMT65R057M1H is particularly beneficial at the lowest input line voltage, as shown in Figure 42. Thermal performance with the 57 mΩ device is reported in Figure 45.

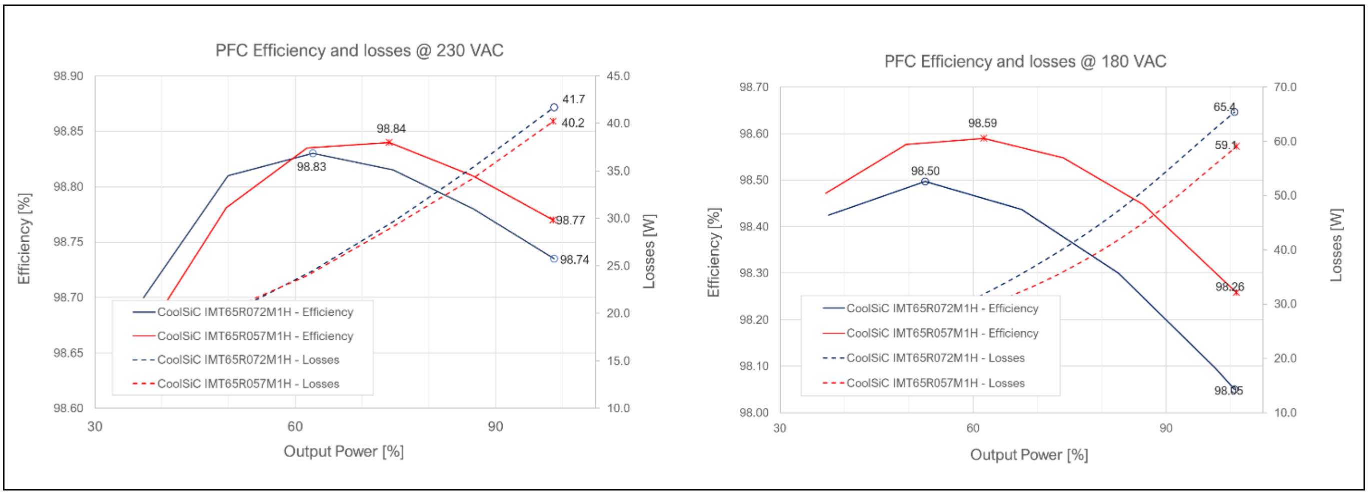


Figure 42 PFC comparison with CoolSiC™ devices with 57 mΩ on-resistance vs. 72 mΩ on-resistance at 230 V_{AC} and 180V_{AC}

2.3 Half-bridge LLC

The half-bridge LLC using CoolGaN™ IGT65R035D2 on the primary-side and IQE046N08LM5 for the SR stage. Figure 43 and Figure 44 shows ZVS turn-on and the lossless turn-off of the half-bridge LLC at 100 percent and 50 percent of the rated load.

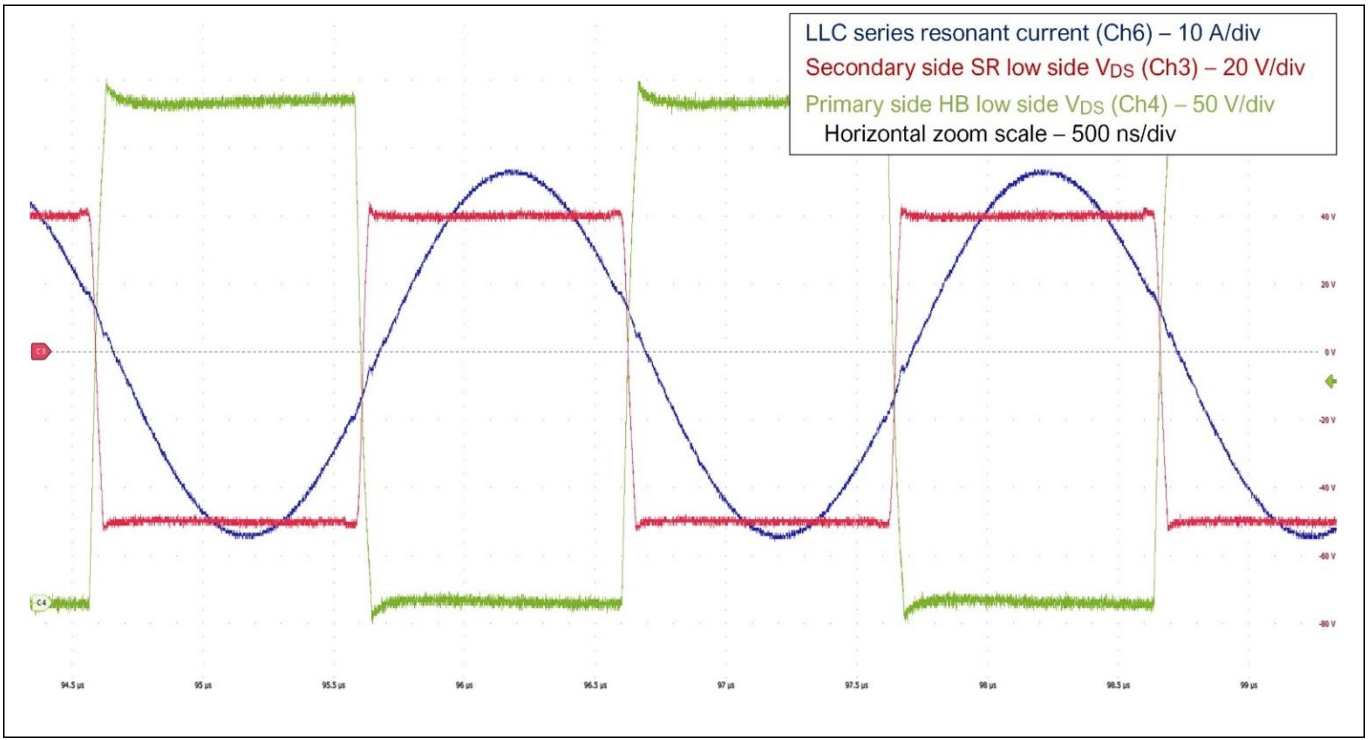


Figure 43 LLC waveforms during steady-state operation at 100 percent of the rated load

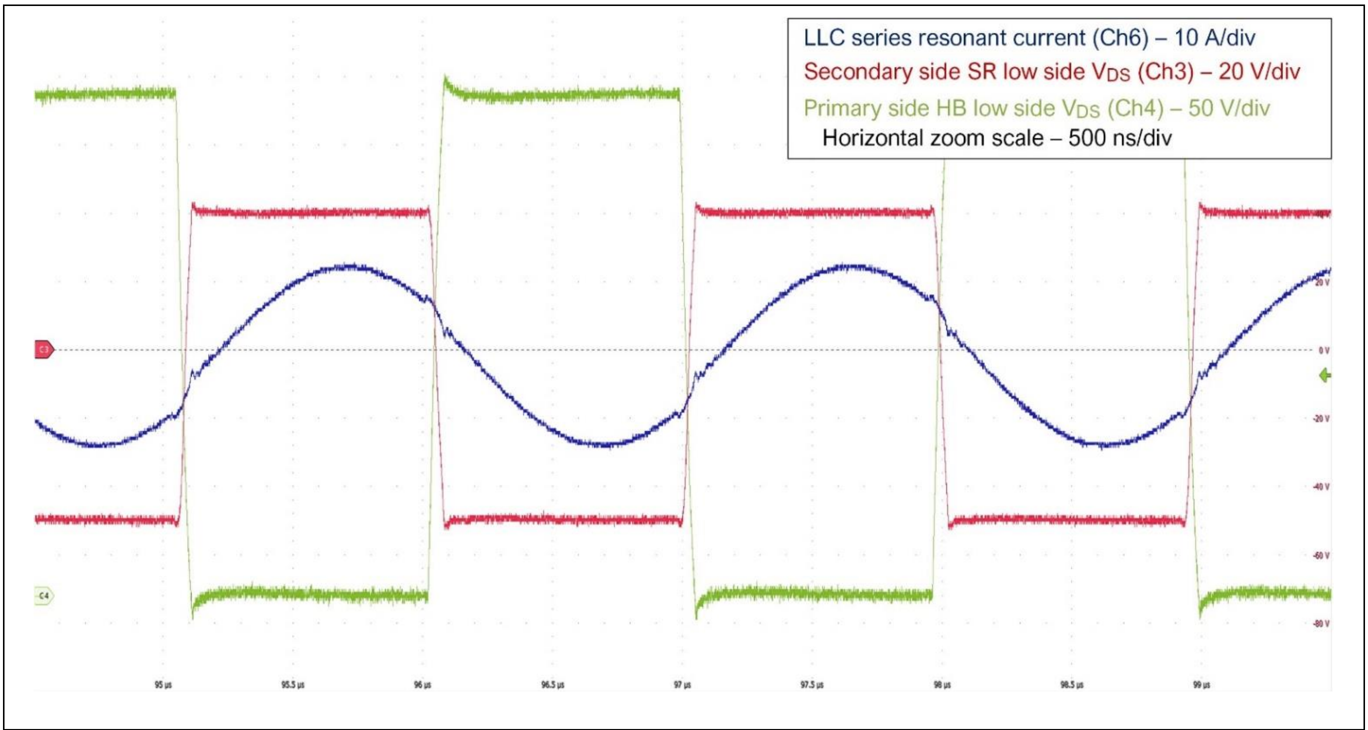


Figure 44 LLC waveforms during steady-state operation at 50 percent of the rated load

2.4 Thermal performance

Thermal performance of the full rectifier has been taken with Type J thermocouples, fan supplied externally, and a 25°C ambient temperature. The PSU temperature has been taken with the full enclosure to provide proper cooling as the enclosure conveys the airflow through the high-temperature component through a “pipe” on the right-hand side of the converter. Critical hotspots such as the PFC high-frequency leg, LLC primary-side, and SR MOSFETs and drivers are shown in Figure 45.

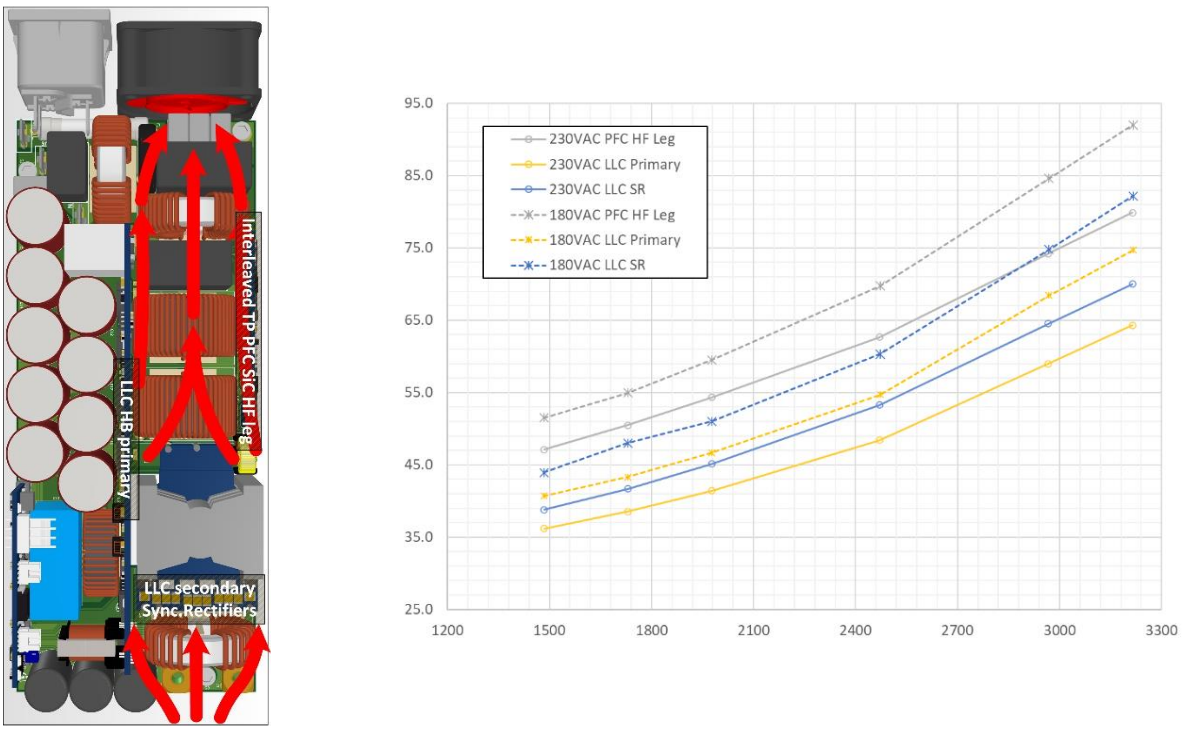


Figure 45 PSU temperature vs. load with IMT65R057M1H at 180 V_{AC} (dashed lines) and 230 V_{AC} (solid)

It is clear from the temperature profiles that the PSU can operate at both 230 VAC and 180 VAC input, with a maximum temperature of nearly 88°C on the PFC SiC MOSFETs IMT65R057M1H as already discussed in Section 2.2.5.1. This also provides enough margin with respect to the maximum ambient temperature of 45°C.

2.4.1 Dynamic conditions

2.4.1.1 Load transients

The PSU has been tested for 10 percent to 50 percent and 10 percent to 90 percent load transient [1], with 1 A/µs slew rate and 20 Hz repetition-rate as shown in Figure 46 and Figure 47. Also, PSU ruggedness against zero to full-load transient and vice versa have been tested. Figure 46 and Figure 47 also show +1.0 V peak overvoltage during the 100 percent to 10 percent transient, and -1.7 V peak undervoltage during the 10 percent to 100 percent transients.

Finally, a feed-forward mechanism of the output current to the PFC voltage loop has been implemented. This allows ultra-fast recovery of the bulk voltage in less than 25 ms, which enables the PSU to withstand the transients with 20 Hz repetition-rate even without a power-buffer like the baby-boost converter.

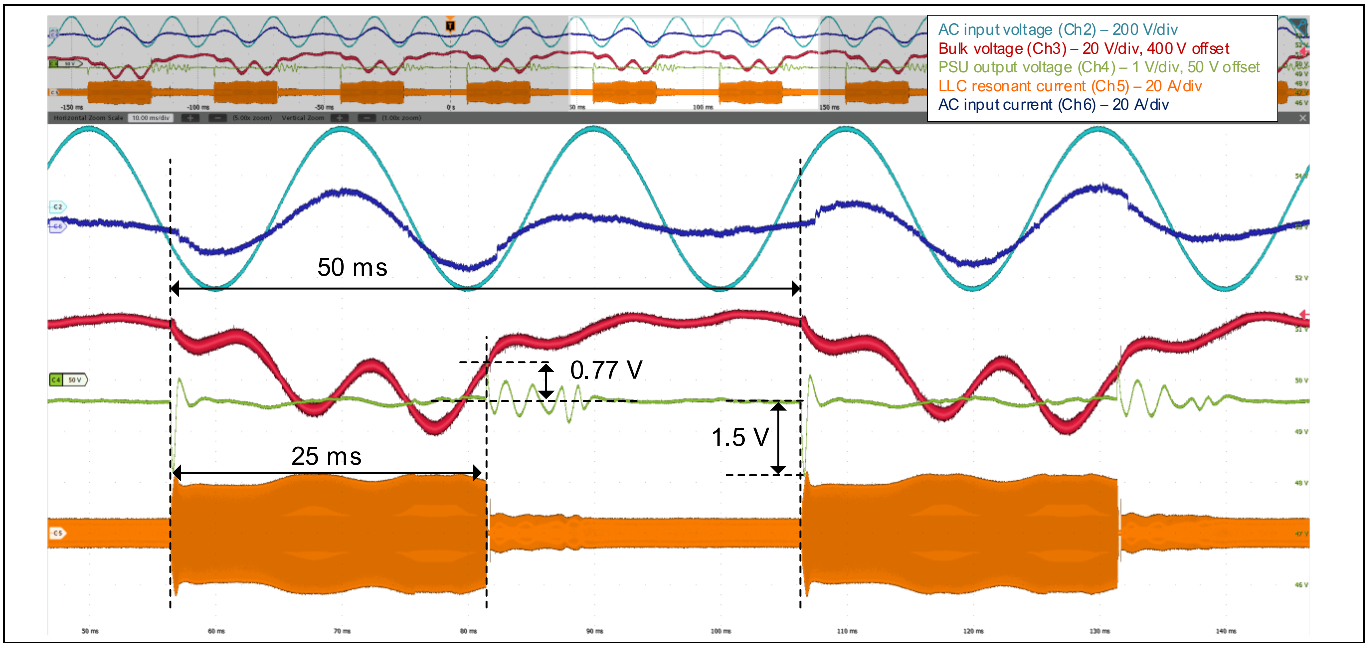


Figure 46 10 to 50 percent to 10 percent load transients of the full PSU at 20 Hz repetition-rate

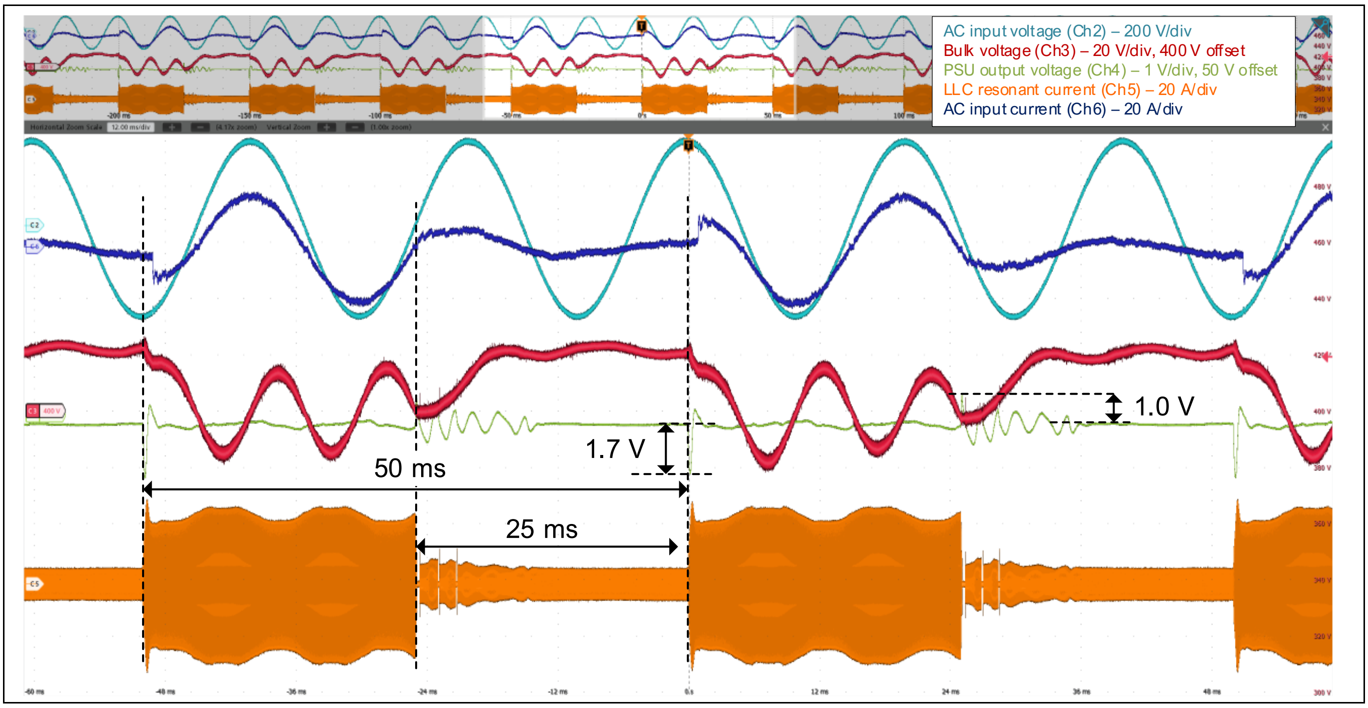


Figure 47 10 percent to 90 percent to 10 percent load transients of the full PSU at 20 Hz repetition-rate

2.4.2 Hold-up time extension

Hold-up time extension with the baby-boost converter (see Section 1.6) has been tested within the PSU. From the operation point of view, the baby-boost stage is always not active, and triggers when a bulk voltage drop below 380 V_{DC} is detected together with absence of AC line input. At this point, the CM8 static switch opens and the voltage at the LLC input is boosted (taking the energy from a deep discharge of the bulk capacitors) until the bulk voltage achieves a cut-off threshold of 250 V_{DC}. Under these conditions, a maximum hold-up time extension of 14.8 ms has been proved at full-load until the PSU output drops, with 900 µF nominal bulk capacitance.

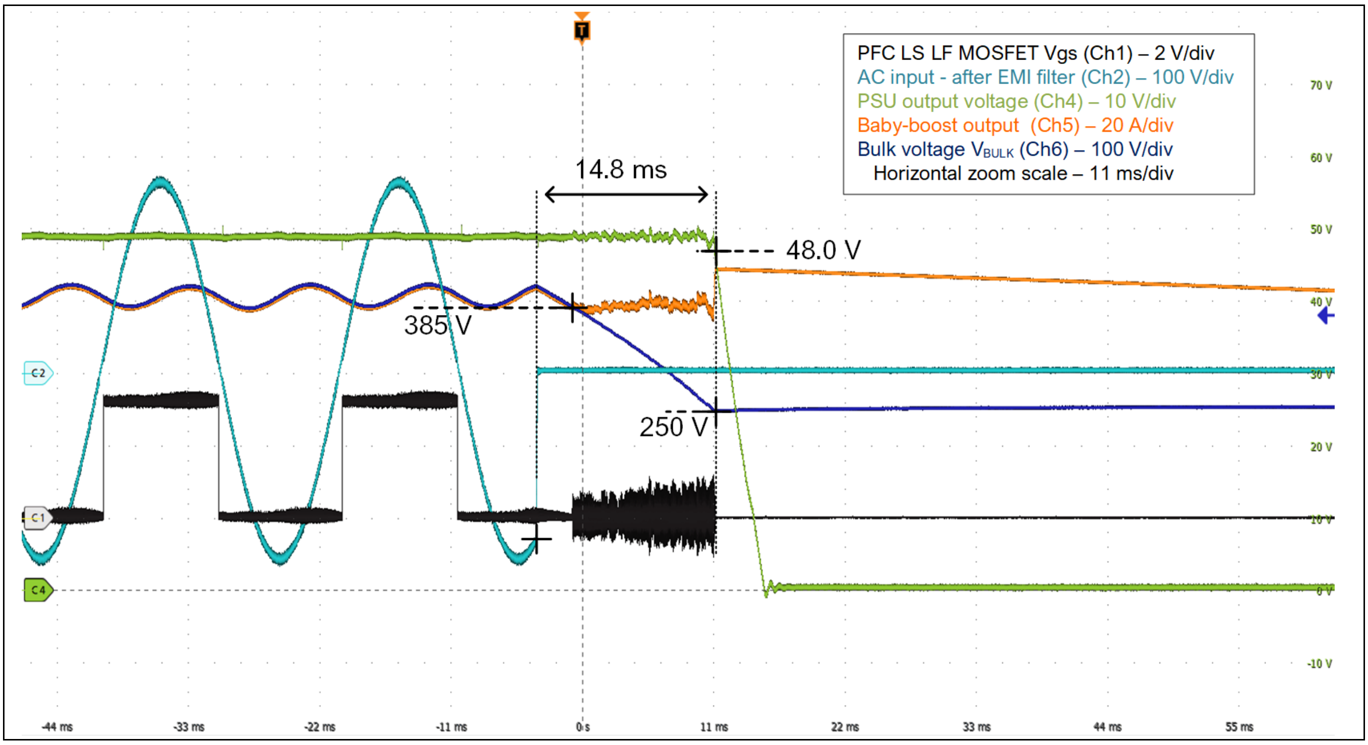


Figure 48 Hold-up time at 100 percent of the rated load

2.4.2.1 AC line-cycle drop-out (ACLDO)

With the baby-boost circuitry fully operating, AC line cycle drop-out has been tested at both 50 percent load and full-load, with a drop of the phase voltage at both 0° and 45° (the worst condition as the bulk voltage is at the peak minimum). The ACLDO is repeated ten times, each time with a 10 ms line drop, and with a time interval of 100 ms in between. The main results of the ACLDO test are reported in Figure 49 to Figure 52.

During each ACLDO event the baby-boost stage is enabled as described in Sections 1.6 and 2.4.2, therefore the bulk voltage discharges faster to a minimum voltage of 260 V_{DC} during each ACLDO event. During the worst-case 100 percent load-abnormal condition, the output voltage remains within +/- 2.0 V_{DC} of the nominal output.

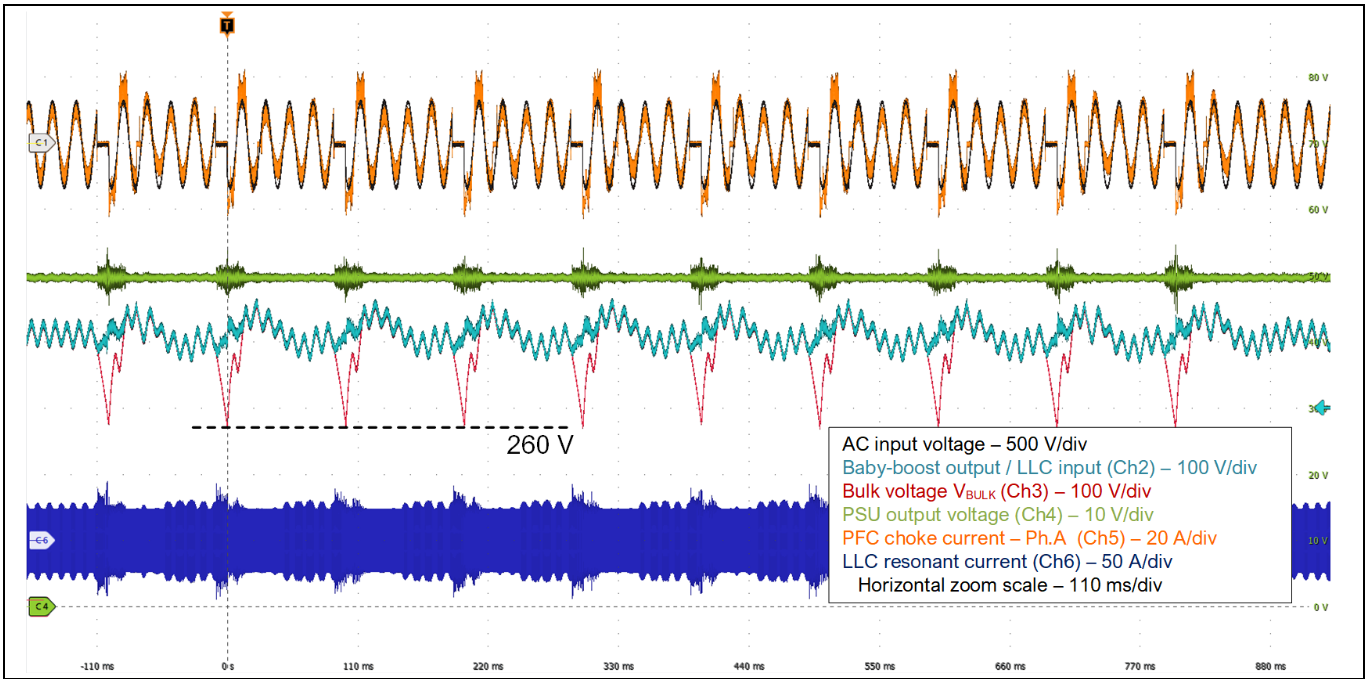


Figure 49 AC line-cycle drop-out (ACLDO) at 100 percent load, AC phase 45 degrees

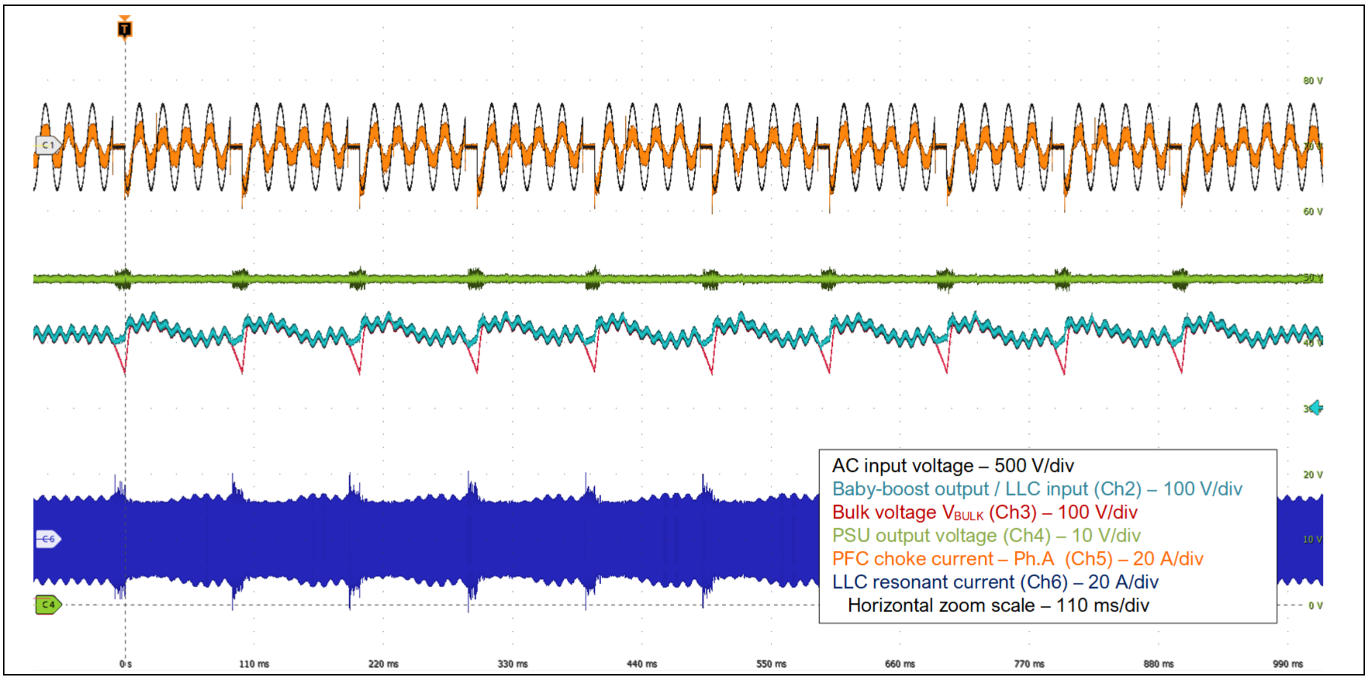


Figure 50 AC line-cycle drop-out (ACLDO) at 50 percent load, AC phase 45 degrees

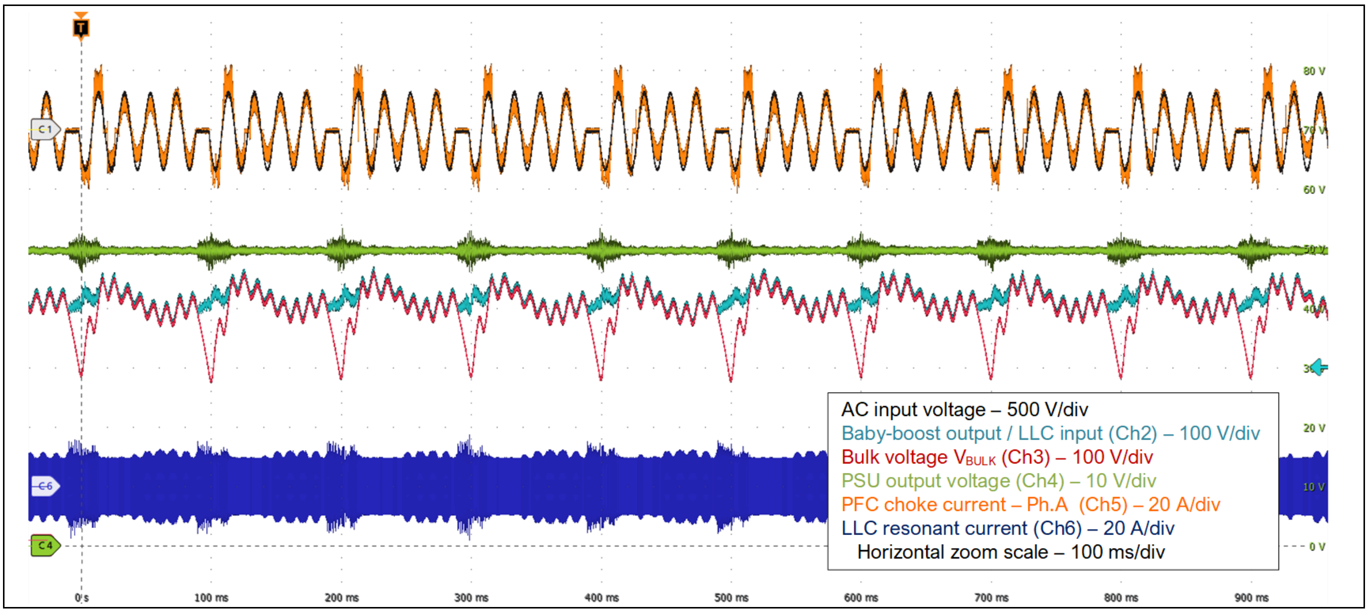


Figure 51 AC line-cycle drop-out (ACLDO) at 100 percent load, AC phase 0 degrees

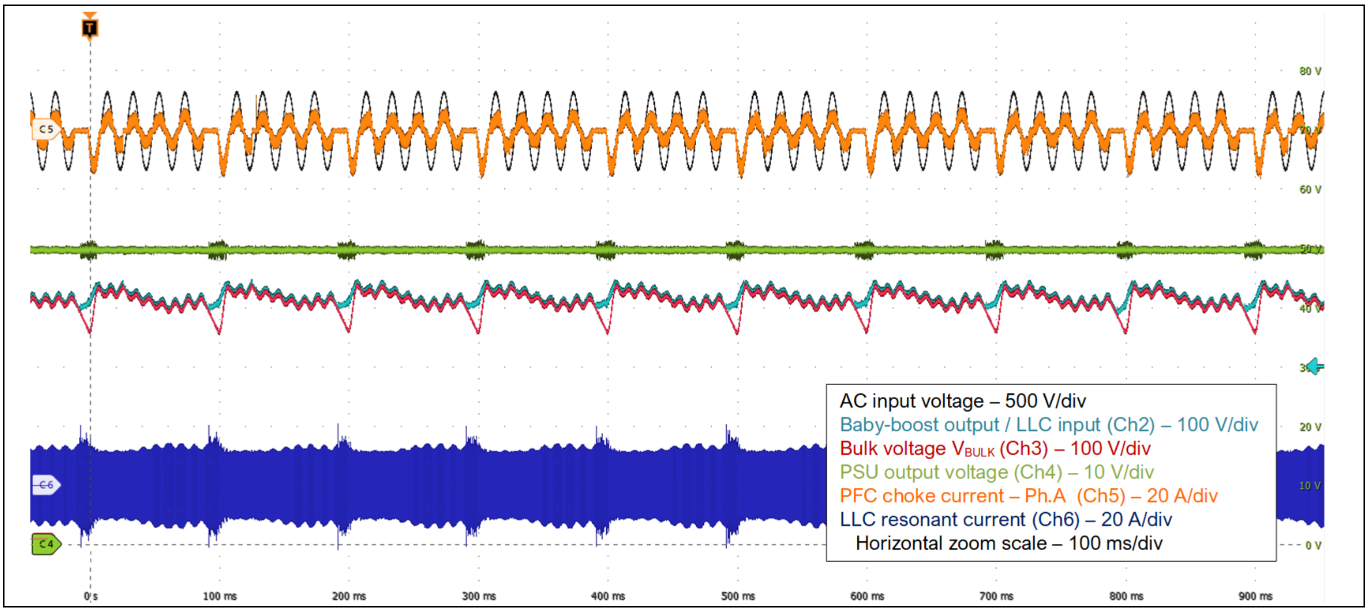


Figure 52 AC line-cycle drop-out (ACLDO) at 50 percent load, AC phase 0 degrees

2.4.3 EMI measurements

The conducted electromagnetic interference (EMI) of the full PSU was measured with the setup shown in Figure 53. The AC voltage is generated by an AC source and the connection to the PFC is done with a line impedance stabilization network (LISN). The spectrum analyzer is connected to the LISN. The load used for the test is a passive resistive load.

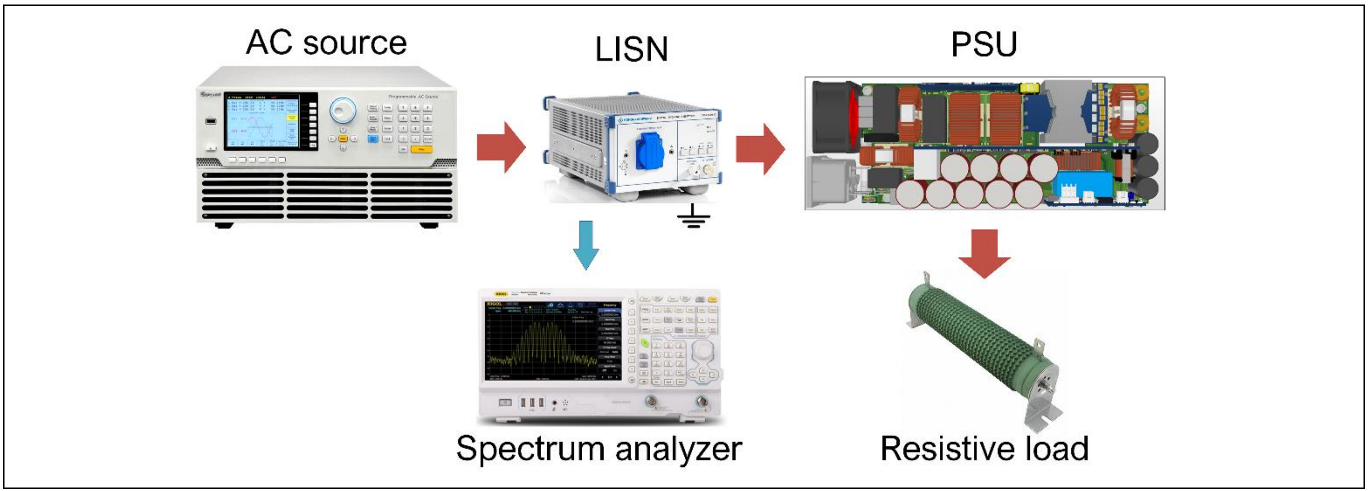


Figure 53 Setup used for EMI test

The EMI tests were performed for both line and neutral with an input of 230 V_{AC} and 3 kW output power. Figure 54 shows the results of the average (AVG) and the positive-peak measurements at 230 V_{AC}. The PSU is fully compliant with Class A limits in both peak and average measurements. Furthermore, the measured positive peak values represent a worst-case compared to the quasi-peak of the standard. A margin of 6 dB is also always achieved.

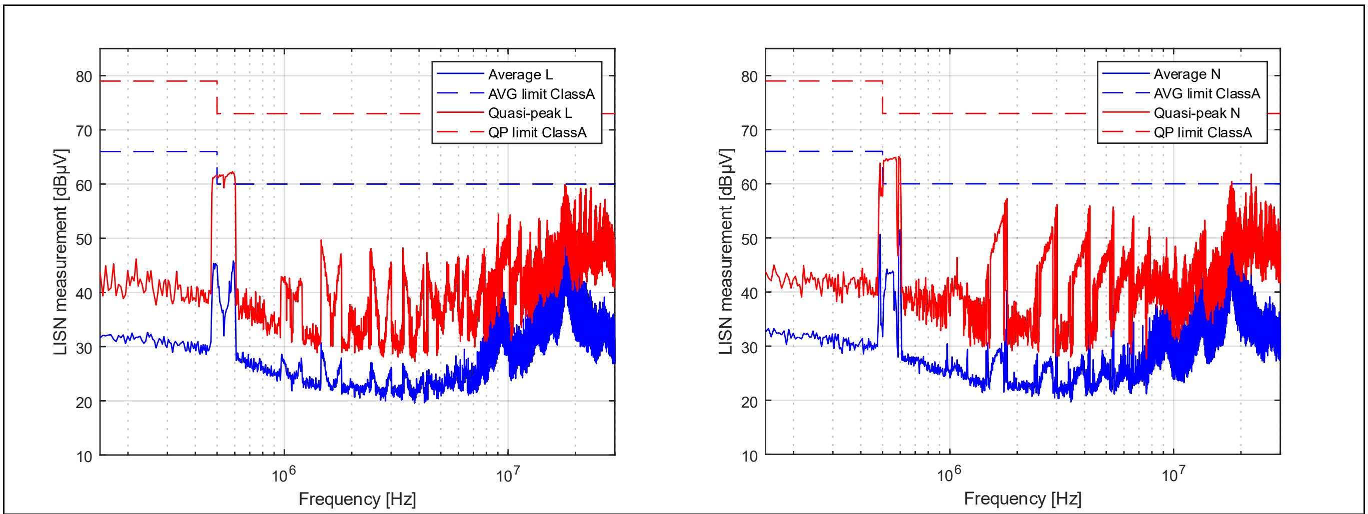


Figure 54 AC input EMI of the PSU at 230 V_{AC} input and 3 kW, and a comparison with the EN 55032 limit

2.4.3.1 EMI improvement through clamping of LF PFC MOSFETs

It is important to remark that a substantial improvement in the EMI behavior can be observed for both line and neutral positive-peak EMI spectra by modifying the zero-crossing sequence of the PFC. In the original driving sequence "without clamping", all the switches of the low- and the high-frequency half-bridges of the PFC are turned-off simultaneously. In this case, a residual current due to PFC modulation will be still stored in the two PFC inductors at the zero crossing. This current resonates with the C_{OSS} of the high-frequency legs, and eventually generate the oscillations shown in Figure 55.

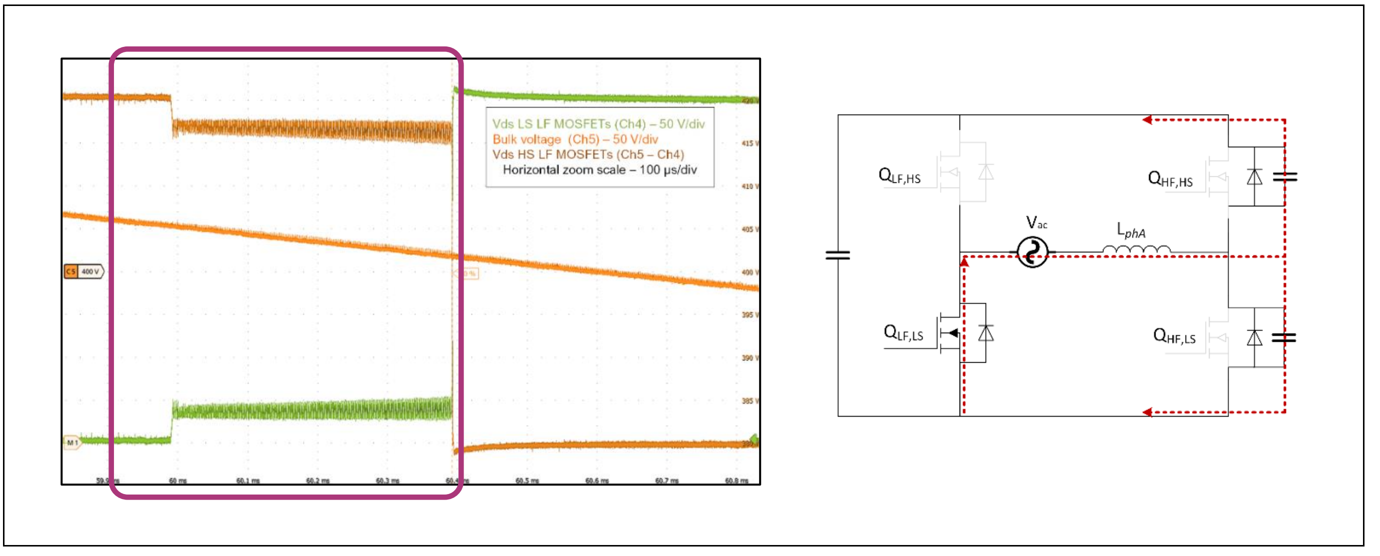


Figure 55 Resonance at zero-crossing (left) and the equivalent simplified circuit for LS LF clamping (right)

A slight modification in the firmware for the turn-off sequence can effectively improve the QP EMI results. If the low-side switch of the low-frequency leg is kept on during the high-frequency leg's turn-off (few switching cycles, e.g. $3/f_{SW}$ - 46 µs), it could clamp the resonating voltage by providing an effective freewheeling path for the residual current to discharge. Furthermore, the $R_{DS(ON)}$ of the LS, LF MOSFET also provides additional passive damping of this current.

From the EMI perspective, the reduction of the resonating voltage during zero-crossing can be appreciated in the positive-peak results in Figure 56 where a peak component of 1.5 MHz and related harmonics is reduced by ~10 dB. Figure 57 provides a comparison of the average EMI but with no significant improvement due to the clamping of the LS LF MOSFET technique during zero-crossing.

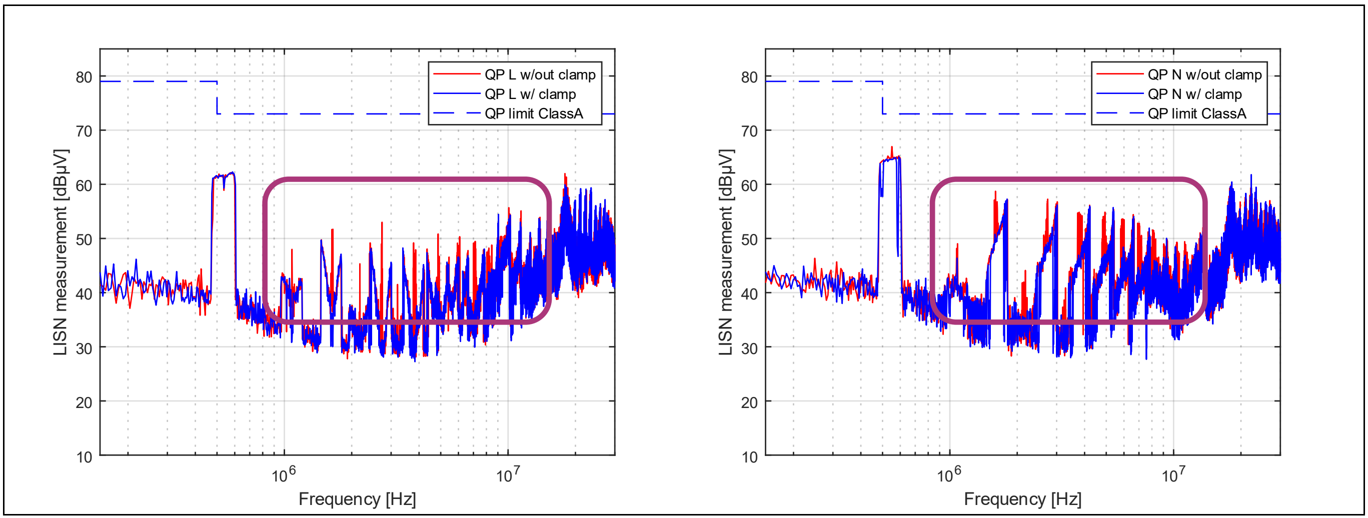


Figure 56 Quasi-peak EMI comparison: With and without extended clamping of LF at zero-crossing

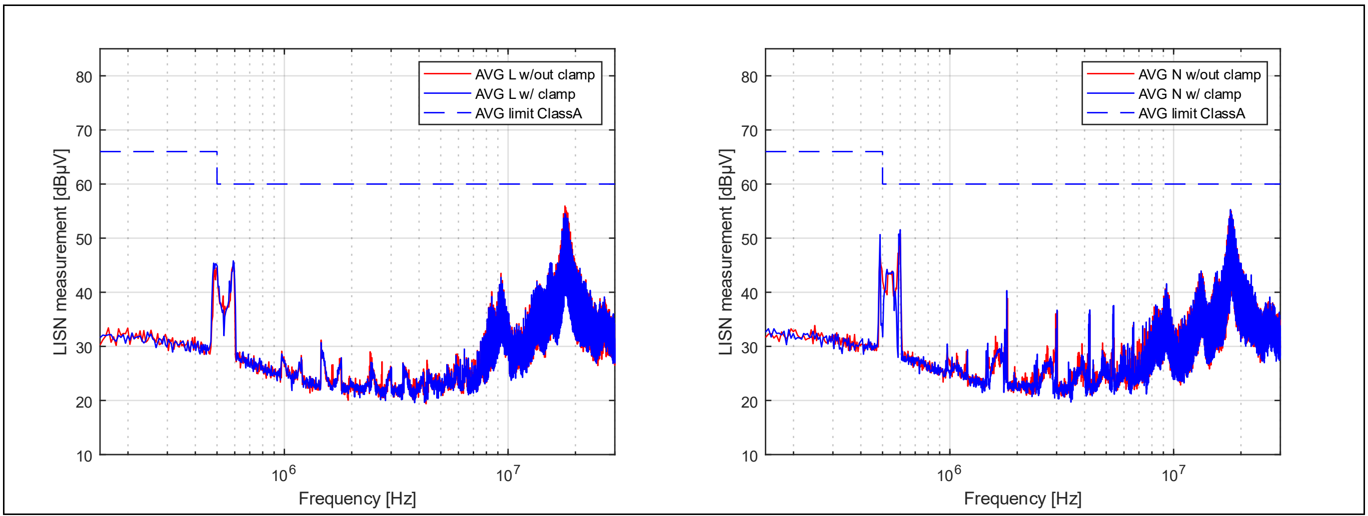


Figure 57 Average EMI comparison: With and without extended clamping of LF at zero-crossing

3 Summary

This document provides a complete system solution from Infineon designed for server PSU applications. The solution incorporates a bridgeless interleaved totem-pole PFC converter and a DC-DC isolated half-bridge LLC converter, achieving efficiency levels of 97.4 percent at 230 V_{AC} and 97.1 percent at 180 V_{AC}, along with a power density of 98 W/in^3.

The REF_3K3W_HFHD_PSU reference board utilizes CoolSiC™ 650 V, CoolMOS™ 600 V MOSFETs, and CoolGaN™ power transistors in TOLL packages, and OptiMOS™ 6 from Infineon. This combination of CoolSiC™, CoolMOS™, CoolGaN™, and OptiMOS™ MOSFETS enable high performance within a compact form factor, as detailed in this application note.

The bridgeless PFC topology and the half-bridge LLC incorporate full digital control through an XMC™ 4000 series microcontroller from Infineon.

Note that the PSU's performance excels not only in steady-state conditions, offering high efficiency, but also meets power line disturbance and hold-up time requirements with additional hold-up time boost converter, which can achieve the required 10 ms hold-up at full-load.

Furthermore, the REF_3K3W_HFHD_PSU board has been tested using a programmable AC source and an electronic load. Efficiency, THD, and PF results are obtained using the WT3000 power analyzer from Yokogawa, alongside waveform analysis with the MSO58 (1 GHz; 6.25 GS/s) oscilloscope from Tektronix.

4 Bill of materials

Infineon main components are marked in bold.

Table 3 Bill of materials for the main board M100003074

Designator	Value	Tolerance	Voltage	Description
C1, C2, C6, C7	4.7nF	Y2	300 V	Capacitor Ceramic
C3	0.82µF	X2	275 V_{AC}	Capacitor Foil
C4, C5	2.2µF	X2	275 V_{AC}	Capacitor Foil
C8, C9, C32, C33, C34, C35	10nF	5%	630 V	Capacitor Ceramic
C10	10uF	10%	450 V	Capacitor Foil
C11, C12, C13, C14, C15, C16, C17, C18, C29	100uF	20%	450 V	Capacitor Polarized
C19, C20, C21, C24, C25, C44, C48	1uF	X7R	35 V	Capacitor Ceramic
C22, C23, C26, C27, C37, C43, C45, C46, C47, C49, C50, C51, C52	4.7uF	X8L	100 V	Capacitor Ceramic
C28, C36, C38, C41, C53, C54	100nF	X7R	630 V	Capacitor Ceramic
C30, C31, C39	820uF	20%	63 V	Capacitor Electrolyt
C40, C42	100pF	X7R	50 V	Capacitor Ceramic
D1, D2	S8KCDICT	–	800 V	Standard Diode
D3	**IDL10G65C5**	–	**650 V**	**Schottky-Diode**
F1	20A	–	–	Sicherung
IC1, IC2	MCR1101-20-3	–	–	Hall Sensor
IC3	**1EDN8511B**	–	–	**Integrated Circuit**
IC4	**1EDB8275F**	–	–	**Integrated Circuit**
J1, J2	7460307	–	–	Screw Terminal
L1, L2	1.4mH	–	–	Common Mode Choke
L3	30uH	–	–	Buffer Choke
L4, L5	385uH	–	–	PFC-Choke
L6	32uH	–	–	Inductor
NTC1	14R	25%	–	NTC Resistor
Q2	**IPT60R080G7**	–	**600 V**	**MOSFET**
Q3	**IPT60R016CM8**	–	**600 V**	**MOSFET**
R1, R17, R18, R19, R20, R21, R22, R23, R24, R29, R30, R31, R32, R33, R35, R38	309k	0.1%	–	Resistor
R2, R6	10R	1%	–	Resistor
R3, R4, R5, R7, R9	4R7	1%	–	Resistor
R8, R27	100R	1%	–	Resistor
R12, R13, R16, R40, R41	R001	1%	–	Resistor

Designator	Value	Tolerance	Voltage	Description
R14, R25, R28, R34, R36, R37, R39, R42, R43, R44	2k7	1%	–	Resistor
R15	0R	1%	–	Resistor
R45	R003	1%	–	Resistor
T1	MG500003079	–	–	PWR Transformer
TR1	MG600003070	–	–	Current Sense Transformer
X1, X4, X5	Faston Connector TE1217421-1	–	–	Connector
X3	SQW-106-01-L-D-ND	–	–	Female Header, 10 Contacts 2mm
X6	200-SQW11301LD	–	–	Female Header, 26 Contacts 2mm

Table 4 **Bill of materials for the ILTP PFC HF power card PW400003071**

Designator	Value	Tolerance	Voltage	Description
C1, C6, C8	10uF	X5R	35 V	Capacitor Ceramic
C2, C4, C5, C7, C9, C10, C11, C13, C14, C15, C19, C20	1uF	X7R	50 V	Capacitor Ceramic
C3, C21, C22, C23, C24	100pF	X7R	50 V	Capacitor Ceramic
C12, C16, C17, C18	100nF	X7R	630 V	Capacitor Ceramic
D1, D2	ES1JAL_M3G	–	600 V	Diode
D3, D5	DFLS140L-7	–	40 V	Standard Diode
D4, D6, D7, D8	BAT165	–	40 V	Schottky-Diode
IC1	**1EDN8511B**	–	–	**Gate Driver IC**
IC2, IC3, IC4	L78L18ACUTR	–	–	Integrated Circuit
IC5, IC6	**2EDB9259**Y	–	–	**Gate Driver IC**
Q1, Q2, Q3, Q4	**IMT65R057M1H**	–	**650 V**	**MOSFET**
R1	43k	1%	–	Resistor
R2, R6	1k	1%	–	Resistor
R3, R4	10R	1%	–	Resistor
R5	12k	1%	–	Resistor
R7, R10, R12, R15	2R2	1%	–	Resistor
R8, R11, R13, R16	1R	1%	–	Resistor
R9, R14, R18, R19	510R	1%	–	Resistor
R17	10K NTC	–	–	Resistor

Table 5 Bill of materials for the LLC power card PW200003075

Designator	Value	Tolerance	Voltage	Description
C2, C26	150uF	20%	16 V	Capacitor Polarized
C3, C7, C8, C9, C17, C18, C30	1uF	X7R	35 V	Capacitor Ceramic
C4, C6, C10, C11	2n2	X7R	50 V	Capacitor Ceramic
C5, C19, C20, C23, C28	100pF	X7R	50 V	Capacitor Ceramic
C12, C14, C15, C35, C36	100nF	X7R	630 V	Capacitor Ceramic
C13	10uF	X7R	25 V	Capacitor Ceramic
C16, C21, C31, C32	10uF	X7R	50 V	Capacitor Ceramic
C24	100nF	X7R	25 V	Capacitor Ceramic
C27	1nF	X7R	50 V	Capacitor Ceramic
C29	33uF	10%	20 V	Capacitor Polarized
C34	330pF	X7R	50 V	Capacitor Ceramic
D1, D9, D10	BAT165	–	40 V	Schottky-Diode
D2, D7, D8	DFLS1200	–	200 V	Diode
D5	FES1JE	–	600 V	Diode
IC1, IC4	**1EDB8275F**	–	–	**Gate Driver IC**
IC2	**1EDN8550B**	–	–	**Gate Driver IC**
IC5, IC9	**1EDN8511B**	–	–	**Gate Driver IC**
IC6	TLV431B	0.5%	1.24 V	TLV431B- Adjustable Precision Shunt Regulator 0.5%
IC7	**ICE2QR2280G**	–	–	**Integrated Circuit**
IC8	VOL617A-3	–	–	Integrated Circuit
L1, L2, L3, L4	SRF2012-361YA	–	–	Common Mode Power Line Choke
Q1, Q2, Q3, Q4	**IGT60R042D2**	–	–	**GaN HEMT Transistor**
Q5, Q6, Q7, Q8	**IPT60R016CM8**	–	**600 V**	**MOSFET**
Q9, Q10	**BSS138N**	–	**60 V**	**MOSFET**
R2, R5, R9, R14, R15, R16, R19, R20, R23, R24, R26, R29, R47	10R	1%	–	Resistor
R3, R4, R27, R28	2R7	1%	–	Resistor
R6, R7, R46, R48	1k	1%	–	Resistor
R8	150R	1%	–	Resistor
R10, R13, R45	33k	1%	–	Resistor
R11, R17, R18, R21, R22, R25, R36	510R	1%	–	Resistor
R12	10K NTC	3%	–	Resistor
R30, R31, R32, R33	270R	1%	–	Resistor
R34, R35, R40	15k	1%	–	Resistor

Designator	Value	Tolerance	Voltage	Description
R37, R39	825R	1%	–	Resistor
R38	3k6	1%	–	Resistor
R41	1k18	0.1%	–	Resistor
R42	1R5	1%	–	Resistor
R43	2K7	1%	–	Resistor
R44	10k	1%	–	Resistor
REL1	G2RL-1A-E2-CV-HA -DC12	–	12 V	Relay
TF1	ICE 8032.0205.024	–	–	Transformer
TR1, TR3	XT01	–	–	Common Mode Power Line Choke

Table 6 Bill of materials for the control card CD100003075

Designator	Value	Tolerance	Voltage	Description
C1, C2, C8, C18, C24, C26, C28, C31, C33, C35, C36, C42, C49, C50, C54, C59, C65, C66, C67, C68, C74, C75	100nF	X7R	25 V	Capacitor Ceramic
C3, C4, C40, C41	10pF	X7R	50 V	Capacitor Ceramic
C5	10uF	X5R	25 V	Capacitor Ceramic
C6, C9, C14, C15, C16, C17, C19, C45, C46, C47, C57, C58, C61, C63, C64, C71	330pF	X7R	50 V	Capacitor Ceramic
C7, C70, C72	100pF	X7R	50 V	Capacitor Ceramic
C10, C23, C25, C27, C30, C32, C34, C48, C55, C56, C69	10uF	X5R	6.3 V	Capacitor Ceramic
C43, C52	47pF	X7R	50 V	Capacitor Ceramic
C60, C62	4n7	X7R	50 V	Capacitor Ceramic
D3, D7, D8, D9, D10, D12	BAT165	–	40 V	Schottky-Diode
D5, D6, D11	GREEN LED	–	–	LED
IC1	**4DIR1400H**	–	–	**Integrated Circuit**
IC2	**TLS4120D0EPV33**	–	–	**Synchronous Step-Down Regulator**
IC3	**TLV1391IDBVR**	–	–	**Single Differential Comparators.**
IC4, IC10	**TLV2376IDR**	–	–	**Integrated Circuit**
IC8	dsPIC33CK256MP203-I/M5	–	–	MCU
IC11, IC12	LMH6642MF	–	–	Integrated Circuit
IC13	**TLS820D0ELV33XUM**	–	–	**Low Dropout Linear Voltage Regulator**

Designator	Value	Tolerance	Voltage	Description
IC14	**XMC4200-Q48K256**	–	–	**Integrated Circuit**
L1	100uH	–	–	Magnetic
L2, L3	Ferrite bead 60Ohm@100MHz	–	–	Magnetic
NTC1	10K	1%	–	NTC Resistor
R1, R6, R11, R12, R17, R41, R44, R71, R72, R76, R77	510R	1%	–	Resistor
R2, R3, R4, R5, R34, R39, R43, R60, R69	15k	1%	–	Resistor
R7, R16, R23, R24, R26, R28	309k	0.1%	–	Resistor
R8, R9, R13, R15, R25, R47, R53	10k	0.1%	–	Resistor
R10, R30, R37, R42, R62	2k7	1%	–	Resistor
R14, R18, R19, R20, R45, R70	100R	1%	–	Resistor
R21, R22, R27, R29	17k8	0.1%	–	Resistor
R31	1k	1%	–	Resistor
R48, R56, R57, R63, R65	4k99	0.1%	–	Resistor
R49, R52	124R	0.1%	–	Resistor
R50, R54, R58	49k9	0.1%	–	Resistor
R51, R55, R59	54k9	0.1%	–	Resistor
R66, R68, R73, R74	261R	1%	–	Resistor
R75	1R8	1%	–	Resistor
X1, X5	FTSH-105-01-L-DV-K	–	–	Connector
X2	TMM-113-03-L-D	–	–	Pin Header, 26 Contacts
X3	Fan connector	–	–	Pin Header, 4 Contacts
X4	TMM-106-03-L-D	–	–	Pin Header, 26 Contacts
X6	B2B-ZR	–	–	Connector
XTAL1	QT325S-12.000MEEQ-T	–	–	Crystal Oscillator

Table 7 Bill of materials for the secondary-side transformer PCB MG700003072

Designator	Value	Tolerance	Voltage	Description
C1, C2, C3, C4, C5, C6, C7, C8, C9, C10, C11	4.7uF	X8L	100 V	Capacitor Ceramic
C13, C14, C15, C16, C17, C18	1uF	X7R	35 V	Capacitor Ceramic
D1, D2	**BAT46WJ**	–	**100 V**	**Schottky Diode**
IC1, IC2	**2EDB7259K**	–	–	**Gate driver IC**
R1, R2	2R2	1%	–	Resistor
R3, R4, R5, R6, R7, R8, R9, R10	1R	1%	–	Resistor
R11, R12	2k	1%	–	Resistor
T1, T2, T3, T4, T5, T6, T7, T8	IQE046N08LM5	–	80 V	MOSFET

5 Schematics

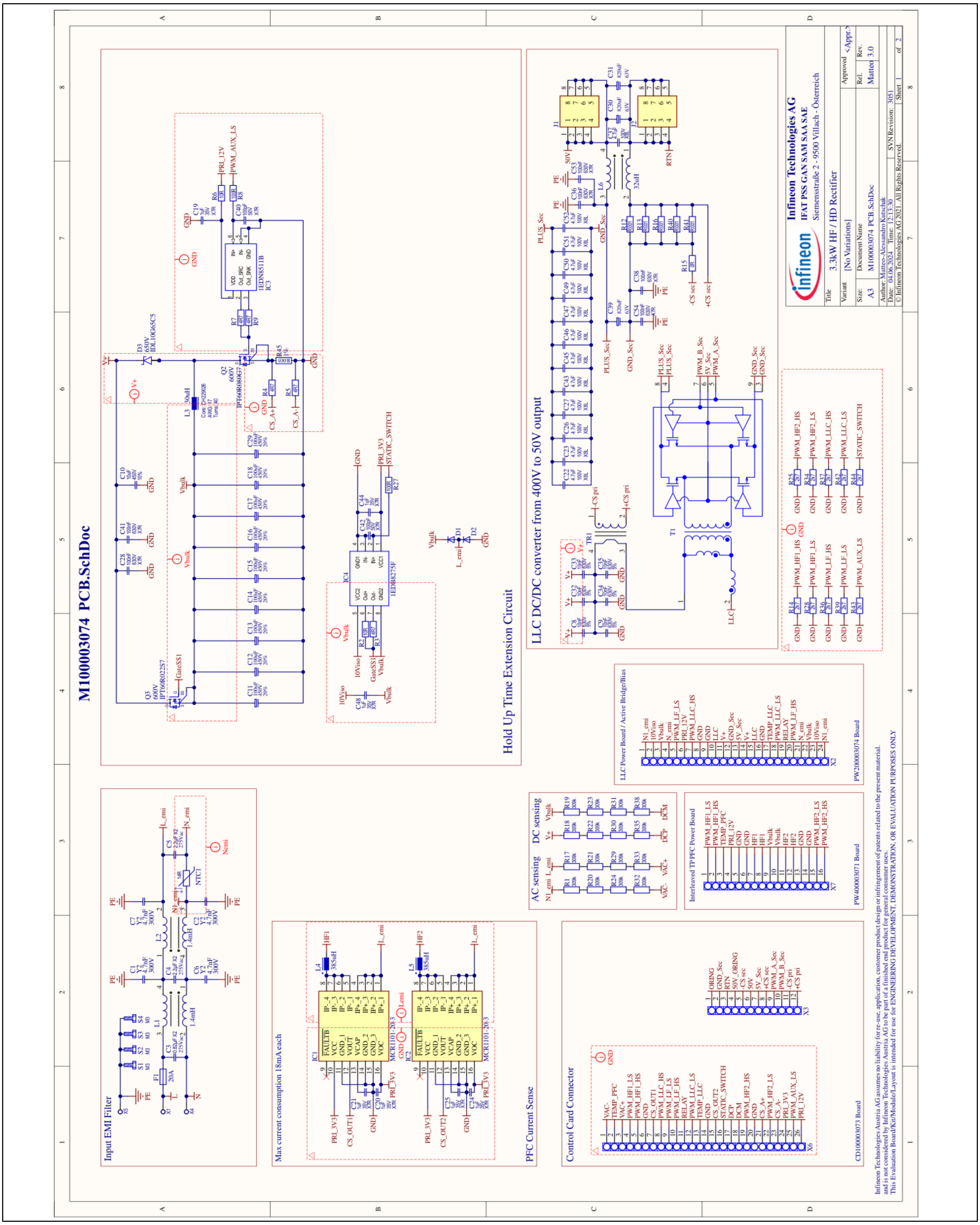


Figure 58 **Schematic diagram of the main board (M100003074)**

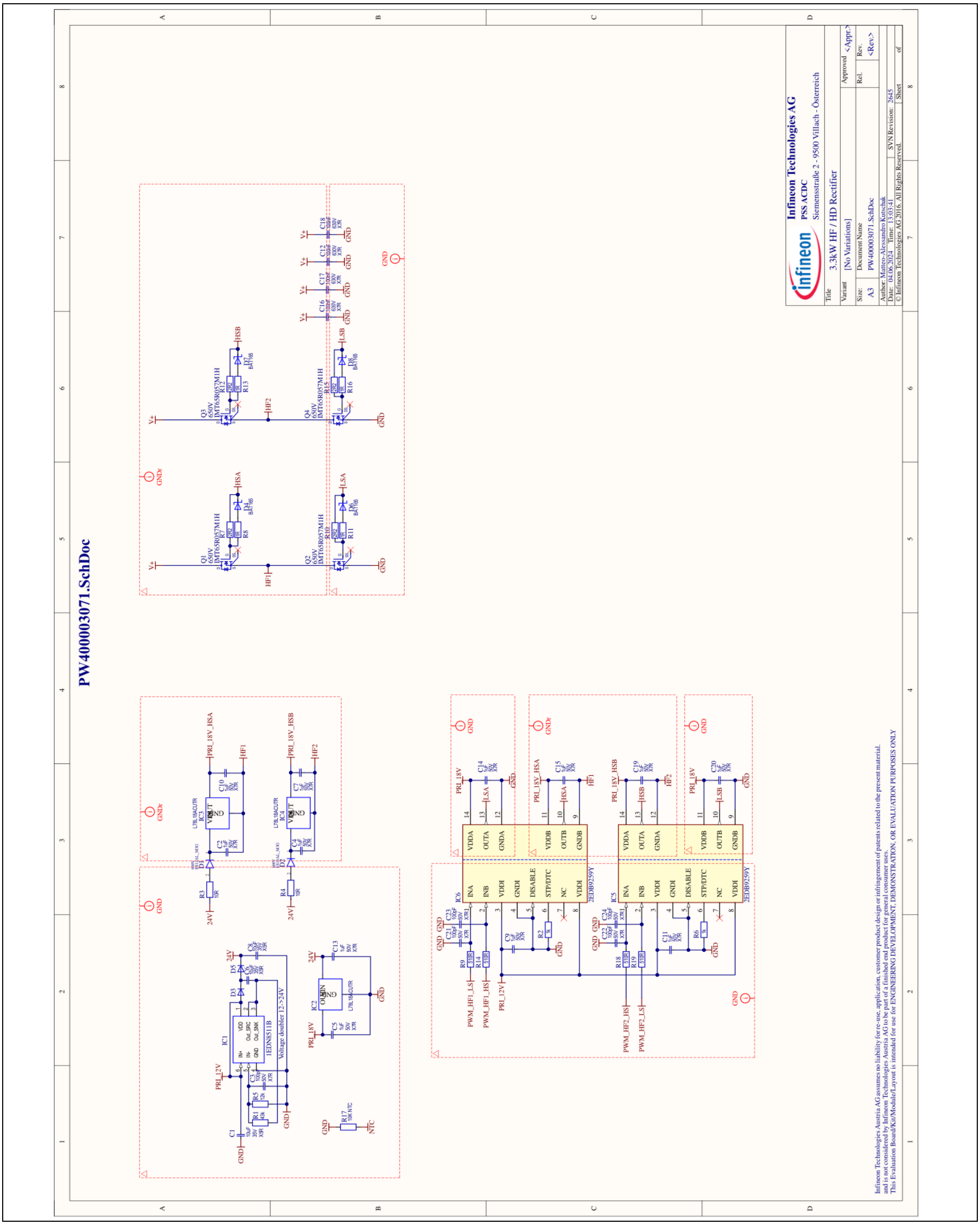


Figure 59 Schematic diagram of the ILTP-PFC high-frequency board (PW400003071)

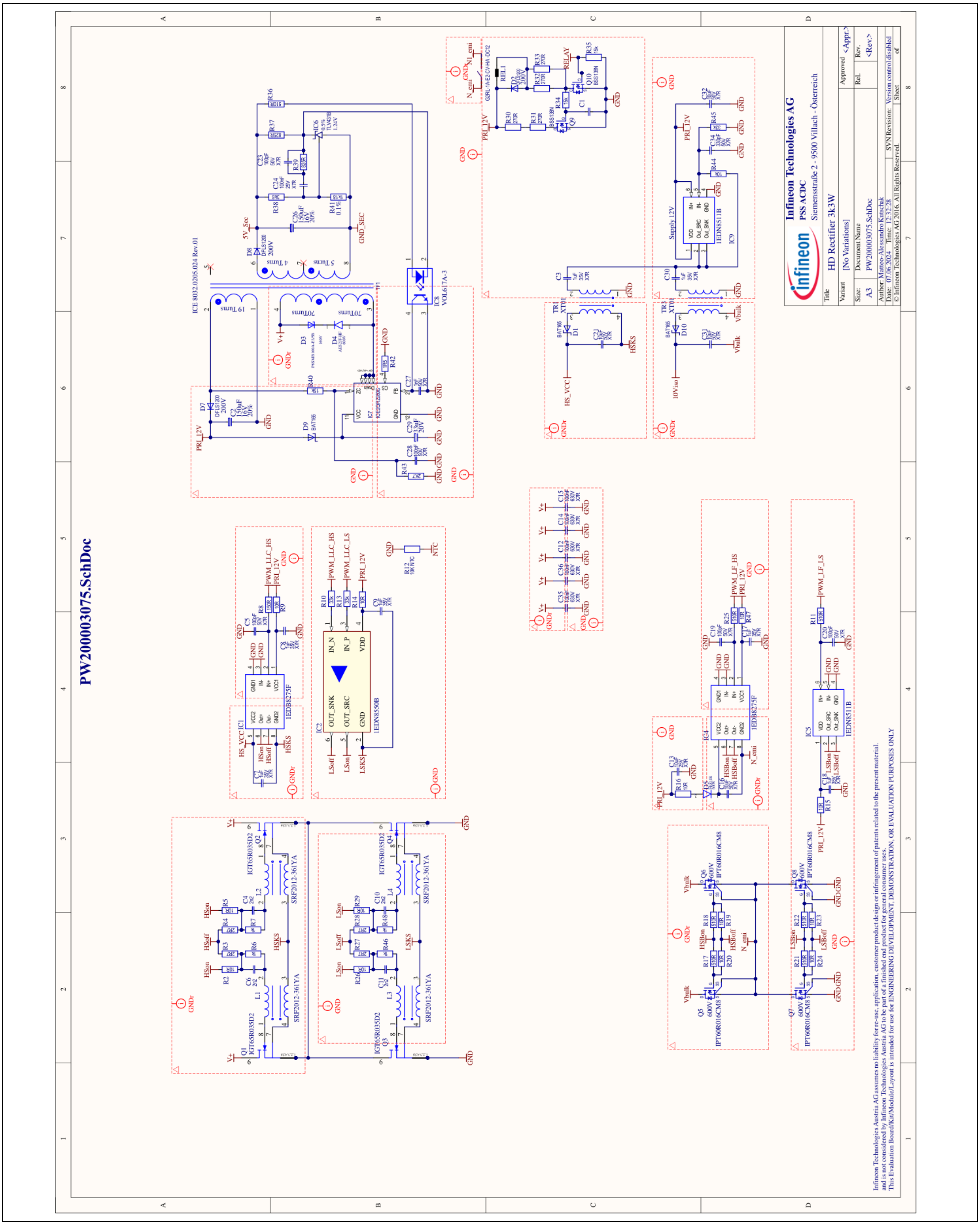


Figure 60 Schematic diagram of the LLC and PFC SR power card (PW200003075)

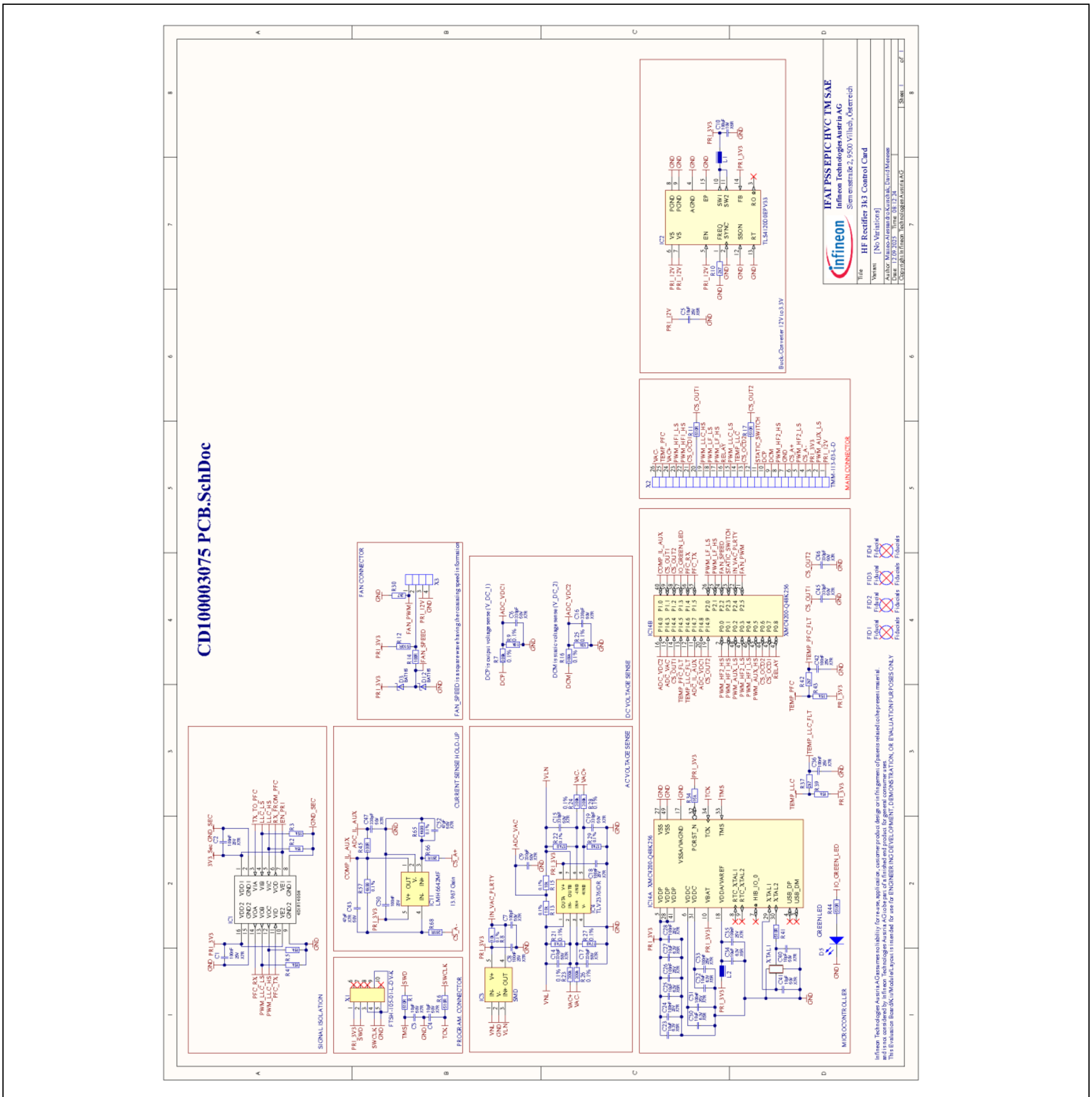


Figure 61 Schematic diagram of the control PCBA (CD100003075) – part 1: PFC control

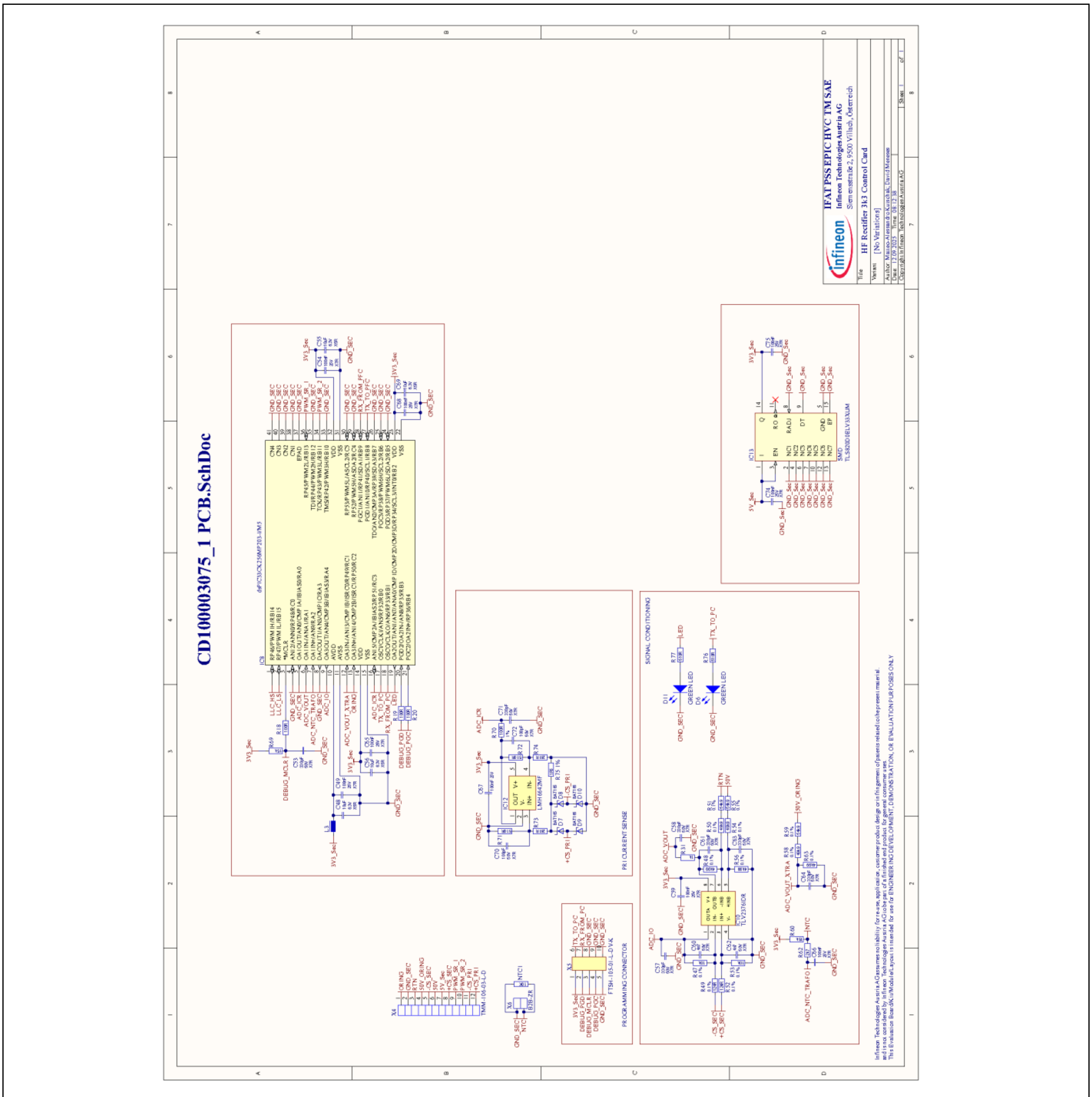


Figure 62 Schematic diagram of the control PCBA (CD100003075) – part 2: LLC control

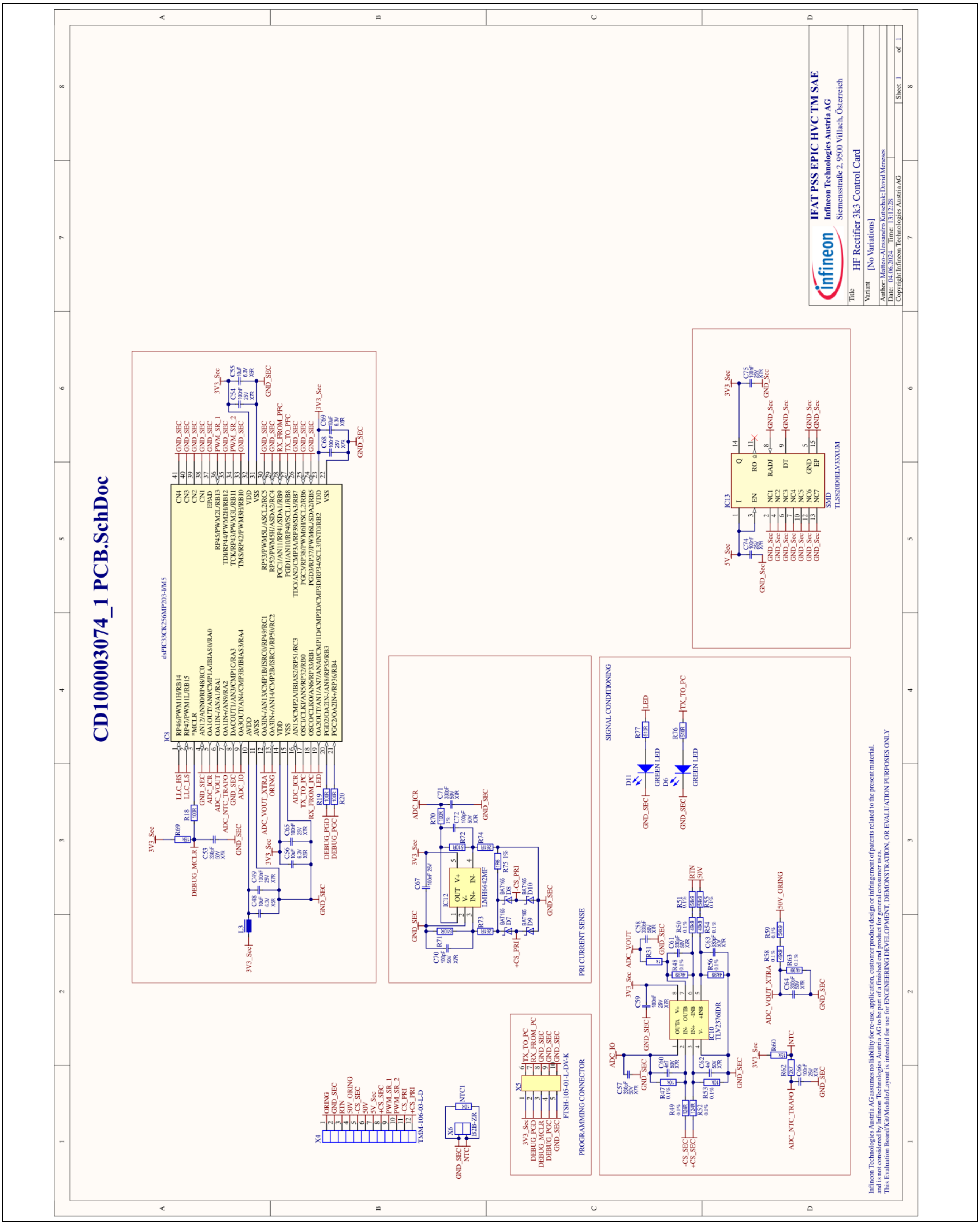


Figure 63 **Schematic diagram of the secondary PCBs (MG700003072)**

References

[1] Open Compute Project (OCP), Open Rack V3 48V PSU Specification Rev: 1.0. Available online: http://www.opencompute.org (accessed on 8 August 2023)

[2] Infineon Technologies AG: Server and datacenter 3 kW 50 V PSU – EVAL_3KW_50V_PSU; February 2021; https://www.infineon.com/cms/en/product/evaluation-boards/eval_3kw_50v_psu

[3] “Guidelines for CoolSiC™ MOSFET gate drive voltage window”, Infineon technologies AG, Application Note no. AN2018-09

[4] M.-A. Kutschak, D. Meneses, and F. Pulsinelli, "3300 W CCM totem pole with 650 V CoolSiC™ in TOLL package and XMC™," 2024 Infineon Technologies AG, Application Note AN_2307_PL52_2308_140931

[5] C. Menditti Matrisciano, A. Laneve and D. Varajao, "Universal Isolated Gate Driving Platform for 650 V GaN HEMTs Half-Bridge with Dead-Time Control and Integrated Bias Supply," PCIM Europe 2023; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, Nuremberg, Germany, 2023, pp. 1-9, doi: 10.30420/566091152

[6] R. G. Mora, Y. Haksoz, E. Persson, “How to parallel CoolGaN™ 600 V HEMT in halfbridge configurations for higher-power applications”, Infineon technologies AG, Engineering Report ER_1908_PL52_1910_100139

[7] “Infineon ISOFACE™ dual-channel digital isolators design guide”

[8] M. Escudero, M. -A. Kutschak, N. Fontana, N. Rodriguez and D. P. Morales, "Non-Linear Capacitance of Si SJ MOSFETs in Resonant Zero Voltage Switching Applications," in IEEE Access, vol. 8, pp. 116117-116131, 2020

[9] A. Laneve, “CoolGaN™ hybrid driving evaluation board with EiceDRIVER™ 1EDB7275F and 1EDN7550B,” Infineon Technologies AG

[10] A. Laneve, A. Rossi, D. Varajao, “A Non-Isolated and Cost-Effective Hybrid Driving Solution for High Voltage GaN HEMTs”, APEC 2024

Acronyms/abbreviations

Table 8 Acronyms/abbreviations

Acronym	Description
ACLDO	AC line-cycle drop-out
BW	bandwidth
BTM	bottom
CCM	continuous conduction mode
DFF	duty-cycle feed-forward
FB	full-bridge
GaN	gallium nitride
HB	half-bridge
HV	high voltage
iTHD	input current total harmonic distortion
LCDO	line cycle drop out
LDO	low dropout voltage regulator
LLC	series parallel resonant converter
OCP	overcurrent protection
OVP	overvoltage protection
PF	power factor
PFC	power factor correction
PSU	power supply unit
PWM	pulse width modulation
Si	silicon
SiC	silicon carbide
SMPS	Switched Mode Power Supply
SR	synchronous rectification
THD	total harmonic distortion
UVLO	undervoltage lockout
UVP	undervoltage protection
WBG	wide bandgap

Revision history

Document revision	Date	Description of changes
V 1.0	2024-09-05	Initial release
V 2.0	2025-01-17	Fixed typo in Table 2
V 3.0	2025-09-23	Updated Figure 4, Figure 17, Figure 21, Figure 61, and Figure 62

Trademarks

All referenced product or service names and trademarks are the property of their respective owners.

Edition 2025-09-23

Published by

Infineon Technologies AG

81726 Munich, Germany

Do you have a question about this document?

Email: erratum@infineon.com

Document reference

AN145544