1ED21x7x Family Application Note

About this document

Scope and purpose

1ED21x7x family is the latest gate driver designed with Infineon's 2nd-generation high-voltage silicon-on-insulator (SOI) technology. This application note compliments the 1ED21x7x family datasheet[1], and highlights the unique features of the new gate driver, when compared with existing IR2127[2] and IRS2127[3] families. In addition, a step by step guide is provided to help customers design their over current protection circuit.

Intended audience

- Engineers who want to learn about new features of 1ED21x7x family
- Design engineers looking for guidance on the design of de-sat circuit, for over current protection

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1 Introduction

1ED21x7x family is the latest gate driver designed with Infineon's 2nd-generation high-voltage SOI technology. Compared with previous part number such as IR2127 and IRS2127 families, 1ED21x7x can now deliver much faster propagation delays in the range of 50 ns, as well as much higher driving current rated at 4 A typical.

The floating channel in 1ED21x7x can be used to drive an Si / SiC power MOSFET or IGBT in the high-side or low-side configuration which operates up to 650 V. Based on Infineon's SOI technology there is an excellent ruggedness and noise immunity with capability to maintain operational logic at negative transient voltages up to -100 V.

The over-current protection (OCP) and under-voltage lockout (UVLO) circuity detects over-current / under-voltage in the driven power transistor and terminates the gate drive output voltage. A multi-function RFE pin can indicate that an over-current shutdown has occurred, provide programmable fault clearance time, as well as shutdown function.

Table 1 below lists various options with different UVLO and CS (current sensing) thresholds, suitable to drive IGBTs or Si / SiC MOSFETs.

Table 1 1ED21x7x family lead definitions

Base part number	Target transistor	Typ. UVLO-Thresholds	Typ. CS Thresholds	Package
1ED2127S65F	IGBT / SiC MOSFET	10.0 V / 8.7 V	0.24 V	PG-DSO-8
1ED21271S65F	Si MOSFET	7.2 V / 6.8 V	1.78 V	PG-DSO-8
1ED2147S65F	Si MOSFET	7.2 V / 6.8 V	0.24 V	PG-DSO-8
1ED21471S65F	IGBT / SiC MOSFET	10.0 V / 8.7 V	1.78 V	PG-DSO-8

2 Pin Description

2.1 Pin configuration

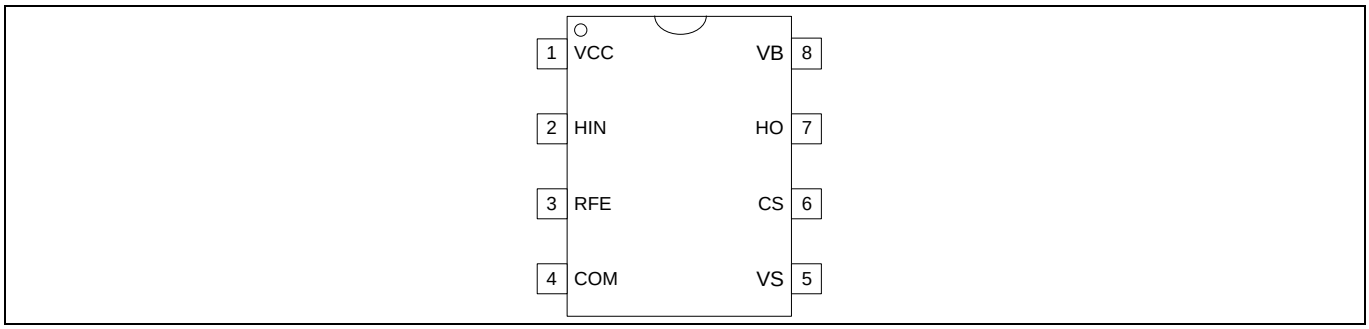


Figure 1 1ED21x7x family pin assignments (top view)

2.2 Pin functionality

Table 2 1ED21x7x family lead definitions

Pin no.	Name	Function
1	VCC	Low-side and logic supply voltage
2	HIN	High-side logic input, in phase with HO
3	RFE	Multi-function pin 1) for logic input to enable I/O functionality, 2) fault reporting of high-side over-current, and 3) programmable fault clear timer with external R/C components.
4	COM	Low-side gate drive return
5	VS	High-side negative power supply
6	CS	Current sense input for over current protection
7	HO	High-side driver output
8	VB	High-side gate drive floating supply

3 Improvements over IR2127 and IRS2127

3.1 Faster propagation delay

Table 3 shows the comparison of Ton and Toff propagation delays, between in the existing IR2127, IRS2127 and new 1ED21x7x families. This great improvement is achieved by the ultra-fast level-shift circuit implemented with Infineon's 2nd-generation high-voltage SOI technology.

Table 3 Comparison of typical Ton and Toff

Parameter	Symbol	IR2127	IRS2127	1ED21x7x
Turn-on propagation delay	Ton	200 ns	150 ns	55 ns
Turn-off propagation delay	Toff	150 ns	150 ns	55 ns

The short Ton and Toff are especially beneficial for application with high switching frequency. In addition, this will also allow the driver to shut down quickly in over current condition, which is critical for power switches with less robust short circuit ratings.

3.2 Higher driving current

The driving capability of 1ED21x7x has also been significantly improved. Table 4 shows the comparison on I_{O+} and I_{O-}.

Table 4 Comparison of Ton and Toff

Parameter	Symbol	IR2127	IRS2127	1ED21x7x
Peak output current turn-on	I_{O+}	250 mA	290 mA	4 A
Peak output current turn-off	I_{O-}	500 mA	600 mA	4 A

The higher driving current will enable customers to drive power switches with higher current rating, or multiple power switches in parallel, without adding separate output buffer circuit. For reference, the output characteristic of 1ED21x7x is illustrated in Figure 2.

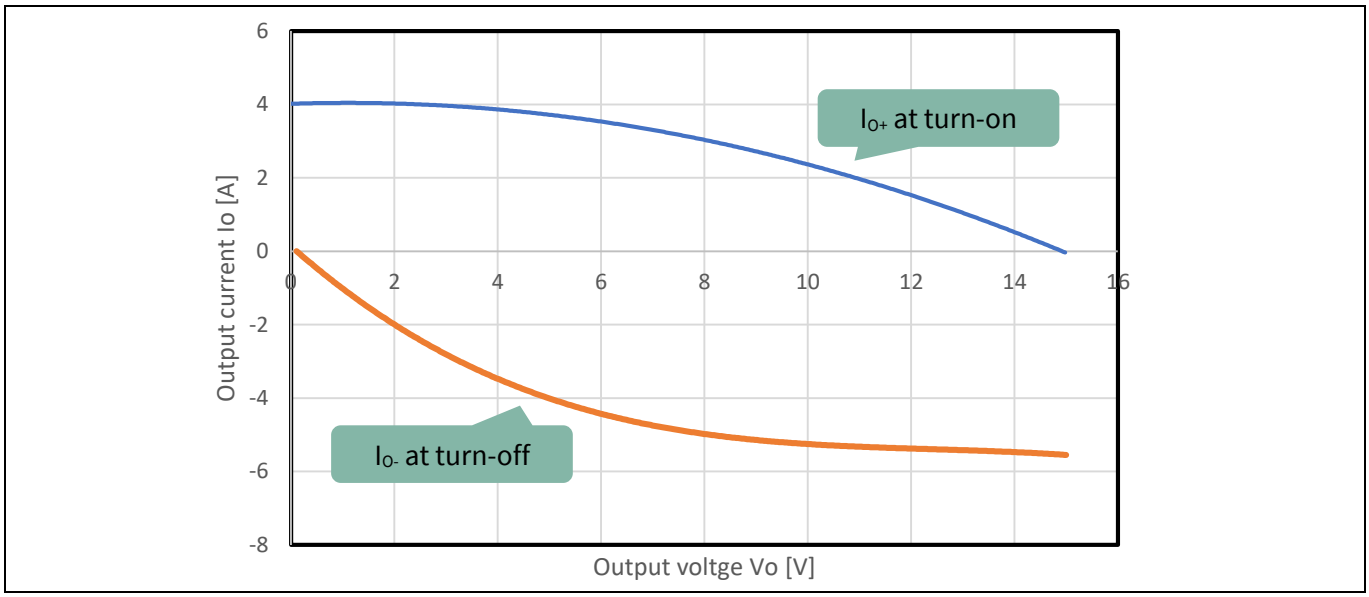


Figure 2 Gate driver output current vs. output voltage

3.3 Better noise immunity

In the original IR2127 and IRS2127, the capacitor C3 between CS and VS can be spuriously charged by dv/dt events while power switch Q1 is off due to the high impedance of the CS pin, as shown in Figure 3. This can cause false triggering of over current protection, especially for the version with 0.25 V CS threshold.

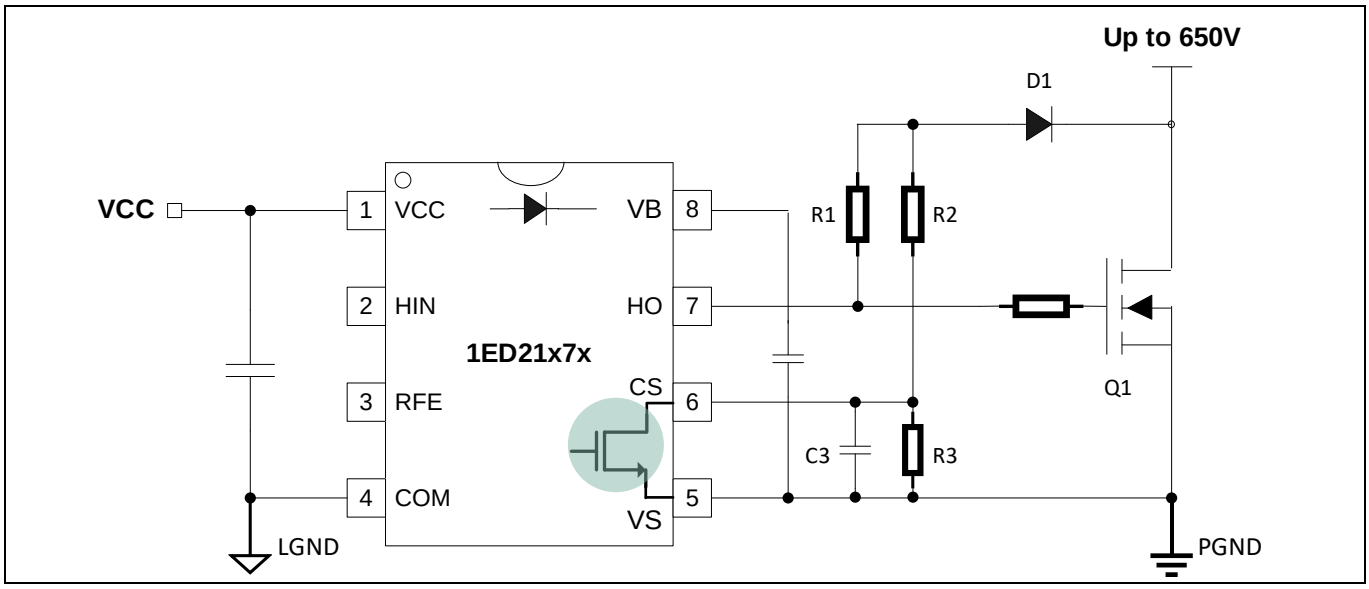


Figure 3 Over-current protection with de-sat detection circuit and internal CS-to-VS FET

In the new 1ED21x7x, we have added an internal FET between CS and VS, as highlighted in Figure 3. This FET has Rdson of 20Ω, and it remains on when HO is low, which help to short C3 to VS when Q1 is off. Only when HO is active, the FET will open and allow CS voltage to rise. The sequence of events is described in detail in section 4.2 and 4.3.

3.4 Integrated bootstrap diode

The 1ED217 features a monolithically integrated bootstrap diode and resistor, unlike the previous IR2127 and IRS2127. This saves the cost and PCB area in customer design, especially in three-phase application.

The behaviour of this bootstrap diode is well documented in [4].

4 Over current protection

4.1 Type of short circuits

In a typical motor drive application as shown in the Figure 4 below, three are mainly three types of short circuits.

1. **Inverter shoot-through**. This can be caused by the turn-on of both high-side and low-side power switches simultaneously in one of the inverter legs, which in turn can result from electromagnetic interference or a malfunction in the controller or gate driver. It could also be caused by wear out and failure of one of the power switches in the leg.
2. **Phase-to-phase short-circuit**. This can be caused by insulation breakdown in the motor between windings due to degradation, overtemperature, or overvoltage events.
3. **Phase-to-earth short-circuit**. This can be caused by insulation breakdown between a motor winding and the motor casing, usually due to degradation, overtemperature, or overvoltage events.

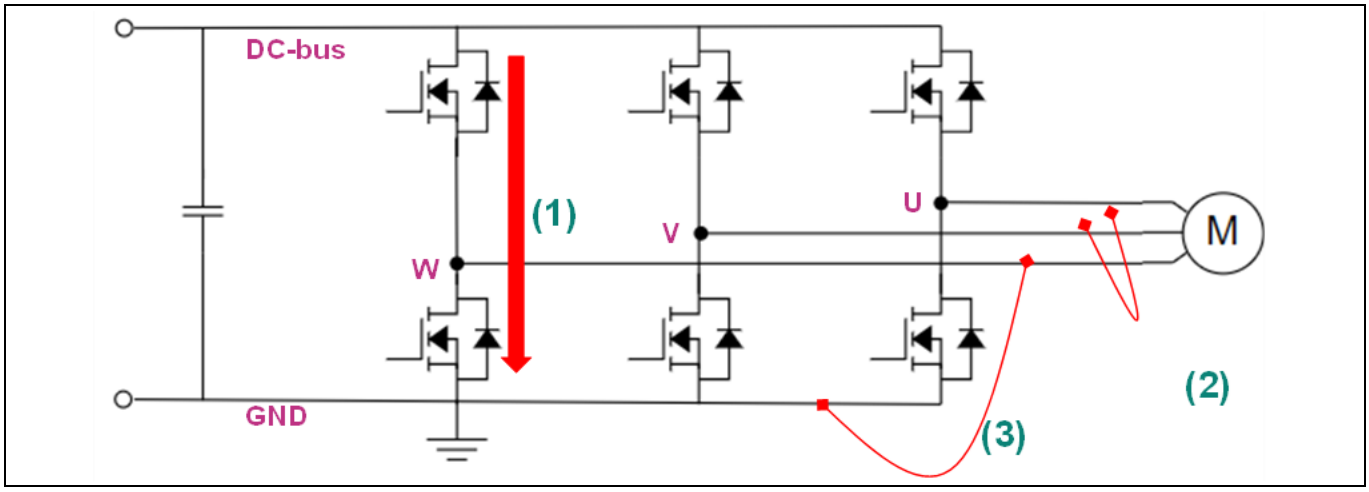


Figure 4 Possible short circuit

While a typical low side shunt resistor can detect the over current condition in the negative DC bus, therefore protect against the first two types of short circuit, it cannot act when phase-to-earth short-circuit happens, because the over current condition may only happen in the high-side switches. In addition, in high power applications, the losses and cost of shunt resistor remain as a design challenge. This is where de-sat protection can be a viable option, for both the high-side and low-side switches.

In addition to the three types of short circuit list above, classified by ***where*** the short circuit happens, there are also different types classified by ***when*** short circuit happens. This is commonly referred as type 1 and type 2 short circuit. The 1ED21x7x gate driver will have different response time due the different blanking time, based on the de-sat detection circuit shown in Figure 5.

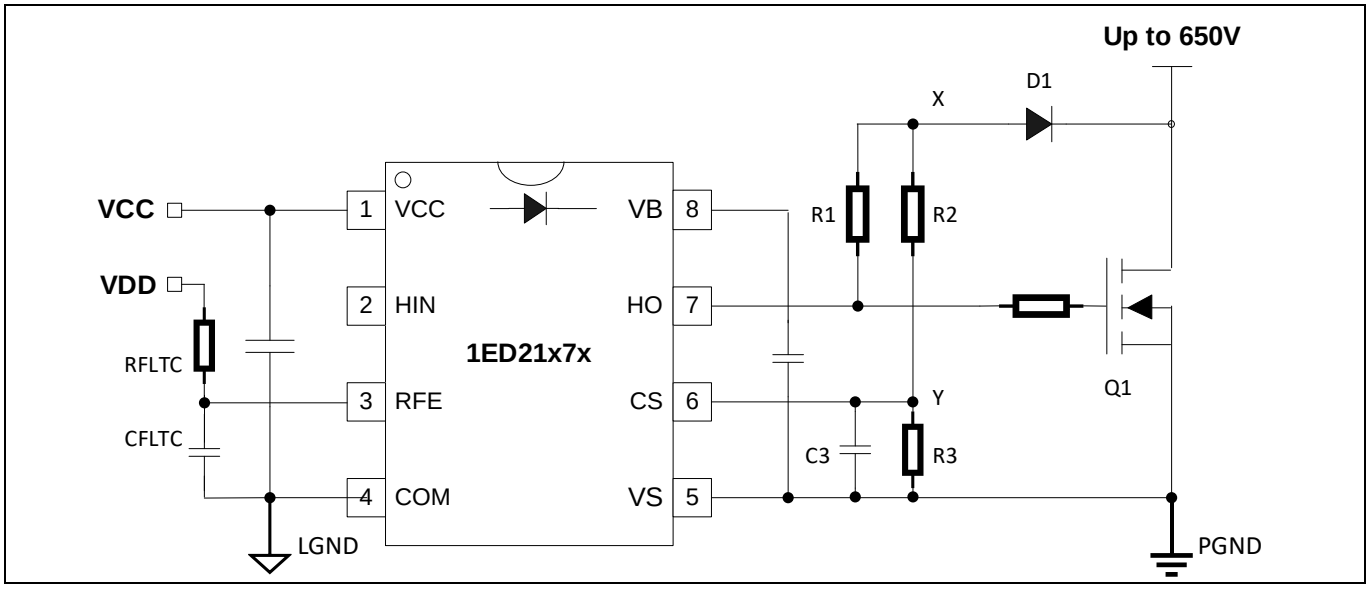


Figure 5 Over-current protection with de-sat detection circuit

4.2 Type 1 short circuit: de-sat protection sequence

Type 1 short circuit happens when short happens before power switch is turned on. Figure 6 shows the sequence of action in type 1 short circuit.

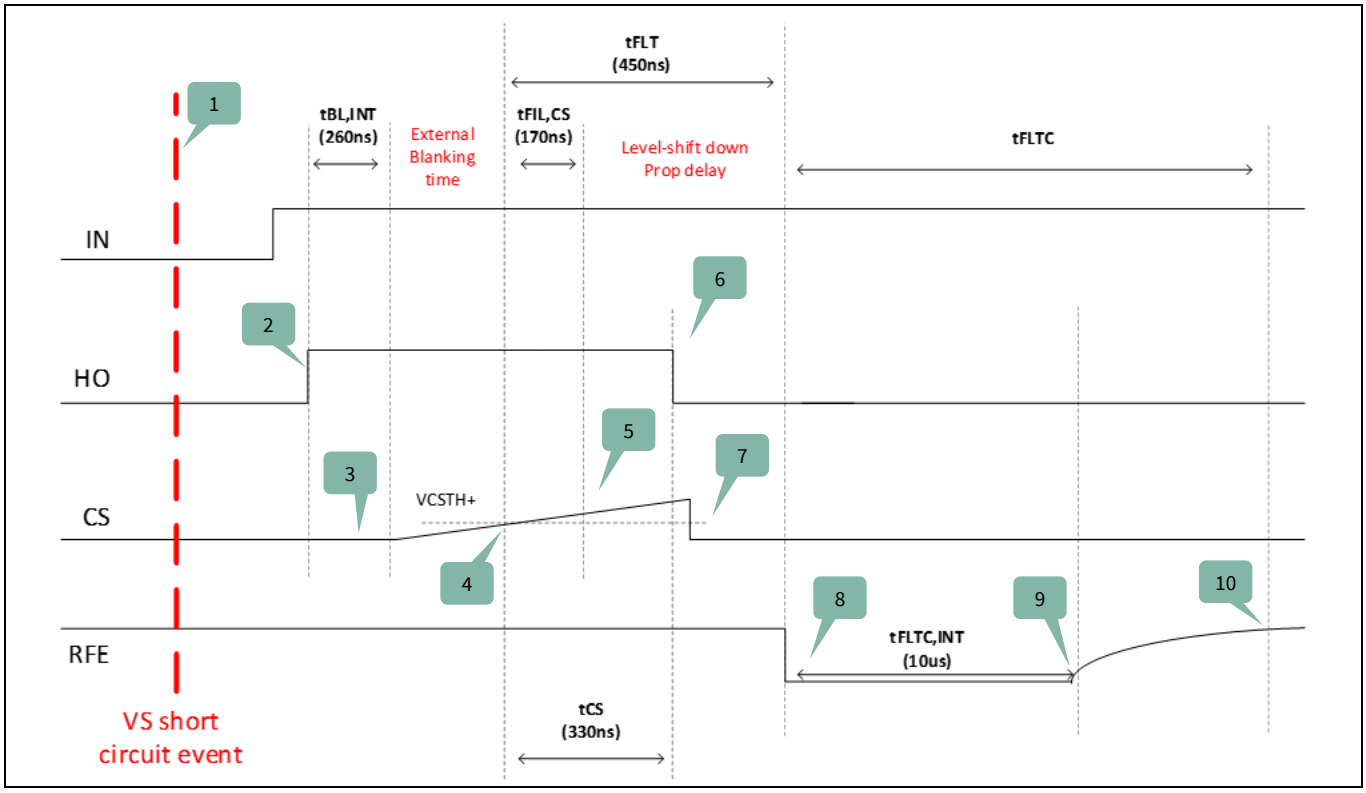


Figure 6 Type 1 short circuit timing sequence

Over current protection

Here the protection sequences.

1. Short circuit happened before HO is turn on.
2. Short circuit current started to rise after HO is on.
3. CS is kept low during the first 260 ns blanking time ($t_{BL, INT}$) after HO is on. During this period, the internal FET between CS and VS remains ON which is important to prevent any false triggering due to noise. At the end of 260 ns blanking time, CS will start to rise.
4. CS voltage reached V_{CSTH+}, after the internal blanking (260 ns) and external filter (with R3 * C3) time.
5. De-sat protection is triggered after the 170 ns CS filter time ($t_{FIL, CS}$),
6. HO is turned off after 330 ns of t_{CS}. Short circuit is disrupted.
7. CS is low since short circuit is cleared.
8. Fault signal transmitted from high side to low side, with RFE signal pulled low.
9. Internal fault clear time of 10 us ($t_{FLTC, INT}$).
10. External fault clear time, programs by RFLTC and CFLTC on RFE pin.

In type 1 short circuit, the total time with short circuit current is:
260 ns ($t_{BL, INT}$) + 330 ns (t_{CS}) = 590 ns plus external filter (R3 * C3)

Figure 7 shows the measured waveform of Type 1 short circuit. In this case, the short circuit lasted total of approximately 740 ns, which also includes the external R3 * C3 filter time.

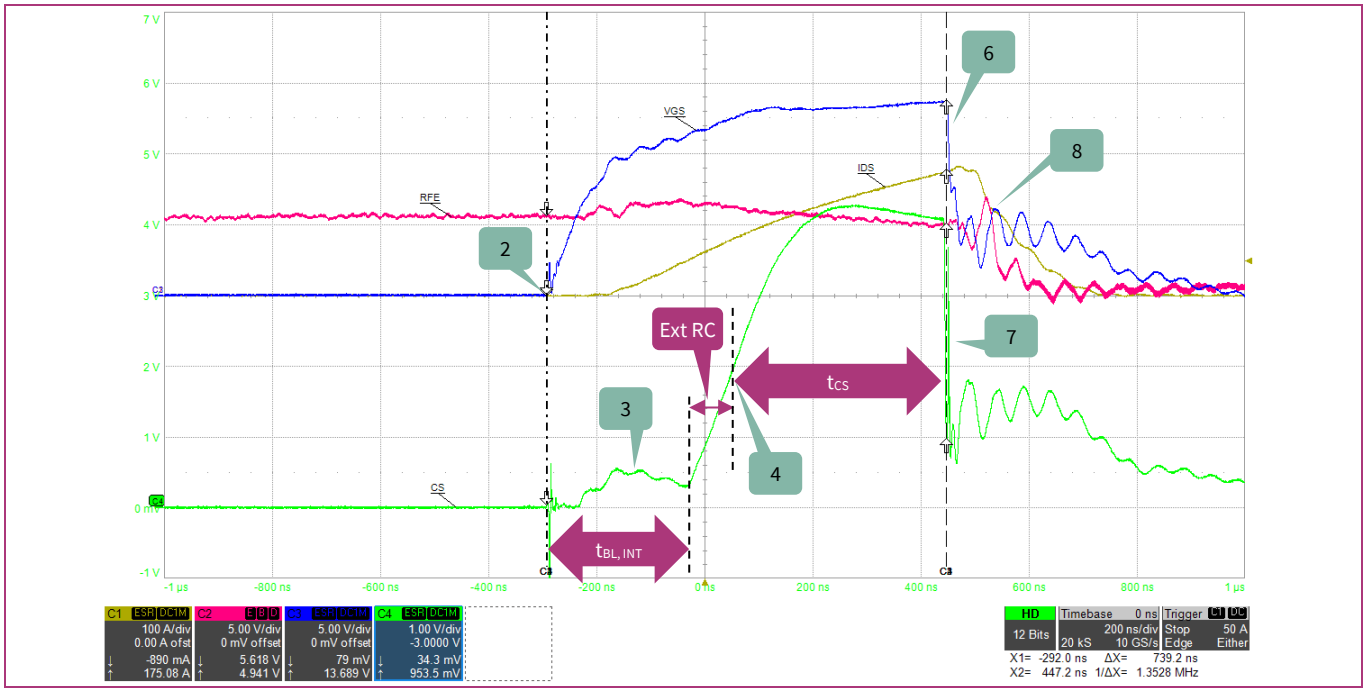


Figure 7 Waveform of type 1 short circuit

- CH1: Short circuit current in power switch Q1
- CH2: RFE to COM voltage
- CH3: V_{GS} of power switch Q1
- CH4: CS to VS voltage

4.3 Type 2 short circuit: de-sat protection sequence

In type 2 short circuit, the short circuit happens when the power switch is in the ON state, as shown in Figure 8 below.

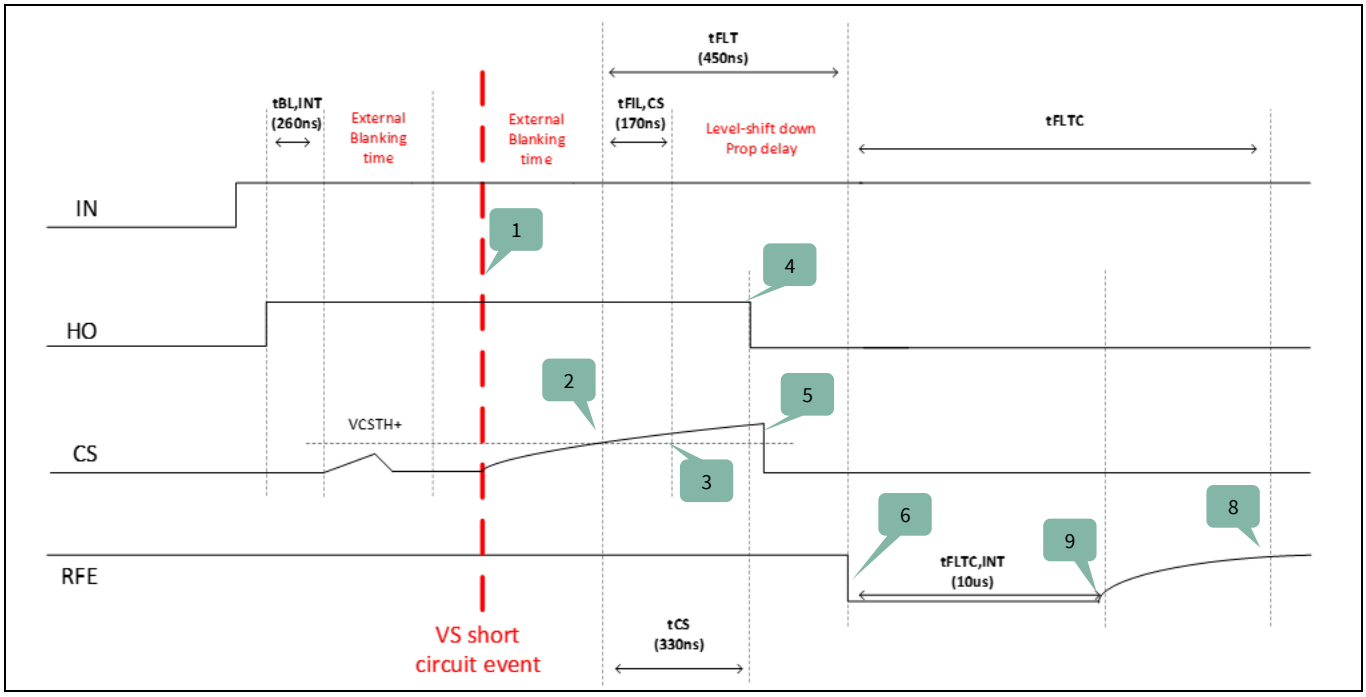


Figure 8 Type 2 short circuit timing sequence

Here the protection sequences.

1. Short circuit happened after HO is turn on, and after the 260 ns blanking time. Short circuit current started to rise. CS voltage start to increase immediately.
2. CS voltage reached V_{CSTH+}, after the external filter (with R3 * C3) time.
3. De-sat protection is triggered after the 170 ns CS filter time,
4. HO is turned off after 330 ns of t_{CS}. Short circuit is disrupted.
5. CS is cleared since short circuit is cleared.
6. Fault signal transmitted from high side to low side, with RFE signal pulled low.
7. Internal fault clear time of 10 us
8. External fault clear time, programs by RFLTC and CFLTC on RFE pin.

In type 2 short circuit, the total time with short circuit current is:
330 ns (t_{CS}) plus external filter (R3 * C3)

Therefore, the de-sat protection time will be quicker in the case, compared with Type 1 short circuit.

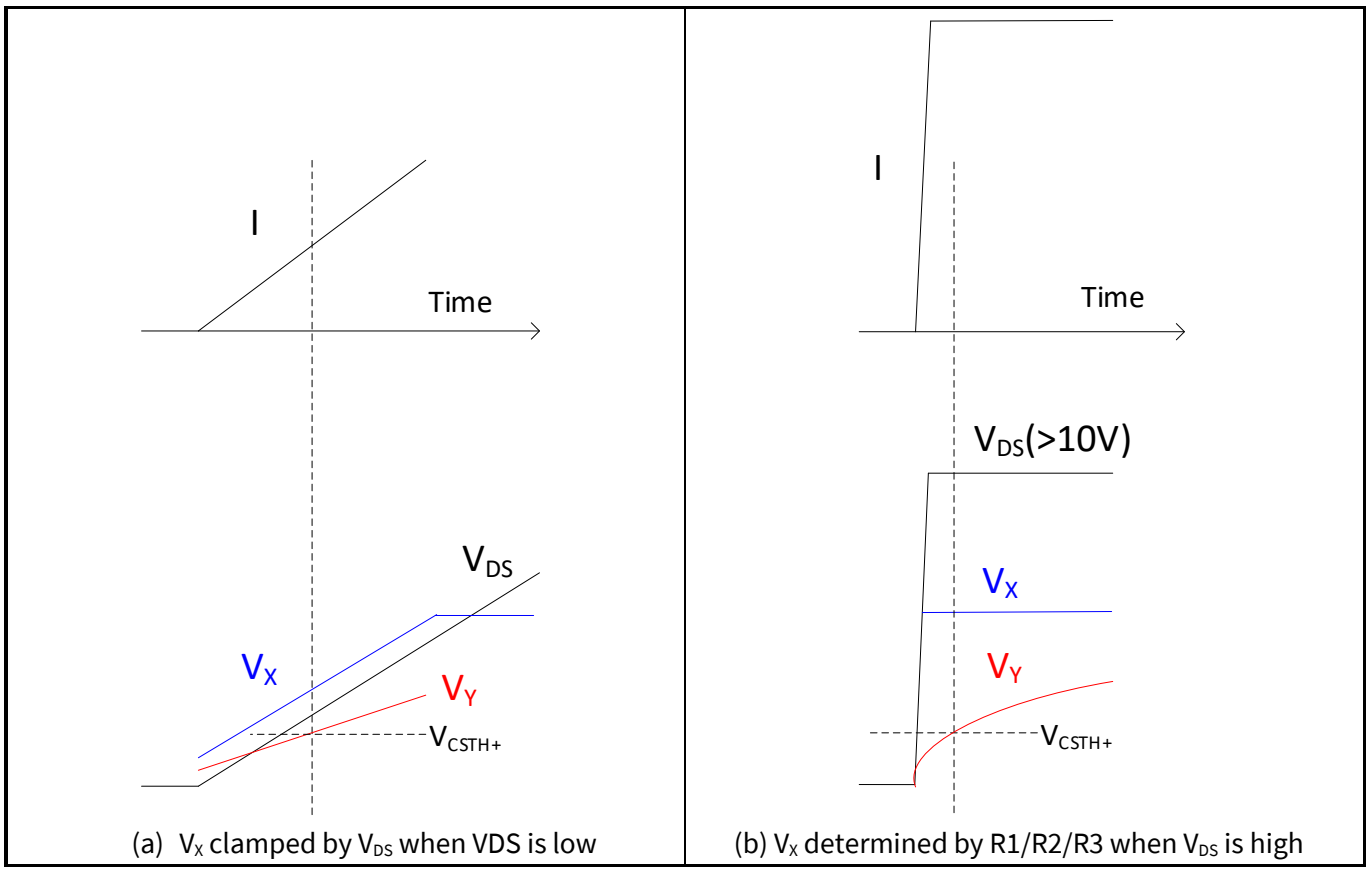
4.4 Over current protection circuit design steps

The 1ED21x7x family has two CS threshold options: 0.25 V and 1.8 V. The 0.25 V option is often used with shunt resistor, in order to minimize the voltage drop across the shunt and its power losses. For the circuit with de-sat diode, 1.8 V option is recommended due to better noise immunity.

In the example below, we will focus on the design steps to choose the R and C values for the over current protection circuit, as shown in Figure 5 above.

Over current protection

It is worthwhile to point out there are two modes of operation, depending on the V_{DS} voltage of power switch Q1. As shown in the Figure 9 (a) below, the voltage at X is clamped by V_{DS_Q1} (plus V_F of de-sat diode D1) when V_{DS_Q1} voltage is low. Voltage at Y is set by the voltage divider of R2 and R3, which should be less than 1.8 V threshold. In this condition when Q1 current rise gradually, the voltage at Y will slowly rise to 1.8 V when CS will be triggered. We will call this mode as slow mode.



(a) V_X clamped by V_{DS} when VDS is low (b) V_X determined by R1/R2/R3 when V_{DS} is high

Figure 9 1ED21x7x de-sat circuit

By comparison in the short circuit condition, both current and V_{DS} voltage rise rapidly, as shown in Figure 9 (b). In this case, the voltage at X will no longer be clamped by V_{DS} of Q1 due to the de-sat diode D1. Instead, it will be determined by voltage divider R1 / R2 / R3 of HO. In order to rapidly drive V_Y in this condition, it is import to set voltage divider of R1+R2 and R3 to more than 1.8 V. Otherwise, it will take **a very long time** to charge C3 to reach 1.8 V even though the VDS of Q1 is already at >100 V. The suggested overdrive voltage is 2x V_{CSTH+} = 3.6 V, which will result in 0.7 * R3 * C3 filter time to reach V_{CSTH+} in case of short circuit. This mode will be referred as fast mode.

In the actual design procedure, we can start from either slow mode or fast mode. However, it is critical to ensure both modes will work as intended in customer application.

Table 5 shows the one example of input condition, starting from slow mode.

Table 5 Example 1: Input condition for de-sat circuit design with 60A OCP threshold

Parameter	Symbol	Slow mode	Fast mode	Notes
V_{DS} of power switch Q1	V_{DS_Q1}	***2.4 V***	5.4 V	$V_{DS_Q1} = V_X - V_{F_D1}$
Voltage at Y	V_Y	1.8 V	3.6 V	2x of 1.8 V CS threshold for overdrive
Forward drop of de-sat diode D1	V_{F_D1}	0.6 V	0.6 V	
Voltage at X	V_X	3.0 V	6.0 V	$V_X = V_{DS_Q1} + V_{F_D1}$ 2x of V_X in fast mode

In the table above, we start with 2.4 V of V_{DS_Q1}, which can be calculated with intended over current protection threshold, for example 60 A with RDSON of 40mohm. This will lead to 5.4 V V_{DS_Q1} during the short circuit.

We can also start with 9V of de-sat voltage for Q1 in fast mode, as shown in Table 6 below.

Table 6 Example 2: Input condition for de-sat circuit design with 9V de-sat voltage threshold

Parameter	Symbol	Slow mode	Fast mode	Notes
V_{DS} of power switch Q1	V_{DS_Q1}	4.0 V	***9.0 V***	$V_{DS_Q1} = V_X - V_{F_D1}$
Voltage at Y	V_Y	1.8 V	3.6 V	0.5x of 1.8 V CS threshold in slow mode
Forward drop of de-sat diode D1	V_{F_D1}	1.0 V	1.0 V	
Voltage at X	V_X	5.0 V	10.0 V	$V_X = V_{DS_Q1} + V_{F_D1}$ 0.5x of V_X in slow mode

In this case, the corresponding V_{DS_Q1} during slow mode will be 4.0 V. Therefore, it is important to ensure V_{DS_Q1} should not reach 4.0 V during normal operation.

After the input conditions are finalized, below are the steps for select R and C components. We will use the fast mode since this is where R1 + R2 and R3 voltage divider is working. For simplicity, we will also assume V_{HO}-to-V_S voltage will be same as V_{CC} and V_{BS}.

Step 1: R1

R1 is chosen to minimize the increased miller capacitance effect from diode D1, and makes sure there is not significant current (V_{HO} - V_X) / R1 being drawn from the HO output. Assuming we want to limit the current to be less than 1 mA, R1 will be 15kohm for V_{CC} = 15 V.

Step 2: R2 and R3

R2 and R3 can be calculated to have 3.6 V at Y, with the R1 value selected in step 1. In this example, we can calculate R2 = 19.2 kΩ and R3 = 10.8 kΩ.

Step 3: C3

C3 should be selected to minimize the charging time during the short circuit condition. The time constant will be R3 || (R1 + R2) * C3. We can select C3 = 22pF which will give us time constant of 180 ns.

It should also provide fast discharged time when CS is shorted to VS during OFF period. The time constant for discharge is $R_{ON,CS}$ * C3 = 20 Ω * 22 pF = 0.4 ns.

Step 4: Double check V_X, V_Y at whole V_{CC} range

It is important to check the over drive voltage at V_Y is acceptable during the whole V_{CC} / V_{BS} range. Table 7 shows the condition of V_X and V_Y for the 2nd example described above.

Table 7 De-sat threshold changes with Vic

Parameter	Symbol	V_{CC} = 12 V	V_{CC} = 15 V	V_{CC} = 18 V	Notes
Voltage at Y	V_Y	2.9 V	3.6 V	4.3 V	VY = VCC * R3 / (R1 + R2 + R3)
Voltage at X	V_X	8.0 V	10.0 V	12.0 V	VX = VY * R2 / R3
V_{DS} of power switch Q1	V_{DS_Q1}	7.0 V	9.0 V	11. 0V	VX + VF_D1

When V_{CC} is lower at 12V, the de-sat voltage with be 7.0 V instead of 9.0 V as in the case of V_{CC} = 15 V.

In addition, the over drive voltage at Y is 2.9 V which means it will take slightly longer for V_Y to reach 1.8V compared with V_{CC} = 15 V condition. However, this should still be acceptable.

When V_{CC} is higher than 15V, the de-sat voltage will also be higher at 11.0 V. And it will take less time for V_Y to charge up.

Unlike the over drive voltage in fast mode, it does not change with V_{CC} voltage in slow mode. As long as the V_Y is 1.8 V, V_X will be 5 V as determined by R2 and R3, and V_{DS_Q1} will be 4.0 V.

Step 5: D1

De-sat diode D1 should be selected to have the same characteristics as the bootstrap diode.

4.5 Enable, fault reporting and programmable fault clear timer (RFE)

In case of over-current, the HO output will be turned off. In addition, the fault condition will be triggered, as shown in both Figure 6 and Figure 8. Once the fault condition occurs, the RFE pin is internally pulled to COM and the fault clear timer is activated. The RFE output stays in the low state until the fault condition has been removed, plus 10 us ($t_{FLTC, INT}$), After this, the voltage on RFE pin will start to rise. The total length of the fault clear time period (t_{FLTC}) is determined by exponential charging characteristics of the capacitor where the time constant is set by R_{FLTC} and C_{FLTC} as shown above in Figure 5.

The design guidelines for this network are listed in Table 8.

Table 8 Design guideline for external RC components

External RC components	Typical value	Notes
R_{FLTC}	0.5 MΩ to 2 MΩ	>> $R_{ON, RFE}$
C_{FLTC}	<= 1 nF	Ceramic

The length of the fault clear time period can be calculated by using the formula below.

$$t_{FLTC} = - (R_{FLTC} * C_{FLTC}) * \ln(1 - V_{IH, RFE} / V_{DD}) + t_{FLTC, INT}$$

The voltage on the RFE pin should not exceed the V_{DD} of the uC power supply.

In addition to the fault reporting and programmable fault clear timer as described above, the same RFE pin also provides enable functionality, which allows the driver to be disabled or enabled by the uC. The timing parameter of shutdown function is listed in the table below.

Table 9 RFE shutdown timing parameter

Parameter	Symbol	Values			Unit	Test condition
		Min.	Typ.	Max.		
RFE low to shutdown propagation delay	t_{SD}	-	60	85	ns	$V_{RFE} < V_{IL, RFE}$ to OUT 90% fall

The shutdown function is useful when all RFE pins are connected together, for example in a three-phase inverter where six of 1ED21x7x gate drivers are used. In this case, all six power switches will be turned off in less than 85ns after over current is detected in one switch.

5 Ruggedness

5.1 NTSOA

In a typical motor drive system, dV/dt is typically designed to be in the range of 3 ~ 5 V/ns. The negative VS transient voltage can exceed this range during some events such as short circuit and over-current shutdown, when di/dt is greater than in normal operation.

Infineon's HVICs have been designed for the robustness required in many of today's demanding applications. An indication of the 1ED21x7x's robustness can be seen in Figure 10, where the 1ED21x7x's Safe Operating Area is shown at V_{CC} = V_{BS} =15 V based on repetitive negative VS spikes. A negative VS transient voltage falling in the grey area (outside SOA) may lead to IC permanent damage; vice versa unwanted functional anomalies or permanent damage to the IC do not appear if negative Vs transients fall inside the SOA.

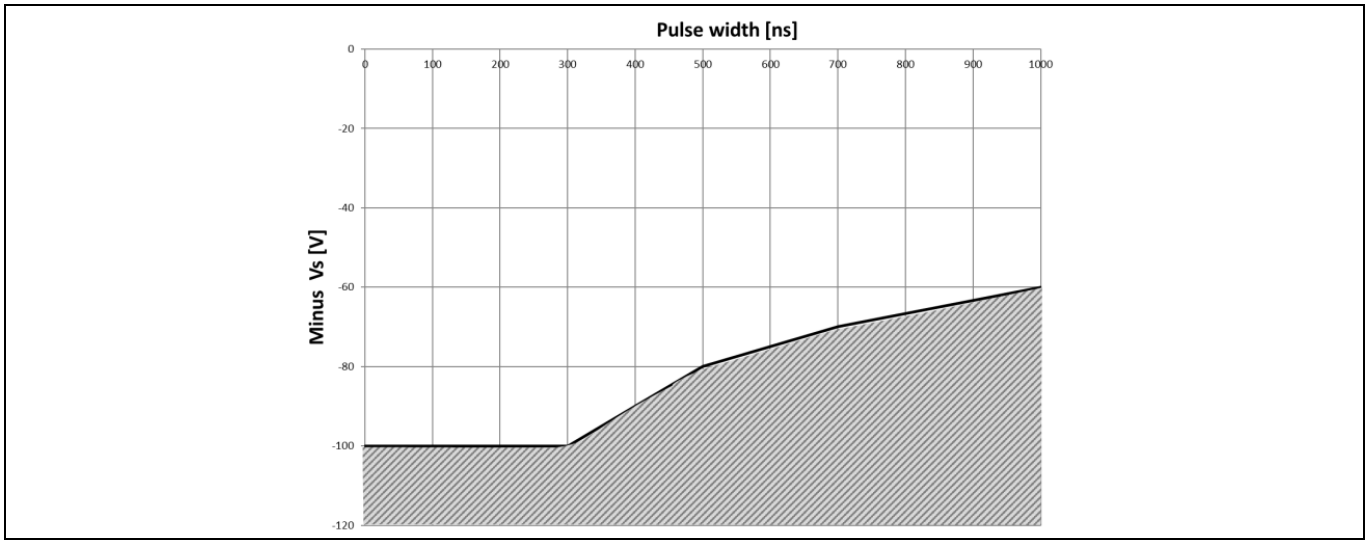


Figure 10 Negative VS transient SOA for 1ED21x7x @ V_{CC} = V_{BS} = 15 V, T_A = 25 °C

In actual test, 1ED21x7x has been shown able to handle even larger negative VS transient outside the SOA, such as the waveform shown in Figure 11. However, please note this is for reference only. Therefore, it is highly recommended that customers always limit the negative VS transients as much as possible by careful PCB layout and component selection.

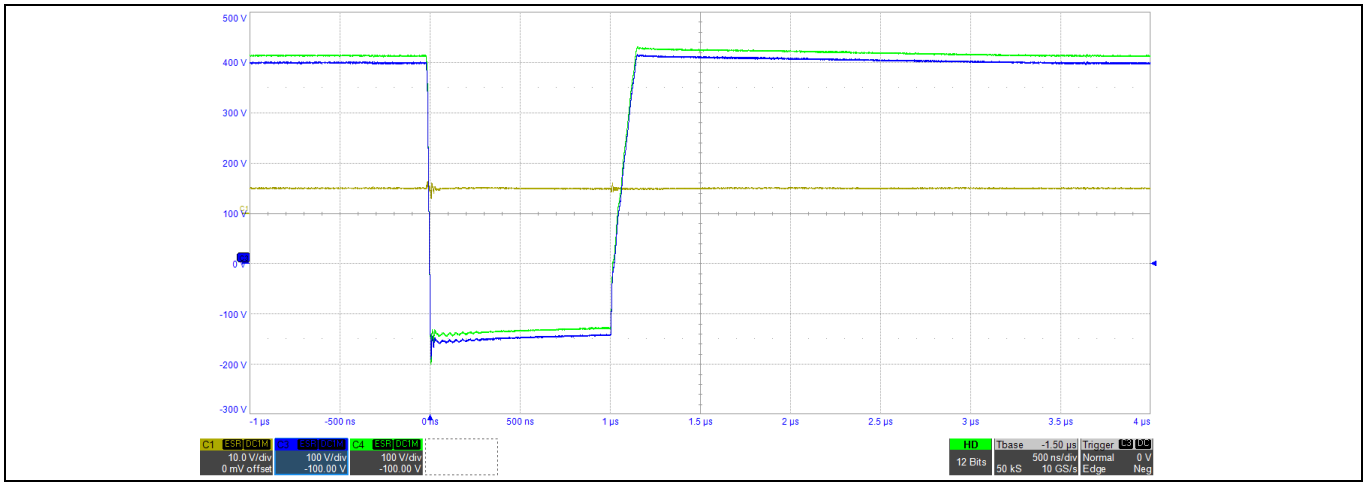


Figure 11 Negative Vs test at 140 V and 1 us

- CH1: RFE to COM voltage
- CH3: VS to COM voltage
- CH4: HO to COM voltage

5.2 dV/dt

While the typical motor drive has dV/dt in the range of 3 ~5 V/ns as mentioned above, it is common to have faster switching transition in different applications such as PFC (power factor correction) circuit, especially when driving wide bandgap devices. It is also plausible to switch slower in other conditions, in order to reduce EMI noises. The 1ED21x7x has been verified to work between 0.3 V/ns to 50 V/ns, as shown in the waveform below.

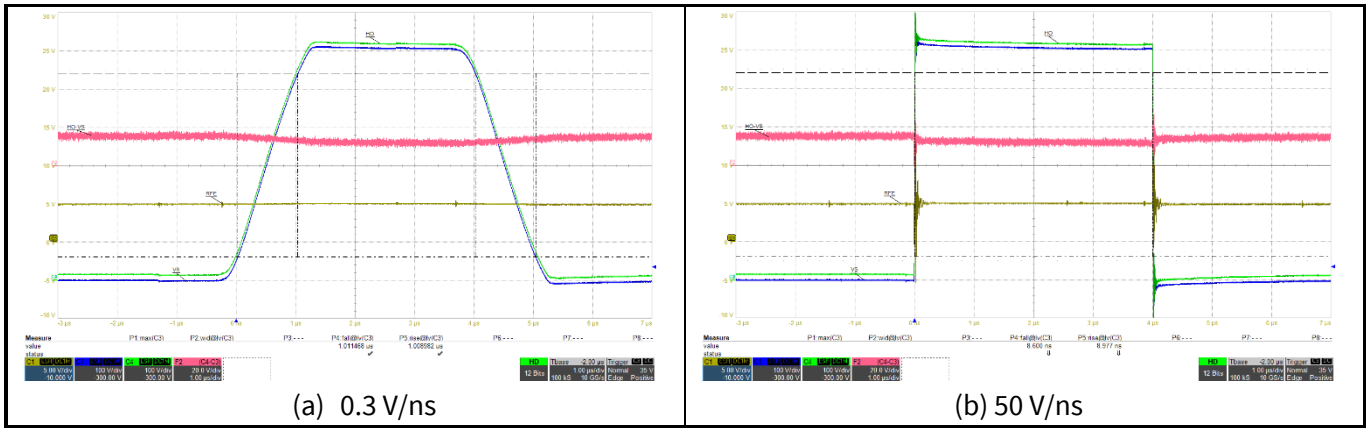
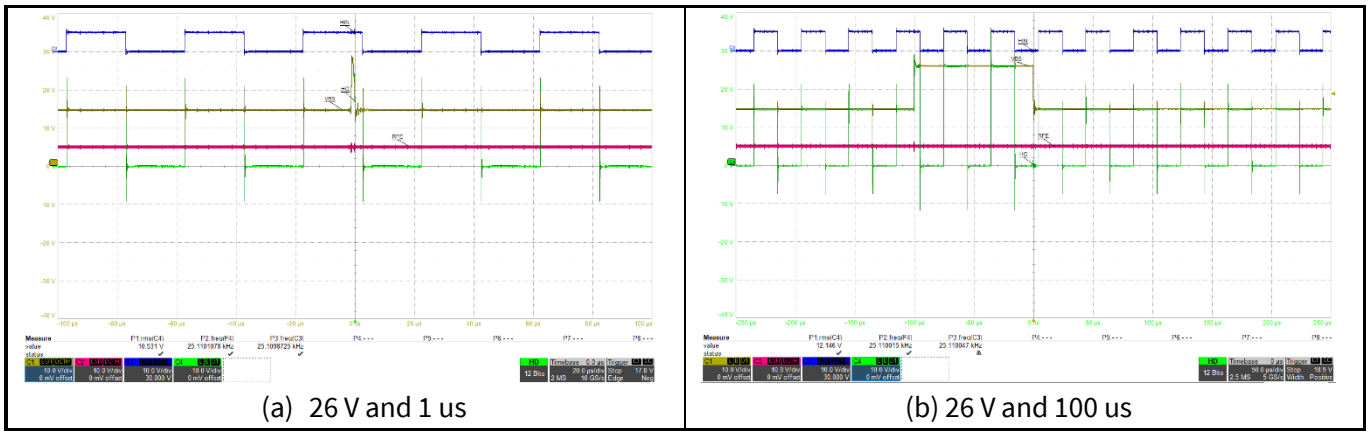


Figure 12 dV/dt test

- CH1: RFE to COM voltage
- CH3: VS to COM voltage
- CH4: HO to COM voltage
- F2: HO to VS voltage

5.3 V_{CC} and V_{BS} Surge

In addition to the minus VS and dv/dt test as described above, 1ED21x7x has also been tested with surge voltage on V_{CC} and V_{BS}, with pulse width at 1us, 10us, and 100us, up to the absolute maximum rating of 2 5V and above. For example, Figure 13 shows the V_{BS} surge from 15V to 26V, for 1us and 100us respectively.



(a) 26 V and 1 us (b) 26 V and 100 us

Figure 13 V_{BS} surge test

- CH1: VB to VS voltage
- CH2: RFE to COM voltage
- CH3: HIN to COM voltage
- CH4: HO to VS voltage

References

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Revision history

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