12 kW high power density and high frequency PSU for AI data centers and servers

REF_12KW_HFHD_PSU

About this document

Scope and purpose

This document introduces a new, complete power supply unit (PSU) for AI data centers and servers.

Intended audience

The document is intended for R&D engineers, hardware designers, and developers of power electronic systems.

Keypoints

- Presents a 12 kW PSU reference design achieving 113 W/in^3 power density and >97% efficiency for AI data centers
- Details two-stage architecture using 3-level flying capacitor PFC and full-bridge LLC converter for compact high-power conversion
- Introduces an auxiliary energy buffer circuit enabling 20 ms hold-up time and grid shaping during transients for improved reliability
- Highlights integration of CoolSiC™, CoolGaN™, and CoolMOS™ devices for optimized switching performance and thermal management
- Provides experimental validation of efficiency, dynamic response, EMI compliance, and thermal behavior under demanding AI workloads

About this product family

Product family

Infineon's 12 kW high-density PSU reference design combines Si, SiC, and GaN technologies to deliver exceptional efficiency and power density. Ideal for AI data center and server power racks, it supports machine learning accelerators and compute-intensive applications.

Target applications

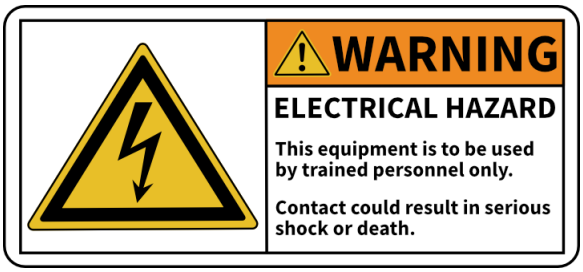
- AI data centers
- High-performance server power racks
- Compute-intensive workloads with rapid load transients
- Cloud infrastructure requiring grid current shaping and hold-up compliance
- Large-scale GPU clusters for machine learning and training tasks

Table of contents

Table of contents

Safety information

Please read this document carefully before starting up the device.



Important notice

Evaluation boards, demonstration boards, reference boards and kits are electronic devices typically provided as an open-frame and unenclosed printed circuit board (PCB) assembly. Each board is functionally qualified by electrical engineers and strictly intended for use in development laboratory environments. Any other use and/or application is strictly prohibited. Our boards and kits are solely for qualified and professional users who have training, expertise, and knowledge of electrical safety risks in the development and application of high-voltage electrical circuits. Please note that evaluation boards, demonstration boards, reference boards and kits are provided “as is” (i.e., without warranty of any kind). Infineon is not responsible for any damage resulting from the use of its evaluation boards, demonstration boards, reference boards or kits. To make our boards as versatile as possible, and to give you (the user) opportunity for the greatest degree of customization, the virtual design data may contain different component values than those specified in the bill of materials (BOM). In this specific case, the BOM data has been used for production. Before operating the board (i.e. applying a power source), please read the application note/user guide carefully and follow the safety instructions. Please check the board for any physical damage, which may have occurred during transport. If you find damaged components or defects on the board, do not connect it to a power source. Contact your supplier for further support. If no damage or defects are found, start the board up as described in the user guide or test report. If you observe unusual operating behavior during the evaluation process, immediately shut off the power supply to the board and consult your supplier for support.

Operating instructions

Do not touch the device during operation, keep a safe distance. Do not touch the device after disconnecting the power supply, as several components may still store electric charge and can discharge through physical contact. Several parts, like heatsinks and transformers, may still be very hot. Allow the components to discharge and cool before touching or servicing. All work such as construction, verification, commissioning, operation, measurements, adaptations, and other work on the device (applicable national accident prevention rules must be observed) must be done by trained personnel. The electrical installation must be completed in accordance with the appropriate safety requirements.

Safety precautions

Note: Please note the following warnings regarding the hazards associated with development systems.

Safety precautions

	**Warning:** *The evaluation or reference board contains DC bus capacitors, which take time to discharge after removal of the main supply. Before working on the converter system, wait five minutes for capacitors to discharge to safe voltage levels. Failure to do so may result in personal injury or death. Darkened display LEDs are not an indication that capacitors have discharged to safe voltage levels.*
	**Warning:** *The evaluation or reference board is connected to the AC input during testing. Hence, high-voltage differential probes must be used when measuring voltage waveforms by oscilloscope. Failure to do so may result in personal injury or death. Darkened display LEDs are not an indication that capacitors have discharged to safe voltage levels.*
	**Warning:** *Remove or disconnect power from the converter before you disconnect or reconnect wires or perform maintenance work. Wait five minutes after removing power to discharge the bus capacitors. Do not attempt to service the drive until the bus capacitors have discharged to zero. Failure to do so may result in personal injury or death.*
	**Caution:** *The heatsink and device surfaces of the evaluation or reference board may become hot during testing. Hence, necessary precautions are required while handling the board. Failure to comply may cause injury.*
	**Caution:** *Only personnel familiar with the converter, power electronics and associated equipment should plan, install, commission, and subsequently service the system. Failure to comply may result in personal injury and/or equipment damage.*
	**Caution:** *The evaluation or reference board contains parts and assemblies sensitive to electrostatic discharge (ESD). Electrostatic control precautions are required when installing, testing, servicing or repairing the assembly. Component damage may result if ESD control procedures are not followed. If you are not familiar with electrostatic control procedures, refer to the applicable ESD protection handbooks and guidelines.*
	**Caution:** *A converter that is incorrectly applied or installed can lead to component damage or reduction in product lifetime. Wiring or application errors such as under sizing the cabling, supplying an incorrect or inadequate AC supply, or excessive ambient temperatures may result in system malfunction.*

1 Background and specifications

1.1 Application background

The growing demand for power in AI applications has created a pressing need for power conversion solutions that are both highly efficient and compact. To support the development of next-generation data center infrastructure, power supplies must deliver high efficiency and high power-density. This requires the whole power conversion chain such as the AC-DC converter, the intermediate bus converter (IBC), and the voltage regulator module (VRM) stages to be capable of providing high power to the data processing hardware (e.g. GPUs) in a small form factor compared to past requirements.

The REF_12KW_HFHD_PSU reference design from Infineon demonstrates a viable approach for achieving higher power density and efficiency simultaneously in the AC-DC power conversion stage compared to current state-of-the-art solutions.

1.2 OCP ORv3 and the ORV HPR2 as a guideline

The Open Compute Project v3 5.5 kW specification [1] has been considered as the guideline for the efficiency profile and the dimensions of the unit during the design stage. To ensure a high power-density solution that is viable, the output power has been increased to 12 kW but in a lower volume, which has been tightened from 40 mm × 73.5 mm × 640 mm of the 5.5 kW PSU as per OCP's specifications (48 W/in^3). Additionally, the ORV HPR2 is discussed considering the upgrade from the 33 kW shelf to the 72 kW shelf with N+1 redundancy incorporating PSUs with 12 kW output power. The dimensions of the 12 kW PSU according to the ORV HPR2 are 40 mm × 83.5 mm × 790 mm, while an internal fan is used for the cooling [2]. The dimensions of the PSU from Infineon are 40 mm × 68 mm × 640 mm, making it possible to fit it in a 19-inch rack, achieving a power density of 113 W/in^3, which is more than double the OCP ORv3 standard. In Figure 3, the 3D renders of the overall PSU are shown along with the dimensions of the PSU according to the OCP and ORV HPR2 guideline.

Additionally, among all the requirements listed in [1], the 20 ms hold-up time requirement at 100% of the output load is the most impactful from a power density point of view, and a fair comparison of the power density parameter among different PSUs requires the hold-up requirement to be satisfied for all of them. Indeed, to satisfy the hold-up time requirement without a hold-up time extension circuit, a much larger capacitance would be needed, reducing the power density. An auxiliary hold-up time extension circuit is therefore implemented in REF_12KW_HFHD_PSU as a viable solution to implement the 20 ms hold-up time with a 113 W/in^3 power density.

1.3 Key features of the 12 kW PSU

REF_12KW_HFHD_PSU can deliver a maximum output power of 12 kW in steady state, in the specified 208 V_{AC} to 277 V_{AC} ±10% voltage range, with a peak efficiency of 97.8% and a minimum efficiency of 96.5%, from 30% to 100% of output power at 230 V_{AC} input voltage, including the fan power consumption.

With a size of just 40 mm × 68 mm × 640 mm (including chassis) and 113 W/in^3 power density, REF_12KW_HFHD_PSU shows a viable approach for achieving higher power density and efficiency simultaneously, in the AC-DC power conversion stage compared to current state-of-the-art solutions.

For easy implementation, REF_12KW_HFHD_PSU uses a two-stage power conversion architecture. For the front-end AC-DC converter, an interleaved 3-level flying capacitor approach is used, which provides power factor correction (PFC) and regulates the intermediate DC bus voltage. For the back-end power conversion stage, an isolated DC-DC LLC converter is selected, providing an isolated and regulated 50 V_{DC} nominal output voltage from the high-voltage rail.

Furthermore, the critical hold-up time requirement is addressed by the REF_12KW_HFHD_PSU power supply in the proposed form factor. The PSU is capable of 20 ms hold-up time at 100% output load deploying an auxiliary energy buffer (EB) converter, implemented with a bidirectional 2-switch buck-boost converter. With the proper control scheme, the same auxiliary converter also provides grid shaping (also known as “peak shaving” or “power smoothing”) function, limiting the slope of the power drawn from the grid during dynamic conditions.

REF_12KW_HFHD_PSU has the following features:

- 12 kW maximum steady state output power
- 97.8% peak efficiency at 230 V_{AC}
- 96.5% efficiency at 230 V_{AC} and 100% of output load
- 40 mm × 68 mm × 640 mm for 12 kW including chassis (vs 40 mm × 73.5 mm × 640 mm for 5.5 kW [1])
- 113 W/in^3 power density
- 20 ms hold-up time extension at 100% of output load
- Power grid shaping function
- Inrush current limiting circuit with no electromechanical relays
- Overcurrent protections on LLC primary and output currents (latching)
- AC input voltage brownout protection
- UVP and OVP protections on output voltage (5 retries before latching)
- UVP and OVP protections on bulk voltage

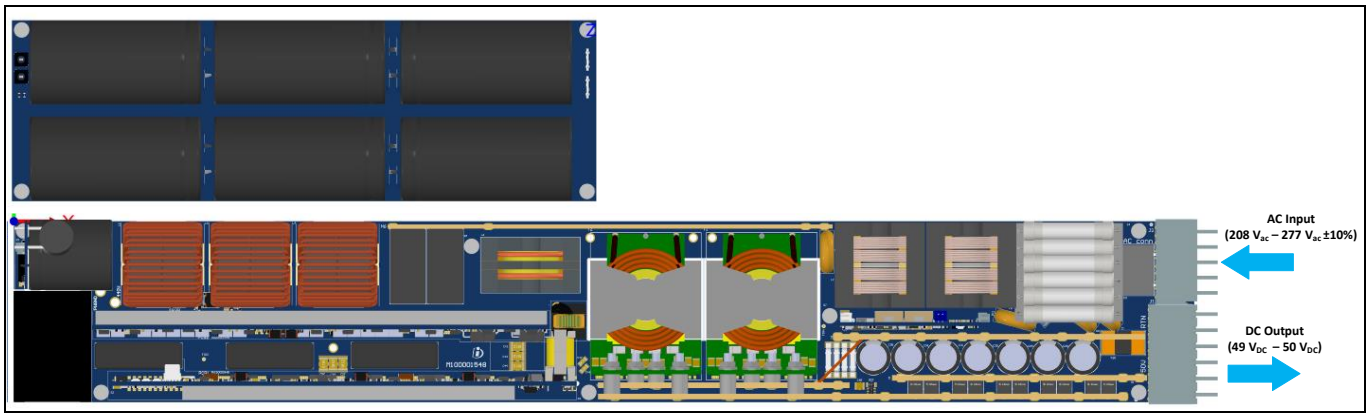


Figure 1 3D renders of the REF_12KW_HFHD_PSU power supply unit

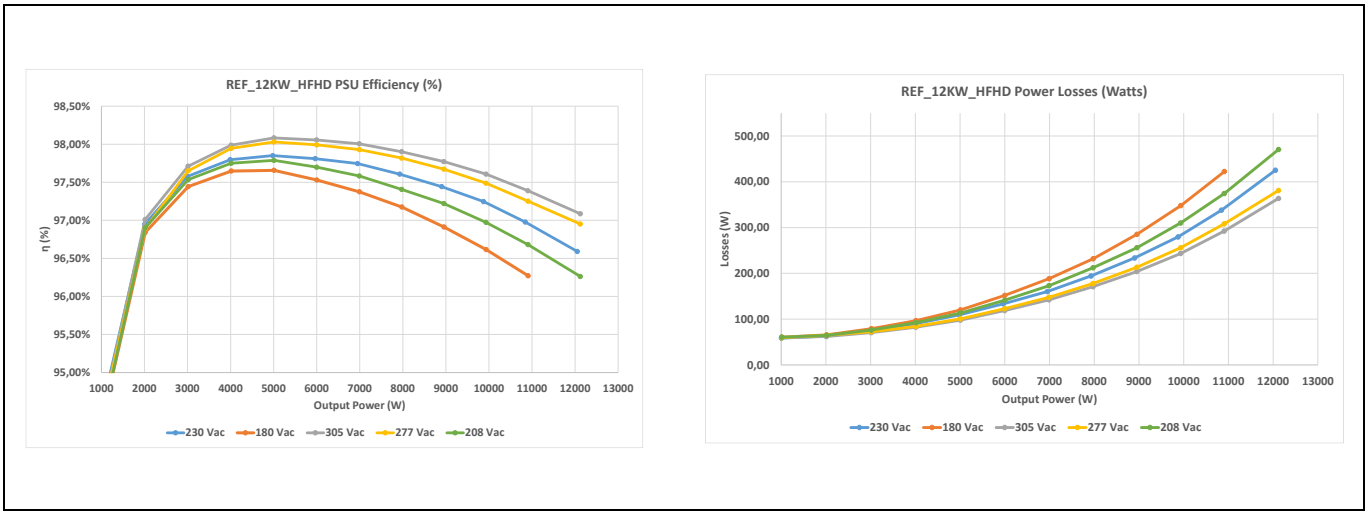


Figure 2 REF_12KW_HFHD_PSU measured efficiency including fan power consumption

The key components from Infineon enabling REF_12KW_HFHD_PSU are:

- CoolSiC™ 650 V Gen 2, 10 mΩ TOLL (IMT65R010M2H), and EiceDRIVER™ 1EDB9275 for the fast switching boosting legs of the 3-Level PFC converter
- CoolSiC™ 650 V Gen 2, 7 mΩ D²PAK (IMBG65R007M2H), and EiceDRIVER™ 1EDB9275 for the synchronous rectification leg of the 3-Level PFC converter
- 600 V CoolMOS™ CM8, 16 mΩ TOLL (IPT60R016CM8), EiceDRIVER™ 1EDB8275 for the static switch of the energy buffer and the inrush switch of the PSU
- CoolGaN™ 650 V HEMT GIT, 25 mΩ TOLL (IGT65R025D2), EiceDRIVER™ 1EDB8275 for HB switches at the primary side of the LLC converter
- IGC016K10S2, 100 V, 1.6 mΩ GaN, and EiceDRIVER™ 2EDB7259K for the synchronous rectification (SR) switches of the secondary side of the LLC converter
- CoolSiC™ 650 V Gen 2, 33 mΩ (IMT65R033M2H), for the energy buffer buck-boost converter
- XMC4402-F64K256 BA microcontroller for the implementation of the PFC and the energy buffer control routines

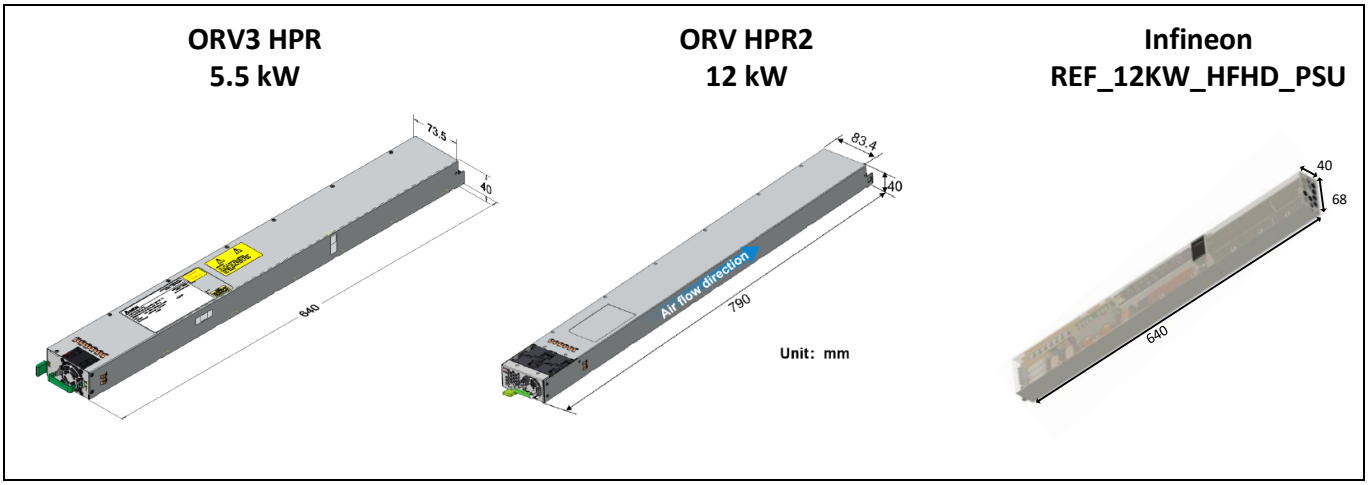


Figure 3 Dimensions of the 12 kW power supply REF_12KW_HFHD_PSU compared to OCP v3 requirement for the 5.5 kW PSU and the ORV HPR2 [2]

1.4 Electrical performance of the 12 kW PSU

Table 1 Steady state performance of the 12 kW PSU

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
AC input supply voltage	$V_{AC,in}$	180	230	305	V	RMS value
Supply voltage frequency	$f_{AC,in}$	–	50	–	Hz	–
Output voltage	V_{out}	49	–	50	V	Droop function is active 50 V_{DC} at no load 49 V_{DC} at 100% load
Output power	–	–	–	12000	W	208 V_{AC} – 305 V_{AC}[1]
Operating ambient temperature	T_{amb}	–	25	–	°C	Unit verified at 25°C ambient temperature
Peak-to-peak output voltage steady-state ripple	$V_{out,rpp}$	–	–	0.25	V	250 MHz probe BW 0.1 µF capacitor locally connected
Power density	–	–	113	–	W/in^3	–
Power factor	$PF_{10\text{-}20\%}$	0.965	–	–	–	$V_{AC,in}$ = 230 V [2] 10-20% of nominal load
	$PF_{20\text{-}100\%}$	0.99	–	–		$V_{AC,in}$ = 230 V [3] 20-100% of nominal load
	$PF_{40\text{-}100\%}$	0.995	-	–		$V_{AC,in}$ = 230 V 40-100% of nominal load
Input current THD	$iTHD_{5\text{-}10\%}$	–	–	12	%	$V_{AC,in}$ = 230 V [3] 5-10% of nominal load
	$iTHD_{10\text{-}30\%}$	–	–	6		$V_{AC,in}$ = 230 V [3] 10-30% of nominal load
	$iTHD_{30\text{-}100\%}$	–	–	3.5		$V_{AC,in}$ = 230 V [3] 30-100% of nominal load

1 Maximum output power can be delivered when input voltage is in the range 208 V_{AC} to 305 V_{AC}
Linear derating curve is applicable from 180 V_{AC} to 208 V_{AC} (Maximum P_{out} = 11 kW at 180 V_{AC})

[2] Minimum PF as per OCP v3 specification
$PF_{min,10\text{-}20\%}$ = 0.95; $PF_{min,20\text{-}100\%}$ = 0.98

[3] Maximum iTHD as per OCP v3 specification
$iTHD_{5\text{-}10\%}$= 15%; $iTHD_{10\text{-}30\%}$ = 10%; $iTHD_{30\text{-}100\%}$ = 5%

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
LLC operating frequency	$f_{SW,LLC}$	303	–	377	kHz	100% of nominal load
Maximum LLC operating frequency	$f_{SW,LLC,max}$	–	550	–	kHz	Steady-state operation
PFC operating frequency	$f_{SW,PFC}$	–	32.5	–	kHz	High frequency 3-level flying capacitor leg
Nominal bulk voltage	V_{bulk}	–	445	–	V	–
Peak-to-peak bulk voltage ripple	$V_{bulk,rpp}$	–	20	–	V	100% of nominal load

Table 2 Efficiency performance of the 12 kW PSU

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Efficiency (PSU inside chassis, cooling fan power consumption included)	$\eta_{min,230V}$	96.5	–	–	–	$V_{AC,in}$ = 230 V [4] 30-100% of nominal load
	$\eta_{pk,230V}$	–	97.8	–	–	$V_{AC,in}$ = 230 V [1] 30-100% of nominal load
	$\eta_{min,180V}$	96.2	–	–	–	$V_{AC,in}$ = 180 V [1] 30-90% of nominal load (11 kW maximum P_{out} at 180 V_{AC})
	$\eta_{pk,180V}$	–	97.6	–	–	$V_{AC,in}$ = 180 V [1] 30-90% of nominal load (11 kW maximum P_{out} at 180 V_{AC})
	$\eta_{min,277V}$	96.9	–	–	–	$V_{AC,in}$ = 277 V [1] 30-100% of nominal load
	$\eta_{pk,277V}$	–	97.95	–	–	$V_{AC,in}$ = 277 V [1] 30-100% of nominal load

[4] Minimum efficiency values as per OCP v3 specification:
$\eta_{min,230V}$ = 96.5%; $\eta_{pk,230V}$ = 97.5%; $\eta_{min,208V}$ = 96.5%; $\eta_{pk,208V}$ = 97.5%

Table 3 Protection limits in 12 kW PSU

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Current limit per phase	$I_{PFC,Ph}$	–	–	78	A	Peak current limit on each phase
Output current OCP	$I_{OUT,OCP}$	–	500	–	A	PSU tries 5 times to restart before latching
Output voltage OVP	$V_{out,OVP}$	–	58	–	V	PSU tries 5 times to restart before latching
Output voltage UVP	$V_{out,UVP}$	–	38	–	V	PSU tries 5 times to restart before latching the fault condition
LLC primary current OCP	$I_{LLC\text{-}pri,OCP}$	–	150	–	A	PSU tries 5 times to restart before latching the fault condition
Input AC voltage brownout protection	$V_{AC,BOPon}$	–	180	–	–	PSU turn on
	$V_{AC,BOPon}$	–	176	–	V	PSU turn off

Table 4 Dynamic performance of the 12 kW PSU

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Output voltage under/overshoot during load transients	$\Delta V_{out,10\text{-}100\%}$	–	–	0.12	V	5 A/µs output load[5] change rate 10-100% of nominal load 100-10% of nominal load
	$\Delta V_{out,10\text{-}140\%}$	–	–	0.3	V	5 A/µs output load change rate 10-140% of nominal load 140-10% of nominal load
Output voltage settling time during load transients	$t_{Vout,set}$	–	–	1	ms	5 A/µs output load[6] change rate 10-100% of nominal load 100-10% of nominal load
AC voltage sag transient	$V_{AC,min,500ms}$	160	–	–	V	Maximum time duration of the voltage sag: 500 ms
Hold-up time	$t_{HU,100\%}$	20	-	–	ms	100% of nominal load

[5] Max undershoot or overshoot according to [1]:
10-50% load step: 0.5 V 10-90% load step: 1.0 V

[6] Max settling time according to [1]: 3.0 ms

2 System overview and description

2.1 System overview

The REF_12KW_HFHD_PSU reference design is shown in Figure 4 with its chassis. The overall dimensions including the steel chassis are 40 mm × 68 mm × 640 mm.

To achieve the power density target, a tri-dimensional mechanical assembly has been necessary and multiple daughterboards are assembled on the main PCB as shown in Figure 4. Further details about the hardware implementation are reported in Section 2.5.

Figure 4 Top-side picture of the REF_12KW_HFHD_PSU without chassis

2.2 Topology selection

Figure 5 shows a simplified schematic of REF_12KW_HFHD_PSU.

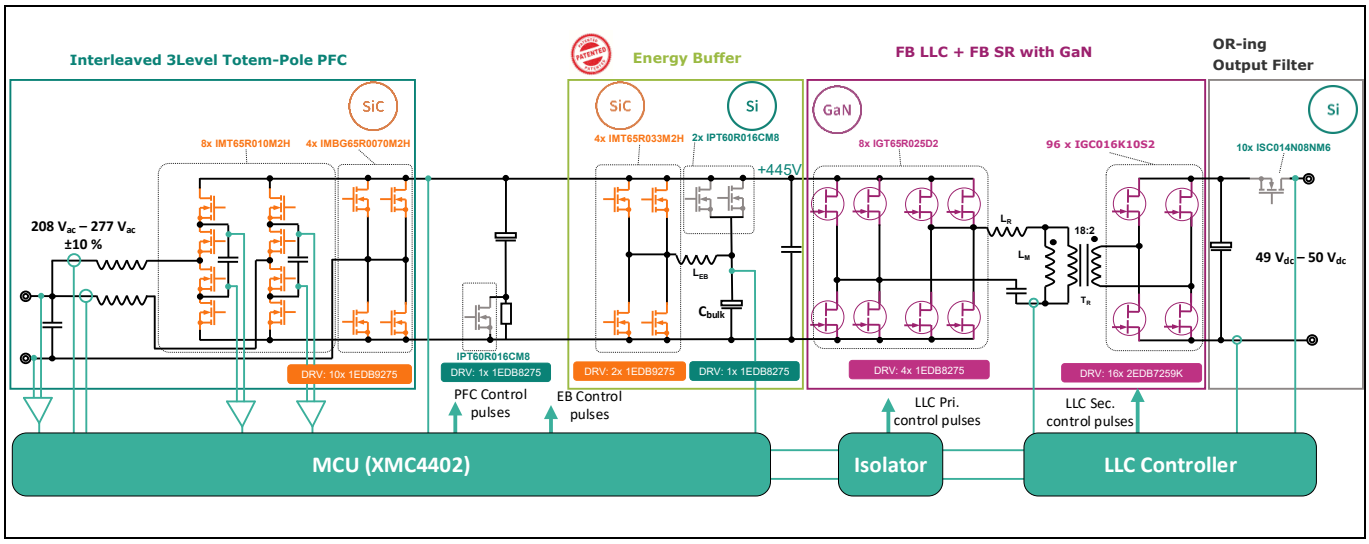


Figure 5 Simplified schematic of REF_12KW_HFHD_PSU (EMI filters are not shown) [3], [4]

REF_12KW_HFHD_PSU is implemented comprising two power conversion stages, the PFC AC-DC power conversion stage, and the isolated DC-DC power conversion stage.

During steady state operation, the first AC-DC conversion stage rectifies and boosts the 180 V_{AC} – 305 V_{AC} input voltage to 445 V_{DC} nominal DC-link voltage also providing a power factor correction function. This intermediate bus voltage is fed to the second power conversion stage, the DC-DC converter. The main function of this stage is to provide isolation and a regulated 50 V_{DC} nominal output voltage.

- The first AC-DC conversion stage is a two-phase interleaved 3-Level flying capacitor PFC converter. The key and main functions of this converter are to rectify and boost the AC input voltage to 445 V_{DC}, provide power factor correction at the AC input, and ensure low Total Harmonic Distortion (THD) of the input current waveform
- The second power conversion stage is the isolated LLC DC-DC conversion stage. For both primary and secondary sides, the full bridge topology is implemented. It provides galvanic reinforced isolation, regulates the output voltage to 50 V_{DC} nominal, and rejects the double line frequency component which is present on the DC link voltage. Furthermore, the droop control function is handled by the same converter, which regulates the output voltage according to the load current with a predefined slope (50 V at 0% Load, 49 V at 100% of the load). The overall primary-to-secondary turn ratio is 18:2 and is achieved with two 9:2 high frequency transformers (XFMRs), with the primary windings connected in series, while the parallel connection is established for the output
- The auxiliary power circuit, called energy buffer, is connected in parallel to the intermediate DC link which is shared between the first AC-DC and the second DC-DC conversion stage. The energy buffer is implemented deploying a two-switch bidirectional buck-boost converter. This power converter is disabled during steady state operation and the bulk capacitance is connected directly to the DC-link with a static switch. The main and key functions of this converter are two. The first is to provide 20 ms hold-up time extension during line cycle drop-out (LCDO), by discharging the electrolytic capacitor bank which is connected on the low voltage side of the buck-boost converter, while keeping the intermediate bus voltage regulated (high-voltage side of the buck-boost converter). The second function is to shape the slope of the power drawn from the grid, providing, as it is called, a grid shaping function (also known as “peak shaving” or “power smoothing”). This is achieved by limiting the amount of energy flowing from the grid to intermediate DC bus during transient events, while the remaining of the required energy is provided by discharging the bulk capacitance connected to the low voltage side of the energy buffer. After the transient event, the bulk capacitance is charged in a controlled way with the energy flowing from the AC-DC converter to the DC link capacitance and then from the DC link capacitance to the bulk capacitance of the energy buffer. The topology of the energy buffer auxiliary circuit, and more specifically the operation and the configuration for the AI datacenters and servers applications, is patented by Infineon Technologies under the patents [3], [4].

2.3 Power stage control and protection

The control of the power stages is realized with two different controller ICs, as shown in Figure 5.

The control of the 3-level flying capacitor interleaved totem-pole PFC is implemented with the Infineon XMC™ 4402 microcontroller, referenced to the primary side ground. With this configuration, the following are possible: power factor correction, current THD control, intermediate DC link voltage regulation, current control for each PFC boost inductor, inrush current control, and energy buffer control. From a protection point of view, XMC™ 4402 implements AC input and boost inductor currents limitation, bulk overvoltage protection (non-latching, i.e., PSU is not turned off when triggered), undervoltage lockout (UVLO), and brownout protection (latching, i.e., PSU turns off when triggered), soft-start, adaptive dead-times. Additionally, bidirectional serial communication is also implemented, transferring data regarding the operation of the PFC converter to the LLC converter and vice versa.

The control of the DC-DC LLC converter is implemented with a third-party microcontroller, referenced to the secondary side ground. Because of this, the PWM signals of the primary side high-voltage switches are passed through a digital isolator for reinforced isolation. With this implementation of the DC-DC stage control, the following features are feasible:

- output voltage regulation
- load dependent adaptive dead-times
- overcurrent protection on the primary resonant current (latching)
- output overcurrent protection (latching)
- output overvoltage protection (latching)
- output undervoltage protection (latching)
- soft-startup sequence
- UART communication with XMC™ 4402

The PWM for the cooling fan is also controlled by the LLC microcontroller and implements fan-stop protection (latching).

2.4 Highlighted products

Infineon power semiconductors and ICs are the key components to enable 12 kW output power with 113 W/in^3 power density.

For the 3-level flying capacitor interleaved totem-pole PFC, a full SiC solution with paralleled MOSFETs has been used:

- Fast switching boost 3-level legs
  - 8x CoolSiC™ 650 V Gen 2, 10 mΩ TOLL (IMT65R010M2H), one per commutation slot
  - 8x single channel EiceDRIVER™ 1EDB9275, one per commutation slot
- Low frequency unfolding leg
  - 4x CoolSiC™ 650 V Gen 2, 7 mΩ D^{2}PAK (IMBG65R007M2H), 2x paralleled devices per commutation slot
  - 2x single channel EiceDRIVER™ 1EDB9275

For the LLC DC-DC isolated converter, a full GaN solution has been adopted, featuring 650 V GaN devices on the primary side and 100 V GaN MOSFETs for the secondary side:

- Primary side
  - 8x CoolGaN™ 650 V HEMT GIT, 25 mΩ TOLL (IGT65R025D2), 2x paralleled devices per commutation slot
  - 4x single channel isolated drivers EiceDRIVER™ 1EDB8275F
- Secondary side synchronous rectifiers
  - 96x IGC016K10S2, 100 V, 1.6 mΩ GaN, 8x total in each secondary-side transformer board for both SR bridges
  - 24x dual channel isolated EiceDRIVER™ 2EDB9259Y, 2x in each secondary-side transformer board

For inrush and static switches, the following components have been chosen:

- For the inrush circuit:
  - 1x CoolMOS™ 600 V CM8, 16 mΩ TOLL (IPT60R016CM8) for the inrush NTC bypass switch
  - 1 x single channel driver EiceDRIVER™ 1EDB8275F
- For the static switch
  - 2x CoolMOS™ 600 V CM8, 16 mΩ TOLL (IPT60R016CM8), for the energy buffer static switch
  - 1x single channel driver EiceDRIVER™ 1EDB8275F

For the energy buffer implementation, the following components have been used:

  - 4x CoolSiC™ 650 V Gen 2, 33 mΩ TOLL (IMT65R033M2H), 2 parallel devices per commutation slot
  - 2 x single channel driver EiceDRIVER™ 1EDB9275

Additionally, in the PSU, the following ICs are used:

- XMC4402-F64K256 BA microcontroller for the implementation of the PFC control

2.5 Hardware implementation

The complete hardware implementation of the unit is shown in Figure 6.

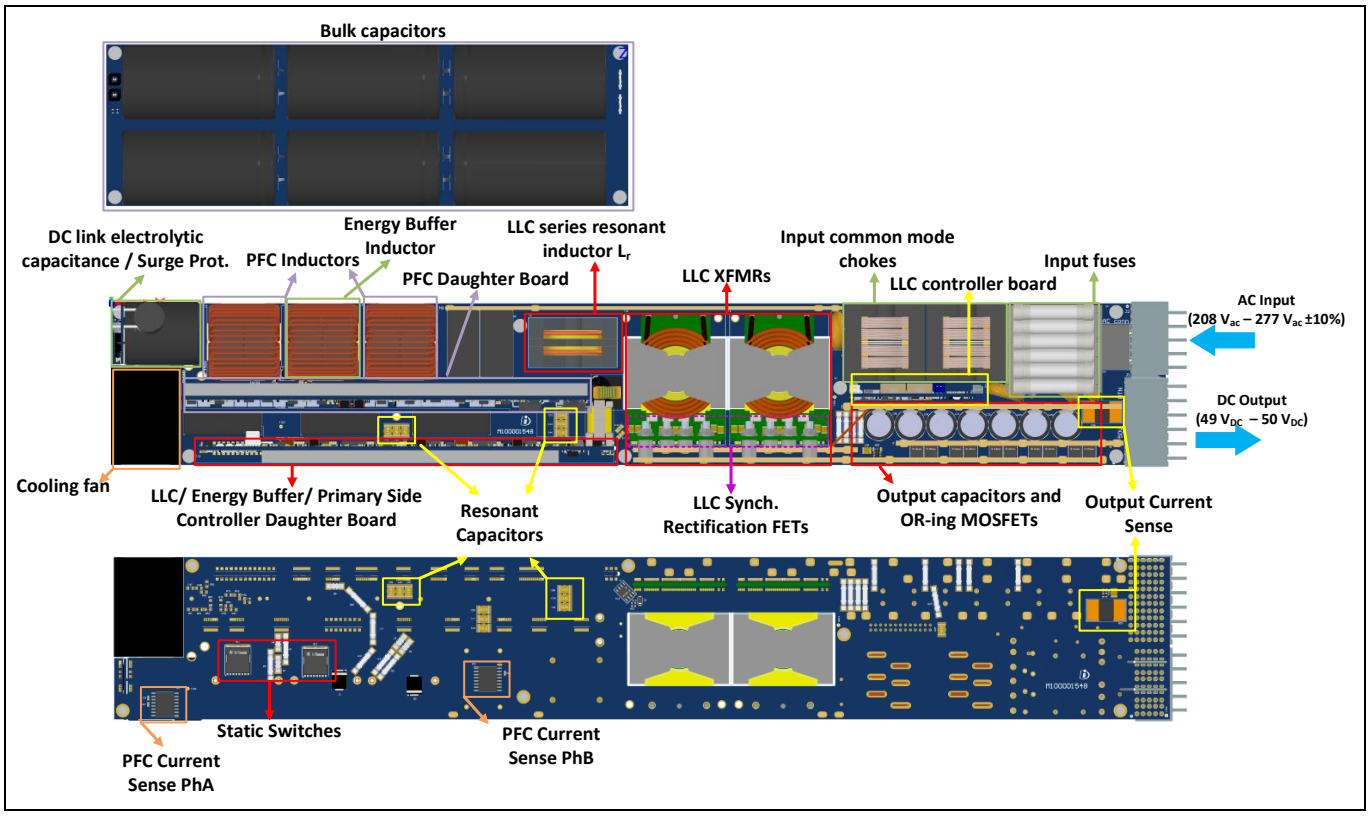


Figure 6 Hardware implementation of REF_12KW_HFHD_PSU (top and bottom)

Overall, the 12 kW Infineon power supply comprises the following boards:

- The main board (M100001549) acting as the main interface and the support for the daughter cards and the following components:
  - AC input EMI filter and fuses
  - PFC inductors, sensors of the PFC inductor current
  - Energy buffer inductor
  - Two integrated LLC XFMRs, the LLC series resonance inductor and the series resonance capacitors
  - Static and inrush switches along with the driving and supporting circuitry
  - Inrush and the re-rush circuits
  - DC output capacitors and ORing circuit
- The PFC daughter card (PW200001549)
- The daughter card on which the LLC switches, the energy buffer switches, the primary side microcontroller, and the main flyback biasing converter are populated (PW100001548)
- The LLC control card (CD200001548)
- The electrolytic capacitor bank (bulk capacitors) (PW400001548) on which the electrolytic capacitors are populated
- The DC link electrolytic capacitor along with the inrush limiting circuit daughterboard (C200001547)

2.5.1 The daughterboards

Figure 7 and Figure 8 show the LLC + EB + controller, and the PFC daughter cards, respectively, as discussed in Section 2.5. In Figure 9, the LLC controller daughterboard is depicted, while in Figure 10 the DC bus electrolytic capacitor board is shown, which is also used for surge protection when the energy buffer is active.

The LLC + EB + controller daughter card (PW100001548) hosts the primary full bridge of the LLC DC-DC converter, together with the two isolated supplies for the two high-side switches. Additionally, the power stage of the energy buffer is also populated on the same daughter board along with the primary side XMC microcontroller. The flyback biasing power supply generates a nominal 18 V rail referenced to negative rail of the primary intermediate DC link and an isolated 7 V rail referenced to the negative terminal of the secondary side of the LLC converter.

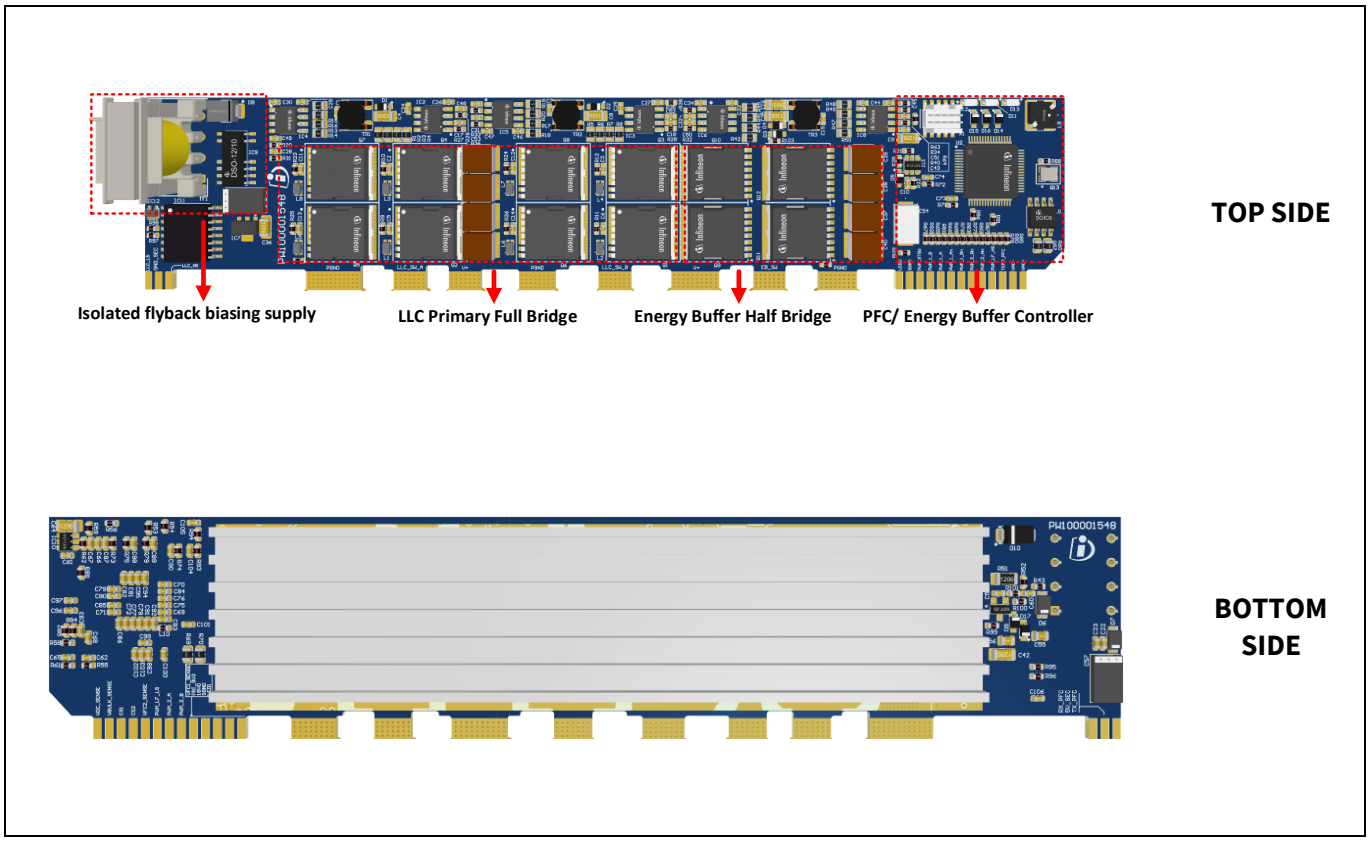


Figure 7 Overview of the LLC+EB+Controller daughter card PW100001548

The PFC daughter card (PW200001549) integrates the two interleaved high frequency 3-level flying capacitor legs and the synchronous rectification bridge of the PFC converter. The driving supply for the low frequency synchronous rectification leg is implemented with the bootstrap technique, while for the high frequency legs a mixed approach is followed, with both bootstrap and isolated biasing supplies. More details are shown in Section 3.1.6.

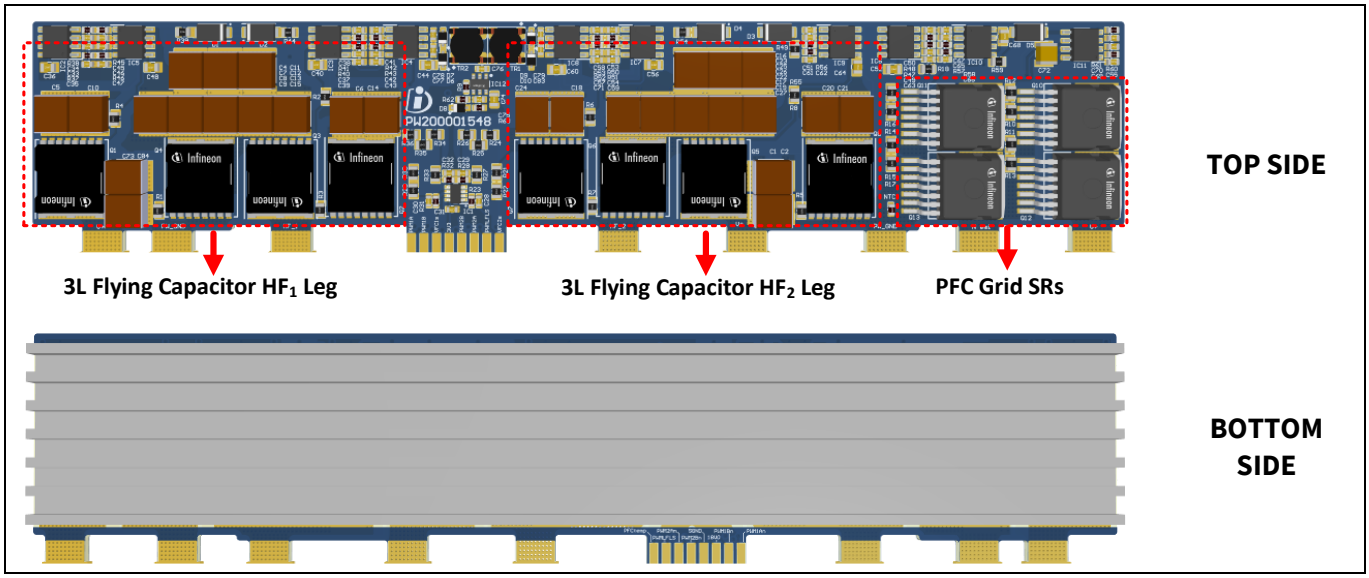


Figure 8 Overview of the PFC power daughter card PW200001429

The secondary-side controller board (CD200001548) integrates a third-party microcontroller and its main functions are:

- Generation of the control pulses for the LLC converter
- Digital control for the output voltage regulation, including
  - A PID controller and droop function to set the output voltage command
- Control of the cooling fan of the PSU
- Implementation of the overvoltage, undervoltage, overcurrent, and overtemperature protection of the LLC converter

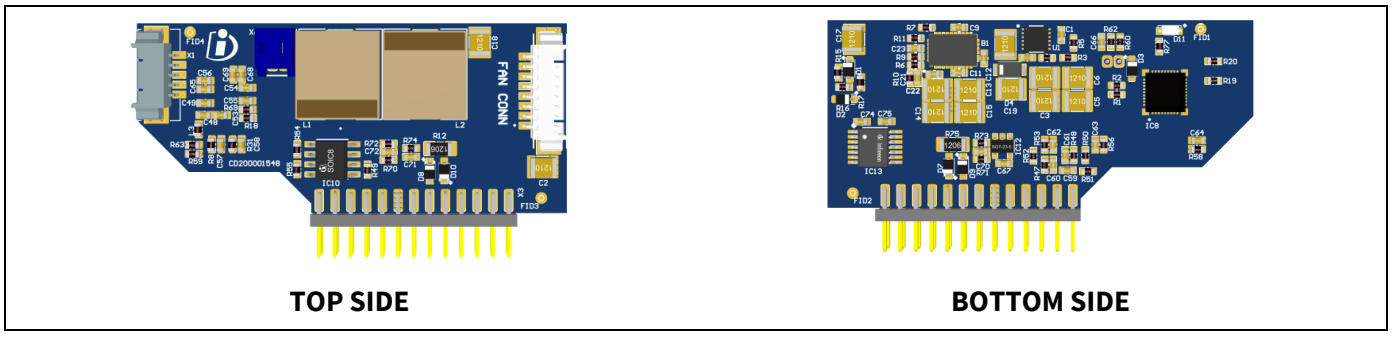


Figure 9 Overview of the secondary side controller board CD200001548

On the DC link electrolytic capacitor daughter card (C200001547) the following components are populated:

- One electrolytic capacitor (240 µF/475 V nominal)
- Inrush current limiting NTC
- Inrush switch connected in parallel to the NTC to bypass it during steady state operation and the driving circuitry for the switch

The main function of this circuit/daughter board is to take the extra amount of energy during a surge event, when the static switches are in a non-conducting state and therefore the bulk capacitance is not connected to the DC-link to absorb the energy during the surge event. Additionally, the capacitor board limits the ripple of

the DC bus during transient events, providing a low enough impedance when the energy buffer operates, helping with the stable operation of the PFC and the energy buffer control loop. The daughterboard is shown in Figure 10.

Figure 10 Overview of the DC link capacitor board C200001547

2.5.2 LLC transformer implementation overview

The LLC transformer is one of the key elements of the overall PSU to achieve high efficiency and increased power density. For the 12 kW PSU from Infineon, a hybrid planar approach is used deploying two identical XFMRs, with the primaries connected in series and the secondaries connected in parallel. Each transformer consists of the main planar magnetics transformer and the external inductor implemented with Litz wire, connected in parallel to the primary side PCBs to achieve the desired magnetizing inductance value, needed for the ZVS operation of the primary full bridge switches. The LLC secondary side full bridge synchronous rectification stage is embedded within the two transformers. More details about the construction of the high frequency transformers are presented in Section 3.2. The 3D renders of the high frequency transformer are depicted in Figure 11.

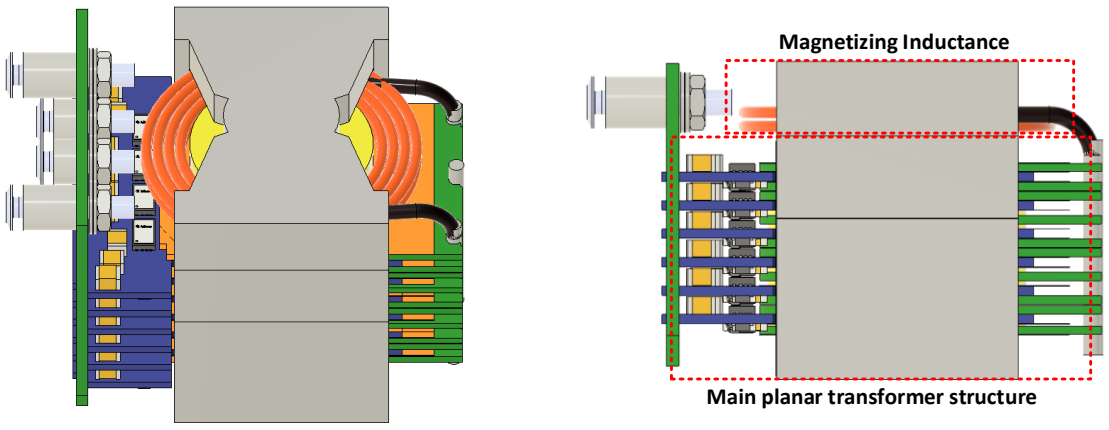


Figure 11 Overview of the LLC high frequency transformer structure

2.6 PSU efficiency and losses

The measured efficiency and the losses of the whole PSU including fan consumption (with the unit inside the chassis) are shown in Figure 12 at different AC line voltages: 305 V_{AC}, 277 V_{AC}, 230 V_{AC}, 208 V_{AC}, and 180 V_{AC}. In Figure 13 the power losses are depicted for the same input voltage values. It is noted that for the minimum input voltage the output power is limited to 11 kW following a linear derating curve until 208 V_{AC} from which the unit can deliver the full power.

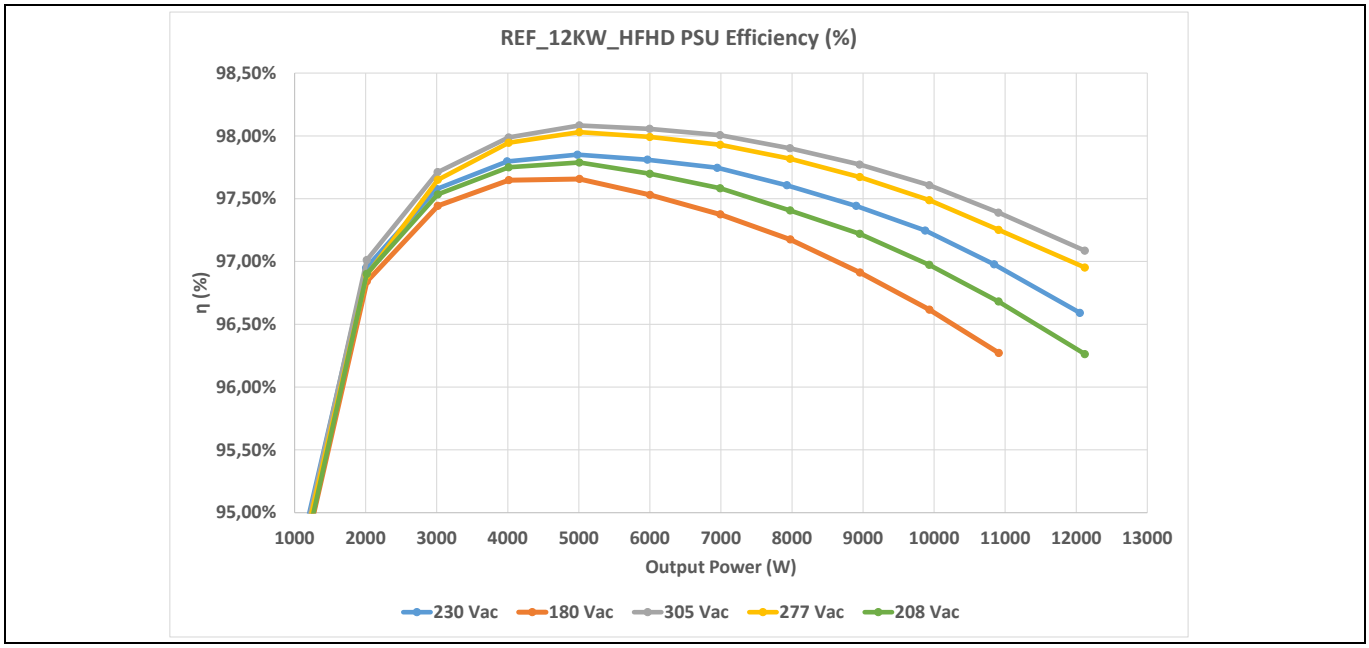


Figure 12 REF_12KW_HFHD_PSU measured efficiency including fan power consumption

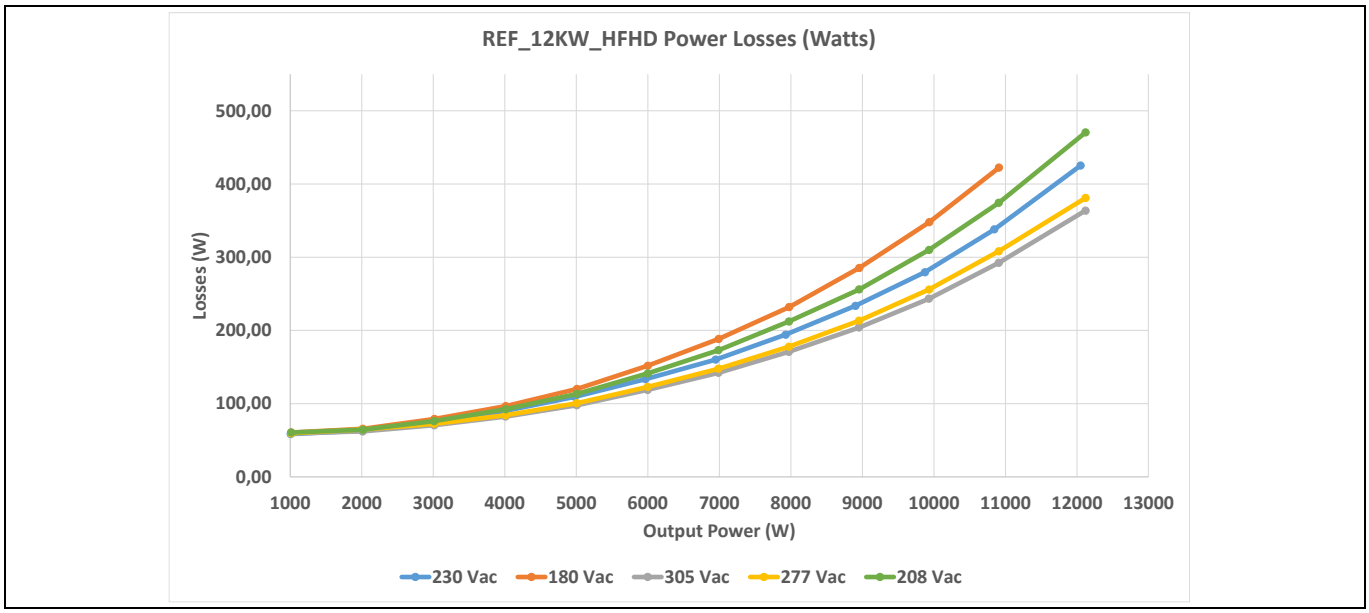


Figure 13 REF_12KW_HFHD_PSU measured power losses including fan power consumption

3 Topology blocks description

Note: *In REF_12KW_HFHD_PSU, all power circuits share power earth (PE) via the metallic chassis. For electrical safety and cooling reasons, it is recommended not to operate the board without the chassis. It is the user's responsibility to ensure proper cooling and PE connections when operating the unit outside the chassis or out of the recommended operating conditions.*

3.1 Flying capacitor 3-level interleaved totem-pole PFC

3.1.1 Performance of the topology block standalone

A simplified schematic of the interleaved 3-level flying capacitor PFC stage of REF_12KW_HFHD_PSU is shown in Figure 14.

The backplane power connector provides the AC input (Molex 46437-9205) to the power supply unit, followed by the input fuses, the surge protection circuit, consisting of MOVs and Gas Discharge Tubes (GDTs), and a two-stage input EMI filter. To support higher power density, the common mode EMI inductors of the EMI filter also integrate the differential mode inductance as shown in [5].

The filtered line AC input is connected to the two interleaved 3-level flying capacitor high frequency legs of the PFC through the boosting inductors. The neutral point after the EMI filter is connected to low frequency synchronous rectification leg of the converter ($Q_{SR,HS}$ and $Q_{SR,LS}$ in Figure 14). The two high-frequency 3-level legs operate at 32.5 kHz switching frequency. The effective frequency on the boosting PFC inductor is double the switching frequency, i.e., 65 kHz, because of the series interleaving achieved with the Phase Shifted PWM (PS-PWM) technique, deployed for the modulation of the flying capacitor legs. According to the PS-PWM modulation scheme the outer switches ($Q_{HF\_An\_x}$ and $Q_{HF\_A\_x}$) and the inner switches ($Q_{HF\_Bn\_x}$ and $Q_{HF\_B\_x}$) are driven with complementary pulses in pairs. Additionally, the control pulses of the switches $Q_{HF\_Bn\_x}$ and $Q_{HF\_B\_x}$ are 180° out of phase with respect to the control pulses of the switches $Q_{HF\_An\_x}$ and $Q_{HF\_A\_x}$. In Figure 15, the control pulses along with the switching node voltage is depicted for a single 3-level leg, when the duty cycle is greater than 0.5 as well as when it is less than 0.5, to showcase the multilevel waveform and the frequency multiplication effect on the leg level.

The control pulse generation logic for the second PFC leg is similar, but the main difference is that the control pulses of the corresponding switches feature a 90° phase compared to the first leg, to achieve the interleaving effect on the converter level, providing an overall effective frequency of 130 kHz. The two low frequency synchronous rectification switches are controlled to rectify the AC current according to the detected line polarity.

Due to high stress, the low frequency synchronous rectification switches have two SiC MOSFETs in parallel per commutation slot to achieve lower equivalent $R_{DS(on)}$ and help the power dissipation by spreading the power losses in more PCB area. Each switch of the unfolding bridge has two 7 mΩ Gen 2 CoolSiC™ devices in parallel, and for the high frequency 3-level legs, 10 mΩ Gen 2 CoolSiC™ devices are selected.

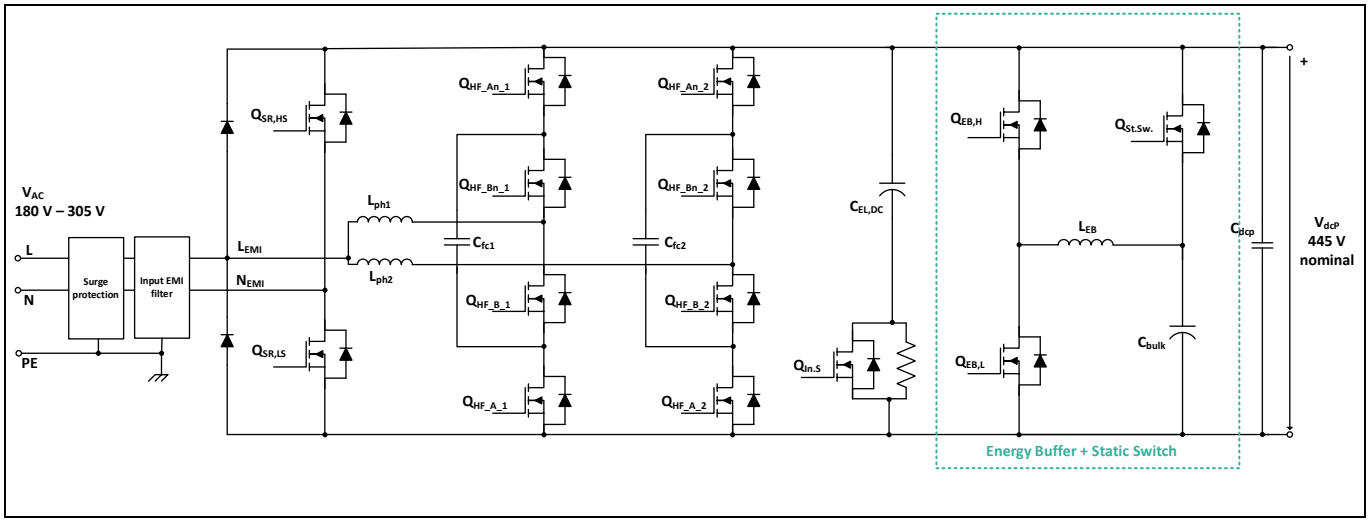


Figure 14 Simplified schematic of the PFC stage in REF_12KW_HFHD_PSU

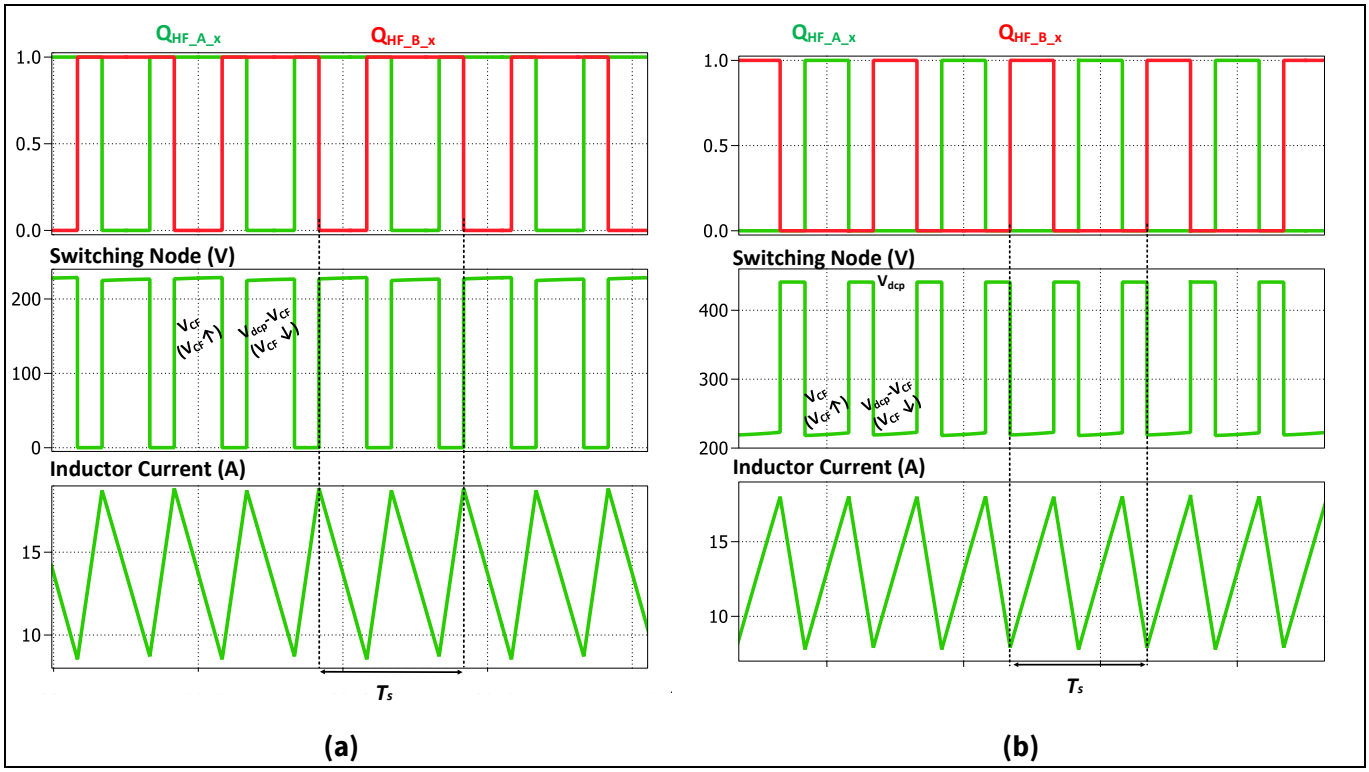


Figure 15 Control pulses and switching node voltage for the 3L flying capacitor leg with (a) duty cycle greater than 0.5 and (b) duty cycle less than 0.5

In Figure 16, the efficiency curve of the PFC standalone is presented, while in Figure 17 the power losses of the PFC converter are depicted for three different input voltage levels (180 V_{ac}, 230 V_{ac}, and 275 V_{ac}). It is to be noted that for PFC efficiency measurements in Figure 16, the cooling fans are supplied externally.

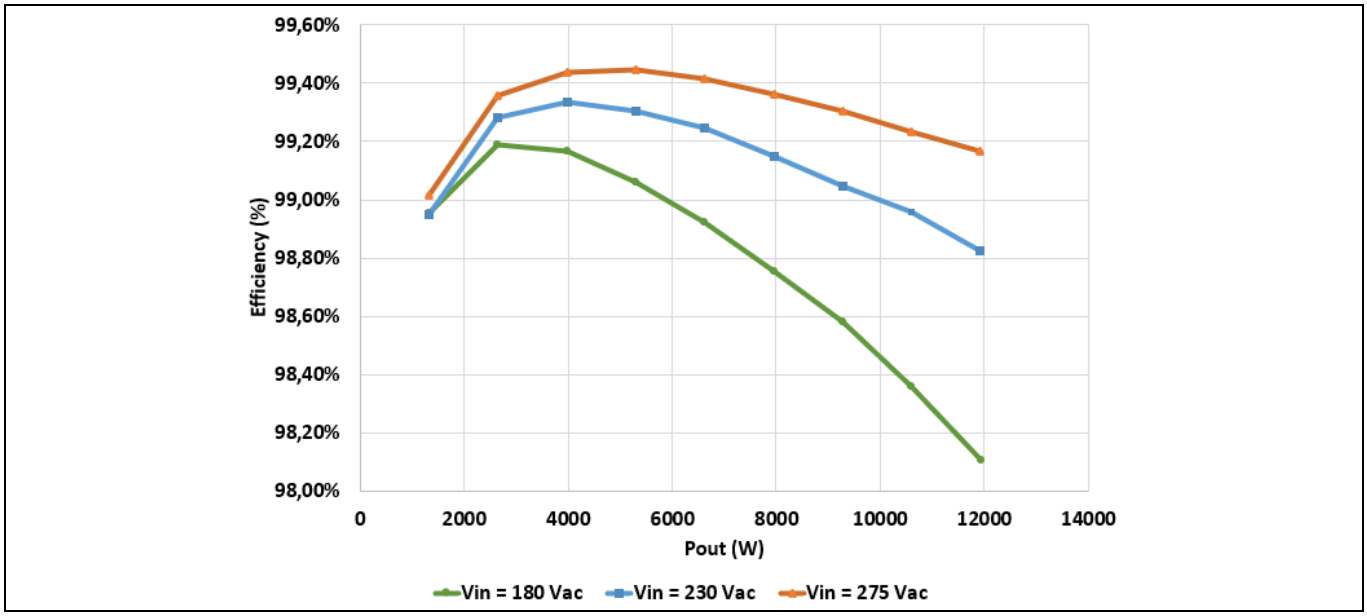


Figure 16 PFC efficiency curves for 180 V_{AC}, 230 V_{AC}, and 275 V_{AC} input voltage

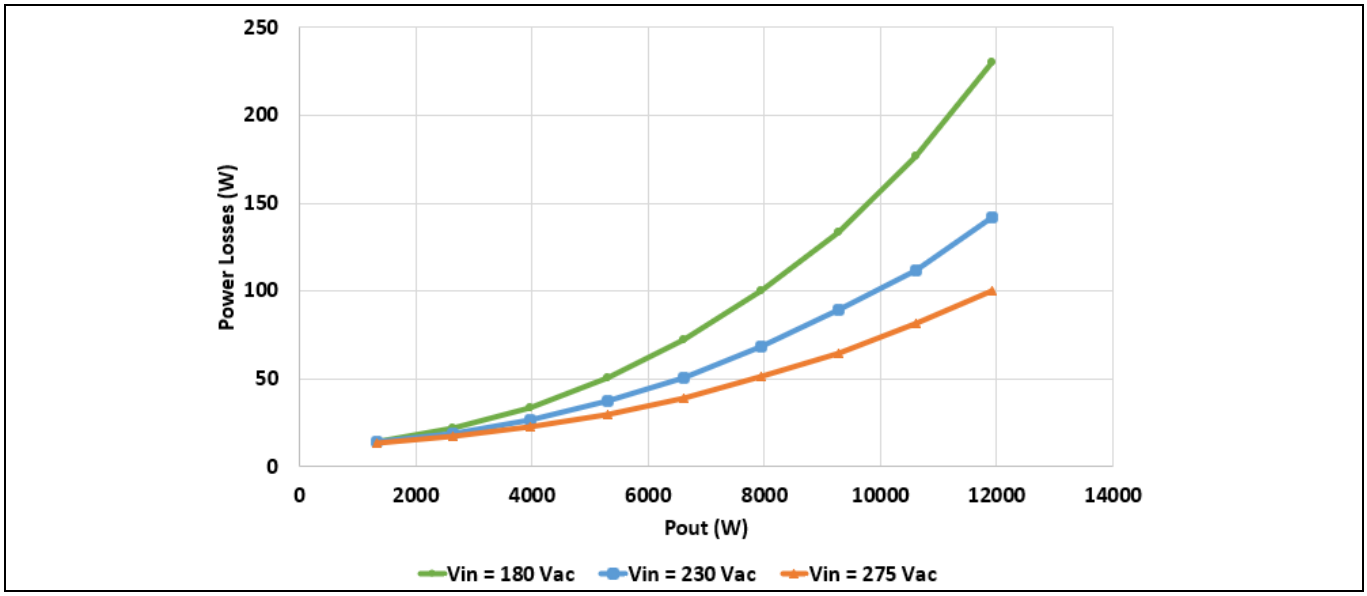


Figure 17 PFC power losses for 180 V_{AC}, 230 V_{AC}, and 275 V_{AC} input voltage

Figure 18 illustrates the distribution of losses among the PFC components at 230 V input AC voltage. The bar plot shows that the majority of the losses are related to conduction losses in the EMI filter as well as the PFC boosting inductors.

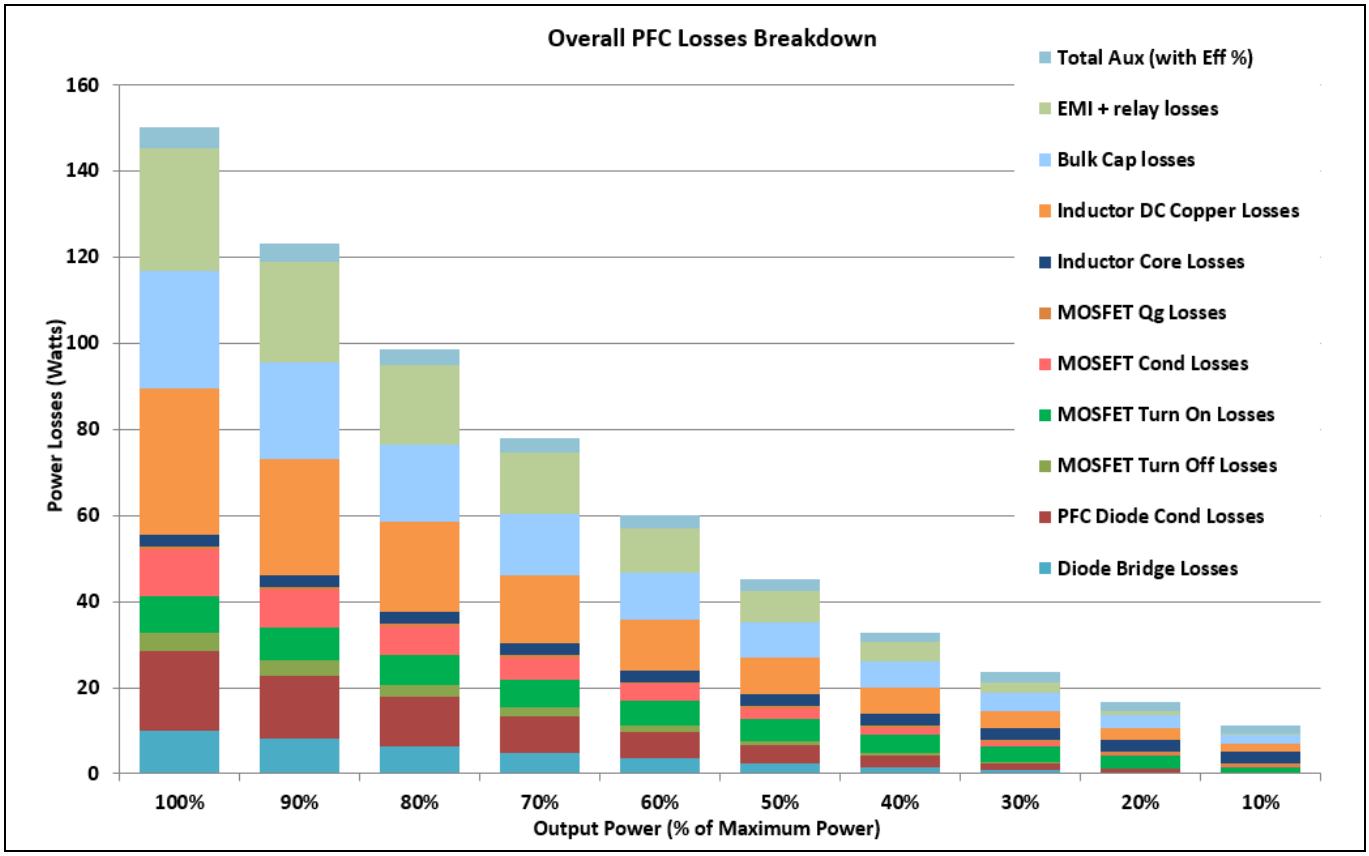


Figure 18 Distribution of the PFC converter power losses at 230 V_{ac} input voltage

3.1.2 Flying capacitor voltage balancing and initial charging

On the previous section, the basic modulation scheme of the flying capacitor 3-level leg is depicted, showcasing the frequency multiplication effect and the multilevel waveform on the switching node. The previous case is ensured only if the voltage across the flying capacitor is well regulated, and the average value of it is equal to half of the DC link voltage.

Theoretically, the PS-PWM technique ensures the natural voltage balancing of the flying capacitor, since the intervals for charging and discharging the flying capacitor are equally distributed along the input voltage's half-period [6]. For duty cycles greater than 0.5, the switching node voltage varies from 0 V to $V_{dcp}/2$, while for duty cycles less than 0.5 the switching node varies from $V_{dcp}/2$ to V_{dcp}. The $V_{dcp}/2$ voltage level can be generated with two different switching combinations: either by enabling switches $Q_{HF\_An\_x}$ and $Q_{HF\_B\_x}$ to generate a switching node voltage with a value equal to V_{dcp}-V_{FC} and discharge the flying capacitor in the same time interval, or by enabling switches $Q_{HF\_A\_x}$ and $Q_{HF\_Bn\_x}$. In the second case, only the flying capacitor is used to generate the switching node voltage, and this is the charging time interval, as shown in Figure 15. The charging and discharging commutation loops for the flying capacitor converter are depicted in Figure 19. The switching states mentioned above explain the theoretical natural voltage balancing mechanism, but in practice the things are quite different. Slightly different propagation delays of the gate drivers and minor mismatches on the devices' $R_{(DS)on}$, because of the different case temperatures, can cause different charging and discharging intervals with different loop path resistances as well, leading to different steady state flying capacitor voltage.

In order to accommodate these phenomena, a closed loop control system is needed. The basic concept to achieve the flying capacitor voltage regulation is to introduce small asymmetries to the duty cycle between the inner ($Q_{HF\_Bn\_x}$ and $Q_{HF\_B\_x}$) and outer switches ($Q_{HF\_An\_x}$ and $Q_{HF\_A\_x}$) to control the relative duration of the charging

and the discharging intervals. Thus, voltage monitoring of the flying capacitor is mandatory. More details about the balancing control loop are given in Section 3.1.4.

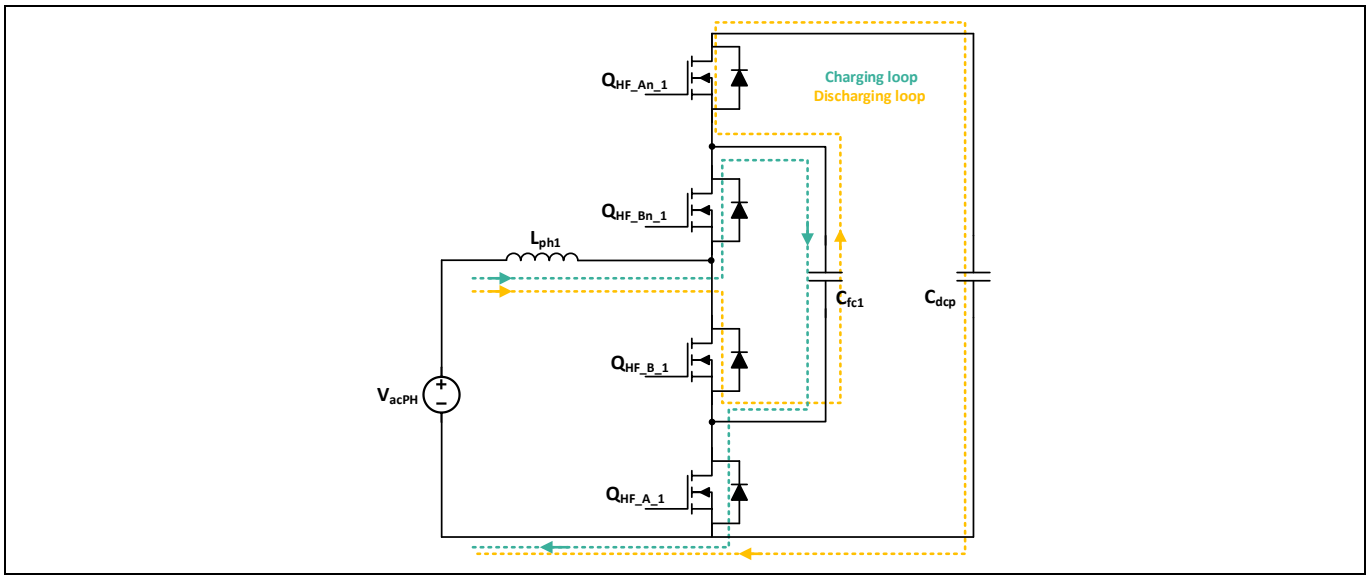


Figure 19 The charging and the discharging commutation loop for the 3L flying capacitor PFC leg

Before the normal PFC operation, the flying capacitor needs to be charged to a voltage close to the one expected during steady state operation in order to reduce voltage stress on the devices during startup and to avoid any unexpected transient phenomena. For REF_12KW_HFHD_PSU a software-based method is used to charge the flying capacitor during startup. During the PFC startup phase, only the $Q_{HF\_A\_x}$ switch is active and the flying capacitor charges through the body diode of the switch $Q_{HF\_Bn\_x}$, the active switch, and the inductor, taking energy from the grid. The charging loop is depicted for illustration purposes in Figure 20. The switch $Q_{HF\_A\_x}$ is deactivated when the flying capacitor voltage is close to the steady state value.

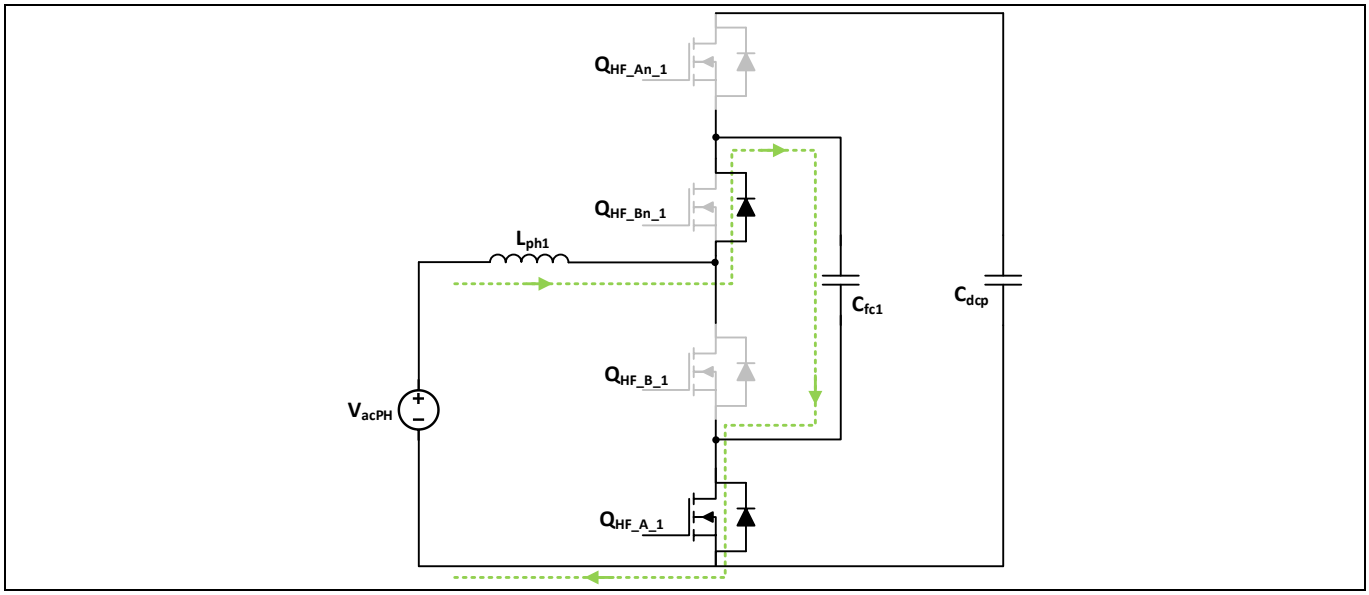


Figure 20 The charging loop of the flying capacitor during the PFC startup

3.1.3 EMI filter and PFC magnetic components

Starting with the EMI filter, the schematics of which are shown in Figure 21, it can be understood that a dual stage filter configuration is used. Two common mode inductors are used with nominal magnetizing inductance equal to 0.5 mH for the choke on the grid side and 1 mH for the choke on the converter side. A magnetic shunt is additionally added in the structure of both common mode chokes to increase the leakage field, and thus, integrate the differential inductance as well. For the common mode choke with 0.5 mH nominal magnetizing inductance the R5KZ core material from DMEGC is used, while for the choke with 1 mH nominal magnetizing inductance the R10KZ material is used from the same manufacturer. In Figure 22, complex permeability curves versus the frequency are depicted for both transformers, showing that for the R10KZ material the permeability, and hence the inductance, drops at higher frequencies, but offers higher inductance, and thus higher attenuation on the lower frequency range. In order to better attenuate the high frequency harmonic content, the R5KZ material is selected for the second choke. The combination offers a good compromise between high and low frequency filtering and it is able to effectively attenuate the noise on the whole spectrum as it is depicted in Section 4.4. For the magnetic shunt, NO 30-16 electrical steel is used. More detailed information about the common mode choke implementation can be found in [7] since the same arrangement is used for REF_8KW_HFHD_PSU. In order to account for the higher input current in this application, the flat wire dimensions for the winding of the choke are 0.6 mm × 5 mm. For the sake of completeness, a picture of the EMI common mode choke is shown in Figure 23.

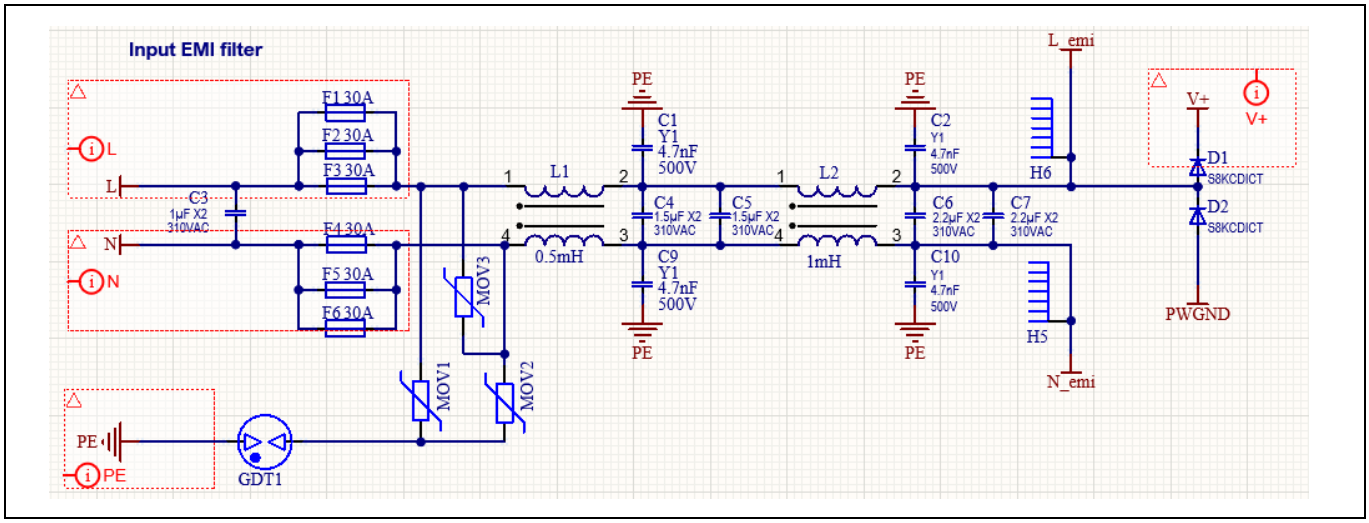


Figure 21 Schematic of the input EMI filter

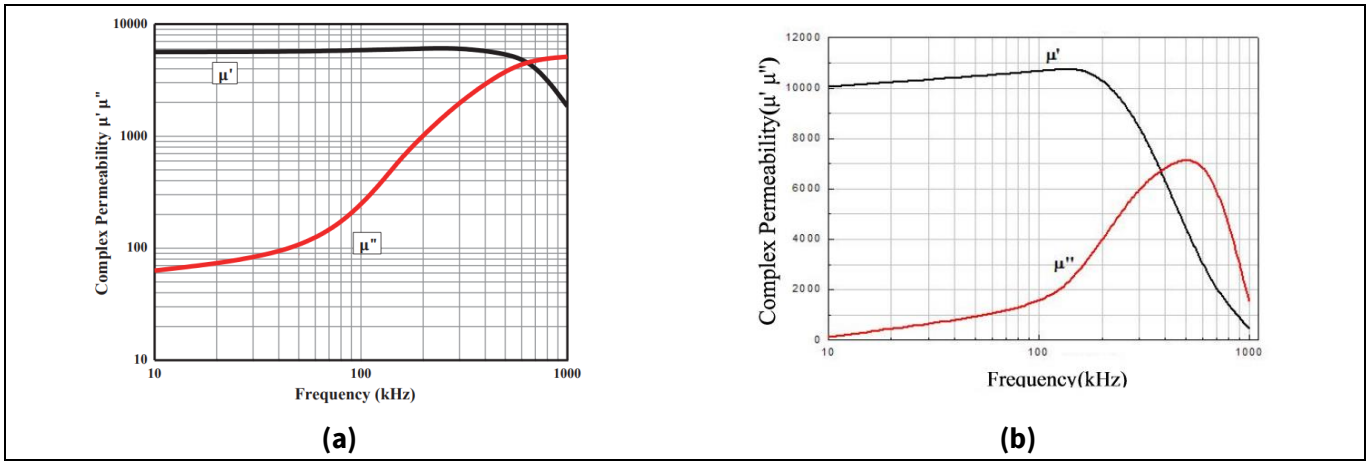


Figure 22 The complex permeability curve versus frequency for (a) the R5KZ and (b) R10KZ materials

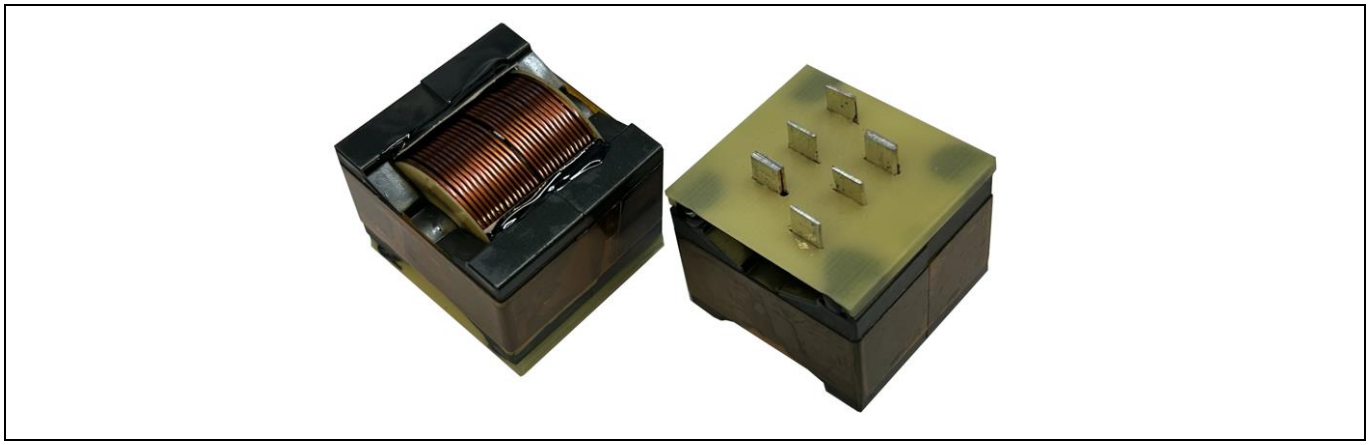


Figure 23 The common mode choke with the integrated differential mode inductance

For the PFC boosting inductor choke, a design based on a toroid core is followed. More specifically, in REF_12KW_HFHD_PSU two toroidal high flux powder cores CH270060GT GT cores from Chang Sung Corporation are used, featuring a good DC bias and core loss behavior. An additional reason to select a toroidal core, when a low relative permeability material is needed, is that with the toroidal core the stray flux is better confined within the magnetic structure, generating less interference with hall effect and magnetoresistive-based current sensors, which can cause distortion in the PFC choke current. Also, the confinement of the flux within the core reduces the losses on the stainless-steel chassis, because of the lower eddy current generation.

For the construction of each PFC choke, two CH270060GT high flux GT cores are used, while the winding is implemented deploying 27 turns of enameled copper wire with a 1.8 mm diameter. The nominal inductance value with zero DC bias is 109 µH. Nevertheless, in the presence of the line frequency component in the PFC current, the inductance value changes within the half period of the AC voltage. The inductance value in the presence of DC bias over the AC line half period is shown in Figure 24.

For the construction of the choke populated in the energy buffer topology, two CH270060GT high flux GT cores are used again, but the number of turns in this case is 39. Enameled copper wire with a 1.6 mm diameter is used for the implementation, while the nominal inductance value is 230 µH at zero DC bias.

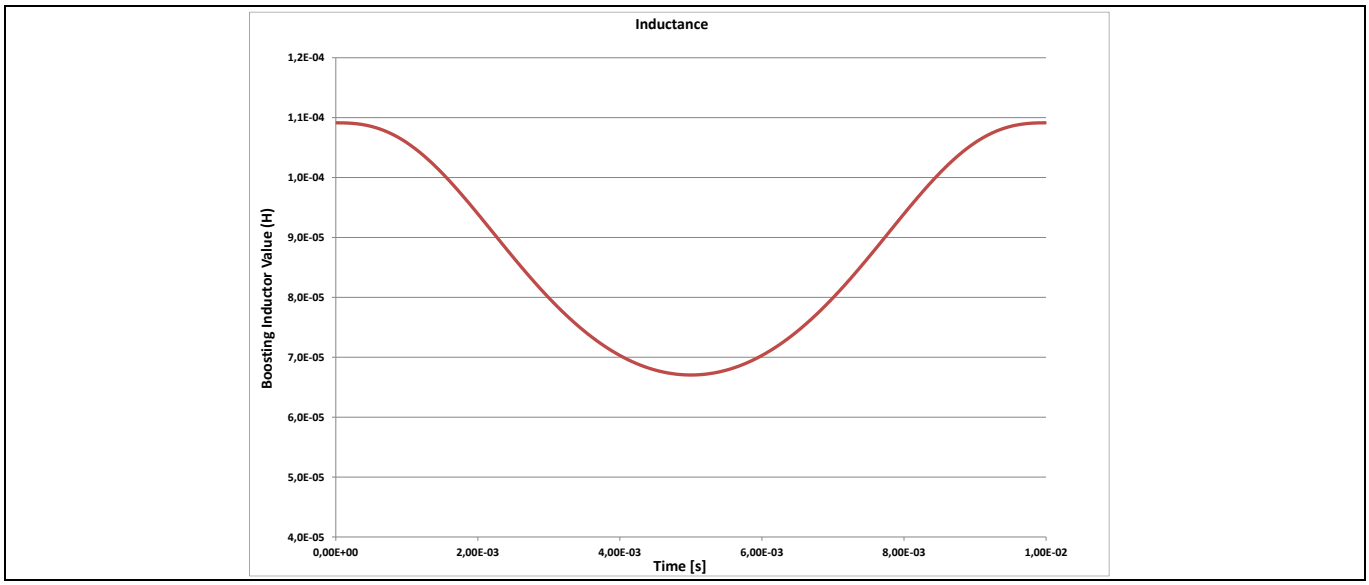


Figure 24 PFC boosting inductance value over the AC line half period at 230 V_{ac} input voltage

In Figure 25, the current per PFC choke is depicted for the half period of the AC input voltage, denoting the actual current, the average value per switching cycle, which follows a sine wave, and the peak-to-peak high frequency current ripple. Figure 25 (b) shows the average value of the magnetic flux density per switching cycle, which is related to the core loss of the inductor.

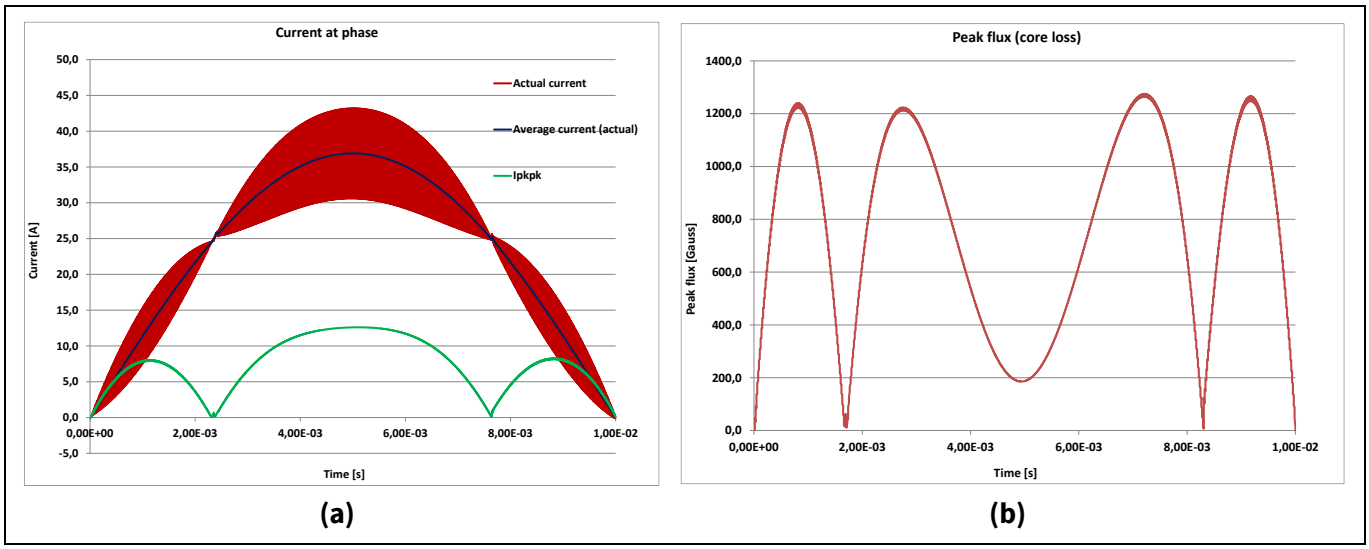


Figure 25 (a) Current waveform for a PFC phase and (b) flux density of the core per switching cycle at 100% of the load for 230 V_{ac} input voltage

3.1.4 Control scheme of the PFC

The 3-level flying capacitor bridgeless PFC of REF_12KW_HFHD_PSU operates in continuous conduction mode (CCM).

The control structure of the PFC stage consists of a cascaded loop control architecture. The outer loop is responsible for regulating the intermediate DC link voltage to a value equal to 445 V. For the DC link voltage regulation, a PI controller is used, and the output of the controller is used as a command along with some feedforward terms for the inner loop. The inner loop is responsible for the grid current control, and more specifically, two PI control loops (one current loop per PFC choke) are implemented. The output of the last-mentioned controllers generates the duty cycle value per PFC leg. In order to balance the flying capacitor voltages, two more PID controllers are used (one per PFC leg). The output of the controller generates the asymmetry on the duty cycles between the PWMx_A and PWMx_B (theoretically PWMx_A and PWMx_B should have the same duty cycle), and it is implemented by subtracting the output of the balancing controller from the PWMx_B duty cycle value. As a final step, the value of the corresponding registers that control the duty cycle of the PWM signals are updated in the microcontroller firmware. The overall control scheme is depicted in Figure 26.

It should be highlighted at this point that at the output of the voltage controller and at the output of both current controllers, feedforward terms are used. To begin with, at the output of the voltage loop controller the load current is multiplied by a gain, and this information is added to the current reference command. The main goal is to achieve faster transient response during the load transients, while keeping the same controller bandwidth. The load current is sensed on the secondary side of the LLC with the LLC microcontroller and UART communication, being used to transfer this information to the XMC4407 primary side controller.

Furthermore, another feedforward term is also added to the output of the PI controller, which is responsible for the PFC current control. This feedforward term takes into account the reference PFC voltage value and the AC input voltage information (polarity and the measured input voltage signal) and calculates the theoretical duty

cycle for the PFC boost operation. Thus, the PI current controller is responsible for compensating any other disturbance related to, for example, the DC link voltage ripple, etc.

At this point it should be noted that on REF_12KW_HFHD_PSU from Infineon, the intermediate DC link voltage is constantly regulated to a value equal to 445 V regardless of the peak value of the AC input voltage. This is feasible because the target DC link voltage is always greater than the peak grid voltage, even in the case when the grid is equal to 305 V_{ac}.

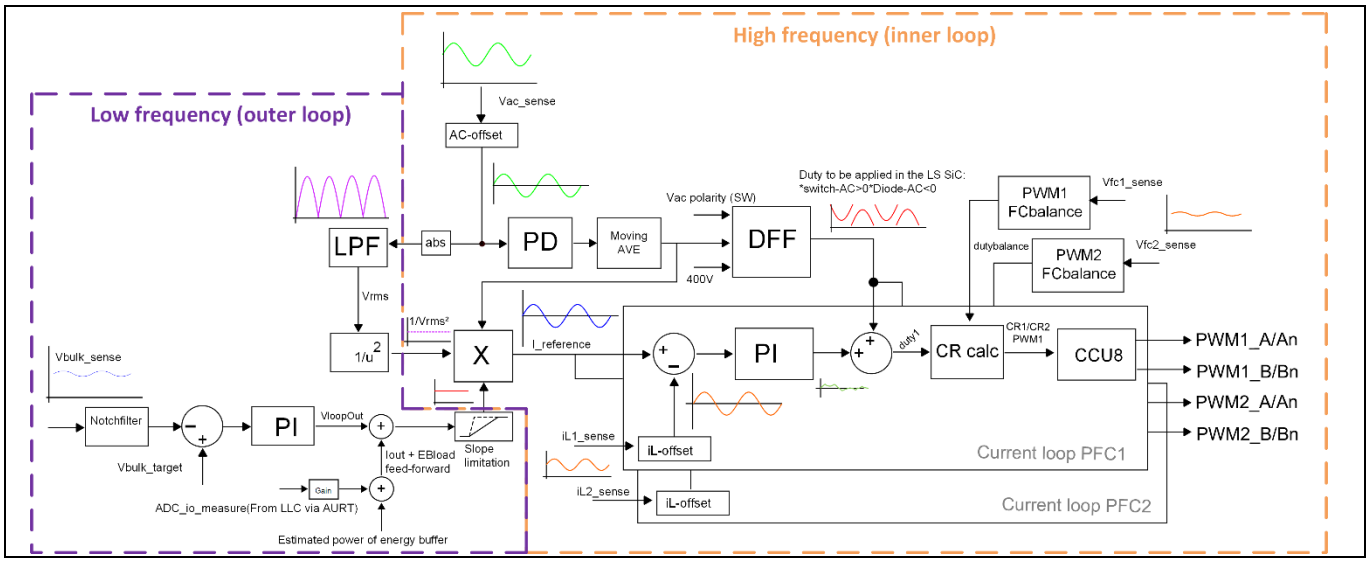


Figure 26 Overall control structure of the 3-level flying capacitor PFC converter

3.1.5 Sensing in the PFC converter

Figure 27 reports a simplified overview of all the measured variables, which are necessary for the control and the protection of the PFC stage in REF_12KW_HFHD_PSU. The microcontroller, with which all the sensing is done, is referenced to the DC-link GND as shown in Figure 27. The sensed variables can be summarized as follows:

- Input AC voltage: Measured with an opamp in differential configuration, also adding 1.65 V of offset to detect both negative and positive polarity. The input voltage polarity is then calculated in the software. The AC input voltage is sensed at the output of the EMI filter for noise reduction
- PFC choke current measurement: Measured with a bidirectional current sensor (one per phase) with magnetoresistive (AMR) technology. The current information is given as an analog signal with 1.5 V of offset, while its sensitivity is 20 mV/A, featuring a bandwidth of 1.3 MHz. In order to ensure the 0 A current value and minimum DC offset on the actual grid current, the output voltage of the sensor is measured before the PFC starts its operation. This is done in order to calculate the real offset value, since the theoretical 1.5 V reference may drift away by some mV. Additionally, the actual voltage of the sensor is also measured during the grid zero crossings, in the short time interval where the current through the boosting choke is zero
- Flying capacitor voltage measurement: Measured with an opamp in differential configuration similar to the circuit used for the AC input voltage sensing, without the offset reference voltage
- Intermediate DC link voltage measurement: Measured using a voltage divider since the microcontroller ADC is referenced on the same GND point. It should be noted that multiple resistors are connected in series to form the voltage divider to meet the voltage clearance requirements

- Bulk capacitance voltage measurement: Measured using a voltage divider since the microcontroller ADC is referenced on the same GND point. Multiple resistors are connected in series for this case as well to meet the voltage clearance requirements

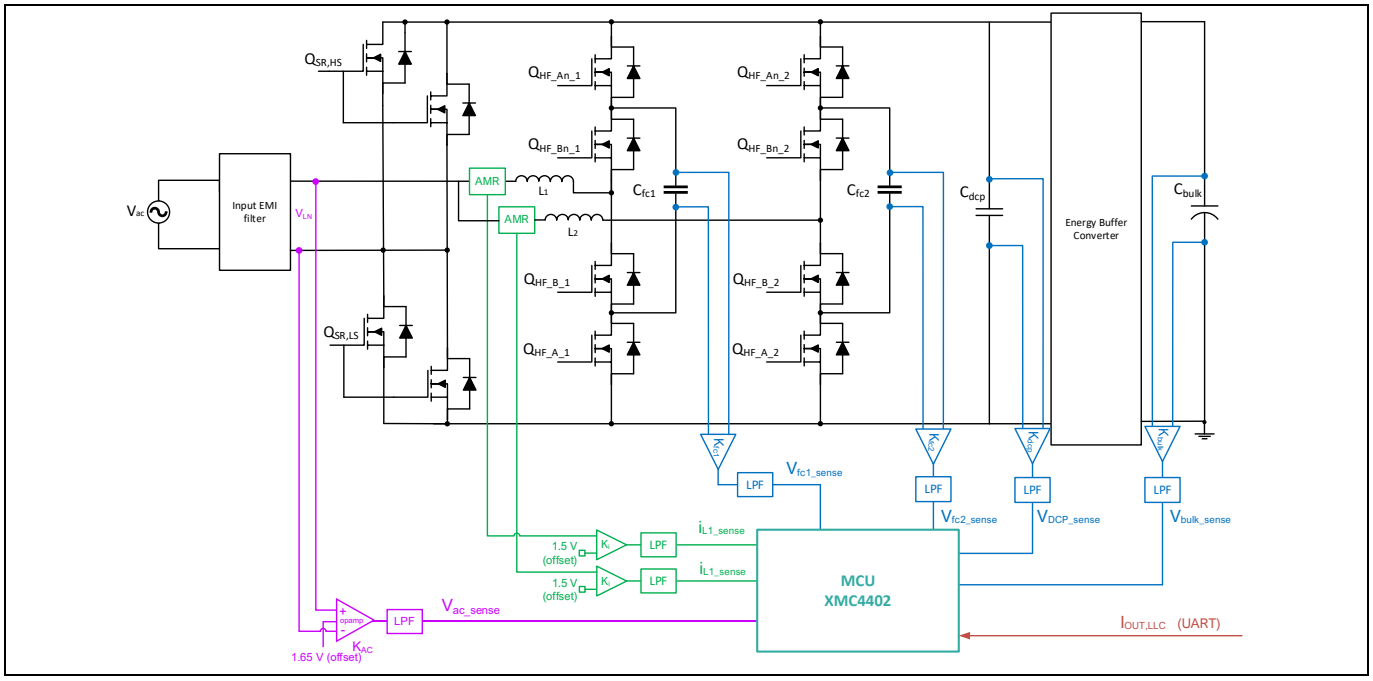


Figure 27 Sensing circuitry of the 3-level flying capacitor PFC converter with XMC™

3.1.6 Driving CoolSiC™ and CoolMOS™ switches

CoolSiC™ Gen 2 switches have been used for all controlled switches of the PFC converter. For the driving voltage of the CoolSiC™, an 18 V/0 V nominal unipolar bias supply has been selected to minimize the $R_{DS(on)}$ of the switches, while maintaining a safe margin for the maximum allowable gate-to-source voltage at the same time.

Figure 28 shows an excerpt of the PFC schematic, denoting the driving scheme for the 3-level flying capacitor high frequency leg. The 18 V rail is generated from the main flyback converter which is referenced to the intermediate DC link voltage GND. To generate the supply voltage for the driver needed to drive the gate capacitance of the switch Q3 (as denoted in Figure 28) the bootstrap technique is used, and the corresponding bootstrap capacitor is charged when Q4 is ON. In order to properly bias the gate driver of the switch Q2, a low power small, isolated power supply is implemented, as shown in Figure 29, using the 1EDN8511B gate driver from Infineon in a self-oscillating configuration to generate the AC excitation voltage for the isolation transformer. Then, the bias supply of the driver of the switch Q1 is generated again with the bootstrap technique, but this time the bootstrap capacitor charges when Q2 is ON. The single channel isolated gate driver 1EDB9275F is used to drive all the PFC switches.

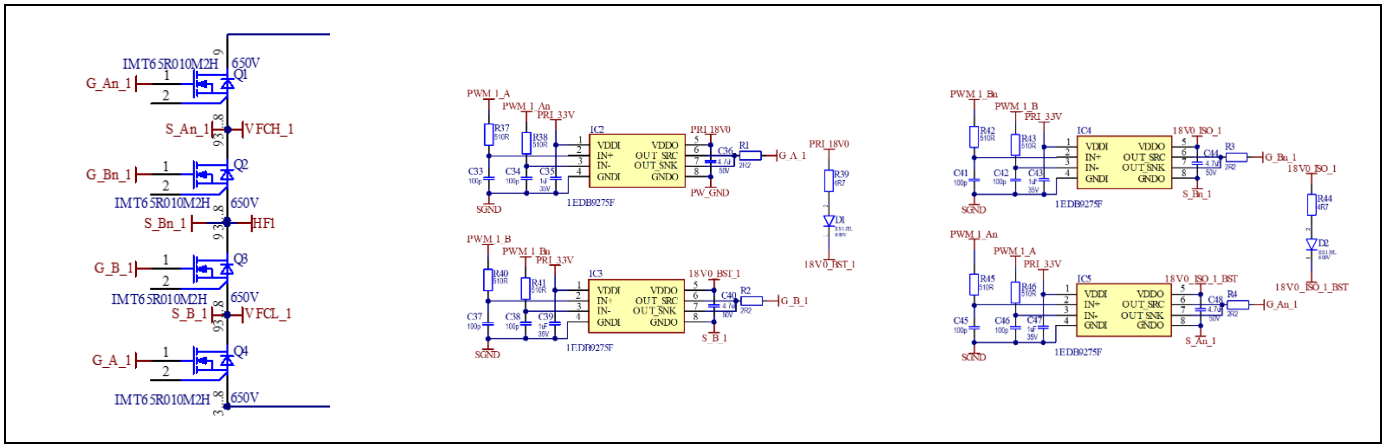


Figure 28 Driving scheme of the CoolSiC™ 3-level flying capacitor high frequency leg

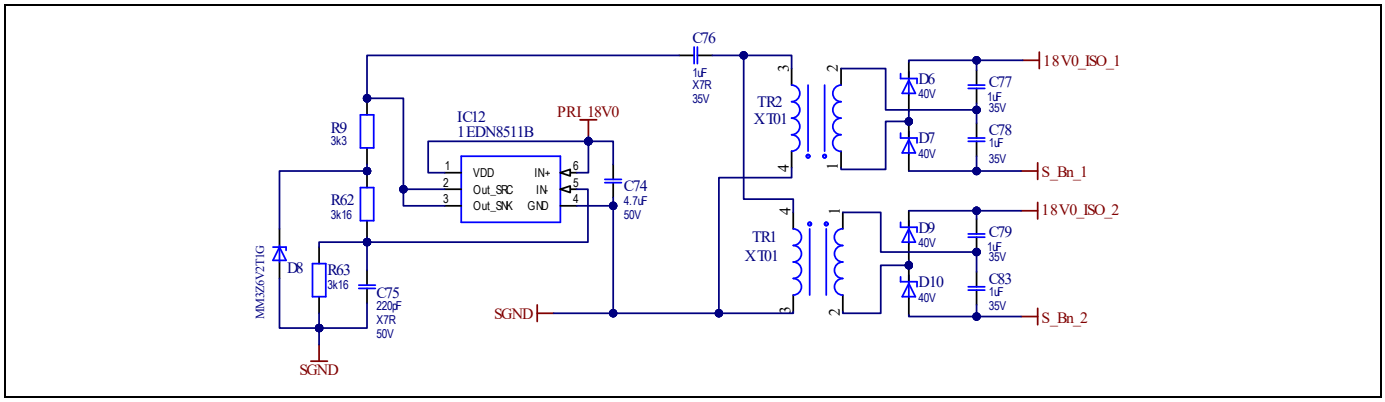


Figure 29 Low power biasing isolated power supply using the 1EDN8511B gate driver

For the low frequency unfolding leg of the PFC stage, CoolSiC™ Gen2 devices are also used, but in this case two devices per commutation slot are used to account for the power losses. The positive thermal coefficient of the SiC makes device paralleling easy. More information about parallelization of SiC devices can be found in [8]. For the driving stage of the low frequency unfolding leg, the single channel isolated gate driver 2EDN7533B is also used, and for the high side gate driver biasing the bootstrap technique is used to lower the BOM cost and minimize the footprint area. In Figure 30, the schematics of the low frequency leg along with the gate driver circuit are depicted.

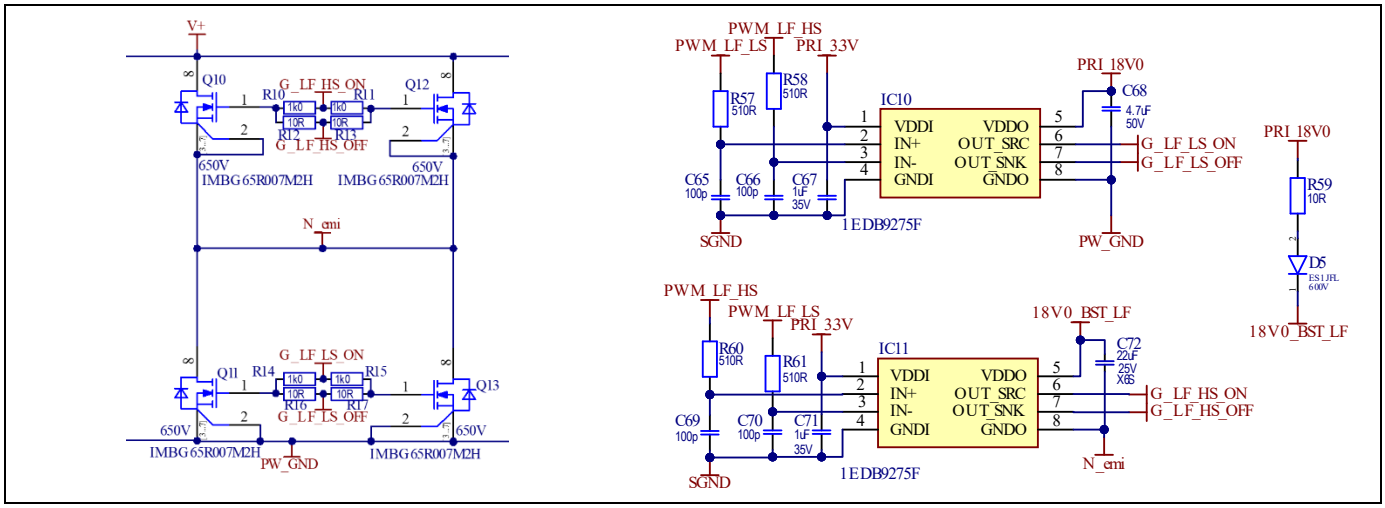


Figure 30 Driving scheme of the CoolSiC™ low frequency unfolding leg of the PFC stage

For the energy buffer half bridge converter, two TOLL CoolSiC™ Gen2 switches in parallel are used for every commutation slot. For each MOSFET pair the single channel isolated gate driver 1EDB9275F is used, and for the biasing of the high side driver a small, low power isolated biasing supply is again implemented using the 1EDN8511B driver in a self-oscillating configuration. In Figure 31 the energy buffer half bridge schematics are shown along with the gate driver circuit.

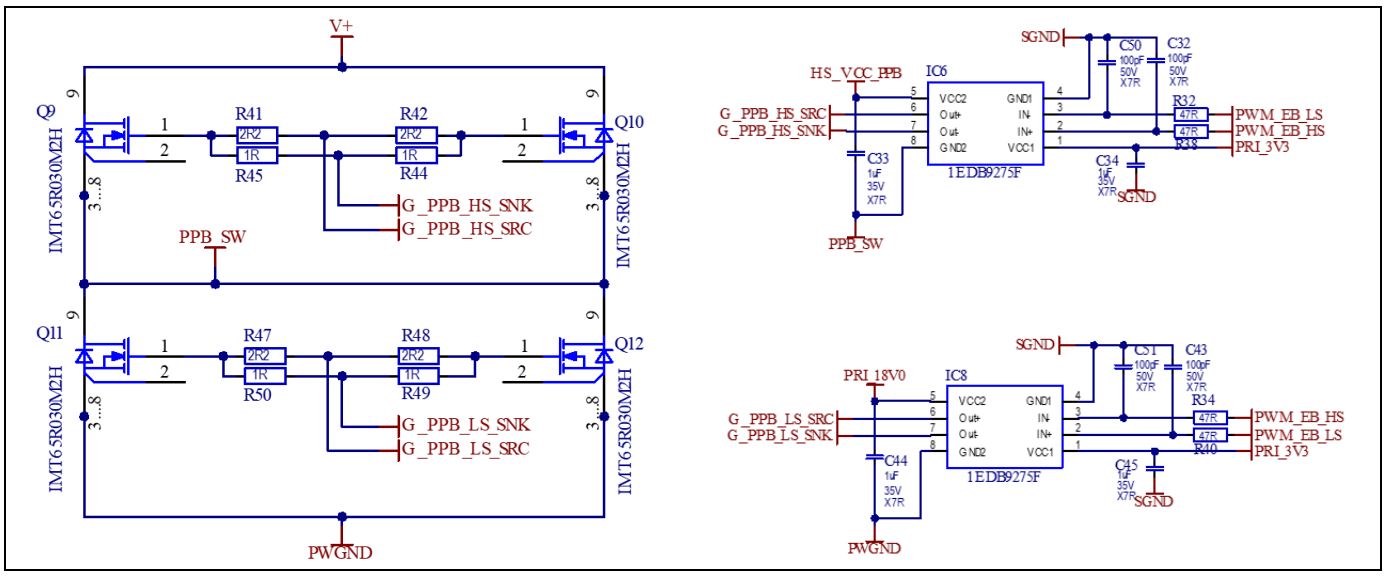


Figure 31 Driving scheme of the CoolSiC™ energy buffer buck-boost converter

CoolMOS™ devices are used for the static switch (two in parallel) in order to directly connect the bulk electrolytic capacitors to the DC link during steady state operation, and also for the MOSFET which is connected in parallel with the inrush current limiting resistor to bypass it during steady state operation. For both the static switch and the inrush switch, the single channel isolated driver 1EDB8275F is deployed, and again a biasing isolated power supply is implemented using the 1EDN8511B gate driver as the square wave oscillator. For the inrush switch there is no need for an isolated supply since the source potential is referenced to the same GND as the microcontroller, which controls the inrush switch operation. Thus, the non-isolated gate driver 1EDN8511B is used to drive the gate of this device. In Figure 32, the driving circuits for the static switch and the inrush switches are shown.

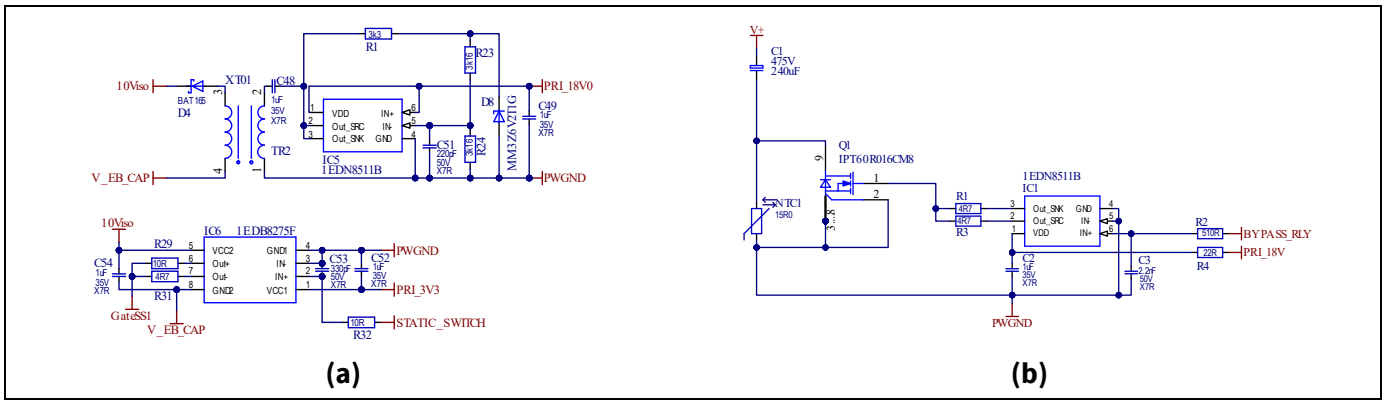


Figure 32 Driving scheme of the CoolMOS™ (a) static switch and (b) inrush switch

3.2 High frequency LLC resonant converter

One of the key elements to increase power density above 100 W/in^3 while keeping the highest possible efficiency is to reduce the volume of the high frequency transformer, by increasing the operating frequency of the DC-DC converter. A simplified schematic of the chosen DC-DC isolated topology is depicted in Figure 33.

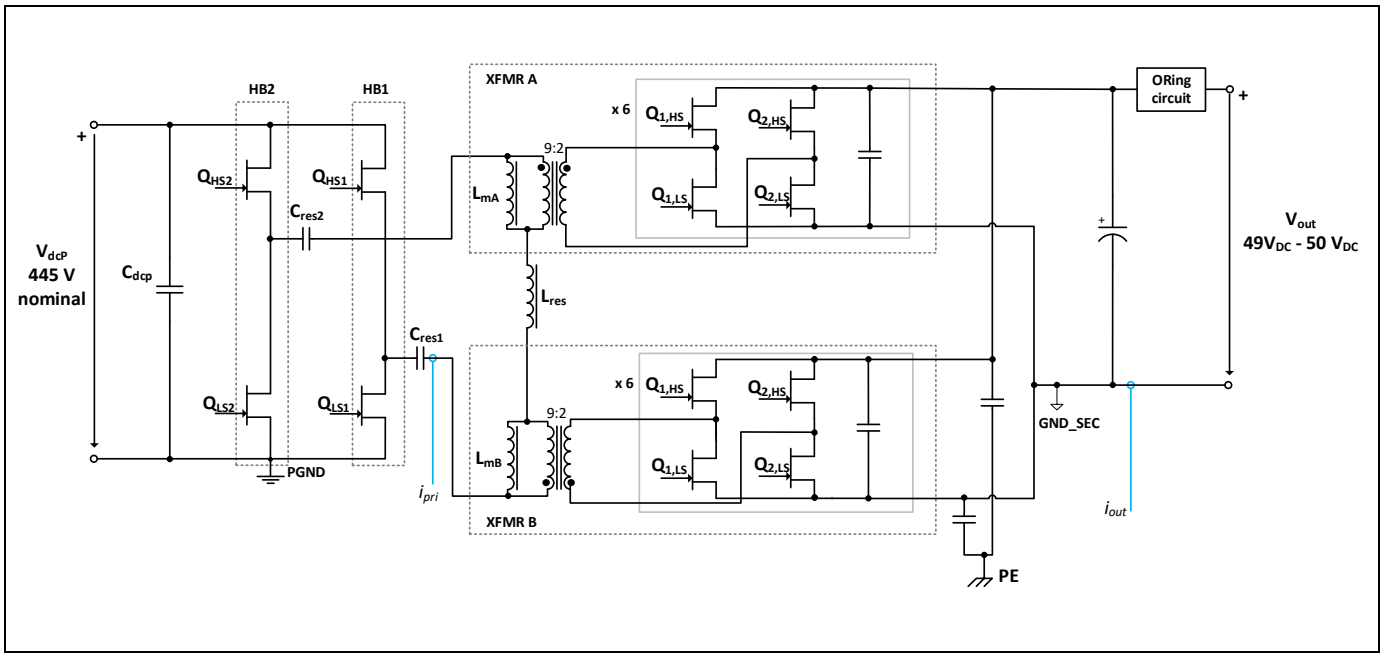


Figure 33 Simplified schematic of the LLC DC-DC converter in REF_12KW_HFHD_PSU

For the primary side of the LLC converter, a full bridge configuration is used by deploying Infineon CoolGaN™ technology. For each primary device slot, two CoolGaN™ devices are connected in parallel to lower the commutation path resistance and to spread the power losses across more devices and a larger PCB area. The full bridge primary devices are populated on a daughterboard along with the primary side microcontroller and the energy buffer semiconductor devices. The two resonant capacitors are implemented in the form of two resonant capacitor banks, and are populated on the main board as shown in Figure 6. For the secondary side, the full bridge configuration is also deployed using the MV CoolGaN™ devices for the synchronous rectification bridge. In order to spread the losses among different devices and lower the path resistance, 96 devices in total are used, which are embedded on the transformer structure. More details about the transformer configuration are given in Section 3.2.2.

For the transformer configuration and connection, a similar approach is followed for the implementation of this power supply unit, as in the one used for REF_8KW_HFHD_PSU [7]. More specifically, the primary side windings of the two transformers are connected in series, while the secondary side H-bridges are connected in parallel to achieve lower current per transformer on the secondary side. Furthermore, the primary series connection helps with the current balancing on the output of each high frequency transformer, since the same magnetizing current is ensured.

3.2.1 Performance of the standalone topology block

Figure 34 shows the measured efficiency and power losses of the LLC converter, plotted for 445 V_{DC} input, which is also the nominal bulk voltage of the PSU. Efficiency peaks at 98.65% at 50% of the rated load and remains above 98.2% from 25% to 100% of the rated output power.

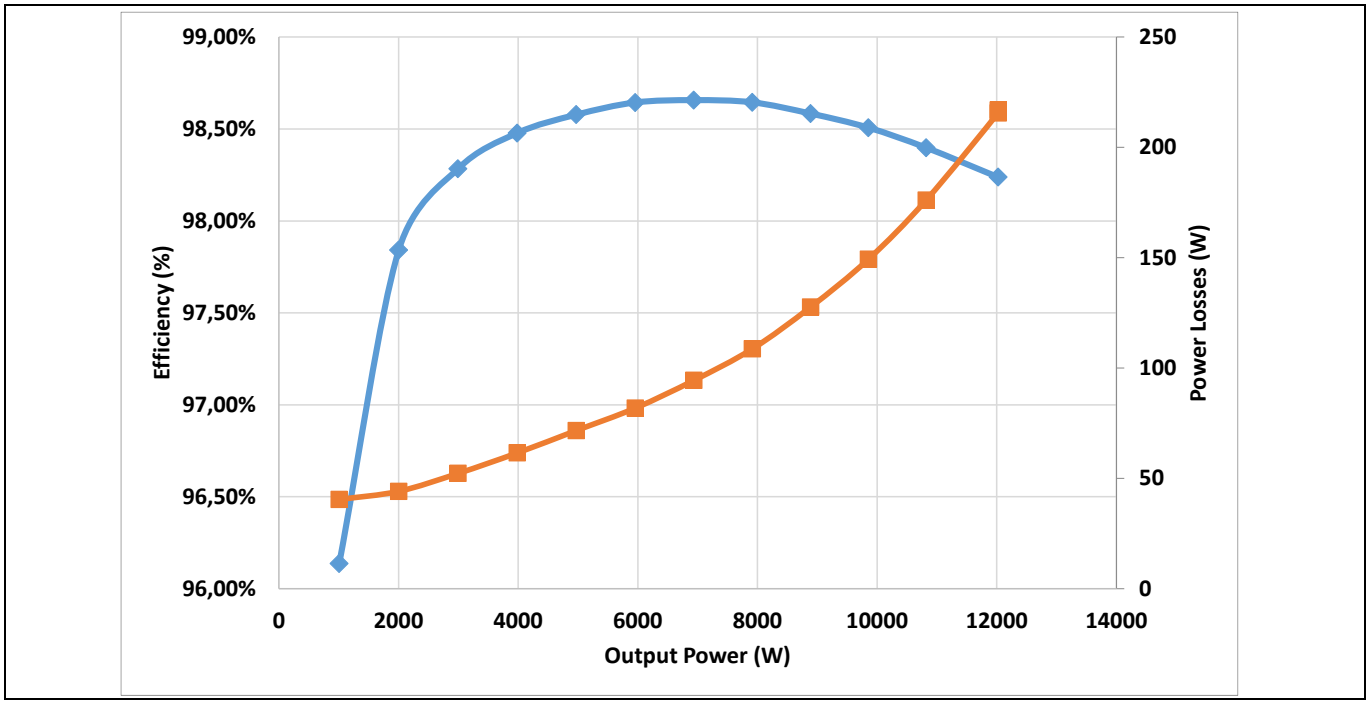


Figure 34 LLC DC-DC standalone: Efficiency and power losses at 445 V input

Figure 35 and Figure 36 shows an estimation of the breakdown of the power losses for the LLC converter only at 100% and 50% load respectively. The main contributors to power losses are conduction losses of the primary side, the synchronous rectifiers, and total copper losses of the series and parallel inductance, and of the main transformer itself.

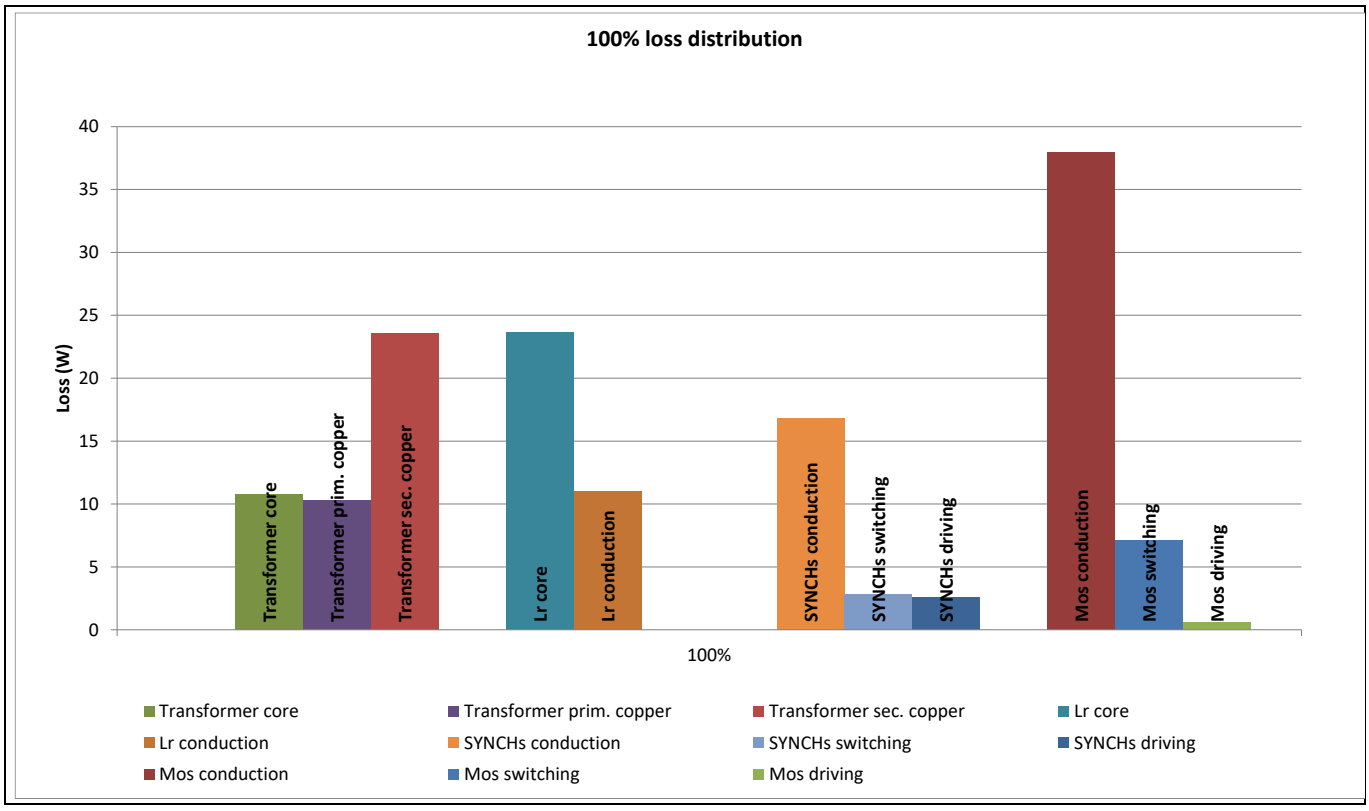


Figure 35 Power loss breakdown for the LLC DC-DC stage at 100% of rated power

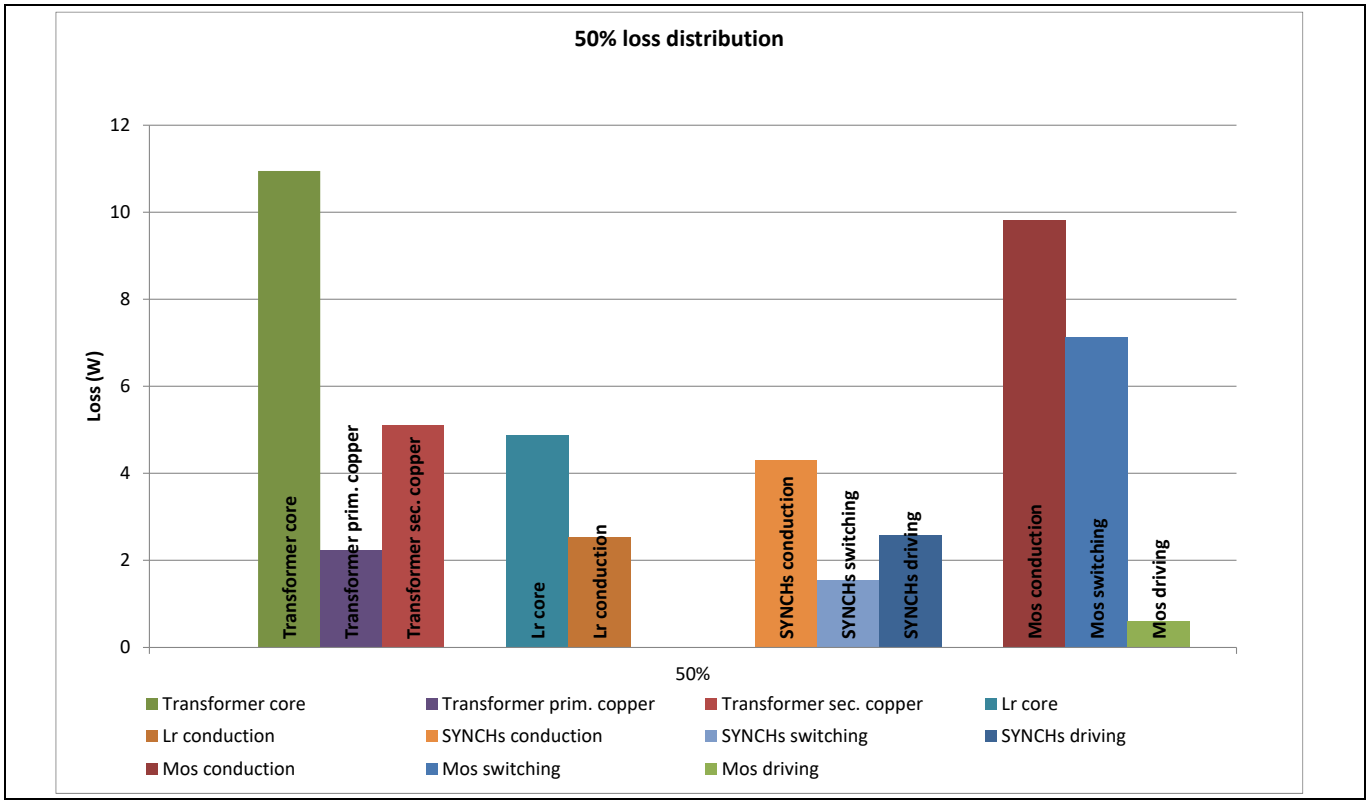


Figure 36 Power loss breakdown for the LLC DC-DC stage at 50% of rated power

3.2.2 LLC-integrated transformers and inductors

Starting with the high frequency transformer, it should be noted that a hybrid planar approach is used. Two similar transformers are implemented with a planar magnetic structure that integrates the synchronous rectification stage as well. For the planar structure, the minimum gap is implemented using a 50 µm thickness Kapton tape to avoid any partial saturation of the core. This leads to a high primary inductance value, which is not adequate to achieve zero voltage switching (ZVS) operation for the primary switches. In order to increase the magnetizing current, an inductor, implemented with Litz wire, is placed on top of the planar transformer structure and is connected in parallel to the primary winding to decrease the total magnetizing inductance. This inductor serves as the main magnetizing inductance. In Figure 37 the detailed structure of the high frequency transformer is shown. The core shape used for the two transformers is PQ40, while the core material is DMR59 from DMEGC, which provides low volumetric core losses in the operating frequency span.

In order to comply with the PSU height limitation (40 mm) imposed by the OCP standard, the maximum height of the transformer should also be limited to 40 mm. For this reason, the overall height of the magnetic structure is 37 mm. Additionally, cutouts are implemented on the main PCB in order to fit the transformers inside the PSU chassis.

As shown in Figure 37, Kapton foil is used between the primary and the secondary winding PCBs in order to increase the dielectric strength. Additionally, FR4 rings spacers are also used to increase the distance between the primary and secondary windings, leading to deceased interwinding capacitance. The decreased interwinding capacitance leads to better EMI performance of the overall PSU and acts in favor of the ZVS on the primary devices. Furthermore, an FR4 ring spacer is also used to increase the distance between the Litz wire, used to implement the magnetizing inductance and the 1.8 mm gap, as depicted in Figure 37. This is needed to minimize the winding fringing losses generated from the stray field near the gap of the magnetic structure.

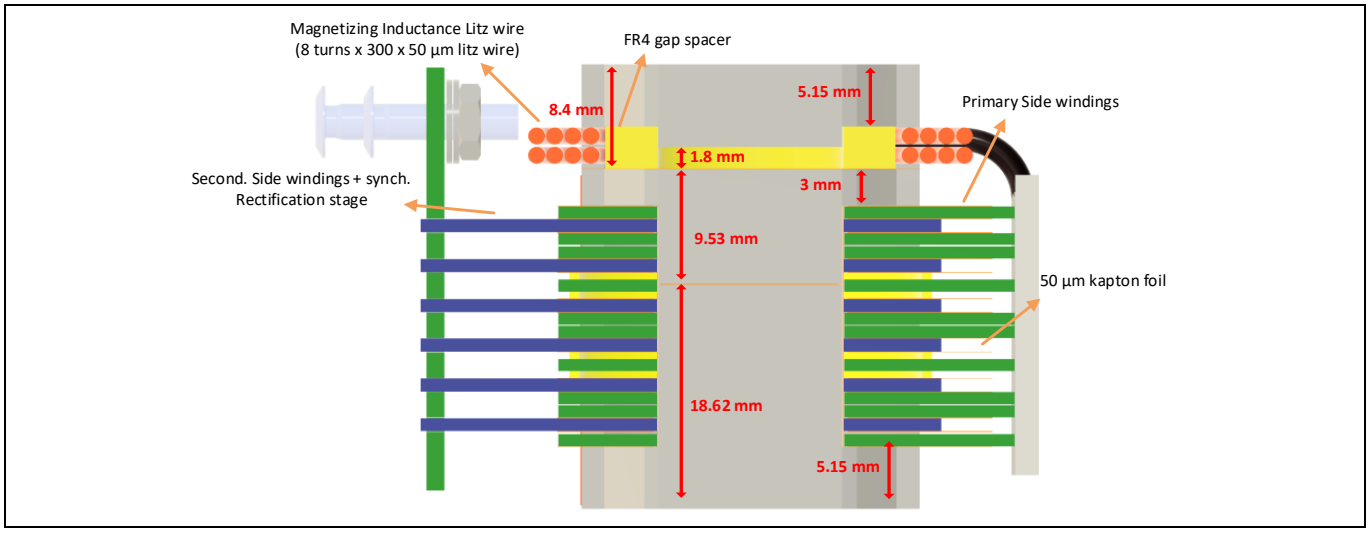


Figure 37 Detailed structure of the high frequency transformer implemented for the LLC converter

The turns ratio of each transformer is 9:2, and by connecting the primaries in series and the secondaries in parallel an effective turns ratio of 18:2 is achieved for the LLC converter. For the construction of each transformer three different versions of PCBs are used, two of which are used to implement the primary winding and one for the secondary. For the primary winding, we need nine turns in total and for this reason two different 6-layer PCBs are designed, one with four turns and another with five turns. In both PCBs, the outer copper layers are etched in order to provide the required clearance and creepage between primary and secondary side. By connecting these two PCBs in series a nine-turn winding can be implemented. The parallel connection of multiple PCBs is also mandatory to account for reduced winding resistance and decreased conduction losses. In this case five PCBs of each are connected in parallel. The PCB layer arrangement for the two PCBs needed to implement the primary winding is depicted in detail in Figure 38.

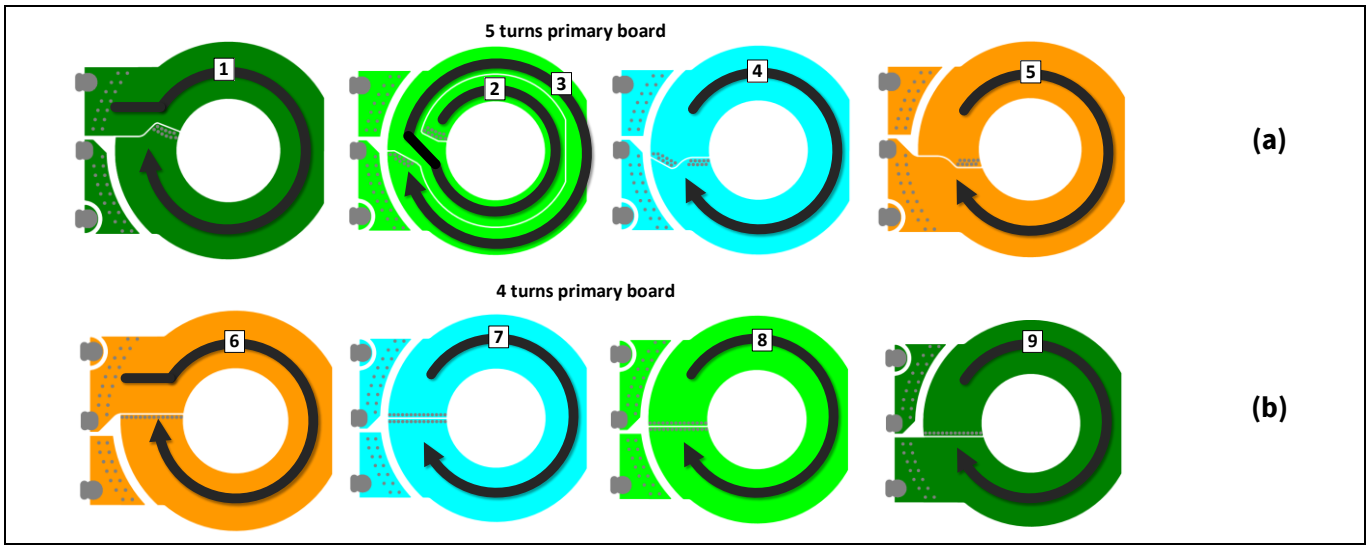


Figure 38 Detailed PCB layer arrangement for (a) the 5-turn primary board and (b) the 4-turn primary board

In Figure 39 the 3D model of the transformer secondary side PCB is shown, along with the PCB layers from top to bottom. On the secondary-side board, a pair of two turns is implemented, while the synchronous rectification full bridge stage with MV CoolGaN™ devices is integrated on the PCB with the driving stage. For the synchronous rectification stage two devices are connected in parallel per commutation slot placed on the top

and bottom of the PCB. The layout of the winding is depicted in Figure 39 (b). The secondary winding starts from the top and bottom layer in parallel for half a turn, then continues in the second and fifth layer with a full turn in parallel on both layers and finishes again on the top and bottom layers implementing the remaining half turn again. To accommodate the high output power, six secondary boards are populated in parallel on each transformer.

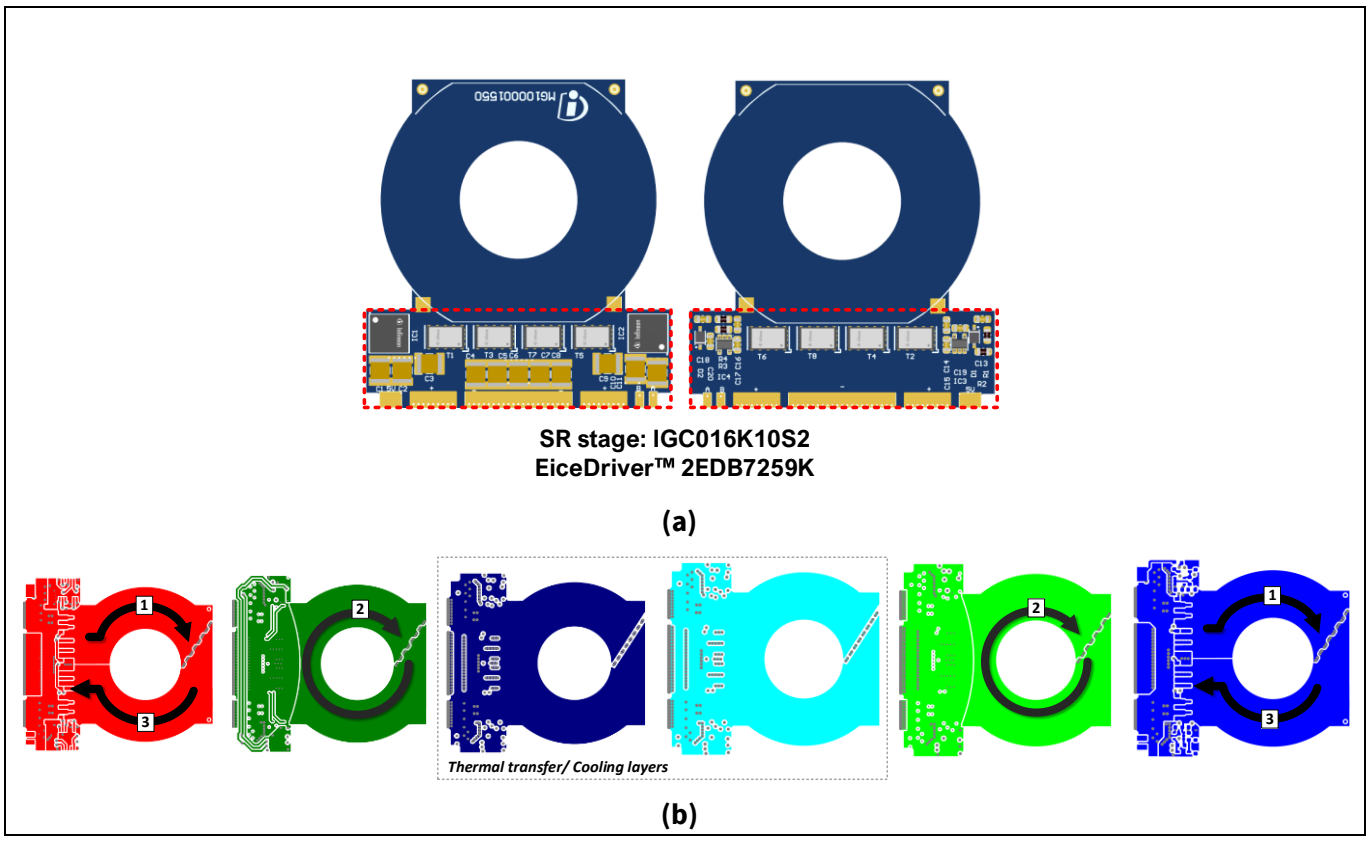


Figure 39 An overview of the primary- and secondary-side winding PCBs

Although only four layers are needed for the winding implementation, a six-layer board has been designed for the secondary board with the two middle layers serving as thermal transfer or cooling layers. These two layers are electrically connected at the output terminals of the secondary boards. The basic idea behind this concept is to dissipate the heat generated internally in the transformer construction using the extra copper inside the transformer as a heat-transfer layer. Then, by electrically connecting the secondary-side board to the copper busbar, through a backplane PCB, the heat can be dissipated more effectively. The thermal simulation results are shown in Figure 40, using a simplified transformer model, comparing the secondary board design with and without the cooling layers considering the same core and copper losses. On both cases, a fixed airflow of 5 m/s is considered at 25°C intake temperature and the same core size. Additionally, since this is a simplified model, only one secondary board is used and in order to block the air going inside the core to cool directly the PCB, an FR4 air blocker is populated to investigate the effectiveness of the cooling layers, as depicted in Figure 40 (c). From the simulation results it is clear that by deploying these two extra thermal transfer layers, the temperature can be reduced by ~10%. It is noted here that the copper thickness of every layer on the secondary-side board is 140 µm, while only 35 µm copper thickness is used for the cooling layers, keeping the overall board close to 1 mm.

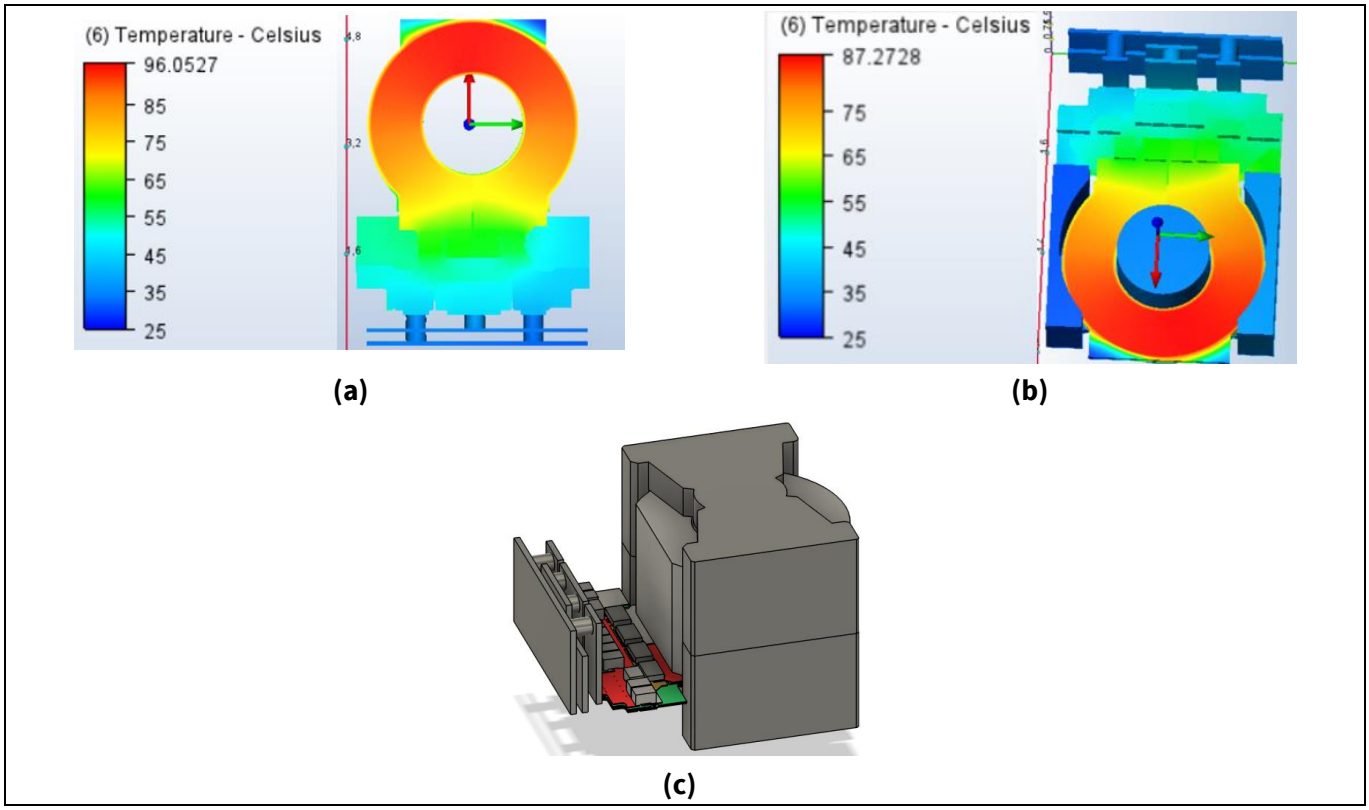


Figure 40 Thermal simulation results and cooling performance comparison between the design (a) without the cooling layers, (b) with the cooling layers, and (c) the simplified model for the simulation

For the series resonance inductor, a separate magnetic component is implemented since the height of the transformer is increased compared to the one used for REF_8KW_HFHD_PSU [7], offering increased window for more parallel connected primary and secondary PCBs to accommodate the higher power level. Thus, the integration of the resonance inductor on top of the magnetic structure is not possible in this case. In Figure 41 the 3D drawings of the resonance inductor are depicted along with the flux direction in the core. As can be seen, the total resonance inductance is divided into two separate inductors with two turns each achieving half of the total resonance inductance. These two resonance inductors are connected in series, achieving a resonance inductor with a value of 1.65 µH nominal. In order to decrease the core losses, the winding direction is done in a way that flux cancelation is achieved on the I piece on the center of the magnetic structure, which separates the two chambers. For the resonance inductor custom PQ35 cores are used with a 2.4 mm gap on each side, and the core material is DMR59 in this case too.

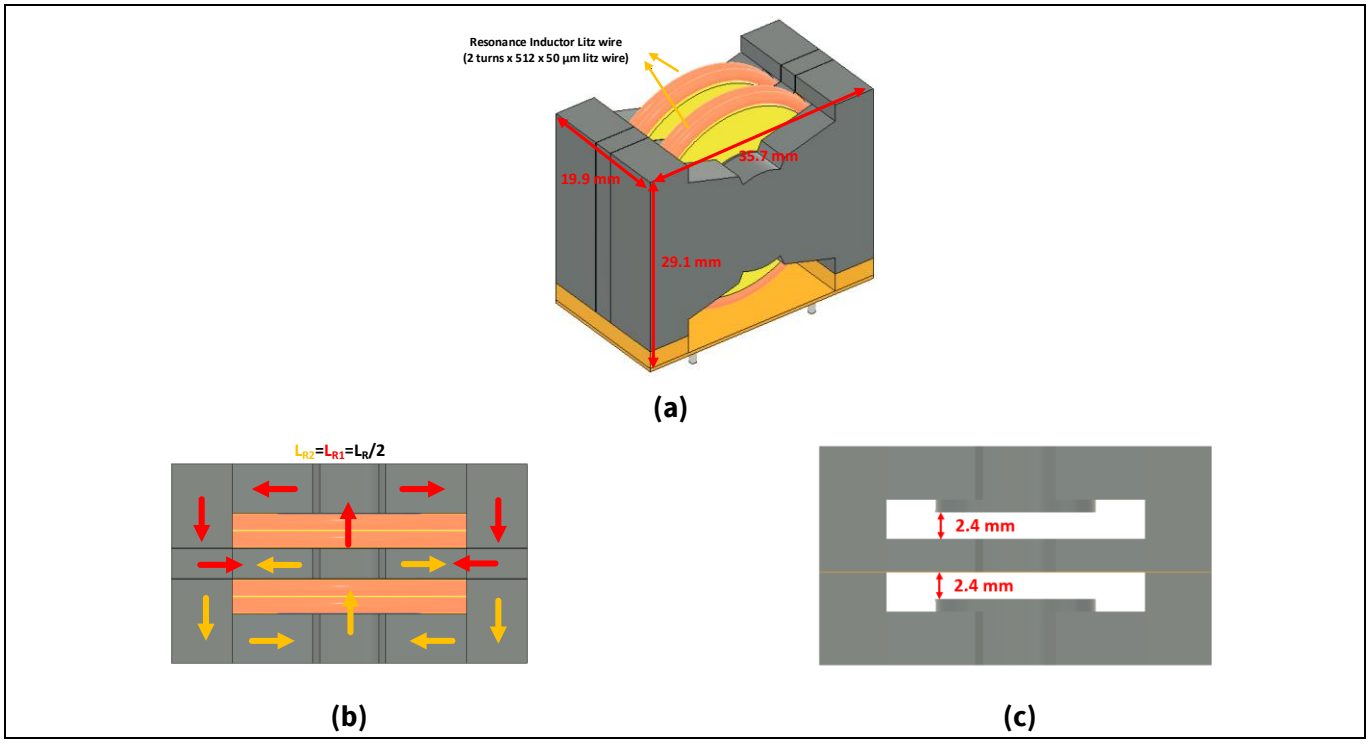


Figure 41 (a) 3D drawings of the resonant inductor structure, (b) graphical visualization of the flux orientation inside the core, and (c) the core structure of the resonance inductor

3.2.3 Driving CoolGaN™ switches of the LLC converter

As explained previously, a full bridge configuration is used for the primary side of the LLC converter. For each high side and low side slot, two CoolGaN™ GIT 650 V devices, 25 mΩ each (IGT65R025D2), are connected in parallel to reduce the conduction losses. For parallelization of the GaN devices, a common mode choke is added in the gate loop to increase the common mode immunity. For further information on how GaN devices can be paralleled effectively, refer to [9].

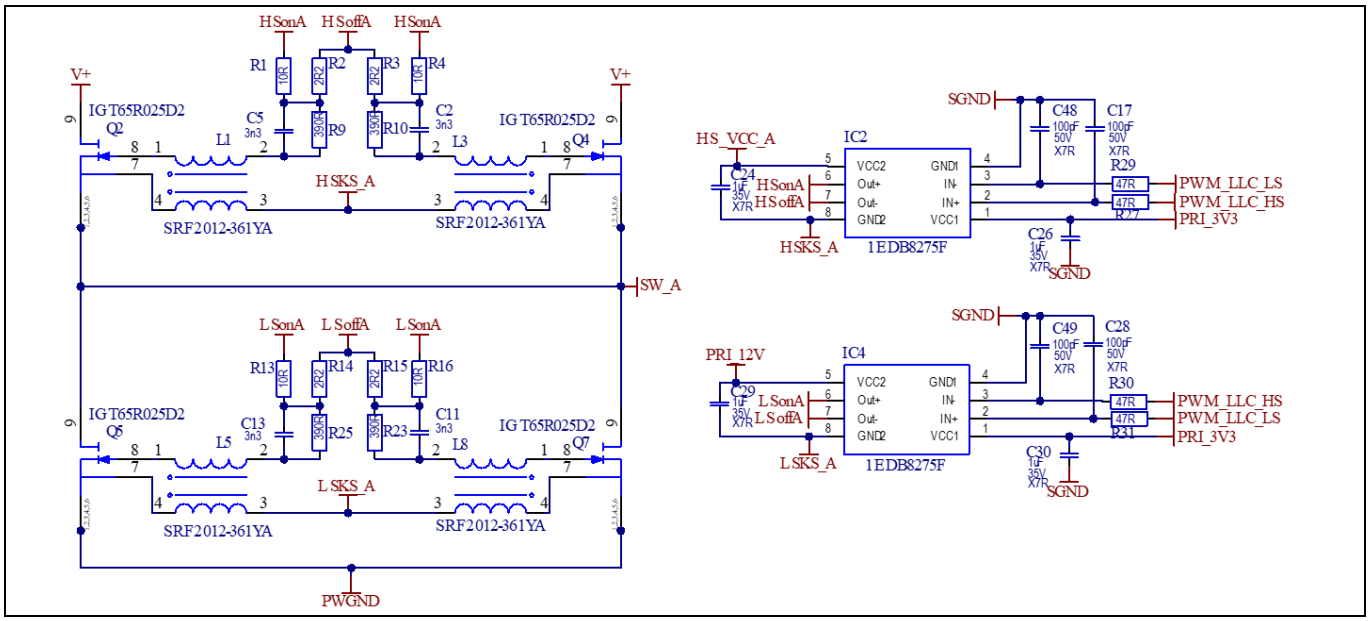


Figure 42 Driving scheme of the CoolGaN™ on the primary side of the LLC converter

For both high and low side switches the single channel isolated gate driver 1EDB8275F is used, and as shown also on the schematics (Figure 42) the PWM signals from the microcontroller are used to interlock the drivers and prevent any shoot-through situation. For the biasing of the drivers 12 V is used. For the low side driver, the 12 V rail (PRI_12V) is generated using an LDO regulator, which is supplied directly from the 18 V rail (PRI_18V0). For the driver, which controls the high side switch, the 12 V rail should be generated with respect to the switching node, and for this reason a low power, isolated power supply is implemented using the 1EDN8511B single channel non-isolated driver, in a self-oscillating configuration, as depicted in Figure 43. The oscillator in this case is powered with the 18 V supply from the flyback converter (PRI_18V0) and the two 12 V isolated rails (HS_VCC_A and HS_VCC_B) are regulated by applying the proper duty cycle to the primary side of the XT01 (TR1 and TR2) transformers.

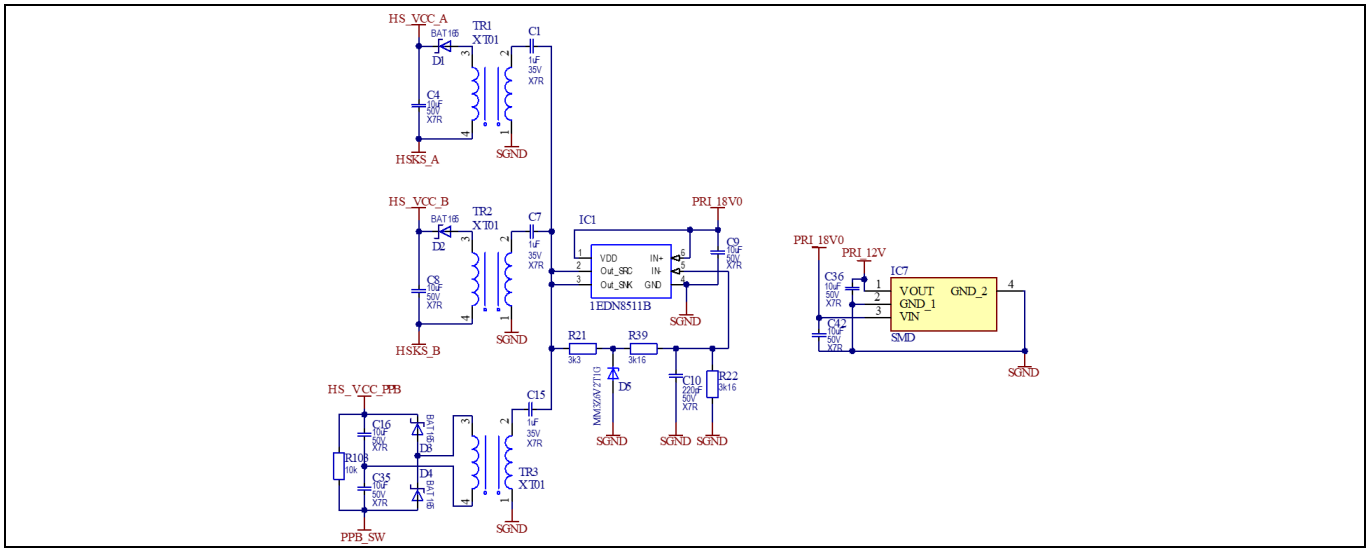


Figure 43 Biasing of the high-side driver for CoolGaN™ driving

For the secondary side of the LLC converter, a full bridge synchronous rectification stage is adopted, deploying 100 V MV CoolGaN™ switches, and more specifically the IGC016K10S2 is selected featuring 1.6 mΩ $R_{DS(on)}$. For each switch of the full bridge converter, two GaN devices are used in parallel to reduce the conduction losses on the given PCB area, as much as possible. For the driving circuit of the GaN devices, the dual channel isolated driver 2EDB7259K is used, and for the biasing of the high side channel of the driver, the bootstrap technique with an additional LDO regulator is used, as shown in Figure 44. An additional LDO regulator is needed, since the bootstrap capacitor can be overcharged due to the higher source-to-drain voltage drop of the GaN devices compared to Si devices. This overcharging can lead to potential damage of the sensitive gate-to-source capacitance of the GaN devices.

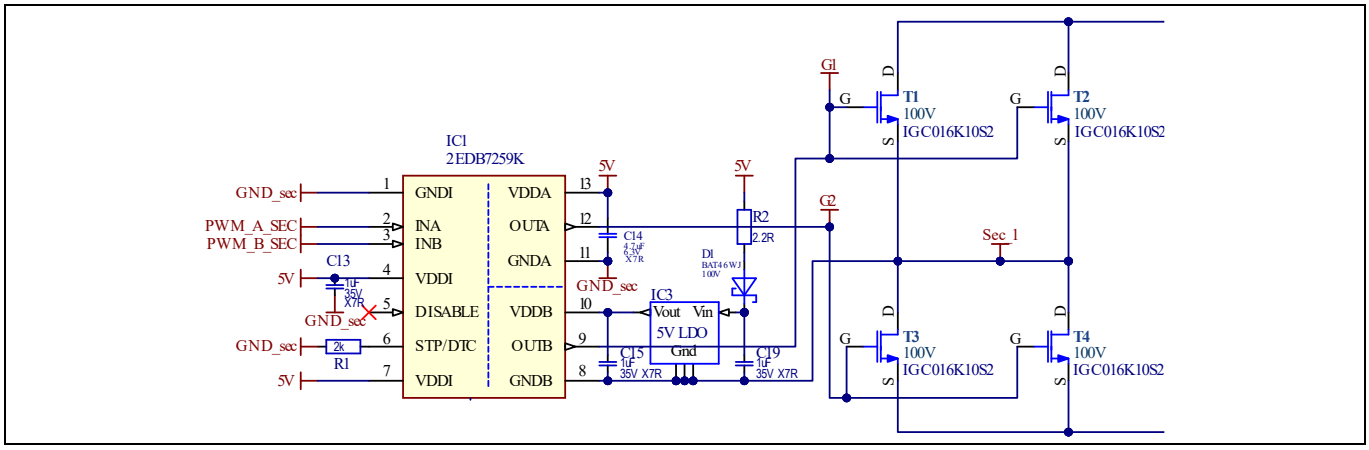


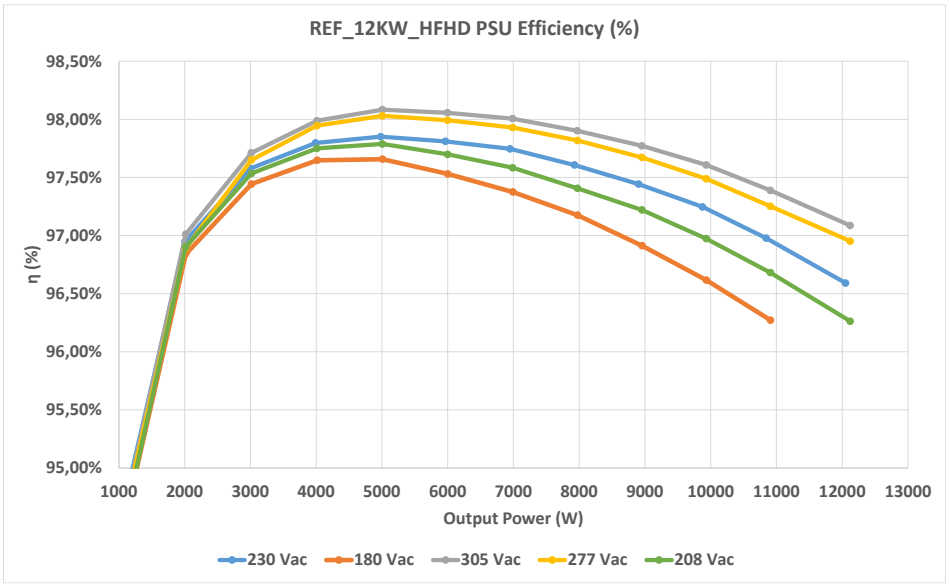
Figure 44 Driving scheme of the CoolGaN™ MV devices on the secondary side of the LLC converter

4 Experimental results

4.1 Steady-state performance

4.1.1 PSU efficiency curves and power losses

Figure 45 shows the efficiency measurements of the whole PSU for steady-state operation at different AC input voltages. The efficiency measurements have been obtained with a WT5000 power analyzer with 10 kHz input and output line filters, with 64 samples averaging. The power converter was enclosed inside the metallic chassis, and the fan consumption is included.



(a)

(b)

Figure 45 (a) Measured efficiency and (b) power losses of REF_12KW_HFHD_PSU for different input line voltages (180 V_{AC}, 208 V_{AC}, 230 V_{AC}, 277 V_{AC}, and 305 V_{AC}) with fan power consumption included

4.1.2 PSU power factor correction and iTHD

Figure 46 and Figure 47 depict the power factor and the total harmonic distortion (iTHD) of the PSU input current measured at 305 V_{AC}, 277 V_{AC}, 230 V_{AC}, 208 V_{AC}, and 180 V_{AC} line voltages and 50 Hz grid frequency. The iTHD and PF measurements have been performed on the full PSU operating in steady state conditions using the WT5000 power analyzer from Yokogawa.

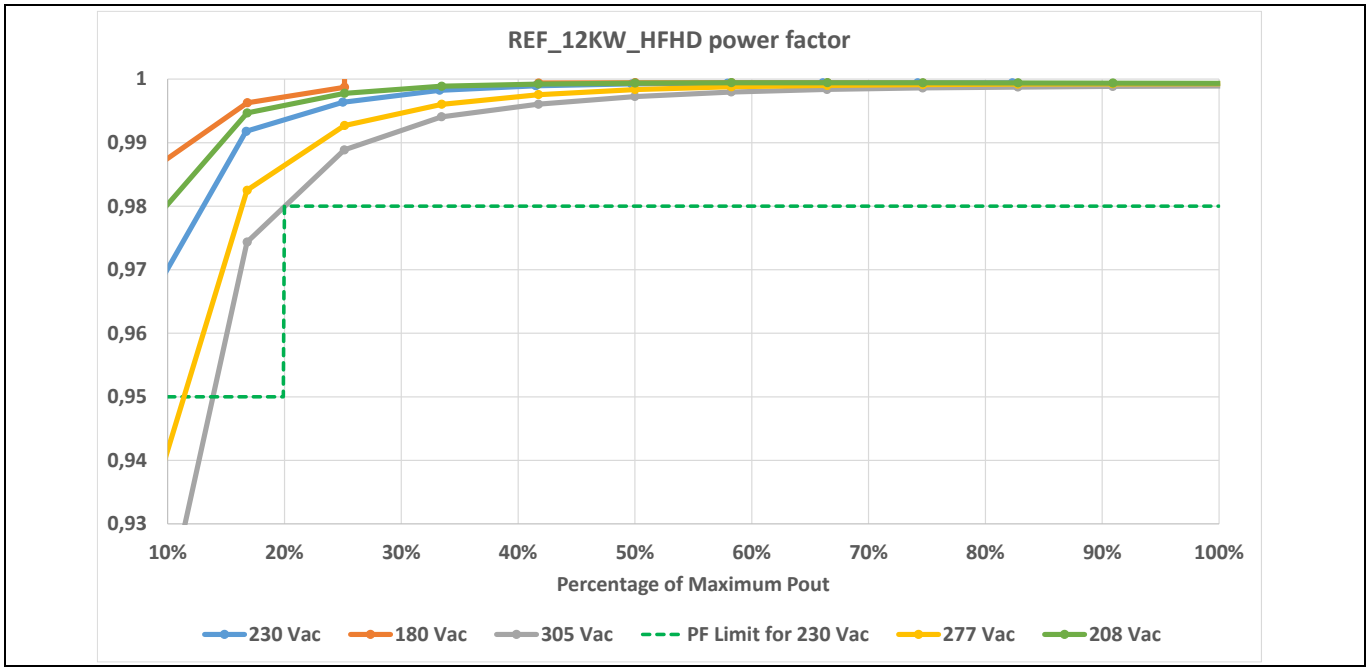


Figure 46 Power factor (PF) of the PSU and OCP power factor limit

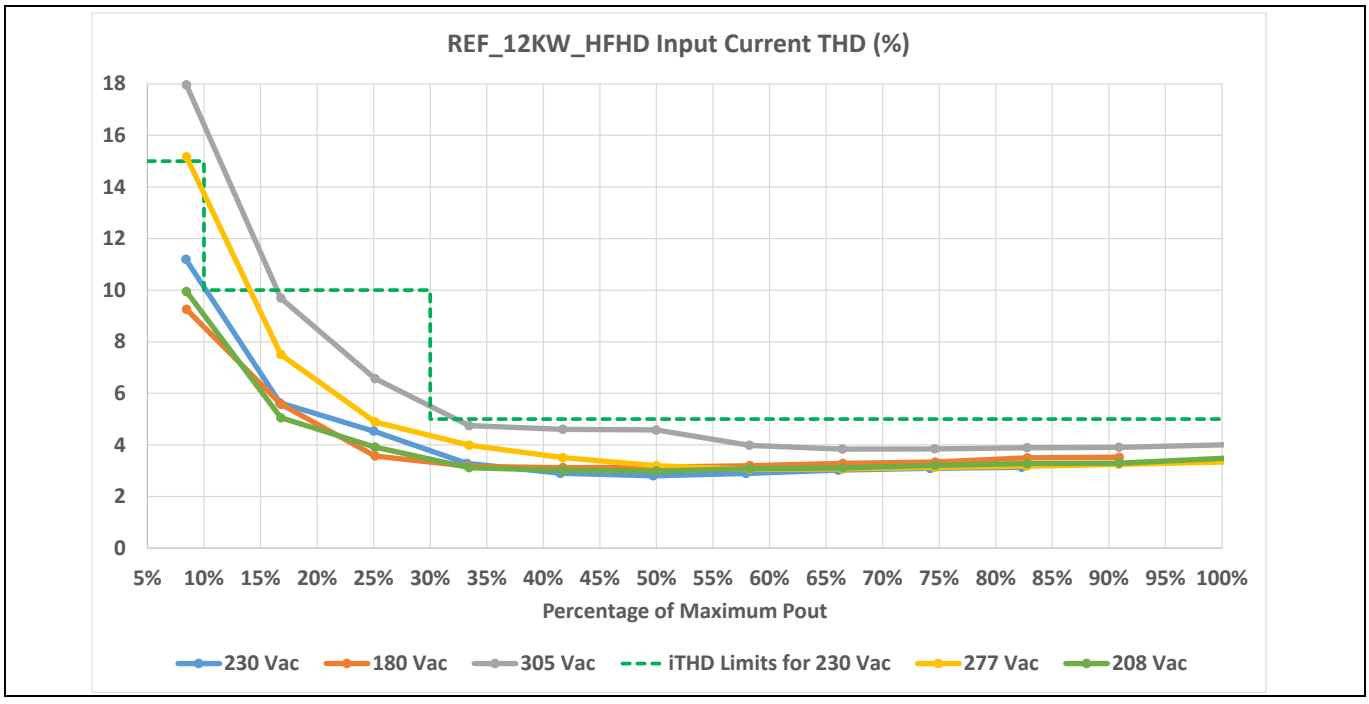


Figure 47 Input current total harmonic distortion (iTHD) of the PSU and OCP iTHD limit

4.1.3 PSU startup

In Figure 48 the full PSU startup is depicted for full load at the output of the power supply. During the startup phase of the PSU, the DC link voltage rises and the C_{dcp} capacitance is charged through the inrush diodes and body diodes of the synchronous rectification leg of the PFC. The small electrolytic capacitor which is located on the DC-link is charged initially through the NTC, which is short circuited during steady state through a MOSFET. As the DC link voltage rises, the main flyback biasing converter is activated and the primary side microcontroller is powered up. The microcontroller initially enables the bottom switches of the 3-level flying capacitor PFC in order to charge the flying capacitor close to the steady state value as explained in Section 3.1.2. When this charging phase is finished, the PFC operates according to the closed loop control described in Section 3.1.4 and the voltage on the intermediate DC-link (V_{dcp}) starts to rise to the steady state value (~445 V).

After the V_{dcp} voltage reaches the steady state value, the energy buffer starts to operate in BUCK mode, transferring energy from the intermediate DC link to the bulk capacitance in order to charge it to the same steady state value. In this time interval, when the energy buffer operates in buck mode, the energy buffer inductor current and the grid current increase in a controlled manner. When the voltage difference between the V_{dcp} and the V_{bulk} is approximatelly10 V the static switch is enabled, and the bulk electrolytic capacitors are connected to the intermediate DC link for steady state operation.

The next step is the startup of the LLC converter. The primary current of the LLC converter (black colored waveform) starts to rise and energy is delivered from the intermediate DC link to the output capacitors and the load. The output voltage also increases monotonically until the steady state value, which is calculated according to the droop function (50 V at 0% of the load, 49 V at 100% of the load). In Figure 49 the converter startup is also depicted when with no load at the output for the sake of completeness denoting the proper operation, with the main difference identified being the different rise time of the output voltage, because of the different gain curve of the LLC converter.

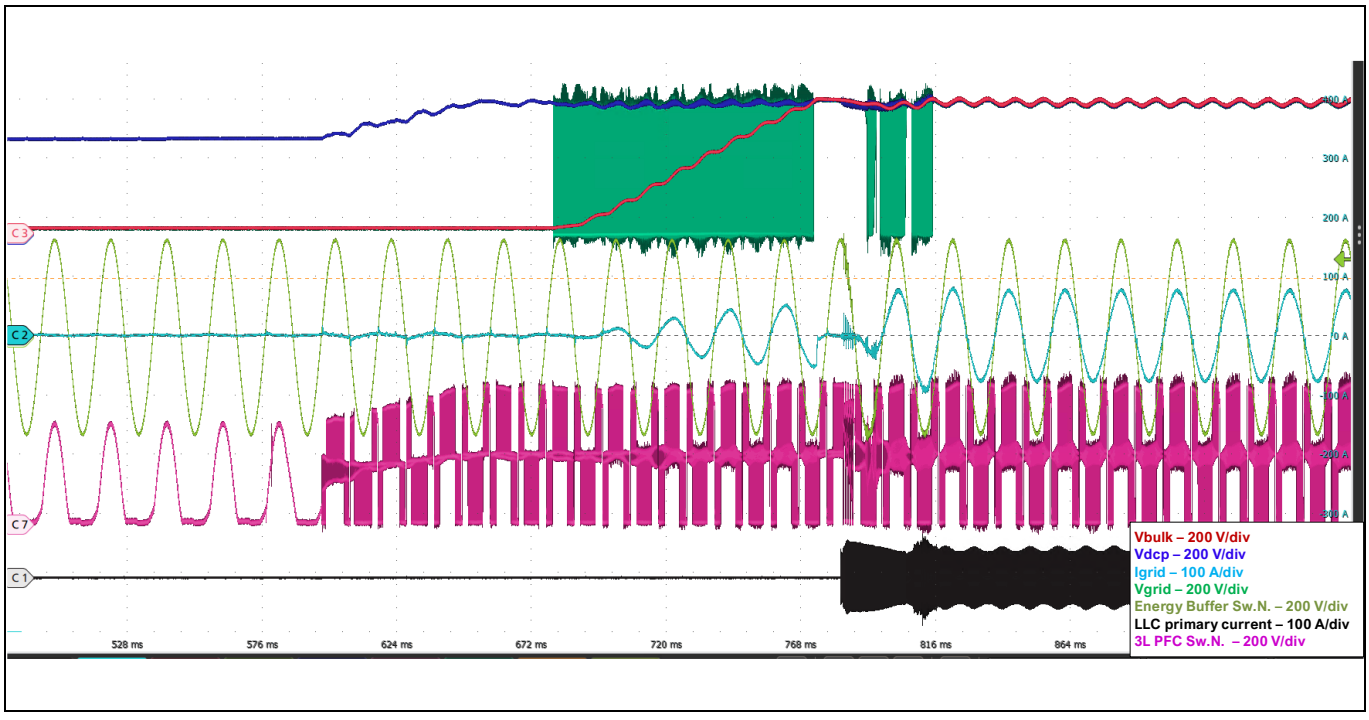


Figure 48 PSU startup at 230 V_{AC} input and full load at the output

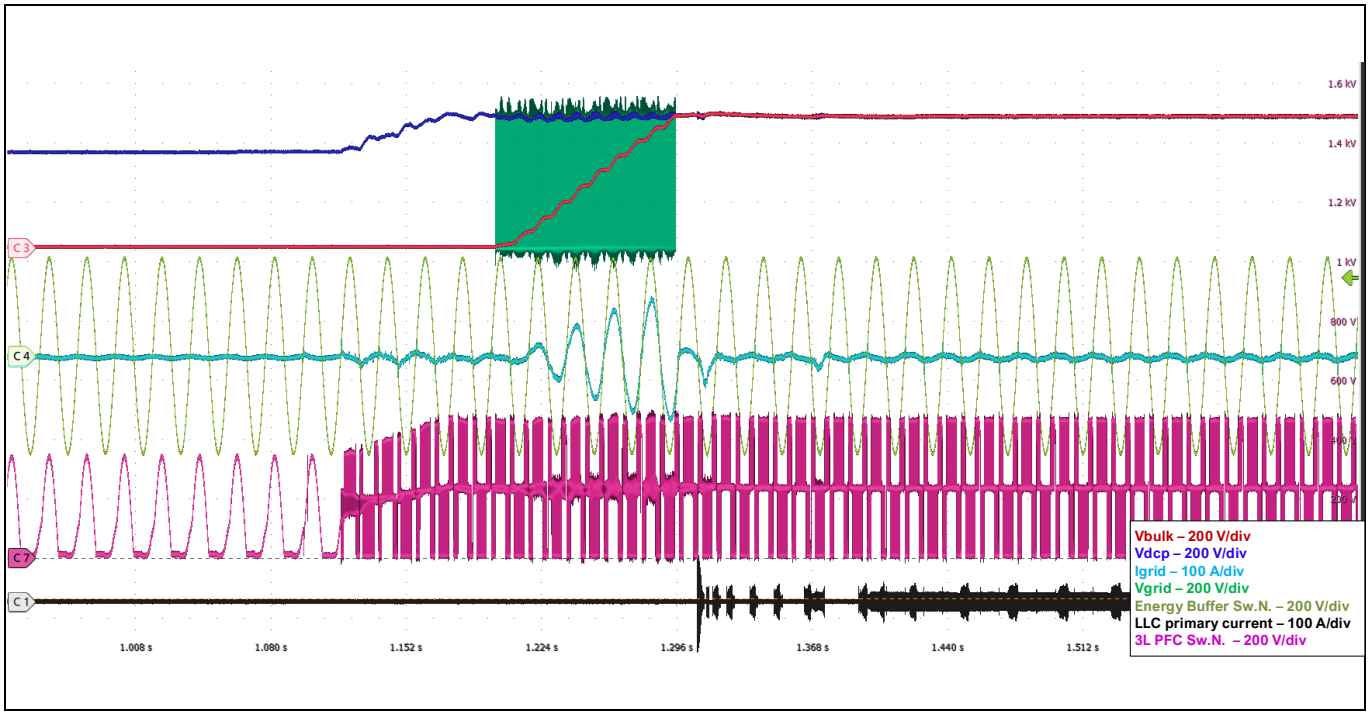


Figure 49 PSU startup at 230 V_{AC} input and no load at the output

It should be noted here that the startup inrush current is maximum when the AC input voltage is at its maximum value, while plugging the PSU to the grid. The maximum inrush current is depicted in Figure 50 for 305 V_{AC}, considering that the PSU starts when the grid is at 90°.

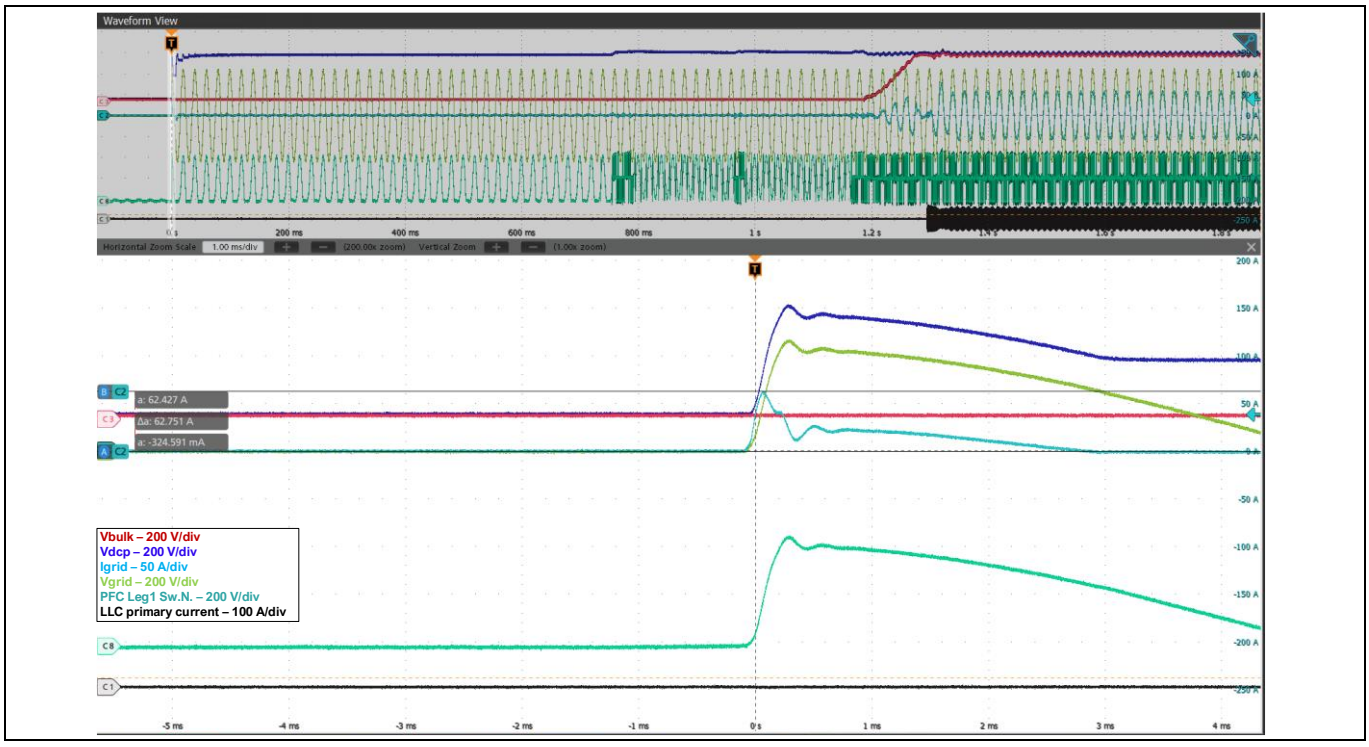


Figure 50 PSU inrush current at 305 V_{AC} input voltage and 90° startup

If we examine the startup behavior of the LLC converter standalone, it is shown that before the closed loop operation is activated, 17 predefined control pulses are given to the primary switches in the open loop to limit

the maximum primary current, since the resonant capacitors and the output capacitors are completely discharged during startup. The maximum frequency during this phase is approximately 1.8 MHz as depicted in Figure 51. After this initial interval, the output voltage of the LLC ramps up using the closed loop control system, which is responsible for the output voltage regulation. For the output voltage regulation, a PID controller is used.

Furthermore, the secondary side microcontroller is also responsible for the pulses generation used for the control of the synchronous rectification switches. The voltage of the secondary side of the transformer along with the primary current are depicted in Figure 52 for the initial startup phase of the LLC converter highlighting four different time stamps during this phase. The control pulses for the synchronous rectification MOSFETs start when the output voltage is approximately 5 V with a small width. The width of the pulses gradually increase as the output voltage rises and the switching frequency of the converter tends to reach the steady state value. The synchronous rectification pulses increase gradually to ensure that there is no step change on the LLC converter gain curve, causing oscillations at the output voltage.

Thus, by gradually changing the pulse duration, a smoother variation of the LLC converter curve can be achieved, also reducing the controller effort. The waveforms of Figure 51 and Figure 52 are for full load operation of the LLC converter.

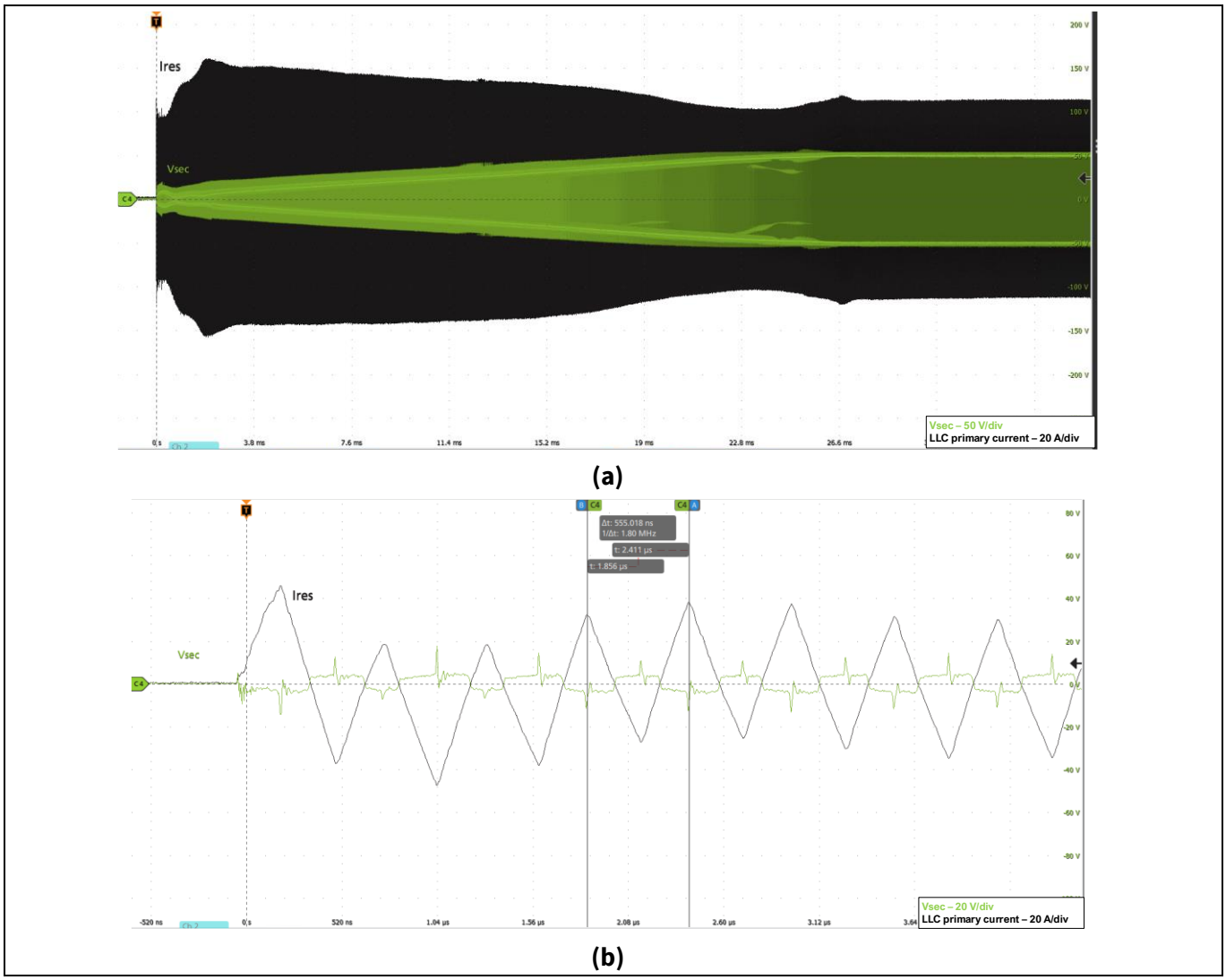


Figure 51 (a) LLC converter startup and (b) zoomed waveforms during the initial startup pulses

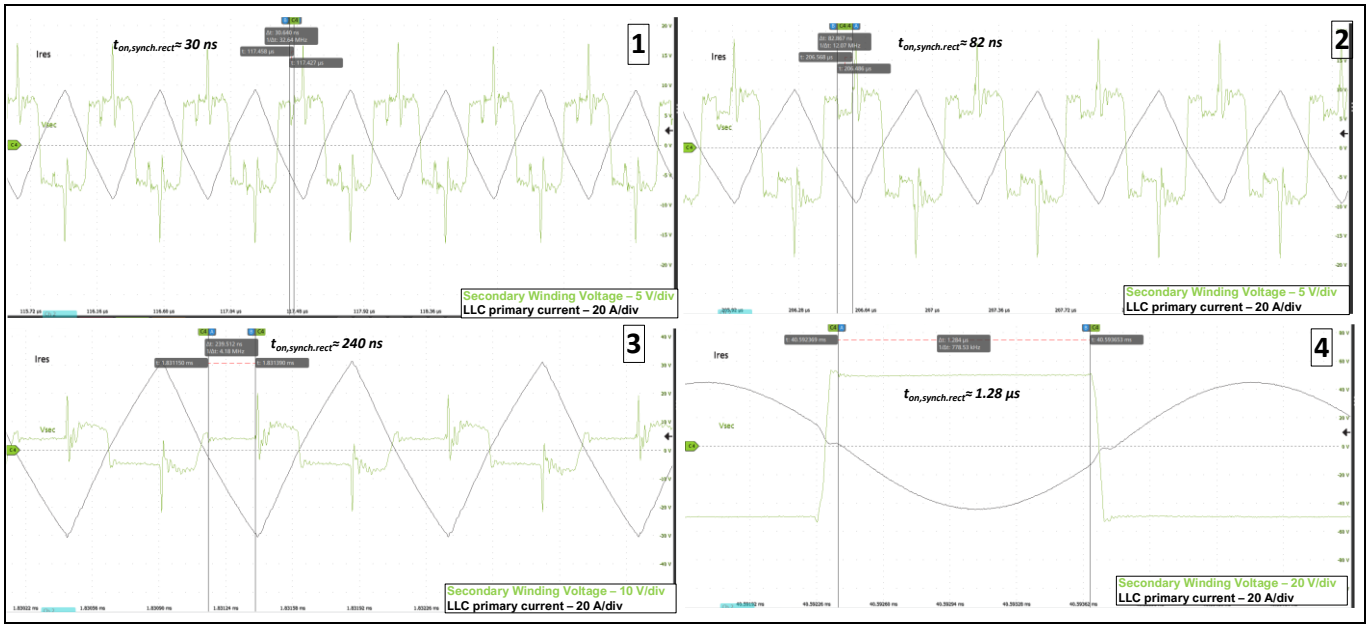


Figure 52 Transformer secondary voltage and LLC primary current for four different phases of the startup of the LLC converter

4.1.4 Steady state waveforms

In Figure 53, Figure 54, and Figure 55 the steady state main waveforms of the PSU are depicted for no load, 50% load, and 100% load conditions respectively for the nominal AC input voltage of 230 V_{AC}.

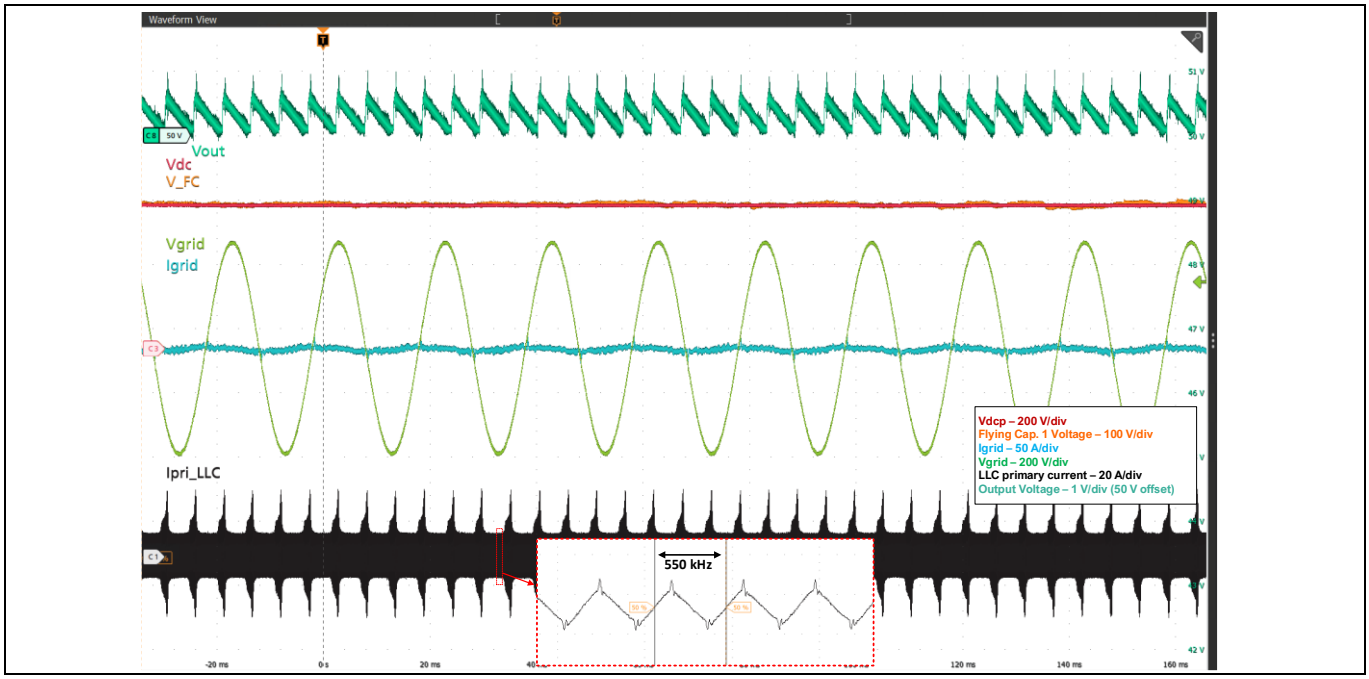


Figure 53 Key-waveforms of the REF_12KW_HFHD PSU for 230 V_{ac} and no load at the output

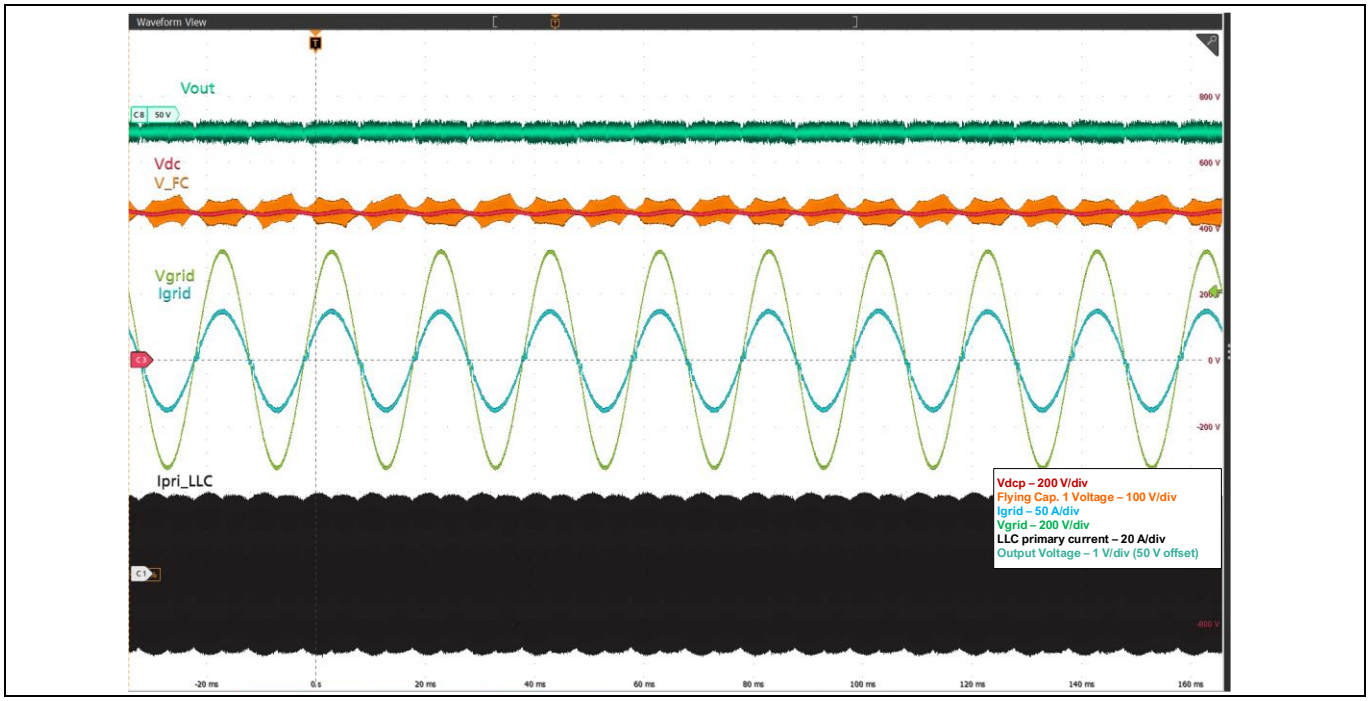


Figure 54 Key-waveforms of the REF_12KW_HFHD PSU for 230 V_{ac} and 50% load at the output

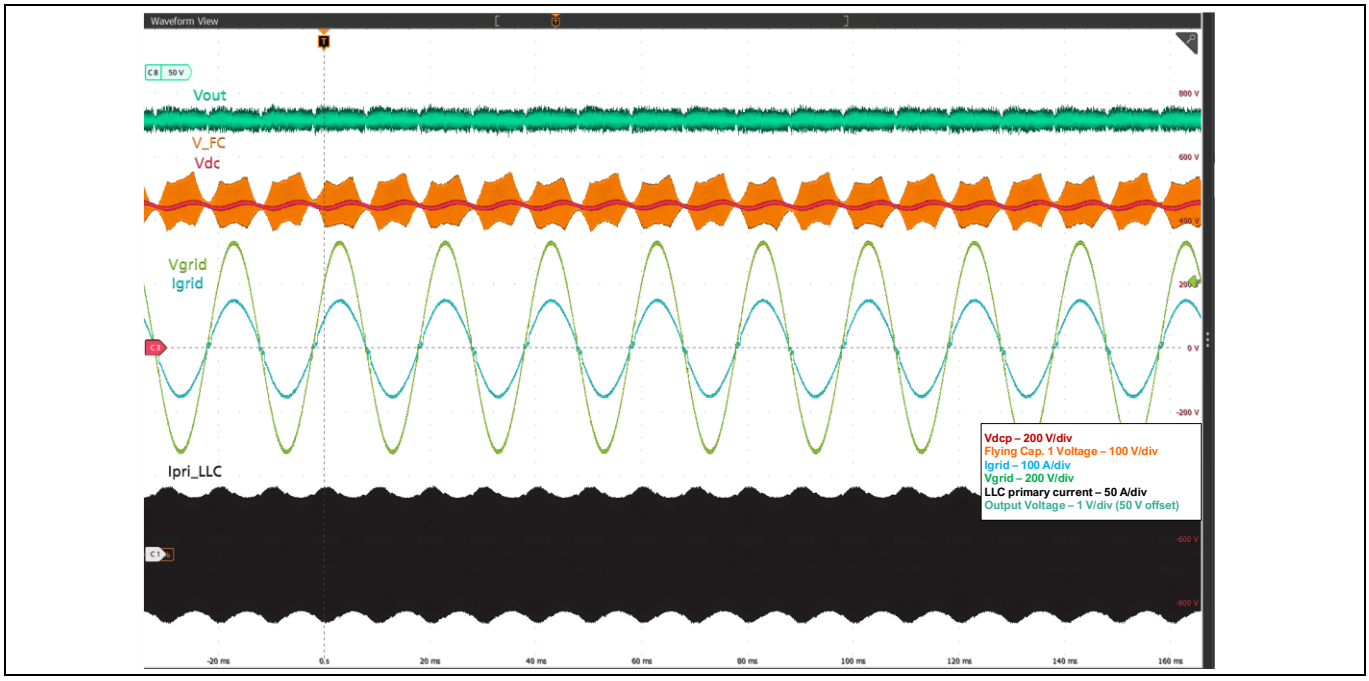


Figure 55 Key-waveforms of the REF_12KW_HFHD PSU for 230 V_{ac} and 100% load at the output.

For operation without load at the output of the PSU, it can be seen from the waveforms that the voltage ripple on the DC link capacitor is negligible, since the amount of power that is processed is minimum and covers only the converter losses. The LLC output voltage reaches 50.7 V and then the operating frequency decreases, also reversing the energy flow, as is shown from the zoomed waveform on the primary LLC current. With this technique, charges are transferred from the output capacitance (the linear decrease of the output voltage is visible) to the DC link through the LLC converter, keeping the operating frequency within predefined limits. The maximum voltage ripple at the output voltage in this case is 700 mV.

For half load and full load conditions, this phenomenon cannot be observed, and the setpoint of the output voltage changes with the output current implementing the droop function. The enveloping curve of the LLC current contains a strong second order harmonic (the line frequency is taken as the fundamental harmonic) in order to compensate for the second order harmonic at the output voltage of the PSU. The second order harmonic component is present on the DC link voltage (V_{dcp}), and thus at the input voltage of the LLC converter, because of the single-phase PFC operation.

The second order harmonic component increases with higher power because the AC component of the power that needs to be decoupled by the capacitor increases as well. Additionally, the flying capacitor voltage ripple is greater with higher power, since the current during the charging and discharging phase is increased. In Figure 56, the steady state waveforms of the PSU are shown for 230 V_{AC} and full load at the output, emphasizing on the low frequency ripple of the intermediate DC link, which is ≈20 V, and the ripple on the flying capacitor which is ≈88 V.

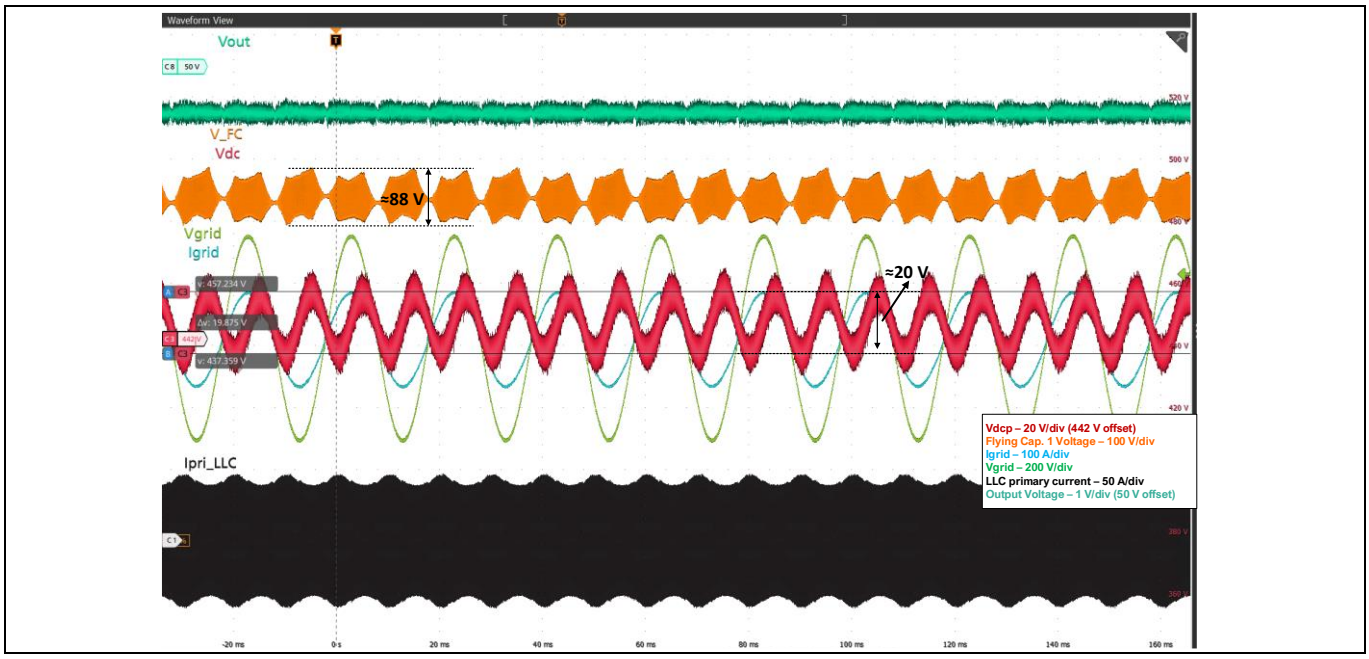


Figure 56 Voltage ripple of the intermediate DC link and flying capacitor of the REF_12KW_HFHD PSU for 230 V_{ac} and 100% load at the output

In Figure 57, the LLC primary current and the switching frequency are shown for full load operation, highlighting the waveforms and the frequency, when the DC link voltage is minimum, maximum, and also when it is equal to the value required for operation on the resonant point. The maximum LLC frequency for steady state operation at full load is 377 kHz, while the minimum frequency is approximately 303 kHz. This frequency range is adequate to compensate for the low frequency component of the DC link voltage as confirmed from Figure 56, since the second order harmonic component cannot be seen on the output voltage of the PSU. For the minimum DC link voltage, the primary current of the LLC converter is maximum, and the converter operates in boost mode, while for maximum DC link voltage the frequency increases, leading to the buck mode operation of the LLC converter. Furthermore, from Figure 57 (c) the resonance frequency can be identified, which for this converter is equal to ≈355 kHz.

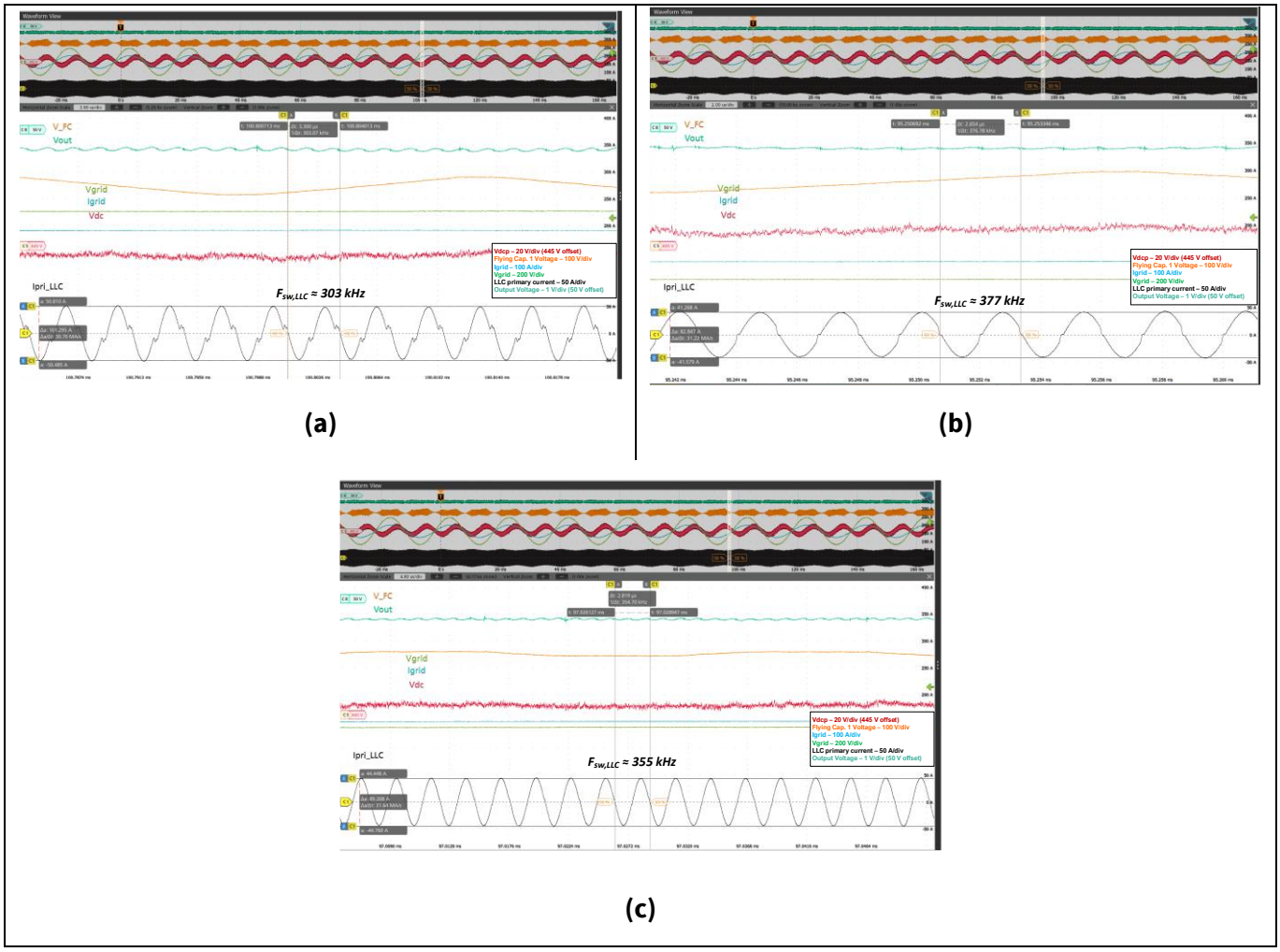


Figure 57 PSU steady state waveforms highlighting the LLC primary current and the switching frequency for (a) minimum V_{dcp}, (b) maximum V_{dcp}, and (c) V_{dcp} equal to the value needed for operation at the resonant point

In Figure 58, the switching node voltages of two high-frequency flying capacitor 3-level legs are shown along with the boosting inductor waveforms, highlighting the multistep waveform of the switching node, and the interleaving effect on the inductor current.

In Figure 59 and Figure 60, the steady state waveforms of the whole PSU are presented for the minimum and maximum AC input voltage respectively, validating the proper operation of REF_12KW_HFHD_PSU for the whole input voltage operating range at 100% load at the output. Additionally, in Figure 61, the ripple of the output voltage is shown for 100% load again, which is measured considering 250 MHz bandwidth and 0.1 µF capacitor locally connected to the probing point on the adapter board.

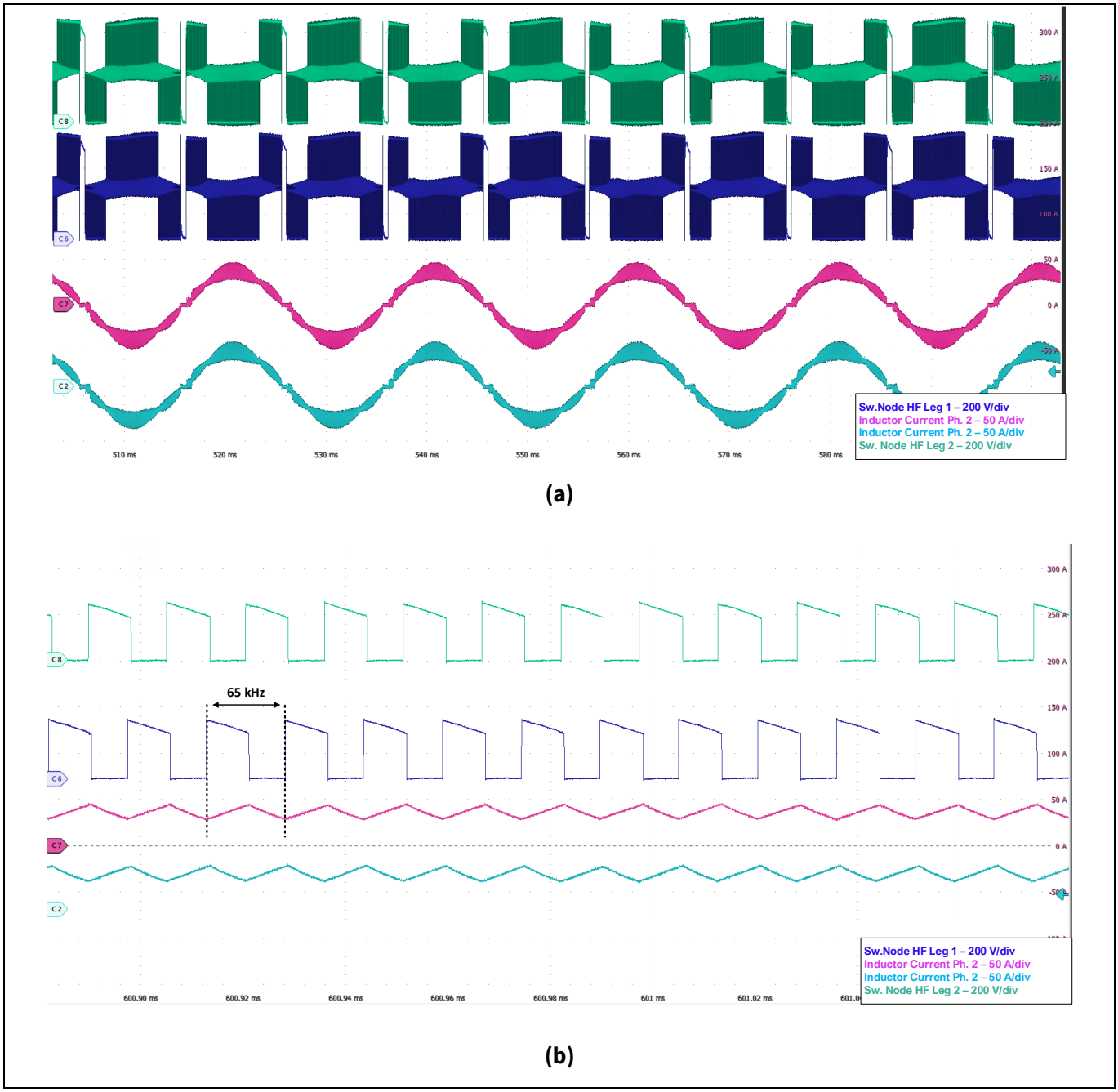


Figure 58 PSU steady state waveforms highlighting the switching node voltages of the two high frequency 3-level legs along with the PFC boosting inductor currents (a) time division equal to 10 ms/div and (b) zoomed waveforms where the phase current is maximum

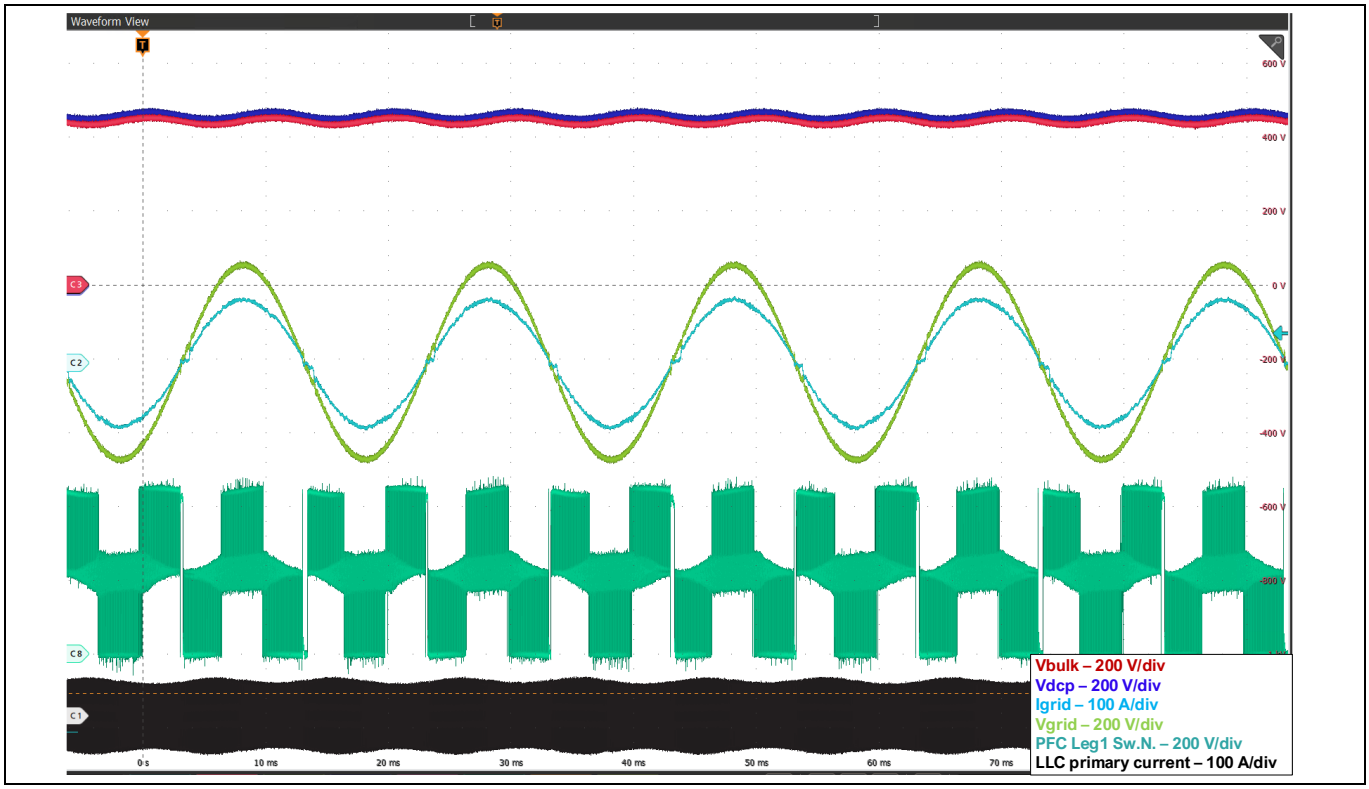


Figure 59 REF_12KW_HFHD_PSU key waveforms for 180 Vac AC input voltage

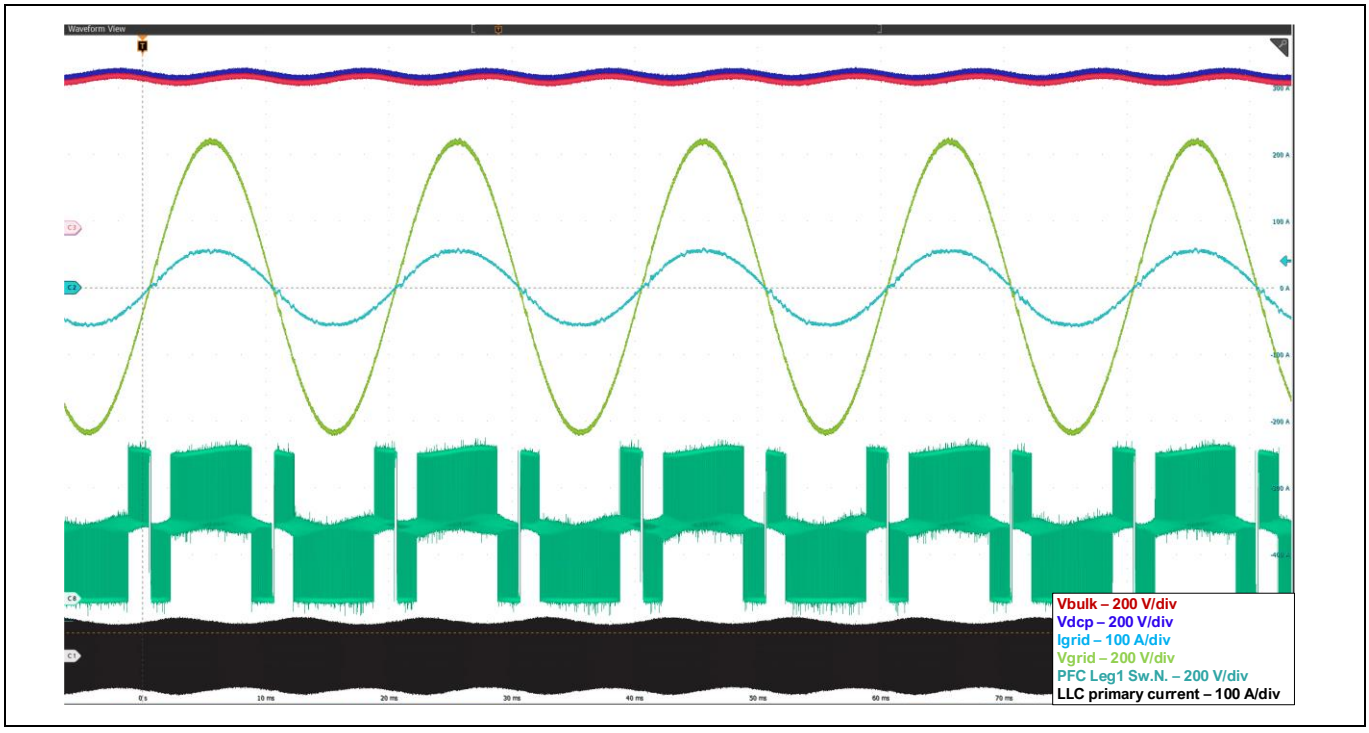


Figure 60 REF_12KW_HFHD_PSU key waveforms for 305 Vac AC input voltage and 100% load at the output

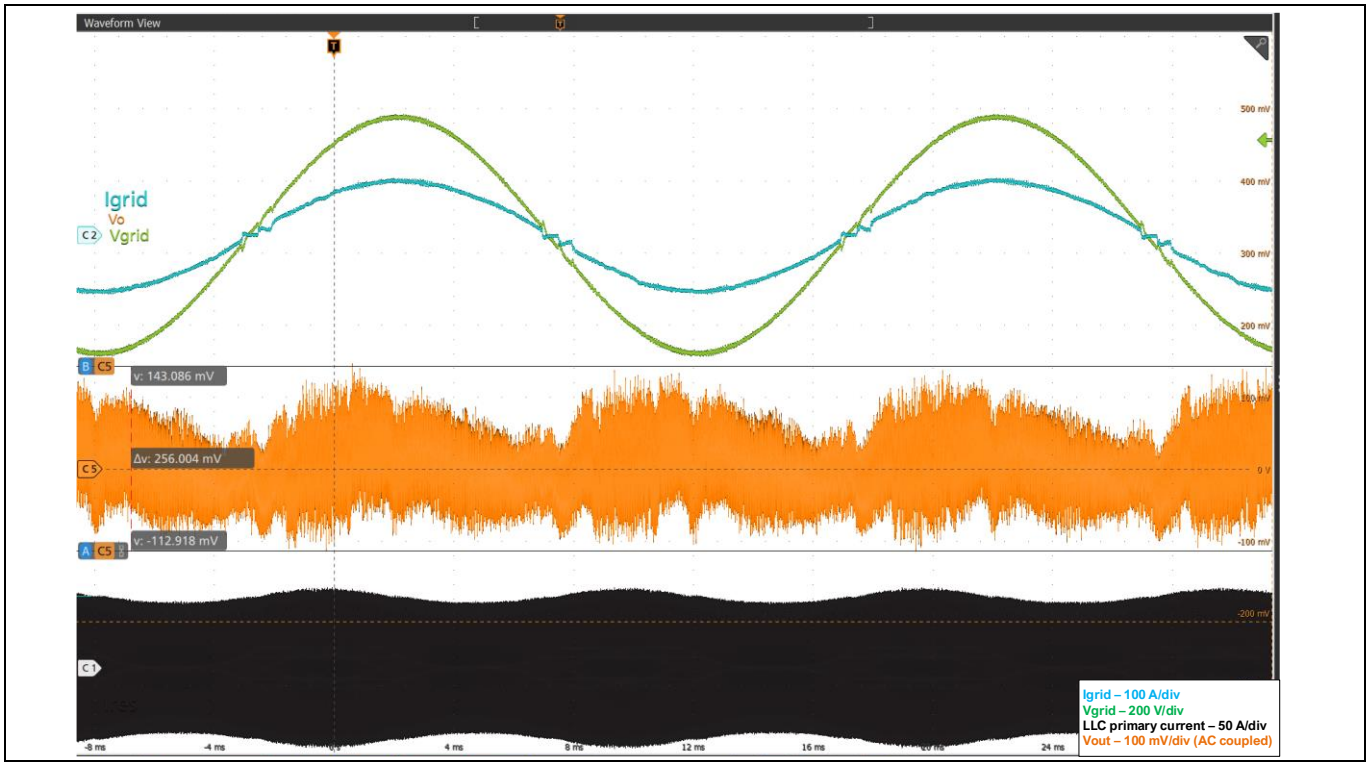


Figure 61 PSU output voltage ripple at 100% load

4.1.5 Thermal performance

Thermal performance of the full PSU has been simulated and verified under several PSU operating conditions. In Figure 62, the results of thermal simulations are shown, depicting the velocity magnitude (m/s) considering a cross section in the center of the PSU.

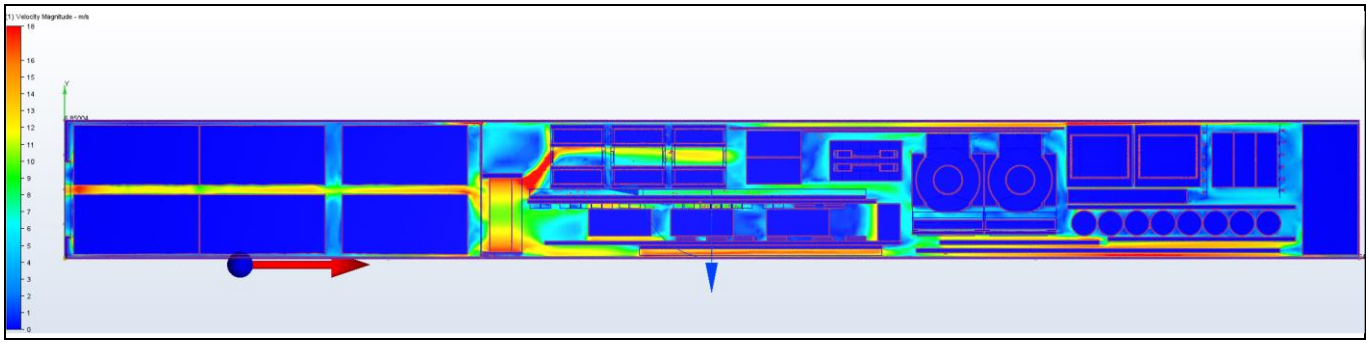


Figure 62 Airflow velocity magnitude – cross section at PSU center

The thermal performance of the PSU is also experimentally verified at different AC input voltages and the results regarding the temperature on the most critical components are summarized in Table 1. All the temperature values shown in Table 1 are recorded at the thermal equilibrium point, the ambient temperature is 25°C, and maximum load is considered in every case.

Table 1 PSU thermal measurements at different input voltages and 25 ° C ambient temperature

V_{AC} (V)	Common mode choke T (°C)	LLC primary MOSFET T (°C)	Synch. Rect. PFC T (°C)	PFC choke T (°C)	Resonant Inductor Lr T (°C)	Synch. Rect. XFMRA T (°C)	Synch. Rect. XFMRA T (°C)	Output capacitor T (°C)
180 V	129	87	88	78	89	86	100	87
208 V	120	91	80	72	92	84	99	85
230 V	108	89	72	66	90	82	97	83
277 V	91	84	61	55	86	77	92	78
305 V	82	81	54	48	83	72	87	74

4.2 Dynamic performance experimental waveforms

4.2.1 Output load transients

REF_12KW_HFHD_PSU has been tested for repetitive load transients, from 10-100% and vice versa, with a 5 A/µs slew rate for the load current during the load jumps, and a 10 Hz repetition rate as shown in Figure 63. A more detailed view during the change of the load current is depicted in Figure 64. As can be seen, the undershoot of the output voltage is zero since the new setpoint command (because of the droop function) is lower than the expected undershoot. When the load is released, the output current drops immediately and the droop function commands the rise of the output voltage. In this case the overshoot is 120 mV, which is well below the imposed limit from [1].

It should be noted that every time that the load increases the static switch is off and the energy buffer starts to operate as can be seen from the buck-boost inductor current. In this case, some energy is taken from the bulk capacitor in order to limit the power drawn from the grid so as to implement the grid shaping function, with which the slope of the power drawn from the grid can be limited. Nevertheless, in this case, the PFC current drops immediately to maintain the V_{dcp} regulation.

The instant decrement of the PFC current is possible because of the LLC current feedforward term which is fed as information to the control loop of the PFC converter. Additionally, the PFC current also decreases immediately when the DC link voltage is above a predefined threshold as a protection limit without latching the fault condition operating in a mode similar to pulse skipping. More details about the energy buffer operation are given in [10].

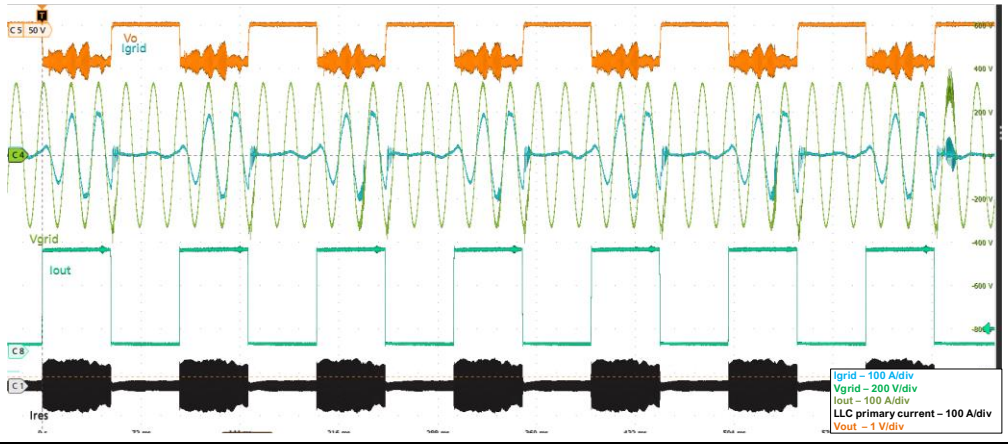


Figure 63 PSU repetitive load transient, 10-100%, and 100-10% output load with 10 Hz repetition frequency

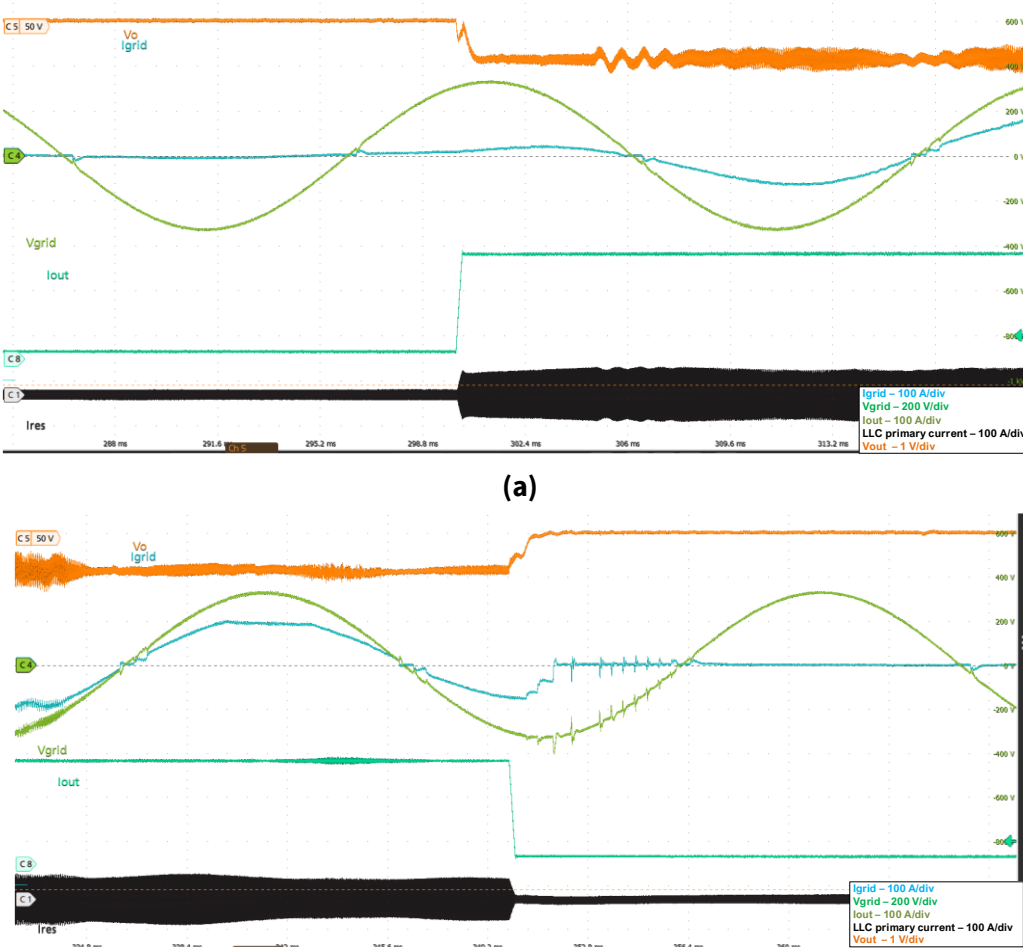


Figure 64 Detailed view of the PSU load transient at (a) 10-100% load current and (b) 100-10% load current

This 10 Hz repetitive load jump can also be continuous, due to the load profile of the data centers. Therefore, it should be ensured that devices do not overheat when the energy buffer operates continuously during this repetitive dynamic condition. Figure 66 depicts the thermal image of the energy buffer devices considering

continuous 10% to 100% load jumps with 10 Hz repetition. The maximum temperature recorded on the device case is 64°C with an open chassis and airflow on top of the daughterboard. The switching frequency of the energy buffer devices is 97.5 kHz.

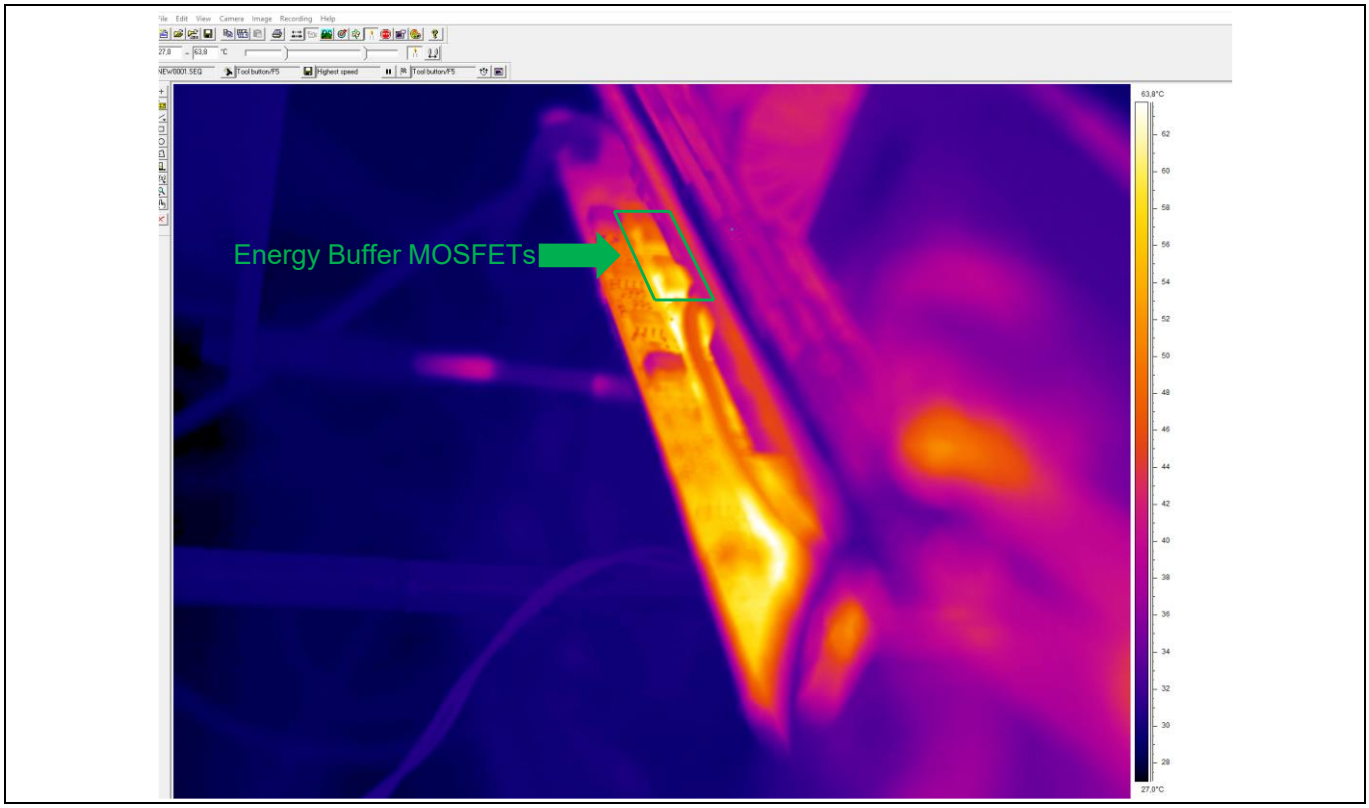


Figure 65 Thermal image of the energy buffer devices during the continuous 10 Hz load jumps from 10% to 100% load

Additionally, proper operation of the PSU is ensured when the load jumps from 0% to 100% (and 100% to no load condition) with 5 A/µs slope as shown in the experimental waveforms of Figure 66.

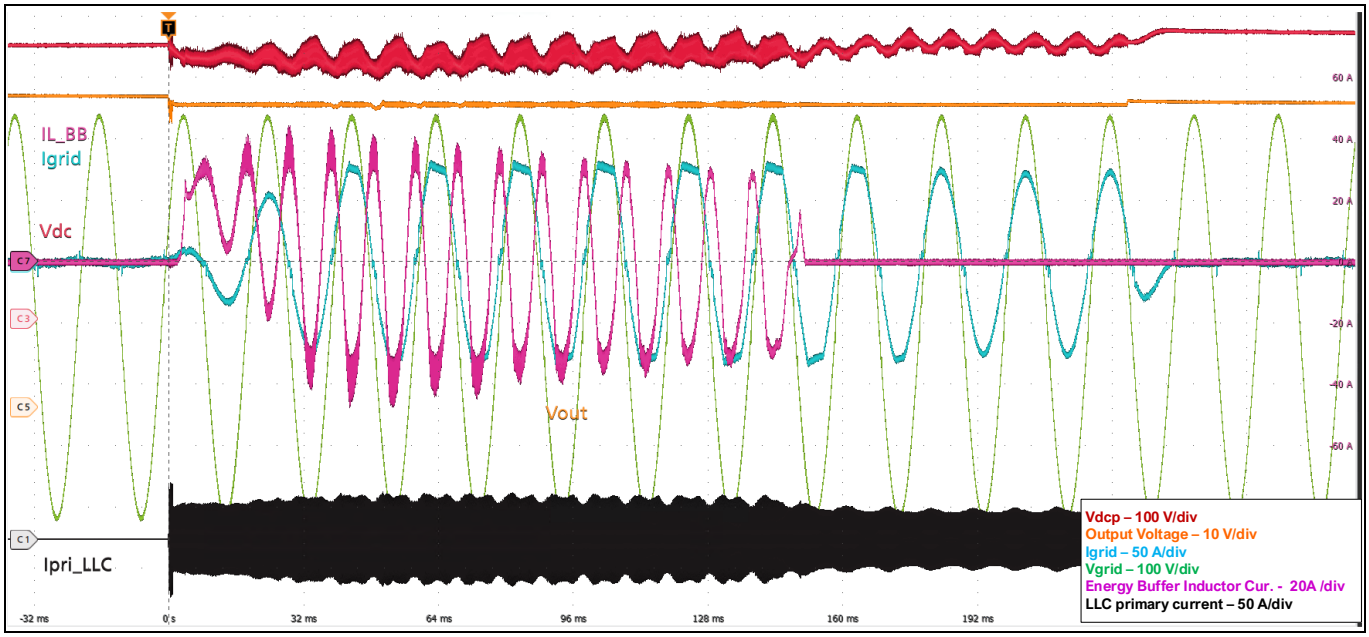


Figure 66 PSU load transient from 0% to 100% and 100% to 0% of the output load

Furthermore, the PSU overloading conditions are tested considering a load jump from 10% to 140% (24 A to 350 A at the output). The 140% load current was sustained at the output for 50 ms and then the load decreased to 24 A, and the experimental results presented in Figure 67 denote the correct behavior of the overall PSU in this overloading dynamic condition.

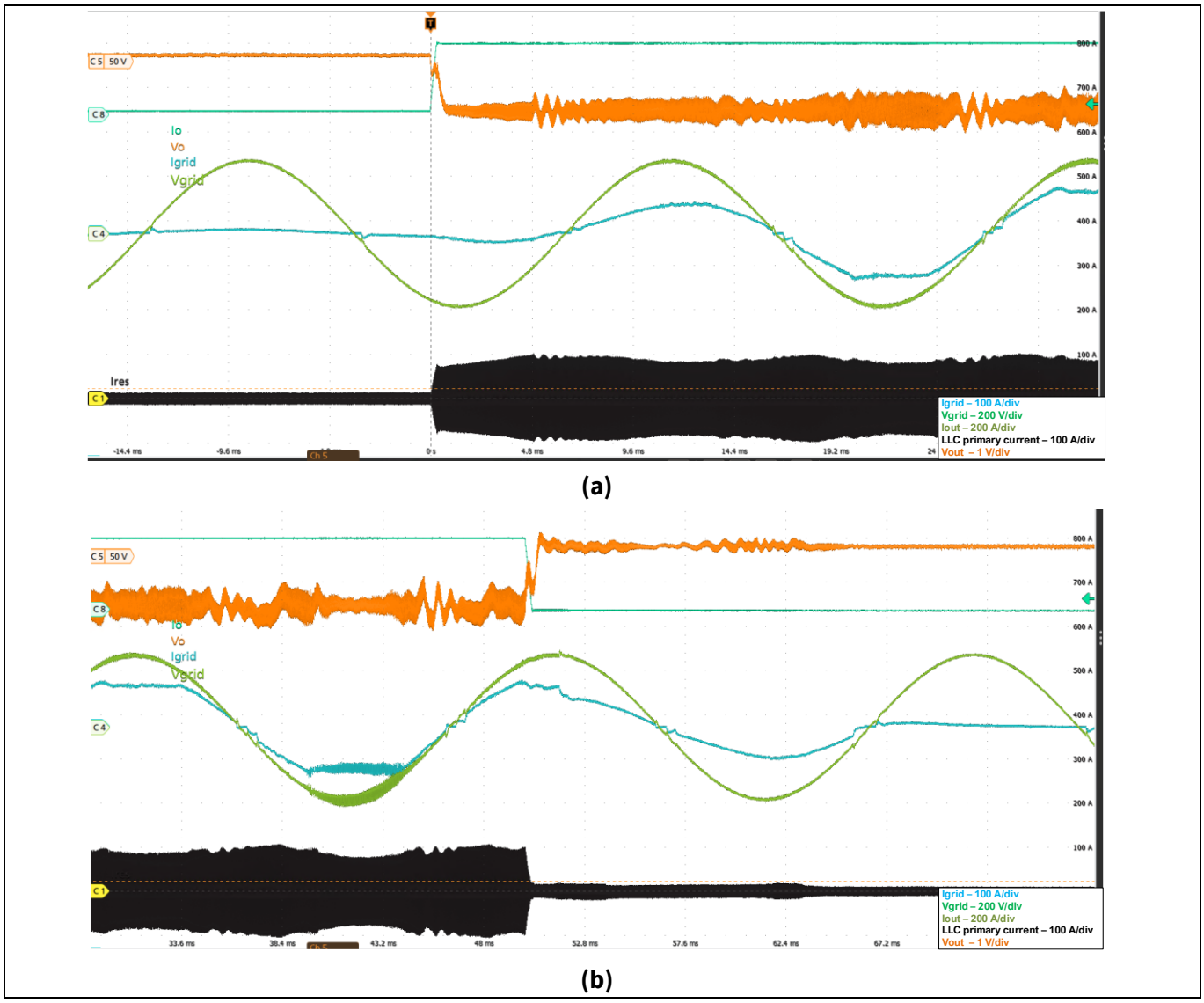


Figure 67 PSU load transient from (a) 10% to 140% and (b) 140% to 10% of the output load

4.2.2 AC input voltage sag

Another dynamic condition that is tested is a grid disturbance condition, called voltage sag. For this condition, the PSU should operate normally and ride through, when the AC input voltage drops from the nominal voltage of 230 V RMS down to 160 V RMS for 500 ms. In Figure 68, the key-waveforms of the converter are depicted for this dynamic condition, considering full load at the output of the converter. In Figure 69 (a) and Figure 68 (b) the same waveforms are zoomed in to the section where the input voltage drops from 230 V_{ac} to 160 V_{ac} and when the AC input voltage recovers.

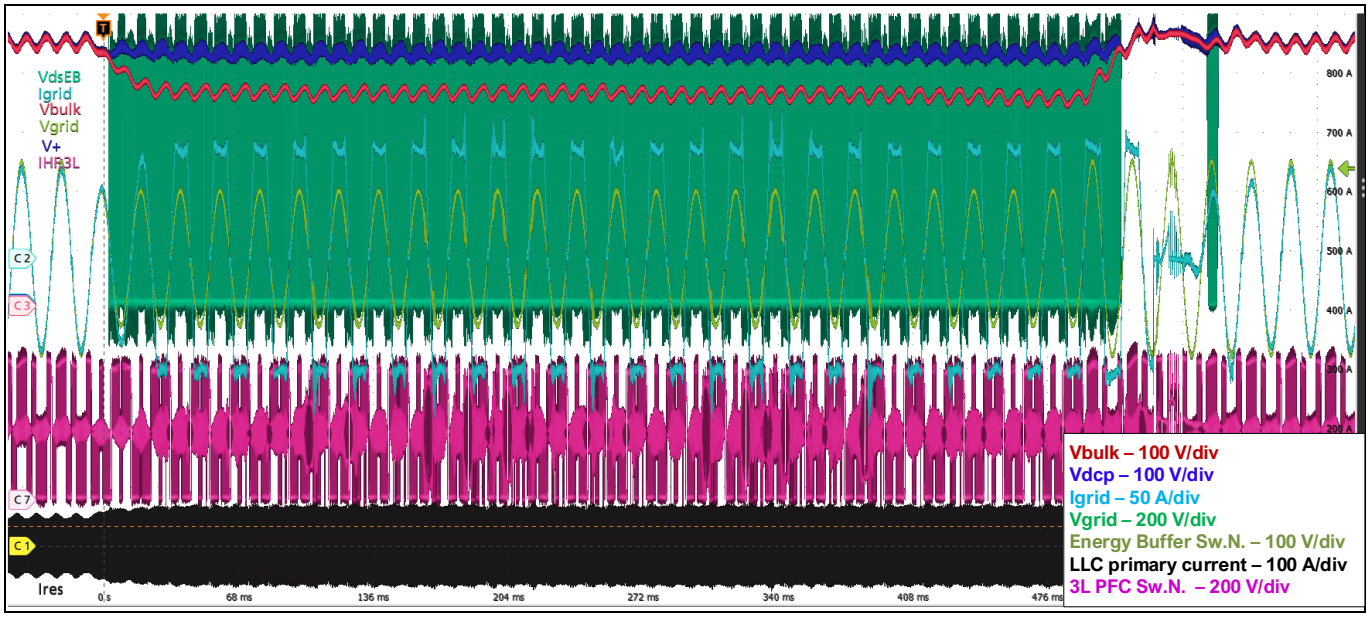
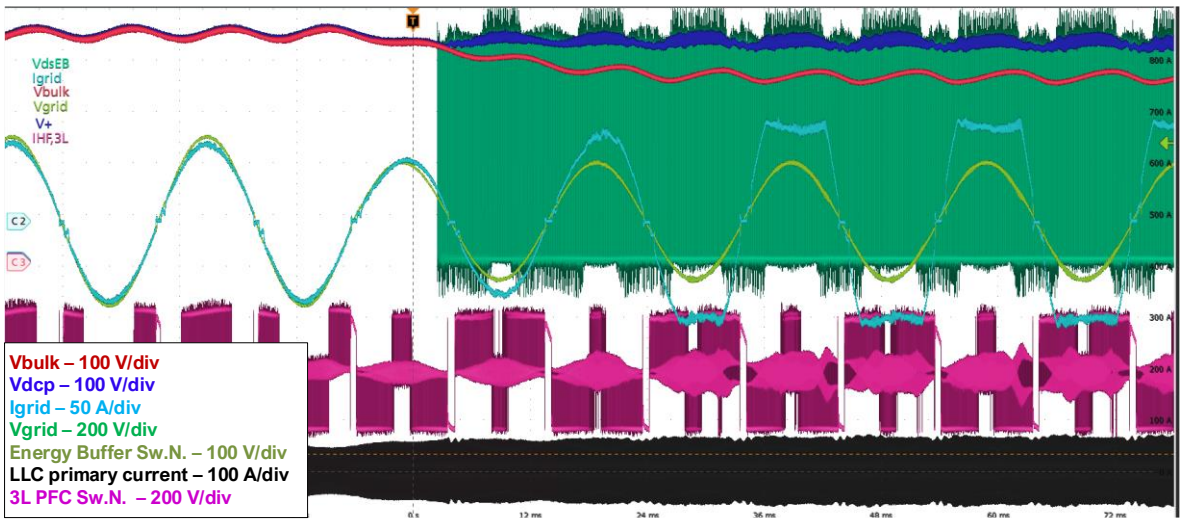
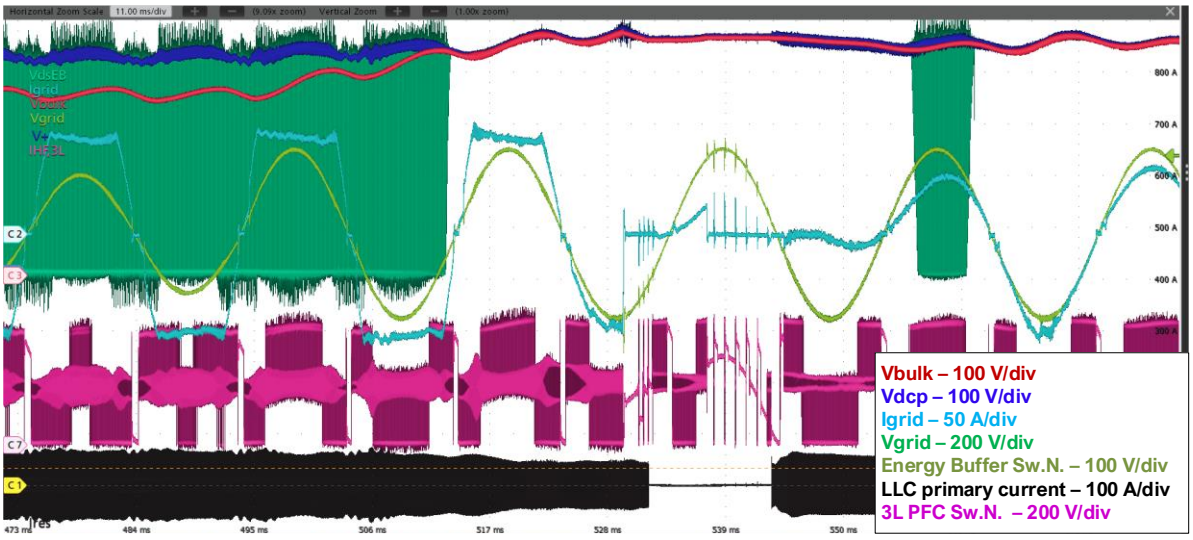


Figure 68 AC input voltage sag for 230 V_{ac} down to 160 V_{ac} considering full load at the output



(a)



(b)

Figure 69 Zoomed waveforms for the AC input voltage sag event (230 V_{AC} to 160 V_{AC}) (a) when the AC input voltage drops and (b) when it is increased again to the nominal value

It should be noted here that due to space limitations, the capacitance of the flying capacitor is limited for this design, leading to an increased voltage ripple during the input voltage sag dynamic condition. For this reason, 650 V devices are used in this design, but if the form factor requirements are relaxed, the capacitance of the flying capacitor can be increased leading to a lower voltage ripple. This allows the potential selection of the Gen2 400 V from Infineon for the switches of the flying capacitor topology.

4.2.3 Hold-up time and line cycle drop-out (LCDO) event

According to specifications presented in [1], the power supply unit should be able to maintain the output voltage value for 20 ms, and this case is defined as the hold-up time requirement. Furthermore, if this specification is covered, the PSU can ride through a dynamic condition, which is called line cycle drop-out (LCDO). This dynamic condition should also be handled according to [1], and this condition refers to the case when the ac input voltage is lost for 20 ms and then recovers. In order to achieve this requirement, the energy storage (DC link electrolytic capacitance) inside the PSU should be increased. Nevertheless, the capacitance should be increased to a very high value since the regulation range of the LLC converter is narrow traditionally.

If high efficiency is the target, deep discharge of the electrolytic capacitors is not feasible, because of the limited regulation range. For this reason, the energy buffer can be used again, making the deep discharge of the electrolytic bulk capacitance feasible while keeping the V_{dcp} voltage (input voltage of the LLC converter) regulated, close to the steady state value. Since the energy buffer allows for this deep discharge, the overall capacitance requirements are mitigated, leading to increased power density.

In Figure 70 the hold-up time extension capability is tested considering full load at the output, when the grid is lost for more than 20 ms verifying the proper behavior of the converter, showcasing the converter's key waveforms. As it depicted the V_{dcp} voltage is maintained close to the steady state value, and the energy buffer discharges the bulk capacitance, while the output voltage is kept constant for more than 20 ms.

Since the hold-up time extension function is verified, in Figure 71 the LCDO dynamic condition is depicted at 100% load. During this event, the energy buffer operates again, discharging the bulk capacitance to keep the DC link voltage regulated. After the grid voltage is restored, the energy buffer continues its operation, transferring energy from the DC link to the bulk capacitance to restore the lost charge, keeping the DC link voltage regulated at the same time. It is noted that the test is performed such that the AC voltage is lost at 45° of the grid, where the DC link voltage is minimum, as a worst-case scenario. More details about the energy buffer behavior and the control scheme used can be found in [10].

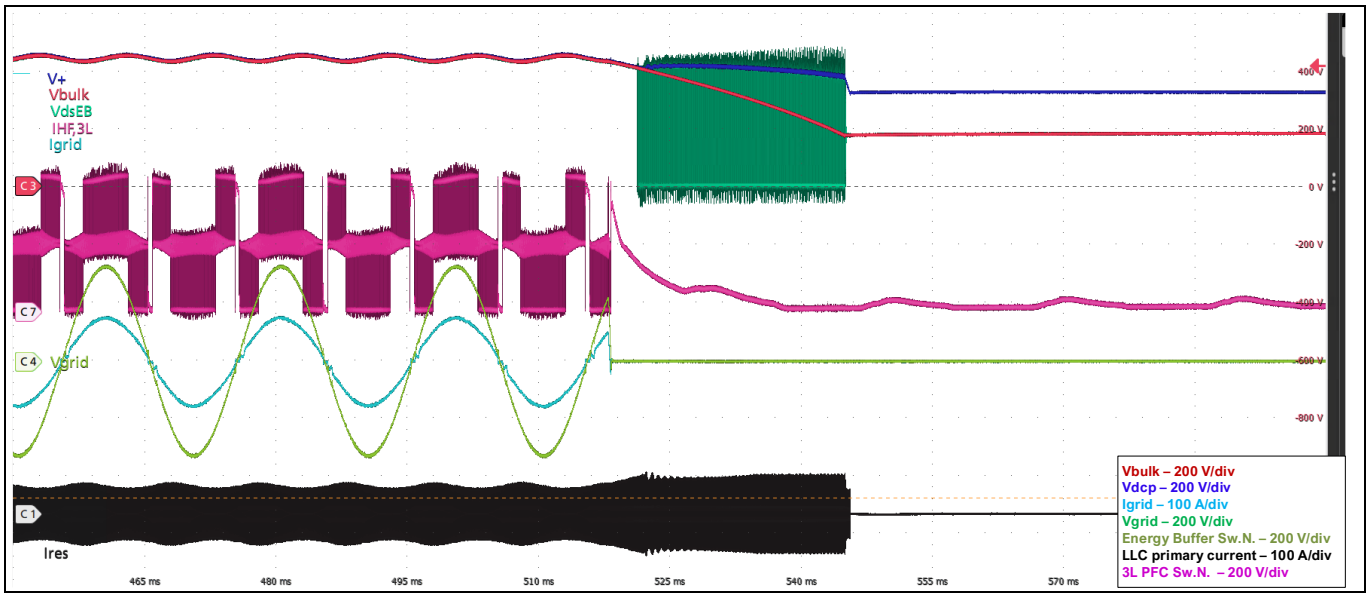


Figure 70 Hold-up time at 100% of the rated load with LCDO duration >20 ms

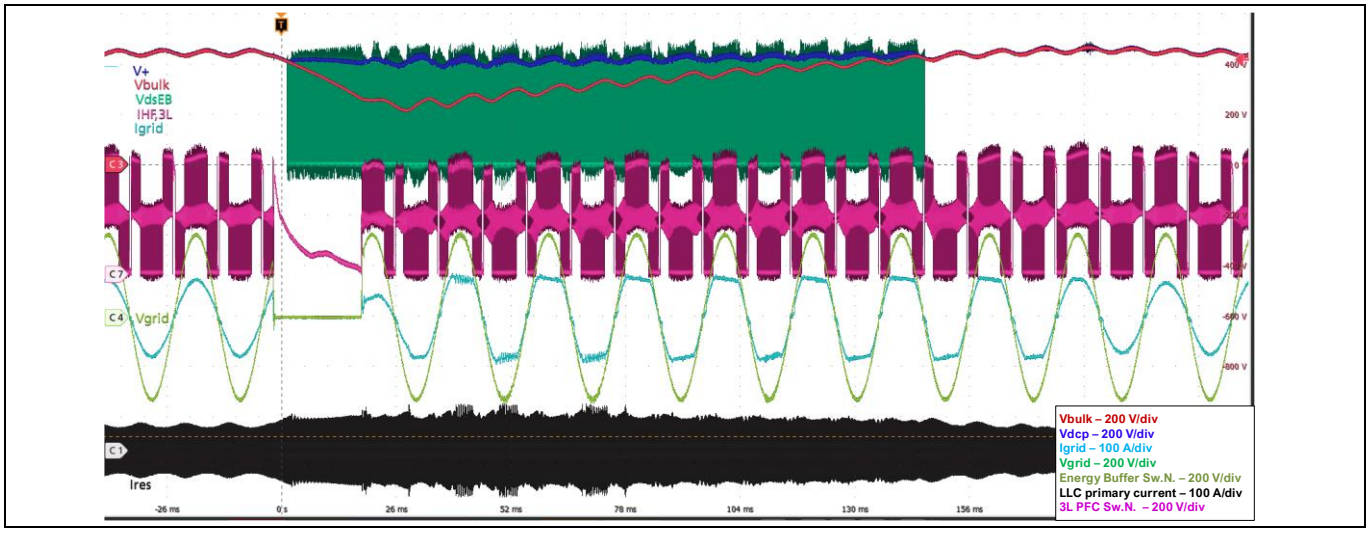


Figure 71 Hold-up time at 100% of the rated load with LCDO duration ≤20 ms

4.3 Surge tests

Preliminary surge tests have been executed on REF_12KW_HFHD_PSU to address concerns related to having the DC-link electrolytic capacitors not directly connected to the bulk voltage V_{bulk}, rather through the energy buffer inductor L_{EB}. This condition does not happen during steady state operation, when the energy buffer static switch is closed and the bulk capacitor bank is connected to the DC-link, but it can occur when transients occur and during the LCDO event when the energy buffer is operational and the static switch is open.

The unit has to comply with IEC61000-4-5 standard Level 4 [1]. The use of differential and common-mode MOVs and GDT along with the EMI filter alone are not sufficient for keeping the V_{bulk} voltage within the absolute maximum blocking voltage of the semiconductors when the energy buffer static switch is open. Therefore, an additional surge circuit has been added to the unit, consisting of a 240 µF electrolytic capacitor in series with an inrush control circuit (bypass switch in parallel to an NTC). During steady-state operation, transients, and LCDO, the electrolytic capacitor is directly connected to the DC-link, being able to absorb the extra energy of the surge pulse also when the bulk capacitance is disconnected.

Figure 72 highlights the components of the unit acting as protection circuit during the surge event. The components MOV1, MOV2, GDT, and EMI filter suppress the common mode L>PE and N>PE surge event, while MOV3, EMI filter, and the line-to-line surge protection circuit suppress differential mode surge events. In Figure 73 the setup for the proof of concept is shown. The setup shown has been used to prove circuit functionality, however it is not IEC certified.

Setup equipment: TESEQ NSG-3040 surge generator, Chroma 6530 AC source, and Tektronix TDS-3045C floating oscilloscope. Rogowski coils are used for current measurements. The surge generator NSG-3040 is coupled with the Chroma AC source. CWG of 1.2/50 µs with a series resistor of 2 Ω is applied by the surge generator. Only differential mode surge is considered in this application note.

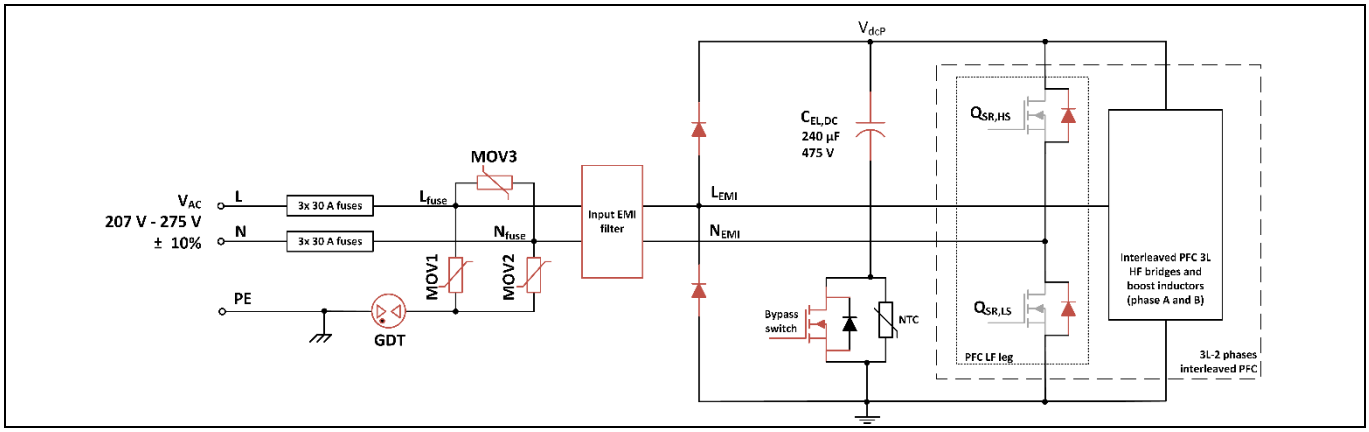


Figure 72 Circuit diagram of the surge protection circuit. Surge protecting devices are highlighted red

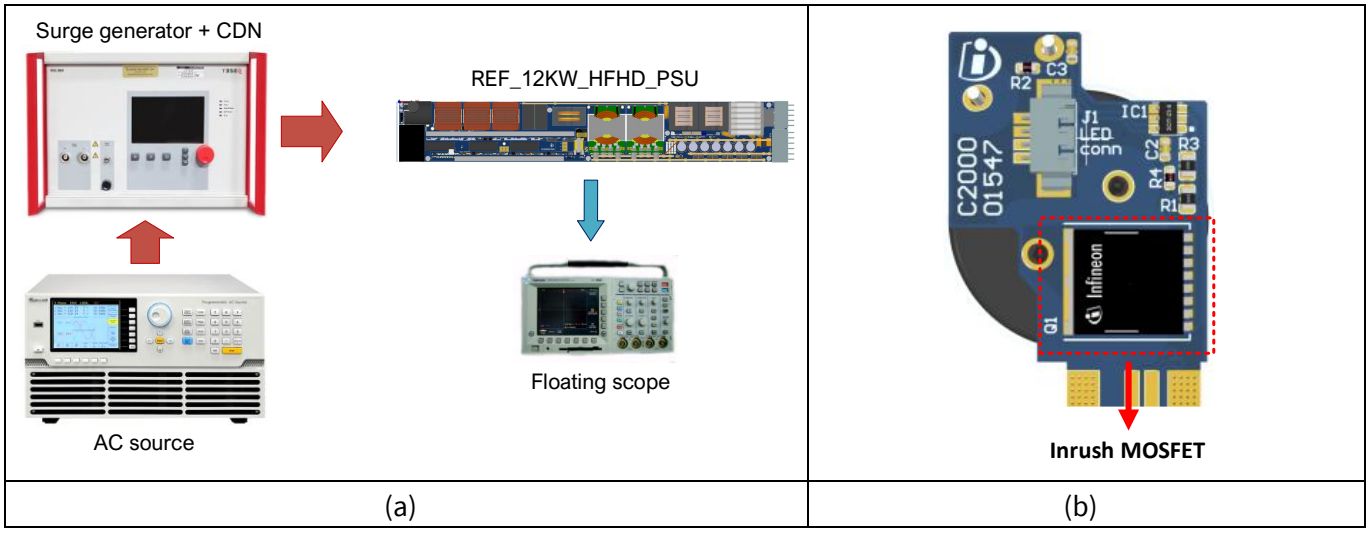


Figure 73 Surge test setup (a) and line-to-line surge protection circuit implementation (b)

Table 2 reports a summary of the different test levels as per the IEC61000-4-5 standard.

Table 2 Open circuit surge test voltage according to IEC61000-4-5

Level	Open-circuit test voltage [kV]	
	Line-to-line (L>N and N>L)	Line-to-ground (L>PE and N>PE)
1	–	0.5 kV
2	0.5 kV	1 kV
3	1 kV	2 kV
4	2 kV	4 kV

The transient surge protection circuit operation has been tested in worst case conditions, meaning no power absorbed from the LLC converter (maximum overvoltage of the DC-link due to surge energy), maximum input AC voltage of 305 Vac to have the highest operating DC-link bulk voltage, and 2 kV line-to-line surge pulse applied at the 90 degree phase of the grid voltage waveform with series resistor of 2 Ω. Figure 74 shows the input waveforms obtained during the performed surge test with setup and conditions as described before.

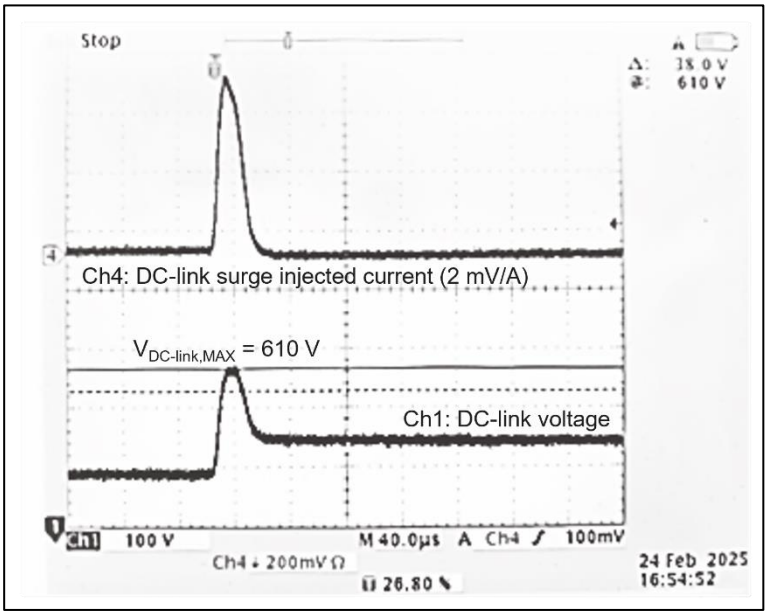


Figure 74 2 kV differential surge test line-to-line (same results for L>N and N>L)

4.4 EMI measurements

The conducted EMI of the full PSU was measured with the setup shown in Figure 75. The setup is not certified according to EN 55032. However, the results are valid for a preliminary assessment of the EMI compliance of the unit.

The load used for the test is a passive resistive load. The equipment used is LISN Schwarzbeck NNLK 8129-2 HV, AC source ITECH IT900P, Spectrum analyzer Rigol RSA 3030N, and DC load Chroma CHR63215E-600-1050. Spectra have been measured with 9 kHz resolution bandwidth from 150 kHz to 30 MHz as per EN 55032.

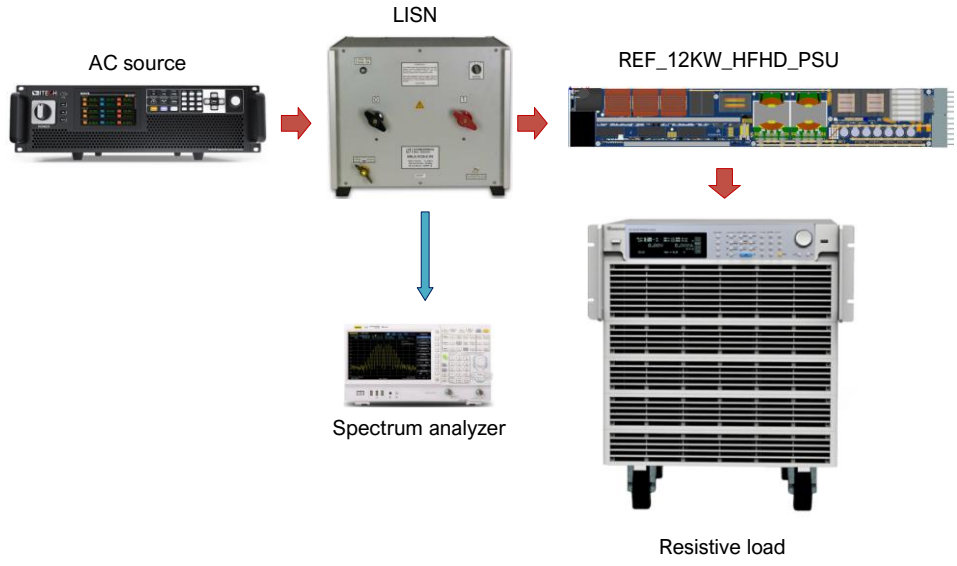


Figure 75 Setup used for EMI test

With the setup discussed, noise floor has been observed even with the DUT connected but not powered. The measured noise floor has been then measured and reported in Figure 76. It is important to notice that the ≥40 dBµV noise floor at frequencies above 8 MHz is related to the setup itself and not on the DUT. Therefore, the

noise measured in Figure 77 in this frequency range has been considered as unrelated to the DUT, but rather to be on the setup.

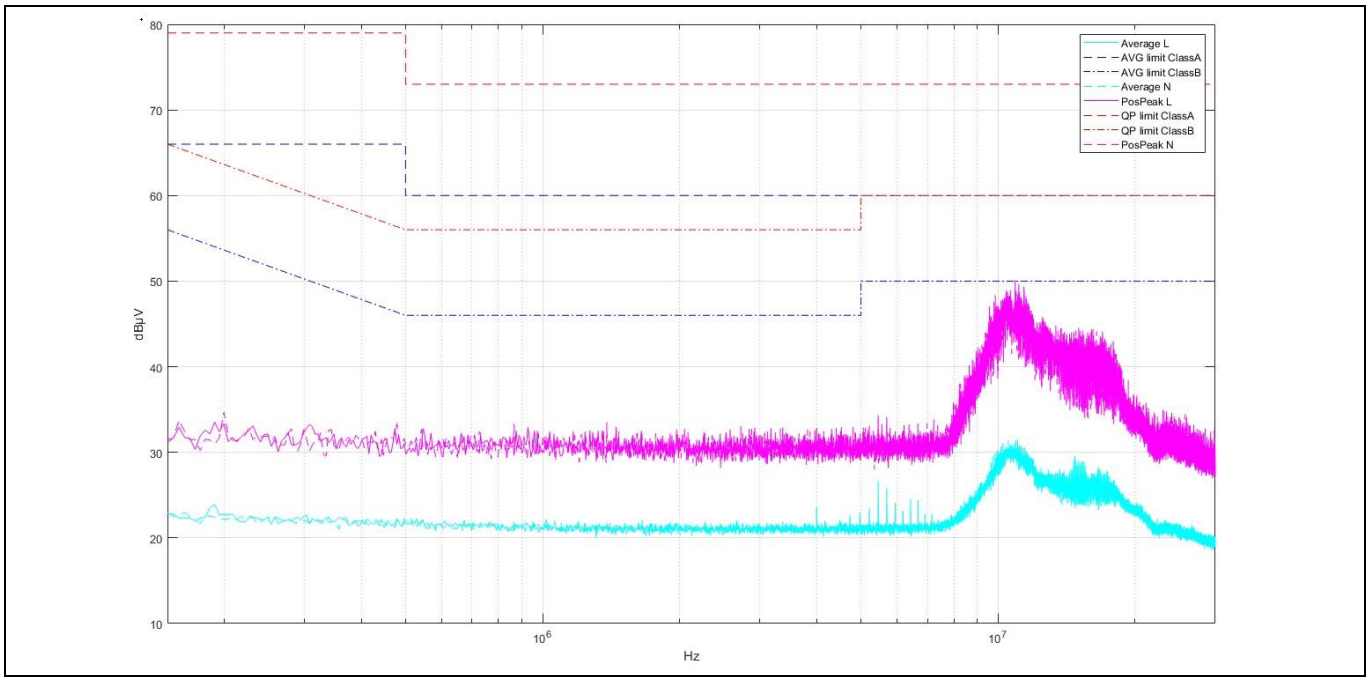


Figure 76 Noise floor in EMI setup measured with DUT connected and off using EN 55032 limits

The EMI tests were performed for both line and neutral inputs, with 230 V_{AC} and 12 kW output power. In order to practically evaluate the effect of the different materials and configurations for the EMI chokes and filter respectively, three different configurations were tested. For the first test, R5KZ material is used for both common mode chokes which offers higher permeability on the higher frequency range. Figure 77 shows the results of the average (AVG) and the positive-peak measurements at 230 V_{AC} with R5KZ. It is shown that the operating frequency range of the LLC converter can be attenuated sufficiently, but the sideband harmonics close to the effective frequency of 130 kHZ (because of the interleaved 3L PFC operation) is slightly above the imposed Class A limit.

The second configuration is tested with R10KZ material on both common mode chokes. With this configuration, it is shown that the lower harmonics can be more attenuated, compared to the configuration of the two R5KZ materials. Additionally, the LLC operating frequency range is less attenuated, and the amplitude of the spectrum is closer to the Class A limits for this frequency range. The experimental results for this configuration are presented in Figure 78.

Finally, the combination of both material is evaluated, since according to the preliminary simulation results it offers good attenuation at the lower frequency spectrum and adequate attenuation on the higher frequency spectrum, as it is also highlighted from the experimental results of Figure 79. For this configuration, which is the final selected configuration for this reference design, the choke with the R10KZ material is populated on the converter side while the choke with the R5KZ material is populated on the grid side.

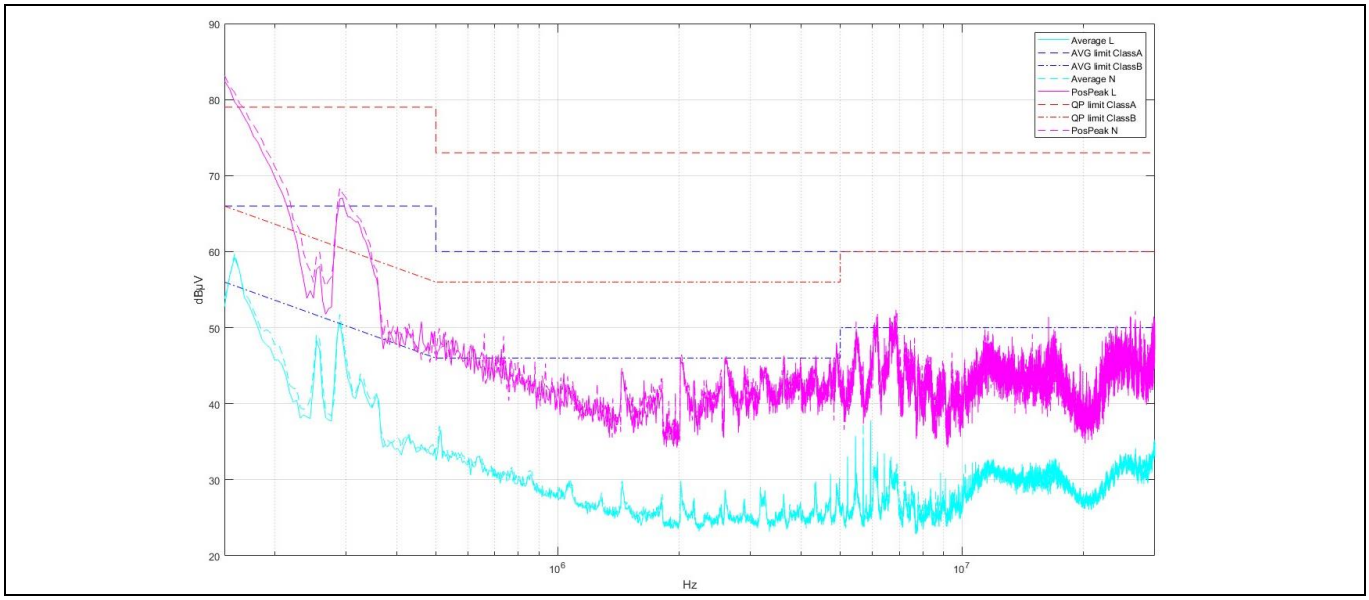


Figure 77 EMI measurements of the DUT at 230 V_{AC} – 12 kW with EN 55032 limits using R5KZ material for both common mode chokes

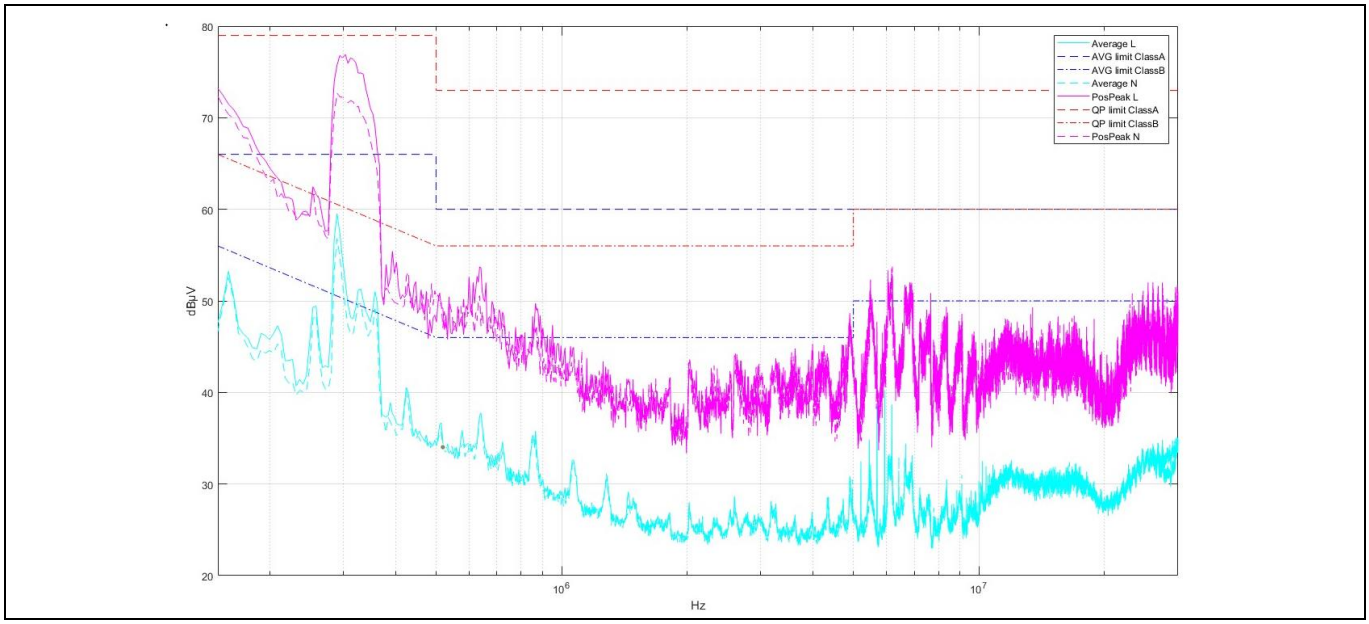


Figure 78 EMI measurements of the DUT at 230 V_{AC} – 12 kW with EN 55032 limits using R10KZ material for both common mode chokes

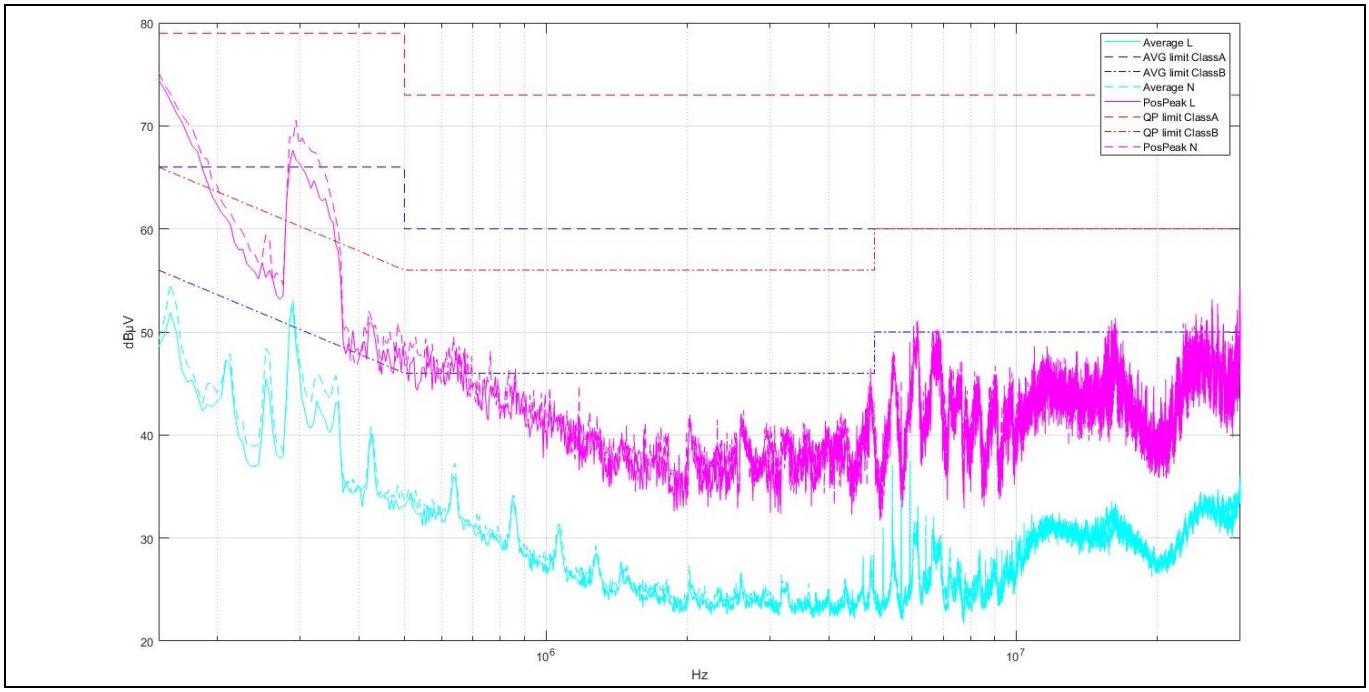


Figure 79 EMI measurements of the DUT at 230 V_{AC} – 12 kW with EN 55032 limits using R5KZ (grid side) and R10KZ (PFC side) material for the common mode chokes

5 Summary

This document provides a complete system solution from Infineon designed for AI data center and server PSU applications.

The solution incorporates a 3-level flying capacitor PFC converter and a DC-DC isolated full-bridge LLC converter, achieving a peak efficiency of 97.8%, and a minimum full load efficiency of 96.5% at 230 V_{AC} including fan power consumption. The efficiency results are obtained with 113 W/in^3 power density.

The REF_12KW_HFHD_PSU reference board utilizes CoolSiC™ 650 V, 600 V CoolMOS™ MOSFETs, and CoolGaN™ power transistors in TOLL packages, and MV CoolGaN™ devices in a 3 mm × 5 mm package, all from Infineon. This combination of CoolSiC™, CoolMOS™, and CoolGaN™ MOSFETS enables high performance within a compact form factor, as it is presented in this document.

The 3-level flying capacitor PFC topology is digitally controlled using the XMC™ 4402 microcontroller from Infineon, while a 3rd party microcontroller is used for the control of the LLC converter.

Note that the PSU performance excels not only in steady-state conditions, offering high efficiency, but also meets power line disturbance and hold-up time requirements with an auxiliary energy buffer circuit incorporating a 2-switch buck-boost converter, which can achieve the required 20 ms hold-up at full load, and also the grid shaping function.

6 List of figures

List of figures

List of figures

7 Bill of materials

Table 3 Bill of materials for the main board M100001549

Designator	Value	Tolerance	Description
C1, C2, C9, C10	4.7 nF	Y1	Capacitor ceramic
C3	1 µF X2	10%	Capacitor foil
C4, C5	1.5 µF X2	10%	Capacitor foil
C6, C7	2.2 µF X2	10%	Capacitor foil
C8, C15, C16	3.5 µF	5%	Capacitor ceramic
C11, C12, C48, C49, C52, C54	1 µF	X7R	Capacitor ceramic
C13, C14, C20, C24, C25	100 nF	X7R	Capacitor ceramic
C17, C18, C53	330 pF	X7R	Capacitor ceramic
C26, C27, C33, C38, C39, C40, C41, C42, C43, C44, C57, C58	33 nF	5%	Capacitor ceramic
C28, C29, C30, C31, C34, C35, C36	680 µF	20%	Capacitor electrolytic
C32, C45	4.7 µF	X8L	Capacitor ceramic
C46, C47	22 µF	X7S	Capacitor unpolarized
C51	220 pF	X7R	Capacitor ceramic
D1, D2	S8KCDICT		Standard diode
D3	DFLS1200		Diode DFLS1200
D4	BAT165		Schottky diode
D8			Zener diode
F1, F2, F3, F4, F5, F6	30 A		Sicherung
GDT1	SL1002A600SP		GDT - Surge arrester
H1	HT100001548		Heatsink
H2	HT200001548		Heatsink
H3	HT300001548		Heatsink
H4	HT400001548		Heatsink
H5, H6	HT600001547		Heatsink
IC1, IC2			Integrated circuit
IC3	TLS208D1EJV		Integrated circuit
IC4	LM5050-1		O-ring gate driver IC
IC5	1EDN8511B		Integrated circuit
IC6	1EDB8275F		Integrated circuit
J1			No description available
J2			No description available
L1	1.0 mH		Common mode choke
L2	0.5 mH		Common mode choke
L3, L4	MG110001547		Pfc-choke
L5	MG200001427		Pfc-choke
L6	1.65 µH		Lr-choke
MOV1, MOV2, MOV3	V320LA20AP		Varistor

Designator	Value	Tolerance	Description
PCB1, PCB3			
Q1, Q2, Q3, Q4, Q5, Q6, Q7, Q8, Q9, Q10	ISC014N08NM6		N-channel MOSFET
Q11, Q12	IPT60R016CM8		Nmosfet
R1	3k3	1%	Resistor
R5, R6	0R		Resistor
R19	51k1	0.1%	Resistor
R22	9k09	0.1%	Resistor
R23, R24	3k16	1%	Resistor
R25, R59	100u	1%	Resistor
R27	100R	1%	Resistor
R29, R32	10R	1%	Resistor
R31	4R7	1%	Resistor
R37, R38, R39, R40, R41, R42, R43, R44, R47, R48, R49, R50, R51, R52, R53, R54	309k	0.1%	Resistor
T1, T2	TF100001547		Power transformer
TR1			Current sense transformer
TR2	XT01		Common mode power line choke
W1, W2, W7, W8, W9	0R		Resistor
W3, W4, W5, W6, W10, W11, W12, W13, W14, W15, W16, W17, W18, W19, W20, W21, W22, W23, W24, W25, W26	0R		Resistor
X2	CD100001547 connector		Female header, 26 contacts 2 mm

Table 4 Bill of materials for the LLC + EB + controller daughter card PW100001548

Designator	Value	Tolerance	Description
C1, C7, C15, C22, C23, C24, C25, C26, C27, C29, C30, C33, C34, C44, C45, C46, C47	1 µF	X7R	Capacitor ceramic
C2, C3, C5, C6, C11, C12, C13, C14	3n3	X7R	Capacitor ceramic
C4, C8, C9, C16, C35, C36, C42, C64	10 µF	X7R	Capacitor ceramic
C10	220 pF	X7R	Capacitor ceramic
C17, C18, C28, C31, C32, C43, C48, C49, C50, C51, C52, C53, C60	100 pF	X7R	Capacitor ceramic
C19, C20, C21, C37, C38, C39, C40, C41	470 nF	X7T	Capacitor ceramic

Designator	Value	Tolerance	Description
C54	68 µF	20%	Capacitor polarized
C55, C56	4.7 µF	X7R	Capacitor ceramic
C57	150 µF	20%	Capacitor polarized
C58	33 µF	20%	Capacitor polarized
C59	1 nF	X7R	Capacitor ceramic
C61, C68, C69, C70, C71, C72, C76, C78, C80, C82, C87, C88, C89, C92, C93, C95, C106	100 nF	X7R	Capacitor unpolarized, capacitor ceramic
C62, C65, C73, C74, C90, C98, C99, C100, C101, C103	330 pF	X7R	Capacitor unpolarized
C66, C67, C75, C77, C79, C81, C83, C84, C85, C86, C91, C94	10 µF	X5R	Capacitor unpolarized
C96, C97, C104, C105	8 pF	X7R	Capacitor ceramic, capacitor unpolarized
C102	1.2 nF	X7R	Capacitor unpolarized
D1, D2, D3, D4, D9, D14, D15, D16	BAT165		Schottky diode, medium power AF Schottky diode, SOD323, reel, green
D5	MM3Z6V2T1G		Zener diode MM3Z6V2T1G
D6, D7	DFLS1200		Diode
D8	SMAJ130A-E3/61		Zener diode
D10	ES1JAL_M3G		Diode
D11	LG Y876 GREEN		LED green
D12	LR Y8SF RED		LED red
D13	LO Y876 ORANGE		LED red
D17	BZX384-B18		Schottky diode
IC1	1EDN8511B		Integrated circuit
IC2, IC3, IC4, IC5	1EDB8275F		Integrated circuit
IC6, IC8	1EDB9275F		Integrated circuit
IC7	L78L12ACUTR		Integrated circuit
IC9	ICE2QR2280G		Integrated circuit
IC10	LV3842X		Synch buck
IC11	ADUM241E1BRIZ		Integrated circuit
IC12	NCV8715SQ33T2G		Positive voltage regulator
L1, L2, L3, L4, L5, L6, L7, L8	SRF2012-361YA		Common mode power line choke
L9	22 µH		WE-SPC SMD power inductor, 22 µH
L10	0.04 Ω 3A		Ferrite beads, 3 A, 0.04 Ω at DC, 60 Ω at 100 MHz
Q1, Q2, Q3, Q4, Q5, Q6, Q7, Q8	IGT65R025D2		GaN HEMT transistor
Q9, Q10, Q11, Q12	IMT65R030M2H		Insulated-gate field-effect transistor (IGFET), N-channel, enhancement, body diode, pin 1 gate, 2 driver source, 3 source, 4 source, 5 source, 6 source, 7 source, 8 source, 9 drain, 9 pins

Designator	Value	Tolerance	Description
Q13	12 MHz		SMD crystal unit for automotive application, 12.000 MHz
Q14			NPN transistor
R1, R4, R5, R8, R13, R16, R17, R20	10R	1%	Resistor
R2, R3, R6, R7, R14, R15, R18, R19, R41, R42, R47, R48	2R2	1%	Resistor
R9, R10, R11, R12, R23, R24, R25, R26, R53, R54, R56, R88, R93, R94	390R	1%	Resistor
R21	3k3	5%	Resistor
R22, R39	3k16	1%	Resistor
R27, R28, R29, R30, R31, R32, R33, R34, R35, R36, R38, R40	47R	1%	Resistor
R37, R46	10K NTC	3%	Resistor
R43, R63, R64, R65, R66, R67, R68, R73, R75, R76, R77, R78, R79, R80, R81, R83, R95, R96, R97, R98, R102	15k	1%	Resistor
R44, R45, R49, R50	1R	1%	Resistor
R51	1R5	1%	Resistor
R52	2K2	1%	Resistor
R55, R61	5k1	0.1%	Resistor
R57, R60, R69, R70	309k	0.1%	Resistor
R58, R99	0R	1%	Resistor
R59, R74	51k	0.1%	Resistor
R62, R89	22k1	0.1%	Resistor
R71, R72, R103	10k	0.1%, 5%	Resistor
R82, R84	6.8k	0.1%	Resistor
R85, R90	1k2	1%	Resistor
R86, R87, R91, R92	510R	1%	Resistor
R100	195R	1%	Resistor
R101	1k1	1%	Resistor
TF1	8032.0205.025		Flyback transformer
TR1, TR2, TR3	XT01		Common mode power line choke
U1	TLV2376IDR		Low-noise, low quiescent current, precision operational amplifier
U2	XMC4400-F64x512		Arm® Cortex®-M4 32-bit processor core
X1	FTSH-105-01-L-DV-K		Connector

Table 5 Bill of materials for the PFC power card PW200001549

Designator	Value	Tolerance	Description
C1, C2, C73, C84	470 nF	X7T	Capacitor unpolarized
C4, C5, C6, C7, C8, C9, C10, C11, C12, C13, C14, C15, C16, C17, C18, C19, C20, C21, C22, C23, C24, C25, C26, C27	1 µF	10%	Capacitor
C28, C29, C30, C32	100 nF	X7R	Capacitor unpolarized
C31, C35, C39, C43, C47, C51, C55, C59, C63, C67, C71, C76, C77, C78, C79, C83	1 µF	X7R	Capacitor unpolarized
C33, C34, C37, C38, C41, C42, C45, C46, C49, C50, C53, C54, C57, C58, C61, C62, C65, C66, C69, C70	100p	X7R	Capacitor unpolarized
C36, C40, C44, C48, C52, C56, C60, C64, C68, C74	4.7 µF	X7R	Capacitor unpolarized
C72	22 µF	X6S	Capacitor ceramic
C75	220 pF	X7R	Capacitor unpolarized
D1, D2, D3, D4, D5	ES1JFL		Diode
D6, D7, D9, D10	BAT165		Schottky diode
D8	MM3Z6V2T1G		Zener diode MM3Z5V1ST1G
IC1	TLV9102IDDFR		Integrated circuit
IC2, IC3, IC4, IC5, IC6, IC7, IC8, IC9, IC10, IC11	1EDB9275F		Integrated circuit
IC12	1EDN8511B		Gate driver IC
NTC	10k		Resistor
Q1, Q2, Q3, Q4, Q5, Q6, Q7, Q8	IMT65R010M2H		Insulated-gate field-effect transistor (IGFET), N-channel, enhancement, body diode, pin 1 gate, 2 driver source, 3 source, 4 source, 5 source, 6 source, 7 source, 8 source, 9 drain, 9 pins
Q10, Q11, Q12, Q13	IMBG65R007M2H		Insulated-gate field-effect transistor (IGFET), N-channel, enhancement, body diode, pin 1 gate, 2 driver source, 3 power source, 4 power source, 5 power source, 6 power source, 7 power source, 8 drain, 8 pins
R1, R2, R3, R4, R5, R6, R7, R8	2R2	1%	Resistor
R9	3k3	1%	Resistor
R10, R11, R14, R15	1k0	1%	Resistor
R12, R13, R16, R17, R59	10R	1%	Resistor
R18, R19	10k	1%	Resistor
R21, R22, R29, R30	680k	0.1%	Resistor
R23, R28, R31, R32	9.31k	0.1%	Resistor

Designator	Value	Tolerance	Description
R24, R25, R26, R27, R33, R34, R35, R36	340k	0.1%	Resistor
R37, R38, R40, R41, R42, R43, R45, R46, R47, R48, R50, R51, R52, R53, R55, R56, R57, R58, R60, R61	510R	1%	Resistor
R39, R44, R49, R54	4R7	1%	Resistor
R62, R63	3k16	1%	Resistor
TR1, TR2	XT01		Common mode power line choke

Table 6 Bill of materials for the control card CD200001528CD100001427

Designator	Value	Tolerance	Description
B1	LT8645SHV2PBF		Switching voltage regulators 65 V, 8 A sync buck silent switcher 2 w/ 2
C1, C12, C49, C54, C59, C65, C66, C67, C68, C74, C75	100 nF	X7R	Capacitor ceramic
C2, C3, C4, C5, C6, C13, C14, C15, C16, C17	22 µF	X7R	Capacitor ceramic
C7, C18, C19	10 µF	X7R	Capacitor ceramic
C9, C11	220 nF	X7S	Capacitor ceramic
C10	100 nF	X7S	Capacitor ceramic
C21	4.7 pF	C0G	Capacitor ceramic
C22	1 µF	X7R	Capacitor ceramic
C23	10 nF	X7S	Capacitor ceramic
C48, C55, C56, C69	10 µF	X5R	Capacitor ceramic
C57, C58, C61, C63, C64, C71	330 pF	X7R	Capacitor ceramic
C60, C62	4n7	X7R	Capacitor ceramic
C70, C72	100 pF	X7R	Capacitor ceramic
D1, D2, D7, D8, D9, D10	BAT165		Schottky diode
D4	DFLS1200		Diode
D11	GREEN LED		LED
IC8	dsPIC33CK256MP203-I/M5		MCU
IC10	TLV2376IDR		Integrated circuit
IC12	LMH6642MF		Integrated circuit
IC13	TLS820D0ELV33XUM		Low drop-out linear voltage regulator
J1	Molex picoblade 53261-0871		PCB mount header, vertical, wire-to-board, 8 position, 1.25 mm [.049 in] centerline, fully shrouded, tin, through hole - solder, signal, natural
L1	IHLP4040DZER470M51		Magnetic
L2	IHLP4040DZER220M11		Magnetic

Designator	Value	Tolerance	Description
L3	Ferrite bead 60 Ω at 100 MHz		Magnetic
NTC1	10K	1%	NTC resistor
R1, R11	0R	1%	Resistor
R3	21k	0.1%	Resistor
R4	130k	1%	Resistor
R5, R48, R56, R63	4k99	0.1%	Resistor
R6	8k87	0.5%	Resistor
R7	180k	1%	Resistor
R8, R31	1k	1%	Resistor
R9	100k	0.5%	Resistor
R10	110k	0.5%	Resistor
R12, R75	1R	1%	Resistor
R15, R62	2k7	1%	Resistor
R16, R19, R20, R49, R52	124R	0.1%	Resistor
R18, R70	100R	1%	Resistor
R47, R53	10k	0.1%	Resistor
R50, R54, R58	49k9	0.1%	Resistor
R51, R55, R59	54k9	0.1%	Resistor
R60, R69	15k	1%	Resistor
R71, R72, R77	510R	1%	Resistor
R73, R74	261R	1%	Resistor
U1	LMR38025SQDRRRQ1		Integrated synchronous buck
X1			Pin header, 5 contacts
X3			2x13 2 mm male connector
X6	B2B-ZR		Connector

Table 7 Bill of materials for the secondary-side transformer PCB MG100001552

Designator	Value	Tolerance	Description
C1, C2, C3, C4, C5, C6, C7, C8, C9, C10, C11	4.7 µF	X8L	Capacitor ceramic
C13, C15, C17, C18, C19, C20	1 µF	X7R	Capacitor ceramic
C14, C16	4.7 µF	X7R	Capacitor unpolarized
D1, D2	BAT46WJ		Schottky diode
IC1, IC2	2EDB7259K		Gate driver IC
IC3, IC4	NCV8715SQ50T2G		Positive voltage regulator
R1, R4	2k	1%	Resistor
R2, R3	2.2R	1%	Resistor
T1, T2, T3, T4, T5, T6, T7, T8	IGC016K10S2		GaN FET

Table 8 Bill of materials for the surge electrolytic capacitor PCB C200001547

Designator	Value	Tolerance	Description
C1	240 µF/475V B43659X0034M305		Capacitor polarized
C2	1 µF	X7R	Capacitor ceramic
C3	2.2 nF	X7R	Capacitor ceramic
IC1	1EDN8511B		Integrated circuit
J1			Connector
NTC1	15R0	20%	NTC resistor
Q1	IPT60R016CM8		Insulated-gate field-effect transistor (IGFET), N-channel, enhancement, body diode, pin 1 gate, 2 driver source, 3 source, 4 source, 5 source, 6 source, 7 source, 8 source, 9 drain, 9 pins
R1, R3	4R7	1%	Resistor
R2	510R	1%	Resistor
R4	22R	1%	Resistor

Table 9 Bill of materials for the energy buffer bulk capacitor PCB PW400001548

Designator	Value	Tolerance	Description
D2	ORANGE LED		LED
D1	BLUE LED		LED
C17, C18, C19, C20, C21, C22	800 µF/475V B43658A0807M052	20%	Capacitor polarized
R1, R2	510R	1%	Resistor
CONN1			Please ship cable together with assembly
J2			Connector
J1, J3			Connector

8 Schematics

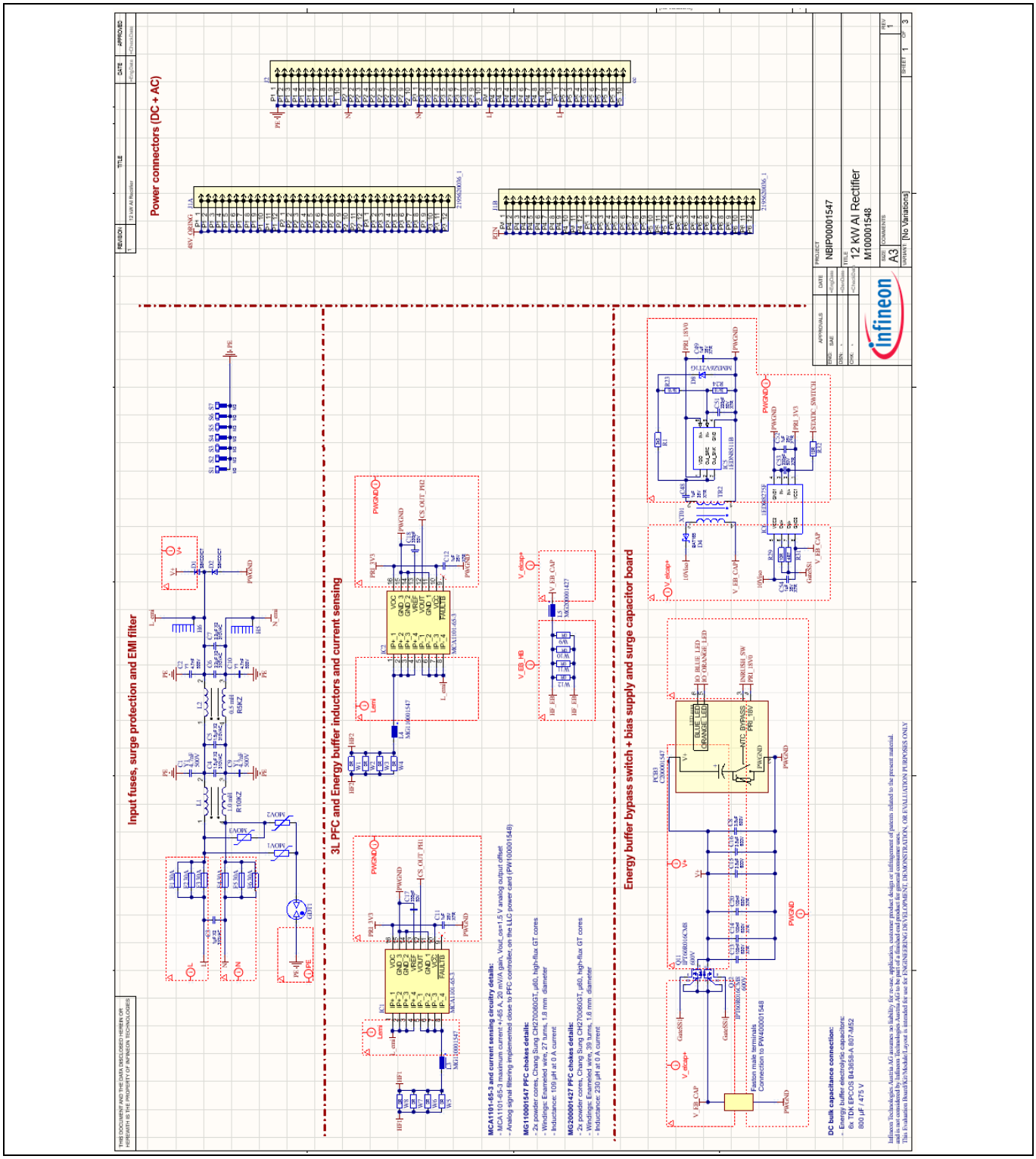


Figure 80 Schematic of the main board (M100001549) – page 1

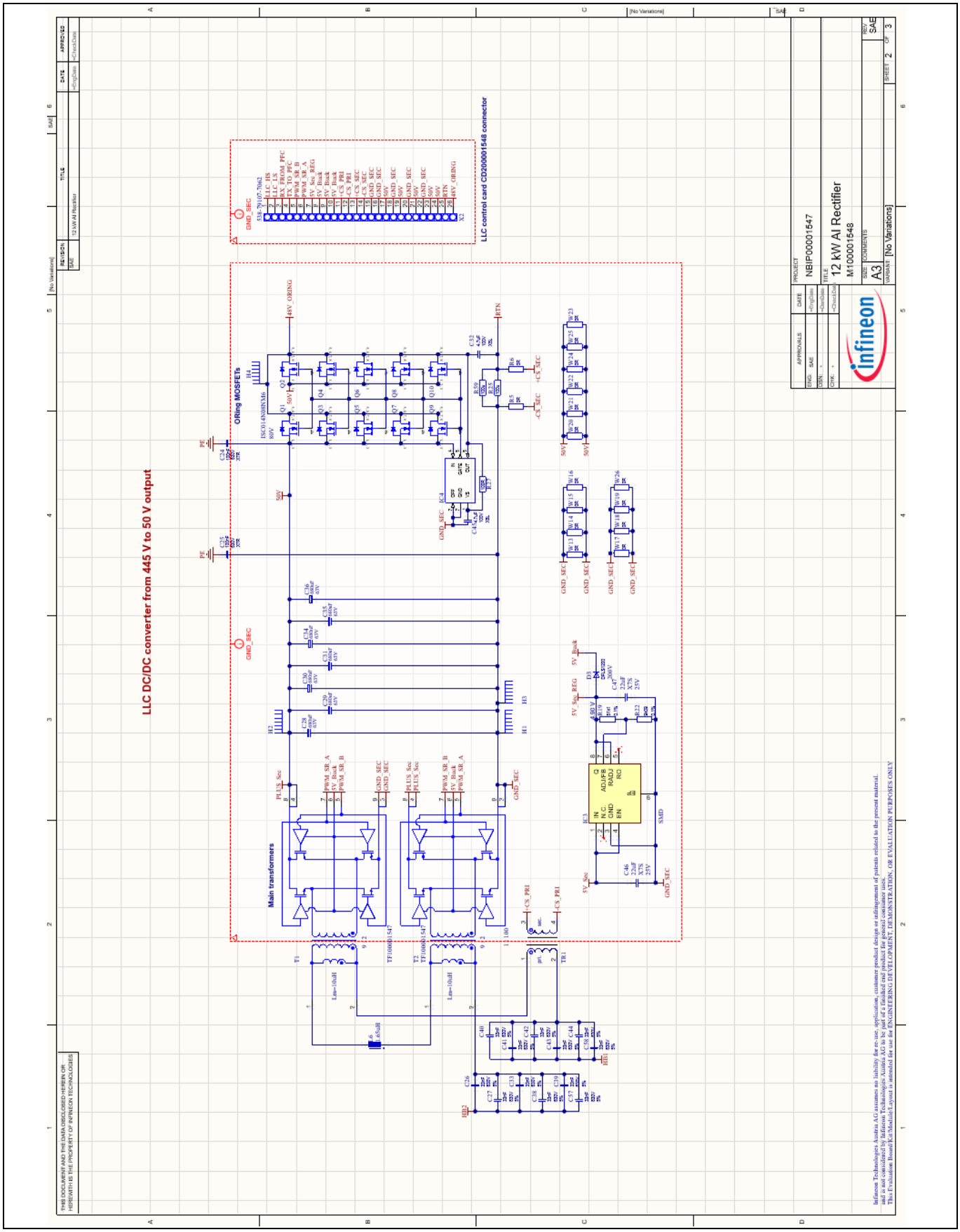


Figure 81 Schematic of the main board (M100001549) – page 2

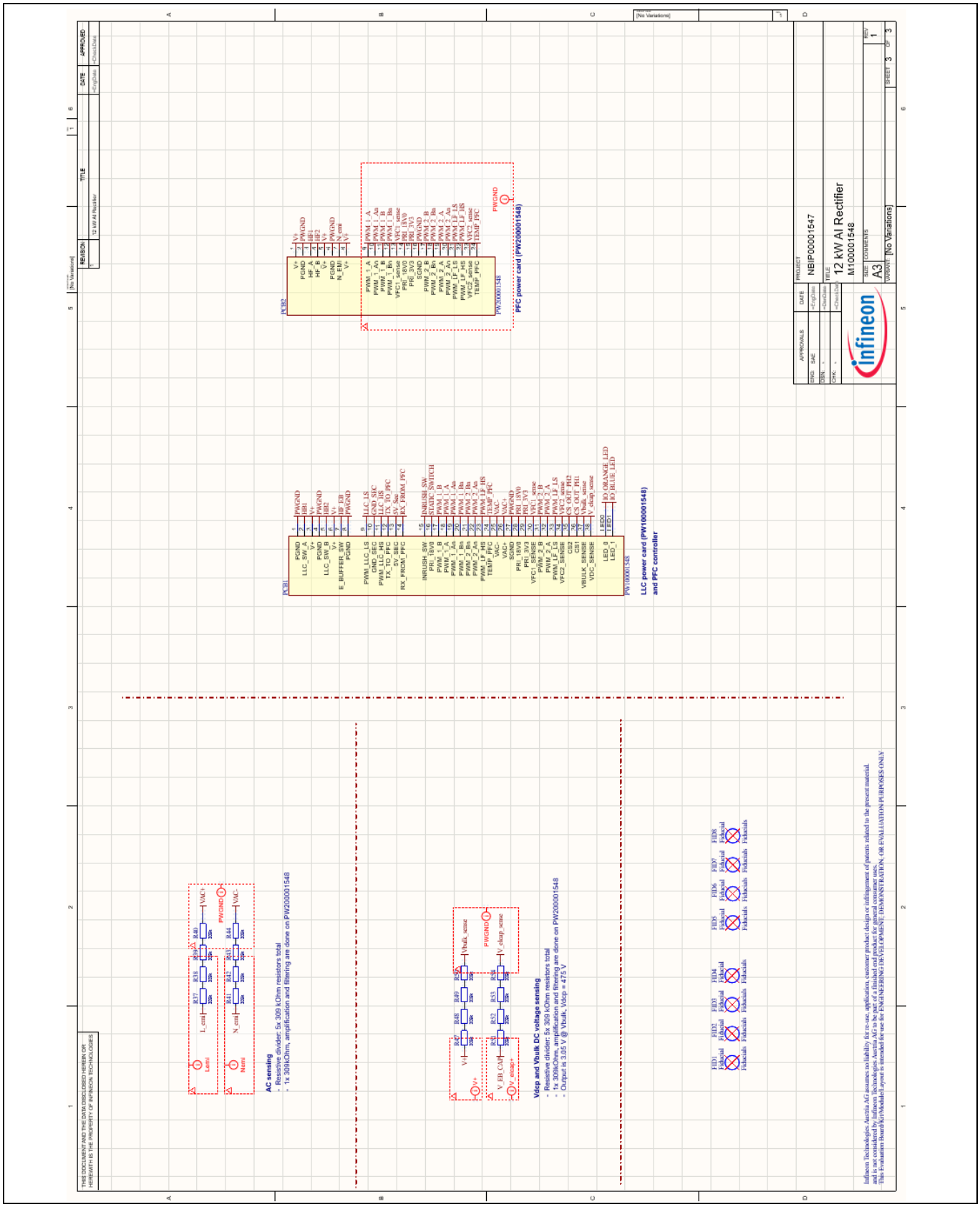


Figure 82 Schematic of the main board (M100001549) – page 3

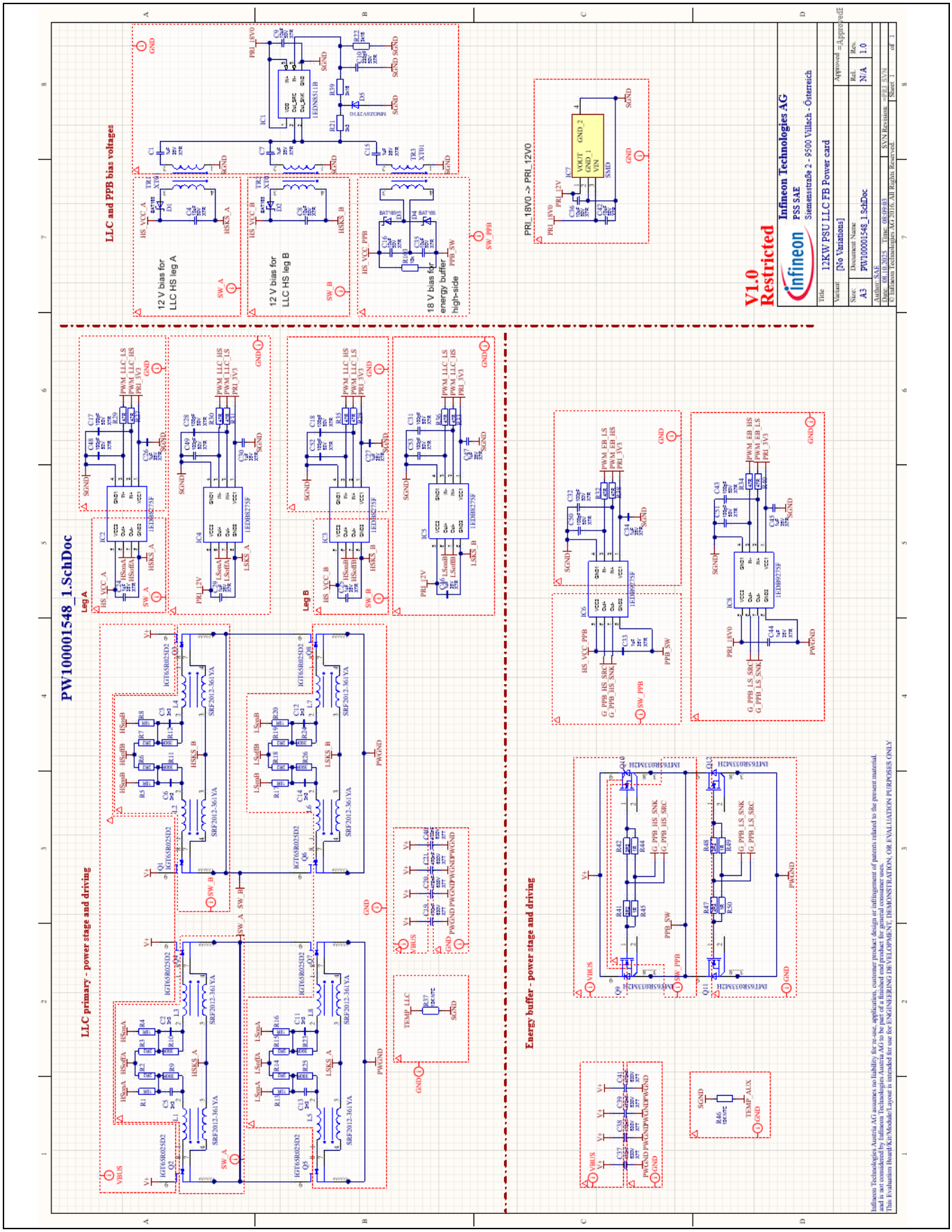


Figure 83 Schematic of the LLC + EB + controller daughterboard (PW100001548) – page 1

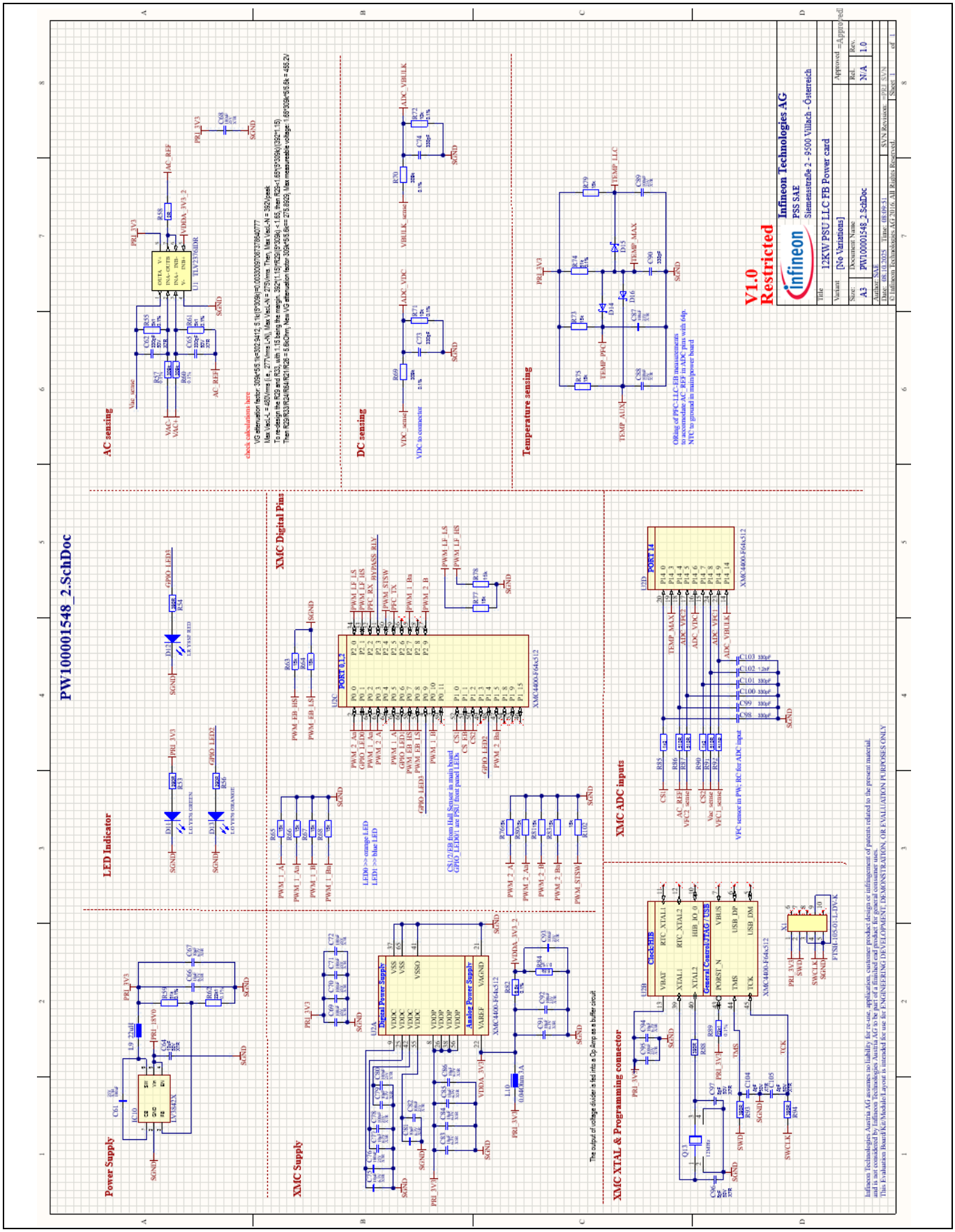


Figure 84 Schematic of the LLC + EB + controller daughterboard (PW100001548) – page 2

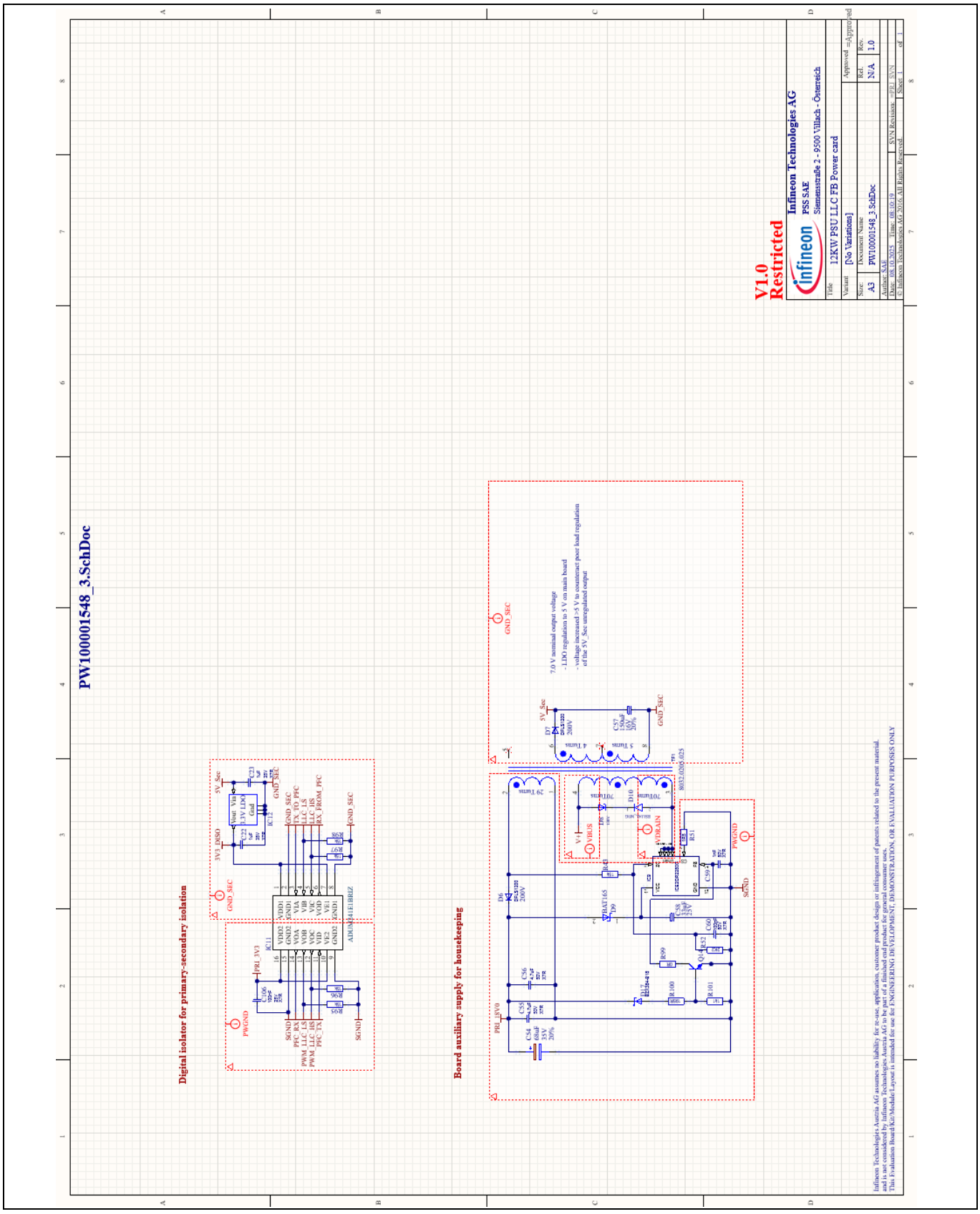


Figure 85 Schematic of the LLC + EB + controller daughterboard (PW100001548) – page 3

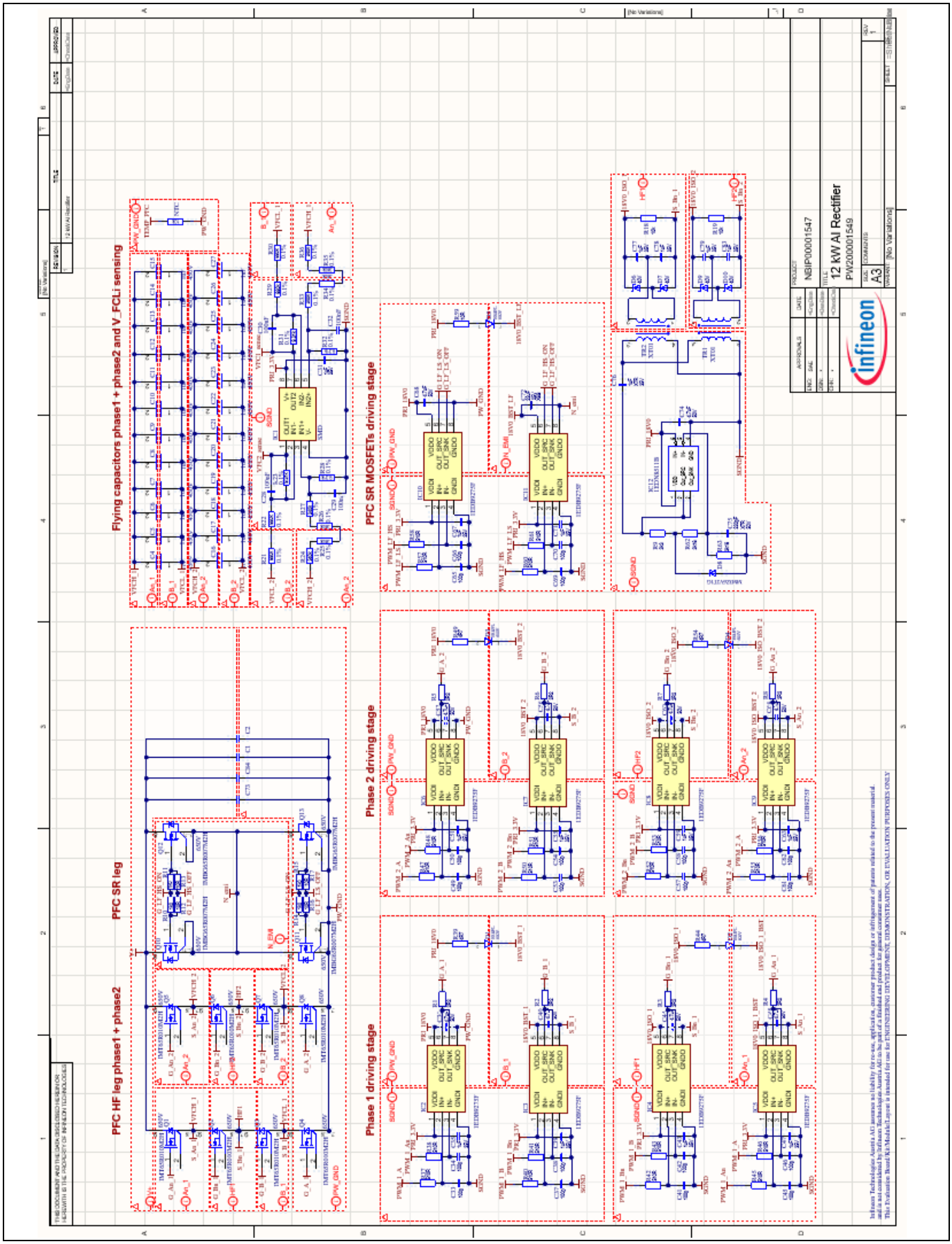


Figure 86 Schematic of the PFC power board (PW200001549)

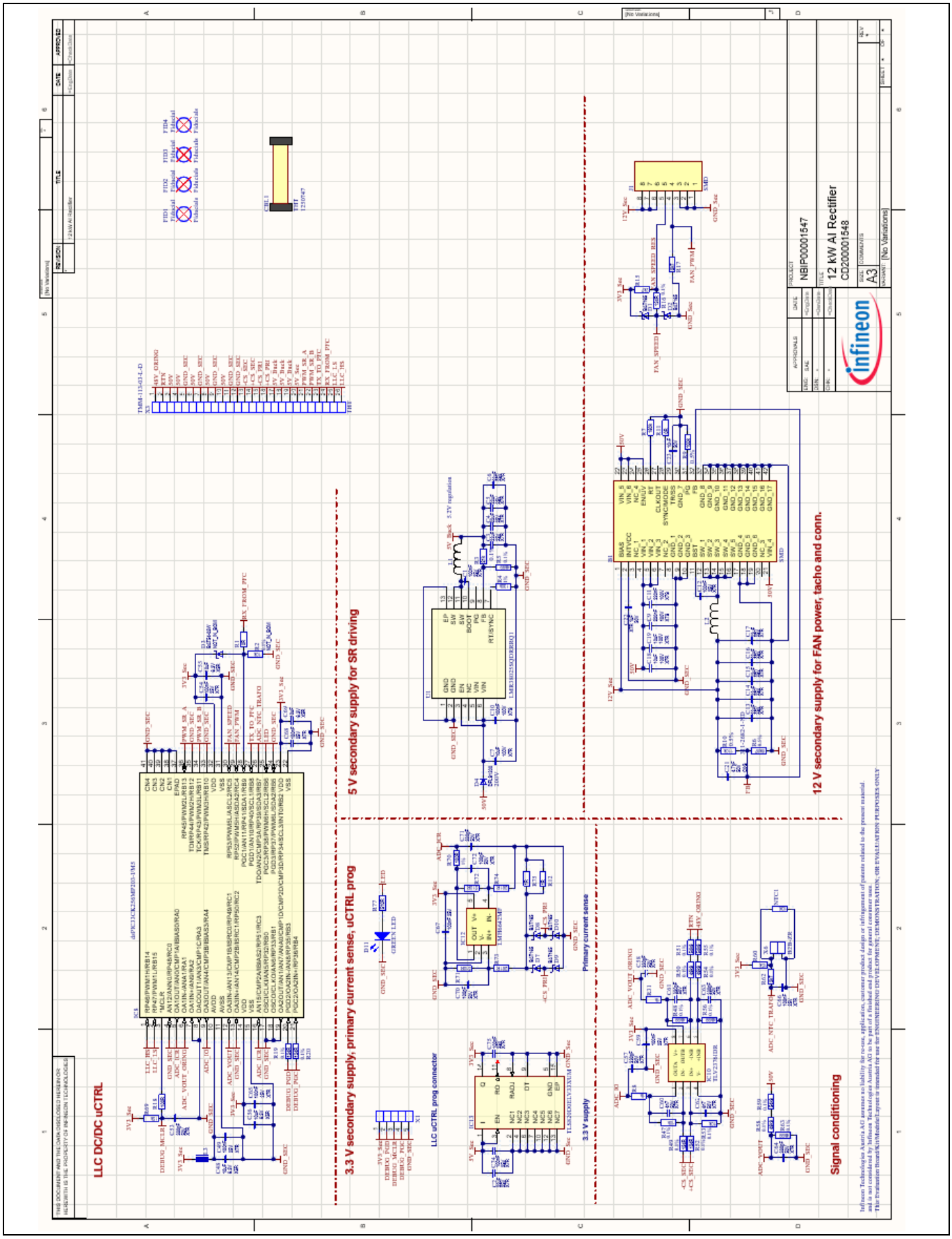


Figure 87 Schematic of the LLC control board (CD200001548)

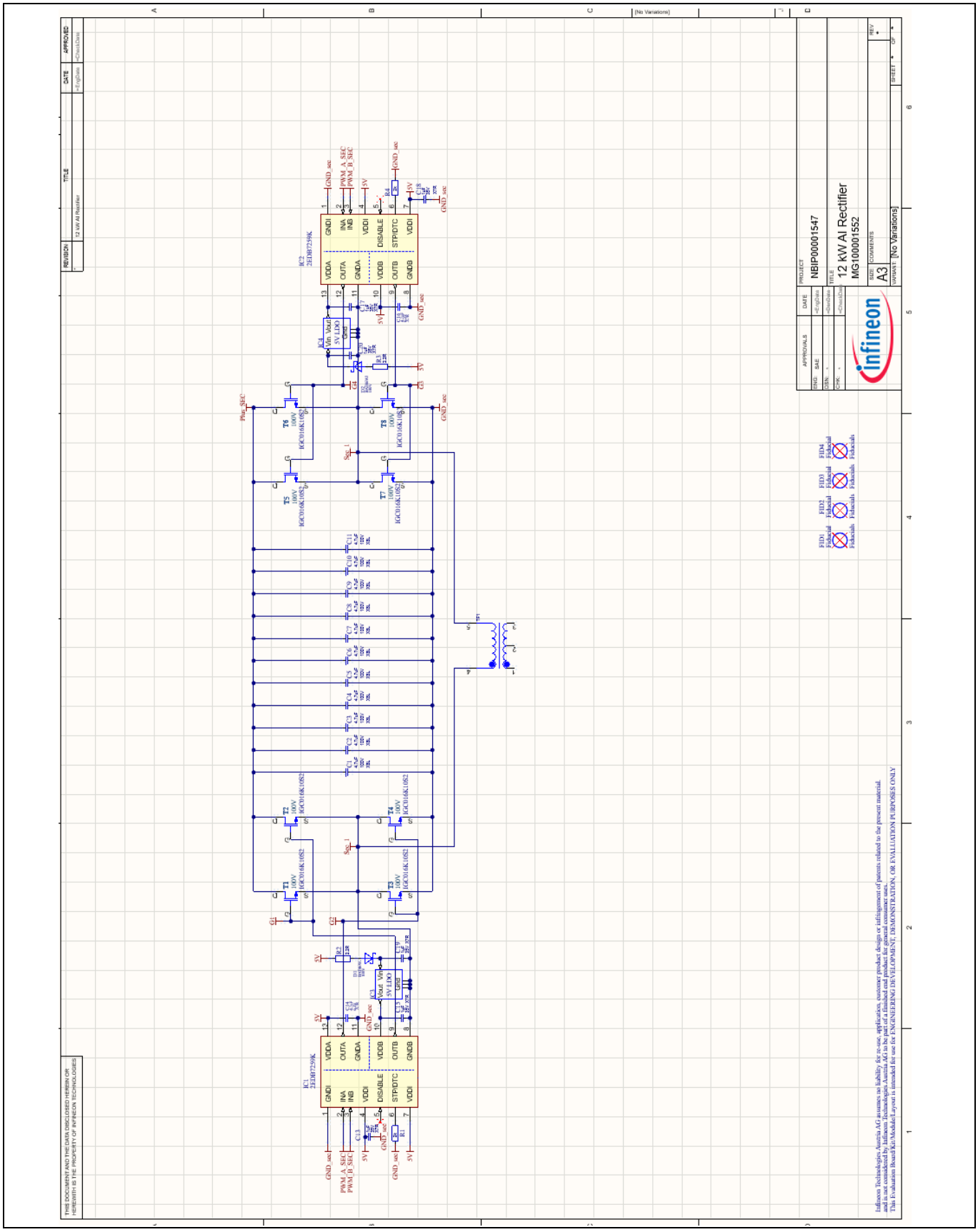


Figure 88 Schematic of the LLC secondary side winding integrating the SR bridge (MG100001552)

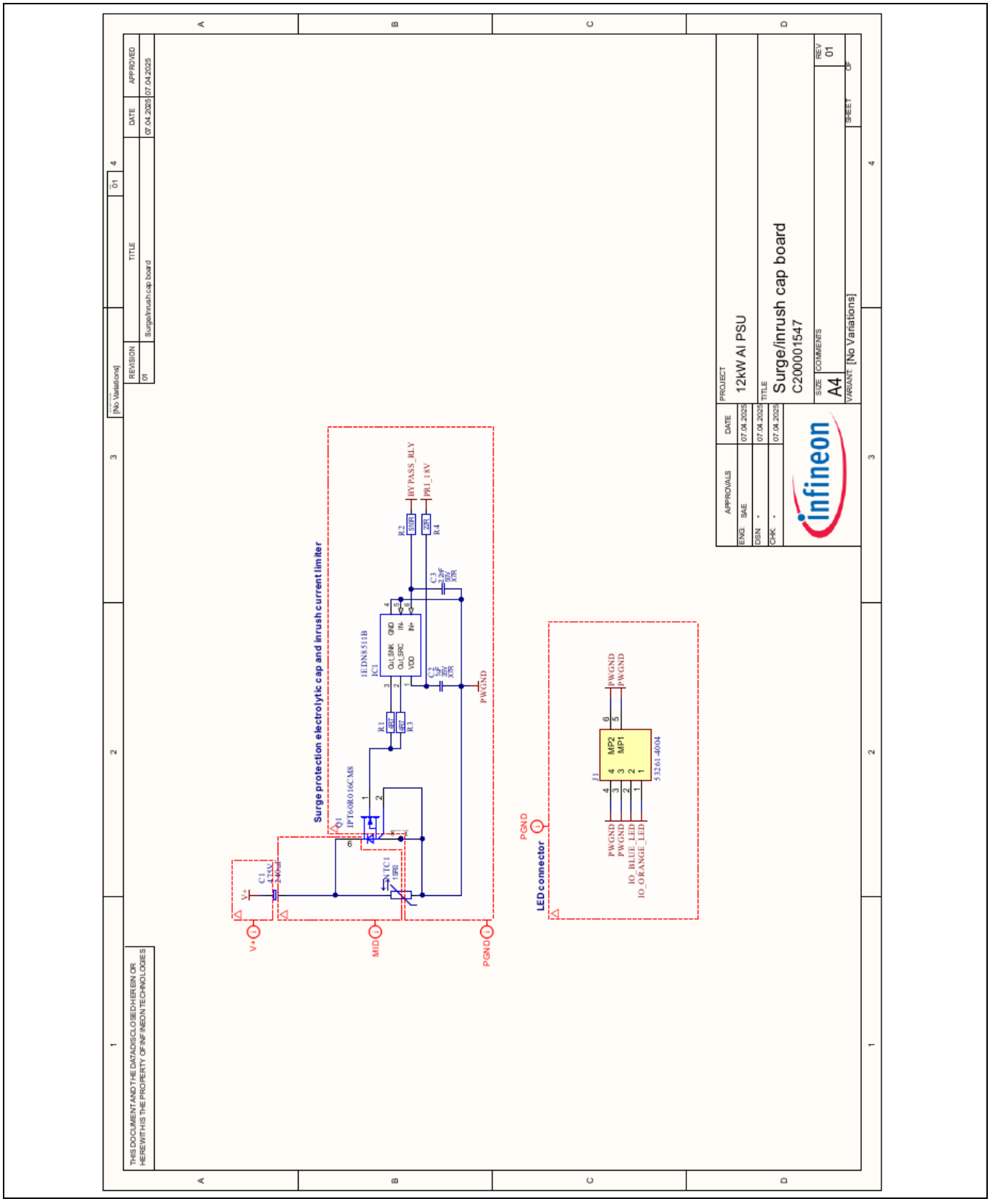


Figure 89 Schematic of the surge electrolytic capacitor board (C200001547)

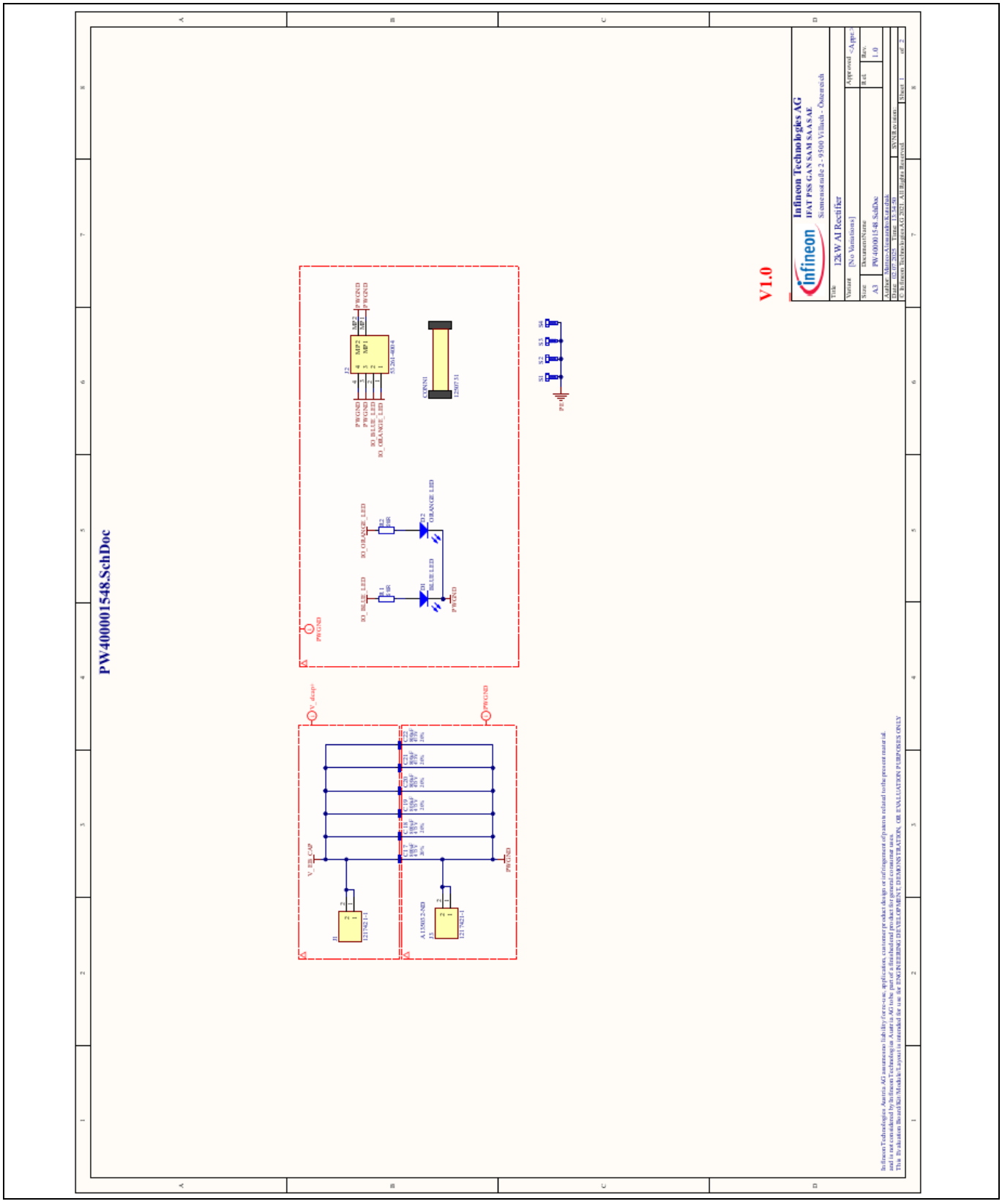


Figure 90 Schematic of the energy buffer bulk capacitor board (PW400001548)

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Acronyms/abbreviations

Table 10 Acronyms/abbreviations

Acronym	Description
ADC	analog to digital converter
BW	bandwidth
CCM	continuous conduction mode
DFF	duty feed-forward
FB	full-bridge
GaN	gallium nitride
HB	half-bridge
HV	high voltage
IBC	Intermediate bus converter
iTHD	input current total harmonic distortion
LCDO	line cycle drop-out
LDO	low dropout voltage regulator
OCP	overcurrent protection
OVP	overvoltage protection
PCB	printed circuit board
PF	power factor
PFC	power factor correction
PGND	power ground
PSU	power supply unit
PWM	pulse width modulation
Si	silicon
SiC	silicon carbide
SMPS	switched mode power supply
SR	synchronous rectification
THD	total harmonic distortion
UVLO	undervoltage lockout
UVP	undervoltage protection
VRM	voltage regulator module
WBG	wide bandgap
XFMR	transformer

Revision history

Document revision	Date	Description of changes
V 1.0	2025-11-30	Initial release

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