International
IOR Rectifier

APPLICATION NOTE

Application Note AN-1213

Scalable Power Solutions for Freescale's Network Processors

By
Tony Ochoa

Table of Contents

Page

Section 1: Summary Freescale & IR Reference Designs.....2

Section 2: Power Map Diagrams T4240, T2080, T1040.....5

Section 3: Core Voltage Requirements T Series Processors 10

Section 4: Core Voltage Power Design & Layout 15

Section 5: Core Voltage Design Validation 17

Section 6: Power Sequencing Requirements 18

Section 7: Power Requirements - System, Bus, Peripheral, SERDES Voltage Rails 20

Section 8: Design Options for Scalability.....23

Section 9: IR Device Highlights and Ordering Codes 26

Introduction

International Rectifier is a “Proven Partner” on Freescale’s Connect Program. This document describes how to implement robust, proven solutions and provides options for scalability for CPU, Memory and I/O voltage rails. All power solutions for Freescale’s QorIQ T-series reference designs have been carefully tested by Freescale and International Rectifier to insure strict adherence to the 3% specification and critical rails. DC, AC and ripple accuracy results were performed to verify the power solution that included scaling processor cores from 24 Cores to 4 Cores with Dhrystone Code for the T4, T2 and T1 series.

The Designs have been verified with Freescale on the RDB/QDS evaluation platforms and given to ODM/IDH partners to seed production level reference designs.

The QorIQ T4240 reference design board (T4240RDB) is a compact (1U), highly integrated board featuring the 24-virtual core T4240 device. With its 1.67 GHz T4240 processor and rich input/output (I/O) mix, the board is designed for evaluating the T4240, T4160, and T4080.



Download T4240 info from Freescale

Click to Download Power Solution for T4240 from IR

The QorIQ T2080 reference design board (T2080RDB) is a highly integrated tool featuring the QorIQ T2080 communications processor. T2080 and T2081 processors in networking and Ethernet applications data plane in enterprise equipment, service provider, wireless infrastructure, aerospace and industrial computing.



Download T2080RDB Info from Freescale

Click to Download Power Solution for T2080 RDB from IR

The QorIQ T1040 reference design board (T1040RDB) is a high performance computing evaluation, development and test platforms supporting the QorIQ T1040/20 communications processors built on Power Architecture® technology.

The QorIQ T1024 processors combine single or dual 64-bit cores, built on Power Architecture® technology, with high-performance Data Path Acceleration

Architecture (DPAA) and network peripheral bus interfaces required for networking and telecommunications applications.



Download T1040RDB Info from Freescale

Click to Download Power Solution for T1040 RDB from IR

REFERENCE DESIGN	CORE POWER	COMM & PERIPHERAL POWER	MOSFET SWITCHES
T4240RDB	IR3565B (4+2) + IR3550	IR3897 x6	(IRFML8244 , IRLML6346 on PCI version)
T2080RDB	IR36021 (2+0) + IR3553 (IR3550 option)	IR3473 x 8, IR3475 x 1	IRF9321 , IRLML6346 , IRLML2502
T1040RDB	IR36021	IR3473 x 5, IR3475 x 2	IRFH6200 , IRFHM4226 , IRLML2030 , IRF9321 IRLML6346 , IRLML2502 , IRLZ24NSPBF
T1024RDB	IR3475	IR3473 x 6, IR3475 x 2	IRF9321, IRFH6200, IRFHM4226, IRLML2030, IRLML2502, IRLML6346

Table 1: Freescale Reference Designs for QorIQ T Series Processors

IR Part Number	Description	Use in QorIQ T Series
IR3565BMFS01TRP	4+2 Multiphase DC/DC converter T4 core + memory voltages	T4 / T2 / T1 core + memory voltage
IR36021MFS01TRP	2+1 Multiphase DC/DC converter	T1 / T2 core + memory voltages
IR36021MFS02TRP	2+0 Multiphase DC/DC converter	T1 / T2 core voltage
IR3550 / IR3551 / IR3553 / IR3742	60A / 50A / 40A / 20A PowIRStage® (required by IR3565 & IR36021)	T4 / T2 / T1 core + memory voltage
IR3897 / IR3898 / IR3899 / IR3895	4A / 6A / 9A / 16A SupIRBuck® Point of Load DC/DC Converters	Comms I/O, Peripherals, System Voltages
IR3891	Dual 4A SupIRBuck ® Point of Load DC/DC Converter Chipset voltages	Comms I/O, Peripherals, System Voltages
IR3856	6A SupIRBuck® Point of Load DC/DC Converter	Comms I/O, Peripherals, System Voltages
IR3473 / IR3475	6A / 10A SupIRBuck® Point of Load DC/DC Converter	Chipset voltages for EnergyStar

Table 2: IR DC DC Converters Required on Freescale Designs

Freescale T4240 Power Reference Design Summary. IR is the proven partner for Freescale's T4 Processors. Each power design was verified by both Freescale and IR engineers with extensive DC and AC analysis of processor mode of operations. The following reference design is available below.

Applications

Networking, telecom/datacom, wireless infrastructure and military/aerospace

Power Rail Requirements

Core Voltage

1.05 V ± 30 mV (boot voltage)*
VID ± 30 mV (normal operation)

Note: VID loaded at Boot from T4240 Fuse Status Register (Figure 4)
*Accuracy includes DC, AC and Load Step Variation (see Figure 5)

Load Step:

T4240: 20A for 12 cores
T4160: 15A for 8 cores
T4080: 10A for 4 cores

Slew rate: 12A/μs

Power Dissipation Range:

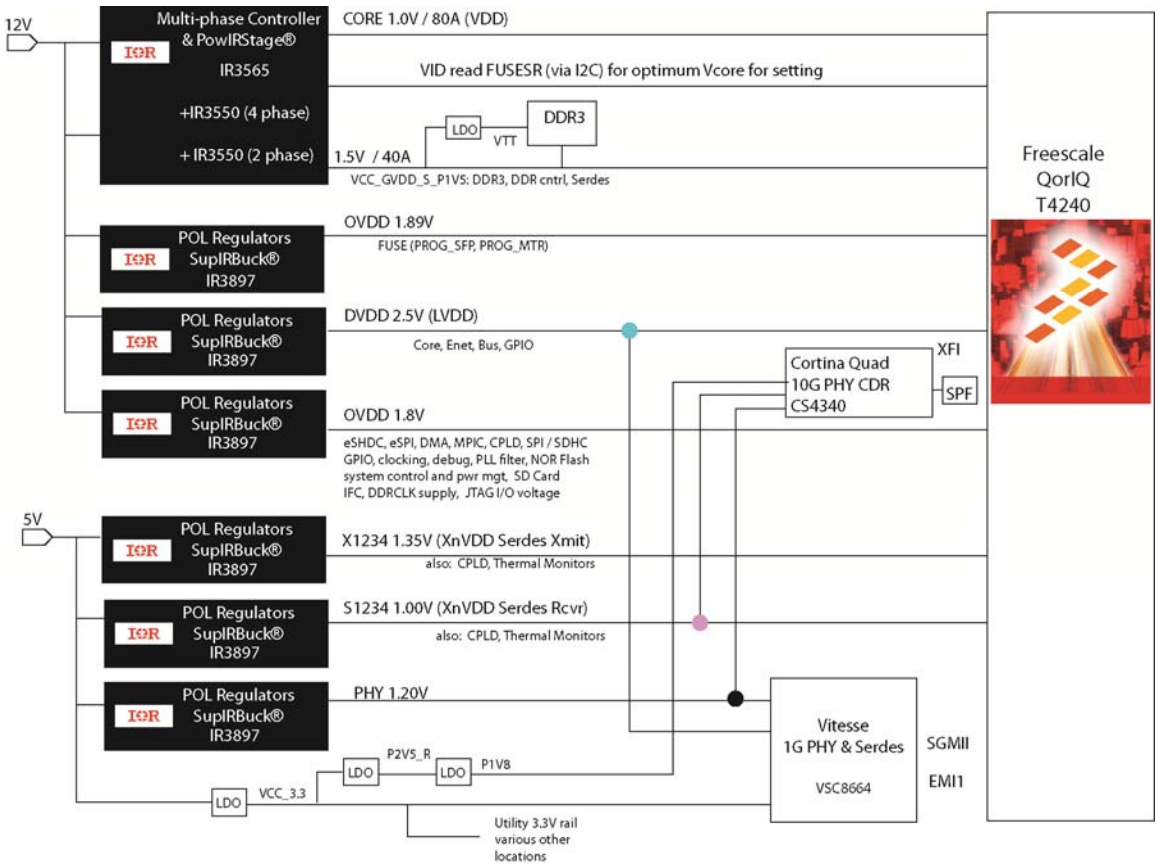
32 to 64W worst case Core + SVDD, for 1.5 to 1.6GHz. (Table 6 and 7, T4240 datasheet)

SERDES Voltage Supplies - SnVdd and XnVdd (schematic as X1234 and X1234). Absolute peak ripple/noise should not exceed 10mV when measured from 50 kHz to 500MHz. IR implemented special filters to meet these specs.

IR's Core and Memory Rails meets Freescale Compliance test verified using Dhrystone codes for worst case transients (see Figure 9)

Power sequencing is validated and shown in Figure 10.

Power Solution: QorIQ T Series T4240/T4160/T4080 24/16/8 Virtual Core



Reference Design Information

Click Here IR-Freescale Power Solution

Freescale T2080 Power Reference Design Summary. IR is the proven partner for Freescale's T2 Processors. Each power design was verified by both Freescale and IR engineers with extensive DC and AC analysis of processor mode of operations. The following reference design is available below.

Applications

Networking, telecom/datacom, wireless infrastructure and military/aerospace

Power Rail Requirements

Core Voltage

1.025 ± 30 mV (boot voltage)
VID ± 30 mV (normal operating)
VID range (0.975 to 1.025V)
VID control (see 4.2.1, page 160).
Note: VID loaded at Boot from T2080 Fuse Status Register (Figure 4)
*Accuracy includes DC, AC and Load Step Variation (see Figure 5)

Load Step:
T2080: 10A for 8 cores
T2081: 10A for 8 cores

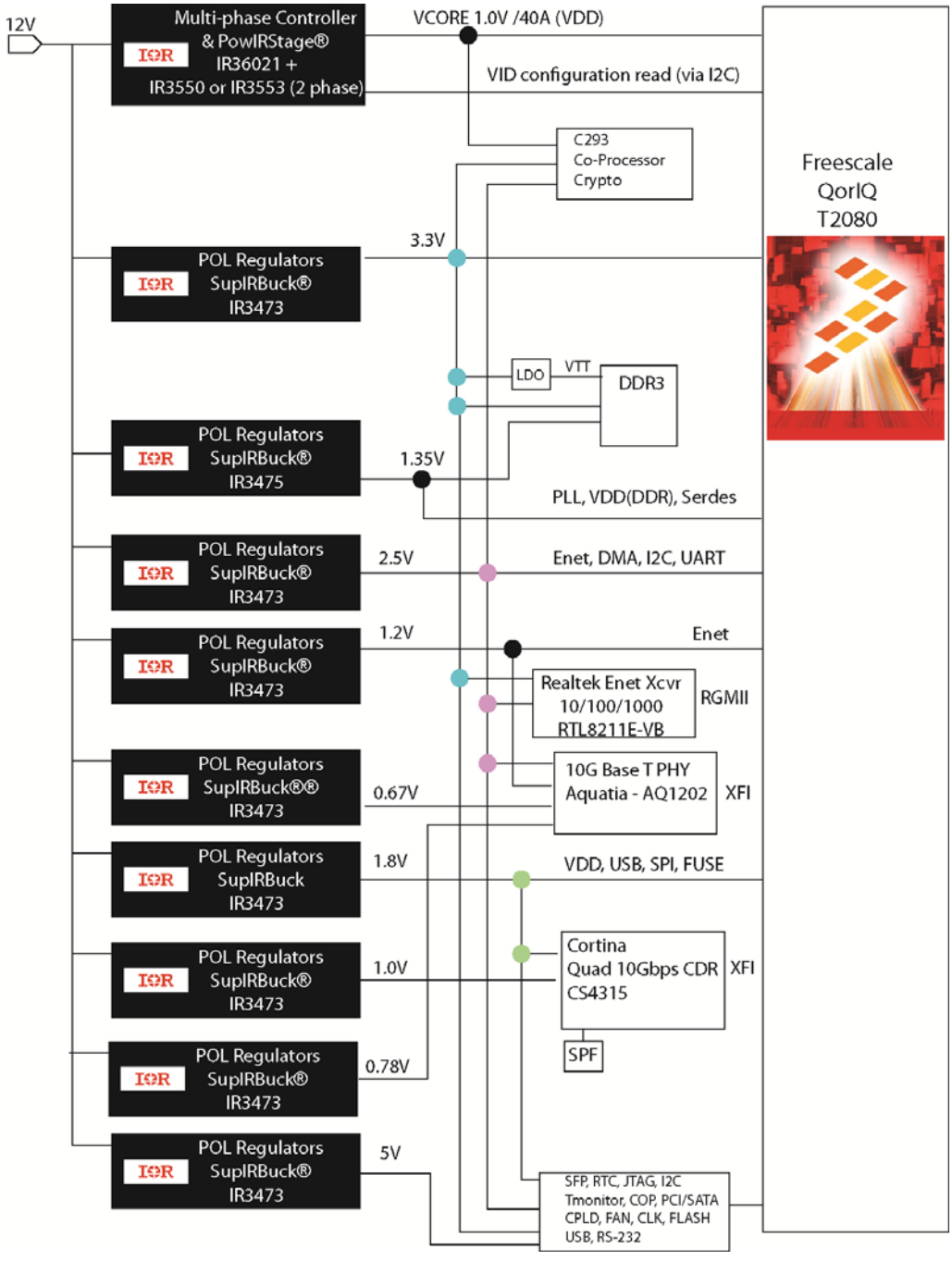
Slew rate: 12A/μs

Power Dissipation Range:
16 to 29W worst case Core, for 1.2 to 1.8 GHz (Table 6 and 7, T2080 datasheet)

IR's Core and Memory Rails meets
Freescale Compliance test verified using Dhrystone codes for worst case transients (see Figure 9).

Note: Freescale used the T4240 platform to scale the threads to test for T2080 over the Dhrystone codes.

Power Solution: QorIQ T Series T2080: T2080/T2081 Eight Virtual Core



Reference Design Information

Click here IR-Freescale Power Solution

Freescale T1040 Power Reference Design Summary. IR is the proven partner for Freescale's T1 Processors. Each power design was verified by both Freescale and IR engineers with extensive DC and AC analysis of processor mode of operations. The following reference design is available below.

Applications

Networking, telecom/datacom, wireless infrastructure and military/aerospace

Power Rail Requirements

Core Voltage

1.025 ± 30 mV (boot voltage)

VID ± 30 mV (normal operating)

VID control (see 4.2.1, page 163, 164)

Note: VID loaded at Boot from T1040 Fuse Status Register (Figure 4)

*Accuracy includes DC, AC and Load Step Variation (see Figure 5)

Load Step:

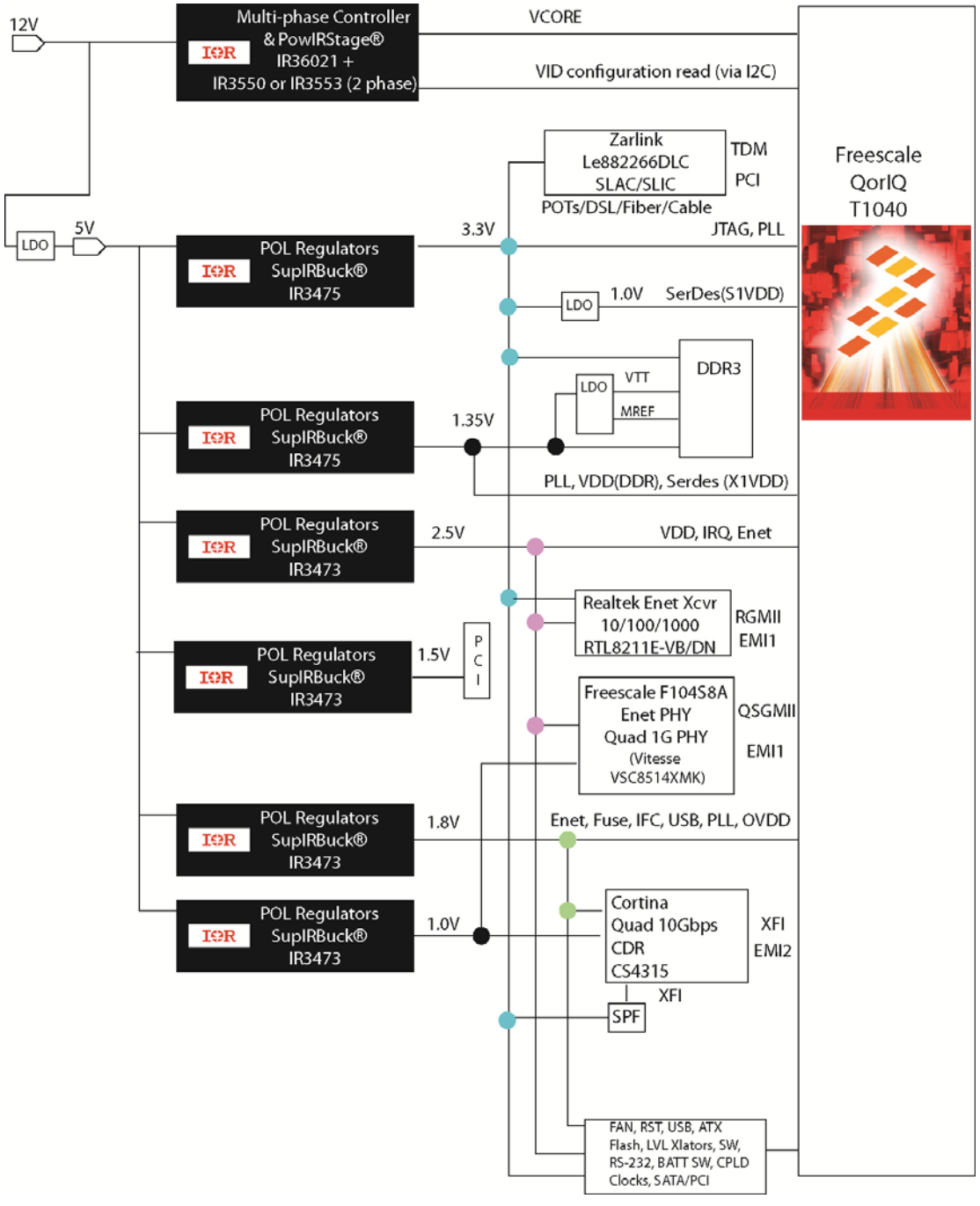
T1040: 5A for 2 cores

Slew rate: 12A/μs

IR's Core and Memory Rails meets Freescale Compliance test verified using Dhrystone codes for worst case transients (see Figure 9).

Note: Freescale used the T4240 platform to scale the threads to test for T2080 over the Dhrystone codes.

Power Solution: QorIQ T Series T1040: T1040 / T1020 Quad- and Dual-Core



Reference Design Information

Click for IR-Freescale Power Solution

Power Requirements - Core Voltage

The T Series processors are binned into 24 discrete clock & VID settings. Freescale CPUs have a 32-bit register that specifies the speed bin, clock and optimum core voltage (Table 3, Figure 4).

FUSESR - Current Chassis Definition		
Bits	Field	Definition
0-1	-	Reserved
2-3	BIN	2'b00 - Speed bin 1 (low) 2'b01 - Speed bin 2 (medium) 2'b10 - Speed bin 3 (high) 2'b11 - Speed bin 4 (premium)
4-8	PLAT_V	5'b00000 – 0.8000V 5'b00001 – 0.8125V 5'b00010 – 0.8250V 5'b00011 – 0.8375V 5'b00100 – 0.8500V 5'b00101 – 0.8625V 5'b00110 – 0.8750V 5'b00111 – 0.8875V 5'b01000 – 0.9000V 5'b01001 – 0.9125V 5'b01010 – 0.9250V 5'b01011 – 0.9375V 5'b01100 – 0.9500V 5'b01101 – 0.9625V 5'b01110 – 0.9750V 5'b01111 – 0.9875V 5'b10000 – 1.0000V 5'b10001 – 1.0125V 5'b10010 – 1.0250V 5'b10011 – 1.0375V 5'b10100 – 1.0500V 5'b10101 – 1.0625V 5'b10110 – 1.0750V 5'b10111– 1.0875V 5'b11000 – 1.1000V 5'b11001 – reserved … 5'b11111 – reserved
9-13	DA_V	Same as PLAT_V
14-18	DB_V	Same as PLAT_V
19-23	DC_V	Same as PLAT_V
24-31	-	Reserved

Table 3: Freescale FUSESR Register

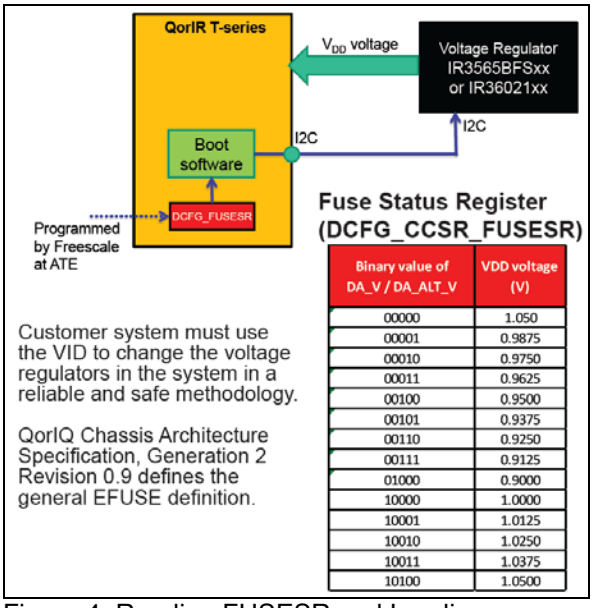


Figure 4: Reading FUSESR and Loading VID for the Optimum Core Voltage

During the T Series boot process the IR voltage regulator starts up to the pre-defined boot voltage which guarantees that the CPU will operate in safe mode. Next, the software must read the VID EFUSE values stored in the Fuse Status register (FUSESR) and then configure the external voltage regulator based on this information. Proper setting will ensure best performance at the optimized core voltage for each processor (the boot voltage is NOT the optimum core voltage for best performance). The optimum core voltage will vary from processor to processor. The software pseudo-code for setting the core (VID) voltage is shown (right). The reason for this software optimization loop is that the core voltage must meet 3% accuracy requirements to ensure that the processor operates within the tolerance band defined by Freescale (see Figure 3 and 4). Freescale's Boot code interfaces with IR's Digital controllers to load the VID Codes from the FUSESR register via I2C / PMBus. The boot code is to be made available on upcoming SDK patches by Freescale. The advantage of IR's Digital Controllers is that the VID can be set real-time during boot up. The IR Digital Controllers can set the VID to an accuracy of ± 5mV steps. Setting each individual processor optimum core voltage accurately will ensure best performance and ideal power consumption operating point while maintaining the 3% accuracy requirements.

Core Voltage - VID Setting & Adjust Output Voltage

/* Pre-configured addresses per Freescale reference designs */
/* IR Part# address = <See Table 4> */
/* Set_voltage_register_address = <0x6A> for IR36021FS01/2 & IR3565BFS01 */
/* Read_Vout_register_address = <0x9A> for IR36021FS01/2 & IR3565BFS01 */
/* Determine Optimal voltage from Fuse Register */
Optimum_Voltage = Read (FUSESR_register[4:8])
/* Send voltage command to Regulator & Check correct voltage */
Send_I2C (voltage_Regulator_I2C_Address, set_voltage_register_address, Optimum_Voltage)
Check Read_I2C(voltage_Regulator_Address, read_Vout_register_address) = Optimum_Voltage

Click to Contact IR for upcoming

SDK code for Freescale QorIQ

DESIGN CHECK

Does the core voltage meet the < 3% accuracy specifications about the optimum voltage after
the VID setting?

Parameter	IR3565BMFS01TRP	IR36021MFS01TRP	IR36021MFS02TRP
Application	T4xxx (CORE + DDR)	T2XXX/T1XXX (CORE + DDR)	T2XXX/T1xxx (CORE Only)
Loop Configuration	4+2	2+1	2+0
VCORE/DDR Boot Voltage(s) (REG DATA 0x17 / 0x18)	1.05V / 1.50V (0x6D / 0xFB)	1.035V / 1.35V (0x6A / 0xDD)	1.035V / *Disabled* *(0x6A / 0x00)*
BASE I2C / PMBus ADDR (Offset) FINAL I2C / PMBus ADDR	0x36 / 0x76 (Offset = +2) 0x38 / 0x78 / 0x79	0x36 / 0x76 (Offset = +2) 0x38 / 0x78 / 0x79	0x36 / 0x76 (Offset = +2) 0x38 / 0x78

Table 4: Programming addresses for Digital Controllers for VID for Core & DDR Voltages

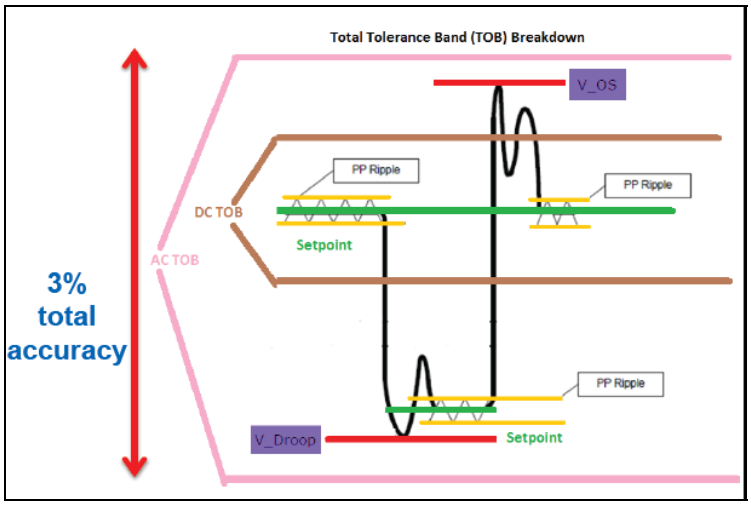


Figure 5: Understanding Core Voltage Requirements

Power Requirements - Core Voltage

To meet Freescale core voltage requirements, the total accuracy must be within 3% over DC, AC and ripple over the transient loads of the processor. Figure 5 shows the relationship of this requirement where both the DC and AC tolerance band must be within the 3% total accuracy for the core voltage of the QorIQ T Series processors. IR's Digital controllers set "VID" in the center of the DC TOB via I2C by reading the T Series EFUSE data. The set point must be centered to account for DC, AC and Output ripple tolerance of the power design over the transient loads of the processor with the worst case excursions at V_os and V_Droop.
IR power solution is compliant and proven on the T Series Reference Designs to meeting the Voltage accuracy specifications. The power design was validated by Freescale over dynamic testing of the processor states using real-time Dhrystone code analysis (see Figure 9) for worst case loads over temperature.

Definitions

VID = Vout set point, settable via I2C / PMBus (5mV LSB).

Total TOB (Accuracy) = DC TOB + Vripple + AC TOB.

DC TOB = difference between VID & output voltage during constant DC load (DMM).

Vripple = Total dV across Vsen/Vrtn during constant DC load, constant VID (O-Scope).

AC TOB = Total dV across Vsen/Vrtn during max loadstep / transient (O-Scope).

V_Droop (Droop) = ABS MIN output voltage level during Load Step, referenced to VID.

V_os (Overshoot) = ABS MAX output voltage level during Load Release, referenced to VID.

Tos (Duration of Overshoot) = Total excursion time that output voltage is above the Total TOB limit.

The Power solutions of the reference designs are finely tuned to meet 3% accuracy without incurring extra cost and space. The Multiphase, Digital controllers have superior transient and accuracy capability due in part to the ability to easily nullify offsets and operate in non-linear modes. International Rectifier's digital controllers (IR3565BFS01, IR36021FS01/2) have been specially configured to meet the stringent accuracy requirements of the T-series applications. The key tuned digital controller parameters and passive component values that are required to meet 3% total accuracy are listed below in Table 5. The major considerations for accuracy are given in the design check listed below.

DESIGN CHECK

Below are some tips to meeting a sub-3% accuracy design.

Component Selection.

1. # of Phases – n
   The # of phases should be chosen for current handling capability, transient response and ripple requirements. The # phase should be minimized for cost. In the case of the Freescale specifications, the transient response and ripple requirements dictate the # of phases rather than the current handling capability. For example, the T4240 requires ~60A current handling capability which would typically only require a 3-phase solution. However the extremely tight transient and ripple requirements force a 4-phase solution to meet accuracy, without using excessive, costly output capacitance. A 4-phase design also improved accuracy current measuring accuracy for transient response. Table 6 list the recommend phases for the T4240 and T2080 processors for best transient response for maximum frequency of operation, up to 1.2GHz and 1.8GHz respectively. Again, see Table 5 for device vs. # phases and optimize externals (Inductors and Caps) recommended for best transient response.
2. Total Output Capacitance – Cout (uF)
   Adding output capacitance is an effective but costly method of meeting the transient and ripple requirements. The Freescale - IR reference designs have optimally balanced the phases vs. output capacitance.
3. Inductor Value – L (uH)
   Selecting the proper L value is a fine balance as lowering L value will help Undershoot but make Overshoot worse. The Freescale - IR reference designs have found the optimum value.
4. Switching Frequency – Fsw (kHz)
   Increasing Fsw will help undershoot response at the expense of efficiency. Eventually it becomes better to add an extra phase and lower the Fsw to meet the Freescale requirements without sacrificing efficiency.
5. Lower the ESL / ESR of the path from inductors to CPU Parasitic inductance and resistance contribute to undershoot and overshoot. Remove nonessential components (Sense resistor, load switches and other resistive elements) in the load path and add more Copper, VIAs, etc. A 4-phase design will be more effective that a 3- phase design in distributing & reducing parasitic ESL/ESR.

Processor	Frequency Benchmark	Core Voltage Max (W)	Recommended # Phases for Best Transient Response
T4240	1.5GHz - 1.6GHz	32W to 64W (core + SVDD)	4 Φ
T2080	1.2GHz to 1.8GHz	16W to 29W (core)	2 Φ

Table 6: Recommended Number Phases for Core Voltage after Dhrystone Code Test for T4 and T2 Processors for best transient response.

Pre-configured Parameter	IR3565BFS01MTRP	IR36021FS01MTRP	IR36021FS02MTRP
Loop 1 / Loop 2 Phases & Boot Voltages	4Φ VCORE & 2Φ DDR3 1.05V / 1.50V	2Φ VCORE & 1Φ DDR3-LV 1.025V / 1.35V	2Φ VCORE *(only)* 1.025V
Fsw & Cout Bulks (470uF 6mΩ SP) MLCCs (10uF 0603)	400kHz / 6,850uF 12 BULK + 112 MLCC	500kHz / 2,625uF 4 BULK + 82 MLCC	500kHz / 2,625uF 4 BULK + 82 MLCC
DIFF Remote Sense	Enabled *(both loops)*	Enabled *(both loops)*	Enabled
DIFF Current Sense (RC=L/DCR)	Rsen=2.40kΩ / Csen=0.22uF	Rsen=3.40kΩ / Csen=0.22uF	Rsen=3.40kΩ / Csen=0.22uF
NTC Temp Comp & Current Gain	Rcs=3.40kΩ / Rs1_s2=2.87kΩ Ccs=100pF / NTC = 10kΩ	Rcs=3.40kΩ / Rs1_s2=2.87kΩ Ccs=100pF / NTC = 10kΩ	Rcs=3.40kΩ / Rs1_s2=2.87kΩ Ccs=100pF / NTC = 10kΩ
Loadline setting for Current Sensing	Rll=1.00mΩ / BW=192kHz (AVP *disabled*)	Rll=1.00mΩ / BW=192kHz (AVP *disabled*)	Rll=1.00mΩ / BW=192kHz (AVP *disabled*)
Control Loop Tuning Parameters Proportional (P), Integrative (I), Differential (D), & (2) Low-Pass Filters (LPF1_2)	Kp, Ki, Kd = -20.6dB, -80.8dB, +12.0dB LPF1,2 = 242.6kHz, 652.1kHz	Kp, Ki, Kd = -19.2dB, -76.3dB, +16.9dB LPF1,2 = 242.6kHz, 798.9kHz	Kp, Ki, Kd = -19.2dB, -76.3dB, +16.9dB LPF1,2 = 242.6kHz, 798.9kHz

Table 5: Pre-set Parameters for IR Digital Controllers & Optimized Component Values (T4, T2 and T1 Processors)

Ease of Design – Digital Controller is Pre-Configured for Freescale Designs.
The Power solutions of the reference designs are finely tuned to meet 3% accuracy without incurring extra cost and space. The Multiphase, Digital controllers have superior transient and accuracy capability due in part to the ability to easily nullify offsets and operate in non-linear modes. International Rectifier's digital controllers (IR3565BFS01, IR36021FS01/2) have been specially configured to meet the stringent accuracy requirements of the T-series applications. The key tuned digital controller parameters and passive component values that are required to meet 3% total accuracy are listed below in Table 5. The major considerations for accuracy are given in the design check listed below. Follow the schematic and general layout guidelines and the component is set to meet the requirements. No programming is necessary.

Accuracy over Temperature
The accuracy is related to how well the current is sensed. This is largely dependent upon the current sense amplifier and the temperature matching of the inductor. IR's digital controllers control these parameters very carefully:
Each phase uses Low offset differential current sense amplifiers. The outputs of the amplifiers are summed together internally.

Total current offset is trimmed to better than 0.00036mV*(loadline/DCR) at the factory.

Individual channel offsets are captured digitally at startup and nulled for phase balance. An External RC network is used to set the loadline and bandwidth. An NTC thermistor in the feedback provides temperature compensation for the inductor winding.

One NTC is needed for each loop (core, DDR); a third NTC is used for to sense heat spots on the board for over-temperature protection. The IR3565 and IR36021 were tested on the Reference Designs by Freescale up to 1.6GHz at 105°C over maximum transients to operate properly for temperature compensation while meeting Freescale accuracy requirements. See also Design Layout recommendations for thermistors in the next section.

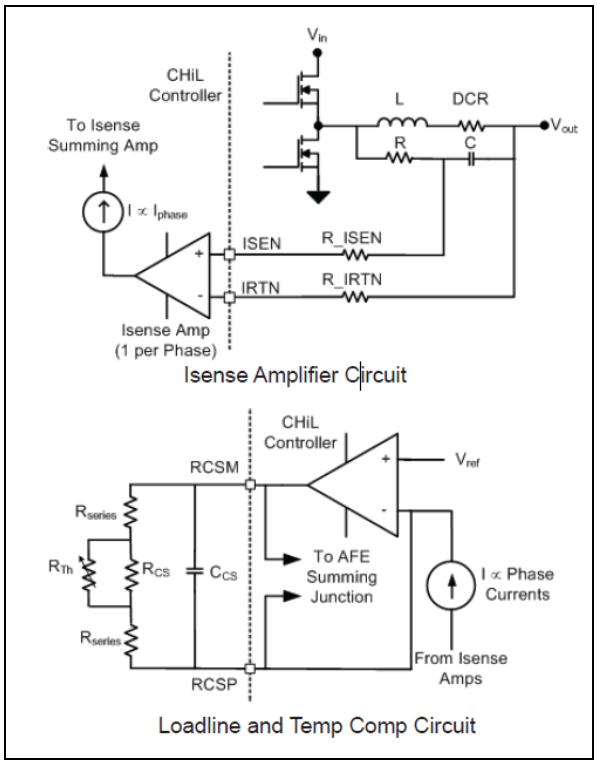


Figure 6: Integrated Voltage Regulator Circuits for Temperature Compensation in IR Digital Controllers

DESIGN CHECK

1) For accurate temperature compensation, place the NTC thermistor in the feedback loop next to the inductor winding.

2) For accurate over temperature protection, place the
OTP thermistor next to the PowIRStage MOSFETs.

Layout Design - Core Voltage

Layout is Critical to Meeting < 3% Accuracy. The IR controller parameters and the Freescale reference designs have been fully optimized for accuracy, thus the only remaining source of inaccuracy is in the layout. The Freescale reference has been verified for performance. The layout files can be obtained by click below (BRD files also available on IR site):

Click for IR-Freescale Layout Power Solution

Click to Download Freescale T4240 RDB Design

LAYOUT CHECK

The most critical considerations are below:

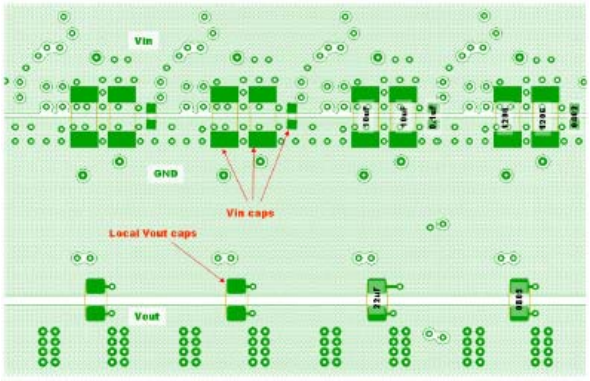


Figure 7a: Capacitor Placement of the input and out decoupling caps (4 phase design example)

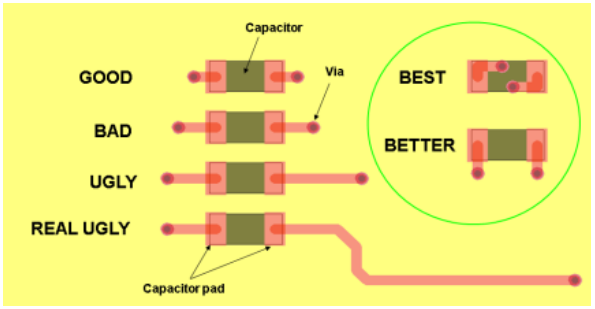


Figure 7b: Placement for decoupling caps as the placement affects the loop inductance

LAYOUT CHECK(continued)

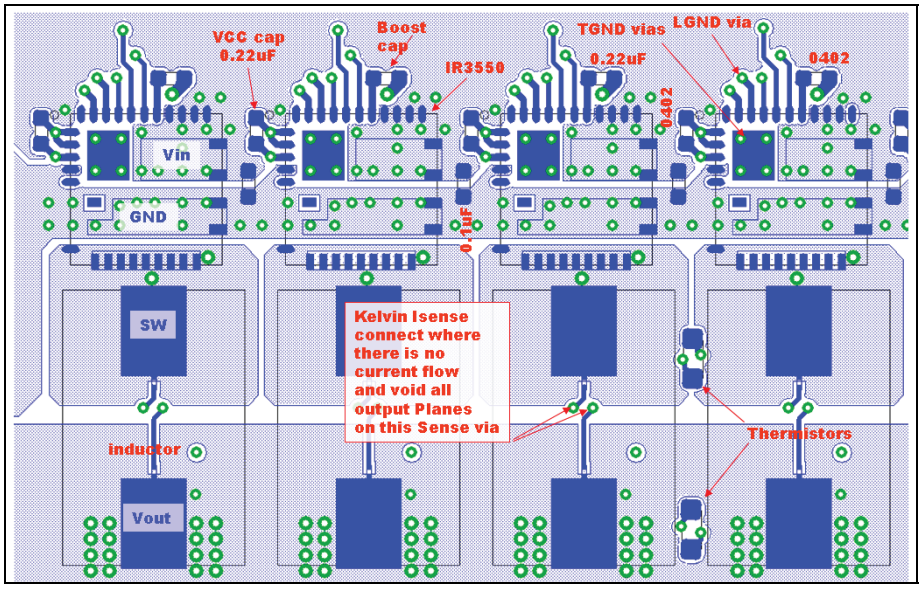


Figure 8a: Inductor, Thermistor, Gate Drive and Isense Placement Use Kelvin sense connections (for the DCR circuit) at points where there is no current flow

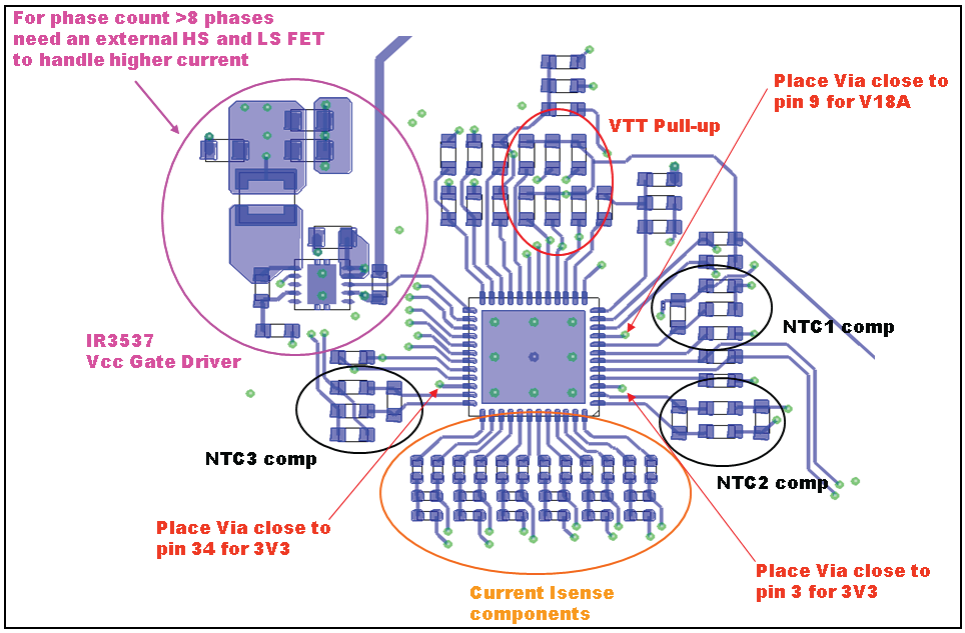


Figure 8b: Inductor, Thermistor, Gate Drive and Isense Placement. Recommended placement of small signal
components

.

Power Design Validation for Core Voltage

The best way to validate the design is to use Freescale's Dhrystone code test to emulate the end user load current profile. Figure 9a shows Freescale's example step load at 105°C. The step load varies with program activity on the processor. The worst case on T4240 is 20A for 23 virtual cores alternating between PH10/PH20 power saving state and L1-resident, intensive computation with AltiVec. IR solution was verified to pass all load transients and maintain core voltage accuracy to < ± 30mV. The data also points out indirectly the excellent transient performance of the regulator as the T4240 is changing the frequency of operations as the processor is transition from 550MHz to 1.1 GHz for optimum performance over heating conditions. Figure 9b shows for a 16A step load the core voltage accuracy and response of the IR3565B after it was set to the EFUSE stored optimal core voltage via VID. The remaining tight voltage margin (5mV and 0.4mV) showed that centering the core voltage for TOB was in fact necessary to meeting the core voltage requirements of VID ± 30mV.

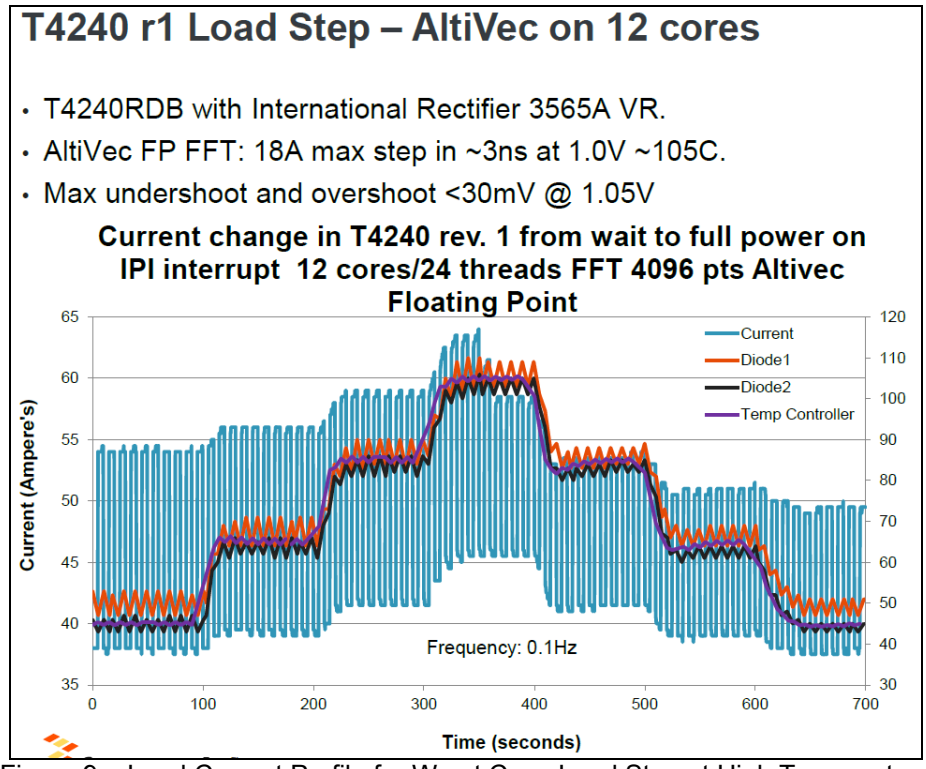


Figure 9a: Load Current Profile for Worst Case Load Step at High Temperature

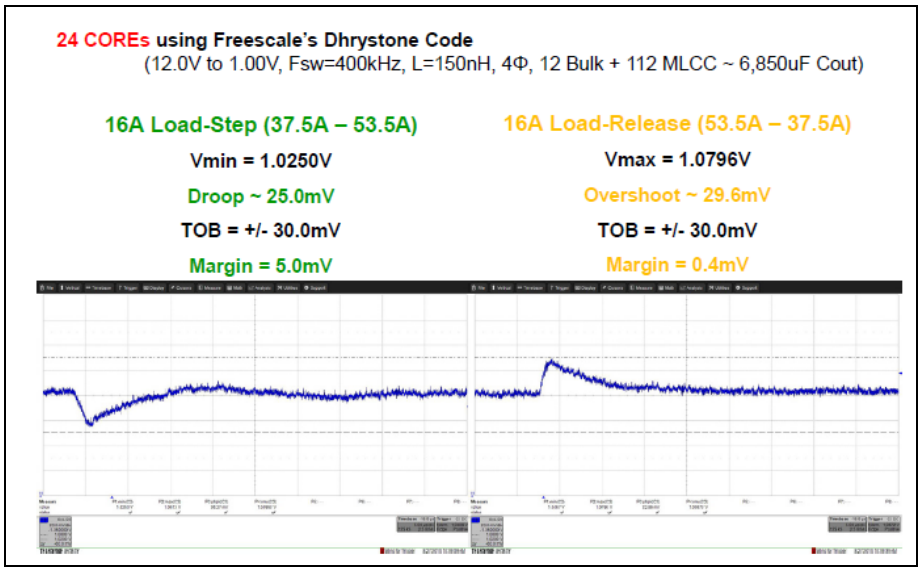


Figure 9b: Core Voltage Accuracy during Dhrystone Code Test for Load Step Response for Various Power Modes

DESIGN CHECK

The current steps vary vs. number of cores: 20 A for 12 cores (24 threads), 15A for 4 cores (8 threads) and 10A for 2 cores (4 threads) with a slew rate of 12 A/μs:

1) The core voltage must maintain the positive
transient power surges to less than VID+50 mV
over shoot.

2) Negative transient undershoot must comply with specification of VID-30mV.

Freescale's full analysis DC and AC analysis and summary of the Dhrystone code test using the IR3565 (IR36021) with the T4240 by varying 4 to 24 threads can be downloaded on the link below.

Click to Download Full DC & AC Analysis

Power Design Validation – Power Sequencing

The supplies must be powered up in the following order:

a. IO rails up first like 3.3V, 2.5V, 1.8V etc;
b. VDD (VCore), SVDD (1st SERDES voltage) and all the derivatives of these voltages via filters.,
c. GVDD/VTT/Vref (DDR), XVDD (2nd SERDES voltage).
d. PORESET_B, drive PROG_SFP = 1.89 V.

IR's Power Devices are sequenced using the PGOOD and Enables to avoid the extra cost of special power sequencing circuits. CPLD or FPGA can also be used to sequence the voltage rails.

See Freescale Reference Design for actual implementation of the power sequencing

Power Solution: QorIQ T Series

Click to Download Freescale

T4240 RDB Design

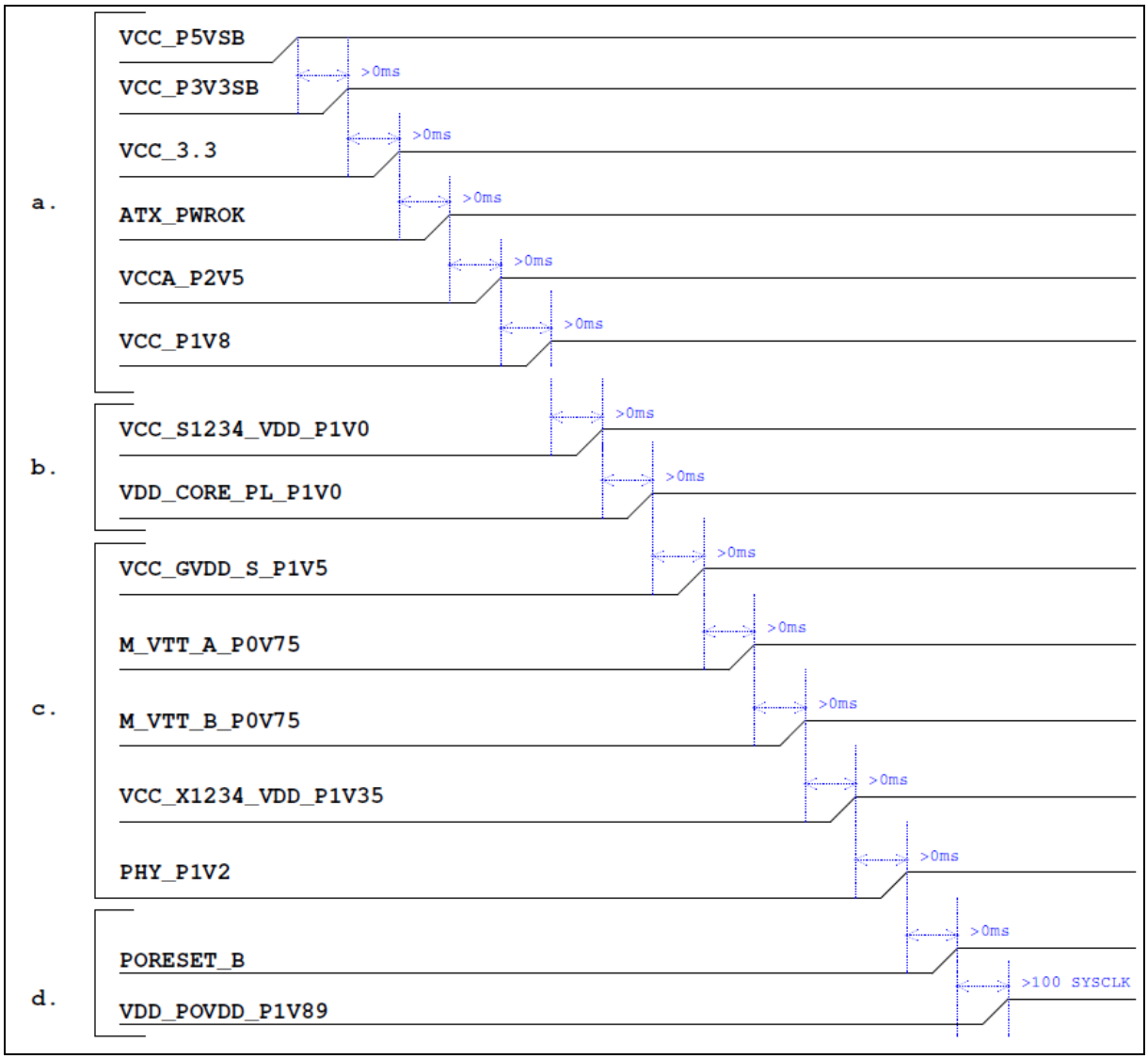


Figure 10: Power Sequencing - T4240

Click to Download Freescale

T4240 RDB Design

Power Requirements - System, Bus, Peripheral Voltage Rails

Shown to the right in Tables 7a/b/c are the IR POL (point of load) regulators used in each the reference designs for the T4240, T2080 and T1040. These voltage rails are organized by current level , output voltage, and voltage rail name. To optimize the design, common voltages from the system, bus, peripheral rails are combined and consolidated. A visual of these rails are shown earlier in the Power Map Diagrams. The POL regulators have been optimized and proven
in design with Freescale's ODM/IDH partners as well as in the reference designs: T4240RDB-PB, T2080RDB-PA (PCIe) and T1040RDB-PA.
For most of the voltage requirements, POL regulators with current handling capabilities from 4A to 10A were selected, namely IR3897 (4A), IR3473 (6A) and IR3475 (10A).
IR SupIRBuck® regulators were selected due to its lowest noise performance attributed to its low jitter regulator design. This along with recommended filters, good layout practice and good component selection provided best low noise performance in a practical implementation.
Although not all the rails will apply to every end application, IR provides many POL regulator options ranging from 3A to 25A to match most needs. See DESIGN OPTIONS. Schematics, layout board files and BOM is provided for each of the power rails from Freescale and International Rectifier and validated in actual designs. The most critical rail that requires the most attention to design are the SERDES rails of the T Series processors.

Processor	T4240	T4160	T4080
Reference Design	T4240RDB-PB		
IR3897 4A POL Regulator	6 @ IR3897: 1.89V - OVDD - Fuse 2.5V - DVCC (LVDD) - Enet, Bus, GPIO 1.8V - OVDD - eSPI, DMS, GPIO, Clocks, JTAG I/O, many more… 1.35V - X1234 - XnVDD - Serdes T4240 1.0V - S1234 - SnVDD - Serdes T4240 1.2V - PHY - Enet PHY		

Table 7a: POL DC DC for T4 Series

Click to Download Power Solution for T4240

Processor	T2080/81
Reference Design	T2080RDB-PA (PCIe)
IR3473 6A POL Regulator	8 @ IR3473: 3.3V - Processor, DDR3, 1G-Enet, JTAG, PLD, RTC, Many more… 2.5V - Enet, DMA, I2C, UART, 1G Enet, 10G Enet, SFP, CPLD, FAN, USB, Clocks, many. 1.2V - Enet (T4240), 10G Enet (T2080) 0.67V - 10G Enet 1.8V - VDD, USB, SPI, FUSE (T2080) 1.0V - 10G Enet 0.78V - 10G Enet 5V - SPF, RTC, JTAG, COP, PCI/SATA, CPLD, many more.
IR3475 10A POL Regulator	1 @ IR3475: 1.35V - DDR3, PLL, DDR(T2080), Serdes

Table 7b: POL DC DC for T2 Series

Click to Download Power Solution for T2080 RDB

Processor	T1040/T1042
Reference Design	T1040RDB-PA
IR3473 6A POL Regulator	4 @ IR3473: 2.5V - VDD, IRQ, Enet (T1040), 1G Enet, FAN, Flash, more more.. 1.5V - PCI 1.8V - Enet, Fuse, IFC, USB, PLL, OVDD 1.0V - 10G Enet, 1G Enet
IR3475 10A POL Regulator	2 @ IR3475: 3.3V - JTAG, PLL, DDR3, 1G Enet, SPF, USB, Flash, CPLD, many more… 1.35V - PLL, DDR (T1040), Serdes (XnVDD)

Table 7c: POL DC DC for T1 Series

Click to Download Power Solution for T1040 RDB

Power Requirements - SERDES Voltage Rails

Freescale's T Series has up to 36 SERDES lanes up to 10GHz. A special power design is required. For a low noise design IR's IR3897 was selected and implemented with special filters to meet low noise specification within the frequency band. IR's SupIRBuck Regulators provide wide range of PSRR and have very low noise and ripple. The solution can be used for 0.8V to 1.1V covering the range of the Freescale's SERDES supplies.

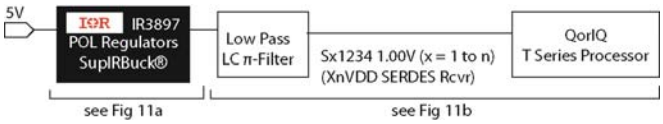
Note: The SERDES Voltage Supplies - SnVdd and XnVdd also denoted on Freescale's schematics as X1234 and S1234.

The challenges of the SERDES design according to Freescale:

- 40 dB per lane noise requirement.
- 10mv p-p maximum noise (50 kHz – 500 MHz) for the PLL and SVDD/XVDD power required

Hence this requires the use of independent filters and dedicated power supplies to reduce fundamental and cross conducted noise. Filters were chosen to reduce droop and reduce crosstalk noise.

Ultra-low noise voltage regulator design for SERDES Supplies is shown in Figure 11a and 11b (2nd Stage High Frequency Noise Filter).



For under 20MHz, the harmonics from the regulator are filtered by the main power inductor. To eliminate the higher frequency components a second stage filter (bead and small ceramic capacitors) is required. This filter addresses the switching noise created by the power FETs at >50MHz. The filter is a Low-Pass LC Pi-Filter topology that was verified by IR and Freescale on the reference designs with the T Series SERDES rails for the T4240 and T2080. To obtain the needed filter performance, implement the filter components exactly as shown in Figure 11b.

DESIGN CHECK

The input Power Noise Specification for the SERDES Rails:

Absolute peak ripple/noise should not exceed 10mV
when measured from 50kHz to 500MHz.

Download T4240 Design (see IR3897)

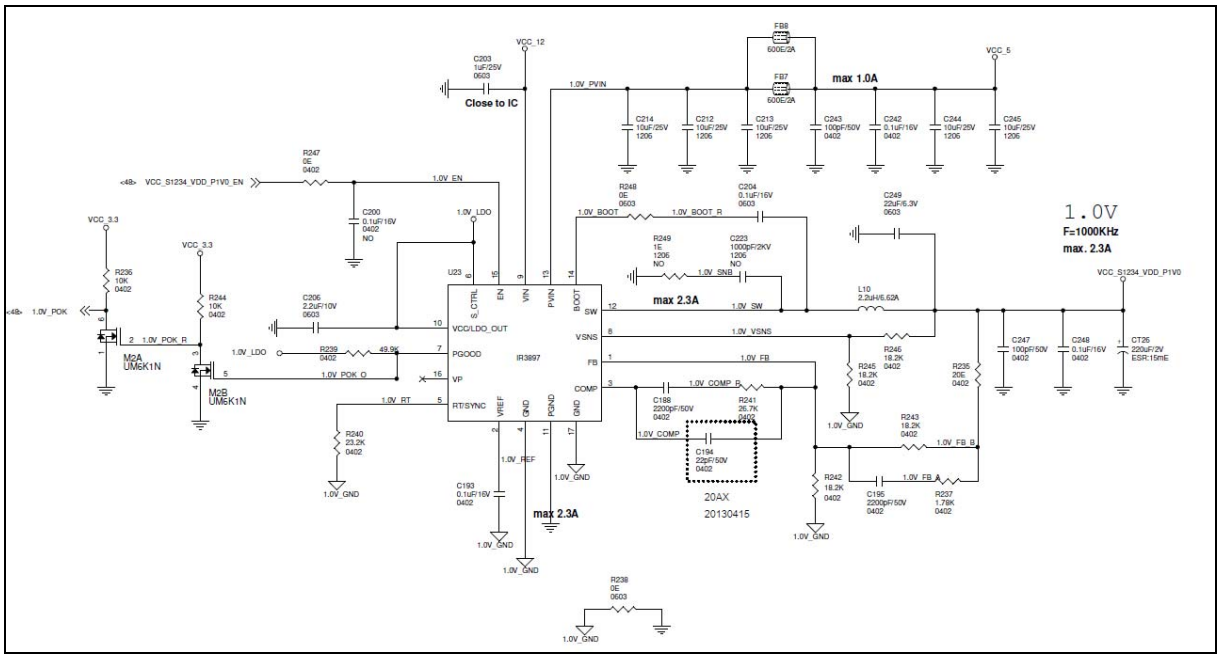


Figure 11a: Ultralow Noise Regulator Design for the SERDES Rails Using IR3897

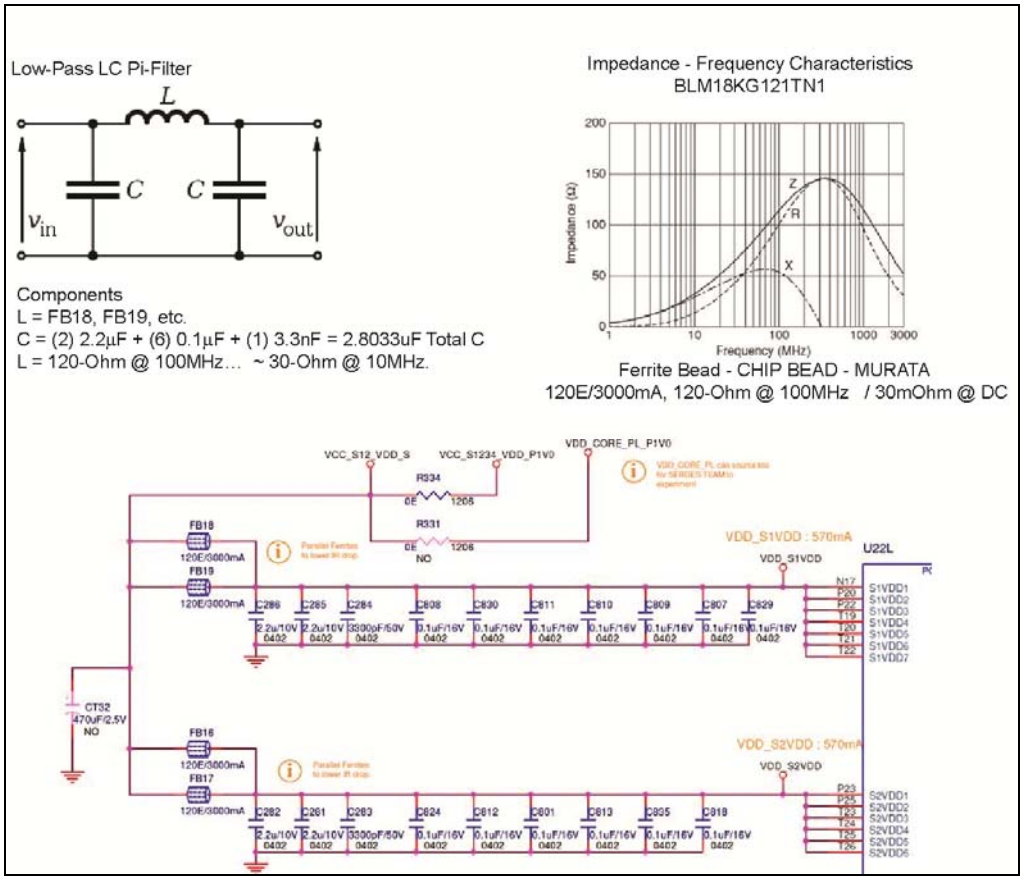


Figure 11b: Second Stage High Frequency Noise Filter from IR3897 to T Series SERDES Rails (shown above T4240 SVDD / XVDD Power Rails)

	Processor	T4240	T4160	T4080	T2080/81	T1040/T1042	T1023/24
	Reference Design	T4240RDB-PB			T2080RDB-PA (PCIe)	T1040RDB-PA	T1024RDB, Release tba
Thermal Power (65°C to 105°C)		42 to 54W	35 to 46W	29 to 38W	9 to 28W	4 to 8W	4 to 6W
Voltage Regulator Solution	Core + DDR Rails	IR3565B + IR3550 (6)	IR3565B + IR3550 (6)	IR3565B + IR3550 (6) Note: IR3550 can be replace with lower current IR3553*	IR36021 + IR3550 (2) Note: IR3550 can be replace with lower current IR3553*	IR36021 + IR3550 (2) Note: IR3550 can be replace with lower current IR3553* or IR3742*	IR3475
	System, Bus, Peripheral, Serdes Rails	IR3897 (6)	IR3897 (6)	IR3897 (6)	IR3473 (8) IR3475 (1)	IR3473 (4) IR3475 (2)	IR3473 (6) IR3475 (2)

* Changes in PowIRStage® may require external component adjustment.

Table 8: Power Solutions Options for Various T Series. The thermal power of the processors changes from 4W to 64W, from 4 to 24 threads. IR offers a scalable design with device options.

Design Options for Scalability

IR's Solution has been verified on reference designs in end applications in the T4240 reference design. The solution can also be used for T2080 designs.
Table 8 above shows the various power solutions for T4, T2 and T1 QorIQ processors ranging from ~64W to 4W (24 to 4 threads) on the core voltage. Note that along with the core voltage, DDR, system, bus I/O, and SERDES rails are required for the T Series processor, fabric communication chipsets and other peripheral ICs for the Freescale reference designs.
To allow for design flexibility and optimization of performance and cost for the core voltage and DDR rails, IR deployed the use of Digital Multi-phase Controllers to meet the fast transient requirements for the various cores of the T Series processors. This allows for scalability at the power MOSFET stage for optimizing design with minimal re-design effort (e.g. T4240 can be easily scaled down for the T4160 and T4080). Some adjustment maybe needed on the configuration register and inductor selection, especially between a 4-phase to 3-phase design. For the T2080, a 2-phase design is recommended
for fast transients. See Table 6 presented early in this document. For system and peripheral rails, IR uses the SupIRBuck POL regulators with integrated FETs to minimize cost with best performance for low noise. Some of these rails are critical for the T Series processor (i.e. SERDES rails). Other rails can be optional depending on the external communication fabric ICs implemented. In most cases, the common voltages were combined to optimize cost using the POL regulators as shown earlier.

Scaling the Phases for Optimum Design

The standard 4-phase reference design (T4240RDB) is guaranteed to meet maximum performance requirements specified by Freescale. For lower performance designs (e.g. less threads, lower frequency), it may be possible to reduce the number to 3-phases and would require the following adjustments:

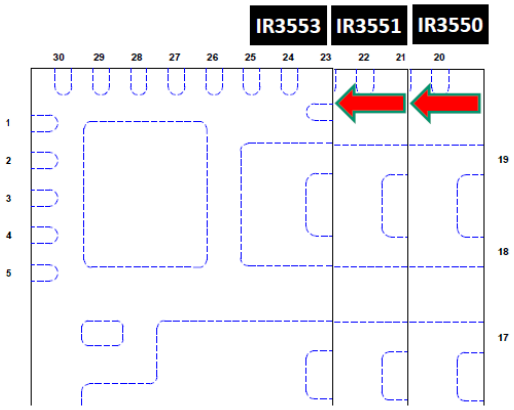
- Configuration Register (1) to enable only 3 MOSFETs
- Adjust the value of the Inductor
- Check and adjust capacitance as necessary

DESIGN CHECK

Confirm the number of phases is adequate to meet Freescale's overshoot, undershoot and ripple specifications.

Scaling the PowIRStages® for Optimum Design

As an alternative to or in addition to scaling the number of phases, IR allows for flexibility to scale the power MOSFET stages of the Multi-phase design. According to the Freescale specifications, T4240 requires at least 63A for worst case excursions at 105°C. The T4240 reference design solution with externals is shown (Figure 13) in a space of 50mm by 30mm using four IR3550 PowIRStage® devices (6mm x 6mm) to meet the Freecale transient (AC, ripple) specifications. For the T4160 and T4080, the PowIRStage® devices can be scaled to the smaller IR3551 (5mm x 6mm) or IR3553 (4mm x 6 mm) for lower current ratings. Note that the pinouts of the IR3551 and the IR3553 fit within the footprint of the IR3550 (Figure 12) allowing for simple component change and no power line trace movement. The same concept can be applied to the second output of the IR3565B for the DDR rail (Figure 14). The regulator for this rail is in a space of 30mm x 25mm including all external components. Note in both cases, some adjustments may be needed on the inductors and capacitors if smaller power MOSFETs are used for best optimization of performance. The schematics and board file are available on both IR and Freescale sites for download.



Part Number	Current Rating	Package	
IR3550	60A	PQFN 6x6	Footprint Compatible
IR3551	50A	PQFN 5X6	
IR3553	40A	PQFN 4x6	
IR3742	20A	PWFN5x6	

Figure 12: IR PowIRStage® MOSFETs allow footprint compatible options for optimum design from 20A to 60A.

Scaling the SupIRBuck® for Optimum Design

Adjacently displayed (Figure 16 to 18) are the board space dimensions of the POL regulators including external components for several of the voltage rails of the T4240 designs. These rails were tested to 105°C along with Freescale processor over Dhrystone code testing on the T4240RDB reference design. Figure 16 shows the critical low noise SERDES rails and the OVDD rail of the T4240 in a space of 28mm x 65mm. The other two (Figure 17 & 18) show the LVDD and PHY rail for the 1G Ethernet device in a $20mm^2$ & $16mm^2$ space.

On the T4240, all of the above POL rails use the IR3897 (4A) Integrated FET Regulators. If more current is required, for example, the IR3897 (4A) can be scaled to an IR3898 (6A) or IR3899 (9A) which are both 4mm x 5mm regulators without changing the footprint and pinout.

For even lower current and tighter form-factor designs, a IR3897 (6A) in 4mm x 5mm can be reduced to a IR3823 (3A) in 3.5 mm x 3.5mm footprint with small change to signal rail placement since the pinouts are the similar. Figure 15 shows the scaling options. For extremely compact designs, IR also offers dual output POL regulators, the IR3891 (2@4A) and IR3892 (2@6A).

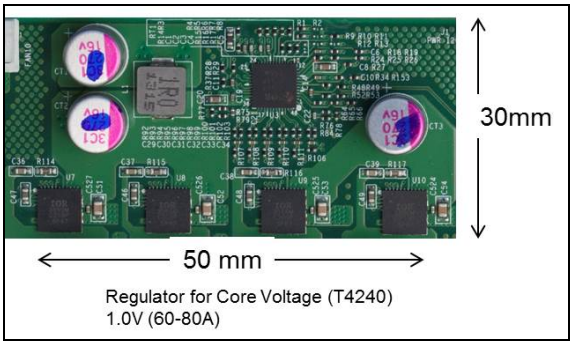


Figure 13: IR 4F Digital Controller + PowIRStage® MOSFET for Core Voltage

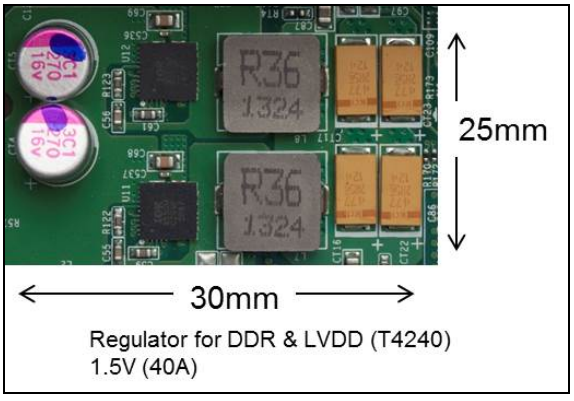
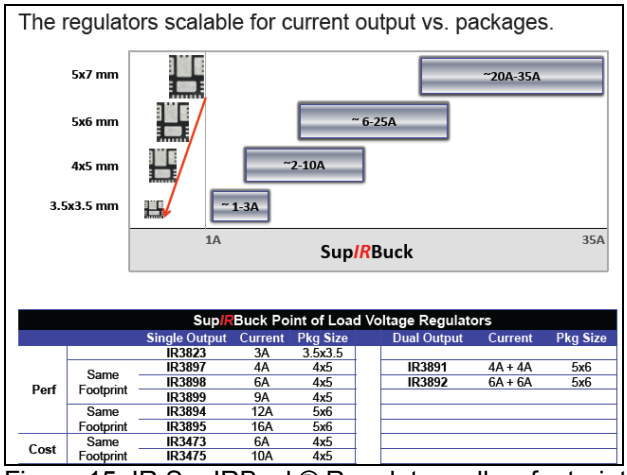


Figure 14: IR 2F Digital Controller + PowIRStage® MOSFET for DDR Voltage

Design Options for Scalability



SupIRBuck Point of Load Voltage Regulators

		Single Output	Current	Pkg Size	Dual Output	Current	Pkg Size
Perf	Same Footprint	IR3823	3A	3.5x3.5			
		IR3897	4A	4x5	IR3891	4A + 4A	5x6
		IR3898	6A	4x5	IR3892	6A + 6A	5x6
		IR3899	9A	4x5			
	Same Footprint	IR3894	12A	5x6			
		IR3895	16A	5x6			
Cost	Same Footprint	IR3473	6A	4x5			
		IR3475	10A	4x5			

Figure 15: IR SupIRBuck® Regulators allow footprint compatible options for optimum design from 2A to 16A.

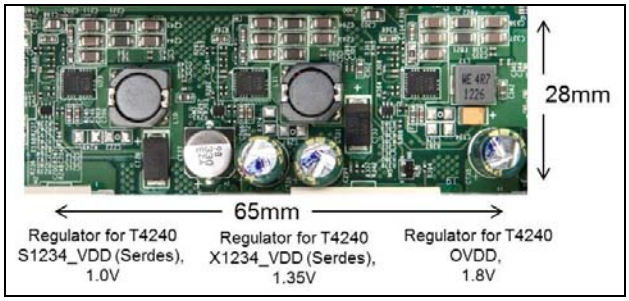


Figure 16: IR SupIRBuck® Regulators for Freescale. Low noise SERDES and Platform Voltage Rails on T4240RDB reference design.

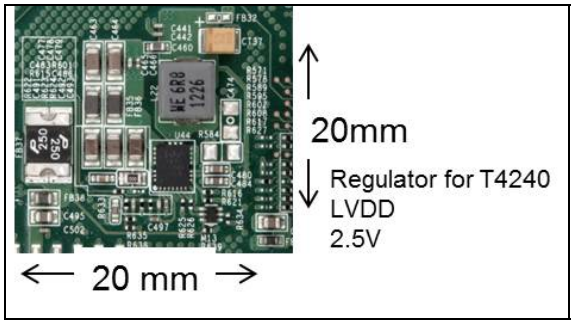


Figure 17: IR SupIRBuck® Regulators for Freescale. Platform Voltage Rails on T4240RDB reference design.

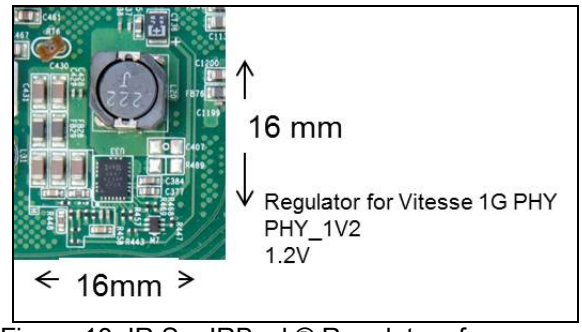


Figure 18: IR SupIRBuck® Regulators for Freescale. Platform Voltage Rails on T4240RDB reference design

Device Highlights & Ordering Information

Multi-Phase Digital Controllers

IR is leader in Multi-phase Digital Controllers.
IR offers pre-programmed options specifically for Freescale's T Series Controllers for both the core + memory voltage rails. The IR3565B is used for the T4 series (Table 9). IR offers unprogrammed Digital Controllers (IR3565BMTRP, IR36021MTRP) for general use. However for ease design for Freescale T Series applications, IR provides specially configured part variants, FS01 & FS02 (Table 9). All of these controllers are proven on Freescale's reference designs and ODM/IDH partner designs.



Superior transient and accuracy capability
Easily nullify offsets and operate in non-linear modes.
Scalable, high current, multiphase regulation.

- High density, High efficiency
- Telemetry delivering system voltages, currents, temperatures and faults
- Power Savings Modes

Processor	Multiphase Controller	Ordering Code	Description
T4240 / T4080 / T4160	IR3565B	IR3565BFS01MTRP	core + memory
T2080 / T2081 / T2085	IR36021	IR36021FS01MTRP	core + memory
T1040 / T2080 option	IR36021	IR36021FS02MTRP	core only

Table 9: IR Digital Controllers for QorIQ T Series

PowIRStages® - FETs

The power MOSFET devices (Table 10) are used on the Freescale designs. The T4240 uses the IR3550 with the option to use the IR3553 to scale to lower power with minimal design change (see DESIGN OPTIONS).



Core Voltage Rail: Scale the PowIRstage

PowIRStage	Current Rating	Ordering Code (for small qty see datasheet)
IR3550	60A	IR3550MTRPBF
IR3551	50A	IR3551MTRPBF
IR3553	40A	IR3553MTRPBF
IR3742	20A	IR3742MTRPBF

Table 10: IR PowIRStage® for QorIQ T Series

- Driver & FETs in one package for highest density,
- Exceptionally high current handling with very low thermal operation
- Scalable solution for higher or lower current

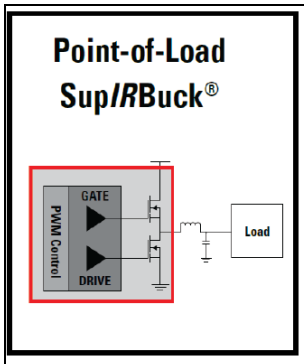
SupIRBuck® POL Regulators

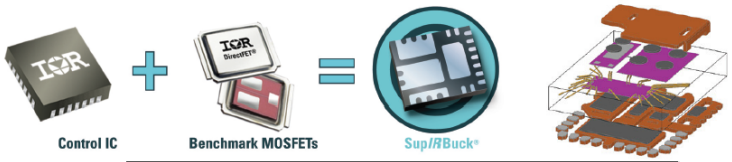
The POL regulators are shown below in Table 11. IR POL regulators are the best in the industry with proven reliability to extended industrial temperature range. The IR3897 (4A), IR3473 (6A) and IR3475 (10A) are used in the T4, T2 & T1 Freescale designs.
See also DESIGN OPTIONS for alternatives. Schematics and board files available by both Freescale and IR.

Click Here for SupIRBuck® Design Tool

For other proven POL voltage rails from 0.6V to 5V (3A to 35A) including schematics, layout, performance data, Simplis & Icepak (Thermal Models). See Design Library below.

Click Here for SupIRBuck Design Library





- Very low noise with best-in-class low jitter
- High (<0.5%) native accuracy
- Scalable portfolio of efficient devices

SupIRBuck Regulator	QorIQ	Description (for small qty see datasheet)
IR3897MTRPBF	T4	4A POL Regulator
IR3473MTRPBF	T2, T1	6A POL Regulator
IR3475MTRPBF	T2, T1	10A POL Regulator
IR3891MTRPBF	option for T4,T2,T1	Dual 4A-4A POL Regulator
IR3892MTRPBF	option for T4,T2,T1	Dual 6A-6A POL Regulator
IR3898/9/4/5-MTRPBF	option for T4,T2,T1	6A/9A/12A/15A POL Regulators

Table 11: IR SupIRBuck® Regulators for QorIQ T Series

Other

IRLML6346 - Super Logic Level device used for power control
IRFH6200 - Low Rds ON (0.89mOhm) for low power sleep