Application Note AN-1173

Power Factor Correction using the IRS2500

By Peter B. Green

Table of Contents

	Page
1. Introduction	2
2. Power Factor and THD	3
3. PFC Boost Pre-regulator	5
4. Design Equations	11
5. Factors affecting PF and THD	12
6. PCB Layout Considerations	14
7. Example Schematic	15
8. Bill of Materials	16
9. Test Results	17
10. Replacing Alternative Controllers	19

Safety Warning!

The IRS2500 based power factor correction pre-regulator is based on a non-isolated Boost SMPS circuit topology. The output typically ranges from 400 to 500VDC. When operating the output produces potentially dangerous voltages!The IRS2500 and associated circuitry should be handled by qualified electrical engineers only!

IRS2500 PFC Pre-regulator

1. Introduction

Many offline applications require power factor correction circuitry in order to minimize transmission line losses and stress on electrical generators and transformers created by high harmonic content and phase shift. Appliances often incorporate switching power supplies (SMPS) which include capacitive filter circuitry followed by a bridge rectifier and bulk capacitor supplying a load.
Without power factor correction circuitry a SMPS draws a high peak current close to the line voltage peak and almost no current over much of the cycle, resulting in a power factor of around 0.5 and a high total harmonic distortion.
Power factor correction circuitry is added which enables the appliance to draw a sinusoidal current from the AC line with negligible phase shift and very low harmonic distortion. This allows optimization of the load seen by the power grid such that power can be supplied without creating additional conductive losses in transmission lines or additional burden on transformers and generators. Costs to electricity providers are therefore reduced, which are hopefully passed on to the consumer.
Although not explicitly specified in standards such as IEC 61000-3-2 relating to power factor and line current harmonics, it is generally a requirement for the total harmonic distortion (THD) of the line input current supplying a PFC pre-regulator to be as low as possible. As is normally the case a tradeoff exists between cost and performance where more expensive high end products rated at higher power typically incorporate active power factor correction circuits, while low cost passive circuits often suffice in cheaper consumer products.
This is a market trend in power supplies used in a variety of appliances as well as electronic lighting ballasts for Fluorescent, high intensity discharge (HID) lamps and LED lighting.
For a product incorporating active power factor correction a THD of less than 20% over a wide input voltage range, normally 100VAC to 305VAC is expected. In many cases THD can be less than 10% over much or all of this voltage range.

Important Safety Information

The IRS2500 based PFCpre-regulator does not provide galvanic isolation of the output from the line input. Therefore if the system is supplied directly from a non-isolated input, an electrical shock hazard exists.The DC output voltage is highenough to produce a potentially lethal electrical shock!
It is recommended that for laboratory evaluation that the IRS2500PFC board be used with an isolated AC or DC input supply. The IRS2500 series Boost topology is suitable only for front end applications where isolation is either not necessary or provided elsewhere in the system.

2. Power Factor and THD

THD is the RMS of harmonic distortion from all components of an AC signal excluding the fundamental, expressed as a percentage of the RMS of the fundamental. In other words it quantifies the amount by which the signal deviates from a pure sinusoid.

$$THD = \frac{\sqrt{\sum_{n=2}^{\infty} An^2}}{A_1} = \frac{\sqrt{(A_{RMS} - A_1^2}}{A_1}$$

where, A_1 is the RMS amplitude of the fundamental and A_{RMS} is the total RMS value of the complete signal.
It should be noted that THD is not directly related to power factor (PF) since phase shift between current and voltage inputs are not factored into the THD calculation. Power factor is defined as the ratio of the *real power*, which is utilized by the load, to the *apparent power* which also includes energy stored in the load and returned to the source as well as current harmonics created by non-resistive loads. In an off line AC system real power is derived from the voltage and the fundamental component of the current only as a function of the phase shift between them. Distortion power is derived from all other harmonics of the current.

It is therefore possible for a circuit to obtain a very low THD without a high power factor if a phase shift exists. The European standard IEC 61000-3-2 class C limits (applicable to lighting ballasts rated above 25W) specifies maximum allowable levels for individual odd harmonics up to the 39th. A THD of less than 10% will normally provide compliance to these limits.

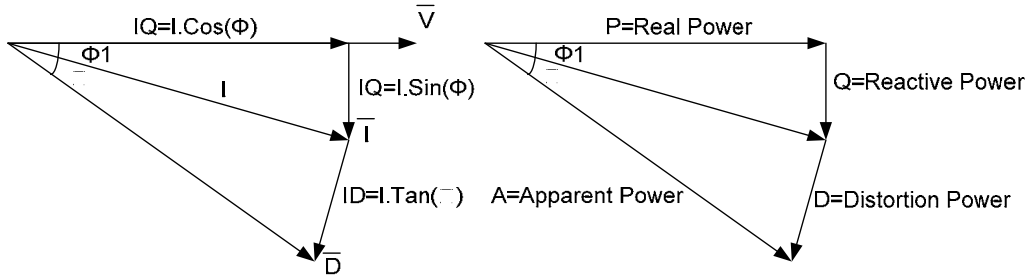


Figure 1. Power Vector Diagram

A general formula for power factor is:

$$PF = \frac{P_{RMS}}{V_{RMS} \cdot I_{RMS}}$$

where P_{RMS} is the real power consumed by the load.

The *displacement power factor* is given the formula:

$$PF = COS(\phi)$$

where Φ is the phase shift between the voltage and sinusoidal current.

The following formula gives the *distortion power factor*:

$$DF = \frac{1}{\sqrt{1 + THD^2}}$$

The following formula combines these to give the total power factor:

$$PF = \frac{COS(\phi_1)}{\sqrt{1 + THD^2}}$$

where Φ_1 refers to the phase shift between the voltage and the fundamental component of the current and THD is expressed as a fraction.

3. PFC Boost Pre-regulator

Figure 1 shows the schematic for a PFC pre-regulator based on a critical conduction mode Boost circuit. The IRS2500 pinout conforms to most industry standard power factor controllers and can be used as a drop in replacement for alternative parts in many applications.
The Boost PFC pre-regulator circuit consists of an EMI filter followed by a bridge rectifier which provides a full wave rectified voltage at the input to the Boost inductor LPFC. CIN provides an essential path for the circulating high frequency switching current. Both CF and CIN are critical to prevent excessive conducted emissions back onto the AC line, however CF produces a phase leading component of input current and CIN contributes to cross over distortion since it never fully discharges at the line zero crossing.
In critical conduction mode (also known as transition or boundary mode) the PWM gate drive signal to MPFC maintains a constant on time during the line cycle apart except where additional on time is added near the zero crossing and a variable off time. Each new cycle starts when the energy stored in LPFC has been fully transferred to the output.

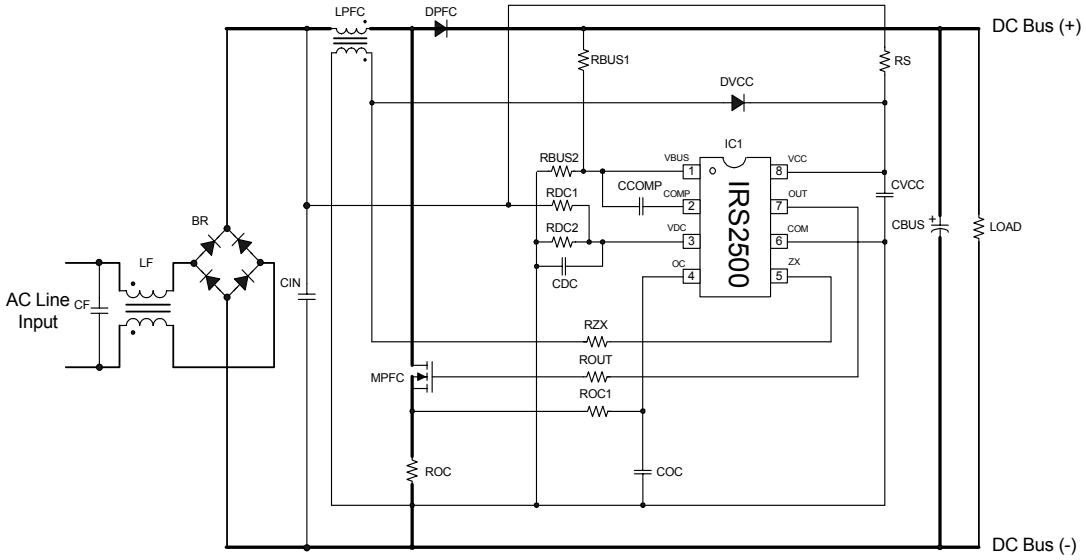


Figure 2: PFC Pre-regulator Schematic

The on and off times not taking into account the additional on time modulation can be calculated by the following formulae:

$$T_{ON} = \frac{L.I_{L(pk)}}{\sqrt{2}.V_{in(rms)}}$$

$$T_{OFF} = \frac{L.I_{L(pk)}.\sin\theta}{V_{out} - \sqrt{2}.V_{in(rms)}.\sin\theta}$$

A feedback loop regulates the output voltage by adjusting the PWM on time gradually over many line cycles so that the input current follows the shape of the input voltage and remains sinusoidal.
When the switch MPFC is turned on, the inductor LPFC is connected between the rectified line input (+) and (-) causing the current in LPFC to increase linearly. When MPFC is turned off, LPFC is connected between the rectified line input (+) and the DC bus capacitor CBUS through diode DPFC. The stored energy in LPFC is transferred to the output, supplying a current into CBUS. MPFC is turned on and off at a high frequency and the voltage on CBUS charges up to a specified voltage. The voltage feedback loop of the IRS2500 regulates the output to the desired voltage by continuously monitoring the DC output and adjusting the on-time of MPFC accordingly. If the output voltage is too high the on-time is decreased and if it is too low the on-time is increased. This negative feedback control loop operates with a slow loop speed and a low loop gain such that the average inductor current smoothly follows the low-frequency line input voltage to obtain high power factor and low THD.
The loop speed is intentionally slow with respect to the AC line frequency so that there is no appreciable change in the on time during a single line half cycle. This allows the current to follow shape of the sinusoidal voltage.

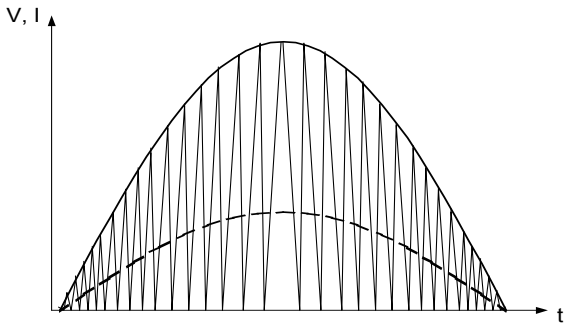


Figure 3: Sinusoidal line input voltage (solid line), triangular PFC Inductor current and smoothed sinusoidal line input current (dashed line) over one half-cycle of the AC line input voltage.

Corrections to the output voltage therefore require several line cycles. With a fixed on-time, and an off-time determined by the inductor current discharging to zero, the result is a system where the switching frequency is free-running and constantly changing from a high frequency near the zero crossing of the AC input line voltage, to a lower frequency at the peaks (Figure 3).

When the line input voltage is low (near the zero crossing), the inductor current will increase only a small amount and the discharge time will be short resulting in a high switching frequency. When the input line voltage is high (near the peak), theinductor current will charge up to a much higher level and the discharge time will be longer giving a lower switching frequency.

The PFC control circuit of the IRS2500 (Figure 4) includes six control pins: VBUS, COMP, ZX, OUT, VDC and OC. The VBUS pin measures the DC bus voltage through an external resistor voltage divider. The COMP pin voltage determines the on-time of MPFC and sets the feedback loop response speed with an external RC integrator. The ZX pin detects when the inductor current discharges to zero each switching cycle using a secondary winding from the PFC inductor. The OUT pin is the low-side gate driver output for the external MOSFET, MPFC. The VDC pin senses the line input cycle providing phase information to control the on time modulation described in the next section. The OC pin senses the current flowing through MPFC and performs cycle-by-cycle over-current protection.

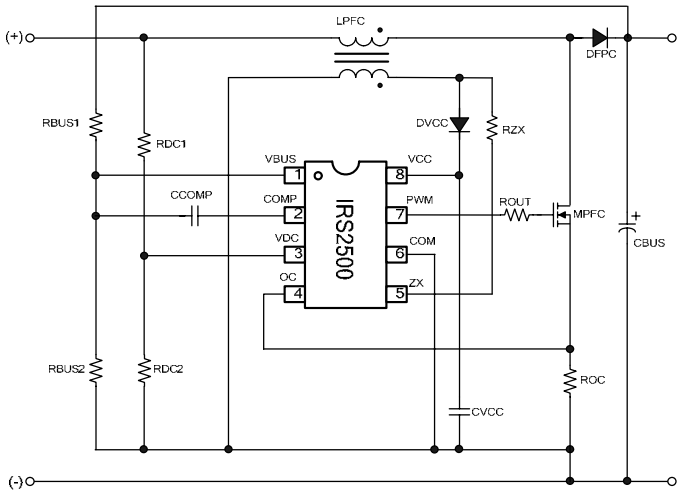


Figure 4: IRS2500 simplified PFC control circuit.

The VBUS pin is compared with a fixed internal 2.5V reference voltage for regulating the DC output voltage. The feedback loop error amplifier increases or decreases the COMP pin voltage. The resulting voltage on the COMP pin sets

the threshold for the charging of the internal timing capacitor shown in Figure 5 and therefore determines the on-time of MPFC.
The error amplifier operates at a slow loop speed preventing rapid changes in PWM duty cycle during a single input line cycle. This prevents distortion achieving high power factor and low THD.

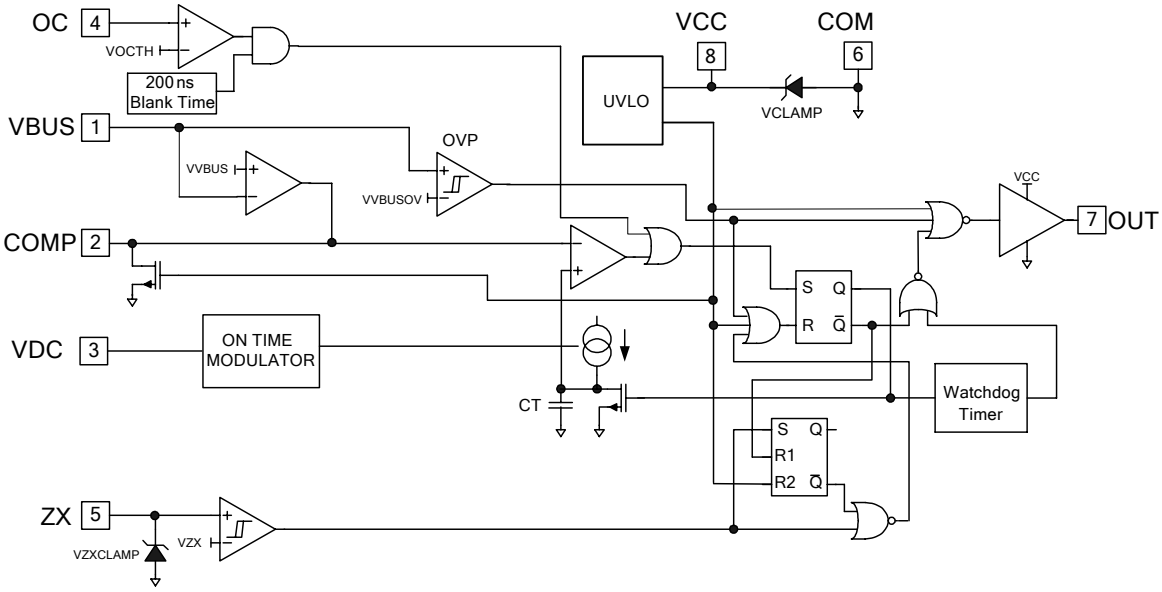


Figure 5: IRS2500 Internal Block Diagram.

The off-time of MPFC is determined by the time it takes the LPFC current to discharge to zero. The zero current level is detected by a secondary winding on LPFC that is connected to the ZX pin through an external current limiting resistor RZX. This winding normally has close to a 1:10 turns ratio relative to the main winding. A positive-going edge exceeding the internal threshold VZX+ signals the beginning of the off-time. A negative-going edge on the ZX pin falling below VZX- will occur when the LPFC current discharges to zero, which signals the end of the off-time and MPFC is turned on again (Figure 12). The ZX pin is internally biased to ensure that the voltage detected from the inductor drops fully to zero before triggering the next PWM cycle. A wide hysteresis prevents false triggering by ringing oscillations. The ZX pin current should not exceed 0.5mA as excessive current can cause incorrect triggering and possible damage to the IRS2500.
The cycle repeats itself indefinitely until the IRS2500 is disabled through an over-voltage condition on the DC bus or if the negative transition of ZX pin voltage does not occur. Should the negative edge on the ZX pin not occur, MPFC will remain off until the watch-dog timer forces a turn-on of MPFC for an on-time duration programmed by the voltage on the COMP pin. The watch-dog pulses occur every 300-400us (tW) indefinitely until a correct positive and negative-going signal is detected at the ZX pin and normal operation is resumed. Should the OC pin voltage exceed the VOCTH over-current threshold during the on-time

the gate drive output will turn off. The circuit will then wait for a negative-going transition on the ZX pin or a forced turn-on from the watch-dog timer to turn the output on again.

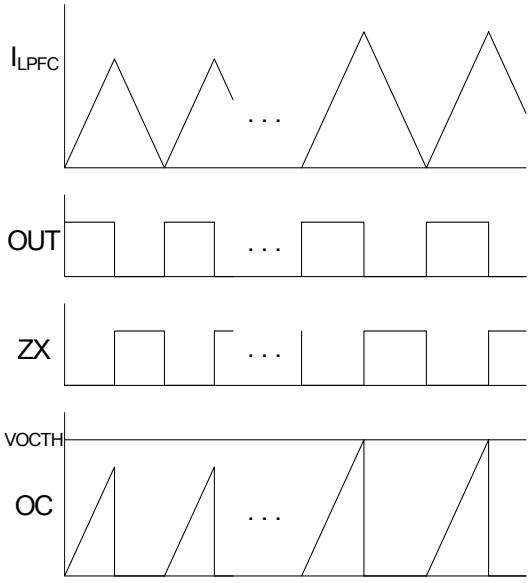


Figure 6: Inductor current, OUT pin, ZX pin and OC pin timing diagram.

A fixed on-time of MPFC over an entire cycle of the line input voltage produces a peak inductor current which naturally follows the sinusoidal shape of the line input voltage. The smoothed, averaged line input current is in phase with the line input voltage for high power factor but a high total harmonic distortion (THD), as well as individual higher harmonics of the current are still possible. This is mostly due to cross-over distortion of the line current near the zero-crossings of the line input voltage. To achieve low harmonics that are acceptable for compliance with international standards and general market requirements, an additional on-time modulation circuit has been added to the PFC control. This circuitdynamically increases the on-time of MPFC as the line input voltage nears the zero-crossings (Figure 7). This causes the peak LPFC current, and therefore the smoothed line input current, to increase near the zero-crossings of the line input voltage. This reduces the amount of cross-over distortion in the line input current which reduces the THD and higher harmonics.
On time modulation is controlled by sensing the full wave rectified voltage at the bridge rectifier output through a resistor divider (RDC1, RDC2). This is scaled such that the peak voltage will be close to 1V at 120VAC and 3V at 265VAC. This function can be disabled by connecting a resistor from pin 3 to VCC in place of the input signal.

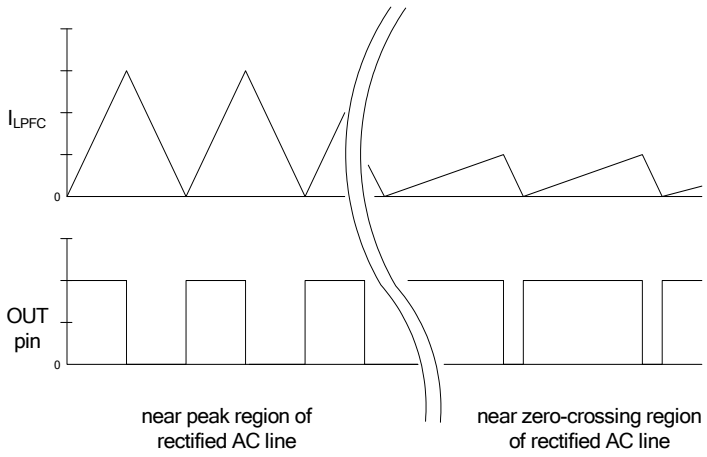


Figure 7: On-time modulation circuit timing diagram.

The IRS2500 incorporates both static and dynamic overvoltage protection. Static over voltage protection monitors the feedback voltage at the VBUS pin and disables the gate drive output if this voltage exceeds the target voltage by 8%. This is activated by an internal comparator set to detect a threshold of 2.7V, which is 8% above the regulation threshold of 2.5V.

However, under startup condition or when a load is removed from the output the error amplifier output voltage at the COMP pin swings low. Since the compensation capacitor CCOMP is connected from this output back to the VBUS input a current will flow during the COMP voltage transition. This pulls down the VBUS voltage, which allows the output voltage to exceed the desired regulation level during the transition and results in an overshoot before the voltage at the VBUS input exceeds the regulation threshold.

In order to compensate for this effect, the IRS2500 includes dynamic detection of the error amplifier output current. During a swing in the negative direction the error amplifier output current peaks at a much high level than the level during steady state operation. This higher current is internally detected and triggers the overvoltage protection circuitry disabling the PWM output until the error amplifier output has settled to a new level. This prevents the output voltage from overshooting the desired level by a significant amount under the transient conditions described. For this reason the loop should be designed such that voltage ripple at COMP is minimized during steady state operation.

4. Design Equations

Step1: CalculatePFC inductor value:

$$L_{PFC} = \frac{(VBUS - \sqrt{2} \cdot VAC_{MIN}) \cdot VAC_{MIN}^2 \cdot \eta}{2 \cdot f_{MIN} \cdot P_{OUT} \cdot VBUS}$$ [Henries]

where,

$VBUS$ = DC bus voltage
VAC_{MIN} = Minimum RMS AC input voltage
η = PFC efficiency (typically 0.95)
f_{MIN} = Minimum PFC switching frequency at minimum AC input voltage
P_{OUT} = Output power

Step 2: Calculate peak PFC inductor current:

$$i_{PK} = \frac{2 \cdot \sqrt{2} \cdot P_{OUT}}{VAC_{MIN} \cdot \eta}$$ [Amps Peak]

Note: The PFC inductor must not saturate at i_{PK} over the specified ballast operating temperature range. Proper core sizing and air-gapping should be considered in the inductor design.

Step 3: Calculate PFC over-current resistor ROC value:

$$R_{OC} = \frac{VOCTH}{i_{PK}}$$ where VOCTH = 1.1V [Ohms]

ROC power rating can be approximated:

$$PR_{OC} \geq \left(\frac{P_{OUT}}{VAC_{MIN} \cdot \eta} \right)^2 \times R_{OC}$$ [Watts]

Step 4: Calculate start-up resistor RVCC value:

$$R_{VCC} < \frac{VAC_{MIN}}{IQCCUV}$$ [Ohms]

$$PRV_{CC} > \frac{V_{ACMAX}^2}{R_{VCC}}$$ [Watts]

RVCC is often comprised of two series resistors (RBUS1A and RBUS1B) in order to withstand the high voltage.
In this case choose RVCC1 and RVCC2 to be the next preferred value down from RVCC/2 with power rating greater than PRVCC/2.

Step 5: Calculate VBUS feedback resistor divider network:

RBUS1 is often comprised of two series resistors (RBUS1A and RBUS1B) in order to withstand the high voltage.

Select an initial value of 10K for RBUS2

$$R_{BUS1} = (V_{BUS} - 2.5) \times \frac{10000}{2.5} \quad \text{[Ohms]}$$

$$R_{BUS1A} = R_{BUS1B} = \frac{R_{BUS1}}{2} \quad \text{[Ohms]}$$

Choose the nearest preferred value for RBUS1A and RBUS1B.
Then re-calculate RBUS2:

$$R_{BUS2} = \frac{2.5 \times (R_{BUS1A} + R_{BUS1B})}{V_{BUS} - 2.5} \quad \text{[Ohms]}$$

Then choose the nearest E96 1% tolerance value for RBUS2.

Step 6: Calculate VDC resistor divider network:

RDC1 is often comprised of two series resistors (RDC1A and RDC1B) in order to withstand the high voltage.

Select an initial value of 10K for RDC2

$$R_{DC1} = (\sqrt{2}.V_{ACMIN} - 1) \times 10000 \quad \text{[Ohms]}$$

Choose the nearest preferred value for RDC1A and RDC1B.

Then re-calculate RDC2:

$$R_{DC2} = \frac{R_{DC1A} + R_{DC1B}}{\sqrt{2}.V_{ACMIN} - 1} \quad \text{[Ohms]}$$

Then choose the nearest E96 1% tolerance value for RDC2.

Step 7: Calculate COMP capacitor:

CCOMP should be selected to roll off the gain of the error amplifier at approximately 20Hz.

$$C_{COMP} = \frac{1}{2\pi \times 20Hz \times R_{BUS2}} \quad \text{[Farads]}$$

Choose the nearest preferred value for CCOMP.

Step 8: Calculate RZX resistor:

Choose Izx as 0.5mA and assume ZX winding maximum voltage VZX of 20V at the ZX winding as an approximation. If the actual VZX is higher than 20V use the true value.

$$R_{ZX} \leq \frac{V_{ZX}}{I_{ZX}} \quad \text{[Ohms]}$$

Choose the next lowest preferred resistor value for RZX.

5. Factors affecting PF and THD

The PFC pre-regulator circuit described above draws a current from the line input which follows the shape of the voltage, however the following limitations exist:

1. Phase shift produced by CF.
The capacitance of CF draws current from the line input, which leads the voltage by 90º. The magnitude of this reactive current is dependent on the size of CF and the AC line input voltage. This is one reason why the power factor always drops as line input voltage increases. For this reason CF should be kept as small as possible while making sure the input filter is adequate for EMC compliance. This does not produce distortion and affects only the power factor.

2. Phase shift produced by CIN.
CIN also causes some phase shift since the voltage across it is full wave rectified.
This should also be kept to a minimum though it must be sufficient to provide a high frequency AC current source for the switching regulator. This is also essential for EMC compliance.

3. Cross over distortion produced by CIN.
CIN also contributes to cross over distortion while CF does not. The circuit can be considered as a resistive load and therefore it is clear that as the AC line input voltage passes through each zero crossing, CIN will need to discharge through the load. Depending on the magnitude of CIN and the load the voltage on CIN never discharges completely to zero at each zero crossing always maintaining a residual voltage. This problem becomes worse in systems where the load is variable such as a dimmable electronic lighting ballast. As the load is reduced the residual voltage on CIN increases.
Since the voltage at CIN does not reach zero, when the AC line input voltage drops below the minimum voltage at CIN there is no current drawn from the line input, which results in the characteristic dead band shown on the input current waveform in figure 7.
It should be noted that the bridge rectifier (BR) also contributes to the cross over distortion to a small extent due to the forward voltage drop of two series diodes that always appears between the AC line voltage and the rectified voltage, therefore there will always be some cross over distortion no matter how small CIN is.

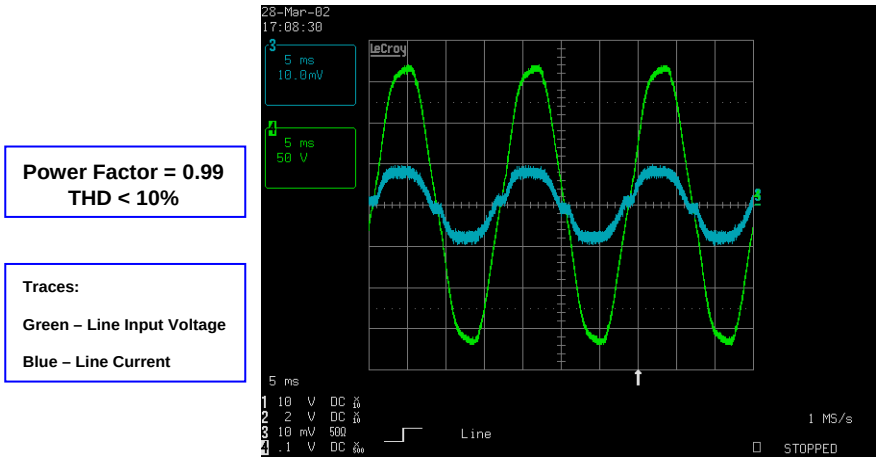


Figure 8: Line input and current in a typical PFC pre-regulator

4. Minimal energy transfer at the zero crossing.
At low line input voltage levels there may be insufficient energy stored in the Boost inductor LPFC to provide enough voltage at the drain of MPFC to forward bias the output diode DPFC. This is due to parasitic capacitances in the windings of LPFC as well as the drain to source capacitance of the MOSFET switch. This being the case it is necessary for the control IC to compensate for this by increasing the MOSFET on time when the voltage approaches zero in order to draw more current. Many PFC control ICs including the IRS2500 include circuitry that gradually increases the on time when the input voltage is close to a zero crossing. This functionality is referred to as *on time modulation.* The line input voltage is generally detected through the divided input signal provided at pin 3. It should be noted here that the residual voltage across CIN will be divided down through RDC1 and RDC2 so that it also appears at pin 3, which prevents the IC from detecting the input voltage below the level of the residual voltage. In order to limit this problem, the IRS2500 must produce sufficient on time modulation to discharge CIN as low as possible and introduce this before the residual voltage level is reached.

5. Ripple at the error amplifier output (COMP)
The output bus voltage from the PFC pre-regulator circuit will always contain some ripple at twice the line frequency, ΔV_{OUT} superimposed on top of the regulated DC output. The magnitude of ΔV_{OUT} depends on the magnitude of the

output storage capacitor CBUS. Since the output voltage is divided and fed back to the inverting input of the error amplifier, a component of ripple will also be fed to the input and compared with the internal 2.5V reference of the IRS2500. This may result in a component of ripple appearing at the error amplifier output (COMP) which determines the PWM on time. It is necessary for the compensation capacitor CCOMP to be large enough to roll off the error amplifier gain at a frequency well below twice the line frequency in order to eliminate this ripple as much as possible. Ripple at the COMP output results in modulation of the on time which causes distortion of the current waveform and should therefore be eliminated as far as possible.

6. Delay before next switching cycle

In critical conduction mode an auxiliary wining on the Boost inductor provides a signal to the ZX (zero crossing) pin of the controller. This indicates when all of the energy from the inductor has been transferred to the output by transitioning from high to low. When this transition is detected the PWM output drive goes high to start the next cycle, however if there is delay then the converter is actually operating in discontinuous mode due to the dead time. This can cause some distortions in the current waveform.

6. PCB Layout Considerations

For correct operation the following guidelines should be followed:

1. CVCC must be as close to IC1 as possible with short direct traces.
2. The feedback path should be kept to a minimum length and separated as much as possible from high frequency switching traces to minimize noise at the VBUS input.
3. The current sense filter components ROC and COC should be located close to the IRS2500 with short direct traces.
4. It is essential that all signal and power grounds should be kept separated from each other to prevent noise from entering the control environment. Signal and power grounds should be connected together at one point only, which must be at the COM pin of the IRS2500. The IRS2500 may not operate in a stable manner if these guidelines are not followed!
   All components associated with the IR2500 should be connected to the IC signal ground (COM) with the shortest path possible.
5. All traces carrying the load current need to be sized accordingly.
6. Gate drive traces should also be kept to a minimum length.

7. Example Schematic

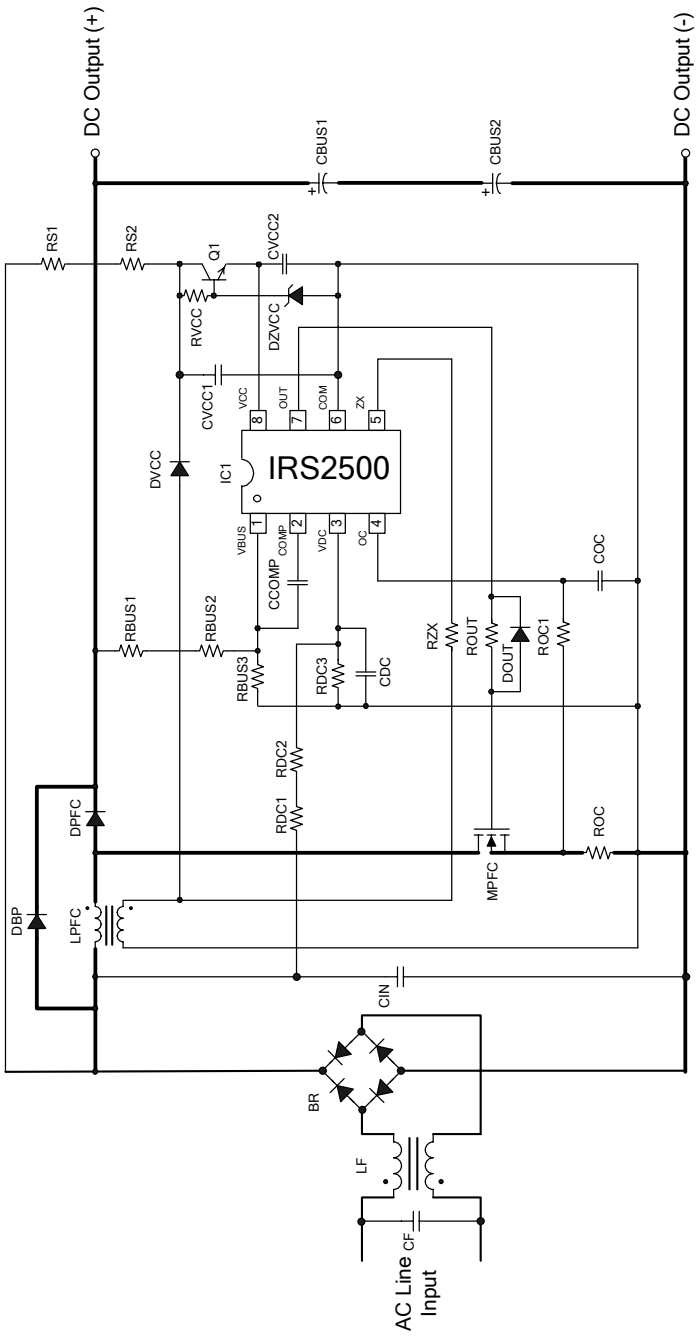


Figure 9: 80W PFC Schematic

8. Bill of Materials

Item	Description	Part #	Manufacturer	Qty	Reference
1	Diode, 75V, 150mA, MiniMELF	DL4148	Diodes Inc	2	DVCC, DOUT
2	Diode, 1000V, 1A	1N4007	Diodes Inc	1	DBP
3	20V, ZenerDiode, 500mW, MiniMELF	ZMM5250B-7	Diodes Inc	1	DZVCC
4	Diode, 600V, 3A, 250nS, SMB	RS3JB-13-F	Diodes Inc	1	DPFC
5	Bridge, 1000V, 1.5A, 4SDIP	DF10S	Fairchild	1	BR1
6	MOSFET, 650V, 0.38 Ohm, TO220	SPP11N60C3	Infineon	1	MPFC
7	NPN Transistor, SOT23, 40V	MMBT2222A-TP	Micro Com	1	Q1
8	IC, PFC Controller	IRS2500SPBF	International Rectifier	1	IC1
9	Inductor CM Line Filter, 250V,0.70A	ELF-15N007A	Panasonic	1	LF
10	Inductor, 520uH, 4.2Apk	SRW2620PQ-X22V102	TDK	1	LPFC
11	Capacitor, 0.10uF, 275VAC, X2/Y2,TH,.591”	ECQ-U2A104ML	Panasonic	1	CF
12	Capacitor, 0.10uF, 400VDC, 0.295”	MKS4-.1/400/10 PCM 7.5	Wima	1	CIN
13	Capacitor, 100uF, 250V			2	CBUS1, CBUS2
14	Capacitor, 1.0uF, 25V,X7R, 1206	C3216X7R1E105K	TDK	1	CCOMP
15	Capacitor, 10nF, 1206	12061C103K4T2A	AVX	1	CDC
16	Capacitor, 1nF, 50V, 1206	12065C102KAT2A	AVX	1	COC
17	Capacitor, 10µF, 50V, 1210	GRM32DF51H106ZA01L	Murata	1	CVCC1
18	Capacitor, 2.2uF, 25V, X7R, 1206	C3216X7R1E225K	TDK	1	CVCC2
19	Resistor, 0.33 Ohm, 0.5W, 2010	MCR50JZHFLR330	Rohm	1	ROC
20	Resistor, 470K, 5%, 1206	ERJ-8GEYJ474V	Panasonic	2	RDC1, RDC2
21	Resistor, 5.6K, 5%, 1206	ERJ-8GEYJ562V	Panasonic	1	RDC3
22	Resistor, 787K, 1%, 1206	ERJ-8SENF7873V	Panasonic	2	RBUS1, RBUS2
23	Resistor, 9.1K, 1%, 1206	ERJ-8ENF9101V	Panasonic	1	RBUS3
24	Resistor, 100K, 5%, 1206	ERJ-8GEYJ104V	Panasonic	2	RS1, RS2
25	Resistor, 18K, 5%, 1206	ERJ-8GEYJ183V	Panasonic	1	RZX
26	Resistor, 1.0K, 5%, 1206	ERJ-8GEYJ102V	Panasonic	1	ROC1
27	Resistor, 3.3K, 5%, 1206	ERJ-8GEYJ332V	Panasonic	1	RVCC
28	CONNECTOR, 2 POSITION			2	
29	PCB			1	

9. Test Results

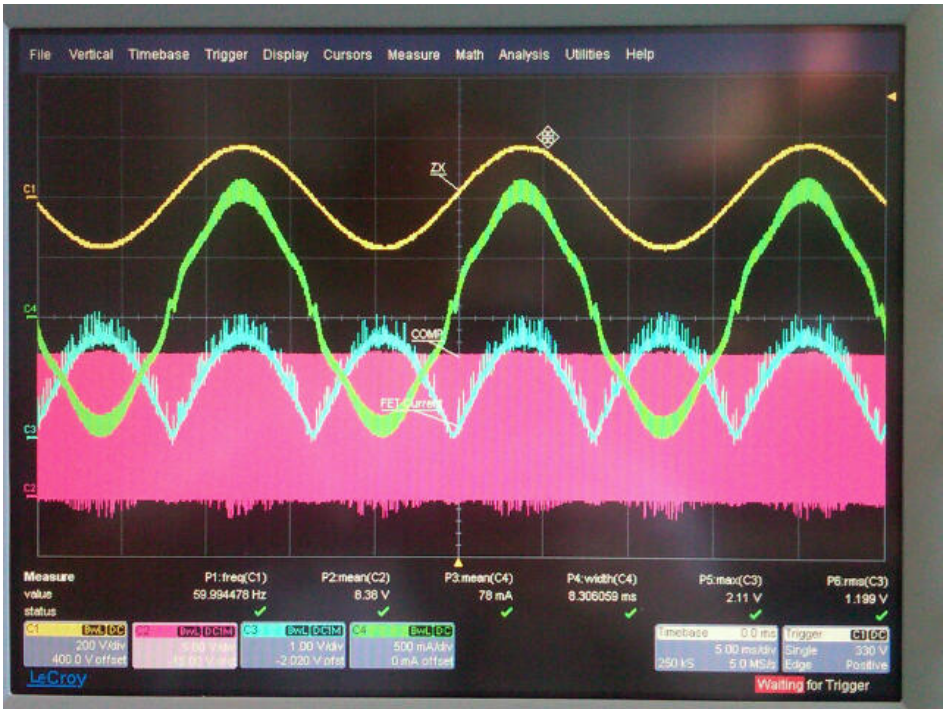


Figure 10: 80W ExampleWaveforms

AC Input Voltage : Yellow
AC Current : Green
VDC Pin Input : Blue
MPFC Gate Drive : Red

Results for power factor and THD were measured over the input voltage range 90VAC to 260VAC (see table 1). In order for the THD results to be accurately measured an electronic AC source was used which produces a pure sinusoidal voltage supply to the board under test. Without using an electronic AC source the input voltage may be distorted as a result of auto-transformers and safety isolating transformers combined with the effects of other loads connected to the AC line. These effects can make THD results appear worse than they actually are.

VAC	VDCmax	VDCmin	P.F.	T.H.D.i	Vout	Pout (W)
90	1	0	0.998	6.4%	440	83.5
100	1.2	0	0.998	5.5%	440	82.7
110	1.4	0	0.998	4.9%	440	82.1
120	1.6	0	0.999	4.4%	440	81.9
140	1.8	0	0.998	4.0%	440	80.9
160	2.0	0	0.998	4.4%	440	80.6
180	2.2	0	0.997	5.4%	440	80.6
200	2.4	0	0.995	6.8%	440	80.6
220	2.6	0	0.993	8.3%	440	80.6
240	2.8	0	0.99	9.8%	440	80.4
260	3	0	0.986	11.3%	440	80.4

Table 1: 80W Example PF and THD Results

10. Replacing Alternative Controllers

Competitor Part Number	Manufacturer	IR Direct Cross	IR Close Cross	IR Cross Possible	Competitor Package	IR Package
L6561(A)	STM	IRS2500			SO8/DIP8	SO8
L6562(A)	STM	IRS2500			SO8/DIP8	SO8
MC33262	On Semi		IRS2500		SO8/DIP8	SO8
UCC28810	TI		IRS2500		SO8/DIP8	SO8
UCC28811	TI		IRS2500		SO8/DIP8	SO8
FAN7527B	Fairchild	IRS2500			SO8/DIP8	SO8

Table 2: Alternative controllers

The IRS2500 can be used as a direct drop in replacement for the controllers listed in table 2 indicated as a *direct cross*. In the case of controllers listed as *close cross* some minor modifications to the application circuit will be necessary in order to replace the existing controller with the IRS2500.
Some controllers such as the MC33262 use a trans-conductance error amplifier where the compensation capacitor is connected from the output to 0V instead of back to the input as in the standard integrating configuration. When replacing this part with the IRS2500 the compensation capacitor must be disconnected from 0V and connected to pin 1.