Application Note AN-1157

CFL Ballast Design
Using Passive PFC and Crest Factor Control

By Masashi Sekine and Tom Ribarich

Table of Contents

Page
Introduction 1
Functional Description 2
Conclusion ….....5

Introduction

Compact fluorescent lamps (CFLs) are now replacing incandescent bulbs because of longer life time and energy saving.
Most CFLs seen in the market are electronic ballast integrated CFLs. Due to the cost, these electronic ballasts don't include PFC circuit witch typically requires additional control IC, inductor and switch, resulting in low power factor and high THD.
This application note describes a CFL ballast using valley fill passive PFC circuit and IR2520D ballast control IC. This ballast design achieves high power factor (>0.9), low THD (<30%) and regulated lamp current crest factor without typical active PFC circuit.

Functional Description

Valley Fill Passive PFC Circuit

Figure 1 shows the valley fill circuitry to achieve high power factor and low THD in simple and low cost.

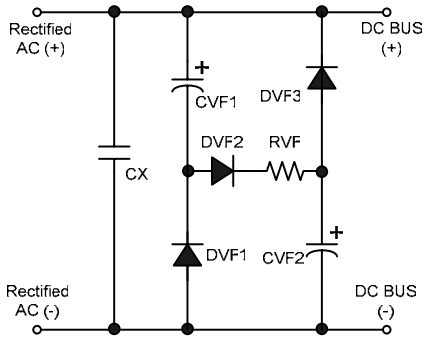


Fig.1: 50% Valley Fill Passive PFC Circuit

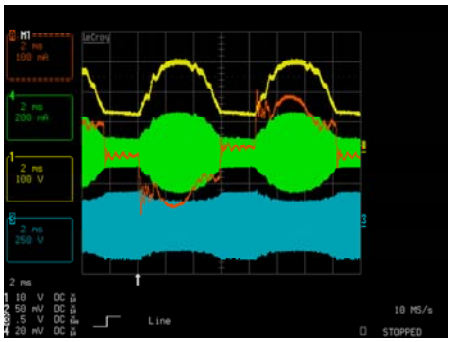


Fig. 2: Valley Fill Circuit Waveforms
Upper: DC BUS (in Yellow), Middle Front: I_{input} (Red)
Middle Back: I_{Lamp} (in Green), Lower: V_{Lamp} (in Blue)

The capacitors CVF1 and CVF2 are charged to ½ of the AC peak voltage in series via the diode DVF2 and resistor RVF on each half cycle of the rectified AC input. RVF is for reducing the peaks in the current waveform as the capacitors charge. They supply output current after the BUS voltage follows the sinusoidal waveform down to $V_{peak}/2$. At this time the caps are essentially in parallel an supply load current until the rectified AC input again exceeds $V_{peak}/2$ on the next half cycle. This valley fill passive PFC circuit presents good power factor (>0.9) and low THD (<30%), the major drawback is the 50% DC BUS ripple witch result in a very high lamp current crest factor. (Fig.2)

The capacitor CX is for filtering the half-bridge inverter switching spikes witch appears at DC BUS. Especially at the light load condition or at the peak of AC input, a big spike occurs at every switching cycle when switching frequency decreases towards resonance causing load voltage and current to increase as seen in Figure 3. Table 1 shows bigger CX cap value gives better filtering, but also decreases PF value.

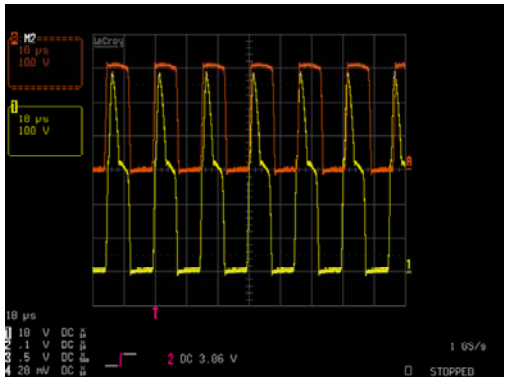


Fig.3: Half-Bridge Inverter Switching Waveforms
Upper: with CX (in Red), Lower: without CX (in Yellow)

CX value	Power Factor
0.047uF	0.960
0.1uF	0.952
0.22uF	0.939
0.33uF	0.923
0.47uF	0.900

Table 1: PF Value vs. CX Value

Lamp Current Crest Factor Control Circuit

If the ballast operating frequency is fixed, 50% DC BUS ripple caused by valley fill circuit generates very high lamp current crest factor because higher DC BUS voltage gives higher lamp current in the resonant output stage. Since high lamp current crest factor shortens lamp life, a compensation circuit is required to decrease lamp current crest factor. Figure 4 shows the crest factor control circuit by modulating half-bridge inverter switching frequency when IR2520D is used for controlling the ballast.

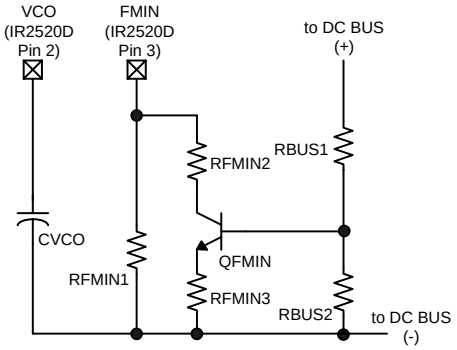


Fig.4: Lamp Current Crest Factor Control Circuit

Since IR2520D has VCO with externally programmable minimum frequency, half-bridge inverter switching frequency is determined by the voltage on VCO pin and the value of resistor connected to FMIN pin. (Please refer to the IR2520D datasheet for detail.) When DC BUS reaches a certain voltage, the voltage on the base of QFMIN connected to the voltage divider, which consists of RBUS1 and RBUS2, exceeds the QFMIN conduction threshold and then QFMIN turns on. At this case, the resistance between FMIN pin and ground becomes parallel RFMIN1 and series RFMIN2 and RFMIN3, which is lower than RFMIN1. Since lower resistance on FMIN pin gives higher switching frequency, the inverter switching frequency at near peak of the DC BUS is higher than at near valley of the DC BUS. As a result, crest factor value witch is given by $I_{LAMP(pk)}$ / $I_{LAMP(avg)}$ will be decreased.

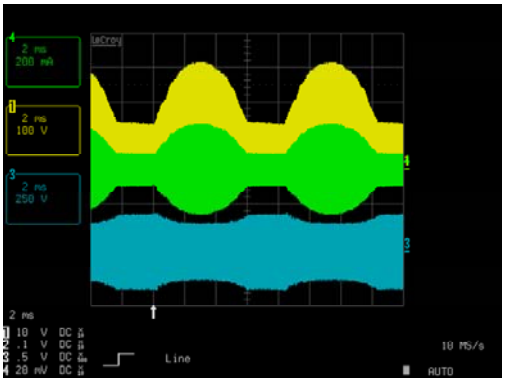


Fig.5: Waveforms without crest factor control circuit
CF =1.95, half-Bridge (Upper), ILMAP (Mid), VLMAP (Lower)

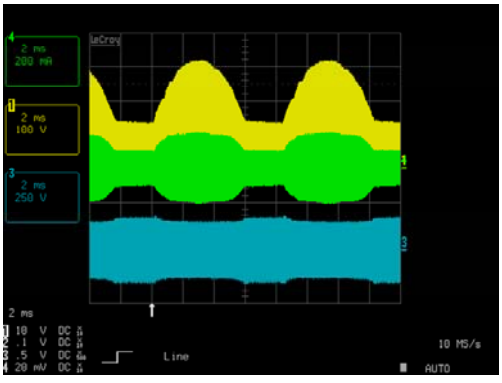


Fig. 6: Waveforms without crest factor control circuit
CF =1.71, Half-Bridge (Upper), ILMAP (Mid), VLMAP (Lower)

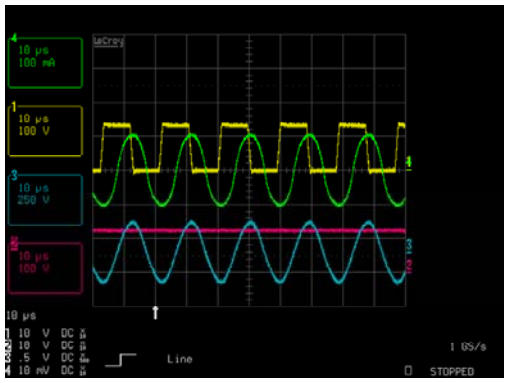


Fig.7: Waveforms at Near DC BUS Valley
f_{SWITCH} =53.0KHz, MLS Drain (Yellow), I_{LMAP} (Green), DC BUS (Red), V_{LMAP} (Blue)

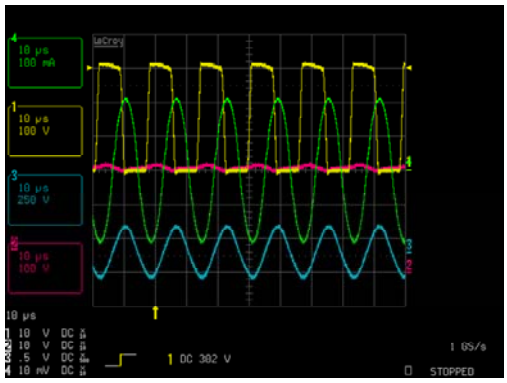


Fig. 8: Waveforms at Near DC BUS Peak
f_{SWITCH} =61.6KHz, MLS Drain (Yellow), I_{LMAP} (Green), DC BUS (Red), V_{LMAP} (Blue)

The purpose of RFMIN3 is emitter degeneration for improving linearity. Without RFMIN3, QFMIN turns on quickly when the voltage on base of QFMIN reaches threshold. This causes lamp current shape distortion because of rapid operating frequency increase.

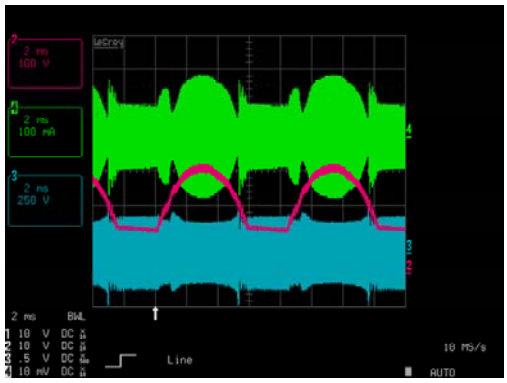


Fig.9: Waveforms with RFMIN3 short
I_{LMAP} (Upper), DC BUS (Mid), V_{LMAP} (Lower)

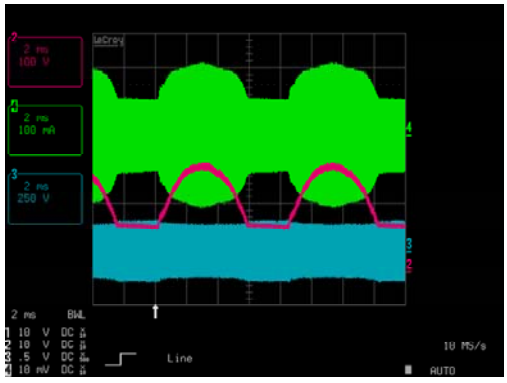


Fig. 10: Waveforms with RFMIN3
I_{LMAP} (Upper), DC BUS (Mid), V_{LMAP} (Lower)

Electronic Ballast Design

Figure 11 shows the complete CFL ballast design. This ballast includes AC input stage with EMI filter, valley fill PFC stage, ballast control stage using IR2520D adaptive ballast control IC and lamp current crest factor control circuit, half-bridge inverter and resonant output stage.

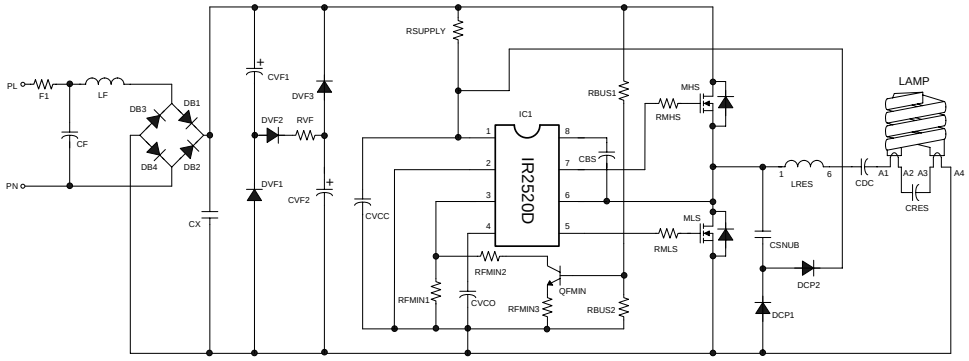


Fig.11: Electronic CFL ballast Circuit using IR2520D

Measurements

Table 2 shows measurement results. Following are the measurement conditions:

1. AC input: 200VAC to 260VAC
2. Lamp Type: 23W Spiral
3. Bill of Material

Qty	Description	Reference
7	Rectifier, 1A 600V	DB1-DB4, DVF1-DVF3,
2	Small Signal Diode, DL-41	DCP1, DCP2
1	RF Chokes, 1mH 200mA	LF
1	Carbon FilmResistor, 1.0R 1W	F1
2	Electrolytic Capacitor, 22uF 400V	CVF1, CVF2
3	Polyester Film Capacitor, 0.047uF 400V	CF, CX, CDC
1	Ceramic Capacitor, 2.2uF 25V	CVCC
1	Ceramic Capacitor, 0.39uF 25V	CVCO
1	Ceramic Capacitor, 0.1uF 25V	CBS
1	Ceramic Capacitor, 1000pF 1KV	CSNUB
1	Polypropylene Capacitor, 4.7nF 1.6KV	CRES
1	Carbon Film Resistor, 1.0M 1/2W	RSUPPLY
1	Metal Film Resisitor, 470R, 1W	RVF
2	Film Chip Resistor, 10 ohm 1/4W,	RMHS, RMLS
1	Film Chip Resistor, 51K 1/4W,	RFMIN1
1	Film Chip Resistor, 180K 1/4W,	RFMIN2
1	Film Chip Resistor, 6.8K 1/4W	RFMIN3
1	Film Chip Resistor, 430K 1/4W	RBUS1
1	Film Chip Resisitor, 1K 1/4W	RBUS2
1	Transistor, NPN 40V, SOT-23	QFMIN
2	IR730, NPN MOSFET, 400V, TO-220	MHS, MLS
1	Ballast Controller, IR2520D	IC1
1	Resonant Inductor, 2.0mH, EF20,	LRES

Parameter / Input	Pin (W)	Iin (mA)	PF	THD (%)	Lamp CF
200VAC	19.7	97.3	0.965	25.8	1.62
220VAC	20.1	88.1	0.961	27.5	1.71
240VAC	21.4	85.4	0.959	28.5	1.78
260VAC	21.5	83.5	0.957	28.9	1.84

Table 2: Major Electrical Parameters

Conclusion

This application note suggests a CFL ballast circuit that achieves good power factor and low THD in cost effective way. The design includes low cost PFC stage and control stage using IR2520D 8-pin ballast control IC. Because of the simplicity of the ballast control method, total number of components used in this ballast is minimized, however, the design satisfies all of the necessary ballast features.