Application Note AN-1151

IRS2168D Additional Design Information

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Table of Contents

	Page
Introduction	1
Ballast Oscillator	2
PFC Circuit	4
Resonant Tank Output Circuit	9
IC Start-Up and Supply Circuit	14
High-Side VBS Bootstrap Supply	17
PCB Layout Guidelines	19
Conclusion	21

Introduction

Designing a fully-functional ballast using the IRS2168D can be a challenging task. Much care should be taken when generating the ballast circuit schematic, selecting component values and ratings, and generating the ballast PCB layout. The purpose of this application note is to provide additional information to help decrease design time and avoid circuit problems due to wrong component values or ratings, incorrect programming of IC parameters, and noise. This application note includes helpful information for programming the ballast oscillator frequency, calculating the PFC inductor value, designing the resonant tank output circuit, and designing the start-up and low- and high-side supply circuitry. Layout guidelines are also included to help avoid noise problems that can cause circuit malfunction or poor ballast performance.

Ballast Oscillator Frequency

The IC oscillator includes an internal CT timing capacitor and an external timing resistor at the RFMIN pin. The frequency is programmed with the RFMIN resistor connected between pin 4 and COM, and, the RPH resistor connected between pin 3 and pin 4 (Figure 1). An internal 2V reference at the RFMIN pin, together with the external RFMIN resistor, sets up a current flowing out of the RFMIN pin. This current is then mirrored internally and used to charge and discharge the internal CT timing capacitor between two fixed thresholds. By increasing RFMIN, the current will decrease, the CT capacitor will charge and discharge slower and the frequency will decrease. Inversely, by decreasing RFMIN, the current will increase, the CT capacitor will charge and discharge faster and the frequency will increase.

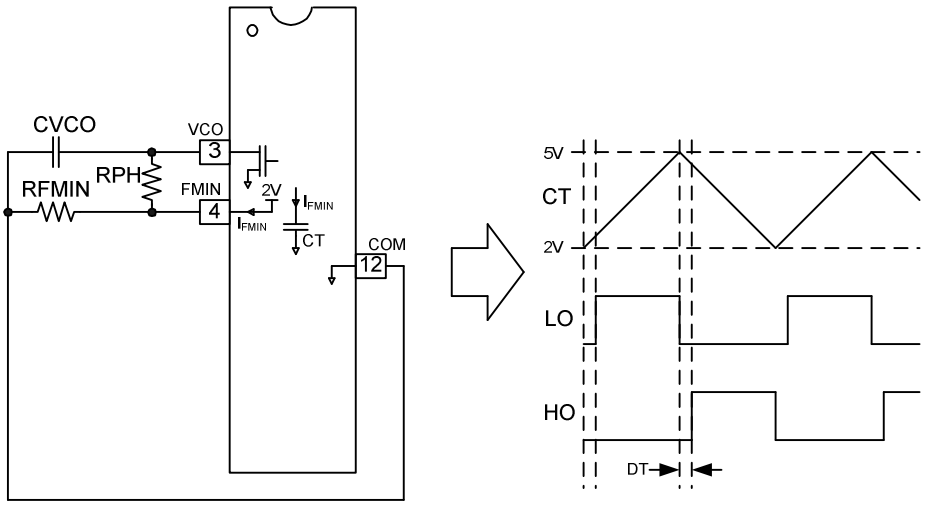


Figure 1, IRS2168D ballast oscillator circuit.

The RFMIN resistor sets the minimum operating frequency of the ballast half-bridge gate drivers (LO and HO) during RUN mode. During PREHEAT mode, the VCO pin is connected to COM so that the higher preheat frequency is programmed with the parallel combination of resistors RFMIN and RPH. The equivalent RFMIN resistance versus frequency graph (Figures 2a and 2b) can be used to select the correct RFMIN and RPH values for the desired preheat and running frequencies. It is recommended that the minimum equivalent RFMIN resistance should be no less than 10K ohm (see IRS2168D Datasheet, page 3).

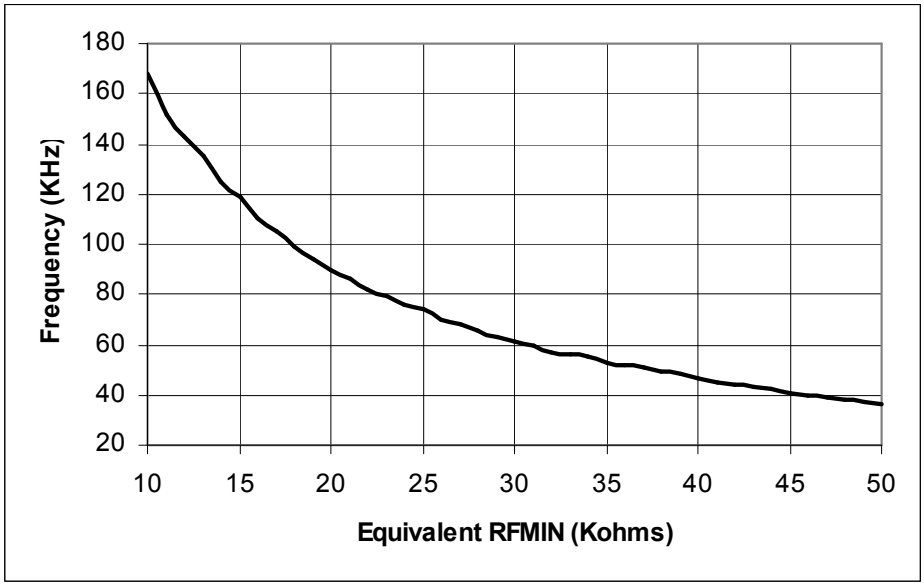


Figure 2a, Equivalent RFMIN vs. Frequency (RFMIN=10K to 50K)

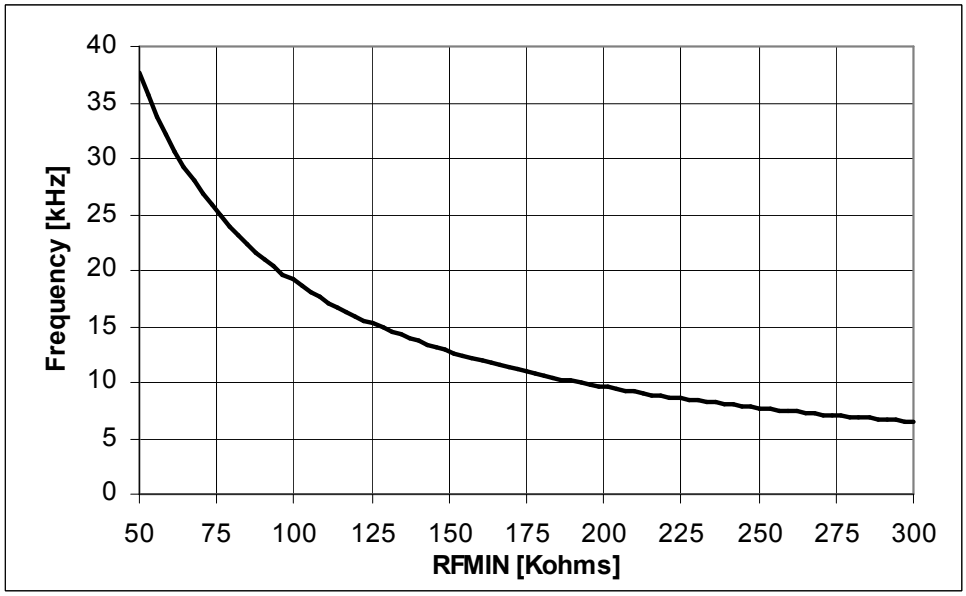


Figure 2b, Equivalent RFMIN vs. Frequency (RFMIN=50K to 300K).

The frequency sweep time (also known as the ignition ramp time) is then programmed with an external CVCO capacitor between the VCO pin and COM. When the VCO pin is disconnected from COM at the end of PREHEAT mode, the voltage at the bottom of the RPH resistor charges up to the 2V level at the RFMIN pin at a time constant given by RPH and CVCO. This causes the total resistance at the RFMIN pin to increase as well and results in a smooth transition of the frequency from the preheat frequency down to the final running frequency.

PFC Inductor Calculations

The IRS2168D includes a boost-type PFC controller that operates in critical-conduction mode. During the PFC MOSFET on-time, the inductor current ramps up linearly to a peak current value (Figure 3) depending on the instantaneous value of the rectified AC line voltage, the inductor value and the on-time. During the PFC MOSFET off-time, the inductor current discharges back down linearly to zero and the PFC switch is turned on again.

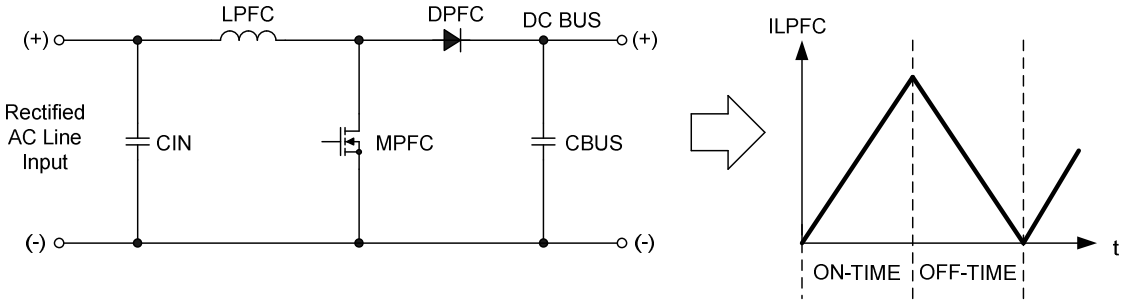


Figure 3, Boost-type converter and inductor current during critical-conduction mode.

The result is a triangular shaped current that varies in frequency depending on the level of the instantaneous rectified AC line voltage (Figure 4). The maximum switching frequency occurs at the zero-crossings of the rectified AC line voltage and the minimum switching frequency occurs at the peak of the rectified AC line voltage.

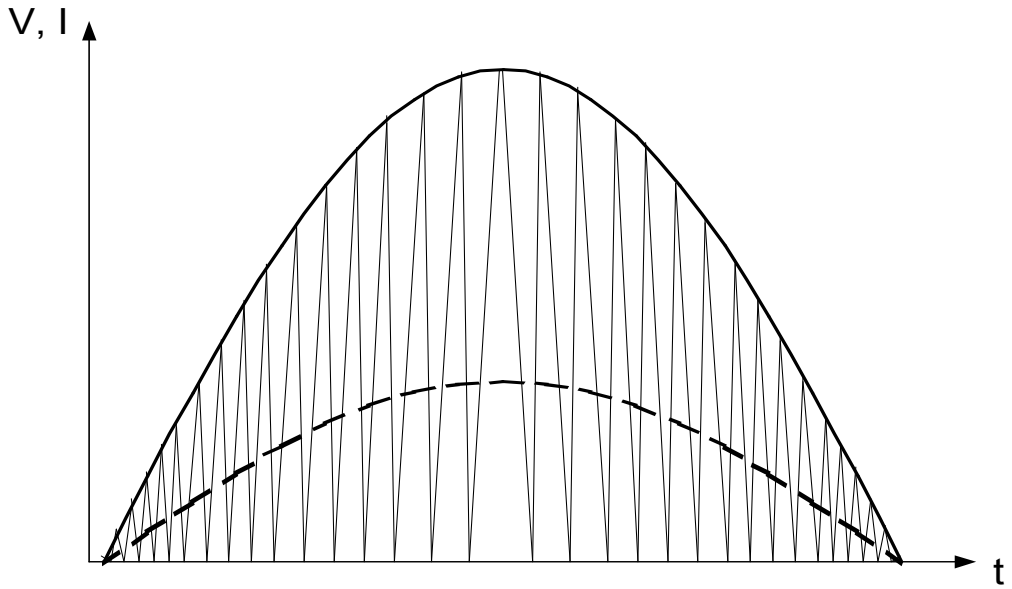


Figure 4, PFC inductor current amplitude and frequency during the AC line voltage cycle.

To calculate the inductor value as a function of the desired minimum switching frequency, the following derivation can be used:

Definition of terms:

$VBUS$	=	DC bus voltage
$VAC_{NOM_{PK}}$	=	Peak voltage at nominal AC input condition $(VAC_{NOM_{PK}} = VAC_{RMS} \cdot \sqrt{2})$
η	=	Boost converter efficiency (typically 0.95)
f_{MIN}	=	Minimum switching frequency occurring at the peak of the AC input voltage
P_{OUT}	=	Ballast output power
I_{PFC}	=	Peak inductor current occurring at the peak of the nominal AC input voltage
I_{PFCMAX}	=	Maximum peak inductor current occurring at the peak of the minimum AC input voltage
t_{ON}	=	PFC on-time
t_{OFF}	=	PFC off-time
L_{PFC}	=	PFC inductor

During the on-time of the PFC MOSFET, the inductor is connected between the rectified AC input voltage and ground and the following equation applies:

$$VAC_{NOM_{PK}} = L_{PFC} \cdot \frac{I_{PFC}}{t_{ON}} \quad \Rightarrow \quad t_{ON} = \frac{L_{PFC} \cdot I_{PFC}}{VAC_{NOM_{PK}}} \quad [\text{Sec}] \quad [1]$$

During the off-time of the PFC MOSFET, the inductor is connected between the rectified AC input voltage and a diode drop above the DC bus and the following equation applies:

$$VBUS - VAC_{NOM_{PK}} = L_{PFC} \cdot \frac{I_{PFC}}{t_{OFF}} \quad \Rightarrow \quad t_{OFF} = \frac{L_{PFC} \cdot I_{PFC}}{VBUS - VAC_{NOM_{PK}}} \quad [\text{Sec}] \quad [2]$$

Combining the on-time and off-time equations to solve for frequency gives the following equation:

$$f_{MIN} = \frac{1}{t_{ON} + t_{OFF}} = \frac{VAC_{NOM_{PK}} \cdot (VBUS - VAC_{NOM_{PK}})}{L_{PFC} \cdot I_{PFC} \cdot VBUS} \quad [\text{Hz}] \quad [3]$$

To solve for the peak inductor current, the following relationship between the input power and output power is used (assuming PF=1):

$$P_{in} \cdot \eta = VAC_{NOM_{RMS}} \cdot IAC_{NOM_{RMS}} \cdot \eta = P_{OUT} \quad \Rightarrow \quad IAC_{NOM_{RMS}} = \frac{P_{OUT}}{VAC_{NOM_{RMS}} \cdot \eta} \quad [4]$$

For a triangular shaped waveform, the peak value is equal to $2\sqrt{2}$ times the r.m.s. value. Applying this ratio to the r.m.s. input current gives the following result for the peak PFC inductor current at the nominal AC line input voltage:

$$I_{PFC} = IAC_{NOM_{RMS}} \cdot 2 \cdot \sqrt{2} = \frac{P_{OUT} \cdot 2 \cdot \sqrt{2}}{VAC_{NOM_{RMS}} \cdot \eta} = \frac{P_{OUT} \cdot 2 \cdot \sqrt{2}}{\frac{VAC_{NOM_{PK}}}{\sqrt{2}} \cdot \eta} = \frac{4 \cdot P_{OUT}}{VAC_{NOM_{PK}} \cdot \eta} \quad [\text{Apk}] \quad [5]$$

The maximum peak inductor current occurs at the peak voltage during minimum AC line input conditions and is calculated as:

$$I_{PFCMAX} = \frac{4 \cdot P_{OUT}}{VAC_{MIN_{PK}} \cdot \eta} \quad [\text{Apk}] \quad [6]$$

The maximum peak inductor cycle-by-cycle current limit is programmed at the OC pin of the IRS2168D with the PFC current sensing resistor, ROC, and an internal 1.25V threshold and is calculated with the following equation:

$$R_{OC} = \frac{1.25}{I_{PFCMAX}} \quad [\text{Ohms}] \quad [7]$$

Substituting the peak inductor current result from equation [5] into the frequency equation [3] gives the following result:

$$f_{MIN} = \frac{VAC^2_{NOM_{PK}} (VBUS - VAC_{NOM_{PK}}) \cdot \eta}{4 \cdot L_{PFC} \cdot P_{OUT} \cdot VBUS} \quad [\text{Hz}] \quad [8]$$

Solving for the PFC inductor gives the following result:

$$L_{PFC} = \frac{VAC^2_{NOM_{PK}} (VBUS - VAC_{NOM_{PK}}) \cdot \eta}{4 \cdot f_{MIN} \cdot P_{OUT} \cdot VBUS} \quad [\text{H}] \quad [9]$$

If the PFC inductor value is known then equation [8] can be used to calculate the minimum PFC switching frequency that occurs at the peak of the rectified AC input voltage. If the desired minimum switching frequency is known then equation [9] can be used to calculate the PFC inductor value but this should be checked carefully with the following additional calculations to make sure that the on-time modulation circuit is working properly so that low THD is achieved.

The IRS2168D PFC control circuit includes an additional on-time modulation circuit for achieving low THD. The on-time modulation circuit increases the on-time as the off-time decreases near the zero-crossing regions of the AC line input. This is necessary to reduce cross-over distortion of the AC line current and therefore reduce THD. To ensure that the on-time modulation circuit

is working properly, the PFC inductor value must be selected such that the PFC off-time at the peak of the AC line, at the nominal AC line input voltage, is slightly higher than the off-time where the on-time modulation begins working. The on-time modulation begins working at an off-time of about 7usec (Figure 5). So selecting an off-time of 8usec will ensure that the on-time modulation is not working at the peak of the AC line voltage and that it is working when the rectified AC line voltage is lower near the AC line zero-crossings.

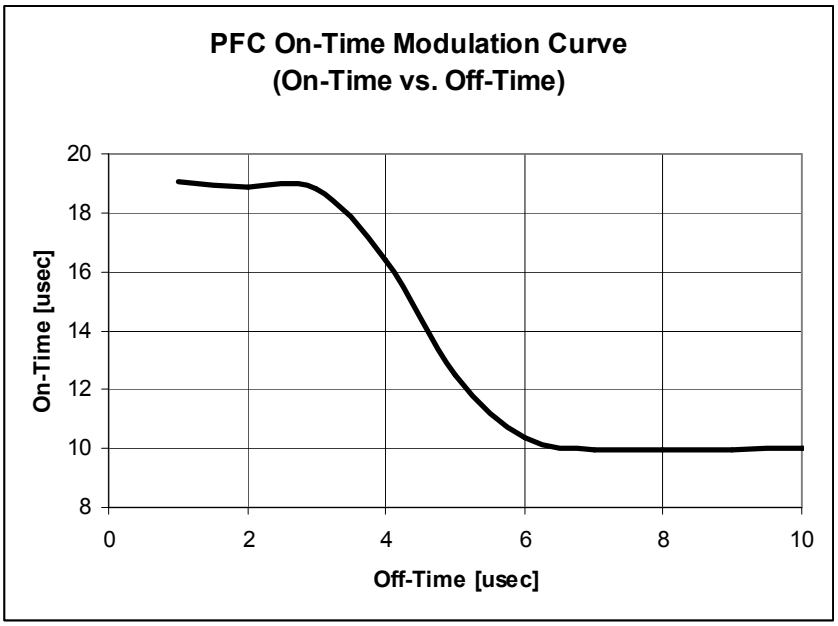


Figure 5, PFC on-time vs. off-time curve for on-time modulation (VCOMP=10V).

Using this off-time requirement of 8usec at the peak of the rectified AC line voltage during nominal AC line voltage conditions, we can derive the following equation to determine the best value for the PFC inductor to ensure that the on-time modulation is working correctly:

$$VBUS - VAC_{NOM_{PK}} = L_{PFC} \cdot \frac{i_{PK}}{t_{OFF}} \quad \Rightarrow \quad L_{PFC} = \frac{(VBUS - VAC_{NOM_{PK}}) \cdot t_{OFF}}{I_{PK}} \qquad [10]$$

Substituting the peak inductor current equation [5] into equation [10] gives:

$$L_{PFC} = \frac{(VBUS - VAC_{NOM_{PK}}) \cdot t_{OFF} \cdot VAC_{NOM_{PK}} \cdot \eta}{4 \cdot P_{OUT}} \qquad [11]$$

Inserting the off-time requirement of 8usec for toff into equation [11] gives the final equation for calculating the correct PFC inductor value:

$$L_{PFC} = \frac{(0.000008)\cdot(VBUS - VAC_{NOM_{PK}})\cdot VAC_{NOM_{PK}}\cdot\eta}{4\cdot P_{OUT}} \quad [H] \quad [12]$$

If the off-time at the peak of the rectified AC input voltage is set too high above 8usec, then the on-time modulation may not be increasing the on-time enough (or not at all) at the AC line zero-crossings and will result in the THD being too high. If the off-time at the peak of the rectified AC input voltage is set too low below 8usec, then the on-time modulation will be working the entire time causing distortion of the AC input current and will also result in the THD being too high. Therefore, equation [12] should be used to calculate the PFC inductor value and equation [8] can be used to then calculate the resulting minimum switching frequency occurring at the peak of the rectified AC line voltage. If equation [9] is used to determine the PFC inductor value based on the desired minimum switching frequency, then equation [2] should be used to check the resulting off-time at the peak of the rectified AC input voltage to make sure it is approximately 8usec. This will ensure that the on-time modulation is working correctly and will result in low THD of the AC line input current.

The PFC control loop speed must be properly set so that the shape of the AC line input current follows the shape of the AC line input voltage. This is necessary so that the electronic ballast appears as a “resistive” load to the AC line. Since the AC line input voltage is changing very slowly (50/60Hz), the PFC loop speed should also be set very low so that the current can follow the shape of the voltage properly. The better the current follows the shape of the voltage, then the lower the resulting harmonic distortion of the current (THD). If the loop speed is set too fast, then distortion of the current will occur and cause high harmonic distortion. If the loop speed is set too slow, then a poor transient response can result and cause large voltage over-shoot and/or under-shoot on the DC bus during load changes. During preheat and ignition modes, the operational transconductance amplifier (OTA) of the PFC circuit includes a high gain mode to increase the loop speed to prevent large transients during lamp ignition. During run mode, the OTA gain is then reduced so that the current follows the voltage for high power factor and low harmonics. The PFC loop speed is set using the external capacitor at the COMP pin (CCOMP) using the gm of the OTA and the desired loop speed bandwidth. Using a typical gm of 100 umhos for the OTA and a loop speed bandwidth of 20Hz, capacitor CCOMP is calculated using the following equation:

$$C_{COMP} = \frac{gm}{2\cdot\pi\cdot BW} = \frac{100}{2\cdot\pi\cdot 20} = 0.796 \Rightarrow 0.82 \quad [uF] \quad [13]$$

Since the PFC loop speed is only a function of the OTA transconductance and the desired bandwidth, this calculated value for CCOMP should remain fixed for all ballast designs.

Resonant Tank Output Circuit

The half-bridge inverter and resonant tank output circuit of the ballast (Figure 6) perform the necessary functions to drive the fluorescent lamp. The circuit includes a half-bridge switching circuit (MHS, MLS), a resonant inductor (LRES:A), a resonant capacitor (CRES), a dc blocking capacitor (CDC), the lamp, and voltage-mode filament heating circuits (LRES:B, CH1, LRES:C, CH2). The functions performed by this circuit include preheating the lamp filaments, igniting the lamp, and supplying a high-frequency AC current through the lamp during running. All of these functions can be achieved by properly selecting the resonant inductor and capacitor, and then controlling the frequency of the inverter stage to preheat, ignite and run the lamp. The output resonant circuit is a high-Q, series L-C circuit during preheat and prior to lamp ignition, and then becomes a low-Q, series L, parallel R-C after ignition and during running.

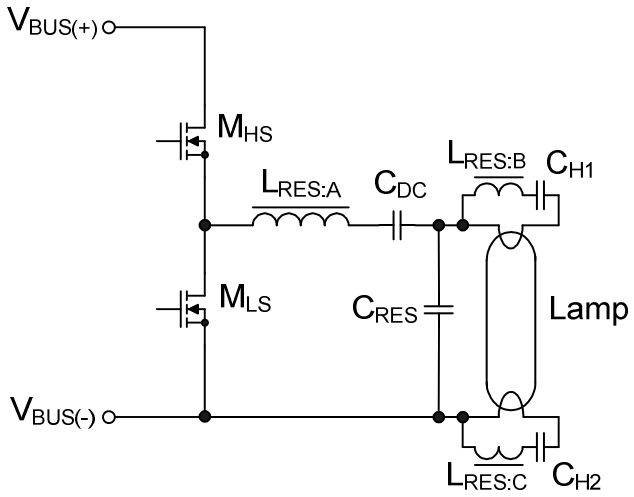


Figure 6, Half-bridge and resonant tank output circuit.

The frequency of the half-bridge inverter driving the resonant tank operates at a higher frequency (above the resonance frequency of the series L-C circuit) during preheat mode. The frequency remains at the preheat frequency for the duration of the preheat time (Figure 7) such that the lamp filaments are heated to their correct emission temperature. The filament heating is achieved with secondary windings from the inductor (LRES:B, LRES:C) and capacitors to limit the heating current (CH1, CH2). After the preheat time has ended, the frequency then sweeps down smoothly through the resonance frequency during ignition mode (Figure 7). This causes the gain across the resonant tank circuit to increase smoothly, as well as the voltage across the lamp, until the lamp ignition threshold voltage is reached. The lamp then ignites and the frequency continues to sweep down to the final run frequency where the gain of the resonant tank circuit sets the correct lamp current (Figure 7). Different lamp types have different preheat, ignition and running requirements. The resonant inductor (LRES) and capacitor (CRES) values, together with the inverter operating frequencies, must be selected carefully in order to satisfy each set of lamp requirements.

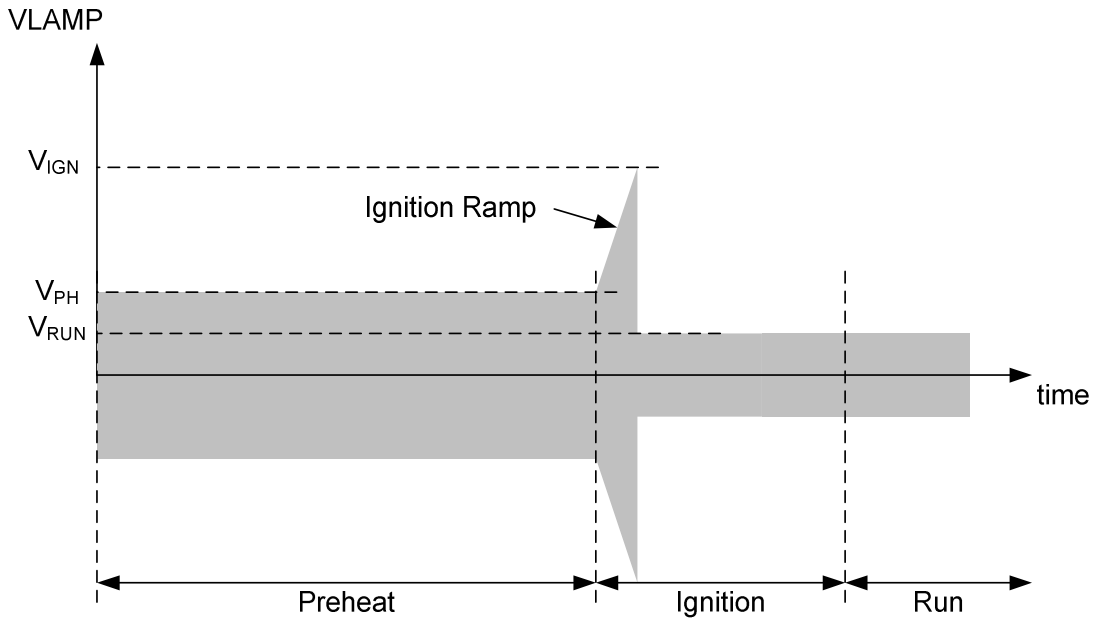


Figure 7, Lamp output voltage timing diagram during preheat, ignition and run modes.

To select the resonant tank component values and operating frequencies the following procedure and equations can be used:

Definition of terms:

V_{BUS}	=	DC bus voltage
V_{LAMP}	=	Nominal r.m.s. lamp voltage during running conditions
f_{RUN}	=	Operating frequency during lamp running conditions
P_{LAMP}	=	Nominal lamp power during running
R_{LAMP}	=	Equivalent lamp resistance during running
L_{RES}	=	Resonant tank inductor
C_{RES}	=	Resonant tank capacitor
V_{PH}	=	Peak output voltage across lamp during preheat mode
f_{PH}	=	Operating frequency during preheat mode
V_{IGN}	=	Maximum peak output voltage across lamp during ignition mode
f_{IGN}	=	Operating frequency occurring during maximum peak ignition voltage
I_{IGN}	=	Maximum peak inductor current during maximum peak ignition voltage

The resonant inductor value is primarily used to set the lamp current during running conditions at the desired running frequency. During run mode, the running frequency can be calculated as a function of the resonant inductor with the following equation:

$$f_{RUN}=\frac{1}{2\pi}\sqrt{\frac{1}{L_{RES}C_{RES}}-\frac{1}{2R_{LAMP}^2C_{RES}^2}+\sqrt{\left[\frac{1}{L_{RES}C_{RES}}-\frac{1}{2R_{LAMP}^2C_{RES}^2}\right]^2-\frac{1-\left(\frac{2V_{BUS}}{V_{LAMP}\pi\sqrt{2}}\right)^2}{L_{RES}^2C_{RES}^2}}} \text{ [Hz]} \quad [14]$$

Solving for the resonant inductor gives the following result:

$$L_{RES}=\frac{2C_{RES}(2\pi f_{RUN})^2+\sqrt{4C_{RES}(2\pi f_{RUN})^4-4\left[C_{RES}^2(2\pi f_{RUN})^4+\frac{(2\pi f_{RUN})^2}{R_{LAMP}^2}\right]\left[1-\left(\frac{2V_{BUS}}{V_{LAMP}\pi\sqrt{2}}\right)^2\right]}}{2\left[C_{RES}^2(2\pi f_{RUN})^4+\frac{(2\pi f_{RUN})^2}{R_{LAMP}^2}\right]} \text{ [H]} \quad [15]$$

Where,

$$R_{LAMP}=\frac{V_{LAMP}^2}{P_{LAMP}} \quad \text{[Ohms]} \quad [16]$$

During preheat mode, the frequency should be selected such that the resulting lamp voltage is low. A low lamp voltage will prevent the lamp from igniting too early during the preheat mode before the filaments are properly heated which can cause end-blackening of the lamp and shorten the lamp lifetime. During preheat mode, the preheat frequency as a function of the peak output voltage across the lamp can be calculated with the following equation:

$$f_{PH}=\frac{1}{2\pi}\sqrt{\frac{1+\frac{2V_{BUS}}{V_{PH}\pi}}{L_{RES}C_{RES}}} \quad \text{[Hz]} \quad [17]$$

During ignition mode, the frequency will ramp down from the preheat frequency to the run frequency at a sweep rate programmed by CVCO of the IRS2168D. As the frequency ramps down, the voltage across the lamp will increase as the frequency decreases towards the resonance frequency. When the voltage reaches the maximum peak output voltage, VIGN, as programmed by the CS pin of the IRS2168D, the ignition regulation circuit will control the frequency to keep VIGN constant during the ignition mode. The frequency occurring during the ignition regulation at VIGN can be calculated with the following equation:

$$f_{IGN} = \frac{1}{2\pi}\sqrt{\frac{1+\frac{2V_{BUS}}{V_{IGN}\pi}}{L_{RES}C_{RES}}} \quad [\text{Hz}] \quad [18]$$

The peak inductor current flowing in LRES during the moment when the maximum peak ignition voltage occurs during the ignition mode is calculated with the following equation:

$$I_{IGN} = f_{IGN}C_{RES}V_{IGN}2\pi \quad [\text{Apk}] \quad [19]$$

The inductor should be designed such that the maximum peak ignition current can be reached without saturation occurring over temperature and tolerances.

To program the DC bus voltage, preheat and run frequencies, and the maximum ignition voltage, the external components around the IRS2168D must be correctly selected. The DC bus voltage is programmed at the VBUS pin using resistors RVBUS1, RVBUS2 and RVBUS (see Figure 10). Assuming RVBUS1 and RVBUS2 to be fixed, RVBUS is calculated using the following equation:

$$R_{VBUS} = \frac{4\left(R_{VBUS1} + R_{VBUS2}\right)}{V_{BUS} - 4} \quad [\text{Apk}] \quad [20]$$

The run frequency is programmed at the FMIN pin with resistor RFMIN. The value of RFMIN can be selected using the graphs in Figure 2.

The preheat frequency is programmed with the parallel combination of resistor RPH and RFMIN. Use the graphs in Figure 2 to select the REQUIV value for the desired preheat frequency, and then calculate RPH using the following equation:

$$R_{PH} = \frac{R_{FMIN} \cdot R_{EQUIV}}{R_{FMIN} - R_{EQUIV}} \quad [\text{Apk}] \quad [21]$$

The maximum peak ignition voltage is programmed at the CS pin with the current sensing resistor, RCS, and an internal 1.25V threshold and can be calculated using the following equation:

$$R_{CS} = \frac{1.25}{I_{IGN}} \quad [\text{Apk}] \quad [22]$$

A typical design example is shown for a T5/54W lamp. The ballast and lamp data is given as the following:

VAC_{RMS}	=	220VAC
VAC_{MIN}	=	185VAC
V_{BUS}	=	410VDC
P_{LAMP}	=	54W
V_{LAMP}	=	152VAC
C_{RES}	=	3.3nF
f_{RUN}	=	40kHz
V_{PH}	=	300Vpk
V_{IGN}	=	1000Vpk
$R_{VBUS1,2}$	=	680kOhms

The lamp data is used together with the design equations to calculate the resonant tank circuit component values, operating frequencies, peak inductor current, and IRS2168D ballast programming component values (Table I). The PFC inductor value, PFC inductor peak current, PFC minimum switching frequency, and the PFC current sensing resistor value have been calculated as well.

Parameter	Calculated Value	Units	Equation Used
R_{LAMP}	428	Ohms	[16]
L_{RES}	1.7	mH	[15]
f_{PH}	84.7	kHz	[17]
f_{IGN}	69.6	kHz	[18]
I_{IGN}	1.4	Apk	[19]
R_{VBUS}	13.4	kOhms	[20]
R_{FMIN}	45.0	kOhms	Graph, Fig.2
R_{PH}	43.0	kOhms	Graph, Fig.2, [21]
R_{CS}	0.9	Ohms	[22]
L_{PFC}	1.1	mH	[12]
I_{PFCMAX}	0.87	Apk	[6]
f_{MIN}	94.8	kHz	[8]
R_{OC}	1.4	Ohms	[7]
C_{COMP}	0.82	uF	[13]

Table I, Calculated resonant tank and PFC circuit parameter values.

When comparing the calculated values versus actual bench measurements, differences can occur due to lamp tolerances, component tolerances, DC bus tolerances and component power losses.

IC Start-Up and Supply Circuitry

The external IC supply circuit is designed to perform four main functions. The first function is to supply the micro-power current to VCC during UVLO and Fault modes. The second function is to set the AC line input voltage turn-on threshold for the complete ballast. The third function is to supply the necessary ICC current to VCC during normal Preheat, Ignition and Running modes. The fourth function is to supply the IBS current to the VBS high-side supply. The first and second functions are performed by the supply resistor, RSUPPLY, connected between the rectified AC line input and VCC (Figure 8). This resistor supplies the necessary micro-power current to VCC during UVLO and Fault modes.

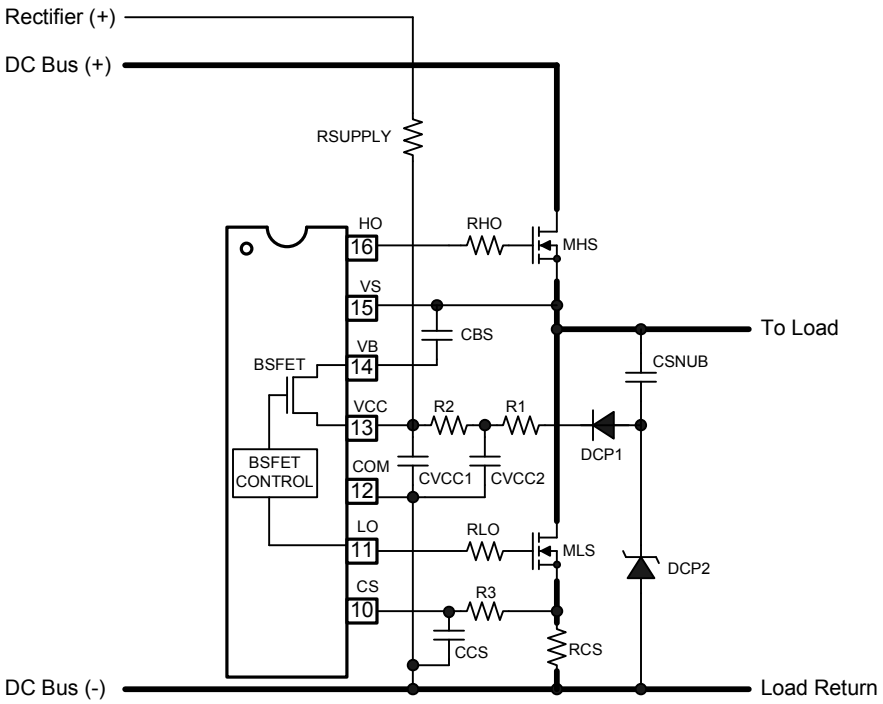


Figure 8, IC start-up and supply circuitry.

During UVLO mode, this resistor determines the AC line turn-on voltage for the IC by supplying the correct amount of current such that VCC reaches the VCCUV+ threshold at the desired AC line voltage. The IRS2168D datasheet lists the nominal IQCCUV current to be 220uA at VCC=8V (IRS2168D datasheet, page 3). To calculate the correct value for the RSUPPLY resistor, the nominal IQCCUV current value just prior to VCC reaching VCCUV+ should be used instead. VCCUV+ minus 100mV is defined as the VCC voltage level just before turn-on. By measuring several ICs on the bench, this current has been determined to be approximately 300uA. The RCPH resistor connected between VCC and the CPH pin needs to be considered as well. During UVLO mode the CPH pin is connected to COM so there is current flowing from VCC through

RCPH to COM as well. The value for RSUPPLY can therefore be calculated using the following equation:

$$R_{SUPPLY} \cong \frac{VAC_{ON_{PK}}}{I_{QCCUV@(VCCUV+)-100mV} + \frac{((VCCUV+)-100mV)}{R_{CPH}}} \quad \text{[Ohms]} \quad [23]$$

$$R_{SUPPLY} \cong \frac{VAC_{ON_{PK}}}{0.000300 + \frac{((VCCUV+)-100mV)}{R_{CPH}}} \quad \text{[Ohms]} \quad [24]$$

Any additional current being supplied from VCC to the external ballast circuitry needs to be included in this calculation as well. So the 300uA value plus the additional current flowing through RCPH may need to be increased depending on what additional circuits (pull-up resistors, filament detection circuits, etc.) are connected to VCC.

The maximum power loss for RSUPPLY occurs when the AC line input voltage is at the maximum value of the specified input voltage range. With RSUPPLY between the output of the full-wave bridge rectifier and VCC, the power loss in resistor RSUPPLY is calculated as:

$$P_{RSUPPLY} \cong \frac{(VAC_{MAX_{RMS}} - VCC)^2}{R_{SUPPLY}} \quad \text{[Watts]} \quad [25]$$

The power loss and resulting temperature of RSUPPLY should be measured on the bench under high AC line conditions to make sure the power rating of RSUPPLY is correct. If necessary, two resistors can be placed in series for RSUPPLY to divide the power loss, reduce the temperature and to reduce the maximum voltage drop across each resistor.

The third function is performed by the charge pump supply circuit connected to the half-bridge switching node, VS (Figure 8). After VCC exceeds VCCUV+, the IC enters Preheat mode and the gate driver outputs LO and HO begin oscillating. LO and HO turn the external half-bridge MOSFETs on and off causing the VS node to switch between the DC bus and COM. The charge pump supply circuit connected to VS (CSNUB, DCP1, DCP2) then takes over as the main supply circuit for the IC and VCC increases quickly from VCCUV+ up to the internal zener clamp voltage (15.6V, typical). During the rising edges of VS from COM to the DC bus each cycle, the charging current through the snubber capacitor CSNUB also flows through the charge pump diode DCP1 to VCC. During the falling edges of VS, the discharging current through CSNUB flows from COM through the lower diode DCP2. In addition to reducing EMI due to the dv/dt of the VS node, the value of CSNUB should also be large enough such that enough current is supplied to VCC during preheat, ignition and running operating conditions. CSNUB must not be too large otherwise VS will not commutate to the

opposite rail within the fixed dead-time period (1.6usec, typical) and non-zero-voltage switching (non-ZVS) will occur. Additional filtering should also be added to the charge pump circuit to protect VCC from high current spikes that can occur in the charge pump due to hard-switching of VS or saturation of the lamp resonant inductor. This additional filtering includes using an 18V zener diode for DCP2, and, placing small current limiting resistors (R1 and R2) before each VCC capacitor (CVCC2 and CVCC1).

High-Side VBS Bootstrap Supply

The fourth function of supplying the high-side circuitry is performed by the internal bootstrap MOSFET (BSFET) and external CBS capacitor. This internal MOSFET is connected between VCC and VB and is only turned on during the LO on-time each cycle. During the LO on-time, the lower half-bridge MOSFET is on and VS is then connected to COM. Current flows from VCC, through the bootstrap MOSFET, to VB, and the external capacitor CBS is charged up. During the on-time of HO, VS is connected to the DC bus and the capacitor CBS discharges slightly as it provides the high-side current for the turn-on of the external high-side half-bridge MOSFET. The capacitor CBS is then replenished again during each LO on-time. The value of CBS should be large enough such that the voltage ripple does not decrease below the UVBS- threshold of the high-side circuitry (9.0V, maximum). Typically 0.1uF is sufficient for most applications. For higher frequency applications, the internal bootstrap MOSFET may not be able to supply enough current to fully charge the high-side supply each cycle. In this case, an external bootstrap diode is required to keep VBS high enough above UVBS- (Figures 9a and 9b). Figure 9a shows LO and HO during operating at about 168kHz and using the internal bootstrap MOSFET. The amplitude of HO (which is equal to VBS) is below 10V and is very close to the nominal UVBS- threshold (8V, typical). Figure 9b shows the improved waveforms using an external bootstrap diode. The amplitude of HO (and VBS) is now close to VCC each cycle and well above the maximum UVBS-. For operating frequencies above 100kHz, the VBS and HO amplitudes should be measured carefully to make sure they are higher than about 10V.

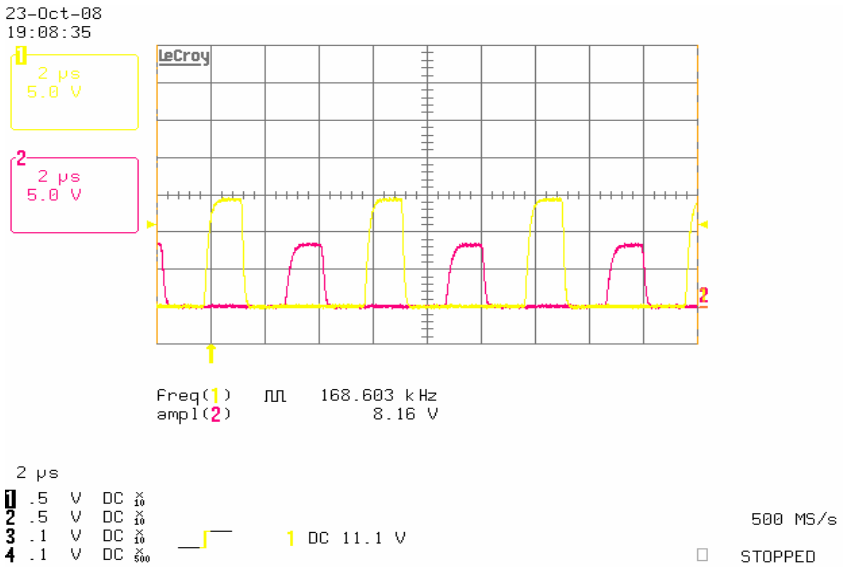


Figure 9a, LO (yellow) and HO (red) using internal bootstrap MOSFET (CBS=0.1uF, CHO=CLO=1nF).

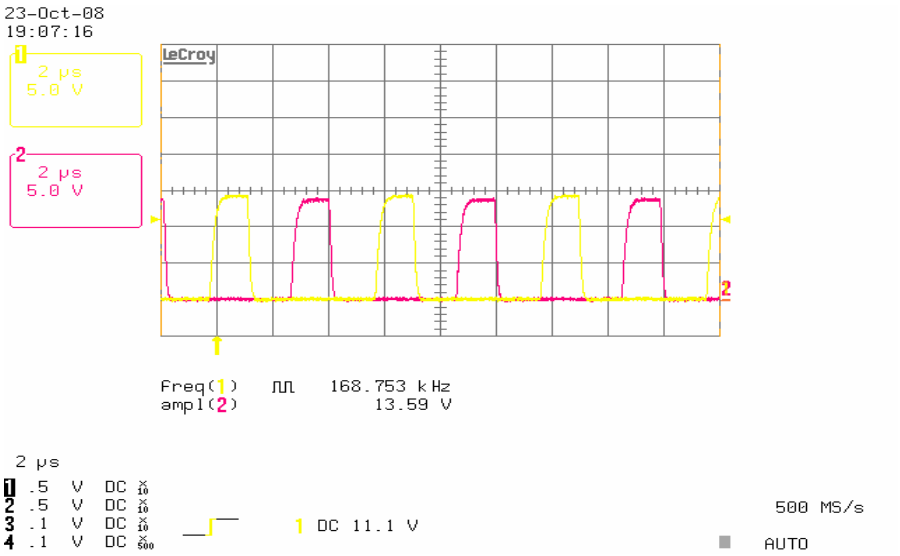


Figure 9b, LO (yellow) and HO (red) using an external bootstrap diode (CBS=0.1uF, CHO=CLO=1nF).

PCB Layout Guidelines

Figure 10 shows the IRS2168D ballast application circuit and Figure 11 shows an example of a good PCB layout. The layout is for a single layer board and includes both SMT and through-hole components. The following critical guidelines should be considered during the design of the layout:

1) Place all filter capacitors as close as possible to their respective pins. The filter capacitors include CVCC2, CBS, CCS, CSD, COC, CCOMP, CVCO, CPH and CVBUS. This will minimize the noise at each pin and prevent the IC from malfunctioning.
2) The ground connection to the IC programming components and filter capacitors should be connected directly to the COM pin of the IC. The COM pin of the IC should then be connected to the circuit power ground at a single point. Do not route the power ground through the COM connection of the IC or the programming components.
3) The double filter at VCC (R1, CVCC1, R2, CVCC2) together with the charge pump zener diode (DCP1) should be included in the circuit to filter high current spikes from flowing to VCC. High current spikes can occur in the charge pump during hard-switching or inductor saturation.
4) Keep the PFC MOSFET drain node (trace between DPFC, MPFC and LPFC) as short as possible to reduce dv/dt noise.
5) Maintain proper creepage distance between high-voltage and low-voltage traces to prevent arcing on the surface of the PCB.
6) Always use gate drive resistors (RLO, RHO, RPFC) between the gate drive output pins (LO, HO, PFC) and the gates of the external power MOSFETs. The gate drive resistors will prevent high currents from flowing in and out of these pins which can occur due to the slewing of the Miller capacitor between the drain and source of each external power MOSFET.

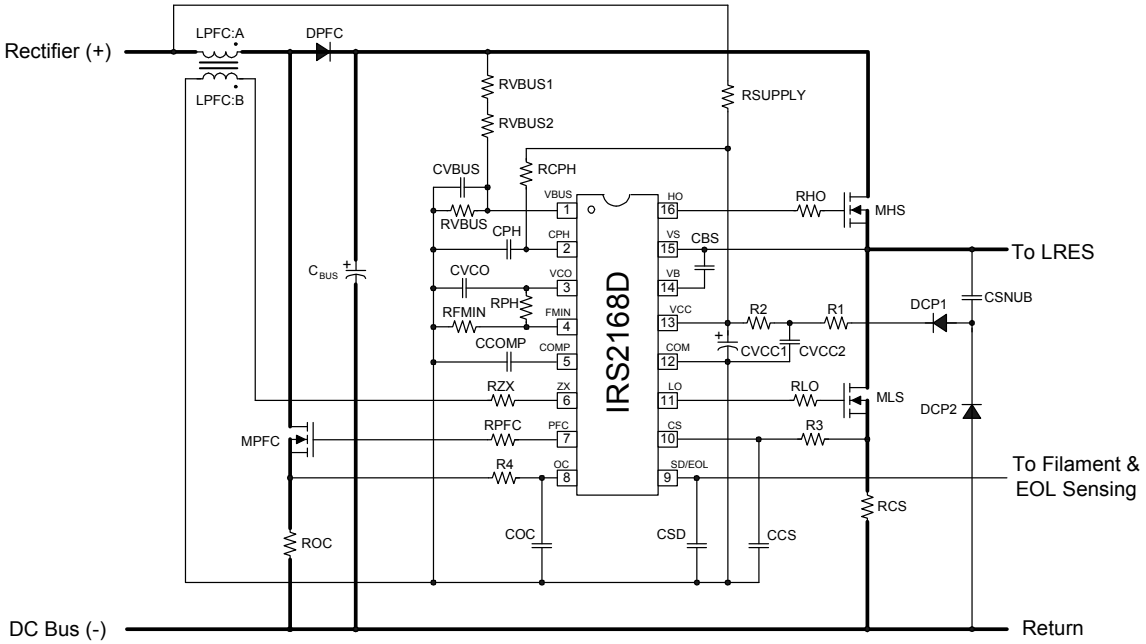


Figure 10, Ballast application circuit diagram.

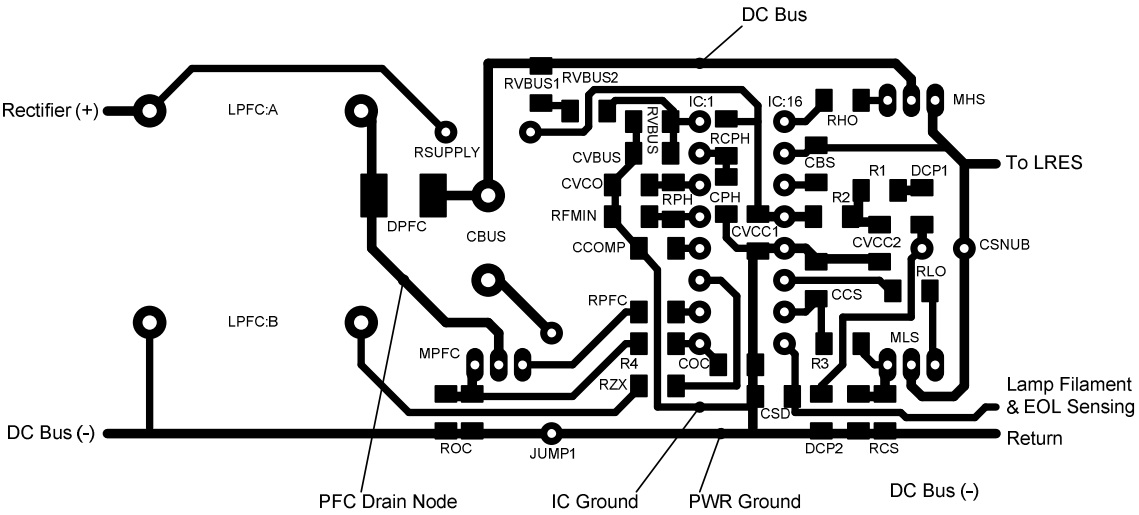


Figure 11, Single-layer PCB layout example with SMT and through-hole components.

Conclusions

The additional design information presented here should help improve the design of the ballast and help reduce potential problems. Ease of programming the ballast frequency, correct design of the PFC inductor, resonant tank design equations, design of the IC supply, and proper PCB layout guidelines, will all help speed up design time, improve performance, and improve the manufacturability and robustness of the final design.

A ballast design assistant (BDA) software is also available to help calculate component values, graph operating points, simulate waveforms, and generate complete schematics and bill of materials. The IRBDA software can be downloaded directly from the International Rectifier website at: www.irf.com.