Application Note AN-1135

PCB Layout with IR Class D Audio Gate Drivers

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0. Introduction

Through the use of IR's Class D audio chipsets, class D audio amplifiers are achieving superior efficiency and audio quality in today's audio market. To optimize the performance of class D audio amplifiers, designers should be diligent in designing the schematic, selecting appropriate components, and laying out the PCB (printed circuit board). While the first 2 steps have well established guidelines for design, the layout of a class D amplifier remains the most obscure part of the design process. The purpose of this application note is to highlight aspects of the PCB layout which require a designer's careful attention.

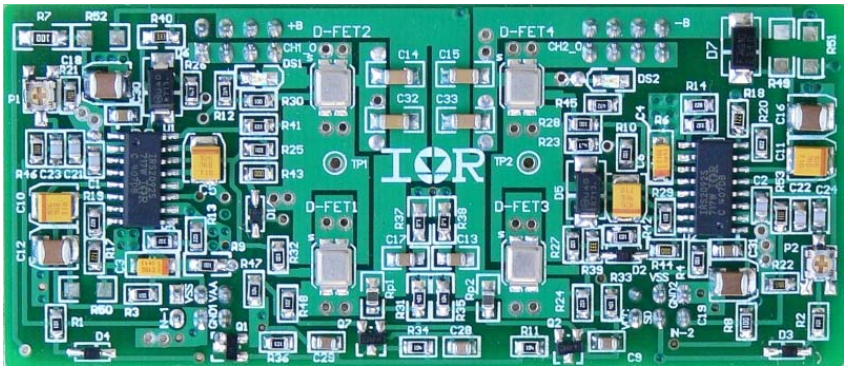
0-1. PCB and Class D Audio Performance

Same as conventional Class A/AB amplifiers, PCB is one of the key components which determine system performance. As amplifiers in Class D deal with much higher frequency components, the influence of PCB design is much more critical to the conventional audio amplifier design.

Three aspects of PCB layout contribute to the overall performance of a class D audio amplifier- component placement, current loops, and common impedance. Each factor has the potential to generate noise or distortion at the output. To control the influence of each factor, the designer should know which current loops, components, and nodes play an important role in the performance of the amplifier and why.

0-2. Component Placement

Component placement is a notable characteristic of PCB layout that affects the amplifier's performance. In another word, component layout determines maximum performance that can be obtained from the given components. Component placement takes the first step with an overall view of three larger factors; signal flow, noise coupling and thermal considerations. This determines where each group of circuitry should be. Then the designer designs details within the functional blocks with two fundamental aspects in mind – common impedance and current loop.



0-3. Current Loops

Current loops that carry large alternating currents have the greatest potential to generate EMI in the circuit and deserve higher priority in the layout. Characterized by high peak currents and sharp edges, the currents flowing through these loops can easily inject noise into surrounding circuitry if left unattended. To minimize the impact of these current loops in the amplifier, PCB designers should minimize the loop area and distance of these current paths. This technique will effectively prevent the switching current waveforms from distorting the audio signal at the output.

0-4. Common Impedance

Common impedance refers to the wires or traces shared by two or more separate circuits. Some circuits require minimum impedance to the ground while others prefer separate routing to ground to minimize cross couplings from adjacent circuits. PCB designers should minimize if not eliminate common impedance shared by noisy and quiet circuits. The concept of “star ground” effectively prevents common impedance from affecting the performance of the amplifier. A detailed discussion on this topic can be found in the “Grounding” section of this application note.

1. Laying Out Class D Power Stages

Class D audio amplifiers can be separated into 2 stages – the gate driving stage and the output stage. Each stage is characterized by specific current loops, components, and common impedances that influence the quality of the amplification. In understanding the composition of each stage, PCB designers can proceed to layout a class D audio amplifier with optimized performance and efficiency.

1-1. How to Place the Key Components

1-1-1. Placement Determines Maximum Performance

The first and most important step for PCB designers is to group components dedicated to a common purpose, such as:

- the audio input circuitry
- the PWM control circuitry
- the gate driver stage
- the switching stage
- the housekeeping voltages required to sustain the performance of the IC
- the shutdown circuitry for turning off the amplifier

By identifying which components belong together, the PCB designer can decide the placement of the remaining circuitry by coupling them appropriately into open areas of the board.

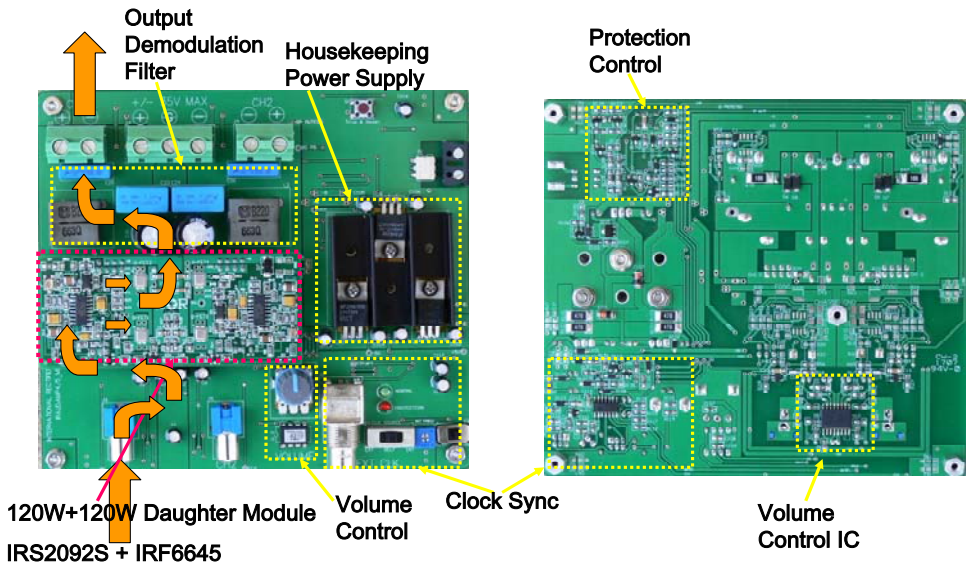


Figure 1 Overview of PCB Design in the IRAUDAMP5

1-1-2. Noise Considerations

There are functional blocks that generate noise. There are functional blocks that are sensitive to noise. The PCB designer should identify them and find out the best combination of the placement based on these facts and mechanical and thermal requirements.

Noise sensitive functions
- the audio input circuitry
- the PWM control circuitry

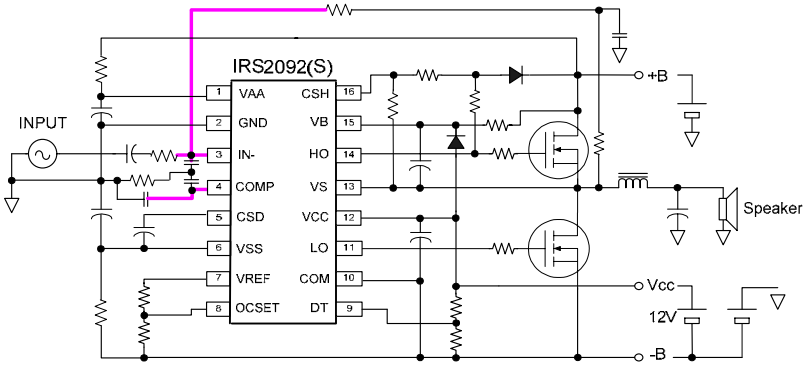


Figure 2 The Most Noise Sensitive Node

Noise generating functions
- the gate driver stage
- the switching stage

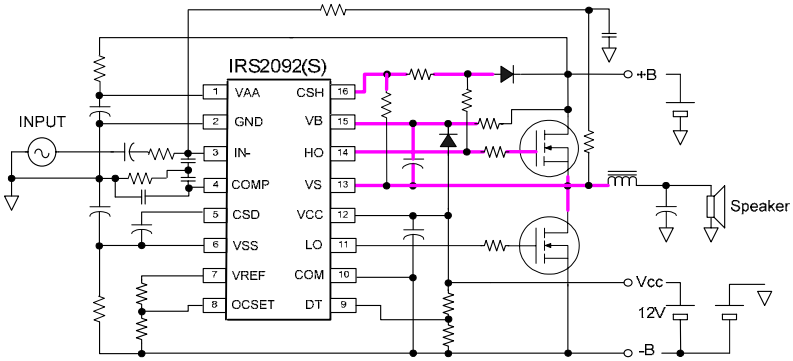


Figure 3 The Most Noisy Nodes

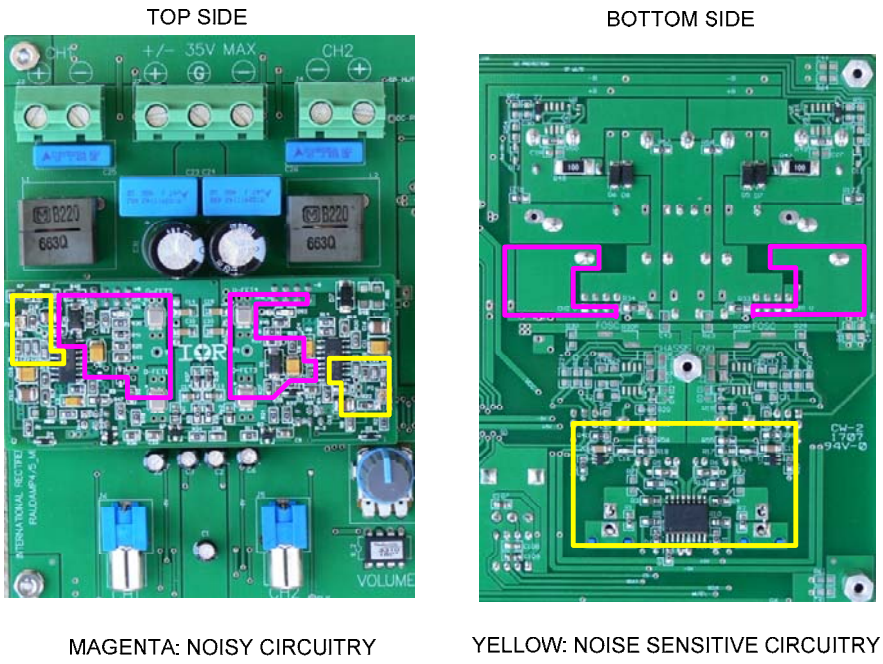


Figure 4 Placement of Noise Sensitive and Noisy Elements on IRAUDAMP5

1-1-3. Thermal Considerations

Surface mount power devices, such as DirectFET, requires certain area to dissipate heat. Power devices are better to be placed with adequate space in between, but should not be too far to accommodate smaller current loop area.
Components that are thermally weak, such as electrolytic capacitors, should stay away from power devices.

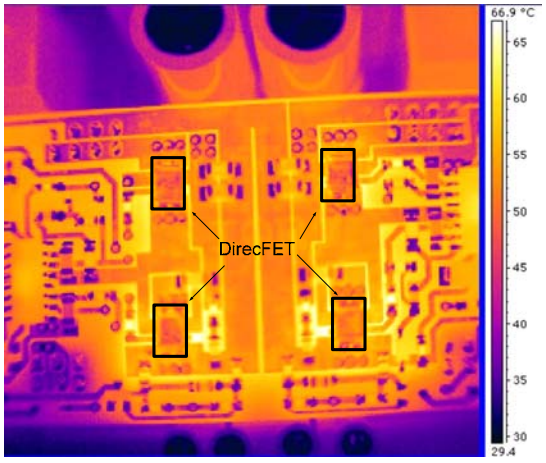


Figure 5 Thermograph of IRAUDAMP5 Daughter Board with Four DirectFETs

1-1-4. Key Components Placement

Taking the above points into consideration, the PCB designer starts placing key components in a given open space. Typical key components that affect overall design and should be regarded in this design stage are followings.

- Audio signal input connector
- Error amplifier OPA
- Gate driver IC
- Power MOSFET
- Bus capacitor
- Output LPF
- Power supply inlet
- Speaker output connector

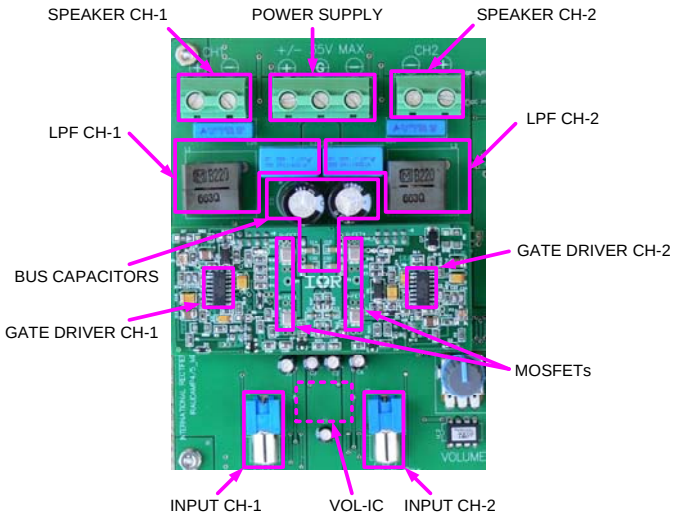


Figure 6 Key Component Floor Plan Example (IRAUDAMP5)

1-2. How to Layout the Gate Drive Stage

1-2-1. Current Loops in MOSFET Gate Drive

There are 5 current loops in the gate driving stage involved in the turning on and off of the switching MOSFETs. Each current loop carries currents with sharp edges and large peaks. This high frequency switching action could potentially add current-induced noise to the output of the amplifier. PCB designers should minimize the loop area and distance to contain the EMI generated by the currents charging and discharging the gate of the MOSFETs.

This section picks up IRS2092 as an example to explain these 5 critical current loops which are common to IR's digital audio gate driver family.

During the turn on of the low side MOSFET, three current loops are active around the gate driving stage of the amplifier, as shown in Figure 7:

- The green loop is the path of current discharging the gate of the high side MOSFET. Current carries charge away from the gate of the high side MOSFET through the internal MOSFET between HO and VS in the audio IC.
- The pink loop is the path of current charging the gate of the low side MOSFET. Charge supplied by the bus capacitor of V_{CC} traverses the internal MOSFET between VCC and LO in the IRS2092 to charge the gate of the low side MOSFET.
- The orange loop is the path of current charging the high side bootstrap capacitor, C_{VBS}. During low side turn on, the VS node is pulled down to –B allowing the diode between VCC and VB to turn on. The bus capacitor of VCC proceeds to charge the bootstrap capacitor in preparation for high side turn on.

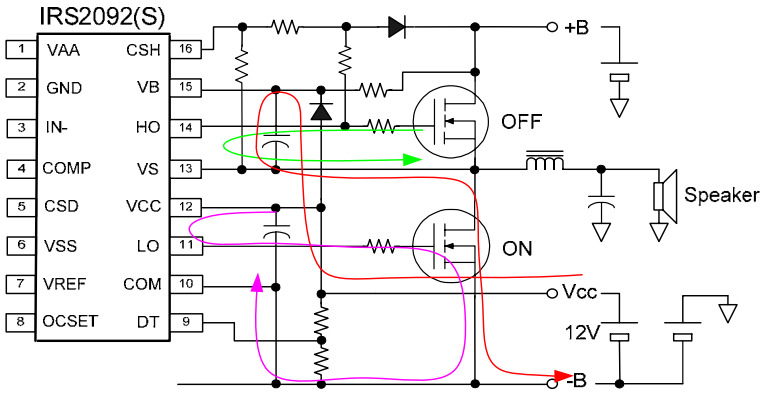


Figure 7 Current Loops During Low Side Turn On

During the turn on of the high side MOSFET, 2 current loops are active around the gate driving stage, as shown in Figure 8:

- The blue loop is the path of current discharging the gate of the low side MOSFET. Current carries charge away from the gate of the low side MOSFET through the internal MOSFET between LO and COM in the audio IC.
- The red loop is the path of current charging the gate of the high side MOSFET. Charge supplied by the high side boot strap capacitor traverses the internal MOSFET between VB and HO in the IRS2092 to charge the gate of the high side MOSFET.

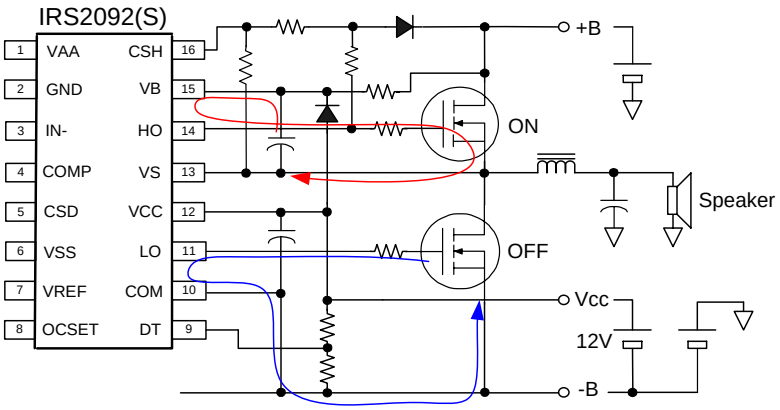


Figure 8 Current Loops During High Side Turn On

The current loops active during each switch transition must be laid out carefully to optimize the performance of the amplifier. The IRAUDAMP4 and IRAUDAMP5 reference board demonstrate how to route current loops effectively in the gate driving stage of a Class D audio amplifier to minimize EMI. These reference designs use the IRS20955S and IRS2092S Class D audio IC respectively and IRF6645 DirectFETs.

1-2-2. How to Layout the Gate Drive Signals

Figure 9 depicts the discharging path of the high side MOSFET during high side turn off whereas figure 10 depicts the charging path of the high side MOSFET. Both the charging and discharging routes traverse a short distance given the size of the board. Furthermore, the path to the gate of the MOSFET from the IC closely tracks the return path to minimize the loop area. The layout of these 2 current loops effectively minimizes the EMI generated by the sharp peak currents switching onboard.

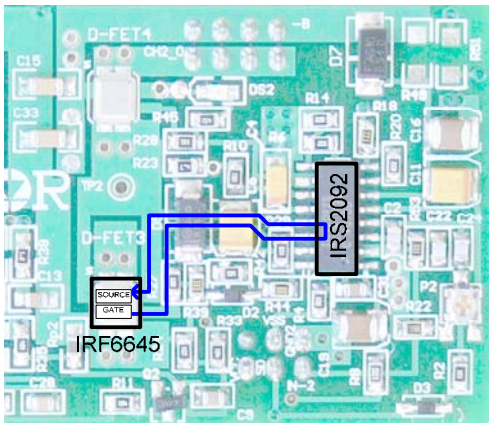


Figure 9 Discharging Path of High Side MOSFET

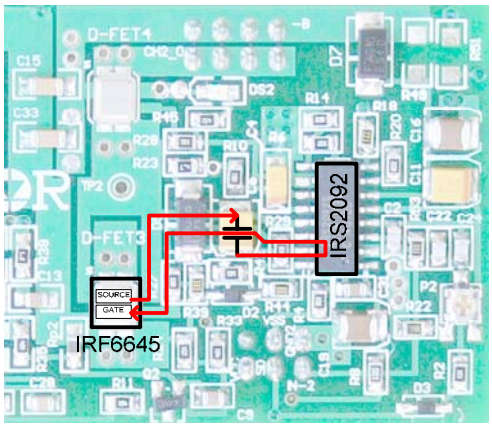


Figure 10 Charging Path of High Side MOSFET

1-2-3. Supply Bypass Capacitor Placement

During operation, the IRS2092S sources and sinks high frequency currents in the bus capacitors of V_{DD}, V_{CC}, and V_{BS}- C_{VDD}, C_{VB}, and C_{VCC}. PCB designers should make an effort to shorten the distance of the traces from the capacitors to the IC as much as possible. The effect of the trace length from the bus capacitors to the IRS2092S is twofold. First, these capacitors belong to major and minor current loops, which are often potential sources of EMI. Secondly, the stray inductances introduced by traces from the capacitors to their respective pins on the IC could easily distort the current waveforms going through these capacitors. In the IRAUDAMP5 layout in figure 11, the bus capacitors lie next to the IC to prevent either effect from hampering the performance of the amplifier.

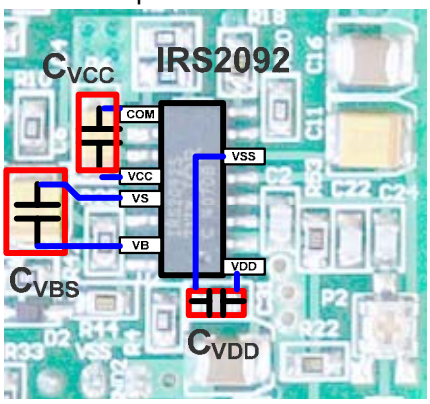


Figure 11 Bus Capacitors Placed Adjacent to the IC

1-3. How to Layout the MOSFETs and the Power Paths

1-3-1. Current Loops in Power Paths

There are 3 current loops carrying high frequency currents through the switching MOSFETs and the low pass filter:

- The orange loop is active when the high side MOSFET is turned on to allow current to flow from the positive terminal of the +B capacitor through the high side MOSFET. The current then proceeds to flow from the low pass filter to the negative terminal of the +B capacitor.
- The green loop is active when the low side MOSFET is turned on to allow current to flow from the positive terminal of the –B capacitor through the low pass filter. The current then proceeds to flow from the low side MOSFET to the negative terminal of the –B capacitor.

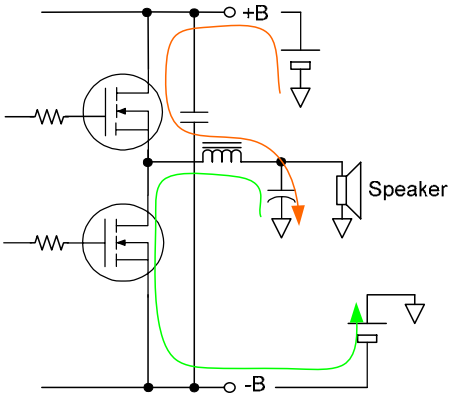


Figure 12 Current Loops in the MOSFETs and Power Paths

- The blue loop in figure 13 is the reverse recovery current of the body diodes in the high side and low side MOSFETs. During each switching cycle, the reverse recovery charge required to turn off the body diodes injects current spikes into the negative voltage bus. A capacitor dedicated to absorbing the high frequency noise should be placed closely to the drain of the high side MOSFET and source of the low side MOSFET to minimize the current loop area and distance.

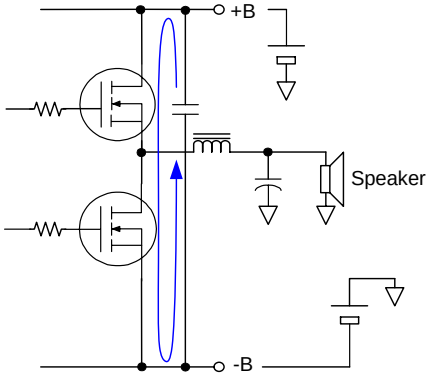


Figure 13 Reverse Recovery Current Loop in the Power Paths

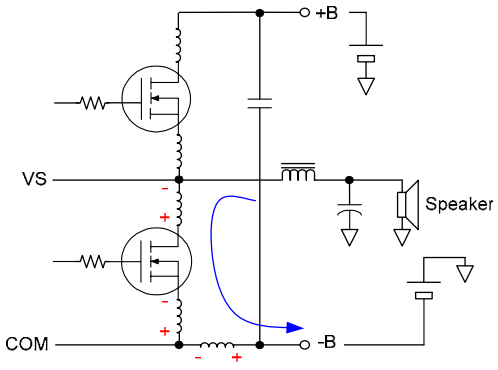


Figure 14 Parasitic Inductances in Half Bridge Configuration

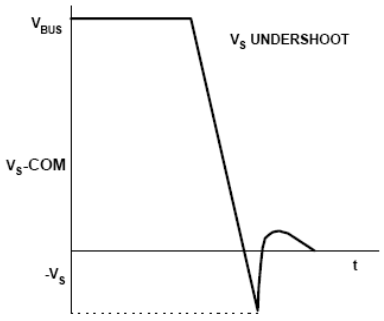


Figure 15 V_S Voltage Spike Waveform

Among the three current loops mentioned in this stage, the reverse recovery current has the most high frequency components. The orange and green loops contain the second most high frequency components. PCB designers should prioritize the loop layouts accordingly when minimizing loop areas and distance. The green loop induces negative voltage spike as shown in figure 14 and 15. Negative spike at VS should be minimized by reducing stray inductances along the current path.

1-3-2. Over Current Sensing

The IC uses voltage drop across the drain and source to sense the load current. When either the low side or high side MOSFET is turned on, the IC will measure the voltage across the drain and source of that MOSFET and compare the value to a user set threshold. When the voltage measured exceeds the trip level, the IC engages shutdown mode and terminates IC operation for a set length of time.

OCP in the IRS20955 and IRS2092 is based on sensing voltage across the drain and source of the low side and high side MOSFET. Three pins- COM, VS, and CSH- are used to measure the V_{DS} of both MOSFETs. During low side turn on, the IC measures the voltage difference between COM and VS; conversely, during high side turn on, the IC measures the voltage difference between VS and CSH.

To ensure that the actual drain source voltage is being measured, COM, VS, and CSH must be as close to the drain and source of the low side MOSFET and the drain and source of the high side MOSFET as possible as shown in figure 16. Note that this requires VS to be close to the drain of the low side MOSFET as well as the source of the high side MOSFET. A good way to achieve this is by placing the low side MOSFET and high side MOSFET close to one another.

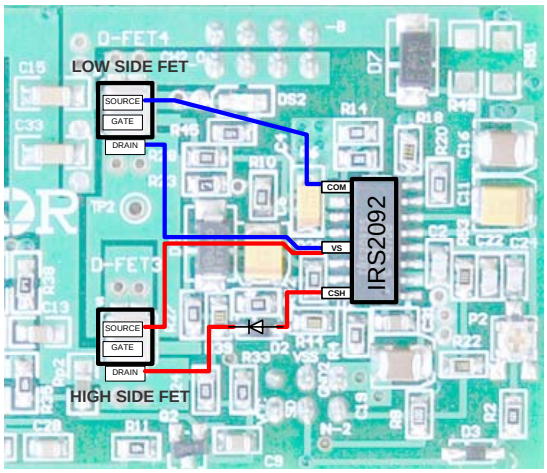


Figure 16 $R_{DS(ON)}$ Based Current Sensing Routing Example

1-3-3. Common Impedance

Common impedance should be minimized between nets that are shared by the switching MOSFETs of different channels. –B and +B should be routed separately from the voltage supplies to the sources of the low side MOSFETs and the drains of the high side MOSFETs for each channel. Essentially, the star ground concept mentioned in the previous stage should be applied in this stage as well to optimize the performance of the class D audio amplifier. Similarly, the ground reference for the LPF should be routed separately from the ground terminal.

2. Two Grounding Concepts

Class D amplifiers have two reference potentials that are referred to by all switching signals in the amplifier- the audio signal reference (analog ground) and the gate drive reference. The nature of each reference requires the PCB designers to apply different grounding concepts to the audio signal reference and gate drive reference.

Table 1 Audio Signal Reference and Gate Drive Reference

	Audio Signal Reference	Gate Drive Reference
Voltage Potential	Ground	Negative Bus Voltage
Referenced by	- Audio Input - Error amplifier - IC input circuitry - Positive and Negative Bus Capacitors - Audio Output	- Gate driving outputs of IC - Half bridge MOSFETs
Layout Consideration	Avoid common impedance between the ground reference of different channels as well as the ground reference for the input and the output.	The gate driving stage contains high frequency current that could contaminate signals in other parts of the amplifier. These high frequency signals must be properly separated from input signal controller to insure optimal performance of the amplifier.
Preferred Layout Technique	**Star Ground Concept**	**Ground Plane Concept**

2-1. Star Ground Concept

Noisy circuitries in the audio amplifier inject noise into ground wires in the form of alternating current. Combined with the impedance in the ground wires of the PCB, high frequency currents become high frequency voltage perturbations in the ground wire. In other words, potential at one point of the ground wire could be different from the voltage potential at another point. Ideally, the PCB designer should design the layout such that the ground referenced by every part of the PCB is equipotent as illustrated in figure 17. The concept of star ground effectively prevents noisier parts of the amplifier from interfering with performance in quieter areas.

Star ground is essentially designating a single terminal on the PCB as the “star ground” of the amplifier. All other ground wires and planes will connect to this point through separate traces, resulting in a “star” pattern around the central ground. The PCB designer should designate different paths to the “star ground” for different output channels of the amplifier as well as the ground referenced by the inputs of the IC.

Follow the simple steps below to effectively implement “star ground”:

1. Establish a “star ground” on the PCB. This point is usually the terminal through which Earth ground connects to the ground of the PCB.
2. Wire the ground reference for each channel input separately to “star ground.”
3. Wire the ground reference for each channel output separately to “star ground.”
4. Pour separate ground planes for the input section of each channel.
5. Connect each ground plane through different traces to “star ground.”
6. Group together circuitry that can share common impedance to ground without affecting the performance of the amplifier.
7. Wire the ground references for each group to “star ground” separately.

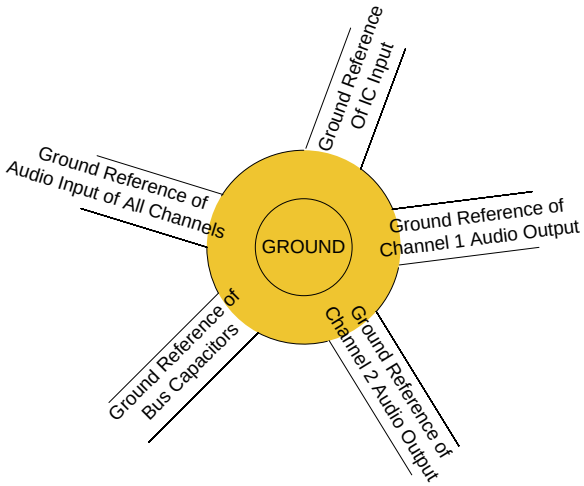


Figure 17 “Star Ground” of a Class D Amplifier

2-2. Ground Plane Concept

A ground plane is a layer of copper that carries a voltage referenced by signals in the amplifier. These planar constructs serve 3 purposes in PCB layout – ensuring that the same voltages referenced at different points of the PCB are the same, shielding the input of the amplifier from the high frequency switching onboard, and allowing the designer to easily ground parts of the PCB without having to run a separate trace.

Effectively applying the ground plane concept to the negative bus voltage is crucial for optimal performance of the amplifier. The gate driving stage and switching MOSFETs all refer to the negative bus voltage during operation. The high frequency switching action in this stage of the amplifier potentially couples noise into the negative bus voltage and surrounding circuitry. PCB designers should apply the ground plane concept to quarantine the switching noise generated in this stage.

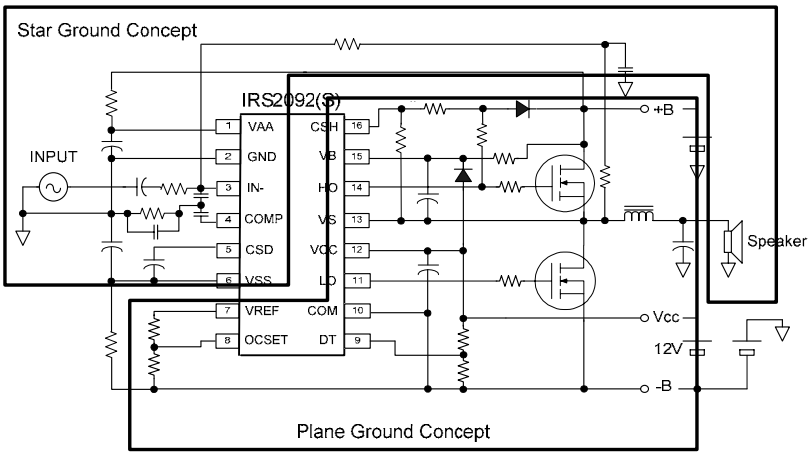


Figure 18 Example of Adoption of Star Ground and Ground Planes in IRS2092 Design

2-3. Shielding

In a design with multi layers, care should be taken for capacitive coupling between the layers. Keep in mind that the Class D amplifier is dealing with >100dB signal-to-noise ratio. A small amount of noise injecting the front end stage could result significant performance degradations. Fig 19 and Fig 20 show a recommended shielding structure for the IRS2092.

The noisiest part of the design is the high side MOSFET and its gate driver stage. Try to avoid stray capacitance between the nodes in the high side circuitry and input OTA stage as much as possible.

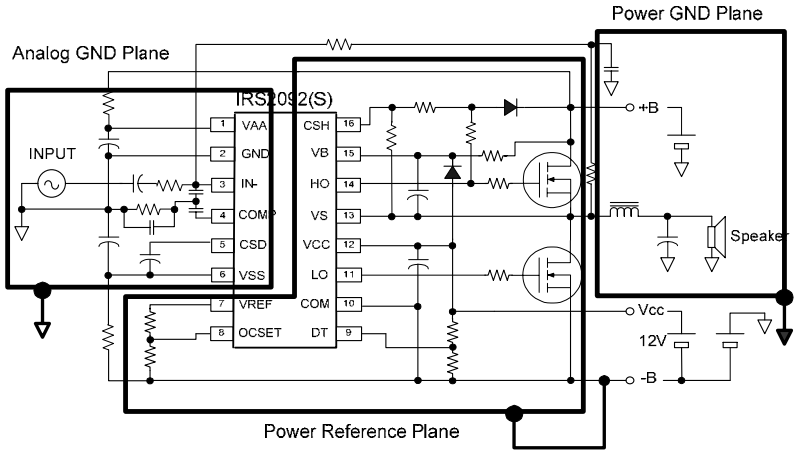


Figure 19 Conceptual View of Shielding Planes with IRS2092

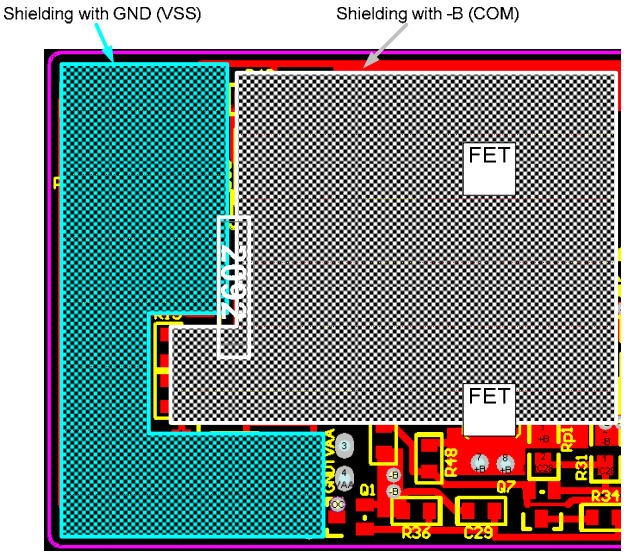


Figure 20 Design Example of Shielding Planes in IRAUDAMP5

3. Summary

Step-by-step design tips on how to layout a Class D amplifier properly is discussed. A good PCB layout occupies small area and yields good overall performance. By following the above guidelines, the PCB designer should be able to build high performance Class D amplifier in a smallest size.

Revision History

2008.5.28

- Minor English mistakes corrected

- Some sentences re-written for clarification