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PFC Converter Design with IR1150 One Cycle Control IC

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This Application Note describes the design methodology of a Continuous Conduction Mode Power Factor Correction circuit utilizing a boost converter and featuring the IR1150S PFC IC. The IR1150 is based on International Rectifier's proprietary "One Cycle Control" technique for PFC converter control. This application note presents a complete, step-by-step, design procedure including converter specifications and necessary design tradeoffs.

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Topics Covered

- *Power Factor Correction*
- *One Cycle Control operation*
- *IR1150 Detailed Description*
- *Design procedure and example*
- *Design Tips*

➢ *For additional data, please visit our website at:*
http://www.irf.com/product-info/smps/
http://www.irf.com/e/ir1150ppdus.html/

Keywords: PFC, Power Factor Correction, THD, One Cycle Control, OCC

Introduction

Power factor is defined as the ratio of **real** power to **apparent** power, where **real** power is the time integral of the instantaneous power measured over a full period and the **apparent** power is simply the product of the rms voltage and rms current measured over the entire period.

$$\text{Real Power} = \frac{1}{T}\int_0^T V_{IN} I_{IN} dt \qquad (1)$$

$$\text{Apparent Power} = V_{inRMS} \cdot I_{inRMS} \qquad (2)$$

$$PF = \frac{P_{REAL}}{P_{APPARENT}} \qquad (3)$$

For a sinusoidal voltage this can be written as:

$$PF = \frac{V_{rms} \cdot I_{rms1} \cdot cos(\phi)}{V_{rms} \cdot I_{rms}} = \frac{I_{rms1}}{I_{rms}} cos(\phi) \qquad (4)$$

V_{rms} is the line voltage RMS value

I_{rms} is the line current RMS value

I_{rms1} is the line current fundamental harmonic

ϕ is the displacement angle between voltage and current

In this case power factor can be split into distortion factor and displacement factor:

$$k_D = \frac{I_{rms1}}{I_{rms}}; k_\phi = cos(\phi) \qquad (5)$$

Phase shift between the voltage and current waveforms is introduced by the reactive nature of the input, either inductive or capacitive.

In a purely resistive load, the voltage and current will be sine waves, in phase, true power will equal apparent power and PF = 1.

$$I_{rms} = \sqrt{\sum_{n=1}^{\infty} I_{rms_n}^2} \qquad (6)$$

$$THD = \frac{\sqrt{I_{rms}^2 - I_{rms1}^2}}{I_{rms1}^2} \qquad (7)$$

One Cycle Control for PFC Applications

The operation of the one cycle control is analyzed in detail in several papers [3][4][5].

The converter output voltage V_o is scaled down thru the output divider and is presented at the input of the error amplifier V_{FB}. The error amplifier is used to provide loop compensation and to generate the error signal or modulation voltage V_m.

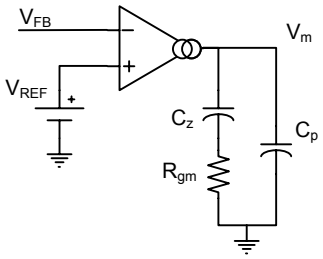


Figure 1 - Error Amplifier

The core of the One Cycle control is a resettable integrator. This block integrates the modulation voltage and is reset at the end of every switching cycle.

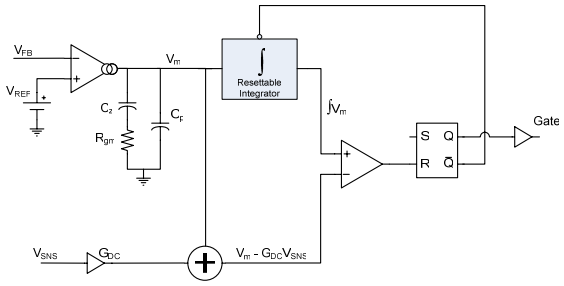


Figure 2 - Core of the One Cycle Control

Since the voltage loop bandwidth is very small the modulation voltage will vary very slowly and can be considered constant during a switching cycle. This means that the output of the integrator will be a linear ramp. The slope of the integrator ramp is directly proportional to the output voltage of the error amplifier, v_m.

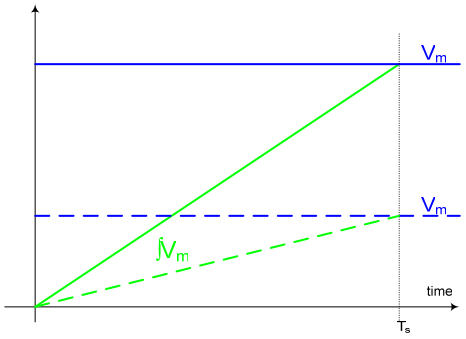


Figure 3 - Resettable integrator characteristic

An important characteristic is that integration time constant of the integrator must match the switching period, so that at the end of each cycle the ramp will match the integrated value.

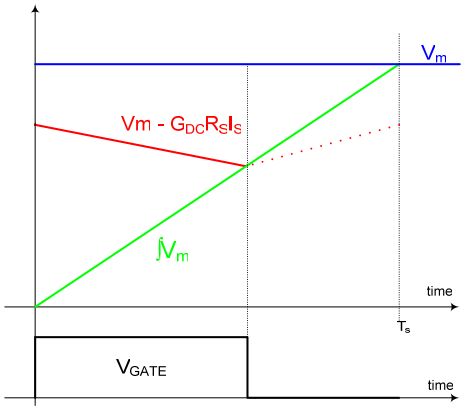


Figure 4 - PWM Signal Generation

The reference for the PWM comparator is obtained by subtracting the voltage across the current sense resistor from the modulation voltage:

$$v_m - G_{DC} \cdot v_{SNS} \qquad (8)$$

This is the required input configuration to the general OCC PWM in order to properly control the boost converter with trailing edge modulation.

By providing a reference threshold dependant on the input current and a ramp signal dependant on the output voltage, the required control of the converter duty cycle is realized to achieve output voltage regulation and power factor correction.

This control technique does not require direct line voltage sensing: the line voltage information is contained in the inductor current.

IR1150 Detailed Description

The IR1150 control IC is intended for boost converters for power factor correction operating at a fixed frequency in continuous conduction mode. The IC operates with essentially two loops, an inner current loop and an outer voltage loop.

The inner current loop sustains the sinusoidal profile of the average input current based on the dependency of the pulse width modulator duty cycle on the input line voltage, to determine the analogous input line current. Thus, the current loop exploits the imbedded input voltage signal to command the average input current following the input voltage. This is true so long as operation in continuous conduction mode is maintained.

There will be some amount of distortion of the current waveform as the line cycle migrates toward the zero crossing and as the converter operates at very light loads given that the inductor has a finite inductance. The resultant harmonic currents under these operating conditions will be well within the Class D specifications of EN61000-3-2, and therefore not an issue.

The outer voltage loop controls the output voltage of the boost converter and the output voltage error amplifier produces a voltage at its output, which directly controls the slope of the integrator ramp, and therefore the amplitude of the average input current. The combination of the two control elements controls the amplitude and shape of the input current so as to be proportional to and in phase with the input voltage.

The IC employs protection circuits providing for robust operation in the intended application and protection from system level over current, over voltage, under voltage, and brownout conditions.

The UVLO circuit monitors the V_{CC} pin and maintains the gate drive signal inactive until the V_{CC} pin voltage reaches the UVLO turn on threshold, $V_{CC\ ON}$.

The Open Loop Protection (OLP) prevents the controller to operate if the voltage on the feedback pin hasn't exceeded 20% of its nominal value. If for some reason the voltage control loop is open, the IC will not start, avoiding a potentially catastrophic failure.

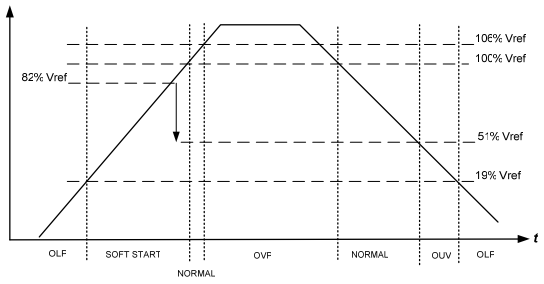


Figure 5 - Output Protections

As soon as the V_{CC} voltage exceeds this threshold, provided that the V_{FB} pin voltage is greater than 20%V_{REF}, the gate drive will begin switching.

In the event that the voltage at the V_{CC} pin should drop below that of the UVLO turn off threshold, $V_{CC\ UVLO}$, the IC then turns off, gate drive is terminated, and the turn on threshold must again be exceeded in order to re start the process.

A dedicated programmable Over Voltage Protection pin (OVP) is available for to protect the output from overvoltage. The PFC voltage feedback loop is usually very slow. If the output voltage exceeds the set OVP limit, the gate drive will be disabled, until the output voltage will approach again its nominal value.

Finally an Output Under Voltage protection OUV is provided: in case of overload or brown out, the converter will automatically limit the current: as a result the output voltage will drop. If the drop exceeds 50% of the nominal output voltage, the controller will shut down and restart.

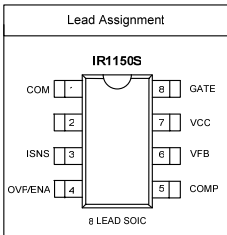
The oscillator is designed such that the switching frequency of the IC is programmable via an external resistor at the FREQ pin. The design incorporates min/max restrictions such that the minimum and maximum operating frequency shall fall within the specified range of 50kHz to 200kHz.

It is generally possible to run the IC at a lower switching frequency, but given the large value of the programming resistor that may lead to inaccurate frequency trimming, outside the range of tolerance specified on the Data Sheet.

An additional feature of the IR1150S is the ability to force the IC into a "sleep" mode. In the sleep mode, the internal blocks of the IC are disabled and the IC draws a very low quiescent current of 200µA. This is a desirable feature designed to reduce system

power dissipation to an absolute minimum during a standby mode, or to shut down the converter at the discretion of the system designer. The sleep mode is activated any time the OVP pin, (pin 4), is at a voltage level lower than 0.62V (typ).

The gate drive output provides sufficient drive capability to efficiently drive MOS gated power switches typical of the application.



Pin#	Symbol	Description
1	COM	Ground
2	FREQ	Frequency Set
3	ISNS	Current Sense
4	OVP/ENA	Overvoltage Fault Detect / Enable
5	COMP	Voltage Loop Compensation
6	VFB	Output Voltage Sense
7	VCC	IC Supply Voltage
8	GATE	Gate Drive Output

Figure 6 - IR1150S Pinout

PFC CONVERTER DESIGN PROCEDURE

This section describes a typical design procedure for a Continuous Conduction Mode boost converter for power factor correction using the IR1150S control IC. Additionally, some of the design tradeoffs typical of PFC converter design are discussed.

A schematic diagram is presented as a reference to a step by step design procedure for designing a typical 300W PFC converter.

An IR1150S Demo Board [2] is available from International Rectifier which highlights the performance of the IR1150 and was designed in accordance with the design procedure presented in this application note.

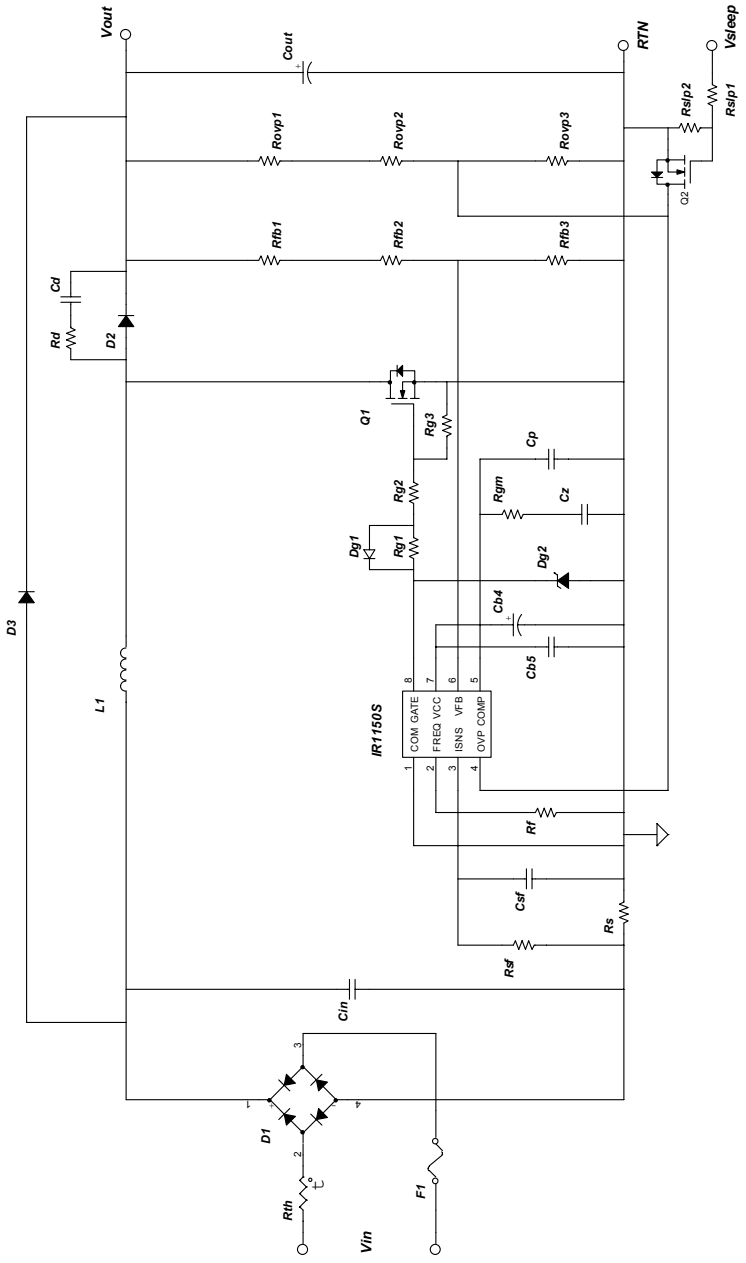
Converter Specifications

AC Input Voltage (rms)	85V(min) - 264V(max)
Input Line Frequency	47-63Hz
Target Efficiency	92% min @ 90VAC / 300W
Power Factor (PF)	0.99 min @ 115VAC / 300W
Harmonic Distortion	4% max @ 115VAC / 300W
AC Inrush Current (peak)	35A max @ 230VAC / 300W
Maximum Ambient	50°C
Operating Temperature	
Nominal DC Output Voltage	385V
Maximum DC Output Voltage	425VDC
Minimum Output Holdup Time	30msec @ 285V_O
Converter Switching Frequency	100kHz
Maximum Soft Start time	50msec

Converter Input and Output Variables Defined

$P_{OUT(MAX)}$	Maximum converter output power delivered to load
$P_{IN(MAX)}$	Maximum converter input power drawn from AC source
η_{MIN}	Minimum worst case efficiency of converter
$I_{IN(RMS)MAX}$	Maximum rms value of input current drawn from AC source
$I_{IN(PK)MAX}$	Maximum peak value of input current drawn from AC source
$I_{IN(AVG)MAX}$	Maximum average value of input current drawn from AC source
$V_{IN(RMS)MIN}$	Minimum rms value of input voltage supplied by AC source
$V_{IN(PK)MIN}$	Minimum peak value of input voltage supplied by AC source

Converter Schematic Diagram



Maximum Input Power and Currents

Majority of the converter design is based on low line current. That's the worst case condition for efficiency and input currents.

(Assume PF to be 0.99 or greater at low line)

Maximum input power can be calculated assuming a nominal efficiency at low line:

$$P_{IN(MAX)} = \frac{P_{O(MAX)}}{\eta_{MIN}} = \frac{300W}{0.92} = 326W$$

The maximum rms AC line current is calculated at the minimum input AC voltage:

$$I_{IN(RMS)MAX} = \frac{P_{O(MAX)}}{\eta_{MIN}(V_{IN(RMS)MIN})PF}$$

$$I_{IN(RMS)MAX} = \frac{300W}{0.92(85V)0.998} = 3.8A$$

Assuming sinusoidal AC current, the peak value of the AC current can be calculated:

$$I_{IN(PK)MAX} = \frac{\sqrt{2}(P_{IN(MAX)})}{V_{IN(RMS)MIN}}$$

$$I_{IN(PK)MAX} = \frac{1.414(326W)}{85V} = 5.4A$$

The AC Line input average current can be calculated assuming sinusoidal waveform:

$$I_{IN(AVG)MAX} = \frac{2 \times I_{IN(PK)MAX}}{\pi}$$

$$I_{IN(AVG)MAX} = \frac{2 \times 5.4A}{\pi} = 3.4A$$

High Frequency Input Capacitor Requirements

$$C_{IN} = k_{\Delta I_L} \frac{I_{IN(RMS)MAX}}{2\pi \times f_{SW} \times r \times V_{IN(RMS)MIN}}$$

$$C_{IN} = 0.3 \frac{3.8A}{2\pi \times 100kHz \times 0.06 \times 85V} = 0.335\mu F$$

Where:

$k_{\Delta IL}$ = Inductor current ripple factor (30% in this design)

r = maximum high frequency voltage ripple factor ($\Delta V_{IN}/V_{IN}$), typically between 3% – 9%, 6% used for this design.

C_{IN} = 0.330µF, 630V

High frequency capacitor is typically a high quality film capacitor rated at beyond the worst case peak of the line voltage. Care must be taken to avoid too large a value as this will introduce current distortion.

This capacitor can be considered part of the EMI input filter: its main purpose is to bypass the high frequency component of the input current with the shortest possible loop.

Boost Inductor Design

Power switch duty cycle must be determined at $V_{IN(PK)MIN}$. This will represent the peak current for the inductor, at the peak of the rectified line voltage at minimum line voltage.

$$V_{IN(PK)MIN} = \sqrt{2} \times V_{IN(RMS)MIN} = 120V$$

$$D = \frac{V_O - V_{IN(PK)MIN}}{V_O} = \frac{385V - 120V}{385V} = 0.69$$

$$\Delta I_L = 0.2 \times I_{IN(PK)MAX} = 0.2 \times 5.4A \cong 1.1A$$

$$I_{L(PK)MAX} = I_{IN(PK)MAX} + \frac{\Delta I_L}{2} = 5.4A + \frac{1.1A}{2} \cong 6A$$

$$L_{BST} \frac{V_{IN(PEAK)MIN} \times D}{f_{SW} \times \Delta I_L} = \frac{120V \times 0.69}{100kHz \times 1.1A} = 752.7\mu H$$

ΔI_L is based on the assumption of 20% ripple current. This is another area where design tradeoffs must be considered.

A smaller value of ripple current would be beneficial in terms of reduced distortion, output capacitor

ripple current at f_{SW}, peak current in the power switch and EMI

However the trade-off here is an increased inductance value to support the reduced ripple current, resulting in increased size and cost.

Care must be taken for a given core selection within a given design that the core does not saturate at peak current levels.

Conversely, a higher value of allowable ripple current, while resulting in a lower required inductor value, will negatively impact performance in the areas previously pointed out.

Cost trade-offs are typical for core materials vs. dissipation, temperature, and inductance roll off with increasing current levels. Consult core manufacturer's data books and application notes for detailed inductor design considerations. Detailed inductor design is beyond the scope of this application note.

Output Capacitor Requirements

Output Capacitor design in PFC converters is typically based on hold up time requirements. Typically, with a proper design, ripple voltage and current in the capacitor will not be an issue.

Typical values of capacitor for PFC applications are 1µF to 2µF per watt of output power.

$$C_{OUT(MIN)} = \frac{2 \cdot P_O \cdot \Delta t}{V_O{}^2 - V_{O(MIN)}{}^2} \qquad (9)$$

$$C_{OUT(MIN)} = \frac{2 \cdot 300W \cdot 30ms}{(385V)^2 - (285V)^2} = 269\mu F$$

Minimum capacitor value must be derated for capacitor tolerance, -20% in this case, in order to guarantee minimum capacitance requirement is satisfied, thus assuring minimum hold up time.

$$C_{OUT} = \frac{C_{OUT(MIN)}}{1 - \Delta C_{TOL}} = \frac{269\mu F}{1 - 0.2} = 336\mu F$$

Standard value of 330µF is used in this case.

CONTROL SECTION DESIGN

Output Voltage Divider

Output voltage of the converter is set by voltage divider R_{FB1}, R_{FB2}, and R_{FB3}.

The total impedance of this divider string should be selected high enough in value so as to reduce power dissipation in divider. This is of particular concern in terms of meeting stringent standby power specifications, and beneficial in optimizing overall system efficiency.

Practical limits do exist however on the maximum impedance of the divider string. The resistor values must not be selected so high as to introduce excessive additional voltage error to the output voltage error amplifier resulting from input bias currents of the amplifier.

A reasonable compromise for divider string overall impedance is a target of approximately 1MΩ.

R_{FB1} and R_{FB2} are typically split equally in value to create the upper resistor in the divider to keep the maximum voltage across each resistor within the voltage rating of these devices, (typically 250V).

Divider resistors are selected with a ±1% tolerance in order to minimize output voltage set point error. The resistor tolerances will stack up in addition to tolerance of the error amplifier reference and the error introduced to the error amplifier due to input bias currents and input offset voltage.

$R_{FB1} = R_{FB2} = 499K\Omega$, 1% tolerance.

This is a standard 1% value.

$$R_{FB3} = \frac{V_{REF}(R_{FB1} + R_{FB2})}{(V_{out} - V_{REF})} \qquad (10)$$

$$R_{FB3} = \frac{7.0V(998K)}{(385\text{V} - 7.0\text{V})} = 18.48K\Omega$$

(use standard value **R_{FB3} =** 18.5kΩ)

Calculate new V_O value based on actual resistor values

$$V_{OUT} = \frac{(R_{FB1} + R_{FB2} + R_{FB3}) \cdot V_{REF}}{R_{FB3}} \quad (11)$$

$$V_{OUT} = \frac{(998K + 18.5K) \cdot 7.0V}{18.5K} = 384.6V$$

Calculate power dissipation of divider resistors

$$P_{R_{FB1}} = P_{R_{FB2}} = \frac{(V_{out} - V_{REF})^2}{2(R_{FB1} + R_{FB2})} \quad (12)$$

$$P_{R_{FB1}} = P_{R_{FB2}} = \frac{(385V - 7V)^2}{2 \times 998k\Omega} = 70mW$$

Output OVP Divider Design

Use caution in OVP set point with regard to setting threshold too high. Output capacitors are typically rated at 450V and caution should be exercised so as not to allow V_O to exceed their maximum voltage rating. Output capacitor surge voltage ratings are intended as a guard band in terms of abnormal operating conditions and shouldn't be use as target spec for OVP.

An over voltage threshold of 425V is an adequate design target.

The same issues, with regard to power dissipation and total impedance of the divider string in the output voltage feedback divider, apply to the OVP divider. Power dissipation of the individual resistors is calculated using the same method as was used in the output voltage feedback divider, as are the resistor values.

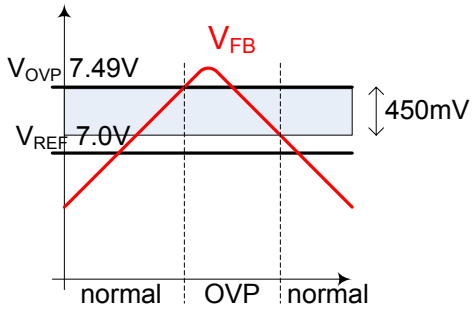
The IR1150S over voltage comparator has a dedicated internal reference voltage, the value of which is a fixed percentage of the output error amplifier reference.

$$V_{(REF)OVP} = 1.07 \cdot V_{REF} = 7.49V \quad (13)$$

If the same divider string is used as for the voltage feedback, the resulting OVP voltage threshold will be set at 7% higher than the nominal output voltage.

$$V_{OVP} = 1.07 \cdot V_{Out} = 412V$$

When the OVP threshold is triggered, the IC will disable the gate drive signal. The comparator has a built in hysteresys of 450mV typ. (see data sheet 'protection section').



Having OVP function on a separate pin allows programming the threshold to the desired value:

$$V_{OVP} = \frac{(R_{OVP1} + R_{OVP2} + R_{OVP3}) \cdot V_{(REF)OVP}}{R_{OVP3}} \quad (14)$$

To design OVP the divider for an over voltage level of 425V as per target specifications of the converter:

R_{OVP1} = R_{OVP2} = 499kΩ, 1%

$$R_{OVP3} = \frac{V_{REF(OVP)}(R_{OVP1} + R_{OVP2})}{V_{OVP} - V_{(REF)OVP}} \quad (15)$$

$$R_{OVP3} = \frac{7.49V(998K)}{(425V - 7.49V)} = 17.9K\Omega$$

Verify the new V_{OVP} value based on actual resistor value

$$V_{OVP} = \frac{(998K + 17.9K)7.49V}{17.9K} = 425V$$

Power dissipation of R_{OVP1} and R_{OVP2} will be the same as R_{FB1} and R_{FB2} given that they are the same values.

Switching Frequency Selection

Switching frequency is user programmable with the IR1150 and is accomplished by selecting the

value for R_f. As such, selection of switching frequency is at the discretion of the user with consideration to overall converter design, with particular consideration of EMI and efficiency requirements.

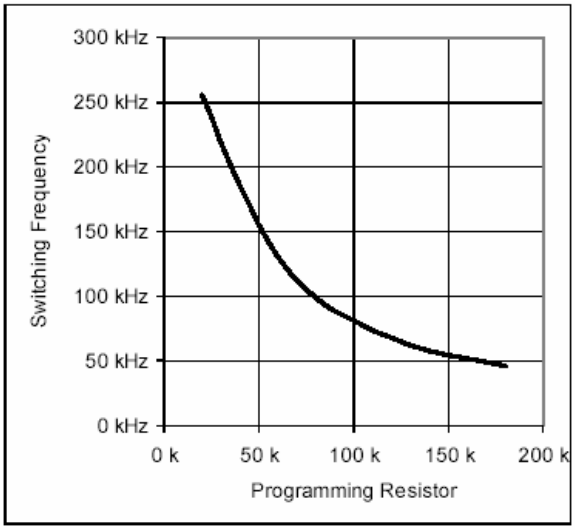


Figure 7 - Oscillator Frequency vs. Programming Resistor Rf

A chart plotting R_f value vs. frequency is provided to determine the appropriate resistor value for the desired switching frequency.

Typical design tradeoffs relative to switching frequency must be carefully considered when selecting an optimum switching frequency for a particular converter design. Some key considerations would be;

Optimized inductor size, power dissipation, and cost EMI requirements, (EN55011, lower limit of 150kHz)

Switching loss in the power switch increase with switching frequency

For the design example of this application note, we will select the switching frequency to be 100kHz, a good tradeoff between EMI performance, optimized inductor, and power switch losses.

Current Loop and Overcurrent Protection

The current sense pin I_{SNS} is the input to the current sense amplifier and the overcurrent protection comparator.

There are essentially two levels of current limitation provided by the IR1150. There is a “soft” current limit, which is essentially a duty cycle limiting fold back type: the converter duty cycle is limited to the point where output power is limited and the output voltage begins to decrease.

There is also a “peak” current limit feature which immediately terminates the present drive pulse once the peak limit threshold, ≈ -1.0V, is exceeded.

The current sense resistor is selected based at minimum input voltage and maximum output power in order to guarantee normal operation under this condition.

The current amplifier has a DC gain G_{DC}=2.5, is internally compensated and bandwidth limited above 280kHz. The operation of the OCC control IC is based on peak current mode, therefore the switch current can be used in alternative to the inductor current as an input to the I_{SNS} pin.

The range for the current sense voltage V_{SNS} is between 0V and -1V, and care must be taken when using a current transformer, to meet this range.

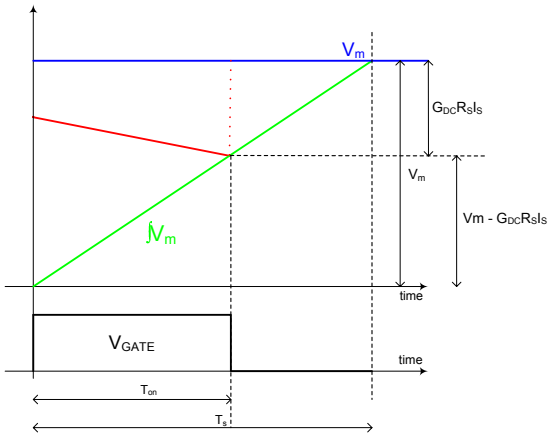


Figure 8 - Ramp relation with duty cycle

The current sense resistor determines the point of soft over-current, that is the point at which input current will be limited and the output voltage will drop.

The worst case is at low line when the current is the highest and also the boost factor of the converter is higher. The current sense resistor R_S must be designed so that at the lowest input line and largest load, the converter will be able to maintain the output voltage.

The required duty cycle at the peak of the sinusoid for desired output voltage at minimum input voltage is given by:

$$D = \frac{V_{out} - V_{IN(PK)MIN}}{V_{out}} \quad (16)$$

$$D = \frac{385V - 120V}{385V} = 0.69$$

When the input voltage is lowered (or the load increased) the voltage loop responds by increasing the modulation voltage V_m.

But when V_m saturates to its maximum, an additional increase in current will limit the duty cycle, therefore causing the output voltage to drop.

It can be seen from Figure 8 that duty cycle is determined at each cycle as the ratio:

$$\frac{v_m - G_{DC} \cdot V_{SNS}}{v_m} = \frac{T_{on}}{T_S} = D \quad (17)$$

$$V_{SNS(max)} = \frac{v_{m(SAT)}(1-D)}{G_{DC}} \quad (18)$$

The required voltage across the current sense resistor to set the “soft” current limit at minimum input voltage is:

$$V_{SNS(max)} = \frac{V_{COMP(EFF)} \cdot (1-D)}{G_{DC}} \quad (19)$$

$$V_{SNS(max)} = \frac{6.05V \cdot (1-0.69)}{2.5} = 0.75V$$

The v_m saturation voltage $V_{COMP(EFF)}$ and the current amplifier DC gain are taken directly from the data sheet (page 4).

Now the value of the sense resistor can be calculated from the max peak inductor current derated with an overload factor (K_{OVL}=10%)

$$I_{IN(PK)OVL} = [\, I_{IN(PK)max} + \frac{\Delta I_L}{2}] K_{OVL} \quad (20)$$

$$I_{IN(PK)OVL} = [\, 5.4A + \frac{1.1}{2}](1.1) = 6.55A$$

From this maximum current level and the required voltage on the current sense pin, we now calculate the resistor value.

$$R_S = \frac{V_{SNS(max)}}{I_{IN(PK)OVL}} = \frac{0.75V}{6.55A} = 0.115\Omega$$

A standard value of 100mΩ can be used: power dissipation in the resistor is now calculated based on worst case rms input current at minimum input voltage:

$$P_{R_S} = I_{IN(RMS)MAX}{}^2 \cdot R_S \quad (21)$$

$$P_{R_S} = 3.8^2 (0.100\Omega) = 1.45W$$

Proper derating guidelines dictate a selected value of R_S = 0.10Ω, 3W (non inductive resistor).

Although the One Cycle Control already provides a cycle by cycle peak current limiting, an additional fast over-current comparator is present for increased protection. If the threshold is reached the current pulse will be terminated.

The system will enter into “peak” current limit should the peak input current exceed;

$$I_{PK_LMT} = \frac{|-1.0V|}{0.100\Omega} = 10A$$

Current Sense Filtering

The current amplifier is internally compensated with a pole at approximately 280 kHz in order to attenuate the high frequency switching noise often associated with peak current mode control.

Blanking time is also provided in order to avoid spurious triggering of the overcurrent protection due to the boost diode reverse recovery spike.

Additional external filtering is typically employed in systems operating with peak current mode control,

and may be incorporated with a simple RC filter scheme as shown in schematic diagram.

$$f_{PSF} = \frac{1}{2\pi \cdot R_{SF} \cdot C_{SF}} \qquad (22)$$

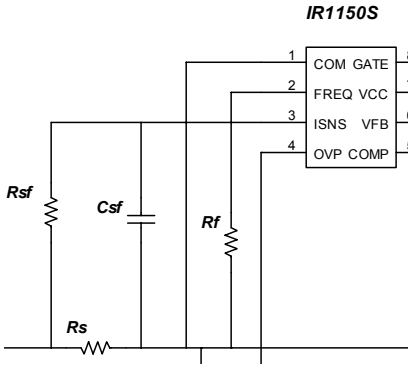


Figure 9 – Current Sense Resistor and Filtering

A corner frequency around 1-1.5MHz is recommended. Typical values for the RC filter are:

R_{SF} = 100Ω (also provides additional current limiting into current sense pin during inrush and transients)

C_{SF} = 1000pF

These component values offer a decent compromise in terms of filtering, (f_P ≈ 1.59MHz), while maintaining the integrity of the current sense signal thus maintaining peak current mode control.

It should be noted that the input impedance of the current amplifier is approximately 2.2KΩ. The 100Ω resistor will form a divider with this 2.2KΩ resistor thus affecting the actual threshold for the soft current limit. The actual voltage at the current limit amplifier input will in effect be approximately 96% of the voltage across the current sense resistor.

Soft Start Design

Soft start is controlled by the rate of rise of the error amplifier output voltage, which is a function of the compensation capacitors C_z and C_p, and the maximum available output current of the error amplifier.

Soft start time is determined by the following equation:

$$t_{SS} = \frac{C_Z \cdot V_{COMP(EFF)}}{i_{EA-OUT(MAX)}} \qquad (23)$$

Since C_p is generally much smaller than C_Z, its effect can be neglected.

$$C_Z = \frac{t_{SS} \cdot i_{OVEA}}{V_{COMP(EFF)}} \qquad (24)$$

i_{OVEA} and $V_{COMP(EFF)}$ are taken from the datasheet.

$$C_Z = \frac{50ms \times 40\mu A}{6.05V} = 0.33\mu F$$

$$t_{ss} = \frac{0.33\mu F \cdot 6.05V}{40\mu A} = 50ms$$

This represents the time needed by the controller to reach full duty cycle capability in the startup phase. The peak current will be limited during this period of time.

VOLTAGE FEEDBACK LOOP

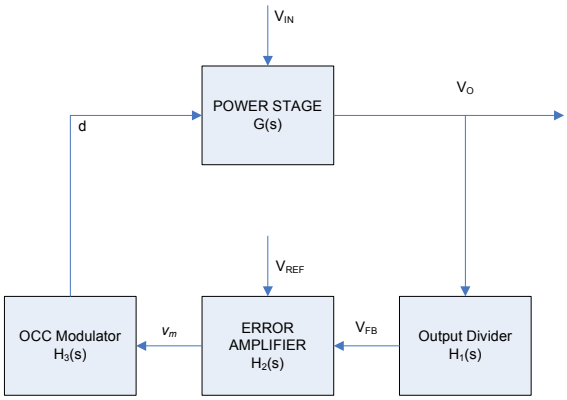


Figure 10 - Voltage Loop

The open loop gain is given by the product:

$$T(s) = G(s) \cdot H_1(s) \cdot H_2(s) \cdot H_3(s) \quad (25)$$

OUTPUT DIVIDER: $H_1(s)$

The output divider scales the output voltage to be compared with the reference voltage in the error amplifier.

Therefore:

$$V_{OUT} = \frac{(R_{FB1} + R_{FB2} + R_{FB3})V_{REF}}{R_{FB3}} \quad (26)$$

$$H_1(s) = \frac{V_{REF}}{V_o} \quad (27)$$

This stage simply attenuates the output voltage signal, by a fixed amount:

$$H_1 = 0.018 = -34.8dB$$

POWER STAGE: $H_3(s) \cdot G(s)$

The low frequency small signal equivalent circuit for the boost power stage is shown in Figure 11. An explanation of this model can be found in [7][8].

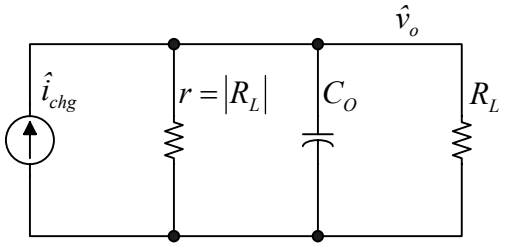


Figure 11 - Small Signal low frequency model for the boost power stage

Definitions:

R_L : Load Resistance

C_O : Output (bulk) capacitor

$\hat{v}_m$: Modulation Voltage – this is the output of the Voltage Error Amplifier

G_{DC} : DC gain of the current amplifier – it is set internally the IC at 2.5V/V

V_{in} : Peak value of input voltage (i.e. $V_{inRMS\,max} \cdot \sqrt{2}$)

For a constant power load the actual RL is negative. This is the typical case when the PFC load is a DC-DC stage: if the input voltage of that stage is reduced it will react by increasing the current, in order to maintain the output power constant.

In this case R_L will cancel with r and will yield:

$$\frac{\hat{v}_o}{\hat{i}_{chg}} = \frac{1}{sC_o} \quad (28)$$

When a purely resistive load is present we have:

$$\frac{\hat{v}_o}{\hat{i}_{chg}} = \frac{R_L/2}{1 + sC_o\frac{R_L}{2}} \quad (29)$$

We will not consider the resistive load case here, since in the majority of cases the PFC load is the input of another DC-DC converter.

In order to derive $\frac{\hat{i}_{chg}}{\hat{v}_m}$ we need to look at the OCC PWM modulator. The control law is:

$$G_{DC} \cdot R_S \cdot \hat{i}_g = \frac{\hat{v}_m}{M(d)} \tag{30}$$

Where $M(d) = \frac{\hat{v}_o}{\hat{v}_g}$

$$\hat{v}_g = V_{in} + \hat{v}_{in} \tag{31}$$

Substituting and eliminating the small signal cross terms:

$$\frac{\hat{i}_g}{\hat{v}_m} = \frac{V_{in}}{V_o R_S G_{DC}} \tag{32}$$

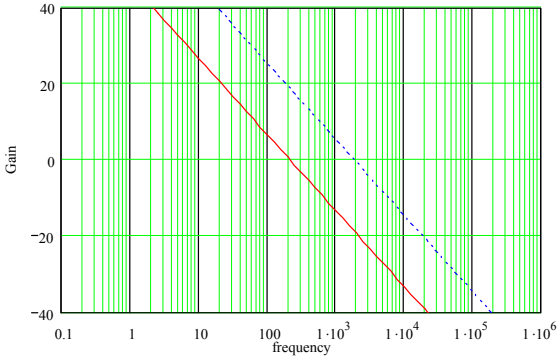


Figure 12 - Power Stage Gain @ 90V (red) and 265V (blue)

The output average current can be calculated from the input current:

$$\hat{i}_g = \frac{\hat{p}_{in}}{V_{in}} = \frac{\hat{i}_{chg} \cdot V_o}{V_{in}} \tag{33}$$

$$\frac{\hat{i}_{chg}}{\hat{v}_m} = \frac{V_{in}^2}{V_o^2 R_S G_{DC}} \tag{34}$$

The control to output for the constant power load case is:

$$\frac{\hat{v}_o}{\hat{v}_m} = \frac{V_{in}^2}{V_o^2 \cdot R_S \cdot G_{DC}} \cdot \frac{1}{sC_o} \tag{35}$$

The power stage gain varies as expected with the input voltage.

ERROR AMPLIFIER: $H_2(s)$

The output voltage error amplifier in the IR1150 control IC is a transconductance type amplifier.

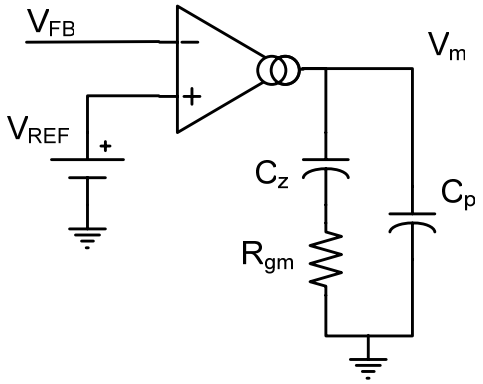


Figure 13 - Error Amplifier

The transfer function is:

$$H_2(s) = \frac{g_m \cdot (1 + sR_{gm}C_Z)}{s(C_Z + C_P + sR_{gm}C_Z C_P)} \tag{36}$$

The compensation network shown on the schematic diagram adds a zero and a pole in the transfer function at:

$$f_{Z0} = \frac{1}{2\pi \cdot R_{gm} \cdot C_Z} \tag{37}$$

$$f_{P0} = \frac{1}{2\pi \cdot R_{gm} \frac{Cz \cdot Cp}{Cz + Cp}} \tag{38}$$

Voltage Loop Compensation

Typical of PFC converters is the requirement to keep the voltage loop bandwidth less than ½ the line frequency in order to avoid distortion of the line current resulting from the voltage loop attempting to regulate out the 120Hz ripple on the output.

There is of course, the associated tradeoff between system transient response and input current distortion, where stability of the voltage loop is generally easily achieved.

The goals of the voltage loop compensation are the limitation of the open loop gain bandwidth to less than ½ the AC line frequency and the amount of second harmonic ripple injected in the COMP pin from the error amplifier.

First we need to calculate the amount of second harmonic ripple on the output capacitor:

$$V_{OPK} = \frac{P_{in}}{2\pi \cdot f_{2nd} \cdot C_O \cdot V_{out}} \qquad (39)$$

$$V_{OPK} = \frac{330W}{2\pi \cdot 120 \cdot 330\mu F \cdot 385V} = 3.4V$$

The amount of 120Hz ripple needs to be small compared with the value of the error amplifier output voltage swing.

A percentage around 1% is typical and will minimize distortion:

$$G_{VA} = \frac{V_{COMP(EFF)} \cdot 0.01}{2 \cdot V_{OPK}} \qquad (40)$$

$$G_{VA} = \frac{6.05V \cdot 0.01}{2 \cdot 3.4V} = 0.089 = -41dB$$

As calculated from (26) the attenuation of the output divider is already:

$$H_1 = 0.018 = -34.8dB$$

The gain of the error amplifier @ 120Hz needs to be:

$$G_{VA} - H_1 = -6.2dB$$

The second pole is usually placed at a much higher frequency than 120Hz, so the error amplifier transfer function can be approximated to:

$$H_2(s) \cong \frac{g_m \cdot (1 + sR_{gm}C_Z)}{sC_Z} \qquad (41)$$

Since C_Z has already been determined for the soft start, only R_{gm} needs to be calculated by forcing:

$$\left|H_2(j2\pi \cdot f_{2nd})\right| = -6.2dB \qquad (42)$$

$$R_{gm} = \sqrt{\left(\frac{G_{VA} - H_1}{g_m}\right)^2 - \left(\frac{1}{2\pi \cdot f_{2nd} \cdot C_Z}\right)^2} \qquad (43)$$

Substituting:

$$R_{gm} = 8.9k\Omega$$

The second pole frequency should be chosen higher than the cross over frequency and significantly lower than the switching frequency in order to attenuate noise: typical value is 1/6 to 1/10 of the switching frequency:

$$f_{P0} = \frac{1}{2\pi \cdot R_{gm} \frac{Cz \cdot Cp}{Cz + Cp}} \cong \frac{1}{2\pi \cdot R_{gm} \cdot Cp} \qquad (44)$$

$$C_p = \frac{1}{2\pi \cdot 8.9k\Omega \cdot 17kHz} = 1nF$$

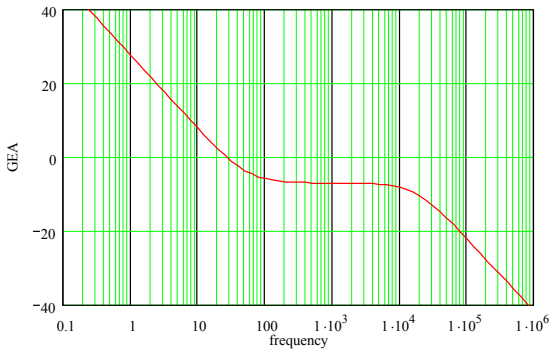


Figure 14 - Error Amplifier Gain

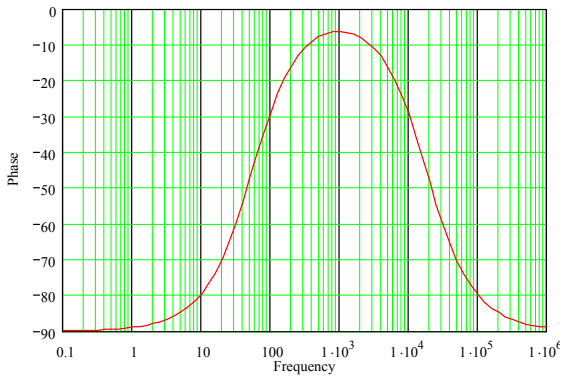


Figure 15 - Error Amplifier Phase

Finally the loop gain can be drawn:

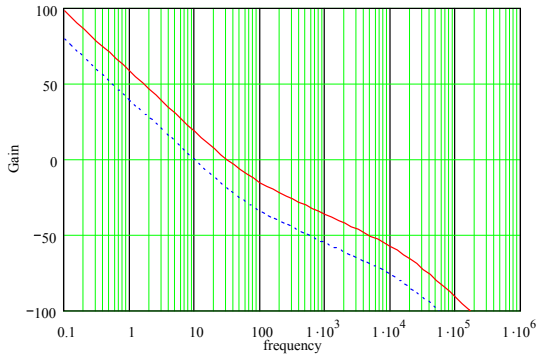


Figure 16 - Loop Gain @ 90V (blue), 265V (red)

Crossover frequency is between 10Hz and 30Hz, depending on the input AC line value, as required.

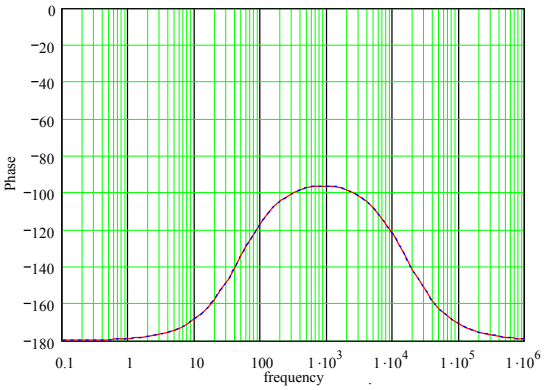


Figure 17 - Loop Phase

Design Tips

IC Decoupling Capacitor

The PFC converter is a harsh environment for the controller in terms of noise and as such, certain precautions must be considered with regard to proper noise decoupling.

The key element to proper bypassing of the IC is the physical location of the bypass capacitor and its connections to the power terminals of the control IC.

In order for the capacitor to provide adequate filtering, it must be located as close as physically possible to the V_{CC} and COM pins and connected thru the shortest available path.

Note the location (Figure 18) of the bypass capacitor directly above the SO8 IC which will provide for the shortest possible traces from the capacitor to the V_{CC} and COM pins. This is crucial in providing the tightest decoupling path possible and minimizing any possible noise pickup due to excessive trace lengths.

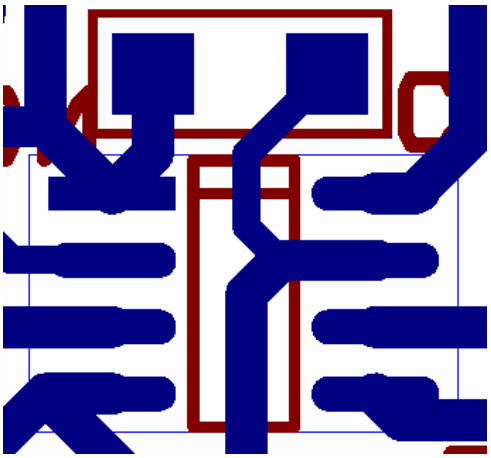


Figure 18 - Proper connection of decoupling capacitor

The value of the decoupling capacitor will depend on several factors, including but not limited to switching frequency, power MOS gate drive capacitance and external gate resistance.

As a general rule a 470nF ceramic capacitor is recommended. This assumes a larger electrolytic capacitor is still present to provide low frequency filtering.

Inductor Design

There is more to consider than merely inductor value when it comes to designing the boost choke.

The mechanical design of the choke can have a significant impact on system level noise due to associated parasitic elements.

The parasitic inter-winding capacitance associated with the boost inductor can resonate and generate high frequency ringing.

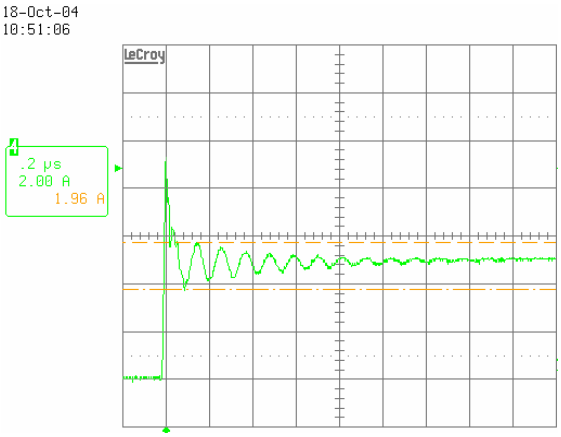


Figure 19 - Ringing on turn on

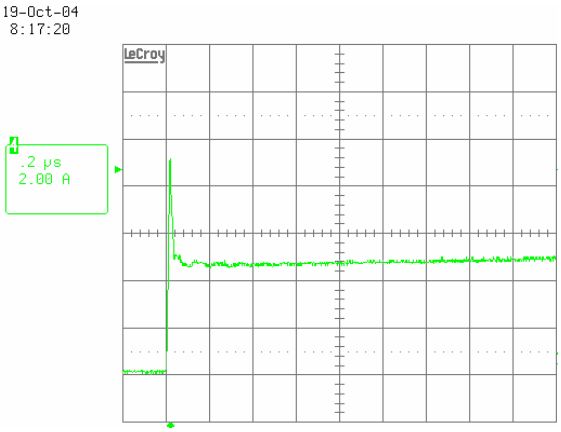


Figure 20 - Single layer choke

Figure 19 shows the power MOSFET turn on current when a multi layer, non optimized boost choke is used. The presence of a high frequency ringing (around 8-10MHz) can be noted. In Figure 20 a single

layer inductor with the same value, but lower inter-winding capacitance is used.

If not controlled this ringing can produce unacceptable voltages to the sensitive pins of the control IC, which can disrupt proper circuit operation.

Although an internal blanking circuit is present to limit the effects of the diode reverse recovery peak on the current loop, it is recommended to add an RC cell on the current sense resistor to increase noise immunity of the control IC.

Another extremely good reason to control the ringing is to limit the Electro Magnetic Interferences (EMI), especially in the radiate range

Gate Drive Considerations

The gate driver of the IR1150S is capable of extremely rapid rise and fall times in addition to the 1.5A peak source and sink current capability. These rapid rise and fall capabilities, while providing for an extremely desirable MosFet drive capacity, can also create noise issues if not properly controlled.

Often times it is difficult to meet EMI requirements when drive speeds are too fast resulting in fast rising dI/dt and dV/dt edges.

This not only taxes the EMI filter, but can introduce additional noise that the controller is forced to deal with. The waveforms of Figure 21 and Figure 22 below illustrate the gate drive voltage of the IR1150S vs. the power MosFet drain current for an IRFP27N60K power switch.

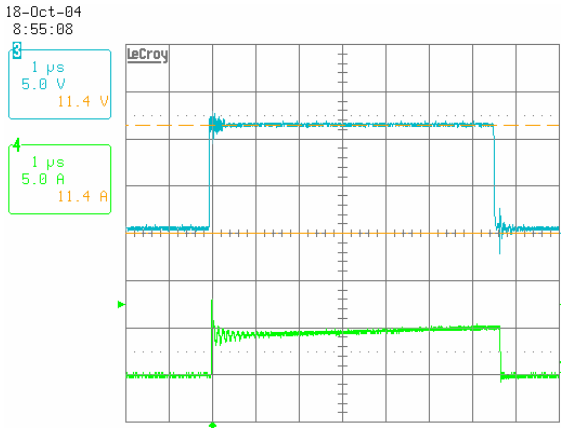


Figure 21 - IR1150S Gate Drive voltage

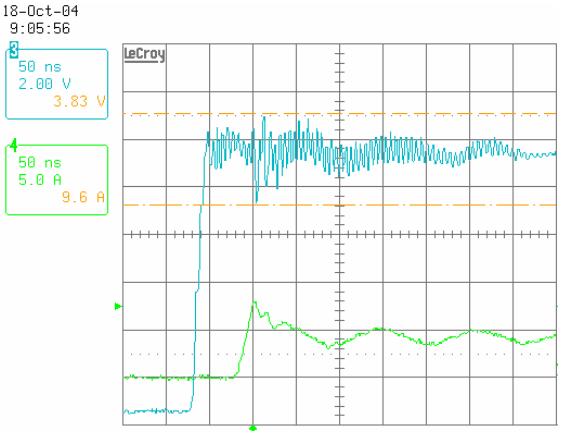


Figure 22 - IR1150S Gate Drive voltage

The rise time must be carefully controlled by virtue of proper selection of gate drive resistors for a specific application. Parasitic elements, both capacitive and inductive, printed circuit board layout, thermal design, system efficiency, and power switch selection are but some of the criteria which is to be considered when selecting the proper drive impedance for a given design. Improper attention to proper gate drive design will most certainly result in performance and noise issues.

PCB Layout

Proper routing of critical circuit paths is elemental in optimum circuit performance and minimal system noise. Parasitic inductance resulting from long trace length in the power path can introduce noise spikes which can deteriorate performance to unacceptable levels. In addition to creating unwanted system noise, these spikes can decrease reliability of power devices and if severe enough, can be destructive to the point of catastrophic failure of the devices. At the very least, uncontrolled parasitic elements as a consequence of inadequate attention to printed circuit board layout will force the designer to control the additional noise and voltage spikes with additional circuitry, adding cost and decreasing efficiency. It is therefore desirable to pay particular attention to optimizing the PCB layout in terms trace routing, placement, and length, in the critical circuit paths. Proper grounding and utilization of ground planes are helpful within the control section while minimized trace lengths are de-

sirable in the high voltage and current switching paths of the power section.

Additional Noise Suppression Considerations

The PFC boost diode reverse recovery characteristic is an enormous contributor to system noise both conducted and radiated. This will tax the EMI filter in addition to basic circuit functionality and reliability.

There are other considerations besides noise, efficiency for example. The power switch must absorb all the reverse recovery current during its turn on period and therefore must also dissipate the resultant additional power. Consequently, there is additional burden on system level overall efficiency as well as the increased noise levels. SiC diodes provide an excellent solution to address these issues as reverse recovery time is virtually zero, thus there are essentially no reverse recovery currents to be dealt with. While the SiC appears to be the salvation of the PFC boost converter, there are considerations such as surge current capabilities that must be addressed before the SiC diode becomes the mainstay of PFC converter design.

In the meantime, a simple RC snubber across the boost diode goes a long way in reducing the noise due to reverse recovery. When properly designed, the snubber will be less dissipative then allowing the full reverse recovery current absorbed by the power switch.

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