International
IOR Rectifier

Application Note AN-1073

Analysis of Different Solutions and Trade-off Cost vs. Power Factor Performance for Electronic Ballasts

By Cecilia Contenti

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The IR2520D is a very versatile and flexible building block to design the typical functions of electronic ballast in a cheap and easy way. In this paper three different circuits have been discussed: low PF ballast is low end low cost, low cost PFC ballast is medium end medium cost and active PFC ballast is high-end higher cost. The right solution can be chosen based on a trade-off between performance needs (PF, Crest Factor and THD requirements) and cost requirements.

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I. INTRODUCTION

Electronic lamp ballasts using an active boost type power factor front end, a Ballast Controller IC and 3 MOSFETs have superior reliability versus different solutions, but different solution can be lower cost, smaller, and use fewer components. This application note will show how to implement an electronic ballast with high power factor maintaining low cost and small size and will honestly point out the short coming of every implementation proposed versus the classical active power factor correction solution. Maintaining low cost and small size is now possible with the launch of International Rectifier's IR2520D high-voltage IC. This new HVIC breaks ground in reducing the components count and the circuit complexity thus allowing designers to develop ballasts capable of meeting the latest European requirements, while maintaining low cost and small size. The new HVIC we will introduce is called IR2520D. The IR2520D is intended for fluorescent lamps and integrates all of the necessary functions for preheat, ignition and on-state operation of the lamp, plus, lamp fault protection and low AC-line protection, together with a complete high- and low-side 600V half-bridge driver as well as an integrated bootstrap diode. One of the biggest advantages of the IR2520D is that it eliminates the need for a high-precision current sensing resistor that is typically used to detect over current. The IC uses the VS pin and the RDSon of the low-side half-bridge MOSFET for over-current protection and to detect non-zero-voltage-switching conditions. The IR2520D has only 8 pins. Please refer to the IR2520D datasheet for further information on the IR2520D.

The application note will analyze several applications and circuit build around this HVIC, such small size ballast without power factor correction, electronic ballast using active power factor correction and electronic ballast using a low cost power factor methods: passive power factor correction and bus voltage compensation.

II. LOW POWER FACTOR CONFIGURATION

This solution is suggested for low cost and small size applications such as integrated CFL and small size ballasts. Limiting the maximum power to 25W the design does not need to conform to THD and PF requirements and this allows saving of the PFC stage reducing the component count and maintaining a very small size. With this configuration the Power Factor (PF) is around 0.5 and the Total Harmonic Distortion (THD) is >100%.

An electronic ballast for driving 26W compact fluorescent lamps from 220VAC has been designed and tested for performance. The circuit is shown in figure 1.

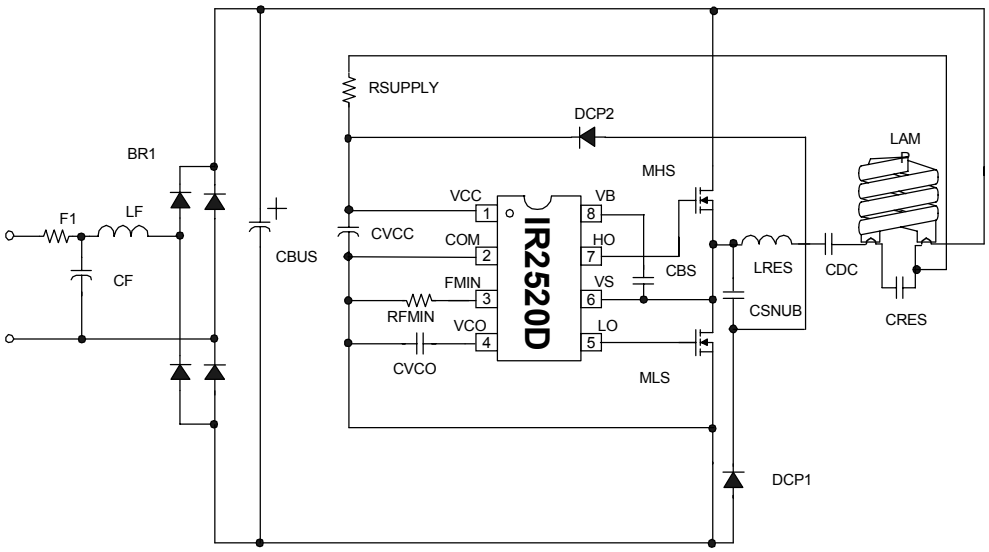


Fig. 1: Low PF Ballast using the IR2520D HVIC.

The circuit provides all of the necessary functions for preheat, ignition and on-state operation of the lamp and also includes the EMI filter and the rectification stage. The circuit is built around the IR2520D Ballast Control IC. The functionality of the IR2520D allows the component count for the complete ballast to be reduced down to 19 components.

Features of the ballast include programmable run frequency, programmable preheat time, open filaments and no-lamp protection, failure to strike and deactivated-lamp protection, low AC line protection, auto-restart after lamp replacement. The limits of these configuration are low PF, about 0.6 and high THD > 100%.

Figure 2 shows the voltage across the lamp and the current in the resonant inductor at Startup and figure 3 shows the lamp voltage and the lamp current during running conditions. The Bill Of Materials (BOM) is shown in Table 1.

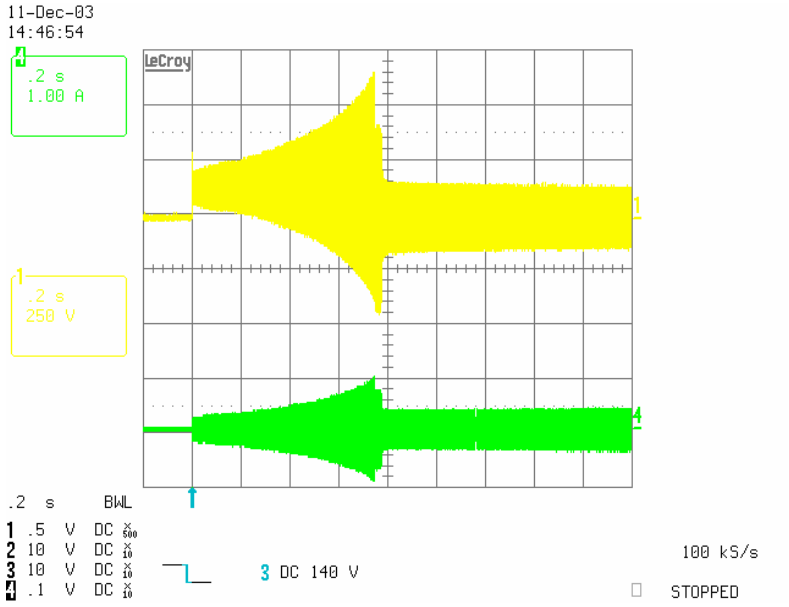


Fig. 2: Voltage across the lamp (yellow) and current in the resonant inductor (green) at Startup

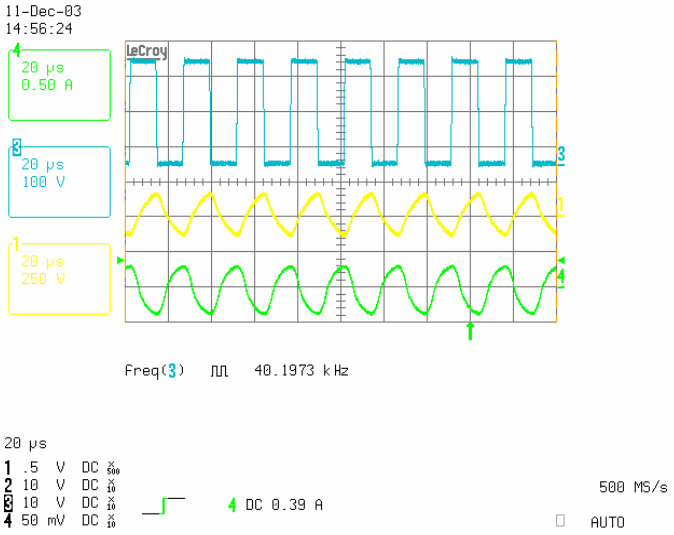


Fig. 3: VS (HB) Voltage (blue), Lamp Voltage (yellow) and the Lamp Current (green) during Run Mode.

Description	Reference
Bridge Rectifier, 1A 1000V	BR1
Resistor, 0.5Ohm, 1/2W	F1
Capacitor, 0.1uF 275 VAC	CF
EMI Inductor, 1mH 370mA	LF
Capacitor, 47nF 400V	CDC
Capacitor, 10uF 350VDC 105C	CBUS
Capacitor, 0.1uF 50V 1206	CBS
Capacitor, 0.47uF 25V 1206	CVCO
Capacitor, 1uF 25V 1206	CVCC
Capacitor, 680pF 1KV SMT 1812	CSNUB
Capacitor, 4.7nF 1KV Polypropylene	CRES
IC, Ballast Driver IR2520D	IC BALLAST
Inductor, 2.25mH, 5%, 1Apk	LRES
Transistor, MOSFET IRFU430	MHS, MLS
Resistor, 1M, 1206, 100V	RSUPPLY1, RSUPPLY2
Resistor, 68.1K, 1%, 1206	RFMIN
Diode, 1N4148 SMT DL35	DCP1, DCP2

TABLE 1) BOM Low PF Ballast, Lamp type: Spiral CFL 26W, Line Input Voltage: 190-240 VAC.

III. HIGH POWER FACTOR CONFIGURATION

This solution is suggested for medium-/ high-end applications. Most applications need a regulated DC bus voltage, a high PF and low THD to conform to EN61000-3-2. The classical solution uses an additional PFC inductor, an additional FET and an additional PFC IC. This solution is the most complete and allows a regulated bus voltage for a wide input range. With this configuration one can easily achieve PF > 0.9 and THD < 10%.

The circuit includes an external active power factor correction front-end and is shown in the figure 4.

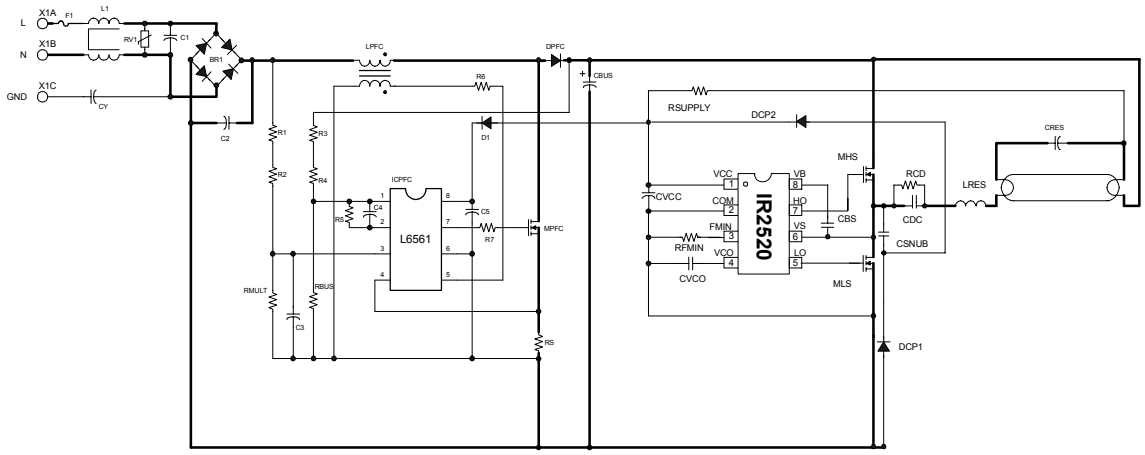


Fig. 4: High PF Ballast using an external active PFC IC.

The circuit consists of an EMI filter, an active power factor correction front-end, a ballast control section and a resonant lamp output stage. The active power factor correction section is a boost converter operating in critical conduction, free-running frequency mode. The power factor front end provides regulated bus voltage, generally 400VDC. The ballast control section provides frequency modulation control of the traditional RCL lamp resonant output circuit and is easily adaptable to a wide variety of lamp types. This solution is better than alternative solutions from the performance point of view and can be used up to high power because a regulated and boosted bus voltage allows the current in the half-bridge FETs to be limited and maintains a good crest factor also with high load (this cannot be achieved using the following passive PFC configuration) and comply with EN-61000-3-2 also for high power (this is not verified with the low PF configuration).

IV. LOW COST POWER FACTOR METHODS

These solutions are suggested for low-end applications. In some applications it is desirable to have a regulated and boosted DC bus voltage and a high power factor, but the classical solution using an additional inductor, an additional FET and an additional IC can be too expensive for the cost range of the product. The goal is a tradeoff between performance and cost. A typical case is low cost CFL (below 25W power). In these applications PFC is often not used because of cost but this causes very high harmonics and does not provide regulation when the AC line varies and the light level varies with the AC line.

V PASSIVE VALLEY FILL CONFIGURATION

A 14W CFL ballast has been designed and tested for performance. The circuit is shown in figure 5.

The circuit is based on a resonant topology driven by a MOSFET half bridge. The circuit is controlled by the IR2520D Ballast Control IC that provides lamp preheat, lamp ignition, running mode and fault protection (lamp fault, open filaments, failure to strike, deactivated lamp and low AC line).

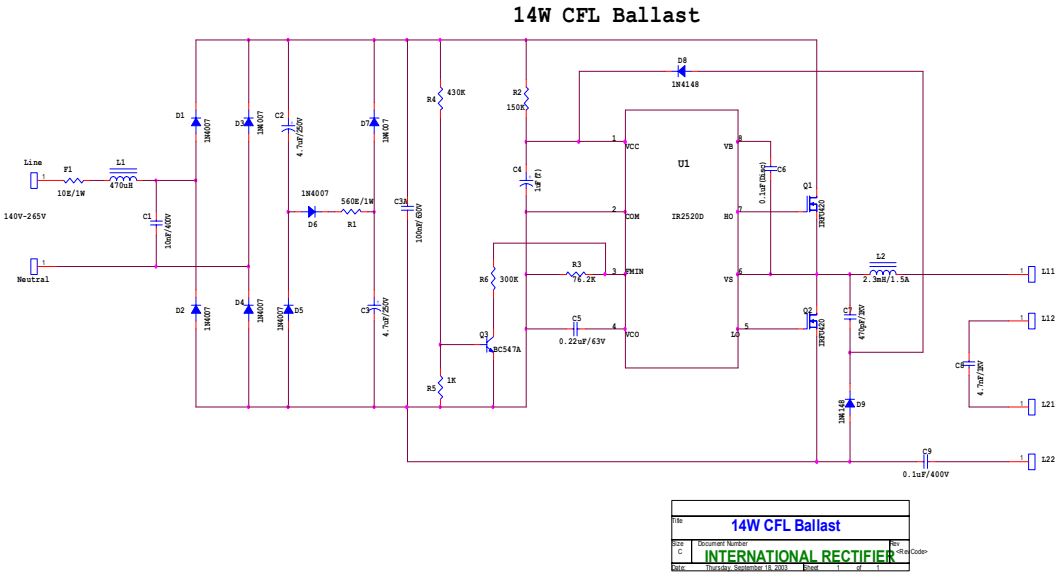


Fig. 5: Passive PF ballast using the IR2520D HVIC

To achieve high PF a Passive Valley Fill configuration has been used on the input stage, a diode and resistor has been added at the standard Passive Valley Fill configuration to reduce THD. High Crest Factor of the lamp current is intrinsic in a Passive Valley Fill Configuration because of the bus shape. The crest factor is very high because the bus voltage change between 2 different values, very different between each other: about VACpk and ½ VACpk. The current associated at the minimum bus voltage will be more than the double of the current associated to the maximum bus voltage and the intrinsic crest factor will be higher than 2. This is valid in the case of constant frequency. Using a resistor to limit the harmonics increases the crest factor even further because the minimum bus voltage decreases.

To limit the crest factor an additional circuit has been used to modulate the frequency of the Half Bridge versus the DC Bus Voltage value. The circuit increases the frequency when the DC bus increases above a threshold, limiting the crest factor of the current. With this configuration one can get THD < 30 %, PF > 0.85, Lamp Current Crest Factor Ipk/Irms (CF) < 1.7 with input: 220-240VAC

Figure 6 shows the bus voltage shape, the lamp current and the lamp voltage. Table 4 shows the BOM

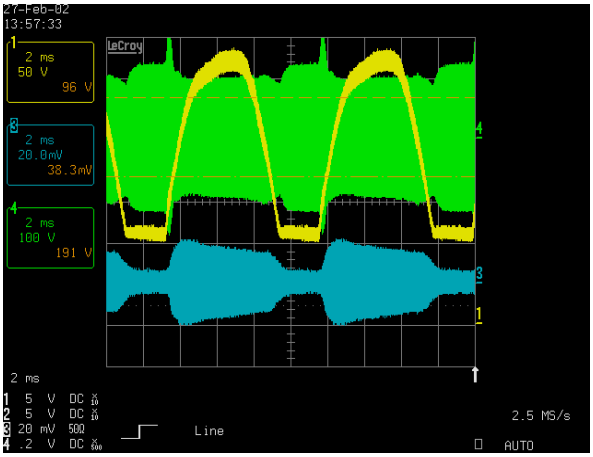


Fig. 6: The bus voltage (in yellow), the lamp current (in blue) and the lamp voltage (in green).

Description	Reference
Bridge Rectifier, 1A 1000V	BR1
Resistor, 0.5Ohm, 1/2W	F1
Capacitor, 0.1uF 275 VAC	CF
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Capacitor, 0.47uF 25V 1206	CVCO
Capacitor, 1uF 25V 1206	CVCC
Capacitor, 680pF 1KV SMT 1812	CSNUB
Capacitor, 4.7nF 1KV Polypropylene	CRES
IC, Ballast Driver IR2520D	IC BALLAST
Inductor, 2.25mH, 5%, 1Apk	LRES
Transistor, MOSFET IRFU430	MHS, MLS
Resistor, 1M, 1206, 100V	RSUPPLY1, RSUPPLY2
Resistor, 68.1K, 1%, 1206	RFMIN
Diode, 1N4148 SMT DL35	DCP1, DCP2

TABLE 2) BOM Passive PF Ballast, Lamp type: Spiral CFL 14W, Line Input Voltage: 200-240 VAC.

Note: Different lamp types require BOM changes.

VI. BOOSTED BUS VOLTAGE REGULATION

This method allows a boosted bus voltage with a high PF and reduced THD, requiring only an additional inductor without the PFC control IC. A circuit using the new IR2520 8 pin ballast control IC has been built and tested for performances. With 26W input power and 110VAC supply we measured PF=0.99, bus voltage = 350V and THD about 12%.

The control circuit proposed is shown in fig.7.

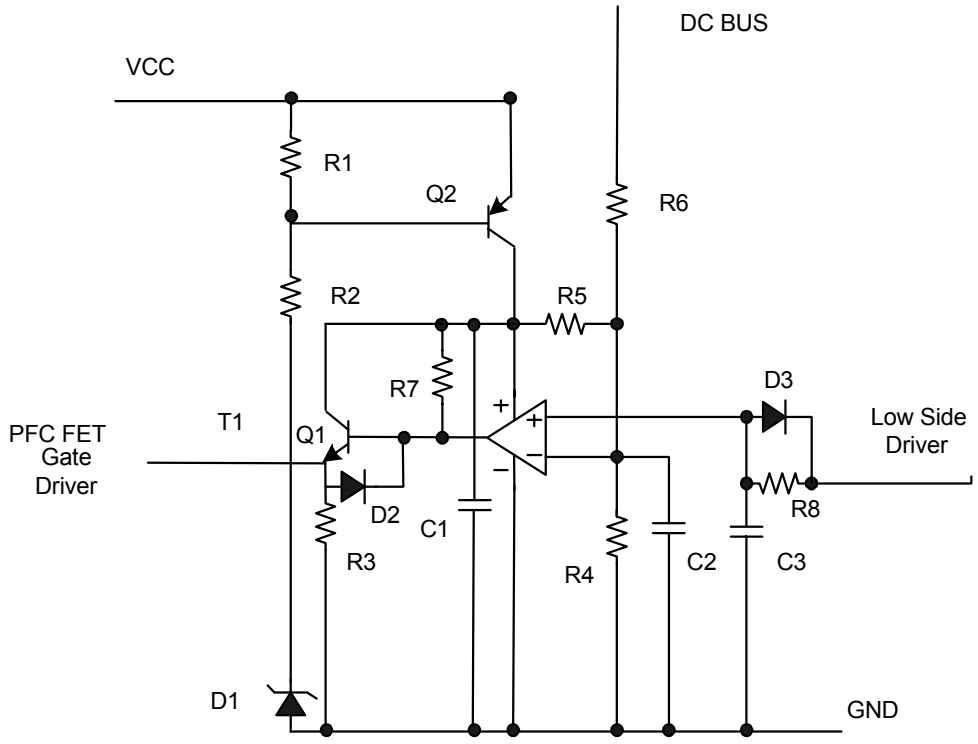


Fig.7: Boost regulation circuit

The circuit includes:
1) UVLO circuit for the comparator: R1, R2, D1, Q2 and C1. This is to prevent the PFC MOSFET from being switched on at any time before the IR2520D is out of UVLO and running normally. The additional circuit supplies the comparator only when the VCC voltage reaches 14V and the current is enough to switch on the zener diode that consequentially switch on Q2. Without this circuit the comparator could start to draw current before the supply voltage reaches the UVLO threshold of the IR2520.

2) Boost regulation circuit: Comparator, R6, R4, C2, R5, D3, R8, R7 and C3. This circuit adjusts the on time of the PFC MOSFET. As the DC bus increases, the on time is reduced.

3) Driving stage for the PFC mosfet: Q1, D2 and R3. This is needed as the comparator output is open collector in order to produce sufficient gate drive current to switch on the fet with fast transition 0-15V.

The complete circuit tested in the lab is showed in fig. 8.

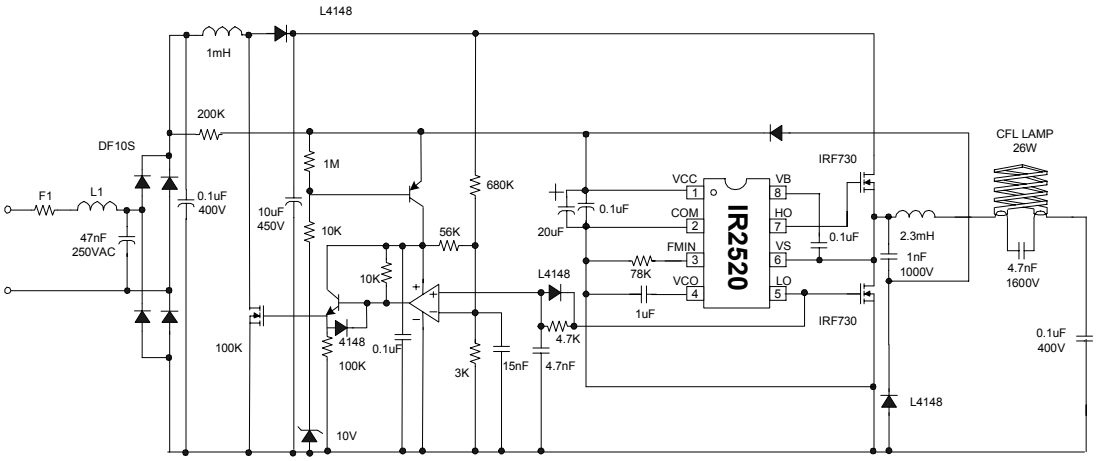


Fig. 8: Complete Boosted Bus Voltage Regulation Circuit

The circuit is similar to a boost type PFC circuit working in critical conduction mode. When the PFC mosfet is turned on, the PFC inductor (1 mH) is connected between the rectified line input (+) and (-) causing the current in the PFC inductor to rise linearly. When the PFC mosfet is turned off, the PFC inductor is connected between the rectified line input (+) and the DC bus capacitor (10 uF) (through the PFC diode) and the stored energy in the PFC inductor causes current to flow into the bus capacitor. As the PFC Mosfet is turned on and off at a high frequency, the voltage on CBUS charges up to a specified voltage. The feedback loop adjusts the bus voltage by continuously monitoring the DC voltage and adjusting the on-time of the PFC mosfet accordingly. In this way the maximum DC bus voltage is limited to a level where the feedback voltage is greater than the maximum

point of the sawtooth waveform, which is approximately 5V. The duty cycle will be greater when the DC bus is low allowing it to increase more rapidly to the desired level.

The load compensation is sufficient to prevent excessive voltage existing on the DC bus during preheat when the load is relatively light. For an increasing DC bus the on-time is decreased, and for a decreasing DC bus the on-time is increased. The duty cycle of the signal driving the PFC mosfet is determined by comparing a fraction of the DC Bus voltage with a reference saw tooth wave generated using the signal in the LO pin used to drive the Low Side fet of the half bridge.

The comparator produces a positive output whenever the voltage in the 0-5V saw tooth- wave generated with the signal in the LO pin exceeds the fraction of the DC bus voltage. In this way the on time of the PFC mosfet can be adjusted between 0 (0% duty cycle), when the DC bus voltage is high, and a maximum (50% duty cycle) when the bus voltage is low.

Figure 9 shows the saw tooth- wave generated with the signal in the LO pin, the bus voltage reference and the PFC mosfet gate driver voltage.

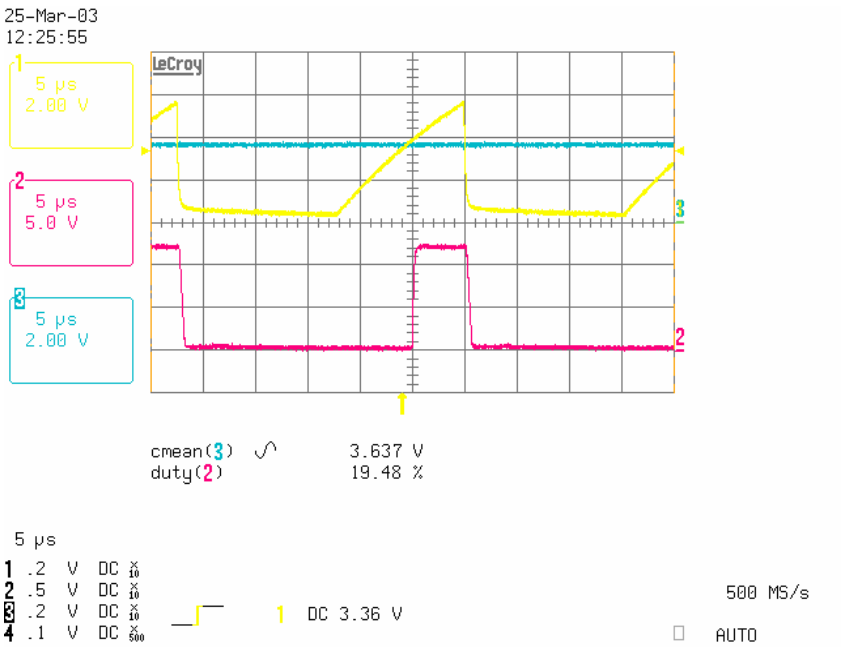


Fig. 9: Saw tooth- wave generated with the signal in the LO pin (yellow), bus voltage reference (blue) and PFC mosfet gate driver signal (red).

The DC bus regulation resulting from this technique is 350Vdc with an input range of 90-130 VAC. The bus value or the AC range can be regulated changing the value of the fraction of DC bus used as negative threshold. To set 320V with 90-130VAC we used R4= 3.9K resistor, to get the same bus voltage with 220V input you need R4=6.8K resistor.

Fig. 10 show the waveform in the PFC mosfet gate driver for different values of the voltage in the – pin of the comparator (bus voltage derivate).

In case of over voltage the duty cycle is zero and the PFC MOSFET is always off.

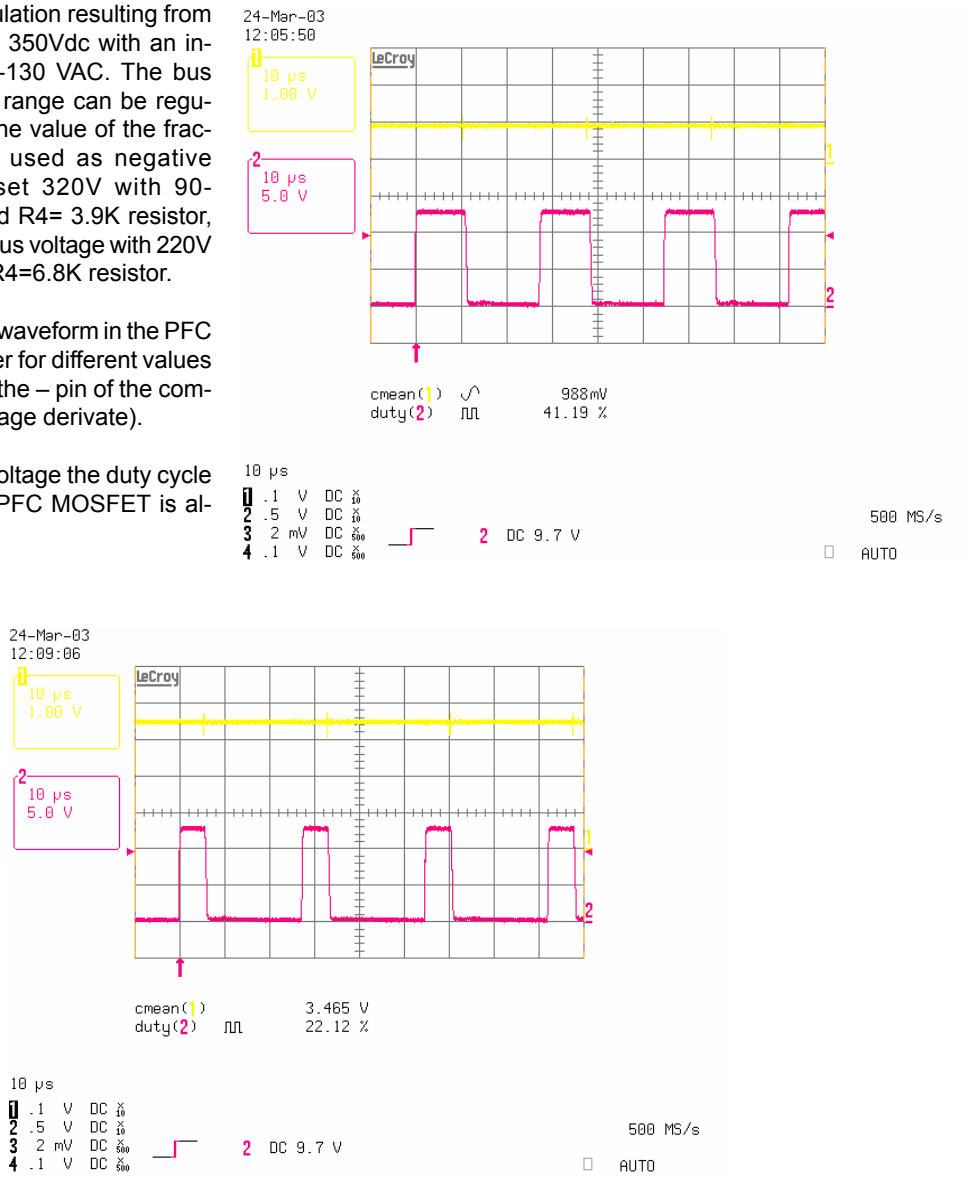


Fig. 10: waveform in the PFC mosfet gate driver for different values of the bus voltage derivate.

Figure 11 shows HB voltage, lamp voltage and DC bus voltage.

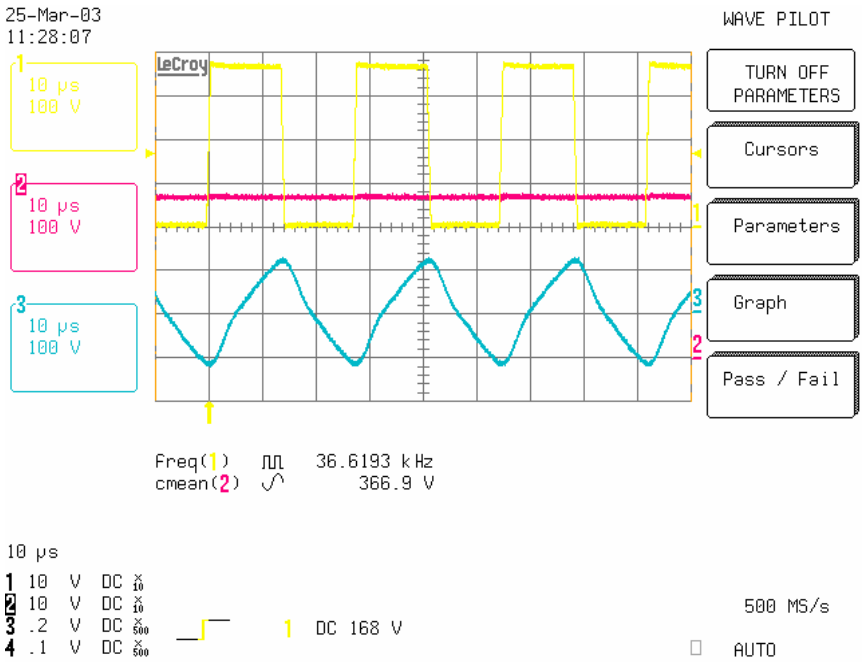


Fig.11: HB Voltage (yellow), DC bus voltage (red) and lamp voltage (blue).

This system allows some degree of line and load compensation but does not produce true regulation of the DC bus. Consequently this approach is suitable for a limited range of supply voltage only and works very well for a typical 120VAC line US application. Main advantages: reduced cost and components count. Disadvantage: the range of VAC in which we obtain low THD and good PFC is narrow (about 40 VAC), the method realizes a bus compensation, not a bus regulation and no protections against continuous mode.

VII. CONCLUSIONS

The IR2520D is a very versatile and flexible building block to design the typical functions of electronic ballast in a cheap and easy way. In this paper three different circuits have been discussed: low PF ballast is low end low cost, low cost PFC ballast is medium end medium cost and active PFC ballast is high-end higher cost. The right solution can be chosen based on a trade-off between performance needs (PF, Crest Factor and THD requirements) and cost requirements.