Product Qualification Report

IPAN60R650CE

CoolMOS™

Description

This product qualification report describes the characteristics of the product with respect to quality and reliability.

The qualification sample selection was done on production lots which were manufactured and tested on standard production processes and meet the defined requirements.

The qualification test results of those products as outlined in this document are based on **JEDEC** for target applications and may reference existing qualification results of similar products. Such referencing is justified by the structural similarity of the products.

Qualification Assessment

Qualified according to **JEDEC Standard** and assessed as PASS

For further information about comparable products, please contact the nearest Infineon Technologies office (www.infineon.com).

IPAN60R650CE
PG-TO220-3
MSL: NA; through hole device

qualified since 2014

Electrical Stress Test Results:

Test Description	Abbr.	Condition	Duration	Lots/SS	Fail/Qty	Result
High Temperature Reverse Bias JESD22 A108	HTRB*	Ta ≥ 150°C VDS ≥ 80%VDSmax	500 h	7 x 77	0 / 539	PASS
High Temperature Gate Bias JESD22 A108	HTGB*	Ta = 150°C VGS = +/-20V	500h	7 x 77	0 / 539	PASS
High Humidity High Temp. Reverse Bias JESD22 A101	H3TRB*	Ta = 85°C rh = 85% V_{DS} = 80V	500h	7 x 77	0 / 539	PASS
Intermitted Operational Life Test MIL-STD 750 / Meth.1037	IOL*	Delta T =100K	7500 cyc	6 x 77	0 / 462	PASS
ESD (HBM) JESD22-A114	HBM	Class 1B 500V to < 1000V				PASS
ESD (CDM) JESD22-C101	CDM	Class C3 ≥ 1000V				PASS

Environmental Stress Test Results:

Test Description	Abbr.	Condition	Duration	Lots/SS	Fail/Qty	Result
Pre-conditioning J-STD020 / JESD22 A113	PC	MSL and 3 x reflow		4 x 462	0 / 1848	PASS
Temperature Cycling JESD22 A104	TC*	-55°C to +150°C	500 cyc	7 x 77	0 / 539	PASS
Autoclave JESD22 A102	AC*	Ta = 121°C rh = 100%	96 h	7 x 77	0 / 539	PASS
Wave solder simulation for SMD devices JESD22 A111	WS*	T=260°C / 1 x 10sec and Temperature Cycling -55°C to +150°C; 100 cyc.		4 x 30	0 / 120	PASS

Notes:

* For SMD devices reliability stress tests performed after preconditioning test (PC) according to JESD22

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Document reference

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