

Customer connector presentation
2EDL90xG3

June 2026

Restricted

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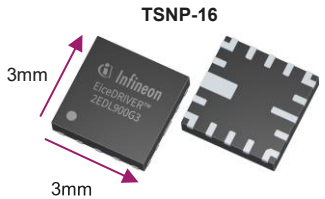
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2EDL90xG3 at-a-glance: Common Footprint Driver for Si and GaN with Integrated Current Sensing and Tri-state single PWM Input + DTC

Key features

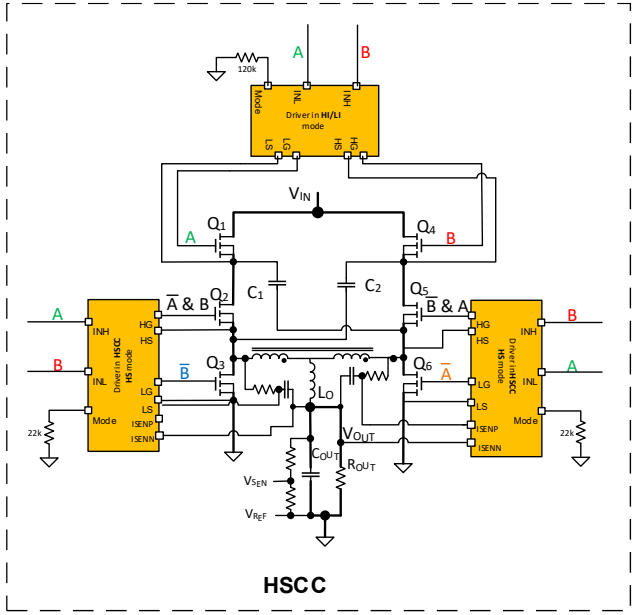
- Level-shifted dual channel floating output driver
- Wide VDD supply voltage range 4 V - 15 V
- 5V gate clamp for high efficiency GaN driving
- UVLO: 3.8 V rise and 3.6 V fall
- Configurable PWM input
  - Single PWM input supported tri-state, adjustable deadtime
  - Hi/Li and Hi/ Li invert independent PWM input
  - HSCC HS/ LS modes
- 3.3 V compliant PWM input logic and endure 5 V max
- **2EDL900G3** 4 A / 6 A source and sink current for **Si switches**
- **2EDL901G3** 1.6 A/ 6 A source and sink current for **GaN switches**
- 120 V absolute maximum voltage on HB and LB
- 15 ns typ prop delay
- 6 ns – 100 ns adjustable deadtime or turn-on delay (DTC)
- Inductor DCR/ shunt based current sensing and report (current sensing amplifier)
  - +/-1% typ accuracy at FS
  - 5 MHz typ bandwidth

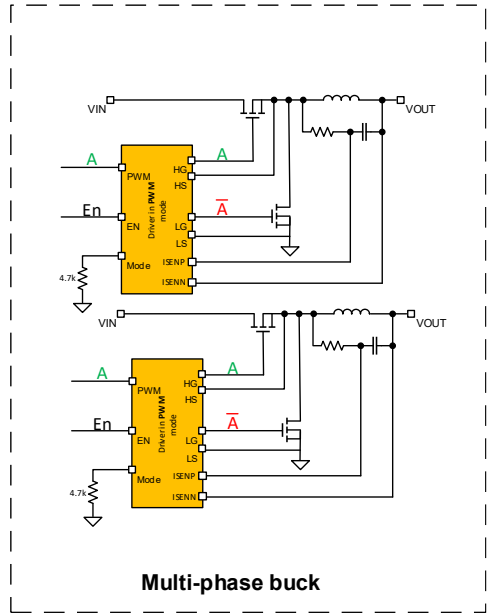


Value Proposition

- **Dual floating architecture supporting wide range of power topologies:**
  - HVBuck, Hybrid SC, 3 levels Buck, HV Series Cap Buck, Switch Cap Converter, HBCD
- Configurable for Hi/Li inputs or single tri-state input for multi-level topologies
- High efficiency and safe GaN driving thanks to integrated gate clamp
- Reduced system BoM with integrated current sensing

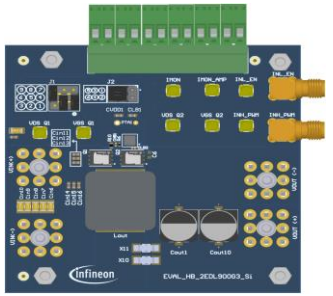
Typical Applications





Resources

- Datasheet
- **Evaluation Board:**
  EVAL_HB_2EDL900G3_Si
  EVAL_HB_2EDL901G3_GaN
- **Simulation Model:**
  2EDL900G3
  2EDL90G3 (planned)



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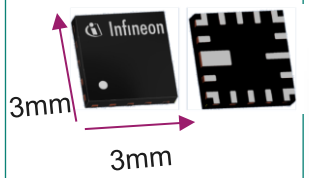
Highest Efficiency Interleaved Buck Topology for MV IBC
Simplifies 6 Phase ILVB Boost SYS Efficiency

Two OPNs

2EDL900G3 (Si Driver)
4 A / 6 A source/sink

7 OptiMOS™

TSNP-16

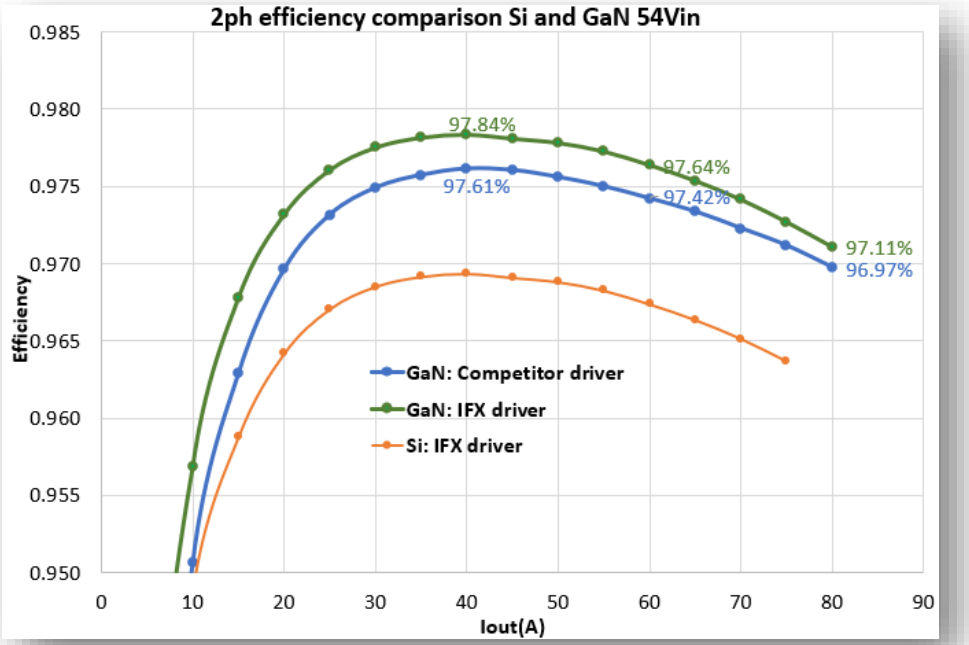


2EDL901G3 (GaN Driver)
1.6A/6A source/sink
5V gate clamp

GaN

- Common footprint
- Interchangeable Si and GaN gate drivers
- Simplifies testing w/ no additional BOM

Infineon **Gate Driver & GaN** enables higher system **efficiency** with unique integrated 5V gate clamp - GaN & Si driver with common footprint design enables **smooth enablement** of Si and GaN on the same board.



Enhanced system performance with GaN

~1% higher efficiency with GaN compared to Si, Infineon Gate Driver delivers 0.2% higher efficiency compared to competition

Common foot print to drive both Si and GaN

- Interchangeable Si and GaN gate drivers
- Simplifies testing w/ no additional BOM

Enables multiple topologies

- Enables HSCC, HSC w/ GaN
- Drives HV-IBC secondary side

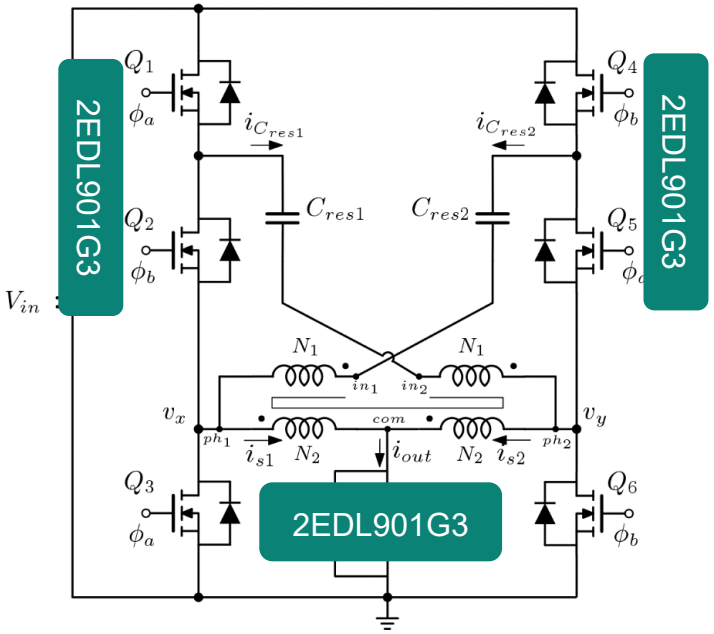
Integration to enable **Common Footprint | control loop, telemetry & protections**

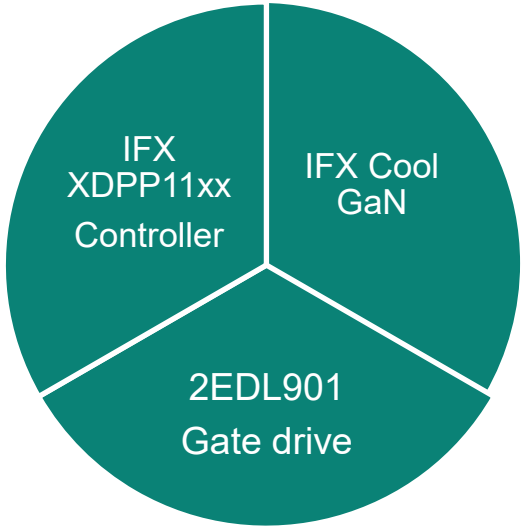
- 5V gate clamp to enable GaN with CFP
- High accuracy (typ 1% at FS) Current Sense Amplifier for fast control loop regulation and protection

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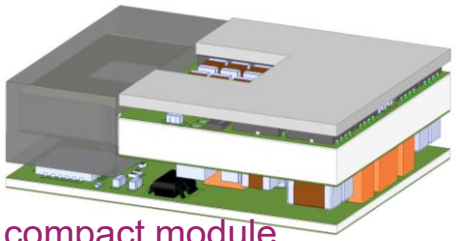
2EDL901G3 + GaN

Enable unregulated HSC topology w/ GaN for IBC Module





Enable
higher power density



compact module

2EDL901G3 Value Proposition in HSC

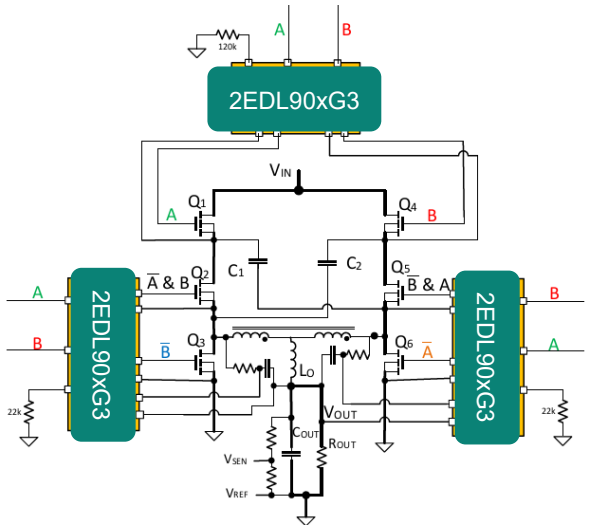
- Dual floating architecture best fit for HSC
- Dual 5 V gate clamp enabling optimal GaN driving
- Small system BoM w/ integrated current sensing

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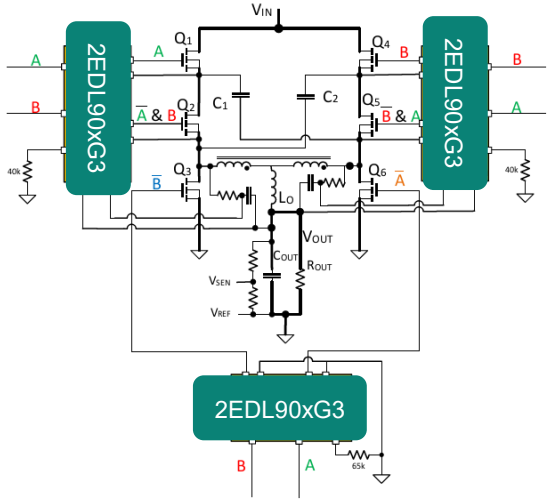
2EDL90xG3 + Si / GaN

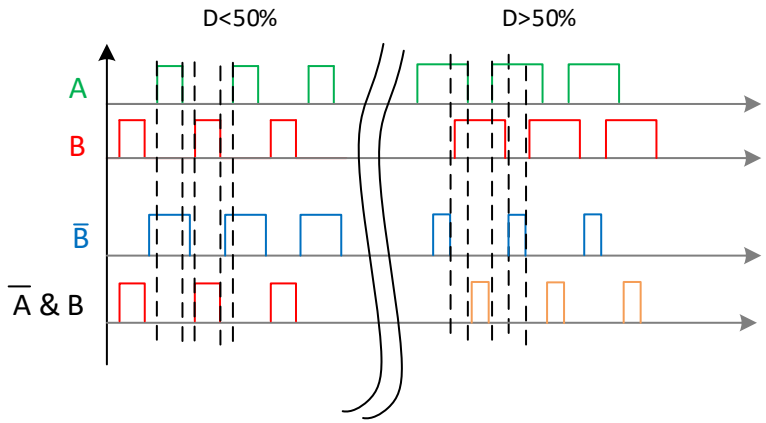
Enable regulated HSC topology for high power PDB & Module solution

HSCC HS



HSCC LS



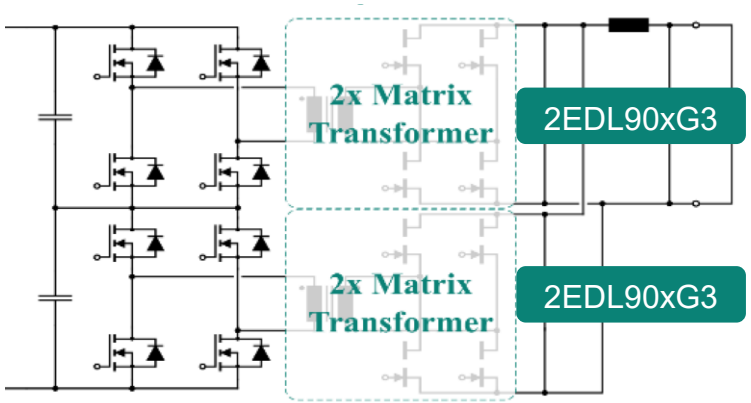


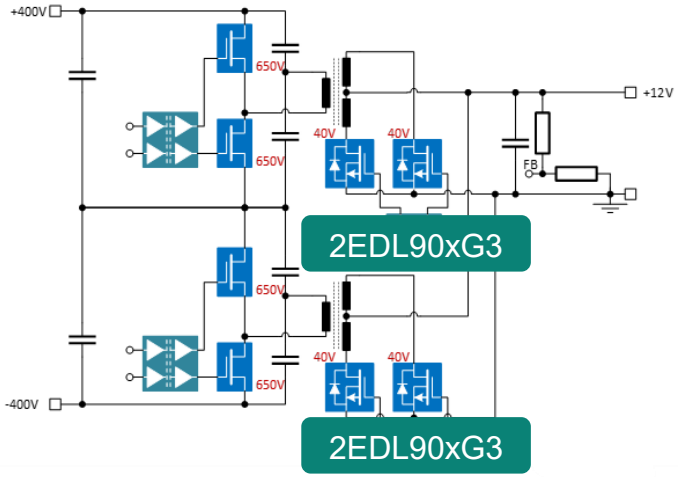
2EDL90xG3 Value Proposition in regulated HSC topology

- Only 2 PWM signals for 6 switches in regulated HSC
- Driving GaN in both HSCC HS and HSCC LS mode
- Configurable deadtime for master driver
- Configurable turn-on delay for slave driver
- Integrated CSA for DCR based or shunt based current sensing

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2EDL90xG3
Use Case in 800 V / ±400 V HV-IBC





2EDL90xG3 Value Proposition in HV-IBC

- Capable of driving both GaN and Si in SR side
- Operating frequency up 2 MHz
- 6 A pull-down reduced switching loss
- Low prop delay 15 ns
- Integrated boot diode

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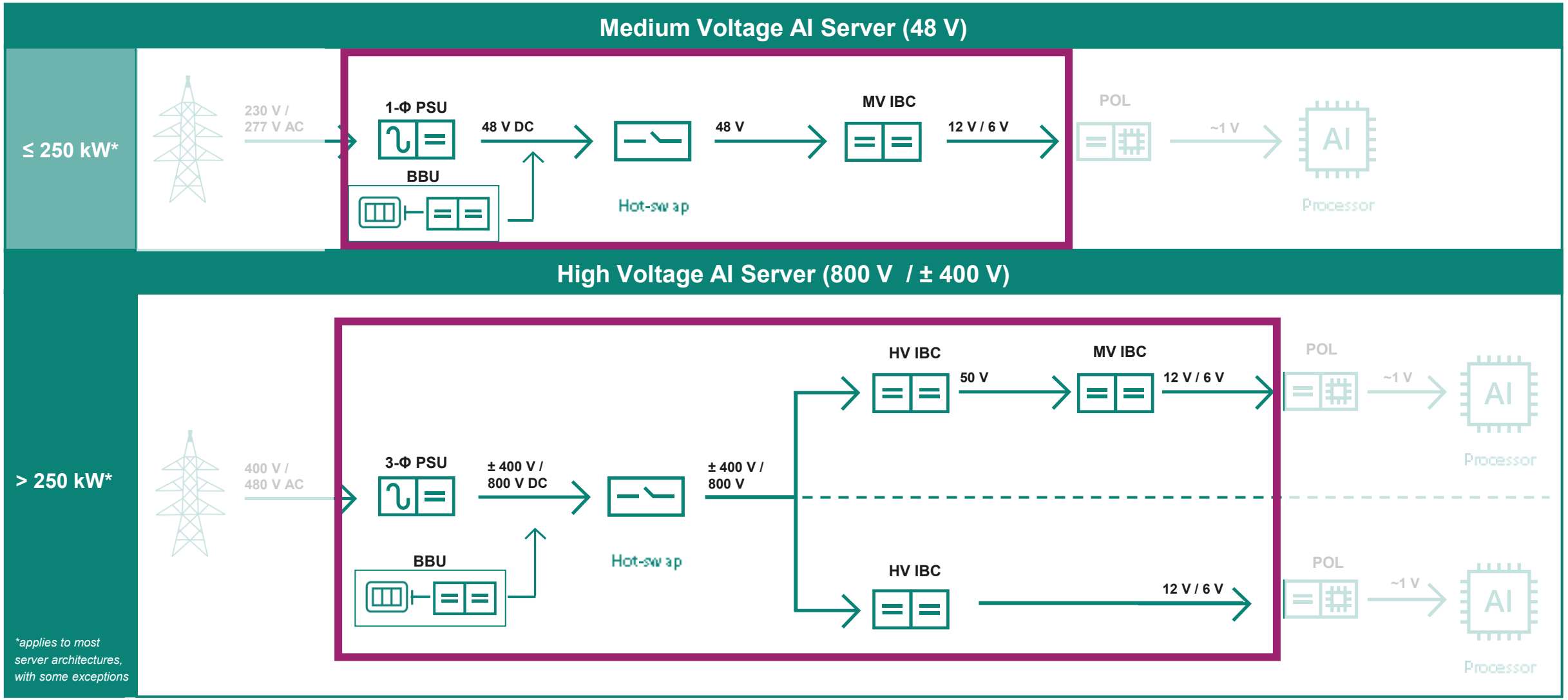
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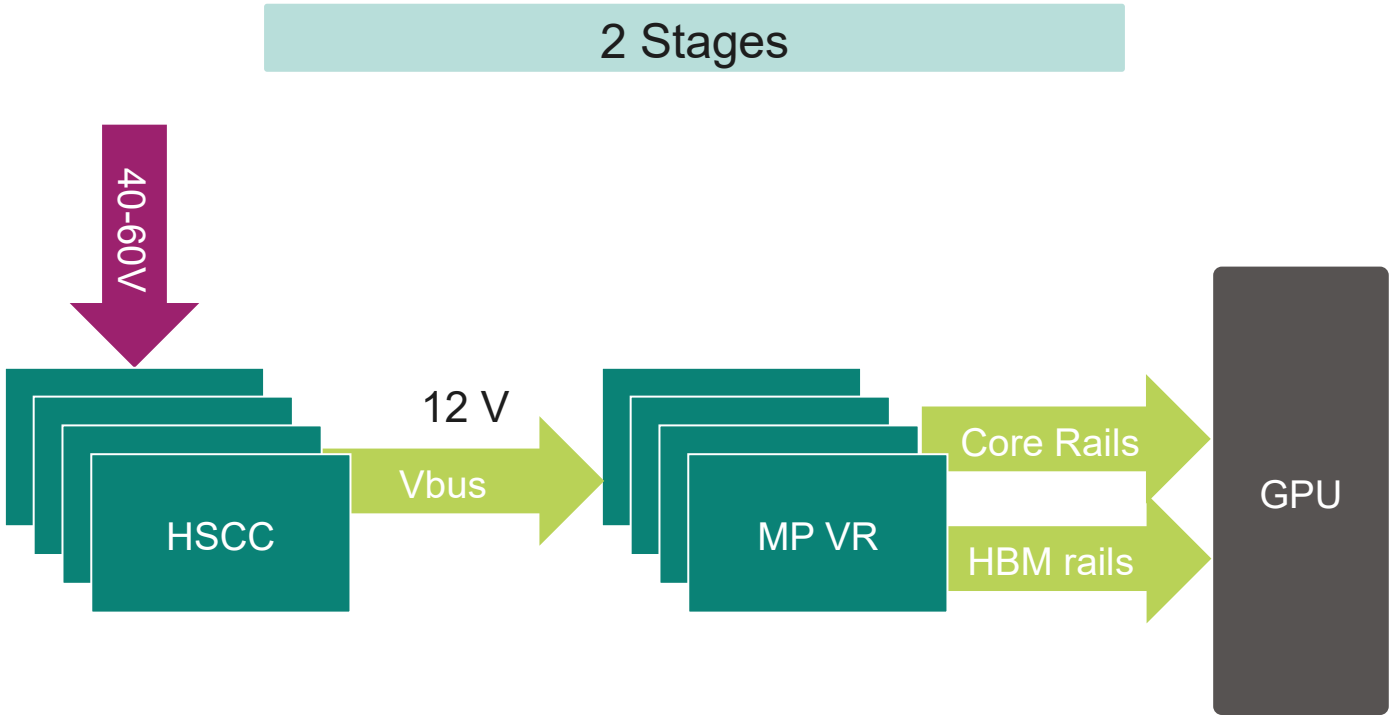
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System Overview
Datacenter/ Server (PSU & IBC)



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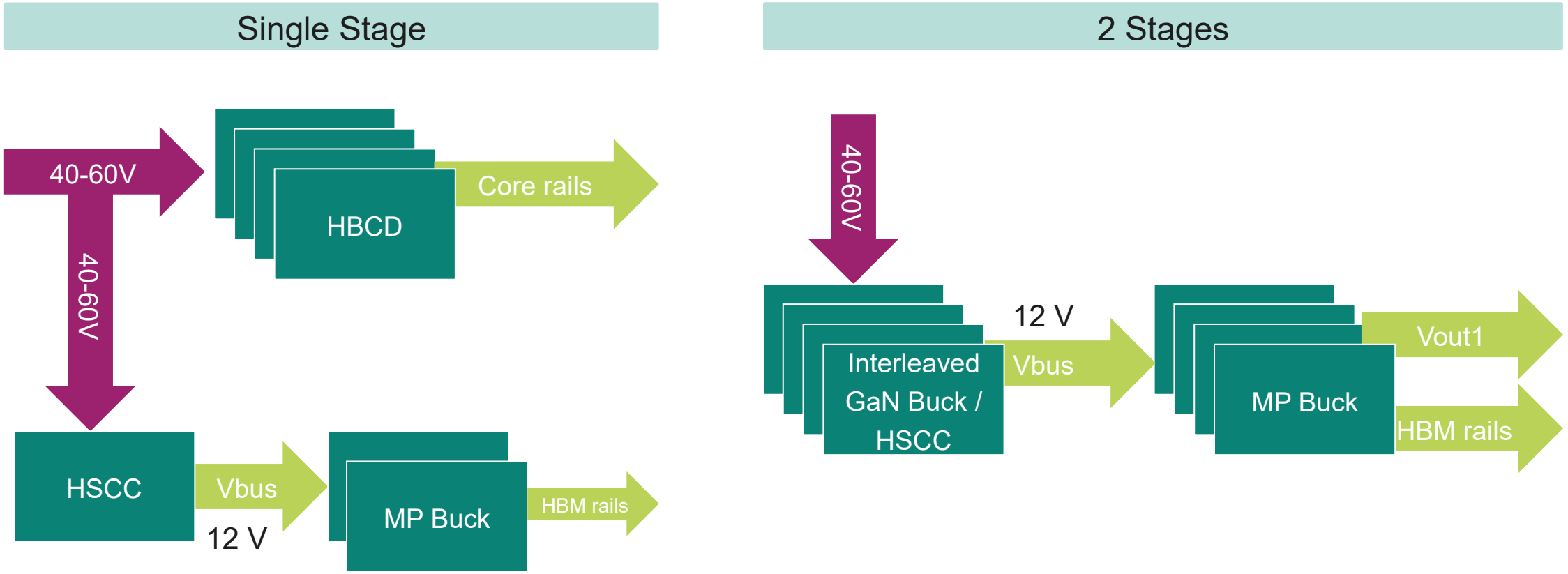
IBC to Core Supply System Architecture
Current State of Art Two Stage Solution



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IBC to Core Supply System Architecture

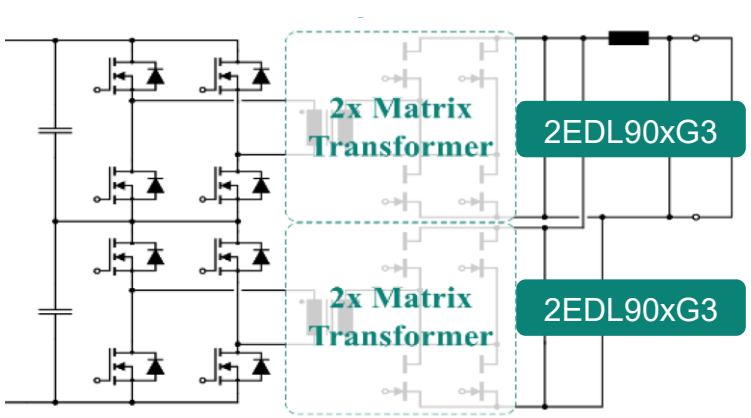
Future trend – common footprint driver + controller to address all topologies

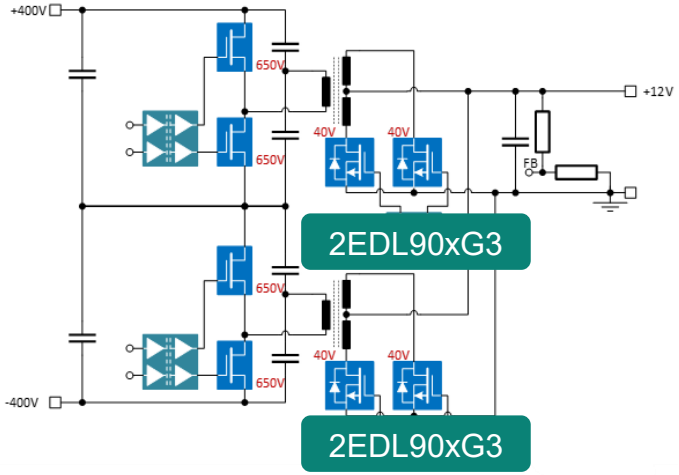


- IFX can provide total solutions for all future designs
- **2EDL90xG3 to address Interleaved Buck, HSCC, HBCD, all possible topologies**

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2EDL90xG3
Further opportunities in 800 V / ±400 V HV-IBC





2EDL90xG3 Value Proposition in HV-IBC

- Capable of driving both GaN and Si in SR side
- Operating frequency up 2 MHz
- 6 A pull-down reduced switching loss
- Low prop delay 15 ns
- Integrated boot diode

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How 2EDL90xG3 addresses the challenges in IBC application?

Key requirements in application	Typical challenges	Infineon solution features and benefits
– Small footprint – Common footprint to drive either Si or GaN – Address multiple topologies in IBC – Integrate CSA – Good thermal performance	– High number of BOM – Impossible to address multiple topologies with the same driver – Single source	– IFX offers the common footprint driver for Si and GaN with different OPNs – IFX offers dual floating output architecture to address multiple topologies in IBC – IFX offers 3x3 smallest footprint with 16 pins and integrated with CSA and other features to enable high power density design

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What is Infineon's 2EDL90xG3 positioning?

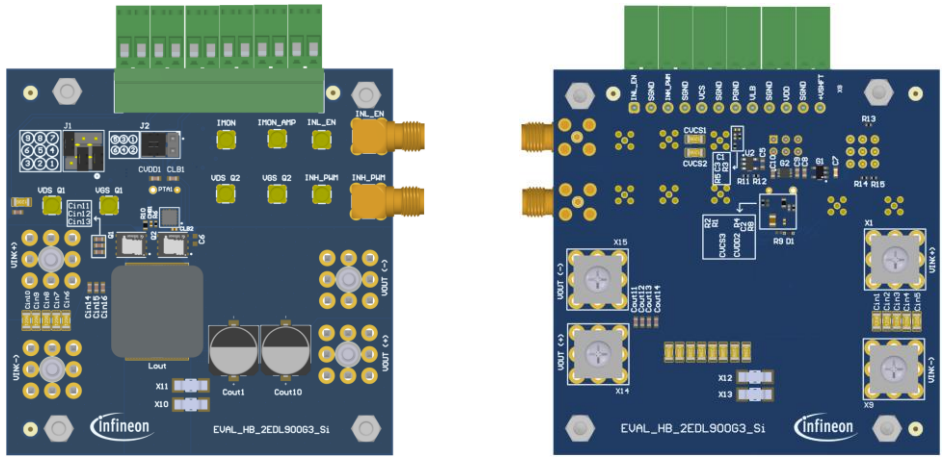
	MV gate driver offering				
PN	2EDL8x2x	2EDL6014AC-G2D	2EDL900G3	2EDL901G3	2EDL501xAA-U2D
Driver type	High and Low	Dual floating	Dual floating	Dual floating	Half-bridge
Package (mm x mm)	3x3 & 4x4	2.2 x 2.2	3 x 3	3 x 3	2 x 2
# of Pins	10 & 8	11	16	16	12
Creepage HV/LV (mm)	0.27 & 0.36	0.5	0.4	0.4	0.2
VDD range (V)	8 … 17	4 … 16	4.5 … 15(TBV)	4.5 … 15(TBV)	4.5 … 5.5
IPU/IPD (A)	3-4/5-6	4/6	4/6 (Si)	1.5(TBV)/6 (GaN)	1.5/4, 1.5/1.5, 4/4
Tprop (ns)	45	20	15	15	20
Min Input Pulse (ns)	40 (max)	10	15 (TBV)	15 (TBV)	10
Negative SW (V)	-12 (<100ns)	-12 (<100ns)	-5 (DC)	-5 (DC)	-5 (DC)
Split Output	N	N	N	N	Y
Starve Function(adj. pull-up strength)	N	Y	N	N	N
Bootstrap switch/diode	Y	N	Y	Y	Y
5V Gate Clamp	N	N	N	Y	N
3-state PWM w/ DTC	N	N	Y	Y	N
Current sense amplifier	N	N	Y	Y	N
Miller Clamp	N	N	N	N	Y
Switch Technology	Si	Si	Si	GaN	GaN
ES / SOP	Available / Released	Available / June 2026	Available / Released	Available / July 2026	Available / September 2026

** 2EDL6014AC-G2D and 2EDL900G3 can drive IFX G5 GaN w/ ext. clamp*

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Kits/boards overview
Evaluation Board for 2EDL90xG3

EVAL_HB_2EDL900G3_Si & EVAL_HB_2EDL901G3_GaN



Technical & order details

Parameter	Value
Topology	Buck
Input voltage	36-60 V
Output voltage	Duty Dependent

Learn more		
Sales name	EVAL_HB_2EDL900G3_Si EVAL_HB_2EDL901G3_GaN	
Infineon order code	SP006165917 SP006165959	
IFX Components	For Si: 2EDL900G3 ISC016N08NM8SC ISC031N08NM6SC	For GaN: 2EDL901G3 IGD015S10S1
Focus Application	IBC	

Features

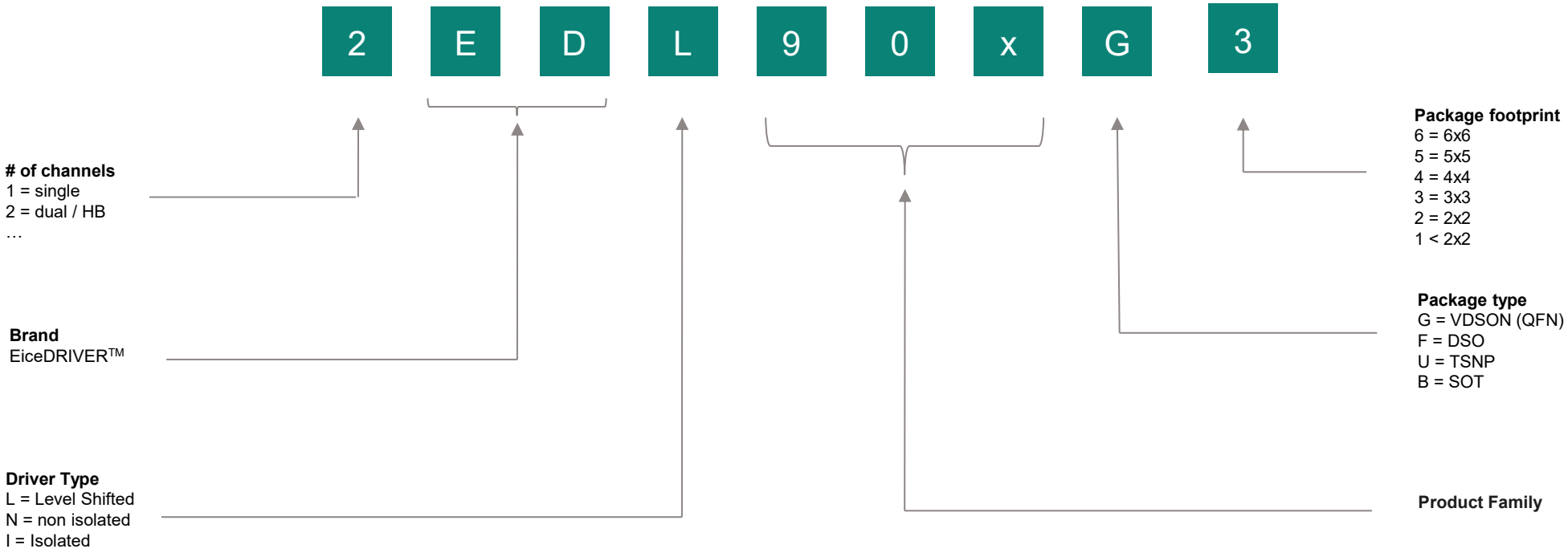
1. Open loop buck converter topology
2. Easy settings for either dual floating or typical half bridge configuration
2. Easy settings for the different mode functionality of 2EDL90xG3
3. Probing test points measurement ready

Benefits

1. Easy configuration and evaluation of functional features of 2EDL90xG3

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Product naming nomenclature



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Ordering information

OPN Ordering part number	SP number Ordering Code	MDQ/MQQ/MOQ*	Registerable	Package
2EDL900G3XTMA1	SP006165917	5000/5000/5000	Yes	PG-TSNP-16-5
2EDL901G3XTMA1	SP006165959	5000/5000/5000	Yes	PG-TSNP-16-5

Note:
The information presented is valid from 01 June 2026. Please check the latest Distribution Price Book for current prices and minimum quantities

* MDQ: Minimum Design Quantity
MQQ: Minimum Quote Quantity
MOQ: Minimum Order Quantity

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Guiding questions

Summary of key arguments

– 2EDL90xG3 enables driving medium voltage Si or GaN with a common footprint device that also simplifies testing of either solution with the same PCB

Questions to ask to the customer

– Which is power topology in your application?
– What is the Vin, Vout and power level?
– Which power switch is be used?

FAQs

– **Which driver is the best for interleaved buck (ILVB) topology?**
– 2EDL90xG3

– **What is the key value proposition of 2EDL90xG3?**
– 2EDL90xG3 enables driving medium voltage Si or GaN with a common footprint device that also simplifies testing of either solution with the same PCB.

– **Which features in the 2EDL90xG3 help reduce the overall system BOM?**
– Integrated current sensing, single tri-state PWM input

– **What can customer implement with the integrated current sensing in 2EDL90xG3?**
– Customer can use it for OCP, SCP and telemetry.

– **What are the advantages of the 5 V gate clamp feature in 2EDL901G3 GaN driver?**
– It enables high efficiency GaN driving with optimal 5 V turn-on while it allows wide input supply range(4-13.2 V).

– **What is the advantage of dual channel floating architecture in 2EDL90xG3?**
– It provides flexibility for all power topologies in IBC. Especially, it enables HSC topology with GaN.

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