

基于英飞凌最新氮化镓技术的数据中心 6kW HV IBC 电源模块方案

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restricted

Agenda

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2	Topology Selection	7
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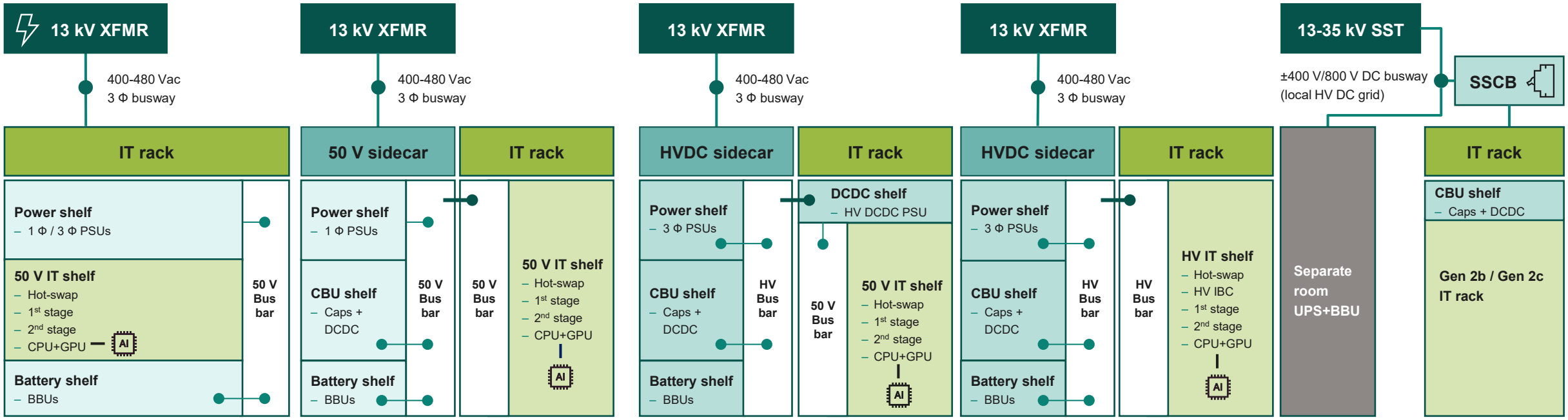
Introduction

AI server rack architecture evolution in the upcoming years

From IT + Power in one rack, power sidecar to hybrid microgrid



Gen 1
PSU and BBU in IT rack

- 1 Φ 5.5 kW / 8 kW / 12 kW 50 V PSU
- 3 Φ 18 kW 50 V PSU

Gen 2a
PSU, CBU and BBU in 50 V sidecar

- 1 Φ 12 kW 50 V PSU

Gen 2b
PSU, CBU and BBU in HVDC sidecar 50 V IT rack

- 3 Φ HVDC 25-30 kW, ±400 V / 800 V PSU
- HV DCDC PSU in IT rack

Gen 2c
PSU, CBU and BBU in HVDC sidecar HV IT rack

- 3 Φ HVDC 25-30 kW, ±400 V / 800 V PSU
- HV IBC on IT shelf

Gen 3
DC Microgrid

- Racks powered by local HV DC grid

50 V architecture

1 Φ / 3 Φ 50 V PSU and BBU | **1 Φ 50 V PSU and BBU**

HVDC architecture

3 Φ HV PSU and HVDC BBU

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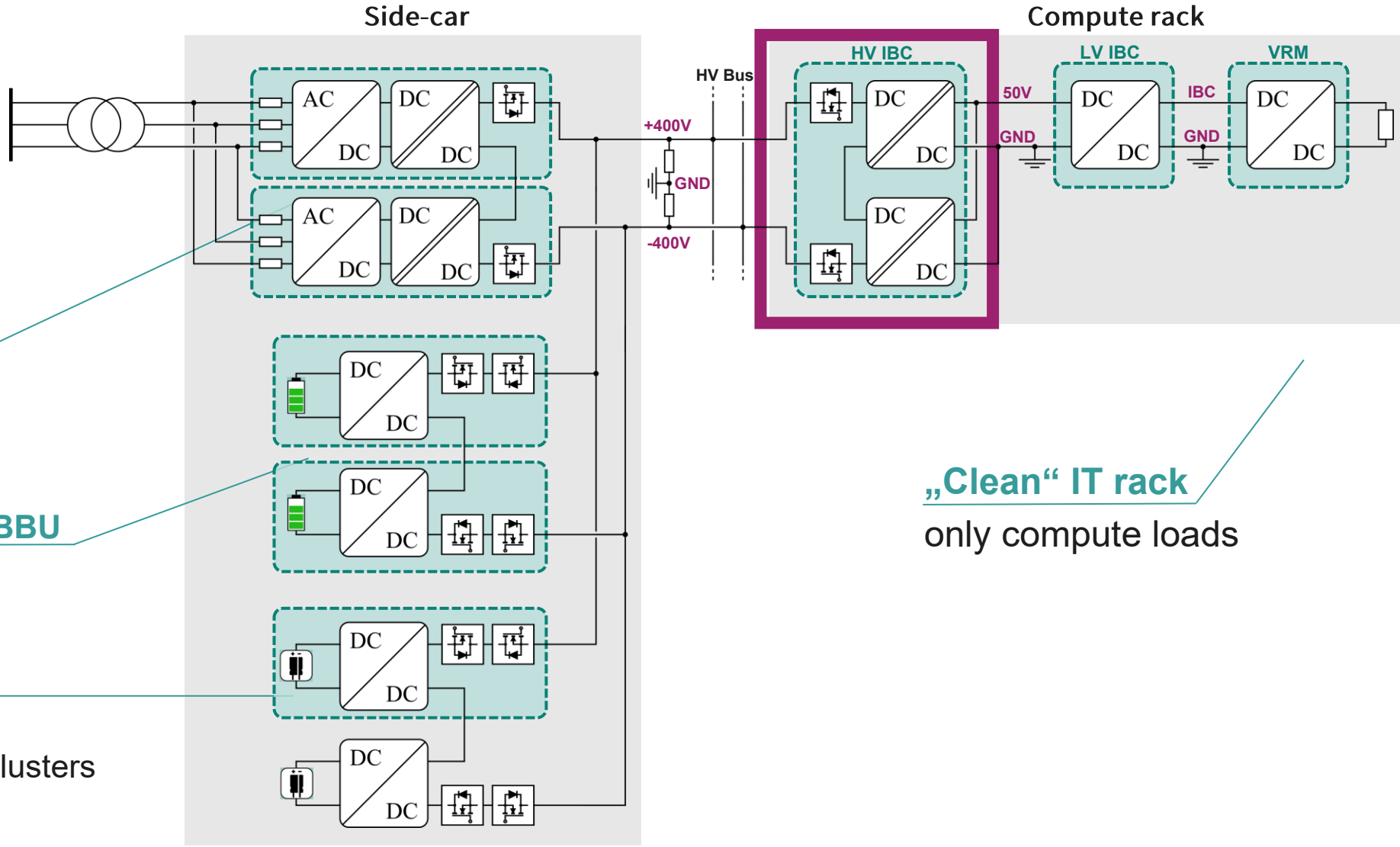
Beyond 250 kW per rack architectures need to adopt HV DC distribution, likely at 800V DC

Gen 3 PSU

~25kW+
400 / +- 400Vout

3- Φ 400-600Vac



3-phase PSUs
generating 400V DC

Li-ion battery-based BBU
for power outages

Super-cap trays
to cope with dynamic
load patterns of GPU clusters

„Clean“ IT rack
only compute loads

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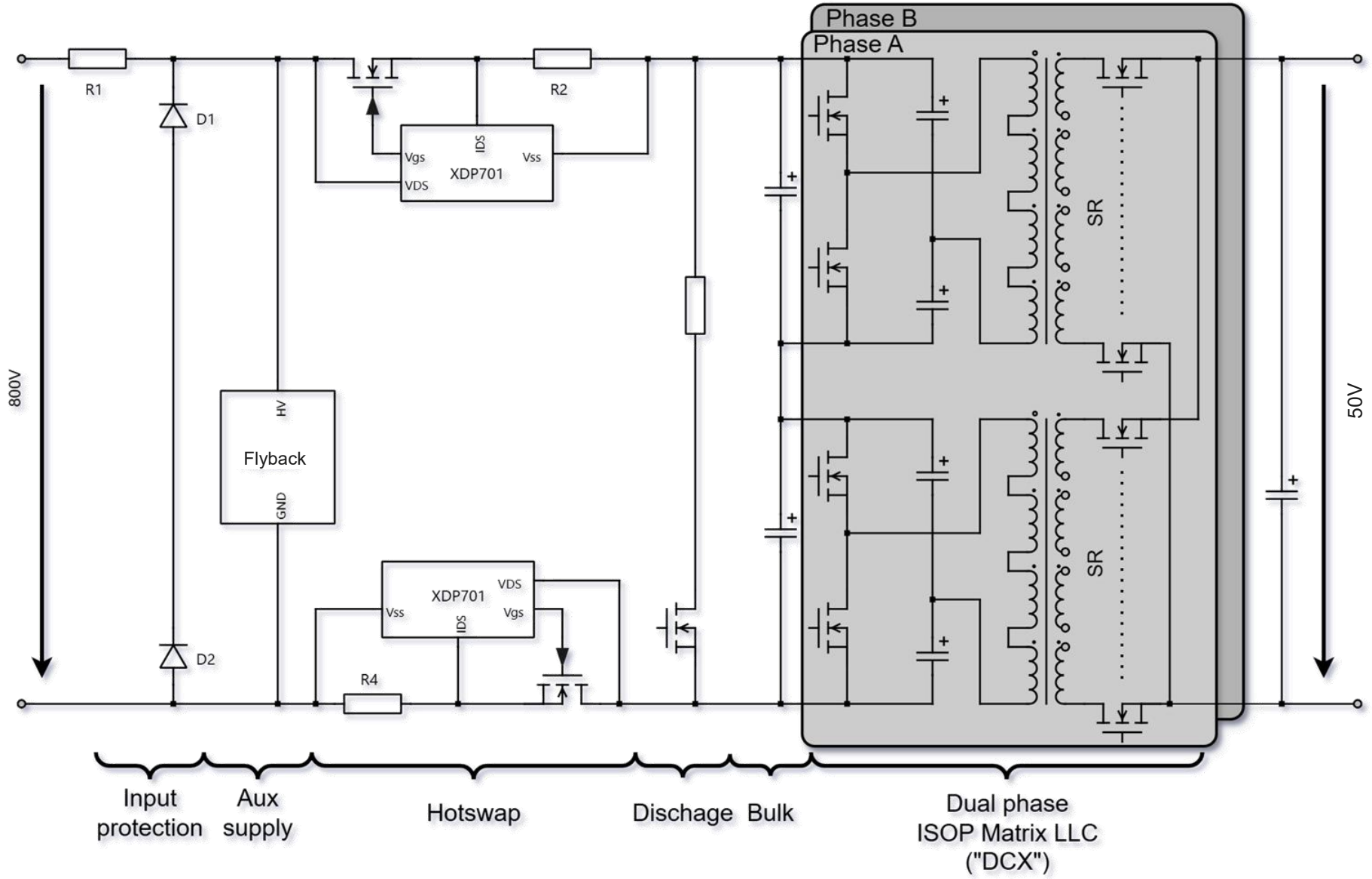
System Diagram



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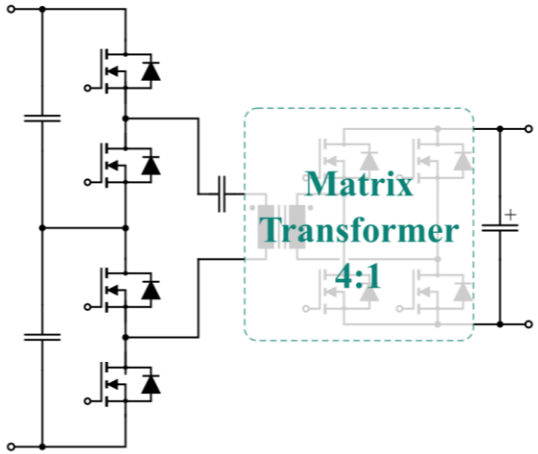
Topology Selection

Topologies for HVDC Bus Architecture

preferred solution

3L Stacked Half-bridge

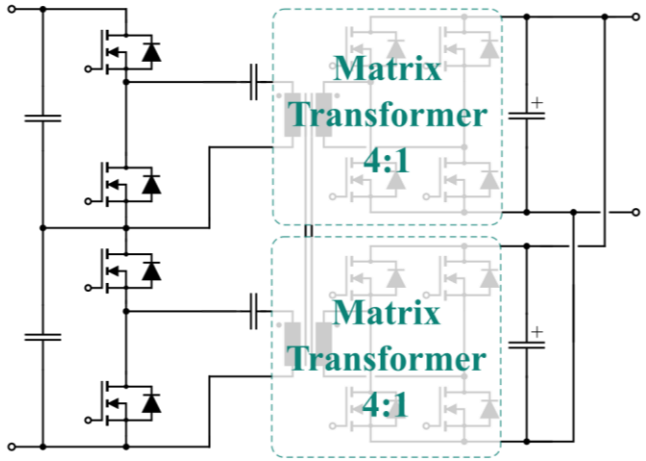


Best for: Power below 3kW

Pros: higher equivalent fsw for transformer, low current for outer devices, small component count, open IP

⇓ **Cons:** very high current for inner primary side devices, higher output current ripple (larger output capacitance)

ISOP Half-bridge DCX

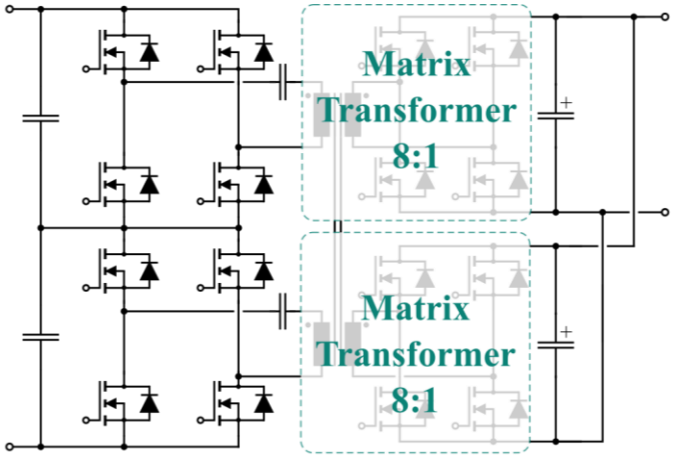


Best for: Power between 3kW and 6kW

⇑ **Pros:** good trade-off between component count and RDSon, low output current ripple (smaller output capacitance), good for medium power designs, open IP

⇓ **Cons:** higher current on primary side compared to FB solution

ISOP Full-bridge DCX



Best for: Power >6kW

⇑ **Pros:** lowest current stress on primary side, low output current ripple (smaller output capacitance), better for high power designs, open IP

⇓ **Cons:** larger number of devices

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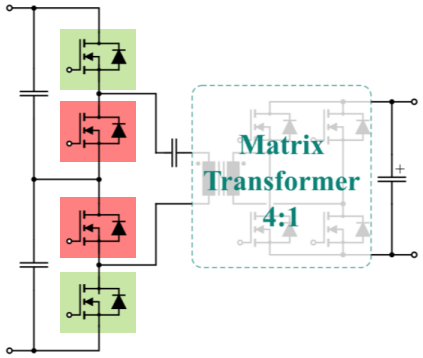
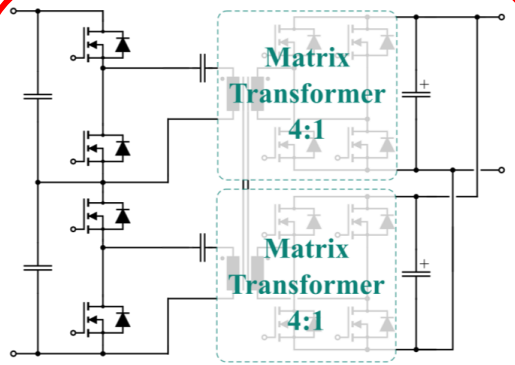
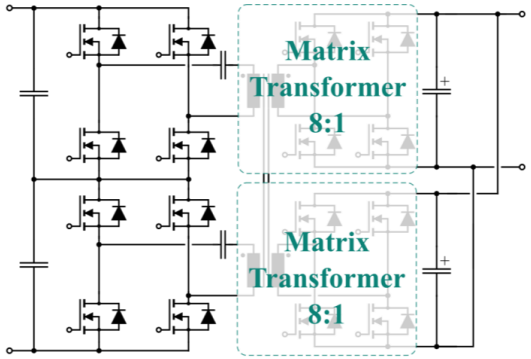
Topologies for HVDC Bus Architecture
Comparison of RMS and Peak Currents

Preferred option







	3L Stacked Half-bridge DCX	ISOP Half-bridge DCX	ISOP Full-bridge DCX
Peak currents	$2\pi \cdot \frac{P}{V_{DC}}$	$\pi \cdot \frac{P}{V_{DC}}$	$\frac{\pi}{2} \cdot \frac{P}{V_{DC}}$
RMS currents	$\frac{\pi}{\sqrt{2}} \cdot \frac{P}{V_{DC}}$	$\frac{\pi}{2} \cdot \frac{P}{V_{DC}}$	$\frac{\pi}{4} \cdot \frac{P}{V_{DC}}$

6x losses

2x losses

Twice the number of components

» 3L Stacked Half-bridge DCX has 2x the effective switching frequency but severely increased conduction losses

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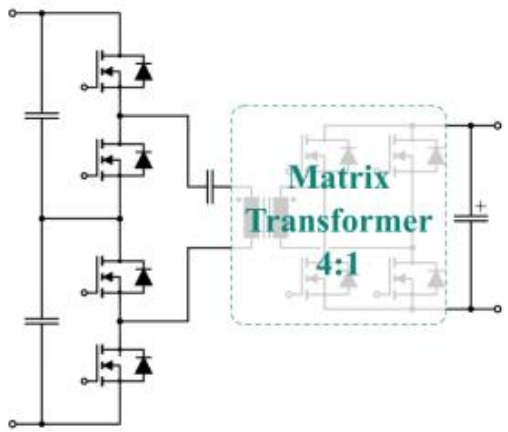
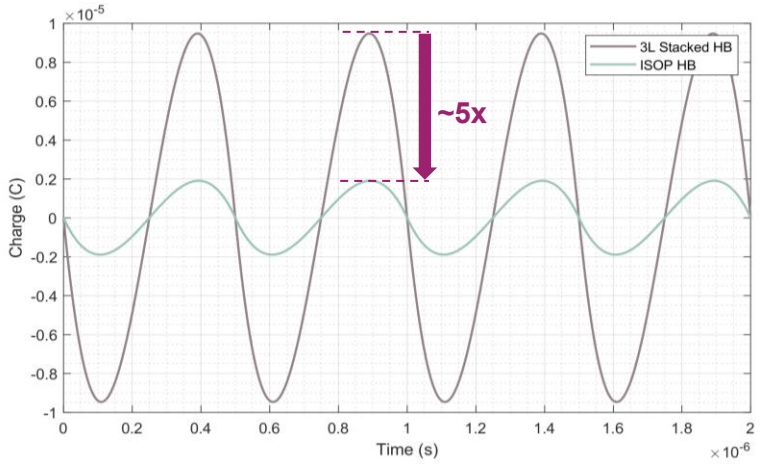
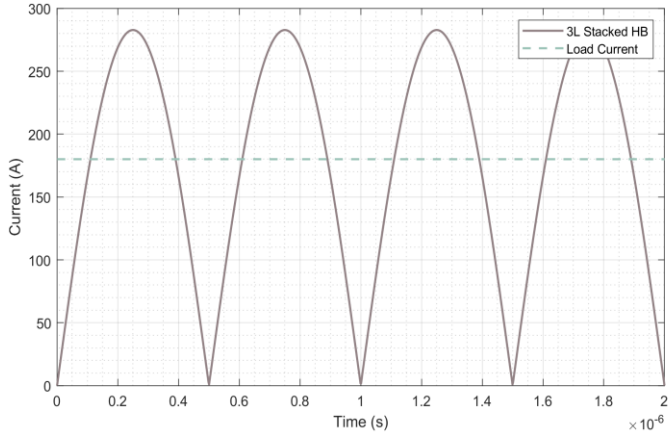
Topologies for HVDC Bus Architecture
Comparison of Output Current Ripple (1.5TDP)

1) 3L Stacked half-bridge DCX



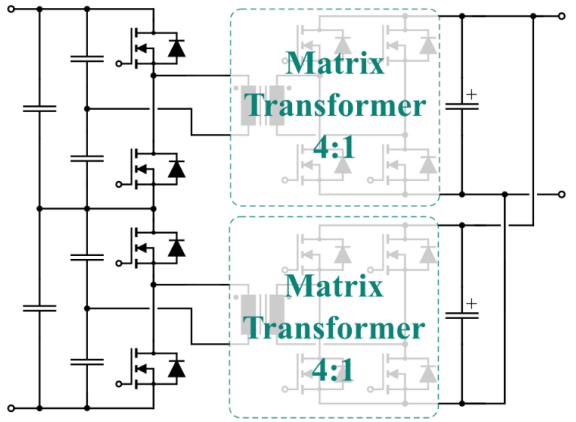


Output current

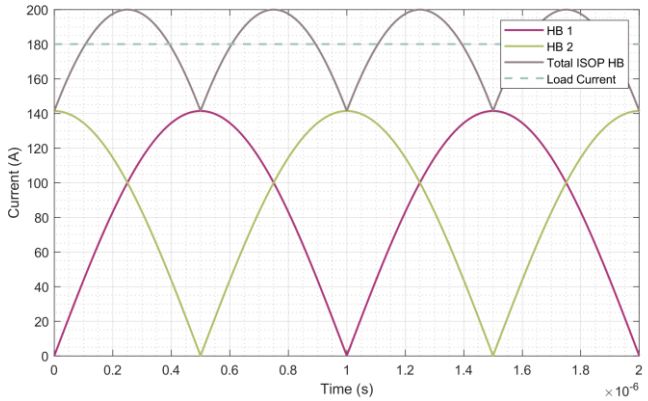


The ISOP half-bridge DCX requires **~5x** less output capacitance for the same output voltage ripple

2) ISOP half-bridge DCX



Output current



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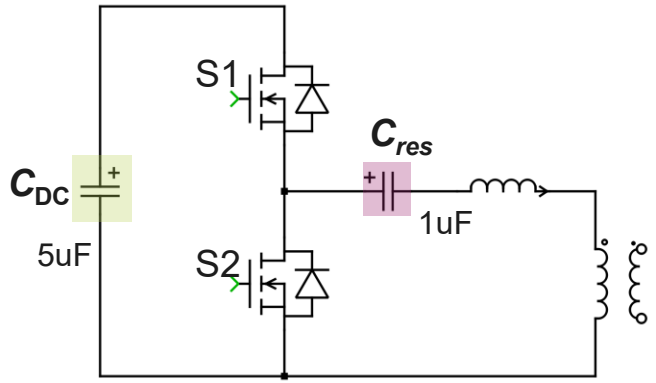
Topologies for HVDC Bus Architecture
Resonant Capacitor Placement

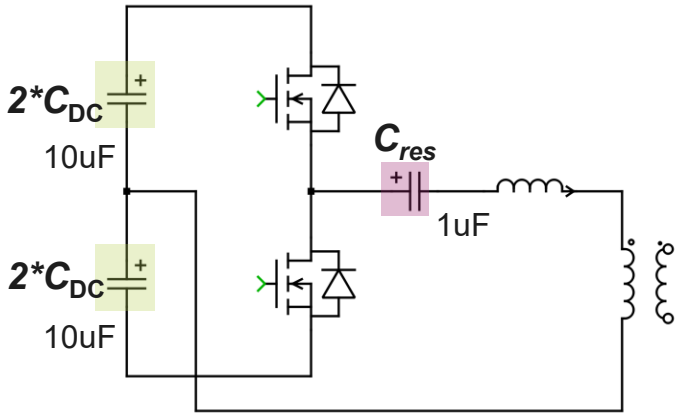
DC-link cap

Resonant cap

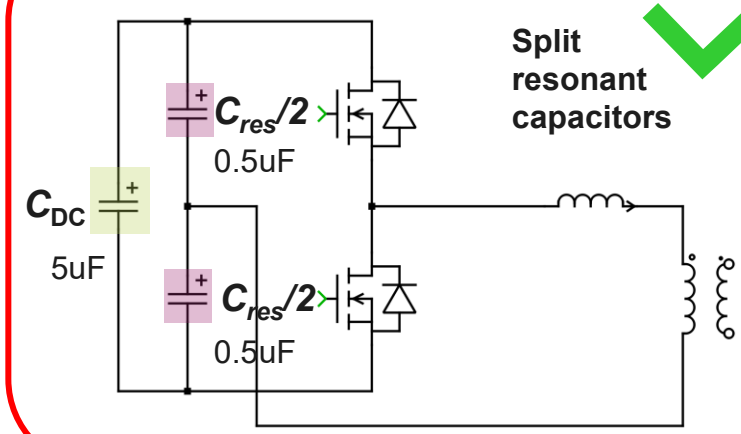
Option 1



Option 2



Option 3



Take an example: C_{DC} = 5uF, C_{res} = 1uF

S1 on: $C_{res.eq} = (1/C_{DC} + 1/C_{res})^{-1}$ = **0.83uF**

S2 on: $C_{res.eq}$ = **1uF**

$C_{res.eq} = (1/2*C_{DC} + 1/C_{res})^{-1}$ = **0.91uF**

$C_{res.eq} = (1/C_{DC} + 1/0.5*C_{res})^{-1} + 0.5*C_{res}$ = **0.96uF**

- **Option 1:** Asymmetric. The highest shift of resonant frequency.
- **Option 2:** No DC-offset on resonant cap. Double amount of C_{DC} required.
- **Option 3:** **Split resonant capacitors**, the lowest shift of resonant frequency caused by small C_{DC}/C_{res} ratio. Only half the current stress on C_{DC}. During start-up the resonant caps get also charged.

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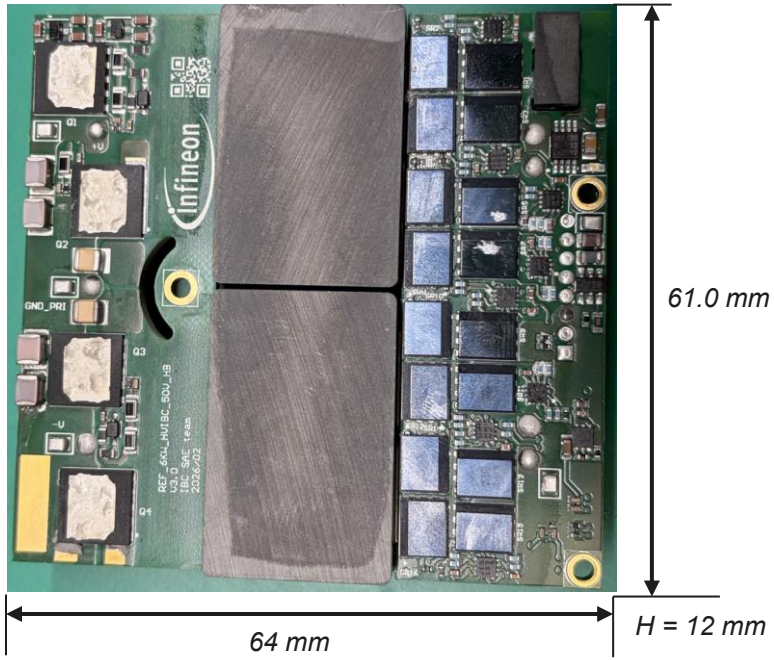
Hardware Design and Experimentation

6 kW Compact Full GaN-Based DC/DC Converter Module from ±400 V to 50 V for High-voltage IBC Application

HV GaN

MV GaN



Parameter	Value
Input voltage range	±400 V_{DC} (800 V_{DC})
Output voltage range	50 V_{DC}
Output current nominal	120 A
Output power maximum	6000 W
Efficiency target	98.5 % (peak efficiency), 98 % (full load)
Ambient temperature	25 °C (w/ Heatsink and Fan)
LLC Resonant frequency	800 kHz
Learn more	
Infineon key components	1. IGLC65R020D2 (650V HV GaN) x 4 2. IGD01XK10S2 (100V MV GaN) x 16 3. 2EDR7259X (HV GaN Gate driver) x 2 4. 2EDL5014AA-U2D (MV GaN Gate driver) x 8 5. 2EP130R (Transformer driver IC for Aux) * 1
Controller	XDPP1188 - 200C
Application	Data center power architectures (HVDC -> 50V IBC), telecom power system and industrial SMPS

Features

- **Full GaN Design :** HV GaN(primary) + MV GaN(secondary)
- **Custom Magnetic Design :** dedicated planar transformer for main power stage and auxiliary stages
- **> 2000 W/in³ Power Density :** surpassing traditional 48 V IBCs
- **High Conversion Ratio(16:1) :** enable efficient intermediate bus conversion from high-voltage DC distribution

Benefits

- **High Power Density :** 6 kW in a half-brick footprint (58.4 mm * 61 mm * 12 mm)
- **High Efficiency :** up to 98.5 % peak efficiency, which represents a state-of-the-art performance level
- **Predictable Operation :** fixed-frequency with Open-loop regulation
- **Highly Integrated Architecture :** combines control, gate driving, protection, thermal monitoring, and auxiliary power in one compact module

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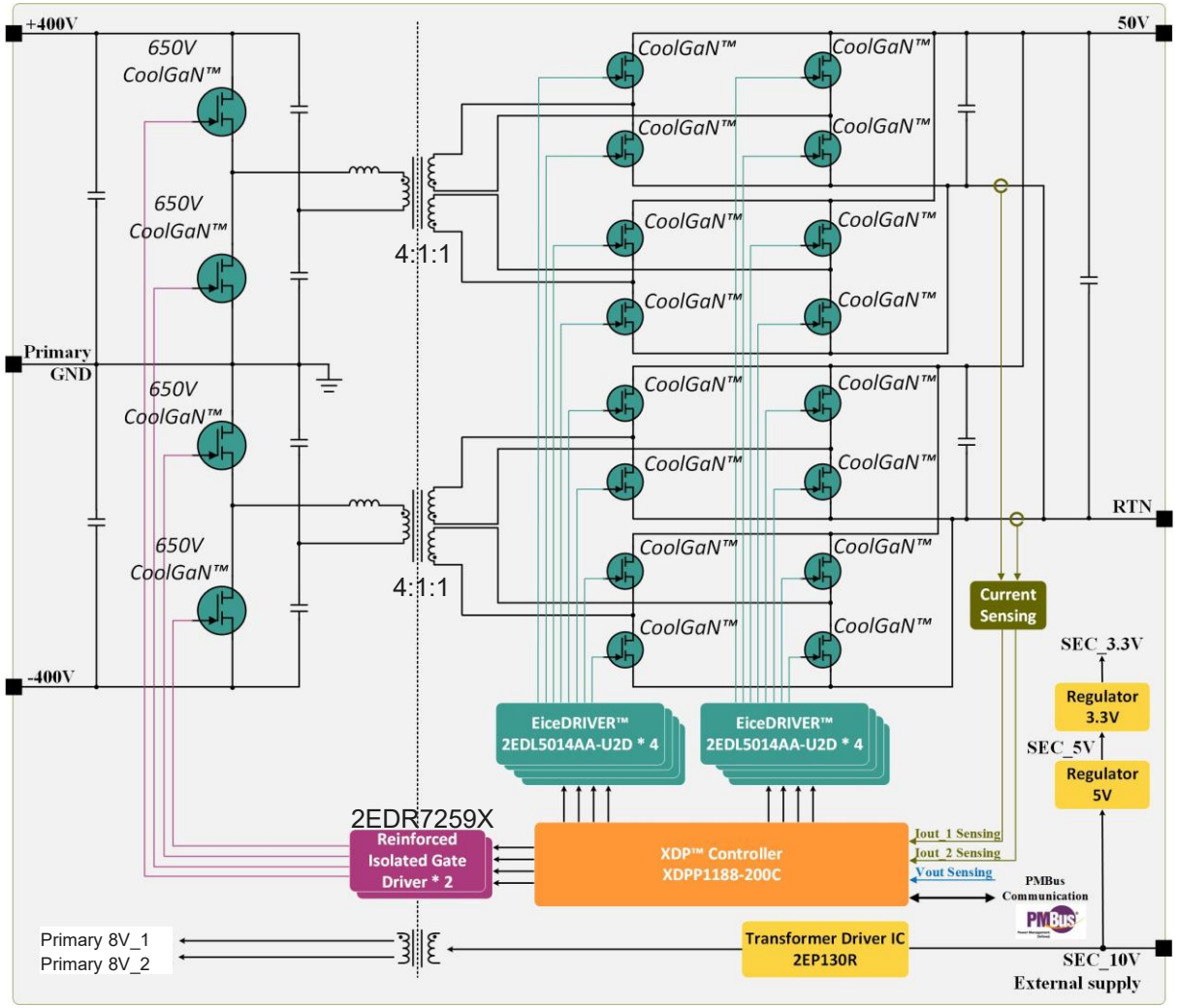
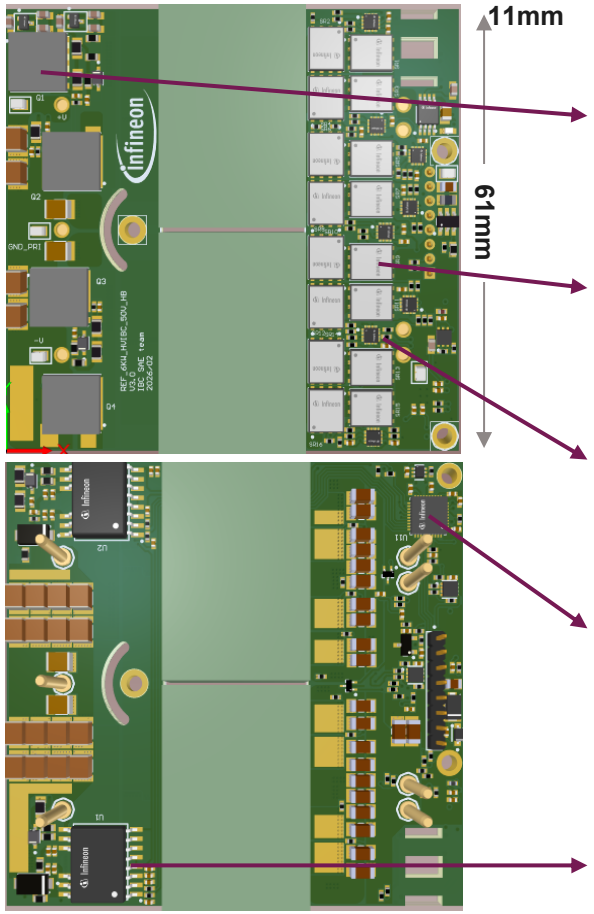
±400V to 50V 6kW HB-IBC Module Overview



Module Architecture

6kW ±400V to 50V HB-IBC module



All switches on top side for best thermal performance → TSC packages

HV Side Devices:
GaN 650V
IGLC65R020D2 x4

LV Side Devices:
GaN 100V
IGD01XK10S2 x16

Low Side Driver:
2EDL5014AA x8

Controller:
XDPP1188-200C x1

HV Side Driver:
2EDR7259X x2
Dual-channel Reinforced Insulation

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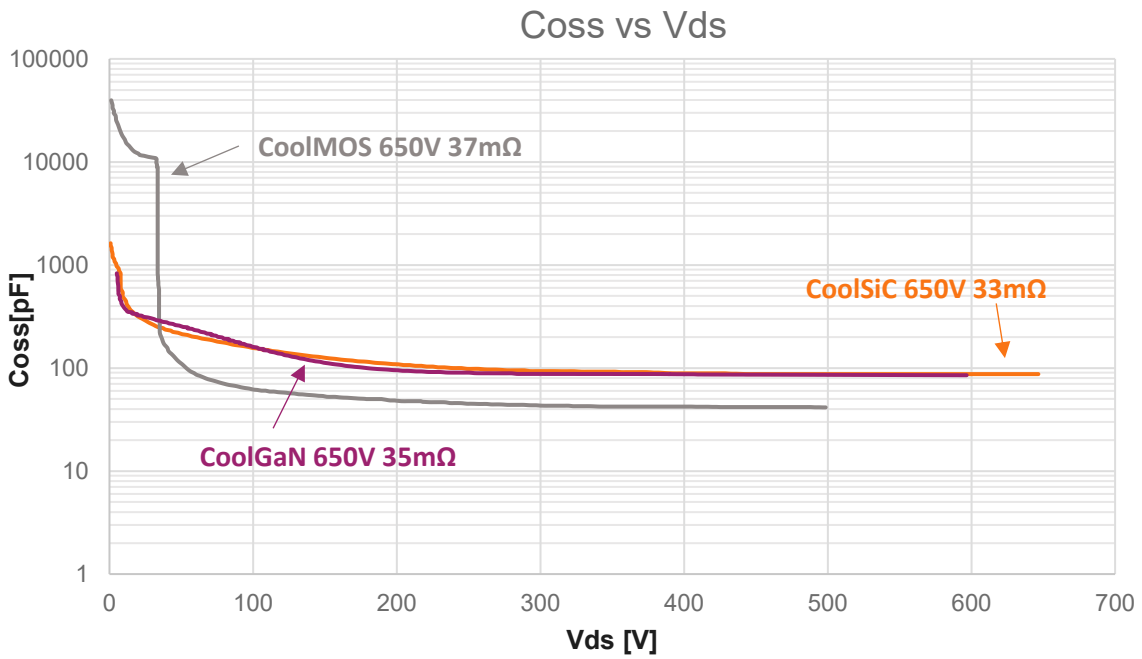
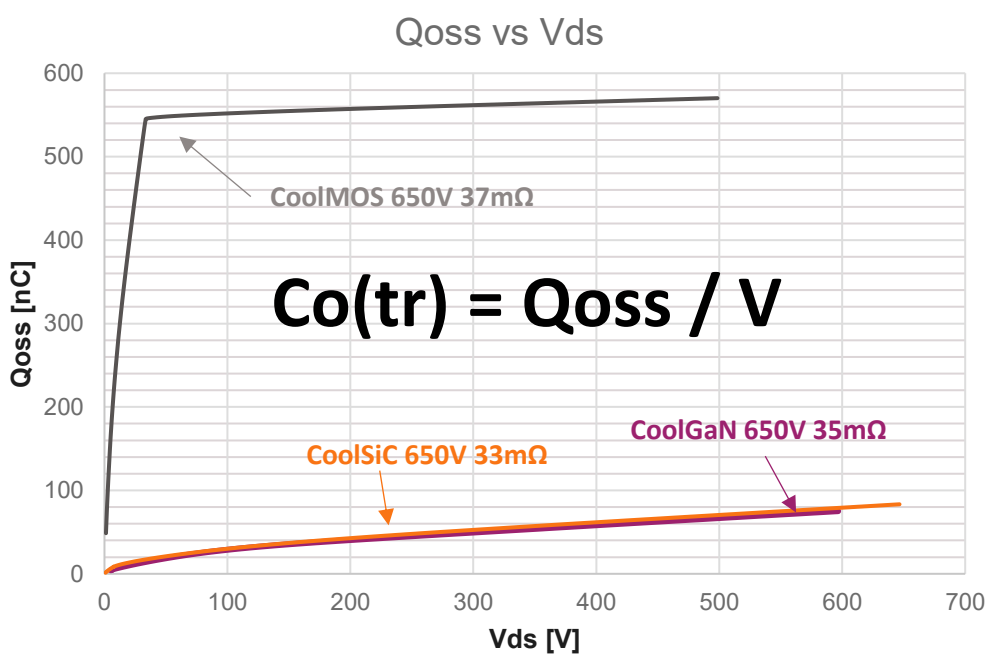
Output Capacitance Characteristics of Power Devices

$$\begin{cases} Q_{oss} = C_{o(tr)} \cdot V \\ Q_{oss} = \int_0^{Vds} Coss(v)\, dv \end{cases}$$

Coss curve → Qoss curve → Co(tr) value



10x ↓



- **CoolGaN™ has ~10x lower Co(tr) than CoolMOS™;**
- **CoolGaN™ has ~15% lower Co(tr) than CoolSiC™.**
- Smaller output capacitance results in **lower switching loss** and **easier zero voltage switching realization (ZVS)**

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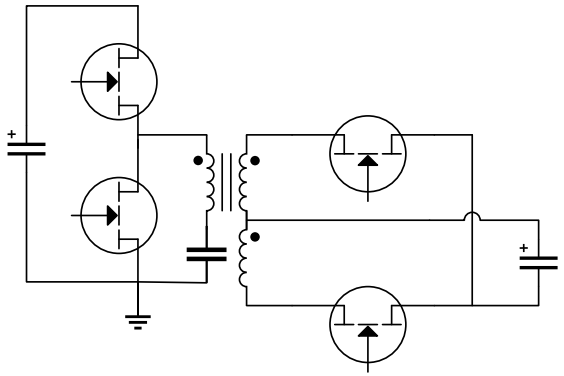
Lower Q_{oss} Unlocks the Benefits of WBG

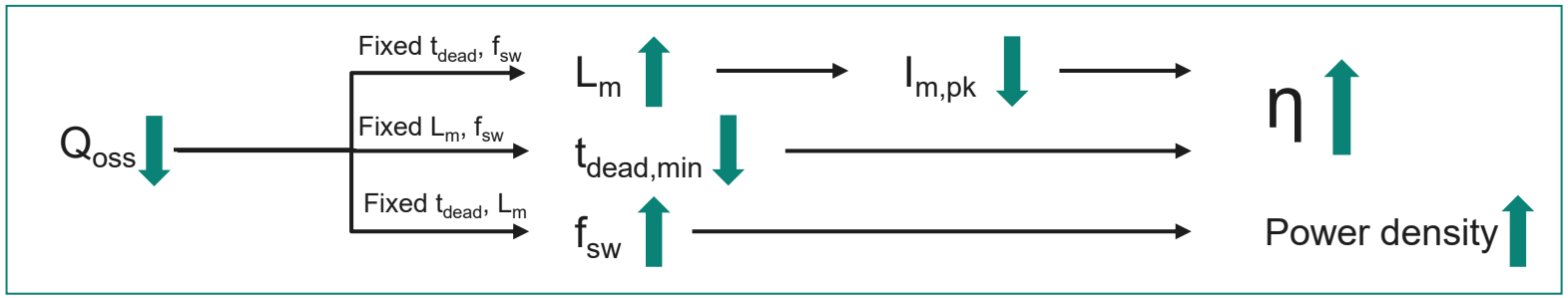
LLC Resonant



– This condition should be met for successful ZVS:

$$t_{dead(min)} = 16 \cdot C_{oss(tr)} \cdot L_m \cdot f_{sw} \quad \text{where } C_{oss(tr)} = \frac{Q_{oss}}{V_{DS}}$$

– Low **Q_{oss}** can be leveraged in different ways:



Note that high V_{SD} during deadtime may degrade the efficiency
Therefore, it calls for deadtime optimization

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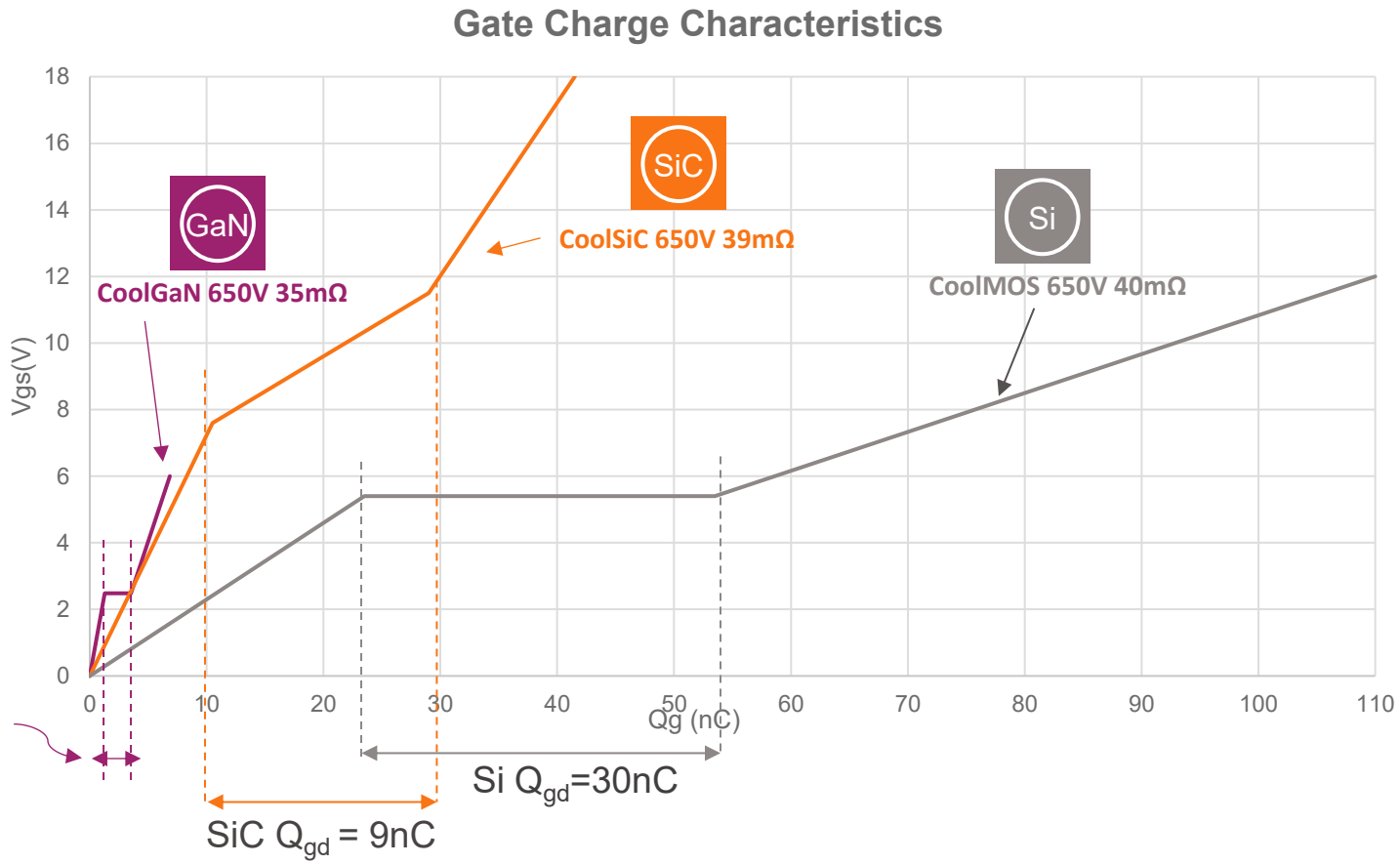
Total Gate Charge of Power Devices

Q_{gd}: Gate-to-drain charge

Lowest!
GaN Q_{gd}=2.3nC



- **CoolGaN: Lowest Qg → Less gate driving loss**
- **CoolGaN: Lowest Qgd → Fast switching, less switching loss**

→ Suitable for high frequency applications

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High-voltage CoolGaN™ Transistor portfolio

Broad portfolio enables optimized product selection

CoolGaN™ Transistor G5										
$R_{DS(on, typ)}$ [mΩ]	650 V								700 V	
	ThinPAK 5x6	DFN 8x8	DSO TSC	ThinPAK 8x8	TOLL	TOLT	QFN 6x8 HB w/o driver	8x8 DSC	DPAK	ThinPAK 5x6
										
500									IGD70R500D2S	
270	IGLR65R270D2								IGD70R270D2S	IGLR70R270D2S
200	IGLR65R200D2								IGD70R200D2S	IGLR70R200D2S
140	IGLR65R140D2	IGLD65R140D2		IGL65R140D2	IGT65R140D2		IGI65D1414A3MS		IGD70R140D2S	IGLR70R140D2S
100/110		IGLD65R110D2		IGL65R110D2		IGLT65R110D2		IGLC65R100D2		
80		IGLD65R080D2		IGL65R080D2						
50/55		IGLD65R055D2	IGOT65R055D2	IGL65R055D2	IGT65R055D2	IGLT65R055D2		IGLC65R050D2		
45			IGOT65R045D2		IGT65R045D2	IGLT65R045D2				
30/35			IGOT65R035D2		IGT65R035D2	IGLT65R035D2		IGLC65R030D2		
20/25			IGOT65R025D2		IGT65R025D2	IGLT65R025D2		IGLC65R020D2		
ES timeline	Released				Released	Released	Released	Q2 CY26	Released	
QS timeline								Q3 CY26		
SOP								Q4 CY26		

*timeline is subject to change

Released | Coming soon

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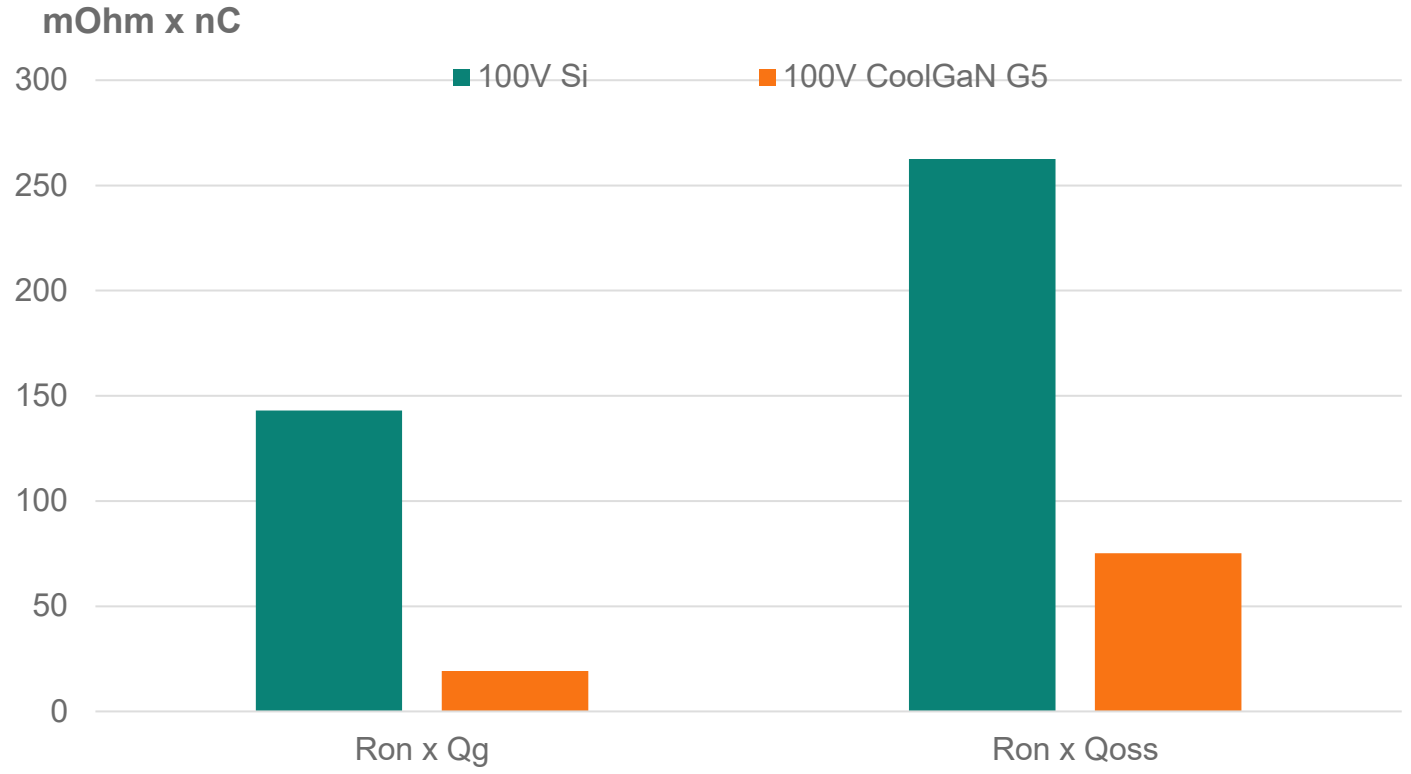
MV CoolGaN™ G5 : FOM Comparison vs. Si



CoolGaN™ G5 Ron x Qg

- Enables **reduced driving losses** especially at light-load conditions
- Allows system to reach **higher efficiency at increased frequency**
- Supports size reduction → **higher power density**

CoolGaN™ G5 with BiC Qoss

- Enables better hard switching performance leading to **higher efficiency combined with high frequencies / power density**

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MV CoolGaN™ G5 w/ Integrated Schottky Diode

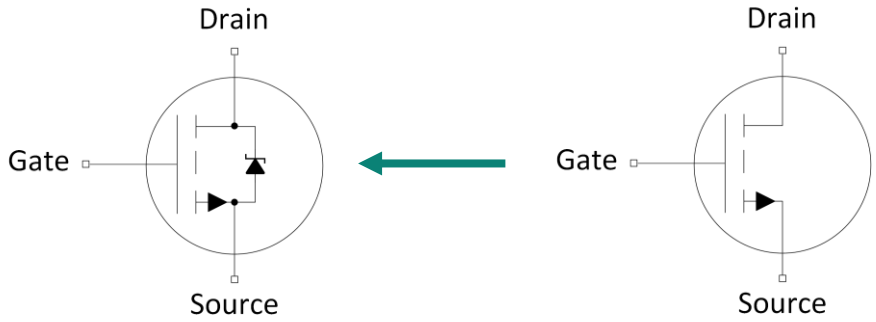
- Fully monolithic GaN Schottky diode integrated
  - **No** Silicon Schottky diode as separate chip
  - **No** reverse recovery added as there is no p-n junction
  - **No** need for external Schottky diode → cost & space savings

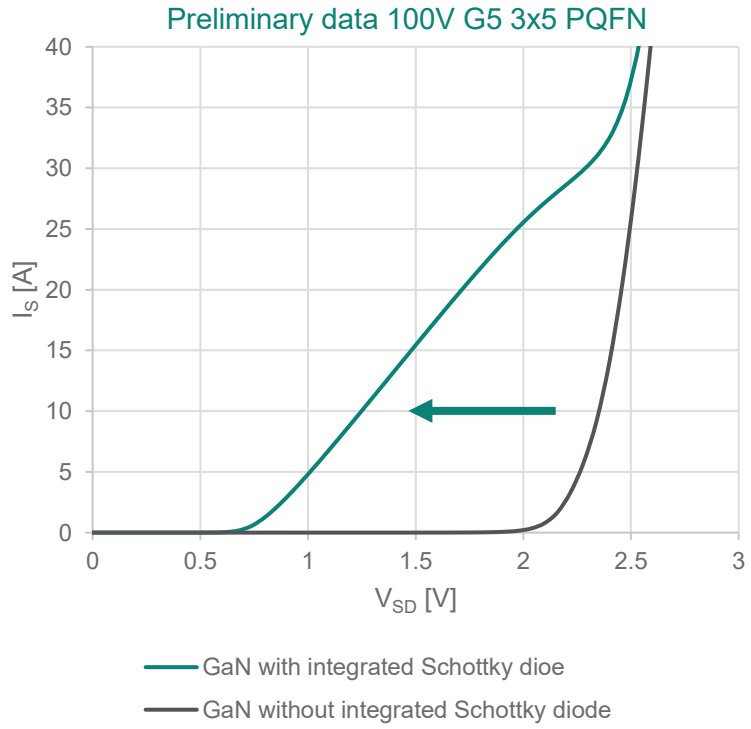
- GaN transistor with improved reverse characteristic
  - Reduction of losses during third quadrant operation

  - More relaxed dead times t_{dt} achievable without significant increase of dead time losses, e.g. motor drive application
    - if controller can not realize deadtimes in the range of 10~20 ns

  - High reduction of losses especially for applications with higher switching frequencies, e.g., non-isolated buck converter

$$P_{Loss_{dt}} = (V_{SD} \cdot I_S \cdot f_{SW}) \cdot (t_{dt,on} + t_{dt,off})$$





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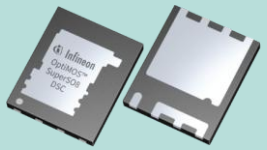
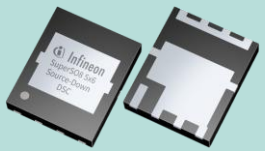
Secondary Side SR Semiconductor Options

Part number	Si ISC018N08NM6SC	Si IQD016N08NM5SC	GaN IGD01XK10S2	GaN IGD00XK08S2
Technology	OptiMOS™ 6	OptiMOS™ 5	CoolGaN™ G5	CoolGaN™ G5
Cooling	Dual side cooling (drain-down)	Dual side cooling (source-down)	Dual side cooling (drain-down)	Dual side cooling (drain-down)
Package	5x6x0.75 mm^3	5x6x0.75 mm^3	5x6x0.75 mm^3	5x6x0.75 mm^3
V_{DS}	80V	80V	100V	80V
Q_{oss} @ 40V	126nC	123nC	94nC	TBD
$R_{dson,typ}$ @ 100°C	2.33mΩ	2.20mΩ	1.87mΩ	TBD
Package	Super-SO8 DSC 	PQFN 5x6 	Super-SO8 DSC 	Super-SO8 DSC 

CoolGaN™ G5

- **Ultra low $R_{DS(on)}$**
- **Monolithically integrated Schottky Diode reduces GaN's effective V_{SD}**
- Ultra low gate charge, low output charge
- Space saving and highly robust package
- Exposed die for top-side thermal excellence

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EiceDRIVER™ Gate Driver IC

2EDR7259X



- Dual-channel reinforced isolated gate driver IC
- DSO package with 8mm input-to-output creepage
- Channel-to-channel isolation
- 5A/9A source/sink current capability
- High CMTI >150V/ns
- 38ns fast input-to-output propagation
- UVLO for both input and output supplies
- Optional dead-time control

2EDL5014AA-U2D



- Dual independent inputs
- UVLO for both high-side and low-side
- Integrated bootstrap switch
- Maximum bootstrap voltage of 120V
- 4A/4A peak source/sink current capability
- Built-in active Miller clamp
- 20ns typical propagation delay
- Offered in TSNP-12 2x2 mm package

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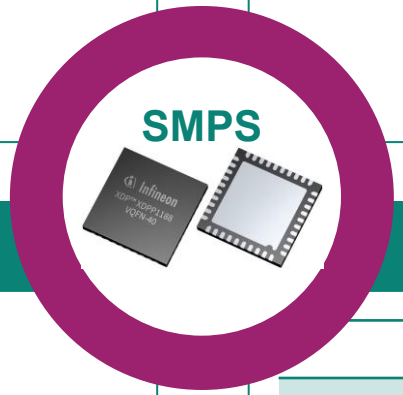
XDP™ Digital Controllers XDPP1188

Key features

- 100 MHz, 32 bit ARM® Cortex®-M0 processor
- 80 kB ROM, 32 kB RAM, 64 kB OTP memory
- High-performance current & voltage ADCs
- Up to 8 high-resolution PWM outputs
- Supports PWM and PFM control loop
- Pre-programmed hardware peripherals with digital control loop
- VQFN-40 5 x 5 mm with 0.4 mm pitch

Topologies

- Full-bridge
- Half-bridge
- Active clamp forward
- LLC
- Non-isolated Buck, Boost
- Inverting Buck-boost
- Interleaved DC-DC



Typical Application

- AI server & data center intermediate bus converters (IBC)
- Telecommunication infrastructure
- Power modules bricks
- DC-DC SMPS
- HV DC

Products

P/N	Package
XDPP1100-Q024	4x4 mm 24-pin
XDPP1100-Q040	6x6 mm 40-pin
XDPP1140-100B/C	4x4 mm 24-pin
XDPP1148-100B/C	4x4 mm 24-pin
XDPP1188-200C	5x5 mm 40-pin

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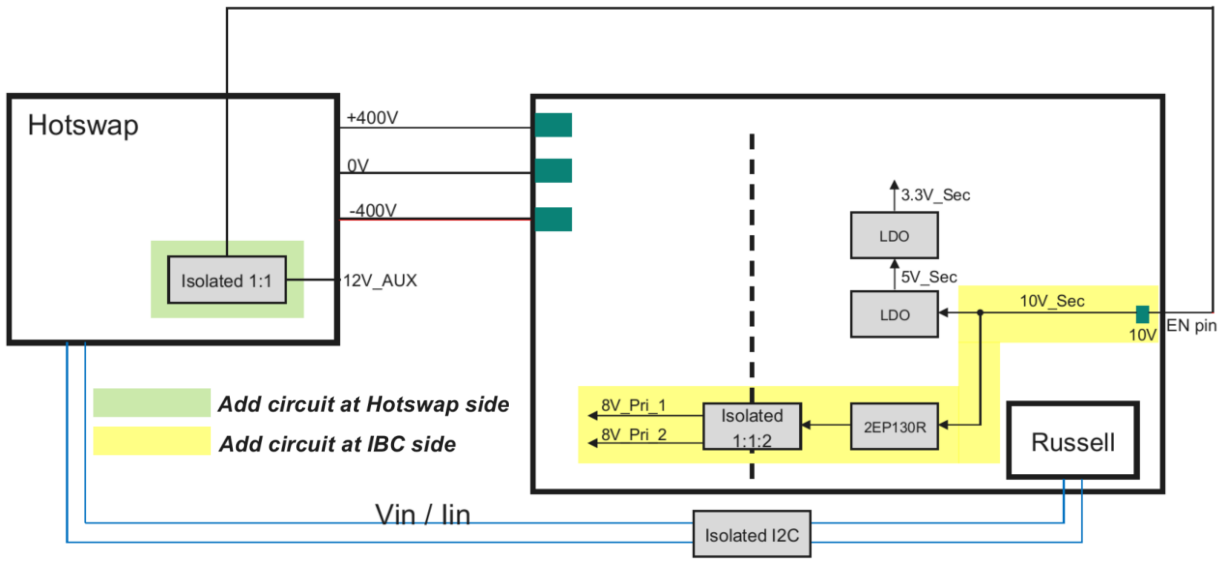
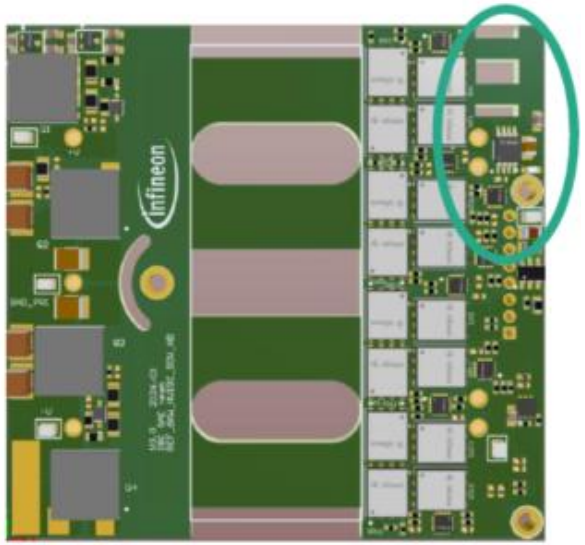
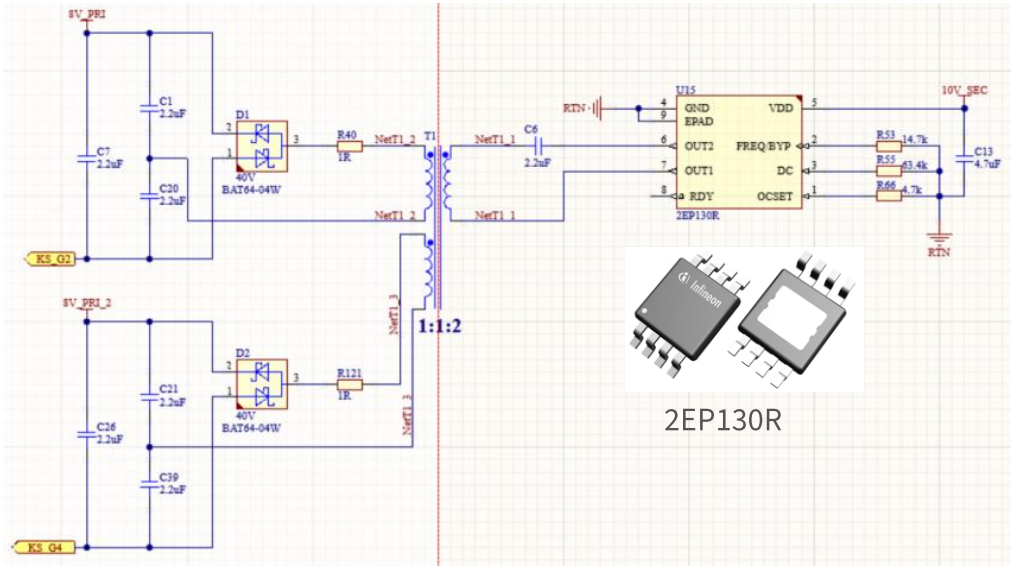
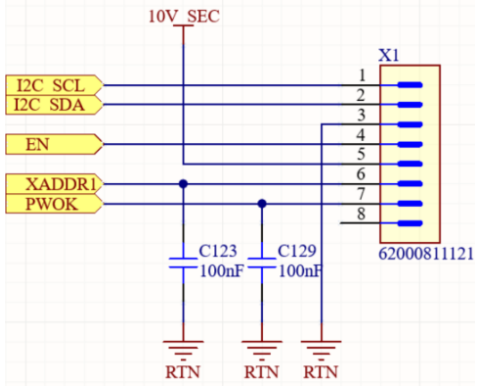
6kW HV-IBC AUX Power Solution









2EP130R Benefits

- Integration of switch output bridge
- Reduction in circuit complexity
- Small footprint for optimized PCB
- Isolated gate driver power supply



3.5W only for each module
Footprint: 10*2mm

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6kW HV-IBC Voltage Balance and Interleave

800V Input for Phase 1# and 2#



- Vin 800V
- Vout 50V@120A load
- Fsw 800kHz
- 90° phase shift between two phases of DCX
- Input voltage for each phase is very balance

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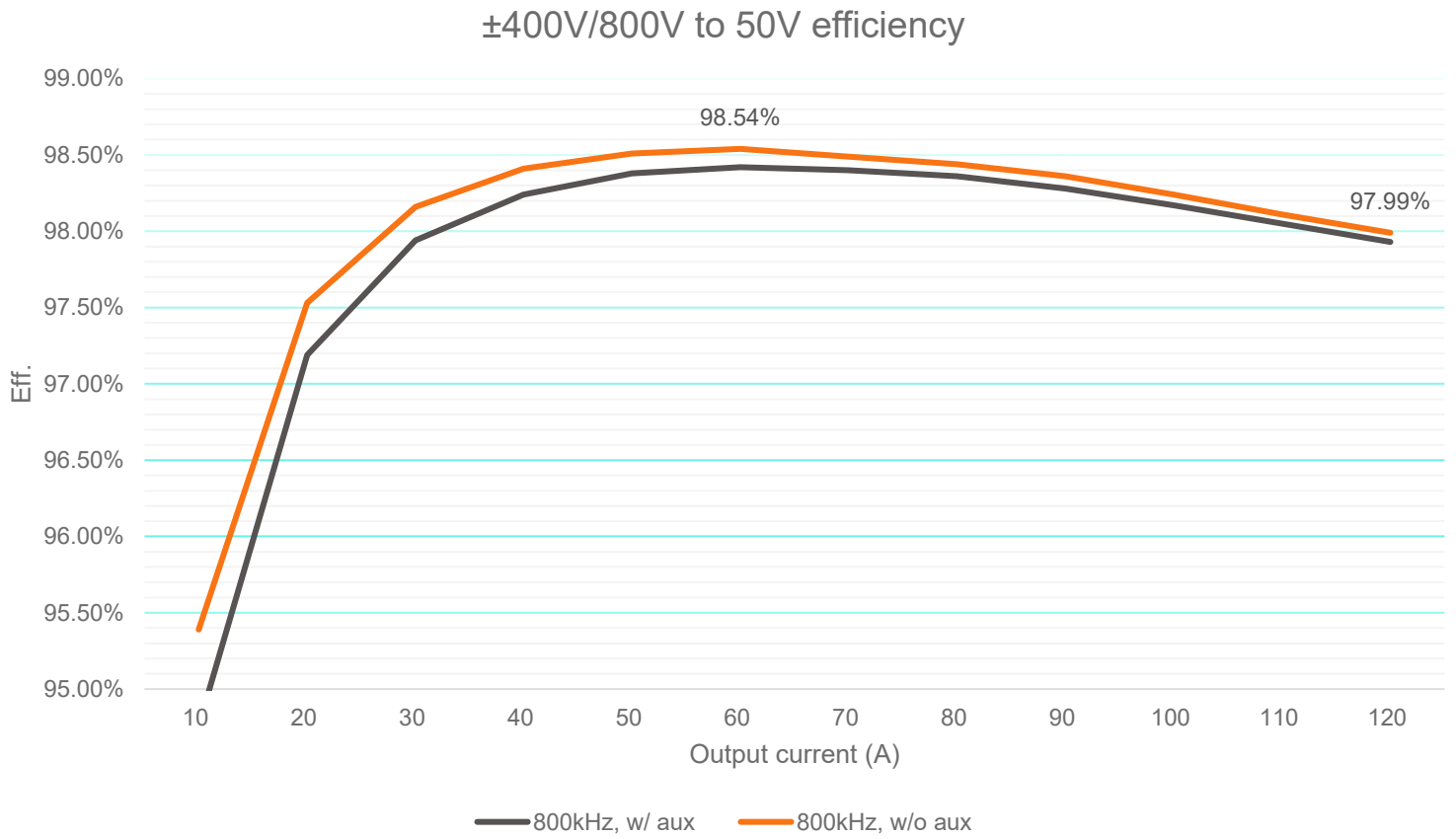
6kW HV-IBC Module Efficiency



Module Efficiency Measurement Results

- Up to 98.5 % peak efficiency, which represents a state-of-the-art performance level
- ~98% efficiency at full load

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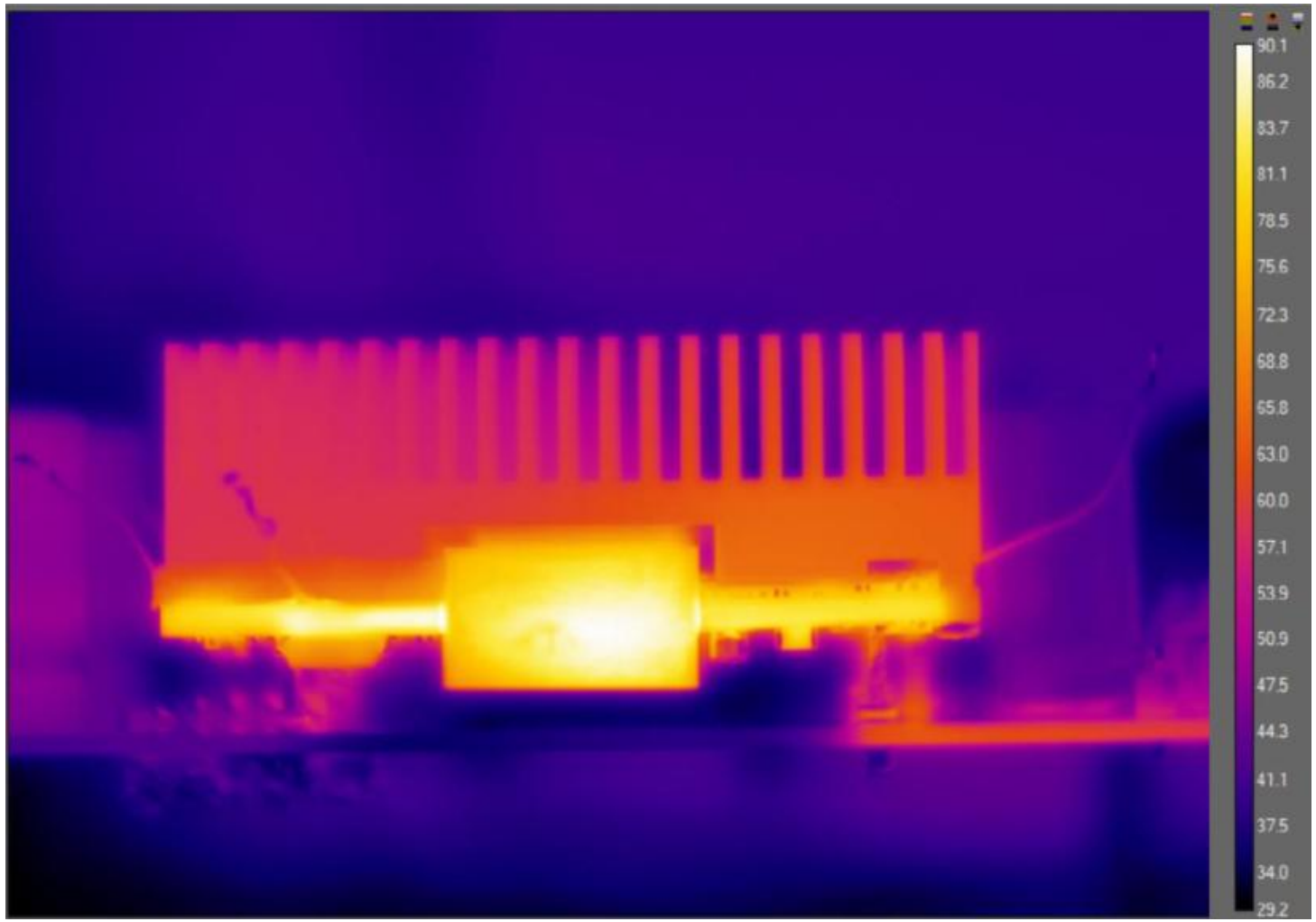
6kW HV-IBC Thermal Performance



- Vin 800V
- Vout 50V@120A load
- Fsw 800kHz
- Run 30mins
- Room temperature
- FAN: 9HV3612P3K012, 25.4CFM

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Summary

- We have demonstrated a 6kW, 800V-to-50V HV-IBC at extreme power density levels of >2000 W/in³
- We have experimentally proven full load efficiency of 98% and peak efficiency of 98.5%
- With switching frequency around 800 kHz, the HV-IBC is a key application for GaN both on primary side and secondary side

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