

CoolSiC™ G2 400 V / 440 V MOSFETs

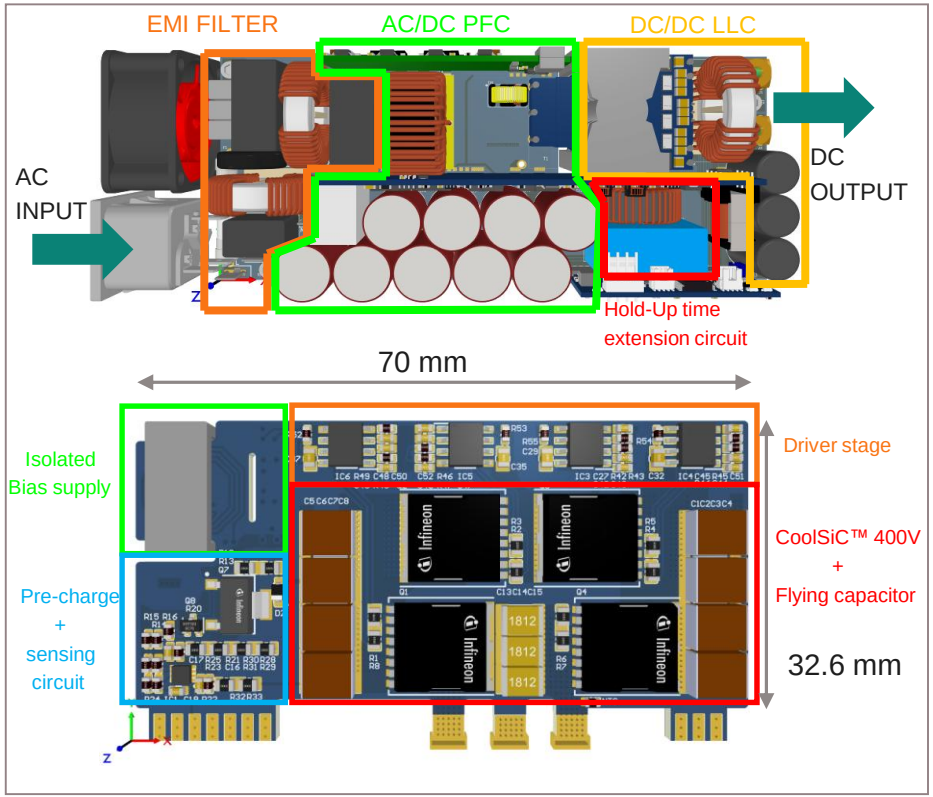
Powering AI with 3-level flying capacitor CCM totem pole PFCs

September 2025

public

Reference Board
3.3kW PSU with 3-Level Flying Capacitor CCM Totem Pole PFC

REF_3K3W_3LFC_PSU



Technical details	
Target applications	Server/Datacenter, Telecom
Input voltage range	180V – 265V
Output voltage range	51 – 49V
Output current nominal	@51V=65A, @50V=66A @48V=69A
Output power max	3300W
Peak efficiency (PFC[1] / PSU[2])	99.15% / 97.52% @ 230V || 99.26% / 97.64% @ 265V || 98.94% / 97.25% @ 180V
Topology	3-level flying capacitor CCM bridgeless totem pole PFC + half-bridge high-freq LLC
Additional technical parameter	1U height, >100W/in^3

Highlights and key information	
Infineon components	IMT40R025M2H, IPT60R022S7, IGT60R042D1, 1EDB9275F, 1EDB8275F, 2EDN7533B, 1EDN8511B, 1EDN8550B, ICE2QR2280G, BAT46WJ, BAT165, BSS128N, IPN60R3K4CE, TLS4120D0EPV33, TLS820D0ELV33, 4DIR1400H, XMC4200
Infineon hero part	**IMT40R025M2H – CoolSiC™ G2 400V**
Timeline for availability (Quarter [year])	Hardware: Q4 CY24 Documentation: Q4 CY24 Available for market (ISaR): Available now!

Features & Benefits

- High-efficiency PSU (97.52%[2] peak) @ >100W/in^3 in 1U form factor
- **Benchmark** to REF_3K3W_HFHD_PSU: efficiency, EMI, PFC choke reduction.
- **Startup, FC-precharging and voltage balancing, isolated gate drive**
- Full digital control (PFC and DCDC) supporting **dynamic tests**, **hold-up time extension** using baby-boost (line-cycle drop-out).
- Full Infineon semiconductor solution: CoolMOS™, CoolSiC™, CoolGaN™
- Improved ease of measurements

1) PFC efficiency including all aux- supply power (except fan) and EMI filter losses.
2) Full-PSU efficiency including fan power consumption.

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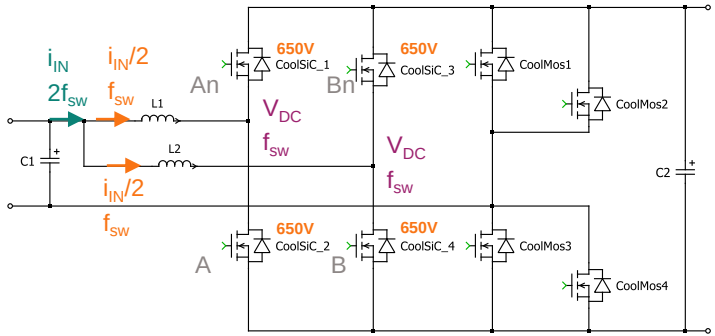
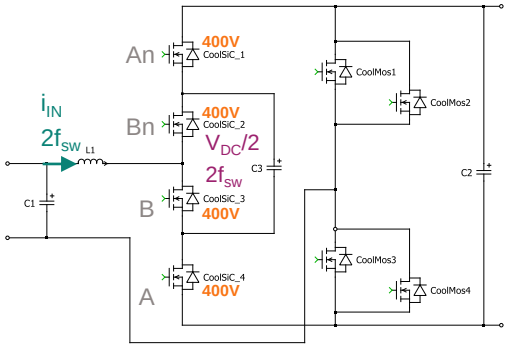
Key target application: AI Servers/Datacenter and Telecom Rectifiers

Covering OCP ORV3 HPRx, MCRPS compliant PSUs between 3.3kW – 12kW: a case study of 3.3kW CCM PFCs

REF_3K3W_HFHD_PSU (2 x 2L PFC)



REF_3K3W_3LFC_PSU (1 x 3LFC PFC)





- **2 x 2L interleaved:**
  - 4 x **CoolSiC™ 650V** – parallel (57mΩ / R_{dson} ↑)
    - 2 x PWM – 180deg – f_{sw}
  - **2 x** PFC chokes
    - $i_{AC}/2$ - V_{DC} - f_{sw} → L
    - Total volume similar than single choke
  - Thermal management
    - **Heat spreading**
    - Inductors and Switches share input current
  - 2 x f_{sw} effective input current + Δi reduction
    - **DM EMI reduction** in respect to single choke PFC

- **1 x 3L-FC:**
  - 4 x **CoolSiC™ 400V** – series (25mΩ – 35mΩ / R_{dson} ↓)
    - 2 x PWM – 180deg – f_{sw}
  - **1 x** PFC choke
    - i_{AC} - $V_{DC}/2$ - $2{\cdot}f_{sw}$ → L/4
    - **Magnetic volume / cost reduction ~60%**
    - **Use of low ESR choke**
  - **Increased efficiency** (>0.3% expected @ 230V)
    - Use of better FOM switches
    - Heat spreading in HF leg MOSFETs
  - 2 x f_{sw} effective input current + Δi reduction
    - **Same DM EMI as interleaved PFC**

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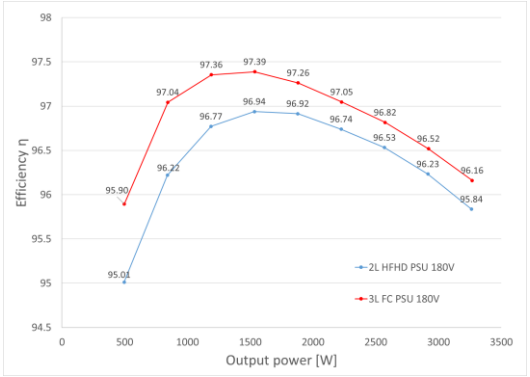
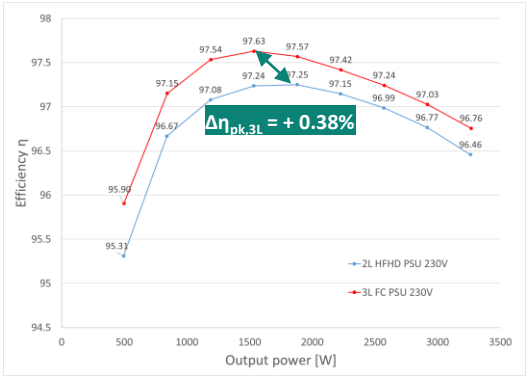
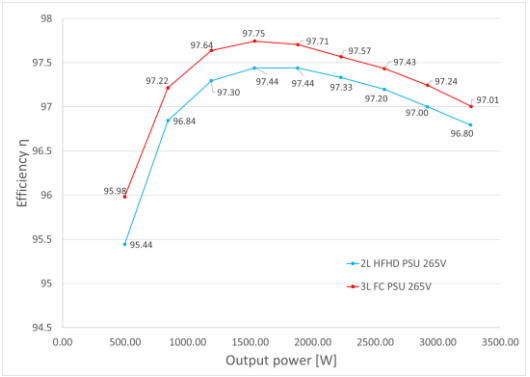
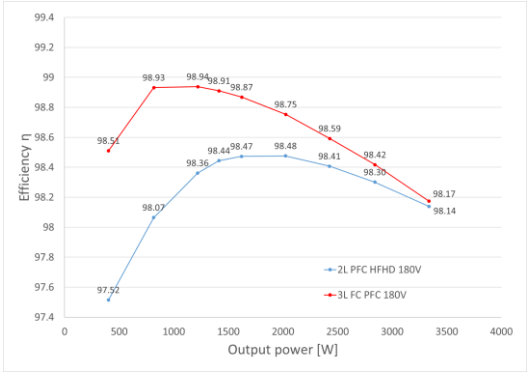
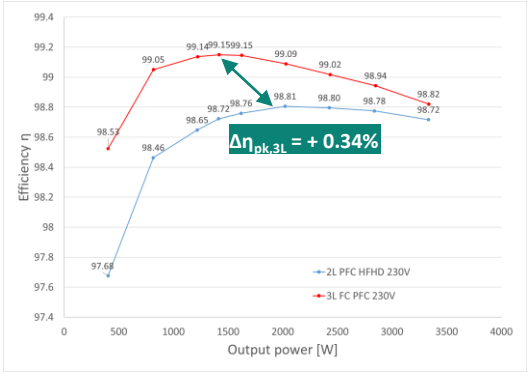
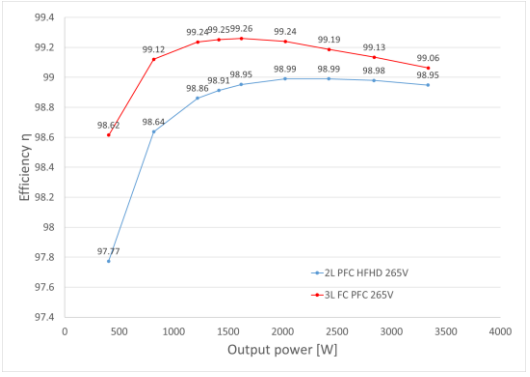
Efficiency measurements: 3L FC PSU vs 2L HFHD PSU

	V_{ac} = 180 V	V_{ac} = 230 V	V_{ac} = 265 V
Full PSU			
PFC			

Note: Ext. Fan supplied & Int. Mounted

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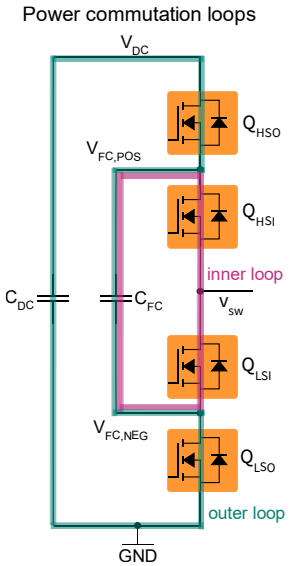
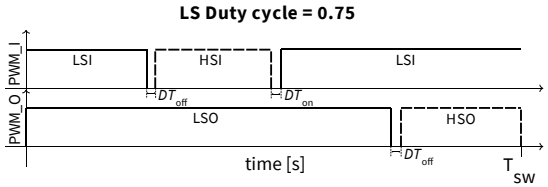
Fundamentals of the 3L-FC-CCM-TP-PFC

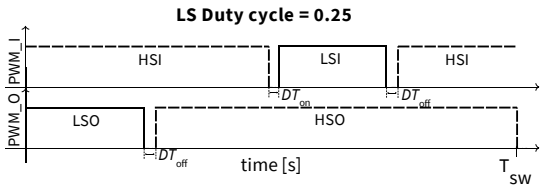
- **Topology and modes of operation**
- Start-up
- Control architecture and balancing of flying capacitor
- Gate driver supply
- Surge

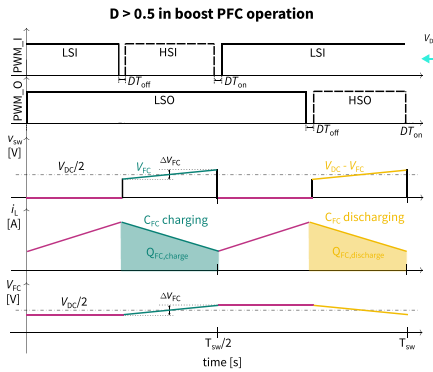
public

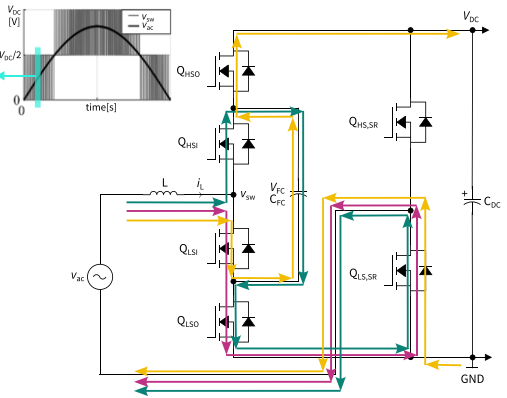
Operation of the 3-level Flying Capacitor CCM TP PFC

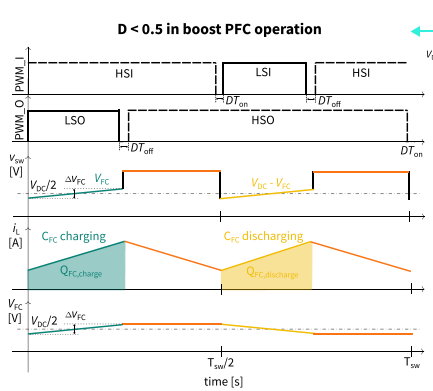


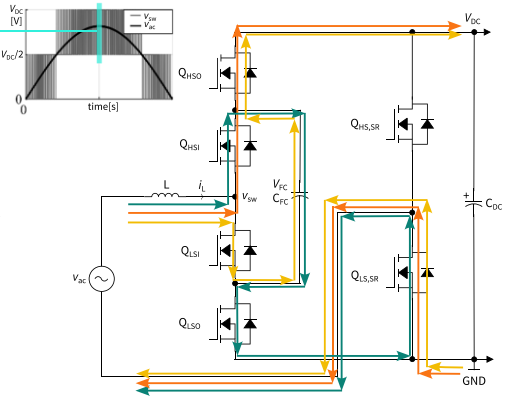












1) **Switching Freq. Multiplication → $f_{sw,eff} = N \cdot f_{sw}$**
2) **Staircased Voltage Waveform → "Multi-Level"**
3) Use of **LV Semiconductors → Better FOM**

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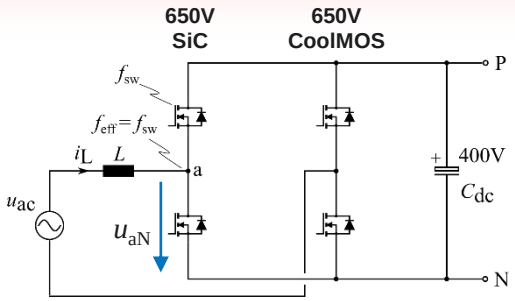
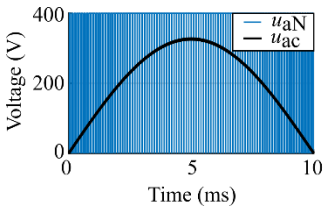
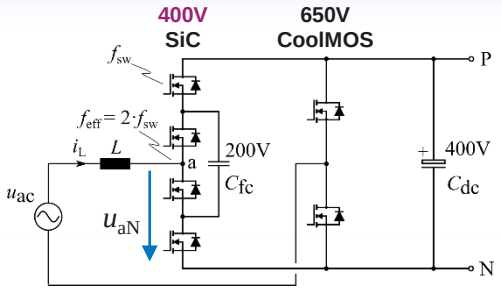
2-Level vs 3-Level Totem-Pole PFCs

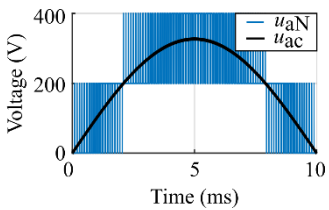
2-Level





3-Level





(N = #Levels -1)

Multi-Level

1) **Switching Freq. Multiplication** → $f_{sw,eff} = N \cdot f_{sw}$
2) **Staircased Voltage Waveform** → **"Multi-Level"**
3) Use of **LV Semiconductors** → **Better FOM**

→ **Reduce Magnetics & Filter Volume**



[Y. Lei, R.C. N. Pilawa et al.,"An Analytical Method to Evaluate and Design Hybrid Switched-Capacitor and Multilevel Converters", IEEE TPEL, 2018]
Courtesy: ETH Zurich

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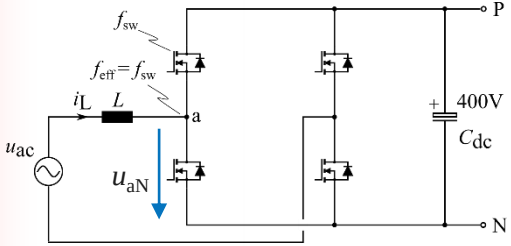
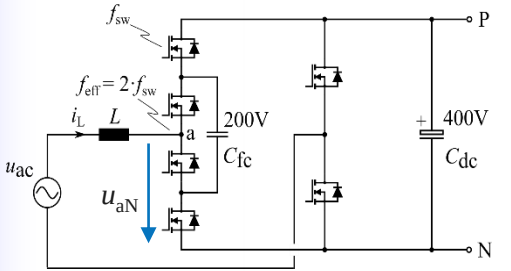
Multi-Level Advantage: Use of Better FOM Switches @ 400V DC-link

2-Level



3-Level



650 V Devices:

R_{on} , E_{sw}



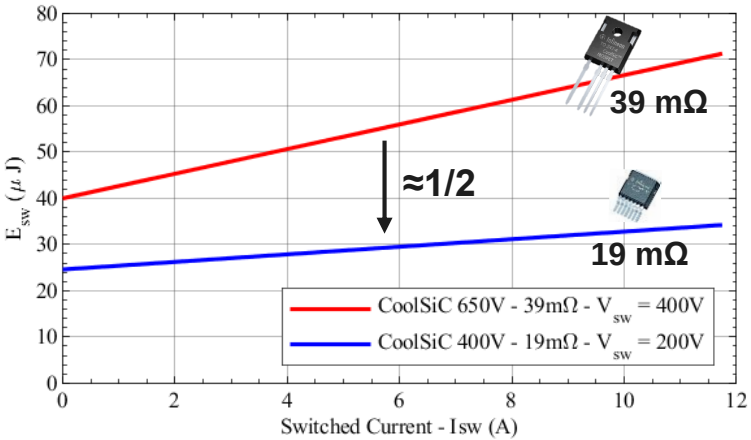
39 mΩ

400 V Devices:

$$\frac{R_{on}}{2}, \frac{E_{sw}}{2}$$



19 mΩ



Note: This is a simplified representation to show that the overlap idealized switching losses reduce by at least half in 3-level topology, but the reduction in reality is higher.

Courtesy: ETH Zurich

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Exploring Multi-Level Trade-Offs



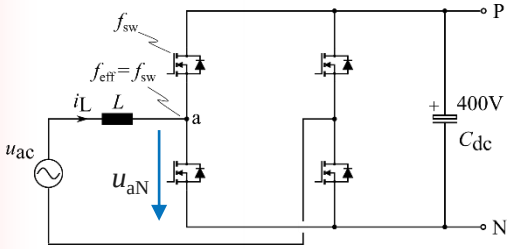
Case 1: $f_{sw}(3L) = f_{sw}(2L)$

- **Same** Semi. **Losses**
- **Much Smaller L / EMI Filter**

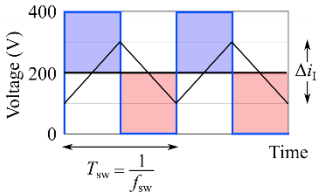
Case 2: $f_{sw}(3L) = f_{sw}(2L)/2$

- **Lower** Semi. **Losses**
- **Smaller L / EMI Filter**

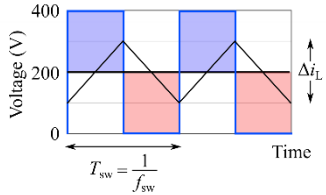
2-Level



$$P_{cond} = I_{rms}^2 R_{on}$$
$$P_{sw} = f_{sw} E_{sw}$$

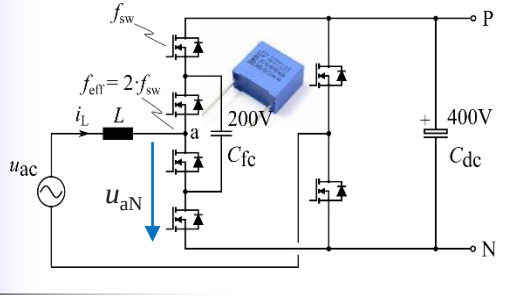




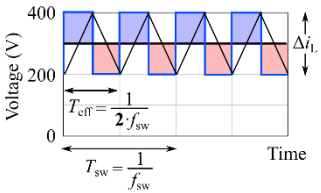




3-Level



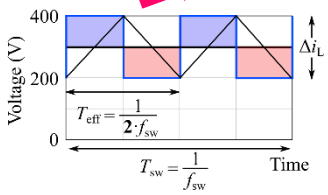
$$P_{cond} = \cancel{2} \cdot I_{rms}^2 \frac{R_{on}}{\cancel{2}}$$
$$P_{sw} = \cancel{2} \cdot f_{sw} \frac{E_{sw}}{\cancel{2}}$$



x4 Smaller



$$P_{cond} = \cancel{2} \cdot I_{rms}^2 \frac{R_{on}}{\cancel{2}}$$
$$P_{sw} = \cancel{2} \cdot \frac{f_{sw}}{2} \frac{E_{sw}}{\cancel{2}}$$



x2 Smaller + Lower Losses



Courtesy: ETH Zürich

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Dimensioning of the Flying Capacitor

- **Value of flying capacitor capacitance (C_{FC}) depends on:**
  - **Switching frequency, f_{sw}** (higher f_{sw} → lower C_{FC}). Switching period, $T_{sw} = \frac{1}{f_{sw}}$.
  - **Maximum allowed voltage ripple, ΔV_{FC}** (higher ΔV_{FC} → lower C_{FC}). Typical worst-case ΔV_{FC} can be 15 – 20% of $V_{FC,typ}$.
  - **Maximum PFC inductor/load current, $i_{L,pk}$** (higher $i_{L,pk}$ → higher C_{FC}). This occurs at low-line, for e.g., $V_{ac,min}$ = 180V.
  - $\Delta Q_{FC} = iL_{,pk} * \Delta t,$ with $\Delta t = (0.5 - |D - 0.5|) * Tsw$ and $\Delta Q_{FC} = C_{FC} * \Delta V_{FC}$
  - $\boldsymbol{C_{FC} \geq \frac{i_{L,pk}}{\Delta VFC * 2 * fsw}}$, considering a worst-case approximation.

- For high power density PSU designs requiring high reliability, **MLCC capacitors with soft-edge termination or metal-cap termination** along with good PCB design can be a good solution.

- Typical MLCCs with **X7T** or similar material have a **drop of capacitance under DC and temperature bias**. Therefore, it is recommended to consider 450V rated capacitors to mitigate the drop in capacitance with DC bias.

- In the REF_3K3W_3LFC_PSU, **6 x C5750X7T2W105K250KA (2220 450V 1uF X7T 10%)** are under evaluation to achieve an effective **C_{FC} = 3uF** under operating conditions.

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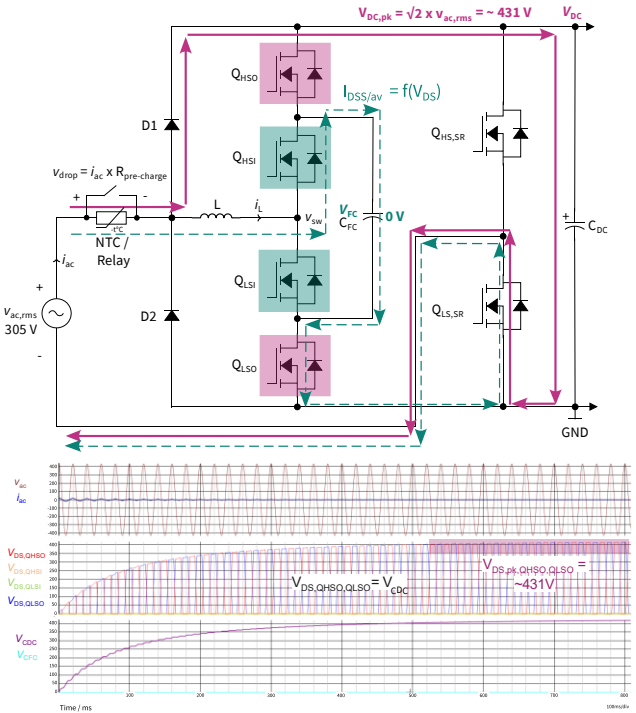
Fundamentals of the 3L-FC-CCM-TP-PFC

- Topology and modes of operation
- **Start-up**
- Control architecture and balancing of flying capacitor
- Gate driver supply
- Surge

public

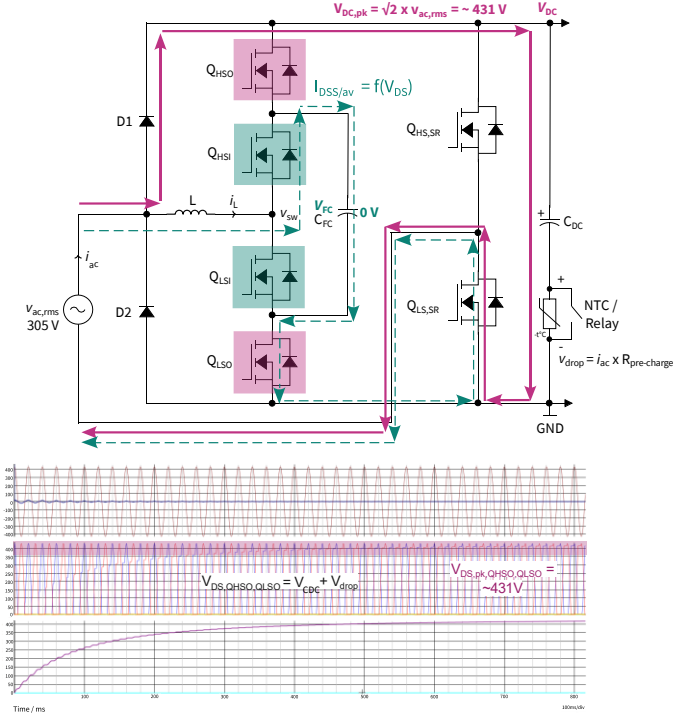
Start-up conditions under two NTC + relay configurations

Scenario 1: NTC + Relay connected in AC-side



V_{DS} overvoltages occur on Q_{HSO} and Q_{LSO} after 500ms as V_{DC} > 400V.
Hardware / firmware intervention to avoid overvoltage is POSSIBLE.

Scenario 2: NTC + Relay connected in DC-side



V_{DS} overvoltages occur on Q_{HSO} and Q_{LSO} immediately as V_{ac} is connected.
Hardware / firmware intervention to avoid overvoltage is NOT POSSIBLE (except using TVS diodes).

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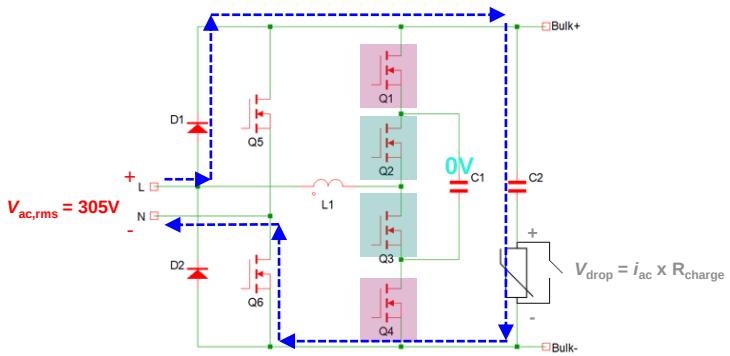
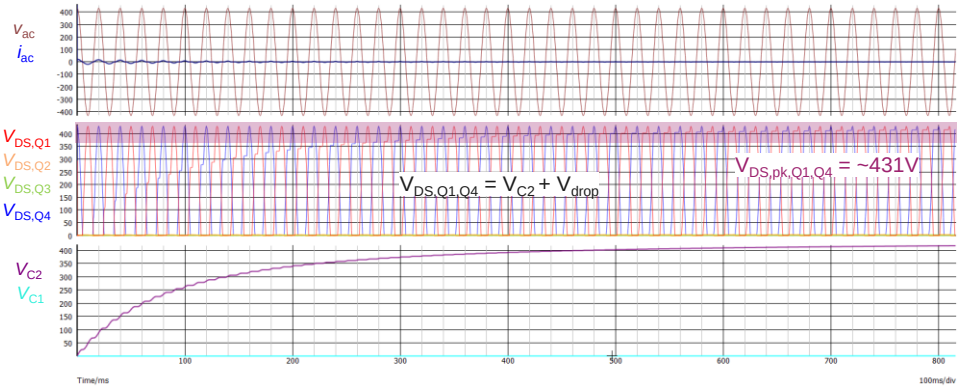
Start-up condition in 3L-FC-PFC for $V_{ac,rms}$ = 305V

NTC + Relay connected in series to DC-link with no TVS clamping diodes





- **Q2** and **Q3** don't have any overvoltage.
  - **400V SiC is enough.**
- **Q1** and **Q4** will have overvoltage for only a **few milli-seconds** during cold-start with $V_{C1(FC)}$ = 0V. **$V_{DS,pk,Q1,Q4}$ = ~431V**.
  - **Q1 and Q4 are NOT switching.** Overvoltage can be considered as a **single-event stress, with cumulative stress time << 1h** for 10k PSU start-up cycles at $V_{ac,rms}$ = 305V**.**
  - **95% derating** is needed and **not 80% derating** which applies for switching frequency (e.g. 65kHz) or similar **repetitive „operating" peak voltages**.
  - **440V SiC is needed and sufficient!**
- **With $V_{(BR)DSS}$ = 440V and $V_{(BR)DSS,tr}$ = 455V:**
  - For $V_{ac,rms}$ <= 305V, $V_{DS,pk,Q1,Q4}$ = ~431V. **95% derating** can be guaranteed.
  - **100% datasheet compliance for all conditions!**
- **With 440V SiC during operational lifetime:**
  - $V_{DS,nom}$ = 200V – 225V, **50% derating** applies!
  - FIT rate depends on $V_{DS,nom}$ and is expected to be <<< 1!

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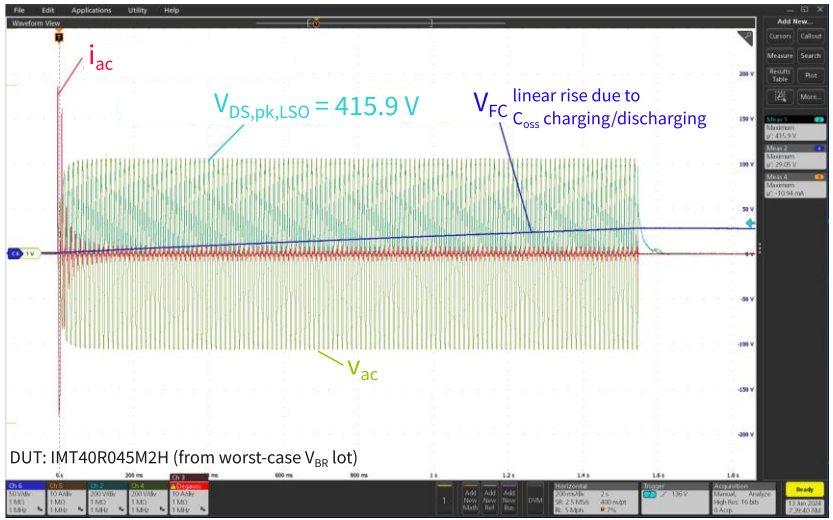
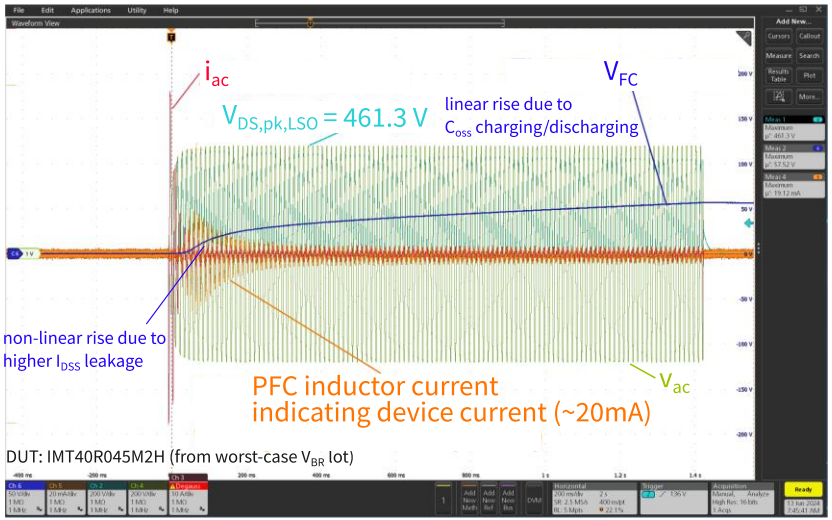
3L-FC-PFC start-up with „Worst Lot“ 400V SiC

Stress test without TVS diodes

Case 1: $V_{ac,rms}$ = 295 V



Case 2: $V_{ac,rms}$ = 325 V



- Even for worst lot and condition (no pre-charge resistor) **no avalanche can be observed**.
- FC charges slowly and smoothly via Q_{oss}.

- For excessive input voltage **some leakage** through the device can be observed.
- Charging is accelerated via addtional I_D
- **Self-limiting** as V_{FC} raises device voltage drops

Extended portfolio with higher $V_{(BR)DSS}$ = 440V conclusively avoid any overvoltage concerns!

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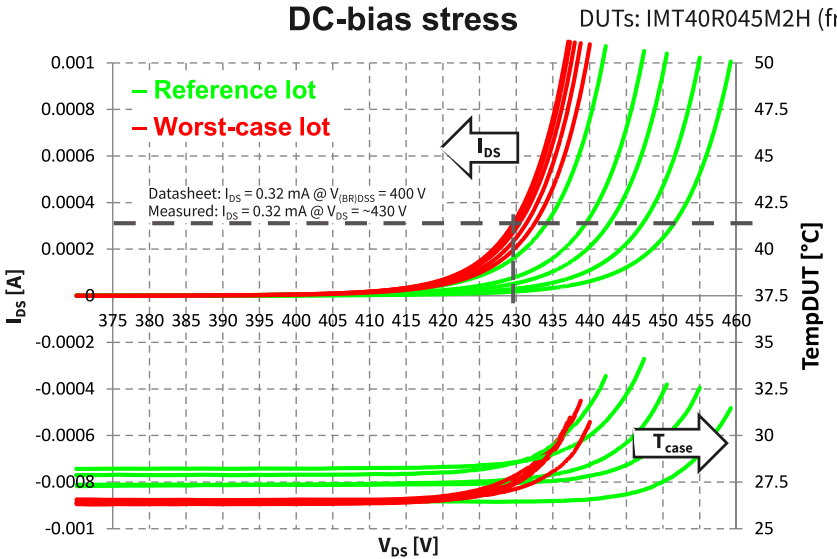
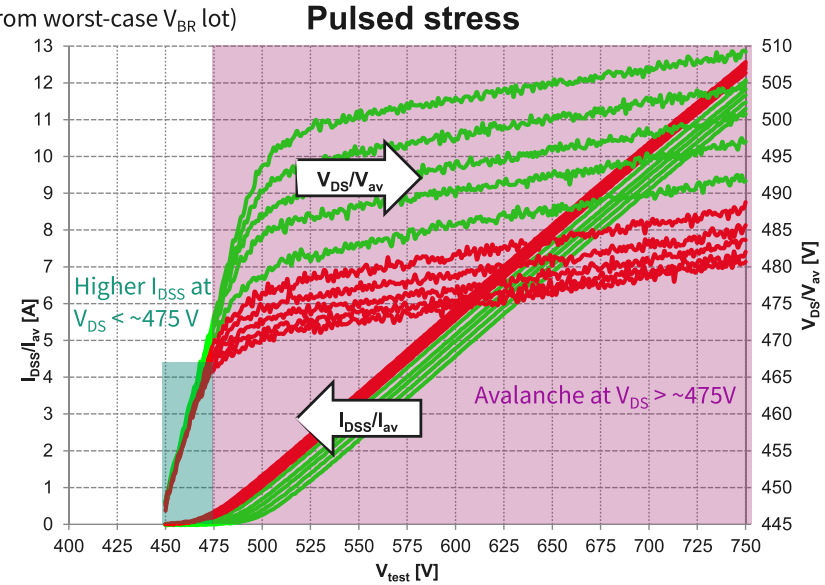
How does CoolSiC 400V behave under overvoltage stress?





Under **DC-bias (much harsher than 50Hz AC peak)**, the DUTs showed **low I_{DSS} < 0.5mA with minimal temperature rises**

- During V_{DS} overvoltage conditions, there are two modes:
  - **Higher I_{DSS} leakage currents** with resistive behaviour
  - **Avalanche breakdown with I_{av} with diode-like behaviour**

Extended portfolio with higher $V_{(BR)DSS}$ = 440V conclusively avoid any overvoltage concerns!

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CoolSiC 440V rated portfolio to enable IPC9592B derating

NTC + Relay connected in series to DC-link with no TVS clamping diodes

Device Type	Parameter	Classes I and II Stress Factors[1,2]
Power MOSFET and IGBT	Drain Current/Collector Current	≤90%/≤90% including peak current
	Drain - Source/Collector - Emitter Voltage	≤90%/≤90% including repetitive spikes for devices rated <200V; energy in single event spikes must not exceed 50% of avalanche rating.
		≤80%/≤80% including repetitive spikes for devices rated >200V; single event spike at 95% of maximum rating.
	Gate - Source Voltage	≤80%
	Maximum Junction Temperature (T_j)	≤T_j maximum - 25 °C
	dv/dt Rating	5V/nsec max. if reverse recovering the body diode. 30V/nsec - 40V/nsec in capacitive charging applications.

Table 5 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	440	-	-	V	V_{GS}=0 V, I_D=1.33 mA
Transient drain-source breakdown voltage [6]	$V_{(BR)DSS,tr}$	455	-	-	V	V_{GS}=0 V, I_D=13.3 mA, t_{pulse}≤10 ms, duty cycle≤50%

[6] Guaranteed by design, rated for transient startup overvoltages to comply with IPC-9592B derating guidelines.

- **CoolSiC 440V** portfolio with **$V_{(BR)DSS,tr}$ = 455V** is proposed to enable IPC9592B derating of 95% for single event voltage peaks to cover corner case startup at V_{ac} = 305V.
- During normal steady-state and transient conditions, **$V_{DS,nom}$ <= 225V results in 50% derating** (better than the 80% recommended in IPC9592B).
- **CoolSiC 650V** portfolio can support 80% derating even during start-up, albeit at higher total BoM cost and marginally lower performance.

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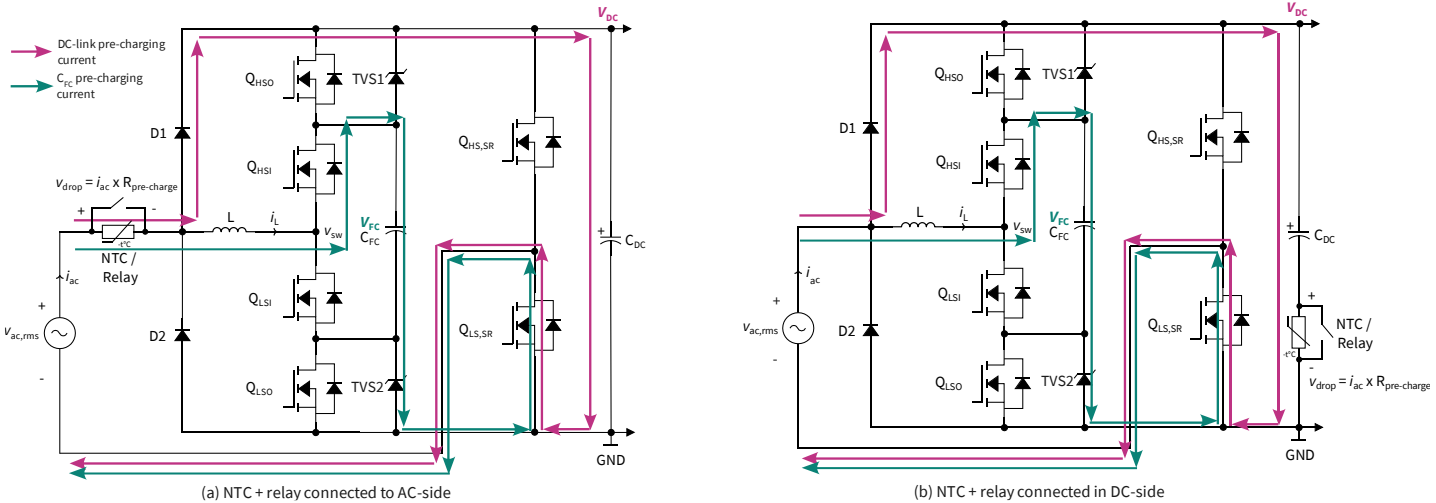
Solutions for FC pre-charging at start-up

1. Using TVS Diodes
2. Using firmware methods
3. Using an active charging current source
4. Start-up without doing “anything” with 440V SiC MOSFETs

1. Passive clamping and flying capacitor pre-charging using TVS diodes



- The additional parasitic capacitance of TVS diodes, C_j, gets added to C_{oss} of the MOSFET causing slower slew rates and add to the E_{oss} losses during hard-turn-on.
- However, **the magnitudes of C_j at V = 0V and 200V/300V are significantly lower than the C_{oss} of the MOSFET**.
  - The additional C_j is expected to have only a **MINIMAL impact**, thanks also to low switching losses in the 3L-FC-PFC.

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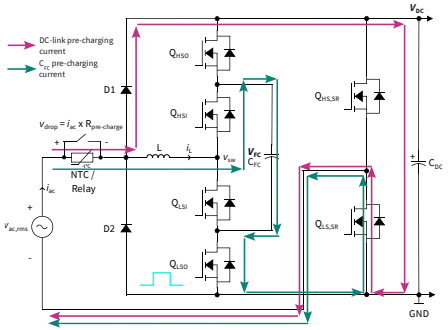
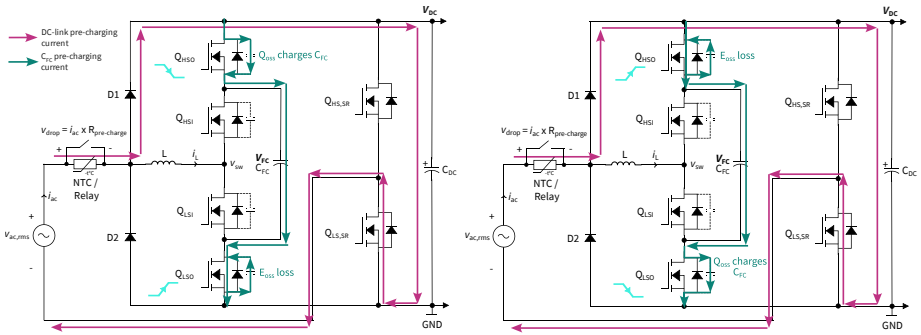
2. Using firmware methods

- Charging the FC in parallel with the DC-link capacitor



- Complementary HF switching of outer leg MOSFETs to pre-charge the flying capacitor using Q_{oss} injection



Pre-charging time depends on: (1) C_{FC}, (2) $f_{sw,pre-charge}$, (3) Q_{oss} (MOSFET dependent)
If gate control of outer MOSFETs are available, firmware implementation of pre-charging is possible by just switching outer leg MOSFETs!

Example: With IMT40R015M2H, C_{FC} = 8uF, $f_{sw,pre-charge}$ = 200kHz, ~50ms are needed to pre-charge the CFC from 0V – 200V.

- Note: any firmware-based method needs a fast-aux. supply and MCU initialization to control the gates of the HF leg MOSFETs.

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3.1. Controlled Current Sources to pre-charge Flying Capacitor

REF_3K3W_3LFC_PSU: No firmware intervention needed!

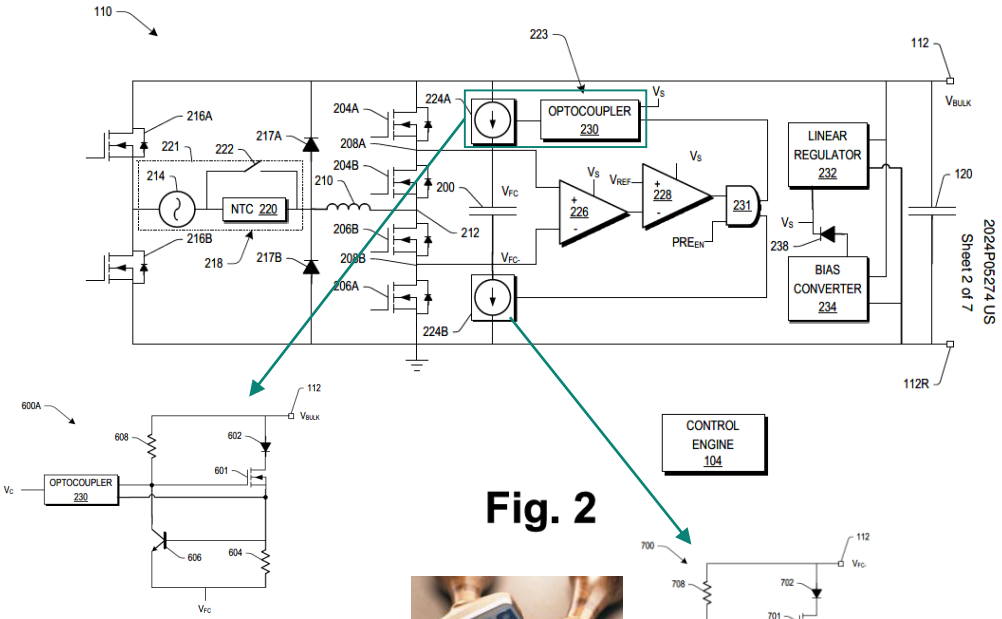

Fig. 6

Fig. 2

Fig. 7



- Filed 12.07.2024
- US 18/771097

- **AC-DC and DC-AC operation**
  - DC-AC for both grid-connected and stand-alone
- Current path enabled with rising of bulk voltage
  - Current source circuits of Fig.6 and Fig.7
  - NTC in AC path to slow down bulk voltage
  - Enable without control intervention
- **Comparator disables current path during steady-state operation**
  - No control dependency
  - Possible to have disable signal from control
- Linear regulator to supply FC sensing, comparator and optocoupler
  - before bias converter starts → **no bias dependency**
- **No control intervention during start-up**

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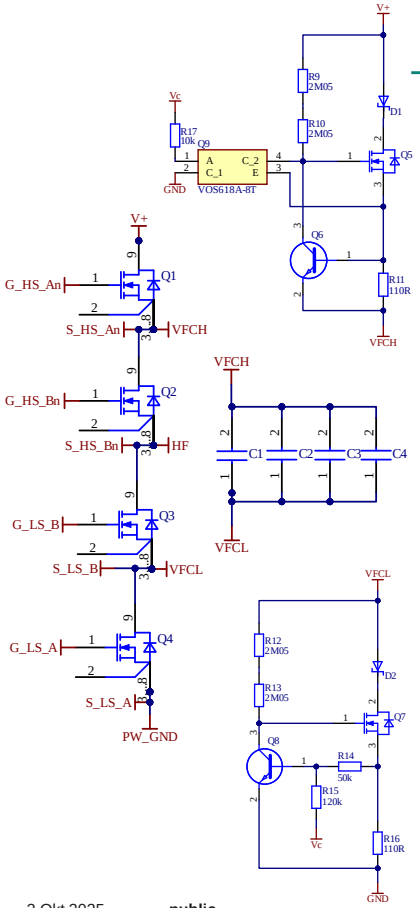
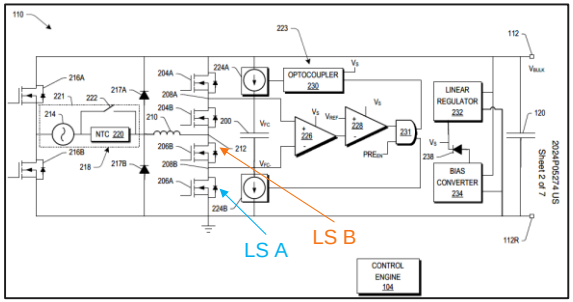
3.2. HW Implementation of active current source for pre-charging

No firmware intervention needed!

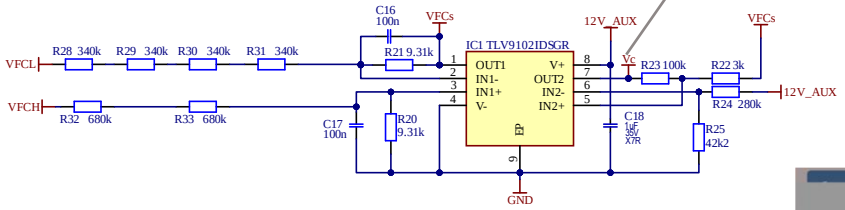


– High side current path



To ADC for FC balance

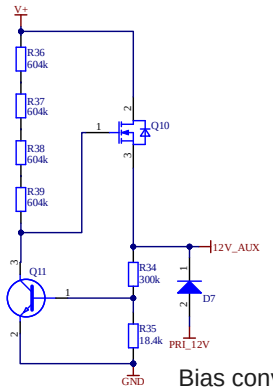
Current path disable



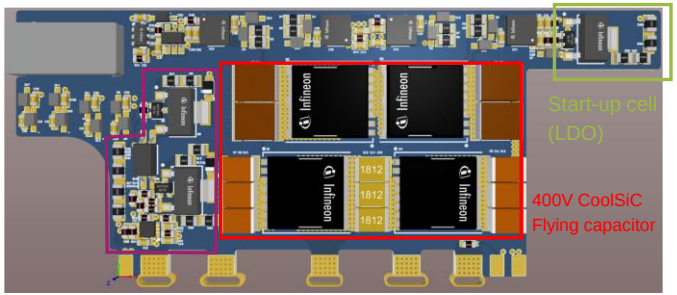
– FC sense and hysteresis comparator

– Low side current path

– Start-up cell (LDO)



Bias converter output



Current source
FC sensing
Comparator

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3.3. Simplified implementation for PFC application only

No firmware intervention needed!

- Start-up
- 7mA current source

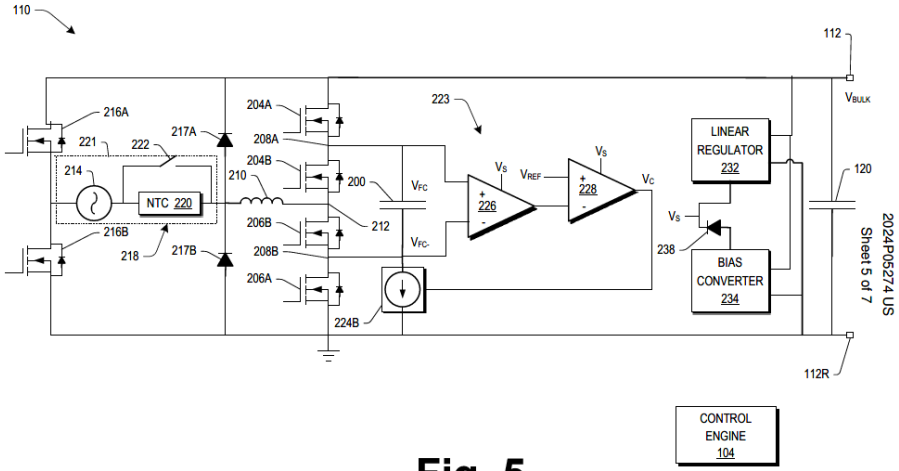
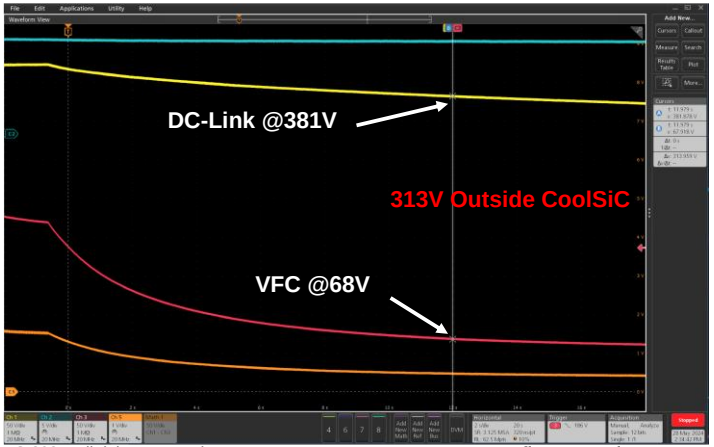


Fig. 5





- AC off

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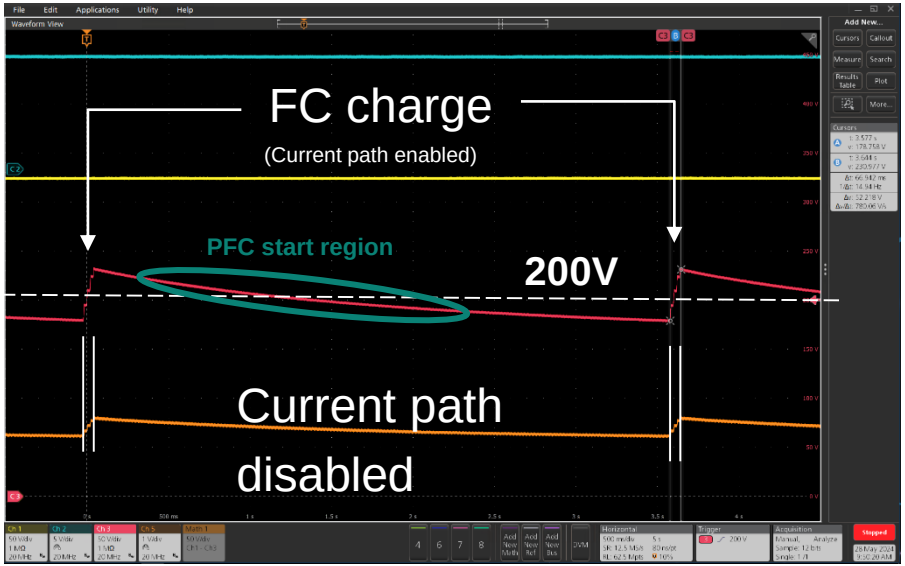
3.4. Enable/Disable charge of Flying Capacitor (230V_{rms}, PFC disabled)

No firmware intervention needed!

- → Vbulk
- → Vcc Fcsensing+opamp
- → Vfc
- → Vfc_sense



- **AC applied but PSU not enabled**
  - Bulk is charged by AC voltage
  - No FC control because PFC is not in operation
  - FC must be controlled to avoid device stress
- **Enable/Disable feature of current source with hysteresis comparator**
  - Hysteresis out of steady-state ripple of FC
- **PFC to start operation when current source is disabled**
  - Green highlighted area
  - When PFC is enabled → FC balancing

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Key considerations for selecting MOSFET voltage class

- **DC-link pre-charging NTC + relay connection**
  - Connected to AC-side: FC pre-charging is possible → evaluate **400V / 440V** MOSFETs.
  - Connected to DC-link: FC pre-charging is possible only if TVS diodes are used → evaluate **440V / 650V** MOSFETs.

- **Input AC voltage range**
  - **180V – 305Vac:**
    - FC pre-charging done → evaluate **400V / 440V** MOSFETs.
    - FC pre-charging NOT done → evaluate **440V** MOSFETs for 95% derating and **650V** MOSFETs for 80% derating at start-up.
  - **100V – 240Vac**:
    - FC pre-charging done → evaluate **400V / 440V** MOSFETs.
    - FC pre-charging NOT done → evaluate **440V** MOSFETs with close to 80% derating and **650V** MOSFETs for 80% derating at start-up.

- **Dimensioning of FC**
  - Sufficient C_{FC} → even AC self-balancing could be sufficient.
  - Limited C_{FC} → FC voltage can be hard to limit without dedicated control loop.
  - With good balancing → **400V / 440V** MOSFETs for 80% derating during operational lifetime.
  - Without good balancing → **650V** MOSFETs for 80% derating during operational lifetime.

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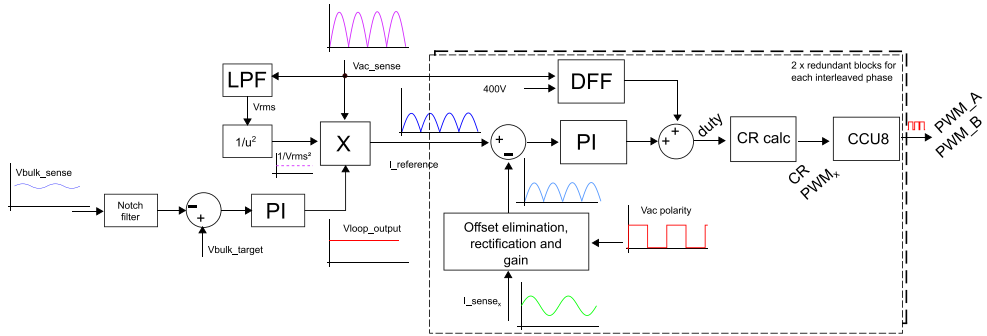
Fundamentals of the 3L-FC-CCM-TP-PFC

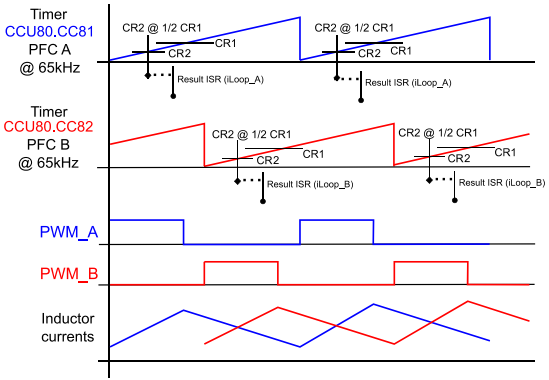
- Topology and modes of operation
- Start-up
- **Control architecture and balancing of flying capacitor**
- Gate driver supply
- Surge

public

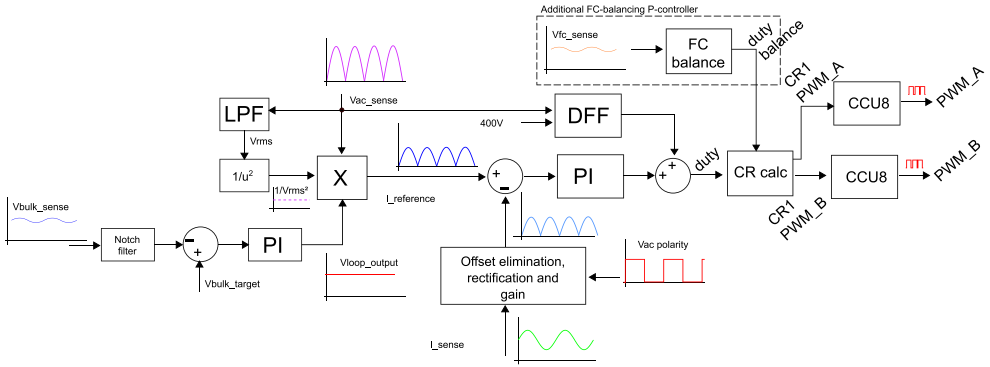
Control architecture and balancing of flying capacitor

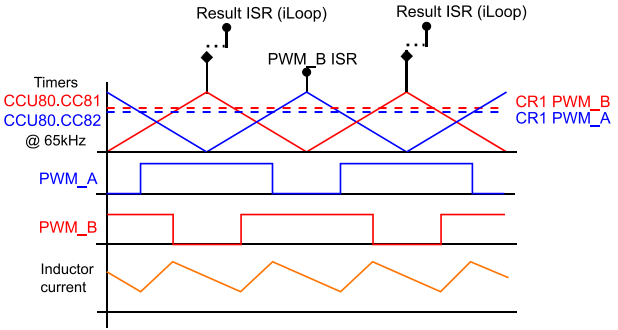
REF_3K3W_HFHD_PSU (2 x int. 2L-CCM-TP-PFC)





REF_3K3W_3LFC_PSU (1 x 3LFC-CCM-TP-PFC)





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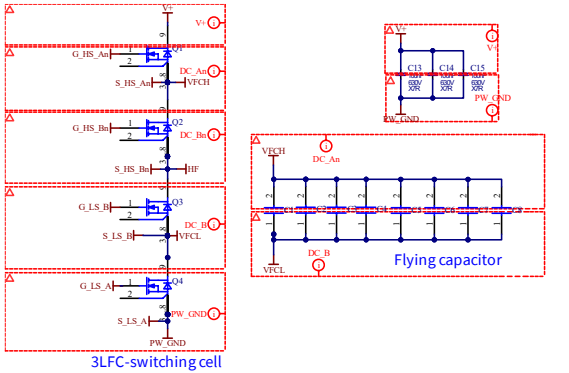
Fundamentals of the 3L-FC-CCM-TP-PFC

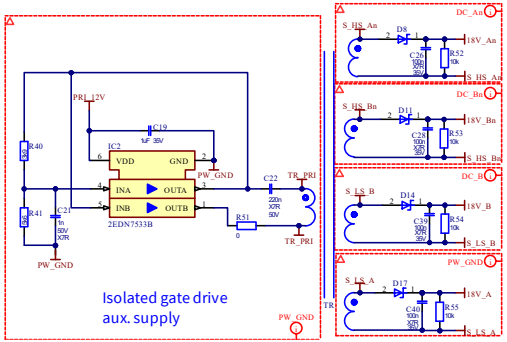
- Topology and modes of operation
- Start-up
- Control architecture and balancing of flying capacitor
- **Gate driver supply**
- Surge

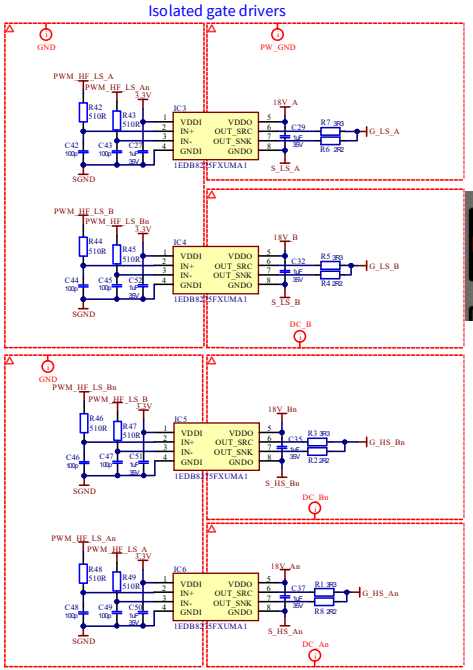
public

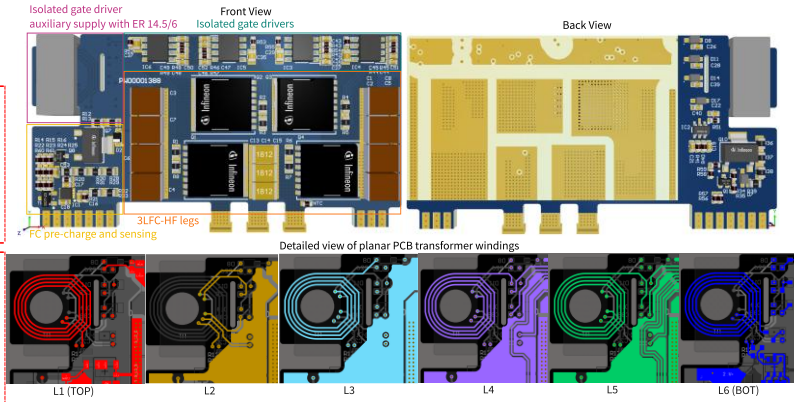
Gate driver supply using isolated aux. supply

REF_3K3W_3LFC_PSU









- Oscillator with multiwinding transformer embedded in PCB
  - Board area as design option (fit into power board)
  - **Inexpensive ferrite core (EQ14.5)**
  - **Simple unipolar gate driving**
- Balance cost – system complexity
  - **All drivers supplied** → abnormal and dynamic conditions

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Fundamentals of the 3L-FC-CCM-TP-PFC

- Topology and modes of operation
- Start-up
- Control architecture and balancing of flying capacitor
- Gate driver supply
- **Surge**

public

Surge conditions

Fundamentally, the **impact of surge on both 2L and 3L CCM TP PFC is similar**. The way to handle surge is also similar.

– **Key difference in 3LFC PFC:** the flying capacitor – how the V_{FC} is impacted during the surge event is interesting, as it impacts the voltage sharing between the inner and outer leg MOSFETs of the HF-leg.

Differential mode surge:

– Adding varistors (MOVx) [1] across the line and adding HV clamping diodes (D1/D2).

– Implementing a **fast detection of surge event and stopping PWM** – input line (V_{ac}) over-voltage protection (OVP) [1] or PFC inductor over-current protection (OCP) and stopping the HF-leg boost/PFC switching. In the HFHD and 3LFC reference designs, the following protective measures are implemented:

  – Switching cycle-by-cycle **"fast" OCP** is implemented using the internal XMC comparator that is triggered if iph,sense > 45A and disables the PWM signals.

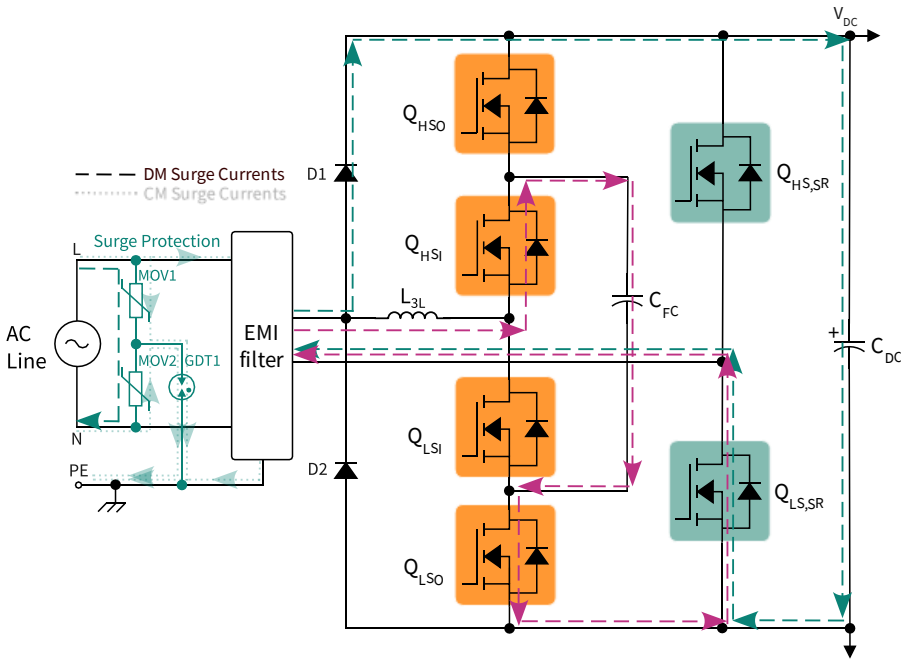
  – **OVP** is implemented for the VDC > 460V and disables the PWM signals.

  – The **diodes D1/D2** not only help during the start-up for DC-link pre-charging but also reroute a part of the surge current to the bulk-capacitors to absorb the surge energy.

Common mode surge:

– Use a combination of MOVs and gas discharge tube (GDT) [2].

Note: to do surge testing on REF_3K3W_3LFC_PSU, add MOVs and GDTs. The design has not been surge tested.



References/citation:

[1] R. Beinarys, S. O'Driscoll and T. T. Vu, "Flying Capacitor Voltage Imbalance Protection in Multilevel Bidirectional Inverters during Surge," 2023 APEC, Orlando, FL, USA, 2023, pp. 2068-2073

[2] AN_2006_PL52_2009_103328 – „Lightning surge discharge design for SMPS applications".

[3] R. Beinarys, S. O'Driscoll, " 400V SiC in Next-Generation 3-Level Flying Capacitor Bridgeless Totem-pole PFC," 2025 APEC

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Summary

3L FC PFC with CoolSiC 400V is a very attractive for high efficiency and power density

- **Switching FoMs** (FoM_{Eoss}, FoM_{Qoss}, FoM_{Qgd}) and **Conduction FoMs** ($R_{ds,on}$ vs T_j) are attractive
- 3L topology enables higher **blocking voltage** esp. in the data center at **277V and above**
- Inherent frequency multiplication and lower voltage swings → **smaller inductors and EMI filter possible**
- Distributed losses and very flat R_{DSon} vs T_j enable to **use of higher R_{DSon}** devices reducing cost further

Very high **PFC efficiency of 99.2% at 230V** have been demonstrated and following challenges have been addressed:

- Balancing the flying cap
- Start-up
- Surge
- Firmware

Now is the time to benefit from Infineon‘s new **CoolSiC 400V** MOSFETs!

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