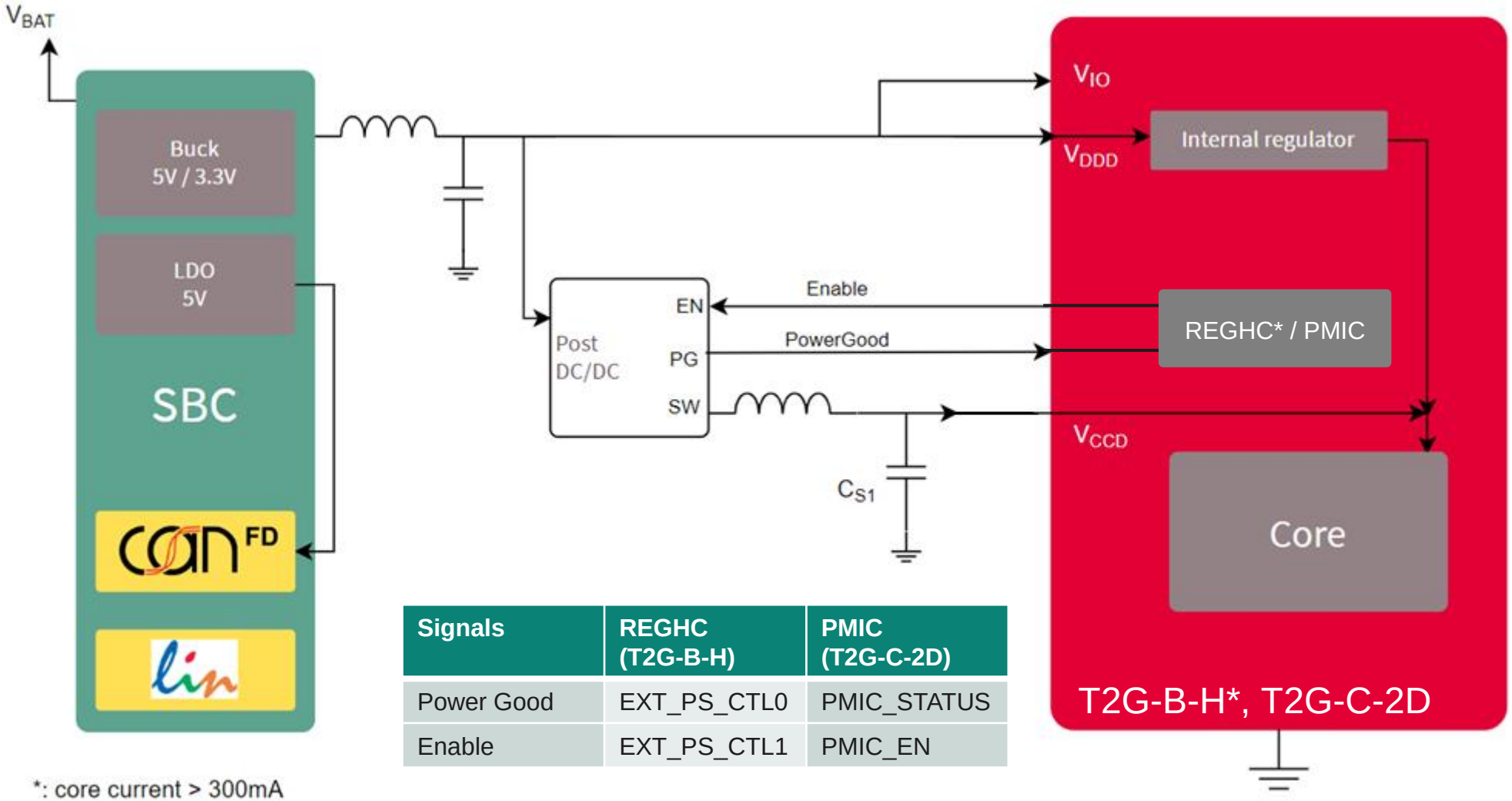
TRAVEO™ T2G
Pre-Charge Core Supply Power Concept



restricted

Standard Power Concept: Charge of Core Supply via int. Regulator

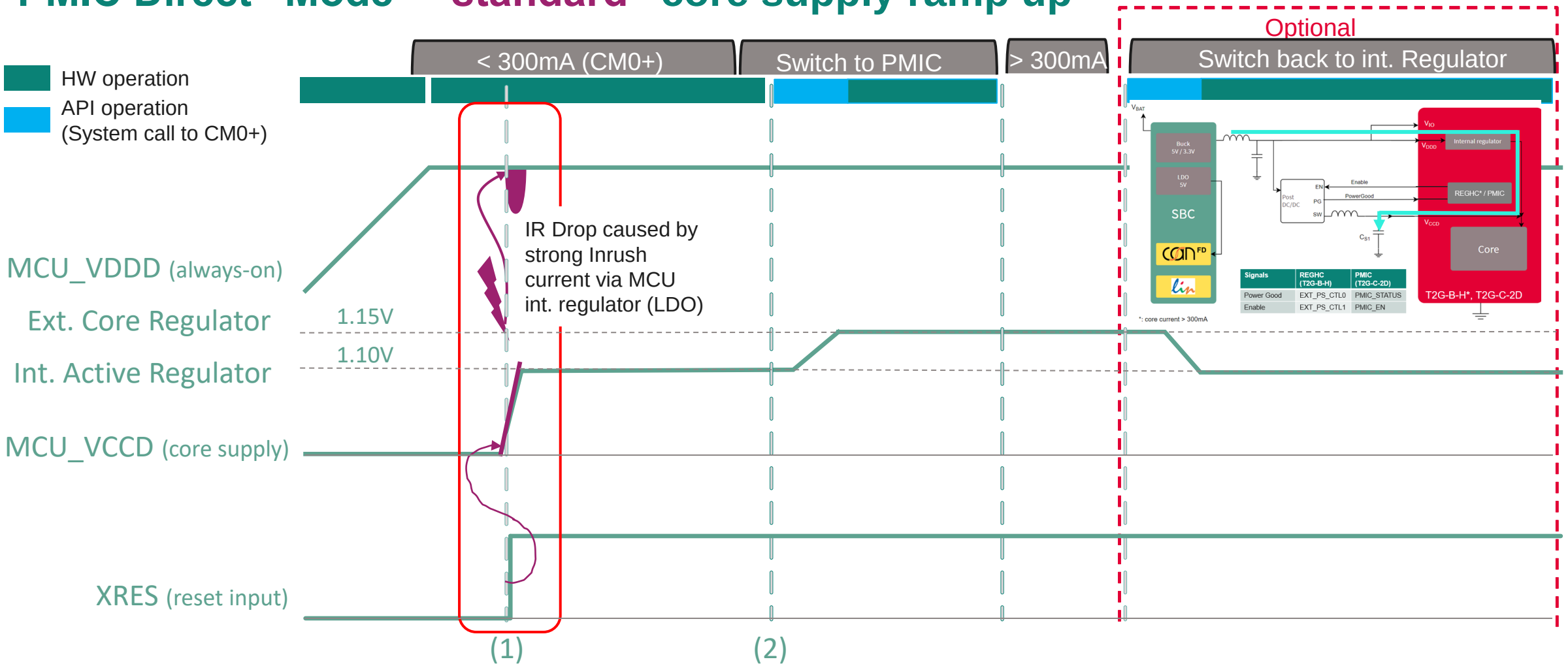
TRAVEO™ T2G: Power Concept
Supply concept example with external core supply ("PMIC direct connection")



Signals	REGHC (T2G-B-H)	PMIC (T2G-C-2D)
Power Good	EXT_PS_CTL0	PMIC_STATUS
Enable	EXT_PS_CTL1	PMIC_EN

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TRAVEO™ T2G: Power Rail Concept for ext. core supply
“PMIC Direct” Mode - “standard” core supply ramp up

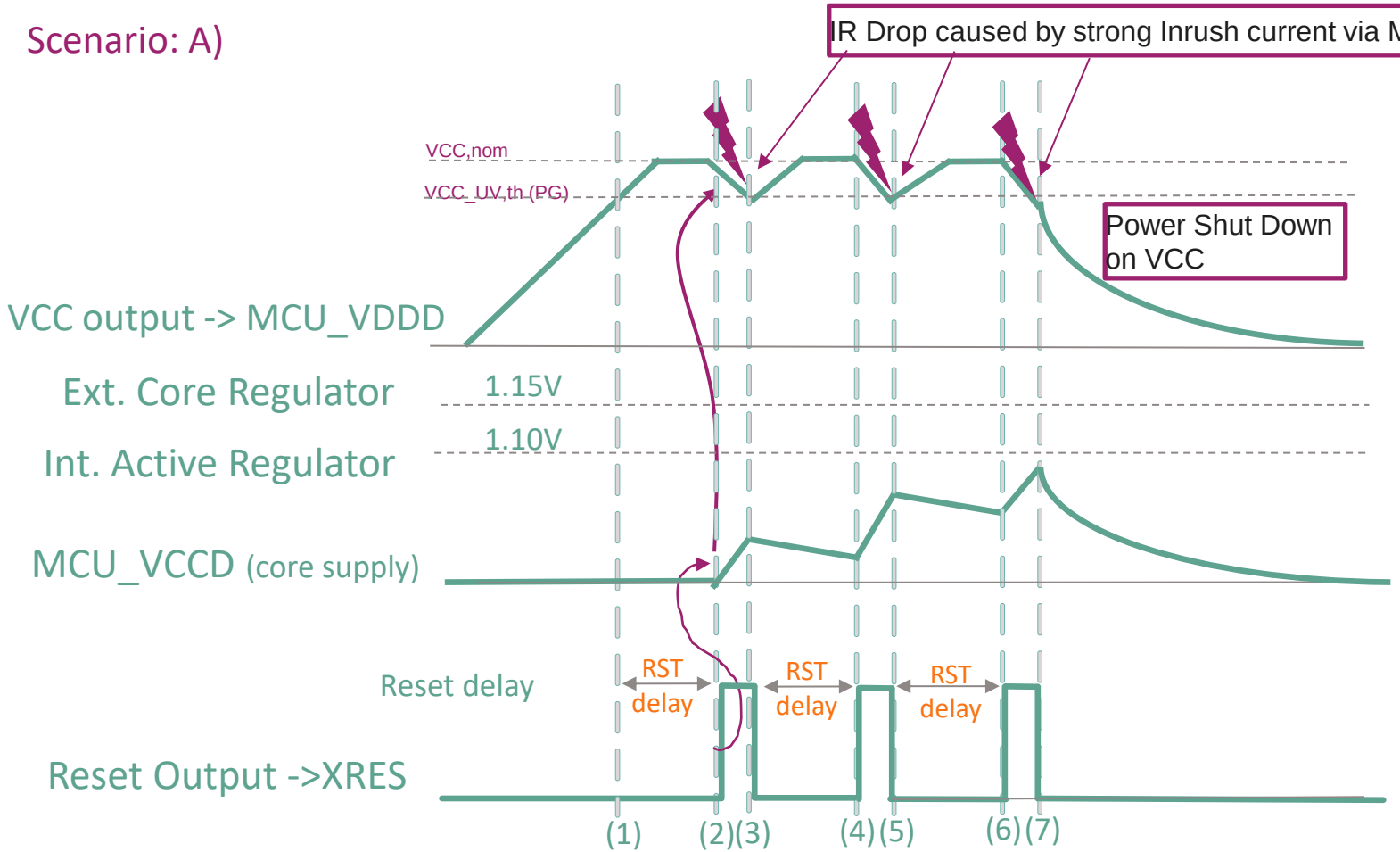


(1) Ramp up Core Supply executed via MCU always-on Domain VDDD (MCU int. LDO), triggered by XRES release
(2) Afterwards enable ext. core supply for core load > 300mA via software (use of API system calls)

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TRAVEO™ T2G: Power Rail Concept for ext. core supply
Possible Risk on System with “standard” core supply ramp up

Scenario: A)



(1) After Passing PG threshold on VCC output a reset release delay is generated.
(2) Reset Release triggers Start of Ramping up the MCU Core Supply driven via MCU always-on Domain VDDD (MCU int. LDO).
(3) MCU int. LDO drive current (inrush current) stronger than VCC output current, which leads to undervoltage at VCC.

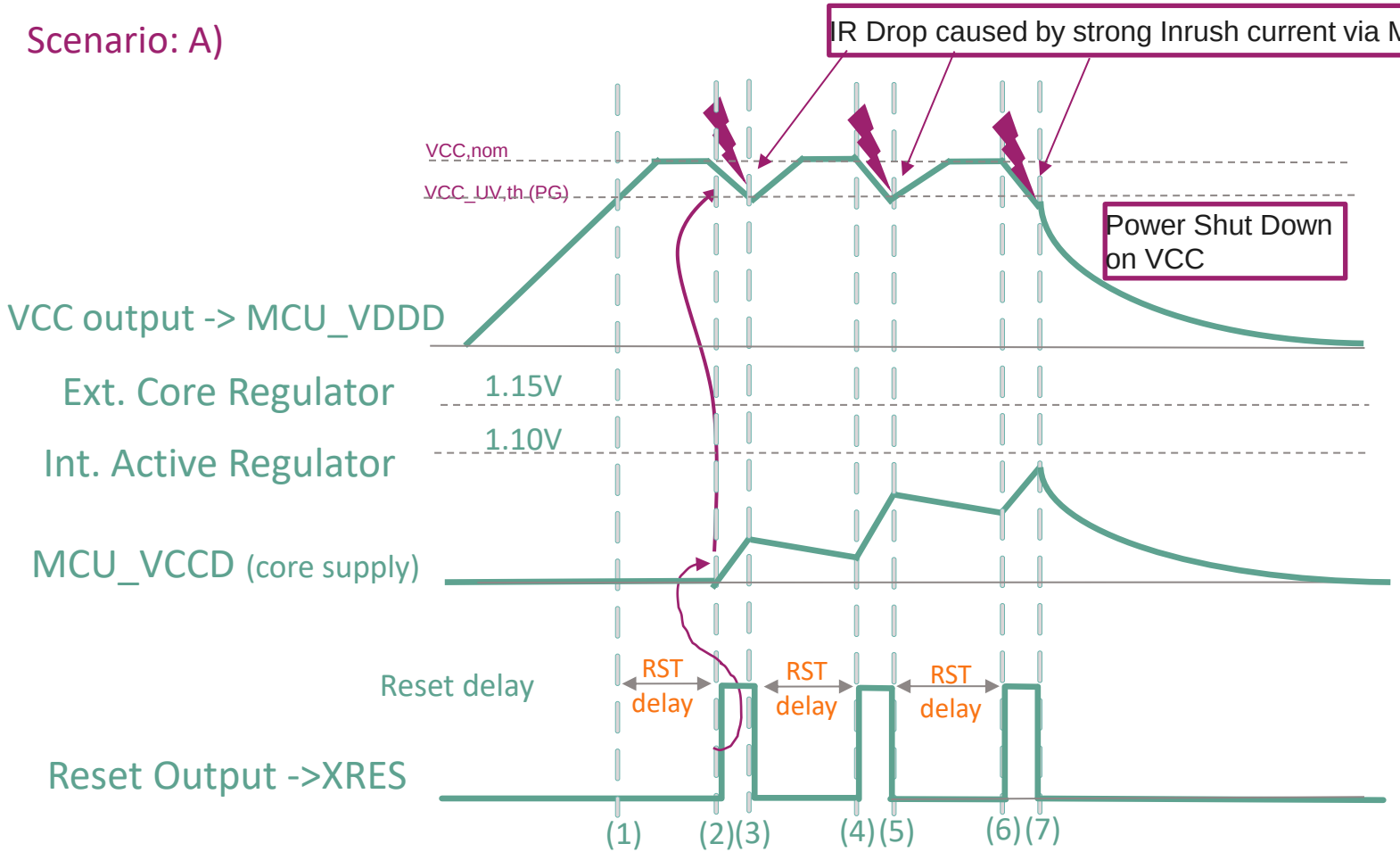
Following Scenarios possible:

A) After consecutive order of undervoltage detections VCC output is shut down (fail state) and only power-on reset re-enables the VCC.
B) Infinite number of retries to ramp-up core supply.
C) Other…

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TRAVEO™ T2G: Power Rail Concept for ext. core supply
Possible Risk on System with “standard” core supply ramp up

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C) Other…

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Requirement to ext. Core Regulator for TRAVEO™ T2G Core Supply (VCCD)

#	Required PMIC specification	Function
1	Output voltage accuracy, Current supply capacity	Refer to ”V_{CCD} of Recommended Operating Conditions” in MCU datasheet for the specific values
2	Non discharge function*	The external PMIC must not discharge the output node at PMIC disable status to prevent unintended current consumption.
3	Pre-bias soft-start*	This function can prevent VCCD voltage drop and overcurrent by PMIC sinking current from the internal active regulator at VCCD power handover from the internal active regulator inside the MCU to the external PMIC.
4	Enable function	MCU controls power supply of external PMIC with the function
5	Power good function	MCU detects the output status of the external PMIC by the power good function of the PMIC.
6	Output capacitance*	External PMIC must be stable operation with capacitance that is acceptable range of the internal active regulator, since the output capacitor of the external PMIC and the decoupling capacitor of the active regulator inside the MCU are shared.

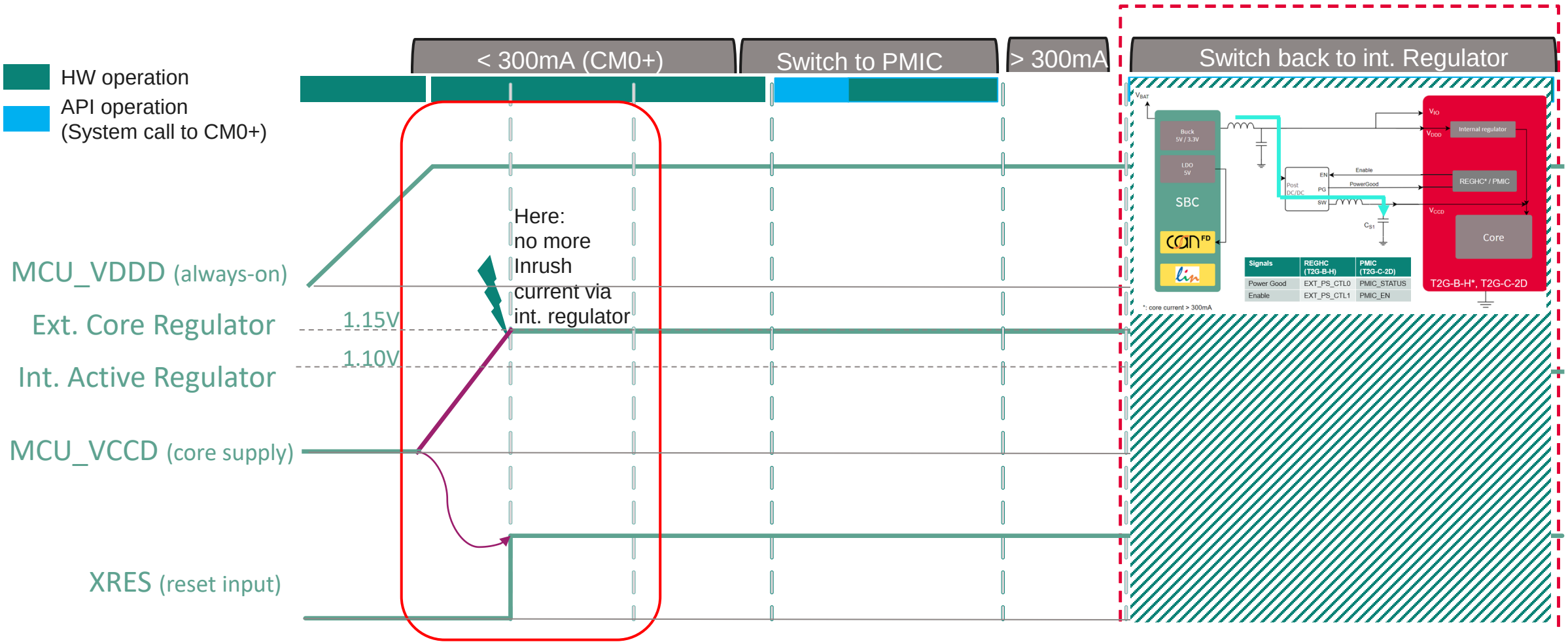
*These are special requirements for general purpose PMIC, but these specifications are not required for the core power structure with load switch.

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Alternate Power Concept: Pre-Charge of Core Supply by ext. Regulator

TRAVEO™ T2G: Power Concept for ext. core supply
“PMIC Direct” Mode - pre-charge core supply (alternate)

– Target: Ramp up Core Supply via ext. regulator before XRES release, to avoid MCU inrush current



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TRAVEO™ T2G: Power Concept
Current Profile, Core Supply Selection and possible Coverage with Pre-Charge Concept

	Body Applications						Graphic Applications		
MCU System	**T2G-B-E**	**T2G-B-H-4M**	**T2G-B-H-4M**	**T2G-B-H-8M**	**T2G-B-H-8M**	**T2G-B-H-16M**	**T2G-C-E-4M**	**T2G-C-2D-4M**	**T2G-C-2D-6M**
Application Core	Cortex M4: 1x	Cortex M7: 1x	Cortex M7: 2x	Cortex M7: 1x	Cortex M7: 2x	Cortex M7: >2x	Cortex M4: 1x	Cortex M7: 1x	Cortex M7: 2x
max DC Core Current	< 150mA	< 300mA	> 300mA	> 300mA	> 300mA	> 300mA	< 150mA	> 300mA	> 300mA
Single Supply Support	yes	yes	no	no	no	no	yes	no	no
- Coverage Pass Transistor vs. ext. Core Regulator	-	-	90% / 10%	40% vs. 60%	40% vs. 60%	0% vs. 100%	-	0% vs. 100%	0% vs. 100%
- Coverage ext. Core Regulator Concept: Pre-Charge vs. "standard"	-	-	80% vs. 20%	90% vs. 10%	80% vs. 20%	80% vs. 20%	-	30% vs. 70%	30% vs. 70%
Always-on Domain (VDDD)	3.3-5V	3.3-5V	3.3-5V	3.3-5V	3.3-5V	3.3-5V	3.3-5V	3.3-5V	3.3-5V
IO Domains	3.3-5V	3.3-5V	3.3-5V	3.3-5V	3.3-5V	3.3-5V	3.3-5V	3.3-5V	3.3-5V
ADC	3.3-5V	3.3-5V	3.3-5V	3.3-5V	3.3-5V	3.3-5V	3.3-5V	3.3-5V	3.3-5V
Memory IF	-	-	3.3V	3.3V	3.3V	3.3V	-	3.3V	1.8V
SMC	no	no	no	no	no	no	yes	yes	Yes
GPU	no	no	no	no	no	no	no	yes	Yes

Main Scope of Pre-Charge Concept due to BOM cost consideration

- GPU: Graphic Processing Unit ; SMC: Stepper Motor Control, PMIC: ext. regulator
- Additional power dissipation by IO to be checked

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TRAVEO™ T2G: Pre-Charge Concept
General System Consideration

- System Consideration:
  - Power Save Mode:
    - Hibernate Mode not supported
    - DeepSleep Mode: Ext. Core Regulator instead of MCU int. DeepSleep Regulator (LDO)
  - Software Handling:
    - „Switch-to-PMIC“ operation still needed and to be done before enabling bigger MCU int. consumption (e.g. core, GPU, Flash)
  - MCU external Reset (XRES) Release:
    - Requirement: MCU XRES release at core voltage level > 1.10V (nom. ext. Level 1.15V) needed
    - Background: Risk of strong Current via VDDD MCU Domain, when Core Voltage < 1.10V during XRES Release
    - How to delay open-drain Power Good (PG) signal: add filter cap + dimensioning of total pull up resistance
      - Release: charge slowly at PG assertion due to open-drain
      - Assertion: faster discharging due to active LOW signal
  - MCU Over-Current Detection (OCD):
    - Over-Current Detection (OCD) feature for core supply in MCU can cause brown-out on MCU always-on domain VDDD, as long as feature is active after HV reset. -> Similar behavior like to the XRES scenario
    - Requirements to bypass capacitance on MCU core supply (see device DS parameter CS1) therefore still valid
    - Setting „No Use of OCD“ recommended in MCU „PMIC“ Mode, to trigger undervoltage reset at core supply (MCU LV BOD: low voltage brown-out detection reset)
  - Ext. Core Regulator Pre-Bias vs. Discharge Function:
    - In normal case Discharge Function will not cause any malfunction to MCU in this concept
  - MCU int. Regulator and Capacitance Range CS1 still mandatory (depends on application functional safety requirement)

- Pro:
  - No inrush current on MCU always-on Domain VDDD after MCU XRES release
  - MCU always-on Domain VDDD can be supplied with smaller supply output current

- Contra:
  - Limited MCU Power Save Mode Capabilities

- Note: Details about ext. core supply concept in: AN226698 – TRAVEO™ T2G: External power supply design guide

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Overview of supported Power Modi by ext. Core Supply Concepts

MCU Power Mode	"Standard" (Inrush @ 3.3V/5V)		Alternate: Core Pre-Charge	
	Ext. Core Reg (post / primary)	npn-Transistor	Ext. Post Core Reg	Ext. Primary Core Reg
Active (MCU: ON <-> OFF only)	Yes	Yes	Yes	Yes
DeepSleep (RAM Retention: ON) with **ext.** core regulator	Yes	Yes	Yes	Yes
DeepSleep (RAM Retention: ON) with **int.** core regulator	Yes	Yes	No	No
Hibernate w/ MCU int. RTC wakeup (RAM Retention: OFF)	Yes	Yes	No	No
Hibernate w/o MCU int. RTC wakeup (RAM Retention: OFF)	Yes	Yes	(yes)*[1]	No

Note: *[1] only possible with IFX PMIC like TLF4A due to integrated control of power state machine

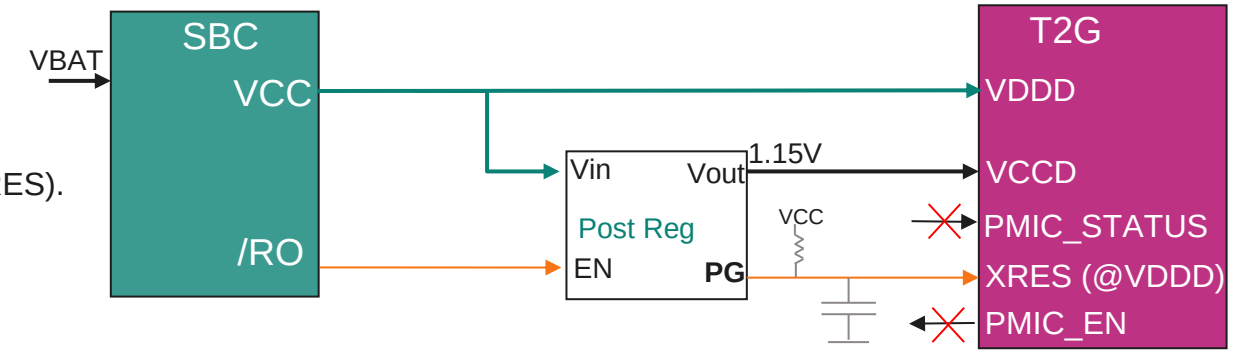
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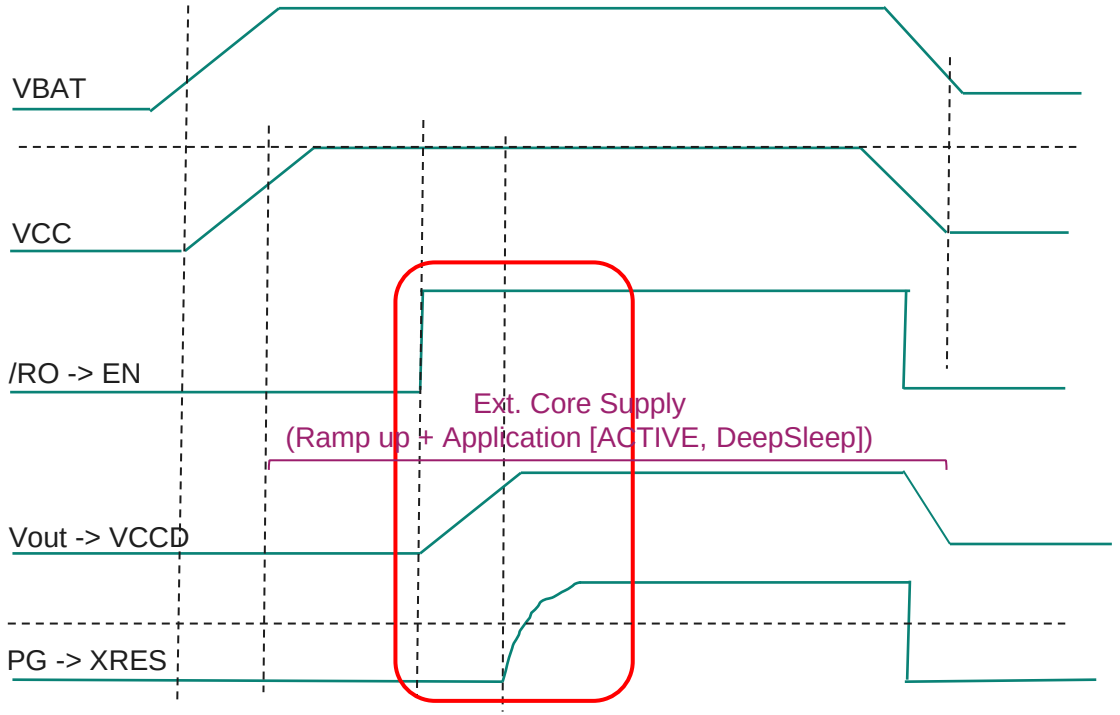
TRAVEO™ T2G: Pre-Charge Concept (Variant A.1)
ext. post core supply for ramp up + application

- System Consideration:
  - Ext. Core Regulator deployed as post Regulator
  - Reset-Out (/RO) enables ext. Core Regulator after passing VCC min. target operation level and reset release time.
  - Power-Good (PG) of ext. core regulator controlling MCU ext. Reset Input (XRES). Connect to MCU PG input (PMIC_STATUS) optional

- Pro:
  - MCU XRES release only, when post-Regulator ready.

- Contra:
  - PG threshold needs to fulfill MCU core supply requirements. Compensation with low pass filter to release the XRES input at target voltage might be not sufficient.

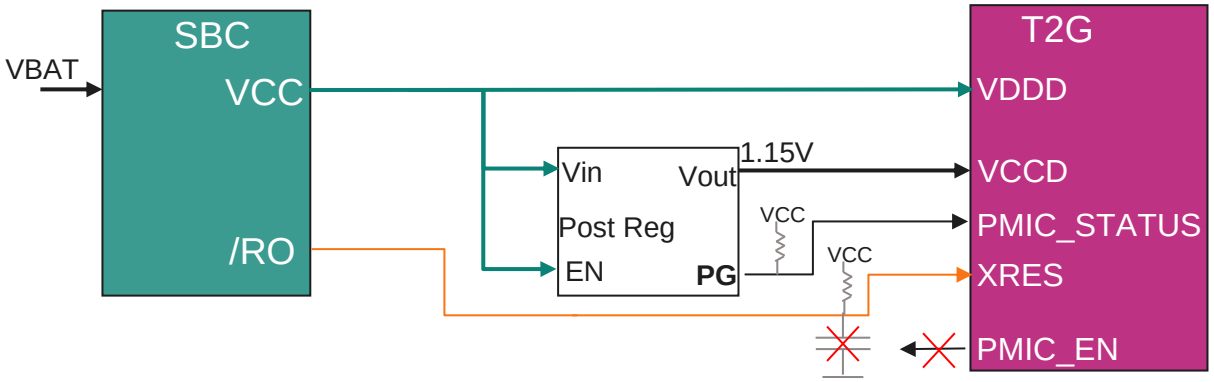




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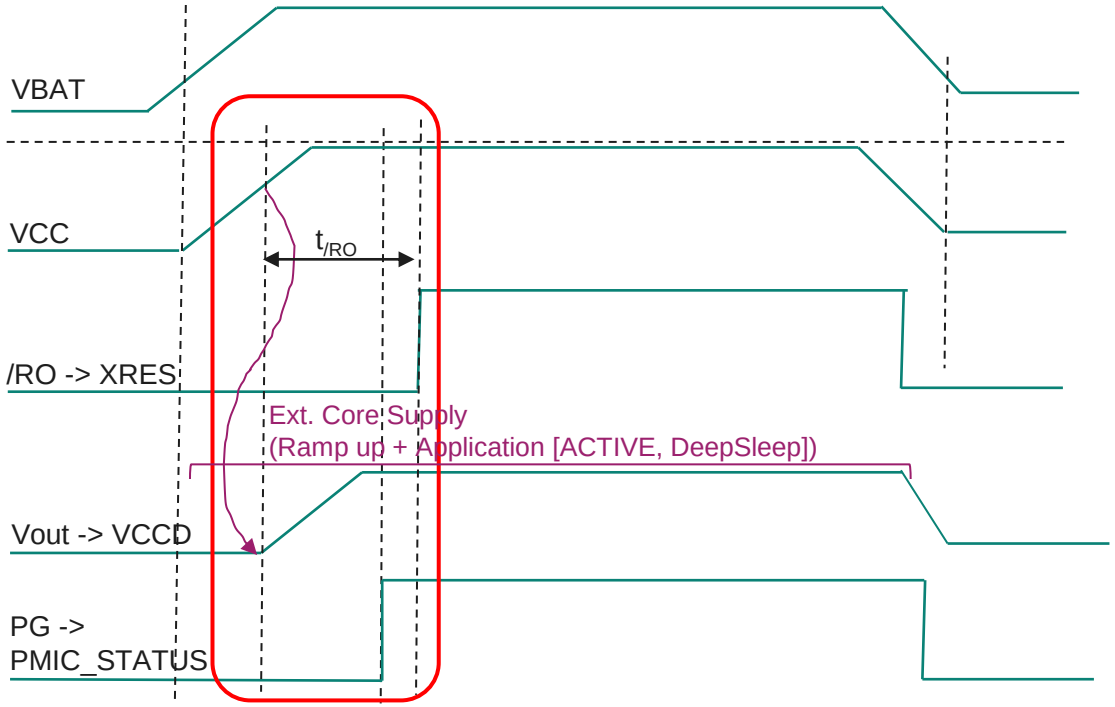
TRAVEO™ T2G: Pre-Charge Concept (Variant B.1)
ext. post core supply for ramp up + application

- System Consideration:
  - Ext. Core Regulator deployed as post Regulator
  - Reset-Out (/RO) of ext. SBC controlling MCU ext. Reset Input (XRES) and optionally as indication Power-Good (PG) of ext. core regulator is connected to MCU PMIC_STATUS.
  - Reset-Out Release ($t_{/RO}$) time needs to be longer than PG release time.
  - Ext. Core Regulator enabled by its own min. Input Level



- Pro:
  - PG threshold requirements of post-Regulator not relevant

- Contra:
  - XRES release by SBC Reset Output not directly related to post-Regulator status

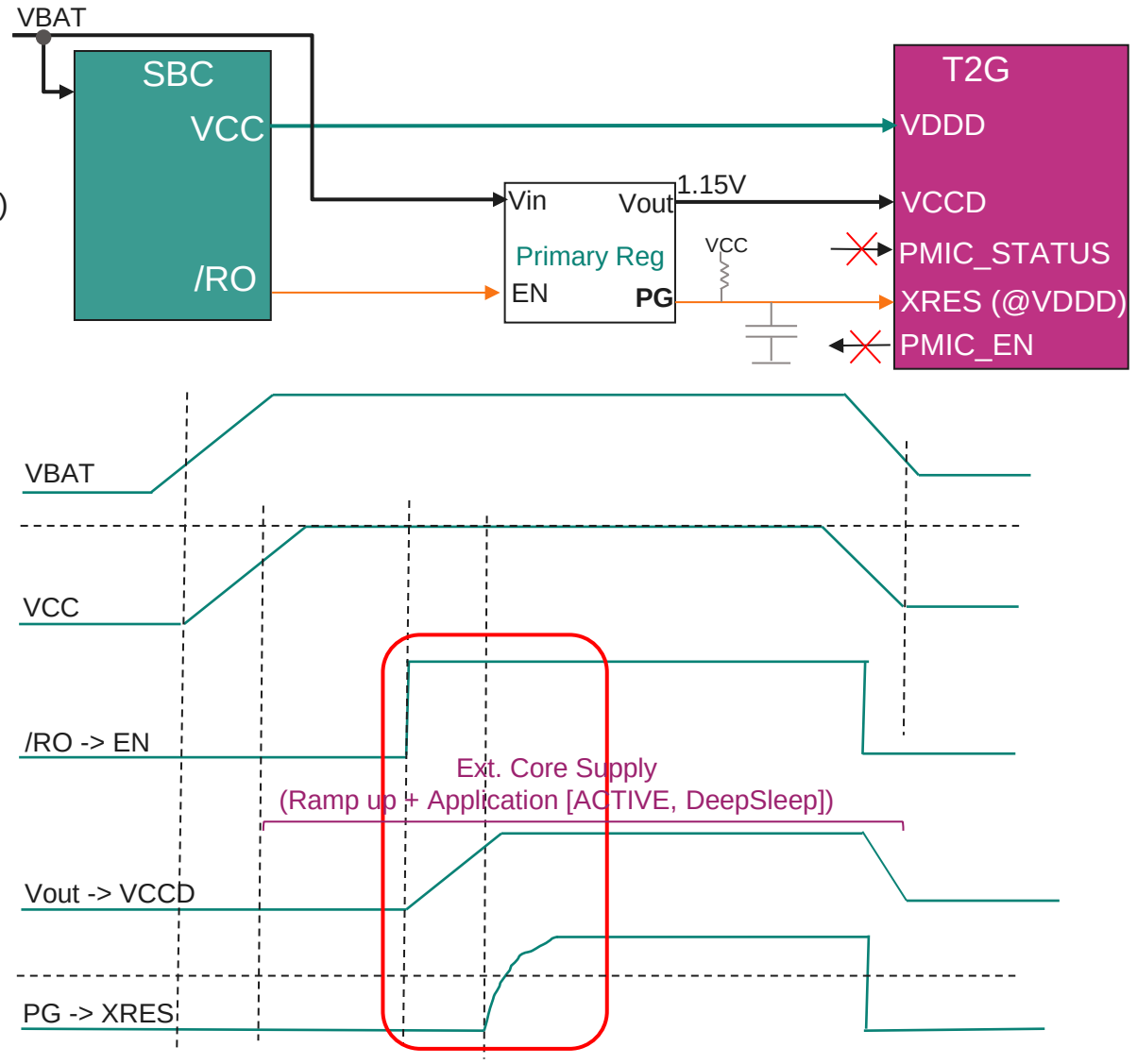


Note: *details in corresponding Traveo™ Archictecture TRM > Reset Chapter

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TRAVEO™ T2G: Pre-Charge Concept (Variant C.1) ext. primary core supply for ramp up + application

- System Consideration:
  - Ext. Core Regulator deployed as primary Regulator
  - Reset-Out (/RO) enables ext. Core Regulator after passing VCC min. target operation level and reset release time.
  - Power-Good (PG) of ext. core regulator controlling MCU ext. Reset Input (XRES)
- Pro:
  - MCU XRES release only, when post-Regulator ready.
  - Weaker Power Supply possible for 3.3V/5V rail (VCC output), because ext. Core Regulator is not supplied by SBC.
- Contra:
  - PG threshold needs to fulfill MCU core supply requirements. Compensation with low pass filter to release the XRES input at target voltage might be not sufficient.
  - Primary Core Regulator itself more epensive than post Regulator, but could be compensated by total Power Supply BOM cost



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Power Concept: HD Pixel Front Lighting (QM) T2G-C-2D-4M (CYT3D)

restricted

T2G-C-2D-4M (CYT3D) Application: HD Pixel Front Lighting (QM)
Image stream at HD Light Module ($T_{A,MCU}$ = 125°C)

HD lighting

Automotive power ICs

- **LED drivers: LITIX™**
- Power MOSFETs: OptiMOS™ 5
- System Basis Chips (SBC): OPTIREG™ SBC
- Switcher
- Linear supplies: OPTIREG™
- Motor drivers: TLE4209G
- High-side switches: PROFET™ +2 12 V

Automotive microcontrollers

- **TRAVEO™ T2G Cluster (T2G-C-2D-4M)**

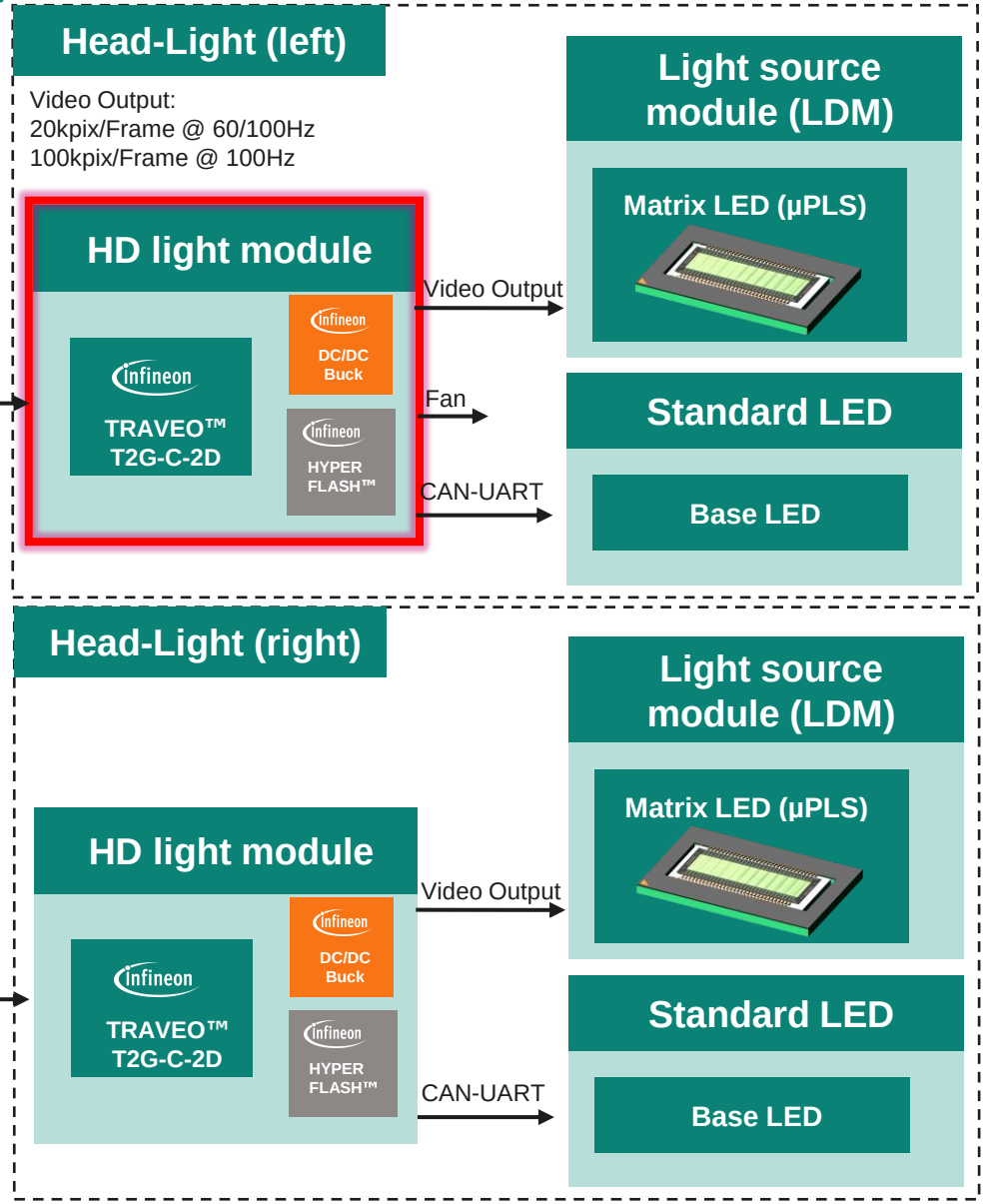
Connectivity ICs

- **Automotive Transceiver**

Sensor Fusion (ADAS)

Inputs from: Camera, Radar, Lidar, Other ECU, navigation, Sensors

CAN(FD) / Ethernet

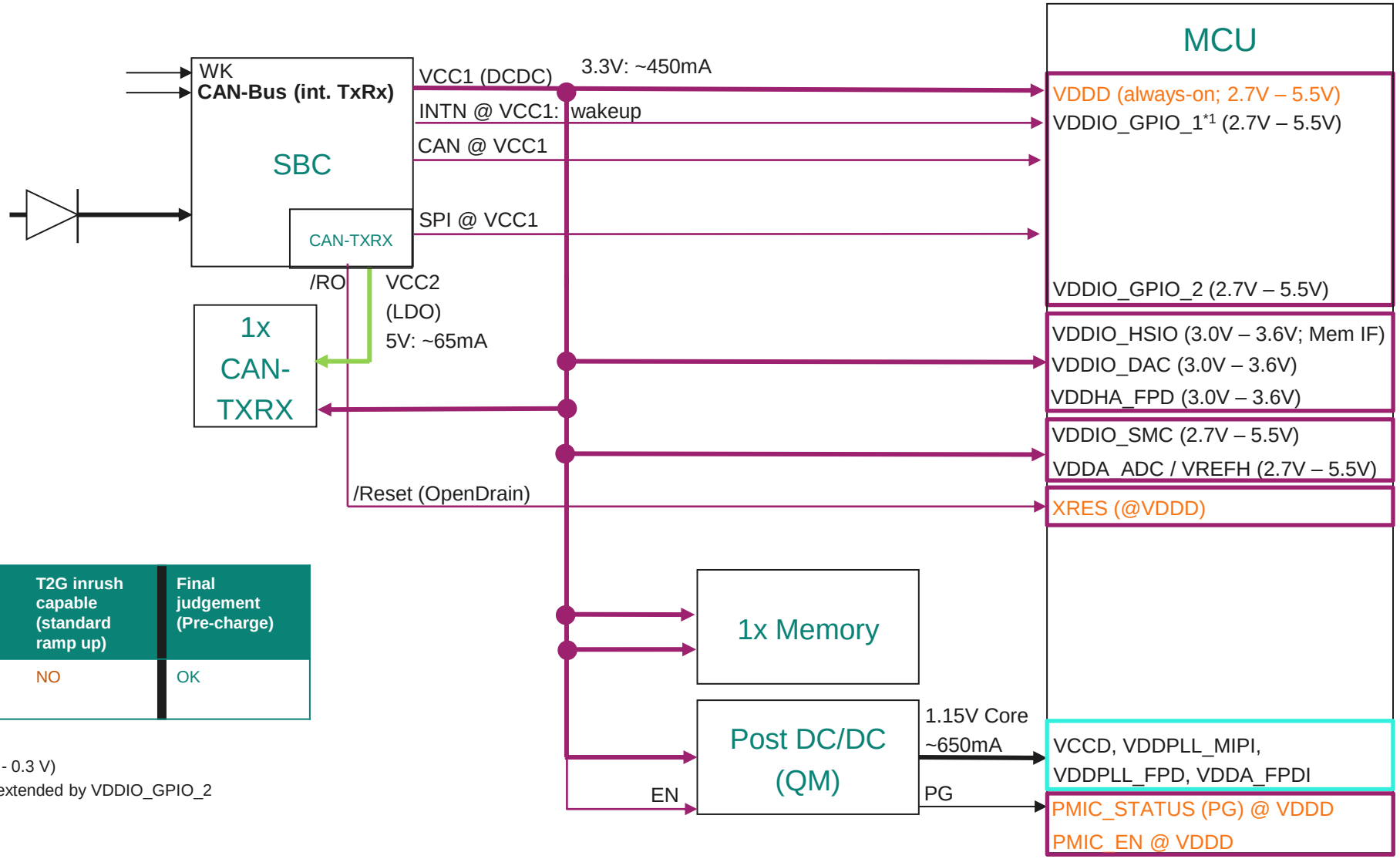


CAN(FD) / Ethernet

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T2G-C-2D-4M (CYT3D) Application: HD Pixel Front Lighting (QM) Power Tree with pre-charge concept (@Variant B.1)

- Used MCU Power Mode:
  - Active only
- Ext. Reset Input (XRES):
  - SBC



Power Supply	ICC1, max	ICC2, max	Static Output Current sufficient	T2G inrush capable (standard ramp up)	Final judgement (Pre-charge)
TLE9471-V33 (QM)	500	100	Yes	NO	OK

- MCU Condition:
  - VDDD ≥ (VDDIO_GPIO_1 - 0.3 V) ≥ (VDDIO_GPIO_2 - 0.3 V)
  - *1: not all Ifs coverable in VDDIO_GPIO_1, optionally extended by VDDIO_GPIO_2

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