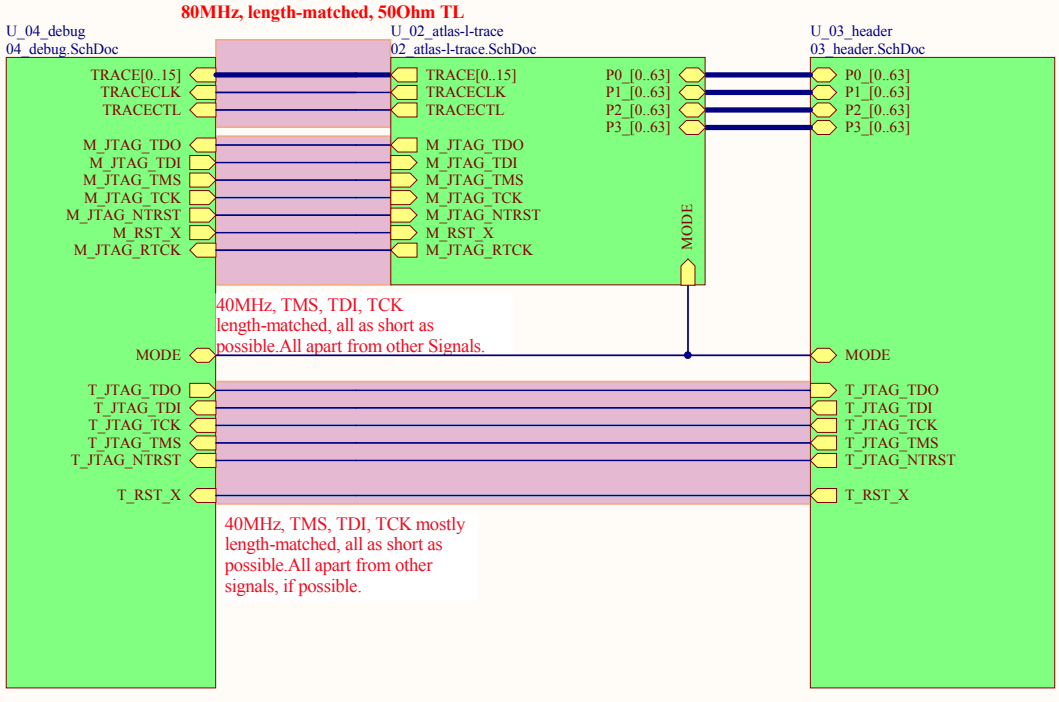

History

Doc Rev.:	Changes:
0.1:	- initial version derived from EMA-MB9DF120-001

```
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/* (V1.3)                                                                    */
/*****************************************************************************/
```

FUJITSU	Product:	EMA-MB9DF125-001	
	Sheet: 1 of 4	Doc Revision:	V0.1
		HW Revision:	V1.0
	Drawn by: Michael Köhler	Date:	5/16/2012
	File: 01_overview.SchDoc		

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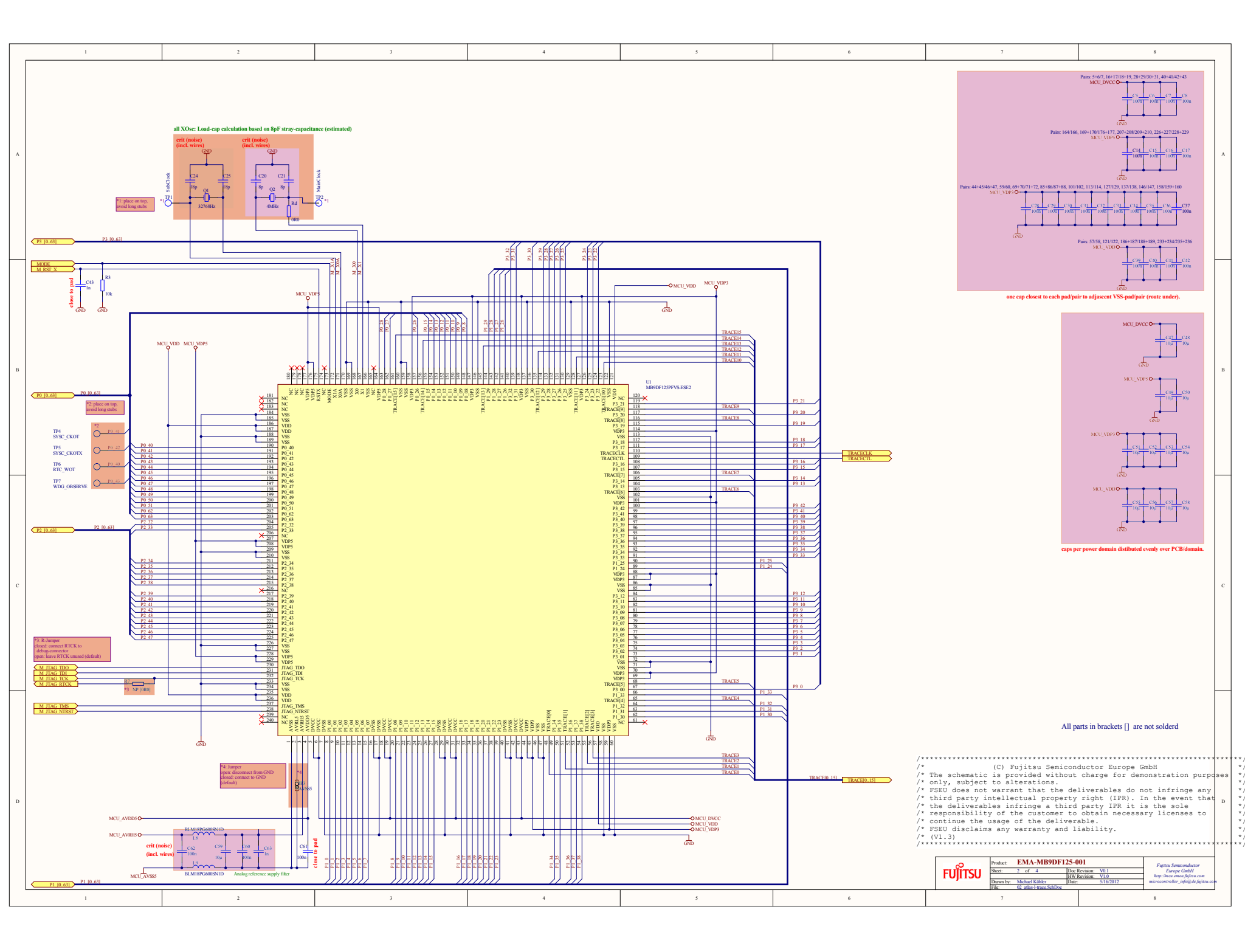
all XOsc: Load-cap calculation based on 8pF stray-capacitance (estimated)
crit (noise) (incl. wires)
crit (noise) (incl. wires)
SubClock
MainClock
32768Hz
4MHz
*1: place on top, avoid long stubs
close to pad
*2: place on top, avoid long stubs
*3: R-Jumper closed: connect RTCK to debug-connector open: leave RTCK unused (default)
*4: Jumper open: disconnect from GND closed: connect to GND (default)
MB9DF125PFVS-ESE2
Pairs: 5+6/7, 16+17/18+19, 28+29/30+31, 40+41/42+43
Pairs: 164/166, 169+170/176+177, 207+208/209+210, 226+227/228+229
Pairs: 44+45/46+47, 59/60, 69+70/71+72, 85+86/87+88, 101/102, 113/114, 127/129, 137/138, 146/147, 158/159+160
Pairs: 57/58, 121/122, 186+187/188+189, 233+234/235+236
one cap closest to each pad/pair to adjascent VSS-pad/pair (route under).
caps per power domain distibuted evenly over PCB/domain.
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(V1.3)
Product: EMA-MB9DF125-001
Sheet: 2 of 4
Doc Revision: V0.1
HW Revision: V1.0
Drawn by: Michael Köhler
Date: 5/16/2012
File: 02_atlas-l-trace.SchDoc
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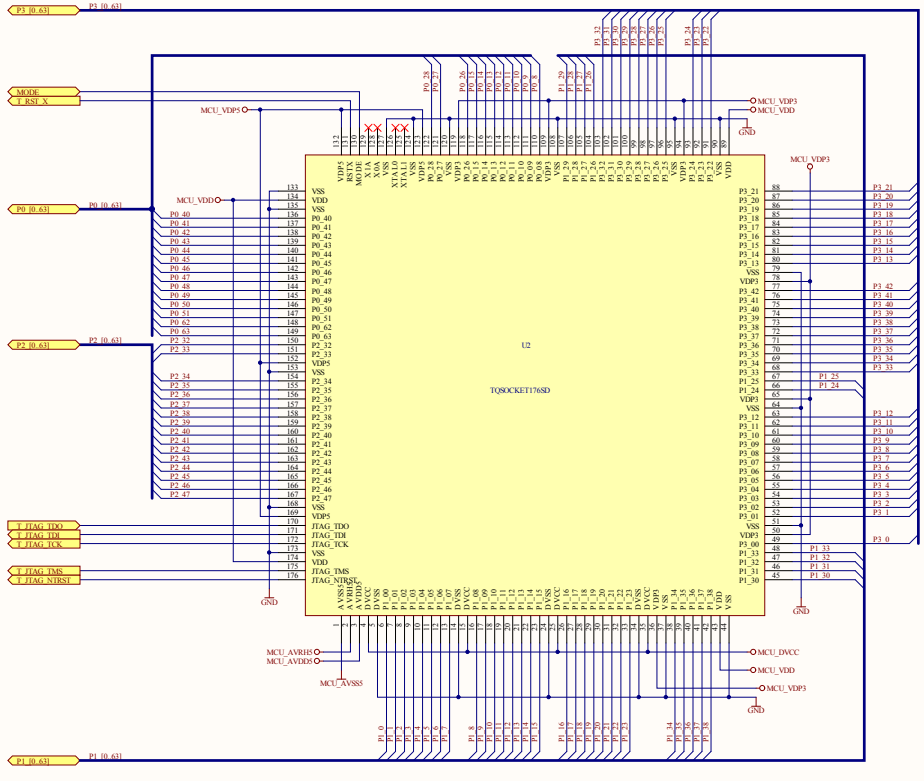


```
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/* (V1.3)                                                        */
/*****************************************************************/
```

All parts in brackets [] are not solderd

Product:	EMA-MB9DF125-001		
Sheet:	3 of 4	Doc Revision:	V0.1
		HW Revision:	V1.0
Drawn by:	Michael Köhler	Date:	5/16/2012
File:	03_header.SchDoc		

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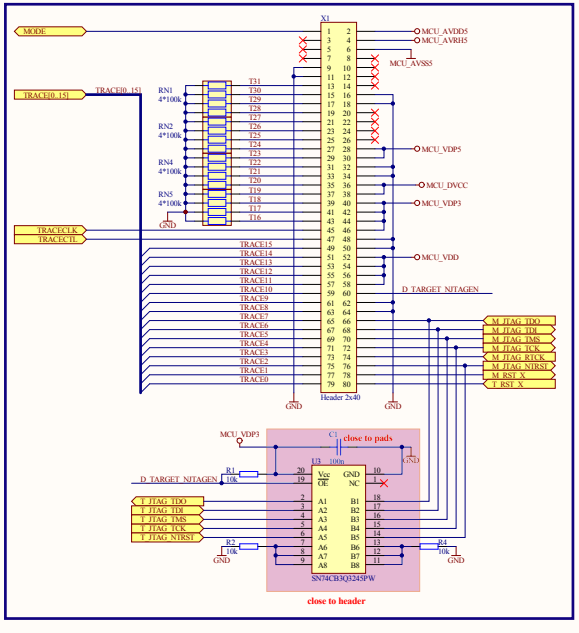
Debug, Trace




```
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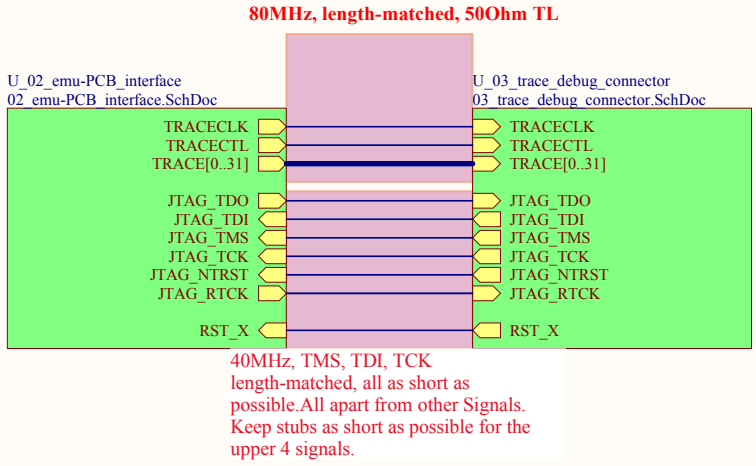
/* (V1.3)                                                                    */
/*****************************************************************************/
```

FUJITSU	Product: EMA-MB9DF125-001		Fujitsu Semiconductor Europe GmbH http://mcu.emea.fujitsu.com microcontroller_info@de.fujitsu.com
	Sheet: 4 of 4	Doc Revision: V0.1	
		HW Revision: V1.0	
	Drawn by: Michael Köhler	Date: 5/16/2012	
	File: 04_debug.SchDoc		




```
History

Doc Rev.:       Changes:
0.2:            initial Version for quotes.
0.3:            added 100nF to voltage-supervisor,
                entered values for R9..14 (DCDC converter,
                voltage supervisor).
0.4             compiled, resolved errors/warnings.
0.5             new MODE-signal from emu-PCB tied to jumper
                via 100k.
0.6             Reset-Supervisor: Part-No. was incomplete,
                completed to "TPS3106K33DBV"
0.7:            Trace-connector hdr/rec swapped (wrong pin-numbering)
                All jumpers set to 2mm pitch (some were 2.54mm)
0.8:             GND connection of C18+C22 close to U2 corrected
                JP10,JP15,JP16 changed to MCU_VDP3/MCU_VDP5
0.9:            Minor corrections to part-numbers/comments according
                to new BOM.
0.10:           !Trace-Connector pinning changed!: TRACE[31..16]
                swapped with TRACECTL/-CLK (same ordering in group)
0.11:           !Trace-Connector pinning changed!:
                        swapped TRACECTL and TRACECLK
                Jumper added to reset-controller to disable trace-
                generated resets.

                Changes due to VDP3 being disableable
                (new information):
                - change net to 3V3 at:
                        - reset-controller.Vdd (from MCU_VDP3)
                        - bus-switch.Vdd (from MCU_VDP3)
                        - LED-VDD, LED-RST supply (from MCU_VDP3)
                        - DEBUG_VDD (fixed; Jumper obsolete =>
                                also renamed)
                        - Trace-Jumpers (replaces MCU_VDP5(!))
                - add diode from VDP5 (at jumper) to
                        DCDC-converter (supply from target
                        for JTAG-interface and 2 LEDs)
                - changed op-mode of DCDC to auto-powersave
                        (MODE-pin from Vin to Gnd)
0.12:           - D3 moved to C19 (same net, but more clearly the power-input)
                - JP10 renumbered to JP18 (a different JP10 was deleted)
0.13:           - D3 removed, added JP19 to select between VDP5 (target)
                        and wall-cube)

HW-Rev. >1.0:
V0.14:          - JTAG_RTCK from debug/trace-connector pin 74 through U1 (switch) to
                        RTCK-jumper (replaces direct TCK-feedback).
                - JTAG: removed pull-jumpers and associated parts
                        (obsolete).
                - TRACE-Connectors: Supply-Jumpers removed, VREF/VSUPPLY tied to 3V3
```


```
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/* (V1.3)                                                            */
/*********************************************************************/
```


Product:	EMA-FCR4-TRACE-001		
Sheet:	1 of 3	Doc Revision:	V0.14
		HW Revision:	Rev1.1
Drawn by:	Olaf Behrendt	Date:	08.06.2011
File:	01_overview.SchDoc		

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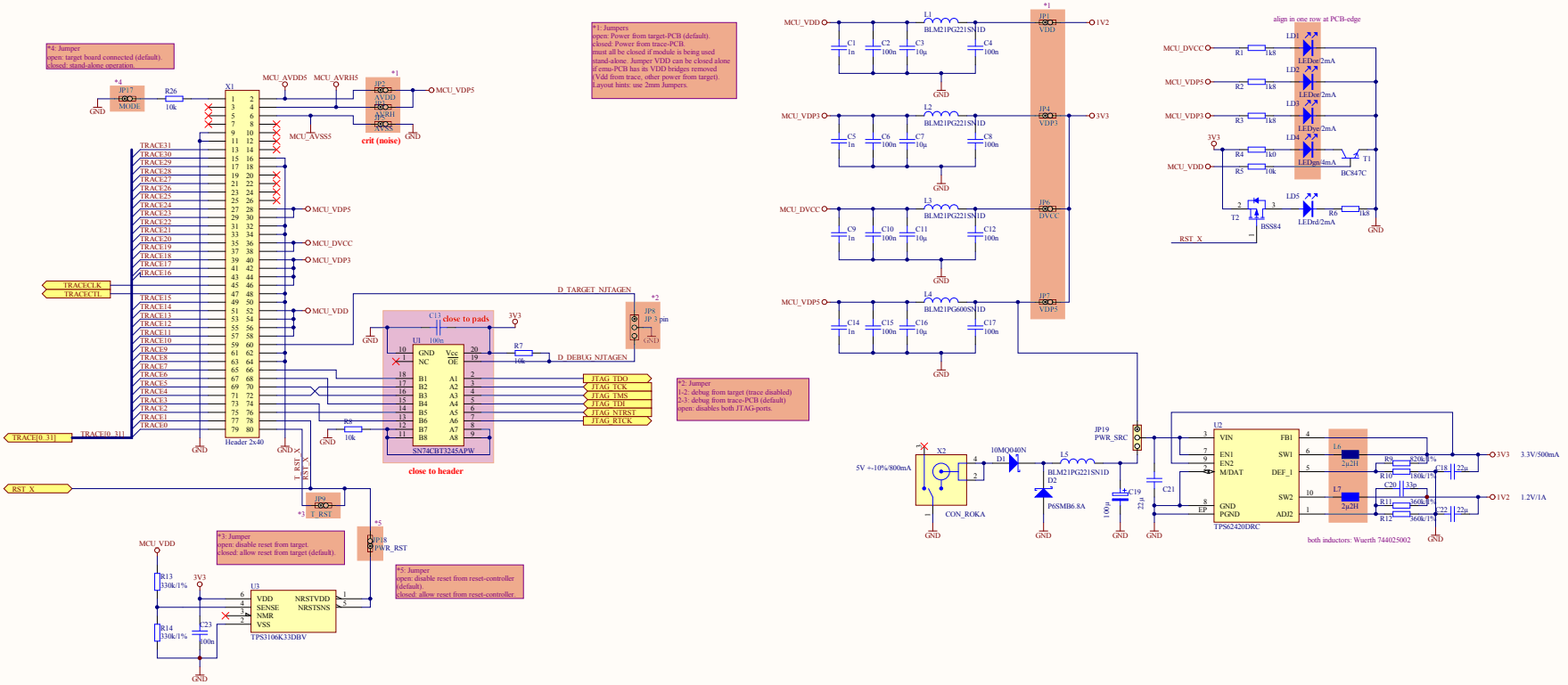


```
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/* (V1.3)                                                                    */
/*****************************************************************************/
```

All parts in brackets [] are not soldered

Product:	EMA-FCR4-TRACE-001		
Sheet:	2 of 3	Doc Revision:	V0.14
		HW Revision:	Rev1.1
Drawn by:	Olaf Behrendt	Date:	08.06.2011
File:	02_emu-PCB_interface.SchDoc		

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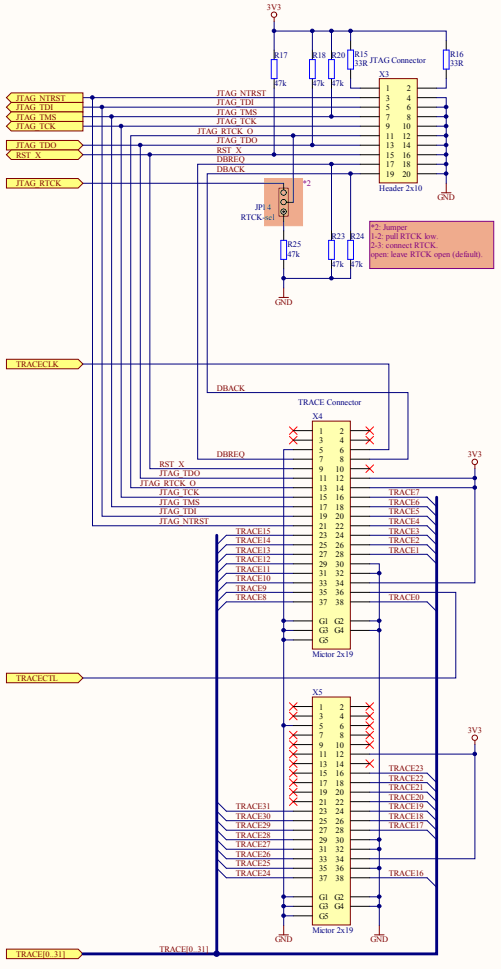


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/* (V1.3)                                                                    */
/*****************************************************************************/
```

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	Sheet: 3 of 3	Doc Revision: V0.14	
		HW Revision: Rev1.1	
	Drawn by: Olaf Behrendt	Date: 08.06.2011	
	File: 03_trace_debug_connector.SchDoc		