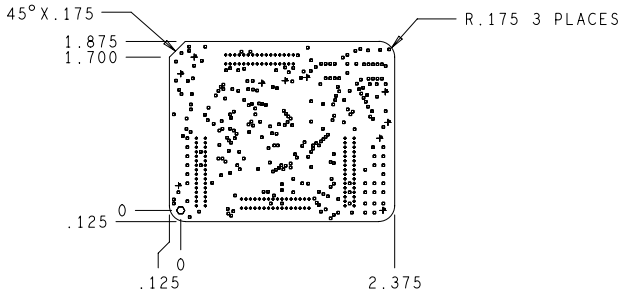
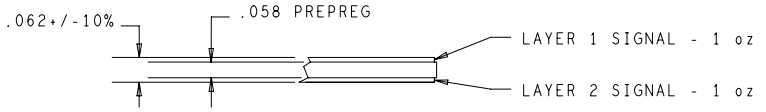
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
1	ALPHA RELEASE	08/28/09	DFK
2	BETA RELEASE	03/24/10	DFK
**	PRODUTION BUILD	03/23/10	DFK





NOTE: 65 MIL 10 MIL SPACING TRACES ON LAYER 1 DIFFERENTIAL IMPEDANCE CONTROLLED TO 90 OHMS +/- 10% TESTED AND CERTIFIED (VENDOR ALLOWED TO ADJUST DIELECTRIC AND LINE WIDTH TO MATCH IMPEDANCE).

NOTES:(UNLESS OTHERWISE SPECIFIED)

1. RoHS COMPLIANT CERTIFICATION OR MATERIAL DECLARATION REQUIRED
2. MATERIAL:
   A. IS410 OR EQUIVALENT. MATERIAL MUST CONFORM TO UL94V-0.
   B. USE HTE COPPER 1 oz. EXTERNAL LAYERS AND 1 oz. COPPER FOR INTERNAL LAYERS WHEN APPLICABLE.
   C. OVERALL METAL TO METAL THICKNESS AS SPECIFIED IN THE CROSS SECTION
3. DRILLING:
   A. DIAMETERS IN DRILL TABLE ARE FINISHED HOLE SIZES +/-.003 TOL. UNLESS OTHERWISE SPECIFIED IN DRILL TABLE.
   B. TEARDROP ALLOWED ON ENTRY OF VIA ON EVERY TRACE LAYER.
4. PLATING:
   COPPER PLATING IN THRU-HOLES .001 min.
5. MARKING:
   A. SILKSCREEN IN WHITE NON-CONDUCTIVE EPOXY INK ON PRIMARY SIDE OF THE BOARD OR BOTH SIDES IF APPLICABLE.
   B. FABRICATOR TO ETCH DATE CODE AND LOGO ON SECONDARY SIDE.
6. FINAL FABRICATION:
   A. SOLDRMASK PRIMARY AND SECONDARY SIDE OF BOARD USING LIQUID PHOTOIMAGABLE MASK MATERIAL OVER BARE COPPER. PER IPC-SM-840. MASK ARTWORKS PROVIDED ARE 1:1. SOLDERMASK COLOR **BLACK**
7. FINISH:
   A. SHALL BE ELECTROLYTIC NICKEL/GOLD. ELECTROLESS NIKEL / IMMERSION GOLD. (ENIG)
   B. NICKEL THICKNESS: 100-200 MICROINCHES.
   C. GOLD THICKNESS: 3-10 MICROINCHES.
8. BOARDS SHALL BE PURCHASED FROM UL RECOGNIZED VENDORS ONLY AND SHALL BE MARKED IN COPPER ON SECONDARY SIDE OF BOARD WITH VENDORS UL IDENT. FLAMABILITY RATING (94-V0), DATE CODE (WWYY), AND RoHS COMPILANT SYMBOL.
9. MANUFACTURE BOARD TO BE IN ACCORDANCE WITH PERFORMANCE STANDARD IPC-6011/6012 CLASS 2 BOARD TO BE INSPECTED PER IPC-600-A CLASS 2.
10. MAXIMUM WRAP OR TWIST SHALL NOT EXCEED .010 in/in.

DRILL CHART: TOP to BOTTOM ALL UNITS ARE IN MILS				
FIGURE	SIZE	TOLERANCE	PLATED	QTY
▫	10.0	+3.0/-10.0	PLATED	271
•	28.0	+3.0/-3.0	PLATED	128
+	43.0	+3.0/-3.0	PLATED	10
o	90.0	+3.0/-3.0	NON-PLATED	1

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ON; ANGLES +/- 2°
2 PL DECIMALS +/- .010
3 PL DECIMALS +/- .005
THIRD ANGLE PROJECTIONS

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SIGNATURES		DATE
DRAWN	ZMK	08/24/09
CHECKED	DFK	08/24/09
ENGRG	DFK	08/24/09
ISSUED		

CYPRESS SEMICONDUCTOR
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Lynnwood, WA 98087
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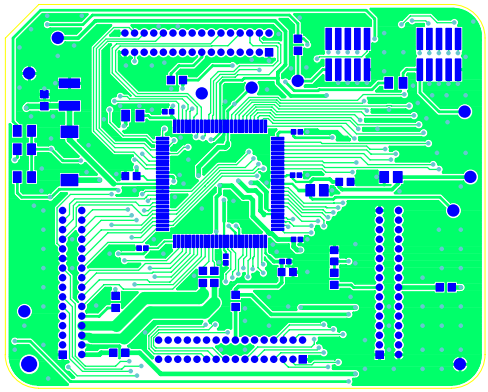
FABRICATION DRAWING CY8C55 FAMILY PROCESSOR MODULE

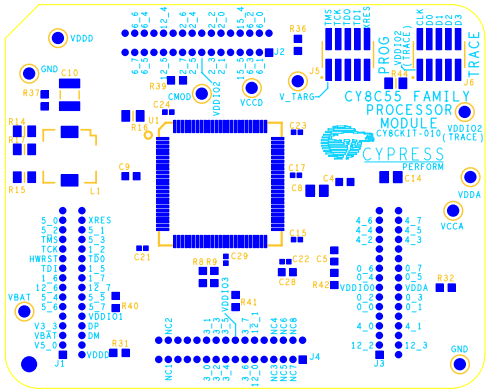
SIZE	FSCM NO	DWG NO	REV
C		PDCR-9546	**

SCALE: 1/1 SHEET: 1 OF 1



PDCR-9546 REV ** PRIMARY SIDE

PDCR-9546 REV ** SECONDARY SIDE



PDCR-9546 REV ** PRIMARY SILKSCREEN

PDCR-9546 REV ** SECONDARY SILKSCREEN