PROFET

Smart High-Side Power Switch BTS50015-1TAD

PSpice Behavioral Model

Application Note

Model Description

- Circuit modeled at concept level after datasheet block diagram
- Parameters fitted for typical behaviour according to datasheet
- Features included in the model
  - typical static and dynamic behavior
  - overvoltage protection for drain pin
  - over temperature detection and protection (shutdown – latch behavior)
  - overcurrent detection and protection (shutdown – latch behavior)
  - loss of ground detection and protection (shutdown)
  - loss of load protection
  - loss of supply detection and protection
  - short circuit protection
  - reverse polarity protection
  - open load detection in ON state
  - short to battery detection
  - inverse load current operation detection
  - undervoltage shutdown and restart

- Limitations of the model
  - other possible thermal dependencies than the ones highlighted above
  - no ESD, EMC, worst-case analysis simulation capability
  - possible convergence issues for using DC sources, steep ramps or high frequency sources within the setup. For workarounds in case of non-convergence issues please check "simulation settings" topic at the end of this Application Note

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How to use the Model

- The delivery package contains important files that enable the use of the model in custom schematic test benches:

  - **BTS50015-1TAD_encrypted.lib** (PSpice behavioral description)
  - **BTS50015-1TAD.olb** (contains the symbol view for the graphical user interface "Capture" compatible with Allegro ver. 16.2 and higher)
  - **BTS50015-1TAD_16.2.olb** (contains the symbol view for the graphical user interface "Capture" compatible with Allegro ver. 16.2)

- These files are meant to be used with Cadence Capture CIS (Allegro Design Entry CIS ) as it will be explained in the following slides

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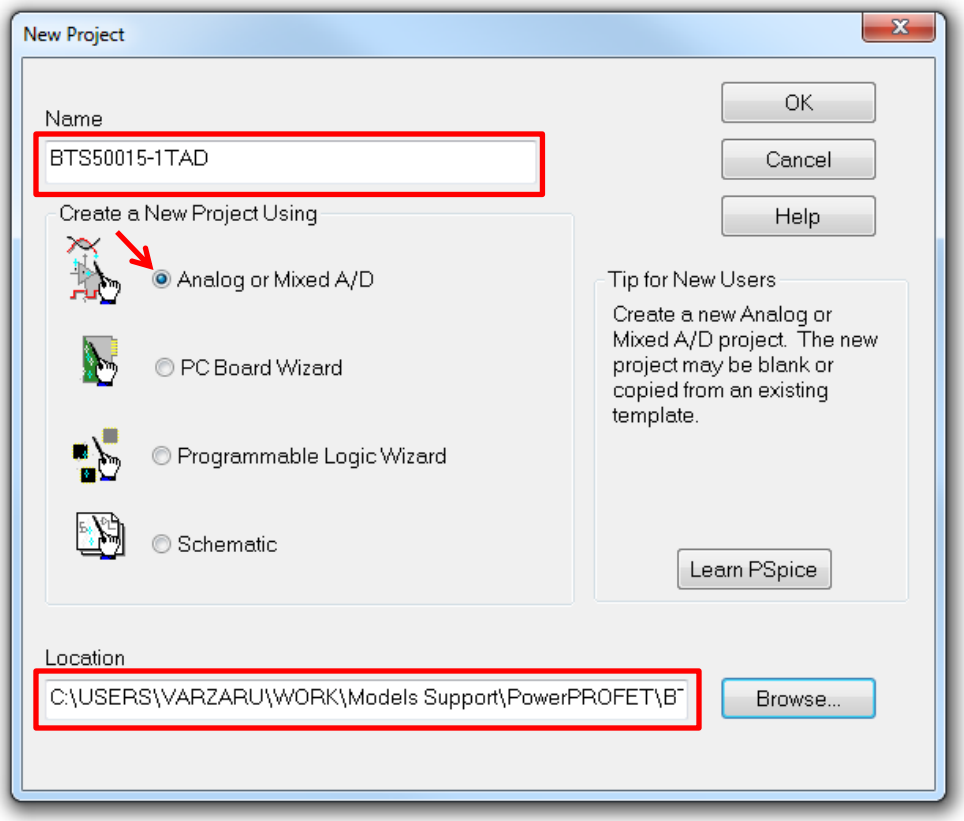
Graphical User Interface Guide [1]

- Once you have opened Cadence *OrCAD Capture CIS* and want to create a new project, in order to use the PSpice model the following steps are necessary:
  - Go to: *File → New → Project…*
  - Enter the project name in the *Name* field
  - Choose *Analog or Mixed A/D* option
  - Specify the root location where the project will be stored and hit *OK*



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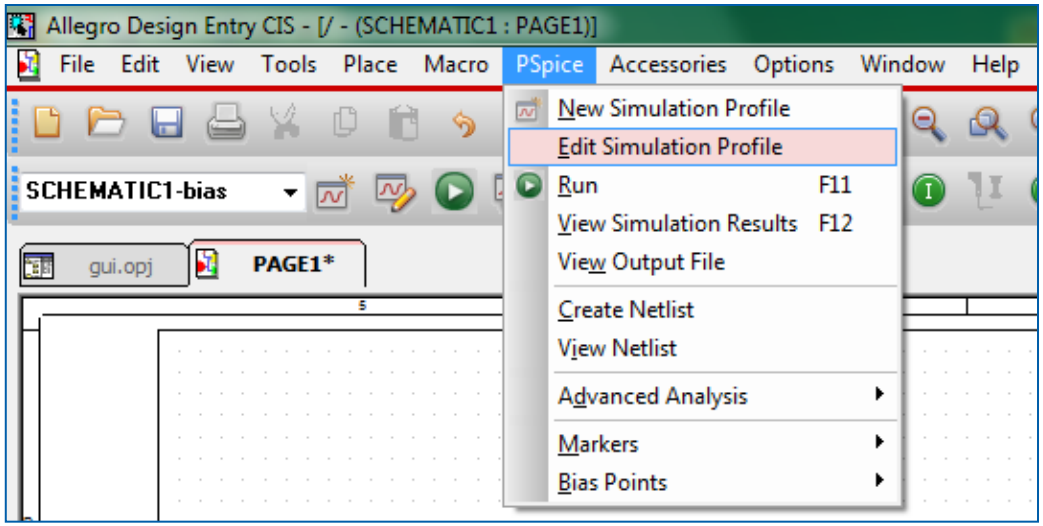
Graphical User Interface Guide [2]

- From the *PSpice* menu choose *Edit Simulation Profile*:



- On the window menu that pops up go to the *Configuration files* tab and from the *Category* options choose *Library*. Under *Details*, at the *Filename* tag click *Browse* and select the model *.lib file (in this case **BTS50015-1TAD_encrypted.lib**) from the folder where you have it stored.

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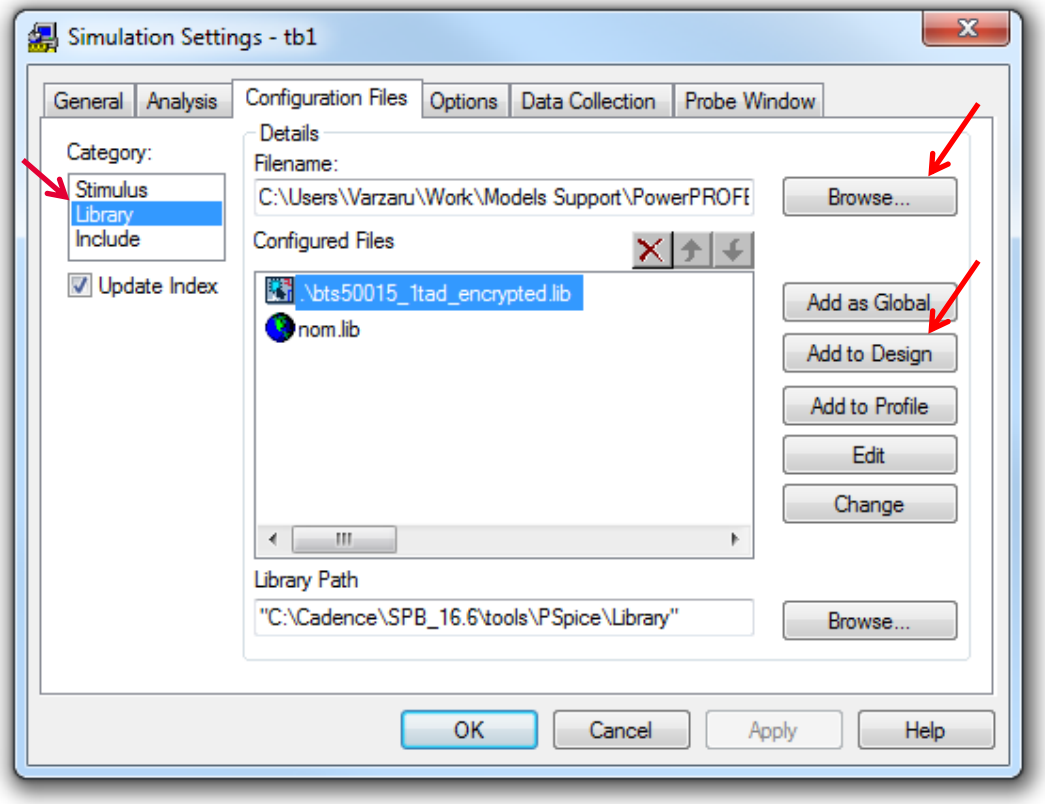
Graphical User Interface Guide [3]

- After validating the selection, you have to choose how you want the library to be available: *Add as Global* to all the designs, *Add to Design* for the current design only or *Add to Profile* local to the current test-bench inside the current design. *Add to Design* is the most common option to choose.



- The next step is adding the Capture part *.olb symbol file.

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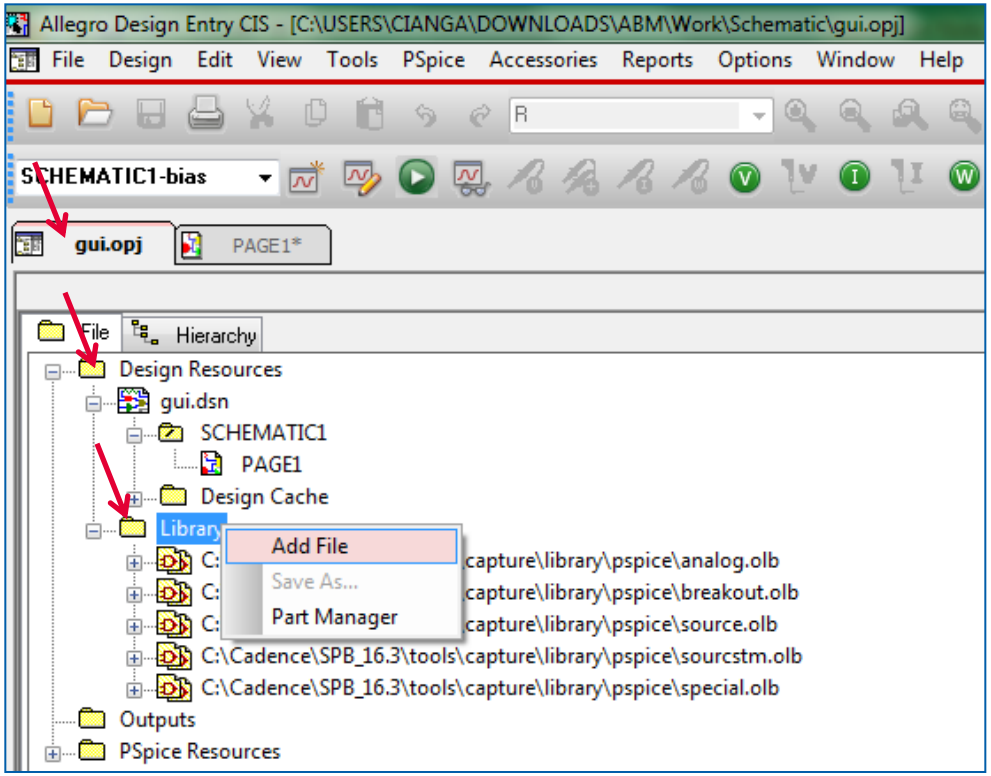
Graphical User Interface Guide [4]

- From the Project tab, under *Design Resources*, right click on *Library* and choose *Add File*.



- Using the window that pops up, browse for your *.olb file (in this case **BTS50015-1TAD.olb**) and select it.

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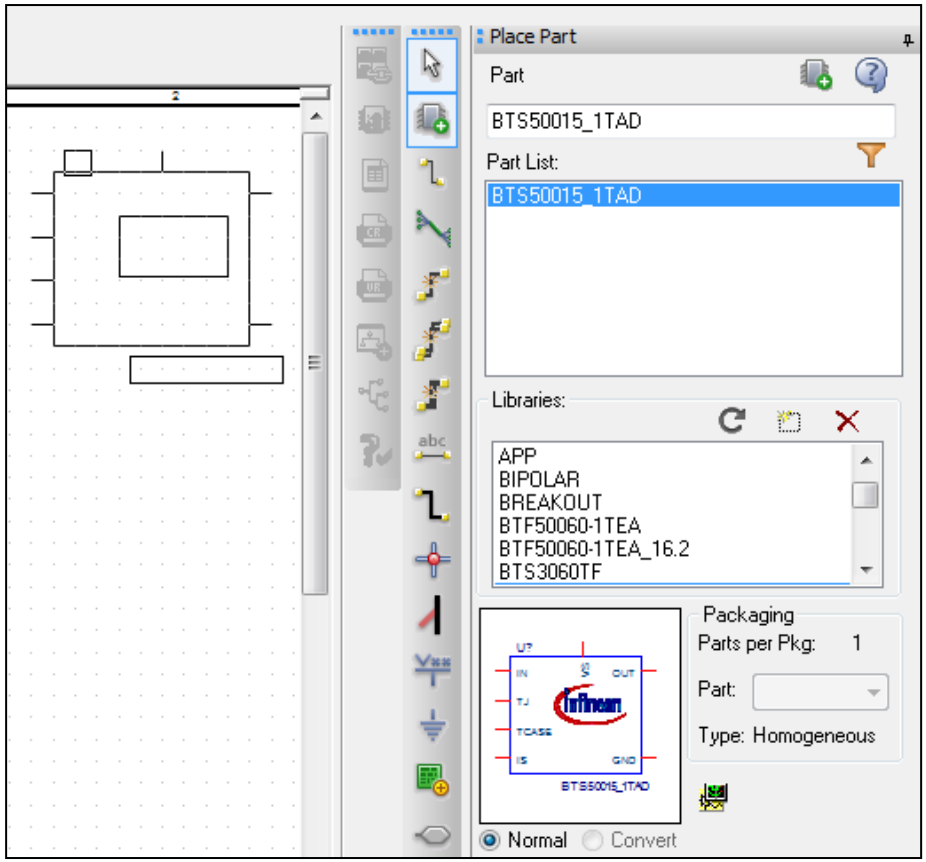
Graphical User Interface Guide [5]

- Adding that file to the design resources makes the model available for use.

- Searching for it in the *Place Part* sidebar, you can place the Model Symbol in a schematic of your choice.



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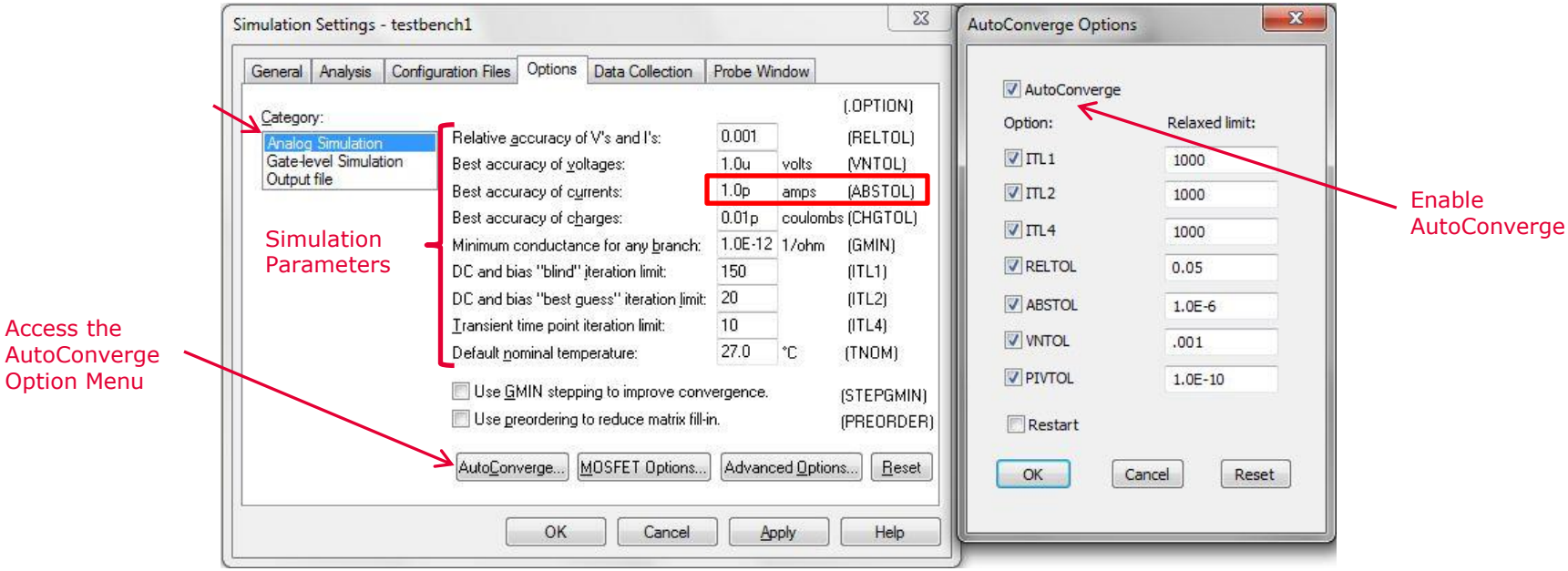
Simulation Settings [1]

- The PSpice model is not guaranteed to work in every test situation with the default simulator settings. Therefore when the simulation does not converge it is recommended to change the simulation options and loosen the parameters. Increasing the *ABSTOL* from 1p to 1n sometimes helps overcoming convergence issues.
- The simulator has a special option called *AutoConverge (PSpice→Edit Simulation Profile→Options)* which may help but usually it is not recommended as it loosen too much the parameters and impact results accuracy; the common approach would be to control each parameter individually and gradually relax the limits while keeping the accuracy in reasonable limits.



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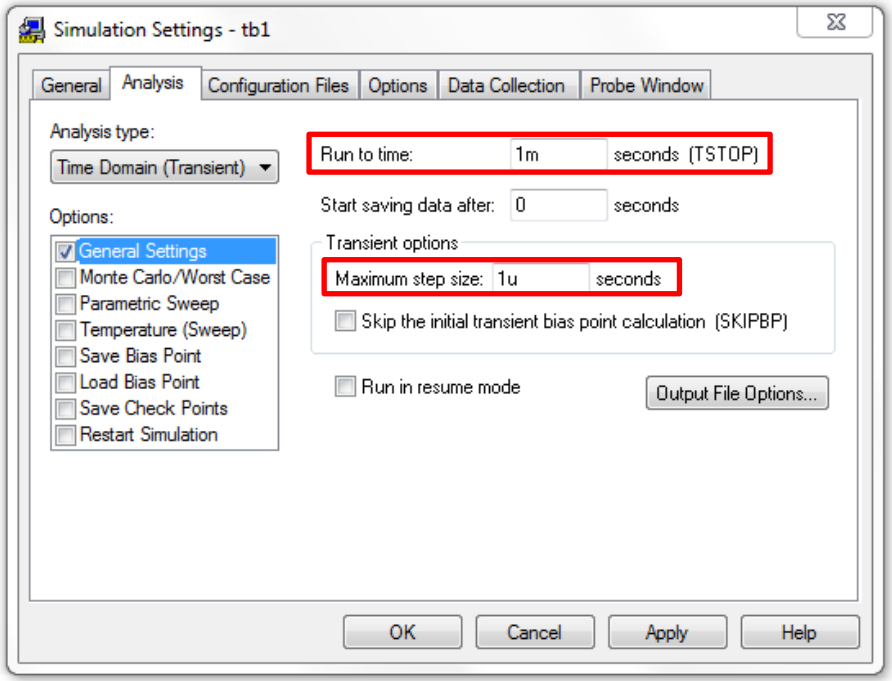
Simulation Settings [2]

- Try limiting *Maximum step size* to 1us but in this case should expect a proportional increase in total simulation time when test duration is large (>100ms); as a general rule, the ratio between *Run to time* and *Maximum step size* should be 1k to 10k for decent simulation time and results accuracy; for high precision simulation results (e.g. switching times), *Maximum step size* smaller than switching period is required
- Enabling autoconverge option could result in some simulation parameters that together with large timesteps would lead to unrealistic results or a convergence fail



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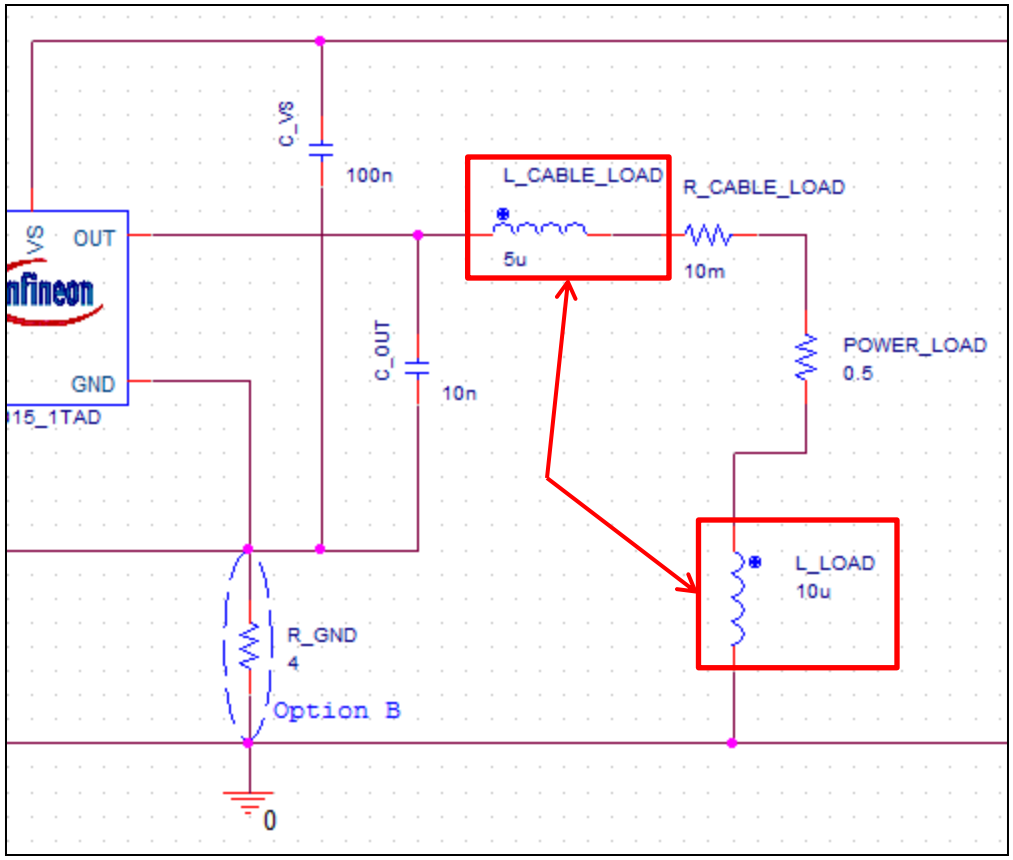
Convergence

- One of the reasons that may cause the simulator to give convergence errors is coming when using two or more inductors/capacitors in series
- For example, the cable inductance and load inductance which come in series; for some particular values, it is recommended to combine both inductors in one device; this may help with handling this issue



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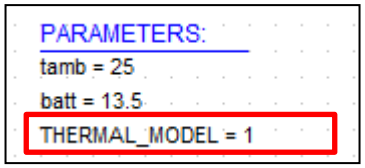
Thermal behavior simulation [1]

- The model contains 4 different Junction to Ambient thermal networks associated to different metallization and cooling areas.
- To switch between the four networks available, change the value of THERMAL_MODEL parameter which can be found on the provided setup test bench
  - THERMAL_MODEL=1: P=1W; T=85°C; PCB type: 1s0p 300mm2
  - THERMAL_MODEL=2: P=1W; T=85°C; PCB type: 1s0p 600mm2
  - THERMAL_MODEL=3: P=1W; T=85°C; PCB type: 1s0p footprint
  - THERMAL_MODEL=4: P=1W; T=85°C; PCB type: 2s2p with thermal via

where: P=power on the power transistor; T=ambient temperature



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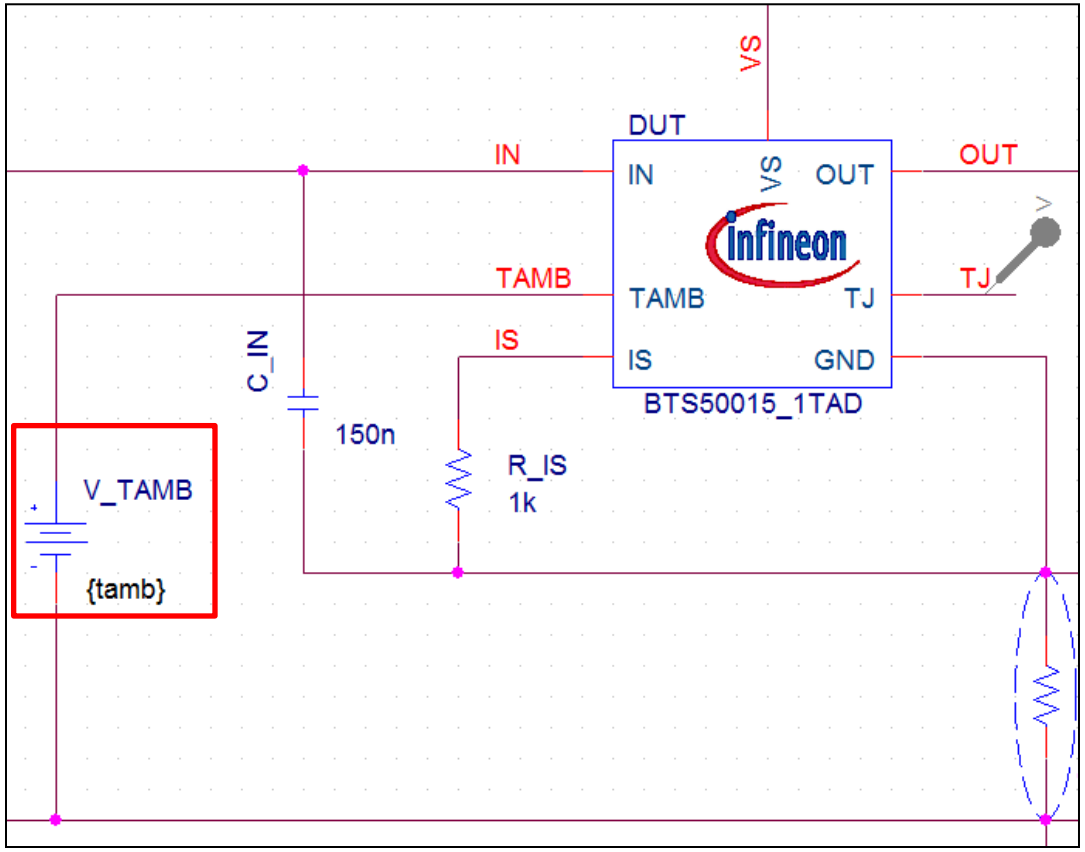
Thermal behavior simulation [2]

- The Ambient temperature of the entire chip can be set by connecting a voltage source to TAMB input pin.
- Junction temperature is always TAMB + temperature due to self-heating of the DMOS (the convention is 1V=1°C)

PARAMETERS:
tamb = 25
batt = 13.5
THERMAL_MODEL = 1



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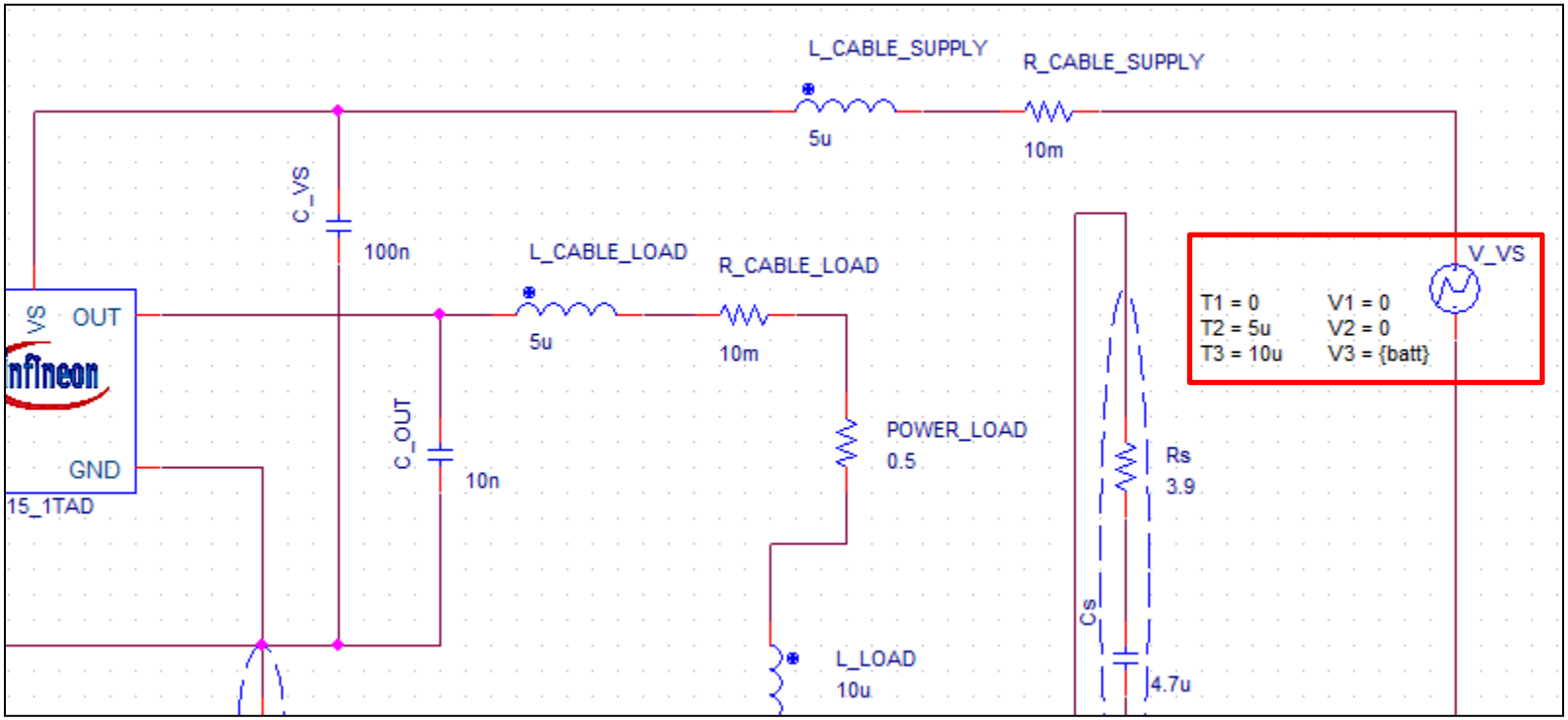
Circuit start-up

- It is recommended that supplies start from 0V at start-up (t=0s); Instead of DC voltage source, try using PWL voltage source on supply pin, similar to one in figure below
- If PWL voltage source is used, there may be cases when the model will not converge for some very limited combinations of ramp levels and steepness.



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