Infineon Automotive Microcontroller Selection Guidelines for OBC and HV/LV DCDC

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Abstract

The OBC and HV/LV DCDC market is moving from distributed controller architectures toward more integrated, safety-capable MCU-centric platforms. This transition is driven by two major industry directions: increasing functional integration at the MCU level and the evolution from conventional two-stage toward single-stage OBCs. As OEMs and Tier 1 suppliers seek to reduce system cost, optimize form factor, and remain competitive in increasingly price-sensitive power conversion markets, the key question is no longer simply whether an MCU can control the power conversion system, but which MCU provides the right balance of performance, cost, safety, and scalability for each switching-frequency range and topology class.

This white paper examines key market-driven technical challenges and explains how AURIX™ TC3x and TC4x MCUs address them through scalable power-conversion control capabilities. Based on quantitative PWM-resolution analysis, AURIX™ TC3x at 400 MHz can support main switching frequencies up to 250 kHz, while AURIX™ TC4x provides additional performance margin for switching frequencies above 250 kHz and potentially beyond 1 MHz. The paper further discusses modulation challenges in single-stage OBC systems and presents architecture-level implementation approaches applicable to both three-phase and single-phase single-stage OBC configurations.

For HV/LV DCDC, the white paper explains and compares how the fast comparator capabilities of AURIX™ TC3x and TC4x MCUs can support peak current mode control (PCMC). Meanwhile, for cost-optimized designs, average current mode control is increasingly being considered as an alternative to peak current mode control, enabling further cost reduction with only an approximately 1% reduction in peak efficiency.

Infineon offers a broad and future-ready MCU portfolio designed to address a wide range of power conversion architectures. This white paper provides practical MCU selection guidelines for OBC and HV/LV DCDC applications, helping OEMs and Tier 1 suppliers identify the best-fit device for their specific system requirements. By enabling the right balance between performance, integration, cost, and scalability, Infineon helps customers avoid both over-sizing and under-sizing while supporting applications from high-end platforms to cost-optimized designs.

Key words

Market trends, x-in-1, Single-stage OBC, HV/LV DCDC, Peak current mode control, AURIX™, PSoC™

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1 OBC and HV/LV DCDC market trends

As illustrated in Figure 1, the main market trends for OBC applications can be summarized as follows:

- The OBC market is converging toward the 11 kW power class. In China, 6.6 kW remains the dominant market segment, while 9 kW solutions are increasingly discussed in the context of 40 A single-phase charging.
- Form-factor optimization is primarily focused on reducing the z-dimension, which is one of the key factors driving the development of single-stage OBC architecture.
- A charging efficiency of approximately 96% represents the current industry benchmark. At the same time, the adoption of vehicle-to-grid (V2G) functionality further increases the importance of improving efficiency under light-load operating conditions.
- The 800 V class is gradually becoming mainstream, while battery voltages of 900 V and above are beginning to gain market share, as reflected in observed customer requirements.

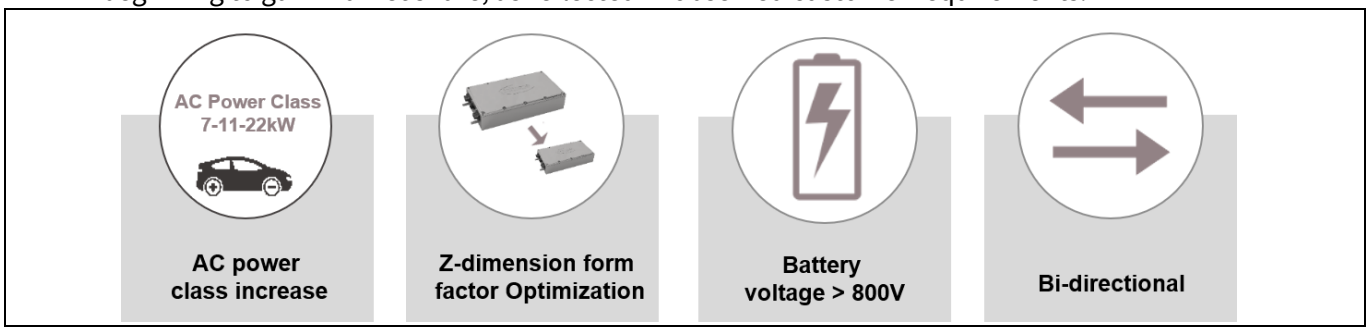

Figure 1 Key trends for OBC

The primary trends for HV/LV DCDC are illustrated in Figure 2:

- Phase shift full bridge and hard switching full bridge remain two predominant topologies in the market.
- Supplying power above 4 kW to a single ECU is not feasible with 12 V and therefore requires a 48 V system; however, the converter topologies remain unchanged.
- Light-load efficiency is a critical design consideration, as DCDC converters operate under light-load conditions for more than 60% of their operating time. However, the relative light-load efficiency advantages of these topologies remain under discussion.

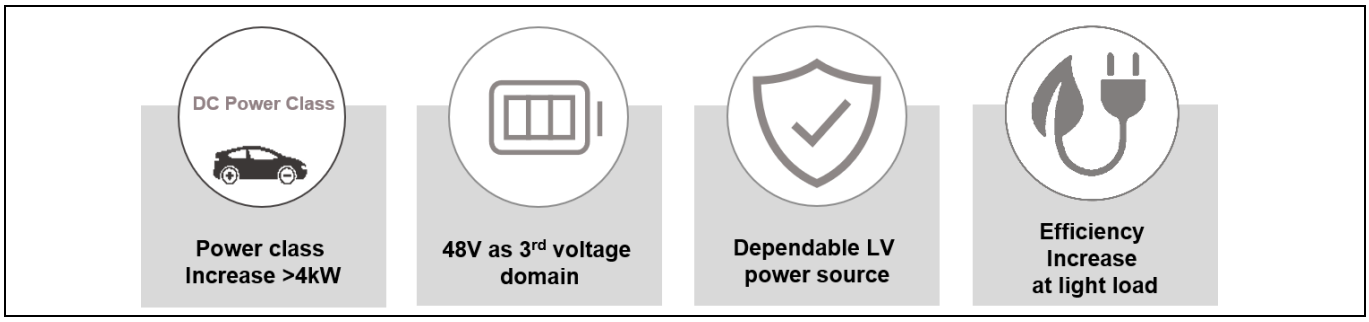

Figure 2 Key trends for HV/LV DCDC

Apart from the topology trends, integration at the functional level (x-in-1) has become essential for achieving system-level cost optimization. As illustrated in Figure 3, two market evolution steps are emerging to reduce system costs: firstly, moving from scenario ① to ③, increased functional integration with fewer MCUs and DSPs is becoming the industry standard. As reinforced isolation technologies have matured and become more cost-effective, the savings from using fewer MCUs and DSPs more than offset the additional isolation cost, resulting in lower overall system costs. Additionally, this approach offers further advantages, including a reduced number of PCBs, fewer automotive-grade connectors, decreased software maintenance requirements,

lower licensing fees, and simplified part number management. Secondly, advancing from scenario ③ to scenario ④ represents a significant step in optimizing the z-dimension of the OBC unit by eliminating bulky electrolytic capacitors.

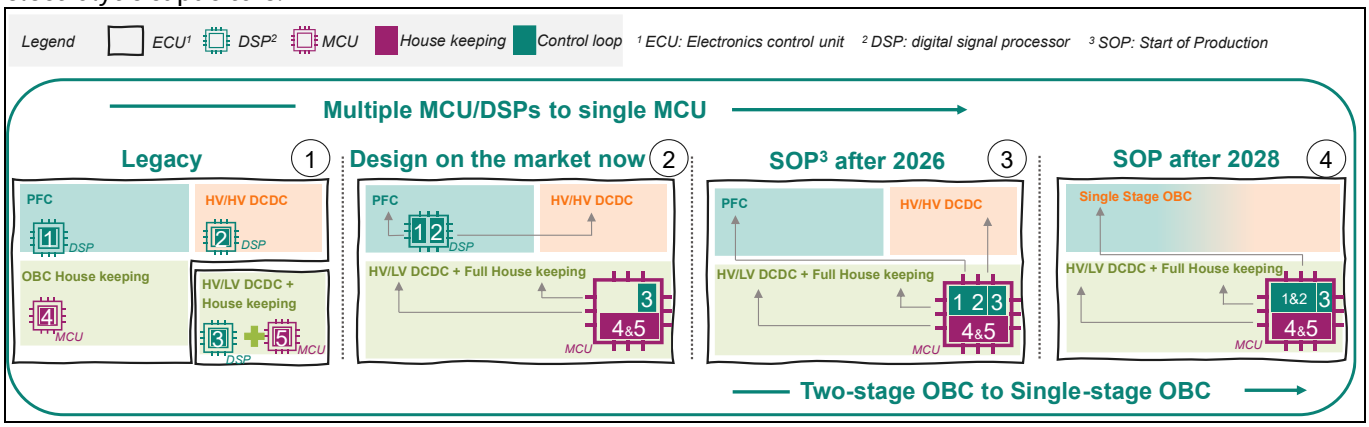

Figure 3 Market evolution paths: MCU+DSPs to single MCU, and Two-stage to Single-stage OBC

For legacy platforms, AURIX™ MCU is typically used for housekeeping functions to guarantee the ASIL-D requirements and partially for control functions. Given the evolution paths, the same MCU is further extended to execute full control loops, which saves significant development costs, especially for entry level platforms.

2 Main specification differences between AURIX™ TC3x and TC4x MCUs for power conversion applications

When selecting an MCU for power conversion applications, power electronics engineers typically prioritize several key specifications, including PWM resolution, on-chip analog comparator reaction time, timer architecture, computational resources, and processor architecture. Accordingly, Table 1 compares these features between AURIX™ TC3x and TC4x MCUs. Notably, AURIX™ TC3x offers enhanced performance with its 400 MHz version [1], building upon the established AURIX™ TC3x architecture. This advancement facilitates faster deployment and reduces integration risk, while preserving investments in existing software, safety concepts, and hardware designs.

Table 1 Comparison of key features between AURIX™ TC3x and TC4x*

	AURIX™ TC3x 300 MHz Version	AURIX™ TC3x 400 MHz Version	AURIX™ TC4x
PWM resolution	5 ns	3.75 ns	156 ps
On-Chip analog comparator reaction time	approximately 150 ns	approximately 150 ns	below 50 ns
Core Performance	TriCore v1.6@ 300 MHz + GTM MCS	TriCore v1.6@ 400 MHz + GTM MCS	TriCore v1.8@ 400 MHz + PPU@ 400 MHz + CDSP + GTM MCS
Bus architecture	Single system peripherals bus (SPB)	Single system peripherals bus (SPB)	Multiple buses

*Please refer to corresponding Datasheet and User Manual for precise number under different conditions

For more detailed specifications regarding AURIX™ TC4x, please refer to the white paper [2].

AURIX™ TC3x MCUs offer PWM resolution up to 3.75 ns, which is sufficient to meet the requirements of most markets. AURIX™ TC4x MCUs introduce a dedicated high-resolution PWM (HRPWM) module that provides a PWM resolution up to 156 ps. This capability is achieved through a digital PLL, ensuring highly accurate and consistent resolution regardless of process, voltage, or temperature variations. This enhanced feature is

designed to support advanced power conversion designs, such as operating switching frequencies at 500 kHz or above.

The practical relevance of HRPWM for OEMs and Tier 1 suppliers depends on the switching frequency range and the associated PWM resolution margin. Therefore, a quantitative assessment is introduced in the following chapter to determine when HRPWM becomes necessary.

3 Quantitative analysis of the necessity for HRPWM with respect to switching frequencies

The PWM resolution requirement can be derived from the effective resolution of the analog-to-digital converter (ADC), which provides the measurement basis for the digital control loop. In typical automotive MCU, a successive-approximation-register (SAR) ADC with 12-bit nominal resolution is commonly used. Considering a total unadjusted error (TUE) of approximately 4 LSBs (2 bits) and a quantization error of 0.5 bit, the resulting effective number of bits (ENOB) is approximately 9.5 bits, as shown in Equation 1.

$$ENOB = 12\ (Resolution) - 2\ (TUE) - 0.5\ (Quantization\ Error) = 9.5\ bits$$

Equation 1 Calculation of Effective number of bits

According to power electronics control theory [3], the PWM resolution should exceed the effective ADC resolution by at least one bit to avoid limit-cycle oscillations at the converter output. Based on the ADC effective resolution derived above, this results in a minimum required PWM resolution of approximately 10.5 bits. Under practical power electronics operating conditions, additional noise, nonlinearity, and measurement uncertainty may further reduce the effective ADC resolution. Therefore, a practical minimum PWM resolution in the range of 10 to 10.5 bits is considered appropriate for the following analysis.

Table 2 AURIX™ TC3x PWM resolution vs switching frequencies

Switching frequency	TC3x @ 300 MHz PWM resolution: 5 ns (GTM @ 200 MHz)			TC3x @ 400 MHz PWM resolution: 3.75 ns (GTM @ 266.66 MHz)		
	Steps	ENOB (log2(steps))	Minimum duty cycle	Steps	ENOB (log2(steps))	Minimum duty cycle
100 kHz	2000	11.0	0.05%	2667	11.4	0.038%
150 kHz	1333.3	10.5	0.08%	1786.7	10.8	0.056%
200 kHz	1000	10.0	0.1%	1333.3	10.5	0.075%
250 kHz	800	9.6	0.13%	1066.7	10.1	0.094%
400 kHz	500	9.0	0.2%	666.7	9.4	0.13%

Table 2 presents a comprehensive analysis of the extent to which AURIX™ TC3x PWM resolution offers sufficient solutions. AURIX™ TC3x 300 MHz variant can sufficiently support switching frequencies up to **200 kHz** and AURIX™ TC3x 400 MHz variant can extend this range up to **250 kHz**. In addition, Table 3 shows that the AURIX™ TC4x, with its integrated HRPWM module, offers more headroom to support higher switching frequencies **above 250 kHz**, potentially extending **beyond 1 MHz**.

Table 3 AURIX™ TC4x PWM resolution vs switching frequencies

Switching frequency	TC4x @ 400 MHz PWM resolution: 2.5 ns (disabling HRPWM)			PWM resolution: 0.5 ns as an example (TC4x support up to 156 ps with HRPWM)		
	Steps	ENOB (log2(steps))	Minimum duty cycle	Steps	ENOB (log2(steps))	Minimum duty cycle
100 kHz	4000	12.0	0.03%	20000	14.3	0.005%
150 kHz	2666.6	11.4	0.04%	13333	13.7	0.007%
200 kHz	2000	11.0	0.05%	10000	13.3	0.01%
250 kHz	1600	10.6	0.06%	8000	13.0	0.0125%
400 kHz	1000	10.0	0.1%	5000	12.3	0.02%

4 AURIX™ TC3x/TC4x modulation solution for single-stage OBC

The essential challenge in single-stage OBC implementations lies in the modulation scheme, particularly for three-phase single-stage OBC topology. This chapter examines the modulation concept for the single-stage OBC shown in Figure 4, which presents one of the most complex topologies regarding modulation schemes. The corresponding implementation approaches are introduced based on both AURIX™ TC3x and TC4x MCUs.

As discussed in Chapter 1, the single-stage converter is increasingly adopted as the preferred OBC topology as illustrated on the left side of Figure 4(a). One possible way to generate the PWM signals for the three-phase single-stage OBC is by implementing the current-based space vector modulation [4].

The right side of Figure 4(a) shows the typical high-frequency transformer current (in orange) and voltage (in purple). A transformer current/voltage cycle within one switching period might consist of 7 current vectors which translate to 6 commutation events. Figure 4(a) - (c) illustrate such commutation events between two consecutive current vectors. Main modulation challenges and requirements are summarized as follows:

- Challenge 1: Since either BDS SiC, BDS GaN or back-to-back SiC must be used, each vector transition requires coordinated commutation of four PWM signals to maintain transformer-current continuity and avoid grid-side short circuits. For example, for the transition from Figure 4(a) (1st current vector) to Figure 4(b) (2nd current vector), SAL1, SAL2 must be turned off and SBL1 and SBL2 must be turned on. For the transition from Figure 4(b) (2nd current vector) to Figure 4(c) (3rd current vector), SBL1, SBL2 must be turned off and SCL1 and SCL2 must be turned on.
- Challenge 2: As illustrated in Figure 5, for each commutation event, two possible switching patterns may be applied. For transition from stage 1 to stage 2 as illustrated in bottom left of Figure 5, the pattern could depend on the corresponding phase-voltage conditions (V_{an}>V_{bn} or V_{an}<V_{bn}) i.e., voltage-based commutation. For transition from stage 2 to stage 3 as illustrated in bottom right of Figure 5, the transformer current polarity could decide the selection of the switching pattern. No universally adopted customer-side solution has yet emerged. Therefore, the MCU implementation must support flexible, real-time switching-pattern selection based on either voltage or current boundary conditions.
- Challenge 3: If an unbalanced three-phase condition occurs, the fourth leg must be activated immediately to compensate for the unbalanced phase. This will add at least two additional commutation events in one switching period. Consequently, it might involve more than three edges within one switching period.

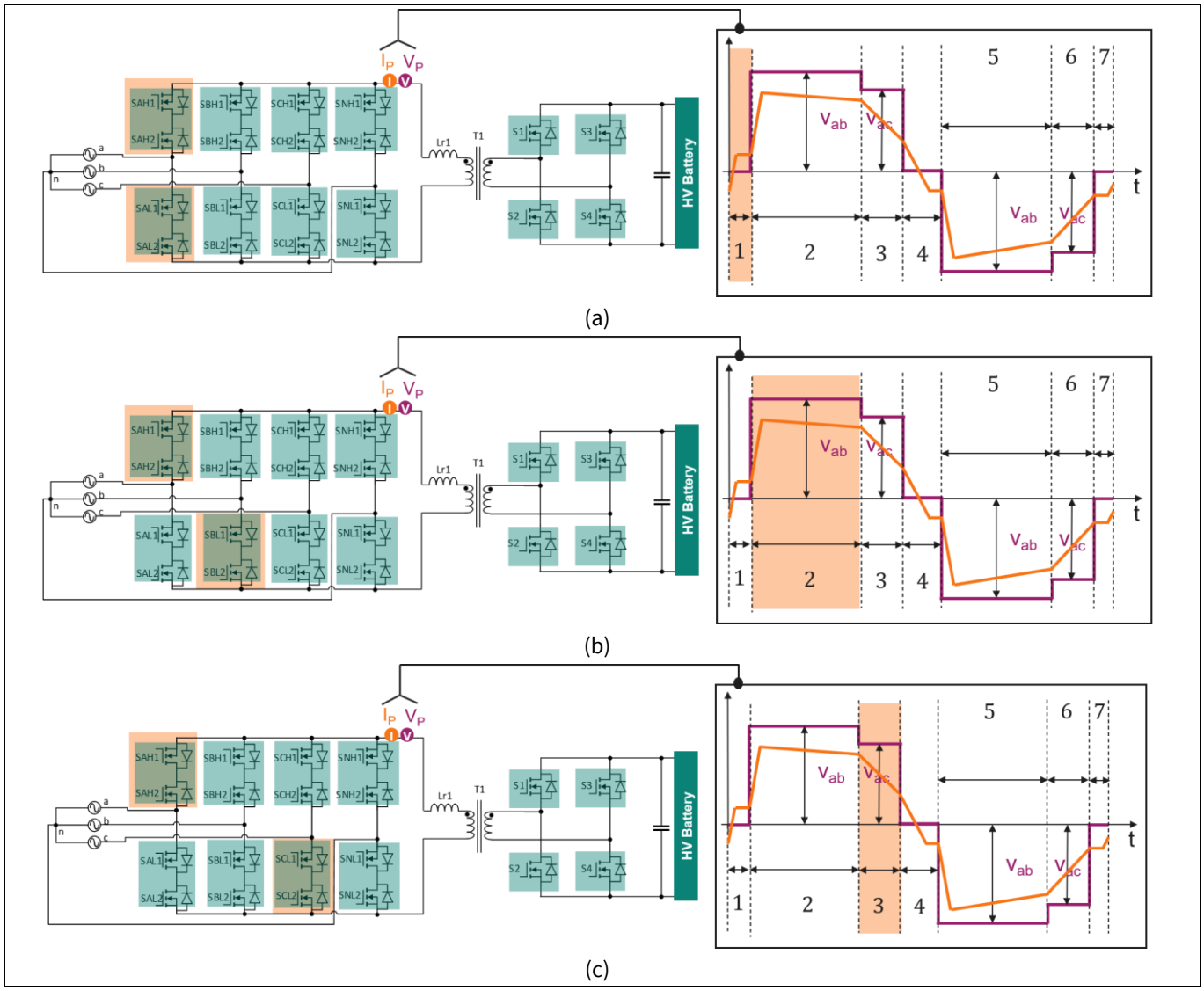

Figure 4 Three-phase single-stage OBC topology and commutation examples between different stages

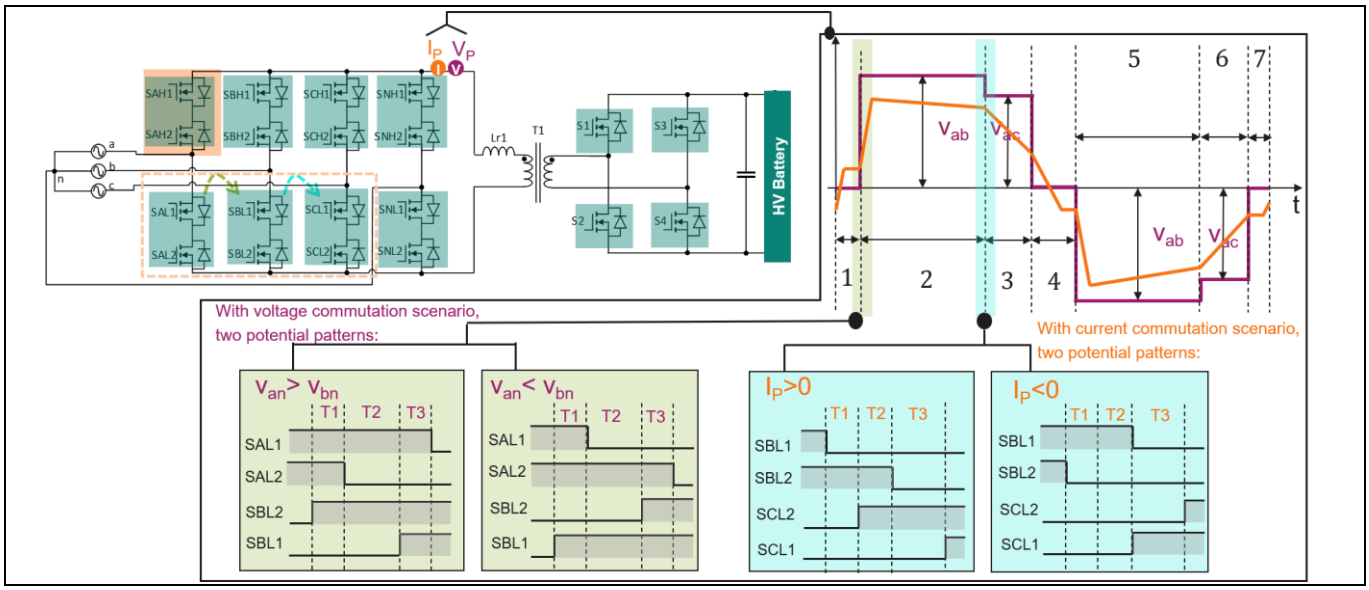

Figure 5 The concept of commutation schemes, bottom left: stage 1 to stage 2 (voltage commutation), bottom right, stage 2 to stage 3 (current commutation)

The solution architectures for modulation scheme generation are illustrated in Figure 6. The three challenges discussed above can be effectively addressed by both AURIX™ TC3x and TC4x MCUs, providing scalable implementation options for single-stage OBC designs.

For switch-pattern selection at each transition, the FCCs process analog input signals and generate boundary flags that determine the appropriate switching pattern. If developers prefer to use external comparators, the corresponding digital boundary flags can be fed directly into GTM. The four-step commutation sequences can be implemented as a fully hardware-based solution. The key architectural difference is that, in AURIX™ TC3x, all shadow-register updates are transferred via the system peripheral bus (SPB). In contrast, AURIX™ TC4x enables shadow-register updates through the dedicated low-latency interface (LLI), thereby reducing update latency and improving real-time responsiveness.

For challenge 3, which is still-evolving system requirements, two implementation paths are available. The multi-channel sequencer (MCS) within the GTM provides an effective and flexible option for handling corner cases. In AURIX™ TC4x, an alternative approach is to utilize the parallel processing unit (PPU), which is directly connected to the LLI. Since the MCS is integrated within the GTM, it can support very low-latency responses for time-critical PWM manipulation.

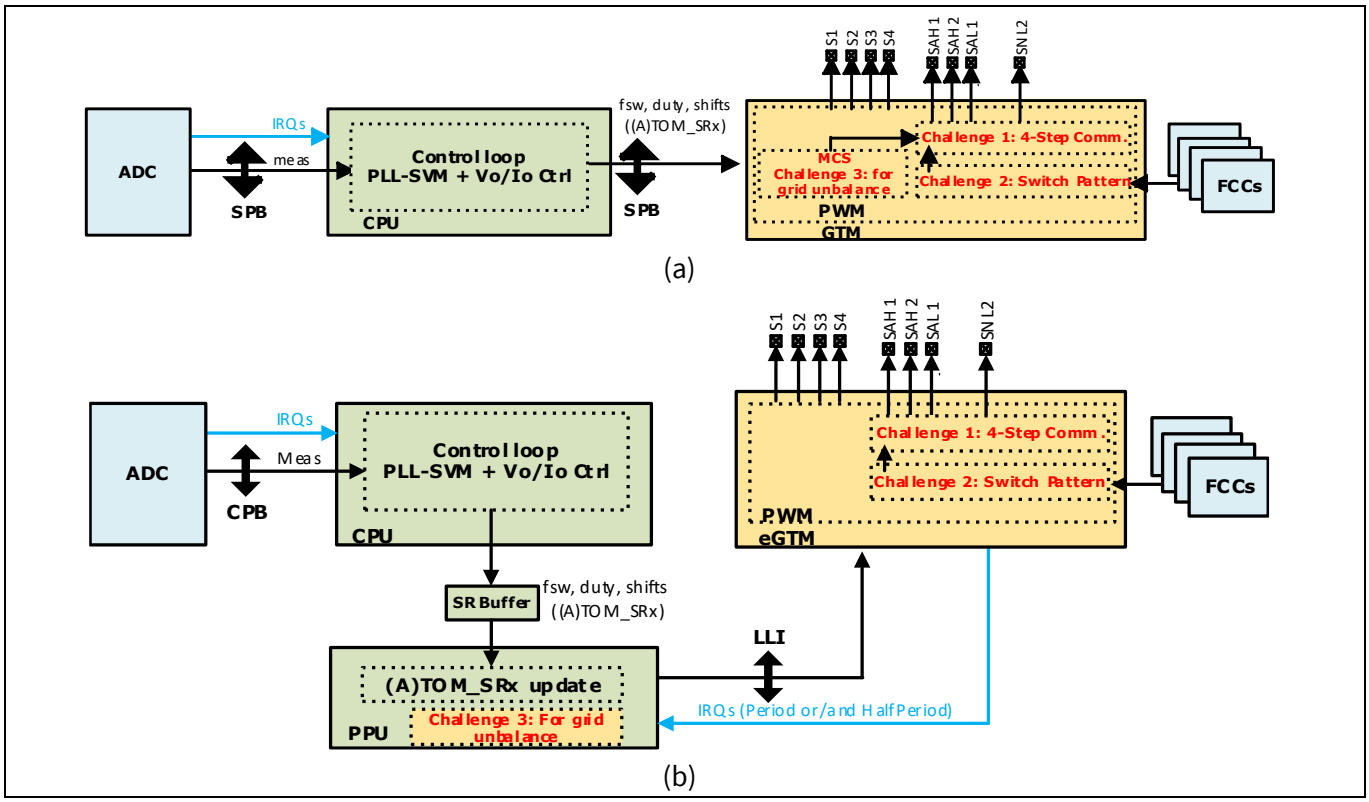

Figure 6 High level implementation architecture based on (a) AURIX™ TC3x, (b) AURIX™ TC4x

It should also be emphasized that the fundamental challenge of this topology is the updating latency. Within one transformer voltage/current period (typically around 10 µs), six or more switching instants may occur. AURIX™ TC3x can address this requirement by using the MCS to manage update latency effectively. AURIX™ TC4x further strengthens this capability through its enhanced bus architecture, making it particularly attractive for demanding high-frequency and highly integrated power-conversion systems. Table 4 shows the qualitative comparison between AURIX™ TC3x and TC4x solutions.

For single-phase single-stage OBC illustrated in Figure 7 (SAH1/2, SAL1/2, SNH1/2, SHL1/2 are in operation from primary side) [5], the three-phase four-step commutation concept can be reused. This enables a common software platform for both three-phase and single-phase operation on the same OBC hardware platform. In

addition, implementing four-step commutation in single-phase operation could be beneficial in some cases e.g., reactive power operation where grid current is not close to zero at grid voltage zero-crossing.

Nevertheless, for a dedicated single-phase single-stage OBC, a simplified modulation scheme can be applied that requires only three-step commutation during the grid-voltage zero-crossing interval. This requirement is less complex than the modulation schemes discussed above; therefore, AURIX™ can fully support this modulation approach.

Table 4 Solution Comparison between AURIX™ TC3x and TC4x MCUs*

		AURIX™ TC3x	AURIX™ TC4x
Challenges 1 and 2: four-step commutation + two patterns decision	Solution	GTM-based full hardware-based solution (2*TOMs + 0.5*ATOM)	eGTM-based full hardware-based solution (1*TOM + 0.5*ATOM+HRPWM)
	Resource consumption	★★	★★★
	Updating latency	★★	★★★
	PWM resolution	★★	★★★
Challenges 3: Unbalanced condition involving 3 – 4 edges within single PWM signal	Solution	MCS	PPU + LLI
	Resource consumption	★★★	★½
	Updating latency	★★★	★★
	Ease of use	★★	★★½

*Rating scale: ★★★ = best relative fit, ★★ = good relative fit, ★ = acceptable relative fit.

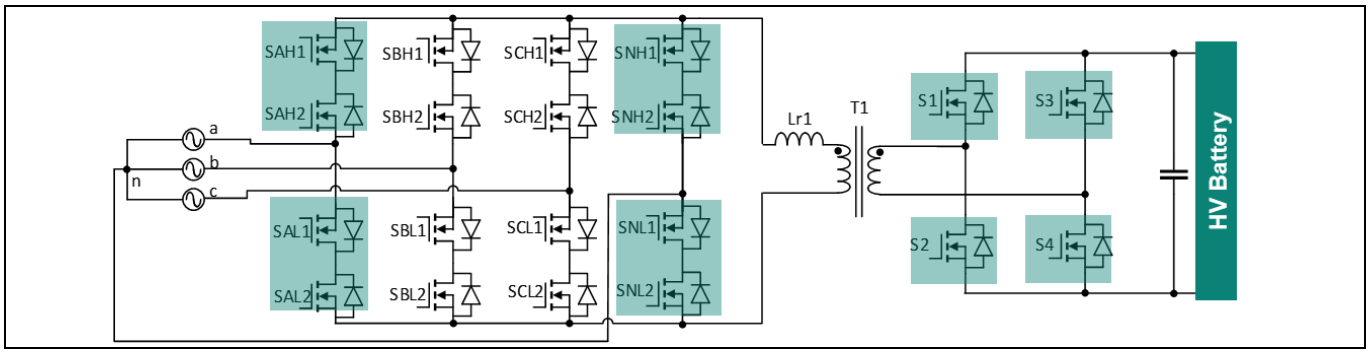

Figure 7 Single-phase single-stage OBC topology (highlighted switches are used for single-phase operation)

5 AURIX™ TC3x/TC4x peak current mode control solution for HV/LV DCDC

For the phase-shift full-bridge topology shown on the left side of Figure 8, the switching frequency is typically maintained at 100 kHz. Due to the frequency-doubling effect, this results in an output current ripple frequency of 200 kHz. Further increasing the switching frequency is challenging from a magnetic design perspective. For example, increasing the switching frequency to 200 kHz would result in an output current ripple frequency of 400 kHz while the output current amplitude is more than 200 A, creating significant challenges for the magnetic design. Therefore, this chapter focuses on PCMC implementation based on a 100 kHz switching frequency.

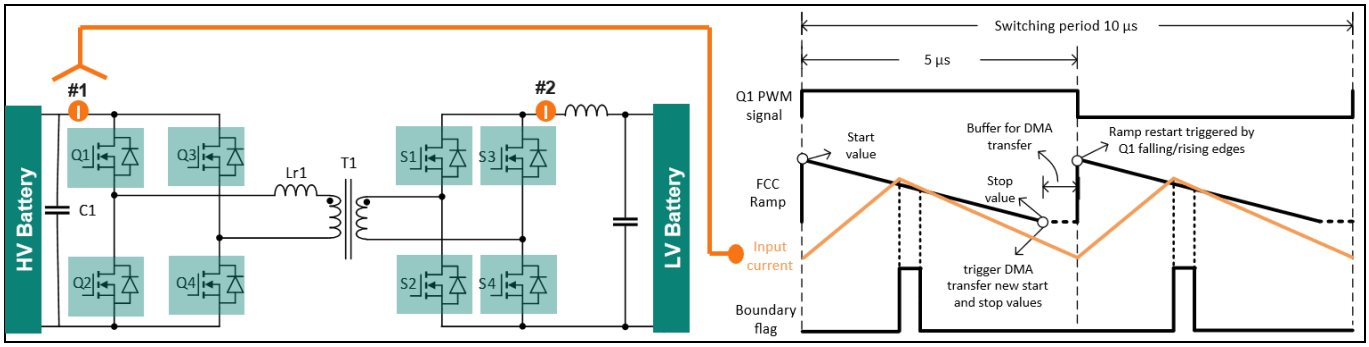

Figure 8 HV/LV DCDC topology with AURIX™ TC3x PCMC diagram

Fast compare comparator (FCC) functionality is integrated into the ADC modules of the AURIX™ TC3x and TC4x MCUs, enabling fast current comparison for PCMC. The corresponding reaction delays for AURIX™ TC3x and TC4x MCUs are summarized in Table 1. PCMC requires slope compensation to avoid subharmonic oscillation. Ramp generation therefore requires a mechanism to restart the ramp and update its initial value for each control cycle. As illustrated on the right side of Figure 8, the ramp configuration in AURIX™ TC3x can support PCMC when the following items are considered:

- The ramp must be configured with both a start value and a stop value. Once the ramp is initiated, it stops only after reaching the configured stop value. Therefore, to ensure that the ramp can be hardware triggered to restart every 5 µs with updated start and stop values, the stop value should be configured such that the ramp counter reaches it before the end of each 5 µs interval, while remaining as close as possible to the interval boundary.
- When the ramp reaches the stop value, it is configured to trigger a DMA transfer to update new start and stop values for the next cycle. The remaining time before the next ramp restart must therefore be sufficient to complete the DMA transfer for just one 32-bit register containing new start and stop values.
- The ramp start value is calculated by the outer control loop. Given the required slope and the available timing budget, the corresponding stop value can then be determined directly.
- The ramp restart is triggered by both the rising and falling edges of the reference PWM signal.
- Ramp slope can be adjusted by changing the step width.

The boundary flag from FCC is then fed to the GTM, where the implementation is identical for both AURIX™ TC3x and TC4x MCUs.

AURIX™ TC4x FCC provides a more flexible ramp restart mechanism. The ramp can be restarted with a hardware trigger, while the new start value can be updated at any time during ramp operation and only becomes effective at the next restart event. This removes the need to align the ramp stop event with the DMA update window and therefore provides greater timing margin. In addition, the ramp increment and decrement steps, as well as the ramp step width, are fully configurable.

When comparing the PCMC implementation options for AURIX™ TC3x and TC4x, the TC3x-based solution may reduce the usable phase-shift range by approximately 4%, implying that the maximum phase shift should be designed below 96%. In contrast, TC4x FCC provides a more efficient ramp restart mechanism, enabling a more direct PCMC implementation. Overall, both AURIX™ TC3x and TC4x MCUs can support PCMC, although they provide different levels of achievable system performance and implementation margin.

In parallel, average current mode control (ACMC) is increasingly being considered as an alternative to PCMC for HV/LV DCDC control. ACMC can eliminate one input-side current-transformer sensor (current sensor #1 in left side of Figure 8), thereby providing a significant opportunity for further cost reduction. The associated trade-off

is a potential reduction in peak system efficiency of approximately 1%, which is considered acceptable in many market applications. Under these conditions, AURIX™ TC3x MCUs should be considered a perfect fit candidate.

6 One complementary offer for the legacy architecture using PSoC™ Control C3

As represented by scenario ② in Figure 3, this option is intended for customers that prefer to retain an established DSP-plus-MCU partitioning rather than migrate directly to a fully integrated ASIL-D MCU-centric architecture. In this context, PSoC™ Control C3 [4] complements the AURIX™ portfolio by supporting legacy platform continuity while enabling selected control-function modernization. It can serve as a DSP candidate for executing control algorithms for the PFC stage and selected HV/HV DCDC control tasks illustrated in Figure 9.

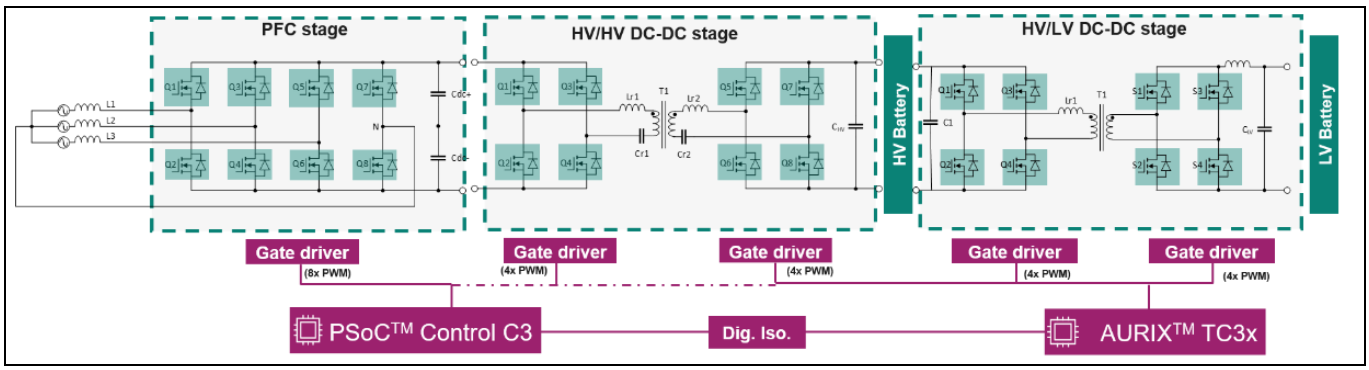

Figure 9 PSoC™ Control C3 +AURIX™ TC36x supporting legacy architecture

7 Summary

Market trends indicate a transition toward functional integration using a single ASIL-D-capable MCU for single-stage OBC and HV/LV DCDC. When selecting an appropriate MCU for such systems, the primary criterion should be the switching-frequency requirement across the dominant operating points. If the switching frequency remains below 250 kHz, AURIX™ TC3x family represents a sufficient solution. If the switching frequency exceeds 250 kHz across most operating points, AURIX™ TC4x family should be considered. This selection principle is largely independent of the converter topology.

For single-stage OBC, key challenges such as four-step commutation, real-time selection between two possible commutation patterns, and multiple commutation events within one switching period can be effectively addressed using the e/GTM in both AURIX™ TC3x and TC4x. For unbalanced grid conditions that require multiple edges within a single PWM channel, the MCS inside the GTM provides an effective implementation option. In addition, the AURIX™ TC4x PPU with LLI enables faster shadow-register updates, thereby supporting higher switching frequencies.

Regarding HV/LV DCDC, both AURIX™ TC3x and TC4x MCUs can support PCMC, while TC4x provides lower FCC reaction time delay and more efficient ramp restart capability. For cost-sensitive design, ACMC is also a viable alternative, as it can reduce sensor cost with only a 1% peak-efficiency trade-off. Therefore, AURIX™ TC4x is preferred for high-performance PCMC implementations, whereas AURIX™ TC3x remains a suitable candidate for cost-optimized PCMC or ACMC solutions.

As a complementary offer, Infineon provides PSoC™ Control C3 as a DSP candidate, enabling customers to maintain the existing architecture based on DSP-plus-MCU while benefiting from Infineon's broader system-level portfolio.

In summary, for OEMs and Tier 1 suppliers targeting higher switching frequencies, tighter timing margins, and maximum implementation flexibility, AURIX™ TC4x family is the preferred candidate. Conversely, for cost-

sensitive mainstream designs in which a limited reduction in peak efficiency is acceptable, AURIX™ TC3x family can still provide sufficient peripherals capabilities, computational performance, ASIL-D functional safety and cyber security support.

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Glossary

MCU	Microcontroller unit
DSP	Digital signal processor
OBC	On-board charger
SPB	System peripheral bus
PWM	Pulse width modulation
DC	Direct current
V2G	Vehicle to grid
ECU	Electronic control unit
PPU	Parallel processing unit
CDSP	Converter digital signal processor
MCS	Multi-channel sequencer
ns	Nanosecond
ps	Picosecond
PVT	Process, voltage, temperature
HRPWM	High-resolution PWM
ADC	Analog-to-digital conversion
SAR	Successive approximation register
LSB	Least significant bit
TUE	Total unadjusted error
ENOB	Effective number of bits
BDS	Bidirectional switches
GTM	Generic timer module
eGTM	Enhanced GTM
PCMC	Peak current mode control
ACMC	Average current mode control
CT	Current transformer
FCC	Fast compare comparator
LLI	Low latency interface
SPB	System peripheral bus
PFC	Power factor correction

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