

Sl. No.	Section	Subsection	Change Description	Current Spec *C content	New Spec *D content	Reason for change	Customer Impact
1	8 Code flash	8.3.1 SROM APIs	Updated description	To execute the SROM APIs, it is recommended to use the core M0+ through inter-processor communication.	To execute the SROM APIs, it is necessary to use the core M0+ through inter-processor communication.	Improvement	None
2	9 Work flash	9.3.2 SROM APIs	Updated description	To execute the SROM APIs, it is recommended to use the core M0+ through inter-processor communication.	To execute the SROM APIs, it is necessary to use the core M0+ through inter-processor communication.	Improvement	None
3	16. Power Supply and Monitoring	16.3.4 Low-voltage-detection (LVD)	Added a note	(none)	Note: When increasing the trip selection bits (PWR_LVD_CTL2.HVLVD1/2_TRIPSEL_HT), the user must increase by one binary unit in 10 µs cycle. Change LVD1 or LVD2 independently, not at the same time.	Added a note	High
4	16. Power Supply and Monitoring	16.3.4 Low-voltage-detection (LVD)	Updated Figure 16-2	+/- of the HVLVD comparator is reversed	Updated +/- of the HVLVD comparator	Correction	Low
5	19. Reset system	19.1.7 Internal system reset	Update	(none)	Note that you must write 0x5FA to the VECTKEY field at the same time you write to the SYSRESETREQ bit of the AIRCR registers; otherwise, the processor ignores the write.	Correction	No
6	20. Watchdog timer	20.3.1 Overview	Updated description	the counter increments to the 32-bit boundary and then wraps around to '0' and counts up.	the counter stops counting.	Updating	No
7	25. Timer, Counter, and PWM	25.2.3 Trigger Inputs	Change the trigger inputs	Table 25-2 shows how the multiplexer should be handled for the input trigger event generation. The TRAVEO™ T2G MCU supports the following input triggers: • Number of specific one-to-one trigger inputs: 3 • Number of general-purpose trigger inputs: 27	Table 25-2 shows how the multiplexer should be handled for the input trigger event generation. The TRAVEO™ T2G cluster MCU supports the following input triggers: • Number of specific one-to-one trigger inputs: 1 • Number of general-purpose trigger inputs: 60	Fixing	Yes
8	25. Timer, Counter, and PWM	Table 25-2. Handling Input Trigger Multiplexers	Change and delete the Input Trigger	(Input Trigger Selection) 2 (Input Trigger) HSIOM column ACT#2 3 4 5 ... 31 HSIOM column ACT#3 PASS (programmable analog subsystem), through 1:1 trigger mux #0, tr_all_cnt_in[0] tr_all_cnt_in[26]	(Input Trigger Selection) 2 (Input Trigger) HSIOM column ACT#2 or PASS (programmable analog subsystem), through 1:1 trigger mux #2 3 4 3 ... 62 HSIOM column ACT#3 PASS (programmable analog subsystem), through 1:1 trigger mux #0, tr_all_cnt_in[0] tr_all_cnt_in[59]	Fixing	Yes
9	25. Timer, Counter, and PWM	Table 25-2. Handling Input Trigger Multiplexers	Change and delete the Input Trigger Source	(Input Trigger Selection) 2 Function" datasheet 3 Function" datasheet 4 tab all counters 5 block. ... 31 block. (Input Trigger Source) Refer to the "Alternate Pin" section in the device Refer to the "Alternate Pin" section in the device Refer to the product sheet "triggersOnetoOne". Not will have this input trigger. Refer to the trigger mux Refer to the trigger mux	(Input Trigger Selection) 2 function pin one-to- one" section in the device datasheet 3 Function" datasheet 4 tab "triggersOnetoOne". Not all counters 3 block in the ... 62 block in the (Input Trigger Source) Refer to the "Alternate assignments" or "Triggers" assignments" or "Triggers" section in the device Refer to the "Alternate Pin" section in the device Refer to the product sheet "triggersOnetoOne". Not will have this input trigger. Refer to the trigger mux device datasheet. Refer to the trigger mux device datasheet.	Fixing	Yes
10	25. Timer, Counter, and PWM	Table 25-2. Handling Input Trigger Multiplexers	Change the note	The input triggers can be generated by different sources. While the general-purpose trigger inputs (tr_all_cnt_in[0] to tr_all_cnt_in[26]) are only from the trigger multiplexer block (see the Trigger Multiplexer chapter on page 503), the one-to-one input triggers can also be generated by external GPIO input pins.	The input triggers can be generated by different sources. While the general-purpose trigger inputs (tr_all_cnt_in[0] to tr_all_cnt_in[59]) are only from the trigger multiplexer block (see the Trigger multiplexer chapter on page 583), the one-to-one input triggers can also be generated by external GPIO input pins.	Fixing	Yes
11	31. Serial memory interface (SMIF)	31.1.2.1 Clocks CLK_IF	Added description	(none)	It is derived from CLK_HFX, see the device specific datasheet for more details.	Updating	No
12	36. Nonvolatile memory programming	System Calls	Updated the note: specific system calls shall not be triggered during non blocking program/erase on Flash Bank0/Bank 1	Note only mentions about ReadSWPU/WriteSWPU	Updated the note to also mention about other affected system calls	Enhancement	Minor
13	36. Nonvolatile memory programming	List of system calls	Removed CM0+, CM4, DAP from the column Normal for system call TransitionToRMA	Support for the bus masters in Normal was mentioned for TransitionToRMA	Removed CM0+, CM4, DAP from the column Normal for TransitionToRMA	Enhancement	No
14	34. Flash Boot	34.2.1.1 Cy_FB_VerifyApplication	Added note	(none)	Note: This function internally enables the power control of crypto engine and configure registers or memories needed to perform authentication of user application. Additionally, the function also disables the power control of crypto engine after an authentication is performed. This means existing configurations related to crypto (for example, configured by HSM software) is overwritten after calling this function and therefore must be handled again after every instance the function is called.	Fixing	No