



002-25800 - TRAVEO(TM) T2G Automotive MCU cluster  
2D family architecture technical reference manual  
Change Log \*E to \*F

Sl. No.	Section	Subsection	Change Description	Current Spec *E content	New Spec *F content	Reason for change	Customer Impact
1	1. Introduction	1.1.2 Communication	Corrected the IEEE certification number	10/100/1000 Mbps Ethernet MAC interfaces with Audio Video Bridging (AVB) and Precision Time Protocol (PTP) support conforming to IEEE-802.3az.	10/100/1000 Mbps Ethernet MAC interfaces with Audio Video Bridging (AVB) and Precision Time Protocol (PTP) support conforming to IEEE-802.1AS.	Fixing	None
2	1. Introduction	1.2,3,9 Ethernet MAC	Corrected the sentences	The input/output frames and flow control are complaint to the Ethernet/IEEE 802.3az standards, and also IEEE-1588 precision-time protocol (PTP). The device supports full-duplex data transport using external PHY devices. The MAC supports glue-free connection to PHYs through IEEE standard MII, RMII, GMII, and RGMII interfaces.	It is compatible with IEEE 802.3 standard. It supports IEEE 802.1AS and 1588 precision clock synchronization protocol. It supports MII, RMII, GMII, and RGMII PHY interfaces. It supports full-duplex data transport using external PHY devices. It supports halfduplex data transport in RMII mode only using external PHY devices.	Fixing	None
3	4 CPU Sub system (CPUSS)	4.6.2.5 ECC Error Injection	Added Note	-	Note: Depending on the application and use case, there may be a need to protect ECC error injection from non-authorized use. For more details, contact Infineon support.	Improvement	None
4	6.4.7 PPU	6.4.7.2 ECC Error Injection	Added Note	-	Note: Depending on the application and use case, there may be a need to protect ECC error injection from non-authorized use. For more details, contact Infineon support.	Improvement	None
5	7 Direct memory access	7.1.6.2 ECC for P-DMA channel configuration SRAMs	Added note	-	Note: Depending on the application and use case there may be a need to protect ECC error injection from non-authorizeduse. For more details, contact Infineon support.	Improvement	None
6	8. Code Flash	8.2.2.5 Code flash ECC Error injection	Added Note	-	Note: Depending on the application and use case, there may be a need to protect ECC error injection from non-authorized use. For more details, contact Infineon support.	Improvement	None
7	8. Code Flash	8.2.2.7 Cache ECC Error injection	Added Note	-	Note: Depending on the application and use case, there may be a need to protect ECC error injection from non-authorized use. For more details, contact Infineon support.	Improvement	None
8	8. Code Flash	8.2.4.1 Dual bank mode and remap functionality Table 8-11	Added Note	-	Note: Access to any code flash banks (in both Single Bank mode and Dual Bank mode), while an SFLASH row is being written, can result in a BUS error.	Improvement	None
9	8. Code Flash	8.3.1 SROM APIs	Updated description	To execute the SROM APIs, it is recommended to use the core M0+ through inter-processor communication.	To execute the SROM APIs, it is necessary to use the core M0+ through inter-processor communication.	Improvement	None
10	9. Work flash	9.2.2.2 Work flash ECC Work flash ECC	Added Note	-	Note: Depending on the application and use case, there may be a need to protect ECC error injection from non-authorized use. For more details, contact Infineon support.	Improvement	None
11	9. Work flash	9.3.2 SROM APIs	Updated description	To execute the following SROM APIs, it is recommended to use the core M0+ through inter-processor communication.	To execute the following SROM APIs, it is necessary to use the core M0+ through inter-processor communication.	Improvement	None
12	10.3 ECC Details	10.3.3 ECC Error Injection	Added Note	-	Note: Depending on the application and use case, there may be a need to protect ECC error injection from non-authorized use. For more details, contact Infineon support.	Improvement	None
13	11.3.4.5 Security Enhancement PPU Configuration in SFlash	Table 11-3	Added TRAVEO T2G Cluster Entry	-	Added TRAVEO™ T2G Cluster Entry items	Specification change	Middle
14	11.3.4.5 Security Enhancement PPU Configuration in SFlash	-	Added Note	-	Note: Depending on the application and use case, there may be a need to protect ECC error injection from non-authorized use. For more details, contact Infineon support	Improvement	None
15	11.4.2 eFuse Bits	Table 11-6	Changed description	Critical Object Hash FACTORY_HASH: SHA-256 SECURE_HASH: SHA-256 SECURE_HASH_ZEROES: SHA-256	Critical Object Hash FACTORY_HASH:SHAKE-128 SECURE_HASH: SHAKE-128 SECURE_HASH_ZEROES: SECURE_HASH	Fixing	None
16	16. Power Supply and Monitoring	3.4	Added a note	-	Note: When increasing the trip selection bits (PWR_LVD_CTL2.HVLVD1/2_TRIPSEL_HT), the user must increase by one binary unit in 10 μs cycle. Change LVD1 or LVD2 independently, not at the same time.	Added a note	High
17	16. Power Supply and Monitoring	3.4	Updated Figure 16-8	+/- of the HVLVD comparator is reversed	Updated +/- of the HVLVD comparator	Correction	Low
18	18 Clocking system	18.2.1 Internal main oscillator (IMO)	Add information	The IMO should not be disabled if it is the source of the clock path feeding high-frequency clock zero (CLK_HF0). CLK_HF0 is the source clock for the CPU. Therefore, if the IMO is in the source path of CLK_HF0, disabling the IMO disables the CPU.	The IMO should not be disabled if it is the source of the clock path feeding high-frequency CLK_HF0 or CLK_HF1. CLK_HF0 is the source clock for the CPU0+ and CLK_HF1 is the source clock for the CPU7. Therefore, if the IMO is in the source path of CLK_HF0 or CLK_HF1, disabling the IMO disables the CPUs.	Add information	None
19	18 Clocking system	18.3.1 PLL without SSCG and Fractional Operation	Add information	18.3.1 PLL without SSCG and Fractional Operation	18.3.1 PLL without SSCG and fractional operation (200-MHz PLL)	Add information	None
20	19. Reset system	19.1.7 Internal system reset	Update	-	Note that you must write 0x5FA to the VECTKEY field at the same time you write to the SYSRESETREQ bit of the AIRCR registers; otherwise, the processor ignores the write.	Correction	None
21	20. Watchdog timer	20.3.1 Overview	Updated description	the counter increments to the 32-bit boundary and then wraps around to '0' and counts up.	the counter stops counting.	Updating	None
22	22.6 Digital Output Driver	Table 22-5	DS_TRM[2:0] 101 111 changed description	101: 40ohm, 1.8-V memory 111: 25ohm, 1.8-V memory	101: 40ohm, 3.3-V memory 111: 25ohm, 3.3-V memory	Correction	None
23	23 Serial Communications Block (SCB)	23.2.4 Clock and Reset Interface	Added clock relationship	-	CLK_PERI>=CLK_SYS(CLK_GR6)=CLK_AHB>=CLK_SCB(PCLK_SCB_CLOCK)	Improvement	None
24	23 Serial Communications Block (SCB)	23.4.5.3 Oversampling and Bit Rate SPI Master Mode	Default value	Note: The SCBx_SPI_CTRL.LATE_MISO_SAMPLE is set to '0' by default.	Note: The SCBx_SPI_CTRL.LATE_MISO_SAMPLE is set to '1' by default.	correction	None
25	23 Serial Communications Block (SCB)	23.6.6.2 Oversampling and Bit Rate	Added description	-	"I2C Master Clock Synchronization" description	Improvement	None



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26	24. CAN FD Controller	24.4.8.4 ECC Error Injection	Added Note	-	Note: Depending on the application and use case, there may be a need to protect ECC error injection from non-authorized use. For more details, contact Infineon support.	Improvement	None
27	25. Timer, Counter, and PWM	Table 25-2. Handling Input Trigger Multiplexers	Change and delete the Input Trigger	(Input Trigger Selection) (Input Trigger) 2 HSIOM columnn ACT#2 3 HSIOM column ACT#3 4 PASS (programmable analog subsystem), through 1:1 trigger mux#0,	(Input Trigger Selection) (Input Trigger) 2 HSIOM column TCx_y_TR0 / TCx_M_y_TR0 / TCx_H_y_TR0 3 HSIOM column TCx_y_TR1 / TCx_M_y_TR1 / TCx_H_y_TR1 4 PASS (programmable analog subsystem), through 1:1 trigger mux #x	Fixing	Yes
28	25. Timer, Counter, and PWM	Table 25-2. Handling Input Trigger Multiplexers	Change and delete the Input Trigger Source	(Input Trigger Selection) (Input Trigger Source) 4 Refer to the product sheet tab "triggersOnetoOne". Not all counters will have this input trigger. 5 Refer to the trigger mux block. ... 31 Refer to the trigger mux block.	(Input Trigger Selection) (Input Trigger Source) 4 Refer to the "Triggers one-to-one" section in the device datasheet. 5 Refer to the trigger mux block in the device datasheet. ... 31 Refer to the trigger mux block in the device datasheet.	Fixing	Yes
29	25. Timer, Counter, and PWM	Table 25-2. Handling Input Trigger Multiplexers	Change the note	The input triggers can be generated by different sources. While the general-purpose trigger inputs (tr_all_cnt_in[0] to tr_all_cnt_in[26]) are only from the trigger multiplexer block (see the Trigger Multiplexer chapter on page 503), the one-to-one input triggers can also be generated by external GPIO input pins.	The input triggers can be generated by different sources. While the general-purpose trigger inputs (tr_all_cnt_in[0] to tr_all_cnt_in[26]) are only from the trigger multiplexer block (see the Trigger Multiplexer chapter on page 583), the one-to-one input triggers can also be generated by external GPIO input pins.	Fixing	No
30	31.Ethernet MAC	31.1.1	Updated standard compliance and RMII half duplex support in supported features	<ul style="list-style-type: none"><li>• Both Full Store and Forward mode and Partial Store and Forward mode for full-duplex operation</li><li>• 10 Mbit/s, 100 Mbit/s, or 1 Gbit/s operation</li><li>• MII, RMII, GMII, and RGMII PHY interface modes</li><li>• OPEN Alliance specified RGMII V2.2</li><li>• 1536 bytes of maximum frame length</li><li>• Three transmit and receive priority queues</li><li>• IEEE Std 802.1Qav – Forwarding and Queuing Enhancements for Time-Sensitive Streams</li><li>• IEEE Std 802.1AS – Timing and Synchronization for Time-Sensitive Application in Bridged LANs</li><li>• IEEE Std 1588 – Precision Time Protocol</li><li>• IEEE Std 802.1Qbb – Priority Based Flow Control</li><li>• 16 of each Screening Type 1 and Type 2 registers</li><li>• IEEE 802.3 Pause frame and MAC PFC priority based pause frame support</li><li>• Receive and transmit IP, TCP, and UDP checksum offload</li><li>• Automatic pad and CRC generation on transmitted frames</li><li>• MDIO interface for PHY management</li><li>• Strict priority, DWRR, or Enhanced Transmission Selection (ETS – 802.1Qaz) on transmit queues</li><li>• Support for 802.3az EEE</li><li>• AHB (32-bit address width, 32-bit data width) or AXI (32-bit address width, 64-bit data width) DMA master interface. See the device-specific datasheet for more information.</li></ul>	<ul style="list-style-type: none"><li>• Both Full Store and Forward mode and Partial Store and Forward mode for full-duplex operation</li><li>• Full Store and Forward mode in half-duplex operation</li><li>• 10 Mbit/s, 100 Mbit/s, or 1 Gbit/s operation</li><li>• MII, RMII, GMII, and RGMII PHY interface modes</li><li>• Full-duplex operation in all interface modes - MII, RMII, GMII and RGMII</li><li>• Half-duplex operation only in RMII mode</li><li>• OPEN Alliance specified RGMII V2.2</li><li>• RMII specification version 1.2 from RMII consortium</li><li>• 1536 bytes of maximum frame length</li><li>• Three transmit and receive priority queues</li><li>• IEEE Std 802.1Qav – Forwarding and Queuing Enhancements for Time-Sensitive Streams</li><li>• IEEE Std 802.1AS – Timing and Synchronization for Time-Sensitive Application in Bridged LANs</li><li>• IEEE Std 1588-2008 – Precision Clock Synchronization Protocol for Networked Measurement and Control Systems</li><li>• IEEE Std 802.1Qbb – Priority Based Flow Control</li><li>• 16 Screening registers (Type 1 and Type 2) for routing incoming traffic to specific receive queues</li><li>• IEEE Std 802.3x - Flow Control in full-duplex operation using Pause frames</li><li>• Half-duplex flow control using backpressure in RMII mode.</li><li>• TCP, UDP, and IP checksum offload engines on both transmit/receive side</li></ul> <ul style="list-style-type: none"><li>• Automatic CRC and pad generation on transmitted frames</li><li>• MDIO interface for PHY management</li><li>• Strict priority, DWRR, or Enhanced Transmission Selection (ETS – 802.1Qaz) on transmit queues</li><li>• Support for 802.3az for Energy Efficient Ethernet.</li><li>• AHB (32-bit address width, 32-bit data width) or AXI (32-bit address width, 64-bit data width) DMA master interface. See the device-specific datasheet for more information.</li></ul>	Added missing information on standard compliance and RMII Half Duplex Operation	High
31	31.Ethernet MAC	Figure 31-1	Updated Block Diagram to include the AHB/AXI Master DMA interface	Block Diagram	Updated Block Diagram	Block diagram was missing the AHB Master information	Low
32	31.Ethernet MAC	31.3.1	Updated description	TX/RX timestamp capture to buffer descriptor entry	TX/RX timestamp capture in TX/RX buffer descriptors	Clear explanation	None
33	31.Ethernet MAC	31.3.1.2	Added additional Note	–	Partial store and forward is available only when the EMAC is configured for full duplex operation and when not using multi buffer frames.	Added note for Partial store and forward mode for Full-duplex operation	Low
34	31.Ethernet MAC	31.3.1.3	Added note	–	For Half-duplex operation always configure the EMAC in Full Store and Forward mode	Added note for missing information Half Duplex operation	Low
35	31.Ethernet MAC	31.3.3	Added description for Half-duplex mode	The MAC transmitter operates in full duplex and transmits frames in accordance with the Ethernet IEEE 802.3 standard.	The MAC transmitter operates in full duplex/half duplex (only in RMII mode) and transmits frames in accordance with the Ethernet IEEE 802.3 standard.	Missing information for RMII Half-Duplex mode	High



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36	31.Ethernet MAC	31.3.3	Added MAC Transmitter operation in Half Duplex mode	In full duplex mode, frames are transmitted immediately. Back-to-back frames are transmitted 96-bit times apart to guarantee the Interpacket Gap.	In full duplex mode, frames are transmitted immediately. Back-to-back frames are transmitted 96-bit times apart to guarantee the Interpacket Gap. In half duplex mode, the transmitter waits for the de-assertion of CRS before transmission. If asserted, the transmitter waits for the CRS to become inactive, and then starts transmission after an Interpacket gap of 96 bit-times. If the collision signal(COL) is asserted during transmission, the transmitter will transmit a jam sequence of 32 bits taken from the data register and then retry transmission after the back-off time has elapsed. If the collision occurs during either the preamble or SFD, then these fields will be completed prior to generation of the jam sequence.	Missing information for RMII Half-Duplex mode	High																														
37	31.Ethernet MAC	31.3.3	Added Half Duplex Flow control operation	–	If the back pressure bit is set in the network control register(ETHx_network_control[8]) in half duplex mode in RMII mode, the transmit block transmits 64 bits of data, which can consist of 16 nibbles of 1011 or in bit rate mode 64 1s, whenever it sees an incoming frame to force a collision. This provides a way of implementing flow control in half duplex mode.	Missing information for RMII Half-Duplex mode	Low																														
38	31.Ethernet MAC	31.3.8	Updated the Register name	Unicast PTP frame recognition is enabled via bit 20 of the ETHx_network_config register.	Unicast PTP frame recognition is enabled via bit 20 of the ETHx_network_control register.	Register name mismatch	Low																														
39	31.Ethernet MAC	31.3.9.2	Description change for PAUSE Frame Transmission	Automatic transmission of pause frames is supported through the transmit pause frame bits of the ETHx_network_control register.	Transmission of pause frames in full-duplex mode is supported through the transmit pause frame bits of the ETHx_network_control register.	Updated description	Low																														
40	31.Ethernet MAC	31.3.9.2	Added note	–	Note: If the MAC is operating in half-duplex mode2 , there will be no transmission of PAUSE frames.	Missing information for RMII Half-Duplex mode	Low																														
41	31.Ethernet MAC	31.3.10.1	Added description for Half-duplex mode	–	If the EMAC is operating in half duplex mode, the pause time counters will not be loaded, but the pause frame received interrupt will still be triggered. To avoid this, it is advised to disable the PAUSE frame interrupts during Half-duplex operation.	Missing information for RMII Half-Duplex mode	Low																														
42	31.Ethernet MAC	31.3.12	Updated description for MDC Clock path	MDC should not toggle faster than 2.5 MHz (minimum period of 400 ns), as defined by the IEEE 802.3 standard. MDC is generated by dividing clk_sys. Three bits in the network configuration register determine by how much pclk should be divided to produce MDC.	MDC should not toggle faster than 2.5 MHz (minimum period of 400 ns), as defined by the IEEE 802.3 standard. MDC is generated by dividing clk_sys. clk_sys is generated from CLK_GR4 (see device specific datasheet for the Clock path for CLK_GR4). Three bits in the network configuration register determine by how much pclk should be divided to produce MDC. clk_sys after the IP is enabled, is given to MDC clock divider as pclk.	Missing information on MDC Clock path with respect to RTRM	Low																														
43	31.Ethernet MAC	Table 31-7	Updated signal name and description in RGMII	<table><tr><td>Signal Name</td><td>Description</td></tr><tr><td>ETHx_TXD</td><td></td></tr><tr><td>ETHx_TX_CTL</td><td>Transmit enable</td></tr><tr><td>ETHx_RXD</td><td></td></tr></table>	Signal Name	Description	ETHx_TXD		ETHx_TX_CTL	Transmit enable	ETHx_RXD		<table><tr><td>Signal Name</td><td>Description</td></tr><tr><td>ETHx_TXD[3:0]</td><td></td></tr><tr><td>ETHx_TX_CTL</td><td>Transmit enable and error signal</td></tr><tr><td>ETHx_RXD[3:0]</td><td></td></tr></table>	Signal Name	Description	ETHx_TXD[3:0]		ETHx_TX_CTL	Transmit enable and error signal	ETHx_RXD[3:0]		Signal description to be matched with RGMIII Specification	None														
Signal Name	Description																																				
ETHx_TXD																																					
ETHx_TX_CTL	Transmit enable																																				
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ETHx_TXD[3:0]																																					
ETHx_TX_CTL	Transmit enable and error signal																																				
ETHx_RXD[3:0]																																					
44	31.Ethernet MAC	31.3.14.3	Added description for RMII Interface	As the name suggests, Reduced Media Independent Interface (RMII) communicates data to PHY through lower number of pins compared to MII. Transmit and received data lines are reduced from four to two, and clock is doubled. The clock source for RMII can be selected either from internal PLL source2 or external high-precision clock through clock line ETHx_REF_CLK; required clock for transmit and receive operations will be generated internally from this reference clock.	As the name suggests, Reduced Media Independent Interface (RMII) communicates data to PHY through lower number of pins compared to MII. Transmit and received data lines are reduced from four to two, and clock is doubled. The clock source for RMII must be routed from GPIO/HSIO through the ETHx_REF_CLK pin. Ethernet MAC supports half-duplex only in RMII mode. The TX_CTL and RX_CTL inputs are used to obtain the carrier sense and collision information inside the MAC layer.	Description for RMII Clock mode was incorrect	High																														
45	31.Ethernet MAC	Table 31-8	Updated table with correct RMII interface signals.	<table><tr><td>Signal Name</td><td>Description</td></tr><tr><td>ETHx_TXD</td><td></td></tr><tr><td>ETHx_TX_CTL</td><td>Transmit enable</td></tr><tr><td>ETHx_RXD</td><td>4 Receive data lines</td></tr><tr><td>ETHx_RX_CTL</td><td>Receive data valid</td></tr><tr><td>ETHx_TX_CLK</td><td>Reference clock to PHY when internal reference clock is selected</td></tr></table>	Signal Name	Description	ETHx_TXD		ETHx_TX_CTL	Transmit enable	ETHx_RXD	4 Receive data lines	ETHx_RX_CTL	Receive data valid	ETHx_TX_CLK	Reference clock to PHY when internal reference clock is selected	<table><tr><td>Signal Name</td><td>Description</td></tr><tr><td>Direction</td><td></td></tr><tr><td>ETHx_TXD[1:0]</td><td></td></tr><tr><td>ETHx_TX_CTL</td><td>Transmit enable</td></tr><tr><td>(TX_EN)</td><td></td></tr><tr><td>ETHx_RXD[1:0]</td><td>2 Receive data lines</td></tr><tr><td>ETHx_RX_ER</td><td></td></tr><tr><td>PHY to MAC</td><td></td></tr><tr><td>ETHx_RX_CTL</td><td>Carrier sense and receive data valid multiplexed (CRSDV)</td></tr></table>	Signal Name	Description	Direction		ETHx_TXD[1:0]		ETHx_TX_CTL	Transmit enable	(TX_EN)		ETHx_RXD[1:0]	2 Receive data lines	ETHx_RX_ER		PHY to MAC		ETHx_RX_CTL	Carrier sense and receive data valid multiplexed (CRSDV)	Incorrect data line description in RMII interface and removed TX_CLK out description in internal mode	Low
Signal Name	Description																																				
ETHx_TXD																																					
ETHx_TX_CTL	Transmit enable																																				
ETHx_RXD	4 Receive data lines																																				
ETHx_RX_CTL	Receive data valid																																				
ETHx_TX_CLK	Reference clock to PHY when internal reference clock is selected																																				
Signal Name	Description																																				
Direction																																					
ETHx_TXD[1:0]																																					
ETHx_TX_CTL	Transmit enable																																				
(TX_EN)																																					
ETHx_RXD[1:0]	2 Receive data lines																																				
ETHx_RX_ER																																					
PHY to MAC																																					
ETHx_RX_CTL	Carrier sense and receive data valid multiplexed (CRSDV)																																				
46	31.Ethernet MAC	31.3.14.3	Removed Note	2. Please check device specific datasheet to know availability of internal reference clock for RMII.	–	RMII supports only external clock for B-H devices.	Low																														





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47	31.Ethernet MAC	31.3.14.4	Updated Clock Sources descriptions	<p>Clock requirements and configurations are different for each interface. Following are the required clocks and source of clocks.</p> <ul style="list-style-type: none"><li>• MII<ul style="list-style-type: none"><li>– Both TX and RX clocks are supplied from external PHY.</li></ul></li><li>• RMII<ul style="list-style-type: none"><li>– Both TX and RX clocks can be supplied from either internal reference clock or from external clock source. 3</li><li>– ETHx_CTL.REFCLK_SRC_SEL must be used to select reference clock source from on-chip system resource or from HSIO.</li></ul></li><li>a) Clock out will be enabled internally when the internal clock source is selected; TX reference clock to PHY can be provided through ETHx_TX_CLK.</li><li>– ETHx_CTL.REFCLK_DIV must be used to divide reference clock and generate required frequency of 50 MHz.</li></ul> <ul style="list-style-type: none"><li>• GMII<ul style="list-style-type: none"><li>– RX clock is supplied from PHY.</li><li>– TX clock source can be selected either from internal clock source or from HSIO.</li><li>– ETHx_CTL.REFCLK_SRC_SEL must be used to select clock source for TX functionality.</li><li>– ETHx_CTL.REFCLK_DIV is used to divide reference clock and to generate required clock of 125 MHz.</li><li>– Clock out will be enabled internally when the internal clock source is selected; TX reference clock to PHY can be provided through ETHx_TX_CLK.</li></ul></li></ul> <p>Note: Use a more precise external clock source than the internal PLL for RGMII and GMII transmit operations.</p>	<p>31.3.14.4 Clock sources for PHY interface</p> <p>Clock requirements and configurations are different for each interface. Following are the required clocks sources for each of them.</p> <ul style="list-style-type: none"><li>• MII<ul style="list-style-type: none"><li>– Both TX and RX clocks are supplied from external PHY.</li></ul></li><li>• RMII<ul style="list-style-type: none"><li>– The reference clock (REF CLK) for RMII must be provided from GPIO/HSIO thorough ETHx_REF_CLK with a clock frequency of 50 MHz. 3</li><li>– ETHx_CTL.REFCLK_SRC_SEL must be used to select reference clock source from GPIO/HSIO.</li><li>– ETHx_CTL.REFCLK_DIV can be used to divide reference clock and generate required frequency of 50 MHz.</li></ul></li><li>• GMII<ul style="list-style-type: none"><li>– RX clock is supplied from PHY.</li><li>– TX clock source can be selected either from internal clock source or from HSIO. 3</li><li>– ETHx_CTL.REFCLK_SRC_SEL must be used select clock source for TX functionality.</li><li>– ETHx_CTL.REFCLK_DIV is used to divide the reference clock to generate required transmit clock of 125 MHz</li><li>– Clock out will be enabled internally when the internal clock source is selected; TX reference clock to PHY can be provided through ETHx_TX_CLK. (see Note)</li></ul></li></ul> <ul style="list-style-type: none"><li>• RGMII<ul style="list-style-type: none"><li>– RX clock is supplied from PHY.</li><li>– TX clock source can be selected either from internal clock source or from HSIO. 3</li><li>– ETHx_CTL.REFCLK_SRC_SEL must be used to select clock source for TX functionality.</li><li>– ETHx_CTL.REFCLK_DIV can be used to divide reference clock to generate required clock of 125 MHz. (see Note)</li><li>– Clock out will be enabled internally and TX clock to PHY can be provided through ETHx_TX_CLK.</li></ul></li></ul> <p>Note: Use a more precise external clock source than the internal PLL for RGMII and GMII transmit operations.</p>	Updated description	Low
48	31.Ethernet MAC	Table 31-10	Updated Clocks to EMAC	–	<p>clk_tsu - TSU clock for TSU timer.clk_tsu is derived from CLK_HF5</p> <p>pclk - MDC clock after MDC clock division, pclk is derived from clk_sys.</p> <p>ref_clk_out - Clock output, usually sent out from ETHx_TX_CLK pin</p>	Information on Clocks to EMAC was missing	Low
49	31.Ethernet MAC	Table 31-11	Added DMA minimum bus frequency requirements for AXI	–	<p>Table 31-11. AXI bus frequency requirements</p> <p>DMA bus width MAC operating speed Minimum AXI frequency</p> <p>64 1 Gbps 65 MHz</p> <p>64 100 Mbps 10 MHz</p> <p>64 10 Mbps 10 MHz</p>	Information on DMA Bus frequency missing in ATRM	Low
50	31.Ethernet MAC	Table 31-12	Added DMA minimum bus frequency requirements for AHB	–	<p>Table 31-12. AHB bus frequency requirements</p> <p>DMA bus width MAC operating speed Minimum AHB frequency</p> <p>32 100 Mbps 15 MHz</p> <p>32 10 Mbps 10 MHz</p>	Information on DMA Bus frequency missing in ATRM	Low
51	31.Ethernet MAC	Table 31-13	Added minimum clock frequency requirements for CLK_SYS and CLK_TSU	–	<p>Table 31-13. Minimum frequency requirements for other clock domains</p> <p>Clock domain Minimum required clock frequency</p> <p>CLK_TSU 5 MHz</p> <p>CLK_SYS 10 MHz</p>	This information is missing in ATRM from BROS	None
52	33 SHDC Host Controller	1	Updated description	3.3-V signal voltage: Default speed (12.5 MB/s at 25 MHz) and high speed (25 MB/s at 50 MHz)	Default speed (12.5 MB/s at 25 MHz) and high speed (25 MB/s at 50 MHz)	Updated description	None
53	33 SHDC Host Controller	2	Updated description	These registers are described in the TRAVEO™ T2G Body Controller High Registers TRM.	These registers are described in the Registers TRM of the respective device.	Updated description	None



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Sl. No.	Section	Subsection	Change Description	Current Spec *E content	New Spec *F content	Reason for change	Customer Impact
54	33 SHDC Host Controller	3.1	Added description	-	<p>Whenever the card clock enable (SDHCx_CORE_CLK_CTRL_R.SD_CLK_EN) is changed the internal TX clock must be running (SDHCx_CORE_CLK_CTRL_R.PLL_ENABLE=1) for that change to propagate. So, if turning off both enables, be sure to first turn off SDHCx_CORE_CLK_CTRL_R.SD_CLK_EN first, wait a few card clock cycles to ensure the gating has occurred, and then turn off SDHCx_CORE_CLK_CTRL_R.PLL_ENABLE. This has an implication when doing SDHCx_CORE_SW_RST.SW_RST_ALL, which resets both bits at the same time, and thus runs into the problem where the card clock will not properly gate. So, in order to properly gate the card clock first clear SDHCx_CORE_CLK_CTRL_R.SD_CLK_EN, wait a few card clock cycles to ensure the gating has occurred, then execute SDHCx_CORE_SW_RST.SW_RST_ALL.</p> <p>When turning on SDHCx_CORE_CLK_CTRL_R.SD_CLK_EN, it is OK to set it simultaneously with SDHCx_CORE_CLK_CTRL_R.PLL_ENABLE. But, whether it's sequenced or not, SDHCx_CORE_CLK_CTRL_R.PLL_ENABLE must be on for SDHCx_CORE_CLK_CTRL_R.SD_CLK_EN to take effect in ungating the card clock. When you write the SDHCx_CORE_CLK_CTRL_R.SC_CLK_EN bit, the first card clock edge occurs on the third internal clock cycle. So wait three card clock periods before enacting any commands on the interface to ensure the card clock is properly ungated.</p>	Added description	Low
55	38. LPDDR4	38.2 Feature not supported	Added note	-	Non-default values modes in MR0 are not supported.	Added note	None
56	38. LPDDR4	38.6.8.1 (LPDDR4_WRAPPER) QoS emulation, PLL setting and module enable	Updated PLL configuration figure	-	Updated Figure 38-8 Example shows a PLL800 configuration for LPDDR4 clocked with 800MHz with an 8MHz crystal	Updated figure	None
57	38. LPDDR4	38.6.8.2.2 Programmable features	Updates user command table	-	Updates Table 38-8. Describes valid user commands which can be issued to the controller: USER_CMD_PHYOPE USER_CMD_PHYOPX	Updated table	None
58	38. LPDDR4	38.6.8.2.2 Programmable features	Updates memory controller state diagram	-	Updated Figure 38-9. Memory controller state diagram, includes the PHYOP states in the state diagram. PHYOPX and PHYOPE	Updated figure	None
59	38. LPDDR4	38.6.8.2.2 Programmable features	Updated the register description value in Table 38-16. Latency priority setting in LPDDR40_LPDDR4_CORE_RTCFG0_RTxx registers	ARQ_LAT_BARRIER- 0 ÷ 255 AWQ_LAT_BARRIER- 0 ÷ 255	ARQ_LAT_BARRIER- 0: Latency barrier is disabled , even if ARQ_LAT_BARRIER_EN is one 1 ÷ 255 AWQ_LAT_BARRIER- 0: Latency barrier is disabled , even if AWQ_LAT_BARRIER_EN is one 1 ÷ 255	Update table	None
60	38. LPDDR4	38.6.8 Configuration	Updated Table 38-22. LPDDR40_LPDDR4_CORE_POM: PHY operation mode register	-	REL_REFEN shall be always set to 1. It enables the refresh during training or reload process DLL_UPD_PERIODIC shall be always set to 1. It enbales the DLL update during the refresh.	Update table	None
61	38. LPDDR4	38.6.8 Configuration	Added PHY Operation section	-	Added additional section PHY Operation, which includes steps to switch to PHY opertaion mode during normal operation.	Added section	None
62	38. LPDDR4	38.6 Functional description	Added new section	-	Added section 38.6.9 Software-aided training 38.6.9.1 (AXI_PERF_CNT) AXI performance counters 38.6.9.2 (EMPU) External memory protection unit	Added section	None
63	38. LPDDR4	38.9 Register description	Added new registers	-	Updated registers in Table 38-41. LPDDR4 registers Added registers: LPDDR40_LPDDR4_CORE_DMCTL1 LPDDR40_LPDDR4_CORE_AUTO_GT Removed registers: LPDDR40_LPDDR4_CORE_BISTSTT0 LPDDR40_LPDDR4_CORE_BISTSTT1 LPDDR40_LPDDR4_CORE_DDRBISTSTT_CH0 LPDDR40_LPDDR4_CORE_DDRBISTSTT_CH1 LPDDR40_LPDDR4_CORE_PBSR LPDDR40_LPDDR4_CORE_BISTM1_CH0 LPDDR40_LPDDR4_CORE_BISTM1_CH1 LPDDR40_LPDDR4_CORE_BISTM2_CH0 LPDDR40_LPDDR4_CORE_BISTM2_CH1 LPDDR40_LPDDR4_CORE_BISTM3_CH0 LPDDR40_LPDDR4_CORE_BISTM3_CH1 LPDDR40_LPDDR4_CORE_BISTM4_CH0 LPDDR40_LPDDR4_CORE_BISTM4_CH1 LPDDR40_LPDDR4_CORE_BISTM5_CH0 LPDDR40_LPDDR4_CORE_BISTM5_CH1 LPDDR40_LPDDR4_CORE_BISTM6_CH0 LPDDR40_LPDDR4_CORE_BISTM6_CH1 LPDDR40_LPDDR4_CORE_BISTM7_CH0 LPDDR40_LPDDR4_CORE_BISTM7_CH1 LPDDR40_LPDDR4_CORE_BISTM8_CH0 LPDDR40_LPDDR4_CORE_BISTM8_CH1 LPDDR40_LPDDR4_CORE_BISTM9_CH0 LPDDR40_LPDDR4_CORE_BISTM9_CH1 LPDDR40_LPDDR4_CORE_BISTM10_CH0 LPDDR40_LPDDR4_CORE_BISTM10_CH1	Added section	None



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					LPDDR40_LPDDR4_CORE_BISTM11_CH0 LPDDR40_LPDDR4_CORE_BISTM11_CH1 LPDDR40_LPDDR4_CORE_BISTM12_CH0 LPDDR40_LPDDR4_CORE_BISTM12_CH1 LPDDR40_LPDDR4_CORE_BISTM13_CH0 LPDDR40_LPDDR4_CORE_BISTM13_CH1 LPDDR40_LPDDR4_CORE_BISTM14_CH0 LPDDR40_LPDDR4_CORE_BISTM14_CH1 LPDDR40_LPDDR4_CORE_BISTM15_CH0 LPDDR40_LPDDR4_CORE_BISTM15_CH1		
64	41. Non-Volatile Memory Programming	System Calls	Updated the note: specific system calls shall not be triggered during non blocking program/erase on Flash Bank0/Bank 1	Note only mentions about Bank 0 Note only mentions about ReadSWPU/WriteSWPU	Updated the note to also mention about Bank 1 Added other affected system calls	enhancement	Yes, Minor
65	41. Non-Volatile Memory Programming	Direct Flash Calls for Second Flash Controller in CYT6BJ devices	Added a note that RemapFmAddr_Ext() shall be called before FmECT_EraseSector_Ext or FmECT_ProgramWord_Ext functions	-	Added the note	enhancement	Yes
66	41. Non-Volatile Memory Programming	Checksum2/ComputeBasicHash2	Added a note that Checksum2 and ComputeBasicHash2 shall not be called on the same bank where active program or erase is ongoing.	-	Added the note	enhancement	None
67	41. Non-Volatile Memory Programming	List of system calls	Removed CM0+, CM7_0, CM7_1, CM7_2, CM7_3, DAP from the column Normal for system call TransitionToRMA	Support for the bus masters in Normal was mentioned for TransitionToRMA	Removed CM0+, CM7_0, CM7_1, CM7_2, CM7_3, DAP from the column Normal for TransitionToRMA	enhancement	None
68	41. Non-Volatile Memory Programming	Checksum2	Added a note on how to specify Ext#0 and Ext#1 code flash regions with this API.	-	Added the note	enhancement	None
69	41. Non-Volatile Memory Programming	FmECT_ProgramWord_Ext	Explained the usage of parameter cWidth in more clarity and mentioned that the parameter is not used for work flash	-	Added the details	enhancement	None
70	41. Non-Volatile Memory Programming	BlankCheckMain_Ext	Added a note that If INumWords is less than 1, then BlankCheckMain_Ext returns SUCCESS which means given region is blank	-	Added the note	enhancement	None
71	41. Non-Volatile Memory Programming	BlankCheckWork_Ext	Added a note that If INumWords is less than 1, then BlankCheckWork_Ext returns SUCCESS which means given region is blank	-	Added the note	enhancement	None
72	42. Flash Boot	42.2.1.1 Cy_FB_VerifyApplication	Added note	-	Note: This function internally enables the power control of crypto engine and configure registers or memories needed to perform authentication of user application. Additionally, the function also disables the power control of crypto engine after an authentication is performed. This means existing configurations related to crypto (for example, configured by HSM software) is overwritten after calling this function and therefore must be handled again after every instance the function is called.	Fixing	None