Sl. No.	Section	Subsection	Change Description	Current Spec *J content	New Spec *K content	Reason for change	Customer Impact
1	7 Direct memory access	7.1.6 P-DMA controller design	Added note	None	To achieve higher throughput, it is recommended to enable the bufferable channel access using register bit DWx_CH_STRUCTx_CH_CTL.B, this indicates an AMBA bridge that a write transaction can complete without waiting for the destination to accept the write transaction data. The SMPU configuration for DWx can be set to higher priority to achieve more performance from DWx using register bit PROT_SMPU_MSx_CTL.PRIO.	Add information	None
2	13 Device security	13.2.1 Life-cycle stages	Added note	None	Note: To facilitate a smooth transition to the RMA life cycle stage in mass-produced products, customers are required to implement the necessary software. Without this implementation, Infineon is unable to perform a thorough analysis. For further information, refer to the AN228680 - Secure system configuration in TRAVEO T2G family application note, which provides guidance on secure system configuration in the TRAVEO™ T2G family.	Add information	None
3	15 Fault subsystem	15.2 Fault and reset	Added note	None	Note: Fault structure 0 cannot be used by user application to capture data through a reset as ROM boot initializes fault structure 0 to capture potential fault sources during boot.	Add information	Yes
4	18 Clocking system	18.2.2.1 ECO trimming	Added note	None	The setting value of GTRIM is determined by the calculated gm as shown in Table 18-2, and the negative resistance value is determined by it. However, depending on the GTRIM boundary and board environment, the expected negative resistance value may not be obtained. To ensure that the expected negative resistance value is achieved, select a GTRIM of the next higher rank.	Add information	None
5	18 Clocking system	18.5.5 CLK_GR	Added note	None	The clock source of CLK_GR is CLK_PERI or CLK_HF. For the connection relationship between CLK_GR and the source clock, see the clock diagram in the datasheet. Also see AN220208 - Clock configuration setup in TRAVEO™ T2G body entry family.	Add information	None
6	21. Real-time clock	21.6.2 Slew rate control	Added description for Consideration RTC busy status flag behavior	None	Consideration RTC busy status flag behavior RTC busy status flag (BACKUP_STATUS.RTC_BUSY register bit) is abnormally stuck at HIGH even after configuring the RTC user registers and BACKUP_RTC_RW.WRITE register bit is cleared by the software. Therefore, use the following software workaround: 1. If BACKUP_STATUS.RTC_BUSY flag is set, then run the following dummy write sequence 2. Start the sequence for maximum 8 retries ('retryCount') and start with 1 a) Write '1' to BACKUP_RTC_RW.WRITE register for 'retryCount' times b) Write '0' to BACKIP_RTC_RW.WRITE register c) Wait for 6 CLK_LF cycles (ILO0 or WCO) d) If BACKUP_STATUS.RTC_BUSY flag is '0', exit the loop e) If 'retryCount' reaches to '8', then handle this error according to user system requirement for failure case unrelated to this stuck issue (e.g. write '1' to BACKUP_RESET.RESET register) else run dummy write sequence from "a". Figure 21-2. RTC software workaround flow chart	Workaround for errata [242] RTC busy status bit stuck issue	Yes
7	22.6 Digital Output Driver	21.6.2 Slew rate control	Updated description	None	Another extension configuration register (GPIO_PRTx_CFG_SLEW_EXT) can be used to have a variable slew rate. When set to all 0s, it will have the fastest slew rate and slowest slew rate when configured to all 1s. By configuring to other value in between, the slew rate of the pin can be further varied as per requirements. The default of this register is all 0s. Note that this is only a extension register and depends on the setting in CFG_OUT register.	Improvement	Yes
8	22.6 Digital Output Driver	21.6.2 Slew rate control	Added Note	None	Note: The extension registers GPIO_PRTx_CFG_SLEW_EXT is available only for the higher variants of the TRAVEO™ T2G family - Body High and Cluster family of devices.	Improvement	Yes
9	22.6 Digital Output Driver	22.6.2 Slew rate control Table 22-2. Table 22-3. Table 22-4. Table 22-5. Table 22-6. Table 22-7.	Added Note	None	Note: Example use cases are an indication only. The drive configuration can be optimized with the help of simulation on PCB level based on IBIS model.	Improvement	None
10	33. Non-Volatile Memory Programming	33.4.22 SoftReset Table 33-79 Table 33-80	Had a typo for bits [23:8]. These bits are unused by the API. Had a typo that these bits define an eFuse address	Bits [23:8] | Value in the range [0,511] | eFuse address	(Removed "Bits [23:8] | Value in the range [0,511] | eFuse address")	Fixing	No
11	33. Non-Volatile Memory Programming	33.4.14 ProgramRow	Added two new notes - first note on behavior of ProgramRow when invoked on non-erased pages with BlankCheck disabled. And second note on behavior when SRAM_SCRATCH_DATA_ADDR ends up in last available SRAM word	None	Note: The ProgramRow function will not return an error if the requested flash page is not in the erased state and blank check is disabled. In such cases, it is the user's responsibility to ensure that the page is erased or that the new data is identical to the data already written to the page. Failure to do so may result in corrupted flash contents and the generation of ECC errors during reading Note: If the SRAM_SCRATCH_DATA_ADDR for ProgramRow ends in the last available SRAM word, an error (0xF0000013, invalid argument location) will be returned. To avoid this issue, it is recommended to avoid using the last word of available SRAM for passing the SRAM_SCRATCH_DATA_ADDR.	improvement	Yes, Minor

12	33. Non-Volatile Memory Programming	33.4.15 ProgramWorkFlash	Added a note on behavior of ProgramWorkflash when SRAM_SCRATCH_DATA_ADDR ends up in last available SRAM word	None	Note: If the SRAM_SCRATCH_DATA_ADDR for ProgramWorkFlash ends in the last available SRAM word, an error (0xF0000013, invalid argument location) will be returned. To avoid this issue, it is recommended to avoid using the last word of available SRAM for passing the SRAM_SCRATCH_DATA_ADDR.	improvement	Yes, Minor
13	33. Non-Volatile Memory Programming	33.5 System Call Status Table 33-94	Updated description of error code 0xF2000000	Status Code | Description 0xF2000000 | CRC8 of the eFuse group failed.The computed CRC is OR'd with this status	Status Code | Description 0xF2000000 | Number of zeroes stored in efuse does not match to computed number	improvement	No
14	34. Flash Boot	34.2.1.1 Cy_FB_VerifyApplication	Added new note	None	Note: It is the customer's responsibility on executing this API on the CM4/7 and IFX does not guarantee it's operation as the function was designed for the secure core (CM0+).	improvement	No
15	34. Flash Boot	34.3.3 Flash boot flow Table 38-7	Added offset "0xF4, 0xF8"	None	[Offset: 0xF4, TOC2_SAFETY_UPDATES_MARKER] When marker is set to 0x4E454343 that means "N ECC" key word the FW performs an additional check of a user application for NC ECC errors. This field is valid in flash boot version 3.1.0.602 and later [Offset: 0xF8, TOC2_SAFETY_CONFIG_FLAG] Configuration field for NC ECC Check. See 38.3.4.4 "Additional safety features and the second (backup) application" for more details	Enhancement	Yes, Minor
16	34. Flash Boot	34.3.4.4 Additional safety features and the second (backup) application	Added new section	None	(Added new section) 34.3.4.4 Additional safety features and the second (backup) application	Enhancement	Yes, Minor