# TRAVEO™ T2G Automotive MCU: TVII-B-H-8M body controller high registers

## Reference manual

## About this document

### Scope and purpose

The TRAVEO™ T2G body controller high registers reference manual provides reference information for registers and contains respective programming details.

### Intended audience

This manual is for system designer and programmers who are designing or programming using TVII-B-H-8M parts.

# Definitions

## Register Permission

The following table lists the register permission based on protection context and priviledges.

| Permission | Description |
|---|---|
| READ | User mode = Read access, privilege mode = Read access, Non-secure = yes |
| PRIVILEGE - WRITE | User mode = Read access, privilege mode = Read and Write access, Non-secure = yes |
| NO-ACCESS | User mode = No access, Privilege mode = No access, Non-secure = yes |
| SECURE - READ | User mode = Read access, Privilege mode = Read access, Non-secure = No |
| FULL | Read and Write access in all modes, Non-secure = yes |

## Software Access

The following table lists the behavior of registers, on various Software Read/Write Accesses.

| SW Access | HW Access | Software Reads Register | Software Writes Register | Software Description |
|---|---|---|---|---|
| R | any | Register contents | Ignored | Software read-only |
| RW | any | Register contents | Register takes data written | Software read and write |
| RW1S | any | Register contents | Every bit is set upon writing 1 | Software read and write 1 to set |
| RW0S | any | Register contents | Every bit is set upon writing 0 | Software read and write 0 to set |
| RW1C | any | Register contents | Every bit is cleared upon writing 1 | Software read and write 1 to clear |
| RW0C | any | Register contents | Every bit is cleared upon writing 0 | Software read and write 0 to clear |
| RW1SC | any | NA | NA | Illegal |
| RW0SC | any | NA | NA | Illegal |
| W | any | Zero | Register takes data written | Software write only |
| W1S | any | Zero | Every bit is set upon writing 1 | Software write 1 to set (no read) |
| W0S | any | Zero | Every bit is set upon writing 0 | Software write 0 to set (no read) |
| W1C | any | Zero | Every bit is cleared upon writing 1 | Software write 1 to clear (no read) |
| W0C | any | Zero | Every bit is cleared upon writing 0 | Software write 0 to clear (no read) |
| W1SC | any | NA | NA | Illegal |
| W0SC | any | NA | NA | Illegal |
| A | any | NA | NA | Illegal |

## Hardware Access

The following table lists the behavior of registers, on various Hardware Read/Write Accesses.

| HW Access | SW Access | Hardware Description |
|---|---|---|
| any | R | Hardware read only |
| any | RW | Hardware read and write |
| any | RW1S | Hardware read and set |
| any | RW0S | Hardware read and set |
| any | RW1C | Hardware read and clear |
| any | RW0C | Hardware read and clear |
| any | RW1SC | Hardware read and set/clear |
| any | RW0SC | Hardware read and set/clear |
| any | W | Write access only |
| any | W1S | Hardware set |
| any | W0S | Hardware set |
| any | W1C | Hardware clear |
| any | W0C | Hardware clear |
| any | W1SC | Hardware set/clear |
| any | W0SC | Hardware set/clear |
| R | A | Not supported |
| RW | A | Hardware read and write |
| RW1S | A | Hardware read and set |
| RW0S | A | Hardware read and set |
| RW1C | A | Hardware read and clear |
| RW0C | A | Hardware read and clear |
| RW1SC | A | Not supported |
| RW0SC | A | Not supported |
| W | A | Not supported |
| W1S | A | Not supported |
| W0S | A | Not supported |
| W1C | A | Not supported |
| W0C | A | Not supported |
| W1SC | A | Not supported |
| W0SC | A | Not supported |

## Core, Bus and Memory Access

The Cortex-M7 CPUSS uses AHB-Lite also for the system interconnect. Most of the IPs are compliant to the AHB-Lite protocol.

The AHB-Lite protocol is little endian; the least significant byte of a word is mapped onto the word's lowest byte address IPs use a bus data width of 32 bit.

This allows for byte (8-bit), halfword (16-bit) and word (32-bit) transfers. We distinguish two types of transfer types:
- MMIO registers: These registers are typically used for IP control and status information. Unless otherwise noted, transfers to these registers must be 32-bit transfers; any other transfer size generates an AHB-Lite bus error. An IP's MMIO registers do not necessarily fully occupy a consecutive memory region; i.e. holes may be present in the region
- Memory structures: This includes generic memory structures, such as system FLASH, system RAM and system ROM, but also IP specific memory structures. Transfer to these memory structures may be 8-bit, 16-bit or 32-bit transfers; any other transfer size generates an AHB-Lite bus error. A memory structure fully occupies a consecutive memory region; i.e. no holes are present in the memory structure region

A bus slave memory region may contain both MMIO registers and zero or more memory structures. Gaps might exist in the bus slave's memory region, either due to gaps in the MMIO memory region or gaps between the MMIO and memory structure region(s)

Gaps in the address space are reserved. Do not access these gaps, if accessed can result in Hard faults or BUS ERROR depending on which bus segment or a peripheral an address space is allocated to.

## List of Partnumber

This TRM is valid for the following part numbers.

| MPN | Package | Code Flash(KB) | Work Flash(KB) | SRAM(KB) |
|---|---|---|---|---|
| CYT4BF8CES | 176-TEQFP | 8384 | 256 | 1024 |
| CYT4BF8CEE | 176-TEQFP | 8384 | 256 | 1024 |
| CYT4A0M1BE | 176-TEQFP | 8384 | 256 | 1024 |
| CYT4BF8DES | 176-TEQFP | 8384 | 256 | 1024 |
| CYT4BF8DEE | 176-TEQFP | 8384 | 256 | 1024 |
| CYT4BF8CDS | 176-TEQFP | 8384 | 256 | 1024 |
| CYT4A0M14S | 176-TEQFP | 8384 | 256 | 1024 |
| CYT4BF8CDE | 176-TEQFP | 8384 | 256 | 1024 |
| CYT4A0M14E | 176-TEQFP | 8384 | 256 | 1024 |
| CYT4BF8CXE | 176-TEQFP | 8384 | 256 | 1024 |
| CYT4BF8DDS | 176-TEQFP | 8384 | 256 | 1024 |
| CYT4BF8DDE | 176-TEQFP | 8384 | 256 | 1024 |
| CYT4BFBCJS | 272-BGA | 8384 | 256 | 1024 |
| CYT4BFBCJE | 272-BGA | 8384 | 256 | 1024 |
| CYT4A0M1AE | 272-BGA | 8384 | 256 | 1024 |
| CYT4BFBDJS | 272-BGA | 8384 | 256 | 1024 |
| CYT4BFBDJE | 272-BGA | 8384 | 256 | 1024 |
| CYT4BFBCHS | 272-BGA | 8384 | 256 | 1024 |
| CYT4A0M15S | 272-BGA | 8384 | 256 | 1024 |
| CYT4BFBCHE | 272-BGA | 8384 | 256 | 1024 |
| CYT4A0M15E | 272-BGA | 8384 | 256 | 1024 |
| CYT4BFBCXE | 272-BGA | 8384 | 256 | 1024 |
| CYT4BFBDHS | 272-BGA | 8384 | 256 | 1024 |
| CYT4BFBDHE | 272-BGA | 8384 | 256 | 1024 |
| CYT4BFCCJS | 320-BGA | 8384 | 256 | 1024 |
| CYT4BFCCJE | 320-BGA | 8384 | 256 | 1024 |
| CYT4BFCDJS | 320-BGA | 8384 | 256 | 1024 |
| CYT4BFCDJE | 320-BGA | 8384 | 256 | 1024 |
| CYT4BFCCHS | 320-BGA | 8384 | 256 | 1024 |
| CYT4A0M16S | 320-BGA | 8384 | 256 | 1024 |
| CYT4BFCCHE | 320-BGA | 8384 | 256 | 1024 |
| CYT4A0M16E | 320-BGA | 8384 | 256 | 1024 |
| CYT4BFCCXE | 320-BGA | 8384 | 256 | 1024 |
| CYT4BFCDHS | 320-BGA | 8384 | 256 | 1024 |
| CYT4BFCDHE | 320-BGA | 8384 | 256 | 1024 |
| CYT4A0100S | 176-TEQFP-OPB | 8384 | 256 | 1024 |
| CYT4BFPSVA | 320-BGA | 8384 | 256 | 1024 |

# Memory mapping

| MMIO | IP | Address | Description |
|---|---|---|---|
| MMIO0 | PERI | 0x40000000 | Peripheral interconnect |
| | PERI_MS | 0x40020000 | Peripheral interconnect, master interface |
| | PERI_PCLK | 0x40040000 | Peripheral PCLK groups |
| MMIO1 | CRYPTO | 0x40100000 | Cryptography component |
| MMIO2 | CPUSS | 0x40200000 | CPU subsystem (CPUSS) |
| | FAULT | 0x40210000 | Fault structures |
| | IPC | 0x40220000 | IPC |
| | PROT | 0x40230000 | Protection |
| | FLASHC | 0x40240000 | Flash controller |
| | SRSS | 0x40260000 | SRSS Core Registers (ver3) |
| | BACKUP | 0x40270000 | SRSS Backup Domain (ver3) |
| | DW 0 | 0x40280000 | Datawire Controller |
| | DW 1 | 0x40290000 | Datawire Controller |
| | DMAC | 0x402a0000 | DMAC |
| | EFUSE | 0x402c0000 | EFUSE MXS40 registers |
| | EFUSE_DATA | 0x402c0800 | eFUSE memory |
| MMIO3 | HSIOM | 0x40300000 | High Speed IO Matrix (HSIOM) |
| | GPIO | 0x40310000 | GPIO port control/configuration |
| | SMARTIO | 0x40320000 | Programmable IO configuration |
| | TCPWM 0 | 0x40380000 | Timer/Counter/PWM |
| | EVTGEN | 0x403f0000 | Event generator |
| MMIO4 | SMIF | 0x40420000 | Serial Memory Interface |
| | SDHC | 0x40460000 | SD/eMMC Host Controller |
| | ETH 0 | 0x40480000 | Ethernet Interface |
| | ETH 1 | 0x40490000 | Ethernet Interface |
| MMIO5 | LIN | 0x40500000 | LIN |
| | CANFD 0 | 0x40520000 | CAN Controller |
| | CANFD 1 | 0x40540000 | CAN Controller |
| | FLEXRAY | 0x40560000 | FlexRay Bus Interface |
| | TCPWM 1 | 0x40580000 | Timer/Counter/PWM |
| MMIO6 | SCB 0 | 0x40600000 | Serial Communications Block (SPI/UART/I2C) |
| | SCB 1 | 0x40610000 | Serial Communications Block (SPI/UART/I2C) |
| | SCB 2 | 0x40620000 | Serial Communications Block (SPI/UART/I2C) |
| | SCB 3 | 0x40630000 | Serial Communications Block (SPI/UART/I2C) |
| | SCB 4 | 0x40640000 | Serial Communications Block (SPI/UART/I2C) |
| | SCB 5 | 0x40650000 | Serial Communications Block (SPI/UART/I2C) |
| | SCB 6 | 0x40660000 | Serial Communications Block (SPI/UART/I2C) |
| | SCB 7 | 0x40670000 | Serial Communications Block (SPI/UART/I2C) |
| | SCB 8 | 0x40680000 | Serial Communications Block (SPI/UART/I2C) |
| | SCB 9 | 0x40690000 | Serial Communications Block (SPI/UART/I2C) |
| | SCB 10 | 0x406a0000 | Serial Communications Block (SPI/UART/I2C) |
| MMIO8 | I2S 0 | 0x40800000 | I2S registers |
| | I2S 1 | 0x40801000 | I2S registers |
| | I2S 2 | 0x40802000 | I2S registers |
| MMIO9 | PASS | 0x40900000 | Programmable Analog Subsystem for S40E |
| SFLASH | SFLASH | 0x17000000 | FLASH Supervisory Region |
| SYSTEM | CM0P | 0xe0000000 | Cortex-M0+ specific registers |
| | CM7 | 0xe0000000 | Cortex-M7 specific registers |
| | SYSAP | 0xe0000000 | System debug Access Port (SYSAP) registers |

# 1 BACKUP

**Description** SRSS Backup Domain (ver3)
**Base Address** 0x40270000
**Size** 0x10000
**Slave Num** MMIO2 - 6

| Register Name | Address | Permission | Description |
|---|---|---|---|
| BACKUP_CTL | 0x40270000 | FULL | Control<br>Note:VDDBAK_CTL VBACKUP_MEAS EN_CHARGE_KEY are not available for this register |
| BACKUP_RTC_RW | 0x40270008 | FULL | RTC Read Write register |
| BACKUP_CAL_CTL | 0x4027000C | FULL | Oscillator calibration for absolute frequency |
| BACKUP_STATUS | 0x40270010 | FULL | Status |
| BACKUP_RTC_TIME | 0x40270014 | FULL | Calendar Seconds, Minutes, Hours, Day of Week |
| BACKUP_RTC_DATE | 0x40270018 | FULL | Calendar Day of Month, Month, Year |
| BACKUP_ALM1_TIME | 0x4027001C | FULL | Alarm 1 Seconds, Minute, Hours, Day of Week |
| BACKUP_ALM1_DATE | 0x40270020 | FULL | Alarm 1 Day of Month, Month |
| BACKUP_ALM2_TIME | 0x40270024 | FULL | Alarm 2 Seconds, Minute, Hours, Day of Week |
| BACKUP_ALM2_DATE | 0x40270028 | FULL | Alarm 2 Day of Month, Month |
| BACKUP_INTR | 0x4027002C | FULL | Interrupt request register |
| BACKUP_INTR_SET | 0x40270030 | FULL | Interrupt set request register |
| BACKUP_INTR_MASK | 0x40270034 | FULL | Interrupt mask register |
| BACKUP_INTR_MASKED | 0x40270038 | FULL | Interrupt masked request register |
| BACKUP_RESET | 0x40270048 | FULL | Backup reset register |
| BACKUP_BREG0 | 0x40271000 | FULL | Backup register region |
| BACKUP_BREG1 | 0x40271004 | FULL | Backup register region |
| BACKUP_BREG2 | 0x40271008 | FULL | Backup register region |
| BACKUP_BREG3 | 0x4027100C | FULL | Backup register region |

## 1.1 Register Details

### 1.1.1 BACKUP_CTL

**Description:** Control
**Address:** 0x40270000
**Offset:** 0x0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** These bits are in vddbak domain.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:4] | | | | WCO_EN [3:3] | None [2:0] | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:14] | | PRESCALER [13:12] | | None [11:10] | | CLK_SEL [9:8] | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:17] | | | | | | | WCO _BYPASS [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 3 | WCO_EN | RW | A | 0 | Watch-crystal oscillator (WCO) enable. If there is a write in progress when this bit is cleared, the WCO will be internally kept on until the write completes. After enabling the WCO software must wait until STATUS.WCO_OK=1 before configuring any component that depends on clk_lf/clk_bak, like for example RTC or WDTs. Follow the procedure in BACKUP_RTC_RW to access this bit. |
| 8:9 | CLK_SEL | RW | A | 0 | Clock select for RTC clock |
| | WCO | | | 0 | Watch-crystal oscillator input, available in Active, DeepSleep, Hibernate, and XRES. |
| | ALTBAK | | | 1 | This allows to use the LFCLK selection as an alternate backup domain clock. Note that LFCLK is only available in Active and DeepSleep power modes. Note that LFCLK clock glitches can propagate into the backup logic when the clock is stopped. For this reason, if the WCO or ILO is intended as the clock source then choose it directly instead of routing through LFCLK. |
| | ILO | | | 2 | Internal Low frequency Oscillator, available in Active, DeepSleep, Hibernate, and XRES. For Hibernate operation CLK_ILO_CONFIG. ILO_BACKUP must be set. If there are multiple ILO, this is ILO0. |
| | LPECO_PRESCALER | | | 3 | Low-power external crystal oscillator prescaler output, available in Active, DeepSleep, Hibernate, and XRES. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 12:13 | PRESCALER | RW | A | 0 | Prescaler for real time clock used when WCO_BYPASS=1 and CLK_SEL = WCO. Configure this field before enabling the WCO, and do not change this setting when WCO_EN=1.<br>0: 32768 Hz square wave. Connect a 32768 Hz square wave to WCO output pin. Do not connect WCO input pin.<br>1: reserved<br>2: reserved<br>3: reserved |
| 16 | WCO_BYPASS | RW | A | 0 | Configures the WCO for different board-level connections to the WCO pins. For example, this can be used to connect an external watch crystal oscillator instead of a watch crystal. In all cases, the two related GPIO pins (WCO input and output pins) must be configured as analog connections using GPIO registers, and they must be hooked at the board level as described below. Configure this field before enabling the WCO, and do not change this setting when WCO_EN=1.<br>0: Watch crystal. Connect a 32.768 kHz watch crystal between WCO input and output pins.<br>1: Clock signal, either a square wave or sine wave. See PRESCALER field for connection information. |

### 1.1.2 BACKUP_RTC_RW

**Description:** RTC Read Write register
**Address:** 0x40270008
**Offset:** 0x8
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** These bits are in vddbak domain but reset in DEEPSLEEP.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:2] | | | | | | WRITE [1:1] | READ [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | READ | RW | A | 0 | Read bit<br>When this bit is set the RTC registers will be copied to user registers and frozen so that a coherent RTC value can safely be read. The RTC will keep on running.<br>Do not set the read bit if the RTC is still busy with a previous update (see RTC_BUSY bit) or if the Write bit is set. Do not set the Read bit at the same time that the Write bit is cleared. |
| 1 | WRITE | RW | A | 0 | Write bit<br>Only when this bit is set can the RTC registers be written to (otherwise writes are ignored). This bit cannot be set if the RTC is still busy with a previous update (see RTC_BUSY bit) or if the Read bit is set or getting set.<br>The user writes to the RTC user registers, when the Write bit is cleared by the user then the user registers content is copied to the actual RTC registers.<br>Only user RTC registers that were written to will get copied, others will not be affected.<br>When the SECONDS field is updated then TICKS will also be reset (WDT is not affected).<br>When the Write bit is cleared by a reset (brown out/DeepSleep) then the RTC update will be ignored/lost.<br>Do not set the Write bit if the RTC if the RTC is still busy with a previous update (see RTC_BUSY). Do not set the Write bit at the same time that the Read bit is cleared. |

### 1.1.3 BACKUP_CAL_CTL

**Description:** Oscillator calibration for absolute frequency
**Address:** 0x4027000C
**Offset:** 0xC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** These bits are in vddbak domain. Calibration only works when the PRESCALER is set to 32768. Writes are ignored unless Write bit is set
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:7] | CALIB_SIGN [6:6] | CALIB_VAL [5:0] | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | CAL_OUT [31:31] | None [30:30] | CAL_SEL [29:28] | | None [27:24] | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:5 | CALIB_VAL | RW | A | 0 | Calibration value for absolute frequency (at a fixed temperature). Each step causes 128 ticks to be added or removed each hour. Effectively that means that each step is 1.085ppm (= 128/(60*60*32,768)). Positive values 0x01-0x3c (1..60) add pulses, negative values remove pulses, thus giving a range of +/-65.1 ppm (limited by 60 minutes per hour, not the range of this field)<br><br>Calibration is performed hourly, starting at 59 minutes and 59 seconds, and applied as 64 ticks every 30 seconds until there have been 2*CALIB_VAL adjustments. |
| 6 | CALIB_SIGN | RW | A | 0 | Calibration sign:<br>0= Negative sign: remove pulses (it takes more clock ticks to count one second)<br>1= Positive sign: add pulses (it takes less clock ticks to count one second) |
| 28:29 | CAL_SEL | RW | A | 0 | Select calibration wave output signal |
| | CAL512 | | | 0 | 512Hz wave, not affected by calibration setting (not supported for 50/60Hz input clock: CTL.PRESCALER!=0) |
| | RESERVED | | | 1 | N/A |
| | CAL2 | | | 2 | 2Hz wave, includes the effect of the calibration setting, (not supported for 50/60Hz input clock: CTL.PRESCALER!=0) |
| | CAL1 | | | 3 | 1Hz wave, includes the effect of the calibration setting (supported for all input clocks) |
| 31 | CAL_OUT | RW | A | 0 | Output enable for wave signal for calibration and allow CALIB_VAL to be written. |

### 1.1.4 BACKUP_STATUS

**Description:** Status
**Address:** 0x40270010
**Offset:** 0x10
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** These bits are in vddbak domain.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:3] | | | | | WCO_OK [2:2] | None [1:1] | RTC_BUSY [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | RTC_BUSY | R | W | 0 | Pending RTC write |
| 2 | WCO_OK | R | W | 0 | Indicates that output has transitioned. |

### 1.1.5 BACKUP_RTC_TIME

**Description:** Calendar Seconds, Minutes, Hours, Day of Week
**Address:** 0x40270014
**Offset:** 0x14
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** These bits are in vddbak domain. Writes are ignored unless Write bit is set. After reset, these will read as zero until the read bit it set and the values are copied from the RTC into these registers..
**Default:** 0x1000000

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:6] | | RTC_SEC [5:0] | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:14] | | RTC_MIN [13:8] | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:23] | CTRL_12HR [22:22] | None [21:21] | RTC_HOUR [20:16] | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:27] | | | | | RTC_DAY [26:24] | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:5 | RTC_SEC | RW | A | 0 | Calendar seconds, 0-59 |
| 8:13 | RTC_MIN | RW | A | 0 | Calendar minutes, 0-59 |
| 16:20 | RTC_HOUR | RW | A | 0 | Calendar hours, value depending on 12/24HR mode<br>0=24HR: [20:16]=0-23<br>1=12HR: [20]:0=AM, 1=PM, [19:16]=1-12 |
| 22 | CTRL_12HR | RW | A | 0 | Select 12/24HR mode: 1=12HR, 0=24HR |
| 24:26 | RTC_DAY | RW | A | 1 | Calendar Day of the week, 1-7<br>It is up to the user to define the meaning of the values, but 1=Monday is recommended |

### 1.1.6 BACKUP_RTC_DATE

**Description:** Calendar Day of Month, Month, Year
**Address:** 0x40270018
**Offset:** 0x18
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** These bits are in vddbak domain. Writes are ignored unless Write bit is set. After reset, these will read as zero until the read bit it set and the values are copied from the RTC into these registers..
**Default:** 0x101

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:5] | | | RTC_DATE [4:0] | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:12] | | | | RTC_MON [11:8] | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:23] | RTC_YEAR [22:16] | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:4 | RTC_DATE | RW | A | 1 | Calendar Day of the Month, 1-31<br>Automatic Leap Year Correction |
| 8:11 | RTC_MON | RW | A | 1 | Calendar Month, 1-12 |
| 16:22 | RTC_YEAR | RW | A | 0 | Calendar year, 0-99 |

### 1.1.7 BACKUP_ALM1_TIME

**Description:** Alarm 1 Seconds, Minute, Hours, Day of Week
**Address:** 0x4027001C
**Offset:** 0x1C
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** These bits are in vddbak domain. This register is only used when BACKUP_ALM1_DATE.ALM_EN=1. Writes are ignored unless Write bit is set. After reset, these will read as zero until the read bit it set and the values are copied from the RTC into these registers..
**Default:** 0x1000000

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | ALM_SEC _EN [7:7] | None [6:6] | ALM_SEC [5:0] | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | ALM_MIN _EN [15:15] | None [14:14] | ALM_MIN [13:8] | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | ALM _HOUR_EN [23:23] | None [22:21] | | ALM_HOUR [20:16] | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | ALM_DAY _EN [31:31] | None [30:27] | | | | ALM_DAY [26:24] | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:5 | ALM_SEC | RW | A | 0 | Alarm seconds, 0-59 |
| 7 | ALM_SEC_EN | RW | A | 0 | Alarm second enable: 0=ignore, 1=match |
| 8:13 | ALM_MIN | RW | A | 0 | Alarm minutes, 0-59 |
| 15 | ALM_MIN_EN | RW | A | 0 | Alarm minutes enable: 0=ignore, 1=match |
| 16:20 | ALM_HOUR | RW | A | 0 | Alarm hours, value depending on 12/24HR mode<br>24HR: [4:0]=0-23<br>12HR: [4]:0=AM, 1=PM, [3:0]=1-12 |
| 23 | ALM_HOUR_EN | RW | A | 0 | Alarm hour enable: 0=ignore, 1=match |
| 24:26 | ALM_DAY | RW | A | 1 | Alarm Day of the week, 1-7<br>It is up to the user to define the meaning of the values, but 1=Monday is recommended |
| 31 | ALM_DAY_EN | RW | A | 0 | Alarm Day of the Week enable: 0=ignore, 1=match |

### 1.1.8 BACKUP_ALM1_DATE

**Description:** Alarm 1 Day of Month, Month
**Address:** 0x40270020
**Offset:** 0x20
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** These bits are in vddbak domain. Writes are ignored unless Write bit is set. After reset, these will read as zero until the read bit it set and the values are copied from the RTC into these registers..
**Default:** 0x101

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | ALM_DATE _EN [7:7] | None [6:5] | | ALM_DATE [4:0] | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | ALM_MON _EN [15:15] | None [14:12] | | | ALM_MON [11:8] | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | ALM_EN [31:31] | None [30:24] | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:4 | ALM_DATE | RW | A | 1 | Alarm Day of the Month, 1-31<br>Leap Year corrected |
| 7 | ALM_DATE_EN | RW | A | 0 | Alarm Day of the Month enable: 0=ignore, 1=match |
| 8:11 | ALM_MON | RW | A | 1 | Alarm Month, 1-12 |
| 15 | ALM_MON_EN | RW | A | 0 | Alarm Month enable: 0=ignore, 1=match |
| 31 | ALM_EN | RW | A | 0 | Master enable for alarm 1.<br>0: Alarm 1 is disabled. Fields for date and time are ignored.<br>1: Alarm 1 is enabled. Alarm triggers whenever the new date and time matches all the enabled date and time fields, which can happen more than once depending on configuration. If none of the date and time fields are enabled, then this alarm triggers once every second. |

### 1.1.9 BACKUP_ALM2_TIME

**Description:** Alarm 2 Seconds, Minute, Hours, Day of Week
**Address:** 0x40270024
**Offset:** 0x24
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** These bits are in vddbak domain. This register is only used when BACKUP_ALM2_DATE.ALM_EN=1. Writes are ignored unless Write bit is set. After reset, these will read as zero until the read bit it set and the values are copied from the RTC into these registers..
**Default:** 0x1000000

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | ALM_SEC _EN [7:7] | None [6:6] | ALM_SEC [5:0] | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | ALM_MIN _EN [15:15] | None [14:14] | ALM_MIN [13:8] | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | ALM _HOUR_EN [23:23] | None [22:21] | | ALM_HOUR [20:16] | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | ALM_DAY _EN [31:31] | None [30:27] | | | | ALM_DAY [26:24] | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:5 | ALM_SEC | RW | A | 0 | Alarm seconds, 0-59 |
| 7 | ALM_SEC_EN | RW | A | 0 | Alarm second enable: 0=ignore, 1=match |
| 8:13 | ALM_MIN | RW | A | 0 | Alarm minutes, 0-59 |
| 15 | ALM_MIN_EN | RW | A | 0 | Alarm minutes enable: 0=ignore, 1=match |
| 16:20 | ALM_HOUR | RW | A | 0 | Alarm hours, value depending on 12/24HR mode<br>24HR: [4:0]=0-23<br>12HR: [4]:0=AM, 1=PM, [3:0]=1-12 |
| 23 | ALM_HOUR_EN | RW | A | 0 | Alarm hour enable: 0=ignore, 1=match |
| 24:26 | ALM_DAY | RW | A | 1 | Alarm Day of the week, 1-7<br>It is up to the user to define the meaning of the values, but 1=Monday is recommended |
| 31 | ALM_DAY_EN | RW | A | 0 | Alarm Day of the Week enable: 0=ignore, 1=match |

### 1.1.10 BACKUP_ALM2_DATE

**Description:** Alarm 2 Day of Month, Month
**Address:** 0x40270028
**Offset:** 0x28
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** These bits are in vddbak domain. Writes are ignored unless Write bit is set. After reset, these will read as zero until the read bit it set and the values are copied from the RTC into these registers..
**Default:** 0x101

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | ALM_DATE _EN [7:7] | None [6:5] | | ALM_DATE [4:0] | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | ALM_MON _EN [15:15] | None [14:12] | | | ALM_MON [11:8] | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | ALM_EN [31:31] | None [30:24] | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:4 | ALM_DATE | RW | A | 1 | Alarm Day of the Month, 1-31<br>Leap Year corrected |
| 7 | ALM_DATE_EN | RW | A | 0 | Alarm Day of the Month enable: 0=ignore, 1=match |
| 8:11 | ALM_MON | RW | A | 1 | Alarm Month, 1-12 |
| 15 | ALM_MON_EN | RW | A | 0 | Alarm Month enable: 0=ignore, 1=match |
| 31 | ALM_EN | RW | A | 0 | Master enable for alarm 2.<br>0: Alarm 2 is disabled. Fields for date and time are ignored.<br>1: Alarm 2 is enabled. Alarm triggers whenever the new date and time matches all the enabled date and time fields, which can happen more than once depending on configuration. If none of the date and time fields are enabled, then this alarm triggers once every second. |

### 1.1.11 BACKUP_INTR

**Description:** Interrupt request register
**Address:** 0x4027002C
**Offset:** 0x2C
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** These bits are in vddbak domain. Interrupt signal from SRSS includes this register and also BACKUP_INTR, if present.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:3] | | | | | CENTURY [2:2] | ALARM2 [1:1] | ALARM1 [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | ALARM1 | RW1C | RW1S | 0 | Alarm 1 Interrupt |
| 1 | ALARM2 | RW1C | RW1S | 0 | Alarm 2 Interrupt |
| 2 | CENTURY | RW1C | RW1S | 0 | Century overflow interrupt |

### 1.1.12 BACKUP_INTR_SET

**Description:** Interrupt set request register
**Address:** 0x40270030
**Offset:** 0x30
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** These bits are in vddbak domain. Allows setting interrupts for firmware testing.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:3] | | | | | CENTURY [2:2] | ALARM2 [1:1] | ALARM1 [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | ALARM1 | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt request register. |
| 1 | ALARM2 | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt request register. |
| 2 | CENTURY | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt request register. |

### 1.1.13 BACKUP_INTR_MASK

**Description:** Interrupt mask register
**Address:** 0x40270034
**Offset:** 0x34
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** These bits are in vddbak domain. When Mask bit is set the interrupt is enabled.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:3] | | | | | CENTURY [2:2] | ALARM2 [1:1] | ALARM1 [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | ALARM1 | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |
| 1 | ALARM2 | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |
| 2 | CENTURY | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |

### 1.1.14 BACKUP_INTR_MASKED

**Description:** Interrupt masked request register
**Address:** 0x40270038
**Offset:** 0x38
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** These bits are in vddbak domain. When read, this register reflects a bitwise and between the interrupt request and mask registers.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:3] | | | | | CENTURY [2:2] | ALARM2 [1:1] | ALARM1 [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | ALARM1 | R | RW | 0 | Logical and of corresponding request and mask bits. |
| 1 | ALARM2 | R | RW | 0 | Logical and of corresponding request and mask bits. |
| 2 | CENTURY | R | RW | 0 | Logical and of corresponding request and mask bits. |

### 1.1.15 BACKUP_RESET

**Description:** Backup reset register
**Address:** 0x40270048
**Offset:** 0x48
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register is used to reset the backup domain from firmware.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | RESET [31:31] | None [30:24] | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 31 | RESET | RW1S | A | 0 | Writing 1 to this register resets the backup logic. Hardware clears it when the reset is complete. After setting this register, firmware should confirm it reads as 0 before attempting to write other backup registers. |

### 1.1.16 BACKUP_BREG

**Description:** Backup register region
**Address:** 0x40271000
**Offset:** 0x1000
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** These bits are in vddbak domain. Backup memory
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | BREG [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | BREG [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | BREG [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | BREG [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | BREG | RW | A | 0 | Backup memory that contains application-specific data. Memory is retained on vbackup supply. |

# 2 CANFD

## 2.1 CANFD 0

**Description** CAN Controller
**Base Address** 0x40520000
**Size** 0x20000
**Slave Num** MMIO5 - 1

| Register Name | Address | Permission | Description |
|---|---|---|---|
| CANFD0_CTL | 0x40521000 | FULL | Global CAN control register |
| CANFD0_STATUS | 0x40521004 | FULL | Global CAN status register |
| CANFD0_INTR0_CAUSE | 0x40521010 | FULL | Consolidated interrupt0 cause register |
| CANFD0_INTR1_CAUSE | 0x40521014 | FULL | Consolidated interrupt1 cause register |
| CANFD0_TS_CTL | 0x40521020 | FULL | Time Stamp control register |
| CANFD0_TS_CNT | 0x40521024 | FULL | Time Stamp counter value |
| CANFD0_ECC_CTL | 0x40521080 | FULL | ECC control |
| CANFD0_ECC_ERR_INJ | 0x40521084 | FULL | ECC error injection |

### 2.1.1 CH 0

| Register Name | Address | Permission | Description |
|---|---|---|---|
| CANFD0_CH0_RXFTOP_CTL | 0x40520180 | FULL | Receive FIFO Top control |
| CANFD0_CH0_RXFTOP0_STAT | 0x405201A0 | FULL | Receive FIFO 0 Top Status |
| CANFD0_CH0_RXFTOP0_DATA | 0x405201A8 | FULL | Receive FIFO 0 Top Data |
| CANFD0_CH0_RXFTOP1_STAT | 0x405201B0 | FULL | Receive FIFO 1 Top Status |
| CANFD0_CH0_RXFTOP1_DATA | 0x405201B8 | FULL | Receive FIFO 1 Top Data |

#### 2.1.1.1 M_TTCAN

| Register Name | Address | Permission | Description |
|---|---|---|---|
| CANFD0_CH0_CREL | 0x40520000 | FULL | Core Release Register |
| CANFD0_CH0_ENDN | 0x40520004 | FULL | Endian Register |
| CANFD0_CH0_DBTP | 0x4052000C | FULL | Data Bit Timing & Prescaler Register |
| CANFD0_CH0_TEST | 0x40520010 | FULL | Test Register |
| CANFD0_CH0_RWD | 0x40520014 | FULL | RAM Watchdog |
| CANFD0_CH0_CCCR | 0x40520018 | FULL | CC Control Register |
| CANFD0_CH0_NBTP | 0x4052001C | FULL | Nominal Bit Timing & Prescaler Register |
| CANFD0_CH0_TSCC | 0x40520020 | FULL | Timestamp Counter Configuration |
| CANFD0_CH0_TSCV | 0x40520024 | FULL | Timestamp Counter Value |
| CANFD0_CH0_TOCC | 0x40520028 | FULL | Timeout Counter Configuration |
| CANFD0_CH0_TOCV | 0x4052002C | FULL | Timeout Counter Value |
| CANFD0_CH0_ECR | 0x40520040 | FULL | Error Counter Register |
| CANFD0_CH0_PSR | 0x40520044 | FULL | Protocol Status Register |
| CANFD0_CH0_TDCR | 0x40520048 | FULL | Transmitter Delay Compensation Register |
| CANFD0_CH0_IR | 0x40520050 | FULL | Interrupt Register |
| CANFD0_CH0_IE | 0x40520054 | FULL | Interrupt Enable |
| CANFD0_CH0_ILS | 0x40520058 | FULL | Interrupt Line Select |
| CANFD0_CH0_ILE | 0x4052005C | FULL | Interrupt Line Enable |
| CANFD0_CH0_GFC | 0x40520080 | FULL | Global Filter Configuration |
| CANFD0_CH0_SIDFC | 0x40520084 | FULL | Standard ID Filter Configuration |
| CANFD0_CH0_XIDFC | 0x40520088 | FULL | Extended ID Filter Configuration |
| CANFD0_CH0_XIDAM | 0x40520090 | FULL | Extended ID AND Mask |
| CANFD0_CH0_HPMS | 0x40520094 | FULL | High Priority Message Status |
| CANFD0_CH0_NDAT1 | 0x40520098 | FULL | New Data 1 |
| CANFD0_CH0_NDAT2 | 0x4052009C | FULL | New Data 2 |
| CANFD0_CH0_RXF0C | 0x405200A0 | FULL | Rx FIFO 0 Configuration |
| CANFD0_CH0_RXF0S | 0x405200A4 | FULL | Rx FIFO 0 Status |
| CANFD0_CH0_RXF0A | 0x405200A8 | FULL | Rx FIFO 0 Acknowledge |
| CANFD0_CH0_RXBC | 0x405200AC | FULL | Rx Buffer Configuration |
| CANFD0_CH0_RXF1C | 0x405200B0 | FULL | Rx FIFO 1 Configuration |
| CANFD0_CH0_RXF1S | 0x405200B4 | FULL | Rx FIFO 1 Status |
| CANFD0_CH0_RXF1A | 0x405200B8 | FULL | Rx FIFO 1 Acknowledge |
| CANFD0_CH0_RXESC | 0x405200BC | FULL | Rx Buffer / FIFO Element Size Configuration |
| CANFD0_CH0_TXBC | 0x405200C0 | FULL | Tx Buffer Configuration |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| CANFD0_CH0_TXFQS | 0x405200C4 | FULL | Tx FIFO/Queue Status |
| CANFD0_CH0_TXESC | 0x405200C8 | FULL | Tx Buffer Element Size Configuration |
| CANFD0_CH0_TXBRP | 0x405200CC | FULL | Tx Buffer Request Pending |
| CANFD0_CH0_TXBAR | 0x405200D0 | FULL | Tx Buffer Add Request |
| CANFD0_CH0_TXBCR | 0x405200D4 | FULL | Tx Buffer Cancellation Request |
| CANFD0_CH0_TXBTO | 0x405200D8 | FULL | Tx Buffer Transmission Occurred |
| CANFD0_CH0_TXBCF | 0x405200DC | FULL | Tx Buffer Cancellation Finished |
| CANFD0_CH0_TXBTIE | 0x405200E0 | FULL | Tx Buffer Transmission Interrupt Enable |
| CANFD0_CH0_TXBCIE | 0x405200E4 | FULL | Tx Buffer Cancellation Finished Interrupt Enable |
| CANFD0_CH0_TXEFC | 0x405200F0 | FULL | Tx Event FIFO Configuration |
| CANFD0_CH0_TXEFS | 0x405200F4 | FULL | Tx Event FIFO Status |
| CANFD0_CH0_TXEFA | 0x405200F8 | FULL | Tx Event FIFO Acknowledge |
| CANFD0_CH0_TTTMC | 0x40520100 | FULL | TT Trigger Memory Configuration |
| CANFD0_CH0_TTRMC | 0x40520104 | FULL | TT Reference Message Configuration |
| CANFD0_CH0_TTOCF | 0x40520108 | FULL | TT Operation Configuration |
| CANFD0_CH0_TTMLM | 0x4052010C | FULL | TT Matrix Limits |
| CANFD0_CH0_TURCF | 0x40520110 | FULL | TUR Configuration |
| CANFD0_CH0_TTOCN | 0x40520114 | FULL | TT Operation Control |
| CANFD0_CH0_TTGTP | 0x40520118 | FULL | TT Global Time Preset |
| CANFD0_CH0_TTTMK | 0x4052011C | FULL | TT Time Mark |
| CANFD0_CH0_TTIR | 0x40520120 | FULL | TT Interrupt Register |
| CANFD0_CH0_TTIE | 0x40520124 | FULL | TT Interrupt Enable |
| CANFD0_CH0_TTILS | 0x40520128 | FULL | TT Interrupt Line Select |
| CANFD0_CH0_TTOST | 0x4052012C | FULL | TT Operation Status |
| CANFD0_CH0_TURNA | 0x40520130 | FULL | TUR Numerator Actual |
| CANFD0_CH0_TTLGT | 0x40520134 | FULL | TT Local & Global Time |
| CANFD0_CH0_TTCTC | 0x40520138 | FULL | TT Cycle Time & Count |
| CANFD0_CH0_TTCPT | 0x4052013C | FULL | TT Capture Time |
| CANFD0_CH0_TTCSM | 0x40520140 | FULL | TT Cycle Sync Mark |

### 2.1.2 CH 1

| Register Name | Address | Permission | Description |
|---|---|---|---|
| CANFD0_CH1_RXFTOP_CTL | 0x40520380 | FULL | Receive FIFO Top control |
| CANFD0_CH1_RXFTOP0_STAT | 0x405203A0 | FULL | Receive FIFO 0 Top Status |
| CANFD0_CH1_RXFTOP0_DATA | 0x405203A8 | FULL | Receive FIFO 0 Top Data |
| CANFD0_CH1_RXFTOP1_STAT | 0x405203B0 | FULL | Receive FIFO 1 Top Status |
| CANFD0_CH1_RXFTOP1_DATA | 0x405203B8 | FULL | Receive FIFO 1 Top Data |

#### 2.1.2.1 M_TTCAN

| Register Name | Address | Permission | Description |
|---|---|---|---|
| CANFD0_CH1_CREL | 0x40520200 | FULL | Core Release Register |
| CANFD0_CH1_ENDN | 0x40520204 | FULL | Endian Register |
| CANFD0_CH1_DBTP | 0x4052020C | FULL | Data Bit Timing & Prescaler Register |
| CANFD0_CH1_TEST | 0x40520210 | FULL | Test Register |
| CANFD0_CH1_RWD | 0x40520214 | FULL | RAM Watchdog |
| CANFD0_CH1_CCCR | 0x40520218 | FULL | CC Control Register |
| CANFD0_CH1_NBTP | 0x4052021C | FULL | Nominal Bit Timing & Prescaler Register |
| CANFD0_CH1_TSCC | 0x40520220 | FULL | Timestamp Counter Configuration |
| CANFD0_CH1_TSCV | 0x40520224 | FULL | Timestamp Counter Value |
| CANFD0_CH1_TOCC | 0x40520228 | FULL | Timeout Counter Configuration |
| CANFD0_CH1_TOCV | 0x4052022C | FULL | Timeout Counter Value |
| CANFD0_CH1_ECR | 0x40520240 | FULL | Error Counter Register |
| CANFD0_CH1_PSR | 0x40520244 | FULL | Protocol Status Register |
| CANFD0_CH1_TDCR | 0x40520248 | FULL | Transmitter Delay Compensation Register |
| CANFD0_CH1_IR | 0x40520250 | FULL | Interrupt Register |
| CANFD0_CH1_IE | 0x40520254 | FULL | Interrupt Enable |
| CANFD0_CH1_ILS | 0x40520258 | FULL | Interrupt Line Select |
| CANFD0_CH1_ILE | 0x4052025C | FULL | Interrupt Line Enable |
| CANFD0_CH1_GFC | 0x40520280 | FULL | Global Filter Configuration |
| CANFD0_CH1_SIDFC | 0x40520284 | FULL | Standard ID Filter Configuration |
| CANFD0_CH1_XIDFC | 0x40520288 | FULL | Extended ID Filter Configuration |
| CANFD0_CH1_XIDAM | 0x40520290 | FULL | Extended ID AND Mask |
| CANFD0_CH1_HPMS | 0x40520294 | FULL | High Priority Message Status |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| CANFD0_CH1_NDAT1 | 0x40520298 | FULL | New Data 1 |
| CANFD0_CH1_NDAT2 | 0x4052029C | FULL | New Data 2 |
| CANFD0_CH1_RXF0C | 0x405202A0 | FULL | Rx FIFO 0 Configuration |
| CANFD0_CH1_RXF0S | 0x405202A4 | FULL | Rx FIFO 0 Status |
| CANFD0_CH1_RXF0A | 0x405202A8 | FULL | Rx FIFO 0 Acknowledge |
| CANFD0_CH1_RXBC | 0x405202AC | FULL | Rx Buffer Configuration |
| CANFD0_CH1_RXF1C | 0x405202B0 | FULL | Rx FIFO 1 Configuration |
| CANFD0_CH1_RXF1S | 0x405202B4 | FULL | Rx FIFO 1 Status |
| CANFD0_CH1_RXF1A | 0x405202B8 | FULL | Rx FIFO 1 Acknowledge |
| CANFD0_CH1_RXESC | 0x405202BC | FULL | Rx Buffer / FIFO Element Size Configuration |
| CANFD0_CH1_TXBC | 0x405202C0 | FULL | Tx Buffer Configuration |
| CANFD0_CH1_TXFQS | 0x405202C4 | FULL | Tx FIFO/Queue Status |
| CANFD0_CH1_TXESC | 0x405202C8 | FULL | Tx Buffer Element Size Configuration |
| CANFD0_CH1_TXBRP | 0x405202CC | FULL | Tx Buffer Request Pending |
| CANFD0_CH1_TXBAR | 0x405202D0 | FULL | Tx Buffer Add Request |
| CANFD0_CH1_TXBCR | 0x405202D4 | FULL | Tx Buffer Cancellation Request |
| CANFD0_CH1_TXBTO | 0x405202D8 | FULL | Tx Buffer Transmission Occurred |
| CANFD0_CH1_TXBCF | 0x405202DC | FULL | Tx Buffer Cancellation Finished |
| CANFD0_CH1_TXBTIE | 0x405202E0 | FULL | Tx Buffer Transmission Interrupt Enable |
| CANFD0_CH1_TXBCIE | 0x405202E4 | FULL | Tx Buffer Cancellation Finished Interrupt Enable |
| CANFD0_CH1_TXEFC | 0x405202F0 | FULL | Tx Event FIFO Configuration |
| CANFD0_CH1_TXEFS | 0x405202F4 | FULL | Tx Event FIFO Status |
| CANFD0_CH1_TXEFA | 0x405202F8 | FULL | Tx Event FIFO Acknowledge |
| CANFD0_CH1_TTTMC | 0x40520300 | FULL | TT Trigger Memory Configuration |
| CANFD0_CH1_TTRMC | 0x40520304 | FULL | TT Reference Message Configuration |
| CANFD0_CH1_TTOCF | 0x40520308 | FULL | TT Operation Configuration |
| CANFD0_CH1_TTMLM | 0x4052030C | FULL | TT Matrix Limits |
| CANFD0_CH1_TURCF | 0x40520310 | FULL | TUR Configuration |
| CANFD0_CH1_TTOCN | 0x40520314 | FULL | TT Operation Control |
| CANFD0_CH1_TTGTP | 0x40520318 | FULL | TT Global Time Preset |
| CANFD0_CH1_TTTMK | 0x4052031C | FULL | TT Time Mark |
| CANFD0_CH1_TTIR | 0x40520320 | FULL | TT Interrupt Register |
| CANFD0_CH1_TTIE | 0x40520324 | FULL | TT Interrupt Enable |
| CANFD0_CH1_TTILS | 0x40520328 | FULL | TT Interrupt Line Select |
| CANFD0_CH1_TTOST | 0x4052032C | FULL | TT Operation Status |
| CANFD0_CH1_TURNA | 0x40520330 | FULL | TUR Numerator Actual |
| CANFD0_CH1_TTLGT | 0x40520334 | FULL | TT Local & Global Time |
| CANFD0_CH1_TTCTC | 0x40520338 | FULL | TT Cycle Time & Count |
| CANFD0_CH1_TTCPT | 0x4052033C | FULL | TT Capture Time |
| CANFD0_CH1_TTCSM | 0x40520340 | FULL | TT Cycle Sync Mark |

### 2.1.3 CH 2

| Register Name | Address | Permission | Description |
|---|---|---|---|
| CANFD0_CH2_RXFTOP_CTL | 0x40520580 | FULL | Receive FIFO Top control |
| CANFD0_CH2_RXFTOP0_STAT | 0x405205A0 | FULL | Receive FIFO 0 Top Status |
| CANFD0_CH2_RXFTOP0_DATA | 0x405205A8 | FULL | Receive FIFO 0 Top Data |
| CANFD0_CH2_RXFTOP1_STAT | 0x405205B0 | FULL | Receive FIFO 1 Top Status |
| CANFD0_CH2_RXFTOP1_DATA | 0x405205B8 | FULL | Receive FIFO 1 Top Data |

#### 2.1.3.1 M_TTCAN

| Register Name | Address | Permission | Description |
|---|---|---|---|
| CANFD0_CH2_CREL | 0x40520400 | FULL | Core Release Register |
| CANFD0_CH2_ENDN | 0x40520404 | FULL | Endian Register |
| CANFD0_CH2_DBTP | 0x4052040C | FULL | Data Bit Timing & Prescaler Register |
| CANFD0_CH2_TEST | 0x40520410 | FULL | Test Register |
| CANFD0_CH2_RWD | 0x40520414 | FULL | RAM Watchdog |
| CANFD0_CH2_CCCR | 0x40520418 | FULL | CC Control Register |
| CANFD0_CH2_NBTP | 0x4052041C | FULL | Nominal Bit Timing & Prescaler Register |
| CANFD0_CH2_TSCC | 0x40520420 | FULL | Timestamp Counter Configuration |
| CANFD0_CH2_TSCV | 0x40520424 | FULL | Timestamp Counter Value |
| CANFD0_CH2_TOCC | 0x40520428 | FULL | Timeout Counter Configuration |
| CANFD0_CH2_TOCV | 0x4052042C | FULL | Timeout Counter Value |
| CANFD0_CH2_ECR | 0x40520440 | FULL | Error Counter Register |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| CANFD0_CH2_PSR | 0x40520444 | FULL | Protocol Status Register |
| CANFD0_CH2_TDCR | 0x40520448 | FULL | Transmitter Delay Compensation Register |
| CANFD0_CH2_IR | 0x40520450 | FULL | Interrupt Register |
| CANFD0_CH2_IE | 0x40520454 | FULL | Interrupt Enable |
| CANFD0_CH2_ILS | 0x40520458 | FULL | Interrupt Line Select |
| CANFD0_CH2_ILE | 0x4052045C | FULL | Interrupt Line Enable |
| CANFD0_CH2_GFC | 0x40520480 | FULL | Global Filter Configuration |
| CANFD0_CH2_SIDFC | 0x40520484 | FULL | Standard ID Filter Configuration |
| CANFD0_CH2_XIDFC | 0x40520488 | FULL | Extended ID Filter Configuration |
| CANFD0_CH2_XIDAM | 0x40520490 | FULL | Extended ID AND Mask |
| CANFD0_CH2_HPMS | 0x40520494 | FULL | High Priority Message Status |
| CANFD0_CH2_NDAT1 | 0x40520498 | FULL | New Data 1 |
| CANFD0_CH2_NDAT2 | 0x4052049C | FULL | New Data 2 |
| CANFD0_CH2_RXF0C | 0x405204A0 | FULL | Rx FIFO 0 Configuration |
| CANFD0_CH2_RXF0S | 0x405204A4 | FULL | Rx FIFO 0 Status |
| CANFD0_CH2_RXF0A | 0x405204A8 | FULL | Rx FIFO 0 Acknowledge |
| CANFD0_CH2_RXBC | 0x405204AC | FULL | Rx Buffer Configuration |
| CANFD0_CH2_RXF1C | 0x405204B0 | FULL | Rx FIFO 1 Configuration |
| CANFD0_CH2_RXF1S | 0x405204B4 | FULL | Rx FIFO 1 Status |
| CANFD0_CH2_RXF1A | 0x405204B8 | FULL | Rx FIFO 1 Acknowledge |
| CANFD0_CH2_RXESC | 0x405204BC | FULL | Rx Buffer / FIFO Element Size Configuration |
| CANFD0_CH2_TXBC | 0x405204C0 | FULL | Tx Buffer Configuration |
| CANFD0_CH2_TXFQS | 0x405204C4 | FULL | Tx FIFO/Queue Status |
| CANFD0_CH2_TXESC | 0x405204C8 | FULL | Tx Buffer Element Size Configuration |
| CANFD0_CH2_TXBRP | 0x405204CC | FULL | Tx Buffer Request Pending |
| CANFD0_CH2_TXBAR | 0x405204D0 | FULL | Tx Buffer Add Request |
| CANFD0_CH2_TXBCR | 0x405204D4 | FULL | Tx Buffer Cancellation Request |
| CANFD0_CH2_TXBTO | 0x405204D8 | FULL | Tx Buffer Transmission Occurred |
| CANFD0_CH2_TXBCF | 0x405204DC | FULL | Tx Buffer Cancellation Finished |
| CANFD0_CH2_TXBTIE | 0x405204E0 | FULL | Tx Buffer Transmission Interrupt Enable |
| CANFD0_CH2_TXBCIE | 0x405204E4 | FULL | Tx Buffer Cancellation Finished Interrupt Enable |
| CANFD0_CH2_TXEFC | 0x405204F0 | FULL | Tx Event FIFO Configuration |
| CANFD0_CH2_TXEFS | 0x405204F4 | FULL | Tx Event FIFO Status |
| CANFD0_CH2_TXEFA | 0x405204F8 | FULL | Tx Event FIFO Acknowledge |
| CANFD0_CH2_TTTMC | 0x40520500 | FULL | TT Trigger Memory Configuration |
| CANFD0_CH2_TTRMC | 0x40520504 | FULL | TT Reference Message Configuration |
| CANFD0_CH2_TTOCF | 0x40520508 | FULL | TT Operation Configuration |
| CANFD0_CH2_TTMLM | 0x4052050C | FULL | TT Matrix Limits |
| CANFD0_CH2_TURCF | 0x40520510 | FULL | TUR Configuration |
| CANFD0_CH2_TTOCN | 0x40520514 | FULL | TT Operation Control |
| CANFD0_CH2_TTGTP | 0x40520518 | FULL | TT Global Time Preset |
| CANFD0_CH2_TTTMK | 0x4052051C | FULL | TT Time Mark |
| CANFD0_CH2_TTIR | 0x40520520 | FULL | TT Interrupt Register |
| CANFD0_CH2_TTIE | 0x40520524 | FULL | TT Interrupt Enable |
| CANFD0_CH2_TTILS | 0x40520528 | FULL | TT Interrupt Line Select |
| CANFD0_CH2_TTOST | 0x4052052C | FULL | TT Operation Status |
| CANFD0_CH2_TURNA | 0x40520530 | FULL | TUR Numerator Actual |
| CANFD0_CH2_TTLGT | 0x40520534 | FULL | TT Local & Global Time |
| CANFD0_CH2_TTCTC | 0x40520538 | FULL | TT Cycle Time & Count |
| CANFD0_CH2_TTCPT | 0x4052053C | FULL | TT Capture Time |
| CANFD0_CH2_TTCSM | 0x40520540 | FULL | TT Cycle Sync Mark |

### 2.1.4 CH 3

| Register Name | Address | Permission | Description |
|---|---|---|---|
| CANFD0_CH3_RXFTOP_CTL | 0x40520780 | FULL | Receive FIFO Top control |
| CANFD0_CH3_RXFTOP0_STAT | 0x405207A0 | FULL | Receive FIFO 0 Top Status |
| CANFD0_CH3_RXFTOP0_DATA | 0x405207A8 | FULL | Receive FIFO 0 Top Data |
| CANFD0_CH3_RXFTOP1_STAT | 0x405207B0 | FULL | Receive FIFO 1 Top Status |
| CANFD0_CH3_RXFTOP1_DATA | 0x405207B8 | FULL | Receive FIFO 1 Top Data |

#### 2.1.4.1 M_TTCAN

| Register Name | Address | Permission | Description |
|---|---|---|---|
| CANFD0_CH3_CREL | 0x40520600 | FULL | Core Release Register |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| CANFD0_CH3_ENDN | 0x40520604 | FULL | Endian Register |
| CANFD0_CH3_DBTP | 0x4052060C | FULL | Data Bit Timing & Prescaler Register |
| CANFD0_CH3_TEST | 0x40520610 | FULL | Test Register |
| CANFD0_CH3_RWD | 0x40520614 | FULL | RAM Watchdog |
| CANFD0_CH3_CCCR | 0x40520618 | FULL | CC Control Register |
| CANFD0_CH3_NBTP | 0x4052061C | FULL | Nominal Bit Timing & Prescaler Register |
| CANFD0_CH3_TSCC | 0x40520620 | FULL | Timestamp Counter Configuration |
| CANFD0_CH3_TSCV | 0x40520624 | FULL | Timestamp Counter Value |
| CANFD0_CH3_TOCC | 0x40520628 | FULL | Timeout Counter Configuration |
| CANFD0_CH3_TOCV | 0x4052062C | FULL | Timeout Counter Value |
| CANFD0_CH3_ECR | 0x40520640 | FULL | Error Counter Register |
| CANFD0_CH3_PSR | 0x40520644 | FULL | Protocol Status Register |
| CANFD0_CH3_TDCR | 0x40520648 | FULL | Transmitter Delay Compensation Register |
| CANFD0_CH3_IR | 0x40520650 | FULL | Interrupt Register |
| CANFD0_CH3_IE | 0x40520654 | FULL | Interrupt Enable |
| CANFD0_CH3_ILS | 0x40520658 | FULL | Interrupt Line Select |
| CANFD0_CH3_ILE | 0x4052065C | FULL | Interrupt Line Enable |
| CANFD0_CH3_GFC | 0x40520680 | FULL | Global Filter Configuration |
| CANFD0_CH3_SIDFC | 0x40520684 | FULL | Standard ID Filter Configuration |
| CANFD0_CH3_XIDFC | 0x40520688 | FULL | Extended ID Filter Configuration |
| CANFD0_CH3_XIDAM | 0x40520690 | FULL | Extended ID AND Mask |
| CANFD0_CH3_HPMS | 0x40520694 | FULL | High Priority Message Status |
| CANFD0_CH3_NDAT1 | 0x40520698 | FULL | New Data 1 |
| CANFD0_CH3_NDAT2 | 0x4052069C | FULL | New Data 2 |
| CANFD0_CH3_RXF0C | 0x405206A0 | FULL | Rx FIFO 0 Configuration |
| CANFD0_CH3_RXF0S | 0x405206A4 | FULL | Rx FIFO 0 Status |
| CANFD0_CH3_RXF0A | 0x405206A8 | FULL | Rx FIFO 0 Acknowledge |
| CANFD0_CH3_RXBC | 0x405206AC | FULL | Rx Buffer Configuration |
| CANFD0_CH3_RXF1C | 0x405206B0 | FULL | Rx FIFO 1 Configuration |
| CANFD0_CH3_RXF1S | 0x405206B4 | FULL | Rx FIFO 1 Status |
| CANFD0_CH3_RXF1A | 0x405206B8 | FULL | Rx FIFO 1 Acknowledge |
| CANFD0_CH3_RXESC | 0x405206BC | FULL | Rx Buffer / FIFO Element Size Configuration |
| CANFD0_CH3_TXBC | 0x405206C0 | FULL | Tx Buffer Configuration |
| CANFD0_CH3_TXFQS | 0x405206C4 | FULL | Tx FIFO/Queue Status |
| CANFD0_CH3_TXESC | 0x405206C8 | FULL | Tx Buffer Element Size Configuration |
| CANFD0_CH3_TXBRP | 0x405206CC | FULL | Tx Buffer Request Pending |
| CANFD0_CH3_TXBAR | 0x405206D0 | FULL | Tx Buffer Add Request |
| CANFD0_CH3_TXBCR | 0x405206D4 | FULL | Tx Buffer Cancellation Request |
| CANFD0_CH3_TXBTO | 0x405206D8 | FULL | Tx Buffer Transmission Occurred |
| CANFD0_CH3_TXBCF | 0x405206DC | FULL | Tx Buffer Cancellation Finished |
| CANFD0_CH3_TXBTIE | 0x405206E0 | FULL | Tx Buffer Transmission Interrupt Enable |
| CANFD0_CH3_TXBCIE | 0x405206E4 | FULL | Tx Buffer Cancellation Finished Interrupt Enable |
| CANFD0_CH3_TXEFC | 0x405206F0 | FULL | Tx Event FIFO Configuration |
| CANFD0_CH3_TXEFS | 0x405206F4 | FULL | Tx Event FIFO Status |
| CANFD0_CH3_TXEFA | 0x405206F8 | FULL | Tx Event FIFO Acknowledge |
| CANFD0_CH3_TTTMC | 0x40520700 | FULL | TT Trigger Memory Configuration |
| CANFD0_CH3_TTRMC | 0x40520704 | FULL | TT Reference Message Configuration |
| CANFD0_CH3_TTOCF | 0x40520708 | FULL | TT Operation Configuration |
| CANFD0_CH3_TTMLM | 0x4052070C | FULL | TT Matrix Limits |
| CANFD0_CH3_TURCF | 0x40520710 | FULL | TUR Configuration |
| CANFD0_CH3_TTOCN | 0x40520714 | FULL | TT Operation Control |
| CANFD0_CH3_TTGTP | 0x40520718 | FULL | TT Global Time Preset |
| CANFD0_CH3_TTTMK | 0x4052071C | FULL | TT Time Mark |
| CANFD0_CH3_TTIR | 0x40520720 | FULL | TT Interrupt Register |
| CANFD0_CH3_TTIE | 0x40520724 | FULL | TT Interrupt Enable |
| CANFD0_CH3_TTILS | 0x40520728 | FULL | TT Interrupt Line Select |
| CANFD0_CH3_TTOST | 0x4052072C | FULL | TT Operation Status |
| CANFD0_CH3_TURNA | 0x40520730 | FULL | TUR Numerator Actual |
| CANFD0_CH3_TTLGT | 0x40520734 | FULL | TT Local & Global Time |
| CANFD0_CH3_TTCTC | 0x40520738 | FULL | TT Cycle Time & Count |
| CANFD0_CH3_TTCPT | 0x4052073C | FULL | TT Capture Time |
| CANFD0_CH3_TTCSM | 0x40520740 | FULL | TT Cycle Sync Mark |

### 2.1.5 CH 4

| Register Name | Address | Permission | Description |
|---|---|---|---|
| CANFD0_CH4_RXFTOP_CTL | 0x40520980 | FULL | Receive FIFO Top control |
| CANFD0_CH4_RXFTOP0_STAT | 0x405209A0 | FULL | Receive FIFO 0 Top Status |
| CANFD0_CH4_RXFTOP0_DATA | 0x405209A8 | FULL | Receive FIFO 0 Top Data |
| CANFD0_CH4_RXFTOP1_STAT | 0x405209B0 | FULL | Receive FIFO 1 Top Status |
| CANFD0_CH4_RXFTOP1_DATA | 0x405209B8 | FULL | Receive FIFO 1 Top Data |

#### 2.1.5.1 M_TTCAN

| Register Name | Address | Permission | Description |
|---|---|---|---|
| CANFD0_CH4_CREL | 0x40520800 | FULL | Core Release Register |
| CANFD0_CH4_ENDN | 0x40520804 | FULL | Endian Register |
| CANFD0_CH4_DBTP | 0x4052080C | FULL | Data Bit Timing & Prescaler Register |
| CANFD0_CH4_TEST | 0x40520810 | FULL | Test Register |
| CANFD0_CH4_RWD | 0x40520814 | FULL | RAM Watchdog |
| CANFD0_CH4_CCCR | 0x40520818 | FULL | CC Control Register |
| CANFD0_CH4_NBTP | 0x4052081C | FULL | Nominal Bit Timing & Prescaler Register |
| CANFD0_CH4_TSCC | 0x40520820 | FULL | Timestamp Counter Configuration |
| CANFD0_CH4_TSCV | 0x40520824 | FULL | Timestamp Counter Value |
| CANFD0_CH4_TOCC | 0x40520828 | FULL | Timeout Counter Configuration |
| CANFD0_CH4_TOCV | 0x4052082C | FULL | Timeout Counter Value |
| CANFD0_CH4_ECR | 0x40520840 | FULL | Error Counter Register |
| CANFD0_CH4_PSR | 0x40520844 | FULL | Protocol Status Register |
| CANFD0_CH4_TDCR | 0x40520848 | FULL | Transmitter Delay Compensation Register |
| CANFD0_CH4_IR | 0x40520850 | FULL | Interrupt Register |
| CANFD0_CH4_IE | 0x40520854 | FULL | Interrupt Enable |
| CANFD0_CH4_ILS | 0x40520858 | FULL | Interrupt Line Select |
| CANFD0_CH4_ILE | 0x4052085C | FULL | Interrupt Line Enable |
| CANFD0_CH4_GFC | 0x40520880 | FULL | Global Filter Configuration |
| CANFD0_CH4_SIDFC | 0x40520884 | FULL | Standard ID Filter Configuration |
| CANFD0_CH4_XIDFC | 0x40520888 | FULL | Extended ID Filter Configuration |
| CANFD0_CH4_XIDAM | 0x40520890 | FULL | Extended ID AND Mask |
| CANFD0_CH4_HPMS | 0x40520894 | FULL | High Priority Message Status |
| CANFD0_CH4_NDAT1 | 0x40520898 | FULL | New Data 1 |
| CANFD0_CH4_NDAT2 | 0x4052089C | FULL | New Data 2 |
| CANFD0_CH4_RXF0C | 0x405208A0 | FULL | Rx FIFO 0 Configuration |
| CANFD0_CH4_RXF0S | 0x405208A4 | FULL | Rx FIFO 0 Status |
| CANFD0_CH4_RXF0A | 0x405208A8 | FULL | Rx FIFO 0 Acknowledge |
| CANFD0_CH4_RXBC | 0x405208AC | FULL | Rx Buffer Configuration |
| CANFD0_CH4_RXF1C | 0x405208B0 | FULL | Rx FIFO 1 Configuration |
| CANFD0_CH4_RXF1S | 0x405208B4 | FULL | Rx FIFO 1 Status |
| CANFD0_CH4_RXF1A | 0x405208B8 | FULL | Rx FIFO 1 Acknowledge |
| CANFD0_CH4_RXESC | 0x405208BC | FULL | Rx Buffer / FIFO Element Size Configuration |
| CANFD0_CH4_TXBC | 0x405208C0 | FULL | Tx Buffer Configuration |
| CANFD0_CH4_TXFQS | 0x405208C4 | FULL | Tx FIFO/Queue Status |
| CANFD0_CH4_TXESC | 0x405208C8 | FULL | Tx Buffer Element Size Configuration |
| CANFD0_CH4_TXBRP | 0x405208CC | FULL | Tx Buffer Request Pending |
| CANFD0_CH4_TXBAR | 0x405208D0 | FULL | Tx Buffer Add Request |
| CANFD0_CH4_TXBCR | 0x405208D4 | FULL | Tx Buffer Cancellation Request |
| CANFD0_CH4_TXBTO | 0x405208D8 | FULL | Tx Buffer Transmission Occurred |
| CANFD0_CH4_TXBCF | 0x405208DC | FULL | Tx Buffer Cancellation Finished |
| CANFD0_CH4_TXBTIE | 0x405208E0 | FULL | Tx Buffer Transmission Interrupt Enable |
| CANFD0_CH4_TXBCIE | 0x405208E4 | FULL | Tx Buffer Cancellation Finished Interrupt Enable |
| CANFD0_CH4_TXEFC | 0x405208F0 | FULL | Tx Event FIFO Configuration |
| CANFD0_CH4_TXEFS | 0x405208F4 | FULL | Tx Event FIFO Status |
| CANFD0_CH4_TXEFA | 0x405208F8 | FULL | Tx Event FIFO Acknowledge |
| CANFD0_CH4_TTTMC | 0x40520900 | FULL | TT Trigger Memory Configuration |
| CANFD0_CH4_TTRMC | 0x40520904 | FULL | TT Reference Message Configuration |
| CANFD0_CH4_TTOCF | 0x40520908 | FULL | TT Operation Configuration |
| CANFD0_CH4_TTMLM | 0x4052090C | FULL | TT Matrix Limits |
| CANFD0_CH4_TURCF | 0x40520910 | FULL | TUR Configuration |
| CANFD0_CH4_TTOCN | 0x40520914 | FULL | TT Operation Control |
| CANFD0_CH4_TTGTP | 0x40520918 | FULL | TT Global Time Preset |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| CANFD0_CH4_TTTMK | 0x4052091C | FULL | TT Time Mark |
| CANFD0_CH4_TTIR | 0x40520920 | FULL | TT Interrupt Register |
| CANFD0_CH4_TTIE | 0x40520924 | FULL | TT Interrupt Enable |
| CANFD0_CH4_TTILS | 0x40520928 | FULL | TT Interrupt Line Select |
| CANFD0_CH4_TTOST | 0x4052092C | FULL | TT Operation Status |
| CANFD0_CH4_TURNA | 0x40520930 | FULL | TUR Numerator Actual |
| CANFD0_CH4_TTLGT | 0x40520934 | FULL | TT Local & Global Time |
| CANFD0_CH4_TTCTC | 0x40520938 | FULL | TT Cycle Time & Count |
| CANFD0_CH4_TTCPT | 0x4052093C | FULL | TT Capture Time |
| CANFD0_CH4_TTCSM | 0x40520940 | FULL | TT Cycle Sync Mark |

## 2.2 CANFD 1

**Description** CAN Controller
**Base Address** 0x40540000
**Size** 0x20000
**Slave Num** MMIO5 - 2

| Register Name | Address | Permission | Description |
|---|---|---|---|
| CANFD1_CTL | 0x40541000 | FULL | Global CAN control register |
| CANFD1_STATUS | 0x40541004 | FULL | Global CAN status register |
| CANFD1_INTR0_CAUSE | 0x40541010 | FULL | Consolidated interrupt0 cause register |
| CANFD1_INTR1_CAUSE | 0x40541014 | FULL | Consolidated interrupt1 cause register |
| CANFD1_ECC_CTL | 0x40541080 | FULL | ECC control |
| CANFD1_ECC_ERR_INJ | 0x40541084 | FULL | ECC error injection |

### 2.2.1 CH 0

| Register Name | Address | Permission | Description |
|---|---|---|---|
| CANFD1_CH0_RXFTOP_CTL | 0x40540180 | FULL | Receive FIFO Top control |
| CANFD1_CH0_RXFTOP0_STAT | 0x405401A0 | FULL | Receive FIFO 0 Top Status |
| CANFD1_CH0_RXFTOP0_DATA | 0x405401A8 | FULL | Receive FIFO 0 Top Data |
| CANFD1_CH0_RXFTOP1_STAT | 0x405401B0 | FULL | Receive FIFO 1 Top Status |
| CANFD1_CH0_RXFTOP1_DATA | 0x405401B8 | FULL | Receive FIFO 1 Top Data |

#### 2.2.1.1 M_TTCAN

| Register Name | Address | Permission | Description |
|---|---|---|---|
| CANFD1_CH0_CREL | 0x40540000 | FULL | Core Release Register |
| CANFD1_CH0_ENDN | 0x40540004 | FULL | Endian Register |
| CANFD1_CH0_DBTP | 0x4054000C | FULL | Data Bit Timing & Prescaler Register |
| CANFD1_CH0_TEST | 0x40540010 | FULL | Test Register |
| CANFD1_CH0_RWD | 0x40540014 | FULL | RAM Watchdog |
| CANFD1_CH0_CCCR | 0x40540018 | FULL | CC Control Register |
| CANFD1_CH0_NBTP | 0x4054001C | FULL | Nominal Bit Timing & Prescaler Register |
| CANFD1_CH0_TSCC | 0x40540020 | FULL | Timestamp Counter Configuration |
| CANFD1_CH0_TSCV | 0x40540024 | FULL | Timestamp Counter Value |
| CANFD1_CH0_TOCC | 0x40540028 | FULL | Timeout Counter Configuration |
| CANFD1_CH0_TOCV | 0x4054002C | FULL | Timeout Counter Value |
| CANFD1_CH0_ECR | 0x40540040 | FULL | Error Counter Register |
| CANFD1_CH0_PSR | 0x40540044 | FULL | Protocol Status Register |
| CANFD1_CH0_TDCR | 0x40540048 | FULL | Transmitter Delay Compensation Register |
| CANFD1_CH0_IR | 0x40540050 | FULL | Interrupt Register |
| CANFD1_CH0_IE | 0x40540054 | FULL | Interrupt Enable |
| CANFD1_CH0_ILS | 0x40540058 | FULL | Interrupt Line Select |
| CANFD1_CH0_ILE | 0x4054005C | FULL | Interrupt Line Enable |
| CANFD1_CH0_GFC | 0x40540080 | FULL | Global Filter Configuration |
| CANFD1_CH0_SIDFC | 0x40540084 | FULL | Standard ID Filter Configuration |
| CANFD1_CH0_XIDFC | 0x40540088 | FULL | Extended ID Filter Configuration |
| CANFD1_CH0_XIDAM | 0x40540090 | FULL | Extended ID AND Mask |
| CANFD1_CH0_HPMS | 0x40540094 | FULL | High Priority Message Status |
| CANFD1_CH0_NDAT1 | 0x40540098 | FULL | New Data 1 |
| CANFD1_CH0_NDAT2 | 0x4054009C | FULL | New Data 2 |
| CANFD1_CH0_RXF0C | 0x405400A0 | FULL | Rx FIFO 0 Configuration |
| CANFD1_CH0_RXF0S | 0x405400A4 | FULL | Rx FIFO 0 Status |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| CANFD1_CH0_RXF0A | 0x405400A8 | FULL | Rx FIFO 0 Acknowledge |
| CANFD1_CH0_RXBC | 0x405400AC | FULL | Rx Buffer Configuration |
| CANFD1_CH0_RXF1C | 0x405400B0 | FULL | Rx FIFO 1 Configuration |
| CANFD1_CH0_RXF1S | 0x405400B4 | FULL | Rx FIFO 1 Status |
| CANFD1_CH0_RXF1A | 0x405400B8 | FULL | Rx FIFO 1 Acknowledge |
| CANFD1_CH0_RXESC | 0x405400BC | FULL | Rx Buffer / FIFO Element Size Configuration |
| CANFD1_CH0_TXBC | 0x405400C0 | FULL | Tx Buffer Configuration |
| CANFD1_CH0_TXFQS | 0x405400C4 | FULL | Tx FIFO/Queue Status |
| CANFD1_CH0_TXESC | 0x405400C8 | FULL | Tx Buffer Element Size Configuration |
| CANFD1_CH0_TXBRP | 0x405400CC | FULL | Tx Buffer Request Pending |
| CANFD1_CH0_TXBAR | 0x405400D0 | FULL | Tx Buffer Add Request |
| CANFD1_CH0_TXBCR | 0x405400D4 | FULL | Tx Buffer Cancellation Request |
| CANFD1_CH0_TXBTO | 0x405400D8 | FULL | Tx Buffer Transmission Occurred |
| CANFD1_CH0_TXBCF | 0x405400DC | FULL | Tx Buffer Cancellation Finished |
| CANFD1_CH0_TXBTIE | 0x405400E0 | FULL | Tx Buffer Transmission Interrupt Enable |
| CANFD1_CH0_TXBCIE | 0x405400E4 | FULL | Tx Buffer Cancellation Finished Interrupt Enable |
| CANFD1_CH0_TXEFC | 0x405400F0 | FULL | Tx Event FIFO Configuration |
| CANFD1_CH0_TXEFS | 0x405400F4 | FULL | Tx Event FIFO Status |
| CANFD1_CH0_TXEFA | 0x405400F8 | FULL | Tx Event FIFO Acknowledge |
| CANFD1_CH0_TTTMC | 0x40540100 | FULL | TT Trigger Memory Configuration |
| CANFD1_CH0_TTRMC | 0x40540104 | FULL | TT Reference Message Configuration |
| CANFD1_CH0_TTOCF | 0x40540108 | FULL | TT Operation Configuration |
| CANFD1_CH0_TTMLM | 0x4054010C | FULL | TT Matrix Limits |
| CANFD1_CH0_TURCF | 0x40540110 | FULL | TUR Configuration |
| CANFD1_CH0_TTOCN | 0x40540114 | FULL | TT Operation Control |
| CANFD1_CH0_TTGTP | 0x40540118 | FULL | TT Global Time Preset |
| CANFD1_CH0_TTTMK | 0x4054011C | FULL | TT Time Mark |
| CANFD1_CH0_TTIR | 0x40540120 | FULL | TT Interrupt Register |
| CANFD1_CH0_TTIE | 0x40540124 | FULL | TT Interrupt Enable |
| CANFD1_CH0_TTILS | 0x40540128 | FULL | TT Interrupt Line Select |
| CANFD1_CH0_TTOST | 0x4054012C | FULL | TT Operation Status |
| CANFD1_CH0_TURNA | 0x40540130 | FULL | TUR Numerator Actual |
| CANFD1_CH0_TTLGT | 0x40540134 | FULL | TT Local & Global Time |
| CANFD1_CH0_TTCTC | 0x40540138 | FULL | TT Cycle Time & Count |
| CANFD1_CH0_TTCPT | 0x4054013C | FULL | TT Capture Time |
| CANFD1_CH0_TTCSM | 0x40540140 | FULL | TT Cycle Sync Mark |

### 2.2.2 CH 1

| Register Name | Address | Permission | Description |
|---|---|---|---|
| CANFD1_CH1_RXFTOP_CTL | 0x40540380 | FULL | Receive FIFO Top control |
| CANFD1_CH1_RXFTOP0_STAT | 0x405403A0 | FULL | Receive FIFO 0 Top Status |
| CANFD1_CH1_RXFTOP0_DATA | 0x405403A8 | FULL | Receive FIFO 0 Top Data |
| CANFD1_CH1_RXFTOP1_STAT | 0x405403B0 | FULL | Receive FIFO 1 Top Status |
| CANFD1_CH1_RXFTOP1_DATA | 0x405403B8 | FULL | Receive FIFO 1 Top Data |

#### 2.2.2.1 M_TTCAN

| Register Name | Address | Permission | Description |
|---|---|---|---|
| CANFD1_CH1_CREL | 0x40540200 | FULL | Core Release Register |
| CANFD1_CH1_ENDN | 0x40540204 | FULL | Endian Register |
| CANFD1_CH1_DBTP | 0x4054020C | FULL | Data Bit Timing & Prescaler Register |
| CANFD1_CH1_TEST | 0x40540210 | FULL | Test Register |
| CANFD1_CH1_RWD | 0x40540214 | FULL | RAM Watchdog |
| CANFD1_CH1_CCCR | 0x40540218 | FULL | CC Control Register |
| CANFD1_CH1_NBTP | 0x4054021C | FULL | Nominal Bit Timing & Prescaler Register |
| CANFD1_CH1_TSCC | 0x40540220 | FULL | Timestamp Counter Configuration |
| CANFD1_CH1_TSCV | 0x40540224 | FULL | Timestamp Counter Value |
| CANFD1_CH1_TOCC | 0x40540228 | FULL | Timeout Counter Configuration |
| CANFD1_CH1_TOCV | 0x4054022C | FULL | Timeout Counter Value |
| CANFD1_CH1_ECR | 0x40540240 | FULL | Error Counter Register |
| CANFD1_CH1_PSR | 0x40540244 | FULL | Protocol Status Register |
| CANFD1_CH1_TDCR | 0x40540248 | FULL | Transmitter Delay Compensation Register |
| CANFD1_CH1_IR | 0x40540250 | FULL | Interrupt Register |
| CANFD1_CH1_IE | 0x40540254 | FULL | Interrupt Enable |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| CANFD1_CH1_ILS | 0x40540258 | FULL | Interrupt Line Select |
| CANFD1_CH1_ILE | 0x4054025C | FULL | Interrupt Line Enable |
| CANFD1_CH1_GFC | 0x40540280 | FULL | Global Filter Configuration |
| CANFD1_CH1_SIDFC | 0x40540284 | FULL | Standard ID Filter Configuration |
| CANFD1_CH1_XIDFC | 0x40540288 | FULL | Extended ID Filter Configuration |
| CANFD1_CH1_XIDAM | 0x40540290 | FULL | Extended ID AND Mask |
| CANFD1_CH1_HPMS | 0x40540294 | FULL | High Priority Message Status |
| CANFD1_CH1_NDAT1 | 0x40540298 | FULL | New Data 1 |
| CANFD1_CH1_NDAT2 | 0x4054029C | FULL | New Data 2 |
| CANFD1_CH1_RXF0C | 0x405402A0 | FULL | Rx FIFO 0 Configuration |
| CANFD1_CH1_RXF0S | 0x405402A4 | FULL | Rx FIFO 0 Status |
| CANFD1_CH1_RXF0A | 0x405402A8 | FULL | Rx FIFO 0 Acknowledge |
| CANFD1_CH1_RXBC | 0x405402AC | FULL | Rx Buffer Configuration |
| CANFD1_CH1_RXF1C | 0x405402B0 | FULL | Rx FIFO 1 Configuration |
| CANFD1_CH1_RXF1S | 0x405402B4 | FULL | Rx FIFO 1 Status |
| CANFD1_CH1_RXF1A | 0x405402B8 | FULL | Rx FIFO 1 Acknowledge |
| CANFD1_CH1_RXESC | 0x405402BC | FULL | Rx Buffer / FIFO Element Size Configuration |
| CANFD1_CH1_TXBC | 0x405402C0 | FULL | Tx Buffer Configuration |
| CANFD1_CH1_TXFQS | 0x405402C4 | FULL | Tx FIFO/Queue Status |
| CANFD1_CH1_TXESC | 0x405402C8 | FULL | Tx Buffer Element Size Configuration |
| CANFD1_CH1_TXBRP | 0x405402CC | FULL | Tx Buffer Request Pending |
| CANFD1_CH1_TXBAR | 0x405402D0 | FULL | Tx Buffer Add Request |
| CANFD1_CH1_TXBCR | 0x405402D4 | FULL | Tx Buffer Cancellation Request |
| CANFD1_CH1_TXBTO | 0x405402D8 | FULL | Tx Buffer Transmission Occurred |
| CANFD1_CH1_TXBCF | 0x405402DC | FULL | Tx Buffer Cancellation Finished |
| CANFD1_CH1_TXBTIE | 0x405402E0 | FULL | Tx Buffer Transmission Interrupt Enable |
| CANFD1_CH1_TXBCIE | 0x405402E4 | FULL | Tx Buffer Cancellation Finished Interrupt Enable |
| CANFD1_CH1_TXEFC | 0x405402F0 | FULL | Tx Event FIFO Configuration |
| CANFD1_CH1_TXEFS | 0x405402F4 | FULL | Tx Event FIFO Status |
| CANFD1_CH1_TXEFA | 0x405402F8 | FULL | Tx Event FIFO Acknowledge |
| CANFD1_CH1_TTTMC | 0x40540300 | FULL | TT Trigger Memory Configuration |
| CANFD1_CH1_TTRMC | 0x40540304 | FULL | TT Reference Message Configuration |
| CANFD1_CH1_TTOCF | 0x40540308 | FULL | TT Operation Configuration |
| CANFD1_CH1_TTMLM | 0x4054030C | FULL | TT Matrix Limits |
| CANFD1_CH1_TURCF | 0x40540310 | FULL | TUR Configuration |
| CANFD1_CH1_TTOCN | 0x40540314 | FULL | TT Operation Control |
| CANFD1_CH1_TTGTP | 0x40540318 | FULL | TT Global Time Preset |
| CANFD1_CH1_TTTMK | 0x4054031C | FULL | TT Time Mark |
| CANFD1_CH1_TTIR | 0x40540320 | FULL | TT Interrupt Register |
| CANFD1_CH1_TTIE | 0x40540324 | FULL | TT Interrupt Enable |
| CANFD1_CH1_TTILS | 0x40540328 | FULL | TT Interrupt Line Select |
| CANFD1_CH1_TTOST | 0x4054032C | FULL | TT Operation Status |
| CANFD1_CH1_TURNA | 0x40540330 | FULL | TUR Numerator Actual |
| CANFD1_CH1_TTLGT | 0x40540334 | FULL | TT Local & Global Time |
| CANFD1_CH1_TTCTC | 0x40540338 | FULL | TT Cycle Time & Count |
| CANFD1_CH1_TTCPT | 0x4054033C | FULL | TT Capture Time |
| CANFD1_CH1_TTCSM | 0x40540340 | FULL | TT Cycle Sync Mark |

### 2.2.3 CH 2

| Register Name | Address | Permission | Description |
|---|---|---|---|
| CANFD1_CH2_RXFTOP_CTL | 0x40540580 | FULL | Receive FIFO Top control |
| CANFD1_CH2_RXFTOP0_STAT | 0x405405A0 | FULL | Receive FIFO 0 Top Status |
| CANFD1_CH2_RXFTOP0_DATA | 0x405405A8 | FULL | Receive FIFO 0 Top Data |
| CANFD1_CH2_RXFTOP1_STAT | 0x405405B0 | FULL | Receive FIFO 1 Top Status |
| CANFD1_CH2_RXFTOP1_DATA | 0x405405B8 | FULL | Receive FIFO 1 Top Data |

#### 2.2.3.1 M_TTCAN

| Register Name | Address | Permission | Description |
|---|---|---|---|
| CANFD1_CH2_CREL | 0x40540400 | FULL | Core Release Register |
| CANFD1_CH2_ENDN | 0x40540404 | FULL | Endian Register |
| CANFD1_CH2_DBTP | 0x4054040C | FULL | Data Bit Timing & Prescaler Register |
| CANFD1_CH2_TEST | 0x40540410 | FULL | Test Register |
| CANFD1_CH2_RWD | 0x40540414 | FULL | RAM Watchdog |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| CANFD1_CH2_CCCR | 0x40540418 | FULL | CC Control Register |
| CANFD1_CH2_NBTP | 0x4054041C | FULL | Nominal Bit Timing & Prescaler Register |
| CANFD1_CH2_TSCC | 0x40540420 | FULL | Timestamp Counter Configuration |
| CANFD1_CH2_TSCV | 0x40540424 | FULL | Timestamp Counter Value |
| CANFD1_CH2_TOCC | 0x40540428 | FULL | Timeout Counter Configuration |
| CANFD1_CH2_TOCV | 0x4054042C | FULL | Timeout Counter Value |
| CANFD1_CH2_ECR | 0x40540440 | FULL | Error Counter Register |
| CANFD1_CH2_PSR | 0x40540444 | FULL | Protocol Status Register |
| CANFD1_CH2_TDCR | 0x40540448 | FULL | Transmitter Delay Compensation Register |
| CANFD1_CH2_IR | 0x40540450 | FULL | Interrupt Register |
| CANFD1_CH2_IE | 0x40540454 | FULL | Interrupt Enable |
| CANFD1_CH2_ILS | 0x40540458 | FULL | Interrupt Line Select |
| CANFD1_CH2_ILE | 0x4054045C | FULL | Interrupt Line Enable |
| CANFD1_CH2_GFC | 0x40540480 | FULL | Global Filter Configuration |
| CANFD1_CH2_SIDFC | 0x40540484 | FULL | Standard ID Filter Configuration |
| CANFD1_CH2_XIDFC | 0x40540488 | FULL | Extended ID Filter Configuration |
| CANFD1_CH2_XIDAM | 0x40540490 | FULL | Extended ID AND Mask |
| CANFD1_CH2_HPMS | 0x40540494 | FULL | High Priority Message Status |
| CANFD1_CH2_NDAT1 | 0x40540498 | FULL | New Data 1 |
| CANFD1_CH2_NDAT2 | 0x4054049C | FULL | New Data 2 |
| CANFD1_CH2_RXF0C | 0x405404A0 | FULL | Rx FIFO 0 Configuration |
| CANFD1_CH2_RXF0S | 0x405404A4 | FULL | Rx FIFO 0 Status |
| CANFD1_CH2_RXF0A | 0x405404A8 | FULL | Rx FIFO 0 Acknowledge |
| CANFD1_CH2_RXBC | 0x405404AC | FULL | Rx Buffer Configuration |
| CANFD1_CH2_RXF1C | 0x405404B0 | FULL | Rx FIFO 1 Configuration |
| CANFD1_CH2_RXF1S | 0x405404B4 | FULL | Rx FIFO 1 Status |
| CANFD1_CH2_RXF1A | 0x405404B8 | FULL | Rx FIFO 1 Acknowledge |
| CANFD1_CH2_RXESC | 0x405404BC | FULL | Rx Buffer / FIFO Element Size Configuration |
| CANFD1_CH2_TXBC | 0x405404C0 | FULL | Tx Buffer Configuration |
| CANFD1_CH2_TXFQS | 0x405404C4 | FULL | Tx FIFO/Queue Status |
| CANFD1_CH2_TXESC | 0x405404C8 | FULL | Tx Buffer Element Size Configuration |
| CANFD1_CH2_TXBRP | 0x405404CC | FULL | Tx Buffer Request Pending |
| CANFD1_CH2_TXBAR | 0x405404D0 | FULL | Tx Buffer Add Request |
| CANFD1_CH2_TXBCR | 0x405404D4 | FULL | Tx Buffer Cancellation Request |
| CANFD1_CH2_TXBTO | 0x405404D8 | FULL | Tx Buffer Transmission Occurred |
| CANFD1_CH2_TXBCF | 0x405404DC | FULL | Tx Buffer Cancellation Finished |
| CANFD1_CH2_TXBTIE | 0x405404E0 | FULL | Tx Buffer Transmission Interrupt Enable |
| CANFD1_CH2_TXBCIE | 0x405404E4 | FULL | Tx Buffer Cancellation Finished Interrupt Enable |
| CANFD1_CH2_TXEFC | 0x405404F0 | FULL | Tx Event FIFO Configuration |
| CANFD1_CH2_TXEFS | 0x405404F4 | FULL | Tx Event FIFO Status |
| CANFD1_CH2_TXEFA | 0x405404F8 | FULL | Tx Event FIFO Acknowledge |
| CANFD1_CH2_TTTMC | 0x40540500 | FULL | TT Trigger Memory Configuration |
| CANFD1_CH2_TTRMC | 0x40540504 | FULL | TT Reference Message Configuration |
| CANFD1_CH2_TTOCF | 0x40540508 | FULL | TT Operation Configuration |
| CANFD1_CH2_TTMLM | 0x4054050C | FULL | TT Matrix Limits |
| CANFD1_CH2_TURCF | 0x40540510 | FULL | TUR Configuration |
| CANFD1_CH2_TTOCN | 0x40540514 | FULL | TT Operation Control |
| CANFD1_CH2_TTGTP | 0x40540518 | FULL | TT Global Time Preset |
| CANFD1_CH2_TTTMK | 0x4054051C | FULL | TT Time Mark |
| CANFD1_CH2_TTIR | 0x40540520 | FULL | TT Interrupt Register |
| CANFD1_CH2_TTIE | 0x40540524 | FULL | TT Interrupt Enable |
| CANFD1_CH2_TTILS | 0x40540528 | FULL | TT Interrupt Line Select |
| CANFD1_CH2_TTOST | 0x4054052C | FULL | TT Operation Status |
| CANFD1_CH2_TURNA | 0x40540530 | FULL | TUR Numerator Actual |
| CANFD1_CH2_TTLGT | 0x40540534 | FULL | TT Local & Global Time |
| CANFD1_CH2_TTCTC | 0x40540538 | FULL | TT Cycle Time & Count |
| CANFD1_CH2_TTCPT | 0x4054053C | FULL | TT Capture Time |
| CANFD1_CH2_TTCSM | 0x40540540 | FULL | TT Cycle Sync Mark |

### 2.2.4 CH 3

| Register Name | Address | Permission | Description |
|---|---|---|---|
| CANFD1_CH3_RXFTOP_CTL | 0x40540780 | FULL | Receive FIFO Top control |
| CANFD1_CH3_RXFTOP0_STAT | 0x405407A0 | FULL | Receive FIFO 0 Top Status |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| CANFD1_CH3_RXFTOP0_DATA | 0x405407A8 | FULL | Receive FIFO 0 Top Data |
| CANFD1_CH3_RXFTOP1_STAT | 0x405407B0 | FULL | Receive FIFO 1 Top Status |
| CANFD1_CH3_RXFTOP1_DATA | 0x405407B8 | FULL | Receive FIFO 1 Top Data |

#### 2.2.4.1 M_TTCAN

| Register Name | Address | Permission | Description |
|---|---|---|---|
| CANFD1_CH3_CREL | 0x40540600 | FULL | Core Release Register |
| CANFD1_CH3_ENDN | 0x40540604 | FULL | Endian Register |
| CANFD1_CH3_DBTP | 0x4054060C | FULL | Data Bit Timing & Prescaler Register |
| CANFD1_CH3_TEST | 0x40540610 | FULL | Test Register |
| CANFD1_CH3_RWD | 0x40540614 | FULL | RAM Watchdog |
| CANFD1_CH3_CCCR | 0x40540618 | FULL | CC Control Register |
| CANFD1_CH3_NBTP | 0x4054061C | FULL | Nominal Bit Timing & Prescaler Register |
| CANFD1_CH3_TSCC | 0x40540620 | FULL | Timestamp Counter Configuration |
| CANFD1_CH3_TSCV | 0x40540624 | FULL | Timestamp Counter Value |
| CANFD1_CH3_TOCC | 0x40540628 | FULL | Timeout Counter Configuration |
| CANFD1_CH3_TOCV | 0x4054062C | FULL | Timeout Counter Value |
| CANFD1_CH3_ECR | 0x40540640 | FULL | Error Counter Register |
| CANFD1_CH3_PSR | 0x40540644 | FULL | Protocol Status Register |
| CANFD1_CH3_TDCR | 0x40540648 | FULL | Transmitter Delay Compensation Register |
| CANFD1_CH3_IR | 0x40540650 | FULL | Interrupt Register |
| CANFD1_CH3_IE | 0x40540654 | FULL | Interrupt Enable |
| CANFD1_CH3_ILS | 0x40540658 | FULL | Interrupt Line Select |
| CANFD1_CH3_ILE | 0x4054065C | FULL | Interrupt Line Enable |
| CANFD1_CH3_GFC | 0x40540680 | FULL | Global Filter Configuration |
| CANFD1_CH3_SIDFC | 0x40540684 | FULL | Standard ID Filter Configuration |
| CANFD1_CH3_XIDFC | 0x40540688 | FULL | Extended ID Filter Configuration |
| CANFD1_CH3_XIDAM | 0x40540690 | FULL | Extended ID AND Mask |
| CANFD1_CH3_HPMS | 0x40540694 | FULL | High Priority Message Status |
| CANFD1_CH3_NDAT1 | 0x40540698 | FULL | New Data 1 |
| CANFD1_CH3_NDAT2 | 0x4054069C | FULL | New Data 2 |
| CANFD1_CH3_RXF0C | 0x405406A0 | FULL | Rx FIFO 0 Configuration |
| CANFD1_CH3_RXF0S | 0x405406A4 | FULL | Rx FIFO 0 Status |
| CANFD1_CH3_RXF0A | 0x405406A8 | FULL | Rx FIFO 0 Acknowledge |
| CANFD1_CH3_RXBC | 0x405406AC | FULL | Rx Buffer Configuration |
| CANFD1_CH3_RXF1C | 0x405406B0 | FULL | Rx FIFO 1 Configuration |
| CANFD1_CH3_RXF1S | 0x405406B4 | FULL | Rx FIFO 1 Status |
| CANFD1_CH3_RXF1A | 0x405406B8 | FULL | Rx FIFO 1 Acknowledge |
| CANFD1_CH3_RXESC | 0x405406BC | FULL | Rx Buffer / FIFO Element Size Configuration |
| CANFD1_CH3_TXBC | 0x405406C0 | FULL | Tx Buffer Configuration |
| CANFD1_CH3_TXFQS | 0x405406C4 | FULL | Tx FIFO/Queue Status |
| CANFD1_CH3_TXESC | 0x405406C8 | FULL | Tx Buffer Element Size Configuration |
| CANFD1_CH3_TXBRP | 0x405406CC | FULL | Tx Buffer Request Pending |
| CANFD1_CH3_TXBAR | 0x405406D0 | FULL | Tx Buffer Add Request |
| CANFD1_CH3_TXBCR | 0x405406D4 | FULL | Tx Buffer Cancellation Request |
| CANFD1_CH3_TXBTO | 0x405406D8 | FULL | Tx Buffer Transmission Occurred |
| CANFD1_CH3_TXBCF | 0x405406DC | FULL | Tx Buffer Cancellation Finished |
| CANFD1_CH3_TXBTIE | 0x405406E0 | FULL | Tx Buffer Transmission Interrupt Enable |
| CANFD1_CH3_TXBCIE | 0x405406E4 | FULL | Tx Buffer Cancellation Finished Interrupt Enable |
| CANFD1_CH3_TXEFC | 0x405406F0 | FULL | Tx Event FIFO Configuration |
| CANFD1_CH3_TXEFS | 0x405406F4 | FULL | Tx Event FIFO Status |
| CANFD1_CH3_TXEFA | 0x405406F8 | FULL | Tx Event FIFO Acknowledge |
| CANFD1_CH3_TTTMC | 0x40540700 | FULL | TT Trigger Memory Configuration |
| CANFD1_CH3_TTRMC | 0x40540704 | FULL | TT Reference Message Configuration |
| CANFD1_CH3_TTOCF | 0x40540708 | FULL | TT Operation Configuration |
| CANFD1_CH3_TTMLM | 0x4054070C | FULL | TT Matrix Limits |
| CANFD1_CH3_TURCF | 0x40540710 | FULL | TUR Configuration |
| CANFD1_CH3_TTOCN | 0x40540714 | FULL | TT Operation Control |
| CANFD1_CH3_TTGTP | 0x40540718 | FULL | TT Global Time Preset |
| CANFD1_CH3_TTTMK | 0x4054071C | FULL | TT Time Mark |
| CANFD1_CH3_TTIR | 0x40540720 | FULL | TT Interrupt Register |
| CANFD1_CH3_TTIE | 0x40540724 | FULL | TT Interrupt Enable |
| CANFD1_CH3_TTILS | 0x40540728 | FULL | TT Interrupt Line Select |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| CANFD1_CH3_TTOST | 0x4054072C | FULL | TT Operation Status |
| CANFD1_CH3_TURNA | 0x40540730 | FULL | TUR Numerator Actual |
| CANFD1_CH3_TTLGT | 0x40540734 | FULL | TT Local & Global Time |
| CANFD1_CH3_TTCTC | 0x40540738 | FULL | TT Cycle Time & Count |
| CANFD1_CH3_TTCPT | 0x4054073C | FULL | TT Capture Time |
| CANFD1_CH3_TTCSM | 0x40540740 | FULL | TT Cycle Sync Mark |

### 2.2.5 CH 4

| Register Name | Address | Permission | Description |
|---|---|---|---|
| CANFD1_CH4_RXFTOP_CTL | 0x40540980 | FULL | Receive FIFO Top control |
| CANFD1_CH4_RXFTOP0_STAT | 0x405409A0 | FULL | Receive FIFO 0 Top Status |
| CANFD1_CH4_RXFTOP0_DATA | 0x405409A8 | FULL | Receive FIFO 0 Top Data |
| CANFD1_CH4_RXFTOP1_STAT | 0x405409B0 | FULL | Receive FIFO 1 Top Status |
| CANFD1_CH4_RXFTOP1_DATA | 0x405409B8 | FULL | Receive FIFO 1 Top Data |

#### 2.2.5.1 M_TTCAN

| Register Name | Address | Permission | Description |
|---|---|---|---|
| CANFD1_CH4_CREL | 0x40540800 | FULL | Core Release Register |
| CANFD1_CH4_ENDN | 0x40540804 | FULL | Endian Register |
| CANFD1_CH4_DBTP | 0x4054080C | FULL | Data Bit Timing & Prescaler Register |
| CANFD1_CH4_TEST | 0x40540810 | FULL | Test Register |
| CANFD1_CH4_RWD | 0x40540814 | FULL | RAM Watchdog |
| CANFD1_CH4_CCCR | 0x40540818 | FULL | CC Control Register |
| CANFD1_CH4_NBTP | 0x4054081C | FULL | Nominal Bit Timing & Prescaler Register |
| CANFD1_CH4_TSCC | 0x40540820 | FULL | Timestamp Counter Configuration |
| CANFD1_CH4_TSCV | 0x40540824 | FULL | Timestamp Counter Value |
| CANFD1_CH4_TOCC | 0x40540828 | FULL | Timeout Counter Configuration |
| CANFD1_CH4_TOCV | 0x4054082C | FULL | Timeout Counter Value |
| CANFD1_CH4_ECR | 0x40540840 | FULL | Error Counter Register |
| CANFD1_CH4_PSR | 0x40540844 | FULL | Protocol Status Register |
| CANFD1_CH4_TDCR | 0x40540848 | FULL | Transmitter Delay Compensation Register |
| CANFD1_CH4_IR | 0x40540850 | FULL | Interrupt Register |
| CANFD1_CH4_IE | 0x40540854 | FULL | Interrupt Enable |
| CANFD1_CH4_ILS | 0x40540858 | FULL | Interrupt Line Select |
| CANFD1_CH4_ILE | 0x4054085C | FULL | Interrupt Line Enable |
| CANFD1_CH4_GFC | 0x40540880 | FULL | Global Filter Configuration |
| CANFD1_CH4_SIDFC | 0x40540884 | FULL | Standard ID Filter Configuration |
| CANFD1_CH4_XIDFC | 0x40540888 | FULL | Extended ID Filter Configuration |
| CANFD1_CH4_XIDAM | 0x40540890 | FULL | Extended ID AND Mask |
| CANFD1_CH4_HPMS | 0x40540894 | FULL | High Priority Message Status |
| CANFD1_CH4_NDAT1 | 0x40540898 | FULL | New Data 1 |
| CANFD1_CH4_NDAT2 | 0x4054089C | FULL | New Data 2 |
| CANFD1_CH4_RXF0C | 0x405408A0 | FULL | Rx FIFO 0 Configuration |
| CANFD1_CH4_RXF0S | 0x405408A4 | FULL | Rx FIFO 0 Status |
| CANFD1_CH4_RXF0A | 0x405408A8 | FULL | Rx FIFO 0 Acknowledge |
| CANFD1_CH4_RXBC | 0x405408AC | FULL | Rx Buffer Configuration |
| CANFD1_CH4_RXF1C | 0x405408B0 | FULL | Rx FIFO 1 Configuration |
| CANFD1_CH4_RXF1S | 0x405408B4 | FULL | Rx FIFO 1 Status |
| CANFD1_CH4_RXF1A | 0x405408B8 | FULL | Rx FIFO 1 Acknowledge |
| CANFD1_CH4_RXESC | 0x405408BC | FULL | Rx Buffer / FIFO Element Size Configuration |
| CANFD1_CH4_TXBC | 0x405408C0 | FULL | Tx Buffer Configuration |
| CANFD1_CH4_TXFQS | 0x405408C4 | FULL | Tx FIFO/Queue Status |
| CANFD1_CH4_TXESC | 0x405408C8 | FULL | Tx Buffer Element Size Configuration |
| CANFD1_CH4_TXBRP | 0x405408CC | FULL | Tx Buffer Request Pending |
| CANFD1_CH4_TXBAR | 0x405408D0 | FULL | Tx Buffer Add Request |
| CANFD1_CH4_TXBCR | 0x405408D4 | FULL | Tx Buffer Cancellation Request |
| CANFD1_CH4_TXBTO | 0x405408D8 | FULL | Tx Buffer Transmission Occurred |
| CANFD1_CH4_TXBCF | 0x405408DC | FULL | Tx Buffer Cancellation Finished |
| CANFD1_CH4_TXBTIE | 0x405408E0 | FULL | Tx Buffer Transmission Interrupt Enable |
| CANFD1_CH4_TXBCIE | 0x405408E4 | FULL | Tx Buffer Cancellation Finished Interrupt Enable |
| CANFD1_CH4_TXEFC | 0x405408F0 | FULL | Tx Event FIFO Configuration |
| CANFD1_CH4_TXEFS | 0x405408F4 | FULL | Tx Event FIFO Status |
| CANFD1_CH4_TXEFA | 0x405408F8 | FULL | Tx Event FIFO Acknowledge |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| CANFD1_CH4_TTTMC | 0x40540900 | FULL | TT Trigger Memory Configuration |
| CANFD1_CH4_TTRMC | 0x40540904 | FULL | TT Reference Message Configuration |
| CANFD1_CH4_TTOCF | 0x40540908 | FULL | TT Operation Configuration |
| CANFD1_CH4_TTMLM | 0x4054090C | FULL | TT Matrix Limits |
| CANFD1_CH4_TURCF | 0x40540910 | FULL | TUR Configuration |
| CANFD1_CH4_TTOCN | 0x40540914 | FULL | TT Operation Control |
| CANFD1_CH4_TTGTP | 0x40540918 | FULL | TT Global Time Preset |
| CANFD1_CH4_TTTMK | 0x4054091C | FULL | TT Time Mark |
| CANFD1_CH4_TTIR | 0x40540920 | FULL | TT Interrupt Register |
| CANFD1_CH4_TTIE | 0x40540924 | FULL | TT Interrupt Enable |
| CANFD1_CH4_TTILS | 0x40540928 | FULL | TT Interrupt Line Select |
| CANFD1_CH4_TTOST | 0x4054092C | FULL | TT Operation Status |
| CANFD1_CH4_TURNA | 0x40540930 | FULL | TUR Numerator Actual |
| CANFD1_CH4_TTLGT | 0x40540934 | FULL | TT Local & Global Time |
| CANFD1_CH4_TTCTC | 0x40540938 | FULL | TT Cycle Time & Count |
| CANFD1_CH4_TTCPT | 0x4054093C | FULL | TT Capture Time |
| CANFD1_CH4_TTCSM | 0x40540940 | FULL | TT Cycle Sync Mark |

## 2.3 Register Details

### 2.3.1 CANFD_CTL

**Description:** Global CAN control register
**Address:** 0x40521000
**Offset:** 0x1000
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:5] | | | STOP_REQ [4:0] | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | MRAM_OFF [31:31] | None [30:24] | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:4 | STOP_REQ | RW | R | 0 | Clock Stop Request for each TTCAN IP .<br>The m_ttcan_clkstop_req of each TTCAN IP is directly driven by these bits. |
| 31 | MRAM_OFF | RW | R | 0 | MRAM off<br>0= Default MRAM on (with MRAM retained in DeepSleep).<br>1= Switch MRAM off (not retained) to save power. Before setting this bit all the CAN channels have to be powered down using the STOP_REQ/ACK bits. When the MRAM is off any access attempt to it is considered an address error (as if MRAM_SIZE=0). After switching the MRAM on again software needs to allow for a certain power up time before MRAM can be used, i.e. before STOP_REQ can be de-asserted. The power up time is equivalent to the system SRAM power up time specified in the CPUSS.RAM_PWR_DELAY_CTL register.<br><br>MRAM_OFF should be set to 0 prior to transitioning to Hibernate mode. |

### 2.3.2 CANFD_STATUS

**Description:** Global CAN status register
**Address:** 0x40521004
**Offset:** 0x1004
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:5] | | | STOP_ACK [4:0] | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:4 | STOP_ACK | R | RW | 0 | Clock Stop Acknowledge for each TTCAN IP.<br>These bits are directly driven by m_ttcan_clkstop_ack of each TTCAN IP.<br>When this bit is set the corresponding TTCAN IP clocks will be gated off, except HCLK will enabled for each AHB write |

### 2.3.3 CANFD_INTR0_CAUSE

**Description:** Consolidated interrupt0 cause register
**Address:** 0x40521010
**Offset:** 0x1010
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:5] | | | INT0 [4:0] | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:4 | INT0 | R | RW | 0 | Show pending m_ttcan_int0 of each channel |

### 2.3.4 CANFD_INTR1_CAUSE

**Description:** Consolidated interrupt1 cause register
**Address:** 0x40521014
**Offset:** 0x1014
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:5] | | | INT1 [4:0] | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:4 | INT1 | R | RW | 0 | Show pending m_ttcan_int1 of each channel |

### 2.3.5 CANFD_TS_CTL

**Description:** Time Stamp control register
**Address:** 0x40521020
**Offset:** 0x1020
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | PRESCALE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | PRESCALE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | ENABLED [31:31] | None [30:24] | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | PRESCALE | RW | R | 0 | Time Stamp counter prescale value.<br>When enabled divide the Host clock (HCLK) by PRESCALE+1 to create Time Stamp clock ticks. |
| 31 | ENABLED | RW | R | 0 | Counter enable bit<br>0 = Count disabled. Stop counting up and keep the counter value<br>1 = Count enabled. Start counting up from the current value |

### 2.3.6 CANFD_TS_CNT

**Description:** Time Stamp counter value
**Address:** 0x40521024
**Offset:** 0x1024
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** Not retained
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | VALUE | RW | A | 0 | The counter value of the Time Stamp Counter.<br>When enabled this counter will count Time Stamp clock ticks from the pre-scaler.<br>When written this counter and the pre-scaler will reset to 0 (write data is ignored). |

### 2.3.7 CANFD_ECC_CTL

**Description:** ECC control
**Address:** 0x40521080
**Offset:** 0x1080
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:17] | | | | | | | ECC_EN [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 16 | ECC_EN | RW | R | 0 | Enable ECC for CANFD SRAM<br>When disabled also all error injection functionality is disabled. |

### 2.3.8 CANFD_ECC_ERR_INJ

**Description:** ECC error injection
**Address:** 0x40521084
**Offset:** 0x1084
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xFFFC

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | ERR_ADDR [7:2] | | | | | | None [1:0] | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | ERR_ADDR [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:21] | | | ERR_EN [20:20] | None [19:16] | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:31] | ERR_PAR [30:24] | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 2:15 | ERR_ADDR | RW | R | 16383 | Specifies the address of the word where an error will be injected on write or an non-correctable error will be suppressed.<br>When the ERR_EN bit is set an error parity (ERR_PAR) is injected when any write, from bus or a CAN channel, is done to this address.<br>When the ERR_EN bit is set and the access address matches ERR_ADDR then a non-correctable ECC error or an Address error will NOT result in a bus error or CAN channel shutdown.<br>Note that error reporting to the fault structure cannot be suppressed. |
| 20 | ERR_EN | RW | R | 0 | Enable error injection (ECC_EN must be 1).<br>When this bit is set the error parity (ERR_PAR) will be used when an AHB write is done to the ERR_ADDR address.<br>When the error word is read a single or double error will be reported to the fault structure just like for a real ECC error (even if this bit is no longer set).<br>When this bit is set (and ECC_EN=1) a non-correctable error (ECC or address error) for the ERR_ADDR will not be reported back to the CAN channel or AHB bus. |
| 24:30 | ERR_PAR | RW | R | 0 | ECC Parity bits to use for ECC error injection at address ERR_ADDR. |

### 2.3.9 CH

#### 2.3.9.1 CANFD_CH_RXFTOP_CTL

**Description:** Receive FIFO Top control
**Address:** 0x40520180
**Offset:** 0x180
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:2] | | | | | | F1TPE [1:1] | F0TPE [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | F0TPE | RW | R | 0 | FIFO 0 Top Pointer Enable.<br>This enables the FIFO top pointer logic to set the FIFO Top Address (FnTA) and message word counter.<br>This logic is also disabled when the IP is being reconfigured (CCCR.CCE=1).<br>When this logic is disabled a Read from RXFTOP0_DATA is undefined. |
| 1 | F1TPE | RW | R | 0 | FIFO 1 Top Pointer Enable. |

### 2.3.9.2 CANFD_CH_RXFTOP0_STAT

**Description:** Receive FIFO 0 Top Status
**Address:** 0x405201A0
**Offset:** 0x1A0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | F0TA [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | F0TA [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | F0TA | R | RW | 0 | Current FIFO 0 Top Address.<br>This is a pointer to the next word in the message buffer defined by the FIFO Start Address (FnSA), Get Index (FnGI), the FIFO message size (FnDS) and the message word counter (FnMWC)<br>FnTA = FnSA + FnGI * msg_size[FnDS] + FnMWC |

### 2.3.9.3 CANFD_CH_RXFTOP0_DATA

**Description:** Receive FIFO 0 Top Data
**Address:** 0x405201A8
**Offset:** 0x1A8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Read side effect, except if read from debug host
**Default:** Undefined as one or more bit fields have a default value that is undefined

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | F0TD [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | F0TD [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | F0TD [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | F0TD [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | F0TD | R | W | Undefined | When enabled (F0TPE=1) read data from MRAM at location FnTA. This register can have a read side effect if the following conditions are met:<br>- M_TTCAN not being reconfigured (CCCR.CCE=0)<br>- FIFO Top Pointer logic is enabled (FnTPE=1)<br>- FIFO is not empty (FnFL!=0)<br>The read side effect is as follows:<br>- if FnMWC pointed to the last word of the message (as indicated by FnDS) then the corresponding message index (FnGI) is automatically acknowledge by a write to FnAI<br>- FnMWC is incremented (or restarted if FnMWC pointed to the last word of the message)<br>- the FIFO top address FnTA is incremented (with FIFO wrap around)<br>When this logic is disabled (F0TPE=0) a Read from this register returns undefined data. |

### 2.3.9.4 CANFD_CH_RXFTOP1_STAT

**Description:** Receive FIFO 1 Top Status
**Address:** 0x405201B0
**Offset:** 0x1B0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | F1TA [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | F1TA [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | F1TA | R | RW | 0 | See F0TA description |

### 2.3.9.5 CANFD_CH_RXFTOP1_DATA

**Description:** Receive FIFO 1 Top Data
**Address:** 0x405201B8
**Offset:** 0x1B8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Read side effect, except if read from debug host
**Default:** Undefined as one or more bit fields have a default value that is undefined

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | F1TD [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | F1TD [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | F1TD [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | F1TD [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | F1TD | R | W | Undefined | See F0TD description |

### 2.3.9.6 M_TTCAN

#### 2.3.9.6.1 CANFD_CH_CREL

**Description:** Core Release Register
**Address:** 0x40520000
**Offset:** 0x0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x32380609

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DAY [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | MON [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | SUBSTEP [23:20] | | | | YEAR [19:16] | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | REL [31:28] | | | | STEP [27:24] | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | DAY | R | R | 9 | Time Stamp Day<br>Two digits, BCD-coded. This field is set by generic parameter on M_TTCAN synthesis. |
| 8:15 | MON | R | R | 6 | Time Stamp Month<br>Two digits, BCD-coded. This field is set by generic parameter on M_TTCAN synthesis. |
| 16:19 | YEAR | R | R | 8 | Time Stamp Year<br>One digit, BCD-coded. This field is set by generic parameter on M_TTCAN synthesis. |
| 20:23 | SUBSTEP | R | R | 3 | Sub-step of Core Release<br>One digit, BCD-coded. |
| 24:27 | STEP | R | R | 2 | Step of Core Release<br>One digit, BCD-coded. |
| 28:31 | REL | R | R | 3 | Core Release<br>One digit, BCD-coded. |

#### 2.3.9.6.2 CANFD_CH_ENDN

**Description:** Endian Register
**Address:** 0x40520004
**Offset:** 0x4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x87654321

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | ETV [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | ETV [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | ETV [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | ETV [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | ETV | R | R | 2271560481 | Endianness Test Value<br>The endianness test value is 0x87654321. |

#### 2.3.9.6.3 CANFD_CH_DBTP

**Description:** Data Bit Timing & Prescaler Register
**Address:** 0x4052000C
**Offset:** 0xC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Protected Write
**Default:** 0xA33

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DTSEG2 [7:4] | | | | DSJW [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:13] | | | DTSEG1 [12:8] | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | TDC [23:23] | None [22:21] | | DBRP [20:16] | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | DSJW | RW | R | 3 | Data (Re)Synchronization Jump Width<br>0x0-0xF Valid values are 0 to 15. The actual interpretation by the hardware of this value is such that one more than the value programmed here is used. |
| 4:7 | DTSEG2 | RW | R | 3 | Data time segment after sample point<br>0x0-0xF Valid values are 0 to 15. The actual interpretation by the hardware of this value is such that one more than the programmed value is used. |
| 8:12 | DTSEG1 | RW | R | 10 | Data time segment before sample point<br>0x00-0x1F Valid values are 0 to 31. The actual interpretation by the hardware of this value is such that one more than the programmed value is used. |
| 16:20 | DBRP | RW | R | 0 | Data Bit Rate Prescaler<br>0x00-0x1F The value by which the oscillator frequency is divided for generating the bit time quanta. The bit time is built up from a multiple of this quanta. Valid values for the Bit Rate Prescaler are 0 to 31. The actual interpretation by the hardware of this value is such that one more than the value programmed here is used. |
| 23 | TDC | RW | R | 0 | Transmitter Delay Compensation<br>0= Transmitter Delay Compensation disabled<br>1= Transmitter Delay Compensation enabled |

### 2.3.9.6.4 CANFD_CH_TEST

**Description:** Test Register
**Address:** 0x40520010
**Offset:** 0x10
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Protected Write
**Default:** Undefined as one or more bit fields have a default value that is undefined

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | RX [7:7] | TX [6:5] | | LBCK [4:4] | CAT [3:3] | CAM [2:2] | TAT [1:1] | TAM [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | TAM | RW | R | 0 | ASC is not supported by M_TTCAN<br>Test ASC Multiplexer Control<br>Controls output pin m_ttcan_ascm in test mode, ORed with the signal from the FSE<br>0= Level at pin m_ttcan_ascm controlled by FSE<br>1= Level at pin m_ttcan_ascm = '1' |
| 1 | TAT | RW | R | 0 | ASC is not supported by M_TTCAN<br>Test ASC Transmit Control<br>Controls output pin m_ttcan_asct in test mode, ORed with the signal from the FSE<br>0= Level at pin m_ttcan_asct controlled by FSE<br>1= Level at pin m_ttcan_asct = '1' |
| 2 | CAM | RW | R | 0 | ASC is not supported by M_TTCAN<br>Check ASC Multiplexer Control<br>Monitors level at output pin m_ttcan_ascm.<br>0= Output pin m_ttcan_ascm = '0'<br>1= Output pin m_ttcan_ascm = '1' |
| 3 | CAT | RW | R | 0 | ASC is not supported by M_TTCAN<br>Check ASC Transmit Control<br>Monitors level at output pin m_ttcan_asct.<br>0= Output pin m_ttcan_asct = '0' |
| 4 | LBCK | RW | R | 0 | Loop Back Mode<br>0= Reset value, Loop Back Mode is disabled<br>1= Loop Back Mode is enabled (Test Modes) |
| 5:6 | TX | RW | R | 0 | Control of Transmit Pin<br>00 Reset value, m_ttcan_tx controlled by the CAN Core, updated at the end of the CAN bit time<br>01 Sample Point can be monitored at pin m_ttcan_tx<br>10 Dominant ('0') level at pin m_ttcan_tx<br>11 Recessive ('1') at pin m_ttcan_tx |
| 7 | RX | R | R | Undefined | Receive Pin<br>Monitors the actual value of pin m_ttcan_rx<br>0= The CAN bus is dominant (m_ttcan_rx = '0')<br>1= The CAN bus is recessive (m_ttcan_rx = '1') |

### 2.3.9.6.5 CANFD_CH_RWD

**Description:** RAM Watchdog
**Address:** 0x40520014
**Offset:** 0x14
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Protected Write
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | WDC [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | WDV [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | WDC | RW | R | 0 | Watchdog Configuration<br>Start value of the Message RAM Watchdog Counter. With the reset value of '00' the counter is disabled. |
| 8:15 | WDV | R | R | 0 | Watchdog Value<br>Actual Message RAM Watchdog Counter Value. |

### 2.3.9.6.6 CANFD_CH_CCCR

**Description:** CC Control Register
**Address:** 0x40520018
**Offset:** 0x18
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Protected Write
**Default:** 0x1

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | TEST [7:7] | DAR [6:6] | MON_ [5:5] | CSR [4:4] | CSA [3:3] | ASM [2:2] | CCE [1:1] | INIT [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | NISO [15:15] | TXP [14:14] | EFBI [13:13] | PXHD [12:12] | None [11:10] | | BRSE [9:9] | FDOE [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | INIT | RW | R | 1 | Initialization<br>0= Normal Operation<br>1= Initialization is started |
| 1 | CCE | RW | R | 0 | Configuration Change Enable<br>0= The CPU has no write access to the protected configuration registers<br>1= The CPU has write access to the protected configuration registers (while CCCR.INIT = '1') |
| 2 | ASM | RW | R | 0 | Restricted Operation Mode<br>Bit ASM can only be set by the Host when both CCE and INIT are set to '1'. The bit can be reset by the Host at any time. For a description of the Restricted Operation Mode.<br>0= Normal CAN operation<br>1= Restricted Operation Mode active |
| 3 | CSA | RW | R | 0 | Clock Stop Acknowledge<br>0= No clock stop acknowledged<br>1= M_TTCAN may be set in power down by stopping m_ttcan_hclk and m_ttcan_cclk |
| 4 | CSR | RW | R | 0 | Clock Stop Request, not supported by M_TTCAN use CTL.STOP_REQ at the group level instead.<br>0= No clock stop is requested<br>1= Clock stop requested. When clock stop is requested, first INIT and then CSA will be set after all pending transfer requests have been completed and the CAN bus reached idle. |
| 5 | MON_ | RW | R | 0 | Bus Monitoring Mode<br>Bit MON can only be set by the Host when both CCE and INIT are set to '1'. The bit can be reset by the Host at any time.<br>0= Bus Monitoring Mode is disabled<br>1= Bus Monitoring Mode is enabled |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 6 | DAR | RW | R | 0 | Disable Automatic Retransmission<br>0= Automatic retransmission of messages not transmitted successfully enabled<br>1= Automatic retransmission disabled |
| 7 | TEST | RW | R | 0 | Test Mode Enable<br>0= Normal operation, register TEST holds reset values<br>1= Test Mode, write access to register TEST enabled |
| 8 | FDOE | RW | R | 0 | FD Operation Enable<br>0= FD operation disabled<br>1= FD operation enabled |
| 9 | BRSE | RW | R | 0 | Bit Rate Switch Enable<br>0= Bit rate switching for transmissions disabled<br>1= Bit rate switching for transmissions enabled |
| 12 | PXHD | RW | R | 0 | Protocol Exception Handling Disable<br>0= Protocol exception handling enabled<br>1= Protocol exception handling disabled |
| 13 | EFBI | RW | R | 0 | Edge Filtering during Bus Integration<br>0= Edge filtering disabled<br>1= Two consecutive dominant tq required to detect an edge for hard synchronization |
| 14 | TXP | RW | R | 0 | Transmit Pause<br>If this bit is set, the M_TTCAN pauses for two CAN bit times before starting the next transmission<br>after itself has successfully transmitted a frame.<br>0= Transmit pause disabled<br>1= Transmit pause enabled |
| 15 | NISO | RW | R | 0 | Non ISO Operation<br>If this bit is set, the M_TTCAN uses the CAN FD frame format as specified by the Bosch CAN FD Specification V1.0.<br>0= CAN FD frame format according to ISO 11898-1:2015<br>1= CAN FD frame format according to Bosch CAN FD Specification V1.0 addressing the non-ISO CAN FD |

### 2.3.9.6.7 CANFD_CH_NBTP

**Description:** Nominal Bit Timing & Prescaler Register
**Address:** 0x4052001C
**Offset:** 0x1C
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Protected Write. With a CAN clock (m_can_cclk) of 8 MHz, the reset value of 0x06000A03 configures the M_CAN for a bit rate of 500 Kbit/s.
**Default:** 0x6000A03

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:7] | NTSEG2 [6:0] | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | NTSEG1 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | NBRP [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | NSJW [31:25] | | | | | | | NBRP [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:6 | NTSEG2 | RW | R | 3 | Nominal Time segment after sample point 0x01-0x7F Valid values are 1 to 127. The actual interpretation by the hardware of this value is such that one more than the programmed value is used. |
| 8:15 | NTSEG1 | RW | R | 10 | Nominal Time segment before sample point 0x01-0xFF Valid values are 1 to 255. The actual interpretation by the hardware of this value is such that one more than the programmed value is used. |
| 16:24 | NBRP | RW | R | 0 | Nominal Bit Rate Prescaler 0x000-0x1FFThe value by which the oscillator frequency is divided for generating the bit time quanta. The bit time is built up from a multiple of this quanta. Valid values for the Bit Rate Prescaler are 0 to 511. The actual interpretation by the hardware of this value is such that one more than the value programmed here is used. |
| 25:31 | NSJW | RW | R | 3 | Nominal (Re)Synchronization Jump Width 0x00-0x7F Valid values are 0 to 127. The actual interpretation by the hardware of this value is such that one more than the value programmed here is used. |

### 2.3.9.6.8 CANFD_CH_TSCC

**Description:** Timestamp Counter Configuration
**Address:** 0x40520020
**Offset:** 0x20
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Protected Write.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:2] | | | | | | TSS [1:0] | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:20] | | | | TCP [19:16] | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:1 | TSS | RW | R | 0 | Timestamp Select, should always be set to external timestamp counter<br>00= Timestamp counter value always 0x0000<br>01= Timestamp counter value incremented according to TCP<br>10= External timestamp counter value used<br>11= Same as '00' |
| 16:19 | TCP | RW | R | 0 | Timestamp Counter Prescaler (still used for TOCC)<br>0x0-0xF Configures the timestamp and timeout counters time unit in multiples of CAN bit times [1...16]. The actual interpretation by the hardware of this value is such that one more<br>than the value programmed here is used. |

### 2.3.9.6.9 CANFD_CH_TSCV

**Description:** Timestamp Counter Value
**Address:** 0x40520024
**Offset:** 0x24
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | TSC [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | TSC [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | TSC | RW | R | 0 | Timestamp Counter, not used for M_TTCAN<br>The internal/external Timestamp Counter value is captured on start of frame (both Rx and Tx).<br>When TSCC.TSS = '01', the Timestamp Counter is incremented in multiples of CAN bit times [1...16] depending on the configuration of TSCC.TCP.<br>A wrap around sets interrupt flag IR.TSW.<br>Write access resets the counter to zero. When TSCC.TSS = '10', TSC reflects the external Timestamp Counter value. A write access has no impact. |

### 2.3.9.6.10 CANFD_CH_TOCC

**Description:** Timeout Counter Configuration
**Address:** 0x40520028
**Offset:** 0x28
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Protected Write.
**Default:** 0xFFFF0000

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:3] | | | | | TOS [2:1] | | ETOC [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | TOP [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | TOP [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | ETOC | RW | R | 0 | Enable Timeout Counter<br>0= Timeout Counter disabled<br>1= Timeout Counter enabled |
| 1:2 | TOS | RW | R | 0 | Timeout Select<br>When operating in Continuous mode, a write to TOCV presets the counter to the value configured by TOCC.TOP and continues down-counting. When the Timeout Counter is controlled by one of the FIFOs, an empty FIFO presets the counter to the value configured by TOCC.TOP. Down-counting is started when the first FIFO element is stored.<br>00= Continuous operation<br>01= Timeout controlled by Tx Event FIFO<br>10= Timeout controlled by Rx FIFO 0<br>11= Timeout controlled by Rx FIFO 1 |
| 16:31 | TOP | RW | R | 65535 | Timeout Period<br>Start value of the Timeout Counter (down-counter). Configures the Timeout Period. |

#### 2.3.9.6.11 CANFD_CH_TOCV

**Description:** Timeout Counter Value
**Address:** 0x4052002C
**Offset:** 0x2C
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xFFFF

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | TOC [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | TOC [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | TOC | RW | R | 65535 | Timeout Counter<br>The Timeout Counter is decremented in multiples of CAN bit times [1...16] depending on the configuration of TSCC.TCP. When decremented to zero, interrupt flag IR.TOO is set and the Timeout Counter is stopped. Start and reset/restart conditions are configured via TOCC.TOS. |

### 2.3.9.6.12 CANFD_CH_ECR

**Description:** Error Counter Register
**Address:** 0x40520040
**Offset:** 0x40
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Read side effect, except if read from debug host
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | TEC [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | RP [15:15] | REC [14:8] | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | CEL [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | TEC | R | RW | 0 | Transmit Error Counter<br>Actual state of the Transmit Error Counter, values between 0 and 255 |
| 8:14 | REC | R | RW | 0 | Receive Error Counter<br>Actual state of the Receive Error Counter, values between 0 and 127 |
| 15 | RP | R | RW | 0 | Receive Error Passive<br>0= The Receive Error Counter is below the error passive level of 128<br>1= The Receive Error Counter has reached the error passive level of 128 |
| 16:23 | CEL | R | RW1C | 0 | CAN Error Logging<br>The counter is incremented each time when a CAN protocol error causes the Transmit Error Counter or the Receive Error Counter to be incremented. It is reset by read access to CEL. The counter stops at 0xFF; the next increment of TEC or REC sets interrupt flag IR.ELO. |

### 2.3.9.6.13 CANFD_CH_PSR

**Description:** Protocol Status Register
**Address:** 0x40520044
**Offset:** 0x44
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Read side effect, except if read from debug host
**Default:** 0x707

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | BO [7:7] | EW [6:6] | EP [5:5] | ACT [4:3] | | LEC [2:0] | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:15] | PXE [14:14] | RFDF [13:13] | RBRS [12:12] | RESI [11:11] | DLEC [10:8] | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:23] | TDCV [22:16] | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:2 | LEC | R | RW1S | 7 | Last Error Code,<br>Set on Read0<br>The LEC indicates the type of the last error to occur on the CAN bus. This field will be cleared to '0' when a message has been transferred (reception or transmission) without error.<br><br>0= No Error: No error occurred since LEC has been reset by successful reception or transmission.<br>1= Stuff Error: More than 5 equal bits in a sequence have occurred in a part of a received message where this is not allowed.<br>2= Form Error: A fixed format part of a received frame has the wrong format.<br>3= AckError: The message transmitted by the M_TTCAN was not acknowledged by another node.<br>4= Bit1Error: During the transmission of a message (with the exception of the arbitration field), the device wanted to send a recessive level (bit of logical value '1'), but the monitored bus value was dominant.<br>5= Bit0Error: During the transmission of a message (or acknowledge bit, or active error flag, or overload flag), the device wanted to send a dominant level (data or identifier bit logical value 0'), but the monitored bus value was recessive. During Bus_Off recovery this status is set each time a sequence of 11 recessive bits has been monitored. This enables the CPU to monitor the proceeding of the Bus_Off recovery sequence (indicating the bus is not stuck at dominant or continuously disturbed).<br>6= CRCError: The CRC check sum of a received message was incorrect. The CRC of an incoming message does not match with the CRC calculated from the received data.<br>7= NoChange: Any read access to the Protocol Status Register re-initializes the LEC to '7'.<br>When the LEC shows the value '7', no CAN bus event was detected since the last CPU read access to the Protocol Status Register. |
| 3:4 | ACT | R | RW | 0 | Activity<br>Monitors the module's CAN communication state.<br>00= Synchronizing - node is synchronizing on CAN communication<br>01= Idle - node is neither receiver nor transmitter<br>10= Receiver - node is operating as receiver<br>11= Transmitter - node is operating as transmitter |
| 5 | EP | R | RW | 0 | Error Passive<br>0= The M_CAN is in the Error_Active state. It normally takes part in bus communication and sends an active error flag when an error has been detected<br>1= The M_CAN is in the Error_Passive state |
| 6 | EW | R | RW | 0 | Warning Status<br>0= Both error counters are below the Error_Warning limit of 96<br>1= At least one of error counter has reached the Error_Warning limit of 96 |
| 7 | BO | R | RW | 0 | Bus_Off Status<br>0= The M_CAN is not Bus_Off<br>1= The M_CAN is in Bus_Off state |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 8:10 | DLEC | R | RW1S | 7 | Data Phase Last Error Code<br>, Set on Read<br>Type of last error that occurred in the data phase of a CAN FD format frame with its BRS flag set. Coding is the same as for LEC. This field will be cleared to zero when a CAN FD format frame with its BRS flag set has been transferred (reception or transmission) without error. |
| 11 | RESI | R | RW1C | 0 | ESI flag of last received CAN FD Message<br>, Reset on Read<br>This bit is set together with RFDF, independent of acceptance filtering.<br>0= Last received CAN FD message did not have its ESI flag set<br>1= Last received CAN FD message had its ESI flag set |
| 12 | RBRS | R | RW1C | 0 | BRS flag of last received CAN FD Message<br>, Reset on Read<br>This bit is set together with RFDF, independent of acceptance filtering.<br>0= Last received CAN FD message did not have its BRS flag set<br>1= Last received CAN FD message had its BRS flag set |
| 13 | RFDF | R | RW1C | 0 | Received a CAN FD Message<br>, Reset on Read<br>This bit is set independent of acceptance filtering.<br>0= Since this bit was reset by the CPU, no CAN FD message has been received<br>1= Message in CAN FD format with FDF flag set has been received |
| 14 | PXE | R | RW1C | 0 | Protocol Exception Event<br>, Reset on Read<br>0= No protocol exception event occurred since last read access<br>1= Protocol exception event occurred |
| 16:22 | TDCV | R | RW | 0 | Transmitter Delay Compensation Value<br>0x00-0x7F Position of the secondary sample point, defined by the sum of the measured delay from m_can_tx to m_can_rx and TDCR.TDCO. The SSP position is, in the data phase, the number of mtq between the start of the transmitted bit and the secondary sample point. Valid values are 0 to 127 mtq. |

### 2.3.9.6.14 CANFD_CH_TDCR

**Description:** Transmitter Delay Compensation Register
**Address:** 0x40520048
**Offset:** 0x48
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Protected Write.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:7] | TDCF [6:0] | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:15] | TDCO [14:8] | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:6 | TDCF | RW | R | 0 | Transmitter Delay Compensation Filter Window Length<br>0x00-0x7F Defines the minimum value for the SSP position, dominant edges on m_ttcan_rx<br>that would result in an earlier SSP position are ignored for transmitter delay measurement.<br>The feature is enabled when TDCF is configured to a value greater than<br>TDCO. Valid values are 0 to 127 mtq |
| 8:14 | TDCO | RW | R | 0 | Transmitter Delay Compensation Offset<br>0x00-0x7F Offset value defining the distance between the measured delay from m_ttcan_tx to m_ttcan_rx and the secondary sample point. Valid values are 0 to 127 mtq. |

### 2.3.9.6.15 CANFD_CH_IR

**Description:** Interrupt Register
**Address:** 0x40520050
**Offset:** 0x50
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | RF1L_ [7:7] | RF1F [6:6] | RF1W [5:5] | RF1N [4:4] | RF0L_ [3:3] | RF0F [2:2] | RF0W [1:1] | RF0N [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | TEFL_ [15:15] | TEFF [14:14] | TEFW [13:13] | TEFN [12:12] | TFE [11:11] | TCF [10:10] | TC [9:9] | HPM [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | EP_ [23:23] | ELO [22:22] | BEU [21:21] | BEC [20:20] | DRX [19:19] | TOO [18:18] | MRAF [17:17] | TSW [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:30] | | ARA [29:29] | PED [28:28] | PEA [27:27] | WDI [26:26] | BO_ [25:25] | EW_ [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | RF0N | RW1C | RW | 0 | Rx FIFO 0 New Message<br>0= No new message written to Rx FIFO 0<br>1= New message written to Rx FIFO 0 |
| 1 | RF0W | RW1C | RW | 0 | Rx FIFO 0 Watermark Reached<br>0= Rx FIFO 0 fill level below watermark<br>1= Rx FIFO 0 fill level reached watermark |
| 2 | RF0F | RW1C | RW | 0 | Rx FIFO 0 Full<br>0= Rx FIFO 0 not full<br>1= Rx FIFO 0 full |
| 3 | RF0L_ | RW1C | RW | 0 | Rx FIFO 0 Message Lost<br>0= No Rx FIFO 0 message lost<br>1= Rx FIFO 0 message lost, also set after write attempt to Rx FIFO 0 of size zero |
| 4 | RF1N | RW1C | RW | 0 | Rx FIFO 1 New Message<br>0= No new message written to Rx FIFO 1<br>1= New message written to Rx FIFO 1 |
| 5 | RF1W | RW1C | RW | 0 | Rx FIFO 1 Watermark Reached<br>0= Rx FIFO 1 fill level below watermark<br>1= Rx FIFO 1 fill level reached watermark |
| 6 | RF1F | RW1C | RW | 0 | Rx FIFO 1 Full<br>0= Rx FIFO 1 not full<br>1= Rx FIFO 1 full |
| 7 | RF1L_ | RW1C | RW | 0 | Rx FIFO 1 Message Lost<br>0= No Rx FIFO 1 message lost<br>1= Rx FIFO 1 message lost, also set after write attempt to Rx FIFO 1 of size zero |
| 8 | HPM | RW1C | RW | 0 | High Priority Message<br>0= No high priority message received<br>1= High priority message received |
| 9 | TC | RW1C | RW | 0 | Transmission Completed<br>0= No transmission completed<br>1= Transmission completed |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 10 | TCF | RW1C | RW | 0 | Transmission Cancellation Finished<br>0= No transmission cancellation finished<br>1= Transmission cancellation finished |
| 11 | TFE | RW1C | RW | 0 | Tx FIFO Empty<br>0= Tx FIFO non-empty<br>1= Tx FIFO empty |
| 12 | TEFN | RW1C | RW | 0 | Tx Event FIFO New Entry<br>0= Tx Event FIFO unchanged<br>1= Tx Handler wrote Tx Event FIFO element |
| 13 | TEFW | RW1C | RW | 0 | Tx Event FIFO Watermark Reached<br>0= Tx Event FIFO fill level below watermark<br>1= Tx Event FIFO fill level reached watermark |
| 14 | TEFF | RW1C | RW | 0 | Tx Event FIFO Full<br>0= Tx Event FIFO not full<br>1= Tx Event FIFO full |
| 15 | TEFL_ | RW1C | RW | 0 | Tx Event FIFO Element Lost<br>0= No Tx Event FIFO element lost<br>1= Tx Event FIFO element lost, also set after write attempt to Tx Event FIFO of size zero |
| 16 | TSW | RW1C | RW | 0 | Timestamp Wraparound<br>0= No timestamp counter wrap-around<br>1= Timestamp counter wrapped around |
| 17 | MRAF | RW1C | RW | 0 | Message RAM Access Failure<br>The flag is set, when the Rx Handler<br>- has not completed acceptance filtering or storage of an accepted message until the arbitration field of the following message has been received. In this case acceptance filtering or message storage is aborted and the Rx Handler starts processing of the following message.<br>- was not able to write a message to the Message RAM. In this case message storage is aborted.<br>In both cases the FIFO put index is not updated resp. the New Data flag for a dedicated Rx Buffer is not set, a partly stored message is overwritten when the next message is stored to this location.<br>The flag is also set when the Tx Handler was not able to read a message from the Message RAM<br>in time. In this case message transmission is aborted. In case of a Tx Handler access failure the M_TTCAN is switched into Restricted Operation Mode. To leave Restricted Operation Mode, the Host CPU has to reset CCCR.ASM.<br>0= No Message RAM access failure occurred<br>1= Message RAM access failure occurred |
| 18 | TOO | RW1C | RW | 0 | Timeout Occurred<br>0= No timeout<br>1= Timeout reached |
| 19 | DRX | RW1C | RW | 0 | Message stored to Dedicated Rx Buffer<br>The flag is set whenever a received message has been stored into a dedicated Rx Buffer.<br>0= No Rx Buffer updated<br>1= At least one received message stored into a Rx Buffer |
| 20 | BEC | RW1C | RW | 0 | Bit Error Corrected<br>This bit always reads as 0. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 21 | BEU | RW1C | RW | 0 | Bit Error Uncorrected<br>Message RAM bit error detected, uncorrected. The flag is set in the folloiwng cases.<br>- M_TTCAN detects uncorrectable ECC error from Message RAM when ECC is enabled and ECC error injection is disabled.<br>- M_TTCAN reads from an out of range Message RAM address.<br>Message RAM bit error sets CCCR.INIT to '1'. This is done to avoid transmission of corrupted data.<br>0= No bit error detected when reading from Message RAM<br>1= Bit error detected, uncorrected |
| 22 | ELO | RW1C | RW | 0 | Error Logging Overflow<br>0= CAN Error Logging Counter did not overflow<br>1= Overflow of CAN Error Logging Counter occurred |
| 23 | EP_ | RW1C | RW | 0 | Error Passive<br>0= Error_Passive status unchanged<br>1= Error_Passive status changed |
| 24 | EW_ | RW1C | RW | 0 | Warning Status<br>0= Error_Warning status unchanged<br>1= Error_Warning status changed |
| 25 | BO_ | RW1C | RW | 0 | Bus_Off Status<br>0= Bus_Off status unchanged<br>1= Bus_Off status changed |
| 26 | WDI | RW1C | RW | 0 | Watchdog Interrupt<br>0= No Message RAM Watchdog event occurred<br>1= Message RAM Watchdog event due to missing READY |
| 27 | PEA | RW1C | RW | 0 | Protocol Error in Arbitration Phase (Nominal Bit Time is used)<br>0= No protocol error in arbitration phase<br>1= Protocol error in arbitration phase detected (PSR.LEC != 0,7) |
| 28 | PED | RW1C | RW | 0 | Protocol Error in Data Phase (Data Bit Time is used)<br>0= No protocol error in data phase<br>1= Protocol error in data phase detected (PSR.DLEC != 0,7) |
| 29 | ARA | RW1C | RW | 0 | Access to Reserved Address<br>0= No access to reserved address occurred<br>1= Access to reserved address occurred |

### 2.3.9.6.16 CANFD_CH_IE

**Description:** Interrupt Enable
**Address:** 0x40520054
**Offset:** 0x54
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | RF1LE [7:7] | RF1FE [6:6] | RF1WE [5:5] | RF1NE [4:4] | RF0LE [3:3] | RF0FE [2:2] | RF0WE [1:1] | RF0NE [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | TEFLE [15:15] | TEFFE [14:14] | TEFWE [13:13] | TEFNE [12:12] | TFEE [11:11] | TCFE [10:10] | TCE [9:9] | HPME [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | EPE [23:23] | ELOE [22:22] | BEUE [21:21] | BECE [20:20] | DRXE [19:19] | TOOE [18:18] | MRAFE [17:17] | TSWE [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:30] | | ARAE [29:29] | PEDE [28:28] | PEAE [27:27] | WDIE [26:26] | BOE [25:25] | EWE [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | RF0NE | RW | R | 0 | Rx FIFO 0 New Message Interrupt Enable<br><br>0= Interrupt Disabled<br>1= Interrupt Enabled |
| 1 | RF0WE | RW | R | 0 | Rx FIFO 0 Watermark Reached Interrupt Enable<br>0= Interrupt Disabled<br>1= Interrupt Enabled |
| 2 | RF0FE | RW | R | 0 | Rx FIFO 0 Full Interrupt Enable<br>0= Interrupt Disabled<br>1= Interrupt Enabled |
| 3 | RF0LE | RW | R | 0 | Rx FIFO 0 Message Lost Interrupt Enable<br>0= Interrupt Disabled<br>1= Interrupt Enabled |
| 4 | RF1NE | RW | R | 0 | Rx FIFO 1 New Message Interrupt Enable<br>0= Interrupt Disabled<br>1= Interrupt Enabled |
| 5 | RF1WE | RW | R | 0 | Rx FIFO 1 Watermark Reached Interrupt Enable<br>0= Interrupt Disabled<br>1= Interrupt Enabled |
| 6 | RF1FE | RW | R | 0 | Rx FIFO 1 Full Interrupt Enable<br>0= Interrupt Disabled<br>1= Interrupt Enabled |
| 7 | RF1LE | RW | R | 0 | Rx FIFO 1 Message Lost Interrupt Enable<br>0= Interrupt Disabled<br>1= Interrupt Enabled |
| 8 | HPME | RW | R | 0 | High Priority Message Interrupt Enable<br>0= Interrupt Disabled<br>1= Interrupt Enabled |
| 9 | TCE | RW | R | 0 | Transmission Completed Interrupt Enable<br>0= Interrupt Disabled<br>1= Interrupt Enabled |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 10 | TCFE | RW | R | 0 | Transmission Cancellation Finished Interrupt Enable<br>0= Interrupt Disabled<br>1= Interrupt Enabled |
| 11 | TFEE | RW | R | 0 | Tx FIFO Empty Interrupt Enable<br>0= Interrupt Disabled<br>1= Interrupt EnabledTx FIFO Empty Interrupt Enable |
| 12 | TEFNE | RW | R | 0 | Tx Event FIDO New Entry Interrupt Enable<br>0= Interrupt Disabled<br>1= Interrupt Enabled |
| 13 | TEFWE | RW | R | 0 | Tx Event FIFO Watermark Reached Interrupt Enable<br>0= Interrupt Disabled<br>1= Interrupt Enabled |
| 14 | TEFFE | RW | R | 0 | Tx Event FIFO Full Interrupt Enable<br>0= Interrupt Disabled<br>1= Interrupt Enabled |
| 15 | TEFLE | RW | R | 0 | Tx Event FIFO Event Lost Interrupt Enable<br>0= Interrupt Disabled<br>1= Interrupt Enabled |
| 16 | TSWE | RW | R | 0 | Timestamp Wraparound Interrupt Enable<br>0= Interrupt Disabled<br>1= Interrupt Enabled |
| 17 | MRAFE | RW | R | 0 | Message RAM Access Failure Interrupt Enable<br>0= Interrupt Disabled<br>1= Interrupt Enabled |
| 18 | TOOE | RW | R | 0 | Timeout Occurred Interrupt Enable<br>0= Interrupt Disabled<br>1= Interrupt Enabled |
| 19 | DRXE | RW | R | 0 | Message stored to Dedicated Rx Buffer Interrupt Enable<br>0= Interrupt Disabled<br>1= Interrupt Enabled |
| 20 | BECE | RW | R | 0 | Bit Error Corrected Interrupt Enable (not used in M_TTCAN)<br>0= Interrupt Disabled<br>1= Interrupt Enabled |
| 21 | BEUE | RW | R | 0 | Bit Error Uncorrected Interrupt Enable<br>0= Interrupt Disabled<br>1= Interrupt Enabled |
| 22 | ELOE | RW | R | 0 | Error Logging Overflow Interrupt Enable<br>0= Interrupt Disabled<br>1= Interrupt Enabled |
| 23 | EPE | RW | R | 0 | Error Passive Interrupt Enable<br>0= Interrupt Disabled<br>1= Interrupt Enabled |
| 24 | EWE | RW | R | 0 | Warning Status Interrupt Enable<br>0= Interrupt Disabled<br>1= Interrupt Enabled |
| 25 | BOE | RW | R | 0 | Bus_Off Status Interrupt Enable<br>0= Interrupt Disabled<br>1= Interrupt Enabled |
| 26 | WDIE | RW | R | 0 | Watchdog Interrupt Enable<br>0= Interrupt Disabled<br>1= Interrupt Enabled |
| 27 | PEAE | RW | R | 0 | Protocol Error in Arbitration Phase Enable<br>0= Interrupt Disabled<br>1= Interrupt Enabled |
| 28 | PEDE | RW | R | 0 | Protocol Error in Data Phase Enable<br>0= Interrupt Disabled<br>1= Interrupt Enabled |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 29 | ARAE | RW | R | 0 | Access to Reserved Address Enable<br>0= Interrupt Disabled<br>1= Interrupt Enabled |

### 2.3.9.6.17 CANFD_CH_ILS

**Description:** Interrupt Line Select
**Address:** 0x40520058
**Offset:** 0x58
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** The Interrupt Line Select register assigns an interrupt generated by a specific interrupt flag from the Interrupt Register to one of the two module interrupt lines. For interrupt generation the respective interrupt line has to be enabled via ILE.EINT0 and ILE.EINT1.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | RF1LL [7:7] | RF1FL [6:6] | RF1WL [5:5] | RF1NL [4:4] | RF0LL [3:3] | RF0FL [2:2] | RF0WL [1:1] | RF0NL [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | TEFLL [15:15] | TEFFL [14:14] | TEFWL [13:13] | TEFNL [12:12] | TFEL [11:11] | TCFL [10:10] | TCL [9:9] | HPML [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | EPL [23:23] | ELOL [22:22] | BEUL [21:21] | BECL [20:20] | DRXL [19:19] | TOOL [18:18] | MRAFL [17:17] | TSWL [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:30] | | ARAL [29:29] | PEDL [28:28] | PEAL [27:27] | WDIL [26:26] | BOL [25:25] | EWL [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | RF0NL | RW | R | 0 | Rx FIFO 0 New Message Interrupt Select<br>0= Assign to interrupt enabled by ILE.EINT0<br>1= Assign to interrupt enabled by ILE.EINT1 |
| 1 | RF0WL | RW | R | 0 | Rx FIFO 0 Watermark Reached Interrupt Select<br>0= Assign to interrupt enabled by ILE.EINT0<br>1= Assign to interrupt enabled by ILE.EINT1 |
| 2 | RF0FL | RW | R | 0 | Rx FIFO 0 Full Interrupt Select<br>0= Assign to interrupt enabled by ILE.EINT0<br>1= Assign to interrupt enabled by ILE.EINT1 |
| 3 | RF0LL | RW | R | 0 | Rx FIFO 0 Message Lost Interrupt Select<br>0= Assign to interrupt enabled by ILE.EINT0<br>1= Assign to interrupt enabled by ILE.EINT1 |
| 4 | RF1NL | RW | R | 0 | Rx FIFO 1 New Message Interrupt Select<br>0= Assign to interrupt enabled by ILE.EINT0<br>1= Assign to interrupt enabled by ILE.EINT1 |
| 5 | RF1WL | RW | R | 0 | Rx FIFO 1 Watermark Reached Interrupt Select<br>0= Assign to interrupt enabled by ILE.EINT0<br>1= Assign to interrupt enabled by ILE.EINT1 |
| 6 | RF1FL | RW | R | 0 | Rx FIFO 1 Full Interrupt Select<br>0= Assign to interrupt enabled by ILE.EINT0<br>1= Assign to interrupt enabled by ILE.EINT1 |
| 7 | RF1LL | RW | R | 0 | Rx FIFO 1 Message Lost Interrupt Select<br>0= Assign to interrupt enabled by ILE.EINT0<br>1= Assign to interrupt enabled by ILE.EINT1 |
| 8 | HPML | RW | R | 0 | High Priority Message Interrupt Select<br>0= Assign to interrupt enabled by ILE.EINT0<br>1= Assign to interrupt enabled by ILE.EINT1 |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 9 | TCL | RW | R | 0 | Transmission Completed Interrupt Select<br>0= Assign to interrupt enabled by ILE.EINT0<br>1= Assign to interrupt enabled by ILE.EINT1 |
| 10 | TCFL | RW | R | 0 | Transmission Cancellation Finished Interrupt Select<br>0= Assign to interrupt enabled by ILE.EINT0<br>1= Assign to interrupt enabled by ILE.EINT1 |
| 11 | TFEL | RW | R | 0 | Tx FIFO Empty Interrupt Select<br>0= Assign to interrupt enabled by ILE.EINT0<br>1= Assign to interrupt enabled by ILE.EINT1 |
| 12 | TEFNL | RW | R | 0 | Tx Event FIFO New Entry Interrupt Select<br>0= Assign to interrupt enabled by ILE.EINT0<br>1= Assign to interrupt enabled by ILE.EINT1 |
| 13 | TEFWL | RW | R | 0 | Tx Event FIFO Watermark Reached Interrupt Select<br>0= Assign to interrupt enabled by ILE.EINT0<br>1= Assign to interrupt enabled by ILE.EINT1 |
| 14 | TEFFL | RW | R | 0 | Tx Event FIFO Full Interrupt Select<br>0= Assign to interrupt enabled by ILE.EINT0<br>1= Assign to interrupt enabled by ILE.EINT1 |
| 15 | TEFLL | RW | R | 0 | Tx Event FIFO Event Lost Interrupt Select<br>0= Assign to interrupt enabled by ILE.EINT0<br>1= Assign to interrupt enabled by ILE.EINT1 |
| 16 | TSWL | RW | R | 0 | Timestamp Wraparound Interrupt Select<br>0= Assign to interrupt enabled by ILE.EINT0<br>1= Assign to interrupt enabled by ILE.EINT1 |
| 17 | MRAFL | RW | R | 0 | Message RAM Access Failure Interrupt Select<br>0= Assign to interrupt enabled by ILE.EINT0<br>1= Assign to interrupt enabled by ILE.EINT1 |
| 18 | TOOL | RW | R | 0 | Timeout Occurred Interrupt Select<br>0= Assign to interrupt enabled by ILE.EINT0<br>1= Assign to interrupt enabled by ILE.EINT1 |
| 19 | DRXL | RW | R | 0 | Message stored to Dedicated Rx Buffer Interrupt Select<br>0= Assign to interrupt enabled by ILE.EINT0<br>1= Assign to interrupt enabled by ILE.EINT1 |
| 20 | BECL | RW | R | 0 | Bit Error Corrected Interrupt Select (not used in M_TTCAN)<br>0= Assign to interrupt enabled by ILE.EINT0<br>1= Assign to interrupt enabled by ILE.EINT1 |
| 21 | BEUL | RW | R | 0 | Bit Error Uncorrected Interrupt Select<br>0= Assign to interrupt enabled by ILE.EINT0<br>1= Assign to interrupt enabled by ILE.EINT1 |
| 22 | ELOL | RW | R | 0 | Error Logging Overflow Interrupt Select<br>0= Assign to interrupt enabled by ILE.EINT0<br>1= Assign to interrupt enabled by ILE.EINT1 |
| 23 | EPL | RW | R | 0 | Error Passive Interrupt Select<br>0= Assign to interrupt enabled by ILE.EINT0<br>1= Assign to interrupt enabled by ILE.EINT1 |
| 24 | EWL | RW | R | 0 | Warning Status Interrupt Select<br>0= Assign to interrupt enabled by ILE.EINT0<br>1= Assign to interrupt enabled by ILE.EINT1 |
| 25 | BOL | RW | R | 0 | Bus_Off Status Interrupt Select<br>0= Assign to interrupt enabled by ILE.EINT0<br>1= Assign to interrupt enabled by ILE.EINT1 |
| 26 | WDIL | RW | R | 0 | Watchdog Interrupt Select<br>0= Assign to interrupt enabled by ILE.EINT0<br>1= Assign to interrupt enabled by ILE.EINT1 |
| 27 | PEAL | RW | R | 0 | Protocol Error in Arbitration Phase Select<br>0= Assign to interrupt enabled by ILE.EINT0<br>1= Assign to interrupt enabled by ILE.EINT1 |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 28 | PEDL | RW | R | 0 | Protocol Error in Data Phase Select<br>0= Assign to interrupt enabled by ILE.EINT0<br>1= Assign to interrupt enabled by ILE.EINT1 |
| 29 | ARAL | RW | R | 0 | Access to Reserved Address Select<br>0= Assign to interrupt enabled by ILE.EINT0<br>1= Assign to interrupt enabled by ILE.EINT1 |

#### 2.3.9.6.18 CANFD_CH_ILE

**Description:** Interrupt Line Enable
**Address:** 0x4052005C
**Offset:** 0x5C
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:2] | | | | | | EINT1 [1:1] | EINT0 [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | EINT0 | RW | R | 0 | Enable Interrupt Line 0<br>0= Interrupt line m_ttcan_int0 disabled<br>1= Interrupt line m_ttcan_int0 enabled |
| 1 | EINT1 | RW | R | 0 | Enable Interrupt Line 1<br>0= Interrupt line m_ttcan_int1 disabled<br>1= Interrupt line m_ttcan_int1 enabled |

### 2.3.9.6.19 CANFD_CH_GFC

**Description:** Global Filter Configuration
**Address:** 0x40520080
**Offset:** 0x80
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Protected Write.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:6] | | ANFS [5:4] | | ANFE [3:2] | | RRFS [1:1] | RRFE [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | RRFE | RW | R | 0 | Reject Remote Frames Extended<br>0= Filter remote frames with 29-bit extended IDs<br>1= Reject all remote frames with 29-bit extended IDs |
| 1 | RRFS | RW | R | 0 | Reject Remote Frames Standard<br>0= Filter remote frames with 11-bit standard IDs<br>1= Reject all remote frames with 11-bit standard IDs |
| 2:3 | ANFE | RW | R | 0 | Accept Non-matching Frames Extended<br>Defines how received messages with 29-bit IDs that do not match any element of the filter list are treated.<br>00= Accept in Rx FIFO 0<br>01= Accept in Rx FIFO 1<br>10= Reject<br>11= Reject |
| 4:5 | ANFS | RW | R | 0 | Accept Non-matching Frames Standard<br>Defines how received messages with 11-bit IDs that do not match any element of the filter list are treated.<br>00= Accept in Rx FIFO 0<br>01= Accept in Rx FIFO 1<br>10= Reject<br>11= Reject |

### 2.3.9.6.20 CANFD_CH_SIDFC

**Description:** Standard ID Filter Configuration
**Address:** 0x40520084
**Offset:** 0x84
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Protected Write.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | FLSSA [7:2] | | | | | | None [1:0] | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | FLSSA [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | LSS [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 2:15 | FLSSA | RW | R | 0 | Filter List Standard Start Address<br>Start address of standard Message ID filter list (32-bit word address). |
| 16:23 | LSS | RW | R | 0 | List Size Standard<br>0= No standard Message ID filter<br>1-128= Number of standard Message ID filter elements<br>128= Values greater than 128 are interpreted as 128 |

### 2.3.9.6.21 CANFD_CH_XIDFC

**Description:** Extended ID Filter Configuration
**Address:** 0x40520088
**Offset:** 0x88
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Protected Write.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | FLESA [7:2] | | | | | | None [1:0] | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | FLESA [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:23] | LSE [22:16] | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 2:15 | FLESA | RW | R | 0 | Filter List Extended Start Address<br>Start address of extended Message ID filter list (32-bit word address). |
| 16:22 | LSE | RW | R | 0 | List Size Extended<br>0= No extended Message ID filter<br>1-64= Number of extended Message ID filter elements<br>64= Values greater than 64 are interpreted as 64 |

### 2.3.9.6.22 CANFD_CH_XIDAM

**Description:** Extended ID AND Mask
**Address:** 0x40520090
**Offset:** 0x90
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Protected Write.
**Default:** 0x1FFFFFFF

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | EIDM [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | EIDM [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | EIDM [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:29] | | | EIDM [28:24] | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:28 | EIDM | RW | R | 536870911 | Extended ID Mask<br>For acceptance filtering of extended frames the Extended ID AND Mask is ANDed with the Message ID of a received frame. Intended for masking of 29-bit IDs in SAE J1939. With the reset value of all bits set to one the mask is not active. |

### 2.3.9.6.23 CANFD_CH_HPMS

**Description:** High Priority Message Status
**Address:** 0x40520094
**Offset:** 0x94
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | MSI [7:6] | | BIDX [5:0] | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | FLST [15:15] | FIDX [14:8] | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:5 | BIDX | R | RW | 0 | Buffer Index<br>Index of Rx FIFO element to which the message was stored. Only valid when MSI[1] = '1'. |
| 6:7 | MSI | R | RW | 0 | Message Storage Indicator<br>00= No FIFO selected<br>01= FIFO message lost<br>10= Message stored in FIFO 0<br>11= Message stored in FIFO 1 |
| 8:14 | FIDX | R | RW | 0 | Filter Index<br>Index of matching filter element. Range is 0 to SIDFC.LSS - 1 resp. XIDFC.LSE - 1. |
| 15 | FLST | R | RW | 0 | Filter List<br>Indicates the filter list of the matching filter element.<br>0= Standard Filter List<br>1= Extended Filter List |

### 2.3.9.6.24 CANFD_CH_NDAT1

**Description:** New Data 1
**Address:** 0x40520098
**Offset:** 0x98
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | ND [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | ND [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | ND [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | ND [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | ND | RW1C | RW | 0 | New Data<br>The register holds the New Data flags of Rx Buffers 0 to 31. The flags are set when the respective Rx Buffer has been updated from a received frame. The flags remain set until the Host clears them.<br>A flag is cleared by writing a '1' to the corresponding bit position. Writing a '0' has no effect. A hard reset will clear the register.<br>0= Rx Buffer not updated<br>1= Rx Buffer updated from new message |

### 2.3.9.6.25 CANFD_CH_NDAT2

**Description:** New Data 2
**Address:** 0x4052009C
**Offset:** 0x9C
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | ND [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | ND [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | ND [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | ND [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | ND | RW1C | RW | 0 | New Data<br>The register holds the New Data flags of Rx Buffers 32 to 63. The flags are set when the respective<br>Rx Buffer has been updated from a received frame.<br>The flags remain set until the Host clears them.<br>A flag is cleared by writing a '1' to the corresponding bit position. Writing a '0' has no effect. A hard reset will clear the register.<br>0= Rx Buffer not updated<br>1= Rx Buffer updated from new message |

### 2.3.9.6.26 CANFD_CH_RXF0C

**Description:** Rx FIFO 0 Configuration
**Address:** 0x405200A0
**Offset:** 0xA0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Protected Write.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | F0SA [7:2] | | | | | | None [1:0] | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | F0SA [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:23] | F0S [22:16] | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | F0OM [31:31] | F0WM [30:24] | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 2:15 | F0SA | RW | R | 0 | Rx FIFO 0 Start Address<br>Start address of Rx FIFO 0 in Message RAM (32-bit word address). |
| 16:22 | F0S | RW | R | 0 | Rx FIFO 0 Size<br>0= No Rx FIFO 0<br>1-64= Number of Rx FIFO 0 elements<br>64= Values greater than 64 are interpreted as 64<br>The Rx FIFO 0 elements are indexed from 0 to F0S-1 |
| 24:30 | F0WM | RW | R | 0 | Rx FIFO 0 Watermark<br>0= Watermark interrupt disabled<br>1-64= Level for Rx FIFO 0 watermark interrupt (IR.RF0W)<br>64= Watermark interrupt disabled |
| 31 | F0OM | RW | R | 0 | FIFO 0 Operation Mode<br>FIFO 0 can be operated in blocking or in overwrite mode.<br>0= FIFO 0 blocking mode<br>1= FIFO 0 overwrite mode |

### 2.3.9.6.27 CANFD_CH_RXF0S

**Description:** Rx FIFO 0 Status
**Address:** 0x405200A4
**Offset:** 0xA4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:7] | F0FL [6:0] | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:14] | | F0GI [13:8] | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:22] | | F0PI [21:16] | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:26] | | | | | | RF0L [25:25] | F0F [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:6 | F0FL | R | RW | 0 | Rx FIFO 0 Fill Level<br>Number of elements stored in Rx FIFO 0, range 0 to 64.<br>When the software reading the value immediately after writing to RXF0A.F0AI, this value should be read twice to ensure that the update is reflected. |
| 8:13 | F0GI | R | RW | 0 | Rx FIFO 0 Get Index<br>Rx FIFO 0 read index pointer, range 0 to 63.<br>This field is updated by the software writing to RXF0A.F0AI.<br>When the software reading the value immediately after writing to RXF0A.F0AI, this value should be read twice to ensure that the update is reflected. |
| 16:21 | F0PI | R | RW | 0 | Rx FIFO 0 Put Index<br>Rx FIFO 0 write index pointer, range 0 to 63. |
| 24 | F0F | R | RW | 0 | Rx FIFO 0 Full<br>0= Rx FIFO 0 not full<br>1= Rx FIFO 0 full<br>When the software reading the value immediately after writing to RXF0A.F0AI, this value should be read twice to ensure that the update is reflected. |
| 25 | RF0L | R | RW | 0 | Rx FIFO 0 Message Lost<br>This bit is a copy of interrupt flag IR.RF0L. When IR.RF0L is reset, this bit is also reset.<br>0= No Rx FIFO 0 message lost<br>1= Rx FIFO 0 message lost, also set after write attempt to Rx FIFO 0 of size zero |

### 2.3.9.6.28 CANFD_CH_RXF0A

**Description:** Rx FIFO 0 Acknowledge
**Address:** 0x405200A8
**Offset:** 0xA8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:6] | | F0AI [5:0] | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:5 | F0AI | RW | A | 0 | Rx FIFO 0 Acknowledge Index<br>After the Host has read a message or a sequence of messages from Rx FIFO 0 it has to write the buffer index of the last element read from Rx FIFO 0 to F0AI. This will set the Rx FIFO 0 Get Index RXF0S.F0GI to F0AI + 1 and update the FIFO 0 Fill Level RXF0S.F0FL. |

### 2.3.9.6.29 CANFD_CH_RXBC

**Description:** Rx Buffer Configuration
**Address:** 0x405200AC
**Offset:** 0xAC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Protected Write.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | RBSA [7:2] | | | | | | None [1:0] | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | RBSA [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 2:15 | RBSA | RW | R | 0 | Rx Buffer Start Address<br>Configures the start address of the Rx Buffers section in the Message RAM (32-bit word address).<br>Also used to reference debug messages A,B,C. |

### 2.3.9.6.30 CANFD_CH_RXF1C

**Description:** Rx FIFO 1 Configuration
**Address:** 0x405200B0
**Offset:** 0xB0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Protected Write.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | F1SA [7:2] | | | | | | None [1:0] | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | F1SA [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:23] | F1S [22:16] | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | F1OM [31:31] | F1WM [30:24] | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 2:15 | F1SA | RW | R | 0 | Rx FIFO 1 Start Address<br>Start address of Rx FIFO 1 in Message RAM (32-bit word address). |
| 16:22 | F1S | RW | R | 0 | Rx FIFO 1 Size<br>0= No Rx FIFO 1<br>1-64= Number of Rx FIFO 1 elements<br>64= Values greater than 64 are interpreted as 64<br>The Rx FIFO 1 elements are indexed from 0 to F1S - 1 |
| 24:30 | F1WM | RW | R | 0 | Rx FIFO 1 Watermark<br>0= Watermark interrupt disabled<br>1-64= Level for Rx FIFO 1 watermark interrupt (IR.RF1W)<br>64= Watermark interrupt disabled |
| 31 | F1OM | RW | R | 0 | FIFO 1 Operation Mode<br>FIFO 1 can be operated in blocking or in overwrite mode.<br>0= FIFO 1 blocking mode<br>1= FIFO 1 overwrite mode |

### 2.3.9.6.31 CANFD_CH_RXF1S

**Description:** Rx FIFO 1 Status
**Address:** 0x405200B4
**Offset:** 0xB4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:7] | F1FL [6:0] | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:14] | | F1GI [13:8] | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:22] | | F1PI [21:16] | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | DMS [31:30] | | None [29:26] | | | | RF1L [25:25] | F1F [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:6 | F1FL | R | RW | 0 | Rx FIFO 1 Fill Level<br>Number of elements stored in Rx FIFO 1, range 0 to 64.<br>When the software reading the value immediately after writing to RXF1A.F1AI, this value should be read twice to ensure that the update is reflected. |
| 8:13 | F1GI | R | RW | 0 | Rx FIFO 1 Get Index<br>Rx FIFO 1 read index pointer, range 0 to 63.<br>This field is updated by the software writing to RXF1A.F1AI.<br>When the software reading the value immediately after writing to RXF1A.F1AI, this value should be read twice to ensure that the update is reflected. |
| 16:21 | F1PI | R | RW | 0 | Rx FIFO 1 Put Index<br>Rx FIFO 1 write index pointer, range 0 to 63. |
| 24 | F1F | R | RW | 0 | Rx FIFO 1 Full<br>0= Rx FIFO 1 not full<br>1= Rx FIFO 1 full<br>When the software reading the value immediately after writing to RXF1A.F1AI, this value should be read twice to ensure that the update is reflected. |
| 25 | RF1L | R | RW | 0 | Rx FIFO 1 Message Lost<br>This bit is a copy of interrupt flag IR.RF1L. When IR.RF1L is reset, this bit is also reset.<br>0= No Rx FIFO 1 message lost<br>1= Rx FIFO 1 message lost, also set after write attempt to Rx FIFO 1 of size zero |
| 30:31 | DMS | R | RW | 0 | Debug Message Status<br>00= Idle state, wait for reception of debug messages, DMA request is cleared<br>01= Debug message A received<br>10= Debug messages A, B received<br>11= Debug messages A, B, C received, DMA request is set |

### 2.3.9.6.32 CANFD_CH_RXF1A

**Description:** Rx FIFO 1 Acknowledge
**Address:** 0x405200B8
**Offset:** 0xB8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:6] | | F1AI [5:0] | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:5 | F1AI | RW | A | 0 | Rx FIFO 1 Acknowledge Index<br>After the Host has read a message or a sequence of messages from Rx FIFO 1 it has to write the buffer index of the last element read from Rx FIFO 1 to F1AI. This will set the Rx FIFO 1 Get Index RXF1S.F1GI to F1AI + 1 and update the FIFO 1 Fill Level RXF1S.F1FL. |

### 2.3.9.6.33 CANFD_CH_RXESC

**Description:** Rx Buffer / FIFO Element Size Configuration
**Address:** 0x405200BC
**Offset:** 0xBC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Protected Write.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:7] | F1DS [6:4] | | | None [3:3] | F0DS [2:0] | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:11] | | | | | RBDS [10:8] | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:2 | F0DS | RW | R | 0 | Rx FIFO 0 Data Field Size<br>000= 8 byte data field<br>001= 12 byte data field<br>010= 16 byte data field<br>011= 20 byte data field<br>100= 24 byte data field<br>101= 32 byte data field<br>110= 48 byte data field<br>111= 64 byte data field |
| 4:6 | F1DS | RW | R | 0 | Rx FIFO 1 Data Field Size<br>000= 8 byte data field<br>001= 12 byte data field<br>010= 16 byte data field<br>011= 20 byte data field<br>100= 24 byte data field<br>101= 32 byte data field<br>110= 48 byte data field<br>111= 64 byte data field |
| 8:10 | RBDS | RW | R | 0 | Rx Buffer Data Field Size<br>000= 8 byte data field<br>001= 12 byte data field<br>010= 16 byte data field<br>011= 20 byte data field<br>100= 24 byte data field<br>101= 32 byte data field<br>110= 48 byte data field<br>111= 64 byte data field |

### 2.3.9.6.34 CANFD_CH_TXBC

**Description:** Tx Buffer Configuration
**Address:** 0x405200C0
**Offset:** 0xC0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Protected Write.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | TBSA [7:2] | | | | | | None [1:0] | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | TBSA [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:22] | | NDTB [21:16] | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:31] | TFQM [30:30] | TFQS [29:24] | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 2:15 | TBSA | RW | R | 0 | Tx Buffers Start Address<br>Start address of Tx Buffers section in Message RAM (32-bit word address). |
| 16:21 | NDTB | RW | R | 0 | Number of Dedicated Transmit Buffers<br>0= No Dedicated Tx Buffers<br>1-32= Number of Dedicated Tx Buffers<br>32= Values greater than 32 are interpreted as 32 |
| 24:29 | TFQS | RW | R | 0 | Transmit FIFO/Queue Size<br>0= No Tx FIFO/Queue<br>1-32= Number of Tx Buffers used for Tx FIFO/Queue<br>32= Values greater than 32 are interpreted as 32 |
| 30 | TFQM | RW | R | 0 | Tx FIFO/Queue Mode<br>0= Tx FIFO operation<br>1= Tx Queue operation |

### 2.3.9.6.35 CANFD_CH_TXFQS

**Description:** Tx FIFO/Queue Status
**Address:** 0x405200C4
**Offset:** 0xC4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:6] | | TFFL [5:0] | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:13] | | | TFGI [12:8] | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:22] | | TFQF [21:21] | TFQPI [20:16] | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:5 | TFFL | R | RW | 0 | Tx FIFO Free Level<br>Number of consecutive free Tx FIFO elements starting from TFGI, range 0 to 32. Read as zero when Tx Queue operation is configured (TXBC.TFQM = '1') |
| 8:12 | TFGI | R | RW | 0 | Tx FIFO Get Index<br>Tx FIFO read index pointer, range 0 to 31. Read as zero when Tx Queue operation is configured TXBC.TFQM = '1'). |
| 16:20 | TFQPI | R | RW | 0 | Tx FIFO/Queue Put Index<br>Tx FIFO/Queue write index pointer, range 0 to 31. |
| 21 | TFQF | R | RW | 0 | Tx FIFO/Queue Full<br>0= Tx FIFO/Queue not full<br>1= Tx FIFO/Queue full |

### 2.3.9.6.36 CANFD_CH_TXESC

**Description:** Tx Buffer Element Size Configuration
**Address:** 0x405200C8
**Offset:** 0xC8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Protected Write.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:3] | | | | | TBDS [2:0] | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:2 | TBDS | RW | R | 0 | Tx Buffer Data Field Size<br>000= 8 byte data field<br>001= 12 byte data field<br>010= 16 byte data field<br>011= 20 byte data field<br>100= 24 byte data field<br>101= 32 byte data field<br>110= 48 byte data field<br>111= 64 byte data field |

### 2.3.9.6.37 CANFD_CH_TXBRP

**Description:** Tx Buffer Request Pending
**Address:** 0x405200CC
**Offset:** 0xCC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | TRP [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | TRP [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | TRP [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | TRP [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | TRP | R | RW | 0 | Transmission Request Pending<br>Each Tx Buffer has its own Transmission Request Pending bit. The bits are set via register TXBAR. The bits are reset after a requested transmission has completed or has been cancelled via register TXBCR.<br>TXBRP bits are set only for those Tx Buffers configured via TXBC. After a TXBRP bit has been set, a Tx scan (Tx Handling) is started to check for the pending Tx request with the highest priority (Tx Buffer with lowest Message ID).<br>A cancellation request resets the corresponding transmission request pending bit of register TXBRP. In case a transmission has already been started when a cancellation is requested, this is done at the end of the transmission, regardless whether the transmission was successful or not. The cancellation request bits are reset directly after the corresponding TXBRP bit has been reset.<br>After a cancellation has been requested, a finished cancellation is signaled via TXBCF<br>after successful transmission together with the corresponding TXBTO bit<br>when the transmission has not yet been started at the point of cancellation<br>when the transmission has been aborted due to lost arbitration<br>when an error occurred during frame transmission<br>In DAR mode all transmissions are automatically cancelled if they are not successful. The corresponding TXBCF bit is set for all unsuccessful transmissions.<br>0= No transmission request pending<br>1= Transmission request pending |

### 2.3.9.6.38 CANFD_CH_TXBAR

**Description:** Tx Buffer Add Request
**Address:** 0x405200D0
**Offset:** 0xD0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | AR [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | AR [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | AR [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | AR [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | AR | RW | RW | 0 | Add Request<br>Each Tx Buffer has its own Add Request bit. Writing a '1' will set the corresponding Add Request<br>bit; writing a '0' has no impact. This enables the Host to set transmission requests for multiple Tx<br>Buffers with one write to TXBAR. TXBAR bits are set only for those Tx Buffers configured via TXBC.<br>When no Tx scan is running, the bits are reset immediately, else the bits remain set until the Tx scan process has completed.<br>0= No transmission request added<br>1= Transmission requested added |

### 2.3.9.6.39 CANFD_CH_TXBCR

**Description:** Tx Buffer Cancellation Request
**Address:** 0x405200D4
**Offset:** 0xD4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | CR [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | CR [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | CR [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | CR [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | CR | RW | R | 0 | Cancellation Request<br>Each Tx Buffer has its own Cancellation Request bit. Writing a '1' will set the corresponding Cancellation Request bit; writing a '0' has no impact. This enables the Host to set cancellation requests for multiple Tx Buffers with one write to TXBCR. TXBCR bits are set only for those Tx Buffers configured via TXBC. The bits remain set until the corresponding bit of TXBRP is reset.<br>0= No cancellation pending<br>1= Cancellation pending |

### 2.3.9.6.40 CANFD_CH_TXBTO

**Description:** Tx Buffer Transmission Occurred
**Address:** 0x405200D8
**Offset:** 0xD8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | TO [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | TO [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | TO [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | TO [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | TO | R | RW | 0 | Transmission Occurred<br>Each Tx Buffer has its own Transmission Occurred bit. The bits are set when the corresponding TXBRP bit is cleared after a successful transmission. The bits are reset when a new transmission is requested by writing a '1' to the corresponding bit of register TXBAR.<br>0= No transmission occurred<br>1= Transmission occurred |

### 2.3.9.6.41 CANFD_CH_TXBCF

**Description:** Tx Buffer Cancellation Finished
**Address:** 0x405200DC
**Offset:** 0xDC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | CF [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | CF [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | CF [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | CF [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | CF | R | RW | 0 | Cancellation Finished<br>Each Tx Buffer has its own Cancellation Finished bit. The bits are set when the corresponding TXBRP bit is cleared after a cancellation was requested via TXBCR. In case the corresponding TXBRP bit was not set at the point of cancellation, CF is set immediately. The bits are reset when a new transmission is requested by writing a '1' to the corresponding bit of register TXBAR.<br>0= No transmit buffer cancellation<br>1= Transmit buffer cancellation finished |

### 2.3.9.6.42 CANFD_CH_TXBTIE

**Description:** Tx Buffer Transmission Interrupt Enable
**Address:** 0x405200E0
**Offset:** 0xE0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | TIE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | TIE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | TIE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | TIE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | TIE | RW | R | 0 | Transmission Interrupt Enable<br>Each Tx Buffer has its own Transmission Interrupt Enable bit.<br>0= Transmission interrupt disabled<br>1= Transmission interrupt enable |

### 2.3.9.6.43 CANFD_CH_TXBCIE

**Description:** Tx Buffer Cancellation Finished Interrupt Enable
**Address:** 0x405200E4
**Offset:** 0xE4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | CFIE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | CFIE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | CFIE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | CFIE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | CFIE | RW | R | 0 | Cancellation Finished Interrupt Enable<br>Each Tx Buffer has its own Cancellation Finished Interrupt Enable bit.<br>0= Cancellation finished interrupt disabled<br>1= Cancellation finished interrupt enabled |

### 2.3.9.6.44 CANFD_CH_TXEFC

**Description:** Tx Event FIFO Configuration
**Address:** 0x405200F0
**Offset:** 0xF0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Protected Write.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | EFSA [7:2] | | | | | | None [1:0] | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | EFSA [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:22] | | EFS [21:16] | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:30] | | EFWM [29:24] | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 2:15 | EFSA | RW | R | 0 | Event FIFO Start Address<br>Start address of Tx Event FIFO in Message RAM (32-bit word address). |
| 16:21 | EFS | RW | R | 0 | Event FIFO Size<br>0= Tx Event FIFO disabled<br>1-32= Number of Tx Event FIFO elements<br>32= Values greater than 32 are interpreted as 32<br>The Tx Event FIFO elements are indexed from 0 to EFS-1 |
| 24:29 | EFWM | RW | R | 0 | Event FIFO Watermark<br>0= Watermark interrupt disabled<br>1-32= Level for Tx Event FIFO watermark interrupt (IR.TEFW)<br>32= Watermark interrupt disabled |

### 2.3.9.6.45 CANFD_CH_TXEFS

**Description:** Tx Event FIFO Status
**Address:** 0x405200F4
**Offset:** 0xF4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:6] | | EFFL [5:0] | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:13] | | | EFGI [12:8] | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:21] | | | EFPI [20:16] | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:26] | | | | | | TEFL [25:25] | EFF [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:5 | EFFL | R | RW | 0 | Event FIFO Fill Level<br>Number of elements stored in Tx Event FIFO, range 0 to 32.<br>When the software reading the value immediately after writing to TXEFA.EFAI, this value should be read twice to ensure that the update is reflected. |
| 8:12 | EFGI | R | RW | 0 | Event FIFO Get Index<br>Tx Event FIFO read index pointer, range 0 to 31.<br>This field is updated by the software writing to TXEFA.EFAI.<br>When the software reading the value immediately after writing to TXEFA.EFAI, this value should be read twice to ensure that the update is reflected. |
| 16:20 | EFPI | R | RW | 0 | Event FIFO Put Index<br>Tx Event FIFO write index pointer, range 0 to 31. |
| 24 | EFF | R | RW | 0 | Event FIFO Full<br>0= Tx Event FIFO not full<br>1= Tx Event FIFO full<br>When the software reading the value immediately after writing to TXEFA.EFAI, this value should be read twice to ensure that the update is reflected. |
| 25 | TEFL | R | RW | 0 | Tx Event FIFO Element Lost<br>This bit is a copy of interrupt flag IR.TEFL. When IR.TEFL is reset, this bit is also reset.<br>0= No Tx Event FIFO element lost<br>1= Tx Event FIFO element lost, also set after write attempt to Tx Event FIFO of size zero. |

### 2.3.9.6.46 CANFD_CH_TXEFA

**Description:** Tx Event FIFO Acknowledge
**Address:** 0x405200F8
**Offset:** 0xF8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:5] | | | EFAI [4:0] | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:4 | EFAI | RW | R | 0 | Event FIFO Acknowledge Index<br>After the Host has read an element or a sequence of elements from the Tx Event FIFO it has to write the index of the last element read from Tx Event FIFO to EFAI. This will set the Tx Event FIFO Get Index TXEFS.EFGI to EFAI + 1 and update the Event FIFO Fill Level TXEFS.EFFL. |

### 2.3.9.6.47 CANFD_CH_TTTMC

**Description:** TT Trigger Memory Configuration
**Address:** 0x40520100
**Offset:** 0x100
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Protected Write.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | TMSA [7:2] | | | | | | None [1:0] | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | TMSA [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:23] | TME [22:16] | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 2:15 | TMSA | RW | R | 0 | Trigger Memory Start Address<br>Start address of Trigger Memory in Message RAM (32-bit word address). |
| 16:22 | TME | RW | R | 0 | Trigger Memory Elements<br>0= No Trigger Memory<br>1-64= Number of Trigger Memory elements<br>64= Values greater than 64 are interpreted as 64 |

### 2.3.9.6.48 CANFD_CH_TTRMC

**Description:** TT Reference Message Configuration
**Address:** 0x40520104
**Offset:** 0x104
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Protected Write.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | RID [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | RID [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | RID [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | RMPS [31:31] | XTD [30:30] | None [29:29] | RID [28:24] | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:28 | RID | RW | R | 0 | Reference Identifier<br>Identifier transmitted with reference message and used for reference message filtering. Standard or extended reference identifier depending on bit XTD. A standard identifier has to be written to ID[28:18]. |
| 30 | XTD | RW | R | 0 | Extended Identifier<br>0= 11-bit standard identifier<br>1= 29-bit extended identifier |
| 31 | RMPS | RW | R | 0 | Reference Message Payload Select<br>Ignored in case of time slaves.<br>0= Reference message has no additional payload<br>1= The following elements are taken from Tx Buffer 0: Message Marker MM, Event FIFO Control EFC, Data Length Code DLC, Data Bytes DB<br>Level 1: bytes 2-8, Level 0,2: bytes 5-8) |

### 2.3.9.6.49 CANFD_CH_TTOCF

**Description:** TT Operation Configuration
**Address:** 0x40520108
**Offset:** 0x108
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Protected Write.
**Default:** 0x10000

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | LDSDL [7:5] | | | TM [4:4] | GEN [3:3] | None [2:2] | OM [1:0] | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | EECS [15:15] | IRTO [14:8] | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | AWL [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:27] | | | | | EVTP [26:26] | ECC [25:25] | EGTF [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:1 | OM | RW | R | 0 | Operation Mode<br>00= Event-driven CAN communication, default<br>01= TTCAN level 1<br>10= TTCAN level 2<br>11= TTCAN level 0 |
| 3 | GEN | RW | R | 0 | Gap Enable<br>0= Strictly time-triggered operation<br>1= External event-synchronized time-triggered operation |
| 4 | TM | RW | R | 0 | Time Master<br>0= Time Master function disabled<br>1= Potential Time Master |
| 5:7 | LDSDL | RW | R | 0 | LD of Synchronization Deviation Limit<br>The Synchronization Deviation Limit SDL is configured by its dual logarithm LDSDL with SDL = 2(LDSDL + 5). It should not exceed the clock tolerance given by the CAN bit timing configuration.<br>0x0-7 LD of Synchronization Deviation Limit (SDL <= 32...4096) |
| 8:14 | IRTO | RW | R | 0 | Initial Reference Trigger Offset<br>0x00-7F Positive offset, range from 0 to 127 |
| 15 | EECS | RW | R | 0 | Enable External Clock Synchronization<br>If enabled, TUR configuration (TURCF.NCL only) may be updated during TTCAN operation.<br>0= External clock synchronization in TTCAN Level 0,2 disabled<br>1= External clock synchronization in TTCAN Level 0,2 enabled |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 16:23 | AWL | RW | R | 1 | Application Watchdog Limit<br>The application watchdog can be disabled by programming AWL to 0x00.<br>0x00-FF Maximum time after which the application has to serve the application watchdog.<br>The application watchdog is incremented once each 256 NTUs. |
| 24 | EGTF | RW | R | 0 | Enable Global Time Filtering<br>0= Global time filtering in TTCAN Level 0,2 is disabled<br>1= Global time filtering in TTCAN Level 0,2 is enabled |
| 25 | ECC | RW | R | 0 | Enable Clock Calibration<br>0= Automatic clock calibration in TTCAN Level 0,2 is disabled<br>1= Automatic clock calibration in TTCAN Level 0,2 is enabled |
| 26 | EVTP | RW | R | 0 | Event Trigger Polarity<br>0= Rising edge trigger<br>1= Falling edge trigger |

### 2.3.9.6.50 CANFD_CH_TTMLM

**Description:** TT Matrix Limits
**Address:** 0x4052010C
**Offset:** 0x10C
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Protected Write.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | CSS [7:6] | | CCM [5:0] | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:12] | | | | TXEW [11:8] | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | ENTT [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:28] | | | | ENTT [27:24] | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:5 | CCM | RW | R | 0 | Cycle Count Max<br>0x00 1 Basic Cycle per Matrix Cycle<br>0x01 2 Basic Cycles per Matrix Cycle<br>0x03 4 Basic Cycles per Matrix Cycle<br>0x07 8 Basic Cycles per Matrix Cycle<br>0x0F 16 Basic Cycles per Matrix Cycle<br>0x1F 32 Basic Cycles per Matrix Cycle<br>0x3F 64 Basic Cycles per Matrix Cycle<br>others Reserved |
| 6:7 | CSS | RW | R | 0 | Cycle Start Synchronization<br>Enables sync pulse output at pin m_ttcan_soc.<br>00= No sync pulse<br>01= Sync pulse at start of basic cycle<br>10= Sync pulse at start of matrix cycle<br>11= Reserved |
| 8:11 | TXEW | RW | R | 0 | Tx Enable Window<br>0x0-F Length of Tx enable window, 1-16 NTU cycles |
| 16:27 | ENTT | RW | R | 0 | Expected Number of Tx Triggers<br>0x000-FFF Expected number of Tx Triggers in one Matrix Cycle |

### 2.3.9.6.51 CANFD_CH_TURCF

**Description:** TUR Configuration
**Address:** 0x40520110
**Offset:** 0x110
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Protected Write.
**Default:** 0x10000000

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | NCL [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | NCL [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | DC [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | ELT [31:31] | None [30:30] | DC [29:24] | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | NCL | RW | R | 0 | Numerator Configuration Low<br>Write access to the TUR Numerator Configuration Low is only possible during configuration with TURCF.ELT = '0' or if TTOCF.EECS (external clock synchronization enabled) is set. When a new value for NCL is written outside TT Configuration Mode, the new value takes effect when TTOST.WECS is cleared to '0'. NCL is locked TTOST.WECS is '1'.<br>0x0000-FFFF Numerator Configuration Low |
| 16:29 | DC | RW | R | 4096 | Denominator Configuration<br>0x0000 Illegal value<br>0x0001-3FFF Denominator Configuration |
| 31 | ELT | RW | R | 0 | Enable Local Time<br>0= Local time is stopped, default<br>1= Local time is enabled |

### 2.3.9.6.52 CANFD_CH_TTOCN

**Description:** TT Operation Control
**Address:** 0x40520114
**Offset:** 0x114
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | TMC [7:6] | | RTIE [5:5] | SWS [4:3] | | SWP [2:2] | ECS [1:1] | SGT [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | LCKC [15:15] | None [14:14] | ESCN [13:13] | NIG [12:12] | TMG [11:11] | FGP [10:10] | GCS [9:9] | TTIE [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | SGT | RW | R | 0 | Set Global time<br>Writing a '1' to SGT sets TTOST.WGDT if the node is the actual Time Master. SGT is reset after one Host clock period. The global time preset takes effect when the node transmits the next reference message with the Master_Ref_Mark modified by the preset value written to TTGTP. |
| 1 | ECS | RW | R | 0 | External Clock Synchronization<br>Writing a '1' to ECS sets TTOST.WECS if the node is the actual Time Master. ECS is reset after one Host clock period. The external clock synchronization takes effect at the start of the next basic cycle. |
| 2 | SWP | RW | R | 0 | Stop Watch Polarity<br>0= Rising edge trigger<br>1= Falling edge trigger |
| 3:4 | SWS | RW | R | 0 | Stop Watch Source<br>00= Stop Watch disabled<br>01= Actual value of cycle time is copied to TTCPT.SWV<br>10= Actual value of local time is copied to TTCPT.SWV<br>11= Actual value of global time is copied to TTCPT.SWV |
| 5 | RTIE | RW | R | 0 | Register Time Mark Interrupt Pulse Enable<br>Register time mark interrupts are configured by register TTTMK. A register time mark interrupt pulse with the length of one NTU is generated when the time referenced by TTOCN.TMC (cycle, local, or global) equals TTTMK.TM, independent of the synchronization state.<br>0= Register Time Mark Interrupt output m_ttcan_rtp disabled<br>1= Register Time Mark Interrupt output m_ttcan_rtp enabled |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 6:7 | TMC | RW | R | 0 | Register Time Mark Compare<br>00= No Register Time Mark Interrupt generated<br>01= Register Time Mark Interrupt if Time Mark = cycle time<br>10= Register Time Mark Interrupt if Time Mark = local time<br>11= Register Time Mark Interrupt if Time Mark = global time |
| 8 | TTIE | RW | R | 0 | Trigger Time Mark Interrupt Pulse Enable<br>External time mark events are configured by trigger memory element TMEX. A<br>trigger time mark interrupt pulse is generated when the trigger memory element becomes active,<br>and the M_TTCAN is in synchronization state In_Schedule or In_Gap.<br>0= Trigger Time Mark Interrupt output m_ttcan_tmp disabled<br>1= Trigger Time Mark Interrupt output m_ttcan_tmp enabled |
| 9 | GCS | RW | R | 0 | Gap Control Select<br>0= Gap control independent from m_ttcan_evt<br>1= Gap control by input pin m_ttcan_evt |
| 10 | FGP | RW | R | 0 | Finish Gap<br>Set by the CPU, reset by each reference message<br>0= No reference message requested<br>1= Application requested start of reference message |
| 11 | TMG | RW | R | 0 | Time Mark Gap<br>0= Reset by each reference message<br>1= Next reference message started when Register Time Mark interrupt TTIR.RTMI is activated |
| 12 | NIG | RW | R | 0 | Next is Gap<br>This bit can only be set when the M_TTCAN is the actual Time Master and when it is configured for external event-synchronized time-triggered operation (TTOCF.GEN = '1')<br>0= No action, reset by reception of any reference message<br>1= Transmit next reference message with Next_is_Gap = '1' |
| 13 | ESCN | RW | R | 0 | External Synchronization Control<br>If enabled the M_TTCAN synchronizes its cycle time phase to an external event signaled by a rising edge at pin m_ttcan_evt.<br>0= External synchronization disabled<br>1= External synchronization enabled |
| 15 | LCKC | R | RW | 0 | TT Operation Control Register Locked<br>Set by a write access to register TTOCN. Reset when the updated configuration has been synchronized into the CAN clock domain.<br>0= Write access to TTOCN enabled<br>1= Write access to TTOCN locked |

### 2.3.9.6.53 CANFD_CH_TTGTP

**Description:** TT Global Time Preset
**Address:** 0x40520118
**Offset:** 0x118
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | TP [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | TP [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | CTP [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | CTP [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | TP | RW | R | 0 | Time Preset<br>TP is write-protected while TTOST.WGTD is set.<br>0x0000-7FFF Next Master Reference Mark = Master Reference Mark + TP<br>0x8000 reserved<br>0x8001-FFFF Next Master Reference Mark = Master Reference Mark - (0x10000 - TP) |
| 16:31 | CTP | RW | R | 0 | Cycle Time Target Phase<br>CTP is write-protected while TTOCN.ESCN or TTOST.SPL are set.<br>0x0000-FFFF Defines target value of cycle time when a rising edge of m_ttcan_evt is expected |

### 2.3.9.6.54 CANFD_CH_TTTMK

**Description:** TT Time Mark
**Address:** 0x4052011C
**Offset:** 0x11C
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | TM_ [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | TM_ [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:23] | TICC [22:16] | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | LCKM [31:31] | None [30:24] | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | TM_ | RW | R | 0 | Time Mark<br>0x0000-FFFF Time Mark |
| 16:22 | TICC | RW | R | 0 | Time Mark Cycle Code<br>Cycle count for which the time mark is valid.<br>0b000000x valid for all cycles<br>0b000001c valid every second cycle at cycle count mod2 = c<br>0b00001cc valid every fourth cycle at cycle count mod4 = cc<br>0b0001ccc valid every eighth cycle at cycle count mod8 = ccc<br>0b001cccc valid every sixteenth cycle at cycle count mod16 = cccc<br>0b01ccccc valid every thirty-second cycle at cycle count mod32 = ccccc<br>0b1cccccc valid every sixty-fourth cycle at cycle count mod64 = cccccc |
| 31 | LCKM | R | RW | 0 | TT Time Mark Register Locked<br>Always set by a write access to registers TTOCN. Set by write access to register TTTMK when TTOCN.TMC != '00'. Reset when the registers have been synchronized into the CAN clock domain.<br>0= Write access to TTTMK enabled<br>1= Write access to TTTMK locked |

### 2.3.9.6.55 CANFD_CH_TTIR

**Description:** TT Interrupt Register
**Address:** 0x40520120
**Offset:** 0x120
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | GTW [7:7] | SWE [6:6] | TTMI [5:5] | RTMI [4:4] | SOG [3:3] | CSM_ [2:2] | SMC [1:1] | SBC [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | IWT [15:15] | ELC [14:14] | SE2 [13:13] | SE1 [12:12] | TXO [11:11] | TXU [10:10] | GTE [9:9] | GTD [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:19] | | | | | CER [18:18] | AW [17:17] | WT [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | SBC | RW1C | RW | 0 | Start of Basic Cycle<br>0= No Basic Cycle started since bit has been reset<br>1= Basic Cycle started |
| 1 | SMC | RW1C | RW | 0 | Start of Matrix Cycle<br>0= No Matrix Cycle started since bit has been reset<br>1= Matrix Cycle started |
| 2 | CSM_ | RW1C | RW | 0 | Change of Synchronization Mode<br>0= No change in master to slave relation or schedule synchronization<br>1= Master to slave relation or schedule synchronization changed,<br>also set when TTOST.SPL is reset |
| 3 | SOG | RW1C | RW | 0 | Start of Gap<br>0= No reference message seen with Next_is_Gap bit set<br>1= Reference message with Next_is_Gap bit set becomes valid |
| 4 | RTMI | RW1C | RW | 0 | Register Time Mark Interrupt<br>Set when time referenced by TTOCN.TMC (cycle, local, or global) equals TTTMK.TM, independent of the synchronization state.<br>0= Time mark not reached<br>1= Time mark reached |
| 5 | TTMI | RW1C | RW | 0 | Trigger Time Mark Event Internal<br>Internal time mark events are configured by trigger memory element TMIN. Set<br>when the trigger memory element becomes active, and the M_TTCAN is in synchronization state In_Gap or In_Schedule.<br>0= Time mark not reached<br>1= Time mark reached (Level 0: cycle time TTOCF.IRTO * 0x200) |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 6 | SWE | RW1C | RW | 0 | Stop Watch Event<br>0= No rising/falling edge at stop watch trigger pin m_ttcan_swt detected<br>1= Rising/falling edge at stop watch trigger pin m_ttcan_swt detected |
| 7 | GTW | RW1C | RW | 0 | Global Time Wrap<br>0= No global time wrap occurred<br>1= Global time wrap from 0xFFFF to 0x0000 occurred |
| 8 | GTD | RW1C | RW | 0 | Global Time Discontinuity<br>0= No discontinuity of global time<br>1= Discontinuity of global time |
| 9 | GTE | RW1C | RW | 0 | Global Time Error<br>Synchronization deviation SD exceeds limit specified by TTOCF.LDSDL, TTCAN Level 0,2 only.<br>0= Synchronization deviation within limit<br>1= Synchronization deviation exceeded limit |
| 10 | TXU | RW1C | RW | 0 | Tx Count Underflow<br>0= Number of Tx Trigger as expected<br>1= Less Tx trigger than expected in one matrix cycle |
| 11 | TXO | RW1C | RW | 0 | Tx Count Overflow<br>0= Number of Tx Trigger as expected<br>1= More Tx trigger than expected in one matrix cycle |
| 12 | SE1 | RW1C | RW | 0 | Scheduling Error 1<br>0= No scheduling error 1<br>1= Scheduling error 1 occurred |
| 13 | SE2 | RW1C | RW | 0 | Scheduling Error 2<br>0= No scheduling error 2<br>1= Scheduling error 2 occurred |
| 14 | ELC | RW1C | RW | 0 | Error Level Changed<br>Not set when error level changed during initialization.<br>0= No change in error level<br>1= Error level changed |
| 15 | IWT | RW1C | RW | 0 | Initialization Watch Trigger<br>The initialization is restarted by resetting IWT.<br>0= No missing reference message during system startup<br>1= No system startup due to missing reference message |
| 16 | WT | RW1C | RW | 0 | Watch Trigger<br>0= No missing reference message<br>1= Missing reference message (Level 0: cycle time 0xFF00) |
| 17 | AW | RW1C | RW | 0 | Application Watchdog<br>0= Application watchdog served in time<br>1= Application watchdog not served in time |
| 18 | CER | RW1C | RW | 0 | Configuration Error<br>Trigger out of order.<br>0= No error found in trigger list<br>1= Error found in trigger list |

### 2.3.9.6.56 CANFD_CH_TTIE

**Description:** TT Interrupt Enable
**Address:** 0x40520124
**Offset:** 0x124
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | GTWE [7:7] | SWEE [6:6] | TTMIE [5:5] | RTMIE [4:4] | SOGE [3:3] | CSME [2:2] | SMCE [1:1] | SBCE [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | IWTE [15:15] | ELCE [14:14] | SE2E [13:13] | SE1E [12:12] | TXOE [11:11] | TXUE [10:10] | GTEE [9:9] | GTDE [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:19] | | | | | CERE [18:18] | AWE_ [17:17] | WTE [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | SBCE | RW | R | 0 | Start of Basic Cycle Interrupt Enable<br>0= Interrupt Disabled<br>1= Interrupt Enabled |
| 1 | SMCE | RW | R | 0 | Start of Matrix Cycle Interrupt Enable<br>0= Interrupt Disabled<br>1= Interrupt Enabled |
| 2 | CSME | RW | R | 0 | Change of Synchronization Mode Interrupt Enable<br>0= Interrupt Disabled<br>1= Interrupt Enabled |
| 3 | SOGE | RW | R | 0 | Start of Gap Interrupt Enable<br>0= Interrupt Disabled<br>1= Interrupt Enabled |
| 4 | RTMIE | RW | R | 0 | Register Time Mark Interrupt Enable<br>0= Interrupt Disabled<br>1= Interrupt Enabled |
| 5 | TTMIE | RW | R | 0 | Trigger Time Mark Event Internal Enable<br>0= Interrupt Disabled<br>1= Interrupt Enabled |
| 6 | SWEE | RW | R | 0 | Stop Watch Event Interrupt Enable<br>0= Interrupt Disabled<br>1= Interrupt Enabled |
| 7 | GTWE | RW | R | 0 | Global Time Wrap Interrupt Enable<br>0= Interrupt Disabled<br>1= Interrupt Enabled |
| 8 | GTDE | RW | R | 0 | Global Time Discontinuity Interrupt Enable<br>0= Interrupt Disabled<br>1= Interrupt Enabled |
| 9 | GTEE | RW | R | 0 | Global Time Error Interrupt Enable<br>0= Interrupt Disabled<br>1= Interrupt Enabled |
| 10 | TXUE | RW | R | 0 | Tx Count Underflow Interrupt Enable<br>0= Interrupt Disabled<br>1= Interrupt Enabled |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 11 | TXOE | RW | R | 0 | Tx Count Overflow Interrupt Enable<br>0= Interrupt Disabled<br>1= Interrupt Enabled |
| 12 | SE1E | RW | R | 0 | Scheduling Error 1 Interrupt Enable<br>0= Interrupt Disabled<br>1= Interrupt Enabled |
| 13 | SE2E | RW | R | 0 | Scheduling Error 2 Interrupt Enable<br>0= Interrupt Disabled<br>1= Interrupt Enabled |
| 14 | ELCE | RW | R | 0 | Change Error Level Interrupt Enable<br>0= Interrupt Disabled<br>1= Interrupt Enabled |
| 15 | IWTE | RW | R | 0 | Initialization Watch Trigger Interrupt Enable<br>0= Interrupt Disabled<br>1= Interrupt Enabled |
| 16 | WTE | RW | R | 0 | Watch Trigger Interrupt Enable<br>0= Interrupt Disabled<br>1= Interrupt Enabled |
| 17 | AWE_ | RW | R | 0 | Application Watchdog Interrupt Enable<br>0= Interrupt Disabled<br>1= Interrupt Enabled |
| 18 | CERE | RW | R | 0 | Configuration Error Interrupt Enable<br>0= Interrupt Disabled<br>1= Interrupt Enabled |

### 2.3.9.6.57 CANFD_CH_TTILS

**Description:** TT Interrupt Line Select
**Address:** 0x40520128
**Offset:** 0x128
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** The TT Interrupt Line Select register assigns an interrupt generated by a specific interrupt flag from the TT Interrupt Register to one of the two module interrupt lines. For interrupt generation the respective interrupt line has to be enabled via ILE.EINT0 and ILE.EINT1. 0= TT interrupt assigned to interrupt line m_ttcan_int0 1= TT interrupt assigned to interrupt line m_ttcan_int1
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | GTWL [7:7] | SWEL [6:6] | TTMIL [5:5] | RTMIL [4:4] | SOGL [3:3] | CSML [2:2] | SMCL [1:1] | SBCL [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | IWTL [15:15] | ELCL [14:14] | SE2L [13:13] | SE1L [12:12] | TXOL [11:11] | TXUL [10:10] | GTEL [9:9] | GTDL [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:19] | | | | | CERL [18:18] | AWL_ [17:17] | WTL [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | SBCL | RW | R | 0 | Start of Basic Cycle Interrupt Select<br>0= Assign to interrupt enabled by ILE.EINT0<br>1= Assign to interrupt enabled by ILE.EINT1 |
| 1 | SMCL | RW | R | 0 | Start of Matrix Cycle Interrupt Select<br>0= Assign to interrupt enabled by ILE.EINT0<br>1= Assign to interrupt enabled by ILE.EINT1 |
| 2 | CSML | RW | R | 0 | Change of Synchronization Mode Interrupt Select<br>0= Assign to interrupt enabled by ILE.EINT0<br>1= Assign to interrupt enabled by ILE.EINT1 |
| 3 | SOGL | RW | R | 0 | Start of Gap Interrupt Select<br>0= Assign to interrupt enabled by ILE.EINT0<br>1= Assign to interrupt enabled by ILE.EINT1 |
| 4 | RTMIL | RW | R | 0 | Register Time Mark Interrupt Select<br>0= Assign to interrupt enabled by ILE.EINT0<br>1= Assign to interrupt enabled by ILE.EINT1 |
| 5 | TTMIL | RW | R | 0 | Trigger Time Mark Event Internal Select<br>0= Assign to interrupt enabled by ILE.EINT0<br>1= Assign to interrupt enabled by ILE.EINT1 |
| 6 | SWEL | RW | R | 0 | Stop Watch Event Interrupt Select<br>0= Assign to interrupt enabled by ILE.EINT0<br>1= Assign to interrupt enabled by ILE.EINT1 |
| 7 | GTWL | RW | R | 0 | Global Time Wrap Interrupt Select<br>0= Assign to interrupt enabled by ILE.EINT0<br>1= Assign to interrupt enabled by ILE.EINT1 |
| 8 | GTDL | RW | R | 0 | Global Time Discontinuity Interrupt Select<br>0= Assign to interrupt enabled by ILE.EINT0<br>1= Assign to interrupt enabled by ILE.EINT1 |
| 9 | GTEL | RW | R | 0 | Global Time Error Interrupt Select<br>0= Assign to interrupt enabled by ILE.EINT0<br>1= Assign to interrupt enabled by ILE.EINT1 |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 10 | TXUL | RW | R | 0 | Tx Count Underflow Interrupt Select<br>0= Assign to interrupt enabled by ILE.EINT0<br>1= Assign to interrupt enabled by ILE.EINT1 |
| 11 | TXOL | RW | R | 0 | Tx Count Overflow Interrupt Select<br>0= Assign to interrupt enabled by ILE.EINT0<br>1= Assign to interrupt enabled by ILE.EINT1 |
| 12 | SE1L | RW | R | 0 | Scheduling Error 1 Interrupt Select<br>0= Assign to interrupt enabled by ILE.EINT0<br>1= Assign to interrupt enabled by ILE.EINT1 |
| 13 | SE2L | RW | R | 0 | Scheduling Error 2 Interrupt Select<br>0= Assign to interrupt enabled by ILE.EINT0<br>1= Assign to interrupt enabled by ILE.EINT1 |
| 14 | ELCL | RW | R | 0 | Change Error Level Interrupt Select<br>0= Assign to interrupt enabled by ILE.EINT0<br>1= Assign to interrupt enabled by ILE.EINT1 |
| 15 | IWTL | RW | R | 0 | Initialization Watch Trigger Interrupt Select<br>0= Assign to interrupt enabled by ILE.EINT0<br>1= Assign to interrupt enabled by ILE.EINT1 |
| 16 | WTL | RW | R | 0 | Watch Trigger Interrupt Select<br>0= Assign to interrupt enabled by ILE.EINT0<br>1= Assign to interrupt enabled by ILE.EINT1 |
| 17 | AWL_ | RW | R | 0 | Application Watchdog Interrupt Select<br>0= Assign to interrupt enabled by ILE.EINT0<br>1= Assign to interrupt enabled by ILE.EINT1 |
| 18 | CERL | RW | R | 0 | Configuration Error Interrupt Select<br>0= Assign to interrupt enabled by ILE.EINT0<br>1= Assign to interrupt enabled by ILE.EINT1 |

### 2.3.9.6.58 CANFD_CH_TTOST

**Description:** TT Operation Status
**Address:** 0x4052012C
**Offset:** 0x12C
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x80

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | QCS [7:7] | QGTP [6:6] | SYS [5:4] | | MS [3:2] | | EL [1:0] | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | RTO [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | GFI [23:23] | WGTD [22:22] | None [21:16] | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | SPL [31:31] | WECS [30:30] | AWE [29:29] | WFE [28:28] | GSI [27:27] | TMP [26:24] | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:1 | EL | R | RW | 0 | Error Level<br>00= Severity 0 - No Error<br>01= Severity 1 - Warning<br>10= Severity 2 - Error<br>11= Severity 3 - Severe Error |
| 2:3 | MS | R | RW | 0 | Master State<br>00= Master_Off, no master properties relevant<br>01= Operating as Time Slave<br>10= Operating as Backup Time Master<br>11= Operating as current Time Master |
| 4:5 | SYS | R | RW | 0 | Synchronization State<br>00= Out of Synchronization<br>01= Synchronizing to TTCAN communication<br>10= Schedule suspended by Gap (In_Gap)<br>11= Synchronized to schedule (In_Schedule) |
| 6 | QGTP | R | RW | 0 | Quality of Global Time Phase<br>Only relevant in TTCAN Level 0 and Level 2, otherwise fixed to '0'.<br>0= Global time not valid<br>1= Global time in phase with Time Master |
| 7 | QCS | R | RW | 1 | Quality of Clock Speed<br>Only relevant in TTCAN Level 0 and Level 2, otherwise fixed to '1'.<br>0= Local clock speed not synchronized to Time Master clock speed<br>1= Synchronization Deviation <= SDL |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 8:15 | RTO | R | RW | 0 | Reference Trigger Offset<br>The Reference Trigger Offset value is a signed integer with a range from -127 (0x81) to 127 (0x7F).<br>There is no notification when the lower limit of -127 is reached. In case the M_TTCAN becomes<br>Time Master (MS[1:0] = '11'), the reset of RTO is delayed due to synchronization between Host and CAN clock domain. For time slaves the value configured by TTOCF.IRTO is read.<br>0x00-FF Actual Reference Trigger offset value |
| 22 | WGTD | R | RW | 0 | Wait for Global Time Discontinuity<br>0= No global time preset pending<br>1= Node waits for the global time preset to take effect. The bit is reset when the node has transmitted a reference message with Disc_Bit = '1' or after it received a reference message. |
| 23 | GFI | R | RW | 0 | Gap Finished Indicator<br>Set when the CPU writes TTOCN.FGP, or by a time mark interrupt if TMG = '1', or via input pin m_ttcan_evt if TTOCN.GCS = '1'. Not set by Ref_Trigger_Gap or when Gap is finished by another node sending a reference message.<br>0= Reset at the end of each reference message<br>1= Gap finished by M_TTCAN |
| 24:26 | TMP | R | RW | 0 | Time Master Priority<br>0x0-7 Priority of actual Time Master |
| 27 | GSI | R | RW | 0 | Gap Started Indicator<br>0= No Gap in schedule, reset by each reference message and for all time slaves<br>1= Gap time after Basic Cycle has started |
| 28 | WFE | R | RW | 0 | Wait for Event<br>0= No Gap announced, reset by a reference message with Next_is_Gap = '0'<br>1= Reference message with Next_is_Gap = '1' received |
| 29 | AWE | R | RW | 0 | Application Watchdog Event<br>The application watchdog is served by reading TTOST. When the watchdog is not served in time, bit AWE is set, all TTCAN communication is stopped, and the M_TTCAN is set into Bus Monitoring Mode.<br>0= Application Watchdog served in time<br>1= Failed to serve Application Watchdog in time |
| 30 | WECS | R | RW | 0 | Wait for External Clock Synchronization<br>0= No external clock synchronization pending<br>1= Node waits for external clock synchronization to take effect. The bit is reset at the start of the next basic cycle. |
| 31 | SPL | R | RW | 0 | Schedule Phase Lock<br>The bit is valid only when external synchronization is enabled (TTOCN.ESCN = '1'). In this case it signals that the difference between cycle time configured by TTGTP.CTP and the cycle time at the rising edge at pin m_ttcan_evt is less or equal 9 NTU.<br>0= Phase outside range<br>1= Phase inside range |

### 2.3.9.6.59 CANFD_CH_TURNA

**Description:** TUR Numerator Actual
**Address:** 0x40520130
**Offset:** 0x130
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x10000

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | NAV [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | NAV [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:18] | | | | | | NAV [17:16] | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:17 | NAV | R | RW | 65536 | Numerator Actual Value<br>0x0EFFF reserved<br>0x0F000-20FFF Actual numerator value<br>0x21000 reserved |

### 2.3.9.6.60 CANFD_CH_TTLGT

**Description:** TT Local & Global Time
**Address:** 0x40520134
**Offset:** 0x134
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | LT [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | LT [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | GT [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | GT [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | LT | R | RW | 0 | Local Time<br>Non-fractional part of local time, incremented once each local NTU.<br>0x0000-FFFF Local time value of TTCAN node |
| 16:31 | GT | R | RW | 0 | Global Time<br>Non-fractional part of the sum of the node's local time and its local offset.<br>0x0000-FFFF Global time value of TTCAN network |

### 2.3.9.6.61 CANFD_CH_TTCTC

**Description:** TT Cycle Time & Count
**Address:** 0x40520138
**Offset:** 0x138
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x3F0000

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | CT [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | CT [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:22] | | CC [21:16] | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | CT | R | RW | 0 | Cycle Time<br>Non-fractional part of the difference of the node's local time and Ref_Mark.<br>0x0000-FFFF Cycle time value of TTCAN Basic Cycle |
| 16:21 | CC | R | RW | 63 | Cycle Count<br>0x00-3F Number of actual Basic Cycle in the System Matrix |

### 2.3.9.6.62 CANFD_CH_TTCPT

**Description:** TT Capture Time
**Address:** 0x4052013C
**Offset:** 0x13C
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:6] | | CCV [5:0] | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | SWV [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | SWV [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:5 | CCV | R | RW | 0 | Cycle Count Value<br>Cycle count value captured together with SWV.<br>0x00-3F Captured cycle count value |
| 16:31 | SWV | R | RW | 0 | Stop Watch Value<br>On a rising/falling edge (as configured via TTOCN.SWP) at the Stop Watch Trigger pin m_ttcan_swt, when TTOCN.SWS is != '00' and TTIR.SWE is '0', the actual time value as selected by TTOCN.SWS (cycle, local, global) is copied to SWV and TTIR.SWE will be set to '1'. Capturing of the next stop watch value is enabled by resetting TTIR.SWE.<br>0x0000-FFFF Captured Stop Watch value |

### 2.3.9.6.63 CANFD_CH_TTCSM

**Description:** TT Cycle Sync Mark
**Address:** 0x40520140
**Offset:** 0x140
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | CSM [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | CSM [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | CSM | R | RW | 0 | Cycle Sync Mark<br>The Cycle Sync Mark is measured |

# 3 CM0P

**Description** Cortex-M0+ specific registers
**Base Address** 0xE0000000
**Size** 0x20000000
**Slave Num** SYSTEM

## 3.1 DWT

| Register Name | Address | Permission | Description |
|---|---|---|---|
| CM0P_DWT_DWT_CTRL | 0xE0001000 | FULL | Watchpoint Comparator Configuration |
| CM0P_DWT_DWT_PCSR | 0xE000101C | FULL | Watchpoint Comparator PC Sample |
| CM0P_DWT_DWT_COMP0 | 0xE0001020 | FULL | Watchpoint Comparator Compare Value |
| CM0P_DWT_DWT_MASK0 | 0xE0001024 | FULL | Watchpoint Comparator Mask |
| CM0P_DWT_DWT_FUNCTION0 | 0xE0001028 | FULL | Watchpoint Comparator Function |
| CM0P_DWT_DWT_COMP1 | 0xE0001030 | FULL | Watchpoint Comparator Compare Value |
| CM0P_DWT_DWT_MASK1 | 0xE0001034 | FULL | Watchpoint Comparator Mask |
| CM0P_DWT_DWT_FUNCTION1 | 0xE0001038 | FULL | Watchpoint Comparator Function |
| CM0P_DWT_DWT_PID4 | 0xE0001FD0 | FULL | Watchpoint Unit CoreSight ROM Table Peripheral ID #4 |
| CM0P_DWT_DWT_PID0 | 0xE0001FE0 | FULL | Watchpoint Unit CoreSight ROM Table Peripheral ID #0 |
| CM0P_DWT_DWT_PID1 | 0xE0001FE4 | FULL | Watchpoint Unit CoreSight ROM Table Peripheral ID #1 |
| CM0P_DWT_DWT_PID2 | 0xE0001FE8 | FULL | Watchpoint Unit CoreSight ROM Table Peripheral ID #2 |
| CM0P_DWT_DWT_PID3 | 0xE0001FEC | FULL | Watchpoint Unit CoreSight ROM Table Peripheral ID #3 |
| CM0P_DWT_DWT_CID0 | 0xE0001FF0 | FULL | Watchpoint Unit CoreSight ROM Table Component ID #0 |
| CM0P_DWT_DWT_CID1 | 0xE0001FF4 | FULL | Watchpoint Unit CoreSight ROM Table Component ID #1 |
| CM0P_DWT_DWT_CID2 | 0xE0001FF8 | FULL | Watchpoint Unit CoreSight ROM Table Component ID #2 |
| CM0P_DWT_DWT_CID3 | 0xE0001FFC | FULL | Watchpoint Unit CoreSight ROM Table Component ID #3 |

## 3.2 BP

| Register Name | Address | Permission | Description |
|---|---|---|---|
| CM0P_BP_BP_CTRL | 0xE0002000 | FULL | Breakpoint Unit Control |
| CM0P_BP_BP_COMP0 | 0xE0002008 | FULL | Breakpoint Compare Register |
| CM0P_BP_BP_COMP1 | 0xE000200C | FULL | Breakpoint Compare Register |
| CM0P_BP_BP_COMP2 | 0xE0002010 | FULL | Breakpoint Compare Register |
| CM0P_BP_BP_COMP3 | 0xE0002014 | FULL | Breakpoint Compare Register |
| CM0P_BP_BP_PID4 | 0xE0002FD0 | FULL | Breakpoint Unit CoreSight ROM Table Peripheral ID #4 |
| CM0P_BP_BP_PID0 | 0xE0002FE0 | FULL | Breakpoint Unit CoreSight ROM Table Peripheral ID #0 |
| CM0P_BP_BP_PID1 | 0xE0002FE4 | FULL | Breakpoint Unit CoreSight ROM Table Peripheral ID #1 |
| CM0P_BP_BP_PID2 | 0xE0002FE8 | FULL | Breakpoint Unit CoreSight ROM Table Peripheral ID #2 |
| CM0P_BP_BP_PID3 | 0xE0002FEC | FULL | Breakpoint Unit CoreSight ROM Table Peripheral ID #3 |
| CM0P_BP_BP_CID0 | 0xE0002FF0 | FULL | Breakpoint Unit CoreSight ROM Table Component ID #0 |
| CM0P_BP_BP_CID1 | 0xE0002FF4 | FULL | Breakpoint Unit CoreSight ROM Table Component ID #1 |
| CM0P_BP_BP_CID2 | 0xE0002FF8 | FULL | Breakpoint Unit CoreSight ROM Table Component ID #2 |
| CM0P_BP_BP_CID3 | 0xE0002FFC | FULL | Breakpoint Unit CoreSight ROM Table Component ID #3 |

## 3.3 SCS

| Register Name | Address | Permission | Description |
|---|---|---|---|
| CM0P_SCS_SYST_CSR | 0xE000E010 | FULL | SysTick Control & Status |
| CM0P_SCS_SYST_RVR | 0xE000E014 | FULL | SysTick Reload Value |
| CM0P_SCS_SYST_CVR | 0xE000E018 | FULL | SysTick Current Value |
| CM0P_SCS_SYST_CALIB | 0xE000E01C | FULL | SysTick Calibration Value |
| CM0P_SCS_ISER | 0xE000E100 | FULL | Interrupt Set-Enable Register |
| CM0P_SCS_ICER | 0xE000E180 | FULL | Interrupt Clear Enable Register |
| CM0P_SCS_ISPR | 0xE000E200 | FULL | Interrupt Set-Pending Register |
| CM0P_SCS_ICPR | 0xE000E280 | FULL | Interrupt Clear-Pending Register |
| CM0P_SCS_IPR0 | 0xE000E400 | FULL | Interrupt Priority Registers |
| CM0P_SCS_IPR1 | 0xE000E404 | FULL | Interrupt Priority Registers |
| CM0P_SCS_IPR2 | 0xE000E408 | FULL | Interrupt Priority Registers |
| CM0P_SCS_IPR3 | 0xE000E40C | FULL | Interrupt Priority Registers |
| CM0P_SCS_IPR4 | 0xE000E410 | FULL | Interrupt Priority Registers |
| CM0P_SCS_IPR5 | 0xE000E414 | FULL | Interrupt Priority Registers |
| CM0P_SCS_IPR6 | 0xE000E418 | FULL | Interrupt Priority Registers |
| CM0P_SCS_IPR7 | 0xE000E41C | FULL | Interrupt Priority Registers |
| CM0P_SCS_CPUID | 0xE000ED00 | FULL | CPUID Register |
| CM0P_SCS_ICSR | 0xE000ED04 | FULL | Interrupt Control State Register |
| CM0P_SCS_VTOR | 0xE000ED08 | FULL | Vector Table Offset Register |
| CM0P_SCS_AIRCR | 0xE000ED0C | FULL | Application Interrupt and Reset Control Register |
| CM0P_SCS_SCR | 0xE000ED10 | FULL | System Control Register |
| CM0P_SCS_CCR | 0xE000ED14 | FULL | Configuration and Control Register |
| CM0P_SCS_SHPR2 | 0xE000ED1C | FULL | System Handler Priority Register 2 |
| CM0P_SCS_SHPR3 | 0xE000ED20 | FULL | System Handler Priority Register 3 |
| CM0P_SCS_SHCSR | 0xE000ED24 | FULL | System Handler Control and State Register |
| CM0P_SCS_DFSR | 0xE000ED30 | FULL | Debug Fault Status Register |
| CM0P_SCS_MPU_TYPE | 0xE000ED90 | FULL | MPU Type Register |
| CM0P_SCS_MPU_CTRL | 0xE000ED94 | FULL | MPU Control Register |
| CM0P_SCS_MPU_RNR | 0xE000ED98 | FULL | MPU Region Number Register |
| CM0P_SCS_MPU_RBAR | 0xE000ED9C | FULL | MPU Region Base Address Register |
| CM0P_SCS_MPU_RASR | 0xE000EDA0 | FULL | MPU Region Attribute and Size Register |
| CM0P_SCS_DHCSR | 0xE000EDF0 | FULL | Debug Halting Control and Status Register |
| CM0P_SCS_DCRSR | 0xE000EDF4 | FULL | Debug Core Register Selector Register |
| CM0P_SCS_DCRDR | 0xE000EDF8 | FULL | Debug Core Register Data Register |
| CM0P_SCS_DEMCR | 0xE000EDFC | FULL | Debug Exception and Monitor Control Register |
| CM0P_SCS_SCS_PID4 | 0xE000EFD0 | FULL | System Control Space ROM Table Peripheral ID #4 |
| CM0P_SCS_SCS_PID0 | 0xE000EFE0 | FULL | System Control Space ROM Table Peripheral ID #0 |
| CM0P_SCS_SCS_PID1 | 0xE000EFE4 | FULL | System Control Space ROM Table Peripheral ID #1 |
| CM0P_SCS_SCS_PID2 | 0xE000EFE8 | FULL | System Control Space ROM Table Peripheral ID #2 |
| CM0P_SCS_SCS_PID3 | 0xE000EFEC | FULL | System Control Space ROM Table Peripheral ID #3 |
| CM0P_SCS_SCS_CID0 | 0xE000EFF0 | FULL | System Control Space ROM Table Component ID #0 |
| CM0P_SCS_SCS_CID1 | 0xE000EFF4 | FULL | System Control Space ROM Table Component ID #1 |
| CM0P_SCS_SCS_CID2 | 0xE000EFF8 | FULL | System Control Space ROM Table Component ID #2 |
| CM0P_SCS_SCS_CID3 | 0xE000EFFC | FULL | System Control Space ROM Table Component ID #3 |

## 3.4 ROM

| Register Name | Address | Permission | Description |
|---|---|---|---|
| CM0P_ROM_ROM_SCS | 0xE00FF000 | FULL | CM0+ CoreSight ROM Table Peripheral #0 |
| CM0P_ROM_ROM_DWT | 0xE00FF004 | FULL | CM0+ CoreSight ROM Table Peripheral #1 |
| CM0P_ROM_ROM_BPU | 0xE00FF008 | FULL | CM0+ CoreSight ROM Table Peripheral #2 |
| CM0P_ROM_ROM_END | 0xE00FF00C | FULL | CM0+ CoreSight ROM Table End Marker |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| CM0P_ROM_ROM_CSMT | 0xE00FFFCC | FULL | CM0+ CoreSight ROM Table Memory Type |
| CM0P_ROM_ROM_PID4 | 0xE00FFFD0 | FULL | CM0+ CoreSight ROM Table Peripheral ID #4 |
| CM0P_ROM_ROM_PID0 | 0xE00FFFE0 | FULL | CM0+ CoreSight ROM Table Peripheral ID #0 |
| CM0P_ROM_ROM_PID1 | 0xE00FFFE4 | FULL | CM0+ CoreSight ROM Table Peripheral ID #1 |
| CM0P_ROM_ROM_PID2 | 0xE00FFFE8 | FULL | CM0+ CoreSight ROM Table Peripheral ID #2 |
| CM0P_ROM_ROM_PID3 | 0xE00FFFEC | FULL | CM0+ CoreSight ROM Table Peripheral ID #3 |
| CM0P_ROM_ROM_CID0 | 0xE00FFFF0 | FULL | CM0+ CoreSight ROM Table Component ID #0 |
| CM0P_ROM_ROM_CID1 | 0xE00FFFF4 | FULL | CM0+ CoreSight ROM Table Component ID #1 |
| CM0P_ROM_ROM_CID2 | 0xE00FFFF8 | FULL | CM0+ CoreSight ROM Table Component ID #2 |
| CM0P_ROM_ROM_CID3 | 0xE00FFFFC | FULL | CM0+ CoreSight ROM Table Component ID #3 |

## 3.5 ROMTABLE

| Register Name | Address | Permission | Description |
|---|---|---|---|
| CM0P_ROMTABLE_ADDR0 | 0xF0000000 | FULL | Link to Cortex M0+ ROM Table. |
| CM0P_ROMTABLE_ADDR1 | 0xF0000004 | FULL | Link to CoreSight CTI Table. |
| CM0P_ROMTABLE_ADDR2 | 0xF0000008 | FULL | Link to Cortex M0+ MTB Table. |
| CM0P_ROMTABLE_DID | 0xF0000FCC | FULL | Device Type Identifier register. |
| CM0P_ROMTABLE_PID4 | 0xF0000FD0 | FULL | Peripheral Identification Register 4. |
| CM0P_ROMTABLE_PID5 | 0xF0000FD4 | FULL | Peripheral Identification Register 5. |
| CM0P_ROMTABLE_PID6 | 0xF0000FD8 | FULL | Peripheral Identification Register 6. |
| CM0P_ROMTABLE_PID7 | 0xF0000FDC | FULL | Peripheral Identification Register 7. |
| CM0P_ROMTABLE_PID0 | 0xF0000FE0 | FULL | Peripheral Identification Register 0. |
| CM0P_ROMTABLE_PID1 | 0xF0000FE4 | FULL | Peripheral Identification Register 1. |
| CM0P_ROMTABLE_PID2 | 0xF0000FE8 | FULL | Peripheral Identification Register 2. |
| CM0P_ROMTABLE_PID3 | 0xF0000FEC | FULL | Peripheral Identification Register 3. |
| CM0P_ROMTABLE_CID0 | 0xF0000FF0 | FULL | Component Identification Register 0. |
| CM0P_ROMTABLE_CID1 | 0xF0000FF4 | FULL | Component Identification Register 1. |
| CM0P_ROMTABLE_CID2 | 0xF0000FF8 | FULL | Component Identification Register 2. |
| CM0P_ROMTABLE_CID3 | 0xF0000FFC | FULL | Component Identification Register 3. |

## 3.6 CTI

| Register Name | Address | Permission | Description |
|---|---|---|---|
| CM0P_CTI_CTICONTROL | 0xF0002000 | FULL | CTI Control Register |
| CM0P_CTI_CTIINTACK | 0xF0002010 | FULL | CTI Interrupt Acknowledge Register |
| CM0P_CTI_CTIAPPSET | 0xF0002014 | FULL | CTI Application Trigger Set Register |
| CM0P_CTI_CTIAPPCLEAR | 0xF0002018 | FULL | CTI Application Trigger Clear Register |
| CM0P_CTI_CTIAPPPULSE | 0xF000201C | FULL | CTI Application Pulse Register |
| CM0P_CTI_CTIINEN0 | 0xF0002020 | FULL | CTI Trigger to Channel Enable Registers |
| CM0P_CTI_CTIINEN1 | 0xF0002024 | FULL | CTI Trigger to Channel Enable Registers |
| CM0P_CTI_CTIINEN2 | 0xF0002028 | FULL | CTI Trigger to Channel Enable Registers |
| CM0P_CTI_CTIINEN3 | 0xF000202C | FULL | CTI Trigger to Channel Enable Registers |
| CM0P_CTI_CTIINEN4 | 0xF0002030 | FULL | CTI Trigger to Channel Enable Registers |
| CM0P_CTI_CTIINEN5 | 0xF0002034 | FULL | CTI Trigger to Channel Enable Registers |
| CM0P_CTI_CTIINEN6 | 0xF0002038 | FULL | CTI Trigger to Channel Enable Registers |
| CM0P_CTI_CTIINEN7 | 0xF000203C | FULL | CTI Trigger to Channel Enable Registers |
| CM0P_CTI_CTIOUTEN0 | 0xF00020A0 | FULL | CTI Channel to Trigger Enable Registers |
| CM0P_CTI_CTIOUTEN1 | 0xF00020A4 | FULL | CTI Channel to Trigger Enable Registers |
| CM0P_CTI_CTIOUTEN2 | 0xF00020A8 | FULL | CTI Channel to Trigger Enable Registers |
| CM0P_CTI_CTIOUTEN3 | 0xF00020AC | FULL | CTI Channel to Trigger Enable Registers |
| CM0P_CTI_CTIOUTEN4 | 0xF00020B0 | FULL | CTI Channel to Trigger Enable Registers |
| CM0P_CTI_CTIOUTEN5 | 0xF00020B4 | FULL | CTI Channel to Trigger Enable Registers |
| CM0P_CTI_CTIOUTEN6 | 0xF00020B8 | FULL | CTI Channel to Trigger Enable Registers |
| CM0P_CTI_CTIOUTEN7 | 0xF00020BC | FULL | CTI Channel to Trigger Enable Registers |
| CM0P_CTI_CTITRIGINSTATUS | 0xF0002130 | FULL | CTI Trigger In Status Register |
| CM0P_CTI_CTITRIGOUTSTATUS | 0xF0002134 | FULL | CTI Trigger Out Status Register |
| CM0P_CTI_CTICHINSTATUS | 0xF0002138 | FULL | CTI Channel In Status Register |
| CM0P_CTI_CTICHOUTSTATUS | 0xF000213C | FULL | CTI Channel Out Status Register |
| CM0P_CTI_CTIGATE | 0xF0002140 | FULL | Enable CTI Channel Gate Register |
| CM0P_CTI_ASICCTL | 0xF0002144 | FULL | External Multiplexor Control Register |
| CM0P_CTI_ITCHINACK | 0xF0002EDC | FULL | ITCHINACK Register |
| CM0P_CTI_ITTRIGINACK | 0xF0002EE0 | FULL | ITTRIGINACK Register |
| CM0P_CTI_ITCHOUT | 0xF0002EE4 | FULL | ITCHOUT Register |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| CM0P_CTI_ITTRIGOUT | 0xF0002EE8 | FULL | ITTRIGOUT Register |
| CM0P_CTI_ITCHOUTACK | 0xF0002EEC | FULL | ITCHOUTACK Register |
| CM0P_CTI_ITTRIGOUTACK | 0xF0002EF0 | FULL | ITTRIGOUTACK Register |
| CM0P_CTI_ITCHIN | 0xF0002EF4 | FULL | ITCHIN Register |
| CM0P_CTI_ITTRIGIN | 0xF0002EF8 | FULL | ITTRIGIN Register |
| CM0P_CTI_ITCTRL | 0xF0002F00 | FULL | Integration Mode Control Register |
| CM0P_CTI_CLAIMSET | 0xF0002FA0 | FULL | Claim Tag Set Register |
| CM0P_CTI_CLAIMCLR | 0xF0002FA4 | FULL | Claim Tag Clear Register |
| CM0P_CTI_LOCKACCESS | 0xF0002FB0 | FULL | Lock Access Register |
| CM0P_CTI_LOCKSTATUS | 0xF0002FB4 | FULL | Lock Status Register |
| CM0P_CTI_AUTHSTATUS | 0xF0002FB8 | FULL | Authentication Status Register |
| CM0P_CTI_DEVID | 0xF0002FC8 | FULL | Device Configuration Register |
| CM0P_CTI_DEVTYPE | 0xF0002FCC | FULL | Device Type Identifier Register |
| CM0P_CTI_PID4 | 0xF0002FD0 | FULL | Peripheral Identification Register 4 |
| CM0P_CTI_PID5 | 0xF0002FD4 | FULL | Peripheral Identification Register 5 |
| CM0P_CTI_PID6 | 0xF0002FD8 | FULL | Peripheral Identification Register 6 |
| CM0P_CTI_PID7 | 0xF0002FDC | FULL | Peripheral Identification Register 7 |
| CM0P_CTI_PID0 | 0xF0002FE0 | FULL | Peripheral Identification Register 0 |
| CM0P_CTI_PID1 | 0xF0002FE4 | FULL | Peripheral Identification Register 1 |
| CM0P_CTI_PID2 | 0xF0002FE8 | FULL | Peripheral Identification Register 2 |
| CM0P_CTI_PID3 | 0xF0002FEC | FULL | Peripheral Identification Register 3 |
| CM0P_CTI_CID0 | 0xF0002FF0 | FULL | Component Identification Register 0 |
| CM0P_CTI_CID1 | 0xF0002FF4 | FULL | Component Identification Register 1 |
| CM0P_CTI_CID2 | 0xF0002FF8 | FULL | Component Identification Register 2 |
| CM0P_CTI_CID3 | 0xF0002FFC | FULL | Component Identification Register 3 |

## 3.7 MTB

| Register Name | Address | Permission | Description |
|---|---|---|---|
| CM0P_MTB_POSITION | 0xF0003000 | FULL | POSITION register |
| CM0P_MTB_MASTER | 0xF0003004 | FULL | MASTER register |
| CM0P_MTB_FLOW | 0xF0003008 | FULL | FLOW register |
| CM0P_MTB_BASE | 0xF000300C | FULL | BASE register |
| CM0P_MTB_LA | 0xF0003FB0 | FULL | Lock Access register |
| CM0P_MTB_LS | 0xF0003FB4 | FULL | Lock Status register |
| CM0P_MTB_AS | 0xF0003FB8 | FULL | Authentication Status register |
| CM0P_MTB_DARCH | 0xF0003FBC | FULL | Device Architecture register |
| CM0P_MTB_DCFG | 0xF0003FC8 | FULL | Device Configuration register |
| CM0P_MTB_DID | 0xF0003FCC | FULL | Device Type Identifier register. |
| CM0P_MTB_PID4 | 0xF0003FD0 | FULL | Peripheral Identification Register 4. |
| CM0P_MTB_PID5 | 0xF0003FD4 | FULL | Peripheral Identification Register 5. |
| CM0P_MTB_PID6 | 0xF0003FD8 | FULL | Peripheral Identification Register 6. |
| CM0P_MTB_PID7 | 0xF0003FDC | FULL | Peripheral Identification Register 7. |
| CM0P_MTB_PID0 | 0xF0003FE0 | FULL | Peripheral Identification Register 0. |
| CM0P_MTB_PID1 | 0xF0003FE4 | FULL | Peripheral Identification Register 1. |
| CM0P_MTB_PID2 | 0xF0003FE8 | FULL | Peripheral Identification Register 2. |
| CM0P_MTB_PID3 | 0xF0003FEC | FULL | Peripheral Identification Register 3. |
| CM0P_MTB_CID0 | 0xF0003FF0 | FULL | Component Identification Register 0. |
| CM0P_MTB_CID1 | 0xF0003FF4 | FULL | Component Identification Register 1. |
| CM0P_MTB_CID2 | 0xF0003FF8 | FULL | Component Identification Register 2. |
| CM0P_MTB_CID3 | 0xF0003FFC | FULL | Component Identification Register 3. |

## 3.8 Register Details

### 3.8.1 DWT

#### 3.8.1.1 CM0P_DWT_DWT_CTRL

**Description:** Watchpoint Comparator Configuration
**Address:** 0xE0001000
**Offset:** 0x0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Defines the number of comparators implemented
**Default:** 0x20000000

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | NUMCOMP [31:28] | | | | None [27:24] | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 28:31 | NUMCOMP | R | | 2 | Number of comparators available |

### 3.8.1.2 CM0P_DWT_DWT_PCSR

**Description:** Watchpoint Comparator PC Sample
**Address:** 0xE000101C
**Offset:** 0x1C
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Samples the current value of the program counter. Unless DWT_PCSR reads as 0xFFFFFFFF, under the conditions described in Program counter sampling support on Arm TRM page C1-344, bit [0] is RAZ. When RAZ, bit [0] does not reflect instruction set state as is the case with similar functionality in other ARM architecture profiles.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | EIASAMPLE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | EIASAMPLE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | EIASAMPLE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | EIASAMPLE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | EIASAMPLE | R | W | X | Executed Instruction Address sample value |

### 3.8.1.3 CM0P_DWT_DWT_COMP0

**Description:** Watchpoint Comparator Compare Value
**Address:** 0xE0001020
**Offset:** 0x20
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Provides a reference value for use by comparator
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | COMP [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | COMP [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | COMP [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | COMP [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | COMP | RW | R | X | Reference value for comparison. See The DWT comparators on Arm TRM page C1-341. |

### 3.8.1.4 CM0P_DWT_DWT_MASK0

**Description:** Watchpoint Comparator Mask
**Address:** 0xE0001024
**Offset:** 0x24
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Provides the size of the ignore mask applied to the access address range matching
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | MASK [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | MASK [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | MASK [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | MASK [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | MASK | RW | R | X | The size of the ignore mask applied to address range matching. See The DWT comparators on Arm TRM page C1-341 for the usage model. The mask range is IMPLEMENTATION DEFINED. Writing all ones to this field and reading it back can be used to determine the maximum mask size supported. |

### 3.8.1.5 CM0P_DWT_DWT_FUNCTION0

**Description:** Watchpoint Comparator Function
**Address:** 0xE0001028
**Offset:** 0x28
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Controls the operation of the comparator
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:4] | | | | FUNCTION [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:25] | | | | | | | MATCHED [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | FUNCTION | RW | R | 0 | Select action on comparator match. |
| | DISABLE | | | 0 | Disabled |
| | IADDR | | | 4 | PC watchpoint event |
| | DADDR_RO | | | 5 | Watchpoint event |
| | DADDR_WO | | | 6 | Watchpoint event |
| | DADDR_RW | | | 7 | Watchpoint event |
| 24 | MATCHED | R | RW | 0 | Comparator match. It indicates that the operation defined by FUNCTION has occurred since the bit was last read:<br>0 the associated comparator has matched.<br>1 the associated comparator has not matched.<br>Reading the register clears this bit to 0. |

### 3.8.1.6 CM0P_DWT_DWT_COMP1

**Description:** Watchpoint Comparator Compare Value
**Address:** 0xE0001030
**Offset:** 0x30
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Provides a reference value for use by comparator
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | COMP [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | COMP [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | COMP [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | COMP [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | COMP | RW | R | X | Reference value for comparison. See The DWT comparators on Arm TRM page C1-341. |

### 3.8.1.7 CM0P_DWT_DWT_MASK1

**Description:** Watchpoint Comparator Mask
**Address:** 0xE0001034
**Offset:** 0x34
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Provides the size of the ignore mask applied to the access address range matching
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | MASK [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | MASK [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | MASK [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | MASK [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | MASK | RW | R | X | The size of the ignore mask applied to address range matching. See The DWT comparators on Arm TRM page C1-341 for the usage model. The mask range is IMPLEMENTATION DEFINED. Writing all ones to this field and reading it back can be used to determine the maximum mask size supported. |

### 3.8.1.8 CM0P_DWT_DWT_FUNCTION1

**Description:** Watchpoint Comparator Function
**Address:** 0xE0001038
**Offset:** 0x38
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Controls the operation of the comparator
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:4] | | | | FUNCTION [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:25] | | | | | | | MATCHED [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | FUNCTION | RW | R | 0 | Select action on comparator match. |
| | DISABLE | | | 0 | Disabled |
| | IADDR | | | 4 | PC watchpoint event |
| | DADDR_RO | | | 5 | Watchpoint event |
| | DADDR_WO | | | 6 | Watchpoint event |
| | DADDR_RW | | | 7 | Watchpoint event |
| 24 | MATCHED | R | RW | 0 | Comparator match. It indicates that the operation defined by FUNCTION has occurred since the bit was last read:<br>0 the associated comparator has matched.<br>1 the associated comparator has not matched.<br>Reading the register clears this bit to 0. |

### 3.8.1.9 CM0P_DWT_DWT_PID4

**Description:** Watchpoint Unit CoreSight ROM Table Peripheral ID #4
**Address:** 0xE0001FD0
**Offset:** 0xFD0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x4

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | | 4 | Peripheral ID #4 |

### 3.8.1.10 CM0P_DWT_DWT_PID0

**Description:** Watchpoint Unit CoreSight ROM Table Peripheral ID #0
**Address:** 0xE0001FE0
**Offset:** 0xFE0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xA

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | | 10 | Peripheral ID #0 |

### 3.8.1.11 CM0P_DWT_DWT_PID1

**Description:** Watchpoint Unit CoreSight ROM Table Peripheral ID #1
**Address:** 0xE0001FE4
**Offset:** 0xFE4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xB0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | | 176 | Peripheral ID #1 |

### 3.8.1.12 CM0P_DWT_DWT_PID2

**Description:** Watchpoint Unit CoreSight ROM Table Peripheral ID #2
**Address:** 0xE0001FE8
**Offset:** 0xFE8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xB

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | | 11 | Peripheral ID #2 |

### 3.8.1.13 CM0P_DWT_DWT_PID3

**Description:** Watchpoint Unit CoreSight ROM Table Peripheral ID #3
**Address:** 0xE0001FEC
**Offset:** 0xFEC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | | 0 | Peripheral ID #3 |

### 3.8.1.14 CM0P_DWT_DWT_CID0

**Description:** Watchpoint Unit CoreSight ROM Table Component ID #0
**Address:** 0xE0001FF0
**Offset:** 0xFF0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xD

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | | 13 | Component ID #0 |

### 3.8.1.15 CM0P_DWT_DWT_CID1

**Description:** Watchpoint Unit CoreSight ROM Table Component ID #1
**Address:** 0xE0001FF4
**Offset:** 0xFF4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xE0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | | 224 | Component ID #1 |

### 3.8.1.16 CM0P_DWT_DWT_CID2

**Description:** Watchpoint Unit CoreSight ROM Table Component ID #2
**Address:** 0xE0001FF8
**Offset:** 0xFF8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x5

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | | 5 | Component ID #2 |

### 3.8.1.17 CM0P_DWT_DWT_CID3

**Description:** Watchpoint Unit CoreSight ROM Table Component ID #3
**Address:** 0xE0001FFC
**Offset:** 0xFFC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xB1

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | | 177 | Component ID #3 |

### 3.8.2 BP

#### 3.8.2.1 CM0P_BP_BP_CTRL

**Description:** Breakpoint Unit Control
**Address:** 0xE0002000
**Offset:** 0x0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Provides BPU implementation information, and the global enable for the BPU.
**Default:** 0x40

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | NUM_CODE [7:4] | | | | None [3:2] | | KEY [1:1] | ENABLE [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | ENABLE | RW | R | 0 | Enables the BPU:<br>0 BPU is disabled.<br>1 BPU is enabled. |
| 1 | KEY | RW | R | 0 | RAZ on reads, SBO for writes. If written as zero, the write to the register is ignored. |
| 4:7 | NUM_CODE | R | | 4 | The number of breakpoint comparators. If NUM_CODE is zero, the implementation does not support any comparators. |

### 3.8.2.2 CM0P_BP_BP_COMP0

**Description:** Breakpoint Compare Register
**Address:** 0xE0002008
**Offset:** 0x8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Holds a breakpoint address for comparison with instruction addresses in the Code memory region, see The system address map on Arm TRM page B3-258 for more information.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | COMP_ADDR [7:2] | | | | | | None [1:1] | ENABLE [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | COMP_ADDR [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | COMP_ADDR [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | MATCH [31:30] | | None [29:29] | COMP_ADDR [28:24] | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | ENABLE | RW | R | 0 | Enables the comparator:<br>Note BP_CTRL.ENABLE must also be set to 1 to enable a comparator. |
| 2:28 | COMP_ADDR | RW | R | X | Stores bits [28:2] of the comparison address. The comparison address is compared with the address from the Code memory region. Bits [31:29] and [1:0] of the comparison address are zero. |
| 30:31 | MATCH | RW | R | X | BP_MATCH defines the behavior when the COMP address is matched. |
| | NONE | | | 0 | No breakpoint matching |
| | LOWER | | | 1 | Breakpoint on lower halfword, upper is unaffected. |
| | UPPER | | | 2 | Breakpoint on upper halfword, lower is unaffected. |
| | BOTH | | | 3 | Breakpoint on both lower and upper halfwords. |

### 3.8.2.3 CM0P_BP_BP_COMP1

**Description:** Breakpoint Compare Register
**Address:** 0xE000200C
**Offset:** 0xC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Holds a breakpoint address for comparison with instruction addresses in the Code memory region, see The system address map on Arm TRM page B3-258 for more information.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | COMP_ADDR [7:2] | | | | | | None [1:1] | ENABLE [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | COMP_ADDR [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | COMP_ADDR [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | MATCH [31:30] | | None [29:29] | COMP_ADDR [28:24] | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | ENABLE | RW | R | 0 | Enables the comparator:<br>Note BP_CTRL.ENABLE must also be set to 1 to enable a comparator. |
| 2:28 | COMP_ADDR | RW | R | X | Stores bits [28:2] of the comparison address. The comparison address is compared with the address from the Code memory region. Bits [31:29] and [1:0] of the comparison address are zero. |
| 30:31 | MATCH | RW | R | X | BP_MATCH defines the behavior when the COMP address is matched. |
| | NONE | | | 0 | No breakpoint matching |
| | LOWER | | | 1 | Breakpoint on lower halfword, upper is unaffected. |
| | UPPER | | | 2 | Breakpoint on upper halfword, lower is unaffected. |
| | BOTH | | | 3 | Breakpoint on both lower and upper halfwords. |

### 3.8.2.4 CM0P_BP_BP_COMP2

**Description:** Breakpoint Compare Register
**Address:** 0xE0002010
**Offset:** 0x10
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Holds a breakpoint address for comparison with instruction addresses in the Code memory region, see The system address map on Arm TRM page B3-258 for more information.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | COMP_ADDR [7:2] | | | | | | None [1:1] | ENABLE [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | COMP_ADDR [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | COMP_ADDR [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | MATCH [31:30] | | None [29:29] | COMP_ADDR [28:24] | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | ENABLE | RW | R | 0 | Enables the comparator:<br>Note BP_CTRL.ENABLE must also be set to 1 to enable a comparator. |
| 2:28 | COMP_ADDR | RW | R | X | Stores bits [28:2] of the comparison address. The comparison address is compared with the address from the Code memory region. Bits [31:29] and [1:0] of the comparison address are zero. |
| 30:31 | MATCH | RW | R | X | BP_MATCH defines the behavior when the COMP address is matched. |
| | NONE | | | 0 | No breakpoint matching |
| | LOWER | | | 1 | Breakpoint on lower halfword, upper is unaffected. |
| | UPPER | | | 2 | Breakpoint on upper halfword, lower is unaffected. |
| | BOTH | | | 3 | Breakpoint on both lower and upper halfwords. |

### 3.8.2.5 CM0P_BP_BP_COMP3

**Description:** Breakpoint Compare Register
**Address:** 0xE0002014
**Offset:** 0x14
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Holds a breakpoint address for comparison with instruction addresses in the Code memory region, see The system address map on Arm TRM page B3-258 for more information.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | COMP_ADDR [7:2] | | | | | | None [1:1] | ENABLE [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | COMP_ADDR [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | COMP_ADDR [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | MATCH [31:30] | | None [29:29] | COMP_ADDR [28:24] | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | ENABLE | RW | R | 0 | Enables the comparator.<br>Note BP_CTRL.ENABLE must also be set to 1 to enable a comparator. |
| 2:28 | COMP_ADDR | RW | R | X | Stores bits [28:2] of the comparison address. The comparison address is compared with the address from the Code memory region. Bits [31:29] and [1:0] of the comparison address are zero. |
| 30:31 | MATCH | RW | R | X | BP_MATCH defines the behavior when the COMP address is matched. |
| | NONE | | | 0 | No breakpoint matching |
| | LOWER | | | 1 | Breakpoint on lower halfword, upper is unaffected. |
| | UPPER | | | 2 | Breakpoint on upper halfword, lower is unaffected. |
| | BOTH | | | 3 | Breakpoint on both lower and upper halfwords. |

### 3.8.2.6 CM0P_BP_BP_PID4

**Description:** Breakpoint Unit CoreSight ROM Table Peripheral ID #4
**Address:** 0xE0002FD0
**Offset:** 0xFD0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x4

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | | 4 | Peripheral ID #4 |

### 3.8.2.7 CM0P_BP_BP_PID0

**Description:** Breakpoint Unit CoreSight ROM Table Peripheral ID #0
**Address:** 0xE0002FE0
**Offset:** 0xFE0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xB

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | | 11 | Peripheral ID #0 |

### 3.8.2.8 CM0P_BP_BP_PID1

**Description:** Breakpoint Unit CoreSight ROM Table Peripheral ID #1
**Address:** 0xE0002FE4
**Offset:** 0xFE4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xB0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | | 176 | Peripheral ID #1 |

### 3.8.2.9 CM0P_BP_BP_PID2

**Description:** Breakpoint Unit CoreSight ROM Table Peripheral ID #2
**Address:** 0xE0002FE8
**Offset:** 0xFE8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xB

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | | 11 | Peripheral ID #2 |

### 3.8.2.10 CM0P_BP_BP_PID3

**Description:** Breakpoint Unit CoreSight ROM Table Peripheral ID #3
**Address:** 0xE0002FEC
**Offset:** 0xFEC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | | 0 | Peripheral ID #3 |

### 3.8.2.11 CM0P_BP_BP_CID0

**Description:** Breakpoint Unit CoreSight ROM Table Component ID #0
**Address:** 0xE0002FF0
**Offset:** 0xFF0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xD

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | | 13 | Component ID #0 |

### 3.8.2.12 CM0P_BP_BP_CID1

**Description:** Breakpoint Unit CoreSight ROM Table Component ID #1
**Address:** 0xE0002FF4
**Offset:** 0xFF4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xE0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | | 224 | Component ID #1 |

### 3.8.2.13 CM0P_BP_BP_CID2

**Description:** Breakpoint Unit CoreSight ROM Table Component ID #2
**Address:** 0xE0002FF8
**Offset:** 0xFF8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x5

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | | 5 | Component ID #2 |

### 3.8.2.14 CM0P_BP_BP_CID3

**Description:** Breakpoint Unit CoreSight ROM Table Component ID #3
**Address:** 0xE0002FFC
**Offset:** 0xFFC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xB1

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | | 177 | Component ID #3 |

### 3.8.3 SCS

#### 3.8.3.1 CM0P_SCS_SYST_CSR

**Description:** SysTick Control & Status
**Address:** 0xE000E010
**Offset:** 0x10
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Controls the SysTick counter and provides status data. The SysTick counter is functional in the Active and Sleep power modes (and not functional in the DeepSleep, and Hibernate power modes).
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:3] | | | | | CLKSOURCE [2:2] | TICKINT [1:1] | ENABLE [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:17] | | | | | | | COUNTFLAG [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | ENABLE | RW | R | 0 | Indicates the enabled status of the SysTick counter:<br>'0': counter is disabled.<br>'1': counter is operating. |
| 1 | TICKINT | RW | R | 0 | Indicates whether counting to '0' causes the status of the SysTick exception to change to pending:<br>'0': count to '0' does not affect the SysTick exception status.<br>'1': count to '0' changes the SysTick exception status to pending.<br><br>Changing the value of the counter to '0' by writing zero to the SYST_CVR register to '0' never changes the status of the SysTick exception. |
| 2 | CLKSOURCE | RW | R | 0 | Indicates the SysTick counter clock source:<br>'0': SysTick uses the low frequency clock 'clk_lf'. For this mode to function, 'clk_lf' should be less than half the frequency of 'clk_sys'. Note that 'clk_lf' is generated by a low accuracy ILO (Internal Low power Oscillator), with a target frequency of 32.768 kHz (frequency can be as low as 15 KHz and as high as 60 kHz).<br>'1': SysTick uses the system/processor clock 'clk_sys'.<br><br>In PSoC4A-BLE (and later products), SysTick counter functionality on the low frequency clock is provided. in SF, TSG6M products, this functionality is not provided. For these products, this field should be set to '1', such that SysTick uses the system clock 'clk_sys'. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 16 | COUNTFLAG | R | RW | 0 | Indicates whether the counter has counted to '0' since the last read of this register:<br>'0': counter has not counted to '0'.<br>'1': counter has counted to '0'.<br><br>COUNTFLAG is set to '1' by a count transition from '1' to '0'.<br>COUNTFLAG is cleared to '0' by a read of this register, and by any write to the SYST_CVR register. |

### 3.8.3.2 CM0P_SCS_SYST_RVR

**Description:** SysTick Reload Value
**Address:** 0xE000E014
**Offset:** 0x14
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Sets or reads the reload value of the SYST_CVR register.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | RELOAD [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | RELOAD [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | RELOAD [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:23 | RELOAD | RW | R | X | The value to load into the SYST_CVR register when the counter reaches 0. |

### 3.8.3.3 CM0P_SCS_SYST_CVR

**Description:** SysTick Current Value
**Address:** 0xE000E018
**Offset:** 0x18
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Reads or clears the current counter value. Any write to the register clears the register to 0.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | CURRENT [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | CURRENT [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | CURRENT [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:23 | CURRENT | RW | R | X | Current counter value.<br>This is the value of the counter at the time it is sampled. |

### 3.8.3.4 CM0P_SCS_SYST_CALIB

**Description:** SysTick Calibration Value
**Address:** 0xE000E01C
**Offset:** 0x1C
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Reads the calibration value and parameters for SysTick.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | TENMS [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | TENMS [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | TENMS [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | NOREF [31:31] | SKEW [30:30] | None [29:24] | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:23 | TENMS | R | RW | X | Optionally, holds a reload value to be used for 10ms (100Hz) timing, subject to system clock skew errors. If this field is '0', the calibration value is not known.<br><br>In PSoC4A-BLE (and later products), SysTick counter functionality on the low frequency clock is provided and this field is 0x00:00147. In earlier products, SysTick counter functionality on the low frequency clock is NOT provided and this field is 0x00:0000. |
| 30 | SKEW | R | RW | X | Indicates whether the 10ms calibration value is exact:<br>'0': 10ms calibration value is exact.<br>'1': 10ms calibration value is inexact, because of the clock frequency.<br><br>In PSoC4A-BLE (and later products), SysTick counter functionality on the low frequency clock is provided and this field is '1' (due to the low accuracy ILO). In earlier products, SysTick counter functionality on the low frequency clock is NOT provided and this field is '0'. |
| 31 | NOREF | R | | 0 | Indicates whether a implementation defined reference clock is provided:<br>'0': the reference clock is provided.<br>'1': the reference clock is not provided.<br>When this bit is '1', the SYST_CSR.CLKSOURCEis forced to '1' and cannot be cleared to '0'.<br><br>In PSoC4A-BLE (and later products), SysTick counter functionality on the low frequency clock is provided and this field is '0'. In earlier products, SysTick counter functionality on the low frequency clock is NOT provided and this field is '1'. |

### 3.8.3.5 CM0P_SCS_ISER

**Description:** Interrupt Set-Enable Register
**Address:** 0xE000E100
**Offset:** 0x100
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Enables, or reads the enabled state of one or more interrupts.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | SETENA [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | SETENA [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | SETENA [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | SETENA [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | SETENA | RW1S | R | 0 | Enables, or reads the enabled state of one or more interrupts. Each bit corresponds to the same numbered interrupt. |

### 3.8.3.6 CM0P_SCS_ICER

**Description:** Interrupt Clear Enable Register
**Address:** 0xE000E180
**Offset:** 0x180
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Disables, or reads the enabled state of one or more interrupts
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | CLRENA [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | CLRENA [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | CLRENA [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | CLRENA [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | CLRENA | RW1C | R | 0 | Disables, or reads the enabled state of one or more interrupts. Each bit corresponds to the same numbered interrupt. |

### 3.8.3.7 CM0P_SCS_ISPR

**Description:** Interrupt Set-Pending Register
**Address:** 0xE000E200
**Offset:** 0x200
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** On writes, sets the status of one or more interrupts to pending. On reads, shows the pending status of the interrupts.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | SETPEND [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | SETPEND [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | SETPEND [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | SETPEND [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | SETPEND | RW1S | R | 0 | Changes the state of one or more interrupts to pending. Each bit corresponds to the same numbered interrupt. |

### 3.8.3.8 CM0P_SCS_ICPR

**Description:** Interrupt Clear-Pending Register
**Address:** 0xE000E280
**Offset:** 0x280
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** On writes, clears the status of one or more interrupts to pending. On reads, shows the pending status of the interrupts.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | CLRPEND [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | CLRPEND [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | CLRPEND [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | CLRPEND [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | CLRPEND | RW1C | R | 0 | Changes the state of one or more interrupts to not pending. Each bit corresponds to the same numbered interrupt. |

### 3.8.3.9 CM0P_SCS_IPR

**Description:** Interrupt Priority Registers
**Address:** 0xE000E400
**Offset:** 0x400
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Sets or reads interrupt priorities. Register n contains priorities for interrupts N=4n .. 4n+3
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | PRI_N0 [7:6] | | None [5:0] | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | PRI_N1 [15:14] | | None [13:8] | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | PRI_N2 [23:22] | | None [21:16] | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | PRI_N3 [31:30] | | None [29:24] | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 6:7 | PRI_N0 | RW | R | 0 | Priority of interrupt number N. |
| 14:15 | PRI_N1 | RW | R | 0 | Priority of interrupt number N+1. |
| 22:23 | PRI_N2 | RW | R | 0 | Priority of interrupt number N+2. |
| 30:31 | PRI_N3 | RW | R | 0 | Priority of interrupt number N+3. |

### 3.8.3.10 CM0P_SCS_CPUID

**Description:** CPUID Register
**Address:** 0xE000ED00
**Offset:** 0xD00
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Contains the part number, version, and implementation information that is specific to this processor.
**Default:** 0x410CC601

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | PARTNO [7:4] | | | | REVISION [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | PARTNO [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VARIANT [23:20] | | | | CONSTANT [19:16] | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | IMPLEMENTER [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | REVISION | R | | 1 | Indicates revision. In ARM implementations this is the minor revision number n in the pn part of the rnpn revision status, see Product revision status on Arm TRM page xii. For release r0p1. |
| 4:15 | PARTNO | R | | 3168 | Indicates part number, Cortex-M0+ |
| 16:19 | CONSTANT | R | | 12 | Indicates the architecture, ARMv6-M |
| 20:23 | VARIANT | R | | 0 | Implementation defined. In ARM implementations this is the major revision number n in the rn part of the rnpn revision status, Product revision status on Arm TRM page xii. |
| 24:31 | IMPLEMENTER | R | | 65 | Implementer code for ARM. |

### 3.8.3.11 CM0P_SCS_ICSR

**Description:** Interrupt Control State Register
**Address:** 0xE000ED04
**Offset:** 0xD04
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Controls and provides status information for the ARMv6-M.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VECTACTIVE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VECTPENDING [15:12] | | | | None [11:9] | | | VECTACTIVE [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | ISRPREEMPT [23:23] | ISRPENDING [22:22] | None [21:21] | VECTPENDING [20:16] | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | NMIPENDSET [31:31] | None [30:29] | | PENDSVSET [28:28] | PENDSVCLR [27:27] | PENDSTSETB [26:26] | PENDSTCLR [25:25] | None [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:8 | VECTACTIVE | R | RW | 0 | The exception number for the current executing exception. 0= Thread mode. This is the same value as IPSR[8:0] |
| 12:20 | VECTPENDING | R | RW | 0 | The exception number for the highest priority pending exception. 0= No pending exceptions.<br>The pending state includes the effect of memory-mapped enable and mask registers. It does not include the PRIMASK special-purpose register qualifier. |
| 22 | ISRPENDING | R | RW | 0 | Indicates if an external configurable, NVIC generated, interrupt is pending. |
| 23 | ISRPREEMPT | R | RW | 0 | Indicates whether a pending exception will be serviced on exit from debug halt state. |
| 25 | PENDSTCLR | RW1C | R | 0 | Clears a pending SysTick, whether set here or by the timer hardware. |
| 26 | PENDSTSETB | RW1S | RW | 0 | Sets a pending SysTick or reads back the current state. Writing PENDSTSET and PENDSTCLR to '1' concurrently is UNPREDICTABLE. |
| 27 | PENDSVCLR | RW1C | R | 0 | Clears a pending PendSV interrupt. |
| 28 | PENDSVSET | RW1S | RW | 0 | Sets a pending PendSV interrupt or reads back the current state. Use this normally to request a context switch. Writing PENDSVSET and PENDSVCLR to '1' concurrently is UNPREDICTABLE. |
| 31 | NMIPENDSET | RW1S | RW | 0 | Activates an NMI exception or reads back the current state.<br>Because NMI is the highest priority exception, it activates as soon as it is registered. |

### 3.8.3.12 CM0P_SCS_VTOR

**Description:** Vector Table Offset Register
**Address:** 0xE000ED08
**Offset:** 0xD08
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Holds the vector table offset address
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | TBLOFF [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | TBLOFF [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | TBLOFF [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 8:31 | TBLOFF | RW | R | 0 | Table offset address.<br>All bits of the Vector table address that are not defined by the VTOR are zero. |

### 3.8.3.13 CM0P_SCS_AIRCR

**Description:** Application Interrupt and Reset Control Register
**Address:** 0xE000ED0C
**Offset:** 0xD0C
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Sets or returns interrupt control data.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:3] | | | | | SYSRESETREQ [2:2] | VECTCLRACTIVE [1:1] | None [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | ENDIANNESS [15:15] | None [14:8] | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VECTKEY [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VECTKEY [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 1 | VECTCLRACTIVE | RW1C | R | 0 | Clears all active state information for fixed and configurable<br>exceptions. The effect of writing a 1 to this bit if the processor is not halted in Debug state is UNPREDICTABLE. |
| 2 | SYSRESETREQ | RW1S | R | 0 | System Reset Request. Writing 1 to this bit asserts a signal to request a reset by the external system. This will cause a full system reset of the CPU and all other components in the device. See Reset management on Arm TRM page B1-240 for more information. |
| 15 | ENDIANNESS | R | | 0 | Indicates the memory system data endianness:<br>0 little endian<br>1 big endian.<br>See Endian support on Arm TRM page A3-44 for more information. |
| 16:31 | VECTKEY | RW | R | X | Vector Key. The value 0x05FA must be written to this register, otherwise the register write is not performed. |

### 3.8.3.14 CM0P_SCS_SCR

**Description:** System Control Register
**Address:** 0xE000ED10
**Offset:** 0xD10
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Sets or returns system control data.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:5] | | | SEVONPEND [4:4] | None [3:3] | SLEEPDEEP [2:2] | SLEEPONEXIT [1:1] | None [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 1 | SLEEPONEXIT | RW | R | 0 | Determines whether, on an exit from an ISR that returns to the base level of execution priority, the processor enters a sleep state:<br>0 do not enter sleep state.<br>1 enter sleep state.<br>See Power management on Arm TRM page B1-240 for more information. |
| 2 | SLEEPDEEP | RW | R | 0 | An implementation can use this bit to select DeepSleep power modes upon execution of WFI/WFE:<br>0: Select Sleep mode<br>1: Select DeepSleep |
| 4 | SEVONPEND | RW | R | 0 | Determines whether an interrupt transition from inactive state to pending state is a wakeup event:<br>0: transitions from inactive to pending are not wakeup events.<br>1: transitions from inactive to pending are wakeup events.<br>See WFE on page A6-197 for more information. |

### 3.8.3.15 CM0P_SCS_CCR

**Description:** Configuration and Control Register
**Address:** 0xE000ED14
**Offset:** 0xD14
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Returns configuration and control data.
**Default:** 0x208

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:4] | | | | UNALIGN_TRP [3:3] | None [2:0] | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:10] | | | | | | STKALIGN [9:9] | None [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 3 | UNALIGN_TRP | R | | 1 | 1: unaligned word and halfword accesses generate a HardFault exception. |
| 9 | STKALIGN | R | | 1 | 1: On exception entry, the SP used prior to the exception is adjusted to be 8-byte aligned and the context to restore it is saved. The SP is restored on the associated exception return. |

### 3.8.3.16 CM0P_SCS_SHPR2

**Description:** System Handler Priority Register 2
**Address:** 0xE000ED1C
**Offset:** 0xD1C
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Sets or returns priority for system handler 11
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | PRI_11 [31:30] | | None [29:24] | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 30:31 | PRI_11 | RW | R | 0 | Priority of system handler 11, SVCall |

### 3.8.3.17 CM0P_SCS_SHPR3

**Description:** System Handler Priority Register 3
**Address:** 0xE000ED20
**Offset:** 0xD20
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Sets or returns priority for system handlers 14-15.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | PRI_14 [23:22] | | None [21:16] | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | PRI_15 [31:30] | | None [29:24] | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 22:23 | PRI_14 | RW | R | 0 | Priority of system handler 14, PendSV |
| 30:31 | PRI_15 | RW | R | 0 | Priority of system handler 15, SysTick |

### 3.8.3.18 CM0P_SCS_SHCSR

**Description:** System Handler Control and State Register
**Address:** 0xE000ED24
**Offset:** 0xD24
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Controls and provides the status of system handlers.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | SVCALLPENDED [15:15] | None [14:8] | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 15 | SVCALLPENDED | RW | RW | 0 | 0 SVCall is not pending.<br>1 SVCall is pending.<br>This bit reflects the pending state on a read, and updates the pending state, to the value written, on a write. (Pending state bits are set to 1 when an exception occurs, and are cleared to 0 when an exception becomes active.) |

### 3.8.3.19 CM0P_SCS_DFSR

**Description:** Debug Fault Status Register
**Address:** 0xE000ED30
**Offset:** 0xD30
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Provides the top level reason why a debug event has occurred. Writing 1 to a register bit clears that bit to 0. A read of the HALTED bit by an instruction executed by stepping returns an UNKNOWN value, For more information see Debug stepping on Arm TRM page C1-325.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:5] | | | EXTERNAL [4:4] | VCATCH [3:3] | DWTTRAP [2:2] | BKPT [1:1] | HALTED [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | HALTED | RW1C | RW1S | 0 | Indicates a debug event generated by a C_HALT or C_STEP request, triggered by a write to the DHCSR:<br>0 no active halt request debug event.<br>1 halt request debug event active.<br>See Debug Halting Control and Status Register, DHCSR for more information. |
| 1 | BKPT | RW1C | RW1S | 0 | Indicates a debug event generated by BKPT instruction execution or a breakpoint match in the BPU:<br>0 no breakpoint debug event.<br>1 at least one breakpoint debug event. |
| 2 | DWTTRAP | RW1C | RW1S | 0 | Indicates a debug event generated by the DWT:<br>0 no debug events generated by the DWT.<br>1 at least one debug event generated by the DWT. |
| 3 | VCATCH | RW1C | RW1S | 0 | Indicates whether a vector catch debug event was generated:<br>0 no vector catch debug event generated.<br>1 vector catch debug event generated.<br>The corresponding FSR shows the primary cause of the exception. |
| 4 | EXTERNAL | RW1C | RW1S | 0 | Indicates an asynchronous debug event generated because of EDBGRQ being asserted:<br>0 no EDBGRQ debug event.<br>1 EDBGRQ debug event. |

### 3.8.3.20 CM0P_SCS_MPU_TYPE

**Description:** MPU Type Register
**Address:** 0xE000ED90
**Offset:** 0xD90
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** The MPU Type Register indicates how many regions the MPU supports. Software can use it to determine if the processor mplements an MPU
**Default:** 0x800

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:1] | | | | | | | SEPARATE [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | DREGION [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | IREGION [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | SEPARATE | R | R | 0 | Indicates support for separate instruction and data address maps. RAZ. ARMv6-M only supports a unified MPU. |
| 8:15 | DREGION | R | R | 8 | Number of regions supported by the MPU. If this field reads-as-zero the processor does not implement an MPU. |
| 16:23 | IREGION | R | R | 0 | Instruction region. RAZ. ARMv6-M only supports a unified MPU. |

### 3.8.3.21 CM0P_SCS_MPU_CTRL

**Description:** MPU Control Register
**Address:** 0xE000ED94
**Offset:** 0xD94
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Enables the MPU, and when the MPU is enabled, controls whether the default memory map is enabled as a background region for privileged accesses, and whether the MPU is enabled for HardFaults and NMIs.
If no regions are enabled and the PRIVDEFENA and ENABLE bits are set, only privileged code can execute from the system address map.
If the MPU is not implemented, this register is RAZ/WI.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:3] | | | | | PRIVDEFENA [2:2] | HFNMIENA [1:1] | ENABLE [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | ENABLE | RW | R | 0 | Enables the MPU:<br>0: The MPU is disabled. Privileged and unprivileged accesses use the<br>default memory map.<br>1: The MPU is enabled. |
| 1 | HFNMIENA | RW | R | 0 | The meaning of this bit is:<br>0: disables the MPU for HardFaults and NMIs.<br>1: when the ENABLE bit is set to 1, enables the MPU for HardFaults and NMIs.<br>Note: If HFNMIENA is set to 1 when ENABLE is set to 0, behavior is UNPREDICTABLE. |
| 2 | PRIVDEFENA | RW | R | 0 | When the ENABLE bit is set to 1, the meaning of this bit is:<br>0: Disables the default memory map. Any instruction or data access that does not access a defined region faults.<br>1: Enables the default memory map as a background region for privileged access. The system address map on Arm TRM page B3-258 describes the default memory map.<br>When the ENABLE bit is set to 0, the processor ignores the PRIVDEFENA bit. |

### 3.8.3.22 CM0P_SCS_MPU_RNR

**Description:** MPU Region Number Register
**Address:** 0xE000ED98
**Offset:** 0xD98
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Selects the region currently accessed by MPU_RBAR and MPU_RASR.
Used with MPU_RBAR and MPU_RASR, see MPU Region Base Address Register, MPU_RBAR, and MPU Region Attribute and Size Register, MPU_RASR.
If an implementation supports N regions then the regions number from 0 to (N-1), and the effect of writing a value of N or greater to the REGION field is UNPREDICTABLE.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | REGION_M [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | REGION_M | RW | R | X | Indicates the memory region accessed by MPU_RBAR and MPU_RSAR.<br>Normally, software must write the required region number to MPU_RNR to select the required memory region, before accessing MPU_RBAR or MPU_RSAR. However, the MPU_RBAR.VALID bit provides an alternative way of writing to MPU_RBAR to update a region base address without first writing the region number to MPU_RNR, see MPU Region Base Address Register, MPU_RBAR. |

### 3.8.3.23 CM0P_SCS_MPU_RBAR

**Description:** MPU Region Base Address Register
**Address:** 0xE000ED9C
**Offset:** 0xD9C
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Holds the base address of the region identified by MPU_RNR. On a write, can also be used to update the base address of a specified region, in the range 0 to 15, updating MPU_RNR with the new region number.
Normally, used with MPU_RBAR, see MPU Region Number Register, MPU_RNR.
If an implementation supports N regions then the regions number from 0 to (N-1). If N is less than 16 the effect of writing a value of N or greater to the REGION field is UNPREDICTABLE.
Software can find the minimum size of region supported by an MPU region by writing all ones to MPURBAR[31:5] for that region, and then reading the register to find the value saved to bits [31:5]. The number of trailing zeros in this bit field indicates the minimum supported alignment and therefore the supported region size. An implementation must support all region size values from the minimum supported to 4GB, see the description of the MPU_RASR.SIZE field in MPU Region Attribute and Size Register, MPU_RASR.
Software must ensure that the value written to the ADDR field aligns with the size of the selected region.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:5] | | | VALID [4:4] | REGION [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDR [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDR [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDR [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | REGION | RW | R | X | On writes, can specify the number of the region to update, see VALID field description.<br>On reads, returns bits [3:0] of MPU_RNR. |
| 4 | VALID | RW | R | X | On writes to the register, indicates whether the write must update the base address of the<br>region identified by the REGION field. updating the MPU_RNR to indicate this new region:<br>0 Update the base address of the region indicated by MPU_RNR, ignoring the<br>value of the REGION field.<br>1 Update the least-significant four bits of the MPU_RNR.REGION field with<br>MPU_RBAR.REGION field value, writing 0b0000 to bits [7:4] of the<br>MPU_RBAR.REGION field, and updating the base address of that region.<br>This bit reads as zero |
| 8:31 | ADDR | RW | R | X | Base address of the region. |

### 3.8.3.24 CM0P_SCS_MPU_RASR

**Description:** MPU Region Attribute and Size Register
**Address:** 0xE000EDA0
**Offset:** 0xDA0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Defines the size, access behavior, and memory type of the region identified by MPU_RNR, and enables that region.
Used with MPU_RBAR, see MPU Region Number Register, MPU_RNR on. Writing a SIZE value greater than the maximum size supported by the corresponding MPU_RBAR has an UNPREDICTABLE effect. The smallest supported region size is 256 bytes. This restricts the lowest possible value of SIZE.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:6] | | SIZE [5:1] | | | | | ENABLE [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | SRD [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | ATTRS [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | ATTRS [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | ENABLE | RW | R | X | Enables this region:<br>0: when the MPU is enabled, this region is disabled.<br>1: When the MPU is enabled, this region is enabled.<br>Enabling a region has no effect unless the MPU_CTRL.ENABLE bit is set to 1, to enable the MPU. |
| 1:5 | SIZE | RW | R | X | Indicates the region size.<br>The permitted values for SIZE are 7-31, that is 0b00111-0b11111. The associated region size, in bytes, is 2^(SIZE+1). SIZE field values less than 7 are reserved, because the smallest supported region size is 256 bytes. |
| 8:15 | SRD | RW | R | X | Subregion Disable. For regions of 256 bytes or larger, each bit of this field controls whether one of the eight equal subregions is enabled.<br>0: subregion enabled.<br>1: subregion disabled. |
| 16:31 | ATTRS | RW | R | X | The MPU Region Attribute field, This field has the following subfields, defined in Region attribute control on Arm TRM page B3-300 of the ARMv6M Architetcure manual (September 2010 version):<br>XN MPU_RASR[28]<br>AP[2:0] MPU_RASR[26:24]<br>TEX[2:0] MPU_RASR[21:19]<br>S MPU_RASR[18]<br>C MPU_RASR[17]<br>B MPU_RASR[16] |

### 3.8.3.25 CM0P_SCS_DHCSR

**Description:** Debug Halting Control and Status Register
**Address:** 0xE000EDF0
**Offset:** 0xDF0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Controls halting debug. When C_DEBUGEN is set to 1, C_STEP and C_MASKINTS must not be
modified when the processor is running. Note: S_HALT is 0 when the processor is running. When C_DEBUGEN is set to 0, the processor ignores the values of all other bits in this register. For more information on the use of DHCSR, see Debug stepping on Arm TRM page C1-325.
Note: any write to this register must have [31:16]=0xA05F - if not, the write is ignored.
**Default:** 0x2000000

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:4] | | | | C_MASKINTS [3:3] | C_STEP [2:2] | C_HALT [1:1] | C_DEBUGEN [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | DBG_KEY_P1 [23:20] | | | | S_LOCKUP [19:19] | S_SLEEP [18:18] | S_HALT [17:17] | S_REGRDY [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | DBG_KEY_P2 [31:26] | | | | | | S_RESET_ST [25:25] | S_RETIRE_ST [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | C_DEBUGEN | RW | R | 0 | Halting debug enable bit. If a debugger writes to DHCSR to change the value of this bit from 0 to 1, it must also write 0 to the C_MASKINTS bit, otherwise behavior is UNPREDICTABLE. This bit can only be written from the DAP. Access to the DHCSR from software running on the processor is IMPLEMENTATION DEFINED. However, writes to this bit from software running on the processor are ignored. |
| 1 | C_HALT | RW | R | X | Processor halt bit. The effects of writes to this bit are:<br>0 Request a halted processor to run.<br>1 Request a running processor to halt.<br>Table C1-7 on Arm TRM page C1-326 shows the effect of writes to this bit when the processor is in Debug state. |
| 2 | C_STEP | RW | R | X | Processor step bit. The effects of writes to this bit are:<br>0 Single-stepping disabled.<br>1 Single-stepping enabled.<br>For more information about the use of this bit see Table C1-7 on Arm TRM page C1-326. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 3 | C_MASKINTS | RW | R | X | When debug is enabled, the debugger can write to this bit to mask PendSV, SysTick and external configurable interrupts. The effect of any attempt to change the value of this bit is UNPREDICTABLE unless both:<br>- before the write to DHCSR, the value of the C_HALT bit is 1<br>- the write to the DHCSR that changes the C_MASKINTS bit also writes 1 to the C_HALT bit<br>This means that a single write to DHCSR cannot set the C_HALT to 0 and change the value of the C_MASKINTS bit. The bit does not affect NMI. When DHCSR.C_DEBUGEN is set to 0, the<br>value of this bit is UNKNOWN. For more information about the use of this bit see Table C1-7 on Arm TRM page C1-326. |
| 16 | S_REGRDY | R | RW | X | A handshake flag for transfers through the DCRDR:<br>- Writing to DCRSR clears the bit to 0.<br>- Completion of the DCRDR transfer then sets the bit to 1.<br>For more information about DCRDR transfers see Debug Core Register Data Register, DCRDR on Arm TRM page C1-337.<br>0: There has been a write to the DCRDR, but the transfer is<br>not complete.<br>1: The transfer to or from the DCRDR is complete.<br>This bit is only valid when the processor is in Debug state, otherwise the bit is UNKNOWN. |
| 17 | S_HALT | R | RW | 0 | Indicates whether the processor is in Debug state. |
| 18 | S_SLEEP | R | RW | 0 | Indicates whether the processor is sleeping. The debugger must set the DHCSR.C_HALT bit to 1 to gain control, or<br>wait for an interrupt or other wakeup event to wakeup the system. |
| 19 | S_LOCKUP | R | RW | 0 | Indicates whether the processor is locked up because of an unrecoverable exception. See Unrecoverable exception cases on Arm TRM page B1-238 for more information. This bit can only read as 1 when accessed by a remote debugger using the<br>DAP. The bit clears to 0 when the processor enters Debug state. |
| 20:23 | DBG_KEY_P1 | W | R | X | Debug key:<br>Software must write 0xA05F to [31:16] to enable write accesses to bits<br>[15:0], otherwise the processor ignores the write access. |
| 24 | S_RETIRE_ST | R | RW | X | When not in Debug state, indicates whether the processor has completed execution of at least one instruction since the last read of DHCSR. This is a sticky bit, that clears to 0 on a read of DHCSR.<br>This bit is UNKNOWN:<br>- after a Local reset, but is set to 1 as soon as the processor completes execution of an instruction<br>- when S_LOCKUP is set to 1<br>- when S_HALT is set to 1.<br>When the processor is not in Debug state, a debugger can check this bit to determine if the processor is stalled on a load, store or fetch access. |
| 25 | S_RESET_ST | R | RW | 1 | Indicates whether the processor has been reset since the last read of DHCSR. This is a sticky bit, that clears to 0 on a read of DHCSR |
| 26:31 | DBG_KEY_P2 | W | R | X | See desciption for Bit 20 |

### 3.8.3.26 CM0P_SCS_DCRSR

**Description:** Debug Core Register Selector Register
**Address:** 0xE000EDF4
**Offset:** 0xDF4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** With the DCRDR, see Debug Core Register Data Register, DCRDR on Arm TRM page C1-337, the DCRSR provides debug access to the ARM core registers and special-purpose registers. A write to DCRSR specifies the register to transfer, whether the transfer is a read or a write, and starts the transfer. This register is only accessible in Debug state. When the processor is in Debug state, the debugger must preserve the Exception number bits in the IPSR, otherwise behavior is UNPREDICTABLE
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:5] | | | REGSEL [4:0] | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:17] | | | | | | | REGWNR [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:4 | REGSEL | RW | R | X | Specifies the ARM core register or special-purpose register to transfer. |
| | R0 | | | 0 | CPU R0 |
| | R1 | | | 1 | CPU R1 |
| | R2 | | | 2 | CPU R2 |
| | R3 | | | 3 | CPU R3 |
| | R4 | | | 4 | CPU R4 |
| | R5 | | | 5 | CPU R5 |
| | R6 | | | 6 | CPU R6 |
| | R7 | | | 7 | CPU R7 |
| | R8 | | | 8 | CPU R8 |
| | R9 | | | 9 | CPU R9 |
| | R10 | | | 10 | CPU R10 |
| | R11 | | | 11 | CPU R11 |
| | R12 | | | 12 | CPU R12 |
| | SP | | | 13 | Current Stack Pointer |
| | LR | | | 14 | CPU LR |
| | DBG_RA | | | 15 | DebugReturnAddress: the address of the first instruction to be executed on exit from Debug state. |
| | XPSR | | | 16 | xPSR |
| | MSP | | | 17 | Main stack pointer, MSP. |
| | PSP | | | 18 | Process stack pointer, PSP |
| | C_P | | | 20 | [31:24]: CONTROL<br>[7:0]: PRIMASK. |
| 16 | REGWNR | RW | R | X | Specifies the type of access for the transfer. |
| | READ | | | 0 | Read transfer |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| | WRITE | | | 1 | Write transfer |

### 3.8.3.27 CM0P_SCS_DCRDR

**Description:** Debug Core Register Data Register
**Address:** 0xE000EDF8
**Offset:** 0xDF8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** With the DCRSR, see Debug Core Register Selector Register, DCRSR on Arm TRM page C1-335, the DCRDR provides debug access to the ARM core registers and special-purpose registers. The DCRDR is the data register for these accesses.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DBGTMP [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | DBGTMP [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | DBGTMP [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | DBGTMP [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | DBGTMP | RW | RW | X | Data temporary cache, for reading and writing CPU registers.<br>This register is UNKNOWN:<br>- on reset<br>- when DHCSR.S_HALT = 0.<br>- when DHCSR.S_REGRDY = 0 during execution of a DCRSR based transaction that updates the register |

### 3.8.3.28 CM0P_SCS_DEMCR

**Description:** Debug Exception and Monitor Control Register
**Address:** 0xE000EDFC
**Offset:** 0xDFC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Manages vector catch behavior and enables the DWT.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:1] | | | | | | | VC_CORERESET [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:11] | | | | | VC_HARDERR [10:10] | None [9:8] | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:25] | | | | | | | DWTENA [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | VC_CORERESET | RW | R | 0 | Enable Reset Vector Catch. This causes a Local reset to halt a running system. If DHCSR.C_DEBUGEN is set to 0, the processor ignores the value of this bit. |
| 10 | VC_HARDERR | RW | R | 0 | Enable halting debug trap on a HardFault exception. If DHCSR.C_DEBUGEN is set to 0, the processor ignores the value of this bit. |
| 24 | DWTENA | RW | R | 0 | Global enable for all features configured and controlled by the DWT unit. When DWTENA is set to 0 DWT registers return UNKNOWN values on reads. In addition, it is IMPLEMENTATION DEFINED whether the processor ignores writes to the DWT while DWTENA is 0. |

### 3.8.3.29 CM0P_SCS_SCS_PID4

**Description:** System Control Space ROM Table Peripheral ID #4
**Address:** 0xE000EFD0
**Offset:** 0xFD0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x4

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | | 4 | Peripheral ID #4 |

### 3.8.3.30 CM0P_SCS_SCS_PID0

**Description:** System Control Space ROM Table Peripheral ID #0
**Address:** 0xE000EFE0
**Offset:** 0xFE0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x8

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | | 8 | Peripheral ID #0 |

### 3.8.3.31 CM0P_SCS_SCS_PID1

**Description:** System Control Space ROM Table Peripheral ID #1
**Address:** 0xE000EFE4
**Offset:** 0xFE4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xB0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | | 176 | Peripheral ID #1 |

### 3.8.3.32 CM0P_SCS_SCS_PID2

**Description:** System Control Space ROM Table Peripheral ID #2
**Address:** 0xE000EFE8
**Offset:** 0xFE8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xB

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | | 11 | Peripheral ID #2 |

### 3.8.3.33 CM0P_SCS_SCS_PID3

**Description:** System Control Space ROM Table Peripheral ID #3
**Address:** 0xE000EFEC
**Offset:** 0xFEC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | | 0 | Peripheral ID #3 |

### 3.8.3.34 CM0P_SCS_SCS_CID0

**Description:** System Control Space ROM Table Component ID #0
**Address:** 0xE000EFF0
**Offset:** 0xFF0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xD

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | | 13 | Component ID #0 |

### 3.8.3.35 CM0P_SCS_SCS_CID1

**Description:** System Control Space ROM Table Component ID #1
**Address:** 0xE000EFF4
**Offset:** 0xFF4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xE0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | | 224 | Component ID #1 |

### 3.8.3.36 CM0P_SCS_SCS_CID2

**Description:** System Control Space ROM Table Component ID #2
**Address:** 0xE000EFF8
**Offset:** 0xFF8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x5

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | | 5 | Component ID #2 |

### 3.8.3.37 CM0P_SCS_SCS_CID3

**Description:** System Control Space ROM Table Component ID #3
**Address:** 0xE000EFFC
**Offset:** 0xFFC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xB1

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | | 177 | Component ID #3 |

### 3.8.4 ROM

#### 3.8.4.1 CM0P_ROM_ROM_SCS

**Description:** CM0+ CoreSight ROM Table Peripheral #0
**Address:** 0xE00FF000
**Offset:** 0x0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xFFF0F003

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | | 4293980163 | Offset to SCS ROM Table |

### 3.8.4.2 CM0P_ROM_ROM_DWT

**Description:** CM0+ CoreSight ROM Table Peripheral #1
**Address:** 0xE00FF004
**Offset:** 0x4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xFFF02003

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | | 4293926915 | Offset to DWT ROM Table |

### 3.8.4.3 CM0P_ROM_ROM_BPU

**Description:** CM0+ CoreSight ROM Table Peripheral #2
**Address:** 0xE00FF008
**Offset:** 0x8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xFFF03003

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | | 4293931011 | Offset to BPU ROM Table |

### 3.8.4.4 CM0P_ROM_ROM_END

**Description:** CM0+ CoreSight ROM Table End Marker
**Address:** 0xE00FF00C
**Offset:** 0xC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | | 0 | End marker in peripheral list |

### 3.8.4.5 CM0P_ROM_ROM_CSMT

**Description:** CM0+ CoreSight ROM Table Memory Type
**Address:** 0xE00FFFCC
**Offset:** 0xFCC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x1

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | | 1 | Memory Type |

### 3.8.4.6 CM0P_ROM_ROM_PID4

**Description:** CM0+ CoreSight ROM Table Peripheral ID #4
**Address:** 0xE00FFFD0
**Offset:** 0xFD0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x4

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | | 4 | Peripheral ID #4 |

### 3.8.4.7 CM0P_ROM_ROM_PID0

**Description:** CM0+ CoreSight ROM Table Peripheral ID #0
**Address:** 0xE00FFFE0
**Offset:** 0xFE0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xC0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | | 192 | Peripheral ID #0 |

### 3.8.4.8 CM0P_ROM_ROM_PID1

**Description:** CM0+ CoreSight ROM Table Peripheral ID #1
**Address:** 0xE00FFFE4
**Offset:** 0xFE4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xB4

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | | 180 | Peripheral ID #1 |

### 3.8.4.9 CM0P_ROM_ROM_PID2

**Description:** CM0+ CoreSight ROM Table Peripheral ID #2
**Address:** 0xE00FFFE8
**Offset:** 0xFE8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xB

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | | 11 | Peripheral ID #2 |

### 3.8.4.10 CM0P_ROM_ROM_PID3

**Description:** CM0+ CoreSight ROM Table Peripheral ID #3
**Address:** 0xE00FFFEC
**Offset:** 0xFEC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | | 0 | Peripheral ID #3 |

### 3.8.4.11 CM0P_ROM_ROM_CID0

**Description:** CM0+ CoreSight ROM Table Component ID #0
**Address:** 0xE00FFFF0
**Offset:** 0xFF0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xD

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | | 13 | Component ID #0 |

### 3.8.4.12 CM0P_ROM_ROM_CID1

**Description:** CM0+ CoreSight ROM Table Component ID #1
**Address:** 0xE00FFFF4
**Offset:** 0xFF4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x10

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | | 16 | Component ID #1 |

### 3.8.4.13 CM0P_ROM_ROM_CID2

**Description:** CM0+ CoreSight ROM Table Component ID #2
**Address:** 0xE00FFFF8
**Offset:** 0xFF8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x5

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | | 5 | Component ID #2 |

### 3.8.4.14 CM0P_ROM_ROM_CID3

**Description:** CM0+ CoreSight ROM Table Component ID #3
**Address:** 0xE00FFFFC
**Offset:** 0xFFC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xB1

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | | 177 | Component ID #3 |

### 3.8.5 ROMTABLE

#### 3.8.5.1 CM0P_ROMTABLE_ADDR0

**Description:** Link to Cortex M0+ ROM Table.
**Address:** 0xF0000000
**Offset:** 0x0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xF00FF003

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:2] | | | | | | FORMAT_32BIT [1:1] | PRESENT [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDR_OFFSET [15:12] | | | | None [11:8] | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDR_OFFSET [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDR_OFFSET [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | PRESENT | R | R | 1 | Entry present. |
| 1 | FORMAT_32BIT | R | R | 1 | ROM Table format:<br>'0: 8-bit format.<br>'1': 32-bit format. |
| 12:31 | ADDR_OFFSET | R | R | 983295 | Address offset of the Cortex-M0 ROM Table base address (0xe00f:f000) wrt. Cypress chip specific ROM Table base address (0xf000:0000).<br>ADDR_OFFSET[19:0] = 0xe00f:f - 0xf000:0 = 0xf00f:f. |

### 3.8.5.2 CM0P_ROMTABLE_ADDR1

**Description:** Link to CoreSight CTI Table.
**Address:** 0xF0000004
**Offset:** 0x4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x2003

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:2] | | | | | | FORMAT_32BIT [1:1] | PRESENT [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDR_OFFSET [15:12] | | | | None [11:8] | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDR_OFFSET [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDR_OFFSET [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | PRESENT | R | R | 1 | Entry present. |
| 1 | FORMAT_32BIT | R | R | 1 | ROM Table format:<br>'0: 8-bit format.<br>'1': 32-bit format. |
| 12:31 | ADDR_OFFSET | R | R | 2 | Address offset of the Cortex-M0 ROM Table base address (0xe00f:f000) wrt. Cypress chip specific ROM Table base address (0xf000:0000).<br>ADDR_OFFSET[19:0] = 0xe00f:f - 0xf000:0 = 0xf00f:f. |

### 3.8.5.3 CM0P_ROMTABLE_ADDR2

**Description:** Link to Cortex M0+ MTB Table.
**Address:** 0xF0000008
**Offset:** 0x8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x3003

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:2] | | | | | | FORMAT_32BIT [1:1] | PRESENT [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDR_OFFSET [15:12] | | | | None [11:8] | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDR_OFFSET [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDR_OFFSET [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | PRESENT | R | R | 1 | Entry present. |
| 1 | FORMAT_32BIT | R | R | 1 | ROM Table format:<br>'0: 8-bit format.<br>'1': 32-bit format. |
| 12:31 | ADDR_OFFSET | R | R | 3 | Address offset of the Cortex-M0 ROM Table base address (0xe00f:f000) wrt. Cypress chip specific ROM Table base address (0xf000:0000).<br>ADDR_OFFSET[19:0] = 0xe00f:f - 0xf000:0 = 0xf00f:f. |

### 3.8.5.4 CM0P_ROMTABLE_DID

**Description:** Device Type Identifier register.
**Address:** 0xF0000FCC
**Offset:** 0xFCC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x1

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 1 | . |

### 3.8.5.5 CM0P_ROMTABLE_PID4

**Description:** Peripheral Identification Register 4.
**Address:** 0xF0000FD0
**Offset:** 0xFD0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** Undefined as one or more bit fields have a default value that is undefined

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT [7:4] | | | | JEP_CONTINUATION [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | JEP_CONTINUATION | R | R | Undefined | JEP106 continuation code. This value is product specific and specified as part of the product definition in the CPUSS.JEPCONTINUATION parameter. |
| 4:7 | COUNT | R | R | 0 | Size of ROM Table is 2^COUNT * 4 KByte. |

### 3.8.5.6 CM0P_ROMTABLE_PID5

**Description:** Peripheral Identification Register 5.
**Address:** 0xF0000FD4
**Offset:** 0xFD4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 0 | . |

### 3.8.5.7 CM0P_ROMTABLE_PID6

**Description:** Peripheral Identification Register 6.
**Address:** 0xF0000FD8
**Offset:** 0xFD8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 0 | . |

### 3.8.5.8 CM0P_ROMTABLE_PID7

**Description:** Peripheral Identification Register 7.
**Address:** 0xF0000FDC
**Offset:** 0xFDC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 0 | . |

### 3.8.5.9 CM0P_ROMTABLE_PID0

**Description:** Peripheral Identification Register 0.
**Address:** 0xF0000FE0
**Offset:** 0xFE0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** Undefined as one or more bit fields have a default value that is undefined

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | PN_MIN [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | PN_MIN | R | R | Undefined | JEP106 part number. 4 lsbs of CPUSS.PARTNUMBER parameter. |

### 3.8.5.10 CM0P_ROMTABLE_PID1

**Description:** Peripheral Identification Register 1.
**Address:** 0xF0000FE4
**Offset:** 0xFE4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** Undefined as one or more bit fields have a default value that is undefined

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | JEPID_MIN [7:4] | | | | PN_MAJ [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | PN_MAJ | R | R | Undefined | JEP106 part number. 4 msbs of CPUSS.PARTNUMBER parameter. |
| 4:7 | JEPID_MIN | R | R | Undefined | JEP106 vendor id. 4 lsbs of CPUSS.JEPID parameter. |

### 3.8.5.11 CM0P_ROMTABLE_PID2

**Description:** Peripheral Identification Register 2.
**Address:** 0xF0000FE8
**Offset:** 0xFE8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** Undefined as one or more bit fields have a default value that is undefined

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | REV [7:4] | | | | None [3:3] | JEPID_MAJ [2:0] | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:2 | JEPID_MAJ | R | R | Undefined | JEP106 vendor id. 4 msbs of CPUSS.JEPID parameter. |
| 4:7 | REV | R | R | Undefined | Major REVision number (chip specific). Identifies the design iteration of the component. For first tape out: 0x1. This field is incremented on subsequent tape outs. |

### 3.8.5.12 CM0P_ROMTABLE_PID3

**Description:** Peripheral Identification Register 3.
**Address:** 0xF0000FEC
**Offset:** 0xFEC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** Undefined as one or more bit fields have a default value that is undefined

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | REV_AND [7:4] | | | | CM [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | CM | R | R | 0 | N/A |
| 4:7 | REV_AND | R | R | Undefined | Minor REVision number (chip specific). For first tape out: 0x1. This field is is incremented on subsequent tape outs. |

### 3.8.5.13 CM0P_ROMTABLE_CID0

**Description:** Component Identification Register 0.
**Address:** 0xF0000FF0
**Offset:** 0xFF0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xD

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 13 | Component identification byte 0 of 4-byte component identification 0xB105:100D. |

### 3.8.5.14 CM0P_ROMTABLE_CID1

**Description:** Component Identification Register 1.
**Address:** 0xF0000FF4
**Offset:** 0xFF4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x10

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 16 | Component identification byte 1 of 4-byte component identification 0xB105:100D. Component class: 'ROM Table'. |

### 3.8.5.15 CM0P_ROMTABLE_CID2

**Description:** Component Identification Register 2.
**Address:** 0xF0000FF8
**Offset:** 0xFF8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x5

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 5 | Component identification byte 2 of 4-byte component identification 0xB105:100D. |

### 3.8.5.16 CM0P_ROMTABLE_CID3

**Description:** Component Identification Register 3.
**Address:** 0xF0000FFC
**Offset:** 0xFFC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xB1

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 177 | Component identification byte 3 of 4-byte component identification 0xB105:100D. |

### 3.8.6 CTI

#### 3.8.6.1 CM0P_CTI_CTICONTROL

**Description:** CTI Control Register
**Address:** 0xF0002000
**Offset:** 0x0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** The CTI Control Register enables the CTI.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:1] | | | | | | | GLBEN [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | GLBEN | RW | R | 0 | Enables or disables the ECT:<br>0 = disabled (reset)<br>1 = enabled.<br>When disabled, all cross triggering mapping logic functionality is disabled for this processor. |

### 3.8.6.2 CM0P_CTI_CTIINTACK

**Description:** CTI Interrupt Acknowledge Register
**Address:** 0xF0002010
**Offset:** 0x10
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** The CTI Interrupt Acknowledge Register is write-only. Any bits written as a 1 cause the CTITRIGOUT output signal to be acknowledged. The acknowledgement is cleared when MAPTRIGOUT is deactivated. This register is used when the CTITRIGOUT is used as a sticky output, that is, no hardware acknowledge is supplied, and a software acknowledge is required.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | INTACK [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | INTACK | W | R | 0 | Acknowledges the corresponding CTITRIGOUT output:<br>1 = CTITRIGOUT is acknowledged and is cleared when MAPTRIGOUT is LOW. 0 = no effect.<br>There is one bit of the register for each CTITRIGOUT output. |

### 3.8.6.3 CM0P_CTI_CTIAPPSET

**Description:** CTI Application Trigger Set Register
**Address:** 0xF0002014
**Offset:** 0x14
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** The CTI Application Trigger Set Register is read/write. A write to this register causes a channel event to be raised, corresponding to the bit written to.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:4] | | | | APPSET [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | APPSET | RW | R | 0 | Setting a bit HIGH generates a channel event for the selected channel. Read:<br>0 = application trigger inactive (reset)<br>1 = application trigger active.<br>Write:<br>0 = no effect<br>1 = generate channel event.<br>There is one bit of the register for each channel. |

### 3.8.6.4 CM0P_CTI_CTIAPPCLEAR

**Description:** CTI Application Trigger Clear Register
**Address:** 0xF0002018
**Offset:** 0x18
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** The CTI Application Trigger Clear Register is write-only. A write to this register causes a channel event to be cleared, corresponding to the bit written to.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:4] | | | | APPCLEAR [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | APPCLEAR | W | R | 0 | Clears corresponding bits in the CTIAPPSET register. 1 = application trigger disabled in the CTIAPPSET register 0 = no effect. There is one bit of the register for each channel. |

### 3.8.6.5 CM0P_CTI_CTIAPPPULSE

**Description:** CTI Application Pulse Register
**Address:** 0xF000201C
**Offset:** 0x1C
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** The CTI Application Pulse Register is write-only. A write to this register causes a channel event pulse, one CTICLK period, to be generated, corresponding to the bit written to. The pulse external to the ECT can be extended to multi-cycle by the handshaking interface circuits. This register clears itself immediately, so it can be repeatedly written to without software having to clear it.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:4] | | | | APPULSE [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | APPULSE | W | R | 0 | Setting a bit HIGH generates a channel event pulse for the selected channel. Write:<br>1 = channel event pulse generated for one CTICLK period 0 = no effect.<br>There is one bit of the register for each channel. |

### 3.8.6.6 CM0P_CTI_CTIINEN

**Description:** CTI Trigger to Channel Enable Registers
**Address:** 0xF0002020
**Offset:** 0x20
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** The CTI Trigger to Channel Enable Registers enable the signalling of an event on CTM channels when the core issues a trigger, CTITRIGIN, to the CTI. There is one register for each of the eight CTITRIGIN inputs. Within each register there is one bit for each of the four channels implemented. These registers do not affect the application trigger operations.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:4] | | | | TRIGINEN [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | TRIGINEN | RW | R | 0 | Enables a cross trigger event to the corresponding channel when an CTITRIGIN is activated.<br>1 = enables the CTITRIGIN signal to generate an event on the respective channel of the CTM.<br>There is one bit of the register for each of the four channels. For example in register CTIINEN0, TRIGINEN[0] set to 1 enables CTITRIGIN onto channel 0.<br>0 = disables the CTITRIGIN signal from generating an event on the respective channel of the CTM. |

### 3.8.6.7 CM0P_CTI_CTIOUTEN

**Description:** CTI Channel to Trigger Enable Registers
**Address:** 0xF00020A0
**Offset:** 0xA0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** The CTI Channel to Trigger Enable Registers define which channels can generate a CTITRIGOUT output. There is one register for each of the eight CTITRIGOUT outputs. Within each register there is one bit for each of the four channels implemented. These registers affect the mapping from application trigger to trigger outputs.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:4] | | | | TRIGOUTEN [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | TRIGOUTEN | RW | R | 0 | Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate an CTITRIGOUT output:<br>0 = the channel input (CTICHIN) from the CTM is not routed to the CTITRIGOUT output 1 = the channel input (CTICHIN) from the CTM is routed to the CTITRIGOUT output. There is one bit for each of the four channels. For example in register CTIOUTEN0, enabling bit 0 enables CTICHIN[0] to cause a trigger event on the CTITRIGOUT[0] output. |

### 3.8.6.8 CM0P_CTI_CTITRIGINSTATUS

**Description:** CTI Trigger In Status Register
**Address:** 0xF0002130
**Offset:** 0x130
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** The CTI Trigger In Status Register provides the status of the CTITRIGIN inputs.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | TRIGINSTATUS [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | TRIGINSTATUS | R | RW | 0 | Shows the status of the CTITRIGIN inputs:<br>1 = CTITRIGIN is active<br>0 = CTITRIGIN is inactive.<br>Because the register provides a view of the raw CTITRIGIN inputs, the reset value is unknown. There is one bit of the register for each trigger input. |

### 3.8.6.9 CM0P_CTI_CTITRIGOUTSTATUS

**Description:** CTI Trigger Out Status Register
**Address:** 0xF0002134
**Offset:** 0x134
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** The CTI Trigger Out Status Register provides the status of the CTITRIGOUT outputs.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | TRIGOUTSTATUS [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | TRIGOUTSTATUS | R | RW | 0 | Shows the status of the CTITRIGOUT outputs.<br>1 = CTITRIGOUT is active<br>0 = CTITRIGOUT is inactive (reset).<br>There is one bit of the register for each trigger output. |

### 3.8.6.10 CM0P_CTI_CTICHINSTATUS

**Description:** CTI Channel In Status Register
**Address:** 0xF0002138
**Offset:** 0x138
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** The CTI Channel In Status Register provides the status of the CTI CTICHIN inputs.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:4] | | | | CTICHINSTATUS [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | CTICHINSTATUS | R | RW | 0 | Shows the status of the CTICHIN inputs:<br>1 = CTICHIN is active<br>0 = CTICHIN is inactive.<br>Because the register provides a view of the raw CTICHIN inputs from the CTM, the reset value is unknown. There is one bit of the register for each channel input. |

### 3.8.6.11 CM0P_CTI_CTICHOUTSTATUS

**Description:** CTI Channel Out Status Register
**Address:** 0xF000213C
**Offset:** 0x13C
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** The CTI Channel Out Status Register provides the status of the CTI CTICHOUT outputs.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:4] | | | | CTICHOUTSTATUS [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | CTICHOUTSTATUS | R | RW | 0 | Shows the status of the CTICHOUT outputs.<br>1 = CTICHOUT is active<br>0 = CTICHOUT is inactive (reset).<br>There is one bit of the register for each channel output. |

### 3.8.6.12 CM0P_CTI_CTIGATE

**Description:** Enable CTI Channel Gate Register
**Address:** 0xF0002140
**Offset:** 0x140
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** The Gate Enable Register prevents the channels from propagating through the CTM to other CTIs. This enables local cross-triggering, for example for causing an interrupt when the ETM trigger occurs. It can be used effectively with CTIAPPSET, CTIAPPCLEAR, and CTIAPPPULSE for asserting trigger outputs by asserting channels, without affecting the rest of the system. On reset, this register is 0xF, and channel propagation is enabled.
**Default:** 0xF

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:4] | | | | CTIGATEEN 3 [3:3] | CTIGATEEN 2 [2:2] | CTIGATEEN 1 [1:1] | CTIGATEEN 0 [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | CTIGATEEN0 | RW | R | 1 | Enable CTICHOUT0. Set to 0 to disable channel propagation. |
| 1 | CTIGATEEN1 | RW | R | 1 | Enable CTICHOUT1. Set to 0 to disable channel propagation. |
| 2 | CTIGATEEN2 | RW | R | 1 | Enable CTICHOUT2. Set to 0 to disable channel propagation. |
| 3 | CTIGATEEN3 | RW | R | 1 | Enable CTICHOUT3. Set to 0 to disable channel propagation. |

### 3.8.6.13 CM0P_CTI_ASICCTL

**Description:** External Multiplexor Control Register
**Address:** 0xF0002144
**Offset:** 0x144
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | ASICCTL [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | ASICCTL | RW | R | 0 | Implementation-defined ASIC control, value written to the register is output on ASICCTL[7:0].<br>If external multiplexing of trigger signals is implemented then the number of multiplexed signals on each trigger must be reflected within the Device ID Register. This is done within a Verilog define EXTMUXNUM. See ECT CoreSight defined registers on Arm TRM page 4-28. |

### 3.8.6.14 CM0P_CTI_ITCHINACK

**Description:** ITCHINACK Register
**Address:** 0xF0002EDC
**Offset:** 0xEDC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register is a write-only register.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:4] | | | | CTCHINACK [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | CTCHINACK | W | R | 0 | Set the value of the CTCHINACK outputs |

### 3.8.6.15 CM0P_CTI_ITTRIGINACK

**Description:** ITTRIGINACK Register
**Address:** 0xF0002EE0
**Offset:** 0xEE0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register is a write-only register.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | CTTRIGINACK [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | CTTRIGINACK | W | R | 0 | Set the value of the CTTRIGINACK outputs |

### 3.8.6.16 CM0P_CTI_ITCHOUT

**Description:** ITCHOUT Register
**Address:** 0xF0002EE4
**Offset:** 0xEE4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register is a write-only register.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:4] | | | | CTCHOUT [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | CTCHOUT | W | R | 0 | Set the value of the CTCHOUT outputs |

### 3.8.6.17 CM0P_CTI_ITTRIGOUT

**Description:** ITTRIGOUT Register
**Address:** 0xF0002EE8
**Offset:** 0xEE8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register is a write-only register.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | CTTRIGOUT [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | CTTRIGOUT | W | R | 0 | Set the value of the CTTRIGOUT outputs |

### 3.8.6.18 CM0P_CTI_ITCHOUTACK

**Description:** ITCHOUTACK Register
**Address:** 0xF0002EEC
**Offset:** 0xEEC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register is a read-only register.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:4] | | | | CTCHOUTACK [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | CTCHOUTACK | R | W | 0 | Read the values of the CTCHOUTACK inputs |

### 3.8.6.19 CM0P_CTI_ITTRIGOUTACK

**Description:** ITTRIGOUTACK Register
**Address:** 0xF0002EF0
**Offset:** 0xEF0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register is a read-only register.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | CTTRIGOUTACK [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | CTTRIGOUTACK | R | W | 0 | Read the values of the CTTRIGOUTACK inputs |

### 3.8.6.20 CM0P_CTI_ITCHIN

**Description:** ITCHIN Register
**Address:** 0xF0002EF4
**Offset:** 0xEF4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register is a read-only register.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:4] | | | | CTCHIN [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | CTCHIN | R | W | 0 | Read the values of the CTCHIN inputs |

### 3.8.6.21 CM0P_CTI_ITTRIGIN

**Description:** ITTRIGIN Register
**Address:** 0xF0002EF8
**Offset:** 0xEF8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register is a read-only register.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | CTTRIGIN [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | CTTRIGIN | R | W | 0 | Read the values of the CTTRIGIN inputs |

### 3.8.6.22 CM0P_CTI_ITCTRL

**Description:** Integration Mode Control Register
**Address:** 0xF0002F00
**Offset:** 0xF00
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register enables the component to switch from a functional mode, the default behavior, to integration mode where the inputs and outputs of the component can be directly controlled for the purpose of integration testing and topology solving.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:1] | | | | | | | MODE [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | MODE | RW | R | 0 | When set, the component enters integration mode, enabling topology detection or integration testing to be performed. At reset the component must enter functional mode. If no integration functionality is implemented, this register must read as zero. |

### 3.8.6.23 CM0P_CTI_CLAIMSET

**Description:** Claim Tag Set Register
**Address:** 0xF0002FA0
**Offset:** 0xFA0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register forms one half of the Claim Tag value. This location allows individual bits to be set, write, and returns the number of bits that can be set, read.
You can determine how many claim bits are implemented by reading this register. For example, if 4 bits are implemented, a read of this register will return 0x0000000F. If no claim tag is implemented, then a read of this register will return 0x00000000.
**Default:** 0xF

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:4] | | | | TAG [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | TAG | RW1S | R | 15 | A bit programmable register bank which sets the Claim Tag Value. A read will return a logic 1 for all implemented locations. |

### 3.8.6.24 CM0P_CTI_CLAIMCLR

**Description:** Claim Tag Clear Register
**Address:** 0xF0002FA4
**Offset:** 0xFA4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register forms one half of the Claim Tag value. This location enables individual bits to be cleared, write, and returns the current Claim Tag value, read. The width (n) of this register can be determined from reading the Claim Tag Set Register.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:4] | | | | TAG [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | TAG | RW1C | R | 0 | A bit programmable register bank that is zero at reset. |

### 3.8.6.25 CM0P_CTI_LOCKACCESS

**Description:** Lock Access Register
**Address:** 0xF0002FB0
**Offset:** 0xFB0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This is used to enable write access to device registers. If LOCKSTATUS[0] == 0x0 then this register is not present.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:4] | | | | ACCESS_CODE [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | ACCESS_CODE | RW | R | 0 | Write Access Code. A write of 0xC5ACCE55 enables further write access to this device. An invalid write will have the affect of removing write access.<br>If LOCKSTATUS[2] is set, then only bits [7:0] of this register are implemented and lock access is obtained by consecutively writing 0xC5, 0xAC, 0xCE, 0x55. Bits [31:8] are unused and any writes to them ignored. |

### 3.8.6.26 CM0P_CTI_LOCKSTATUS

**Description:** Lock Status Register
**Address:** 0xF0002FB4
**Offset:** 0xFB4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This indicates the status of the Lock control mechanism. This lock prevents accidental writes by code under debug.
This register must always be present although there might not be any lock-access control mechanism. The lock mechanism, where present and locked, must block write accesses to any control register, except the Lock Access Register. For most components this covers all registers except for the Lock Access Register 0xFB0.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:3] | | | | | IMPLEMENTS_8B [2:2] | ACCESS_PERMITTED [1:1] | EXISTS [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | EXISTS | R | W | 0 | Indicates that a lock control mechanism exists for this device |
| 1 | ACCESS_PERMITTED | R | W | 0 | The values of this bit mean:<br>0 = Access permitted.<br>1 = Write access to the component is blocked. All writes to control registers are ignored. Reads are permitted |
| 2 | IMPLEMENTS_8B | R | W | 0 | This component implements an 8-bit Lock Access Register. |

### 3.8.6.27 CM0P_CTI_AUTHSTATUS

**Description:** Authentication Status Register
**Address:** 0xF0002FB8
**Offset:** 0xFB8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Reports the required security level and current status of those enables. Where functionality changes on a given security level then this change in status must be reported in this register
**Default:** 0x5

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | SNIDBG [7:6] | | SIDBG [5:4] | | NSNIDBG [3:2] | | NSIDBG [1:0] | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:1 | NSIDBG | R | W | 1 | Non-Secure Invasive Debug<br>0: Functionality not implemented or controlled elsewhere<br>1: Functionality disabled<br>2: Reserved<br>3: Functionality enabled |
| 2:3 | NSNIDBG | R | W | 1 | Non-Secure Non-Invasive Debug<br>0: Functionality not implemented or controlled elsewhere<br>1: Functionality disabled<br>2: Reserved<br>3: Functionality enabled |
| 4:5 | SIDBG | R | W | 0 | Secure Invasive Debug<br>0: Functionality not implemented or controlled elsewhere<br>1: Functionality disabled<br>2: Reserved<br>3: Functionality enabled |
| 6:7 | SNIDBG | R | W | 0 | Secure Non-Invasive Debug<br>0: Functionality not implemented or controlled elsewhere<br>1: Functionality disabled<br>2: Reserved<br>3: Functionality enabled |

### 3.8.6.28 CM0P_CTI_DEVID

**Description:** Device Configuration Register
**Address:** 0xF0002FC8
**Offset:** 0xFC8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register is implementation-defined for each Part Number and Designer. This indicates the capabilities of the component. The entire 32-bit field can be used because the data width is determined by the particular component. Unused bits must read as zero.
If the component is configurable then it is recommended that this register reflects any changes to a standard configuration.
**Default:** 0x40804

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:5] | | | NRMUXING [4:0] | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | NRTRIG [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:20] | | | | NRCHAN [19:16] | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:4 | NRMUXING | R | R | 4 | Indicates the number of multiplexing available on Trigger Inputs and Trigger Outputs using ASICCTL. Default value of 5'b00000 indicating no multiplexing present. Reflects the value of the Verilog `define EXTMUXNUM that you must alter accordingly. |
| 8:15 | NRTRIG | R | R | 8 | Number of ECT triggers available. |
| 16:19 | NRCHAN | R | R | 4 | Number of ECT channels available. |

### 3.8.6.29 CM0P_CTI_DEVTYPE

**Description:** Device Type Identifier Register
**Address:** 0xF0002FCC
**Offset:** 0xFCC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** 0x14 indicates this device has a major type of debug control logic component (0x4) and sub-type corresponding to cross trigger (0x1).
**Default:** 0x14

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | SUB_TYPE [7:4] | | | | CLASS [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | CLASS | R | R | 4 | debug control logic component |
| 4:7 | SUB_TYPE | R | R | 1 | cross trigger |

### 3.8.6.30 CM0P_CTI_PID4

**Description:** Peripheral Identification Register 4
**Address:** 0xF0002FD0
**Offset:** 0xFD0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x4

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 4 | N/A |

### 3.8.6.31 CM0P_CTI_PID5

**Description:** Peripheral Identification Register 5
**Address:** 0xF0002FD4
**Offset:** 0xFD4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 0 | N/A |

### 3.8.6.32 CM0P_CTI_PID6

**Description:** Peripheral Identification Register 6
**Address:** 0xF0002FD8
**Offset:** 0xFD8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 0 | N/A |

### 3.8.6.33 CM0P_CTI_PID7

**Description:** Peripheral Identification Register 7
**Address:** 0xF0002FDC
**Offset:** 0xFDC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 0 | N/A |

### 3.8.6.34 CM0P_CTI_PID0

**Description:** Peripheral Identification Register 0
**Address:** 0xF0002FE0
**Offset:** 0xFE0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x6

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 6 | N/A |

### 3.8.6.35 CM0P_CTI_PID1

**Description:** Peripheral Identification Register 1
**Address:** 0xF0002FE4
**Offset:** 0xFE4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xB9

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 185 | N/A |

### 3.8.6.36 CM0P_CTI_PID2

**Description:** Peripheral Identification Register 2
**Address:** 0xF0002FE8
**Offset:** 0xFE8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x2B

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 43 | N/A |

### 3.8.6.37 CM0P_CTI_PID3

**Description:** Peripheral Identification Register 3
**Address:** 0xF0002FEC
**Offset:** 0xFEC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | ECOREVNUM [7:4] | | | | None [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 4:7 | ECOREVNUM | R | R | 0 | ECO revision for MTB |

### 3.8.6.38 CM0P_CTI_CID0

**Description:** Component Identification Register 0
**Address:** 0xF0002FF0
**Offset:** 0xFF0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xD

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 13 | N/A |

### 3.8.6.39 CM0P_CTI_CID1

**Description:** Component Identification Register 1
**Address:** 0xF0002FF4
**Offset:** 0xFF4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x90

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 144 | N/A |

### 3.8.6.40 CM0P_CTI_CID2

**Description:** Component Identification Register 2
**Address:** 0xF0002FF8
**Offset:** 0xFF8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x5

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 5 | N/A |

### 3.8.6.41 CM0P_CTI_CID3

**Description:** Component Identification Register 3
**Address:** 0xF0002FFC
**Offset:** 0xFFC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xB1

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 177 | N/A |

### 3.8.7 MTB

#### 3.8.7.1 CM0P_MTB_POSITION

**Description:** POSITION register
**Address:** 0xF0003000
**Offset:** 0x0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Contains the trace write pointer and the wrap bit. Available in all MTB configurations. You can modify all fields by software. Automatic hardware mechanisms update all fields. A debug agent might use the WRAP bit to determine whether the trace information above and below the pointer address is valid.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | POINTER [7:3] | | | | | WRAP [2:2] | None [1:0] | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | POINTER [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | POINTER [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | POINTER [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 2 | WRAP | RW | RW | X | This bit is set to 1 automatically when the POINTER value wraps as determined by the MASTER.MASK field in the MASTER Trace Control Register. |
| 3:31 | POINTER | RW | RW | X | Trace packet location pointer. Because a packet consists of two words, the POINTER field is the location of the first word of a packet. This field contains bits [31:3] of the address, in the SRAM, where the next trace packet will be written. The field points to an unused location and is automatically incremented.<br><br>A debug agent can calculate the system address, on the AHB-Lite bus, of the SRAM location pointed to by the POSITION register using the following equation:<br><br>system address = BASE + ((P + (2^AWIDTH - (BASE MOD 2^AWIDTH))) MOD 2^AWIDTH).<br><br>Where P = POSITION AND 0xFFFF_FFF8.<br>Where BASE is the BASE register value.<br><br>Note:<br>- The size of the SRAM is parameterized and the most significant bits of the POINTER field can be RAZ/WI, depending on the AWIDTH parameter value.<br>- POSITION register bits greater than or equal to AWIDTH are RAZ/WI, therefore, the active POINTER field bits are [AWIDTH-4:0].<br>- The POINTER field value is relative to the base address of the SRAM in the system memory map. |

### 3.8.7.2 CM0P_MTB_MASTER

**Description:** MASTER register
**Address:** 0xF0003004
**Offset:** 0x4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Contains:
- The main trace enable bit.
- Other trace control fields.

Usage constraints - Before the MASTER.EN or MASTER.TSTARTEN bits are set to 1, software must initialize the POSITION and FLOW registers.
- If the FLOW.WATERMARK field is used to stop tracing or to halt the processor, the MASTER.MASK field must still be set to a value that prevents the POSITION.POINTER field from wrapping before it reaches the FLOW.WATERMARK value.
- The EDBGRQ output value is also affected by the Debug authentication interface.

Configurations: Available in all MTB configurations.
Attributes:
- You can modify all fields by software.
- Automatic hardware mechanisms update the EN and HALTREQ bits.

Following example MASK and POINTER values to illustrate the effect of the MASK field on the POINTER.

MASK POINTER POINTER + 1 POINTER next
0x0 0x1 0x2 0x0
0x0 0x5 0x6 0x4
0x3 0xF 0x10 0x0
0x3 0x1F 0x20 0x10

**Default:** 0x80

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | SFRWPRIV [7:7] | TSTOPEN [6:6] | TSTARTEN [5:5] | MASK [4:0] | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:10] | | | | | | HALTREQ [9:9] | RAMPRIV [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | EN [31:31] | None [30:24] | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:4 | MASK | RW | R | X | This value determines the maximum size of the trace buffer in SRAM. It specifies the most-significant bit of the POSITION.POINTER field that can be updated by automatic increment. If the trace tries to advance past this power of two, the POSITION.WRAP bit is set to 1, the POSITION.POINTER[MASK:0] bits are set to zero, and the POSITION.POINTER[AWIDTH-4:MASK+1] bits remain unchanged.<br>This field causes the trace packet information to be stored in a circular buffer of size 2(MASK+4) bytes, that can be positioned in memory at multiples of this size.<br>Valid values of this field are zero to AWIDTH-4. Values greater than the maximum have the same effect as the maximum. |
| 5 | TSTARTEN | RW | R | 0 | Trace start input enable. If this bit is 1 and the TSTART signal is HIGH, then the EN bit is set to 1. Tracing continues until a stop condition occurs. |
| 6 | TSTOPEN | RW | R | 0 | Trace stop input enable. If this bit is 1 and the TSTOP signal is HIGH, then the EN bit is set to 0. If a trace packet is being written to memory, the write is completed before tracing is stopped. |
| 7 | SFRWPRIV | RW | R | 1 | Special Function Register Write Privilege bit. If this bit is 0, then User or Privileged AHB-Lite read and write accesses to the Special Function Registers are permitted. If this bit is 1, then only Privileged write accesses are permitted and User write accesses are ignored. The HPROT[1] signal determines if an access is User or Privileged.<br>Note<br>- SFR read accesses are not controlled by this bit and are always permitted.<br>- This bit is implemented only if User/Privilege support is present in the MTB configuration. If User/Privilege support is absent, then the behavior of this bit is RAZ/WI and the value of the HPROT[1] signal is ignored. |
| 8 | RAMPRIV | RW | R | 0 | SRAM Privilege bit. If this bit is 0, then User or Privileged AHB-Lite read and write accesses to the SRAM are permitted. If this bit is 1, then only Privileged AHB-Lite read and write accesses to the SRAM are permitted and User accesses are RAZ/WI. The HPROT[1] signal determines if an access is User or Privileged.<br>Note<br>This bit is implemented only if User/Privilege support is present in the MTB configuration. If User/Privilege support is absent, then the behavior of this bit is RAZ/WI and the value of the HPROT[1] signal is ignored. |
| 9 | HALTREQ | RW | RW | 0 | Halt request bit. This bit is connected to the halt request signal of the trace logic, EDBGRQ.<br>When HALTREQ is set to 1, EDBGRQ is asserted if DBGEN is also HIGH.<br>The HALTREQ bit can be automatically set to 1 using the FLOW.WATERMARK field. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 31 | EN | RW | RW | 0 | Main trace enable bit.<br>When this bit is 1 trace data is written into the SRAM memory location addressed by POSITION.POINTER.<br>The POSITION.POINTER value auto increments after the trace data packet is written.<br>The EN bit can be automatically set to 0 using the FLOW.WATERMARK field and the FLOW.AUTOSTOP bit.<br>The EN bit is automatically set to 1 if the TSTARTEN bit is 1 and the TSTART signal is HIGH.<br>The EN bit is automatically set to 0 if TSTOPEN bit is 1 and the TSTOP signal is HIGH.<br>Note:<br>If the EN bit is set to 0 because the FLOW.WATERMARK field is set, then it is not automatically set to 1 if the TSTARTEN bit is 1 and the TSTART input is HIGH. In this case tracing can only be restarted if the FLOW.WATERMARK or POSITION.POINTER value is changed by software. |

### 3.8.7.3 CM0P_MTB_FLOW

**Description:** FLOW register
**Address:** 0xF0003008
**Offset:** 0x8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Contains:
- The WATERMARK address.
- The AUTOSTOP and AUTOHALT control bits.
Usage constraints: There are no additional usage constraints.
Configurations: Available in all MTB configurations.
Attributes: You can modify all fields by software.
Note
- If you stop tracing, using the watermark auto stop feature, you cannot restart tracing until software clears the watermark auto stop. You can achieve this in one of the following ways:
- Changing the POSITION.POINTER field value to point to the beginning of the trace buffer.
- Setting the FLOW.AUTOSTOP bit to 0.
- A debug agent can use the AUTOSTOP bit to fill the trace buffer once only without halting the processor.
- A debug agent can use the AUTOHALT bit to fill the trace buffer once before causing the Cortex-M0+ processor to enter the Debug state. To enter Debug state, the Cortex-M0+ processor might have to perform additional branch type operations. Therefore you must set the WATERMARK field below the final entry in the trace buffer region.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | WATERMARK [7:3] | | | | | None [2:2] | AUTOHALT [1:1] | AUTOSTOP [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | WATERMARK [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | WATERMARK [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | WATERMARK [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | AUTOSTOP | RW | R | 0 | If this bit is 1 and WATERMARK is equal to POSITION.POINTER, then the MASTER.EN bit is automatically set to 0. This stops tracing. |
| 1 | AUTOHALT | RW | R | 0 | If this bit is 1 and WATERMARK is equal to POSITION.POINTER, then the MASTER.HALTREQ bit is automatically set to 1. If the DBGEN signal is HIGH, the MTB asserts this halt request to the Cortex-M0+ processor by asserting the EDBGRQ signal. |
| 3:31 | WATERMARK | RW | R | X | WATERMARK value. This field contains an address in the same format as the POSITION.POINTER field. When the POSITION.POINTER matches the WATERMARK field value, actions defined by the AUTOHALT and AUTOSTOP bits are performed. |

### 3.8.7.4 CM0P_MTB_BASE

**Description:** BASE register
**Address:** 0xF000300C
**Offset:** 0xC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Purpose: Indicates where the SRAM is located in the processor memory map. This register is provided to enable auto discovery of the MTB SRAM location, by a debug agent.
Usage constraints: There are no additional usage constraints.
Configurations: Available in all MTB configurations.
**Default:** 0xF0010000

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | BASE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | BASE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | BASE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | BASE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | BASE | R | R | 4026597376 | The value provided is the value of the SRAMBASEADDR[31:0] signal.<br>MTB SRAM base address in the processor memory map, which is fixed for this platform. |

### 3.8.7.5 CM0P_MTB_LA

**Description:** Lock Access register
**Address:** 0xF0003FB0
**Offset:** 0xFB0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 0 | N/A |

### 3.8.7.6 CM0P_MTB_LS

**Description:** Lock Status register
**Address:** 0xF0003FB4
**Offset:** 0xFB4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 0 | N/A |

### 3.8.7.7 CM0P_MTB_AS

**Description:** Authentication Status register
**Address:** 0xF0003FB8
**Offset:** 0xFB8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xA

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | AS_31TO4 [7:4] | | | | AS_3 [3:3] | NIDEN [2:2] | AS_1 [1:1] | DBGEN [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | AS_31TO4 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | AS_31TO4 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | AS_31TO4 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | DBGEN | R | R | 0 | Invasive debug enable |
| 1 | AS_1 | R | R | 1 | N/A |
| 2 | NIDEN | R | R | 0 | Non-invasive debug enable |
| 3 | AS_3 | R | R | 1 | N/A |
| 4:31 | AS_31TO4 | R | R | 0 | N/A |

### 3.8.7.8 CM0P_MTB_DARCH

**Description:** Device Architecture register
**Address:** 0xF0003FBC
**Offset:** 0xFBC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x47700A31

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | ARCH_ID [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | ARCH_ID [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | ARCHITECT [23:21] | | | RES_20 [20:20] | REVISION [19:16] | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | ARCHITECT [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | ARCH_ID | R | R | 2609 | Basic Trace Router Architecture<br>Major Architecture Revision 0 |
| 16:19 | REVISION | R | R | 0 | Minor Architecture Revision |
| 20 | RES_20 | R | R | 1 | Reserved |
| 21:31 | ARCHITECT | R | R | 571 | Architect ARM |

### 3.8.7.9 CM0P_MTB_DCFG

**Description:** Device Configuration register
**Address:** 0xF0003FC8
**Offset:** 0xFC8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 0 | N/A |

### 3.8.7.10 CM0P_MTB_DID

**Description:** Device Type Identifier register.
**Address:** 0xF0003FCC
**Offset:** 0xFCC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x31

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | SUB_TYPE [7:4] | | | | CLASS [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | CLASS | R | R | 1 | Trace Sink |
| 4:7 | SUB_TYPE | R | R | 3 | Basic Trace Router |

### 3.8.7.11 CM0P_MTB_PID4

**Description:** Peripheral Identification Register 4.
**Address:** 0xF0003FD0
**Offset:** 0xFD0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x4

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 4 | N/A |

### 3.8.7.12 CM0P_MTB_PID5

**Description:** Peripheral Identification Register 5.
**Address:** 0xF0003FD4
**Offset:** 0xFD4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 0 | N/A |

### 3.8.7.13 CM0P_MTB_PID6

**Description:** Peripheral Identification Register 6.
**Address:** 0xF0003FD8
**Offset:** 0xFD8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 0 | N/A |

### 3.8.7.14 CM0P_MTB_PID7

**Description:** Peripheral Identification Register 7.
**Address:** 0xF0003FDC
**Offset:** 0xFDC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 0 | N/A |

### 3.8.7.15 CM0P_MTB_PID0

**Description:** Peripheral Identification Register 0.
**Address:** 0xF0003FE0
**Offset:** 0xFE0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x32

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 50 | N/A |

### 3.8.7.16 CM0P_MTB_PID1

**Description:** Peripheral Identification Register 1.
**Address:** 0xF0003FE4
**Offset:** 0xFE4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xB9

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 185 | N/A |

### 3.8.7.17 CM0P_MTB_PID2

**Description:** Peripheral Identification Register 2.
**Address:** 0xF0003FE8
**Offset:** 0xFE8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x1B

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 27 | N/A |

### 3.8.7.18 CM0P_MTB_PID3

**Description:** Peripheral Identification Register 3.
**Address:** 0xF0003FEC
**Offset:** 0xFEC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | ECOREVNUM [7:4] | | | | None [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 4:7 | ECOREVNUM | R | R | 0 | ECO revision for MTB |

### 3.8.7.19 CM0P_MTB_CID0

**Description:** Component Identification Register 0.
**Address:** 0xF0003FF0
**Offset:** 0xFF0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xD

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 13 | N/A |

### 3.8.7.20 CM0P_MTB_CID1

**Description:** Component Identification Register 1.
**Address:** 0xF0003FF4
**Offset:** 0xFF4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x90

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 144 | N/A |

### 3.8.7.21 CM0P_MTB_CID2

**Description:** Component Identification Register 2.
**Address:** 0xF0003FF8
**Offset:** 0xFF8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x5

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 5 | N/A |

### 3.8.7.22 CM0P_MTB_CID3

**Description:** Component Identification Register 3.
**Address:** 0xF0003FFC
**Offset:** 0xFFC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xB1

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 177 | N/A |

# 4 CM7

**Description** Cortex-M7 specific registers
**Base Address** 0xE0000000
**Size** 0x20000000
**Slave Num** SYSTEM

## 4.1 ITM

| Register Name | Address | Permission | Description |
|---|---|---|---|
| CM7_ITM_STIM0 | 0xE0000000 | FULL | Stimulus Port registers |
| CM7_ITM_STIM1 | 0xE0000004 | FULL | Stimulus Port registers |
| CM7_ITM_STIM2 | 0xE0000008 | FULL | Stimulus Port registers |
| CM7_ITM_STIM3 | 0xE000000C | FULL | Stimulus Port registers |
| CM7_ITM_STIM4 | 0xE0000010 | FULL | Stimulus Port registers |
| CM7_ITM_STIM5 | 0xE0000014 | FULL | Stimulus Port registers |
| CM7_ITM_STIM6 | 0xE0000018 | FULL | Stimulus Port registers |
| CM7_ITM_STIM7 | 0xE000001C | FULL | Stimulus Port registers |
| CM7_ITM_STIM8 | 0xE0000020 | FULL | Stimulus Port registers |
| CM7_ITM_STIM9 | 0xE0000024 | FULL | Stimulus Port registers |
| CM7_ITM_STIM10 | 0xE0000028 | FULL | Stimulus Port registers |
| CM7_ITM_STIM11 | 0xE000002C | FULL | Stimulus Port registers |
| CM7_ITM_STIM12 | 0xE0000030 | FULL | Stimulus Port registers |
| CM7_ITM_STIM13 | 0xE0000034 | FULL | Stimulus Port registers |
| CM7_ITM_STIM14 | 0xE0000038 | FULL | Stimulus Port registers |
| CM7_ITM_STIM15 | 0xE000003C | FULL | Stimulus Port registers |
| CM7_ITM_STIM16 | 0xE0000040 | FULL | Stimulus Port registers |
| CM7_ITM_STIM17 | 0xE0000044 | FULL | Stimulus Port registers |
| CM7_ITM_STIM18 | 0xE0000048 | FULL | Stimulus Port registers |
| CM7_ITM_STIM19 | 0xE000004C | FULL | Stimulus Port registers |
| CM7_ITM_STIM20 | 0xE0000050 | FULL | Stimulus Port registers |
| CM7_ITM_STIM21 | 0xE0000054 | FULL | Stimulus Port registers |
| CM7_ITM_STIM22 | 0xE0000058 | FULL | Stimulus Port registers |
| CM7_ITM_STIM23 | 0xE000005C | FULL | Stimulus Port registers |
| CM7_ITM_STIM24 | 0xE0000060 | FULL | Stimulus Port registers |
| CM7_ITM_STIM25 | 0xE0000064 | FULL | Stimulus Port registers |
| CM7_ITM_STIM26 | 0xE0000068 | FULL | Stimulus Port registers |
| CM7_ITM_STIM27 | 0xE000006C | FULL | Stimulus Port registers |
| CM7_ITM_STIM28 | 0xE0000070 | FULL | Stimulus Port registers |
| CM7_ITM_STIM29 | 0xE0000074 | FULL | Stimulus Port registers |
| CM7_ITM_STIM30 | 0xE0000078 | FULL | Stimulus Port registers |
| CM7_ITM_STIM31 | 0xE000007C | FULL | Stimulus Port registers |
| CM7_ITM_TER | 0xE0000E00 | FULL | Trace Enable Register |
| CM7_ITM_TPR | 0xE0000E40 | FULL | ITM Trace Privilege Register |
| CM7_ITM_TCR | 0xE0000E80 | FULL | Trace Control Register |
| CM7_ITM_ITATRDR | 0xE0000EF0 | FULL | Integration Mode Read ATB Ready |
| CM7_ITM_ITATVAL | 0xE0000EF8 | FULL | Integration Mode Write ATB Valid |
| CM7_ITM_TCTRL | 0xE0000F00 | FULL | Integration Mode Control Register |
| CM7_ITM_LAR | 0xE0000FB0 | FULL | Lock Access Register |
| CM7_ITM_LSR | 0xE0000FB4 | FULL | Lock Status Register |
| CM7_ITM_PID4 | 0xE0000FD0 | FULL | Peripheral Identification Register 4. |
| CM7_ITM_PID5 | 0xE0000FD4 | FULL | Peripheral Identification Register 5. |
| CM7_ITM_PID6 | 0xE0000FD8 | FULL | Peripheral Identification Register 6. |
| CM7_ITM_PID7 | 0xE0000FDC | FULL | Peripheral Identification Register 7. |
| CM7_ITM_PID0 | 0xE0000FE0 | FULL | Peripheral Identification Register 0. |
| CM7_ITM_PID1 | 0xE0000FE4 | FULL | Peripheral Identification Register 1. |
| CM7_ITM_PID2 | 0xE0000FE8 | FULL | Peripheral Identification Register 2. |
| CM7_ITM_PID3 | 0xE0000FEC | FULL | Peripheral Identification Register 3. |
| CM7_ITM_CID0 | 0xE0000FF0 | FULL | Component Identification Register 0. |
| CM7_ITM_CID1 | 0xE0000FF4 | FULL | Component Identification Register 1. |
| CM7_ITM_CID2 | 0xE0000FF8 | FULL | Component Identification Register 2. |
| CM7_ITM_CID3 | 0xE0000FFC | FULL | Component Identification Register 3. |

## 4.2 DWT

| Register Name | Address | Permission | Description |
|---|---|---|---|
| CM7_DWT_CTRL | 0xE0001000 | FULL | Control register |
| CM7_DWT_CYCCNT | 0xE0001004 | FULL | Cycle Count register |
| CM7_DWT_CPICNT | 0xE0001008 | FULL | CPI Count register |
| CM7_DWT_EXCCNT | 0xE000100C | FULL | Exception Overhead Count register |
| CM7_DWT_SLEEPCNT | 0xE0001010 | FULL | Sleep Count register |
| CM7_DWT_LSUCNT | 0xE0001014 | FULL | LSU Count register |
| CM7_DWT_FOLDCNT | 0xE0001018 | FULL | Folded-instruction Count register |
| CM7_DWT_PCSR | 0xE000101C | FULL | Program Counter Sample Register |
| CM7_DWT_COMP0 | 0xE0001020 | FULL | Comparator registers |
| CM7_DWT_MASK0 | 0xE0001024 | FULL | Comparator Mask registers |
| CM7_DWT_FUNCTION0 | 0xE0001028 | FULL | Comparator Function registers |
| CM7_DWT_COMP1 | 0xE0001030 | FULL | Comparator registers |
| CM7_DWT_MASK1 | 0xE0001034 | FULL | Comparator Mask registers |
| CM7_DWT_FUNCTION1 | 0xE0001038 | FULL | Comparator Function registers |
| CM7_DWT_COMP2 | 0xE0001040 | FULL | Comparator registers |
| CM7_DWT_MASK2 | 0xE0001044 | FULL | Comparator Mask registers |
| CM7_DWT_FUNCTION2 | 0xE0001048 | FULL | Comparator Function registers |
| CM7_DWT_COMP3 | 0xE0001050 | FULL | Comparator registers |
| CM7_DWT_MASK3 | 0xE0001054 | FULL | Comparator Mask registers |
| CM7_DWT_FUNCTION3 | 0xE0001058 | FULL | Comparator Function registers |
| CM7_DWT_LAR | 0xE0001FB0 | FULL | Lock Access Register |
| CM7_DWT_LSR | 0xE0001FB4 | FULL | Lock Status Register |
| CM7_DWT_PID4 | 0xE0001FD0 | FULL | Peripheral Identification Register 4. |
| CM7_DWT_PID5 | 0xE0001FD4 | FULL | Peripheral Identification Register 5. |
| CM7_DWT_PID6 | 0xE0001FD8 | FULL | Peripheral Identification Register 6. |
| CM7_DWT_PID7 | 0xE0001FDC | FULL | Peripheral Identification Register 7. |
| CM7_DWT_PID0 | 0xE0001FE0 | FULL | Peripheral Identification Register 0. |
| CM7_DWT_PID1 | 0xE0001FE4 | FULL | Peripheral Identification Register 1. |
| CM7_DWT_PID2 | 0xE0001FE8 | FULL | Peripheral Identification Register 2. |
| CM7_DWT_PID3 | 0xE0001FEC | FULL | Peripheral Identification Register 3. |
| CM7_DWT_CID0 | 0xE0001FF0 | FULL | Component Identification Register 0. |
| CM7_DWT_CID1 | 0xE0001FF4 | FULL | Component Identification Register 1. |
| CM7_DWT_CID2 | 0xE0001FF8 | FULL | Component Identification Register 2. |
| CM7_DWT_CID3 | 0xE0001FFC | FULL | Component Identification Register 3. |

## 4.3 FPB

| Register Name | Address | Permission | Description |
|---|---|---|---|
| CM7_FPB_CTRL | 0xE0002000 | FULL | FlashPatch Control Register |
| CM7_FPB_REMAP | 0xE0002004 | FULL | FlashPatch Remap register |
| CM7_FPB_COMP0 | 0xE0002008 | FULL | FlashPatch Comparator register |
| CM7_FPB_COMP1 | 0xE000200C | FULL | FlashPatch Comparator register |
| CM7_FPB_COMP2 | 0xE0002010 | FULL | FlashPatch Comparator register |
| CM7_FPB_COMP3 | 0xE0002014 | FULL | FlashPatch Comparator register |
| CM7_FPB_COMP4 | 0xE0002018 | FULL | FlashPatch Comparator register |
| CM7_FPB_COMP5 | 0xE000201C | FULL | FlashPatch Comparator register |
| CM7_FPB_COMP6 | 0xE0002020 | FULL | FlashPatch Comparator register |
| CM7_FPB_COMP7 | 0xE0002024 | FULL | FlashPatch Comparator register |
| CM7_FPB_LAR | 0xE0002FB0 | FULL | Lock Access Register |
| CM7_FPB_LSR | 0xE0002FB4 | FULL | Lock Status Register |
| CM7_FPB_PID4 | 0xE0002FD0 | FULL | Peripheral Identification Register 4. |
| CM7_FPB_PID5 | 0xE0002FD4 | FULL | Peripheral Identification Register 5. |
| CM7_FPB_PID6 | 0xE0002FD8 | FULL | Peripheral Identification Register 6. |
| CM7_FPB_PID7 | 0xE0002FDC | FULL | Peripheral Identification Register 7. |
| CM7_FPB_PID0 | 0xE0002FE0 | FULL | Peripheral Identification Register 0. |
| CM7_FPB_PID1 | 0xE0002FE4 | FULL | Peripheral Identification Register 1. |
| CM7_FPB_PID2 | 0xE0002FE8 | FULL | Peripheral Identification Register 2. |
| CM7_FPB_PID3 | 0xE0002FEC | FULL | Peripheral Identification Register 3. |
| CM7_FPB_CID0 | 0xE0002FF0 | FULL | Component Identification Register 0. |
| CM7_FPB_CID1 | 0xE0002FF4 | FULL | Component Identification Register 1. |
| CM7_FPB_CID2 | 0xE0002FF8 | FULL | Component Identification Register 2. |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| CM7_FPB_CID3 | 0xE0002FFC | FULL | Component Identification Register 3. |

## 4.4 SCS

| Register Name | Address | Permission | Description |
|---|---|---|---|
| CM7_SCS_ACTLR | 0xE000E008 | FULL | Auxiliary Control Register |
| CM7_SCS_SYST_CSR | 0xE000E010 | FULL | SysTick Control and Status Register |
| CM7_SCS_SYST_RVR | 0xE000E014 | FULL | SysTick Reload Value Register |
| CM7_SCS_SYST_CVR | 0xE000E018 | FULL | SysTick Current Value Register |
| CM7_SCS_SYST_CALIB | 0xE000E01C | FULL | SysTick Calibration value Register |
| CM7_SCS_NVIC_ISER0 | 0xE000E100 | FULL | Interrupt Set-Enable Registers |
| CM7_SCS_NVIC_ISER1 | 0xE000E104 | FULL | Interrupt Set-Enable Registers |
| CM7_SCS_NVIC_ISER2 | 0xE000E108 | FULL | Interrupt Set-Enable Registers |
| CM7_SCS_NVIC_ISER3 | 0xE000E10C | FULL | Interrupt Set-Enable Registers |
| CM7_SCS_NVIC_ISER4 | 0xE000E110 | FULL | Interrupt Set-Enable Registers |
| CM7_SCS_NVIC_ISER5 | 0xE000E114 | FULL | Interrupt Set-Enable Registers |
| CM7_SCS_NVIC_ISER6 | 0xE000E118 | FULL | Interrupt Set-Enable Registers |
| CM7_SCS_NVIC_ISER7 | 0xE000E11C | FULL | Interrupt Set-Enable Registers |
| CM7_SCS_NVIC_ICER0 | 0xE000E180 | FULL | Interrupt Clear-Enable Registers |
| CM7_SCS_NVIC_ICER1 | 0xE000E184 | FULL | Interrupt Clear-Enable Registers |
| CM7_SCS_NVIC_ICER2 | 0xE000E188 | FULL | Interrupt Clear-Enable Registers |
| CM7_SCS_NVIC_ICER3 | 0xE000E18C | FULL | Interrupt Clear-Enable Registers |
| CM7_SCS_NVIC_ICER4 | 0xE000E190 | FULL | Interrupt Clear-Enable Registers |
| CM7_SCS_NVIC_ICER5 | 0xE000E194 | FULL | Interrupt Clear-Enable Registers |
| CM7_SCS_NVIC_ICER6 | 0xE000E198 | FULL | Interrupt Clear-Enable Registers |
| CM7_SCS_NVIC_ICER7 | 0xE000E19C | FULL | Interrupt Clear-Enable Registers |
| CM7_SCS_NVIC_ISPR0 | 0xE000E200 | FULL | Interrupt Set-Pending Registers |
| CM7_SCS_NVIC_ISPR1 | 0xE000E204 | FULL | Interrupt Set-Pending Registers |
| CM7_SCS_NVIC_ISPR2 | 0xE000E208 | FULL | Interrupt Set-Pending Registers |
| CM7_SCS_NVIC_ISPR3 | 0xE000E20C | FULL | Interrupt Set-Pending Registers |
| CM7_SCS_NVIC_ISPR4 | 0xE000E210 | FULL | Interrupt Set-Pending Registers |
| CM7_SCS_NVIC_ISPR5 | 0xE000E214 | FULL | Interrupt Set-Pending Registers |
| CM7_SCS_NVIC_ISPR6 | 0xE000E218 | FULL | Interrupt Set-Pending Registers |
| CM7_SCS_NVIC_ISPR7 | 0xE000E21C | FULL | Interrupt Set-Pending Registers |
| CM7_SCS_NVIC_ICPR0 | 0xE000E280 | FULL | Interrupt Clear-Pending Registers |
| CM7_SCS_NVIC_ICPR1 | 0xE000E284 | FULL | Interrupt Clear-Pending Registers |
| CM7_SCS_NVIC_ICPR2 | 0xE000E288 | FULL | Interrupt Clear-Pending Registers |
| CM7_SCS_NVIC_ICPR3 | 0xE000E28C | FULL | Interrupt Clear-Pending Registers |
| CM7_SCS_NVIC_ICPR4 | 0xE000E290 | FULL | Interrupt Clear-Pending Registers |
| CM7_SCS_NVIC_ICPR5 | 0xE000E294 | FULL | Interrupt Clear-Pending Registers |
| CM7_SCS_NVIC_ICPR6 | 0xE000E298 | FULL | Interrupt Clear-Pending Registers |
| CM7_SCS_NVIC_ICPR7 | 0xE000E29C | FULL | Interrupt Clear-Pending Registers |
| CM7_SCS_NVIC_IABR0 | 0xE000E300 | FULL | Interrupt Active Bit Registers |
| CM7_SCS_NVIC_IABR1 | 0xE000E304 | FULL | Interrupt Active Bit Registers |
| CM7_SCS_NVIC_IABR2 | 0xE000E308 | FULL | Interrupt Active Bit Registers |
| CM7_SCS_NVIC_IABR3 | 0xE000E30C | FULL | Interrupt Active Bit Registers |
| CM7_SCS_NVIC_IABR4 | 0xE000E310 | FULL | Interrupt Active Bit Registers |
| CM7_SCS_NVIC_IABR5 | 0xE000E314 | FULL | Interrupt Active Bit Registers |
| CM7_SCS_NVIC_IABR6 | 0xE000E318 | FULL | Interrupt Active Bit Registers |
| CM7_SCS_NVIC_IABR7 | 0xE000E31C | FULL | Interrupt Active Bit Registers |
| CM7_SCS_NVIC_IPR0 | 0xE000E400 | FULL | Interrupt Priority Registers |
| CM7_SCS_NVIC_IPR1 | 0xE000E404 | FULL | Interrupt Priority Registers |
| CM7_SCS_NVIC_IPR2 | 0xE000E408 | FULL | Interrupt Priority Registers |
| CM7_SCS_NVIC_IPR3 | 0xE000E40C | FULL | Interrupt Priority Registers |
| CM7_SCS_NVIC_IPR4 | 0xE000E410 | FULL | Interrupt Priority Registers |
| CM7_SCS_NVIC_IPR5 | 0xE000E414 | FULL | Interrupt Priority Registers |
| CM7_SCS_NVIC_IPR6 | 0xE000E418 | FULL | Interrupt Priority Registers |
| CM7_SCS_NVIC_IPR7 | 0xE000E41C | FULL | Interrupt Priority Registers |
| CM7_SCS_NVIC_IPR8 | 0xE000E420 | FULL | Interrupt Priority Registers |
| CM7_SCS_NVIC_IPR9 | 0xE000E424 | FULL | Interrupt Priority Registers |
| CM7_SCS_NVIC_IPR10 | 0xE000E428 | FULL | Interrupt Priority Registers |
| CM7_SCS_NVIC_IPR11 | 0xE000E42C | FULL | Interrupt Priority Registers |
| CM7_SCS_NVIC_IPR12 | 0xE000E430 | FULL | Interrupt Priority Registers |
| CM7_SCS_NVIC_IPR13 | 0xE000E434 | FULL | Interrupt Priority Registers |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| CM7_SCS_NVIC_IPR14 | 0xE000E438 | FULL | Interrupt Priority Registers |
| CM7_SCS_NVIC_IPR15 | 0xE000E43C | FULL | Interrupt Priority Registers |
| CM7_SCS_NVIC_IPR16 | 0xE000E440 | FULL | Interrupt Priority Registers |
| CM7_SCS_NVIC_IPR17 | 0xE000E444 | FULL | Interrupt Priority Registers |
| CM7_SCS_NVIC_IPR18 | 0xE000E448 | FULL | Interrupt Priority Registers |
| CM7_SCS_NVIC_IPR19 | 0xE000E44C | FULL | Interrupt Priority Registers |
| CM7_SCS_NVIC_IPR20 | 0xE000E450 | FULL | Interrupt Priority Registers |
| CM7_SCS_NVIC_IPR21 | 0xE000E454 | FULL | Interrupt Priority Registers |
| CM7_SCS_NVIC_IPR22 | 0xE000E458 | FULL | Interrupt Priority Registers |
| CM7_SCS_NVIC_IPR23 | 0xE000E45C | FULL | Interrupt Priority Registers |
| CM7_SCS_NVIC_IPR24 | 0xE000E460 | FULL | Interrupt Priority Registers |
| CM7_SCS_NVIC_IPR25 | 0xE000E464 | FULL | Interrupt Priority Registers |
| CM7_SCS_NVIC_IPR26 | 0xE000E468 | FULL | Interrupt Priority Registers |
| CM7_SCS_NVIC_IPR27 | 0xE000E46C | FULL | Interrupt Priority Registers |
| CM7_SCS_NVIC_IPR28 | 0xE000E470 | FULL | Interrupt Priority Registers |
| CM7_SCS_NVIC_IPR29 | 0xE000E474 | FULL | Interrupt Priority Registers |
| CM7_SCS_NVIC_IPR30 | 0xE000E478 | FULL | Interrupt Priority Registers |
| CM7_SCS_NVIC_IPR31 | 0xE000E47C | FULL | Interrupt Priority Registers |
| CM7_SCS_NVIC_IPR32 | 0xE000E480 | FULL | Interrupt Priority Registers |
| CM7_SCS_NVIC_IPR33 | 0xE000E484 | FULL | Interrupt Priority Registers |
| CM7_SCS_NVIC_IPR34 | 0xE000E488 | FULL | Interrupt Priority Registers |
| CM7_SCS_NVIC_IPR35 | 0xE000E48C | FULL | Interrupt Priority Registers |
| CM7_SCS_NVIC_IPR36 | 0xE000E490 | FULL | Interrupt Priority Registers |
| CM7_SCS_NVIC_IPR37 | 0xE000E494 | FULL | Interrupt Priority Registers |
| CM7_SCS_NVIC_IPR38 | 0xE000E498 | FULL | Interrupt Priority Registers |
| CM7_SCS_NVIC_IPR39 | 0xE000E49C | FULL | Interrupt Priority Registers |
| CM7_SCS_NVIC_IPR40 | 0xE000E4A0 | FULL | Interrupt Priority Registers |
| CM7_SCS_NVIC_IPR41 | 0xE000E4A4 | FULL | Interrupt Priority Registers |
| CM7_SCS_NVIC_IPR42 | 0xE000E4A8 | FULL | Interrupt Priority Registers |
| CM7_SCS_NVIC_IPR43 | 0xE000E4AC | FULL | Interrupt Priority Registers |
| CM7_SCS_NVIC_IPR44 | 0xE000E4B0 | FULL | Interrupt Priority Registers |
| CM7_SCS_NVIC_IPR45 | 0xE000E4B4 | FULL | Interrupt Priority Registers |
| CM7_SCS_NVIC_IPR46 | 0xE000E4B8 | FULL | Interrupt Priority Registers |
| CM7_SCS_NVIC_IPR47 | 0xE000E4BC | FULL | Interrupt Priority Registers |
| CM7_SCS_NVIC_IPR48 | 0xE000E4C0 | FULL | Interrupt Priority Registers |
| CM7_SCS_NVIC_IPR49 | 0xE000E4C4 | FULL | Interrupt Priority Registers |
| CM7_SCS_NVIC_IPR50 | 0xE000E4C8 | FULL | Interrupt Priority Registers |
| CM7_SCS_NVIC_IPR51 | 0xE000E4CC | FULL | Interrupt Priority Registers |
| CM7_SCS_NVIC_IPR52 | 0xE000E4D0 | FULL | Interrupt Priority Registers |
| CM7_SCS_NVIC_IPR53 | 0xE000E4D4 | FULL | Interrupt Priority Registers |
| CM7_SCS_NVIC_IPR54 | 0xE000E4D8 | FULL | Interrupt Priority Registers |
| CM7_SCS_NVIC_IPR55 | 0xE000E4DC | FULL | Interrupt Priority Registers |
| CM7_SCS_NVIC_IPR56 | 0xE000E4E0 | FULL | Interrupt Priority Registers |
| CM7_SCS_NVIC_IPR57 | 0xE000E4E4 | FULL | Interrupt Priority Registers |
| CM7_SCS_NVIC_IPR58 | 0xE000E4E8 | FULL | Interrupt Priority Registers |
| CM7_SCS_NVIC_IPR59 | 0xE000E4EC | FULL | Interrupt Priority Registers |
| CM7_SCS_CPUID | 0xE000ED00 | FULL | CPUID Base Register |
| CM7_SCS_ICSR | 0xE000ED04 | FULL | Interrupt Control and State Register |
| CM7_SCS_VTOR | 0xE000ED08 | FULL | Vector Table Offset Register |
| CM7_SCS_AIRCR | 0xE000ED0C | FULL | Application Interrupt and Reset Control Register |
| CM7_SCS_SCR | 0xE000ED10 | FULL | System Control Register |
| CM7_SCS_CCR | 0xE000ED14 | FULL | Configuration and Control Register |
| CM7_SCS_SHPR1 | 0xE000ED18 | FULL | System Handler Priority Register 1 |
| CM7_SCS_SHPR2 | 0xE000ED1C | FULL | System Handler Priority Register 2 |
| CM7_SCS_SHPR3 | 0xE000ED20 | FULL | System Handler Priority Register 3 |
| CM7_SCS_SHCSR | 0xE000ED24 | FULL | System Handler Control and State Register |
| CM7_SCS_CFSR | 0xE000ED28 | FULL | Configurable Fault Status Register |
| CM7_SCS_HFSR | 0xE000ED2C | FULL | HardFault Status Register |
| CM7_SCS_DFSR | 0xE000ED30 | FULL | Debug Fault Status Register |
| CM7_SCS_MMFAR | 0xE000ED34 | FULL | MemManage Fault Address Register |
| CM7_SCS_BFAR | 0xE000ED38 | FULL | BusFault Address Register |
| CM7_SCS_ID_PFR0 | 0xE000ED40 | FULL | Processor Feature Register 0 |
| CM7_SCS_ID_PFR1 | 0xE000ED44 | FULL | Processor Feature Register 1 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| CM7_SCS_ID_DFR0 | 0xE000ED48 | FULL | Debug Feature Register 0 |
| CM7_SCS_ID_AFR0 | 0xE000ED4C | FULL | Auxiliary Feature Register 0 |
| CM7_SCS_ID_MMFR0 | 0xE000ED50 | FULL | Memory Model Feature Register 0 |
| CM7_SCS_ID_MMFR1 | 0xE000ED54 | FULL | Memory Model Feature Register 1 |
| CM7_SCS_ID_MMFR2 | 0xE000ED58 | FULL | Memory Model Feature Register 2 |
| CM7_SCS_ID_MMFR3 | 0xE000ED5C | FULL | Memory Model Feature Register 3 |
| CM7_SCS_ID_ISAR0 | 0xE000ED60 | FULL | Instruction Set Attributes Register 0 |
| CM7_SCS_ID_ISAR1 | 0xE000ED64 | FULL | Instruction Set Attributes Register 1 |
| CM7_SCS_ID_ISAR2 | 0xE000ED68 | FULL | Instruction Set Attributes Register 2 |
| CM7_SCS_ID_ISAR3 | 0xE000ED6C | FULL | Instruction Set Attributes Register 3 |
| CM7_SCS_ID_ISAR4 | 0xE000ED70 | FULL | Instruction Set Attributes Register 4 |
| CM7_SCS_CLIDR | 0xE000ED78 | FULL | Cache Level ID Register |
| CM7_SCS_CTR | 0xE000ED7C | FULL | Cache Type Register |
| CM7_SCS_CCSIDR | 0xE000ED80 | FULL | Cache Size ID Register |
| CM7_SCS_CSSELR | 0xE000ED84 | FULL | Cache Size Selection Register |
| CM7_SCS_CPACR | 0xE000ED88 | FULL | Coprocessor Access Control Register |
| CM7_SCS_MPU_TYPE | 0xE000ED90 | FULL | MPU Type Register |
| CM7_SCS_MPU_CTRL | 0xE000ED94 | FULL | MPU Control Register |
| CM7_SCS_MPU_RNR | 0xE000ED98 | FULL | MPU Region Number Register |
| CM7_SCS_MPU_RBAR | 0xE000ED9C | FULL | MPU Region Base Address Register |
| CM7_SCS_MPU_RASR | 0xE000EDA0 | FULL | MPU Region Attribute and Size Register |
| CM7_SCS_MPU_RBAR_A1 | 0xE000EDA4 | FULL | MPU alias registers |
| CM7_SCS_MPU_RASR_A1 | 0xE000EDA8 | FULL | MPU alias registers |
| CM7_SCS_MPU_RBAR_A2 | 0xE000EDAC | FULL | MPU alias registers |
| CM7_SCS_MPU_RASR_A2 | 0xE000EDB0 | FULL | MPU alias registers |
| CM7_SCS_MPU_RBAR_A3 | 0xE000EDB4 | FULL | MPU alias registers |
| CM7_SCS_MPU_RASR_A3 | 0xE000EDB8 | FULL | MPU alias registers |
| CM7_SCS_DHCSR | 0xE000EDF0 | FULL | Debug Halting Control and Status Register |
| CM7_SCS_DCRSR | 0xE000EDF4 | FULL | Debug Core Register Selector Register |
| CM7_SCS_DCRDR | 0xE000EDF8 | FULL | Debug Core Register Data Register |
| CM7_SCS_DEMCR | 0xE000EDFC | FULL | Debug Exception and Monitor Control Register |
| CM7_SCS_STIR | 0xE000EF00 | FULL | Software Triggered Interrupt Register |
| CM7_SCS_FPCCR | 0xE000EF34 | FULL | FP Context Control Register |
| CM7_SCS_FPCAR | 0xE000EF38 | FULL | FP Context Control Register |
| CM7_SCS_FPDSCR | 0xE000EF3C | FULL | FP Context Control Register |
| CM7_SCS_MVFR0 | 0xE000EF40 | FULL | Media and VFP Feature Register 0 |
| CM7_SCS_MVFR1 | 0xE000EF44 | FULL | Media and VFP Feature Register 1 |
| CM7_SCS_MVFR2 | 0xE000EF48 | FULL | Media and VFP Feature Register 2 |
| CM7_SCS_ICIALLU | 0xE000EF50 | FULL | Instruction cache invalidate all to Point of Unification (PoU) |
| CM7_SCS_ICIMVAU | 0xE000EF58 | FULL | Instruction cache invalidate by address to PoU |
| CM7_SCS_DCIMVAC | 0xE000EF5C | FULL | Data cache invalidate by address to Point of Coherency (PoC) |
| CM7_SCS_DCISW | 0xE000EF60 | FULL | Data cache invalidate by set/way |
| CM7_SCS_DCCMVAU | 0xE000EF64 | FULL | Data cache by address to PoU |
| CM7_SCS_DCCMVAC | 0xE000EF68 | FULL | Data cache clean by address to PoU |
| CM7_SCS_DCCSW | 0xE000EF6C | FULL | Data cache clean by set/way |
| CM7_SCS_DCCIMVAC | 0xE000EF70 | FULL | Data cache clean and invalidate by address to PoC |
| CM7_SCS_DCCISW | 0xE000EF74 | FULL | Data cache clean and invalidate by set/way |
| CM7_SCS_CM7_ITCMCR | 0xE000EF90 | FULL | Instruction Tightly Coupled Memory Control Register |
| CM7_SCS_CM7_DTCMCR | 0xE000EF94 | FULL | Data Tightly Coupled Memory Control Register |
| CM7_SCS_CM7_AHBPCR | 0xE000EF98 | FULL | AHBP Control Register |
| CM7_SCS_CM7_CACR | 0xE000EF9C | FULL | L1 Cache Control Register |
| CM7_SCS_CM7_AHBSCR | 0xE000EFA0 | FULL | AHB Slave Control Register |
| CM7_SCS_CM7_ABFSR | 0xE000EFA8 | FULL | Auxiliary Bus Fault Status Register |
| CM7_SCS_IEBR0 | 0xE000EFB0 | FULL | Instruction Error bank Register 0 |
| CM7_SCS_IEBR1 | 0xE000EFB4 | FULL | Instruction Error bank Register 1 |
| CM7_SCS_DEBR0 | 0xE000EFB8 | FULL | Data Error Bank Register 0 |
| CM7_SCS_DEBR1 | 0xE000EFBC | FULL | Data Error Bank Register 1 |
| CM7_SCS_PID4 | 0xE000EFD0 | FULL | Peripheral Identification Register 4 |
| CM7_SCS_PID5 | 0xE000EFD4 | FULL | Peripheral Identification Register 5 |
| CM7_SCS_PID6 | 0xE000EFD8 | FULL | Peripheral Identification Register 6 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| CM7_SCS_PID7 | 0xE000EFDC | FULL | Peripheral Identification Register 7 |
| CM7_SCS_PID0 | 0xE000EFE0 | FULL | Peripheral Identification Register 0 |
| CM7_SCS_PID1 | 0xE000EFE4 | FULL | Peripheral Identification Register 1 |
| CM7_SCS_PID2 | 0xE000EFE8 | FULL | Peripheral Identification Register 2 |
| CM7_SCS_PID3 | 0xE000EFEC | FULL | Peripheral Identification Register 3 |
| CM7_SCS_CID0 | 0xE000EFF0 | FULL | Component Identification Register 0 |
| CM7_SCS_CID1 | 0xE000EFF4 | FULL | Component Identification Register 1 |
| CM7_SCS_CID2 | 0xE000EFF8 | FULL | Component Identification Register 2 |
| CM7_SCS_CID3 | 0xE000EFFC | FULL | Component Identification Register 3 |

## 4.5 ETM

| Register Name | Address | Permission | Description |
|---|---|---|---|
| CM7_ETM_TRCPRGCTLR | 0xE0041004 | FULL | Programming Control Register |
| CM7_ETM_TRCSTATR | 0xE004100C | FULL | Status Register |
| CM7_ETM_TRCCONFIGR | 0xE0041010 | FULL | Trace Configuration Register |
| CM7_ETM_TRCEVENTCTL0R | 0xE0041020 | FULL | Event Control 0 Register |
| CM7_ETM_TRCEVENTCTL1R | 0xE0041024 | FULL | Event Control 1 Register |
| CM7_ETM_TRCSTALLCTLR | 0xE004102C | FULL | Stall Control Register |
| CM7_ETM_TRCTSCTLR | 0xE0041030 | FULL | Global Timestamp Control Register |
| CM7_ETM_TRCSYNCPR | 0xE0041034 | FULL | Synchronization Period Register |
| CM7_ETM_TRCCCCTLR | 0xE0041038 | FULL | Cycle Count Control Register |
| CM7_ETM_TRCTRACEIDR | 0xE0041040 | FULL | Trace ID Register |
| CM7_ETM_TRCVICTLR | 0xE0041080 | FULL | ViewInst Main Control Register |
| CM7_ETM_TRCVIPCSSCTLR | 0xE004108C | FULL | ViewInst Start-Stop Processor Comparator Control Register |
| CM7_ETM_TRCCNTRLDVR | 0xE0041140 | FULL | Counter Reload Valkue Registers |
| CM7_ETM_TRCIDR8 | 0xE0041180 | FULL | ID Register 8 |
| CM7_ETM_TRCIDR9 | 0xE0041184 | FULL | ID Register 9 |
| CM7_ETM_TRCIDR10 | 0xE0041188 | FULL | ID Register 10 |
| CM7_ETM_TRCIDR11 | 0xE004118C | FULL | ID Register 11 |
| CM7_ETM_TRCIDR12 | 0xE0041190 | FULL | ID Register 12 |
| CM7_ETM_TRCIDR13 | 0xE0041194 | FULL | ID Register 13 |
| CM7_ETM_TRCIMPSPEC0 | 0xE00411C0 | FULL | Implementation Specific Register 0 |
| CM7_ETM_TRCIDR0 | 0xE00411E0 | FULL | ID Register 0 |
| CM7_ETM_TRCIDR1 | 0xE00411E4 | FULL | ID Register 1 |
| CM7_ETM_TRCIDR2 | 0xE00411E8 | FULL | ID Register 2 |
| CM7_ETM_TRCIDR3 | 0xE00411EC | FULL | ID Register 3 |
| CM7_ETM_TRCIDR4 | 0xE00411F0 | FULL | ID Register 4 |
| CM7_ETM_TRCIDR5 | 0xE00411F4 | FULL | ID Register 5 |
| CM7_ETM_TRCRSCTLR2 | 0xE0041208 | FULL | Resource Selection Register 2 |
| CM7_ETM_TRCRSCTLR3 | 0xE004120C | FULL | Resource Selection Register 3 |
| CM7_ETM_TRCSSCCR0 | 0xE0041280 | FULL | Single-shot Comparator Control Register0 |
| CM7_ETM_TRCSSCSR0 | 0xE00412A0 | FULL | Single-shot Comparator Status Register 0 |
| CM7_ETM_TRCSSPCICR0 | 0xE00412C0 | FULL | Single-shot Comparator Status Register 0 |
| CM7_ETM_TRCOSLSR | 0xE0041304 | FULL | OS Lock Status Register |
| CM7_ETM_TRCPDCR | 0xE0041310 | FULL | Power Down Control Register |
| CM7_ETM_TRCPDSR | 0xE0041314 | FULL | Power Down Status Register |
| CM7_ETM_TRCITMISCOUTR | 0xE0041EDC | FULL | Integration Miscellaneous Outputs Register |
| CM7_ETM_TRCITMISCINR | 0xE0041EE0 | FULL | Integration Miscellaneous Inputs Register |
| CM7_ETM_TRCITATBIDR | 0xE0041EE4 | FULL | Integration ATB Identification Register |
| CM7_ETM_TRCITDDATAR | 0xE0041EE8 | FULL | Integration Data ATB Data Register |
| CM7_ETM_TRCITIDATAR | 0xE0041EEC | FULL | Integration Instruction ATB Data Register |
| CM7_ETM_TRCITDATBINR | 0xE0041EF0 | FULL | Integration Data ATB In Register |
| CM7_ETM_TRCITIATBINR | 0xE0041EF4 | FULL | Integration Instruction ATB In Register |
| CM7_ETM_TRCITDATBOUTR | 0xE0041EF8 | FULL | Integration Data ATB Out Register |
| CM7_ETM_TRCITIATBOUTR | 0xE0041EFC | FULL | Integration Instruction ATB Out Register |
| CM7_ETM_TRCITCTRL | 0xE0041F00 | FULL | Integration Mode Control Register |
| CM7_ETM_TRCCLAIMSET | 0xE0041FA0 | FULL | Claim Tag Set Register |
| CM7_ETM_TRCCLAIMCLR | 0xE0041FA4 | FULL | Claim Tag Clear Register |
| CM7_ETM_TRCLAR | 0xE0041FB0 | FULL | Software Lock Access Register |
| CM7_ETM_TRCLSR | 0xE0041FB4 | FULL | Software Lock Status Register |
| CM7_ETM_TRCAUTHSTATUS | 0xE0041FB8 | FULL | Authentication Status Register |
| CM7_ETM_TRCDEVARCH | 0xE0041FBC | FULL | Device Architecture Register |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| CM7_ETM_TRCDEVID | 0xE0041FC8 | FULL | Device ID Register |
| CM7_ETM_TRCDEVTYPE | 0xE0041FCC | FULL | CoreSight Device Type Register |
| CM7_ETM_PID4 | 0xE0041FD0 | FULL | Peripheral Identification Register 4. |
| CM7_ETM_PID5 | 0xE0041FD4 | FULL | Peripheral Identification Register 5. |
| CM7_ETM_PID6 | 0xE0041FD8 | FULL | Peripheral Identification Register 6. |
| CM7_ETM_PID7 | 0xE0041FDC | FULL | Peripheral Identification Register 7. |
| CM7_ETM_PID0 | 0xE0041FE0 | FULL | Peripheral Identification Register 0. |
| CM7_ETM_PID1 | 0xE0041FE4 | FULL | Peripheral Identification Register 1. |
| CM7_ETM_PID2 | 0xE0041FE8 | FULL | Peripheral Identification Register 2. |
| CM7_ETM_PID3 | 0xE0041FEC | FULL | Peripheral Identification Register 3. |
| CM7_ETM_CID0 | 0xE0041FF0 | FULL | Component Identification Register 0. |
| CM7_ETM_CID1 | 0xE0041FF4 | FULL | Component Identification Register 1. |
| CM7_ETM_CID2 | 0xE0041FF8 | FULL | Component Identification Register 2. |
| CM7_ETM_CID3 | 0xE0041FFC | FULL | Component Identification Register 3. |

## 4.6 CM7CTI

| Register Name | Address | Permission | Description |
|---|---|---|---|
| CM7_CM7CTI_CTICONTROL | 0xE0042000 | FULL | CTI Control Register |
| CM7_CM7CTI_CTIINTACK | 0xE0042010 | FULL | CTI Interrupt Acknowledge Register |
| CM7_CM7CTI_CTIAPPSET | 0xE0042014 | FULL | CTI Application Trigger Set Register |
| CM7_CM7CTI_CTIAPPCLEAR | 0xE0042018 | FULL | CTI Application Trigger Clear Register |
| CM7_CM7CTI_CTIAPPPULSE | 0xE004201C | FULL | CTI Application Pulse Register |
| CM7_CM7CTI_CTIINEN0 | 0xE0042020 | FULL | CTI Trigger to Channel Enable Registers |
| CM7_CM7CTI_CTIINEN1 | 0xE0042024 | FULL | CTI Trigger to Channel Enable Registers |
| CM7_CM7CTI_CTIINEN2 | 0xE0042028 | FULL | CTI Trigger to Channel Enable Registers |
| CM7_CM7CTI_CTIINEN3 | 0xE004202C | FULL | CTI Trigger to Channel Enable Registers |
| CM7_CM7CTI_CTIINEN4 | 0xE0042030 | FULL | CTI Trigger to Channel Enable Registers |
| CM7_CM7CTI_CTIINEN5 | 0xE0042034 | FULL | CTI Trigger to Channel Enable Registers |
| CM7_CM7CTI_CTIINEN6 | 0xE0042038 | FULL | CTI Trigger to Channel Enable Registers |
| CM7_CM7CTI_CTIINEN7 | 0xE004203C | FULL | CTI Trigger to Channel Enable Registers |
| CM7_CM7CTI_CTIOUTEN0 | 0xE00420A0 | FULL | CTI Channel to Trigger Enable Registers |
| CM7_CM7CTI_CTIOUTEN1 | 0xE00420A4 | FULL | CTI Channel to Trigger Enable Registers |
| CM7_CM7CTI_CTIOUTEN2 | 0xE00420A8 | FULL | CTI Channel to Trigger Enable Registers |
| CM7_CM7CTI_CTIOUTEN3 | 0xE00420AC | FULL | CTI Channel to Trigger Enable Registers |
| CM7_CM7CTI_CTIOUTEN4 | 0xE00420B0 | FULL | CTI Channel to Trigger Enable Registers |
| CM7_CM7CTI_CTIOUTEN5 | 0xE00420B4 | FULL | CTI Channel to Trigger Enable Registers |
| CM7_CM7CTI_CTIOUTEN6 | 0xE00420B8 | FULL | CTI Channel to Trigger Enable Registers |
| CM7_CM7CTI_CTIOUTEN7 | 0xE00420BC | FULL | CTI Channel to Trigger Enable Registers |
| CM7_CM7CTI_CTITRIGINSTATUS | 0xE0042130 | FULL | CTI Trigger In Status Register |
| CM7_CM7CTI_CTITRIGOUTSTATUS | 0xE0042134 | FULL | CTI Trigger Out Status Register |
| CM7_CM7CTI_CTICHINSTATUS | 0xE0042138 | FULL | CTI Channel In Status Register |
| CM7_CM7CTI_CTICHOUTSTATUS | 0xE004213C | FULL | CTI Channel Out Status Register |
| CM7_CM7CTI_CTIGATE | 0xE0042140 | FULL | Enable CTI Channel Gate Register |
| CM7_CM7CTI_ASICCTL | 0xE0042144 | FULL | External Multiplexor Control Register |
| CM7_CM7CTI_ITCHINACK | 0xE0042EDC | FULL | ITCHINACK Register |
| CM7_CM7CTI_ITTRIGINACK | 0xE0042EE0 | FULL | ITTRIGINACK Register |
| CM7_CM7CTI_ITCHOUT | 0xE0042EE4 | FULL | ITCHOUT Register |
| CM7_CM7CTI_ITTRIGOUT | 0xE0042EE8 | FULL | ITTRIGOUT Register |
| CM7_CM7CTI_ITCHOUTACK | 0xE0042EEC | FULL | ITCHOUTACK Register |
| CM7_CM7CTI_ITTRIGOUTACK | 0xE0042EF0 | FULL | ITTRIGOUTACK Register |
| CM7_CM7CTI_ITCHIN | 0xE0042EF4 | FULL | ITCHIN Register |
| CM7_CM7CTI_ITTRIGIN | 0xE0042EF8 | FULL | ITTRIGIN Register |
| CM7_CM7CTI_ITCTRL | 0xE0042F00 | FULL | Integration Mode Control Register |
| CM7_CM7CTI_CLAIMSET | 0xE0042FA0 | FULL | Claim Tag Set Register |
| CM7_CM7CTI_CLAIMCLR | 0xE0042FA4 | FULL | Claim Tag Clear Register |
| CM7_CM7CTI_LOCKACCESS | 0xE0042FB0 | FULL | Lock Access Register |
| CM7_CM7CTI_LOCKSTATUS | 0xE0042FB4 | FULL | Lock Status Register |
| CM7_CM7CTI_AUTHSTATUS | 0xE0042FB8 | FULL | Authentication Status Register |
| CM7_CM7CTI_DEVID | 0xE0042FC8 | FULL | Device Configuration Register |
| CM7_CM7CTI_DEVTYPE | 0xE0042FCC | FULL | Device Type Identifier Register |
| CM7_CM7CTI_PID4 | 0xE0042FD0 | FULL | Peripheral Identification Register 4 |
| CM7_CM7CTI_PID5 | 0xE0042FD4 | FULL | Peripheral Identification Register 5 |
| CM7_CM7CTI_PID6 | 0xE0042FD8 | FULL | Peripheral Identification Register 6 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| CM7_CM7CTI_PID7 | 0xE0042FDC | FULL | Peripheral Identification Register 7 |
| CM7_CM7CTI_PID0 | 0xE0042FE0 | FULL | Peripheral Identification Register 0 |
| CM7_CM7CTI_PID1 | 0xE0042FE4 | FULL | Peripheral Identification Register 1 |
| CM7_CM7CTI_PID2 | 0xE0042FE8 | FULL | Peripheral Identification Register 2 |
| CM7_CM7CTI_PID3 | 0xE0042FEC | FULL | Peripheral Identification Register 3 |
| CM7_CM7CTI_CID0 | 0xE0042FF0 | FULL | Component Identification Register 0 |
| CM7_CM7CTI_CID1 | 0xE0042FF4 | FULL | Component Identification Register 1 |
| CM7_CM7CTI_CID2 | 0xE0042FF8 | FULL | Component Identification Register 2 |
| CM7_CM7CTI_CID3 | 0xE0042FFC | FULL | Component Identification Register 3 |

## 4.7 TRCCTI

| Register Name | Address | Permission | Description |
|---|---|---|---|
| CM7_TRCCTI_CTICONTROL | 0xE0080000 | FULL | CTI Control Register |
| CM7_TRCCTI_CTIINTACK | 0xE0080010 | FULL | CTI Interrupt Acknowledge Register |
| CM7_TRCCTI_CTIAPPSET | 0xE0080014 | FULL | CTI Application Trigger Set Register |
| CM7_TRCCTI_CTIAPPCLEAR | 0xE0080018 | FULL | CTI Application Trigger Clear Register |
| CM7_TRCCTI_CTIAPPPULSE | 0xE008001C | FULL | CTI Application Pulse Register |
| CM7_TRCCTI_CTIINEN0 | 0xE0080020 | FULL | CTI Trigger to Channel Enable Registers |
| CM7_TRCCTI_CTIINEN1 | 0xE0080024 | FULL | CTI Trigger to Channel Enable Registers |
| CM7_TRCCTI_CTIINEN2 | 0xE0080028 | FULL | CTI Trigger to Channel Enable Registers |
| CM7_TRCCTI_CTIINEN3 | 0xE008002C | FULL | CTI Trigger to Channel Enable Registers |
| CM7_TRCCTI_CTIINEN4 | 0xE0080030 | FULL | CTI Trigger to Channel Enable Registers |
| CM7_TRCCTI_CTIINEN5 | 0xE0080034 | FULL | CTI Trigger to Channel Enable Registers |
| CM7_TRCCTI_CTIINEN6 | 0xE0080038 | FULL | CTI Trigger to Channel Enable Registers |
| CM7_TRCCTI_CTIINEN7 | 0xE008003C | FULL | CTI Trigger to Channel Enable Registers |
| CM7_TRCCTI_CTIOUTEN0 | 0xE00800A0 | FULL | CTI Channel to Trigger Enable Registers |
| CM7_TRCCTI_CTIOUTEN1 | 0xE00800A4 | FULL | CTI Channel to Trigger Enable Registers |
| CM7_TRCCTI_CTIOUTEN2 | 0xE00800A8 | FULL | CTI Channel to Trigger Enable Registers |
| CM7_TRCCTI_CTIOUTEN3 | 0xE00800AC | FULL | CTI Channel to Trigger Enable Registers |
| CM7_TRCCTI_CTIOUTEN4 | 0xE00800B0 | FULL | CTI Channel to Trigger Enable Registers |
| CM7_TRCCTI_CTIOUTEN5 | 0xE00800B4 | FULL | CTI Channel to Trigger Enable Registers |
| CM7_TRCCTI_CTIOUTEN6 | 0xE00800B8 | FULL | CTI Channel to Trigger Enable Registers |
| CM7_TRCCTI_CTIOUTEN7 | 0xE00800BC | FULL | CTI Channel to Trigger Enable Registers |
| CM7_TRCCTI_CTITRIGINSTATUS | 0xE0080130 | FULL | CTI Trigger In Status Register |
| CM7_TRCCTI_CTITRIGOUTSTATUS | 0xE0080134 | FULL | CTI Trigger Out Status Register |
| CM7_TRCCTI_CTICHINSTATUS | 0xE0080138 | FULL | CTI Channel In Status Register |
| CM7_TRCCTI_CTICHOUTSTATUS | 0xE008013C | FULL | CTI Channel Out Status Register |
| CM7_TRCCTI_CTIGATE | 0xE0080140 | FULL | Enable CTI Channel Gate Register |
| CM7_TRCCTI_ASICCTL | 0xE0080144 | FULL | External Multiplexor Control Register |
| CM7_TRCCTI_ITCHINACK | 0xE0080EDC | FULL | ITCHINACK Register |
| CM7_TRCCTI_ITTRIGINACK | 0xE0080EE0 | FULL | ITTRIGINACK Register |
| CM7_TRCCTI_ITCHOUT | 0xE0080EE4 | FULL | ITCHOUT Register |
| CM7_TRCCTI_ITTRIGOUT | 0xE0080EE8 | FULL | ITTRIGOUT Register |
| CM7_TRCCTI_ITCHOUTACK | 0xE0080EEC | FULL | ITCHOUTACK Register |
| CM7_TRCCTI_ITTRIGOUTACK | 0xE0080EF0 | FULL | ITTRIGOUTACK Register |
| CM7_TRCCTI_ITCHIN | 0xE0080EF4 | FULL | ITCHIN Register |
| CM7_TRCCTI_ITTRIGIN | 0xE0080EF8 | FULL | ITTRIGIN Register |
| CM7_TRCCTI_ITCTRL | 0xE0080F00 | FULL | Integration Mode Control Register |
| CM7_TRCCTI_CLAIMSET | 0xE0080FA0 | FULL | Claim Tag Set Register |
| CM7_TRCCTI_CLAIMCLR | 0xE0080FA4 | FULL | Claim Tag Clear Register |
| CM7_TRCCTI_LOCKACCESS | 0xE0080FB0 | FULL | Lock Access Register |
| CM7_TRCCTI_LOCKSTATUS | 0xE0080FB4 | FULL | Lock Status Register |
| CM7_TRCCTI_AUTHSTATUS | 0xE0080FB8 | FULL | Authentication Status Register |
| CM7_TRCCTI_DEVID | 0xE0080FC8 | FULL | Device Configuration Register |
| CM7_TRCCTI_DEVTYPE | 0xE0080FCC | FULL | Device Type Identifier Register |
| CM7_TRCCTI_PID4 | 0xE0080FD0 | FULL | Peripheral Identification Register 4 |
| CM7_TRCCTI_PID5 | 0xE0080FD4 | FULL | Peripheral Identification Register 5 |
| CM7_TRCCTI_PID6 | 0xE0080FD8 | FULL | Peripheral Identification Register 6 |
| CM7_TRCCTI_PID7 | 0xE0080FDC | FULL | Peripheral Identification Register 7 |
| CM7_TRCCTI_PID0 | 0xE0080FE0 | FULL | Peripheral Identification Register 0 |
| CM7_TRCCTI_PID1 | 0xE0080FE4 | FULL | Peripheral Identification Register 1 |
| CM7_TRCCTI_PID2 | 0xE0080FE8 | FULL | Peripheral Identification Register 2 |
| CM7_TRCCTI_PID3 | 0xE0080FEC | FULL | Peripheral Identification Register 3 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| CM7_TRCCTI_CID0 | 0xE0080FF0 | FULL | Component Identification Register 0 |
| CM7_TRCCTI_CID1 | 0xE0080FF4 | FULL | Component Identification Register 1 |
| CM7_TRCCTI_CID2 | 0xE0080FF8 | FULL | Component Identification Register 2 |
| CM7_TRCCTI_CID3 | 0xE0080FFC | FULL | Component Identification Register 3 |

## 4.8 ETB_CSTF

### 4.8.1 TRC_CSTF

| Register Name | Address | Permission | Description |
|---|---|---|---|
| CM7_ETB_CSTF_CSTFCTL | 0xE008C000 | FULL | Funnel Control Register |
| CM7_ETB_CSTF_CSTFPCTL | 0xE008C004 | FULL | Priority Control Register |
| CM7_ETB_CSTF_ITATBDATA0 | 0xE008CEEC | FULL | Integration Register |
| CM7_ETB_CSTF_ITATBCTR2 | 0xE008CEF0 | FULL | Integration Register |
| CM7_ETB_CSTF_ITATBCTR1 | 0xE008CEF4 | FULL | Integration Register |
| CM7_ETB_CSTF_ITATBCTR0 | 0xE008CEF8 | FULL | Integration Register |
| CM7_ETB_CSTF_ITCTRL | 0xE008CF00 | FULL | Integration Mode Control Register |
| CM7_ETB_CSTF_CLAIMSET | 0xE008CFA0 | FULL | Claim Tag Set Register |
| CM7_ETB_CSTF_CLAIMCLR | 0xE008CFA4 | FULL | Claim Tag Clear Register |
| CM7_ETB_CSTF_LOCKACCESS | 0xE008CFB0 | FULL | Lock Access Register |
| CM7_ETB_CSTF_LOCKSTATUS | 0xE008CFB4 | FULL | Lock Status Register |
| CM7_ETB_CSTF_AUTHSTATUS | 0xE008CFB8 | FULL | Authentication Status Register |
| CM7_ETB_CSTF_DEVID | 0xE008CFC8 | FULL | Device ID |
| CM7_ETB_CSTF_DEVTYPE | 0xE008CFCC | FULL | Device Type Identifier Register |
| CM7_ETB_CSTF_PID4 | 0xE008CFD0 | FULL | Peripheral Identification Register 4 |
| CM7_ETB_CSTF_PID5 | 0xE008CFD4 | FULL | Peripheral Identification Register 5 |
| CM7_ETB_CSTF_PID6 | 0xE008CFD8 | FULL | Peripheral Identification Register 6 |
| CM7_ETB_CSTF_PID7 | 0xE008CFDC | FULL | Peripheral Identification Register 7 |
| CM7_ETB_CSTF_PID0 | 0xE008CFE0 | FULL | Peripheral Identification Register 0 |
| CM7_ETB_CSTF_PID1 | 0xE008CFE4 | FULL | Peripheral Identification Register 1 |
| CM7_ETB_CSTF_PID2 | 0xE008CFE8 | FULL | Peripheral Identification Register 2 |
| CM7_ETB_CSTF_PID3 | 0xE008CFEC | FULL | Peripheral Identification Register 3 |
| CM7_ETB_CSTF_CID0 | 0xE008CFF0 | FULL | Component Identification Register 0 |
| CM7_ETB_CSTF_CID1 | 0xE008CFF4 | FULL | Component Identification Register 1 |
| CM7_ETB_CSTF_CID2 | 0xE008CFF8 | FULL | Component Identification Register 2 |
| CM7_ETB_CSTF_CID3 | 0xE008CFFC | FULL | Component Identification Register 3 |

## 4.9 ETB

| Register Name | Address | Permission | Description |
|---|---|---|---|
| CM7_ETB_ETBRDP | 0xE008D004 | FULL | RAM Depth Register |
| CM7_ETB_ETBSTS | 0xE008D00C | FULL | Status Register |
| CM7_ETB_ETBRRD | 0xE008D010 | FULL | RAM Read Data Register |
| CM7_ETB_ETBRRP | 0xE008D014 | FULL | RAM Read Pointer Register |
| CM7_ETB_ETBRWP | 0xE008D018 | FULL | RAM Write Pointer Register |
| CM7_ETB_ETBTRG | 0xE008D01C | FULL | Trigger Counter Register |
| CM7_ETB_ETBCTL | 0xE008D020 | FULL | Control Register |
| CM7_ETB_ETBRWD | 0xE008D024 | FULL | RAM Write Data Register |
| CM7_ETB_ETBFFSR | 0xE008D300 | FULL | Formatter and Flush Status Register |
| CM7_ETB_ETBFFCR | 0xE008D304 | FULL | Formatter and Flush Control Register |
| CM7_ETB_ITMISCOP0 | 0xE008DEE0 | FULL | Integration Register |
| CM7_ETB_ITTRFLINACK | 0xE008DEE4 | FULL | Integration Register |
| CM7_ETB_ITTRFLIN | 0xE008DEE8 | FULL | Integration Register |
| CM7_ETB_ITATBDATA0 | 0xE008DEEC | FULL | Integration Register |
| CM7_ETB_ITATBCTR2 | 0xE008DEF0 | FULL | Integration Register |
| CM7_ETB_ITATBCTR1 | 0xE008DEF4 | FULL | Integration Register |
| CM7_ETB_ITATBCTR0 | 0xE008DEF8 | FULL | Integration Register |
| CM7_ETB_ITCTRL | 0xE008DF00 | FULL | Integration Mode Control Register |
| CM7_ETB_CLAIMSET | 0xE008DFA0 | FULL | Claim Tag Set Register |
| CM7_ETB_CLAIMCLR | 0xE008DFA4 | FULL | Claim Tag Clear Register |
| CM7_ETB_LOCKACCESS | 0xE008DFB0 | FULL | Lock Access Register |
| CM7_ETB_LOCKSTATUS | 0xE008DFB4 | FULL | Lock Status Register |
| CM7_ETB_AUTHSTATUS | 0xE008DFB8 | FULL | Authentication Status Register |
| CM7_ETB_DEVID | 0xE008DFC8 | FULL | Device ID |
| CM7_ETB_DEVTYPE | 0xE008DFCC | FULL | Device Type Identifier Register |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| CM7_ETB_PID4 | 0xE008DFD0 | FULL | Peripheral Identification Register 4 |
| CM7_ETB_PID5 | 0xE008DFD4 | FULL | Peripheral Identification Register 5 |
| CM7_ETB_PID6 | 0xE008DFD8 | FULL | Peripheral Identification Register 6 |
| CM7_ETB_PID7 | 0xE008DFDC | FULL | Peripheral Identification Register 7 |
| CM7_ETB_PID0 | 0xE008DFE0 | FULL | Peripheral Identification Register 0 |
| CM7_ETB_PID1 | 0xE008DFE4 | FULL | Peripheral Identification Register 1 |
| CM7_ETB_PID2 | 0xE008DFE8 | FULL | Peripheral Identification Register 2 |
| CM7_ETB_PID3 | 0xE008DFEC | FULL | Peripheral Identification Register 3 |
| CM7_ETB_CID0 | 0xE008DFF0 | FULL | Component Identification Register 0 |
| CM7_ETB_CID1 | 0xE008DFF4 | FULL | Component Identification Register 1 |
| CM7_ETB_CID2 | 0xE008DFF8 | FULL | Component Identification Register 2 |
| CM7_ETB_CID3 | 0xE008DFFC | FULL | Component Identification Register 3 |

## 4.10 TPIU

| Register Name | Address | Permission | Description |
|---|---|---|---|
| CM7_TPIU_TPIU_SPSR | 0xE008E000 | FULL | Supported Port Size Register |
| CM7_TPIU_TPIU_CPSR | 0xE008E004 | FULL | Current Port Size Register |
| CM7_TPIU_TPIU_STMR | 0xE008E100 | FULL | Supported Trigger Modes Register |
| CM7_TPIU_TPIU_TCVR | 0xE008E104 | FULL | Trigger Counter Value Register |
| CM7_TPIU_TPIU_TMR | 0xE008E108 | FULL | Trigger Multiplier register |
| CM7_TPIU_TPIU_STPMR | 0xE008E200 | FULL | Supported Test Patterns/Modes register |
| CM7_TPIU_TPIU_CTPMR | 0xE008E204 | FULL | Current Test Pattern/Modes register |
| CM7_TPIU_TPIU_TPRCR | 0xE008E208 | FULL | TPIU Test Pattern Repeat Counter Register |
| CM7_TPIU_TPIU_FFSR | 0xE008E300 | FULL | Formatter and Flush Status Register |
| CM7_TPIU_TPIU_FFCR | 0xE008E304 | FULL | Formatter and Flush Control Register |
| CM7_TPIU_TPIU_FSCR | 0xE008E308 | FULL | Formatter Synchronization Counter Register |
| CM7_TPIU_TPIU_EXCTLIPR | 0xE008E400 | FULL | TPIU EXCTL In Port Register |
| CM7_TPIU_TPIU_EXCTLOPR | 0xE008E404 | FULL | TPIU EXCTL Out Port register |
| CM7_TPIU_ITTRFLINACK | 0xE008EEE4 | FULL | Integration Test Trigger In and Flush In Acknowledge register |
| CM7_TPIU_ITTRFLIN | 0xE008EEE8 | FULL | Integration Test Trigger In and Flush In register |
| CM7_TPIU_ITATBDATA0 | 0xE008EEEC | FULL | Integration Test ATB Data register 0 |
| CM7_TPIU_ITATBCTR2 | 0xE008EEF0 | FULL | Integration Test ATB Control Register 2 |
| CM7_TPIU_ITATBCTR1 | 0xE008EEF4 | FULL | Integration Test ATB Control Register 1 |
| CM7_TPIU_ITATBCTR0 | 0xE008EEF8 | FULL | Integration Test ATB Control Register 0 |
| CM7_TPIU_ITCTRL | 0xE008EF00 | FULL | Integration Mode Control register |
| CM7_TPIU_CLAIMSET | 0xE008EFA0 | FULL | Claim Tag Set Register |
| CM7_TPIU_CLAIMCLR | 0xE008EFA4 | FULL | Claim Tag Clear Register |
| CM7_TPIU_LOCKACCESS | 0xE008EFB0 | FULL | Lock Access Register |
| CM7_TPIU_LOCKSTATUS | 0xE008EFB4 | FULL | Lock Status Register |
| CM7_TPIU_AUTHSTATUS | 0xE008EFB8 | FULL | Authentication Status register |
| CM7_TPIU_DEVID | 0xE008EFC8 | FULL | Device Configuration register |
| CM7_TPIU_DEVTYPE | 0xE008EFCC | FULL | Device Type Identifier register |
| CM7_TPIU_PID4 | 0xE008EFD0 | FULL | Peripheral Identification Register 4 |
| CM7_TPIU_PID0 | 0xE008EFE0 | FULL | Peripheral Identification Register 0 |
| CM7_TPIU_PID1 | 0xE008EFE4 | FULL | Peripheral Identification Register 1 |
| CM7_TPIU_PID2 | 0xE008EFE8 | FULL | Peripheral Identification Register 2 |
| CM7_TPIU_PID3 | 0xE008EFEC | FULL | Peripheral Identification Register 3 |
| CM7_TPIU_CID0 | 0xE008EFF0 | FULL | Component Identification Register 0 |
| CM7_TPIU_CID1 | 0xE008EFF4 | FULL | Component Identification Register 1 |
| CM7_TPIU_CID2 | 0xE008EFF8 | FULL | Component Identification Register 2 |
| CM7_TPIU_CID3 | 0xE008EFFC | FULL | Component Identification Register 3 |

## 4.11 ROMTABLE

| Register Name | Address | Permission | Description |
|---|---|---|---|
| CM7_ROMTABLE_TRC_CTI | 0xE00BF000 | FULL | CM7 CoreSight ROM Table Peripheral #0 |
| CM7_ROMTABLE_TRC_TRC_CSTF | 0xE00BF004 | FULL | CM7 CoreSight ROM Table Peripheral #1 |
| CM7_ROMTABLE_TRC_ETB | 0xE00BF008 | FULL | CM7 CoreSight ROM Table Peripheral #2 |
| CM7_ROMTABLE_TRC_TPIU | 0xE00BF00C | FULL | CM7 CoreSight ROM Table Peripheral #3 |
| CM7_ROMTABLE_TRC_CSMT | 0xE00BFFCC | FULL | CM7 CoreSight ROM Table Memory Type |
| CM7_ROMTABLE_TRC_PID4 | 0xE00BFFD0 | FULL | CM7 CoreSight ROM Table Peripheral ID #4 |
| CM7_ROMTABLE_TRC_PID0 | 0xE00BFFE0 | FULL | CM7 CoreSight ROM Table Peripheral ID #0 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| CM7_ROMTABLE_TRC_PID1 | 0xE00BFFE4 | FULL | CM7 CoreSight ROM Table Peripheral ID #1 |
| CM7_ROMTABLE_TRC_PID2 | 0xE00BFFE8 | FULL | CM7 CoreSight ROM Table Peripheral ID #2 |
| CM7_ROMTABLE_TRC_PID3 | 0xE00BFFEC | FULL | CM7 CoreSight ROM Table Peripheral ID #3 |
| CM7_ROMTABLE_TRC_CID0 | 0xE00BFFF0 | FULL | CM7 CoreSight ROM Table Component ID #0 |
| CM7_ROMTABLE_TRC_CID1 | 0xE00BFFF4 | FULL | CM7 CoreSight ROM Table Component ID #1 |
| CM7_ROMTABLE_TRC_CID2 | 0xE00BFFF8 | FULL | CM7 CoreSight ROM Table Component ID #2 |
| CM7_ROMTABLE_TRC_CID3 | 0xE00BFFFC | FULL | CM7 CoreSight ROM Table Component ID #3 |

## 4.12 ROMTABLE

| Register Name | Address | Permission | Description |
|---|---|---|---|
| CM7_ROMTABLE_CM7 | 0xE00FE000 | FULL | CM7 CoreSight ROM Table Peripheral #0 |
| CM7_ROMTABLE_CM7_ETM | 0xE00FE004 | FULL | CM7 CoreSight ROM Table Peripheral #1 |
| CM7_ROMTABLE_CM7_CTI | 0xE00FE008 | FULL | CM7 CoreSight ROM Table Peripheral #2 |
| CM7_ROMTABLE_DBG_TRC_ROM | 0xE00FE010 | FULL | CM7 CoreSight ROM Table Peripheral #3 |
| CM7_ROMTABLE_CSMT | 0xE00FEFCC | FULL | CM7 CoreSight ROM Table Memory Type |
| CM7_ROMTABLE_PID4 | 0xE00FEFD0 | FULL | CM7 CoreSight ROM Table Peripheral ID #4 |
| CM7_ROMTABLE_PID0 | 0xE00FEFE0 | FULL | CM7 CoreSight ROM Table Peripheral ID #0 |
| CM7_ROMTABLE_PID1 | 0xE00FEFE4 | FULL | CM7 CoreSight ROM Table Peripheral ID #1 |
| CM7_ROMTABLE_PID2 | 0xE00FEFE8 | FULL | CM7 CoreSight ROM Table Peripheral ID #2 |
| CM7_ROMTABLE_PID3 | 0xE00FEFEC | FULL | CM7 CoreSight ROM Table Peripheral ID #3 |
| CM7_ROMTABLE_CID0 | 0xE00FEFF0 | FULL | CM7 CoreSight ROM Table Component ID #0 |
| CM7_ROMTABLE_CID1 | 0xE00FEFF4 | FULL | CM7 CoreSight ROM Table Component ID #1 |
| CM7_ROMTABLE_CID2 | 0xE00FEFF8 | FULL | CM7 CoreSight ROM Table Component ID #2 |
| CM7_ROMTABLE_CID3 | 0xE00FEFFC | FULL | CM7 CoreSight ROM Table Component ID #3 |

## 4.13 ROM

| Register Name | Address | Permission | Description |
|---|---|---|---|
| CM7_ROM_SCS | 0xE00FF000 | FULL | CM7 CoreSight ROM Table Peripheral #0 |
| CM7_ROM_DWT | 0xE00FF004 | FULL | CM7 CoreSight ROM Table Peripheral #1 |
| CM7_ROM_FPB | 0xE00FF008 | FULL | CM7 CoreSight ROM Table Peripheral #2 |
| CM7_ROM_ITM | 0xE00FF00C | FULL | CM7 CoreSight ROM Table Peripheral #3 |
| CM7_ROM_CSMT | 0xE00FFFCC | FULL | CM7 CoreSight ROM Table Memory Type |
| CM7_ROM_PID4 | 0xE00FFFD0 | FULL | CM7 CoreSight ROM Table Peripheral ID #4 |
| CM7_ROM_PID0 | 0xE00FFFE0 | FULL | CM7 CoreSight ROM Table Peripheral ID #0 |
| CM7_ROM_PID1 | 0xE00FFFE4 | FULL | CM7 CoreSight ROM Table Peripheral ID #1 |
| CM7_ROM_PID2 | 0xE00FFFE8 | FULL | CM7 CoreSight ROM Table Peripheral ID #2 |
| CM7_ROM_PID3 | 0xE00FFFEC | FULL | CM7 CoreSight ROM Table Peripheral ID #3 |
| CM7_ROM_CID0 | 0xE00FFFF0 | FULL | CM7 CoreSight ROM Table Component ID #0 |
| CM7_ROM_CID1 | 0xE00FFFF4 | FULL | CM7 CoreSight ROM Table Component ID #1 |
| CM7_ROM_CID2 | 0xE00FFFF8 | FULL | CM7 CoreSight ROM Table Component ID #2 |
| CM7_ROM_CID3 | 0xE00FFFFC | FULL | CM7 CoreSight ROM Table Component ID #3 |

## 4.14 Register Details

### 4.14.1 ITM

#### 4.14.1.1 CM7_ITM_STIM

**Description:** Stimulus Port registers
**Address:** 0xE0000000
**Offset:** 0x0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** The ITM_STIMx register characteristics are:
Purpose: Provide the interface for generating instrumentation messages.
Usage constraints:
- Accessible by word-aligned byte, halfword, and word accesses.
- The number of ITM_STIM registers is an IMPLEMENTATION DEFINED multiple of eight, see Trace Privilege Register, ITM_TPR on page C1-775.
- When DEMCR.TRCENA is 0, the ITM_STIM registers are UNKNOWN on reads and ignore writes.
Configurations: Always implemented.
Attributes: See Table C1-11 on Arm TRM page C1-773, and the register field descriptions.
The address of ITM_STIMn is (0xE0000000 + 4n).
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | STIMULUS [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | STIMULUS [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | STIMULUS [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | STIMULUS [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | STIMULUS | RW | R | X | Data write to the stimulus port FIFO, for forwarding as a software event packet.<br>When read, bit[0] indicates whether the stimulus port FIFO can accept data:<br>0: Stimulus port FIFO full.<br>1: Stimulus port FIFO can accept at least one word.<br>This bit is UNKNOWN after a Power-on reset. |

### 4.14.1.2 CM7_ITM_TER

**Description:** Trace Enable Register
**Address:** 0xE0000E00
**Offset:** 0xE00
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** The ITM_TERx characteristics are:
Purpose: Provide an individual enable bit for each ITM_STIM register.
Usage constraints
- Each ITM_TER provides enable bits for 32 ITM_STIM registers.
- Bits corresponding to unimplemented ITM_STIM registers are RAZ/WI. See Trace Privilege Register, ITM_TPR on page C1-775 for information about the number of implemented ITM_STIM registers.
- The processor ignores any unprivileged write to an ITM_TERx bit if the corresponding ITM_TPR.PRIVMASK bit is set to 1, see Trace Privilege Register, ITM_TPR on Arm TRM page C1-775.
Configurations: Always implemented.
Attributes: See Table C1-11 on Arm TRM page C1-773.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | STIMENA [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | STIMENA [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | STIMENA [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | STIMENA [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | STIMENA | RW | R | 0 | For bit STIMENA[n]:<br>0: Stimulus port (n) disabled<br>1: Stimulus port (n) enabled |

#### 4.14.1.3 CM7_ITM_TPR

**Description:** ITM Trace Privilege Register
**Address:** 0xE0000E40
**Offset:** 0xE40
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Characteristics and bit assignments.of the ITM_TPR register.
Purpose: Enables an operating system to control the stimulus ports that are accessible by user code.
Usage constraints: You can only write to this register in privileged mode.
Configurations: This register is available if the ITM is configured in your implementation.
Attributes: Refer to the ITM register summary table.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:4] | | | | PRIVMASK [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | PRIVMASK | RW | R | 0 | Bit mask to enable tracing on ITM stimulus ports:<br>bit [0] = stimulus ports [7:0]<br>bit [1] = stimulus ports [15:8]<br>bit [2] = stimulus ports [23:16]<br>bit [3] = stimulus ports [31:24] |

#### 4.14.1.4 CM7_ITM_TCR

**Description:** Trace Control Register
**Address:** 0xE0000E80
**Offset:** 0xE80
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** The ITM_TCR characteristics are:
Purpose: Configures and controls transfers through the ITM interface.
Usage constraints: For information about constraints that apply in a system that supports multiple trace streams
see CoreSight requirements for the TraceBusID field on Arm TRM page C1-778.
Configurations: Always implemented.
Attributes: See Table C1-11 on Arm TRM page C1-773, and the register field descriptions.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:5] | | | SWOENA [4:4] | TXENA [3:3] | SYNCENA [2:2] | TSENA [1:1] | ITMENA [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:12] | | | | GTSFREQ [11:10] | | TSPRESCALE [9:8] | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | BUSY [23:23] | TRACEBUSID [22:16] | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | ITMENA | RW | R | 0 | Enables the ITM:<br>0 Disabled.<br>1 Enabled.<br>This is the master enable for the ITM unit. A debugger must set this bit to 1 to permit writes to all Stimulus Port registers.<br>A Power-on reset clears this bit to 0. |
| 1 | TSENA | RW | R | 0 | Enables Local timestamp generation:<br>0 Disabled.<br>1 Enabled.<br>A Power-on reset clears this bit to 0. |
| 2 | SYNCENA | RW | R | 0 | Enables Synchronization packet transmission for a synchronous TPIU:<br>0 Disabled.<br>1 Enabled.<br>A Power-on reset clears this bit to 0.<br>Note: If a debugger sets this bit to 1 it must also configure DWT_CTRL.SYNCTAP for the correct synchronization speed, see Control register, DWT_CTRL on Arm TRM page C1-797. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 3 | TXENA | RW | R | 0 | Enables forwarding of hardware event packet from the DWT unit to the ITM for output to the TPIU:<br>0 Disabled.<br>1 Enabled.<br>It is IMPLEMENTATION DEFINED whether the DWT discards packets that it cannot forward to the ITM.<br>Note: If a debugger changes this bit from 0 to 1, the DWT might forward a hardware event packet that it has previously generated.<br>A Power-on reset clears this bit to 0. |
| 4 | SWOENA | RW | R | 0 | Enables asynchronous clocking of the timestamp counter:<br>0 Timestamp counter uses the processor system clock.<br>1 Timestamp counter uses asynchronous clock from the TPIU interface. The timestamp counter is held in reset while the output line is idle.<br>Which clocking modes are implemented is IMPLEMENTATION DEFINED. If the implementation does not support both modes this bit is either RAZ or RAO, to indicate the implemented mode.<br>When this is a RW bit, on a Power-on reset, the value of this bit is UNKNOWN |
| 8:9 | TSPRESCALE | RW | R | 0 | Local timestamp prescaler, used with the trace packet reference clock. The possible values are:<br>00 No prescaling.<br>01 Divide by 4.<br>10 Divide by 16.<br>11 Divide by 64.<br>If implemented, a Power-on reset clears this field to zero.<br>If the processor does not implement the timestamp prescaler then these bits are reserved, RAZ/WI. |
| 10:11 | GTSFREQ | RW | R | 0 | Global timestamp frequency. Defines how often the ITM generates a global timestamp, based on the global timestamp clock frequency, or disables generation of global timestamps. The possible values are:<br>00 Disable generation of global timestamps.<br>01 Generate timestamp request whenever the ITM detects a change in global<br>timestamp counter bits[47:7]. This is approximately every 128 cycles.<br>10 Generate timestamp request whenever the ITM detects a change in global timestamp counter bits[47:13]. This is approximately every 8192 cycles.<br>11 Generate a timestamp after every packet, if the output FIFO is empty.<br>For more information see Global timestamping on Arm TRM page C1-771.<br>A Power-on reset clears this field to zero.<br>If the implementation does not support global timestamping then these bits are reserved, RAZ/WI. |
| 16:22 | TRACEBUSID | RW | R | 0 | Identifier for multi-source trace stream formatting. If multi-source trace is in use, the debugger must write a non-zero value to this field. For more information see CoreSight requirements for the TraceBusID field on Arm TRM page C1-778.<br>On a Power-on reset, the value of this field is UNKNOWN. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 23 | BUSY | RW | R | 0 | Indicates whether the ITM is currently processing events:<br>0 ITM is not processing any events.<br>1 ITM events present and being drained.<br>These bits are read-only. |

### 4.14.1.5 CM7_ITM_ITATRDR

**Description:** Integration Mode Read ATB Ready
**Address:** 0xE0000EF0
**Offset:** 0xEF0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 0 | N/A |

#### 4.14.1.6 CM7_ITM_ITATVAL

**Description:** Integration Mode Write ATB Valid
**Address:** 0xE0000EF8
**Offset:** 0xEF8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | W | R | 0 | N/A |

### 4.14.1.7 CM7_ITM_TCTRL

**Description:** Integration Mode Control Register
**Address:** 0xE0000F00
**Offset:** 0xF00
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | N/A |

#### 4.14.1.8 CM7_ITM_LAR

**Description:** Lock Access Register
**Address:** 0xE0000FB0
**Offset:** 0xFB0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | W | R | 0 | N/A |

#### 4.14.1.9 CM7_ITM_LSR

**Description:** Lock Status Register
**Address:** 0xE0000FB4
**Offset:** 0xFB4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 0 | N/A |

### 4.14.1.10 CM7_ITM_PID4

**Description:** Peripheral Identification Register 4.
**Address:** 0xE0000FD0
**Offset:** 0xFD0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x4

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 4 | N/A |

#### 4.14.1.11 CM7_ITM_PID5

**Description:** Peripheral Identification Register 5.
**Address:** 0xE0000FD4
**Offset:** 0xFD4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 0 | N/A |

### 4.14.1.12 CM7_ITM_PID6

**Description:** Peripheral Identification Register 6.
**Address:** 0xE0000FD8
**Offset:** 0xFD8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 0 | N/A |

#### 4.14.1.13 CM7_ITM_PID7

**Description:** Peripheral Identification Register 7.
**Address:** 0xE0000FDC
**Offset:** 0xFDC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 0 | N/A |

### 4.14.1.14 CM7_ITM_PID0

**Description:** Peripheral Identification Register 0.
**Address:** 0xE0000FE0
**Offset:** 0xFE0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x1

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 1 | N/A |

### 4.14.1.15 CM7_ITM_PID1

**Description:** Peripheral Identification Register 1.
**Address:** 0xE0000FE4
**Offset:** 0xFE4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xB0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 176 | N/A |

### 4.14.1.16 CM7_ITM_PID2

**Description:** Peripheral Identification Register 2.
**Address:** 0xE0000FE8
**Offset:** 0xFE8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xB

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 11 | N/A |

### 4.14.1.17 CM7_ITM_PID3

**Description:** Peripheral Identification Register 3.
**Address:** 0xE0000FEC
**Offset:** 0xFEC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | ECOREVNUM [7:4] | | | | None [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 4:7 | ECOREVNUM | R | R | 0 | ECO revision |

### 4.14.1.18 CM7_ITM_CID0

**Description:** Component Identification Register 0.
**Address:** 0xE0000FF0
**Offset:** 0xFF0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xD

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 13 | N/A |

### 4.14.1.19 CM7_ITM_CID1

**Description:** Component Identification Register 1.
**Address:** 0xE0000FF4
**Offset:** 0xFF4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xE0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 224 | N/A |

### 4.14.1.20 CM7_ITM_CID2

**Description:** Component Identification Register 2.
**Address:** 0xE0000FF8
**Offset:** 0xFF8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x5

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 5 | N/A |

### 4.14.1.21 CM7_ITM_CID3

**Description:** Component Identification Register 3.
**Address:** 0xE0000FFC
**Offset:** 0xFFC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xB1

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 177 | N/A |

### 4.14.2 DWT

#### 4.14.2.1 CM7_DWT_CTRL

**Description:** Control register
**Address:** 0xE0001000
**Offset:** 0x0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** The CTRL register characteristics are:
Purpose: Provides configuration and status information for the DWT unit, and used to control features of the unit.
Usage constraints: There are no usage constraints.
Configurations: Always implemented.
Attributes: See Table C1-21 and the register field descriptions.
**Default:** 0x40000000

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | POSTINIT [7:5] | | | POSTPRESET [4:1] | | | | CYCCNTENA [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:13] | | | PCSAMPLENA [12:12] | SYNCTAP [11:10] | | CYCTAP [9:9] | POSTINIT [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:23] | CYCEVTENA [22:22] | FOLDEVTENA [21:21] | LSUEVTENA [20:20] | SLEEPEVTENA [19:19] | EXCEVTENA [18:18] | CPIEVTENA [17:17] | EXCTRCENA [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | NUMCOMP [31:28] | | | | NOTRCPKT [27:27] | NOEXTTRIG [26:26] | NOCYCCNT [25:25] | NOPRFCNT [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | CYCCNTENA | RW | R | 0 | Enables CYCCNT:<br>0 Disabled.<br>1 Enabled.<br>This bit is UNK/SBZP if the NOCYCCNT bit is RAO. |
| 1:4 | POSTPRESET | RW | R | 0 | Reload value for the POSTCNT counter. For more information see The POSTCNT timer on Arm TRM page C1-792.<br>This field is UNK/SBZP if the NOCYCCNT bit is RAO. |
| 5:8 | POSTINIT | RW | R | 0 | Initial value for the POSTCNT counter. For more information see Enabling POSTCNT, and behavior of accesses to the DWT_CTRL.POSTINIT field and The POSTCNT timer on Arm TRM page C1-792.<br>This field is UNK/SBZP if the NOCYCCNT bit is RAO.<br>Note<br>This field was previously called POSTCNT. The changed name gives a better indication of its function. |
| 9 | CYCTAP | RW | R | 0 | Selects the position of the POSTCNT tap on the CYCCNT counter:<br>0 POSTCNT tap at CYCCNT[6].<br>1 POSTCNT tap at CYCCNT[10].<br>For more information see The POSTCNT timer on Arm TRM page C1-792.<br>This bit is UNK/SBZP if the NOCYCCNT bit is RAO. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 10:11 | SYNCTAP | RW | R | 0 | Selects the position of the synchronization packet counter tap on the CYCCNT counter. This determines the Synchronization packet rate:<br>00 Disabled. No Synchronization packets.<br>01 Synchronization counter tap at CYCCNT[24].<br>10 Synchronization counter tap at CYCCNT[26].<br>11 Synchronization counter tap at CYCCNT[28].<br>For more information see The synchronization packet timer on Arm TRM page C1-794.<br>This field is UNK/SBZP if the NOCYCCNT bit is RAO. |
| 12 | PCSAMPLENA | RW | R | 0 | Enables use of POSTCNT counter as a timer for Periodic PC sample packet generation:<br>0 No Periodic PC sample packets generated.<br>1 Periodic PC sample packets generated.<br>See The POSTCNT timer on Arm TRM page C1-792 for more information.<br>This bit is UNK/SBZP if the NOTRCPKT bit is RAO or the NOCYCCNT bit is RAO. |
| 16 | EXCTRCENA | RW | R | 0 | Enables generation of exception trace:<br>0 Disabled.<br>1 Enabled.<br>This bit is UNK/SBZP if the NOTRCPKT bit is RAO. |
| 17 | CPIEVTENA | RW | R | 0 | Enables generation of the CPI counter overflow event:<br>0 Disabled.<br>1 Enabled.<br>This bit is UNK/SBZP if the NOPRFCNT bit is RAO. |
| 18 | EXCEVTENA | RW | R | 0 | Enables generation of the Exception overhead counter overflow event:<br>0 Disabled.<br>1 Enabled.<br>This bit is UNK/SBZP if the NOPRFCNT bit is RAO. |
| 19 | SLEEPEVTENA | RW | R | 0 | Enables generation of the Sleep counter overflow event.<br>0 Disabled.<br>1 Enabled.<br>This bit is UNK/SBZP if the NOPRFCNT bit is RAO. |
| 20 | LSUEVTENA | RW | R | 0 | Enables generation of the LSU counter overflow event.<br>0 Disabled.<br>1 Enabled.<br>This bit is UNK/SBZP if the NOPRFCNT bit is RAO. |
| 21 | FOLDEVTENA | RW | R | 0 | Enables generation of the Folded-instruction counter overflow event:<br>0 Disabled.<br>1 Enabled.<br>This bit is UNK/SBZP if the NOPRFCNT bit is RAO. |
| 22 | CYCEVTENA | RW | R | 0 | Enables POSTCNT underflow Event counter packets generation:<br>0 No POSTCNT underflow packets generated.<br>1 POSTCNT underflow packets generated, if PCSAMPLENA set to 0.<br>See The POSTCNT timer on Arm TRM page C1-792 for more information.<br>This bit is UNK/SBZP if the NOTRCPKT bit is RAO or the NOCYCCNT bit is RAO. |
| 24 | NOPRFCNT | RW | R | 0 | Shows whether the implementation supports the profiling counters:<br>0 Supported.<br>1 Not supported.<br>For more information see Profiling counter support on Arm TRM page C1-794.<br>This bit is read-only. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 25 | NOCYCCNT | RW | R | 0 | Shows whether the implementation supports a cycle counter:<br>0 Cycle counter supported.<br>1 Cycle counter not supported.<br>For more information see CYCCNT cycle counter and related timers on Arm TRM page C1-792. This bit is read-only. |
| 26 | NOEXTTRIG | RW | R | 0 | Shows whether the implementation includes external match signals, CMPMATCH[N]:<br>0 CMPMATCH[N] supported.<br>1 CMPMATCH[N] not supported.<br>This bit is read-only. |
| 27 | NOTRCPKT | RW | R | 0 | Shows whether the implementation supports trace sampling and exception tracing:<br>0 Trace sampling and exception tracing supported.<br>1 Trace sampling and exception tracing not supported.<br>If this bit is RAZ, the NOCYCCNT bit must also RAZ.<br>This bit is read-only. |
| 28:31 | NUMCOMP | RW | R | 4 | Number of comparators implemented.<br>A value of zero indicates no comparator support.<br>These bits are read-only. |

### 4.14.2.2 CM7_DWT_CYCCNT

**Description:** Cycle Count register
**Address:** 0xE0001004
**Offset:** 0x4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** The CYCCNT register characteristics are:
Purpose: Shows or sets the value of the processor cycle counter, CYCCNT.
Usage constraints: The DWT unit suspends CYCCNT counting when the processor is in Debug state.
Configurations:
Implemented only when CTRL.NOCYCCNT is RAZ, see Control register, CTRL on page C1-797.
When CTRL.NOCYCCNT is RAO no cycle counter is implemented and this register is UNK/SBZP.
Attributes: See Table C1-21 on Arm TRM page C1-797.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | CYCNT [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | CYCNT [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | CYCNT [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | CYCNT [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | CYCNT | RW | RW | 0 | Incrementing cycle counter value. When enabled, CYCCNT increments on each processor clock cycle. On overflow, CYCCNT wraps to zero. |

### 4.14.2.3 CM7_DWT_CPICNT

**Description:** CPI Count register
**Address:** 0xE0001008
**Offset:** 0x8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** The CPICNT register characteristics are:
Purpose: Counts additional cycles required to execute multi-cycle instructions and instruction fetch stalls.
Usage constraints: The counter initializes to 0 when software enables its counter overflow event by setting the CTRL.CPIEVTENA bit to 1.
Configurations:
Implemented only when CTRL.NOPRFCNT is RAZ, see Control register, CTRL on page C1-797.
If CTRL.NOPRFCNT is RAO, indicating that the implementation does not include the profiling counters, this register is UNK/SBZP.
Attributes: See Table C1-21 on Arm TRM page C1-797.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | CPICNT [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | CPICNT | RW | RW | 0 | Base instruction overhead counter. Counts one on each cycle when all of the following are true:<br>- No instruction is executed.<br>- No load-store operation is in progress, see LSU Count register, DWT_LSUCNT on page C1-803.<br>- No exception-entry or exception-exit operation is in progress, see Exception Overhead Count register, DWT_EXCCNT on Arm TRM page C1-802.<br>- Not in a power saving mode, see Sleep Count register, DWT_SLEEPCNT on page C1-802.<br>The definition of 'no instruction is executed' is IMPLEMENTATION DEFINED. ARM recommends that this counts each cycle on which no instruction is retired.<br>An event is emitted on counter overflow. Initialized to zero when DWT_CTRL.CPIEVTENA transitions from 0 to 1. |

### 4.14.2.4 CM7_DWT_EXCCNT

**Description:** Exception Overhead Count register
**Address:** 0xE000100C
**Offset:** 0xC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** The EXCCNT register characteristics are:
Purpose: Counts the total cycles spent in exception processing.
Usage constraints: The counter initializes to 0 when software enables its counter overflow event by setting the CTRL.EXCEVTENA bit to 1.
Configurations
Implemented only when CTRL.NOPRFCNT is RAZ, see Control register, CTRL on page C1-797.
If CTRL.NOPRFCNT is RAO, indicating that the implementation does not include the profiling counters, this register is UNK/SBZP.
Attributes: See Table C1-21 on Arm TRM page C1-797.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | EXCCNT [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | EXCCNT | RW | RW | 0 | The exception overhead counter. Counts one on each cycle when all of the following are true:<br>- No instruction is executed, see CPI Count register, DWT_CPICNT on Arm TRM page C1-801.<br>- An exception-entry or exception-exit related operation is in progress.<br>Exception-entry or exception-exit related operations include the stacking of registers on exception entry, unstacking of registers on exception exit, and preemption.<br>An event is emitted on counter overflow. Initialized to zero when DWT_CTRL.EXCEVTENA transitions from 0 to 1. |

### 4.14.2.5 CM7_DWT_SLEEPCNT

**Description:** Sleep Count register
**Address:** 0xE0001010
**Offset:** 0x10
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** The SLEEPCNT register characteristics are:
Purpose: Counts the total number of cycles that the processor is sleeping.
Usage constraints: The counter initializes to 0 when software enables its counter overflow event by setting the CTRL.SLEEPEVTENA bit to 1.
Configurations:
Implemented only when CTRL.NOPRFCNT is RAZ, see Control register, CTRL on page C1-797.
If CTRL.NOPRFCNT is RAO, indicating that the implementation does not include the profiling counters, this register is UNK/SBZP.
Attributes: See Table C1-21 on Arm TRM page C1-797.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | SLEEPCNT [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | SLEEPCNT | RW | RW | 0 | Sleep counter. Counts one on each cycle when all of the following are true:<br>- No instruction is executed, see CPI Count register, DWT_CPICNT on page C1-801.<br>- No load-store operation is in progress, see LSU Count register, DWT_LSUCNT.<br>- No exception-entry or exception-exit operation is in progress, see Exception<br>Overhead Count register, DWT_EXCCNT on Arm TRM page C1-802.<br>- In a power saving mode.<br>Power saving modes include WFI, WFE, and Sleep on exit, see Power management on page B1-616. |

### 4.14.2.6 CM7_DWT_LSUCNT

**Description:** LSU Count register
**Address:** 0xE0001014
**Offset:** 0x14
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** The LSUCNT register characteristics are:
Purpose: Increments on the additional cycles required to execute all load or store instructions
Usage constraints: The counter initializes to 0 when software enables its counter overflow event by setting the CTRL.LSUEVTENA bit to 1.
Configurations:
Implemented only when CTRL.NOPRFCNT is RAZ, see Control register, CTRL on page C1-797.
If CTRL.NOPRFCNT is RAO, indicating that the implementation does not include the profiling counters, this register is UNK/SBZP.
Attributes: See Table C1-21 on Arm TRM page C1-797.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | LSUCNT [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | LSUCNT | RW | RW | 0 | Load-store overhead counter. Counts one on each cycle when all of the following are true:<br>- No instruction is executed, see CPI Count register, DWT_CPICNT on page C1-801.<br>- No exception-entry or exception-exit operation is in progress, see Exception Overhead Count register, DWT_EXCCNT on Arm TRM page C1-802.<br>- A load-store operation is in progress. |

### 4.14.2.7 CM7_DWT_FOLDCNT

**Description:** Folded-instruction Count register
**Address:** 0xE0001018
**Offset:** 0x18
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** The FOLDCNT register characteristics are:
Purpose: Increments on each instruction that takes 0 cycles.
Usage constraints:
- The counter initializes to 0 when software enables its counter overflow event by setting the CTRL.FOLDEVTENA bit to 1.
- If an implementation includes profiling counters but does not support instruction folding, this counter can be RAZ/WI.
Configurations:
Implemented only when CTRL.NOPRFCNT is RAZ, see Control register, CTRL on Arm TRM page C1-797.
If CTRL.NOPRFCNT is RAO, indicating that the implementation does not include the profiling counters, this register is UNK/SBZP.
Attributes: See Table C1-21 on page C1-797.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | FOLDCNT [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | FOLDCNT | RW | RW | 0 | Folded instruction counter. Counts on each cycle when atleast two instructions are executed. The counter is incremented by the number<br>of instructions executed, minus one.<br>At least one instruction is executed is the opposite of<br>No instruction is executed. See CPI Count register, DWT_CPICNT on Arm TRM page C1-801.<br>An event is emitted on counter overflow. Initialized to zero when DWT_CTRL.LSUEVTENA transitions from 0 to 1. |

### 4.14.2.8 CM7_DWT_PCSR

**Description:** Program Counter Sample Register
**Address:** 0xE000101C
**Offset:** 0x1C
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** The PCSR characteristics are:
Purpose: Samples the current value of the program counter.
Usage constraints: There are no usage constraints.
Note: Bit[0] of any sampled value is RAZ and does not reflect instruction set state as it does in a PC sample on the ARMv7-A and ARMv7-R architecture profiles.
Configurations: An optional feature. Register is RAZ/WI if not implemented.
Attributes: See Table C1-21 on Arm TRM page C1-797.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | EIASAMPLE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | EIASAMPLE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | EIASAMPLE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | EIASAMPLE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | EIASAMPLE | RW | RW | 0 | Executed Instruction Address sample value. |

### 4.14.2.9 CM7_DWT_COMP0

**Description:** Comparator registers
**Address:** 0xE0001020
**Offset:** 0x20
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** The COMPn register characteristics are:
Purpose: Provides a reference value for use by comparator n.
Usage constraints: The operation of comparator n depends also on the registers MASKn and FUNCTIONn, see Comparator Mask registers, MASKn and Comparator Function registers, FUNCTIONn on page C1-806.
Configurations:
Implemented only when CTRL.NUMCOMP is nonzero, see Control register, CTRL on page C1-797.
CTRL.NUMCOMP defines the number of implemented COMPn registers. Implemented COMPn registers number from 0 to (NUMCOMP-1). Unimplemented registers are UNK/SBZP.
Attributes: See Table C1-21 on Arm TRM page C1-797.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | COMP [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | COMP [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | COMP [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | COMP [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | COMP | RW | R | 0 | Reference value for comparison. |

### 4.14.2.10 CM7_DWT_MASK0

**Description:** Comparator Mask registers
**Address:** 0xE0001024
**Offset:** 0x24
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** The MASKn register characteristics are:
Purpose: Provides the size of the ignore mask applied to the access address for address range matching by comparator n.
Usage constraints: The operation of comparator n depends also on the registers COMPn and FUNCTIONn, see Comparator registers, COMPn and Comparator Function registers, FUNCTIONn on Arm TRM page C1-806.
Configurations:
Implemented only when CTRL.NUMCOMP is nonzero, see Control register, CTRL on Arm TRM page C1-797.
CTRL.NUMCOMP defines the number of implemented MASKn registers. Implemented MASKn registers number from 0 to (NUMCOMP-1). Unimplemented registers are UNK/SBZP.
Attributes: See Table C1-21 on Arm TRM page C1-797.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:5] | | | MASK [4:0] | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:4 | MASK | RW | R | 0 | The size of the ignore mask, 0-31 bits, applied to address range matching.<br>The maximum mask size is IMPLEMENTATION DEFINED. A debugger can write 0b11111 to this field and then read the register back to determine the maximum mask size supported. |

### 4.14.2.11 CM7_DWT_FUNCTION0

**Description:** Comparator Function registers
**Address:** 0xE0001028
**Offset:** 0x28
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** The FUNCTIONn register characteristics are:
Purpose: Controls the operation of comparator n.
Usage constraints:
The operation of comparator n depends also on the registers COMPn and MASKn, see Comparator registers, COMPn on Arm TRM page C1-805 and Comparator Mask registers, MASKn on Arm TRM page C1-805.
Reading this register clears some fields to zero. See the register field descriptions for more information, and for the usage constraints of individual fields.
Configurations:
Implemented only when CTRL.NUMCOMP is nonzero, see Control register, CTRL on Arm TRM page C1-797.
CTRL.NUMCOMP defines the number of implemented FUNCTIONn registers. Implemented FUNCTIONn registers number from 0 to (NUMCOMP-1). Unimplemented registers are UNK/SBZP.
Attributes: See Table C1-21 on Arm TRM page C1-797. See the register field descriptions for information about the values of the RO bits in the register.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | CYCMATCH [7:7] | None [6:6] | EMITRANGE [5:5] | None [4:4] | FUNCTION [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | DATAVADDR0 [15:12] | | | | DATAVSIZE [11:10] | | LNK1ENA [9:9] | DATAVMATCH [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:20] | | | | DATAVADDR1 [19:16] | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:25] | | | | | | | MATCHED [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | FUNCTION | RW | R | 0 | Selects action taken on comparator match:<br>0000 = Disabled or LinkAddr(), see LinkAddr support on Arm TRM page C1-789.<br>For non-zero values:<br>- If DATAVMATCH is set to 1, see Table C1-16 on Arm TRM page C1-786<br>- If DATAVMATCH is set to 0 then:<br>- If CYCMATCH is set to 0, see Table C1-14 on Arm TRM page C1-782<br>- If CYCMATCH is set to 1, see Table C1-15 on Arm TRM page C1-785.<br>This field resets to zero. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 5 | EMITRANGE | RW | R | 0 | If the implementation supports trace sampling, enables generation of Data trace address packets, that hold Daddr[15:0]:<br>0 Data trace address packets disabled.<br>1 Enable Data trace address packet generation.<br>For more information see Address comparison functions on Arm TRM page C1-781. If DWT_CTRL.NOTRCPKT is RAZ then this bit is UNK/SBZP. |
| 7 | CYCMATCH | RW | R | 0 | DWT_FUNCTION0 only.<br>If the implementation supports cycle counting, enable cycle count comparison for comparator 0:<br>0 No comparison is performed.<br>1 Compare DWT_COMP0 with the cycle counter, DWT_CYCCNT.<br>If DWT_CTRL.NOCYCCNT is RAZ then this bit is UNK/SBZP. |
| 8 | DATAVMATCH | RW | R | 0 | Enables data value comparison, if supported:<br>0 Perform address comparison.<br>1 Perform data value comparison.<br>For comparator 0, when the CYCMATCH is set to 1, DATAVMATCH must be set to 0 for it to perform cycle count comparison.<br>See LNK1ENA, DATAVSIZE, DATAVADDR0 and DATAVADDR1 for related information.<br>If the implementation does not support data value comparison this bit is RAZ/WI. |
| 9 | LNK1ENA | RW | R | 0 | Indicates whether the implementation supports use of a second linked comparator:<br>0 Second linked comparator not supported.<br>1 Second linked comparator supported.<br>When LNK1ENA is RAO, the DATAVADDR1 field specifies the comparator to use as the second linked comparator.<br>This bit is read-only |
| 10:11 | DATAVSIZE | RW | R | 0 | For data value matching, specifies the size of the required data comparison:<br>00 Byte.<br>01 Halfword.<br>10 Word.<br>The value 0b11 is reserved. Using this value means behavior is UNPREDICTABLE. |
| 12:15 | DATAVADDR0 | RW | R | 0 | When the DATAVMATCH bit is set to 1 this field can hold the comparator number of a comparator to use for linked address comparison. For more information see LinkAddr support on Arm TRM page C1-789.<br>The DWT unit ignores the value of this field if the DATAVMATCH bit is set to 0. |
| 16:19 | DATAVADDR1 | RW | R | 0 | When the DATAVMATCH and LNK1ENA bits are both 1, this field can hold the comparator number of a second comparator to use for linked address comparison. For more information see LinkAddr support on Arm TRM page C1-789.<br>The DWT unit ignores the value of this field unless the LNK1ENA bit is RAO and the DATAVMATCH bit is set to 1.<br>If LNK1ENA is RAZ, this field is RAZ/WI. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 24 | MATCHED | RW | R | 0 | Comparator match:<br>0 No match.<br>1 Match.<br>A value of 1 indicates that the operation defined by the FUNCTION field occurred since the last read of the register<br>Reading the register clears this bit to 0. This bit is read-only. |

### 4.14.2.12 CM7_DWT_COMP1

**Description:** Comparator registers
**Address:** 0xE0001030
**Offset:** 0x30
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** The COMPn register characteristics are:
Purpose: Provides a reference value for use by comparator n.
Usage constraints: The operation of comparator n depends also on the registers MASKn and FUNCTIONn, see Comparator Mask registers, MASKn and Comparator Function registers, FUNCTIONn on page C1-806.
Configurations:
Implemented only when CTRL.NUMCOMP is nonzero, see Control register, CTRL on page C1-797.
CTRL.NUMCOMP defines the number of implemented COMPn registers. Implemented COMPn registers number from 0 to (NUMCOMP-1). Unimplemented registers are UNK/SBZP.
Attributes: See Table C1-21 on Arm TRM page C1-797.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | COMP [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | COMP [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | COMP [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | COMP [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | COMP | RW | R | 0 | Reference value for comparison. |

### 4.14.2.13 CM7_DWT_MASK1

**Description:** Comparator Mask registers
**Address:** 0xE0001034
**Offset:** 0x34
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** The MASKn register characteristics are:
Purpose: Provides the size of the ignore mask applied to the access address for address range matching by comparator n.
Usage constraints: The operation of comparator n depends also on the registers COMPn and FUNCTIONn, see Comparator registers, COMPn and Comparator Function registers, FUNCTIONn on page C1-806.
Configurations:
Implemented only when CTRL.NUMCOMP is nonzero, see Control register, CTRL on page C1-797.
CTRL.NUMCOMP defines the number of implemented MASKn registers. Implemented MASKn registers number from 0 to (NUMCOMP-1). Unimplemented registers are UNK/SBZP.
Attributes: See Table C1-21 on Arm TRM page C1-797.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:5] | | | MASK [4:0] | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:4 | MASK | RW | R | 0 | The size of the ignore mask, 0-31 bits, applied to address range matching.<br>The maximum mask size is IMPLEMENTATION DEFINED. A debugger can write 0b11111 to this field and then read the register back to determine the maximum mask size supported. |

### 4.14.2.14 CM7_DWT_FUNCTION1

**Description:** Comparator Function registers
**Address:** 0xE0001038
**Offset:** 0x38
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** The FUNCTIONn register characteristics are:
Purpose: Controls the operation of comparator n.
Usage constraints:
The operation of comparator n depends also on the registers COMPn and MASKn, see Comparator registers, COMPn on Arm TRM page C1-805 and Comparator Mask registers, MASKn on page C1-805.
Reading this register clears some fields to zero. See the register field descriptions for more information, and for the usage constraints of individual fields.
Configurations:
Implemented only when CTRL.NUMCOMP is nonzero, see Control register, CTRL on Arm TRM page C1-797.
CTRL.NUMCOMP defines the number of implemented FUNCTIONn registers. Implemented FUNCTIONn registers number from 0 to (NUMCOMP-1). Unimplemented registers are UNK/SBZP.
Attributes: See Table C1-21 on Arm TRM page C1-797. See the register field descriptions for information about the values of the RO bits in the register.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | CYCMATCH [7:7] | None [6:6] | EMITRANGE [5:5] | None [4:4] | FUNCTION [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | DATAVADDR0 [15:12] | | | | DATAVSIZE [11:10] | | LNK1ENA [9:9] | DATAVMATCH [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:20] | | | | DATAVADDR1 [19:16] | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:25] | | | | | | | MATCHED [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | FUNCTION | RW | R | 0 | Selects action taken on comparator match:<br>0000 = Disabled or LinkAddr(), see LinkAddr support on Arm TRM page C1-789.<br>For non-zero values:<br>- If DATAVMATCH is set to 1, see Table C1-16 on Arm TRM page C1-786<br>- If DATAVMATCH is set to 0 then:<br>- If CYCMATCH is set to 0, see Table C1-14 on Arm TRM page C1-782<br>- If CYCMATCH is set to 1, see Table C1-15 on Arm TRM page C1-785.<br>This field resets to zero. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 5 | EMITRANGE | RW | R | 0 | If the implementation supports trace sampling, enables generation of Data trace address packets, that hold Daddr[15:0]:<br>0 Data trace address packets disabled.<br>1 Enable Data trace address packet generation.<br>For more information see Address comparison functions on Arm TRM page C1-781. If DWT_CTRL.NOTRCPKT is RAZ then this bit is UNK/SBZP. |
| 7 | CYCMATCH | RW | R | 0 | DWT_FUNCTION0 only.<br>If the implementation supports cycle counting, enable cycle count comparison for comparator 0:<br>0 No comparison is performed.<br>1 Compare DWT_COMP0 with the cycle counter, DWT_CYCCNT.<br>If DWT_CTRL.NOCYCCNT is RAZ then this bit is UNK/SBZP. |
| 8 | DATAVMATCH | RW | R | 0 | Enables data value comparison, if supported:<br>0 Perform address comparison.<br>1 Perform data value comparison.<br>For comparator 0, when the CYCMATCH is set to 1, DATAVMATCH must be set to 0 for it to perform cycle count comparison.<br>See LNK1ENA, DATAVSIZE, DATAVADDR0 and DATAVADDR1 for related information.<br>If the implementation does not support data value comparison this bit is RAZ/WI. |
| 9 | LNK1ENA | RW | R | 0 | Indicates whether the implementation supports use of a second linked comparator:<br>0 Second linked comparator not supported.<br>1 Second linked comparator supported.<br>When LNK1ENA is RAO, the DATAVADDR1 field specifies the comparator to use as the second linked comparator.<br>This bit is read-only |
| 10:11 | DATAVSIZE | RW | R | 0 | For data value matching, specifies the size of the required data comparison:<br>00 Byte.<br>01 Halfword.<br>10 Word.<br>The value 0b11 is reserved. Using this value means behavior is UNPREDICTABLE. |
| 12:15 | DATAVADDR0 | RW | R | 0 | When the DATAVMATCH bit is set to 1 this field can hold the comparator number of a comparator to use for linked address comparison. For more information see LinkAddr support on Arm TRM page C1-789.<br>The DWT unit ignores the value of this field if the DATAVMATCH bit is set to 0. |
| 16:19 | DATAVADDR1 | RW | R | 0 | When the DATAVMATCH and LNK1ENA bits are both 1, this field can hold the comparator number of a second comparator to use for linked address comparison. For more information see LinkAddr support on Arm TRM page C1-789.<br>The DWT unit ignores the value of this field unless the LNK1ENA bit is RAO and the DATAVMATCH bit is set to 1.<br>If LNK1ENA is RAZ, this field is RAZ/WI. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 24 | MATCHED | RW | R | 0 | Comparator match:<br>0 No match.<br>1 Match.<br>A value of 1 indicates that the operation defined by the FUNCTION field occurred since the last read of the register<br>Reading the register clears this bit to 0. This bit is read-only. |

### 4.14.2.15 CM7_DWT_COMP2

**Description:** Comparator registers
**Address:** 0xE0001040
**Offset:** 0x40
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** The COMPn register characteristics are:
Purpose: Provides a reference value for use by comparator n.
Usage constraints: The operation of comparator n depends also on the registers MASKn and FUNCTIONn, see Comparator Mask registers, MASKn and Comparator Function registers, FUNCTIONn on Arm TRM page C1-806.
Configurations:
Implemented only when CTRL.NUMCOMP is nonzero, see Control register, CTRL on Arm TRM page C1-797.
CTRL.NUMCOMP defines the number of implemented COMPn registers. Implemented COMPn registers number from 0 to (NUMCOMP-1). Unimplemented registers are UNK/SBZP.
Attributes: See Table C1-21 on Arm TRM page C1-797.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | COMP [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | COMP [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | COMP [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | COMP [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | COMP | RW | R | 0 | Reference value for comparison. |

### 4.14.2.16 CM7_DWT_MASK2

**Description:** Comparator Mask registers
**Address:** 0xE0001044
**Offset:** 0x44
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** The MASKn register characteristics are:
Purpose: Provides the size of the ignore mask applied to the access address for address range matching by comparator n.
Usage constraints: The operation of comparator n depends also on the registers COMPn and FUNCTIONn, see Comparator registers, COMPn and Comparator Function registers, FUNCTIONn on Arm TRM page C1-806.
Configurations:
Implemented only when CTRL.NUMCOMP is nonzero, see Control register, CTRL on Arm TRM page C1-797.
CTRL.NUMCOMP defines the number of implemented MASKn registers. Implemented MASKn registers number from 0 to (NUMCOMP-1). Unimplemented registers are UNK/SBZP.
Attributes: See Table C1-21 on Arm TRM page C1-797.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:5] | | | MASK [4:0] | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:4 | MASK | RW | R | 0 | The size of the ignore mask, 0-31 bits, applied to address range matching.<br>The maximum mask size is IMPLEMENTATION DEFINED. A debugger can write 0b11111 to this field and then read the register back to determine the maximum mask size supported. |

### 4.14.2.17 CM7_DWT_FUNCTION2

**Description:** Comparator Function registers
**Address:** 0xE0001048
**Offset:** 0x48
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** The FUNCTIONn register characteristics are:
Purpose: Controls the operation of comparator n.
Usage constraints:
The operation of comparator n depends also on the registers COMPn and MASKn, see Comparator registers, COMPn on Arm TRM page C1-805 and Comparator Mask registers, MASKn on Arm TRM page C1-805.
Reading this register clears some fields to zero. See the register field descriptions for more information, and for the usage constraints of individual fields.
Configurations:
Implemented only when CTRL.NUMCOMP is nonzero, see Control register, CTRL on Arm TRM page C1-797.
CTRL.NUMCOMP defines the number of implemented FUNCTIONn registers. Implemented FUNCTIONn registers number from 0 to (NUMCOMP-1). Unimplemented registers are UNK/SBZP.
Attributes: See Table C1-21 on Arm TRM page C1-797. See the register field descriptions for information about the values of the RO bits in the register.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | CYCMATCH [7:7] | None [6:6] | EMITRANGE [5:5] | None [4:4] | FUNCTION [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | DATAVADDR0 [15:12] | | | | DATAVSIZE [11:10] | | LNK1ENA [9:9] | DATAVMATCH [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:20] | | | | DATAVADDR1 [19:16] | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:25] | | | | | | | MATCHED [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | FUNCTION | RW | R | 0 | Selects action taken on comparator match:<br>0000 = Disabled or LinkAddr(), see LinkAddr support on Arm TRM page C1-789.<br>For non-zero values:<br>- If DATAVMATCH is set to 1, see Table C1-16 on Arm TRM page C1-786<br>- If DATAVMATCH is set to 0 then:<br>- If CYCMATCH is set to 0, see Table C1-14 on Arm TRM page C1-782<br>- If CYCMATCH is set to 1, see Table C1-15 on Arm TRM page C1-785.<br>This field resets to zero. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 5 | EMITRANGE | RW | R | 0 | If the implementation supports trace sampling, enables generation of Data trace address packets, that hold Daddr[15:0]:<br>0 Data trace address packets disabled.<br>1 Enable Data trace address packet generation.<br>For more information see Address comparison functions on Arm TRM page C1-781. If DWT_CTRL.NOTRCPKT is RAZ then this bit is UNK/SBZP. |
| 7 | CYCMATCH | RW | R | 0 | DWT_FUNCTION0 only.<br>If the implementation supports cycle counting, enable cycle count comparison for comparator 0:<br>0 No comparison is performed.<br>1 Compare DWT_COMP0 with the cycle counter, DWT_CYCCNT.<br>If DWT_CTRL.NOCYCCNT is RAZ then this bit is UNK/SBZP. |
| 8 | DATAVMATCH | RW | R | 0 | Enables data value comparison, if supported:<br>0 Perform address comparison.<br>1 Perform data value comparison.<br>For comparator 0, when the CYCMATCH is set to 1, DATAVMATCH must be set to 0 for it to perform cycle count comparison.<br>See LNK1ENA, DATAVSIZE, DATAVADDR0 and DATAVADDR1 for related information.<br>If the implementation does not support data value comparison this bit is RAZ/WI. |
| 9 | LNK1ENA | RW | R | 0 | Indicates whether the implementation supports use of a second linked comparator:<br>0 Second linked comparator not supported.<br>1 Second linked comparator supported.<br>When LNK1ENA is RAO, the DATAVADDR1 field specifies the comparator to use as the second linked comparator.<br>This bit is read-only |
| 10:11 | DATAVSIZE | RW | R | 0 | For data value matching, specifies the size of the required data comparison:<br>00 Byte.<br>01 Halfword.<br>10 Word.<br>The value 0b11 is reserved. Using this value means behavior is UNPREDICTABLE. |
| 12:15 | DATAVADDR0 | RW | R | 0 | When the DATAVMATCH bit is set to 1 this field can hold the comparator number of a comparator to use for linked address comparison. For more information see LinkAddr support on Arm TRM page C1-789.<br>The DWT unit ignores the value of this field if the DATAVMATCH bit is set to 0. |
| 16:19 | DATAVADDR1 | RW | R | 0 | When the DATAVMATCH and LNK1ENA bits are both 1, this field can hold the comparator number of a second comparator to use for linked address comparison. For more information see LinkAddr support on Arm TRM page C1-789.<br>The DWT unit ignores the value of this field unless the LNK1ENA bit is RAO and the DATAVMATCH bit is set to 1.<br>If LNK1ENA is RAZ, this field is RAZ/WI. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 24 | MATCHED | RW | R | 0 | Comparator match:<br>0 No match.<br>1 Match.<br>A value of 1 indicates that the operation defined by the FUNCTION field occurred since the last read of the register<br>Reading the register clears this bit to 0. This bit is read-only. |

### 4.14.2.18 CM7_DWT_COMP3

**Description:** Comparator registers
**Address:** 0xE0001050
**Offset:** 0x50
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** The COMPn register characteristics are:
Purpose: Provides a reference value for use by comparator n.
Usage constraints: The operation of comparator n depends also on the registers MASKn and FUNCTIONn, see Comparator Mask registers, MASKn and Comparator Function registers, FUNCTIONn on Arm TRM page C1-806.
Configurations:
Implemented only when CTRL.NUMCOMP is nonzero, see Control register, CTRL on Arm TRM page C1-797.
CTRL.NUMCOMP defines the number of implemented COMPn registers. Implemented COMPn registers number from 0 to (NUMCOMP-1). Unimplemented registers are UNK/SBZP.
Attributes: See Table C1-21 on Arm TRM page C1-797.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | COMP [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | COMP [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | COMP [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | COMP [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | COMP | RW | R | 0 | Reference value for comparison. |

### 4.14.2.19 CM7_DWT_MASK3

**Description:** Comparator Mask registers
**Address:** 0xE0001054
**Offset:** 0x54
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** The MASKn register characteristics are:
Purpose: Provides the size of the ignore mask applied to the access address for address range matching by comparator n.
Usage constraints: The operation of comparator n depends also on the registers COMPn and FUNCTIONn, see Comparator registers, COMPn and Comparator Function registers, FUNCTIONn on Arm TRM page C1-806.
Configurations:
Implemented only when CTRL.NUMCOMP is nonzero, see Control register, CTRL on Arm TRM page C1-797.
CTRL.NUMCOMP defines the number of implemented MASKn registers. Implemented MASKn registers number from 0 to (NUMCOMP-1). Unimplemented registers are UNK/SBZP.
Attributes: See Table C1-21 on Arm TRM page C1-797.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:5] | | | MASK [4:0] | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:4 | MASK | RW | R | 0 | The size of the ignore mask, 0-31 bits, applied to address range matching.<br>The maximum mask size is IMPLEMENTATION DEFINED. A debugger can write 0b11111 to this field and then read the register back to determine the maximum mask size supported. |

### 4.14.2.20 CM7_DWT_FUNCTION3

**Description:** Comparator Function registers
**Address:** 0xE0001058
**Offset:** 0x58
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** The FUNCTIONn register characteristics are:
Purpose: Controls the operation of comparator n.
Usage constraints:
The operation of comparator n depends also on the registers COMPn and MASKn, see Comparator registers, COMPn on Arm TRM page C1-805 and Comparator Mask registers, MASKn on Arm TRM page C1-805.
Reading this register clears some fields to zero. See the register field descriptions for more information, and for the usage constraints of individual fields.
Configurations:
Implemented only when CTRL.NUMCOMP is nonzero, see Control register, CTRL on Arm TRM page C1-797.
CTRL.NUMCOMP defines the number of implemented FUNCTIONn registers. Implemented FUNCTIONn registers number from 0 to (NUMCOMP-1). Unimplemented registers are UNK/SBZP.
Attributes: See Table C1-21 on Arm TRM page C1-797. See the register field descriptions for information about the values of the RO bits in the register.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | CYCMATCH [7:7] | None [6:6] | EMITRANGE [5:5] | None [4:4] | FUNCTION [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | DATAVADDR0 [15:12] | | | | DATAVSIZE [11:10] | | LNK1ENA [9:9] | DATAVMATCH [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:20] | | | | DATAVADDR1 [19:16] | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:25] | | | | | | | MATCHED [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | FUNCTION | RW | R | 0 | Selects action taken on comparator match:<br>0000 = Disabled or LinkAddr(), see LinkAddr support on Arm TRM page C1-789.<br>For non-zero values:<br>- If DATAVMATCH is set to 1, see Table C1-16 on Arm TRM page C1-786<br>- If DATAVMATCH is set to 0 then:<br>- If CYCMATCH is set to 0, see Table C1-14 on Arm TRM page C1-782<br>- If CYCMATCH is set to 1, see Table C1-15 on Arm TRM page C1-785.<br>This field resets to zero. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 5 | EMITRANGE | RW | R | 0 | If the implementation supports trace sampling, enables generation of Data trace address packets, that hold Daddr[15:0]:<br>0 Data trace address packets disabled.<br>1 Enable Data trace address packet generation.<br>For more information see Address comparison functions on Arm TRM page C1-781. If DWT_CTRL.NOTRCPKT is RAZ then this bit is UNK/SBZP. |
| 7 | CYCMATCH | RW | R | 0 | DWT_FUNCTION0 only.<br>If the implementation supports cycle counting, enable cycle count comparison for comparator 0:<br>0 No comparison is performed.<br>1 Compare DWT_COMP0 with the cycle counter, DWT_CYCCNT.<br>If DWT_CTRL.NOCYCCNT is RAZ then this bit is UNK/SBZP. |
| 8 | DATAVMATCH | RW | R | 0 | Enables data value comparison, if supported:<br>0 Perform address comparison.<br>1 Perform data value comparison.<br>For comparator 0, when the CYCMATCH is set to 1, DATAVMATCH must be set to 0 for it to perform cycle count comparison.<br>See LNK1ENA, DATAVSIZE, DATAVADDR0 and DATAVADDR1 for related information.<br>If the implementation does not support data value comparison this bit is RAZ/WI. |
| 9 | LNK1ENA | RW | R | 0 | Indicates whether the implementation supports use of a second linked comparator:<br>0 Second linked comparator not supported.<br>1 Second linked comparator supported.<br>When LNK1ENA is RAO, the DATAVADDR1 field specifies the comparator to use as the second linked comparator.<br>This bit is read-only |
| 10:11 | DATAVSIZE | RW | R | 0 | For data value matching, specifies the size of the required data comparison:<br>00 Byte.<br>01 Halfword.<br>10 Word.<br>The value 0b11 is reserved. Using this value means behavior is UNPREDICTABLE. |
| 12:15 | DATAVADDR0 | RW | R | 0 | When the DATAVMATCH bit is set to 1 this field can hold the comparator number of a comparator to use for linked address comparison. For more information see LinkAddr support on Arm TRM page C1-789.<br>The DWT unit ignores the value of this field if the DATAVMATCH bit is set to 0. |
| 16:19 | DATAVADDR1 | RW | R | 0 | When the DATAVMATCH and LNK1ENA bits are both 1, this field can hold the comparator number of a second comparator to use for linked address comparison. For more information see LinkAddr support on Arm TRM page C1-789.<br>The DWT unit ignores the value of this field unless the LNK1ENA bit is RAO and the DATAVMATCH bit is set to 1.<br>If LNK1ENA is RAZ, this field is RAZ/WI. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 24 | MATCHED | RW | R | 0 | Comparator match:<br>0 No match.<br>1 Match.<br>A value of 1 indicates that the operation defined by the FUNCTION field occurred since the last read of the register<br>Reading the register clears this bit to 0. This bit is read-only. |

### 4.14.2.21 CM7_DWT_LAR

**Description:** Lock Access Register
**Address:** 0xE0001FB0
**Offset:** 0xFB0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | W | R | 0 | N/A |

### 4.14.2.22 CM7_DWT_LSR

**Description:** Lock Status Register
**Address:** 0xE0001FB4
**Offset:** 0xFB4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 0 | N/A |

### 4.14.2.23 CM7_DWT_PID4

**Description:** Peripheral Identification Register 4.
**Address:** 0xE0001FD0
**Offset:** 0xFD0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x4

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 4 | N/A |

### 4.14.2.24 CM7_DWT_PID5

**Description:** Peripheral Identification Register 5.
**Address:** 0xE0001FD4
**Offset:** 0xFD4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 0 | N/A |

### 4.14.2.25 CM7_DWT_PID6

**Description:** Peripheral Identification Register 6.
**Address:** 0xE0001FD8
**Offset:** 0xFD8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 0 | N/A |

### 4.14.2.26 CM7_DWT_PID7

**Description:** Peripheral Identification Register 7.
**Address:** 0xE0001FDC
**Offset:** 0xFDC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 0 | N/A |

### 4.14.2.27 CM7_DWT_PID0

**Description:** Peripheral Identification Register 0.
**Address:** 0xE0001FE0
**Offset:** 0xFE0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x2

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 2 | N/A |

### 4.14.2.28 CM7_DWT_PID1

**Description:** Peripheral Identification Register 1.
**Address:** 0xE0001FE4
**Offset:** 0xFE4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xB0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 176 | N/A |

### 4.14.2.29 CM7_DWT_PID2

**Description:** Peripheral Identification Register 2.
**Address:** 0xE0001FE8
**Offset:** 0xFE8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xB

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 11 | N/A |

#### 4.14.2.30 CM7_DWT_PID3

**Description:** Peripheral Identification Register 3.
**Address:** 0xE0001FEC
**Offset:** 0xFEC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | ECOREVNUM [7:4] | | | | None [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 4:7 | ECOREVNUM | R | R | 0 | ECO revision |

### 4.14.2.31 CM7_DWT_CID0

**Description:** Component Identification Register 0.
**Address:** 0xE0001FF0
**Offset:** 0xFF0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xD

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 13 | N/A |

### 4.14.2.32 CM7_DWT_CID1

**Description:** Component Identification Register 1.
**Address:** 0xE0001FF4
**Offset:** 0xFF4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xE0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 224 | N/A |

### 4.14.2.33 CM7_DWT_CID2

**Description:** Component Identification Register 2.
**Address:** 0xE0001FF8
**Offset:** 0xFF8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x5

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 5 | N/A |

### 4.14.2.34 CM7_DWT_CID3

**Description:** Component Identification Register 3.
**Address:** 0xE0001FFC
**Offset:** 0xFFC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xB1

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 177 | N/A |

### 4.14.3 FPB

#### 4.14.3.1 CM7_FPB_CTRL

**Description:** FlashPatch Control Register
**Address:** 0xE0002000
**Offset:** 0x0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** The FP_CTRL Register characteristics are:
Purpose: Provides FPB implementation information, and the global enable for the FPB unit.
Usage constraints: There are no usage constraints.
Configurations: Always implemented.
Attributes: See Table C1-23.
**Default:** 0x260

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | NUM_CODE_LO [7:4] | | | | None [3:2] | | KEY [1:1] | ENABLE [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:15] | NUM_CODE_HI [14:12] | | | NUM_LIT [11:8] | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | REV [31:28] | | | | None [27:24] | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | ENABLE | RW | R | 0 | Enable bit for the FPB:<br>0 Flash Patch Breakpoint disabled.<br>1 Flash Patch Breakpoint enabled.<br>A Power-on reset clears this bit to 0. |
| 1 | KEY | RW | R | 0 | On any write to FP_CTRL, this bit must be 1. A write to the register with this bit set to zero is ignored. The Flash Patch Breakpoint unit ignores the write unless this bit is 1. This bit is RAZ. |
| 4:7 | NUM_CODE_LO | RW | R | 6 | The least significant bits, being bits[3:0], of NUM_CODE, the number of instruction address comparators.<br>If NUM_CODE[6:0] is zero, the implementation does not support any instruction address comparators.<br>These bits are read only. |
| 8:11 | NUM_LIT | RW | R | 2 | The number of literal address comparators supported, starting from NUM_CODE upwards. UNK/SBZP if Flash Patch is not implemented. Flash Patch is not implemented if<br>FP_REMAP[29] is 0.<br>If this field is zero, the implementation does not support literal comparators. These bits are read-only. |
| 12:14 | NUM_CODE_HI | RW | R | 0 | The most significant bits, being bits[6:4], of NUM_CODE, the number of instruction address comparators, see bits[7:4].<br>These bits are read only. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 28:31 | REV | RW | R | 0 | Flash Patch Breakpoint architecture revision: 0000 Flash Patch Breakpoint version 1.<br>0001 Flash Patch Breakpoint version 2. Supports breakpoints on any location in the 4GB address range. |

### 4.14.3.2 CM7_FPB_REMAP

**Description:** FlashPatch Remap register
**Address:** 0xE0002004
**Offset:** 0x4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** The FP_REMAP register characteristics are:
Purpose: Indicates whether the implementation supports flash patch remap, and if it does, holds the SRAM address for remap.
Usage constraints: There are no usage constraints.
Configurations: Not Implemented. RAZ/WI for CM7.
Attributes: See Table C1-23 on Arm TRM page C1-816.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | REMAP [7:5] | | | None [4:0] | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | REMAP [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | REMAP [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | RMPSPT [31:30] | | None [29:29] | REMAP [28:24] | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 5:28 | REMAP | RW | R | 0 | If the FPB supports flash patch remap, this field:<br>- Holds bits[28:5] of the base address in SRAM to which the FPB remaps the address.<br>- Has an UNKNOWN value on reset.<br>If the FPB only supports breakpoint functionality this field is UNK/SBZP. |
| 30:31 | RMPSPT | RW | R | 0 | Indicates whether the FPB unit supports flash patch remap:<br>0 Remapping not supported. The FPB only supports breakpoint functionality.<br>1 Hard-wired remap to SRAM region.<br>These bits are read only. |

### 4.14.3.3 CM7_FPB_COMP

**Description:** FlashPatch Comparator register
**Address:** 0xE0002008
**Offset:** 0x8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** The FP_COMPn register characteristics are:
Purpose:
Holds an address for comparison with addresses in the Code memory region, see The system address map on page B3-648. The effect of a match depends on whether the comparator is an instruction address comparator or a literal address comparator:
Instruction address comparators
Either:
- Defines an instruction address to remap to an address based on the address specified in the FP_REMAP register.
- Defines a breakpoint address.
Literal address comparators
Defines a literal address to remap to an address based on the address specified in the FP_REMAP register.
The FP_CTRL register determines which comparators are instruction address comparators and which are literal address comparators. The version of the FPB unit determines the bit assignment for the FP_COMP register. The FP_CTRL.REV field determines which version of the FPB unit is attached. See FlashPatch Control Register, FP_CTRL on page C1-816.
The FP_REMAP.RMPSPT field determines if the FPB unit supports Flash Patch. For more information about address remapping see FlashPatch Remap register, FP_REMAP on page C1-818.
If the FPB unit is configured for remap then FP_COMPn defines a 29-bit word-aligned address.
If the FPB unit is configured for breakpoints, version 1 defines a 29-bit word-aligned address and the breakpoint can be set on either or both half-words at this address. For version 2 FPB units configured for breakpoints, FP_COMPn defines a 32-bit half-word aligned address.
Usage constraints: To enable a comparator, both the FP_CTRL.ENABLE bit and the required FP_COMPn.ENABLE bit must be set to 1.
Configuration: Always implemented. see FlashPatch Control Register, FP_CTRL on Arm TRM page C1-816 for information about the number of implemented FlashPatch comparator registers.
Attributes: See Table C1-23 on Arm TRM page C1-816.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | See ARM documentation for details. |

### 4.14.3.4 CM7_FPB_LAR

**Description:** Lock Access Register
**Address:** 0xE0002FB0
**Offset:** 0xFB0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | W | R | 0 | N/A |

#### 4.14.3.5 CM7_FPB_LSR

**Description:** Lock Status Register
**Address:** 0xE0002FB4
**Offset:** 0xFB4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 0 | N/A |

### 4.14.3.6 CM7_FPB_PID4

**Description:** Peripheral Identification Register 4.
**Address:** 0xE0002FD0
**Offset:** 0xFD0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x4

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 4 | N/A |

### 4.14.3.7 CM7_FPB_PID5

**Description:** Peripheral Identification Register 5.
**Address:** 0xE0002FD4
**Offset:** 0xFD4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 0 | N/A |

### 4.14.3.8 CM7_FPB_PID6

**Description:** Peripheral Identification Register 6.
**Address:** 0xE0002FD8
**Offset:** 0xFD8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 0 | N/A |

### 4.14.3.9 CM7_FPB_PID7

**Description:** Peripheral Identification Register 7.
**Address:** 0xE0002FDC
**Offset:** 0xFDC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 0 | N/A |

### 4.14.3.10 CM7_FPB_PID0

**Description:** Peripheral Identification Register 0.
**Address:** 0xE0002FE0
**Offset:** 0xFE0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xE

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 14 | N/A |

### 4.14.3.11 CM7_FPB_PID1

**Description:** Peripheral Identification Register 1.
**Address:** 0xE0002FE4
**Offset:** 0xFE4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xB0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 176 | N/A |

### 4.14.3.12 CM7_FPB_PID2

**Description:** Peripheral Identification Register 2.
**Address:** 0xE0002FE8
**Offset:** 0xFE8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xB

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 11 | N/A |

### 4.14.3.13 CM7_FPB_PID3

**Description:** Peripheral Identification Register 3.
**Address:** 0xE0002FEC
**Offset:** 0xFEC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | ECOREVNUM [7:4] | | | | None [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 4:7 | ECOREVNUM | R | R | 0 | ECO revision |

### 4.14.3.14 CM7_FPB_CID0

**Description:** Component Identification Register 0.
**Address:** 0xE0002FF0
**Offset:** 0xFF0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xD

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 13 | N/A |

### 4.14.3.15 CM7_FPB_CID1

**Description:** Component Identification Register 1.
**Address:** 0xE0002FF4
**Offset:** 0xFF4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xE0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 224 | N/A |

### 4.14.3.16 CM7_FPB_CID2

**Description:** Component Identification Register 2.
**Address:** 0xE0002FF8
**Offset:** 0xFF8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x5

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 5 | N/A |

### 4.14.3.17 CM7_FPB_CID3

**Description:** Component Identification Register 3.
**Address:** 0xE0002FFC
**Offset:** 0xFFC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xB1

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 177 | N/A |

### 4.14.4 SCS

#### 4.14.4.1 CM7_SCS_ACTLR

**Description:** Auxiliary Control Register
**Address:** 0xE000E008
**Offset:** 0x8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer the following ARM documents for details about CPU register descriptions:<br>ARMV7M : http://infocenter.arm.com/help/index.jsp?topic=/com.arm.doc.ddi0403e.d/index.html<br>CM7 TRM: http://infocenter.arm.com/help/index.jsp?topic=/com.arm.doc.ddi0489f/index.html |

### 4.14.4.2 CM7_SCS_SYST_CSR

**Description:** SysTick Control and Status Register
**Address:** 0xE000E010
**Offset:** 0x10
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer ARMv7M architecture spec and CM7 TRM for description. See links in CM7_SCS.ACTLR description. |

### 4.14.4.3 CM7_SCS_SYST_RVR

**Description:** SysTick Reload Value Register
**Address:** 0xE000E014
**Offset:** 0x14
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer ARMv7M architecture spec and CM7 TRM for description. See links in CM7_SCS.ACTLR description. |

#### 4.14.4.4 CM7_SCS_SYST_CVR

**Description:** SysTick Current Value Register
**Address:** 0xE000E018
**Offset:** 0x18
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer ARMv7M architecture spec and CM7 TRM for description. See links in CM7_SCS.ACTLR description. |

### 4.14.4.5 CM7_SCS_SYST_CALIB

**Description:** SysTick Calibration value Register
**Address:** 0xE000E01C
**Offset:** 0x1C
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer ARMv7M architecture spec and CM7 TRM for description. See links in CM7_SCS.ACTLR description. |

### 4.14.4.6 CM7_SCS_NVIC_ISER

**Description:** Interrupt Set-Enable Registers
**Address:** 0xE000E100
**Offset:** 0x100
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer ARMv7M architecture spec and CM7 TRM for description. See links in CM7_SCS.ACTLR description. |

### 4.14.4.7 CM7_SCS_NVIC_ICER

**Description:** Interrupt Clear-Enable Registers
**Address:** 0xE000E180
**Offset:** 0x180
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer ARMv7M architecture spec and CM7 TRM for description. See links in CM7_SCS.ACTLR description. |

### 4.14.4.8 CM7_SCS_NVIC_ISPR

**Description:** Interrupt Set-Pending Registers
**Address:** 0xE000E200
**Offset:** 0x200
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer ARMv7M architecture spec and CM7 TRM for description. See links in CM7_SCS.ACTLR description. |

### 4.14.4.9 CM7_SCS_NVIC_ICPR

**Description:** Interrupt Clear-Pending Registers
**Address:** 0xE000E280
**Offset:** 0x280
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer ARMv7M architecture spec and CM7 TRM for description. See links in CM7_SCS.ACTLR description. |

### 4.14.4.10 CM7_SCS_NVIC_IABR

**Description:** Interrupt Active Bit Registers
**Address:** 0xE000E300
**Offset:** 0x300
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer ARMv7M architecture spec and CM7 TRM for description. See links in CM7_SCS.ACTLR description. |

### 4.14.4.11 CM7_SCS_NVIC_IPR

**Description:** Interrupt Priority Registers
**Address:** 0xE000E400
**Offset:** 0x400
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer ARMv7M architecture spec and CM7 TRM for description. See links in CM7_SCS.ACTLR description. |

### 4.14.4.12 CM7_SCS_CPUID

**Description:** CPUID Base Register
**Address:** 0xE000ED00
**Offset:** 0xD00
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer ARMv7M architecture spec and CM7 TRM for description. See links in CM7_SCS.ACTLR description. |

### 4.14.4.13 CM7_SCS_ICSR

**Description:** Interrupt Control and State Register
**Address:** 0xE000ED04
**Offset:** 0xD04
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer ARMv7M architecture spec and CM7 TRM for description. See links in CM7_SCS.ACTLR description. |

### 4.14.4.14 CM7_SCS_VTOR

**Description:** Vector Table Offset Register
**Address:** 0xE000ED08
**Offset:** 0xD08
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer ARMv7M architecture spec and CM7 TRM for description. See links in CM7_SCS.ACTLR description. |

### 4.14.4.15 CM7_SCS_AIRCR

**Description:** Application Interrupt and Reset Control Register
**Address:** 0xE000ED0C
**Offset:** 0xD0C
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer ARMv7M architecture spec and CM7 TRM for description. See links in CM7_SCS.ACTLR description. |

### 4.14.4.16 CM7_SCS_SCR

**Description:** System Control Register
**Address:** 0xE000ED10
**Offset:** 0xD10
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer ARMv7M architecture spec and CM7 TRM for description. See links in CM7_SCS.ACTLR description. |

### 4.14.4.17 CM7_SCS_CCR

**Description:** Configuration and Control Register
**Address:** 0xE000ED14
**Offset:** 0xD14
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer ARMv7M architecture spec and CM7 TRM for description. See links in CM7_SCS.ACTLR description. |

### 4.14.4.18 CM7_SCS_SHPR1

**Description:** System Handler Priority Register 1
**Address:** 0xE000ED18
**Offset:** 0xD18
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer ARMv7M architecture spec and CM7 TRM for description. See links in CM7_SCS.ACTLR description. |

### 4.14.4.19 CM7_SCS_SHPR2

**Description:** System Handler Priority Register 2
**Address:** 0xE000ED1C
**Offset:** 0xD1C
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer ARMv7M architecture spec and CM7 TRM for description. See links in CM7_SCS.ACTLR description. |

### 4.14.4.20 CM7_SCS_SHPR3

**Description:** System Handler Priority Register 3
**Address:** 0xE000ED20
**Offset:** 0xD20
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer ARMv7M architecture spec and CM7 TRM for description. See links in CM7_SCS.ACTLR description. |

### 4.14.4.21 CM7_SCS_SHCSR

**Description:** System Handler Control and State Register
**Address:** 0xE000ED24
**Offset:** 0xD24
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer ARMv7M architecture spec and CM7 TRM for description. See links in CM7_SCS.ACTLR description. |

### 4.14.4.22 CM7_SCS_CFSR

**Description:** Configurable Fault Status Register
**Address:** 0xE000ED28
**Offset:** 0xD28
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer ARMv7M architecture spec and CM7 TRM for description. See links in CM7_SCS.ACTLR description. |

### 4.14.4.23 CM7_SCS_HFSR

**Description:** HardFault Status Register
**Address:** 0xE000ED2C
**Offset:** 0xD2C
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer ARMv7M architecture spec and CM7 TRM for description. See links in CM7_SCS.ACTLR description. |

### 4.14.4.24 CM7_SCS_DFSR

**Description:** Debug Fault Status Register
**Address:** 0xE000ED30
**Offset:** 0xD30
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer ARMv7M architecture spec and CM7 TRM for description. See links in CM7_SCS.ACTLR description. |

### 4.14.4.25 CM7_SCS_MMFAR

**Description:** MemManage Fault Address Register
**Address:** 0xE000ED34
**Offset:** 0xD34
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer ARMv7M architecture spec and CM7 TRM for description. See links in CM7_SCS.ACTLR description. |

### 4.14.4.26 CM7_SCS_BFAR

**Description:** BusFault Address Register
**Address:** 0xE000ED38
**Offset:** 0xD38
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer ARMv7M architecture spec and CM7 TRM for description. See links in CM7_SCS.ACTLR description. |

### 4.14.4.27 CM7_SCS_ID_PFR0

**Description:** Processor Feature Register 0
**Address:** 0xE000ED40
**Offset:** 0xD40
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x30

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 48 | Refer ARMv7M architecture spec and CM7 TRM for description. See links in CM7_SCS.ACTLR description. |

### 4.14.4.28 CM7_SCS_ID_PFR1

**Description:** Processor Feature Register 1
**Address:** 0xE000ED44
**Offset:** 0xD44
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x200

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 512 | Refer ARMv7M architecture spec and CM7 TRM for description. See links in CM7_SCS.ACTLR description. |

### 4.14.4.29 CM7_SCS_ID_DFR0

**Description:** Debug Feature Register 0
**Address:** 0xE000ED48
**Offset:** 0xD48
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x100000

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 1048576 | Refer ARMv7M architecture spec and CM7 TRM for description. See links in CM7_SCS.ACTLR description. |

### 4.14.4.30 CM7_SCS_ID_AFR0

**Description:** Auxiliary Feature Register 0
**Address:** 0xE000ED4C
**Offset:** 0xD4C
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 0 | Refer ARMv7M architecture spec and CM7 TRM for description. See links in CM7_SCS.ACTLR description. |

### 4.14.4.31 CM7_SCS_ID_MMFR0

**Description:** Memory Model Feature Register 0
**Address:** 0xE000ED50
**Offset:** 0xD50
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x100030

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 1048624 | Reset value depends on ITCMSIZE and DTCMSIZE. Refer ARMv7M architecture spec and CM7 TRM for description. See links in CM7_SCS.ACTLR description. |

### 4.14.4.32 CM7_SCS_ID_MMFR1

**Description:** Memory Model Feature Register 1
**Address:** 0xE000ED54
**Offset:** 0xD54
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 0 | Refer ARMv7M architecture spec and CM7 TRM for description. See links in CM7_SCS.ACTLR description. |

### 4.14.4.33 CM7_SCS_ID_MMFR2

**Description:** Memory Model Feature Register 2
**Address:** 0xE000ED58
**Offset:** 0xD58
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x1000000

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 16777216 | Refer ARMv7M architecture spec and CM7 TRM for description. See links in CM7_SCS.ACTLR description. |

### 4.14.4.34 CM7_SCS_ID_MMFR3

**Description:** Memory Model Feature Register 3
**Address:** 0xE000ED5C
**Offset:** 0xD5C
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 0 | Refer ARMv7M architecture spec and CM7 TRM for description. See links in CM7_SCS.ACTLR description. |

### 4.14.4.35 CM7_SCS_ID_ISAR0

**Description:** Instruction Set Attributes Register 0
**Address:** 0xE000ED60
**Offset:** 0xD60
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x1101110

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 17830160 | Refer ARMv7M architecture spec and CM7 TRM for description. See links in CM7_SCS.ACTLR description. |

### 4.14.4.36 CM7_SCS_ID_ISAR1

**Description:** Instruction Set Attributes Register 1
**Address:** 0xE000ED64
**Offset:** 0xD64
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x2112000

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 34676736 | Refer ARMv7M architecture spec and CM7 TRM for description. See links in CM7_SCS.ACTLR description. |

### 4.14.4.37 CM7_SCS_ID_ISAR2

**Description:** Instruction Set Attributes Register 2
**Address:** 0xE000ED68
**Offset:** 0xD68
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x20232231

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 539173425 | Refer ARMv7M architecture spec and CM7 TRM for description. See links in CM7_SCS.ACTLR description. |

### 4.14.4.38 CM7_SCS_ID_ISAR3

**Description:** Instruction Set Attributes Register 3
**Address:** 0xE000ED6C
**Offset:** 0xD6C
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x1111131

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 17895729 | Refer ARMv7M architecture spec and CM7 TRM for description. See links in CM7_SCS.ACTLR description. |

### 4.14.4.39 CM7_SCS_ID_ISAR4

**Description:** Instruction Set Attributes Register 4
**Address:** 0xE000ED70
**Offset:** 0xD70
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x1310132

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 19988786 | Refer ARMv7M architecture spec and CM7 TRM for description. See links in CM7_SCS.ACTLR description. |

### 4.14.4.40 CM7_SCS_CLIDR

**Description:** Cache Level ID Register
**Address:** 0xE000ED78
**Offset:** 0xD78
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x9000003

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 150994947 | Value depends on cache implementation. Refer ARMv7M architecture spec and CM7 TRM for description. See links in CM7_SCS.ACTLR description. |

### 4.14.4.41 CM7_SCS_CTR

**Description:** Cache Type Register
**Address:** 0xE000ED7C
**Offset:** 0xD7C
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x8303C003

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 2198061059 | Refer ARMv7M architecture spec and CM7 TRM for description. See links in CM7_SCS.ACTLR description. |

### 4.14.4.42 CM7_SCS_CCSIDR

**Description:** Cache Size ID Register
**Address:** 0xE000ED80
**Offset:** 0xD80
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 0 | Refer ARMv7M architecture spec and CM7 TRM for description. See links in CM7_SCS.ACTLR description. |

### 4.14.4.43 CM7_SCS_CSSELR

**Description:** Cache Size Selection Register
**Address:** 0xE000ED84
**Offset:** 0xD84
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer ARMv7M architecture spec and CM7 TRM for description. See links in CM7_SCS.ACTLR description. |

### 4.14.4.44 CM7_SCS_CPACR

**Description:** Coprocessor Access Control Register
**Address:** 0xE000ED88
**Offset:** 0xD88
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer ARMv7M architecture spec and CM7 TRM for description. See links in CM7_SCS.ACTLR description. |

### 4.14.4.45 CM7_SCS_MPU_TYPE

**Description:** MPU Type Register
**Address:** 0xE000ED90
**Offset:** 0xD90
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer ARMv7M architecture spec and CM7 TRM for description. See links in CM7_SCS.ACTLR description. |

### 4.14.4.46 CM7_SCS_MPU_CTRL

**Description:** MPU Control Register
**Address:** 0xE000ED94
**Offset:** 0xD94
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer ARMv7M architecture spec and CM7 TRM for description. See links in CM7_SCS.ACTLR description. |

### 4.14.4.47 CM7_SCS_MPU_RNR

**Description:** MPU Region Number Register
**Address:** 0xE000ED98
**Offset:** 0xD98
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer ARMv7M architecture spec and CM7 TRM for description. See links in CM7_SCS.ACTLR description. |

### 4.14.4.48 CM7_SCS_MPU_RBAR

**Description:** MPU Region Base Address Register
**Address:** 0xE000ED9C
**Offset:** 0xD9C
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer ARMv7M architecture spec and CM7 TRM for description. See links in CM7_SCS.ACTLR description. |

### 4.14.4.49 CM7_SCS_MPU_RASR

**Description:** MPU Region Attribute and Size Register
**Address:** 0xE000EDA0
**Offset:** 0xDA0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer ARMv7M architecture spec and CM7 TRM for description. See links in CM7_SCS.ACTLR description. |

### 4.14.4.50 CM7_SCS_MPU_RBAR_A1

**Description:** MPU alias registers
**Address:** 0xE000EDA4
**Offset:** 0xDA4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer ARMv7M architecture spec and CM7 TRM for description. See links in CM7_SCS.ACTLR description. |

### 4.14.4.51 CM7_SCS_MPU_RASR_A1

**Description:** MPU alias registers
**Address:** 0xE000EDA8
**Offset:** 0xDA8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer ARMv7M architecture spec and CM7 TRM for description. See links in CM7_SCS.ACTLR description. |

### 4.14.4.52 CM7_SCS_MPU_RBAR_A2

**Description:** MPU alias registers
**Address:** 0xE000EDAC
**Offset:** 0xDAC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer ARMv7M architecture spec and CM7 TRM for description. See links in CM7_SCS.ACTLR description. |

### 4.14.4.53 CM7_SCS_MPU_RASR_A2

**Description:** MPU alias registers
**Address:** 0xE000EDB0
**Offset:** 0xDB0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer ARMv7M architecture spec and CM7 TRM for description. See links in CM7_SCS.ACTLR description. |

### 4.14.4.54 CM7_SCS_MPU_RBAR_A3

**Description:** MPU alias registers
**Address:** 0xE000EDB4
**Offset:** 0xDB4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer ARMv7M architecture spec and CM7 TRM for description. See links in CM7_SCS.ACTLR description. |

### 4.14.4.55 CM7_SCS_MPU_RASR_A3

**Description:** MPU alias registers
**Address:** 0xE000EDB8
**Offset:** 0xDB8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer ARMv7M architecture spec and CM7 TRM for description. See links in CM7_SCS.ACTLR description. |

### 4.14.4.56 CM7_SCS_DHCSR

**Description:** Debug Halting Control and Status Register
**Address:** 0xE000EDF0
**Offset:** 0xDF0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer ARMv7M architecture spec and CM7 TRM for description. See links in CM7_SCS.ACTLR description. |

### 4.14.4.57 CM7_SCS_DCRSR

**Description:** Debug Core Register Selector Register
**Address:** 0xE000EDF4
**Offset:** 0xDF4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer ARMv7M architecture spec and CM7 TRM for description. See links in CM7_SCS.ACTLR description. |

### 4.14.4.58 CM7_SCS_DCRDR

**Description:** Debug Core Register Data Register
**Address:** 0xE000EDF8
**Offset:** 0xDF8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer ARMv7M architecture spec and CM7 TRM for description. See links in CM7_SCS.ACTLR description. |

### 4.14.4.59 CM7_SCS_DEMCR

**Description:** Debug Exception and Monitor Control Register
**Address:** 0xE000EDFC
**Offset:** 0xDFC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer ARMv7M architecture spec and CM7 TRM for description. See links in CM7_SCS.ACTLR description. |

### 4.14.4.60 CM7_SCS_STIR

**Description:** Software Triggered Interrupt Register
**Address:** 0xE000EF00
**Offset:** 0xF00
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer ARMv7M architecture spec and CM7 TRM for description. See links in CM7_SCS.ACTLR description. |

### 4.14.4.61 CM7_SCS_FPCCR

**Description:** FP Context Control Register
**Address:** 0xE000EF34
**Offset:** 0xF34
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer ARMv7M architecture spec and CM7 TRM for description. See links in CM7_SCS.ACTLR description. |

### 4.14.4.62 CM7_SCS_FPCAR

**Description:** FP Context Control Register
**Address:** 0xE000EF38
**Offset:** 0xF38
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer ARMv7M architecture spec and CM7 TRM for description. See links in CM7_SCS.ACTLR description. |

### 4.14.4.63 CM7_SCS_FPDSCR

**Description:** FP Context Control Register
**Address:** 0xE000EF3C
**Offset:** 0xF3C
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer ARMv7M architecture spec and CM7 TRM for description. See links in CM7_SCS.ACTLR description. |

### 4.14.4.64 CM7_SCS_MVFR0

**Description:** Media and VFP Feature Register 0
**Address:** 0xE000EF40
**Offset:** 0xF40
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x10110221

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 269550113 | 0x10110221 for Double Precision FPU;<br>0x10110021 for Single Precision FPU. |

### 4.14.4.65 CM7_SCS_MVFR1

**Description:** Media and VFP Feature Register 1
**Address:** 0xE000EF44
**Offset:** 0xF44
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x12000011

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 301989905 | 0x12000011 for Double Precision FPU;<br>0x11000011 for Single Precision FPU. |

### 4.14.4.66 CM7_SCS_MVFR2

**Description:** Media and VFP Feature Register 2
**Address:** 0xE000EF48
**Offset:** 0xF48
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x40

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 64 | Refer ARMv7M architecture spec and CM7 TRM for description. See links in CM7_SCS.ACTLR description. |

### 4.14.4.67 CM7_SCS_ICIALLU

**Description:** Instruction cache invalidate all to Point of Unification (PoU)
**Address:** 0xE000EF50
**Offset:** 0xF50
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** Undefined as one or more bit fields have a default value that is undefined

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | W | R | Undefined | Refer ARMv7M architecture spec and CM7 TRM for description. See links in CM7_SCS.ACTLR description. |

### 4.14.4.68 CM7_SCS_ICIMVAU

**Description:** Instruction cache invalidate by address to PoU
**Address:** 0xE000EF58
**Offset:** 0xF58
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** Undefined as one or more bit fields have a default value that is undefined

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | W | R | Undefined | Refer ARMv7M architecture spec and CM7 TRM for description. See links in CM7_SCS.ACTLR description. |

### 4.14.4.69 CM7_SCS_DCIMVAC

**Description:** Data cache invalidate by address to Point of Coherency (PoC)
**Address:** 0xE000EF5C
**Offset:** 0xF5C
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** Undefined as one or more bit fields have a default value that is undefined

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | W | R | Undefined | Refer ARMv7M architecture spec and CM7 TRM for description. See links in CM7_SCS.ACTLR description. |

### 4.14.4.70 CM7_SCS_DCISW

**Description:** Data cache invalidate by set/way
**Address:** 0xE000EF60
**Offset:** 0xF60
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** Undefined as one or more bit fields have a default value that is undefined

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | W | R | Undefined | Refer ARMv7M architecture spec and CM7 TRM for description. See links in CM7_SCS.ACTLR description. |

### 4.14.4.71 CM7_SCS_DCCMVAU

**Description:** Data cache by address to PoU
**Address:** 0xE000EF64
**Offset:** 0xF64
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** Undefined as one or more bit fields have a default value that is undefined

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | W | R | Undefined | Refer ARMv7M architecture spec and CM7 TRM for description. See links in CM7_SCS.ACTLR description. |

### 4.14.4.72 CM7_SCS_DCCMVAC

**Description:** Data cache clean by address to PoU
**Address:** 0xE000EF68
**Offset:** 0xF68
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** Undefined as one or more bit fields have a default value that is undefined

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | W | R | Undefined | Refer ARMv7M architecture spec and CM7 TRM for description. See links in CM7_SCS.ACTLR description. |

### 4.14.4.73 CM7_SCS_DCCSW

**Description:** Data cache clean by set/way
**Address:** 0xE000EF6C
**Offset:** 0xF6C
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** Undefined as one or more bit fields have a default value that is undefined

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | W | R | Undefined | Refer ARMv7M architecture spec and CM7 TRM for description. See links in CM7_SCS.ACTLR description. |

### 4.14.4.74 CM7_SCS_DCCIMVAC

**Description:** Data cache clean and invalidate by address to PoC
**Address:** 0xE000EF70
**Offset:** 0xF70
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** Undefined as one or more bit fields have a default value that is undefined

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | W | R | Undefined | Refer ARMv7M architecture spec and CM7 TRM for description. See links in CM7_SCS.ACTLR description. |

### 4.14.4.75 CM7_SCS_DCCISW

**Description:** Data cache clean and invalidate by set/way
**Address:** 0xE000EF74
**Offset:** 0xF74
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** Undefined as one or more bit fields have a default value that is undefined

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | W | R | Undefined | Refer ARMv7M architecture spec and CM7 TRM for description. See links in CM7_SCS.ACTLR description. |

### 4.14.4.76 CM7_SCS_CM7_ITCMCR

**Description:** Instruction Tightly Coupled Memory Control Register
**Address:** 0xE000EF90
**Offset:** 0xF90
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer ARMv7M architecture spec and CM7 TRM for description. See links in CM7_SCS.ACTLR description. |

### 4.14.4.77 CM7_SCS_CM7_DTCMCR

**Description:** Data Tightly Coupled Memory Control Register
**Address:** 0xE000EF94
**Offset:** 0xF94
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer ARMv7M architecture spec and CM7 TRM for description. See links in CM7_SCS.ACTLR description. |

### 4.14.4.78 CM7_SCS_CM7_AHBPCR

**Description:** AHBP Control Register
**Address:** 0xE000EF98
**Offset:** 0xF98
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer ARMv7M architecture spec and CM7 TRM for description. See links in CM7_SCS.ACTLR description. |

### 4.14.4.79 CM7_SCS_CM7_CACR

**Description:** L1 Cache Control Register
**Address:** 0xE000EF9C
**Offset:** 0xF9C
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer ARMv7M architecture spec and CM7 TRM for description. See links in CM7_SCS.ACTLR description. |

### 4.14.4.80 CM7_SCS_CM7_AHBSCR

**Description:** AHB Slave Control Register
**Address:** 0xE000EFA0
**Offset:** 0xFA0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer ARMv7M architecture spec and CM7 TRM for description. See links in CM7_SCS.ACTLR description. |

### 4.14.4.81 CM7_SCS_CM7_ABFSR

**Description:** Auxiliary Bus Fault Status Register
**Address:** 0xE000EFA8
**Offset:** 0xFA8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer ARMv7M architecture spec and CM7 TRM for description. See links in CM7_SCS.ACTLR description. |

### 4.14.4.82 CM7_SCS_IEBR0

**Description:** Instruction Error bank Register 0
**Address:** 0xE000EFB0
**Offset:** 0xFB0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer ARMv7M architecture spec and CM7 TRM for description. See links in CM7_SCS.ACTLR description. |

### 4.14.4.83 CM7_SCS_IEBR1

**Description:** Instruction Error bank Register 1
**Address:** 0xE000EFB4
**Offset:** 0xFB4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer ARMv7M architecture spec and CM7 TRM for description. See links in CM7_SCS.ACTLR description. |

### 4.14.4.84 CM7_SCS_DEBR0

**Description:** Data Error Bank Register 0
**Address:** 0xE000EFB8
**Offset:** 0xFB8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer ARMv7M architecture spec and CM7 TRM for description. See links in CM7_SCS.ACTLR description. |

### 4.14.4.85 CM7_SCS_DEBR1

**Description:** Data Error Bank Register 1
**Address:** 0xE000EFBC
**Offset:** 0xFBC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer ARMv7M architecture spec and CM7 TRM for description. See links in CM7_SCS.ACTLR description. |

### 4.14.4.86 CM7_SCS_PID4

**Description:** Peripheral Identification Register 4
**Address:** 0xE000EFD0
**Offset:** 0xFD0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x4

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 4 | N/A |

### 4.14.4.87 CM7_SCS_PID5

**Description:** Peripheral Identification Register 5
**Address:** 0xE000EFD4
**Offset:** 0xFD4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 0 | N/A |

### 4.14.4.88 CM7_SCS_PID6

**Description:** Peripheral Identification Register 6
**Address:** 0xE000EFD8
**Offset:** 0xFD8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 0 | N/A |

### 4.14.4.89 CM7_SCS_PID7

**Description:** Peripheral Identification Register 7
**Address:** 0xE000EFDC
**Offset:** 0xFDC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 0 | N/A |

### 4.14.4.90 CM7_SCS_PID0

**Description:** Peripheral Identification Register 0
**Address:** 0xE000EFE0
**Offset:** 0xFE0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xC

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 12 | Table 9-5 of CM7 TRM.<br>It states 0x0000000C is identification value for implementations without FPU. What is it with FPU? |

### 4.14.4.91 CM7_SCS_PID1

**Description:** Peripheral Identification Register 1
**Address:** 0xE000EFE4
**Offset:** 0xFE4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xB0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 176 | N/A |

### 4.14.4.92 CM7_SCS_PID2

**Description:** Peripheral Identification Register 2
**Address:** 0xE000EFE8
**Offset:** 0xFE8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xB

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 11 | N/A |

### 4.14.4.93 CM7_SCS_PID3

**Description:** Peripheral Identification Register 3
**Address:** 0xE000EFEC
**Offset:** 0xFEC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | ECOREVNUM [7:4] | | | | None [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 4:7 | ECOREVNUM | R | R | 0 | N/A |

### 4.14.4.94 CM7_SCS_CID0

**Description:** Component Identification Register 0
**Address:** 0xE000EFF0
**Offset:** 0xFF0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xD

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 13 | N/A |

### 4.14.4.95 CM7_SCS_CID1

**Description:** Component Identification Register 1
**Address:** 0xE000EFF4
**Offset:** 0xFF4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xE0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 224 | N/A |

### 4.14.4.96 CM7_SCS_CID2

**Description:** Component Identification Register 2
**Address:** 0xE000EFF8
**Offset:** 0xFF8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x5

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 5 | N/A |

### 4.14.4.97 CM7_SCS_CID3

**Description:** Component Identification Register 3
**Address:** 0xE000EFFC
**Offset:** 0xFFC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xB1

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 177 | N/A |

### 4.14.5 ETM

#### 4.14.5.1 CM7_ETM_TRCPRGCTLR

**Description:** Programming Control Register
**Address:** 0xE0041004
**Offset:** 0x4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer the following ARM CM7 ETM TRM for register description:<br>http://infocenter.arm.com/help/index.jsp?topic=/com.arm.doc.ddi0494d/index.html |

### 4.14.5.2 CM7_ETM_TRCSTATR

**Description:** Status Register
**Address:** 0xE004100C
**Offset:** 0xC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 0 | N/A |

### 4.14.5.3 CM7_ETM_TRCCONFIGR

**Description:** Trace Configuration Register
**Address:** 0xE0041010
**Offset:** 0x10
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer ARM documentation. See links in CM7_ETM_TRCPRGCTLR. |

### 4.14.5.4 CM7_ETM_TRCEVENTCTL0R

**Description:** Event Control 0 Register
**Address:** 0xE0041020
**Offset:** 0x20
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer ARM documentation. See links in CM7_ETM_TRCPRGCTLR. |

### 4.14.5.5 CM7_ETM_TRCEVENTCTL1R

**Description:** Event Control 1 Register
**Address:** 0xE0041024
**Offset:** 0x24
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer ARM documentation. See links in CM7_ETM_TRCPRGCTLR. |

### 4.14.5.6 CM7_ETM_TRCSTALLCTLR

**Description:** Stall Control Register
**Address:** 0xE004102C
**Offset:** 0x2C
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer ARM documentation. See links in CM7_ETM_TRCPRGCTLR. |

### 4.14.5.7 CM7_ETM_TRCTSCTLR

**Description:** Global Timestamp Control Register
**Address:** 0xE0041030
**Offset:** 0x30
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer ARM documentation. See links in CM7_ETM_TRCPRGCTLR. |

### 4.14.5.8 CM7_ETM_TRCSYNCPR

**Description:** Synchronization Period Register
**Address:** 0xE0041034
**Offset:** 0x34
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xA

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 10 | Refer ARM documentation. See links in CM7_ETM_TRCPRGCTLR. |

### 4.14.5.9 CM7_ETM_TRCCCCTLR

**Description:** Cycle Count Control Register
**Address:** 0xE0041038
**Offset:** 0x38
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer ARM documentation. See links in CM7_ETM_TRCPRGCTLR. |

### 4.14.5.10 CM7_ETM_TRCTRACEIDR

**Description:** Trace ID Register
**Address:** 0xE0041040
**Offset:** 0x40
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer ARM documentation. See links in CM7_ETM_TRCPRGCTLR. |

### 4.14.5.11 CM7_ETM_TRCVICTLR

**Description:** ViewInst Main Control Register
**Address:** 0xE0041080
**Offset:** 0x80
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer ARM documentation. See links in CM7_ETM_TRCPRGCTLR. |

### 4.14.5.12 CM7_ETM_TRCVIPCSSCTLR

**Description:** ViewInst Start-Stop Processor Comparator Control Register
**Address:** 0xE004108C
**Offset:** 0x8C
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer ARM documentation. See links in CM7_ETM_TRCPRGCTLR. |

### 4.14.5.13 CM7_ETM_TRCCNTRLDVR

**Description:** Counter Reload Valkue Registers
**Address:** 0xE0041140
**Offset:** 0x140
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer ARM documentation. See links in CM7_ETM_TRCPRGCTLR. |

### 4.14.5.14 CM7_ETM_TRCIDR8

**Description:** ID Register 8
**Address:** 0xE0041180
**Offset:** 0x180
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x1

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 1 | Refer ARM documentation. See links in CM7_ETM_TRCPRGCTLR. |

### 4.14.5.15 CM7_ETM_TRCIDR9

**Description:** ID Register 9
**Address:** 0xE0041184
**Offset:** 0x184
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 0 | Refer ARM documentation. See links in CM7_ETM_TRCPRGCTLR. |

### 4.14.5.16 CM7_ETM_TRCIDR10

**Description:** ID Register 10
**Address:** 0xE0041188
**Offset:** 0x188
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 0 | Refer ARM documentation. See links in CM7_ETM_TRCPRGCTLR. |

### 4.14.5.17 CM7_ETM_TRCIDR11

**Description:** ID Register 11
**Address:** 0xE004118C
**Offset:** 0x18C
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 0 | Refer ARM documentation. See links in CM7_ETM_TRCPRGCTLR. |

### 4.14.5.18 CM7_ETM_TRCIDR12

**Description:** ID Register 12
**Address:** 0xE0041190
**Offset:** 0x190
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x1

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 1 | Refer ARM documentation. See links in CM7_ETM_TRCPRGCTLR. |

### 4.14.5.19 CM7_ETM_TRCIDR13

**Description:** ID Register 13
**Address:** 0xE0041194
**Offset:** 0x194
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 0 | Refer ARM documentation. See links in CM7_ETM_TRCPRGCTLR. |

### 4.14.5.20 CM7_ETM_TRCIMPSPEC0

**Description:** Implementation Specific Register 0
**Address:** 0xE00411C0
**Offset:** 0x1C0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer ARM documentation. See links in CM7_ETM_TRCPRGCTLR. |

### 4.14.5.21 CM7_ETM_TRCIDR0

**Description:** ID Register 0
**Address:** 0xE00411E0
**Offset:** 0x1E0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xC000EE1

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 201330401 | Refer ARM documentation. See links in CM7_ETM_TRCPRGCTLR. |

### 4.14.5.22 CM7_ETM_TRCIDR1

**Description:** ID Register 1
**Address:** 0xE00411E4
**Offset:** 0x1E4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x4100F401

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 1090581505 | Refer ARM documentation. See links in CM7_ETM_TRCPRGCTLR. |

### 4.14.5.23 CM7_ETM_TRCIDR2

**Description:** ID Register 2
**Address:** 0xE00411E8
**Offset:** 0x1E8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x4

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 4 | Refer ARM documentation. See links in CM7_ETM_TRCPRGCTLR. |

### 4.14.5.24 CM7_ETM_TRCIDR3

**Description:** ID Register 3
**Address:** 0xE00411EC
**Offset:** 0x1EC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x37090004

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 923336708 | Refer ARM documentation. See links in CM7_ETM_TRCPRGCTLR. |

### 4.14.5.25 CM7_ETM_TRCIDR4

**Description:** ID Register 4
**Address:** 0xE00411F0
**Offset:** 0x1F0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x114000

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 1130496 | Refer ARM documentation. See links in CM7_ETM_TRCPRGCTLR. |

### 4.14.5.26 CM7_ETM_TRCIDR5

**Description:** ID Register 5
**Address:** 0xE00411F4
**Offset:** 0x1F4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x90C70002

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 2428960770 | Refer ARM documentation. See links in CM7_ETM_TRCPRGCTLR. |

### 4.14.5.27 CM7_ETM_TRCRSCTLR2

**Description:** Resource Selection Register 2
**Address:** 0xE0041208
**Offset:** 0x208
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer ARM documentation. See links in CM7_ETM_TRCPRGCTLR. |

### 4.14.5.28 CM7_ETM_TRCRSCTLR3

**Description:** Resource Selection Register 3
**Address:** 0xE004120C
**Offset:** 0x20C
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer ARM documentation. See links in CM7_ETM_TRCPRGCTLR. |

### 4.14.5.29 CM7_ETM_TRCSSCCR0

**Description:** Single-shot Comparator Control Register0
**Address:** 0xE0041280
**Offset:** 0x280
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer ARM documentation. See links in CM7_ETM_TRCPRGCTLR. |

### 4.14.5.30 CM7_ETM_TRCSSCSR0

**Description:** Single-shot Comparator Status Register 0
**Address:** 0xE00412A0
**Offset:** 0x2A0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer ARM documentation. See links in CM7_ETM_TRCPRGCTLR. |

### 4.14.5.31 CM7_ETM_TRCSSPCICR0

**Description:** Single-shot Comparator Status Register 0
**Address:** 0xE00412C0
**Offset:** 0x2C0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer ARM documentation. See links in CM7_ETM_TRCPRGCTLR. |

### 4.14.5.32 CM7_ETM_TRCOSLSR

**Description:** OS Lock Status Register
**Address:** 0xE0041304
**Offset:** 0x304
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 0 | Refer ARM documentation. See links in CM7_ETM_TRCPRGCTLR. |

### 4.14.5.33 CM7_ETM_TRCPDCR

**Description:** Power Down Control Register
**Address:** 0xE0041310
**Offset:** 0x310
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer ARM documentation. See links in CM7_ETM_TRCPRGCTLR. |

### 4.14.5.34 CM7_ETM_TRCPDSR

**Description:** Power Down Status Register
**Address:** 0xE0041314
**Offset:** 0x314
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x3

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 3 | Refer ARM documentation. See links in CM7_ETM_TRCPRGCTLR. |

### 4.14.5.35 CM7_ETM_TRCITMISCOUTR

**Description:** Integration Miscellaneous Outputs Register
**Address:** 0xE0041EDC
**Offset:** 0xEDC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | W | R | 0 | Refer ARM documentation. See links in CM7_ETM_TRCPRGCTLR. |

### 4.14.5.36 CM7_ETM_TRCITMISCINR

**Description:** Integration Miscellaneous Inputs Register
**Address:** 0xE0041EE0
**Offset:** 0xEE0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 0 | Refer ARM documentation. See links in CM7_ETM_TRCPRGCTLR. |

### 4.14.5.37 CM7_ETM_TRCITATBIDR

**Description:** Integration ATB Identification Register
**Address:** 0xE0041EE4
**Offset:** 0xEE4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | W | R | 0 | Refer ARM documentation. See links in CM7_ETM_TRCPRGCTLR. |

### 4.14.5.38 CM7_ETM_TRCITDDATAR

**Description:** Integration Data ATB Data Register
**Address:** 0xE0041EE8
**Offset:** 0xEE8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | W | R | 0 | Refer ARM documentation. See links in CM7_ETM_TRCPRGCTLR. |

### 4.14.5.39 CM7_ETM_TRCITIDATAR

**Description:** Integration Instruction ATB Data Register
**Address:** 0xE0041EEC
**Offset:** 0xEEC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | W | R | 0 | Refer ARM documentation. See links in CM7_ETM_TRCPRGCTLR. |

### 4.14.5.40 CM7_ETM_TRCITDATBINR

**Description:** Integration Data ATB In Register
**Address:** 0xE0041EF0
**Offset:** 0xEF0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 0 | Refer ARM documentation. See links in CM7_ETM_TRCPRGCTLR. |

### 4.14.5.41 CM7_ETM_TRCITIATBINR

**Description:** Integration Instruction ATB In Register
**Address:** 0xE0041EF4
**Offset:** 0xEF4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 0 | Refer ARM documentation. See links in CM7_ETM_TRCPRGCTLR. |

### 4.14.5.42 CM7_ETM_TRCITDATBOUTR

**Description:** Integration Data ATB Out Register
**Address:** 0xE0041EF8
**Offset:** 0xEF8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | W | R | 0 | Refer ARM documentation. See links in CM7_ETM_TRCPRGCTLR. |

### 4.14.5.43 CM7_ETM_TRCITIATBOUTR

**Description:** Integration Instruction ATB Out Register
**Address:** 0xE0041EFC
**Offset:** 0xEFC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | W | R | 0 | Refer ARM documentation. See links in CM7_ETM_TRCPRGCTLR. |

### 4.14.5.44 CM7_ETM_TRCITCTRL

**Description:** Integration Mode Control Register
**Address:** 0xE0041F00
**Offset:** 0xF00
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer ARM documentation. See links in CM7_ETM_TRCPRGCTLR. |

### 4.14.5.45 CM7_ETM_TRCCLAIMSET

**Description:** Claim Tag Set Register
**Address:** 0xE0041FA0
**Offset:** 0xFA0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x4

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 4 | Refer ARM documentation. See links in CM7_ETM_TRCPRGCTLR. |

### 4.14.5.46 CM7_ETM_TRCCLAIMCLR

**Description:** Claim Tag Clear Register
**Address:** 0xE0041FA4
**Offset:** 0xFA4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer ARM documentation. See links in CM7_ETM_TRCPRGCTLR. |

### 4.14.5.47 CM7_ETM_TRCLAR

**Description:** Software Lock Access Register
**Address:** 0xE0041FB0
**Offset:** 0xFB0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | W | R | 0 | Refer ARM documentation. See links in CM7_ETM_TRCPRGCTLR. |

### 4.14.5.48 CM7_ETM_TRCLSR

**Description:** Software Lock Status Register
**Address:** 0xE0041FB4
**Offset:** 0xFB4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 0 | Refer ARM documentation. See links in CM7_ETM_TRCPRGCTLR. |

### 4.14.5.49 CM7_ETM_TRCAUTHSTATUS

**Description:** Authentication Status Register
**Address:** 0xE0041FB8
**Offset:** 0xFB8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 0 | Refer ARM documentation. See links in CM7_ETM_TRCPRGCTLR. |

### 4.14.5.50 CM7_ETM_TRCDEVARCH

**Description:** Device Architecture Register
**Address:** 0xE0041FBC
**Offset:** 0xFBC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x47704A13

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 1198541331 | Refer ARM documentation. See links in CM7_ETM_TRCPRGCTLR. |

### 4.14.5.51 CM7_ETM_TRCDEVID

**Description:** Device ID Register
**Address:** 0xE0041FC8
**Offset:** 0xFC8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 0 | Refer ARM documentation. See links in CM7_ETM_TRCPRGCTLR. |

### 4.14.5.52 CM7_ETM_TRCDEVTYPE

**Description:** CoreSight Device Type Register
**Address:** 0xE0041FCC
**Offset:** 0xFCC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x13

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 19 | Refer ARM documentation. See links in CM7_ETM_TRCPRGCTLR. |

### 4.14.5.53 CM7_ETM_PID4

**Description:** Peripheral Identification Register 4.
**Address:** 0xE0041FD0
**Offset:** 0xFD0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x4

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 4 | Refer ARM documentation. See links in CM7_ETM_TRCPRGCTLR. |

### 4.14.5.54 CM7_ETM_PID5

**Description:** Peripheral Identification Register 5.
**Address:** 0xE0041FD4
**Offset:** 0xFD4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 0 | Refer ARM documentation. See links in CM7_ETM_TRCPRGCTLR. |

### 4.14.5.55 CM7_ETM_PID6

**Description:** Peripheral Identification Register 6.
**Address:** 0xE0041FD8
**Offset:** 0xFD8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 0 | Refer ARM documentation. See links in CM7_ETM_TRCPRGCTLR. |

### 4.14.5.56 CM7_ETM_PID7

**Description:** Peripheral Identification Register 7.
**Address:** 0xE0041FDC
**Offset:** 0xFDC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 0 | Refer ARM documentation. See links in CM7_ETM_TRCPRGCTLR. |

### 4.14.5.57 CM7_ETM_PID0

**Description:** Peripheral Identification Register 0.
**Address:** 0xE0041FE0
**Offset:** 0xFE0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x75

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 117 | Refer ARM documentation. See links in CM7_ETM_TRCPRGCTLR. |

### 4.14.5.58 CM7_ETM_PID1

**Description:** Peripheral Identification Register 1.
**Address:** 0xE0041FE4
**Offset:** 0xFE4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xB9

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 185 | Refer ARM documentation. See links in CM7_ETM_TRCPRGCTLR. |

### 4.14.5.59 CM7_ETM_PID2

**Description:** Peripheral Identification Register 2.
**Address:** 0xE0041FE8
**Offset:** 0xFE8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x1B

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 27 | Refer ARM documentation. See links in CM7_ETM_TRCPRGCTLR. |

### 4.14.5.60 CM7_ETM_PID3

**Description:** Peripheral Identification Register 3.
**Address:** 0xE0041FEC
**Offset:** 0xFEC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | ECOREVNUM [7:4] | | | | None [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 4:7 | ECOREVNUM | R | R | 0 | Refer ARM documentation. See links in CM7_ETM_TRCPRGCTLR. |

### 4.14.5.61 CM7_ETM_CID0

**Description:** Component Identification Register 0.
**Address:** 0xE0041FF0
**Offset:** 0xFF0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xD

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 13 | Refer ARM documentation. See links in CM7_ETM_TRCPRGCTLR. |

### 4.14.5.62 CM7_ETM_CID1

**Description:** Component Identification Register 1.
**Address:** 0xE0041FF4
**Offset:** 0xFF4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x90

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 144 | Refer ARM documentation. See links in CM7_ETM_TRCPRGCTLR. |

### 4.14.5.63 CM7_ETM_CID2

**Description:** Component Identification Register 2.
**Address:** 0xE0041FF8
**Offset:** 0xFF8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x5

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 5 | Refer ARM documentation. See links in CM7_ETM_TRCPRGCTLR. |

### 4.14.5.64 CM7_ETM_CID3

**Description:** Component Identification Register 3.
**Address:** 0xE0041FFC
**Offset:** 0xFFC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xB1

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 177 | Refer ARM documentation. See links in CM7_ETM_TRCPRGCTLR. |

### 4.14.6 CM7CTI

#### 4.14.6.1 CM7_CM7CTI_CTICONTROL

**Description:** CTI Control Register
**Address:** 0xE0042000
**Offset:** 0x0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** The CTI Control Register enables the CTI.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:1] | | | | | | | GLBEN [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | GLBEN | RW | R | 0 | Enables or disables the ECT:<br>0 = disabled (reset)<br>1 = enabled.<br>When disabled, all cross triggering mapping logic functionality is disabled for this processor. |

### 4.14.6.2 CM7_CM7CTI_CTIINTACK

**Description:** CTI Interrupt Acknowledge Register
**Address:** 0xE0042010
**Offset:** 0x10
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** The CTI Interrupt Acknowledge Register is write-only. Any bits written as a 1 cause the CTITRIGOUT output signal to be acknowledged. The acknowledgement is cleared when MAPTRIGOUT is deactivated. This register is used when the CTITRIGOUT is used as a sticky output, that is, no hardware acknowledge is supplied, and a software acknowledge is required.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | INTACK [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | INTACK | W | R | 0 | Acknowledges the corresponding CTITRIGOUT output:<br>1 = CTITRIGOUT is acknowledged and is cleared when MAPTRIGOUT is LOW. 0 = no effect.<br>There is one bit of the register for each CTITRIGOUT output. |

### 4.14.6.3 CM7_CM7CTI_CTIAPPSET

**Description:** CTI Application Trigger Set Register
**Address:** 0xE0042014
**Offset:** 0x14
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** The CTI Application Trigger Set Register is read/write. A write to this register causes a channel event to be raised, corresponding to the bit written to.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:4] | | | | APPSET [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | APPSET | RW | R | 0 | Setting a bit HIGH generates a channel event for the selected channel. Read:<br>0 = application trigger inactive (reset)<br>1 = application trigger active.<br>Write:<br>0 = no effect<br>1 = generate channel event.<br>There is one bit of the register for each channel. |

### 4.14.6.4 CM7_CM7CTI_CTIAPPCLEAR

**Description:** CTI Application Trigger Clear Register
**Address:** 0xE0042018
**Offset:** 0x18
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** The CTI Application Trigger Clear Register is write-only. A write to this register causes a channel event to be cleared, corresponding to the bit written to.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:4] | | | | APPCLEAR [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | APPCLEAR | W | R | 0 | Clears corresponding bits in the CTIAPPSET register. 1 = application trigger disabled in the CTIAPPSET register 0 = no effect. There is one bit of the register for each channel. |

### 4.14.6.5 CM7_CM7CTI_CTIAPPPULSE

**Description:** CTI Application Pulse Register
**Address:** 0xE004201C
**Offset:** 0x1C
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** The CTI Application Pulse Register is write-only. A write to this register causes a channel event pulse, one CTICLK period, to be generated, corresponding to the bit written to. The pulse external to the ECT can be extended to multi-cycle by the handshaking interface circuits. This register clears itself immediately, so it can be repeatedly written to without software having to clear it.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:4] | | | | APPULSE [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | APPULSE | W | R | 0 | Setting a bit HIGH generates a channel event pulse for the selected channel. Write:<br>1 = channel event pulse generated for one CTICLK period 0 = no effect.<br>There is one bit of the register for each channel. |

#### 4.14.6.6 CM7_CM7CTI_CTIINEN

**Description:** CTI Trigger to Channel Enable Registers
**Address:** 0xE0042020
**Offset:** 0x20
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** The CTI Trigger to Channel Enable Registers enable the signalling of an event on CTM channels when the core issues a trigger, CTITRIGIN, to the CTI. There is one register for each of the eight CTITRIGIN inputs. Within each register there is one bit for each of the four channels implemented. These registers do not affect the application trigger operations.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:4] | | | | TRIGINEN [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | TRIGINEN | RW | R | 0 | Enables a cross trigger event to the corresponding channel when an CTITRIGIN is activated.<br>1 = enables the CTITRIGIN signal to generate an event on the respective channel of the CTM.<br>There is one bit of the register for each of the four channels. For example in register CTIINEN0, TRIGINEN[0] set to 1 enables CTITRIGIN onto channel 0.<br>0 = disables the CTITRIGIN signal from generating an event on the respective channel of the CTM. |

### 4.14.6.7 CM7_CM7CTI_CTIOUTEN

**Description:** CTI Channel to Trigger Enable Registers
**Address:** 0xE00420A0
**Offset:** 0xA0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** The CTI Channel to Trigger Enable Registers define which channels can generate a CTITRIGOUT output. There is one register for each of the eight CTITRIGOUT outputs. Within each register there is one bit for each of the four channels implemented. These registers affect the mapping from application trigger to trigger outputs.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:4] | | | | TRIGOUTEN [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | TRIGOUTEN | RW | R | 0 | Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate an CTITRIGOUT output:<br>0 = the channel input (CTICHIN) from the CTM is not routed to the CTITRIGOUT output 1 = the channel input (CTICHIN) from the CTM is routed to the CTITRIGOUT output. There is one bit for each of the four channels. For example in register CTIOUTEN0, enabling bit 0 enables CTICHIN[0] to cause a trigger event on the CTITRIGOUT[0] output. |

### 4.14.6.8 CM7_CM7CTI_CTITRIGINSTATUS

**Description:** CTI Trigger In Status Register
**Address:** 0xE0042130
**Offset:** 0x130
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** The CTI Trigger In Status Register provides the status of the CTITRIGIN inputs.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | TRIGINSTATUS [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | TRIGINSTATUS | R | RW | 0 | Shows the status of the CTITRIGIN inputs:<br>1 = CTITRIGIN is active<br>0 = CTITRIGIN is inactive.<br>Because the register provides a view of the raw CTITRIGIN inputs, the reset value is unknown. There is one bit of the register for each trigger input. |

### 4.14.6.9 CM7_CM7CTI_CTITRIGOUTSTATUS

**Description:** CTI Trigger Out Status Register
**Address:** 0xE0042134
**Offset:** 0x134
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** The CTI Trigger Out Status Register provides the status of the CTITRIGOUT outputs.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | TRIGOUTSTATUS [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | TRIGOUTSTATUS | R | RW | 0 | Shows the status of the CTITRIGOUT outputs.<br>1 = CTITRIGOUT is active<br>0 = CTITRIGOUT is inactive (reset).<br>There is one bit of the register for each trigger output. |

### 4.14.6.10 CM7_CM7CTI_CTICHINSTATUS

**Description:** CTI Channel In Status Register
**Address:** 0xE0042138
**Offset:** 0x138
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** The CTI Channel In Status Register provides the status of the CTI CTICHIN inputs.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:4] | | | | CTICHINSTATUS [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | CTICHINSTATUS | R | RW | 0 | Shows the status of the CTICHIN inputs:<br>1 = CTICHIN is active<br>0 = CTICHIN is inactive.<br>Because the register provides a view of the raw CTICHIN inputs from the CTM, the reset value is unknown. There is one bit of the register for each channel input. |

### 4.14.6.11 CM7_CM7CTI_CTICHOUTSTATUS

**Description:** CTI Channel Out Status Register
**Address:** 0xE004213C
**Offset:** 0x13C
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** The CTI Channel Out Status Register provides the status of the CTI CTICHOUT outputs.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:4] | | | | CTICHOUTSTATUS [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | CTICHOUTSTATUS | R | RW | 0 | Shows the status of the CTICHOUT outputs.<br>1 = CTICHOUT is active<br>0 = CTICHOUT is inactive (reset).<br>There is one bit of the register for each channel output. |

### 4.14.6.12 CM7_CM7CTI_CTIGATE

**Description:** Enable CTI Channel Gate Register
**Address:** 0xE0042140
**Offset:** 0x140
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** The Gate Enable Register prevents the channels from propagating through the CTM to other CTIs. This enables local cross-triggering, for example for causing an interrupt when the ETM trigger occurs. It can be used effectively with CTIAPPSET, CTIAPPCLEAR, and CTIAPPPULSE for asserting trigger outputs by asserting channels, without affecting the rest of the system. On reset, this register is 0xF, and channel propagation is enabled.
**Default:** 0xF

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:4] | | | | CTIGATEEN 3 [3:3] | CTIGATEEN 2 [2:2] | CTIGATEEN 1 [1:1] | CTIGATEEN 0 [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | CTIGATEEN0 | RW | R | 1 | Enable CTICHOUT0. Set to 0 to disable channel propagation. |
| 1 | CTIGATEEN1 | RW | R | 1 | Enable CTICHOUT1. Set to 0 to disable channel propagation. |
| 2 | CTIGATEEN2 | RW | R | 1 | Enable CTICHOUT2. Set to 0 to disable channel propagation. |
| 3 | CTIGATEEN3 | RW | R | 1 | Enable CTICHOUT3. Set to 0 to disable channel propagation. |

### 4.14.6.13 CM7_CM7CTI_ASICCTL

**Description:** External Multiplexor Control Register
**Address:** 0xE0042144
**Offset:** 0x144
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | ASICCTL [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | ASICCTL | RW | R | 0 | Implementation-defined ASIC control, value written to the register is output on ASICCTL[7:0].<br>If external multiplexing of trigger signals is implemented then the number of multiplexed signals on each trigger must be reflected within the Device ID Register. This is done within a Verilog define EXTMUXNUM. See ECT CoreSight defined registers on Arm TRM page 4-28. |

### 4.14.6.14 CM7_CM7CTI_ITCHINACK

**Description:** ITCHINACK Register
**Address:** 0xE0042EDC
**Offset:** 0xEDC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register is a write-only register.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:4] | | | | CTCHINACK [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | CTCHINACK | W | R | 0 | Set the value of the CTCHINACK outputs |

### 4.14.6.15 CM7_CM7CTI_ITTRIGINACK

**Description:** ITTRIGINACK Register
**Address:** 0xE0042EE0
**Offset:** 0xEE0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register is a write-only register.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | CTTRIGINACK [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | CTTRIGINACK | W | R | 0 | Set the value of the CTTRIGINACK outputs |

### 4.14.6.16 CM7_CM7CTI_ITCHOUT

**Description:** ITCHOUT Register
**Address:** 0xE0042EE4
**Offset:** 0xEE4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register is a write-only register.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:4] | | | | CTCHOUT [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | CTCHOUT | W | R | 0 | Set the value of the CTCHOUT outputs |

### 4.14.6.17 CM7_CM7CTI_ITTRIGOUT

**Description:** ITTRIGOUT Register
**Address:** 0xE0042EE8
**Offset:** 0xEE8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register is a write-only register.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | CTTRIGOUT [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | CTTRIGOUT | W | R | 0 | Set the value of the CTTRIGOUT outputs |

### 4.14.6.18 CM7_CM7CTI_ITCHOUTACK

**Description:** ITCHOUTACK Register
**Address:** 0xE0042EEC
**Offset:** 0xEEC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register is a read-only register.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:4] | | | | CTCHOUTACK [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | CTCHOUTACK | R | W | 0 | Read the values of the CTCHOUTACK inputs |

### 4.14.6.19 CM7_CM7CTI_ITTRIGOUTACK

**Description:** ITTRIGOUTACK Register
**Address:** 0xE0042EF0
**Offset:** 0xEF0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register is a read-only register.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | CTTRIGOUTACK [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | CTTRIGOUTACK | R | W | 0 | Read the values of the CTTRIGOUTACK inputs |

### 4.14.6.20 CM7_CM7CTI_ITCHIN

**Description:** ITCHIN Register
**Address:** 0xE0042EF4
**Offset:** 0xEF4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register is a read-only register.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:4] | | | | CTCHIN [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | CTCHIN | R | W | 0 | Read the values of the CTCHIN inputs |

### 4.14.6.21 CM7_CM7CTI_ITTRIGIN

**Description:** ITTRIGIN Register
**Address:** 0xE0042EF8
**Offset:** 0xEF8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register is a read-only register.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | CTTRIGIN [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | CTTRIGIN | R | W | 0 | Read the values of the CTTRIGIN inputs |

### 4.14.6.22 CM7_CM7CTI_ITCTRL

**Description:** Integration Mode Control Register
**Address:** 0xE0042F00
**Offset:** 0xF00
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register enables the component to switch from a functional mode, the default behavior, to integration mode where the inputs and outputs of the component can be directly controlled for the purpose of integration testing and topology solving.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:1] | | | | | | | MODE [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | MODE | RW | R | 0 | When set, the component enters integration mode, enabling topology detection or integration testing to be performed. At reset the component must enter functional mode. If no integration functionality is implemented, this register must read as zero. |

### 4.14.6.23 CM7_CM7CTI_CLAIMSET

**Description:** Claim Tag Set Register
**Address:** 0xE0042FA0
**Offset:** 0xFA0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register forms one half of the Claim Tag value. This location allows individual bits to be set, write, and returns the number of bits that can be set, read.
You can determine how many claim bits are implemented by reading this register. For example, if 4 bits are implemented, a read of this register will return 0x0000000F. If no claim tag is implemented, then a read of this register will return 0x00000000.
**Default:** 0xF

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:4] | | | | TAG [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | TAG | RW1S | R | 15 | A bit programmable register bank which sets the Claim Tag Value. A read will return a logic 1 for all implemented locations. |

### 4.14.6.24 CM7_CM7CTI_CLAIMCLR

**Description:** Claim Tag Clear Register
**Address:** 0xE0042FA4
**Offset:** 0xFA4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register forms one half of the Claim Tag value. This location enables individual bits to be cleared, write, and returns the current Claim Tag value, read. The width (n) of this register can be determined from reading the Claim Tag Set Register.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:4] | | | | TAG [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | TAG | RW1C | R | 0 | A bit programmable register bank that is zero at reset. |

### 4.14.6.25 CM7_CM7CTI_LOCKACCESS

**Description:** Lock Access Register
**Address:** 0xE0042FB0
**Offset:** 0xFB0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This is used to enable write access to device registers. If LOCKSTATUS[0] == 0x0 then this register is not present.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:4] | | | | ACCESS_CODE [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | ACCESS_CODE | RW | R | 0 | Write Access Code. A write of 0xC5ACCE55 enables further write access to this device. An invalid write will have the affect of removing write access.<br>If LOCKSTATUS[2] is set, then only bits [7:0] of this register are implemented and lock access is obtained by consecutively writing 0xC5, 0xAC, 0xCE, 0x55. Bits [31:8] are unused and any writes to them ignored. |

### 4.14.6.26 CM7_CM7CTI_LOCKSTATUS

**Description:** Lock Status Register
**Address:** 0xE0042FB4
**Offset:** 0xFB4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This indicates the status of the Lock control mechanism. This lock prevents accidental writes by code under debug.
This register must always be present although there might not be any lock-access control mechanism. The lock mechanism, where present and locked, must block write accesses to any control register, except the Lock Access Register. For most components this covers all registers except for the Lock Access Register 0xFB0.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:3] | | | | | IMPLEMENTS_8B [2:2] | ACCESS_PERMITTED [1:1] | EXISTS [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | EXISTS | R | W | 0 | Indicates that a lock control mechanism exists for this device |
| 1 | ACCESS_PERMITTED | R | W | 0 | The values of this bit mean:<br>0 = Access permitted.<br>1 = Write access to the component is blocked. All writes to control registers are ignored. Reads are permitted |
| 2 | IMPLEMENTS_8B | R | W | 0 | This component implements an 8-bit Lock Access Register. |

### 4.14.6.27 CM7_CM7CTI_AUTHSTATUS

**Description:** Authentication Status Register
**Address:** 0xE0042FB8
**Offset:** 0xFB8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Reports the required security level and current status of those enables. Where functionality changes on a given security level then this change in status must be reported in this register
**Default:** 0x5

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | SNIDBG [7:6] | | SIDBG [5:4] | | NSNIDBG [3:2] | | NSIDBG [1:0] | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:1 | NSIDBG | R | W | 1 | Non-Secure Invasive Debug<br>0: Functionality not implemented or controlled elsewhere<br>1: Functionality disabled<br>2: Reserved<br>3: Functionality enabled |
| 2:3 | NSNIDBG | R | W | 1 | Non-Secure Non-Invasive Debug<br>0: Functionality not implemented or controlled elsewhere<br>1: Functionality disabled<br>2: Reserved<br>3: Functionality enabled |
| 4:5 | SIDBG | R | W | 0 | Secure Invasive Debug<br>0: Functionality not implemented or controlled elsewhere<br>1: Functionality disabled<br>2: Reserved<br>3: Functionality enabled |
| 6:7 | SNIDBG | R | W | 0 | Secure Non-Invasive Debug<br>0: Functionality not implemented or controlled elsewhere<br>1: Functionality disabled<br>2: Reserved<br>3: Functionality enabled |

### 4.14.6.28 CM7_CM7CTI_DEVID

**Description:** Device Configuration Register
**Address:** 0xE0042FC8
**Offset:** 0xFC8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register is implementation-defined for each Part Number and Designer. This indicates the capabilities of the component. The entire 32-bit field can be used because the data width is determined by the particular component. Unused bits must read as zero.
If the component is configurable then it is recommended that this register reflects any changes to a standard configuration.
**Default:** 0x40804

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:5] | | | NRMUXING [4:0] | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | NRTRIG [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:20] | | | | NRCHAN [19:16] | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:4 | NRMUXING | R | R | 4 | Indicates the number of multiplexing available on Trigger Inputs and Trigger Outputs using ASICCTL. Default value of 5'b00000 indicating no multiplexing present. Reflects the value of the Verilog `define EXTMUXNUM that you must alter accordingly. |
| 8:15 | NRTRIG | R | R | 8 | Number of ECT triggers available. |
| 16:19 | NRCHAN | R | R | 4 | Number of ECT channels available. |

### 4.14.6.29 CM7_CM7CTI_DEVTYPE

**Description:** Device Type Identifier Register
**Address:** 0xE0042FCC
**Offset:** 0xFCC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** 0x14 indicates this device has a major type of debug control logic component (0x4) and sub-type corresponding to cross trigger (0x1).
**Default:** 0x14

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | SUB_TYPE [7:4] | | | | CLASS [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | CLASS | R | R | 4 | debug control logic component |
| 4:7 | SUB_TYPE | R | R | 1 | cross trigger |

### 4.14.6.30 CM7_CM7CTI_PID4

**Description:** Peripheral Identification Register 4
**Address:** 0xE0042FD0
**Offset:** 0xFD0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x4

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 4 | N/A |

### 4.14.6.31 CM7_CM7CTI_PID5

**Description:** Peripheral Identification Register 5
**Address:** 0xE0042FD4
**Offset:** 0xFD4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 0 | N/A |

### 4.14.6.32 CM7_CM7CTI_PID6

**Description:** Peripheral Identification Register 6
**Address:** 0xE0042FD8
**Offset:** 0xFD8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 0 | N/A |

### 4.14.6.33 CM7_CM7CTI_PID7

**Description:** Peripheral Identification Register 7
**Address:** 0xE0042FDC
**Offset:** 0xFDC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 0 | N/A |

### 4.14.6.34 CM7_CM7CTI_PID0

**Description:** Peripheral Identification Register 0
**Address:** 0xE0042FE0
**Offset:** 0xFE0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x6

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 6 | N/A |

### 4.14.6.35 CM7_CM7CTI_PID1

**Description:** Peripheral Identification Register 1
**Address:** 0xE0042FE4
**Offset:** 0xFE4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xB9

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 185 | N/A |

### 4.14.6.36 CM7_CM7CTI_PID2

**Description:** Peripheral Identification Register 2
**Address:** 0xE0042FE8
**Offset:** 0xFE8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x2B

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 43 | N/A |

### 4.14.6.37 CM7_CM7CTI_PID3

**Description:** Peripheral Identification Register 3
**Address:** 0xE0042FEC
**Offset:** 0xFEC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | ECOREVNUM [7:4] | | | | None [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 4:7 | ECOREVNUM | R | R | 0 | ECO revision for MTB |

### 4.14.6.38 CM7_CM7CTI_CID0

**Description:** Component Identification Register 0
**Address:** 0xE0042FF0
**Offset:** 0xFF0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xD

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 13 | N/A |

### 4.14.6.39 CM7_CM7CTI_CID1

**Description:** Component Identification Register 1
**Address:** 0xE0042FF4
**Offset:** 0xFF4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x90

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 144 | N/A |

### 4.14.6.40 CM7_CM7CTI_CID2

**Description:** Component Identification Register 2
**Address:** 0xE0042FF8
**Offset:** 0xFF8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x5

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 5 | N/A |

### 4.14.6.41 CM7_CM7CTI_CID3

**Description:** Component Identification Register 3
**Address:** 0xE0042FFC
**Offset:** 0xFFC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xB1

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 177 | N/A |

### 4.14.7 TRCCTI

#### 4.14.7.1 CM7_TRCCTI_CTICONTROL

**Description:** CTI Control Register
**Address:** 0xE0080000
**Offset:** 0x0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** The CTI Control Register enables the CTI.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:1] | | | | | | | GLBEN [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | GLBEN | RW | R | 0 | Enables or disables the ECT:<br>0 = disabled (reset)<br>1 = enabled.<br>When disabled, all cross triggering mapping logic functionality is disabled for this processor. |

### 4.14.7.2 CM7_TRCCTI_CTIINTACK

**Description:** CTI Interrupt Acknowledge Register
**Address:** 0xE0080010
**Offset:** 0x10
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** The CTI Interrupt Acknowledge Register is write-only. Any bits written as a 1 cause the CTITRIGOUT output signal to be acknowledged. The acknowledgement is cleared when MAPTRIGOUT is deactivated. This register is used when the CTITRIGOUT is used as a sticky output, that is, no hardware acknowledge is supplied, and a software acknowledge is required.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | INTACK [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | INTACK | W | R | 0 | Acknowledges the corresponding CTITRIGOUT output:<br>1 = CTITRIGOUT is acknowledged and is cleared when MAPTRIGOUT is LOW. 0 = no effect.<br>There is one bit of the register for each CTITRIGOUT output. |

### 4.14.7.3 CM7_TRCCTI_CTIAPPSET

**Description:** CTI Application Trigger Set Register
**Address:** 0xE0080014
**Offset:** 0x14
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** The CTI Application Trigger Set Register is read/write. A write to this register causes a channel event to be raised, corresponding to the bit written to.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:4] | | | | APPSET [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | APPSET | RW | R | 0 | Setting a bit HIGH generates a channel event for the selected channel. Read:<br>0 = application trigger inactive (reset)<br>1 = application trigger active.<br>Write:<br>0 = no effect<br>1 = generate channel event.<br>There is one bit of the register for each channel. |

### 4.14.7.4 CM7_TRCCTI_CTIAPPCLEAR

**Description:** CTI Application Trigger Clear Register
**Address:** 0xE0080018
**Offset:** 0x18
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** The CTI Application Trigger Clear Register is write-only. A write to this register causes a channel event to be cleared, corresponding to the bit written to.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:4] | | | | APPCLEAR [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | APPCLEAR | W | R | 0 | Clears corresponding bits in the CTIAPPSET register. 1 = application trigger disabled in the CTIAPPSET register 0 = no effect.<br>There is one bit of the register for each channel. |

### 4.14.7.5 CM7_TRCCTI_CTIAPPPULSE

**Description:** CTI Application Pulse Register
**Address:** 0xE008001C
**Offset:** 0x1C
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** The CTI Application Pulse Register is write-only. A write to this register causes a channel event pulse, one CTICLK period, to be generated, corresponding to the bit written to. The pulse external to the ECT can be extended to multi-cycle by the handshaking interface circuits. This register clears itself immediately, so it can be repeatedly written to without software having to clear it.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:4] | | | | APPULSE [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | APPULSE | W | R | 0 | Setting a bit HIGH generates a channel event pulse for the selected channel. Write:<br>1 = channel event pulse generated for one CTICLK period 0 = no effect.<br>There is one bit of the register for each channel. |

### 4.14.7.6 CM7_TRCCTI_CTIINEN

**Description:** CTI Trigger to Channel Enable Registers
**Address:** 0xE0080020
**Offset:** 0x20
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** The CTI Trigger to Channel Enable Registers enable the signalling of an event on CTM channels when the core issues a trigger, CTITRIGIN, to the CTI. There is one register for each of the eight CTITRIGIN inputs. Within each register there is one bit for each of the four channels implemented. These registers do not affect the application trigger operations.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:4] | | | | TRIGINEN [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | TRIGINEN | RW | R | 0 | Enables a cross trigger event to the corresponding channel when an CTITRIGIN is activated.<br>1 = enables the CTITRIGIN signal to generate an event on the respective channel of the CTM.<br>There is one bit of the register for each of the four channels. For example in register CTIINEN0, TRIGINEN[0] set to 1 enables CTITRIGIN onto channel 0.<br>0 = disables the CTITRIGIN signal from generating an event on the respective channel of the CTM. |

### 4.14.7.7 CM7_TRCCTI_CTIOUTEN

**Description:** CTI Channel to Trigger Enable Registers
**Address:** 0xE00800A0
**Offset:** 0xA0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** The CTI Channel to Trigger Enable Registers define which channels can generate a CTITRIGOUT output. There is one register for each of the eight CTITRIGOUT outputs. Within each register there is one bit for each of the four channels implemented. These registers affect the mapping from application trigger to trigger outputs.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:4] | | | | TRIGOUTEN [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | TRIGOUTEN | RW | R | 0 | Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate an CTITRIGOUT output:<br>0 = the channel input (CTICHIN) from the CTM is not routed to the CTITRIGOUT output 1 = the channel input (CTICHIN) from the CTM is routed to the CTITRIGOUT output. There is one bit for each of the four channels. For example in register CTIOUTEN0, enabling bit 0 enables CTICHIN[0] to cause a trigger event on the CTITRIGOUT[0] output. |

### 4.14.7.8 CM7_TRCCTI_CTITRIGINSTATUS

**Description:** CTI Trigger In Status Register
**Address:** 0xE0080130
**Offset:** 0x130
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** The CTI Trigger In Status Register provides the status of the CTITRIGIN inputs.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | TRIGINSTATUS [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | TRIGINSTATUS | R | RW | 0 | Shows the status of the CTITRIGIN inputs:<br>1 = CTITRIGIN is active<br>0 = CTITRIGIN is inactive.<br>Because the register provides a view of the raw CTITRIGIN inputs, the reset value is unknown. There is one bit of the register for each trigger input. |

### 4.14.7.9 CM7_TRCCTI_CTITRIGOUTSTATUS

**Description:** CTI Trigger Out Status Register
**Address:** 0xE0080134
**Offset:** 0x134
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** The CTI Trigger Out Status Register provides the status of the CTITRIGOUT outputs.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | TRIGOUTSTATUS [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | TRIGOUTSTATUS | R | RW | 0 | Shows the status of the CTITRIGOUT outputs.<br>1 = CTITRIGOUT is active<br>0 = CTITRIGOUT is inactive (reset).<br>There is one bit of the register for each trigger output. |

### 4.14.7.10 CM7_TRCCTI_CTICHINSTATUS

**Description:** CTI Channel In Status Register
**Address:** 0xE0080138
**Offset:** 0x138
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** The CTI Channel In Status Register provides the status of the CTI CTICHIN inputs.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:4] | | | | CTICHINSTATUS [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | CTICHINSTATUS | R | RW | 0 | Shows the status of the CTICHIN inputs:<br>1 = CTICHIN is active<br>0 = CTICHIN is inactive.<br>Because the register provides a view of the raw CTICHIN inputs from the CTM, the reset value is unknown. There is one bit of the register for each channel input. |

### 4.14.7.11 CM7_TRCCTI_CTICHOUTSTATUS

**Description:** CTI Channel Out Status Register
**Address:** 0xE008013C
**Offset:** 0x13C
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** The CTI Channel Out Status Register provides the status of the CTI CTICHOUT outputs.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:4] | | | | CTICHOUTSTATUS [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | CTICHOUTSTATUS | R | RW | 0 | Shows the status of the CTICHOUT outputs.<br>1 = CTICHOUT is active<br>0 = CTICHOUT is inactive (reset).<br>There is one bit of the register for each channel output. |

### 4.14.7.12 CM7_TRCCTI_CTIGATE

**Description:** Enable CTI Channel Gate Register
**Address:** 0xE0080140
**Offset:** 0x140
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** The Gate Enable Register prevents the channels from propagating through the CTM to other CTIs. This enables local cross-triggering, for example for causing an interrupt when the ETM trigger occurs. It can be used effectively with CTIAPPSET, CTIAPPCLEAR, and CTIAPPPULSE for asserting trigger outputs by asserting channels, without affecting the rest of the system. On reset, this register is 0xF, and channel propagation is enabled.
**Default:** 0xF

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:4] | | | | CTIGATEEN 3 [3:3] | CTIGATEEN 2 [2:2] | CTIGATEEN 1 [1:1] | CTIGATEEN 0 [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | CTIGATEEN0 | RW | R | 1 | Enable CTICHOUT0. Set to 0 to disable channel propagation. |
| 1 | CTIGATEEN1 | RW | R | 1 | Enable CTICHOUT1. Set to 0 to disable channel propagation. |
| 2 | CTIGATEEN2 | RW | R | 1 | Enable CTICHOUT2. Set to 0 to disable channel propagation. |
| 3 | CTIGATEEN3 | RW | R | 1 | Enable CTICHOUT3. Set to 0 to disable channel propagation. |

### 4.14.7.13 CM7_TRCCTI_ASICCTL

**Description:** External Multiplexor Control Register
**Address:** 0xE0080144
**Offset:** 0x144
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | ASICCTL [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | ASICCTL | RW | R | 0 | Implementation-defined ASIC control, value written to the register is output on ASICCTL[7:0].<br>If external multiplexing of trigger signals is implemented then the number of multiplexed signals on each trigger must be reflected within the Device ID Register. This is done within a Verilog define EXTMUXNUM. See ECT CoreSight defined registers on Arm TRM page 4-28. |

### 4.14.7.14 CM7_TRCCTI_ITCHINACK

**Description:** ITCHINACK Register
**Address:** 0xE0080EDC
**Offset:** 0xEDC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register is a write-only register.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:4] | | | | CTCHINACK [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | CTCHINACK | W | R | 0 | Set the value of the CTCHINACK outputs |

### 4.14.7.15 CM7_TRCCTI_ITTRIGINACK

**Description:** ITTRIGINACK Register
**Address:** 0xE0080EE0
**Offset:** 0xEE0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register is a write-only register.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | CTTRIGINACK [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | CTTRIGINACK | W | R | 0 | Set the value of the CTTRIGINACK outputs |

### 4.14.7.16 CM7_TRCCTI_ITCHOUT

**Description:** ITCHOUT Register
**Address:** 0xE0080EE4
**Offset:** 0xEE4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register is a write-only register.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:4] | | | | CTCHOUT [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | CTCHOUT | W | R | 0 | Set the value of the CTCHOUT outputs |

### 4.14.7.17 CM7_TRCCTI_ITTRIGOUT

**Description:** ITTRIGOUT Register
**Address:** 0xE0080EE8
**Offset:** 0xEE8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register is a write-only register.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | CTTRIGOUT [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | CTTRIGOUT | W | R | 0 | Set the value of the CTTRIGOUT outputs |

### 4.14.7.18 CM7_TRCCTI_ITCHOUTACK

**Description:** ITCHOUTACK Register
**Address:** 0xE0080EEC
**Offset:** 0xEEC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register is a read-only register.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:4] | | | | CTCHOUTACK [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | CTCHOUTACK | R | W | 0 | Read the values of the CTCHOUTACK inputs |

### 4.14.7.19 CM7_TRCCTI_ITTRIGOUTACK

**Description:** ITTRIGOUTACK Register
**Address:** 0xE0080EF0
**Offset:** 0xEF0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register is a read-only register.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | CTTRIGOUTACK [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | CTTRIGOUTACK | R | W | 0 | Read the values of the CTTRIGOUTACK inputs |

### 4.14.7.20 CM7_TRCCTI_ITCHIN

**Description:** ITCHIN Register
**Address:** 0xE0080EF4
**Offset:** 0xEF4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register is a read-only register.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:4] | | | | CTCHIN [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | CTCHIN | R | W | 0 | Read the values of the CTCHIN inputs |

### 4.14.7.21 CM7_TRCCTI_ITTRIGIN

**Description:** ITTRIGIN Register
**Address:** 0xE0080EF8
**Offset:** 0xEF8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register is a read-only register.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | CTTRIGIN [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | CTTRIGIN | R | W | 0 | Read the values of the CTTRIGIN inputs |

### 4.14.7.22 CM7_TRCCTI_ITCTRL

**Description:** Integration Mode Control Register
**Address:** 0xE0080F00
**Offset:** 0xF00
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register enables the component to switch from a functional mode, the default behavior, to integration mode where the inputs and outputs of the component can be directly controlled for the purpose of integration testing and topology solving.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:1] | | | | | | | MODE [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | MODE | RW | R | 0 | When set, the component enters integration mode, enabling topology detection or integration testing to be performed. At reset the component must enter functional mode. If no integration functionality is implemented, this register must read as zero. |

### 4.14.7.23 CM7_TRCCTI_CLAIMSET

**Description:** Claim Tag Set Register
**Address:** 0xE0080FA0
**Offset:** 0xFA0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register forms one half of the Claim Tag value. This location allows individual bits to be set, write, and returns the number of bits that can be set, read.
You can determine how many claim bits are implemented by reading this register. For example, if 4 bits are implemented, a read of this register will return 0x0000000F. If no claim tag is implemented, then a read of this register will return 0x00000000.
**Default:** 0xF

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:4] | | | | TAG [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | TAG | RW1S | R | 15 | A bit programmable register bank which sets the Claim Tag Value. A read will return a logic 1 for all implemented locations. |

### 4.14.7.24 CM7_TRCCTI_CLAIMCLR

**Description:** Claim Tag Clear Register
**Address:** 0xE0080FA4
**Offset:** 0xFA4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register forms one half of the Claim Tag value. This location enables individual bits to be cleared, write, and returns the current Claim Tag value, read. The width (n) of this register can be determined from reading the Claim Tag Set Register.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:4] | | | | TAG [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | TAG | RW1C | R | 0 | A bit programmable register bank that is zero at reset. |

### 4.14.7.25 CM7_TRCCTI_LOCKACCESS

**Description:** Lock Access Register
**Address:** 0xE0080FB0
**Offset:** 0xFB0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This is used to enable write access to device registers. If LOCKSTATUS[0] == 0x0 then this register is not present.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:4] | | | | ACCESS_CODE [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | ACCESS_CODE | RW | R | 0 | Write Access Code. A write of 0xC5ACCE55 enables further write access to this device. An invalid write will have the affect of removing write access.<br>If LOCKSTATUS[2] is set, then only bits [7:0] of this register are implemented and lock access is obtained by consecutively writing 0xC5, 0xAC, 0xCE, 0x55. Bits [31:8] are unused and any writes to them ignored. |

### 4.14.7.26 CM7_TRCCTI_LOCKSTATUS

**Description:** Lock Status Register
**Address:** 0xE0080FB4
**Offset:** 0xFB4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This indicates the status of the Lock control mechanism. This lock prevents accidental writes by code under debug.
This register must always be present although there might not be any lock-access control mechanism. The lock mechanism, where present and locked, must block write accesses to any control register, except the Lock Access Register. For most components this covers all registers except for the Lock Access Register 0xFB0.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:3] | | | | | IMPLEMENTS_8B [2:2] | ACCESS_PERMITTED [1:1] | EXISTS [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | EXISTS | R | W | 0 | Indicates that a lock control mechanism exists for this device |
| 1 | ACCESS_PERMITTED | R | W | 0 | The values of this bit mean:<br>0 = Access permitted.<br>1 = Write access to the component is blocked. All writes to control registers are ignored. Reads are permitted |
| 2 | IMPLEMENTS_8B | R | W | 0 | This component implements an 8-bit Lock Access Register. |

### 4.14.7.27 CM7_TRCCTI_AUTHSTATUS

**Description:** Authentication Status Register
**Address:** 0xE0080FB8
**Offset:** 0xFB8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Reports the required security level and current status of those enables. Where functionality changes on a given security level then this change in status must be reported in this register
**Default:** 0x5

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | SNIDBG [7:6] | | SIDBG [5:4] | | NSNIDBG [3:2] | | NSIDBG [1:0] | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:1 | NSIDBG | R | W | 1 | Non-Secure Invasive Debug<br>0: Functionality not implemented or controlled elsewhere<br>1: Functionality disabled<br>2: Reserved<br>3: Functionality enabled |
| 2:3 | NSNIDBG | R | W | 1 | Non-Secure Non-Invasive Debug<br>0: Functionality not implemented or controlled elsewhere<br>1: Functionality disabled<br>2: Reserved<br>3: Functionality enabled |
| 4:5 | SIDBG | R | W | 0 | Secure Invasive Debug<br>0: Functionality not implemented or controlled elsewhere<br>1: Functionality disabled<br>2: Reserved<br>3: Functionality enabled |
| 6:7 | SNIDBG | R | W | 0 | Secure Non-Invasive Debug<br>0: Functionality not implemented or controlled elsewhere<br>1: Functionality disabled<br>2: Reserved<br>3: Functionality enabled |

### 4.14.7.28 CM7_TRCCTI_DEVID

**Description:** Device Configuration Register
**Address:** 0xE0080FC8
**Offset:** 0xFC8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register is implementation-defined for each Part Number and Designer. This indicates the capabilities of the component. The entire 32-bit field can be used because the data width is determined by the particular component. Unused bits must read as zero.
If the component is configurable then it is recommended that this register reflects any changes to a standard configuration.
**Default:** 0x40804

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:5] | | | NRMUXING [4:0] | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | NRTRIG [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:20] | | | | NRCHAN [19:16] | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:4 | NRMUXING | R | R | 4 | Indicates the number of multiplexing available on Trigger Inputs and Trigger Outputs using ASICCTL. Default value of 5'b00000 indicating no multiplexing present. Reflects the value of the Verilog `define EXTMUXNUM that you must alter accordingly. |
| 8:15 | NRTRIG | R | R | 8 | Number of ECT triggers available. |
| 16:19 | NRCHAN | R | R | 4 | Number of ECT channels available. |

### 4.14.7.29 CM7_TRCCTI_DEVTYPE

**Description:** Device Type Identifier Register
**Address:** 0xE0080FCC
**Offset:** 0xFCC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** 0x14 indicates this device has a major type of debug control logic component (0x4) and sub-type corresponding to cross trigger (0x1).
**Default:** 0x14

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | SUB_TYPE [7:4] | | | | CLASS [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | CLASS | R | R | 4 | debug control logic component |
| 4:7 | SUB_TYPE | R | R | 1 | cross trigger |

### 4.14.7.30 CM7_TRCCTI_PID4

**Description:** Peripheral Identification Register 4
**Address:** 0xE0080FD0
**Offset:** 0xFD0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x4

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 4 | N/A |

### 4.14.7.31 CM7_TRCCTI_PID5

**Description:** Peripheral Identification Register 5
**Address:** 0xE0080FD4
**Offset:** 0xFD4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 0 | N/A |

### 4.14.7.32 CM7_TRCCTI_PID6

**Description:** Peripheral Identification Register 6
**Address:** 0xE0080FD8
**Offset:** 0xFD8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 0 | N/A |

### 4.14.7.33 CM7_TRCCTI_PID7

**Description:** Peripheral Identification Register 7
**Address:** 0xE0080FDC
**Offset:** 0xFDC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 0 | N/A |

### 4.14.7.34 CM7_TRCCTI_PID0

**Description:** Peripheral Identification Register 0
**Address:** 0xE0080FE0
**Offset:** 0xFE0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x6

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 6 | N/A |

### 4.14.7.35 CM7_TRCCTI_PID1

**Description:** Peripheral Identification Register 1
**Address:** 0xE0080FE4
**Offset:** 0xFE4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xB9

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 185 | N/A |

### 4.14.7.36 CM7_TRCCTI_PID2

**Description:** Peripheral Identification Register 2
**Address:** 0xE0080FE8
**Offset:** 0xFE8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x2B

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 43 | N/A |

### 4.14.7.37 CM7_TRCCTI_PID3

**Description:** Peripheral Identification Register 3
**Address:** 0xE0080FEC
**Offset:** 0xFEC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | ECOREVNUM [7:4] | | | | None [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 4:7 | ECOREVNUM | R | R | 0 | ECO revision for MTB |

### 4.14.7.38 CM7_TRCCTI_CID0

**Description:** Component Identification Register 0
**Address:** 0xE0080FF0
**Offset:** 0xFF0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xD

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 13 | N/A |

### 4.14.7.39 CM7_TRCCTI_CID1

**Description:** Component Identification Register 1
**Address:** 0xE0080FF4
**Offset:** 0xFF4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x90

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 144 | N/A |

### 4.14.7.40 CM7_TRCCTI_CID2

**Description:** Component Identification Register 2
**Address:** 0xE0080FF8
**Offset:** 0xFF8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x5

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 5 | N/A |

### 4.14.7.41 CM7_TRCCTI_CID3

**Description:** Component Identification Register 3
**Address:** 0xE0080FFC
**Offset:** 0xFFC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xB1

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 177 | N/A |

### 4.14.8 ETB_CSTF

### 4.14.8.1 TRC_CSTF

#### 4.14.8.1.1 CM7_ETB_CSTF_CSTFCTL

**Description:** Funnel Control Register
**Address:** 0xE008C000
**Offset:** 0x0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer CoreSight TRM for details of register description: http://infocenter.arm.com/help/index.jsp?topic=/com.arm.doc.100536_0302_01_en/index.html |

#### 4.14.8.1.2 CM7_ETB_CSTF_CSTFPCTL

**Description:** Priority Control Register
**Address:** 0xE008C004
**Offset:** 0x4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. |

#### 4.14.8.1.3 CM7_ETB_CSTF_ITATBDATA0

**Description:** Integration Register
**Address:** 0xE008CEEC
**Offset:** 0xEEC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. |

#### 4.14.8.1.4 CM7_ETB_CSTF_ITATBCTR2

**Description:** Integration Register
**Address:** 0xE008CEF0
**Offset:** 0xEF0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. |

#### 4.14.8.1.5 CM7_ETB_CSTF_ITATBCTR1

**Description:** Integration Register
**Address:** 0xE008CEF4
**Offset:** 0xEF4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. |

#### 4.14.8.1.6 CM7_ETB_CSTF_ITATBCTR0

**Description:** Integration Register
**Address:** 0xE008CEF8
**Offset:** 0xEF8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. |

#### 4.14.8.1.7 CM7_ETB_CSTF_ITCTRL

**Description:** Integration Mode Control Register
**Address:** 0xE008CF00
**Offset:** 0xF00
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. |

#### 4.14.8.1.8 CM7_ETB_CSTF_CLAIMSET

**Description:** Claim Tag Set Register
**Address:** 0xE008CFA0
**Offset:** 0xFA0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. |

#### 4.14.8.1.9 CM7_ETB_CSTF_CLAIMCLR

**Description:** Claim Tag Clear Register
**Address:** 0xE008CFA4
**Offset:** 0xFA4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. |

#### 4.14.8.1.10 CM7_ETB_CSTF_LOCKACCESS

**Description:** Lock Access Register
**Address:** 0xE008CFB0
**Offset:** 0xFB0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. |

#### 4.14.8.1.11 CM7_ETB_CSTF_LOCKSTATUS

**Description:** Lock Status Register
**Address:** 0xE008CFB4
**Offset:** 0xFB4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. |

#### 4.14.8.1.12 CM7_ETB_CSTF_AUTHSTATUS

**Description:** Authentication Status Register
**Address:** 0xE008CFB8
**Offset:** 0xFB8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. |

#### 4.14.8.1.13 CM7_ETB_CSTF_DEVID

**Description:** Device ID
**Address:** 0xE008CFC8
**Offset:** 0xFC8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. |

#### 4.14.8.1.14 CM7_ETB_CSTF_DEVTYPE

**Description:** Device Type Identifier Register
**Address:** 0xE008CFCC
**Offset:** 0xFCC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. |

#### 4.14.8.1.15 CM7_ETB_CSTF_PID4

**Description:** Peripheral Identification Register 4
**Address:** 0xE008CFD0
**Offset:** 0xFD0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x4

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 4 | Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. |

#### 4.14.8.1.16 CM7_ETB_CSTF_PID5

**Description:** Peripheral Identification Register 5
**Address:** 0xE008CFD4
**Offset:** 0xFD4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 0 | Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. |

#### 4.14.8.1.17 CM7_ETB_CSTF_PID6

**Description:** Peripheral Identification Register 6
**Address:** 0xE008CFD8
**Offset:** 0xFD8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 0 | Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. |

#### 4.14.8.1.18 CM7_ETB_CSTF_PID7

**Description:** Peripheral Identification Register 7
**Address:** 0xE008CFDC
**Offset:** 0xFDC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 0 | Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. |

#### 4.14.8.1.19 CM7_ETB_CSTF_PID0

**Description:** Peripheral Identification Register 0
**Address:** 0xE008CFE0
**Offset:** 0xFE0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x6

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 6 | Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. |

#### 4.14.8.1.20 CM7_ETB_CSTF_PID1

**Description:** Peripheral Identification Register 1
**Address:** 0xE008CFE4
**Offset:** 0xFE4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xB9

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 185 | Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. |

#### 4.14.8.1.21 CM7_ETB_CSTF_PID2

**Description:** Peripheral Identification Register 2
**Address:** 0xE008CFE8
**Offset:** 0xFE8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x2B

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 43 | Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. |

#### 4.14.8.1.22 CM7_ETB_CSTF_PID3

**Description:** Peripheral Identification Register 3
**Address:** 0xE008CFEC
**Offset:** 0xFEC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | ECOREVNUM [7:4] | | | | None [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 4:7 | ECOREVNUM | R | R | 0 | Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. |

#### 4.14.8.1.23 CM7_ETB_CSTF_CID0

**Description:** Component Identification Register 0
**Address:** 0xE008CFF0
**Offset:** 0xFF0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xD

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 13 | Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. |

#### 4.14.8.1.24 CM7_ETB_CSTF_CID1

**Description:** Component Identification Register 1
**Address:** 0xE008CFF4
**Offset:** 0xFF4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x90

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 144 | Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. |

#### 4.14.8.1.25 CM7_ETB_CSTF_CID2

**Description:** Component Identification Register 2
**Address:** 0xE008CFF8
**Offset:** 0xFF8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x5

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 5 | Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. |

#### 4.14.8.1.26 CM7_ETB_CSTF_CID3

**Description:** Component Identification Register 3
**Address:** 0xE008CFFC
**Offset:** 0xFFC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xB1

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 177 | Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. |

### 4.14.9 ETB

#### 4.14.9.1 CM7_ETB_ETBRDP

**Description:** RAM Depth Register
**Address:** 0xE008D004
**Offset:** 0x4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. |

### 4.14.9.2 CM7_ETB_ETBSTS

**Description:** Status Register
**Address:** 0xE008D00C
**Offset:** 0xC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. |

### 4.14.9.3 CM7_ETB_ETBRRD

**Description:** RAM Read Data Register
**Address:** 0xE008D010
**Offset:** 0x10
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. |

### 4.14.9.4 CM7_ETB_ETBRRP

**Description:** RAM Read Pointer Register
**Address:** 0xE008D014
**Offset:** 0x14
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. |

### 4.14.9.5 CM7_ETB_ETBRWP

**Description:** RAM Write Pointer Register
**Address:** 0xE008D018
**Offset:** 0x18
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. |

### 4.14.9.6 CM7_ETB_ETBTRG

**Description:** Trigger Counter Register
**Address:** 0xE008D01C
**Offset:** 0x1C
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. |

### 4.14.9.7 CM7_ETB_ETBCTL

**Description:** Control Register
**Address:** 0xE008D020
**Offset:** 0x20
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. |

### 4.14.9.8 CM7_ETB_ETBRWD

**Description:** RAM Write Data Register
**Address:** 0xE008D024
**Offset:** 0x24
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. |

### 4.14.9.9 CM7_ETB_ETBFFSR

**Description:** Formatter and Flush Status Register
**Address:** 0xE008D300
**Offset:** 0x300
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. |

### 4.14.9.10 CM7_ETB_ETBFFCR

**Description:** Formatter and Flush Control Register
**Address:** 0xE008D304
**Offset:** 0x304
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. |

### 4.14.9.11 CM7_ETB_ITMISCOP0

**Description:** Integration Register
**Address:** 0xE008DEE0
**Offset:** 0xEE0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. |

### 4.14.9.12 CM7_ETB_ITTRFLINACK

**Description:** Integration Register
**Address:** 0xE008DEE4
**Offset:** 0xEE4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. |

### 4.14.9.13 CM7_ETB_ITTRFLIN

**Description:** Integration Register
**Address:** 0xE008DEE8
**Offset:** 0xEE8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. |

### 4.14.9.14 CM7_ETB_ITATBDATA0

**Description:** Integration Register
**Address:** 0xE008DEEC
**Offset:** 0xEEC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. |

### 4.14.9.15 CM7_ETB_ITATBCTR2

**Description:** Integration Register
**Address:** 0xE008DEF0
**Offset:** 0xEF0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. |

### 4.14.9.16 CM7_ETB_ITATBCTR1

**Description:** Integration Register
**Address:** 0xE008DEF4
**Offset:** 0xEF4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. |

### 4.14.9.17 CM7_ETB_ITATBCTR0

**Description:** Integration Register
**Address:** 0xE008DEF8
**Offset:** 0xEF8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. |

### 4.14.9.18 CM7_ETB_ITCTRL

**Description:** Integration Mode Control Register
**Address:** 0xE008DF00
**Offset:** 0xF00
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. |

### 4.14.9.19 CM7_ETB_CLAIMSET

**Description:** Claim Tag Set Register
**Address:** 0xE008DFA0
**Offset:** 0xFA0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register forms one half of the Claim Tag value. This location allows individual bits to be set, write, and returns the number of bits that can be set, read.
You can determine how many claim bits are implemented by reading this register. For example, if 4 bits are implemented, a read of this register will return 0x0000000F. If no claim tag is implemented, then a read of this register will return 0x00000000.
**Default:** 0xF

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:4] | | | | TAG [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | TAG | RW1S | R | 15 | A bit programmable register bank which sets the Claim Tag Value. A read will return a logic 1 for all implemented locations. |

### 4.14.9.20 CM7_ETB_CLAIMCLR

**Description:** Claim Tag Clear Register
**Address:** 0xE008DFA4
**Offset:** 0xFA4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register forms one half of the Claim Tag value. This location enables individual bits to be cleared, write, and returns the current Claim Tag value, read. The width (n) of this register can be determined from reading the Claim Tag Set Register.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:4] | | | | TAG [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | TAG | RW1C | R | 0 | A bit programmable register bank that is zero at reset. |

### 4.14.9.21 CM7_ETB_LOCKACCESS

**Description:** Lock Access Register
**Address:** 0xE008DFB0
**Offset:** 0xFB0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This is used to enable write access to device registers. If LOCKSTATUS[0] == 0x0 then this register is not present.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:4] | | | | ACCESS_CODE [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | ACCESS_CODE | RW | R | 0 | Write Access Code. A write of 0xC5ACCE55 enables further write access to this device. An invalid write will have the affect of removing write access.<br>If LOCKSTATUS[2] is set, then only bits [7:0] of this register are implemented and lock access is obtained by consecutively writing 0xC5, 0xAC, 0xCE, 0x55. Bits [31:8] are unused and any writes to them ignored. |

### 4.14.9.22 CM7_ETB_LOCKSTATUS

**Description:** Lock Status Register
**Address:** 0xE008DFB4
**Offset:** 0xFB4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This indicates the status of the Lock control mechanism. This lock prevents accidental writes by code under debug.
This register must always be present although there might not be any lock-access control mechanism. The lock mechanism, where present and locked, must block write accesses to any control register, except the Lock Access Register. For most components this covers all registers except for the Lock Access Register 0xFB0.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:3] | | | | | IMPLEMENTS_8B [2:2] | ACCESS_PERMITTED [1:1] | EXISTS [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | EXISTS | R | W | 0 | Indicates that a lock control mechanism exists for this device |
| 1 | ACCESS_PERMITTED | R | W | 0 | The values of this bit mean:<br>0 = Access permitted.<br>1 = Write access to the component is blocked. All writes to control registers are ignored. Reads are permitted |
| 2 | IMPLEMENTS_8B | R | W | 0 | This component implements an 8-bit Lock Access Register. |

### 4.14.9.23 CM7_ETB_AUTHSTATUS

**Description:** Authentication Status Register
**Address:** 0xE008DFB8
**Offset:** 0xFB8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Reports the required security level and current status of those enables. Where functionality changes on a given security level then this change in status must be reported in this register
**Default:** 0x5

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | SNIDBG [7:6] | | SIDBG [5:4] | | NSNIDBG [3:2] | | NSIDBG [1:0] | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:1 | NSIDBG | R | W | 1 | Non-Secure Invasive Debug<br>0: Functionality not implemented or controlled elsewhere<br>1: Functionality disabled<br>2: Reserved<br>3: Functionality enabled |
| 2:3 | NSNIDBG | R | W | 1 | Non-Secure Non-Invasive Debug<br>0: Functionality not implemented or controlled elsewhere<br>1: Functionality disabled<br>2: Reserved<br>3: Functionality enabled |
| 4:5 | SIDBG | R | W | 0 | Secure Invasive Debug<br>0: Functionality not implemented or controlled elsewhere<br>1: Functionality disabled<br>2: Reserved<br>3: Functionality enabled |
| 6:7 | SNIDBG | R | W | 0 | Secure Non-Invasive Debug<br>0: Functionality not implemented or controlled elsewhere<br>1: Functionality disabled<br>2: Reserved<br>3: Functionality enabled |

### 4.14.9.24 CM7_ETB_DEVID

**Description:** Device ID
**Address:** 0xE008DFC8
**Offset:** 0xFC8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register is implementation-defined for each Part Number and Designer. This indicates the capabilities of the component. The entire 32-bit field can be used because the data width is determined by the particular component. Unused bits must read as zero.
If the component is configurable then it is recommended that this register reflects any changes to a standard configuration.
**Default:** 0x40804

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:5] | | | NRMUXING [4:0] | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | NRTRIG [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:20] | | | | NRCHAN [19:16] | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:4 | NRMUXING | R | R | 4 | Indicates the number of multiplexing available on Trigger Inputs and Trigger Outputs using ASICCTL. Default value of 5'b00000 indicating no multiplexing present. Reflects the value of the Verilog `define EXTMUXNUM that you must alter accordingly. |
| 8:15 | NRTRIG | R | R | 8 | Number of ECT triggers available. |
| 16:19 | NRCHAN | R | R | 4 | Number of ECT channels available. |

### 4.14.9.25 CM7_ETB_DEVTYPE

**Description:** Device Type Identifier Register
**Address:** 0xE008DFCC
**Offset:** 0xFCC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Indicates device type
**Default:** 0x12

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | SUB_TYPE [7:4] | | | | CLASS [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | CLASS | R | R | 2 | debug control logic component |
| 4:7 | SUB_TYPE | R | R | 1 | cross trigger |

### 4.14.9.26 CM7_ETB_PID4

**Description:** Peripheral Identification Register 4
**Address:** 0xE008DFD0
**Offset:** 0xFD0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x4

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 4 | Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. |

### 4.14.9.27 CM7_ETB_PID5

**Description:** Peripheral Identification Register 5
**Address:** 0xE008DFD4
**Offset:** 0xFD4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 0 | Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. |

### 4.14.9.28 CM7_ETB_PID6

**Description:** Peripheral Identification Register 6
**Address:** 0xE008DFD8
**Offset:** 0xFD8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 0 | Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. |

### 4.14.9.29 CM7_ETB_PID7

**Description:** Peripheral Identification Register 7
**Address:** 0xE008DFDC
**Offset:** 0xFDC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 0 | Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. |

### 4.14.9.30 CM7_ETB_PID0

**Description:** Peripheral Identification Register 0
**Address:** 0xE008DFE0
**Offset:** 0xFE0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x6

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 6 | Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. |

### 4.14.9.31 CM7_ETB_PID1

**Description:** Peripheral Identification Register 1
**Address:** 0xE008DFE4
**Offset:** 0xFE4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xB9

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 185 | Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. |

### 4.14.9.32 CM7_ETB_PID2

**Description:** Peripheral Identification Register 2
**Address:** 0xE008DFE8
**Offset:** 0xFE8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x2B

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 43 | Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. |

### 4.14.9.33 CM7_ETB_PID3

**Description:** Peripheral Identification Register 3
**Address:** 0xE008DFEC
**Offset:** 0xFEC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | ECOREVNUM [7:4] | | | | None [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 4:7 | ECOREVNUM | R | R | 0 | Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. |

### 4.14.9.34 CM7_ETB_CID0

**Description:** Component Identification Register 0
**Address:** 0xE008DFF0
**Offset:** 0xFF0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xD

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 13 | Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. |

### 4.14.9.35 CM7_ETB_CID1

**Description:** Component Identification Register 1
**Address:** 0xE008DFF4
**Offset:** 0xFF4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x90

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 144 | Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. |

### 4.14.9.36 CM7_ETB_CID2

**Description:** Component Identification Register 2
**Address:** 0xE008DFF8
**Offset:** 0xFF8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x5

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 5 | Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. |

### 4.14.9.37 CM7_ETB_CID3

**Description:** Component Identification Register 3
**Address:** 0xE008DFFC
**Offset:** 0xFFC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xB1

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 177 | Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. |

### 4.14.10 TPIU

#### 4.14.10.1 CM7_TPIU_TPIU_SPSR

**Description:** Supported Port Size Register
**Address:** 0xE008E000
**Offset:** 0x0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x1

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 1 | Refer CM7 TRM and CoreSight TRM for register descriptions:<br>CoreSight TRM:<br>https://svn.design.cypress.com:18080/viewvc/chips/trunk/s40/MXS40/Platform/MXS40-SAS/SupportFiles/ARM_docs/CoreSight/DDI0480G_coresight_soc_r3p2_trm.pdf?revision=69465&view=markup<br>CM7 TRM :<br>http://infocenter.arm.com/help/index.jsp?topic=/com.arm.doc.ddi0489f/index.html |

### 4.14.10.2 CM7_TPIU_TPIU_CPSR

**Description:** Current Port Size Register
**Address:** 0xE008E004
**Offset:** 0x4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x1

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 1 | Refer DDI0480G ARM Coresight Soc-400 TRM Section 3.12 for register descriptions |

### 4.14.10.3 CM7_TPIU_TPIU_STMR

**Description:** Supported Trigger Modes Register
**Address:** 0xE008E100
**Offset:** 0x100
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x11F

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 287 | Refer DDI0480G ARM Coresight Soc-400 TRM Section 3.12 for register descriptions |

### 4.14.10.4 CM7_TPIU_TPIU_TCVR

**Description:** Trigger Counter Value Register
**Address:** 0xE008E104
**Offset:** 0x104
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer DDI0480G ARM Coresight Soc-400 TRM Section 3.12 for register descriptions |

### 4.14.10.5 CM7_TPIU_TPIU_TMR

**Description:** Trigger Multiplier register
**Address:** 0xE008E108
**Offset:** 0x108
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer DDI0480G ARM Coresight Soc-400 TRM Section 3.12 for register descriptions |

### 4.14.10.6 CM7_TPIU_TPIU_STPMR

**Description:** Supported Test Patterns/Modes register
**Address:** 0xE008E200
**Offset:** 0x200
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x3000F

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 196623 | Refer DDI0480G ARM Coresight Soc-400 TRM Section 3.12 for register descriptions |

### 4.14.10.7 CM7_TPIU_TPIU_CTPMR

**Description:** Current Test Pattern/Modes register
**Address:** 0xE008E204
**Offset:** 0x204
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer DDI0480G ARM Coresight Soc-400 TRM Section 3.12 for register descriptions |

### 4.14.10.8 CM7_TPIU_TPIU_TPRCR

**Description:** TPIU Test Pattern Repeat Counter Register
**Address:** 0xE008E208
**Offset:** 0x208
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer DDI0480G ARM Coresight Soc-400 TRM Section 3.12 for register descriptions |

### 4.14.10.9 CM7_TPIU_TPIU_FFSR

**Description:** Formatter and Flush Status Register
**Address:** 0xE008E300
**Offset:** 0x300
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer DDI0480G ARM Coresight Soc-400 TRM Section 3.12 for register descriptions |

### 4.14.10.10 CM7_TPIU_TPIU_FFCR

**Description:** Formatter and Flush Control Register
**Address:** 0xE008E304
**Offset:** 0x304
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer DDI0480G ARM Coresight Soc-400 TRM Section 3.12 for register descriptions |

### 4.14.10.11 CM7_TPIU_TPIU_FSCR

**Description:** Formatter Synchronization Counter Register
**Address:** 0xE008E308
**Offset:** 0x308
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x40

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 64 | Refer DDI0480G ARM Coresight Soc-400 TRM Section 3.12 for register descriptions |

### 4.14.10.12 CM7_TPIU_TPIU_EXCTLIPR

**Description:** TPIU EXCTL In Port Register
**Address:** 0xE008E400
**Offset:** 0x400
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 0 | Refer DDI0480G ARM Coresight Soc-400 TRM Section 3.12 for register descriptions |

### 4.14.10.13 CM7_TPIU_TPIU_EXCTLOPR

**Description:** TPIU EXCTL Out Port register
**Address:** 0xE008E404
**Offset:** 0x404
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 0 | Refer DDI0480G ARM Coresight Soc-400 TRM Section 3.12 for register descriptions |

### 4.14.10.14 CM7_TPIU_ITTRFLINACK

**Description:** Integration Test Trigger In and Flush In Acknowledge register
**Address:** 0xE008EEE4
**Offset:** 0xEE4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 0 | Refer DDI0480G ARM Coresight Soc-400 TRM Section 3.12 for register descriptions |

### 4.14.10.15 CM7_TPIU_ITTRFLIN

**Description:** Integration Test Trigger In and Flush In register
**Address:** 0xE008EEE8
**Offset:** 0xEE8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer DDI0480G ARM Coresight Soc-400 TRM Section 3.12 for register descriptions |

### 4.14.10.16 CM7_TPIU_ITATBDATA0

**Description:** Integration Test ATB Data register 0
**Address:** 0xE008EEEC
**Offset:** 0xEEC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer DDI0480G ARM Coresight Soc-400 TRM Section 3.12 for register descriptions |

### 4.14.10.17 CM7_TPIU_ITATBCTR2

**Description:** Integration Test ATB Control Register 2
**Address:** 0xE008EEF0
**Offset:** 0xEF0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer DDI0480G ARM Coresight Soc-400 TRM Section 3.12 for register descriptions |

### 4.14.10.18 CM7_TPIU_ITATBCTR1

**Description:** Integration Test ATB Control Register 1
**Address:** 0xE008EEF4
**Offset:** 0xEF4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer DDI0480G ARM Coresight Soc-400 TRM Section 3.12 for register descriptions |

### 4.14.10.19 CM7_TPIU_ITATBCTR0

**Description:** Integration Test ATB Control Register 0
**Address:** 0xE008EEF8
**Offset:** 0xEF8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | RW | R | 0 | Refer DDI0480G ARM Coresight Soc-400 TRM Section 3.12 for register descriptions |

### 4.14.10.20 CM7_TPIU_ITCTRL

**Description:** Integration Mode Control register
**Address:** 0xE008EF00
**Offset:** 0xF00
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register enables the component to switch from a functional mode, the default behavior, to integration mode where the inputs and outputs of the component can be directly controlled for the purpose of integration testing and topology solving.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:1] | | | | | | | MODE [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | MODE | RW | R | 0 | When set, the component enters integration mode, enabling topology detection or integration testing to be performed. At reset the component must enter functional mode. If no integration functionality is implemented, this register must read as zero. |

### 4.14.10.21 CM7_TPIU_CLAIMSET

**Description:** Claim Tag Set Register
**Address:** 0xE008EFA0
**Offset:** 0xFA0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register forms one half of the Claim Tag value. This location allows individual bits to be set, write, and returns the number of bits that can be set, read.
You can determine how many claim bits are implemented by reading this register. For example, if 4 bits are implemented, a read of this register will return 0x0000000F. If no claim tag is implemented, then a read of this register will return 0x00000000.
**Default:** 0xF

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:4] | | | | TAG [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | TAG | RW1S | R | 15 | A bit programmable register bank which sets the Claim Tag Value. A read will return a logic 1 for all implemented locations. |

### 4.14.10.22 CM7_TPIU_CLAIMCLR

**Description:** Claim Tag Clear Register
**Address:** 0xE008EFA4
**Offset:** 0xFA4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register forms one half of the Claim Tag value. This location enables individual bits to be cleared, write, and returns the current Claim Tag value, read. The width (n) of this register can be determined from reading the Claim Tag Set Register.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:4] | | | | TAG [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | TAG | RW1C | R | 0 | A bit programmable register bank that is zero at reset. |

### 4.14.10.23 CM7_TPIU_LOCKACCESS

**Description:** Lock Access Register
**Address:** 0xE008EFB0
**Offset:** 0xFB0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This is used to enable write access to device registers. If LOCKSTATUS[0] == 0x0 then this register is not present.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:4] | | | | ACCESS_CODE [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | ACCESS_CODE | RW | R | 0 | Write Access Code. A write of 0xC5ACCE55 enables further write access to this device. An invalid write will have the affect of removing write access.<br>If LOCKSTATUS[2] is set, then only bits [7:0] of this register are implemented and lock access is obtained by consecutively writing 0xC5, 0xAC, 0xCE, 0x55. Bits [31:8] are unused and any writes to them ignored. |

### 4.14.10.24 CM7_TPIU_LOCKSTATUS

**Description:** Lock Status Register
**Address:** 0xE008EFB4
**Offset:** 0xFB4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This indicates the status of the Lock control mechanism. This lock prevents accidental writes by code under debug.
This register must always be present although there might not be any lock-access control mechanism. The lock mechanism, where present and locked, must block write accesses to any control register, except the Lock Access Register. For most components this covers all registers except for the Lock Access Register 0xFB0.
**Default:** 0x3

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:3] | | | | | NTT [2:2] | SLK [1:1] | SLI [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | SLI | R | W | 1 | Software Lock Implemented. Indicates that a lock control mechanism is present from this interface.<br>0 Indicates that a lock control mechanism is not present from this interface. Write operations to the LAR are ignored.<br>1 Indicates that a lock control mechanism is present from this interface. |
| 1 | SLK | R | W | 1 | Software Lock Status. Returns the present lock status of the device, from the current interface.<br>0 Indicates that write operations are permitted from this interface.<br>1 Indicates that write operations are not permitted from this interface. Read operations are permitted. |
| 2 | NTT | R | W | 0 | Register size indicator. Always 0. Indicates that the LAR is implemented as 32-bit. |

### 4.14.10.25 CM7_TPIU_AUTHSTATUS

**Description:** Authentication Status register
**Address:** 0xE008EFB8
**Offset:** 0xFB8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Reports the required security level and current status of those enables. Where functionality changes on a given security level then this change in status must be reported in this register
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | SNIDBG [7:6] | | SIDBG [5:4] | | NSNIDBG [3:2] | | NSIDBG [1:0] | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:1 | NSIDBG | R | W | 0 | Non-Secure Invasive Debug<br>0: Functionality not implemented or controlled elsewhere<br>1: Functionality disabled<br>2: Reserved<br>3: Functionality enabled |
| 2:3 | NSNIDBG | R | W | 0 | Non-Secure Non-Invasive Debug<br>0: Functionality not implemented or controlled elsewhere<br>1: Functionality disabled<br>2: Reserved<br>3: Functionality enabled |
| 4:5 | SIDBG | R | W | 0 | Secure Invasive Debug<br>0: Functionality not implemented or controlled elsewhere<br>1: Functionality disabled<br>2: Reserved<br>3: Functionality enabled |
| 6:7 | SNIDBG | R | W | 0 | Secure Non-Invasive Debug<br>0: Functionality not implemented or controlled elsewhere<br>1: Functionality disabled<br>2: Reserved<br>3: Functionality enabled |

### 4.14.10.26 CM7_TPIU_DEVID

**Description:** Device Configuration register
**Address:** 0xE008EFC8
**Offset:** 0xFC8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register is implementation-defined for each Part Number and Designer. This indicates the capabilities of the component. The entire 32-bit field can be used because the data width is determined by the particular component. Unused bits must read as zero.
If the component is configurable then it is recommended that this register reflects any changes to a standard configuration.
**Default:** 0xA0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | FIFOSIZE [7:6] | | CLKRELAT [5:5] | MUXNUM [4:0] | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:12] | | | | SWOUARTNRZ [11:11] | SWOMAN [10:10] | TCLKDATA [9:9] | FIFOSIZE [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:4 | MUXNUM | R | R | 0 | Indicates the hidden level of input multiplexing. When non-zero, this value indicates the type of multiplexing on the input to the ATB. Currently only 0x00 is supported, that is, no multiplexing is present. This value helps detect the ATB structure. |
| 5 | CLKRELAT | R | R | 1 | Indicates the relationship between atclk and traceclkin. 1: atclk and traceclkin are asynchronous. |
| 6:8 | FIFOSIZE | R | R | 2 | FIFO size in powers of 2.<br>0b010: FIFO size of 4 entries, that is, 16 bytes. |
| 9 | TCLKDATA | R | R | 0 | Indicates whether trace clock plus data is supported.<br>0: Trace clock and data is supported. |
| 10 | SWOMAN | R | R | 0 | Indicates whether Serial Wire Output, Manchester encoded format, is supported.<br>0: Serial Wire Output, Manchester encoded format, is not supported. |
| 11 | SWOUARTNRZ | R | R | 0 | Indicates whether Serial Wire Output, UART or NRZ, is supported.<br>0: Serial Wire Output, UART or NRZ, is not supported. |

### 4.14.10.27 CM7_TPIU_DEVTYPE

**Description:** Device Type Identifier register
**Address:** 0xE008EFCC
**Offset:** 0xFCC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Indicates device type
**Default:** 0x11

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | SUB [7:4] | | | | MAJOR [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | MAJOR | R | R | 1 | Major classification of the type of the debug component as specified in the ARM(R) CoreSight(TM) Architecture Specification for this debug and trace component.<br>0b0001: Indicates that this component is a trace sink component. |
| 4:7 | SUB | R | R | 1 | Sub-classification of the type of the debug component as specified in the ARM(R) CoreSight(TM) Architecture Specification within the major classification as specified in the MAJOR field.<br>0b0001: Indicates that this component is a trace port component. |

### 4.14.10.28 CM7_TPIU_PID4

**Description:** Peripheral Identification Register 4
**Address:** 0xE008EFD0
**Offset:** 0xFD0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x4

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 4 | Refer DDI0480G ARM Coresight Soc-400 TRM Section 3.12 for register descriptions |

### 4.14.10.29 CM7_TPIU_PID0

**Description:** Peripheral Identification Register 0
**Address:** 0xE008EFE0
**Offset:** 0xFE0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x12

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 18 | Refer DDI0480G ARM Coresight Soc-400 TRM Section 3.12 for register descriptions |

### 4.14.10.30 CM7_TPIU_PID1

**Description:** Peripheral Identification Register 1
**Address:** 0xE008EFE4
**Offset:** 0xFE4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xB9

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 185 | Refer DDI0480G ARM Coresight Soc-400 TRM Section 3.12 for register descriptions |

### 4.14.10.31 CM7_TPIU_PID2

**Description:** Peripheral Identification Register 2
**Address:** 0xE008EFE8
**Offset:** 0xFE8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x4B

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 75 | Refer DDI0480G ARM Coresight Soc-400 TRM Section 3.12 for register descriptions |

### 4.14.10.32 CM7_TPIU_PID3

**Description:** Peripheral Identification Register 3
**Address:** 0xE008EFEC
**Offset:** 0xFEC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | ECOREVNUM [7:4] | | | | None [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 4:7 | ECOREVNUM | R | R | 0 | Refer DDI0480G ARM Coresight Soc-400 TRM Section 3.12 for register descriptions |

### 4.14.10.33 CM7_TPIU_CID0

**Description:** Component Identification Register 0
**Address:** 0xE008EFF0
**Offset:** 0xFF0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xD

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 13 | Refer DDI0480G ARM Coresight Soc-400 TRM Section 3.12 for register descriptions |

### 4.14.10.34 CM7_TPIU_CID1

**Description:** Component Identification Register 1
**Address:** 0xE008EFF4
**Offset:** 0xFF4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x90

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 144 | Refer DDI0480G ARM Coresight Soc-400 TRM Section 3.12 for register descriptions |

### 4.14.10.35 CM7_TPIU_CID2

**Description:** Component Identification Register 2
**Address:** 0xE008EFF8
**Offset:** 0xFF8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x5

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 5 | Refer DDI0480G ARM Coresight Soc-400 TRM Section 3.12 for register descriptions |

### 4.14.10.36 CM7_TPIU_CID3

**Description:** Component Identification Register 3
**Address:** 0xE008EFFC
**Offset:** 0xFFC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xB1

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 177 | Refer DDI0480G ARM Coresight Soc-400 TRM Section 3.12 for register descriptions |

### 4.14.11 ROMTABLE

#### 4.14.11.1 CM7_ROMTABLE_TRC_CTI

**Description:** CM7 CoreSight ROM Table Peripheral #0
**Address:** 0xE00BF000
**Offset:** 0x0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xFFFC1003

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | | 4294709251 | Offset to TRC CTI ROM Table |

### 4.14.11.2 CM7_ROMTABLE_TRC_TRC_CSTF

**Description:** CM7 CoreSight ROM Table Peripheral #1
**Address:** 0xE00BF004
**Offset:** 0x4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xFFFCD003

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | | 4294758403 | Offset to CSTF ROM Table |

### 4.14.11.3 CM7_ROMTABLE_TRC_ETB

**Description:** CM7 CoreSight ROM Table Peripheral #2
**Address:** 0xE00BF008
**Offset:** 0x8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xFFFCE003

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | | 4294762499 | Offset to ETB ROM Table |

### 4.14.11.4 CM7_ROMTABLE_TRC_TPIU

**Description:** CM7 CoreSight ROM Table Peripheral #3
**Address:** 0xE00BF00C
**Offset:** 0xC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xFFFCF003

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | | 4294766595 | Offset to TPIU ROM Table |

### 4.14.11.5 CM7_ROMTABLE_TRC_CSMT

**Description:** CM7 CoreSight ROM Table Memory Type
**Address:** 0xE00BFFCC
**Offset:** 0xFCC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x1

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | | 1 | Memory Type |

### 4.14.11.6 CM7_ROMTABLE_TRC_PID4

**Description:** CM7 CoreSight ROM Table Peripheral ID #4
**Address:** 0xE00BFFD0
**Offset:** 0xFD0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x4

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | | 4 | Peripheral ID #4 |

### 4.14.11.7 CM7_ROMTABLE_TRC_PID0

**Description:** CM7 CoreSight ROM Table Peripheral ID #0
**Address:** 0xE00BFFE0
**Offset:** 0xFE0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xC0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | | 192 | Peripheral ID #0 |

### 4.14.11.8 CM7_ROMTABLE_TRC_PID1

**Description:** CM7 CoreSight ROM Table Peripheral ID #1
**Address:** 0xE00BFFE4
**Offset:** 0xFE4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xB4

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | | 180 | Peripheral ID #1 |

### 4.14.11.9 CM7_ROMTABLE_TRC_PID2

**Description:** CM7 CoreSight ROM Table Peripheral ID #2
**Address:** 0xE00BFFE8
**Offset:** 0xFE8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xB

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | | 11 | Peripheral ID #2 |

### 4.14.11.10 CM7_ROMTABLE_TRC_PID3

**Description:** CM7 CoreSight ROM Table Peripheral ID #3
**Address:** 0xE00BFFEC
**Offset:** 0xFEC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | | 0 | Peripheral ID #3 |

### 4.14.11.11 CM7_ROMTABLE_TRC_CID0

**Description:** CM7 CoreSight ROM Table Component ID #0
**Address:** 0xE00BFFF0
**Offset:** 0xFF0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xD

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | | 13 | Component ID #0 |

### 4.14.11.12 CM7_ROMTABLE_TRC_CID1

**Description:** CM7 CoreSight ROM Table Component ID #1
**Address:** 0xE00BFFF4
**Offset:** 0xFF4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x10

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | | 16 | Component ID #1 |

### 4.14.11.13 CM7_ROMTABLE_TRC_CID2

**Description:** CM7 CoreSight ROM Table Component ID #2
**Address:** 0xE00BFFF8
**Offset:** 0xFF8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x5

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | | 5 | Component ID #2 |

### 4.14.11.14 CM7_ROMTABLE_TRC_CID3

**Description:** CM7 CoreSight ROM Table Component ID #3
**Address:** 0xE00BFFFC
**Offset:** 0xFFC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xB1

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | | 177 | Component ID #3 |

### 4.14.12 ROMTABLE

#### 4.14.12.1 CM7_ROMTABLE_CM7

**Description:** CM7 CoreSight ROM Table Peripheral #0
**Address:** 0xE00FE000
**Offset:** 0x0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x1003

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | | 4099 | Offset to CM7 ROM Table |

### 4.14.12.2 CM7_ROMTABLE_CM7_ETM

**Description:** CM7 CoreSight ROM Table Peripheral #1
**Address:** 0xE00FE004
**Offset:** 0x4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xFFF43003

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | | 4294193155 | Offset to ETM ROM Table |

### 4.14.12.3 CM7_ROMTABLE_CM7_CTI

**Description:** CM7 CoreSight ROM Table Peripheral #2
**Address:** 0xE00FE008
**Offset:** 0x8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xFFF44003

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | | 4294197251 | Offset to CTI ROM Table |

### 4.14.12.4 CM7_ROMTABLE_DBG_TRC_ROM

**Description:** CM7 CoreSight ROM Table Peripheral #3
**Address:** 0xE00FE010
**Offset:** 0x10
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xFFFC1003

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | | 4294709251 | Offset to DBG_TRC ROM Table |

### 4.14.12.5 CM7_ROMTABLE_CSMT

**Description:** CM7 CoreSight ROM Table Memory Type
**Address:** 0xE00FEFCC
**Offset:** 0xFCC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x1

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | | 1 | Memory Type |

### 4.14.12.6 CM7_ROMTABLE_PID4

**Description:** CM7 CoreSight ROM Table Peripheral ID #4
**Address:** 0xE00FEFD0
**Offset:** 0xFD0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x4

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | | 4 | Peripheral ID #4 |

### 4.14.12.7 CM7_ROMTABLE_PID0

**Description:** CM7 CoreSight ROM Table Peripheral ID #0
**Address:** 0xE00FEFE0
**Offset:** 0xFE0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xC0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | | 192 | Peripheral ID #0 |

### 4.14.12.8 CM7_ROMTABLE_PID1

**Description:** CM7 CoreSight ROM Table Peripheral ID #1
**Address:** 0xE00FEFE4
**Offset:** 0xFE4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xB4

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | | 180 | Peripheral ID #1 |

### 4.14.12.9 CM7_ROMTABLE_PID2

**Description:** CM7 CoreSight ROM Table Peripheral ID #2
**Address:** 0xE00FEFE8
**Offset:** 0xFE8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xB

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | | 11 | Peripheral ID #2 |

### 4.14.12.10 CM7_ROMTABLE_PID3

**Description:** CM7 CoreSight ROM Table Peripheral ID #3
**Address:** 0xE00FEFEC
**Offset:** 0xFEC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | | 0 | Peripheral ID #3 |

### 4.14.12.11 CM7_ROMTABLE_CID0

**Description:** CM7 CoreSight ROM Table Component ID #0
**Address:** 0xE00FEFF0
**Offset:** 0xFF0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xD

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | | 13 | Component ID #0 |

### 4.14.12.12 CM7_ROMTABLE_CID1

**Description:** CM7 CoreSight ROM Table Component ID #1
**Address:** 0xE00FEFF4
**Offset:** 0xFF4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x10

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | | 16 | Component ID #1 |

### 4.14.12.13 CM7_ROMTABLE_CID2

**Description:** CM7 CoreSight ROM Table Component ID #2
**Address:** 0xE00FEFF8
**Offset:** 0xFF8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x5

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | | 5 | Component ID #2 |

### 4.14.12.14 CM7_ROMTABLE_CID3

**Description:** CM7 CoreSight ROM Table Component ID #3
**Address:** 0xE00FEFFC
**Offset:** 0xFFC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xB1

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | | 177 | Component ID #3 |

### 4.14.13 ROM

#### 4.14.13.1 CM7_ROM_SCS

**Description:** CM7 CoreSight ROM Table Peripheral #0
**Address:** 0xE00FF000
**Offset:** 0x0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xFFF0F003

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | | 4293980163 | Offset to SCS ROM Table |

### 4.14.13.2 CM7_ROM_DWT

**Description:** CM7 CoreSight ROM Table Peripheral #1
**Address:** 0xE00FF004
**Offset:** 0x4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xFFF02003

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | | 4293926915 | Offset to DWT ROM Table |

### 4.14.13.3 CM7_ROM_FPB

**Description:** CM7 CoreSight ROM Table Peripheral #2
**Address:** 0xE00FF008
**Offset:** 0x8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xFFF03003

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | | 4293931011 | Offset to FPB ROM Table |

### 4.14.13.4 CM7_ROM_ITM

**Description:** CM7 CoreSight ROM Table Peripheral #3
**Address:** 0xE00FF00C
**Offset:** 0xC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xFFF01003

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | | 4293922819 | Offset to ITM ROM Table |

### 4.14.13.5 CM7_ROM_CSMT

**Description:** CM7 CoreSight ROM Table Memory Type
**Address:** 0xE00FFFCC
**Offset:** 0xFCC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x1

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | | 1 | Memory Type |

### 4.14.13.6 CM7_ROM_PID4

**Description:** CM7 CoreSight ROM Table Peripheral ID #4
**Address:** 0xE00FFFD0
**Offset:** 0xFD0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x4

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | | 4 | Peripheral ID #4 |

### 4.14.13.7 CM7_ROM_PID0

**Description:** CM7 CoreSight ROM Table Peripheral ID #0
**Address:** 0xE00FFFE0
**Offset:** 0xFE0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xC7

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | | 199 | Peripheral ID #0 |

### 4.14.13.8 CM7_ROM_PID1

**Description:** CM7 CoreSight ROM Table Peripheral ID #1
**Address:** 0xE00FFFE4
**Offset:** 0xFE4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xB4

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | | 180 | Peripheral ID #1 |

### 4.14.13.9 CM7_ROM_PID2

**Description:** CM7 CoreSight ROM Table Peripheral ID #2
**Address:** 0xE00FFFE8
**Offset:** 0xFE8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xB

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | | 11 | Peripheral ID #2 |

### 4.14.13.10 CM7_ROM_PID3

**Description:** CM7 CoreSight ROM Table Peripheral ID #3
**Address:** 0xE00FFFEC
**Offset:** 0xFEC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | | 0 | Peripheral ID #3 |

### 4.14.13.11 CM7_ROM_CID0

**Description:** CM7 CoreSight ROM Table Component ID #0
**Address:** 0xE00FFFF0
**Offset:** 0xFF0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xD

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | | 13 | Component ID #0 |

### 4.14.13.12 CM7_ROM_CID1

**Description:** CM7 CoreSight ROM Table Component ID #1
**Address:** 0xE00FFFF4
**Offset:** 0xFF4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x10

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | | 16 | Component ID #1 |

### 4.14.13.13 CM7_ROM_CID2

**Description:** CM7 CoreSight ROM Table Component ID #2
**Address:** 0xE00FFFF8
**Offset:** 0xFF8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x5

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | | 5 | Component ID #2 |

### 4.14.13.14 CM7_ROM_CID3

**Description:** CM7 CoreSight ROM Table Component ID #3
**Address:** 0xE00FFFFC
**Offset:** 0xFFC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xB1

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | | 177 | Component ID #3 |

# 5 CPUSS

**Description** CPU subsystem (CPUSS)
**Base Address** 0x40200000
**Size** 0x10000
**Slave Num** MMIO2 - 0

| Register Name | Address | Permission | Description |
|---|---|---|---|
| CPUSS_IDENTITY | 0x40200000 | FULL | Identity |
| CPUSS_CM7_0_STATUS | 0x40200004 | FULL | CM7 0 status |
| CPUSS_FAST_0_CLOCK_CTL | 0x40200008 | FULL | Fast 0 clock control |
| CPUSS_CM7_0_CTL | 0x4020000C | FULL | CM7 0 control |
| CPUSS_CM7_0_INT_STATUS0 | 0x40200100 | FULL | CM7 0 interrupt status |
| CPUSS_CM7_0_INT_STATUS1 | 0x40200104 | FULL | CM7 0 interrupt status |
| CPUSS_CM7_0_INT_STATUS2 | 0x40200108 | FULL | CM7 0 interrupt status |
| CPUSS_CM7_0_INT_STATUS3 | 0x4020010C | FULL | CM7 0 interrupt status |
| CPUSS_CM7_0_INT_STATUS4 | 0x40200110 | FULL | CM7 0 interrupt status |
| CPUSS_CM7_0_INT_STATUS5 | 0x40200114 | FULL | CM7 0 interrupt status |
| CPUSS_CM7_0_INT_STATUS6 | 0x40200118 | FULL | CM7 0 interrupt status |
| CPUSS_CM7_0_INT_STATUS7 | 0x4020011C | FULL | CM7 0 interrupt status |
| CPUSS_CM7_0_VECTOR_TABLE_BASE | 0x40200200 | FULL | CM7 0 vector table base |
| CPUSS_CM7_0_NMI_CTL0 | 0x40200240 | FULL | CM7 0 NMI control |
| CPUSS_CM7_0_NMI_CTL1 | 0x40200244 | FULL | CM7 0 NMI control |
| CPUSS_CM7_0_NMI_CTL2 | 0x40200248 | FULL | CM7 0 NMI control |
| CPUSS_CM7_0_NMI_CTL3 | 0x4020024C | FULL | CM7 0 NMI control |
| CPUSS_TRC_DBG_CLOCK_CTL | 0x40200320 | FULL | Trace and debug clock control |
| CPUSS_CM7_1_STATUS | 0x40200404 | FULL | CM7 1status |
| CPUSS_FAST_1_CLOCK_CTL | 0x40200408 | FULL | Fast 1 clock control |
| CPUSS_CM7_1_CTL | 0x4020040C | FULL | CM7 1 control |
| CPUSS_CM7_1_INT_STATUS0 | 0x40200500 | FULL | CM7 1 interrupt status |
| CPUSS_CM7_1_INT_STATUS1 | 0x40200504 | FULL | CM7 1 interrupt status |
| CPUSS_CM7_1_INT_STATUS2 | 0x40200508 | FULL | CM7 1 interrupt status |
| CPUSS_CM7_1_INT_STATUS3 | 0x4020050C | FULL | CM7 1 interrupt status |
| CPUSS_CM7_1_INT_STATUS4 | 0x40200510 | FULL | CM7 1 interrupt status |
| CPUSS_CM7_1_INT_STATUS5 | 0x40200514 | FULL | CM7 1 interrupt status |
| CPUSS_CM7_1_INT_STATUS6 | 0x40200518 | FULL | CM7 1 interrupt status |
| CPUSS_CM7_1_INT_STATUS7 | 0x4020051C | FULL | CM7 1 interrupt status |
| CPUSS_CM7_1_VECTOR_TABLE_BASE | 0x40200600 | FULL | CM7 1 vector table base |
| CPUSS_CM7_1_NMI_CTL0 | 0x40200640 | FULL | CM7 1 NMI control |
| CPUSS_CM7_1_NMI_CTL1 | 0x40200644 | FULL | CM7 1 NMI control |
| CPUSS_CM7_1_NMI_CTL2 | 0x40200648 | FULL | CM7 1 NMI control |
| CPUSS_CM7_1_NMI_CTL3 | 0x4020064C | FULL | CM7 1 NMI control |
| CPUSS_CM0_CTL | 0x40201000 | FULL | CM0+ control |
| CPUSS_CM0_STATUS | 0x40201004 | FULL | CM0+ status |
| CPUSS_SLOW_CLOCK_CTL | 0x40201008 | FULL | Slow clock control |
| CPUSS_PERI_CLOCK_CTL | 0x4020100C | FULL | Peripheral interconnect clock control |
| CPUSS_MEM_CLOCK_CTL | 0x40201010 | FULL | Memory clock control |
| CPUSS_CM0_INT0_STATUS | 0x40201100 | FULL | CM0+ interrupt 0 status |
| CPUSS_CM0_INT1_STATUS | 0x40201104 | FULL | CM0+ interrupt 1 status |
| CPUSS_CM0_INT2_STATUS | 0x40201108 | FULL | CM0+ interrupt 2 status |
| CPUSS_CM0_INT3_STATUS | 0x4020110C | FULL | CM0+ interrupt 3 status |
| CPUSS_CM0_INT4_STATUS | 0x40201110 | FULL | CM0+ interrupt 4 status |
| CPUSS_CM0_INT5_STATUS | 0x40201114 | FULL | CM0+ interrupt 5 status |
| CPUSS_CM0_INT6_STATUS | 0x40201118 | FULL | CM0+ interrupt 6 status |
| CPUSS_CM0_INT7_STATUS | 0x4020111C | FULL | CM0+ interrupt 7 status |
| CPUSS_CM0_VECTOR_TABLE_BASE | 0x40201120 | FULL | CM0+ vector table base |
| CPUSS_CM0_NMI_CTL0 | 0x40201140 | FULL | CM0+ NMI control |
| CPUSS_CM0_NMI_CTL1 | 0x40201144 | FULL | CM0+ NMI control |
| CPUSS_CM0_NMI_CTL2 | 0x40201148 | FULL | CM0+ NMI control |
| CPUSS_CM0_NMI_CTL3 | 0x4020114C | FULL | CM0+ NMI control |
| CPUSS_CM7_0_PWR_CTL | 0x40201200 | FULL | CM7 0 power control |
| CPUSS_CM7_0_PWR_DELAY_CTL | 0x40201204 | FULL | CM7 0 power delay control |
| CPUSS_CM7_1_PWR_CTL | 0x40201210 | FULL | CM7 1 power control |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| CPUSS_CM7_1_PWR_DELAY_CTL | 0x40201214 | FULL | CM7 1 power delay control |
| CPUSS_RAM0_CTL0 | 0x40201300 | FULL | RAM 0 control |
| CPUSS_RAM0_STATUS | 0x40201304 | FULL | RAM 0 status |
| CPUSS_RAM0_PWR_MACRO_CTL0 | 0x40201340 | FULL | RAM 0 power control |
| CPUSS_RAM0_PWR_MACRO_CTL1 | 0x40201344 | FULL | RAM 0 power control |
| CPUSS_RAM0_PWR_MACRO_CTL2 | 0x40201348 | FULL | RAM 0 power control |
| CPUSS_RAM0_PWR_MACRO_CTL3 | 0x4020134C | FULL | RAM 0 power control |
| CPUSS_RAM0_PWR_MACRO_CTL4 | 0x40201350 | FULL | RAM 0 power control |
| CPUSS_RAM0_PWR_MACRO_CTL5 | 0x40201354 | FULL | RAM 0 power control |
| CPUSS_RAM0_PWR_MACRO_CTL6 | 0x40201358 | FULL | RAM 0 power control |
| CPUSS_RAM0_PWR_MACRO_CTL7 | 0x4020135C | FULL | RAM 0 power control |
| CPUSS_RAM0_PWR_MACRO_CTL8 | 0x40201360 | FULL | RAM 0 power control |
| CPUSS_RAM0_PWR_MACRO_CTL9 | 0x40201364 | FULL | RAM 0 power control |
| CPUSS_RAM0_PWR_MACRO_CTL10 | 0x40201368 | FULL | RAM 0 power control |
| CPUSS_RAM0_PWR_MACRO_CTL11 | 0x4020136C | FULL | RAM 0 power control |
| CPUSS_RAM0_PWR_MACRO_CTL12 | 0x40201370 | FULL | RAM 0 power control |
| CPUSS_RAM0_PWR_MACRO_CTL13 | 0x40201374 | FULL | RAM 0 power control |
| CPUSS_RAM0_PWR_MACRO_CTL14 | 0x40201378 | FULL | RAM 0 power control |
| CPUSS_RAM0_PWR_MACRO_CTL15 | 0x4020137C | FULL | RAM 0 power control |
| CPUSS_RAM1_CTL0 | 0x40201380 | FULL | RAM 1 control |
| CPUSS_RAM1_STATUS | 0x40201384 | FULL | RAM 1 status |
| CPUSS_RAM1_PWR_CTL | 0x40201388 | FULL | RAM 1 power control |
| CPUSS_RAM2_CTL0 | 0x402013A0 | FULL | RAM 2 control |
| CPUSS_RAM2_STATUS | 0x402013A4 | FULL | RAM 2 status |
| CPUSS_RAM2_PWR_CTL | 0x402013A8 | FULL | RAM 2 power control |
| CPUSS_RAM_PWR_DELAY_CTL | 0x402013C0 | FULL | Power up delay used for all SRAM power domains |
| CPUSS_ROM_CTL | 0x402013C4 | FULL | ROM control |
| CPUSS_ECC_CTL | 0x402013C8 | FULL | ECC control |
| CPUSS_PRODUCT_ID | 0x40201400 | FULL | Product identifier and version (same as CoreSight RomTables) |
| CPUSS_DP_STATUS | 0x40201410 | FULL | Debug port status |
| CPUSS_AP_CTL | 0x40201414 | FULL | Access port control |
| CPUSS_BUFF_CTL | 0x40201500 | FULL | Buffer control |
| CPUSS_SYSTICK_CTL | 0x40201600 | FULL | SysTick timer control |
| CPUSS_CAL_SUP_SET | 0x40201800 | FULL | Calibration support set and read |
| CPUSS_CAL_SUP_CLR | 0x40201804 | FULL | Calibration support clear and reset |
| CPUSS_CM0_PC_CTL | 0x40202000 | READ | CM0+ protection context control |
| CPUSS_CM0_PC0_HANDLER | 0x40202040 | READ | CM0+ protection context 0 handler |
| CPUSS_CM0_PC1_HANDLER | 0x40202044 | READ | CM0+ protection context 1 handler |
| CPUSS_CM0_PC2_HANDLER | 0x40202048 | READ | CM0+ protection context 2 handler |
| CPUSS_CM0_PC3_HANDLER | 0x4020204C | READ | CM0+ protection context 3 handler |
| CPUSS_PROTECTION | 0x402020C4 | READ | Protection status |
| CPUSS_TRIM_ROM_CTL | 0x40202100 | READ | ROM trim control |
| CPUSS_TRIM_RAM_CTL | 0x40202104 | READ | RAM trim control for less than 100MHz SRAMs |
| CPUSS_TRIM_RAM200_CTL | 0x40202108 | READ | RAM trim control for 100MHz - 200MHz SRAMs |
| CPUSS_TRIM_RAM350_CTL | 0x4020210C | READ | RAM trim control for more than 200MHz SRAMs |
| CPUSS_CM0_SYSTEM_INT_CTL0 | 0x40208000 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL1 | 0x40208004 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL2 | 0x40208008 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL3 | 0x4020800C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL4 | 0x40208010 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL5 | 0x40208014 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL6 | 0x40208018 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL7 | 0x4020801C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL8 | 0x40208020 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL9 | 0x40208024 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL10 | 0x40208028 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL11 | 0x4020802C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL12 | 0x40208030 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL13 | 0x40208034 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL14 | 0x40208038 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL15 | 0x4020803C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL16 | 0x40208040 | FULL | CM0+ system interrupt control |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| CPUSS_CM0_SYSTEM_INT_CTL17 | 0x40208044 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL18 | 0x40208048 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL19 | 0x4020804C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL20 | 0x40208050 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL21 | 0x40208054 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL22 | 0x40208058 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL23 | 0x4020805C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL24 | 0x40208060 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL25 | 0x40208064 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL26 | 0x40208068 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL27 | 0x4020806C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL28 | 0x40208070 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL29 | 0x40208074 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL30 | 0x40208078 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL31 | 0x4020807C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL32 | 0x40208080 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL33 | 0x40208084 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL34 | 0x40208088 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL35 | 0x4020808C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL36 | 0x40208090 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL37 | 0x40208094 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL38 | 0x40208098 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL39 | 0x4020809C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL40 | 0x402080A0 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL41 | 0x402080A4 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL42 | 0x402080A8 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL43 | 0x402080AC | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL44 | 0x402080B0 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL45 | 0x402080B4 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL46 | 0x402080B8 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL47 | 0x402080BC | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL48 | 0x402080C0 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL49 | 0x402080C4 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL50 | 0x402080C8 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL51 | 0x402080CC | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL52 | 0x402080D0 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL53 | 0x402080D4 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL54 | 0x402080D8 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL55 | 0x402080DC | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL56 | 0x402080E0 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL57 | 0x402080E4 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL58 | 0x402080E8 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL59 | 0x402080EC | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL60 | 0x402080F0 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL61 | 0x402080F4 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL62 | 0x402080F8 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL63 | 0x402080FC | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL64 | 0x40208100 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL65 | 0x40208104 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL66 | 0x40208108 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL67 | 0x4020810C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL68 | 0x40208110 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL69 | 0x40208114 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL70 | 0x40208118 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL71 | 0x4020811C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL72 | 0x40208120 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL73 | 0x40208124 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL74 | 0x40208128 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL75 | 0x4020812C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL76 | 0x40208130 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL77 | 0x40208134 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL78 | 0x40208138 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL79 | 0x4020813C | FULL | CM0+ system interrupt control |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| CPUSS_CM0_SYSTEM_INT_CTL80 | 0x40208140 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL81 | 0x40208144 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL82 | 0x40208148 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL83 | 0x4020814C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL84 | 0x40208150 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL85 | 0x40208154 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL86 | 0x40208158 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL87 | 0x4020815C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL88 | 0x40208160 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL89 | 0x40208164 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL90 | 0x40208168 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL91 | 0x4020816C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL92 | 0x40208170 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL93 | 0x40208174 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL94 | 0x40208178 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL95 | 0x4020817C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL96 | 0x40208180 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL97 | 0x40208184 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL98 | 0x40208188 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL99 | 0x4020818C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL100 | 0x40208190 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL101 | 0x40208194 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL102 | 0x40208198 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL103 | 0x4020819C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL104 | 0x402081A0 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL105 | 0x402081A4 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL106 | 0x402081A8 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL107 | 0x402081AC | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL108 | 0x402081B0 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL109 | 0x402081B4 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL110 | 0x402081B8 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL111 | 0x402081BC | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL112 | 0x402081C0 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL113 | 0x402081C4 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL114 | 0x402081C8 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL115 | 0x402081CC | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL116 | 0x402081D0 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL117 | 0x402081D4 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL118 | 0x402081D8 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL119 | 0x402081DC | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL120 | 0x402081E0 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL121 | 0x402081E4 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL122 | 0x402081E8 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL123 | 0x402081EC | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL124 | 0x402081F0 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL125 | 0x402081F4 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL126 | 0x402081F8 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL127 | 0x402081FC | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL128 | 0x40208200 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL129 | 0x40208204 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL130 | 0x40208208 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL131 | 0x4020820C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL132 | 0x40208210 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL133 | 0x40208214 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL134 | 0x40208218 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL135 | 0x4020821C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL136 | 0x40208220 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL137 | 0x40208224 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL138 | 0x40208228 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL139 | 0x4020822C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL140 | 0x40208230 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL141 | 0x40208234 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL142 | 0x40208238 | FULL | CM0+ system interrupt control |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| CPUSS_CM0_SYSTEM_INT_CTL143 | 0x4020823C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL144 | 0x40208240 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL145 | 0x40208244 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL146 | 0x40208248 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL147 | 0x4020824C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL148 | 0x40208250 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL149 | 0x40208254 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL150 | 0x40208258 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL151 | 0x4020825C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL152 | 0x40208260 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL153 | 0x40208264 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL154 | 0x40208268 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL155 | 0x4020826C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL156 | 0x40208270 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL157 | 0x40208274 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL158 | 0x40208278 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL159 | 0x4020827C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL160 | 0x40208280 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL161 | 0x40208284 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL162 | 0x40208288 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL163 | 0x4020828C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL164 | 0x40208290 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL165 | 0x40208294 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL166 | 0x40208298 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL167 | 0x4020829C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL168 | 0x402082A0 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL169 | 0x402082A4 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL170 | 0x402082A8 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL171 | 0x402082AC | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL172 | 0x402082B0 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL173 | 0x402082B4 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL174 | 0x402082B8 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL175 | 0x402082BC | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL176 | 0x402082C0 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL177 | 0x402082C4 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL178 | 0x402082C8 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL179 | 0x402082CC | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL180 | 0x402082D0 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL181 | 0x402082D4 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL182 | 0x402082D8 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL183 | 0x402082DC | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL184 | 0x402082E0 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL185 | 0x402082E4 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL186 | 0x402082E8 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL187 | 0x402082EC | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL188 | 0x402082F0 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL189 | 0x402082F4 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL190 | 0x402082F8 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL191 | 0x402082FC | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL192 | 0x40208300 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL193 | 0x40208304 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL194 | 0x40208308 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL195 | 0x4020830C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL196 | 0x40208310 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL197 | 0x40208314 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL198 | 0x40208318 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL199 | 0x4020831C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL200 | 0x40208320 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL201 | 0x40208324 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL202 | 0x40208328 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL203 | 0x4020832C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL204 | 0x40208330 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL205 | 0x40208334 | FULL | CM0+ system interrupt control |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| CPUSS_CM0_SYSTEM_INT_CTL206 | 0x40208338 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL207 | 0x4020833C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL208 | 0x40208340 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL209 | 0x40208344 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL210 | 0x40208348 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL211 | 0x4020834C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL212 | 0x40208350 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL213 | 0x40208354 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL214 | 0x40208358 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL215 | 0x4020835C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL216 | 0x40208360 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL217 | 0x40208364 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL218 | 0x40208368 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL219 | 0x4020836C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL220 | 0x40208370 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL221 | 0x40208374 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL222 | 0x40208378 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL223 | 0x4020837C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL224 | 0x40208380 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL225 | 0x40208384 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL226 | 0x40208388 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL227 | 0x4020838C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL228 | 0x40208390 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL229 | 0x40208394 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL230 | 0x40208398 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL231 | 0x4020839C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL232 | 0x402083A0 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL233 | 0x402083A4 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL234 | 0x402083A8 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL235 | 0x402083AC | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL236 | 0x402083B0 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL237 | 0x402083B4 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL238 | 0x402083B8 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL239 | 0x402083BC | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL240 | 0x402083C0 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL241 | 0x402083C4 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL242 | 0x402083C8 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL243 | 0x402083CC | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL244 | 0x402083D0 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL245 | 0x402083D4 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL246 | 0x402083D8 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL247 | 0x402083DC | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL248 | 0x402083E0 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL249 | 0x402083E4 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL250 | 0x402083E8 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL251 | 0x402083EC | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL252 | 0x402083F0 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL253 | 0x402083F4 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL254 | 0x402083F8 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL255 | 0x402083FC | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL256 | 0x40208400 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL257 | 0x40208404 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL258 | 0x40208408 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL259 | 0x4020840C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL260 | 0x40208410 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL261 | 0x40208414 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL262 | 0x40208418 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL263 | 0x4020841C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL264 | 0x40208420 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL265 | 0x40208424 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL266 | 0x40208428 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL267 | 0x4020842C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL268 | 0x40208430 | FULL | CM0+ system interrupt control |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| CPUSS_CM0_SYSTEM_INT_CTL269 | 0x40208434 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL270 | 0x40208438 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL271 | 0x4020843C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL272 | 0x40208440 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL273 | 0x40208444 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL274 | 0x40208448 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL275 | 0x4020844C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL276 | 0x40208450 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL277 | 0x40208454 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL278 | 0x40208458 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL279 | 0x4020845C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL280 | 0x40208460 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL281 | 0x40208464 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL282 | 0x40208468 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL283 | 0x4020846C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL284 | 0x40208470 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL285 | 0x40208474 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL286 | 0x40208478 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL287 | 0x4020847C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL288 | 0x40208480 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL289 | 0x40208484 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL290 | 0x40208488 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL291 | 0x4020848C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL292 | 0x40208490 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL293 | 0x40208494 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL294 | 0x40208498 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL295 | 0x4020849C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL296 | 0x402084A0 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL297 | 0x402084A4 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL298 | 0x402084A8 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL299 | 0x402084AC | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL300 | 0x402084B0 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL301 | 0x402084B4 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL302 | 0x402084B8 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL303 | 0x402084BC | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL304 | 0x402084C0 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL305 | 0x402084C4 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL306 | 0x402084C8 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL307 | 0x402084CC | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL308 | 0x402084D0 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL309 | 0x402084D4 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL310 | 0x402084D8 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL311 | 0x402084DC | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL312 | 0x402084E0 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL313 | 0x402084E4 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL314 | 0x402084E8 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL315 | 0x402084EC | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL316 | 0x402084F0 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL317 | 0x402084F4 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL318 | 0x402084F8 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL319 | 0x402084FC | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL320 | 0x40208500 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL321 | 0x40208504 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL322 | 0x40208508 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL323 | 0x4020850C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL324 | 0x40208510 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL325 | 0x40208514 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL326 | 0x40208518 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL327 | 0x4020851C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL328 | 0x40208520 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL329 | 0x40208524 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL330 | 0x40208528 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL331 | 0x4020852C | FULL | CM0+ system interrupt control |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| CPUSS_CM0_SYSTEM_INT_CTL332 | 0x40208530 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL333 | 0x40208534 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL334 | 0x40208538 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL335 | 0x4020853C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL336 | 0x40208540 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL337 | 0x40208544 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL338 | 0x40208548 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL339 | 0x4020854C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL340 | 0x40208550 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL341 | 0x40208554 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL342 | 0x40208558 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL343 | 0x4020855C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL344 | 0x40208560 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL345 | 0x40208564 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL346 | 0x40208568 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL347 | 0x4020856C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL348 | 0x40208570 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL349 | 0x40208574 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL350 | 0x40208578 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL351 | 0x4020857C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL352 | 0x40208580 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL353 | 0x40208584 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL354 | 0x40208588 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL355 | 0x4020858C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL356 | 0x40208590 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL357 | 0x40208594 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL358 | 0x40208598 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL359 | 0x4020859C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL360 | 0x402085A0 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL361 | 0x402085A4 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL362 | 0x402085A8 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL363 | 0x402085AC | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL364 | 0x402085B0 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL365 | 0x402085B4 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL366 | 0x402085B8 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL367 | 0x402085BC | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL368 | 0x402085C0 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL369 | 0x402085C4 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL370 | 0x402085C8 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL371 | 0x402085CC | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL372 | 0x402085D0 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL373 | 0x402085D4 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL374 | 0x402085D8 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL375 | 0x402085DC | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL376 | 0x402085E0 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL377 | 0x402085E4 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL378 | 0x402085E8 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL379 | 0x402085EC | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL380 | 0x402085F0 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL381 | 0x402085F4 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL382 | 0x402085F8 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL383 | 0x402085FC | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL384 | 0x40208600 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL385 | 0x40208604 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL386 | 0x40208608 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL387 | 0x4020860C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL388 | 0x40208610 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL389 | 0x40208614 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL390 | 0x40208618 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL391 | 0x4020861C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL392 | 0x40208620 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL393 | 0x40208624 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL394 | 0x40208628 | FULL | CM0+ system interrupt control |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| CPUSS_CM0_SYSTEM_INT_CTL395 | 0x4020862C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL396 | 0x40208630 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL397 | 0x40208634 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL398 | 0x40208638 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL399 | 0x4020863C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL400 | 0x40208640 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL401 | 0x40208644 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL402 | 0x40208648 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL403 | 0x4020864C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL404 | 0x40208650 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL405 | 0x40208654 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL406 | 0x40208658 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL407 | 0x4020865C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL408 | 0x40208660 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL409 | 0x40208664 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL410 | 0x40208668 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL411 | 0x4020866C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL412 | 0x40208670 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL413 | 0x40208674 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL414 | 0x40208678 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL415 | 0x4020867C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL416 | 0x40208680 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL417 | 0x40208684 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL418 | 0x40208688 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL419 | 0x4020868C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL420 | 0x40208690 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL421 | 0x40208694 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL422 | 0x40208698 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL423 | 0x4020869C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL424 | 0x402086A0 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL425 | 0x402086A4 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL426 | 0x402086A8 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL427 | 0x402086AC | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL428 | 0x402086B0 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL429 | 0x402086B4 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL430 | 0x402086B8 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL431 | 0x402086BC | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL432 | 0x402086C0 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL433 | 0x402086C4 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL434 | 0x402086C8 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL435 | 0x402086CC | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL436 | 0x402086D0 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL437 | 0x402086D4 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL438 | 0x402086D8 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL439 | 0x402086DC | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL440 | 0x402086E0 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL441 | 0x402086E4 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL442 | 0x402086E8 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL443 | 0x402086EC | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL444 | 0x402086F0 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL445 | 0x402086F4 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL446 | 0x402086F8 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL447 | 0x402086FC | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL448 | 0x40208700 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL449 | 0x40208704 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL450 | 0x40208708 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL451 | 0x4020870C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL452 | 0x40208710 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL453 | 0x40208714 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL454 | 0x40208718 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL455 | 0x4020871C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL456 | 0x40208720 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL457 | 0x40208724 | FULL | CM0+ system interrupt control |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| CPUSS_CM0_SYSTEM_INT_CTL458 | 0x40208728 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL459 | 0x4020872C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL460 | 0x40208730 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL461 | 0x40208734 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL462 | 0x40208738 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL463 | 0x4020873C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL464 | 0x40208740 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL465 | 0x40208744 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL466 | 0x40208748 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL467 | 0x4020874C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL468 | 0x40208750 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL469 | 0x40208754 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL470 | 0x40208758 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL471 | 0x4020875C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL472 | 0x40208760 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL473 | 0x40208764 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL474 | 0x40208768 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL475 | 0x4020876C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL476 | 0x40208770 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL477 | 0x40208774 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL478 | 0x40208778 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL479 | 0x4020877C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL480 | 0x40208780 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL481 | 0x40208784 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL482 | 0x40208788 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL483 | 0x4020878C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL484 | 0x40208790 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL485 | 0x40208794 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL486 | 0x40208798 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL487 | 0x4020879C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL488 | 0x402087A0 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL489 | 0x402087A4 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL490 | 0x402087A8 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL491 | 0x402087AC | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL492 | 0x402087B0 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL493 | 0x402087B4 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL494 | 0x402087B8 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL495 | 0x402087BC | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL496 | 0x402087C0 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL497 | 0x402087C4 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL498 | 0x402087C8 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL499 | 0x402087CC | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL500 | 0x402087D0 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL501 | 0x402087D4 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL502 | 0x402087D8 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL503 | 0x402087DC | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL504 | 0x402087E0 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL505 | 0x402087E4 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL506 | 0x402087E8 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL507 | 0x402087EC | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL508 | 0x402087F0 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL509 | 0x402087F4 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL510 | 0x402087F8 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL511 | 0x402087FC | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL512 | 0x40208800 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL513 | 0x40208804 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL514 | 0x40208808 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL515 | 0x4020880C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL516 | 0x40208810 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL517 | 0x40208814 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL518 | 0x40208818 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL519 | 0x4020881C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL520 | 0x40208820 | FULL | CM0+ system interrupt control |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| CPUSS_CM0_SYSTEM_INT_CTL521 | 0x40208824 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL522 | 0x40208828 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL523 | 0x4020882C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL524 | 0x40208830 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL525 | 0x40208834 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL526 | 0x40208838 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL527 | 0x4020883C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL528 | 0x40208840 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL529 | 0x40208844 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL530 | 0x40208848 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL531 | 0x4020884C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL532 | 0x40208850 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL533 | 0x40208854 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL534 | 0x40208858 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL535 | 0x4020885C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL536 | 0x40208860 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL537 | 0x40208864 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL538 | 0x40208868 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL539 | 0x4020886C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL540 | 0x40208870 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL541 | 0x40208874 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL542 | 0x40208878 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL543 | 0x4020887C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL544 | 0x40208880 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL545 | 0x40208884 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL546 | 0x40208888 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL547 | 0x4020888C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL548 | 0x40208890 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL549 | 0x40208894 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL550 | 0x40208898 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL551 | 0x4020889C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL552 | 0x402088A0 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL553 | 0x402088A4 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL554 | 0x402088A8 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL555 | 0x402088AC | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL556 | 0x402088B0 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL557 | 0x402088B4 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL558 | 0x402088B8 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL559 | 0x402088BC | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL560 | 0x402088C0 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL561 | 0x402088C4 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL562 | 0x402088C8 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL563 | 0x402088CC | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL564 | 0x402088D0 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL565 | 0x402088D4 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL566 | 0x402088D8 | FULL | CM0+ system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL0 | 0x4020A000 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL1 | 0x4020A004 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL2 | 0x4020A008 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL3 | 0x4020A00C | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL4 | 0x4020A010 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL5 | 0x4020A014 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL6 | 0x4020A018 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL7 | 0x4020A01C | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL8 | 0x4020A020 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL9 | 0x4020A024 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL10 | 0x4020A028 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL11 | 0x4020A02C | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL12 | 0x4020A030 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL13 | 0x4020A034 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL14 | 0x4020A038 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL15 | 0x4020A03C | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL16 | 0x4020A040 | FULL | CM7 0 system interrupt control |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| CPUSS_CM7_0_SYSTEM_INT_CTL17 | 0x4020A044 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL18 | 0x4020A048 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL19 | 0x4020A04C | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL20 | 0x4020A050 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL21 | 0x4020A054 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL22 | 0x4020A058 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL23 | 0x4020A05C | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL24 | 0x4020A060 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL25 | 0x4020A064 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL26 | 0x4020A068 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL27 | 0x4020A06C | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL28 | 0x4020A070 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL29 | 0x4020A074 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL30 | 0x4020A078 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL31 | 0x4020A07C | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL32 | 0x4020A080 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL33 | 0x4020A084 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL34 | 0x4020A088 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL35 | 0x4020A08C | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL36 | 0x4020A090 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL37 | 0x4020A094 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL38 | 0x4020A098 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL39 | 0x4020A09C | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL40 | 0x4020A0A0 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL41 | 0x4020A0A4 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL42 | 0x4020A0A8 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL43 | 0x4020A0AC | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL44 | 0x4020A0B0 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL45 | 0x4020A0B4 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL46 | 0x4020A0B8 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL47 | 0x4020A0BC | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL48 | 0x4020A0C0 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL49 | 0x4020A0C4 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL50 | 0x4020A0C8 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL51 | 0x4020A0CC | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL52 | 0x4020A0D0 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL53 | 0x4020A0D4 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL54 | 0x4020A0D8 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL55 | 0x4020A0DC | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL56 | 0x4020A0E0 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL57 | 0x4020A0E4 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL58 | 0x4020A0E8 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL59 | 0x4020A0EC | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL60 | 0x4020A0F0 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL61 | 0x4020A0F4 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL62 | 0x4020A0F8 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL63 | 0x4020A0FC | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL64 | 0x4020A100 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL65 | 0x4020A104 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL66 | 0x4020A108 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL67 | 0x4020A10C | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL68 | 0x4020A110 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL69 | 0x4020A114 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL70 | 0x4020A118 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL71 | 0x4020A11C | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL72 | 0x4020A120 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL73 | 0x4020A124 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL74 | 0x4020A128 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL75 | 0x4020A12C | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL76 | 0x4020A130 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL77 | 0x4020A134 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL78 | 0x4020A138 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL79 | 0x4020A13C | FULL | CM7 0 system interrupt control |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| CPUSS_CM7_0_SYSTEM_INT_CTL80 | 0x4020A140 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL81 | 0x4020A144 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL82 | 0x4020A148 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL83 | 0x4020A14C | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL84 | 0x4020A150 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL85 | 0x4020A154 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL86 | 0x4020A158 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL87 | 0x4020A15C | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL88 | 0x4020A160 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL89 | 0x4020A164 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL90 | 0x4020A168 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL91 | 0x4020A16C | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL92 | 0x4020A170 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL93 | 0x4020A174 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL94 | 0x4020A178 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL95 | 0x4020A17C | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL96 | 0x4020A180 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL97 | 0x4020A184 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL98 | 0x4020A188 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL99 | 0x4020A18C | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL100 | 0x4020A190 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL101 | 0x4020A194 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL102 | 0x4020A198 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL103 | 0x4020A19C | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL104 | 0x4020A1A0 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL105 | 0x4020A1A4 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL106 | 0x4020A1A8 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL107 | 0x4020A1AC | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL108 | 0x4020A1B0 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL109 | 0x4020A1B4 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL110 | 0x4020A1B8 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL111 | 0x4020A1BC | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL112 | 0x4020A1C0 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL113 | 0x4020A1C4 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL114 | 0x4020A1C8 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL115 | 0x4020A1CC | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL116 | 0x4020A1D0 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL117 | 0x4020A1D4 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL118 | 0x4020A1D8 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL119 | 0x4020A1DC | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL120 | 0x4020A1E0 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL121 | 0x4020A1E4 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL122 | 0x4020A1E8 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL123 | 0x4020A1EC | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL124 | 0x4020A1F0 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL125 | 0x4020A1F4 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL126 | 0x4020A1F8 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL127 | 0x4020A1FC | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL128 | 0x4020A200 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL129 | 0x4020A204 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL130 | 0x4020A208 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL131 | 0x4020A20C | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL132 | 0x4020A210 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL133 | 0x4020A214 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL134 | 0x4020A218 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL135 | 0x4020A21C | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL136 | 0x4020A220 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL137 | 0x4020A224 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL138 | 0x4020A228 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL139 | 0x4020A22C | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL140 | 0x4020A230 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL141 | 0x4020A234 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL142 | 0x4020A238 | FULL | CM7 0 system interrupt control |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| CPUSS_CM7_0_SYSTEM_INT_CTL143 | 0x4020A23C | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL144 | 0x4020A240 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL145 | 0x4020A244 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL146 | 0x4020A248 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL147 | 0x4020A24C | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL148 | 0x4020A250 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL149 | 0x4020A254 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL150 | 0x4020A258 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL151 | 0x4020A25C | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL152 | 0x4020A260 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL153 | 0x4020A264 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL154 | 0x4020A268 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL155 | 0x4020A26C | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL156 | 0x4020A270 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL157 | 0x4020A274 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL158 | 0x4020A278 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL159 | 0x4020A27C | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL160 | 0x4020A280 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL161 | 0x4020A284 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL162 | 0x4020A288 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL163 | 0x4020A28C | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL164 | 0x4020A290 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL165 | 0x4020A294 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL166 | 0x4020A298 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL167 | 0x4020A29C | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL168 | 0x4020A2A0 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL169 | 0x4020A2A4 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL170 | 0x4020A2A8 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL171 | 0x4020A2AC | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL172 | 0x4020A2B0 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL173 | 0x4020A2B4 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL174 | 0x4020A2B8 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL175 | 0x4020A2BC | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL176 | 0x4020A2C0 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL177 | 0x4020A2C4 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL178 | 0x4020A2C8 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL179 | 0x4020A2CC | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL180 | 0x4020A2D0 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL181 | 0x4020A2D4 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL182 | 0x4020A2D8 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL183 | 0x4020A2DC | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL184 | 0x4020A2E0 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL185 | 0x4020A2E4 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL186 | 0x4020A2E8 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL187 | 0x4020A2EC | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL188 | 0x4020A2F0 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL189 | 0x4020A2F4 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL190 | 0x4020A2F8 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL191 | 0x4020A2FC | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL192 | 0x4020A300 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL193 | 0x4020A304 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL194 | 0x4020A308 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL195 | 0x4020A30C | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL196 | 0x4020A310 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL197 | 0x4020A314 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL198 | 0x4020A318 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL199 | 0x4020A31C | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL200 | 0x4020A320 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL201 | 0x4020A324 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL202 | 0x4020A328 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL203 | 0x4020A32C | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL204 | 0x4020A330 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL205 | 0x4020A334 | FULL | CM7 0 system interrupt control |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| CPUSS_CM7_0_SYSTEM_INT_CTL206 | 0x4020A338 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL207 | 0x4020A33C | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL208 | 0x4020A340 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL209 | 0x4020A344 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL210 | 0x4020A348 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL211 | 0x4020A34C | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL212 | 0x4020A350 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL213 | 0x4020A354 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL214 | 0x4020A358 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL215 | 0x4020A35C | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL216 | 0x4020A360 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL217 | 0x4020A364 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL218 | 0x4020A368 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL219 | 0x4020A36C | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL220 | 0x4020A370 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL221 | 0x4020A374 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL222 | 0x4020A378 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL223 | 0x4020A37C | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL224 | 0x4020A380 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL225 | 0x4020A384 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL226 | 0x4020A388 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL227 | 0x4020A38C | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL228 | 0x4020A390 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL229 | 0x4020A394 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL230 | 0x4020A398 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL231 | 0x4020A39C | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL232 | 0x4020A3A0 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL233 | 0x4020A3A4 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL234 | 0x4020A3A8 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL235 | 0x4020A3AC | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL236 | 0x4020A3B0 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL237 | 0x4020A3B4 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL238 | 0x4020A3B8 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL239 | 0x4020A3BC | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL240 | 0x4020A3C0 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL241 | 0x4020A3C4 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL242 | 0x4020A3C8 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL243 | 0x4020A3CC | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL244 | 0x4020A3D0 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL245 | 0x4020A3D4 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL246 | 0x4020A3D8 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL247 | 0x4020A3DC | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL248 | 0x4020A3E0 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL249 | 0x4020A3E4 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL250 | 0x4020A3E8 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL251 | 0x4020A3EC | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL252 | 0x4020A3F0 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL253 | 0x4020A3F4 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL254 | 0x4020A3F8 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL255 | 0x4020A3FC | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL256 | 0x4020A400 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL257 | 0x4020A404 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL258 | 0x4020A408 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL259 | 0x4020A40C | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL260 | 0x4020A410 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL261 | 0x4020A414 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL262 | 0x4020A418 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL263 | 0x4020A41C | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL264 | 0x4020A420 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL265 | 0x4020A424 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL266 | 0x4020A428 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL267 | 0x4020A42C | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL268 | 0x4020A430 | FULL | CM7 0 system interrupt control |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| CPUSS_CM7_0_SYSTEM_INT_CTL269 | 0x4020A434 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL270 | 0x4020A438 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL271 | 0x4020A43C | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL272 | 0x4020A440 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL273 | 0x4020A444 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL274 | 0x4020A448 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL275 | 0x4020A44C | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL276 | 0x4020A450 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL277 | 0x4020A454 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL278 | 0x4020A458 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL279 | 0x4020A45C | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL280 | 0x4020A460 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL281 | 0x4020A464 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL282 | 0x4020A468 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL283 | 0x4020A46C | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL284 | 0x4020A470 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL285 | 0x4020A474 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL286 | 0x4020A478 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL287 | 0x4020A47C | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL288 | 0x4020A480 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL289 | 0x4020A484 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL290 | 0x4020A488 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL291 | 0x4020A48C | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL292 | 0x4020A490 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL293 | 0x4020A494 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL294 | 0x4020A498 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL295 | 0x4020A49C | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL296 | 0x4020A4A0 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL297 | 0x4020A4A4 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL298 | 0x4020A4A8 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL299 | 0x4020A4AC | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL300 | 0x4020A4B0 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL301 | 0x4020A4B4 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL302 | 0x4020A4B8 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL303 | 0x4020A4BC | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL304 | 0x4020A4C0 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL305 | 0x4020A4C4 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL306 | 0x4020A4C8 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL307 | 0x4020A4CC | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL308 | 0x4020A4D0 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL309 | 0x4020A4D4 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL310 | 0x4020A4D8 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL311 | 0x4020A4DC | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL312 | 0x4020A4E0 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL313 | 0x4020A4E4 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL314 | 0x4020A4E8 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL315 | 0x4020A4EC | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL316 | 0x4020A4F0 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL317 | 0x4020A4F4 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL318 | 0x4020A4F8 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL319 | 0x4020A4FC | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL320 | 0x4020A500 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL321 | 0x4020A504 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL322 | 0x4020A508 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL323 | 0x4020A50C | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL324 | 0x4020A510 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL325 | 0x4020A514 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL326 | 0x4020A518 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL327 | 0x4020A51C | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL328 | 0x4020A520 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL329 | 0x4020A524 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL330 | 0x4020A528 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL331 | 0x4020A52C | FULL | CM7 0 system interrupt control |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| CPUSS_CM7_0_SYSTEM_INT_CTL332 | 0x4020A530 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL333 | 0x4020A534 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL334 | 0x4020A538 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL335 | 0x4020A53C | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL336 | 0x4020A540 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL337 | 0x4020A544 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL338 | 0x4020A548 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL339 | 0x4020A54C | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL340 | 0x4020A550 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL341 | 0x4020A554 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL342 | 0x4020A558 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL343 | 0x4020A55C | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL344 | 0x4020A560 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL345 | 0x4020A564 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL346 | 0x4020A568 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL347 | 0x4020A56C | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL348 | 0x4020A570 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL349 | 0x4020A574 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL350 | 0x4020A578 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL351 | 0x4020A57C | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL352 | 0x4020A580 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL353 | 0x4020A584 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL354 | 0x4020A588 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL355 | 0x4020A58C | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL356 | 0x4020A590 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL357 | 0x4020A594 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL358 | 0x4020A598 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL359 | 0x4020A59C | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL360 | 0x4020A5A0 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL361 | 0x4020A5A4 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL362 | 0x4020A5A8 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL363 | 0x4020A5AC | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL364 | 0x4020A5B0 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL365 | 0x4020A5B4 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL366 | 0x4020A5B8 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL367 | 0x4020A5BC | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL368 | 0x4020A5C0 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL369 | 0x4020A5C4 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL370 | 0x4020A5C8 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL371 | 0x4020A5CC | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL372 | 0x4020A5D0 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL373 | 0x4020A5D4 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL374 | 0x4020A5D8 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL375 | 0x4020A5DC | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL376 | 0x4020A5E0 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL377 | 0x4020A5E4 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL378 | 0x4020A5E8 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL379 | 0x4020A5EC | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL380 | 0x4020A5F0 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL381 | 0x4020A5F4 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL382 | 0x4020A5F8 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL383 | 0x4020A5FC | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL384 | 0x4020A600 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL385 | 0x4020A604 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL386 | 0x4020A608 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL387 | 0x4020A60C | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL388 | 0x4020A610 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL389 | 0x4020A614 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL390 | 0x4020A618 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL391 | 0x4020A61C | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL392 | 0x4020A620 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL393 | 0x4020A624 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL394 | 0x4020A628 | FULL | CM7 0 system interrupt control |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| CPUSS_CM7_0_SYSTEM_INT_CTL395 | 0x4020A62C | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL396 | 0x4020A630 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL397 | 0x4020A634 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL398 | 0x4020A638 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL399 | 0x4020A63C | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL400 | 0x4020A640 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL401 | 0x4020A644 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL402 | 0x4020A648 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL403 | 0x4020A64C | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL404 | 0x4020A650 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL405 | 0x4020A654 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL406 | 0x4020A658 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL407 | 0x4020A65C | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL408 | 0x4020A660 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL409 | 0x4020A664 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL410 | 0x4020A668 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL411 | 0x4020A66C | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL412 | 0x4020A670 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL413 | 0x4020A674 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL414 | 0x4020A678 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL415 | 0x4020A67C | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL416 | 0x4020A680 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL417 | 0x4020A684 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL418 | 0x4020A688 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL419 | 0x4020A68C | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL420 | 0x4020A690 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL421 | 0x4020A694 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL422 | 0x4020A698 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL423 | 0x4020A69C | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL424 | 0x4020A6A0 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL425 | 0x4020A6A4 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL426 | 0x4020A6A8 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL427 | 0x4020A6AC | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL428 | 0x4020A6B0 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL429 | 0x4020A6B4 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL430 | 0x4020A6B8 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL431 | 0x4020A6BC | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL432 | 0x4020A6C0 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL433 | 0x4020A6C4 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL434 | 0x4020A6C8 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL435 | 0x4020A6CC | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL436 | 0x4020A6D0 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL437 | 0x4020A6D4 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL438 | 0x4020A6D8 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL439 | 0x4020A6DC | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL440 | 0x4020A6E0 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL441 | 0x4020A6E4 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL442 | 0x4020A6E8 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL443 | 0x4020A6EC | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL444 | 0x4020A6F0 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL445 | 0x4020A6F4 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL446 | 0x4020A6F8 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL447 | 0x4020A6FC | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL448 | 0x4020A700 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL449 | 0x4020A704 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL450 | 0x4020A708 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL451 | 0x4020A70C | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL452 | 0x4020A710 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL453 | 0x4020A714 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL454 | 0x4020A718 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL455 | 0x4020A71C | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL456 | 0x4020A720 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL457 | 0x4020A724 | FULL | CM7 0 system interrupt control |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| CPUSS_CM7_0_SYSTEM_INT_CTL458 | 0x4020A728 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL459 | 0x4020A72C | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL460 | 0x4020A730 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL461 | 0x4020A734 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL462 | 0x4020A738 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL463 | 0x4020A73C | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL464 | 0x4020A740 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL465 | 0x4020A744 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL466 | 0x4020A748 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL467 | 0x4020A74C | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL468 | 0x4020A750 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL469 | 0x4020A754 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL470 | 0x4020A758 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL471 | 0x4020A75C | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL472 | 0x4020A760 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL473 | 0x4020A764 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL474 | 0x4020A768 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL475 | 0x4020A76C | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL476 | 0x4020A770 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL477 | 0x4020A774 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL478 | 0x4020A778 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL479 | 0x4020A77C | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL480 | 0x4020A780 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL481 | 0x4020A784 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL482 | 0x4020A788 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL483 | 0x4020A78C | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL484 | 0x4020A790 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL485 | 0x4020A794 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL486 | 0x4020A798 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL487 | 0x4020A79C | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL488 | 0x4020A7A0 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL489 | 0x4020A7A4 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL490 | 0x4020A7A8 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL491 | 0x4020A7AC | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL492 | 0x4020A7B0 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL493 | 0x4020A7B4 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL494 | 0x4020A7B8 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL495 | 0x4020A7BC | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL496 | 0x4020A7C0 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL497 | 0x4020A7C4 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL498 | 0x4020A7C8 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL499 | 0x4020A7CC | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL500 | 0x4020A7D0 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL501 | 0x4020A7D4 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL502 | 0x4020A7D8 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL503 | 0x4020A7DC | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL504 | 0x4020A7E0 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL505 | 0x4020A7E4 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL506 | 0x4020A7E8 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL507 | 0x4020A7EC | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL508 | 0x4020A7F0 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL509 | 0x4020A7F4 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL510 | 0x4020A7F8 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL511 | 0x4020A7FC | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL512 | 0x4020A800 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL513 | 0x4020A804 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL514 | 0x4020A808 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL515 | 0x4020A80C | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL516 | 0x4020A810 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL517 | 0x4020A814 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL518 | 0x4020A818 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL519 | 0x4020A81C | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL520 | 0x4020A820 | FULL | CM7 0 system interrupt control |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| CPUSS_CM7_0_SYSTEM_INT_CTL521 | 0x4020A824 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL522 | 0x4020A828 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL523 | 0x4020A82C | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL524 | 0x4020A830 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL525 | 0x4020A834 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL526 | 0x4020A838 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL527 | 0x4020A83C | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL528 | 0x4020A840 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL529 | 0x4020A844 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL530 | 0x4020A848 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL531 | 0x4020A84C | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL532 | 0x4020A850 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL533 | 0x4020A854 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL534 | 0x4020A858 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL535 | 0x4020A85C | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL536 | 0x4020A860 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL537 | 0x4020A864 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL538 | 0x4020A868 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL539 | 0x4020A86C | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL540 | 0x4020A870 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL541 | 0x4020A874 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL542 | 0x4020A878 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL543 | 0x4020A87C | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL544 | 0x4020A880 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL545 | 0x4020A884 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL546 | 0x4020A888 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL547 | 0x4020A88C | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL548 | 0x4020A890 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL549 | 0x4020A894 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL550 | 0x4020A898 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL551 | 0x4020A89C | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL552 | 0x4020A8A0 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL553 | 0x4020A8A4 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL554 | 0x4020A8A8 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL555 | 0x4020A8AC | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL556 | 0x4020A8B0 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL557 | 0x4020A8B4 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL558 | 0x4020A8B8 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL559 | 0x4020A8BC | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL560 | 0x4020A8C0 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL561 | 0x4020A8C4 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL562 | 0x4020A8C8 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL563 | 0x4020A8CC | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL564 | 0x4020A8D0 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL565 | 0x4020A8D4 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_0_SYSTEM_INT_CTL566 | 0x4020A8D8 | FULL | CM7 0 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL0 | 0x4020C000 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL1 | 0x4020C004 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL2 | 0x4020C008 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL3 | 0x4020C00C | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL4 | 0x4020C010 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL5 | 0x4020C014 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL6 | 0x4020C018 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL7 | 0x4020C01C | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL8 | 0x4020C020 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL9 | 0x4020C024 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL10 | 0x4020C028 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL11 | 0x4020C02C | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL12 | 0x4020C030 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL13 | 0x4020C034 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL14 | 0x4020C038 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL15 | 0x4020C03C | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL16 | 0x4020C040 | FULL | CM7 1 system interrupt control |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| CPUSS_CM7_1_SYSTEM_INT_CTL17 | 0x4020C044 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL18 | 0x4020C048 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL19 | 0x4020C04C | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL20 | 0x4020C050 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL21 | 0x4020C054 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL22 | 0x4020C058 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL23 | 0x4020C05C | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL24 | 0x4020C060 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL25 | 0x4020C064 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL26 | 0x4020C068 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL27 | 0x4020C06C | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL28 | 0x4020C070 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL29 | 0x4020C074 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL30 | 0x4020C078 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL31 | 0x4020C07C | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL32 | 0x4020C080 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL33 | 0x4020C084 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL34 | 0x4020C088 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL35 | 0x4020C08C | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL36 | 0x4020C090 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL37 | 0x4020C094 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL38 | 0x4020C098 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL39 | 0x4020C09C | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL40 | 0x4020C0A0 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL41 | 0x4020C0A4 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL42 | 0x4020C0A8 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL43 | 0x4020C0AC | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL44 | 0x4020C0B0 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL45 | 0x4020C0B4 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL46 | 0x4020C0B8 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL47 | 0x4020C0BC | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL48 | 0x4020C0C0 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL49 | 0x4020C0C4 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL50 | 0x4020C0C8 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL51 | 0x4020C0CC | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL52 | 0x4020C0D0 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL53 | 0x4020C0D4 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL54 | 0x4020C0D8 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL55 | 0x4020C0DC | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL56 | 0x4020C0E0 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL57 | 0x4020C0E4 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL58 | 0x4020C0E8 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL59 | 0x4020C0EC | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL60 | 0x4020C0F0 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL61 | 0x4020C0F4 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL62 | 0x4020C0F8 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL63 | 0x4020C0FC | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL64 | 0x4020C100 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL65 | 0x4020C104 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL66 | 0x4020C108 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL67 | 0x4020C10C | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL68 | 0x4020C110 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL69 | 0x4020C114 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL70 | 0x4020C118 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL71 | 0x4020C11C | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL72 | 0x4020C120 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL73 | 0x4020C124 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL74 | 0x4020C128 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL75 | 0x4020C12C | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL76 | 0x4020C130 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL77 | 0x4020C134 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL78 | 0x4020C138 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL79 | 0x4020C13C | FULL | CM7 1 system interrupt control |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| CPUSS_CM7_1_SYSTEM_INT_CTL80 | 0x4020C140 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL81 | 0x4020C144 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL82 | 0x4020C148 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL83 | 0x4020C14C | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL84 | 0x4020C150 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL85 | 0x4020C154 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL86 | 0x4020C158 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL87 | 0x4020C15C | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL88 | 0x4020C160 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL89 | 0x4020C164 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL90 | 0x4020C168 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL91 | 0x4020C16C | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL92 | 0x4020C170 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL93 | 0x4020C174 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL94 | 0x4020C178 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL95 | 0x4020C17C | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL96 | 0x4020C180 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL97 | 0x4020C184 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL98 | 0x4020C188 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL99 | 0x4020C18C | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL100 | 0x4020C190 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL101 | 0x4020C194 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL102 | 0x4020C198 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL103 | 0x4020C19C | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL104 | 0x4020C1A0 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL105 | 0x4020C1A4 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL106 | 0x4020C1A8 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL107 | 0x4020C1AC | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL108 | 0x4020C1B0 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL109 | 0x4020C1B4 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL110 | 0x4020C1B8 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL111 | 0x4020C1BC | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL112 | 0x4020C1C0 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL113 | 0x4020C1C4 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL114 | 0x4020C1C8 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL115 | 0x4020C1CC | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL116 | 0x4020C1D0 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL117 | 0x4020C1D4 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL118 | 0x4020C1D8 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL119 | 0x4020C1DC | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL120 | 0x4020C1E0 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL121 | 0x4020C1E4 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL122 | 0x4020C1E8 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL123 | 0x4020C1EC | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL124 | 0x4020C1F0 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL125 | 0x4020C1F4 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL126 | 0x4020C1F8 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL127 | 0x4020C1FC | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL128 | 0x4020C200 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL129 | 0x4020C204 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL130 | 0x4020C208 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL131 | 0x4020C20C | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL132 | 0x4020C210 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL133 | 0x4020C214 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL134 | 0x4020C218 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL135 | 0x4020C21C | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL136 | 0x4020C220 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL137 | 0x4020C224 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL138 | 0x4020C228 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL139 | 0x4020C22C | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL140 | 0x4020C230 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL141 | 0x4020C234 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL142 | 0x4020C238 | FULL | CM7 1 system interrupt control |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| CPUSS_CM7_1_SYSTEM_INT_CTL143 | 0x4020C23C | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL144 | 0x4020C240 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL145 | 0x4020C244 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL146 | 0x4020C248 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL147 | 0x4020C24C | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL148 | 0x4020C250 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL149 | 0x4020C254 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL150 | 0x4020C258 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL151 | 0x4020C25C | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL152 | 0x4020C260 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL153 | 0x4020C264 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL154 | 0x4020C268 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL155 | 0x4020C26C | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL156 | 0x4020C270 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL157 | 0x4020C274 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL158 | 0x4020C278 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL159 | 0x4020C27C | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL160 | 0x4020C280 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL161 | 0x4020C284 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL162 | 0x4020C288 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL163 | 0x4020C28C | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL164 | 0x4020C290 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL165 | 0x4020C294 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL166 | 0x4020C298 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL167 | 0x4020C29C | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL168 | 0x4020C2A0 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL169 | 0x4020C2A4 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL170 | 0x4020C2A8 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL171 | 0x4020C2AC | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL172 | 0x4020C2B0 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL173 | 0x4020C2B4 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL174 | 0x4020C2B8 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL175 | 0x4020C2BC | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL176 | 0x4020C2C0 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL177 | 0x4020C2C4 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL178 | 0x4020C2C8 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL179 | 0x4020C2CC | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL180 | 0x4020C2D0 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL181 | 0x4020C2D4 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL182 | 0x4020C2D8 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL183 | 0x4020C2DC | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL184 | 0x4020C2E0 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL185 | 0x4020C2E4 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL186 | 0x4020C2E8 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL187 | 0x4020C2EC | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL188 | 0x4020C2F0 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL189 | 0x4020C2F4 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL190 | 0x4020C2F8 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL191 | 0x4020C2FC | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL192 | 0x4020C300 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL193 | 0x4020C304 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL194 | 0x4020C308 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL195 | 0x4020C30C | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL196 | 0x4020C310 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL197 | 0x4020C314 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL198 | 0x4020C318 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL199 | 0x4020C31C | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL200 | 0x4020C320 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL201 | 0x4020C324 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL202 | 0x4020C328 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL203 | 0x4020C32C | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL204 | 0x4020C330 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL205 | 0x4020C334 | FULL | CM7 1 system interrupt control |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| CPUSS_CM7_1_SYSTEM_INT_CTL206 | 0x4020C338 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL207 | 0x4020C33C | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL208 | 0x4020C340 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL209 | 0x4020C344 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL210 | 0x4020C348 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL211 | 0x4020C34C | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL212 | 0x4020C350 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL213 | 0x4020C354 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL214 | 0x4020C358 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL215 | 0x4020C35C | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL216 | 0x4020C360 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL217 | 0x4020C364 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL218 | 0x4020C368 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL219 | 0x4020C36C | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL220 | 0x4020C370 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL221 | 0x4020C374 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL222 | 0x4020C378 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL223 | 0x4020C37C | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL224 | 0x4020C380 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL225 | 0x4020C384 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL226 | 0x4020C388 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL227 | 0x4020C38C | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL228 | 0x4020C390 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL229 | 0x4020C394 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL230 | 0x4020C398 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL231 | 0x4020C39C | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL232 | 0x4020C3A0 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL233 | 0x4020C3A4 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL234 | 0x4020C3A8 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL235 | 0x4020C3AC | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL236 | 0x4020C3B0 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL237 | 0x4020C3B4 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL238 | 0x4020C3B8 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL239 | 0x4020C3BC | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL240 | 0x4020C3C0 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL241 | 0x4020C3C4 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL242 | 0x4020C3C8 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL243 | 0x4020C3CC | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL244 | 0x4020C3D0 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL245 | 0x4020C3D4 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL246 | 0x4020C3D8 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL247 | 0x4020C3DC | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL248 | 0x4020C3E0 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL249 | 0x4020C3E4 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL250 | 0x4020C3E8 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL251 | 0x4020C3EC | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL252 | 0x4020C3F0 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL253 | 0x4020C3F4 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL254 | 0x4020C3F8 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL255 | 0x4020C3FC | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL256 | 0x4020C400 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL257 | 0x4020C404 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL258 | 0x4020C408 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL259 | 0x4020C40C | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL260 | 0x4020C410 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL261 | 0x4020C414 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL262 | 0x4020C418 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL263 | 0x4020C41C | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL264 | 0x4020C420 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL265 | 0x4020C424 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL266 | 0x4020C428 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL267 | 0x4020C42C | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL268 | 0x4020C430 | FULL | CM7 1 system interrupt control |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| CPUSS_CM7_1_SYSTEM_INT_CTL269 | 0x4020C434 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL270 | 0x4020C438 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL271 | 0x4020C43C | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL272 | 0x4020C440 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL273 | 0x4020C444 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL274 | 0x4020C448 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL275 | 0x4020C44C | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL276 | 0x4020C450 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL277 | 0x4020C454 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL278 | 0x4020C458 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL279 | 0x4020C45C | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL280 | 0x4020C460 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL281 | 0x4020C464 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL282 | 0x4020C468 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL283 | 0x4020C46C | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL284 | 0x4020C470 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL285 | 0x4020C474 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL286 | 0x4020C478 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL287 | 0x4020C47C | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL288 | 0x4020C480 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL289 | 0x4020C484 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL290 | 0x4020C488 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL291 | 0x4020C48C | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL292 | 0x4020C490 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL293 | 0x4020C494 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL294 | 0x4020C498 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL295 | 0x4020C49C | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL296 | 0x4020C4A0 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL297 | 0x4020C4A4 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL298 | 0x4020C4A8 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL299 | 0x4020C4AC | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL300 | 0x4020C4B0 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL301 | 0x4020C4B4 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL302 | 0x4020C4B8 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL303 | 0x4020C4BC | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL304 | 0x4020C4C0 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL305 | 0x4020C4C4 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL306 | 0x4020C4C8 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL307 | 0x4020C4CC | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL308 | 0x4020C4D0 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL309 | 0x4020C4D4 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL310 | 0x4020C4D8 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL311 | 0x4020C4DC | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL312 | 0x4020C4E0 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL313 | 0x4020C4E4 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL314 | 0x4020C4E8 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL315 | 0x4020C4EC | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL316 | 0x4020C4F0 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL317 | 0x4020C4F4 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL318 | 0x4020C4F8 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL319 | 0x4020C4FC | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL320 | 0x4020C500 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL321 | 0x4020C504 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL322 | 0x4020C508 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL323 | 0x4020C50C | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL324 | 0x4020C510 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL325 | 0x4020C514 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL326 | 0x4020C518 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL327 | 0x4020C51C | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL328 | 0x4020C520 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL329 | 0x4020C524 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL330 | 0x4020C528 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL331 | 0x4020C52C | FULL | CM7 1 system interrupt control |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| CPUSS_CM7_1_SYSTEM_INT_CTL332 | 0x4020C530 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL333 | 0x4020C534 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL334 | 0x4020C538 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL335 | 0x4020C53C | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL336 | 0x4020C540 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL337 | 0x4020C544 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL338 | 0x4020C548 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL339 | 0x4020C54C | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL340 | 0x4020C550 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL341 | 0x4020C554 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL342 | 0x4020C558 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL343 | 0x4020C55C | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL344 | 0x4020C560 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL345 | 0x4020C564 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL346 | 0x4020C568 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL347 | 0x4020C56C | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL348 | 0x4020C570 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL349 | 0x4020C574 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL350 | 0x4020C578 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL351 | 0x4020C57C | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL352 | 0x4020C580 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL353 | 0x4020C584 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL354 | 0x4020C588 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL355 | 0x4020C58C | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL356 | 0x4020C590 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL357 | 0x4020C594 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL358 | 0x4020C598 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL359 | 0x4020C59C | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL360 | 0x4020C5A0 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL361 | 0x4020C5A4 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL362 | 0x4020C5A8 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL363 | 0x4020C5AC | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL364 | 0x4020C5B0 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL365 | 0x4020C5B4 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL366 | 0x4020C5B8 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL367 | 0x4020C5BC | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL368 | 0x4020C5C0 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL369 | 0x4020C5C4 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL370 | 0x4020C5C8 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL371 | 0x4020C5CC | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL372 | 0x4020C5D0 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL373 | 0x4020C5D4 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL374 | 0x4020C5D8 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL375 | 0x4020C5DC | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL376 | 0x4020C5E0 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL377 | 0x4020C5E4 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL378 | 0x4020C5E8 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL379 | 0x4020C5EC | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL380 | 0x4020C5F0 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL381 | 0x4020C5F4 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL382 | 0x4020C5F8 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL383 | 0x4020C5FC | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL384 | 0x4020C600 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL385 | 0x4020C604 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL386 | 0x4020C608 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL387 | 0x4020C60C | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL388 | 0x4020C610 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL389 | 0x4020C614 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL390 | 0x4020C618 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL391 | 0x4020C61C | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL392 | 0x4020C620 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL393 | 0x4020C624 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL394 | 0x4020C628 | FULL | CM7 1 system interrupt control |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| CPUSS_CM7_1_SYSTEM_INT_CTL395 | 0x4020C62C | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL396 | 0x4020C630 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL397 | 0x4020C634 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL398 | 0x4020C638 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL399 | 0x4020C63C | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL400 | 0x4020C640 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL401 | 0x4020C644 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL402 | 0x4020C648 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL403 | 0x4020C64C | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL404 | 0x4020C650 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL405 | 0x4020C654 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL406 | 0x4020C658 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL407 | 0x4020C65C | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL408 | 0x4020C660 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL409 | 0x4020C664 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL410 | 0x4020C668 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL411 | 0x4020C66C | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL412 | 0x4020C670 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL413 | 0x4020C674 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL414 | 0x4020C678 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL415 | 0x4020C67C | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL416 | 0x4020C680 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL417 | 0x4020C684 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL418 | 0x4020C688 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL419 | 0x4020C68C | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL420 | 0x4020C690 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL421 | 0x4020C694 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL422 | 0x4020C698 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL423 | 0x4020C69C | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL424 | 0x4020C6A0 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL425 | 0x4020C6A4 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL426 | 0x4020C6A8 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL427 | 0x4020C6AC | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL428 | 0x4020C6B0 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL429 | 0x4020C6B4 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL430 | 0x4020C6B8 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL431 | 0x4020C6BC | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL432 | 0x4020C6C0 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL433 | 0x4020C6C4 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL434 | 0x4020C6C8 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL435 | 0x4020C6CC | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL436 | 0x4020C6D0 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL437 | 0x4020C6D4 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL438 | 0x4020C6D8 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL439 | 0x4020C6DC | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL440 | 0x4020C6E0 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL441 | 0x4020C6E4 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL442 | 0x4020C6E8 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL443 | 0x4020C6EC | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL444 | 0x4020C6F0 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL445 | 0x4020C6F4 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL446 | 0x4020C6F8 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL447 | 0x4020C6FC | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL448 | 0x4020C700 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL449 | 0x4020C704 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL450 | 0x4020C708 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL451 | 0x4020C70C | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL452 | 0x4020C710 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL453 | 0x4020C714 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL454 | 0x4020C718 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL455 | 0x4020C71C | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL456 | 0x4020C720 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL457 | 0x4020C724 | FULL | CM7 1 system interrupt control |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| CPUSS_CM7_1_SYSTEM_INT_CTL458 | 0x4020C728 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL459 | 0x4020C72C | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL460 | 0x4020C730 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL461 | 0x4020C734 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL462 | 0x4020C738 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL463 | 0x4020C73C | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL464 | 0x4020C740 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL465 | 0x4020C744 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL466 | 0x4020C748 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL467 | 0x4020C74C | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL468 | 0x4020C750 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL469 | 0x4020C754 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL470 | 0x4020C758 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL471 | 0x4020C75C | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL472 | 0x4020C760 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL473 | 0x4020C764 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL474 | 0x4020C768 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL475 | 0x4020C76C | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL476 | 0x4020C770 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL477 | 0x4020C774 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL478 | 0x4020C778 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL479 | 0x4020C77C | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL480 | 0x4020C780 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL481 | 0x4020C784 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL482 | 0x4020C788 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL483 | 0x4020C78C | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL484 | 0x4020C790 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL485 | 0x4020C794 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL486 | 0x4020C798 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL487 | 0x4020C79C | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL488 | 0x4020C7A0 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL489 | 0x4020C7A4 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL490 | 0x4020C7A8 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL491 | 0x4020C7AC | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL492 | 0x4020C7B0 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL493 | 0x4020C7B4 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL494 | 0x4020C7B8 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL495 | 0x4020C7BC | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL496 | 0x4020C7C0 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL497 | 0x4020C7C4 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL498 | 0x4020C7C8 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL499 | 0x4020C7CC | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL500 | 0x4020C7D0 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL501 | 0x4020C7D4 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL502 | 0x4020C7D8 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL503 | 0x4020C7DC | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL504 | 0x4020C7E0 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL505 | 0x4020C7E4 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL506 | 0x4020C7E8 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL507 | 0x4020C7EC | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL508 | 0x4020C7F0 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL509 | 0x4020C7F4 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL510 | 0x4020C7F8 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL511 | 0x4020C7FC | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL512 | 0x4020C800 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL513 | 0x4020C804 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL514 | 0x4020C808 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL515 | 0x4020C80C | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL516 | 0x4020C810 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL517 | 0x4020C814 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL518 | 0x4020C818 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL519 | 0x4020C81C | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL520 | 0x4020C820 | FULL | CM7 1 system interrupt control |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| CPUSS_CM7_1_SYSTEM_INT_CTL521 | 0x4020C824 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL522 | 0x4020C828 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL523 | 0x4020C82C | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL524 | 0x4020C830 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL525 | 0x4020C834 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL526 | 0x4020C838 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL527 | 0x4020C83C | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL528 | 0x4020C840 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL529 | 0x4020C844 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL530 | 0x4020C848 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL531 | 0x4020C84C | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL532 | 0x4020C850 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL533 | 0x4020C854 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL534 | 0x4020C858 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL535 | 0x4020C85C | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL536 | 0x4020C860 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL537 | 0x4020C864 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL538 | 0x4020C868 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL539 | 0x4020C86C | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL540 | 0x4020C870 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL541 | 0x4020C874 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL542 | 0x4020C878 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL543 | 0x4020C87C | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL544 | 0x4020C880 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL545 | 0x4020C884 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL546 | 0x4020C888 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL547 | 0x4020C88C | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL548 | 0x4020C890 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL549 | 0x4020C894 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL550 | 0x4020C898 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL551 | 0x4020C89C | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL552 | 0x4020C8A0 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL553 | 0x4020C8A4 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL554 | 0x4020C8A8 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL555 | 0x4020C8AC | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL556 | 0x4020C8B0 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL557 | 0x4020C8B4 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL558 | 0x4020C8B8 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL559 | 0x4020C8BC | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL560 | 0x4020C8C0 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL561 | 0x4020C8C4 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL562 | 0x4020C8C8 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL563 | 0x4020C8CC | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL564 | 0x4020C8D0 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL565 | 0x4020C8D4 | FULL | CM7 1 system interrupt control |
| CPUSS_CM7_1_SYSTEM_INT_CTL566 | 0x4020C8D8 | FULL | CM7 1 system interrupt control |

## 5.1 Register Details

### 5.1.1 CPUSS_IDENTITY

**Description:** Identity
**Address:** 0x40200000
**Offset:** 0x0
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** This register is typically used by SW that is executed on different bus masters or with different protection contexts.
**Default:** Undefined as one or more bit fields have a default value that is undefined

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | PC [7:4] | | | | None [3:2] | | NS [1:1] | P [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:12] | | | | MS [11:8] | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | P | R | W | Undefined | This field specifies the privileged setting ('0': user mode; '1': privileged mode) of the transfer that reads the register. |
| 1 | NS | R | W | Undefined | This field specifies the security setting ('0': secure mode; '1': non-secure mode) of the transfer that reads the register. |
| 4:7 | PC | R | W | Undefined | This field specifies the protection context of the transfer that reads the register. |
| 8:11 | MS | R | W | Undefined | This field specifies the bus master identifier of the transfer that reads the register. |

### 5.1.2 CPUSS_CM7_0_STATUS

**Description:** CM7 0 status
**Address:** 0x40200004
**Offset:** 0x4
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x13

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:5] | | | PWR_DONE [4:4] | None [3:2] | | SLEEPDEEP [1:1] | SLEEPING [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:13] | | | TCMC_AHB_MS [12:12] | TCMC_EXT_MS_3 [11:11] | TCMC_EXT_MS_2_TO_0 [10:10] | TCMC_CM7_1_MS [9:9] | None [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | SLEEPING | R | W | 1 | Specifies if the CPU is in Active, Sleep or DeepSleep power mode:<br>- Active power mode: SLEEPING is '0'.<br>- Sleep power mode: SLEEPING is '1' and SLEEPDEEP is '0'.<br>- DeepSleep power mode: SLEEPING is '1' and SLEEPDEEP is '1'. |
| 1 | SLEEPDEEP | R | W | 1 | Specifies if the CPU is in Sleep or DeepSleep power mode. See SLEEPING field. |
| 4 | PWR_DONE | R | W | 1 | After a PWR_MODE change this flag indicates if the new power mode has taken effect or not.<br>Note: this flag can also change as a result of a change in debug power up req |
| 9 | TCMC_CM7_1_MS | R | W | 0 | Outstanding transactions from CM7 1.<br>'0': There are no outstanding transactions to the CM7 I/D-TCM slave port (AHBS) from CM7 1.<br>'1': There are outstanding transactions to the CM7 I/D-TCM slave port (AHBS) from CM7 1. Do not switch the CM7 power off. |
| 10 | TCMC_EXT_MS_2_TO_0 | R | W | 0 | Outstanding transactions from external AXI masters 2 to 0.<br>'0': There are no outstanding transactions to the CM7 I/D-TCM slave port (AHBS) from external AXI masters 2 to 0.<br>'1': There are outstanding transactions to the CM7 I/D-TCM slave port (AHBS) from external AXI masters 2 to 0. Do not switch the CM7 power off. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 11 | TCMC_EXT_MS_3 | R | W | 0 | Outstanding transactions from external AXI master 3.<br>'0': There are no outstanding transactions to the CM7 I/D-TCM slave port (AHBS) from external AXI master 3.<br>'1': There are outstanding transactions to the CM7 I/D-TCM slave port (AHBS) from external AXI master 3. Do not switch the CM7 power off. |
| 12 | TCMC_AHB_MS | R | W | 0 | Ongoing AHB transaction.<br>'0': There is no ongoing transaction to the CM7 I/D-TCM slave port (AHBS) from an AHB master.<br>'1': There is an ongoing transaction to the CM7 I/D-TCM slave port (AHBS) from an AHB master. Do not switch the CM7 power off. |

### 5.1.3 CPUSS_FAST_0_CLOCK_CTL

**Description:** Fast 0 clock control
**Address:** 0x40200008
**Offset:** 0x8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Clock division control to divide and generate clk_fast_0 from clk_hf<x>.
Note that this register is retained. However, the counter that is used to implement the division is not and will be initialized by HW to '0' when transitioning from DeepSleep to Active power mode.
Note that CM7 clocks must be running before accessing this register.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | FRAC_DIV [7:3] | | | | | None [2:0] | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | INT_DIV [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 3:7 | FRAC_DIV | RW | R | 0 | Fractional division by (FRAC_DIV/32). Allows for fractional divisions in the range [0, 31/32]. Note that fractional division results in clock jitter as some clock periods may be 1 'clk_hf<x>' cycle longer than other clock periods. |
| 8:15 | INT_DIV | RW | R | 0 | Integer division by (1+INT_DIV). Allows for integer divisions in the range [1, 256] (INT_DIV is in the range [0, 255]). |

### 5.1.4 CPUSS_CM7_0_CTL

**Description:** CM7 0 control
**Address:** 0x4020000C
**Offset:** 0xC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Note that CM7 clocks must be running before accessing this register.
**Default:** 0x1F

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:5] | | | CPU_WAIT [4:4] | PPB_LOCK [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:12] | | | | INIT_RMW_EN [11:10] | | INIT_TCM_EN [9:8] | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | TCMC_EN [23:23] | DTCM _READ _WS [22:22] | DTCM _ECC_INJ _EN [21:21] | DTCM _ECC_EN [20:20] | ITCM_ECC _CHECK _DIS [19:19] | ITCM _READ _WS [18:18] | ITCM_ECC _INJ_EN [17:17] | ITCM_ECC _EN [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | IDC_MASK [31:31] | None [30:29] | | IXC_MASK [28:28] | UFC_MASK [27:27] | OFC _MASK [26:26] | DZC_MASK [25:25] | IOC_MASK [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | PPB_LOCK | RW | R | 15 | Write disable for specific CPU registers:<br>Bit 0: ITCMR register. '0': enabled; '1': disabled.<br>Bit 1: DTCMR register. '0': enabled; '1': disabled.<br>Bit 2: AHBPCR register. '0': enabled; '1': disabled.<br>Bit 3: VTOR register. '0': enabled; '1': disabled. |
| 4 | CPU_WAIT | RW | R | 1 | When this signal is '1' out of reset, it forces the CPU into a quiescent state that delays its boot-up sequence and instruction execution until this signal is driven '0'. This allows the TCMs to be loaded by the system before the CPU performs any TCM accesses. The CPU AHBS interface functions while CPU_WAIT is '1' and services transactions initiated by the system (e.g. DMA controller) to load the TCMs. |
| 8:9 | INIT_TCM_EN | RW | R | 0 | TCM enable initialization after reset:<br>Bit 0: ITCM. '0': disabled; '1': enabled.<br>Bit 1: DTCM. '0': disabled; '1': enabled. |
| 10:11 | INIT_RMW_EN | RW | R | 0 | TCM read-modify-write enable initialization after reset:<br>Bit 0: ITCM. '0': disabled; '1': enabled.<br>Bit 1: DTCM. '0': disabled; '1': enabled.<br><br>Note: When TCM ECC is enabled, the read-modify-write functionality should be enabled. This prevents partial (sub-word) writes to the TCM. |
| 16 | ITCM_ECC_EN | RW | R | 0 | ITCM ECC enable:<br>'0': Disabled.<br>'1': Enabled. |
| 17 | ITCM_ECC_INJ_EN | RW | R | 0 | ITCM ECC error injection enable:<br>'0': Disabled.<br>'1': Enabled. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 18 | ITCM_READ_WS | RW | R | 0 | ITCM read wait states (writes have no wait states).<br>'0': 0 wait states.<br>'1': 1 wait state. |
| 19 | ITCM_ECC_CHECK_DIS | RW | R | 0 | Disable ECC checking and thus fault reports. This also disables ECC correction (required to enable initialization). Intended usage is initialization. This bit is ignored when TCM_ECC_EN=0. |
| 20 | DTCM_ECC_EN | RW | R | 0 | DTCM ECC enable:<br>'0': Disabled.<br>'1': Enabled. |
| 21 | DTCM_ECC_INJ_EN | RW | R | 0 | DTCM ECC error injection enable:<br>'0': Disabled.<br>'1': Enabled. |
| 22 | DTCM_READ_WS | RW | R | 0 | DTCM read wait states (writes have no wait states).<br>'0': 0 wait states.<br>'1': 1 wait state. |
| 23 | TCMC_EN | RW | R | 0 | CM7 TCMC access control:<br>'0': Disable access to the CM7 I/D-TCM slave port (AHBS). Access attempts will get a bus error response.<br>'1': Enable access to the CM7 I/D-TCM slave port (AHBS).<br><br>Before switching the CM7 power off, set this field to 0, and confirm that there are no outstanding AXI transactions and no ongoing AHB transactions to the CM7 TCMs, by checking that bits TCMC_* in CM7_x_STATUS are '0'. |
| 24 | IOC_MASK | RW | R | 0 | CPU floating point unit (FPU) exception mask for the CPU's FPCSR.IOC 'invalid operation' exception condition:<br>'0': The CPU's exception condition does NOT activate the CPU's floating point interrupt.<br>'1': the CPU's exception condition activates the CPU's floating point interrupt.<br><br>Note: the ARM architecture does NOT support FPU exceptions; i.e. there is no precise FPU exception handler. Instead, FPU conditions are captured in the CPU's FPCSR register and the conditions are provided as CPU interface signals. The interface signals are 'masked' with the fields a provide by this register (CM7_0_CTL). The 'masked' signals are reduced/OR-ed into a single CPU floating point interrupt signal. The associated CPU interrupt handler allows for imprecise handling of FPU exception conditions.<br><br>Note: the CPU's FPCSR exception conditions are 'sticky'. Typically, the CPU FPU interrupt handler will clear the exception condition(s) to '0'.<br><br>Note: by default, the FPU exception masks are '0'. Therefore, FPU exception conditions will NOT activate the CPU's floating point interrupt. |
| 25 | DZC_MASK | RW | R | 0 | CPU FPU exception mask for the CPU's FPCSR.DZC 'divide by zero' exception condition:<br>'0': The CPU's exception condition does NOT activate the CPU's floating point interrupt.<br>'1': the CPU's exception condition activates the CPU's floating point interrupt. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 26 | OFC_MASK | RW | R | 0 | CPU FPU exception mask for the CPU's FPCSR.OFC 'overflow' exception condition:<br>'0': The CPU's exception condition does NOT activate the CPU's floating point interrupt.<br>'1': the CPU's exception condition activates the CPU's floating point interrupt. |
| 27 | UFC_MASK | RW | R | 0 | CPU FPU exception mask for the CPU's FPCSR.UFC 'underflow' exception condition:<br>'0': The CPU's exception condition does NOT activate the CPU's floating point interrupt.<br>'1': the CPU's exception condition activates the CPU's floating point interrupt. |
| 28 | IXC_MASK | RW | R | 0 | CPU FPU exception mask for the CPU's FPCSR.IXC 'inexact' exception condition:<br>'0': The CPU's exception condition does NOT activate the CPU's floating point interrupt.<br>'1': the CPU's exception condition activates the CPU's floating point interrupt.<br><br>Note: the 'inexact' condition is set as a result of rounding. Rounding may occur frequently and is typically not an error condition. To prevent frequent CPU FPU interrupts as a result of rounding, this field is typically set to '0'. |
| 31 | IDC_MASK | RW | R | 0 | CPU FPU exception mask for the CPU's FPCSR.IDC 'input denormalized' exception condition:<br>'0': The CPU's exception condition does NOT activate the CPU's floating point interrupt.<br>'1': the CPU's exception condition activates the CPU's floating point interrupt.<br><br>Note: if the CPU FPCSR.FZ field is set to '1', denormalized inputs are 'flushed to zero'. Dependent on the FPU algorithm, this may or may not occur frequently. To prevent frequent CPU FPU interrupts as a result of denormalized inputs, this field may be set to '0'. |

### 5.1.5 CPUSS_CM7_0_INT_STATUS

**Description:** CM7 0 interrupt status
**Address:** 0x40200100
**Offset:** 0x100
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | SYSTEM_INT_IDX [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:10] | | | | | | SYSTEM_INT_IDX [9:8] | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | SYSTEM_INT_VALID [31:31] | None [30:24] | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:9 | SYSTEM_INT_IDX | R | W | Undefined | Lowest CM7_0 activated system interrupt index for CPU interrupt.<br><br>See description of CM0_INT0_STATUS. |
| 31 | SYSTEM_INT_VALID | R | W | 0 | See description of CM0_INT0_STATUS. |

### 5.1.6 CPUSS_CM7_0_VECTOR_TABLE_BASE

**Description:** CM7 0 vector table base
**Address:** 0x40200200
**Offset:** 0x200
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Note that CM7 clocks must be running before accessing this register.
**Default:** 0x1000000

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDR25 [7:7] | None [6:0] | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDR25 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDR25 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDR25 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 7:31 | ADDR25 | RW | R | 131072 | The default CM7 vector table base address is 0x0100:0000 (CM7 VTOR and reset exception handler address after reset). This is the location of the system ROM memory.<br><br>The system ROM is mirrored at 0x0000:0000. This is required for the CM0+ boot process (the CM0+ VTOR and reset exception handler address is at fixed address 0x0000:00000 after reset). The system ROM requires mirroring as the CM7 CPUs' ITCMs are located at base address 0x0000:0000 and effectively cut a hole in the system ROM mirror address space (but the 0x0100:0000 address space is not affected). |

### 5.1.7 CPUSS_CM7_0_NMI_CTL

**Description:** CM7 0 NMI control
**Address:** 0x40200240
**Offset:** 0x240
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Note that multiple (four) CM7_0_NMI_CTL registers exist, allowing for multiple (four) system interrupts to be connnected to the CPU NMI. The four selected system interrupts are logically OR'd into a single CPU NMI input. The NMI handler may need to investigate all selected system interrupt sources to identify the source of CPU NMI.
**Default:** 0x3FF

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | SYSTEM_INT_IDX [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:10] | | | | | | SYSTEM_INT_IDX [9:8] | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:9 | SYSTEM_INT_IDX | RW | R | 1023 | System interrupt select for CPU NMI. The reset value ('1023') ensures that the CPU NMI is NOT connected to any system interrupt after DeepSleep reset. |

### 5.1.8 CPUSS_TRC_DBG_CLOCK_CTL

**Description:** Trace and debug clock control
**Address:** 0x40200320
**Offset:** 0x320
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Clock division control to divide and generate clk_trc_dbg from clk_hf0_dbg (clk_hf0_dbg is same as clk_hf0, but runs only when debugger is connected i.e when CDBGPWRUPREQ=1).
**Default:** 0x200

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | INT_DIV [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 8:15 | INT_DIV | RW | R | 2 | Integer division by (1+INT_DIV). Allows for integer divisions in the range [1, 256] (INT_DIV is in the range [0, 255]).<br>Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to '0' when transitioning from DeepSleep to Active power mode. |

### 5.1.9 CPUSS_CM7_1_STATUS

**Description:** CM7 1status
**Address:** 0x40200404
**Offset:** 0x404
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x13

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:5] | | | PWR_DONE [4:4] | None [3:2] | | SLEEPDEEP [1:1] | SLEEPING [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:13] | | | TCMC_AHB_MS [12:12] | TCMC_EXT_MS_3 [11:11] | TCMC_EXT_MS_2_TO_0 [10:10] | None [9:9] | TCMC_CM7_0_MS [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | SLEEPING | R | W | 1 | Specifies if the CPU is in Active, Sleep or DeepSleep power mode:<br>- Active power mode: SLEEPING is '0'.<br>- Sleep power mode: SLEEPING is '1' and SLEEPDEEP is '0'.<br>- DeepSleep power mode: SLEEPING is '1' and SLEEPDEEP is '1'. |
| 1 | SLEEPDEEP | R | W | 1 | Specifies if the CPU is in Sleep or DeepSleep power mode. See SLEEPING field. |
| 4 | PWR_DONE | R | W | 1 | After a PWR_MODE change this flag indicates if the new power mode has taken effect or not.<br>Note: this flag can also change as a result of a change in debug power up req |
| 8 | TCMC_CM7_0_MS | R | W | 0 | Outstanding transactions from CM7 0.<br>'0': There are no outstanding transactions to the CM7 I/D-TCM slave port (AHBS) from CM7 0.<br>'1': There are outstanding transactions to the CM7 I/D-TCM slave port (AHBS) from CM7 0. Do not switch the CM7 power off. |
| 10 | TCMC_EXT_MS_2_TO_0 | R | W | 0 | Refer CM7_0_STATUS description. |
| 11 | TCMC_EXT_MS_3 | R | W | 0 | Refer CM7_0_STATUS description. |
| 12 | TCMC_AHB_MS | R | W | 0 | Refer CM7_0_STATUS description. |

### 5.1.10 CPUSS_FAST_1_CLOCK_CTL

**Description:** Fast 1 clock control
**Address:** 0x40200408
**Offset:** 0x408
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Clock division control to divide and generate clk_fast_1 from clk_hf<x>. Note that this register is retained. However, the counter that is used to implement the division is not and will be initialized by HW to '0' when transitioning from DeepSleep to Active power mode.
Note that CM7 clocks must be running before accessing this register.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | FRAC_DIV [7:3] | | | | | None [2:0] | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | INT_DIV [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 3:7 | FRAC_DIV | RW | R | 0 | Refer FAST_0_CLOCK_CTL description. |
| 8:15 | INT_DIV | RW | R | 0 | Refer FAST_0_CLOCK_CTL description. |

### 5.1.11 CPUSS_CM7_1_CTL

**Description:** CM7 1 control
**Address:** 0x4020040C
**Offset:** 0x40C
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Note that CM7 clocks must be running before accessing this register.
**Default:** 0x1F

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:5] | | | CPU_WAIT [4:4] | PPB_LOCK [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:12] | | | | INIT_RMW_EN [11:10] | | INIT_TCM_EN [9:8] | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | TCMC_EN [23:23] | DTCM _READ _WS [22:22] | DTCM _ECC_INJ _EN [21:21] | DTCM _ECC_EN [20:20] | ITCM_ECC _CHECK _DIS [19:19] | ITCM _READ _WS [18:18] | ITCM_ECC _INJ_EN [17:17] | ITCM_ECC _EN [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | IDC_MASK [31:31] | None [30:29] | | IXC_MASK [28:28] | UFC_MASK [27:27] | OFC _MASK [26:26] | DZC_MASK [25:25] | IOC_MASK [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | PPB_LOCK | RW | R | 15 | Refer CM7_0_CTL description. |
| 4 | CPU_WAIT | RW | R | 1 | Refer CM7_0_CTL description. |
| 8:9 | INIT_TCM_EN | RW | R | 0 | Refer CM7_0_CTL description. |
| 10:11 | INIT_RMW_EN | RW | R | 0 | Refer CM7_0_CTL description. |
| 16 | ITCM_ECC_EN | RW | R | 0 | Refer CM7_0_CTL description. |
| 17 | ITCM_ECC_INJ_EN | RW | R | 0 | Refer CM7_0_CTL description. |
| 18 | ITCM_READ_WS | RW | R | 0 | Refer CM7_0_CTL description. |
| 19 | ITCM_ECC_CHECK_DIS | RW | R | 0 | Disable ECC checking and thus fault reports. This also disables ECC correction (required to enable initialization). Intended usage is initialization. This bit is ignored when TCM_ECC_EN=0. |
| 20 | DTCM_ECC_EN | RW | R | 0 | Refer CM7_0_CTL description. |
| 21 | DTCM_ECC_INJ_EN | RW | R | 0 | Refer CM7_0_CTL description. |
| 22 | DTCM_READ_WS | RW | R | 0 | Refer CM7_0_CTL description. |
| 23 | TCMC_EN | RW | R | 0 | Refer CM7_0_CTL description. |
| 24 | IOC_MASK | RW | R | 0 | Refer CM7_0_CTL description. |
| 25 | DZC_MASK | RW | R | 0 | Refer CM7_0_CTL description. |
| 26 | OFC_MASK | RW | R | 0 | Refer CM7_0_CTL description. |
| 27 | UFC_MASK | RW | R | 0 | Refer CM7_0_CTL description. |
| 28 | IXC_MASK | RW | R | 0 | Refer CM7_0_CTL description. |
| 31 | IDC_MASK | RW | R | 0 | Refer CM7_0_CTL description. |

### 5.1.12 CPUSS_CM7_1_INT_STATUS

**Description:** CM7 1 interrupt status
**Address:** 0x40200500
**Offset:** 0x500
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | SYSTEM_INT_IDX [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:10] | | | | | | SYSTEM_INT_IDX [9:8] | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | SYSTEM_INT_VALID [31:31] | None [30:24] | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:9 | SYSTEM_INT_IDX | R | W | Undefined | Lowest CM7_1 activated system interrupt index for CPU interrupt 0.<br><br>See description of CM0_INT0_STATUS. |
| 31 | SYSTEM_INT_VALID | R | W | 0 | See description of CM0_INT0_STATUS. |

### 5.1.13 CPUSS_CM7_1_VECTOR_TABLE_BASE

**Description:** CM7 1 vector table base
**Address:** 0x40200600
**Offset:** 0x600
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Note that CM7 clocks must be running before accessing this register.
**Default:** 0x1000000

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDR25 [7:7] | None [6:0] | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDR25 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDR25 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDR25 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 7:31 | ADDR25 | RW | R | 131072 | The default CM7 vector table base address is 0x0100:0000 (CM7 VTOR and reset exception handler address after reset). This is the location of the system ROM memory.<br><br>The system ROM is mirrored at 0x0000:0000. This is required for the CM0+ boot process (the CM0+ VTOR and reset exception handler address is at fixed address 0x0000:00000 after reset). The system ROM requires mirroring as the CM7 CPUs' ITCMs are located at base address 0x0000:0000 and effectively cut a hole in the system ROM mirror address space (but the 0x0100:0000 address space is not affected). |

### 5.1.14 CPUSS_CM7_1_NMI_CTL

**Description:** CM7 1 NMI control
**Address:** 0x40200640
**Offset:** 0x640
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x3FF

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | SYSTEM_INT_IDX [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:10] | | | | | | SYSTEM_INT_IDX [9:8] | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:9 | SYSTEM_INT_IDX | RW | R | 1023 | Refer CM7_0_NMI_CTL description. |

### 5.1.15 CPUSS_CM0_CTL

**Description:** CM0+ control
**Address:** 0x40201000
**Offset:** 0x1000
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xFA050002

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:2] | | | | | | ENABLED [1:1] | SLV _STALL [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VECTKEYSTAT [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VECTKEYSTAT [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | SLV_STALL | RW | R | 0 | Processor debug access control:<br>'0': Access.<br>'1': Stall access.<br><br>This field is used to stall/delay debug accesses. This is useful to protect execution of code that needs to be protected from debug accesses. |
| 1 | ENABLED | RW | RW1S | 1 | Processor enable:<br>'0': Disabled. Processor clock is turned off and reset is activated. After SW clears this field to '0', HW automatically sets this field to '1'. This effectively results in a CM0+ reset, followed by a CM0+ warm boot.<br>'1': Enabled.<br>Note: The intent is that this bit is modified only through an external probe or by the CM7 while the CM0+ is in Sleep or DeepSleep power mode. If this field is cleared to '0' by the CM0+ itself, it should be done under controlled conditions (such that undesirable side effects can be prevented).<br><br>Note: The CM0+ CPU has a AIRCR.SYSRESETREQ register field that allows the CM0+ to reset the complete device (ENABLED only disables/enables the CM0+), resulting in a warm boot. This CPU register field has similar 'built-in protection' as this CM0_CTL register to prevent accidental system writes (the upper 16-bits of the register need to be written with a 0x05fa key value; see CPU user manual for more details). |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 16:31 | VECTKEYSTAT | R | | 64005 | Register key (to prevent accidental writes).<br>- Should be written with a 0x05fa key value for the write to take effect.<br>- Always reads as 0xfa05.<br>Note: Although the SW attribute for this field says "R', SW need to write the key 0x05fa in this field for this register write to happen. This is a built in protection provided to prevent accidental writes from SW. |

### 5.1.16 CPUSS_CM0_STATUS

**Description:** CM0+ status
**Address:** 0x40201004
**Offset:** 0x1004
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:2] | | | | | | SLEEPDEEP [1:1] | SLEEPING [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | SLEEPING | R | W | 0 | Specifies if the CPU is in Active, Sleep or DeepSleep power mode:<br>- Active power mode: SLEEPING is '0'.<br>- Sleep power mode: SLEEPING is '1' and SLEEPDEEP is '0'.<br>- DeepSleep power mode: SLEEPING is '1' and SLEEPDEEP is '1'. |
| 1 | SLEEPDEEP | R | W | 0 | Specifies if the CPU is in Sleep or DeepSleep power mode. See SLEEPING field. |

### 5.1.17 CPUSS_SLOW_CLOCK_CTL

**Description:** Slow clock control
**Address:** 0x40201008
**Offset:** 0x1008
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | INT_DIV [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 8:15 | INT_DIV | RW | R | 0 | Specifies the slow clock divider (from the memory/AXI clock 'clk_mem' to the slow clock 'clk_slow'). Integer division by (1+INT_DIV). Allows for integer divisions in the range [1, 256] (INT_DIV is in the range [0, 255]).<br><br>Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to '0' when transitioning from DeepSleep to Active power mode. |

### 5.1.18 CPUSS_PERI_CLOCK_CTL

**Description:** Peripheral interconnect clock control
**Address:** 0x4020100C
**Offset:** 0x100C
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Clock division control to divide and generate clk_peri from clk_hf0.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | INT_DIV [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 8:15 | INT_DIV | RW | R | 0 | Integer division by (1+INT_DIV). Allows for integer divisions in the range [1, 256] (INT_DIV is in the range [0, 255]).<br>Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to '0' when transitioning from DeepSleep to Active power mode. |

### 5.1.19 CPUSS_MEM_CLOCK_CTL

**Description:** Memory clock control
**Address:** 0x40201010
**Offset:** 0x1010
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Clock division control to divide and generate clk_mem from clk_hf0.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | INT_DIV [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 8:15 | INT_DIV | RW | R | 0 | Integer division by (1+INT_DIV). Allows for integer divisions in the range [1, 256] (INT_DIV is in the range [0, 255]).<br>Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to '0' when transitioning from DeepSleep to Active power mode. |

### 5.1.20 CPUSS_CM0_INT0_STATUS

**Description:** CM0+ interrupt 0 status
**Address:** 0x40201100
**Offset:** 0x1100
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** Undefined as one or more bit fields have a default value that is undefined

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | SYSTEM_INT_IDX [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:10] | | | | | | SYSTEM_INT_IDX [9:8] | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | SYSTEM_INT_VALID [31:31] | None [30:24] | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:9 | SYSTEM_INT_IDX | R | W | Undefined | Lowest CM0+ activated system interrupt index for CPU interrupt 0.<br><br>Multiple system interrupts can be mapped on the same CPU interrupt.The selected system interrupt is the system interrupt with the lowest system interrupt index that has an activated interrupt request at the time of the fetch (system_interrupts[SYSTEM_INT_IDX] is '1').<br><br>The CPU interrupt handler SW can read SYSTEM_INT_IDX to determine the system interrupt that activated the handler. |
| 31 | SYSTEM_INT_VALID | R | W | 0 | Valid indication for SYSTEM_INT_IDX. When '0', no system interrupt for CPU interrupt 0 is valid/activated. |

### 5.1.21 CPUSS_CM0_INT1_STATUS

**Description:** CM0+ interrupt 1 status
**Address:** 0x40201104
**Offset:** 0x1104
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** Undefined as one or more bit fields have a default value that is undefined

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | SYSTEM_INT_IDX [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:10] | | | | | | SYSTEM_INT_IDX [9:8] | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | SYSTEM_INT_VALID [31:31] | None [30:24] | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:9 | SYSTEM_INT_IDX | R | W | Undefined | Lowest CM0+ activated system interrupt index for CPU interrupt 1.<br><br>See description of CM0_INT0_STATUS. |
| 31 | SYSTEM_INT_VALID | R | W | 0 | See description of CM0_INT0_STATUS. |

### 5.1.22 CPUSS_CM0_INT2_STATUS

**Description:** CM0+ interrupt 2 status
**Address:** 0x40201108
**Offset:** 0x1108
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** Undefined as one or more bit fields have a default value that is undefined

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | SYSTEM_INT_IDX [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:10] | | | | | | SYSTEM_INT_IDX [9:8] | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | SYSTEM_INT_VALID [31:31] | None [30:24] | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:9 | SYSTEM_INT_IDX | R | W | Undefined | Lowest CM0+ activated system interrupt index for CPU interrupt 2.<br><br>See description of CM0_INT0_STATUS. |
| 31 | SYSTEM_INT_VALID | R | W | 0 | See description of CM0_INT0_STATUS. |

### 5.1.23 CPUSS_CM0_INT3_STATUS

**Description:** CM0+ interrupt 3 status
**Address:** 0x4020110C
**Offset:** 0x110C
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** Undefined as one or more bit fields have a default value that is undefined

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | SYSTEM_INT_IDX [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:10] | | | | | | SYSTEM_INT_IDX [9:8] | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | SYSTEM_INT_VALID [31:31] | None [30:24] | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:9 | SYSTEM_INT_IDX | R | W | Undefined | Lowest CM0+ activated system interrupt index for CPU interrupt 3.<br><br>See description of CM0_INT0_STATUS. |
| 31 | SYSTEM_INT_VALID | R | W | 0 | See description of CM0_INT0_STATUS. |

### 5.1.24 CPUSS_CM0_INT4_STATUS

**Description:** CM0+ interrupt 4 status
**Address:** 0x40201110
**Offset:** 0x1110
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** Undefined as one or more bit fields have a default value that is undefined

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | SYSTEM_INT_IDX [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:10] | | | | | | SYSTEM_INT_IDX [9:8] | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | SYSTEM_INT_VALID [31:31] | None [30:24] | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:9 | SYSTEM_INT_IDX | R | W | Undefined | Lowest CM0+ activated system interrupt index for CPU interrupt 4.<br><br>See description of CM0_INT0_STATUS. |
| 31 | SYSTEM_INT_VALID | R | W | 0 | See description of CM0_INT0_STATUS. |

### 5.1.25 CPUSS_CM0_INT5_STATUS

**Description:** CM0+ interrupt 5 status
**Address:** 0x40201114
**Offset:** 0x1114
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** Undefined as one or more bit fields have a default value that is undefined

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | SYSTEM_INT_IDX [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:10] | | | | | | SYSTEM_INT_IDX [9:8] | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | SYSTEM_INT_VALID [31:31] | None [30:24] | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:9 | SYSTEM_INT_IDX | R | W | Undefined | Lowest CM0+ activated system interrupt index for CPU interrupt 5.<br><br>See description of CM0_INT0_STATUS. |
| 31 | SYSTEM_INT_VALID | R | W | 0 | See description of CM0_INT0_STATUS. |

### 5.1.26 CPUSS_CM0_INT6_STATUS

**Description:** CM0+ interrupt 6 status
**Address:** 0x40201118
**Offset:** 0x1118
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** Undefined as one or more bit fields have a default value that is undefined

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | SYSTEM_INT_IDX [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:10] | | | | | | SYSTEM_INT_IDX [9:8] | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | SYSTEM_INT_VALID [31:31] | None [30:24] | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:9 | SYSTEM_INT_IDX | R | W | Undefined | Lowest CM0+ activated system interrupt index for CPU interrupt 6.<br><br>See description of CM0_INT0_STATUS. |
| 31 | SYSTEM_INT_VALID | R | W | 0 | See description of CM0_INT0_STATUS. |

### 5.1.27 CPUSS_CM0_INT7_STATUS

**Description:** CM0+ interrupt 7 status
**Address:** 0x4020111C
**Offset:** 0x111C
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** Undefined as one or more bit fields have a default value that is undefined

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | SYSTEM_INT_IDX [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:10] | | | | | | SYSTEM_INT_IDX [9:8] | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | SYSTEM_INT_VALID [31:31] | None [30:24] | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:9 | SYSTEM_INT_IDX | R | W | Undefined | Lowest CM0+ activated system interrupt index for CPU interrupt 7.<br><br>See description of CM0_INT0_STATUS. |
| 31 | SYSTEM_INT_VALID | R | W | 0 | See description of CM0_INT0_STATUS. |

### 5.1.28 CPUSS_CM0_VECTOR_TABLE_BASE

**Description:** CM0+ vector table base
**Address:** 0x40201120
**Offset:** 0x1120
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDR24 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDR24 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDR24 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 8:31 | ADDR24 | RW | | 0 | The default CM0+ vector table base address is 0x0000:0000 (CM0+ VTOR and reset exception handler address after reset). This is the location of the mirror system ROM memory.<br><br>This register is provided for SW purposes. It 'survives' a CM0+ warm reset cycle (CM0_CTL.ENABLED).<br><br>Note: the use of the mirror system ROM memory can be disabled using the protection infrastructure (SMPU). |

### 5.1.29 CPUSS_CM0_NMI_CTL

**Description:** CM0+ NMI control
**Address:** 0x40201140
**Offset:** 0x1140
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Note that multiple (four) CM0_NMI_CTL registers exist, allowing for multiple (four) system interrupts to be connnected to the CPU NMI. The four selected system interrupts are logically OR'd into a single CPU NMI input. The NMI handler may need to investigate all selected system interrupt sources to identify the source of CPU NMI.
**Default:** 0x3FF

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | SYSTEM_INT_IDX [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:10] | | | | | | SYSTEM_INT_IDX [9:8] | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:9 | SYSTEM_INT_IDX | RW | R | 1023 | System interrupt select for CPU NMI. The reset value ('1023') ensures that the CPU NMI is NOT connected to any system interrupt after DeepSleep reset. |

### 5.1.30 CPUSS_CM7_0_PWR_CTL

**Description:** CM7 0 power control
**Address:** 0x40201200
**Offset:** 0x1200
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register controls the CM7_0 power state. Please note that this register must not be modified while the CM7_0 is executing; doing so may corrupt/abort pending bus transaction by the CM7_0 and cause unexpected behaviors in the system, including deadlock. The intended usage of this register is by the CM0+ while the CM7_0 is in DeepSleep mode.
Note that CM7 clocks must be running before accessing this register.
**Default:** 0xFA050000

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:2] | | | | | | PWR_MODE [1:0] | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VECTKEYSTAT [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VECTKEYSTAT [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:1 | PWR_MODE | RW | R | 0 | Power mode. |
| | OFF | | | 0 | Switch CM7_0 off<br>Power off, clock off, isolate, reset and no retain. |
| | RESET | | | 1 | Reset CM7_0<br>Clock off, no isolated, no retain and reset.<br><br>Note: The CM7_0 CPU has a AIRCR.SYSRESETREQ register field that allows the CM7_0 to reset the complete device (RESET only resets the CM7_0), resulting in a warm boot. |
| | RETAINED | | | 2 | Put CM7_0 in Retained mode<br>This can only become effective if CM7_0 is in SleepDeep mode. Check PWR_DONE flag to see if CM7_0 RETAINED state has been reached.<br>Power off, clock off, isolate, no reset and retain. |
| | ENABLED | | | 3 | Switch CM7_0 on.<br>Power on, clock on, no isolate, no reset and no retain. |
| 16:31 | VECTKEYSTAT | R | | 64005 | Register key (to prevent accidental writes).<br>- Should be written with a 0x05fa key value for the write to take effect.<br>- Always reads as 0xfa05.<br><br>Note: Although the SW attribute for this field says "R', SW need to write the key 0x05fa in this field for this register write to happen. This is a built in protection provided to prevent accidental writes from SW. |

### 5.1.31 CPUSS_CM7_0_PWR_DELAY_CTL

**Description:** CM7 0 power delay control
**Address:** 0x40201204
**Offset:** 0x1204
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Note that CM7 clocks must be running before accessing this register.
**Default:** 0x12C

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | UP [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:10] | | | | | | UP [9:8] | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:9 | UP | RW | R | 300 | Number clock cycles delay needed after power domain power up |

### 5.1.32 CPUSS_CM7_1_PWR_CTL

**Description:** CM7 1 power control
**Address:** 0x40201210
**Offset:** 0x1210
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Note that CM7 clocks must be running before accessing this register.
**Default:** 0xFA050000

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:2] | | | | | | PWR_MODE [1:0] | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VECTKEYSTAT [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VECTKEYSTAT [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:1 | PWR_MODE | RW | R | 0 | Refer CM7_0_PWR_CTL description. |
| | OFF | | | 0 | Refer CM7_0_PWR_CTL description. |
| | RESET | | | 1 | Refer CM7_0_PWR_CTL description. |
| | RETAINED | | | 2 | Refer CM7_0_PWR_CTL description. |
| | ENABLED | | | 3 | Refer CM7_0_PWR_CTL description. |
| 16:31 | VECTKEYSTAT | R | | 64005 | Refer CM7_0_PWR_CTL description. |

### 5.1.33 CPUSS_CM7_1_PWR_DELAY_CTL

**Description:** CM7 1 power delay control
**Address:** 0x40201214
**Offset:** 0x1214
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Note that CM7 clocks must be running before accessing this register.
**Default:** 0x12C

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | UP [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:10] | | | | | | UP [9:8] | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:9 | UP | RW | R | 300 | Number clock cycles delay needed after power domain power up |

### 5.1.34 CPUSS_RAM0_CTL0

**Description:** RAM 0 control
**Address:** 0x40201300
**Offset:** 0x1300
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x30001

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:2] | | | | | | SLOW_WS [1:0] | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:10] | | | | | | FAST_WS [9:8] | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:20] | | | | ECC_CHECK_DIS [19:19] | ECC_INJ_EN [18:18] | ECC_AUTO_CORRECT [17:17] | ECC_EN [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:1 | SLOW_WS | RW | R | 1 | Memory wait states for the slow clock domain ('clk_slow') intefrace. The number of wait states is expressed in 'clk_mem' clock domain cycles. |
| 8:9 | FAST_WS | RW | R | 0 | Memory wait states for the fast clock domain ('clk_fast_0/1') interface. The number of wait states is expressed in 'clk_mem' clock domain cycles. |
| 16 | ECC_EN | RW | R | 1 | Enable ECC checking:<br>'0': Disabled.<br>'1': Enabled. |
| 17 | ECC_AUTO_CORRECT | RW | R | 1 | HW ECC autocorrect functionality:<br>'0': Disabled.<br>'1': Enabled. HW automatically writes back SRAM with corrected data when a recoverable ECC error is detected. |
| 18 | ECC_INJ_EN | RW | R | 0 | Enable ECC parity injection. Instead of calculating the parity from the write data to the RAM, the parity is taken from ECC_CTL PARITY upon a match of ECC_CTL WORD_ADDR. The write data can be of any size. This bit is ignored when ECC_EN=0.<br>Note: Parity injection invalidates the write buffer for this word address. If only a part of 64-bit data is written and consistency should be maintained, RAMC#_STATUS WB_EMPTY=1 should be checked before. |
| 19 | ECC_CHECK_DIS | RW | R | 0 | Disable ECC checking and thus fault reports. This also disables ECC correction (required to enable initialization). Intended usage is initialization. This bit is ignored when ECC_EN=0. |

### 5.1.35 CPUSS_RAM0_STATUS

**Description:** RAM 0 status
**Address:** 0x40201304
**Offset:** 0x1304
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register is for the CPUSS system SRAM controller 0.
**Default:** 0x1

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:1] | | | | | | | WB _EMPTY [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | WB_EMPTY | R | W | 1 | Write buffer empty. This information is used when entering DeepSleep power mode: WB_EMPTY must be '1' before a transition to system DeepSleep power mode.<br>'0': Write buffer NOT empty.<br>'1': Write buffer empty.<br><br>Note: the SRAM controller write buffer is only used when ECC checking is enabled. (RAMi_CTL.ECC_EN is '1'). |

### 5.1.36 CPUSS_RAM0_PWR_MACRO_CTL

**Description:** RAM 0 power control
**Address:** 0x40201340
**Offset:** 0x1340
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** These registers control the system SRAM 0 power states of a single macro. System SRAM 0 consists of up to sixteen 32 kB macros. Each macro is a single power partition and is controlled through a dedicated control field in one of these registers.
**Default:** 0xFA050003

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:2] | | | | | | PWR_MODE [1:0] | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VECTKEYSTAT [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VECTKEYSTAT [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:1 | PWR_MODE | RW | R | 3 | Power mode. |
| | OFF | | | 0 | Turn OFF the SRAM. This will trun OFF both array and periphery power of the SRAM and SRAM memory contents are lost. |
| | RESERVED | | | 1 | undefined |
| | RETAINED | | | 2 | Keep SRAM in Retained mode. This will turn OFF the SRAM periphery power, but array power is ON to retain memory contents. |
| | ENABLED | | | 3 | Enable SRAM for regular operation. |
| 16:31 | VECTKEYSTAT | R | | 64005 | Register key (to prevent accidental writes).<br>- Should be written with a 0x05fa key value for the write to take effect.<br>- Always reads as 0xfa05.<br>Note: Although the SW attribute for this field says "R', SW need to write the key 0x05fa in this field for this register write to happen. This is a built in protection provided to prevent accidental writes from SW. |

### 5.1.37 CPUSS_RAM1_CTL0

**Description:** RAM 1 control
**Address:** 0x40201380
**Offset:** 0x1380
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register is for the CPUSS system SRAM controller 1.
**Default:** 0x30001

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:2] | | | | | | SLOW_WS [1:0] | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:10] | | | | | | FAST_WS [9:8] | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:20] | | | | ECC_CHECK_DIS [19:19] | ECC_INJ_EN [18:18] | ECC_AUTO_CORRECT [17:17] | ECC_EN [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:1 | SLOW_WS | RW | R | 1 | Refer RAM0_CTL0 descriotion. |
| 8:9 | FAST_WS | RW | R | 0 | Refer RAM0_CTL0 descriotion. |
| 16 | ECC_EN | RW | R | 1 | Refer RAM0_CTL0 descriotion. |
| 17 | ECC_AUTO_CORRECT | RW | R | 1 | Refer RAM0_CTL0 descriotion. |
| 18 | ECC_INJ_EN | RW | R | 0 | Enable ECC parity injection. Instead of calculating the parity from the write data to the RAM, the parity is taken from ECC_CTL PARITY upon a match of ECC_CTL WORD_ADDR. The write data can be of any size. This bit is ignored when ECC_EN=0.<br>Note: Parity injection invalidates the write buffer for this word address. If only a part of 64-bit data is written and consistency should be maintained, RAMC#_STATUS WB_EMPTY=1 should be checked before. |
| 19 | ECC_CHECK_DIS | RW | R | 0 | Disable ECC checking and thus fault reports. This also disables ECC correction (required to enable initialization). Intended usage is initialization. This bit is ignored when ECC_EN=0. |

### 5.1.38 CPUSS_RAM1_STATUS

**Description:** RAM 1 status
**Address:** 0x40201384
**Offset:** 0x1384
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register is for the CPUSS system SRAM controller 1.
**Default:** 0x1

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:1] | | | | | | | WB _EMPTY [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | WB_EMPTY | R | W | 1 | Refer RAM0_STATUS description. |

### 5.1.39 CPUSS_RAM1_PWR_CTL

**Description:** RAM 1 power control
**Address:** 0x40201388
**Offset:** 0x1388
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register controls the system SRAM 1 power states. System SRAM 1 consists of a single power partition.
**Default:** 0xFA050003

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:2] | | | | | | PWR_MODE [1:0] | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VECTKEYSTAT [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VECTKEYSTAT [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:1 | PWR_MODE | RW | R | 3 | Power mode. |
| | OFF | | | 0 | Refer RAM0_PWR_MACRO_CTL description. |
| | RESERVED | | | 1 | Undefined. |
| | RETAINED | | | 2 | Refer RAM0_PWR_MACRO_CTL description. |
| | ENABLED | | | 3 | Refer RAM0_PWR_MACRO_CTL description. |
| 16:31 | VECTKEYSTAT | R | | 64005 | Refer RAM0_PWR_MACRO_CTL description. |

### 5.1.40 CPUSS_RAM2_CTL0

**Description:** RAM 2 control
**Address:** 0x402013A0
**Offset:** 0x13A0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register is for the CPUSS system SRAM controller 2.
**Default:** 0x30001

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:2] | | | | | | SLOW_WS [1:0] | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:10] | | | | | | FAST_WS [9:8] | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:20] | | | | ECC_CHECK_DIS [19:19] | ECC_INJ_EN [18:18] | ECC_AUTO_CORRECT [17:17] | ECC_EN [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:1 | SLOW_WS | RW | R | 1 | Refer RAM0_CTL0 descriotion. |
| 8:9 | FAST_WS | RW | R | 0 | Refer RAM0_CTL0 descriotion. |
| 16 | ECC_EN | RW | R | 1 | Refer RAM0_CTL0 descriotion. |
| 17 | ECC_AUTO_CORRECT | RW | R | 1 | Refer RAM0_CTL0 descriotion. |
| 18 | ECC_INJ_EN | RW | R | 0 | Enable ECC parity injection. Instead of calculating the parity from the write data to the RAM, the parity is taken from ECC_CTL PARITY upon a match of ECC_CTL WORD_ADDR. The write data can be of any size. This bit is ignored when ECC_EN=0.<br>Note: Parity injection invalidates the write buffer for this word address. If only a part of 64-bit data is written and consistency should be maintained, RAMC#_STATUS WB_EMPTY=1 should be checked before. |
| 19 | ECC_CHECK_DIS | RW | R | 0 | Disable ECC checking and thus fault reports. This also disables ECC correction (required to enable initialization). Intended usage is initialization. This bit is ignored when ECC_EN=0. |

### 5.1.41 CPUSS_RAM2_STATUS

**Description:** RAM 2 status
**Address:** 0x402013A4
**Offset:** 0x13A4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x1

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:1] | | | | | | | WB _EMPTY [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | WB_EMPTY | R | W | 1 | Refer RAM0_STATUS description. |

### 5.1.42 CPUSS_RAM2_PWR_CTL

**Description:** RAM 2 power control
**Address:** 0x402013A8
**Offset:** 0x13A8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xFA050003

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:2] | | | | | | PWR_MODE [1:0] | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VECTKEYSTAT [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VECTKEYSTAT [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:1 | PWR_MODE | RW | R | 3 | Power mode. |
| | OFF | | | 0 | Refer RAM0_PWR_MACRO_CTL description. |
| | RESERVED | | | 1 | Undefined. |
| | RETAINED | | | 2 | Refer RAM0_PWR_MACRO_CTL description. |
| | ENABLED | | | 3 | Refer RAM0_PWR_MACRO_CTL description. |
| 16:31 | VECTKEYSTAT | R | | 64005 | Refer RAM0_PWR_MACRO_CTL description. |

### 5.1.43 CPUSS_RAM_PWR_DELAY_CTL

**Description:** Power up delay used for all SRAM power domains
**Address:** 0x402013C0
**Offset:** 0x13C0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x96

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | UP [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:10] | | | | | | UP [9:8] | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:9 | UP | RW | R | 150 | Number clock cycles delay needed after power domain power up |

### 5.1.44 CPUSS_ROM_CTL

**Description:** ROM control
**Address:** 0x402013C4
**Offset:** 0x13C4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x1

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:2] | | | | | | SLOW_WS [1:0] | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:10] | | | | | | FAST_WS [9:8] | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:1 | SLOW_WS | RW | R | 1 | Memory wait states for the slow clock domain ('clk_slow'). The number of wait states is expressed in 'clk_mem' clock domain cycles.<br><br>Timing paths to and from the memory have a (fixed) minimum duration that always needs to be considered/met. The 'clk_mem' clock domain frequency determines this field's value such that the timing paths minimum duration is met.<br>ROM_CTL.SLOW_WS = '0' when clk_mem <=100 MHz.<br>ROM_CTL.SLOW_WS = '1' when 100MHz < clk_mem <=200MHz. |
| 8:9 | FAST_WS | RW | R | 0 | Memory wait states for the fast clock domain ('clk_fast'). The number of wait states is expressed in 'clk_mem' clock domain cycles.<br>ROM_CTL.FAST_WS = '0' when clk_mem <= 200MHz. |

### 5.1.45 CPUSS_ECC_CTL

**Description:** ECC control
**Address:** 0x402013C8
**Offset:** 0x13C8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | WORD_ADDR [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | WORD_ADDR [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | WORD_ADDR [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | PARITY [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:23 | WORD_ADDR | RW | R | 0 | Specifies the word address where an error will be injected.<br>- On a write transfer to this SRAM address and when the corresponding RAM0/RAM1/RAM2/ITCM/DTCM ECC_INJ_EN bit is '1', the parity (PARITY) is injected. This field needs to be written with the offset address within the memory, divided by the ECC word width in bytes (for RAM0/RAM1/RAM2/ITCM this is 8, for DTCM this is 4). For example, if the RAM0 start address is 0x2800000, and an error is to be injected to address 0x28000080, then this field needs to configured to 0x000010. |
| 24:31 | PARITY | RW | R | 0 | ECC parity to use for ECC error injection at address WORD_ADDR. For the DTCM which has only 7 parity bits, PARITY[6:0] is used as ECC parity. |

### 5.1.46 CPUSS_PRODUCT_ID

**Description:** Product identifier and version (same as CoreSight RomTables)
**Address:** 0x40201400
**Offset:** 0x1400
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** Undefined as one or more bit fields have a default value that is undefined

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | FAMILY_ID [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:12] | | | | FAMILY_ID [11:8] | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | MINOR_REV [23:20] | | | | MAJOR_REV [19:16] | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:11 | FAMILY_ID | R | W | 259 | Family ID. Common ID for a product family. |
| 16:19 | MAJOR_REV | R | W | Undefined | Major Revision, starts with 1, increments with all layer tape-out (implemented with metal ECO-able tie-off) |
| 20:23 | MINOR_REV | R | W | Undefined | Minir Revision, starts with 1, increments with metal layer only tape-out (implemented with metal ECO-able tie-off) |

### 5.1.47 CPUSS_DP_STATUS

**Description:** Debug port status
**Address:** 0x40201410
**Offset:** 0x1410
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x4

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:3] | | | | | SWJ_JTAG_SEL [2:2] | SWJ_DEBUG_EN [1:1] | SWJ_CONNECTED [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | SWJ_CONNECTED | R | W | 0 | Specifies if the SWJ debug port is connected; i.e. debug host interface is active:<br>'0': Not connected/not active.<br>'1': Connected/active. |
| 1 | SWJ_DEBUG_EN | R | W | 0 | Specifies if SWJ debug is enabled, i.e. CDBGPWRUPACK is '1' and thus debug clocks are on:<br>'0': Disabled.<br>'1': Enabled. |
| 2 | SWJ_JTAG_SEL | R | W | 1 | Specifies if the JTAG or SWD interface is selected. This signal is valid when DP_CTL.PTM_SEL is '0' (SWJ mode selected) and SWJ_CONNECTED is '1' (SWJ is connected).<br>'0': SWD selected.<br>'1': JTAG selected. |

### 5.1.48 CPUSS_AP_CTL

**Description:** Access port control
**Address:** 0x40201414
**Offset:** 0x1414
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register enables individual test controller access ports (AP). Note that the system AP is further controlled by a AP specific MPU, the SMPU and PPUs. The system AP MPU may be programmed to provide no or limited test controller access capabilities.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:3] | | | | | SYS _ENABLE [2:2] | CM7 _ENABLE [1:1] | CM0 _ENABLE [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:19] | | | | | SYS _DISABLE [18:18] | CM7 _DISABLE [17:17] | CM0 _DISABLE [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | CM0_ENABLE | RW | R | 0 | Enables the CM0 AP interface:<br>'0': Disabled.<br>'1': Enabled. |
| 1 | CM7_ENABLE | RW | R | 0 | Enables the CM7_0 and CM7_1 AP interface:<br>'0': Disabled.<br>'1': Enabled. |
| 2 | SYS_ENABLE | RW | R | 0 | Enables the system AP interface:<br>'0': Disabled.<br>'1': Enabled. |
| 16 | CM0_DISABLE | RW1S | R | 0 | Disables the CM0 AP interface:<br>'0': Enabled.<br>'1': Disabled.<br><br>Typically, this field is set by the Cypress boot code with information from eFUSE. The access port is only enabled when CM0_DISABLE is '0' and CM0_ENABLE is '1'. |
| 17 | CM7_DISABLE | RW1S | R | 0 | Disables the CM7_0 and CM7_1 AP interface:<br>'0': Enabled.<br>'1': Disabled.<br><br>Typically, this field is set by the Cypress boot code with information from eFUSE. The access port is only enabled when CM7_DISABLE is '0' and CM7_ENABLE is '1'. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 18 | SYS_DISABLE | RW1S | R | 0 | Disables the system AP interface:<br>'0': Enabled.<br>'1': Disabled.<br><br>Typically, this field is set by the Cypress boot code with information from eFUSE. The access port is only enabled when SYS_DISABLE is '0' and SYS_ENABLE is '1'. |

### 5.1.49 CPUSS_BUFF_CTL

**Description:** Buffer control
**Address:** 0x40201500
**Offset:** 0x1500
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** The ARM CM0+ and CM7 CPUs use bufferable write transfers to the peripherals by default. As a result, CPU completion of the write transfer does not guarantee that the write transfer reached its destination, as the transfer may be buffered/posted in the bus infrastructure. Moreover, it is possible that the write transfer does not take place at all due to a PPU violation or a slave error, and in this case the resulting bus error response is not passed to the CPU. This may cause complications if the CPU assumes that completion of the write transfer implies that the write transfer has taken effect in a peripheral (e.g. clearing a peripheral's interrupt cause field). There are multiple possibilities to address this complication:
- Follow the write transfer with a read transfer from the same address, and check that the read data matches the expectation.
- Configure a fault structure such that the following faults are reported: MS_PPU_0 to MS_PPU_4 to report PPU violations, timeout or bus errors in the PERI master interfaces, and GROUP_FAULT_0 to GROUP_FAULT_15 (only for the existing peripheral groups) to report decode or slave errors in the peripheral groups. The CPU can perform a read transfer after a series of write transfers to the same peripheral group. If the read transfer completes and no faults are reported, then the write transfers have been executed. Note that the fault reporting has some latency, so the faults may be reported after the completion of the read transfer.
- Use the CPU MPU to set write transfers to non-bufferable/non-posted.
- Use BUFF_CTL.WRITE_BUFF to ensure that all write transfers are non-bufferable/non-posted.
**Default:** 0x1

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:1] | | | | | | | WRITE_BUFF [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | WRITE_BUFF | RW | R | 1 | Specifies if write transfer can be buffered in the bus infrastructure bridges:<br>'0': Write transfers are not buffered, independent of the transfer's bufferable attribute.<br>'1': Write transfers can be buffered, if the transfer's bufferable attribute indicates that the transfer is a bufferable/posted write. |

### 5.1.50 CPUSS_SYSTICK_CTL

**Description:** SysTick timer control
**Address:** 0x40201600
**Offset:** 0x1600
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** The CPUSS SYSTICK_CTL MMIO NOREF, SKEW, TENMS register fields are reflected in the CPU's SysTick timer calibration register: SYST_CALIB (the CLOCK_SOURCE field is NOT reflected and only SW accessible through the CPUSS SYSTICK_CTL MMIO register).
**Default:** 0x40000147

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | TENMS [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | TENMS [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | TENMS [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | NOREF [31:31] | SKEW [30:30] | None [29:26] | | | | CLOCK_SOURCE [25:24] | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:23 | TENMS | RW | R | 327 | Specifies the number of clock source cycles (minus 1) that make up 10 ms. E.g., for a 32,768 Hz reference clock, TENMS is 328 - 1 = 327. |
| 24:25 | CLOCK_SOURCE | RW | R | 0 | Specifies an external clock source:<br>'0': The low frequency clock 'clk_lf' is selected. The precision of this clock depends on whether the low frequency clock source is a SRSS internal RC oscillator (imprecise) or a device external crystal oscillator (precise).<br>'1': The internal main oscillator (IMO) clock 'clk_imo' is selected. The MXS40 platform uses a fixed frequency IMO clock.<br>o '2': The external crystal oscillator (ECO) clock 'clk_eco' is selected.<br>'3': The SRSS 'clk_timer' is selected ('clk_timer' is a divided/gated version of 'clk_hf' or 'clk_imo').<br><br>Note: If NOREF is '1', the CLOCK_SOURCE value is NOT used.<br>Note: It is SW's responsibility to provide the correct NOREF, SKEW and TENMS field values for the selected clock source. |
| 30 | SKEW | RW | R | 1 | Specifies the precision of the clock source and if the TENMS field represents exactly 10 ms (clock source frequency is a multiple of 100 Hz). This affects the suitability of the SysTick timer as a SW real-time clock:<br>'0': Precise.<br>'1': Imprecise. |
| 31 | NOREF | RW | R | 0 | Specifies if an external clock source is provided:<br>'0': An external clock source is provided.<br>'1': An external clock source is NOT provided and only the CPU internal clock can be used as SysTick timer clock source. |

### 5.1.51 CPUSS_CAL_SUP_SET

**Description:** Calibration support set and read
**Address:** 0x40201800
**Offset:** 0x1800
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** For ETAS support
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | DATA | RW1S | RW | 0 | Read without side effect, write 1 to set |

### 5.1.52 CPUSS_CAL_SUP_CLR

**Description:** Calibration support clear and reset
**Address:** 0x40201804
**Offset:** 0x1804
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Read side effect: reset on read (even when read from debug host)
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | DATA | RW1C | A | 0 | Read side effect: when read all bits are cleared, write 1 to clear a specific bit<br>Note: no exception for the debug host, it also causes the read side effect |

### 5.1.53 CPUSS_CM0_PC_CTL

**Description:** CM0+ protection context control
**Address:** 0x40202000
**Offset:** 0x2000
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** The CM0_PC_CTL and CM0_Pci_HANDLER register are typically initialized by the boot code.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:4] | | | | VALID [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | VALID | RW | R | 0 | Valid fields for the protection context handler CM0_PCi_HANDLER registers:<br>Bit 0: Valid field for CM0_PC0_HANDLER.<br>Bit 1: Valid field for CM0_PC1_HANDLER.<br>Bit 2: Valid field for CM0_PC2_HANDLER.<br>Bit 3: Valid field for CM0_PC3_HANDLER. |

### 5.1.54 CPUSS_CM0_PC0_HANDLER

**Description:** CM0+ protection context 0 handler
**Address:** 0x40202040
**Offset:** 0x2040
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDR [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDR [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDR [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDR [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | ADDR | RW | R | 0 | Address of the protection context 0 handler. This field is used to detect entry to Cypress 'trusted' code through an exception/interrupt. |

### 5.1.55 CPUSS_CM0_PC1_HANDLER

**Description:** CM0+ protection context 1 handler
**Address:** 0x40202044
**Offset:** 0x2044
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDR [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDR [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDR [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDR [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | ADDR | RW | R | 0 | Address of the protection context 1 handler. |

### 5.1.56 CPUSS_CM0_PC2_HANDLER

**Description:** CM0+ protection context 2 handler
**Address:** 0x40202048
**Offset:** 0x2048
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDR [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDR [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDR [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDR [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | ADDR | RW | R | 0 | Address of the protection context 2 handler. |

### 5.1.57 CPUSS_CM0_PC3_HANDLER

**Description:** CM0+ protection context 3 handler
**Address:** 0x4020204C
**Offset:** 0x204C
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDR [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDR [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDR [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDR [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | ADDR | RW | R | 0 | Address of the protection context 3 handler. |

### 5.1.58 CPUSS_PROTECTION

**Description:** Protection status
**Address:** 0x402020C4
**Offset:** 0x20C4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:3] | | | | | STATE [2:0] | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:2 | STATE | RW | R | 0 | Protection state:<br>'0': UNKNOWN.<br>'1': VIRGIN.<br>'2': NORMAL.<br>'3': SECURE.<br>'4': DEAD.<br><br>The following state transistions are allowed (and enforced by HW):<br>- UNKNOWN => VIRGIN/NORMAL/SECURE/DEAD<br>- NORMAL => DEAD<br>- SECURE => DEAD<br>An attempt to make a NOT allowed state transition will NOT affect this register field. |
| | UNKNOWN | | | 0 | N/A |
| | VIRGIN | | | 1 | N/A |
| | NORMAL | | | 2 | N/A |
| | SECURE | | | 3 | N/A |
| | DEAD | | | 4 | N/A |

### 5.1.59 CPUSS_TRIM_ROM_CTL

**Description:** ROM trim control
**Address:** 0x40202100
**Offset:** 0x2100
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register is used to trim ALL ROM memories in the device. Different operating Voltages may require different trim settings.
SW should change the TRIM settings appropriately while chaning the core operating voltage (E.g while switchting from 1.1v to 0.9v or vice versa on a ULP device).
Refer respective ROM IP BROS for the trim settings required based on operating voltage.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:3] | | | | | TRIM [2:0] | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:2 | TRIM | RW | R | 2 | For ARM ROMs the bits are defined as follows<br>[2:0] EMA: Extra Margin Adjustment (0 is the fastest setting)<br>Recommended default value: EMA=2 (ROM_TRIM_DEFAULT=0x0000_0002, ROM_TRIM_WIDTH=3)<br><br>For Synopsys ROMs the bits are defined as follows:<br>[3:0] RM: Read-Write margin control. This is used for setting the Read-Write margin. It programs the sense amplifier differential setting and allows the trade off between speed and robustness.<br>- RM[1:0] values control access time and cycle time of the memory. RM[1:0] = '0' is the slowest possible mode of operation for the memory. This setting is required for VDDMIN operation.<br>- RM[3:2] are factory pins reserved for debug mode and should be set to '0'.<br>[4] RME: Read-Write margin enable control. This selects between the default Read-Write margin setting, and the external pin Read-Write margin settting.<br>Recommended default value for LP: RME=1, RM=2 (ROM_TRIM_DEFAULT=0x0000_0012, ROM_TRIM_WIDTH=5)<br>Recommended default value for ULP: RME=1, RM=3 (ROM_TRIM_DEFAULT=0x0000_0013, ROM_TRIM_WIDTH=5) |

### 5.1.60 CPUSS_TRIM_RAM_CTL

**Description:** RAM trim control for less than 100MHz SRAMs
**Address:** 0x40202104
**Offset:** 0x2104
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register is used to trim SRAM memories clocked at 100MHz or less in the device.
Different operating Voltages may require different trim settings.
SW should change the TRIM settings appropriately while chaning the core operating voltage (E.g while switchting from 1.1v to 0.9v or vice versa on a ULP device).
Refer respective SRAM IP BROS for the trim settings required based on operating voltage.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | TRIM [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | TRIM | RW | R | 98 | For ARM RAMs the bits are defined as follows<br>[2:0] EMA: Extra Margin Adjustment (0 is the fastest setting)<br>[4:3] EMAW: Extra Margin Adjustment for Writes (0 is the fastest setting)<br>'[7:5] CTL_BIAS: Control the SRAM retention mode back bias control circuit in the SRAM power switches that implement bias control: 0=no back bias; 1=max back bias, 7=min back bias'<br>Recommended default value: CTL_BIAS=3, EMAW=0, EMA=2 (RAM_TRIM_DEFAULT=0x0000_0062, RAM_TRIM_WIDTH=8)<br><br>Note: DW0, DW1 SRAMs uses bias control power switches.<br><br>For Synopsys RAMs the bits are defined as follows:<br>[3:0] Read-Write margin control. This is used for setting the Read-Write margin. It programs the sense amplifier differential setting and allows the trade off between speed and robustness.<br>- RM[1:0] values control access time and cycle time of the memory. RM[1:0] = '0' is the slowest possible mode of operation for the memory. This setting is required for VDDMIN operation.<br>- RM[3:2] are factory pins reserved for debug mode and should be set to '0'.<br>[4] RME: Read-Write margin enable control. This selects between the default Read-Write margin setting, and the external RM[3:0] Read-Write margin settting.<br>[7:5] WPULSE: Write Assist Pulse to control pulse width of negative voltage on SRAM bitline.<br>[9:8] RA: Read Assist control for WL under-drive.<br>[14:12] WA: Write assist enable control (Active High).<br>- WA[2:0] Write Assist pins to control negative voltage on SRAM bitline.<br>Recommended default value for LP: WA=4, RA=0, WPULSE=0, RME=1, RM=3 (RAM_TRIM_DEFAULT=0x0000_4013, RAM_TRIM_WIDTH=15)<br>Recommended default value for ULP: WA=6, RA=0, WPULSE=0, RME=1, RM=2 (RAM_TRIM_DEFAULT=0x0000_6012, RAM_TRIM_WIDTH=15) |

### 5.1.61 CPUSS_TRIM_RAM200_CTL

**Description:** RAM trim control for 100MHz - 200MHz SRAMs
**Address:** 0x40202108
**Offset:** 0x2108
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** See TRIM_RAM_CTL
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | TRIM [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | TRIM | RW | R | 98 | See TRIM_RAM_CTL for description.<br>System SRAM memories (SRAM0,1,2) are connected to this register.<br><br>System SRAM0 uses bias control power switch,so bits [7:5] of this register controls the bias pins of the SRAM0 power switch. |

### 5.1.62 CPUSS_TRIM_RAM350_CTL

**Description:** RAM trim control for more than 200MHz SRAMs
**Address:** 0x4020210C
**Offset:** 0x210C
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** See TRIM_RAM_CTL
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | TRIM [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | TRIM | RW | R | 98 | See TRIM_RAM_CTL for description.<br>CM7 Cache and TCM memories are connected to this register.<br><br>All CM7 cache and TCM SRAM macros are controlled using bias control power switches, so bits [7:5] of this register controls the bias pins of the CM7 cache and TCM SRAM power switches. |

### 5.1.63 CPUSS_CM0_SYSTEM_INT_CTL

**Description:** CM0+ system interrupt control
**Address:** 0x40208000
**Offset:** 0x8000
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:3] | | | | | CM0_CPU_INT_IDX [2:0] | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | CPU_INT_VALID [31:31] | None [30:24] | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:2 | CM0_CPU_INT_IDX | RW | R | Undefined | CPU interrupt index (legal range [0, 7]). This field specifies to which CPU interrupt the system interrupt is mapped. E.g., if CPU_INT_IDX is '6', the system interrupt is mapped to CPU interrupt '6'.<br><br>Note: it is possible to map multiple system interrupts to the same CPU interrupt. It is advised to assign different priorities to the CPU interrupts and to assign system interrupts to CPU interrupts accordingly. |
| 31 | CPU_INT_VALID | RW | R | 0 | Interrupt enable:<br>'0': Disabled. The system interrupt will NOT be mapped to any CPU interrupt.<br>'1': Enabled. The system interrupt is mapped on CPU interrupt CPU_INT_IDX.<br><br>Note: the CPUs have dedicated XXX_SYSTEM_INT_CTL registers. In other words, the CPUs can use different CPU interrupts for the same system interrupt. However, typically only one of the CPUs will have the ENABLED field of a specific system interrupt set to '1'. |

### 5.1.64 CPUSS_CM7_0_SYSTEM_INT_CTL

**Description:** CM7 0 system interrupt control
**Address:** 0x4020A000
**Offset:** 0xA000
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Only present when SYSTEM_IRQ_PRESENT is '1'
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:4] | | | | CPU_INT_IDX [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | CPU_INT_VALID [31:31] | None [30:24] | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | CPU_INT_IDX | RW | R | Undefined | CPU interrupt index (legal range [0, 15]). This field specifies to which CPU interrupt the system interrupt is mapped. E.g., if CPU_INT_IDX is '6', the system interrupt is mapped to CPU interrupt '6'.<br><br>Note: it is possible to map multiple system interrupts to the same CPU interrupt. It is advised to assign different priorities to the CPU interrupts and to assign system interrupts to CPU interrupts accordingly. |
| 31 | CPU_INT_VALID | RW | R | 0 | Interrupt enable:<br>'0': Disabled. The system interrupt will NOT be mapped to any CPU interrupt.<br>'1': Enabled. The system interrupt is mapped on CPU interrupt CPU_INT_IDX.<br><br>Note: the CPUs have dedicated XXX_SYSTEM_INT_CTL registers. In other words, the CPUs can use different CPU interrupts for the same system interrupt. However, typically only one of the CPUs will have the ENABLED field of a specific system interrupt set to '1'. |

### 5.1.65 CPUSS_CM7_1_SYSTEM_INT_CTL

**Description:** CM7 1 system interrupt control
**Address:** 0x4020C000
**Offset:** 0xC000
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Only present when SYSTEM_IRQ_PRESENT is '1' and CM7_1_PRESENT is '1'
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:4] | | | | CPU_INT_IDX [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | CPU_INT_VALID [31:31] | None [30:24] | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | CPU_INT_IDX | RW | R | Undefined | Refer CM7_0_SYSTEM_INT_CTL description. |
| 31 | CPU_INT_VALID | RW | R | 0 | Refer CM7_0_SYSTEM_INT_CTL description. |

# 6 CRYPTO

**Description** Cryptography component
**Base Address** 0x40100000
**Size** 0x10000
**Slave Num** MMIO1 - 0

# 7 DMAC

**Description** DMAC
**Base Address** 0x402A0000
**Size** 0x10000
**Slave Num** MMIO2 - 9

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DMAC_CTL | 0x402A0000 | FULL | Control |
| DMAC_ACTIVE | 0x402A0008 | FULL | Active channels |

## 7.1 CH 0

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DMAC_CH0_CTL | 0x402A1000 | FULL | Channel control |
| DMAC_CH0_IDX | 0x402A1010 | FULL | Channel current indices |
| DMAC_CH0_SRC | 0x402A1014 | FULL | Channel current source address |
| DMAC_CH0_DST | 0x402A1018 | FULL | Channel current destination address |
| DMAC_CH0_CURR | 0x402A1020 | FULL | Channel current descriptor pointer |
| DMAC_CH0_TR_CMD | 0x402A1028 | FULL | Channle software trigger |
| DMAC_CH0_DESCR_STATUS | 0x402A1040 | FULL | Channel descriptor status |
| DMAC_CH0_DESCR_CTL | 0x402A1060 | FULL | Channel descriptor control |
| DMAC_CH0_DESCR_SRC | 0x402A1064 | FULL | Channel descriptor source |
| DMAC_CH0_DESCR_DST | 0x402A1068 | FULL | Channel descriptor destination |
| DMAC_CH0_DESCR_X_SIZE | 0x402A106C | FULL | Channel descriptor X size |
| DMAC_CH0_DESCR_X_INCR | 0x402A1070 | FULL | Channel descriptor X increment |
| DMAC_CH0_DESCR_Y_SIZE | 0x402A1074 | FULL | Channel descriptor Y size |
| DMAC_CH0_DESCR_Y_INCR | 0x402A1078 | FULL | Channel descriptor Y increment |
| DMAC_CH0_DESCR_NEXT | 0x402A107C | FULL | Channel descriptor next pointer |
| DMAC_CH0_INTR | 0x402A1080 | FULL | Interrupt |
| DMAC_CH0_INTR_SET | 0x402A1084 | FULL | Interrupt set |
| DMAC_CH0_INTR_MASK | 0x402A1088 | FULL | Interrupt mask |
| DMAC_CH0_INTR_MASKED | 0x402A108C | FULL | Interrupt masked |

## 7.2 CH 1

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DMAC_CH1_CTL | 0x402A1100 | FULL | Channel control |
| DMAC_CH1_IDX | 0x402A1110 | FULL | Channel current indices |
| DMAC_CH1_SRC | 0x402A1114 | FULL | Channel current source address |
| DMAC_CH1_DST | 0x402A1118 | FULL | Channel current destination address |
| DMAC_CH1_CURR | 0x402A1120 | FULL | Channel current descriptor pointer |
| DMAC_CH1_TR_CMD | 0x402A1128 | FULL | Channle software trigger |
| DMAC_CH1_DESCR_STATUS | 0x402A1140 | FULL | Channel descriptor status |
| DMAC_CH1_DESCR_CTL | 0x402A1160 | FULL | Channel descriptor control |
| DMAC_CH1_DESCR_SRC | 0x402A1164 | FULL | Channel descriptor source |
| DMAC_CH1_DESCR_DST | 0x402A1168 | FULL | Channel descriptor destination |
| DMAC_CH1_DESCR_X_SIZE | 0x402A116C | FULL | Channel descriptor X size |
| DMAC_CH1_DESCR_X_INCR | 0x402A1170 | FULL | Channel descriptor X increment |
| DMAC_CH1_DESCR_Y_SIZE | 0x402A1174 | FULL | Channel descriptor Y size |
| DMAC_CH1_DESCR_Y_INCR | 0x402A1178 | FULL | Channel descriptor Y increment |
| DMAC_CH1_DESCR_NEXT | 0x402A117C | FULL | Channel descriptor next pointer |
| DMAC_CH1_INTR | 0x402A1180 | FULL | Interrupt |
| DMAC_CH1_INTR_SET | 0x402A1184 | FULL | Interrupt set |
| DMAC_CH1_INTR_MASK | 0x402A1188 | FULL | Interrupt mask |
| DMAC_CH1_INTR_MASKED | 0x402A118C | FULL | Interrupt masked |

## 7.3 CH 2

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DMAC_CH2_CTL | 0x402A1200 | FULL | Channel control |
| DMAC_CH2_IDX | 0x402A1210 | FULL | Channel current indices |
| DMAC_CH2_SRC | 0x402A1214 | FULL | Channel current source address |
| DMAC_CH2_DST | 0x402A1218 | FULL | Channel current destination address |
| DMAC_CH2_CURR | 0x402A1220 | FULL | Channel current descriptor pointer |
| DMAC_CH2_TR_CMD | 0x402A1228 | FULL | Channle software trigger |
| DMAC_CH2_DESCR_STATUS | 0x402A1240 | FULL | Channel descriptor status |
| DMAC_CH2_DESCR_CTL | 0x402A1260 | FULL | Channel descriptor control |
| DMAC_CH2_DESCR_SRC | 0x402A1264 | FULL | Channel descriptor source |
| DMAC_CH2_DESCR_DST | 0x402A1268 | FULL | Channel descriptor destination |
| DMAC_CH2_DESCR_X_SIZE | 0x402A126C | FULL | Channel descriptor X size |
| DMAC_CH2_DESCR_X_INCR | 0x402A1270 | FULL | Channel descriptor X increment |
| DMAC_CH2_DESCR_Y_SIZE | 0x402A1274 | FULL | Channel descriptor Y size |
| DMAC_CH2_DESCR_Y_INCR | 0x402A1278 | FULL | Channel descriptor Y increment |
| DMAC_CH2_DESCR_NEXT | 0x402A127C | FULL | Channel descriptor next pointer |
| DMAC_CH2_INTR | 0x402A1280 | FULL | Interrupt |
| DMAC_CH2_INTR_SET | 0x402A1284 | FULL | Interrupt set |
| DMAC_CH2_INTR_MASK | 0x402A1288 | FULL | Interrupt mask |
| DMAC_CH2_INTR_MASKED | 0x402A128C | FULL | Interrupt masked |

## 7.4 CH 3

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DMAC_CH3_CTL | 0x402A1300 | FULL | Channel control |
| DMAC_CH3_IDX | 0x402A1310 | FULL | Channel current indices |
| DMAC_CH3_SRC | 0x402A1314 | FULL | Channel current source address |
| DMAC_CH3_DST | 0x402A1318 | FULL | Channel current destination address |
| DMAC_CH3_CURR | 0x402A1320 | FULL | Channel current descriptor pointer |
| DMAC_CH3_TR_CMD | 0x402A1328 | FULL | Channle software trigger |
| DMAC_CH3_DESCR_STATUS | 0x402A1340 | FULL | Channel descriptor status |
| DMAC_CH3_DESCR_CTL | 0x402A1360 | FULL | Channel descriptor control |
| DMAC_CH3_DESCR_SRC | 0x402A1364 | FULL | Channel descriptor source |
| DMAC_CH3_DESCR_DST | 0x402A1368 | FULL | Channel descriptor destination |
| DMAC_CH3_DESCR_X_SIZE | 0x402A136C | FULL | Channel descriptor X size |
| DMAC_CH3_DESCR_X_INCR | 0x402A1370 | FULL | Channel descriptor X increment |
| DMAC_CH3_DESCR_Y_SIZE | 0x402A1374 | FULL | Channel descriptor Y size |
| DMAC_CH3_DESCR_Y_INCR | 0x402A1378 | FULL | Channel descriptor Y increment |
| DMAC_CH3_DESCR_NEXT | 0x402A137C | FULL | Channel descriptor next pointer |
| DMAC_CH3_INTR | 0x402A1380 | FULL | Interrupt |
| DMAC_CH3_INTR_SET | 0x402A1384 | FULL | Interrupt set |
| DMAC_CH3_INTR_MASK | 0x402A1388 | FULL | Interrupt mask |
| DMAC_CH3_INTR_MASKED | 0x402A138C | FULL | Interrupt masked |

## 7.5 CH 4

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DMAC_CH4_CTL | 0x402A1400 | FULL | Channel control |
| DMAC_CH4_IDX | 0x402A1410 | FULL | Channel current indices |
| DMAC_CH4_SRC | 0x402A1414 | FULL | Channel current source address |
| DMAC_CH4_DST | 0x402A1418 | FULL | Channel current destination address |
| DMAC_CH4_CURR | 0x402A1420 | FULL | Channel current descriptor pointer |
| DMAC_CH4_TR_CMD | 0x402A1428 | FULL | Channle software trigger |
| DMAC_CH4_DESCR_STATUS | 0x402A1440 | FULL | Channel descriptor status |
| DMAC_CH4_DESCR_CTL | 0x402A1460 | FULL | Channel descriptor control |
| DMAC_CH4_DESCR_SRC | 0x402A1464 | FULL | Channel descriptor source |
| DMAC_CH4_DESCR_DST | 0x402A1468 | FULL | Channel descriptor destination |
| DMAC_CH4_DESCR_X_SIZE | 0x402A146C | FULL | Channel descriptor X size |
| DMAC_CH4_DESCR_X_INCR | 0x402A1470 | FULL | Channel descriptor X increment |
| DMAC_CH4_DESCR_Y_SIZE | 0x402A1474 | FULL | Channel descriptor Y size |
| DMAC_CH4_DESCR_Y_INCR | 0x402A1478 | FULL | Channel descriptor Y increment |
| DMAC_CH4_DESCR_NEXT | 0x402A147C | FULL | Channel descriptor next pointer |
| DMAC_CH4_INTR | 0x402A1480 | FULL | Interrupt |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DMAC_CH4_INTR_SET | 0x402A1484 | FULL | Interrupt set |
| DMAC_CH4_INTR_MASK | 0x402A1488 | FULL | Interrupt mask |
| DMAC_CH4_INTR_MASKED | 0x402A148C | FULL | Interrupt masked |

## 7.6 CH 5

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DMAC_CH5_CTL | 0x402A1500 | FULL | Channel control |
| DMAC_CH5_IDX | 0x402A1510 | FULL | Channel current indices |
| DMAC_CH5_SRC | 0x402A1514 | FULL | Channel current source address |
| DMAC_CH5_DST | 0x402A1518 | FULL | Channel current destination address |
| DMAC_CH5_CURR | 0x402A1520 | FULL | Channel current descriptor pointer |
| DMAC_CH5_TR_CMD | 0x402A1528 | FULL | Channle software trigger |
| DMAC_CH5_DESCR_STATUS | 0x402A1540 | FULL | Channel descriptor status |
| DMAC_CH5_DESCR_CTL | 0x402A1560 | FULL | Channel descriptor control |
| DMAC_CH5_DESCR_SRC | 0x402A1564 | FULL | Channel descriptor source |
| DMAC_CH5_DESCR_DST | 0x402A1568 | FULL | Channel descriptor destination |
| DMAC_CH5_DESCR_X_SIZE | 0x402A156C | FULL | Channel descriptor X size |
| DMAC_CH5_DESCR_X_INCR | 0x402A1570 | FULL | Channel descriptor X increment |
| DMAC_CH5_DESCR_Y_SIZE | 0x402A1574 | FULL | Channel descriptor Y size |
| DMAC_CH5_DESCR_Y_INCR | 0x402A1578 | FULL | Channel descriptor Y increment |
| DMAC_CH5_DESCR_NEXT | 0x402A157C | FULL | Channel descriptor next pointer |
| DMAC_CH5_INTR | 0x402A1580 | FULL | Interrupt |
| DMAC_CH5_INTR_SET | 0x402A1584 | FULL | Interrupt set |
| DMAC_CH5_INTR_MASK | 0x402A1588 | FULL | Interrupt mask |
| DMAC_CH5_INTR_MASKED | 0x402A158C | FULL | Interrupt masked |

## 7.7 CH 6

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DMAC_CH6_CTL | 0x402A1600 | FULL | Channel control |
| DMAC_CH6_IDX | 0x402A1610 | FULL | Channel current indices |
| DMAC_CH6_SRC | 0x402A1614 | FULL | Channel current source address |
| DMAC_CH6_DST | 0x402A1618 | FULL | Channel current destination address |
| DMAC_CH6_CURR | 0x402A1620 | FULL | Channel current descriptor pointer |
| DMAC_CH6_TR_CMD | 0x402A1628 | FULL | Channle software trigger |
| DMAC_CH6_DESCR_STATUS | 0x402A1640 | FULL | Channel descriptor status |
| DMAC_CH6_DESCR_CTL | 0x402A1660 | FULL | Channel descriptor control |
| DMAC_CH6_DESCR_SRC | 0x402A1664 | FULL | Channel descriptor source |
| DMAC_CH6_DESCR_DST | 0x402A1668 | FULL | Channel descriptor destination |
| DMAC_CH6_DESCR_X_SIZE | 0x402A166C | FULL | Channel descriptor X size |
| DMAC_CH6_DESCR_X_INCR | 0x402A1670 | FULL | Channel descriptor X increment |
| DMAC_CH6_DESCR_Y_SIZE | 0x402A1674 | FULL | Channel descriptor Y size |
| DMAC_CH6_DESCR_Y_INCR | 0x402A1678 | FULL | Channel descriptor Y increment |
| DMAC_CH6_DESCR_NEXT | 0x402A167C | FULL | Channel descriptor next pointer |
| DMAC_CH6_INTR | 0x402A1680 | FULL | Interrupt |
| DMAC_CH6_INTR_SET | 0x402A1684 | FULL | Interrupt set |
| DMAC_CH6_INTR_MASK | 0x402A1688 | FULL | Interrupt mask |
| DMAC_CH6_INTR_MASKED | 0x402A168C | FULL | Interrupt masked |

## 7.8 CH 7

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DMAC_CH7_CTL | 0x402A1700 | FULL | Channel control |
| DMAC_CH7_IDX | 0x402A1710 | FULL | Channel current indices |
| DMAC_CH7_SRC | 0x402A1714 | FULL | Channel current source address |
| DMAC_CH7_DST | 0x402A1718 | FULL | Channel current destination address |
| DMAC_CH7_CURR | 0x402A1720 | FULL | Channel current descriptor pointer |
| DMAC_CH7_TR_CMD | 0x402A1728 | FULL | Channle software trigger |
| DMAC_CH7_DESCR_STATUS | 0x402A1740 | FULL | Channel descriptor status |
| DMAC_CH7_DESCR_CTL | 0x402A1760 | FULL | Channel descriptor control |
| DMAC_CH7_DESCR_SRC | 0x402A1764 | FULL | Channel descriptor source |
| DMAC_CH7_DESCR_DST | 0x402A1768 | FULL | Channel descriptor destination |
| DMAC_CH7_DESCR_X_SIZE | 0x402A176C | FULL | Channel descriptor X size |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DMAC_CH7_DESCR_X_INCR | 0x402A1770 | FULL | Channel descriptor X increment |
| DMAC_CH7_DESCR_Y_SIZE | 0x402A1774 | FULL | Channel descriptor Y size |
| DMAC_CH7_DESCR_Y_INCR | 0x402A1778 | FULL | Channel descriptor Y increment |
| DMAC_CH7_DESCR_NEXT | 0x402A177C | FULL | Channel descriptor next pointer |
| DMAC_CH7_INTR | 0x402A1780 | FULL | Interrupt |
| DMAC_CH7_INTR_SET | 0x402A1784 | FULL | Interrupt set |
| DMAC_CH7_INTR_MASK | 0x402A1788 | FULL | Interrupt mask |
| DMAC_CH7_INTR_MASKED | 0x402A178C | FULL | Interrupt masked |

## 7.9 Register Details

### 7.9.1 DMAC_CTL

**Description:** Control
**Address:** 0x402A0000
**Offset:** 0x0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | ENABLED [31:31] | None [30:24] | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 31 | ENABLED | RW | R | 0 | IP enable:<br>'0': Disabled. All non-retention registers (command and status registers) are reset to their default value when the IP is disabled. All retention registers retain their value when the IP is disabled.<br>'1': Enabled. |
| | DISABLED | | | 0 | N/A |
| | ENABLED | | | 1 | N/A |

### 7.9.2 DMAC_ACTIVE

**Description:** Active channels
**Address:** 0x402A0008
**Offset:** 0x8
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | ACTIVE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | ACTIVE | R | W | 0 | Specifies active channels; i.e. enabled channels whose trigger got activated. |

### 7.9.3 CH

#### 7.9.3.1 DMAC_CH_CTL

**Description:** Channel control
**Address:** 0x402A1000
**Offset:** 0x0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x2

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | PC [7:4] | | | | None [3:3] | B [2:2] | NS [1:1] | P [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:10] | | | | | | PRIO [9:8] | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | ENABLED [31:31] | None [30:24] | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | P | RW | R | 0 | User/privileged access control:<br>'0': user mode.<br>'1': privileged mode.<br><br>This field is set with the user/privileged access control of the transaction that writes this register; i.e. the access control is inherited from the write transaction and not specified by the transaction write data.<br><br>All transactions for this channel use the P field for the user/privileged access control. |
| 1 | NS | RW | R | 1 | Secure/on-secure access control:<br>'0': secure.<br>'1': non-secure.<br><br>This field is set with the secure/non-secure access control of the transaction that writes this register; i.e. the access control is inherited from the write transaction and not specified by the transaction write data.<br><br>All transactions for this channel use the NS field for the secure/non-secure access control. |
| 2 | B | RW | R | 0 | Non-bufferable/bufferable access control:<br>'0': non-bufferable.<br>'1': bufferable.<br><br>This field is used to indicate to an AMBA bridge that a write transaction can complete without waiting for the destination to accept the write transaction data.<br><br>All transactions for this channel uses the B field for the non-bufferable/bufferable access control. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 4:7 | PC | RW | R | 0 | Protection context.<br><br>This field is set with the protection context of the transaction that writes this register; i.e. the context is inherited from the write transaction and not specified by the transaction write data.<br><br>All transactions for this channel uses the PC field for the protection context. |
| 8:9 | PRIO | RW | R | 0 | Channel priority:<br>'0': highest priority.<br>'1'<br>'2'<br>'3': lowest priority.<br><br>Channels with the same priority constitute a priority group and within this priority group, the following 'roundrobin' arbitration is applied.<br>A 'round' consists of a contiguous sequence of channel activations, within this priority group, without any repetition. Within a round, higher priority is given to the lower channel indices. The notion of a round guarantees that within a group, higher channel indices do not yield to lower indices indefinitely. |
| 31 | ENABLED | RW | RW1C | 0 | Channel enable:<br>'0': Disabled. The channel's trigger is ignored and the channel cannot be made pending and therefore cannot be made active. If a pending channel is disabled, the channel is made non pending. If the activate channel is disabled, the channel is de-activated (bus transactions are completed).<br>'1': Enabled.<br><br>SW sets this field to '1' to enable a specific channel.<br><br>HW sets this field to '0' when an error interrupt cause is activated. |

### 7.9.3.2 DMAC_CH_IDX

**Description:** Channel current indices
**Address:** 0x402A1010
**Offset:** 0x10
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** Undefined as one or more bit fields have a default value that is undefined

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | X [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | X [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | Y [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | Y [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | X | R | W | Undefined | Specifies the X loop index. In the range of [0, X_COUNT], with X_COUNT taken from the current descriptor.<br><br>Note: HW sets this field to '0' when it loads a descriptor. |
| 16:31 | Y | R | W | Undefined | Specifies the Y loop index, with Y_COUNT taken from the current descriptor.<br><br>Note: HW sets this field to '0' when it loads a descriptor.. |

### 7.9.3.3 DMAC_CH_SRC

**Description:** Channel current source address
**Address:** 0x402A1014
**Offset:** 0x14
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** Undefined as one or more bit fields have a default value that is undefined

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDR [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDR [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDR [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDR [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | ADDR | R | W | Undefined | Current address of source location. |

### 7.9.3.4 DMAC_CH_DST

**Description:** Channel current destination address
**Address:** 0x402A1018
**Offset:** 0x18
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** Undefined as one or more bit fields have a default value that is undefined

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDR [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDR [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDR [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDR [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | ADDR | R | W | Undefined | Current address of destination location. |

### 7.9.3.5 DMAC_CH_CURR

**Description:** Channel current descriptor pointer
**Address:** 0x402A1020
**Offset:** 0x20
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** Undefined as one or more bit fields have a default value that is undefined

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | PTR [7:2] | | | | | | None [1:0] | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | PTR [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | PTR [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | PTR [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 2:31 | PTR | RW | RW | Undefined | Address of current descriptor. When this field is '0', there is no valid descriptor.<br><br>Note: HW updates the current descriptor pointer CH_CURR_PTR with DESCR_NEXT_PTR after execution of the current descriptor. |

### 7.9.3.6 DMAC_CH_TR_CMD

**Description:** Channle software trigger
**Address:** 0x402A1028
**Offset:** 0x28
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:1] | | | | | | | ACTIVATE [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | ACTIVATE | RW1S | A | 0 | Software trigger. When written with '1', a trigger is generated which sets 'trigger pending' (only if the channel is enabled). A read always returns a 0. |

### 7.9.3.7 DMAC_CH_DESCR_STATUS

**Description:** Channel descriptor status
**Address:** 0x402A1040
**Offset:** 0x40
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALID [31:31] | None [30:24] | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 31 | VALID | R | W | 0 | Indicates whether the descriptor information present in DESCR_CTL, DESCR_SRC, DESCR_DST, DESCR_X_SIZE, DESCR_X_INCR, DESCR_Y_SIZE, DESCR_Y_INCR, DESCR_NEXT status registers is valid or not. |

### 7.9.3.8 DMAC_CH_DESCR_CTL

**Description:** Channel descriptor control
**Address:** 0x402A1060
**Offset:** 0x60
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** Copy of DESCR_CTL of the currently active descriptor.
**Default:** Undefined as one or more bit fields have a default value that is undefined

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | TR_IN_TYPE [7:6] | | TR_OUT_TYPE [5:4] | | INTR_TYPE [3:2] | | WAIT_FOR_DEACT [1:0] | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:9] | | | | | | | DATA_PREFETCH [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:18] | | | | | | DATA_SIZE [17:16] | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:31] | DESCR_TYPE [30:28] | | | DST_TRANSFER_SIZE [27:27] | SRC_TRANSFER_SIZE [26:26] | None [25:25] | CH_DISABLE [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:1 | WAIT_FOR_DEACT | R | W | Undefined | Specifies whether the controller should wait for the input trigger to be deactivated; i.e. the selected system trigger is not active. This field is used to synchronize the controller with the agent that generated the trigger. This field is ONLY used at the completion of the transfer as specified by TR_IN. E.g., a TX FIFO indicates that it is empty and it needs a new data sample. The agent removes the trigger ONLY when the data sample has been written by the controller AND received by the agent. Furthermore, the agent's trigger may be delayed by a few cycles before it reaches the controller. This field is used for level sensitive trigger, which reflect state (pulse sensitive triggers should have this field set to '0'). The wait cycles incurred by this field reduce DW controller performance.<br>'0': Do not wait for trigger de-activation (for pulse sensitive triggers).<br>'1': Wait for up to 4 cycles.<br>'2': Wait for up to 16 cycles.<br>'3': Wait indefinitely. This option may result in controller lockup if the trigger is not de-activated. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 2:3 | INTR_TYPE | R | W | Undefined | Specifies when a completion interrupt is generated (CH_STATUS.INTR_CAUSE is set to COMPLETION):<br>'0': An interrupt is generated after a single transfer.<br>'1': An interrupt is generated after a single 1D transfer or a memory copy transfer<br>- If the descriptor type is 'single', the interrupt is generated after a single transfer.<br>- If the descriptor type is '1D' or '2D', the interrupt is generated after the execution of a 1D transfer.<br>- If the descriptor type is 'memory copy', the interrupt is generated after the execution of a memory copy transfer.<br>- If the descriptor type is 'scatter' the interrupt is generated after the execution of a scatter transfer.<br>'2': An interrupt is generated after the execution of the current descriptor (independent of the value of DESCR_NEXT_PTR.ADDR of the current descriptor).<br>'3': An interrupt is generated after the execution of the current descriptor and the current descriptor's DESCR_NEXT_PTR.ADDR is '0'. |
| 4:5 | TR_OUT_TYPE | R | W | Undefined | Specifies when an output trigger is generated:<br>'0': An output trigger is generated after a single transfer.<br>'1': An output trigger is generated after a single 1D transfer or a memory copy transfer.<br>- If the descriptor type is 'single', the output trigger is generated after a single transfer.<br>- If the descriptor type is '1D' or '2D', the output trigger is generated after the execution of a 1D transfer.<br>- If the descriptor type is 'memory copy', the output trigger is generated after the execution of a memory copy transfer.<br>- If the descriptor type is 'scatter', the output trigger is generated after the execution of a scatter transfer.<br>'2': An output trigger is generated after the execution of the current descriptor.<br>'3': An output trigger is generated after the execution of a descriptor list: after the execution of the current descriptor AND the current descriptor's DESCR_NEXT_PTR.ADDR is '0'. |
| 6:7 | TR_IN_TYPE | R | W | Undefined | Specifies the input trigger type (not to be confused with the descriptor type):<br>'0': A trigger results in the execution of a single transfer. The descriptor type can be single, 1D or 2D.<br>'1': A trigger results in the execution of a single 1D transfer.<br>- If the descriptor type is 'single', the trigger results in the execution of a single transfer.<br>- If the descriptor type is '1D' or '2D', the trigger results in the execution of a 1D transfer.<br>- If the descriptor type is 'memory copy', the trigger results in the execution of a memory copy transfer.<br>- If the descriptor type is 'scatter', the trigger results in the execution of an scatter transfer.<br>'2': A trigger results in the execution of the current descriptor.<br>'3': A trigger results in the execution of the current descriptor and continues (without requiring another input trigger) with the execution of the next descriptor using the next descriptor's information. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 8 | DATA_PREFETCH | R | W | Undefined | Source data prefetch:<br>'0': No source data prefetch. Source data transfers are only initiated AFTER the input trigger is activated.<br>'1': Source data prefetch. Source data transfers are initiated as soon as the channel is enabled, the current descriptor pointer is NOT '0' and there is space available in the channel's data FIFO. When the input trigger is activated, the trigger can initiate destination data transfers with data that is already in the channel's data FIFO. This effectively shortens the initial delay of the data transfer.<br><br>Note: data prefetch should be used with care, to ensure that data coherency is guaranteed and that prefetches do not cause undesired side effects. |
| 16:17 | DATA_SIZE | R | W | Undefined | Specifies the data element size:<br>'0': Byte (8 bits).<br>'1': Halfword (16 bits).<br>'2': Word (32 bits).<br>DATA_SIZE, SRC_TRANSFER_SIZE and DST_TRANSFER_SIZE together determine how data elements are transferred. The following are the 9 legal settings:<br>- DATA is 8 bit, SRC is 8 bit, DST is 8 bit.<br>- DATA is 8 bit, SRC is 32 bit (higher 24 bits are dropped), DST is 8 bit.<br>- DATA is 8 bit, SRC is 8 bit, DST is 32 bit (higher 24 bits are made '0').<br>- DATA is 8 bit, SRC is 32 bit (higher 24 bits are dropped), DST is 32 bit (higher 24 bits are made '0').<br>- DATA is 16 bit, SRC is 16 bit, DST is 16 bit.<br>- DATA is 16 bit, SRC is 32 bit (higher 16 bits are dropped), DST is 16 bit.<br>- DATA is 16 bit, SRC is 16 bit, DST is 32 bit (higher 16 bits are made '0').<br>- DATA is 16 bit, SRC is 32 bit (higher 16 bits are dropped), DST is 32 bit (higher 16 bits are made '0').<br>- DATA is 32 bit, SRC is 32 bit, DST is 32 bit.<br><br>Note: this field is not used for a 'memory copy' descriptor type. Note: this field must be set to '2' for a 'initialization' descriptor type. |
| 24 | CH_DISABLE | R | W | Undefined | Specifies whether the channel is disabled or not after completion of the current descriptor (independent of the value of the DESCR_NEXT_PTR value):<br>'0': Channel is not disabled.<br>'1': Channel is disabled. |
| 26 | SRC_TRANSFER_SIZE | R | W | Undefined | Specifies the bus transfer size to the source location:<br>'0': As specified by DATA_SIZE.<br>'1': Word (32 bits).<br>Distinguishing bus transfer size from data element size allows for source components with data elements that are smaller than their 32-bit bus interface width. E.g., an ADC source has a 32-bit bus transfer size, but only provides a 16-bit data element.<br><br>Note: this field is not used for a 'memory copy' descriptor type. Note: this field must be set to '1' for a 'scatter' descriptor type. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 27 | DST_TRANSFER_SIZE | R | W | Undefined | Specifies the bus transfer size to the destination location:<br>'0': As specified by DATA_SIZE.<br>'1': Word (32 bits).<br>Distinguishing bus transfer size from data element size allows for destination components with data elements that are smaller than their 32-bit bus interface width. E.g., a DAC destination has a 32-bit bus transfer size, but only requires a 16-bit data element.<br><br>Note: this field is not used for a 'memory copy' descriptor type. Note: this field must be set to '1' for a 'scatter' descriptor type. |
| 28:30 | DESCR_TYPE | R | W | Undefined | Specifies the descriptor type (not to be confused with the trigger type):<br>'0': Single transfer.<br>The DESCR_X_SIZE, DESCR_X_INCR, DESCR_Y_SIZE and DESCR_Y_INCR registers are NOT present. The DESCR_NEXT_PTR is at offset 0x0c.<br>'1': 1D transfer.<br>The DESCR_X_SIZE and DESCR_X_INCR registers are present, the DESCR_Y_SIZE and DESCR_Y_INCR are NOT present. A 1D transfer consists out of DESCR_X_SIZE.X_COUNT+1 single transfers. The DESCR_NEXT_PTR is at offset 0x14.<br>'2': 2D transfer.<br>The DESCR_X_SIZE, DESCR_X_INCR, DESCR_Y_SIZE and DESCR_Y_INCR registers are present. A 2D transfer consists of (DESCR_X_SIZE.X_COUNT+1)*(DESCR_Y_SIZE.Y_COUNT+1) single transfers. The DESCR_NEXT_PTR is at offset 0x1c.<br>'3': Memory copy.<br>The DESCR_X_SIZE register is present, the DESCR_X_INCR, DESCR_Y_SIZE and DESCR_Y_INCR are NOT present. A memory copy transfer copies DESCR_X_SIZE.X_COUNT+1 Bytes and may use Byte, halfword and word transfers. The DESCR_NEXT_PTR is at offset 0x10.<br>'4': Scatter transfer. The DESCR_X_SIZE register is present, the DESCR_DST, DESCR_X_INCR, DESCR_Y_SIZE and DESCR_Y_INCR are NOT present.<br>'5'-'7': Undefined.<br><br>After the execution of the current descriptor, the DESCR_NEXT_PTR address is copied to the channel's CH_CURR_PTR address and CH_STATUS.X_IDX and CH_STATUS.Y_IDX are set to '0'. |

### 7.9.3.9 DMAC_CH_DESCR_SRC

**Description:** Channel descriptor source
**Address:** 0x402A1064
**Offset:** 0x64
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** Copy of DESCR_SRC of the currently active descriptor.
**Default:** Undefined as one or more bit fields have a default value that is undefined

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDR [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDR [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDR [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDR [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | ADDR | R | W | Undefined | Base address of source location. |

### 7.9.3.10 DMAC_CH_DESCR_DST

**Description:** Channel descriptor destination
**Address:** 0x402A1068
**Offset:** 0x68
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** Copy of DESCR_DST of the currently active descriptor.
**Default:** Undefined as one or more bit fields have a default value that is undefined

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDR [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDR [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDR [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDR [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | ADDR | R | W | Undefined | Base address of destination location. |

### 7.9.3.11 DMAC_CH_DESCR_X_SIZE

**Description:** Channel descriptor X size
**Address:** 0x402A106C
**Offset:** 0x6C
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** Copy of DESCR_X_SIZE of the currently active descriptor.
**Default:** Undefined as one or more bit fields have a default value that is undefined

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | X_COUNT [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | X_COUNT [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | X_COUNT | R | W | Undefined | Number of iterations (minus 1) of the 'X loop' (X_COUNT+1 is the number of single transfers in a 1D transfer). This field is an unsigned number in the range [0, 65535], representing 1 through 65536 iterations.<br><br>For the 'memory copy' descriptor type, (X_COUNT + 1) is the number of transferred Bytes. For the 'scatter' descriptor type, ceiling(X_COUNT/2) is the number of (address, write data) initialization pairs processed. |

### 7.9.3.12 DMAC_CH_DESCR_X_INCR

**Description:** Channel descriptor X increment
**Address:** 0x402A1070
**Offset:** 0x70
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** Copy of DESCR_X_INCR of the currently active descriptor.
**Default:** Undefined as one or more bit fields have a default value that is undefined

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | SRC_X [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | SRC_X [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | DST_X [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | DST_X [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | SRC_X | R | W | Undefined | Specifies increment of source address for each X loop iteration (in multiples of SRC_TRANSFER_SIZE). This field is a signed number (sign-magnitude format) in the range [-32768, 32767]. If this field is '0', the source address is not incremented. This is useful for reading from RX FIFO structures. |
| 16:31 | DST_X | R | W | Undefined | Specifies increment of destination address for each X loop iteration (in multiples of DST_TRANSFER_SIZE). This field is a signed number (sign-magnitude format) in the range [-32768, 32767]. If this field is '0', the destination address is not incremented. This is useful for writing to TX FIFO structures. |

### 7.9.3.13 DMAC_CH_DESCR_Y_SIZE

**Description:** Channel descriptor Y size
**Address:** 0x402A1074
**Offset:** 0x74
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** Copy of DESCR_Y_SIZE of the currently active descriptor.
**Default:** Undefined as one or more bit fields have a default value that is undefined

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | Y_COUNT [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | Y_COUNT [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | Y_COUNT | R | W | Undefined | Number of iterations (minus 1) of the 'Y loop' (X_COUNT+1)*(Y_COUNT+1) is the number of single transfers in a 2D transfer). This field is an unsigned number in the range [0, 65535], representing 1 through 65536 iterations. |

### 7.9.3.14 DMAC_CH_DESCR_Y_INCR

**Description:** Channel descriptor Y increment
**Address:** 0x402A1078
**Offset:** 0x78
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** Copy of DESCR_Y_INCR of the currently active descriptor.
**Default:** Undefined as one or more bit fields have a default value that is undefined

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | SRC_Y [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | SRC_Y [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | DST_Y [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | DST_Y [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | SRC_Y | R | W | Undefined | Specifies increment of source address for each Y loop iteration (in multiples of SRC_TRANSFER_SIZE). This field is a signed number in the range [-32768, 32767]. |
| 16:31 | DST_Y | R | W | Undefined | Specifies increment of destination address for each Y loop iteration (in multiples of DST_TRANSFER_SIZE). This field is a signed number in the range [-32768, 32767]. |

### 7.9.3.15 DMAC_CH_DESCR_NEXT

**Description:** Channel descriptor next pointer
**Address:** 0x402A107C
**Offset:** 0x7C
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** Copy of DESCR_NEXT_PTR of the currently active descriptor. For a single transfer descriptor type, this register is at offset 0x0c. For a 1D transfer descriptor type, this register is at offset 0x14. For a 2D transfer descriptor type, this register is at offset 0x1c. For a memory copy transfer descriptor type, this register is at offset 0x10. For a scatter transfer descriptor type, this register is at offset 0x0c.
**Default:** Undefined as one or more bit fields have a default value that is undefined

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | PTR [7:2] | | | | | | None [1:0] | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | PTR [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | PTR [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | PTR [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 2:31 | PTR | R | W | Undefined | Address of next descriptor in descriptor list. When this field is '0', this is the last descriptor in the descriptor list. |

### 7.9.3.16 DMAC_CH_INTR

**Description:** Interrupt
**Address:** 0x402A1080
**Offset:** 0x80
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** The register fields are not retained. This is to ensure that they come up as '0' after coming out of DeepSleep system power mode.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DESCR_BUS_ERROR [7:7] | ACTIVE_CH_DISABLED [6:6] | CURR_PTR_NULL [5:5] | DST_MISAL [4:4] | SRC_MISAL [3:3] | DST_BUS_ERROR [2:2] | SRC_BUS_ERROR [1:1] | COMPLETION [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | COMPLETION | RW1C | RW1S | 0 | Activated (set to '1') on completion of data transfer(s) as specified by the descriptor's CH_DESCR_CTL.INTR_TYPE. |
| 1 | SRC_BUS_ERROR | RW1C | RW1S | 0 | Activated (set to '1') on a bus error for a load from the source. |
| 2 | DST_BUS_ERROR | RW1C | RW1S | 0 | Activated (set to '1') on a bus error for a store to the destination. |
| 3 | SRC_MISAL | RW1C | RW1S | 0 | Activated (set to '1') on a misalignment of the source address. |
| 4 | DST_MISAL | RW1C | RW1S | 0 | Activated (set to '1') on a misalignment of the destination address. |
| 5 | CURR_PTR_NULL | RW1C | RW1S | 0 | Activated (set to '1') when the channel is enabled (CH_CTL.ENABLED is '1') and CH_CURR_PTR is '0'. |
| 6 | ACTIVE_CH_DISABLED | RW1C | RW1S | 0 | Activated (set to '1') if the channel is disabled by SW (accidentally/incorrectly) when the data transfer engine is busy. |
| 7 | DESCR_BUS_ERROR | RW1C | RW1S | 0 | Activated (set to '1') on a bus error for a load of the descriptor. |

### 7.9.3.17 DMAC_CH_INTR_SET

**Description:** Interrupt set
**Address:** 0x402A1084
**Offset:** 0x84
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** When read, this register reflects the INTR register.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DESCR_BUS_ERROR [7:7] | ACTIVE_CH_DISABLED [6:6] | CURR_PTR_NULL [5:5] | DST_MISAL [4:4] | SRC_MISAL [3:3] | DST_BUS_ERROR [2:2] | SRC_BUS_ERROR [1:1] | COMPLETION [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | COMPLETION | RW1S | A | 0 | Write this field with '1' to set INTR.COMPLETION field to '1' (a write of '0' has no effect). |
| 1 | SRC_BUS_ERROR | RW1S | A | 0 | Write this field with '1' to set INTR.SRC_BUS_ERROR field to '1' (a write of '0' has no effect). |
| 2 | DST_BUS_ERROR | RW1S | A | 0 | Write this field with '1' to set INTR.DST_BUS_ERROR field to '1' (a write of '0' has no effect). |
| 3 | SRC_MISAL | RW1S | A | 0 | Write this field with '1' to set INTR.SRC_MISAL field to '1' (a write of '0' has no effect). |
| 4 | DST_MISAL | RW1S | A | 0 | Write this field with '1' to set INTR.DST_MISAL field to '1' (a write of '0' has no effect). |
| 5 | CURR_PTR_NULL | RW1S | A | 0 | Write this field with '1' to set INTR.CURR_PTR_NULL field to '1' (a write of '0' has no effect). |
| 6 | ACTIVE_CH_DISABLED | RW1S | A | 0 | Write this field with '1' to set INTR.ACT_CH_DISABLED field to '1' (a write of '0' has no effect). |
| 7 | DESCR_BUS_ERROR | RW1S | A | 0 | Write this field with '1' to set INTR.DESCR_BUS_ERROR field to '1' (a write of '0' has no effect). |

### 7.9.3.18 DMAC_CH_INTR_MASK

**Description:** Interrupt mask
**Address:** 0x402A1088
**Offset:** 0x88
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DESCR_BUS_ERROR [7:7] | ACTIVE_CH_DISABLED [6:6] | CURR_PTR_NULL [5:5] | DST_MISAL [4:4] | SRC_MISAL [3:3] | DST_BUS_ERROR [2:2] | SRC_BUS_ERROR [1:1] | COMPLETION [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | COMPLETION | RW | R | 0 | Mask for INTR.COMPLETION interrupt. |
| 1 | SRC_BUS_ERROR | RW | R | 0 | Mask for INTR.SRC_BUS_ERROR interrupt. |
| 2 | DST_BUS_ERROR | RW | R | 0 | Mask for INTR.DST_BUS_ERROR interrupt. |
| 3 | SRC_MISAL | RW | R | 0 | Mask for INTR.SRC_MISAL interrupt. |
| 4 | DST_MISAL | RW | R | 0 | Mask for INTR.DST_MISAL interrupt. |
| 5 | CURR_PTR_NULL | RW | R | 0 | Mask for INTR.CURR_PTR_NULL interrupt. |
| 6 | ACTIVE_CH_DISABLED | RW | R | 0 | Mask for INTR.ACTIVE_CH_DISABLED interrupt. |
| 7 | DESCR_BUS_ERROR | RW | R | 0 | Mask for INTR.DESCR_BUS_ERROR interrupt. |

### 7.9.3.19 DMAC_CH_INTR_MASKED

**Description:** Interrupt masked
**Address:** 0x402A108C
**Offset:** 0x8C
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** When read, this register reflects a bitwise AND between the INTR and INTR_MASK registers. This register allows SW to read the status of all mask enabled interrupt causes with a single load operation, rather than two load operations: one for INTR and one for INTR_MASK. This simplifies Firmware development. The associated interrupt is active ('1'), when INTR_MASKED != 0.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DESCR_BUS_ERROR [7:7] | ACTIVE_CH_DISABLED [6:6] | CURR_PTR_NULL [5:5] | DST_MISAL [4:4] | SRC_MISAL [3:3] | DST_BUS_ERROR [2:2] | SRC_BUS_ERROR [1:1] | COMPLETION [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | COMPLETION | R | W | 0 | Logical and of corresponding INTR.COMPLETION and INTR_MASK.COMPLETION fields. |
| 1 | SRC_BUS_ERROR | R | W | 0 | Logical and of corresponding INTR.SRC_BUS_ERROR and INTR_MASK.SRC_BUS_ERROR fields. |
| 2 | DST_BUS_ERROR | R | W | 0 | Logical and of corresponding INTR.DST_BUS_ERROR and INTR_MASK.DST_BUS_ERROR fields. |
| 3 | SRC_MISAL | R | W | 0 | Logical and of corresponding INTR.SRC_MISAL and INTR_MASK.SRC_MISAL fields. |
| 4 | DST_MISAL | R | W | 0 | Logical and of corresponding INTR.DST_MISAL and INTR_MASK.DST_MISAL fields. |
| 5 | CURR_PTR_NULL | R | W | 0 | Logical and of corresponding INTR.CURR_PTR_NULL and INTR_MASK.CURR_PTR_NULL fields. |
| 6 | ACTIVE_CH_DISABLED | R | W | 0 | Logical and of corresponding INTR.ACTIVE_CH_DISABLED and INTR_MASK.ACTIVE_CH_DISABLED fields. |
| 7 | DESCR_BUS_ERROR | R | W | 0 | Logical and of corresponding INTR.DESCR_BUS_ERROR and INTR_MASK.DESCR_BUS_ERROR fields. |

# 8 DW

## 8.1 DW 0

**Description** Datawire Controller
**Base Address** 0x40280000
**Size** 0x10000
**Slave Num** MMIO2 - 7

### 8.1.1 0

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CTL0 | 0x40280000 | FULL | Control |
| DW0_STATUS0 | 0x40280004 | FULL | Status |
| DW0_ACT_DESCR_CTL0 | 0x40280020 | FULL | Active descriptor control |
| DW0_ACT_DESCR_SRC0 | 0x40280024 | FULL | Active descriptor source |
| DW0_ACT_DESCR_DST0 | 0x40280028 | FULL | Active descriptor destination |
| DW0_ACT_DESCR_X_CTL0 | 0x40280030 | FULL | Active descriptor X loop control |
| DW0_ACT_DESCR_Y_CTL0 | 0x40280034 | FULL | Active descriptor Y loop control |
| DW0_ACT_DESCR_NEXT_PTR0 | 0x40280038 | FULL | Active descriptor next pointer |
| DW0_ACT_SRC0 | 0x40280040 | FULL | Active source |
| DW0_ACT_DST0 | 0x40280044 | FULL | Active destination |
| DW0_ECC_CTL0 | 0x40280080 | FULL | ECC control |
| DW0_CRC_CTL0 | 0x40280100 | FULL | CRC control |
| DW0_CRC_DATA_CTL0 | 0x40280110 | FULL | CRC data control |
| DW0_CRC_POL_CTL0 | 0x40280120 | FULL | CRC polynomial control |
| DW0_CRC_LFSR_CTL0 | 0x40280130 | FULL | CRC LFSR control |
| DW0_CRC_REM_CTL0 | 0x40280140 | FULL | CRC remainder control |
| DW0_CRC_REM_RESULT0 | 0x40280148 | FULL | CRC remainder result |

#### 8.1.1.1 CH_STRUCT 0

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT0_CH_CTL | 0x40288000 | FULL | Channel control |
| DW0_CH_STRUCT0_CH_STATUS | 0x40288004 | FULL | Channel status |
| DW0_CH_STRUCT0_CH_IDX | 0x40288008 | FULL | Channel current indices |
| DW0_CH_STRUCT0_CH_CURR_PTR | 0x4028800C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT0_INTR | 0x40288010 | FULL | Interrupt |
| DW0_CH_STRUCT0_INTR_SET | 0x40288014 | FULL | Interrupt set |
| DW0_CH_STRUCT0_INTR_MASK | 0x40288018 | FULL | Interrupt mask |
| DW0_CH_STRUCT0_INTR_MASKED | 0x4028801C | FULL | Interrupt masked |
| DW0_CH_STRUCT0_SRAM_DATA0 | 0x40288020 | FULL | SRAM data 0 |
| DW0_CH_STRUCT0_SRAM_DATA1 | 0x40288024 | FULL | SRAM data 1 |
| DW0_CH_STRUCT0_TR_CMD | 0x40288028 | FULL | Channel software trigger |

#### 8.1.1.2 CH_STRUCT 1

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT1_CH_CTL | 0x40288040 | FULL | Channel control |
| DW0_CH_STRUCT1_CH_STATUS | 0x40288044 | FULL | Channel status |
| DW0_CH_STRUCT1_CH_IDX | 0x40288048 | FULL | Channel current indices |
| DW0_CH_STRUCT1_CH_CURR_PTR | 0x4028804C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT1_INTR | 0x40288050 | FULL | Interrupt |
| DW0_CH_STRUCT1_INTR_SET | 0x40288054 | FULL | Interrupt set |
| DW0_CH_STRUCT1_INTR_MASK | 0x40288058 | FULL | Interrupt mask |
| DW0_CH_STRUCT1_INTR_MASKED | 0x4028805C | FULL | Interrupt masked |
| DW0_CH_STRUCT1_SRAM_DATA0 | 0x40288060 | FULL | SRAM data 0 |
| DW0_CH_STRUCT1_SRAM_DATA1 | 0x40288064 | FULL | SRAM data 1 |
| DW0_CH_STRUCT1_TR_CMD | 0x40288068 | FULL | Channel software trigger |

#### 8.1.1.3 CH_STRUCT 2

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT2_CH_CTL | 0x40288080 | FULL | Channel control |
| DW0_CH_STRUCT2_CH_STATUS | 0x40288084 | FULL | Channel status |
| DW0_CH_STRUCT2_CH_IDX | 0x40288088 | FULL | Channel current indices |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT2_CH_CURR_PTR | 0x4028808C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT2_INTR | 0x40288090 | FULL | Interrupt |
| DW0_CH_STRUCT2_INTR_SET | 0x40288094 | FULL | Interrupt set |
| DW0_CH_STRUCT2_INTR_MASK | 0x40288098 | FULL | Interrupt mask |
| DW0_CH_STRUCT2_INTR_MASKED | 0x4028809C | FULL | Interrupt masked |
| DW0_CH_STRUCT2_SRAM_DATA0 | 0x402880A0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT2_SRAM_DATA1 | 0x402880A4 | FULL | SRAM data 1 |
| DW0_CH_STRUCT2_TR_CMD | 0x402880A8 | FULL | Channel software trigger |

### 8.1.1.4 CH_STRUCT 3

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT3_CH_CTL | 0x402880C0 | FULL | Channel control |
| DW0_CH_STRUCT3_CH_STATUS | 0x402880C4 | FULL | Channel status |
| DW0_CH_STRUCT3_CH_IDX | 0x402880C8 | FULL | Channel current indices |
| DW0_CH_STRUCT3_CH_CURR_PTR | 0x402880CC | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT3_INTR | 0x402880D0 | FULL | Interrupt |
| DW0_CH_STRUCT3_INTR_SET | 0x402880D4 | FULL | Interrupt set |
| DW0_CH_STRUCT3_INTR_MASK | 0x402880D8 | FULL | Interrupt mask |
| DW0_CH_STRUCT3_INTR_MASKED | 0x402880DC | FULL | Interrupt masked |
| DW0_CH_STRUCT3_SRAM_DATA0 | 0x402880E0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT3_SRAM_DATA1 | 0x402880E4 | FULL | SRAM data 1 |
| DW0_CH_STRUCT3_TR_CMD | 0x402880E8 | FULL | Channel software trigger |

### 8.1.1.5 CH_STRUCT 4

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT4_CH_CTL | 0x40288100 | FULL | Channel control |
| DW0_CH_STRUCT4_CH_STATUS | 0x40288104 | FULL | Channel status |
| DW0_CH_STRUCT4_CH_IDX | 0x40288108 | FULL | Channel current indices |
| DW0_CH_STRUCT4_CH_CURR_PTR | 0x4028810C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT4_INTR | 0x40288110 | FULL | Interrupt |
| DW0_CH_STRUCT4_INTR_SET | 0x40288114 | FULL | Interrupt set |
| DW0_CH_STRUCT4_INTR_MASK | 0x40288118 | FULL | Interrupt mask |
| DW0_CH_STRUCT4_INTR_MASKED | 0x4028811C | FULL | Interrupt masked |
| DW0_CH_STRUCT4_SRAM_DATA0 | 0x40288120 | FULL | SRAM data 0 |
| DW0_CH_STRUCT4_SRAM_DATA1 | 0x40288124 | FULL | SRAM data 1 |
| DW0_CH_STRUCT4_TR_CMD | 0x40288128 | FULL | Channel software trigger |

### 8.1.1.6 CH_STRUCT 5

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT5_CH_CTL | 0x40288140 | FULL | Channel control |
| DW0_CH_STRUCT5_CH_STATUS | 0x40288144 | FULL | Channel status |
| DW0_CH_STRUCT5_CH_IDX | 0x40288148 | FULL | Channel current indices |
| DW0_CH_STRUCT5_CH_CURR_PTR | 0x4028814C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT5_INTR | 0x40288150 | FULL | Interrupt |
| DW0_CH_STRUCT5_INTR_SET | 0x40288154 | FULL | Interrupt set |
| DW0_CH_STRUCT5_INTR_MASK | 0x40288158 | FULL | Interrupt mask |
| DW0_CH_STRUCT5_INTR_MASKED | 0x4028815C | FULL | Interrupt masked |
| DW0_CH_STRUCT5_SRAM_DATA0 | 0x40288160 | FULL | SRAM data 0 |
| DW0_CH_STRUCT5_SRAM_DATA1 | 0x40288164 | FULL | SRAM data 1 |
| DW0_CH_STRUCT5_TR_CMD | 0x40288168 | FULL | Channel software trigger |

### 8.1.1.7 CH_STRUCT 6

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT6_CH_CTL | 0x40288180 | FULL | Channel control |
| DW0_CH_STRUCT6_CH_STATUS | 0x40288184 | FULL | Channel status |
| DW0_CH_STRUCT6_CH_IDX | 0x40288188 | FULL | Channel current indices |
| DW0_CH_STRUCT6_CH_CURR_PTR | 0x4028818C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT6_INTR | 0x40288190 | FULL | Interrupt |
| DW0_CH_STRUCT6_INTR_SET | 0x40288194 | FULL | Interrupt set |
| DW0_CH_STRUCT6_INTR_MASK | 0x40288198 | FULL | Interrupt mask |
| DW0_CH_STRUCT6_INTR_MASKED | 0x4028819C | FULL | Interrupt masked |
| DW0_CH_STRUCT6_SRAM_DATA0 | 0x402881A0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT6_SRAM_DATA1 | 0x402881A4 | FULL | SRAM data 1 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT6_TR_CMD | 0x402881A8 | FULL | Channel software trigger |

### 8.1.1.8 CH_STRUCT 7

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT7_CH_CTL | 0x402881C0 | FULL | Channel control |
| DW0_CH_STRUCT7_CH_STATUS | 0x402881C4 | FULL | Channel status |
| DW0_CH_STRUCT7_CH_IDX | 0x402881C8 | FULL | Channel current indices |
| DW0_CH_STRUCT7_CH_CURR_PTR | 0x402881CC | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT7_INTR | 0x402881D0 | FULL | Interrupt |
| DW0_CH_STRUCT7_INTR_SET | 0x402881D4 | FULL | Interrupt set |
| DW0_CH_STRUCT7_INTR_MASK | 0x402881D8 | FULL | Interrupt mask |
| DW0_CH_STRUCT7_INTR_MASKED | 0x402881DC | FULL | Interrupt masked |
| DW0_CH_STRUCT7_SRAM_DATA0 | 0x402881E0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT7_SRAM_DATA1 | 0x402881E4 | FULL | SRAM data 1 |
| DW0_CH_STRUCT7_TR_CMD | 0x402881E8 | FULL | Channel software trigger |

### 8.1.1.9 CH_STRUCT 8

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT8_CH_CTL | 0x40288200 | FULL | Channel control |
| DW0_CH_STRUCT8_CH_STATUS | 0x40288204 | FULL | Channel status |
| DW0_CH_STRUCT8_CH_IDX | 0x40288208 | FULL | Channel current indices |
| DW0_CH_STRUCT8_CH_CURR_PTR | 0x4028820C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT8_INTR | 0x40288210 | FULL | Interrupt |
| DW0_CH_STRUCT8_INTR_SET | 0x40288214 | FULL | Interrupt set |
| DW0_CH_STRUCT8_INTR_MASK | 0x40288218 | FULL | Interrupt mask |
| DW0_CH_STRUCT8_INTR_MASKED | 0x4028821C | FULL | Interrupt masked |
| DW0_CH_STRUCT8_SRAM_DATA0 | 0x40288220 | FULL | SRAM data 0 |
| DW0_CH_STRUCT8_SRAM_DATA1 | 0x40288224 | FULL | SRAM data 1 |
| DW0_CH_STRUCT8_TR_CMD | 0x40288228 | FULL | Channel software trigger |

### 8.1.1.10 CH_STRUCT 9

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT9_CH_CTL | 0x40288240 | FULL | Channel control |
| DW0_CH_STRUCT9_CH_STATUS | 0x40288244 | FULL | Channel status |
| DW0_CH_STRUCT9_CH_IDX | 0x40288248 | FULL | Channel current indices |
| DW0_CH_STRUCT9_CH_CURR_PTR | 0x4028824C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT9_INTR | 0x40288250 | FULL | Interrupt |
| DW0_CH_STRUCT9_INTR_SET | 0x40288254 | FULL | Interrupt set |
| DW0_CH_STRUCT9_INTR_MASK | 0x40288258 | FULL | Interrupt mask |
| DW0_CH_STRUCT9_INTR_MASKED | 0x4028825C | FULL | Interrupt masked |
| DW0_CH_STRUCT9_SRAM_DATA0 | 0x40288260 | FULL | SRAM data 0 |
| DW0_CH_STRUCT9_SRAM_DATA1 | 0x40288264 | FULL | SRAM data 1 |
| DW0_CH_STRUCT9_TR_CMD | 0x40288268 | FULL | Channel software trigger |

### 8.1.1.11 CH_STRUCT 10

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT10_CH_CTL | 0x40288280 | FULL | Channel control |
| DW0_CH_STRUCT10_CH_STATUS | 0x40288284 | FULL | Channel status |
| DW0_CH_STRUCT10_CH_IDX | 0x40288288 | FULL | Channel current indices |
| DW0_CH_STRUCT10_CH_CURR_PTR | 0x4028828C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT10_INTR | 0x40288290 | FULL | Interrupt |
| DW0_CH_STRUCT10_INTR_SET | 0x40288294 | FULL | Interrupt set |
| DW0_CH_STRUCT10_INTR_MASK | 0x40288298 | FULL | Interrupt mask |
| DW0_CH_STRUCT10_INTR_MASKED | 0x4028829C | FULL | Interrupt masked |
| DW0_CH_STRUCT10_SRAM_DATA0 | 0x402882A0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT10_SRAM_DATA1 | 0x402882A4 | FULL | SRAM data 1 |
| DW0_CH_STRUCT10_TR_CMD | 0x402882A8 | FULL | Channel software trigger |

### 8.1.1.12 CH_STRUCT 11

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT11_CH_CTL | 0x402882C0 | FULL | Channel control |
| DW0_CH_STRUCT11_CH_STATUS | 0x402882C4 | FULL | Channel status |
| DW0_CH_STRUCT11_CH_IDX | 0x402882C8 | FULL | Channel current indices |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT11_CH_CURR_PTR | 0x402882CC | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT11_INTR | 0x402882D0 | FULL | Interrupt |
| DW0_CH_STRUCT11_INTR_SET | 0x402882D4 | FULL | Interrupt set |
| DW0_CH_STRUCT11_INTR_MASK | 0x402882D8 | FULL | Interrupt mask |
| DW0_CH_STRUCT11_INTR_MASKED | 0x402882DC | FULL | Interrupt masked |
| DW0_CH_STRUCT11_SRAM_DATA0 | 0x402882E0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT11_SRAM_DATA1 | 0x402882E4 | FULL | SRAM data 1 |
| DW0_CH_STRUCT11_TR_CMD | 0x402882E8 | FULL | Channel software trigger |

#### 8.1.1.13 CH_STRUCT 12

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT12_CH_CTL | 0x40288300 | FULL | Channel control |
| DW0_CH_STRUCT12_CH_STATUS | 0x40288304 | FULL | Channel status |
| DW0_CH_STRUCT12_CH_IDX | 0x40288308 | FULL | Channel current indices |
| DW0_CH_STRUCT12_CH_CURR_PTR | 0x4028830C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT12_INTR | 0x40288310 | FULL | Interrupt |
| DW0_CH_STRUCT12_INTR_SET | 0x40288314 | FULL | Interrupt set |
| DW0_CH_STRUCT12_INTR_MASK | 0x40288318 | FULL | Interrupt mask |
| DW0_CH_STRUCT12_INTR_MASKED | 0x4028831C | FULL | Interrupt masked |
| DW0_CH_STRUCT12_SRAM_DATA0 | 0x40288320 | FULL | SRAM data 0 |
| DW0_CH_STRUCT12_SRAM_DATA1 | 0x40288324 | FULL | SRAM data 1 |
| DW0_CH_STRUCT12_TR_CMD | 0x40288328 | FULL | Channel software trigger |

#### 8.1.1.14 CH_STRUCT 13

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT13_CH_CTL | 0x40288340 | FULL | Channel control |
| DW0_CH_STRUCT13_CH_STATUS | 0x40288344 | FULL | Channel status |
| DW0_CH_STRUCT13_CH_IDX | 0x40288348 | FULL | Channel current indices |
| DW0_CH_STRUCT13_CH_CURR_PTR | 0x4028834C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT13_INTR | 0x40288350 | FULL | Interrupt |
| DW0_CH_STRUCT13_INTR_SET | 0x40288354 | FULL | Interrupt set |
| DW0_CH_STRUCT13_INTR_MASK | 0x40288358 | FULL | Interrupt mask |
| DW0_CH_STRUCT13_INTR_MASKED | 0x4028835C | FULL | Interrupt masked |
| DW0_CH_STRUCT13_SRAM_DATA0 | 0x40288360 | FULL | SRAM data 0 |
| DW0_CH_STRUCT13_SRAM_DATA1 | 0x40288364 | FULL | SRAM data 1 |
| DW0_CH_STRUCT13_TR_CMD | 0x40288368 | FULL | Channel software trigger |

#### 8.1.1.15 CH_STRUCT 14

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT14_CH_CTL | 0x40288380 | FULL | Channel control |
| DW0_CH_STRUCT14_CH_STATUS | 0x40288384 | FULL | Channel status |
| DW0_CH_STRUCT14_CH_IDX | 0x40288388 | FULL | Channel current indices |
| DW0_CH_STRUCT14_CH_CURR_PTR | 0x4028838C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT14_INTR | 0x40288390 | FULL | Interrupt |
| DW0_CH_STRUCT14_INTR_SET | 0x40288394 | FULL | Interrupt set |
| DW0_CH_STRUCT14_INTR_MASK | 0x40288398 | FULL | Interrupt mask |
| DW0_CH_STRUCT14_INTR_MASKED | 0x4028839C | FULL | Interrupt masked |
| DW0_CH_STRUCT14_SRAM_DATA0 | 0x402883A0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT14_SRAM_DATA1 | 0x402883A4 | FULL | SRAM data 1 |
| DW0_CH_STRUCT14_TR_CMD | 0x402883A8 | FULL | Channel software trigger |

#### 8.1.1.16 CH_STRUCT 15

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT15_CH_CTL | 0x402883C0 | FULL | Channel control |
| DW0_CH_STRUCT15_CH_STATUS | 0x402883C4 | FULL | Channel status |
| DW0_CH_STRUCT15_CH_IDX | 0x402883C8 | FULL | Channel current indices |
| DW0_CH_STRUCT15_CH_CURR_PTR | 0x402883CC | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT15_INTR | 0x402883D0 | FULL | Interrupt |
| DW0_CH_STRUCT15_INTR_SET | 0x402883D4 | FULL | Interrupt set |
| DW0_CH_STRUCT15_INTR_MASK | 0x402883D8 | FULL | Interrupt mask |
| DW0_CH_STRUCT15_INTR_MASKED | 0x402883DC | FULL | Interrupt masked |
| DW0_CH_STRUCT15_SRAM_DATA0 | 0x402883E0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT15_SRAM_DATA1 | 0x402883E4 | FULL | SRAM data 1 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT15_TR_CMD | 0x402883E8 | FULL | Channel software trigger |

### 8.1.1.17 CH_STRUCT 16

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT16_CH_CTL | 0x40288400 | FULL | Channel control |
| DW0_CH_STRUCT16_CH_STATUS | 0x40288404 | FULL | Channel status |
| DW0_CH_STRUCT16_CH_IDX | 0x40288408 | FULL | Channel current indices |
| DW0_CH_STRUCT16_CH_CURR_PTR | 0x4028840C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT16_INTR | 0x40288410 | FULL | Interrupt |
| DW0_CH_STRUCT16_INTR_SET | 0x40288414 | FULL | Interrupt set |
| DW0_CH_STRUCT16_INTR_MASK | 0x40288418 | FULL | Interrupt mask |
| DW0_CH_STRUCT16_INTR_MASKED | 0x4028841C | FULL | Interrupt masked |
| DW0_CH_STRUCT16_SRAM_DATA0 | 0x40288420 | FULL | SRAM data 0 |
| DW0_CH_STRUCT16_SRAM_DATA1 | 0x40288424 | FULL | SRAM data 1 |
| DW0_CH_STRUCT16_TR_CMD | 0x40288428 | FULL | Channel software trigger |

### 8.1.1.18 CH_STRUCT 17

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT17_CH_CTL | 0x40288440 | FULL | Channel control |
| DW0_CH_STRUCT17_CH_STATUS | 0x40288444 | FULL | Channel status |
| DW0_CH_STRUCT17_CH_IDX | 0x40288448 | FULL | Channel current indices |
| DW0_CH_STRUCT17_CH_CURR_PTR | 0x4028844C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT17_INTR | 0x40288450 | FULL | Interrupt |
| DW0_CH_STRUCT17_INTR_SET | 0x40288454 | FULL | Interrupt set |
| DW0_CH_STRUCT17_INTR_MASK | 0x40288458 | FULL | Interrupt mask |
| DW0_CH_STRUCT17_INTR_MASKED | 0x4028845C | FULL | Interrupt masked |
| DW0_CH_STRUCT17_SRAM_DATA0 | 0x40288460 | FULL | SRAM data 0 |
| DW0_CH_STRUCT17_SRAM_DATA1 | 0x40288464 | FULL | SRAM data 1 |
| DW0_CH_STRUCT17_TR_CMD | 0x40288468 | FULL | Channel software trigger |

### 8.1.1.19 CH_STRUCT 18

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT18_CH_CTL | 0x40288480 | FULL | Channel control |
| DW0_CH_STRUCT18_CH_STATUS | 0x40288484 | FULL | Channel status |
| DW0_CH_STRUCT18_CH_IDX | 0x40288488 | FULL | Channel current indices |
| DW0_CH_STRUCT18_CH_CURR_PTR | 0x4028848C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT18_INTR | 0x40288490 | FULL | Interrupt |
| DW0_CH_STRUCT18_INTR_SET | 0x40288494 | FULL | Interrupt set |
| DW0_CH_STRUCT18_INTR_MASK | 0x40288498 | FULL | Interrupt mask |
| DW0_CH_STRUCT18_INTR_MASKED | 0x4028849C | FULL | Interrupt masked |
| DW0_CH_STRUCT18_SRAM_DATA0 | 0x402884A0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT18_SRAM_DATA1 | 0x402884A4 | FULL | SRAM data 1 |
| DW0_CH_STRUCT18_TR_CMD | 0x402884A8 | FULL | Channel software trigger |

### 8.1.1.20 CH_STRUCT 19

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT19_CH_CTL | 0x402884C0 | FULL | Channel control |
| DW0_CH_STRUCT19_CH_STATUS | 0x402884C4 | FULL | Channel status |
| DW0_CH_STRUCT19_CH_IDX | 0x402884C8 | FULL | Channel current indices |
| DW0_CH_STRUCT19_CH_CURR_PTR | 0x402884CC | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT19_INTR | 0x402884D0 | FULL | Interrupt |
| DW0_CH_STRUCT19_INTR_SET | 0x402884D4 | FULL | Interrupt set |
| DW0_CH_STRUCT19_INTR_MASK | 0x402884D8 | FULL | Interrupt mask |
| DW0_CH_STRUCT19_INTR_MASKED | 0x402884DC | FULL | Interrupt masked |
| DW0_CH_STRUCT19_SRAM_DATA0 | 0x402884E0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT19_SRAM_DATA1 | 0x402884E4 | FULL | SRAM data 1 |
| DW0_CH_STRUCT19_TR_CMD | 0x402884E8 | FULL | Channel software trigger |

### 8.1.1.21 CH_STRUCT 20

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT20_CH_CTL | 0x40288500 | FULL | Channel control |
| DW0_CH_STRUCT20_CH_STATUS | 0x40288504 | FULL | Channel status |
| DW0_CH_STRUCT20_CH_IDX | 0x40288508 | FULL | Channel current indices |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT20_CH_CURR_PTR | 0x4028850C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT20_INTR | 0x40288510 | FULL | Interrupt |
| DW0_CH_STRUCT20_INTR_SET | 0x40288514 | FULL | Interrupt set |
| DW0_CH_STRUCT20_INTR_MASK | 0x40288518 | FULL | Interrupt mask |
| DW0_CH_STRUCT20_INTR_MASKED | 0x4028851C | FULL | Interrupt masked |
| DW0_CH_STRUCT20_SRAM_DATA0 | 0x40288520 | FULL | SRAM data 0 |
| DW0_CH_STRUCT20_SRAM_DATA1 | 0x40288524 | FULL | SRAM data 1 |
| DW0_CH_STRUCT20_TR_CMD | 0x40288528 | FULL | Channel software trigger |

### 8.1.1.22 CH_STRUCT 21

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT21_CH_CTL | 0x40288540 | FULL | Channel control |
| DW0_CH_STRUCT21_CH_STATUS | 0x40288544 | FULL | Channel status |
| DW0_CH_STRUCT21_CH_IDX | 0x40288548 | FULL | Channel current indices |
| DW0_CH_STRUCT21_CH_CURR_PTR | 0x4028854C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT21_INTR | 0x40288550 | FULL | Interrupt |
| DW0_CH_STRUCT21_INTR_SET | 0x40288554 | FULL | Interrupt set |
| DW0_CH_STRUCT21_INTR_MASK | 0x40288558 | FULL | Interrupt mask |
| DW0_CH_STRUCT21_INTR_MASKED | 0x4028855C | FULL | Interrupt masked |
| DW0_CH_STRUCT21_SRAM_DATA0 | 0x40288560 | FULL | SRAM data 0 |
| DW0_CH_STRUCT21_SRAM_DATA1 | 0x40288564 | FULL | SRAM data 1 |
| DW0_CH_STRUCT21_TR_CMD | 0x40288568 | FULL | Channel software trigger |

### 8.1.1.23 CH_STRUCT 22

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT22_CH_CTL | 0x40288580 | FULL | Channel control |
| DW0_CH_STRUCT22_CH_STATUS | 0x40288584 | FULL | Channel status |
| DW0_CH_STRUCT22_CH_IDX | 0x40288588 | FULL | Channel current indices |
| DW0_CH_STRUCT22_CH_CURR_PTR | 0x4028858C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT22_INTR | 0x40288590 | FULL | Interrupt |
| DW0_CH_STRUCT22_INTR_SET | 0x40288594 | FULL | Interrupt set |
| DW0_CH_STRUCT22_INTR_MASK | 0x40288598 | FULL | Interrupt mask |
| DW0_CH_STRUCT22_INTR_MASKED | 0x4028859C | FULL | Interrupt masked |
| DW0_CH_STRUCT22_SRAM_DATA0 | 0x402885A0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT22_SRAM_DATA1 | 0x402885A4 | FULL | SRAM data 1 |
| DW0_CH_STRUCT22_TR_CMD | 0x402885A8 | FULL | Channel software trigger |

### 8.1.1.24 CH_STRUCT 23

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT23_CH_CTL | 0x402885C0 | FULL | Channel control |
| DW0_CH_STRUCT23_CH_STATUS | 0x402885C4 | FULL | Channel status |
| DW0_CH_STRUCT23_CH_IDX | 0x402885C8 | FULL | Channel current indices |
| DW0_CH_STRUCT23_CH_CURR_PTR | 0x402885CC | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT23_INTR | 0x402885D0 | FULL | Interrupt |
| DW0_CH_STRUCT23_INTR_SET | 0x402885D4 | FULL | Interrupt set |
| DW0_CH_STRUCT23_INTR_MASK | 0x402885D8 | FULL | Interrupt mask |
| DW0_CH_STRUCT23_INTR_MASKED | 0x402885DC | FULL | Interrupt masked |
| DW0_CH_STRUCT23_SRAM_DATA0 | 0x402885E0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT23_SRAM_DATA1 | 0x402885E4 | FULL | SRAM data 1 |
| DW0_CH_STRUCT23_TR_CMD | 0x402885E8 | FULL | Channel software trigger |

### 8.1.1.25 CH_STRUCT 24

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT24_CH_CTL | 0x40288600 | FULL | Channel control |
| DW0_CH_STRUCT24_CH_STATUS | 0x40288604 | FULL | Channel status |
| DW0_CH_STRUCT24_CH_IDX | 0x40288608 | FULL | Channel current indices |
| DW0_CH_STRUCT24_CH_CURR_PTR | 0x4028860C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT24_INTR | 0x40288610 | FULL | Interrupt |
| DW0_CH_STRUCT24_INTR_SET | 0x40288614 | FULL | Interrupt set |
| DW0_CH_STRUCT24_INTR_MASK | 0x40288618 | FULL | Interrupt mask |
| DW0_CH_STRUCT24_INTR_MASKED | 0x4028861C | FULL | Interrupt masked |
| DW0_CH_STRUCT24_SRAM_DATA0 | 0x40288620 | FULL | SRAM data 0 |
| DW0_CH_STRUCT24_SRAM_DATA1 | 0x40288624 | FULL | SRAM data 1 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT24_TR_CMD | 0x40288628 | FULL | Channel software trigger |

### 8.1.1.26 CH_STRUCT 25

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT25_CH_CTL | 0x40288640 | FULL | Channel control |
| DW0_CH_STRUCT25_CH_STATUS | 0x40288644 | FULL | Channel status |
| DW0_CH_STRUCT25_CH_IDX | 0x40288648 | FULL | Channel current indices |
| DW0_CH_STRUCT25_CH_CURR_PTR | 0x4028864C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT25_INTR | 0x40288650 | FULL | Interrupt |
| DW0_CH_STRUCT25_INTR_SET | 0x40288654 | FULL | Interrupt set |
| DW0_CH_STRUCT25_INTR_MASK | 0x40288658 | FULL | Interrupt mask |
| DW0_CH_STRUCT25_INTR_MASKED | 0x4028865C | FULL | Interrupt masked |
| DW0_CH_STRUCT25_SRAM_DATA0 | 0x40288660 | FULL | SRAM data 0 |
| DW0_CH_STRUCT25_SRAM_DATA1 | 0x40288664 | FULL | SRAM data 1 |
| DW0_CH_STRUCT25_TR_CMD | 0x40288668 | FULL | Channel software trigger |

### 8.1.1.27 CH_STRUCT 26

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT26_CH_CTL | 0x40288680 | FULL | Channel control |
| DW0_CH_STRUCT26_CH_STATUS | 0x40288684 | FULL | Channel status |
| DW0_CH_STRUCT26_CH_IDX | 0x40288688 | FULL | Channel current indices |
| DW0_CH_STRUCT26_CH_CURR_PTR | 0x4028868C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT26_INTR | 0x40288690 | FULL | Interrupt |
| DW0_CH_STRUCT26_INTR_SET | 0x40288694 | FULL | Interrupt set |
| DW0_CH_STRUCT26_INTR_MASK | 0x40288698 | FULL | Interrupt mask |
| DW0_CH_STRUCT26_INTR_MASKED | 0x4028869C | FULL | Interrupt masked |
| DW0_CH_STRUCT26_SRAM_DATA0 | 0x402886A0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT26_SRAM_DATA1 | 0x402886A4 | FULL | SRAM data 1 |
| DW0_CH_STRUCT26_TR_CMD | 0x402886A8 | FULL | Channel software trigger |

### 8.1.1.28 CH_STRUCT 27

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT27_CH_CTL | 0x402886C0 | FULL | Channel control |
| DW0_CH_STRUCT27_CH_STATUS | 0x402886C4 | FULL | Channel status |
| DW0_CH_STRUCT27_CH_IDX | 0x402886C8 | FULL | Channel current indices |
| DW0_CH_STRUCT27_CH_CURR_PTR | 0x402886CC | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT27_INTR | 0x402886D0 | FULL | Interrupt |
| DW0_CH_STRUCT27_INTR_SET | 0x402886D4 | FULL | Interrupt set |
| DW0_CH_STRUCT27_INTR_MASK | 0x402886D8 | FULL | Interrupt mask |
| DW0_CH_STRUCT27_INTR_MASKED | 0x402886DC | FULL | Interrupt masked |
| DW0_CH_STRUCT27_SRAM_DATA0 | 0x402886E0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT27_SRAM_DATA1 | 0x402886E4 | FULL | SRAM data 1 |
| DW0_CH_STRUCT27_TR_CMD | 0x402886E8 | FULL | Channel software trigger |

### 8.1.1.29 CH_STRUCT 28

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT28_CH_CTL | 0x40288700 | FULL | Channel control |
| DW0_CH_STRUCT28_CH_STATUS | 0x40288704 | FULL | Channel status |
| DW0_CH_STRUCT28_CH_IDX | 0x40288708 | FULL | Channel current indices |
| DW0_CH_STRUCT28_CH_CURR_PTR | 0x4028870C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT28_INTR | 0x40288710 | FULL | Interrupt |
| DW0_CH_STRUCT28_INTR_SET | 0x40288714 | FULL | Interrupt set |
| DW0_CH_STRUCT28_INTR_MASK | 0x40288718 | FULL | Interrupt mask |
| DW0_CH_STRUCT28_INTR_MASKED | 0x4028871C | FULL | Interrupt masked |
| DW0_CH_STRUCT28_SRAM_DATA0 | 0x40288720 | FULL | SRAM data 0 |
| DW0_CH_STRUCT28_SRAM_DATA1 | 0x40288724 | FULL | SRAM data 1 |
| DW0_CH_STRUCT28_TR_CMD | 0x40288728 | FULL | Channel software trigger |

### 8.1.1.30 CH_STRUCT 29

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT29_CH_CTL | 0x40288740 | FULL | Channel control |
| DW0_CH_STRUCT29_CH_STATUS | 0x40288744 | FULL | Channel status |
| DW0_CH_STRUCT29_CH_IDX | 0x40288748 | FULL | Channel current indices |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT29_CH_CURR_PTR | 0x4028874C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT29_INTR | 0x40288750 | FULL | Interrupt |
| DW0_CH_STRUCT29_INTR_SET | 0x40288754 | FULL | Interrupt set |
| DW0_CH_STRUCT29_INTR_MASK | 0x40288758 | FULL | Interrupt mask |
| DW0_CH_STRUCT29_INTR_MASKED | 0x4028875C | FULL | Interrupt masked |
| DW0_CH_STRUCT29_SRAM_DATA0 | 0x40288760 | FULL | SRAM data 0 |
| DW0_CH_STRUCT29_SRAM_DATA1 | 0x40288764 | FULL | SRAM data 1 |
| DW0_CH_STRUCT29_TR_CMD | 0x40288768 | FULL | Channel software trigger |

### 8.1.1.31 CH_STRUCT 30

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT30_CH_CTL | 0x40288780 | FULL | Channel control |
| DW0_CH_STRUCT30_CH_STATUS | 0x40288784 | FULL | Channel status |
| DW0_CH_STRUCT30_CH_IDX | 0x40288788 | FULL | Channel current indices |
| DW0_CH_STRUCT30_CH_CURR_PTR | 0x4028878C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT30_INTR | 0x40288790 | FULL | Interrupt |
| DW0_CH_STRUCT30_INTR_SET | 0x40288794 | FULL | Interrupt set |
| DW0_CH_STRUCT30_INTR_MASK | 0x40288798 | FULL | Interrupt mask |
| DW0_CH_STRUCT30_INTR_MASKED | 0x4028879C | FULL | Interrupt masked |
| DW0_CH_STRUCT30_SRAM_DATA0 | 0x402887A0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT30_SRAM_DATA1 | 0x402887A4 | FULL | SRAM data 1 |
| DW0_CH_STRUCT30_TR_CMD | 0x402887A8 | FULL | Channel software trigger |

### 8.1.1.32 CH_STRUCT 31

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT31_CH_CTL | 0x402887C0 | FULL | Channel control |
| DW0_CH_STRUCT31_CH_STATUS | 0x402887C4 | FULL | Channel status |
| DW0_CH_STRUCT31_CH_IDX | 0x402887C8 | FULL | Channel current indices |
| DW0_CH_STRUCT31_CH_CURR_PTR | 0x402887CC | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT31_INTR | 0x402887D0 | FULL | Interrupt |
| DW0_CH_STRUCT31_INTR_SET | 0x402887D4 | FULL | Interrupt set |
| DW0_CH_STRUCT31_INTR_MASK | 0x402887D8 | FULL | Interrupt mask |
| DW0_CH_STRUCT31_INTR_MASKED | 0x402887DC | FULL | Interrupt masked |
| DW0_CH_STRUCT31_SRAM_DATA0 | 0x402887E0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT31_SRAM_DATA1 | 0x402887E4 | FULL | SRAM data 1 |
| DW0_CH_STRUCT31_TR_CMD | 0x402887E8 | FULL | Channel software trigger |

### 8.1.1.33 CH_STRUCT 32

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT32_CH_CTL | 0x40288800 | FULL | Channel control |
| DW0_CH_STRUCT32_CH_STATUS | 0x40288804 | FULL | Channel status |
| DW0_CH_STRUCT32_CH_IDX | 0x40288808 | FULL | Channel current indices |
| DW0_CH_STRUCT32_CH_CURR_PTR | 0x4028880C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT32_INTR | 0x40288810 | FULL | Interrupt |
| DW0_CH_STRUCT32_INTR_SET | 0x40288814 | FULL | Interrupt set |
| DW0_CH_STRUCT32_INTR_MASK | 0x40288818 | FULL | Interrupt mask |
| DW0_CH_STRUCT32_INTR_MASKED | 0x4028881C | FULL | Interrupt masked |
| DW0_CH_STRUCT32_SRAM_DATA0 | 0x40288820 | FULL | SRAM data 0 |
| DW0_CH_STRUCT32_SRAM_DATA1 | 0x40288824 | FULL | SRAM data 1 |
| DW0_CH_STRUCT32_TR_CMD | 0x40288828 | FULL | Channel software trigger |

### 8.1.1.34 CH_STRUCT 33

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT33_CH_CTL | 0x40288840 | FULL | Channel control |
| DW0_CH_STRUCT33_CH_STATUS | 0x40288844 | FULL | Channel status |
| DW0_CH_STRUCT33_CH_IDX | 0x40288848 | FULL | Channel current indices |
| DW0_CH_STRUCT33_CH_CURR_PTR | 0x4028884C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT33_INTR | 0x40288850 | FULL | Interrupt |
| DW0_CH_STRUCT33_INTR_SET | 0x40288854 | FULL | Interrupt set |
| DW0_CH_STRUCT33_INTR_MASK | 0x40288858 | FULL | Interrupt mask |
| DW0_CH_STRUCT33_INTR_MASKED | 0x4028885C | FULL | Interrupt masked |
| DW0_CH_STRUCT33_SRAM_DATA0 | 0x40288860 | FULL | SRAM data 0 |
| DW0_CH_STRUCT33_SRAM_DATA1 | 0x40288864 | FULL | SRAM data 1 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT33_TR_CMD | 0x40288868 | FULL | Channel software trigger |

### 8.1.1.35 CH_STRUCT 34

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT34_CH_CTL | 0x40288880 | FULL | Channel control |
| DW0_CH_STRUCT34_CH_STATUS | 0x40288884 | FULL | Channel status |
| DW0_CH_STRUCT34_CH_IDX | 0x40288888 | FULL | Channel current indices |
| DW0_CH_STRUCT34_CH_CURR_PTR | 0x4028888C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT34_INTR | 0x40288890 | FULL | Interrupt |
| DW0_CH_STRUCT34_INTR_SET | 0x40288894 | FULL | Interrupt set |
| DW0_CH_STRUCT34_INTR_MASK | 0x40288898 | FULL | Interrupt mask |
| DW0_CH_STRUCT34_INTR_MASKED | 0x4028889C | FULL | Interrupt masked |
| DW0_CH_STRUCT34_SRAM_DATA0 | 0x402888A0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT34_SRAM_DATA1 | 0x402888A4 | FULL | SRAM data 1 |
| DW0_CH_STRUCT34_TR_CMD | 0x402888A8 | FULL | Channel software trigger |

### 8.1.1.36 CH_STRUCT 35

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT35_CH_CTL | 0x402888C0 | FULL | Channel control |
| DW0_CH_STRUCT35_CH_STATUS | 0x402888C4 | FULL | Channel status |
| DW0_CH_STRUCT35_CH_IDX | 0x402888C8 | FULL | Channel current indices |
| DW0_CH_STRUCT35_CH_CURR_PTR | 0x402888CC | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT35_INTR | 0x402888D0 | FULL | Interrupt |
| DW0_CH_STRUCT35_INTR_SET | 0x402888D4 | FULL | Interrupt set |
| DW0_CH_STRUCT35_INTR_MASK | 0x402888D8 | FULL | Interrupt mask |
| DW0_CH_STRUCT35_INTR_MASKED | 0x402888DC | FULL | Interrupt masked |
| DW0_CH_STRUCT35_SRAM_DATA0 | 0x402888E0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT35_SRAM_DATA1 | 0x402888E4 | FULL | SRAM data 1 |
| DW0_CH_STRUCT35_TR_CMD | 0x402888E8 | FULL | Channel software trigger |

### 8.1.1.37 CH_STRUCT 36

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT36_CH_CTL | 0x40288900 | FULL | Channel control |
| DW0_CH_STRUCT36_CH_STATUS | 0x40288904 | FULL | Channel status |
| DW0_CH_STRUCT36_CH_IDX | 0x40288908 | FULL | Channel current indices |
| DW0_CH_STRUCT36_CH_CURR_PTR | 0x4028890C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT36_INTR | 0x40288910 | FULL | Interrupt |
| DW0_CH_STRUCT36_INTR_SET | 0x40288914 | FULL | Interrupt set |
| DW0_CH_STRUCT36_INTR_MASK | 0x40288918 | FULL | Interrupt mask |
| DW0_CH_STRUCT36_INTR_MASKED | 0x4028891C | FULL | Interrupt masked |
| DW0_CH_STRUCT36_SRAM_DATA0 | 0x40288920 | FULL | SRAM data 0 |
| DW0_CH_STRUCT36_SRAM_DATA1 | 0x40288924 | FULL | SRAM data 1 |
| DW0_CH_STRUCT36_TR_CMD | 0x40288928 | FULL | Channel software trigger |

### 8.1.1.38 CH_STRUCT 37

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT37_CH_CTL | 0x40288940 | FULL | Channel control |
| DW0_CH_STRUCT37_CH_STATUS | 0x40288944 | FULL | Channel status |
| DW0_CH_STRUCT37_CH_IDX | 0x40288948 | FULL | Channel current indices |
| DW0_CH_STRUCT37_CH_CURR_PTR | 0x4028894C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT37_INTR | 0x40288950 | FULL | Interrupt |
| DW0_CH_STRUCT37_INTR_SET | 0x40288954 | FULL | Interrupt set |
| DW0_CH_STRUCT37_INTR_MASK | 0x40288958 | FULL | Interrupt mask |
| DW0_CH_STRUCT37_INTR_MASKED | 0x4028895C | FULL | Interrupt masked |
| DW0_CH_STRUCT37_SRAM_DATA0 | 0x40288960 | FULL | SRAM data 0 |
| DW0_CH_STRUCT37_SRAM_DATA1 | 0x40288964 | FULL | SRAM data 1 |
| DW0_CH_STRUCT37_TR_CMD | 0x40288968 | FULL | Channel software trigger |

### 8.1.1.39 CH_STRUCT 38

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT38_CH_CTL | 0x40288980 | FULL | Channel control |
| DW0_CH_STRUCT38_CH_STATUS | 0x40288984 | FULL | Channel status |
| DW0_CH_STRUCT38_CH_IDX | 0x40288988 | FULL | Channel current indices |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT38_CH_CURR_PTR | 0x4028898C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT38_INTR | 0x40288990 | FULL | Interrupt |
| DW0_CH_STRUCT38_INTR_SET | 0x40288994 | FULL | Interrupt set |
| DW0_CH_STRUCT38_INTR_MASK | 0x40288998 | FULL | Interrupt mask |
| DW0_CH_STRUCT38_INTR_MASKED | 0x4028899C | FULL | Interrupt masked |
| DW0_CH_STRUCT38_SRAM_DATA0 | 0x402889A0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT38_SRAM_DATA1 | 0x402889A4 | FULL | SRAM data 1 |
| DW0_CH_STRUCT38_TR_CMD | 0x402889A8 | FULL | Channel software trigger |

### 8.1.1.40 CH_STRUCT 39

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT39_CH_CTL | 0x402889C0 | FULL | Channel control |
| DW0_CH_STRUCT39_CH_STATUS | 0x402889C4 | FULL | Channel status |
| DW0_CH_STRUCT39_CH_IDX | 0x402889C8 | FULL | Channel current indices |
| DW0_CH_STRUCT39_CH_CURR_PTR | 0x402889CC | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT39_INTR | 0x402889D0 | FULL | Interrupt |
| DW0_CH_STRUCT39_INTR_SET | 0x402889D4 | FULL | Interrupt set |
| DW0_CH_STRUCT39_INTR_MASK | 0x402889D8 | FULL | Interrupt mask |
| DW0_CH_STRUCT39_INTR_MASKED | 0x402889DC | FULL | Interrupt masked |
| DW0_CH_STRUCT39_SRAM_DATA0 | 0x402889E0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT39_SRAM_DATA1 | 0x402889E4 | FULL | SRAM data 1 |
| DW0_CH_STRUCT39_TR_CMD | 0x402889E8 | FULL | Channel software trigger |

### 8.1.1.41 CH_STRUCT 40

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT40_CH_CTL | 0x40288A00 | FULL | Channel control |
| DW0_CH_STRUCT40_CH_STATUS | 0x40288A04 | FULL | Channel status |
| DW0_CH_STRUCT40_CH_IDX | 0x40288A08 | FULL | Channel current indices |
| DW0_CH_STRUCT40_CH_CURR_PTR | 0x40288A0C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT40_INTR | 0x40288A10 | FULL | Interrupt |
| DW0_CH_STRUCT40_INTR_SET | 0x40288A14 | FULL | Interrupt set |
| DW0_CH_STRUCT40_INTR_MASK | 0x40288A18 | FULL | Interrupt mask |
| DW0_CH_STRUCT40_INTR_MASKED | 0x40288A1C | FULL | Interrupt masked |
| DW0_CH_STRUCT40_SRAM_DATA0 | 0x40288A20 | FULL | SRAM data 0 |
| DW0_CH_STRUCT40_SRAM_DATA1 | 0x40288A24 | FULL | SRAM data 1 |
| DW0_CH_STRUCT40_TR_CMD | 0x40288A28 | FULL | Channel software trigger |

### 8.1.1.42 CH_STRUCT 41

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT41_CH_CTL | 0x40288A40 | FULL | Channel control |
| DW0_CH_STRUCT41_CH_STATUS | 0x40288A44 | FULL | Channel status |
| DW0_CH_STRUCT41_CH_IDX | 0x40288A48 | FULL | Channel current indices |
| DW0_CH_STRUCT41_CH_CURR_PTR | 0x40288A4C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT41_INTR | 0x40288A50 | FULL | Interrupt |
| DW0_CH_STRUCT41_INTR_SET | 0x40288A54 | FULL | Interrupt set |
| DW0_CH_STRUCT41_INTR_MASK | 0x40288A58 | FULL | Interrupt mask |
| DW0_CH_STRUCT41_INTR_MASKED | 0x40288A5C | FULL | Interrupt masked |
| DW0_CH_STRUCT41_SRAM_DATA0 | 0x40288A60 | FULL | SRAM data 0 |
| DW0_CH_STRUCT41_SRAM_DATA1 | 0x40288A64 | FULL | SRAM data 1 |
| DW0_CH_STRUCT41_TR_CMD | 0x40288A68 | FULL | Channel software trigger |

### 8.1.1.43 CH_STRUCT 42

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT42_CH_CTL | 0x40288A80 | FULL | Channel control |
| DW0_CH_STRUCT42_CH_STATUS | 0x40288A84 | FULL | Channel status |
| DW0_CH_STRUCT42_CH_IDX | 0x40288A88 | FULL | Channel current indices |
| DW0_CH_STRUCT42_CH_CURR_PTR | 0x40288A8C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT42_INTR | 0x40288A90 | FULL | Interrupt |
| DW0_CH_STRUCT42_INTR_SET | 0x40288A94 | FULL | Interrupt set |
| DW0_CH_STRUCT42_INTR_MASK | 0x40288A98 | FULL | Interrupt mask |
| DW0_CH_STRUCT42_INTR_MASKED | 0x40288A9C | FULL | Interrupt masked |
| DW0_CH_STRUCT42_SRAM_DATA0 | 0x40288AA0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT42_SRAM_DATA1 | 0x40288AA4 | FULL | SRAM data 1 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT42_TR_CMD | 0x40288AA8 | FULL | Channel software trigger |

### 8.1.1.44 CH_STRUCT 43

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT43_CH_CTL | 0x40288AC0 | FULL | Channel control |
| DW0_CH_STRUCT43_CH_STATUS | 0x40288AC4 | FULL | Channel status |
| DW0_CH_STRUCT43_CH_IDX | 0x40288AC8 | FULL | Channel current indices |
| DW0_CH_STRUCT43_CH_CURR_PTR | 0x40288ACC | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT43_INTR | 0x40288AD0 | FULL | Interrupt |
| DW0_CH_STRUCT43_INTR_SET | 0x40288AD4 | FULL | Interrupt set |
| DW0_CH_STRUCT43_INTR_MASK | 0x40288AD8 | FULL | Interrupt mask |
| DW0_CH_STRUCT43_INTR_MASKED | 0x40288ADC | FULL | Interrupt masked |
| DW0_CH_STRUCT43_SRAM_DATA0 | 0x40288AE0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT43_SRAM_DATA1 | 0x40288AE4 | FULL | SRAM data 1 |
| DW0_CH_STRUCT43_TR_CMD | 0x40288AE8 | FULL | Channel software trigger |

### 8.1.1.45 CH_STRUCT 44

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT44_CH_CTL | 0x40288B00 | FULL | Channel control |
| DW0_CH_STRUCT44_CH_STATUS | 0x40288B04 | FULL | Channel status |
| DW0_CH_STRUCT44_CH_IDX | 0x40288B08 | FULL | Channel current indices |
| DW0_CH_STRUCT44_CH_CURR_PTR | 0x40288B0C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT44_INTR | 0x40288B10 | FULL | Interrupt |
| DW0_CH_STRUCT44_INTR_SET | 0x40288B14 | FULL | Interrupt set |
| DW0_CH_STRUCT44_INTR_MASK | 0x40288B18 | FULL | Interrupt mask |
| DW0_CH_STRUCT44_INTR_MASKED | 0x40288B1C | FULL | Interrupt masked |
| DW0_CH_STRUCT44_SRAM_DATA0 | 0x40288B20 | FULL | SRAM data 0 |
| DW0_CH_STRUCT44_SRAM_DATA1 | 0x40288B24 | FULL | SRAM data 1 |
| DW0_CH_STRUCT44_TR_CMD | 0x40288B28 | FULL | Channel software trigger |

### 8.1.1.46 CH_STRUCT 45

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT45_CH_CTL | 0x40288B40 | FULL | Channel control |
| DW0_CH_STRUCT45_CH_STATUS | 0x40288B44 | FULL | Channel status |
| DW0_CH_STRUCT45_CH_IDX | 0x40288B48 | FULL | Channel current indices |
| DW0_CH_STRUCT45_CH_CURR_PTR | 0x40288B4C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT45_INTR | 0x40288B50 | FULL | Interrupt |
| DW0_CH_STRUCT45_INTR_SET | 0x40288B54 | FULL | Interrupt set |
| DW0_CH_STRUCT45_INTR_MASK | 0x40288B58 | FULL | Interrupt mask |
| DW0_CH_STRUCT45_INTR_MASKED | 0x40288B5C | FULL | Interrupt masked |
| DW0_CH_STRUCT45_SRAM_DATA0 | 0x40288B60 | FULL | SRAM data 0 |
| DW0_CH_STRUCT45_SRAM_DATA1 | 0x40288B64 | FULL | SRAM data 1 |
| DW0_CH_STRUCT45_TR_CMD | 0x40288B68 | FULL | Channel software trigger |

### 8.1.1.47 CH_STRUCT 46

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT46_CH_CTL | 0x40288B80 | FULL | Channel control |
| DW0_CH_STRUCT46_CH_STATUS | 0x40288B84 | FULL | Channel status |
| DW0_CH_STRUCT46_CH_IDX | 0x40288B88 | FULL | Channel current indices |
| DW0_CH_STRUCT46_CH_CURR_PTR | 0x40288B8C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT46_INTR | 0x40288B90 | FULL | Interrupt |
| DW0_CH_STRUCT46_INTR_SET | 0x40288B94 | FULL | Interrupt set |
| DW0_CH_STRUCT46_INTR_MASK | 0x40288B98 | FULL | Interrupt mask |
| DW0_CH_STRUCT46_INTR_MASKED | 0x40288B9C | FULL | Interrupt masked |
| DW0_CH_STRUCT46_SRAM_DATA0 | 0x40288BA0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT46_SRAM_DATA1 | 0x40288BA4 | FULL | SRAM data 1 |
| DW0_CH_STRUCT46_TR_CMD | 0x40288BA8 | FULL | Channel software trigger |

### 8.1.1.48 CH_STRUCT 47

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT47_CH_CTL | 0x40288BC0 | FULL | Channel control |
| DW0_CH_STRUCT47_CH_STATUS | 0x40288BC4 | FULL | Channel status |
| DW0_CH_STRUCT47_CH_IDX | 0x40288BC8 | FULL | Channel current indices |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT47_CH_CURR_PTR | 0x40288BCC | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT47_INTR | 0x40288BD0 | FULL | Interrupt |
| DW0_CH_STRUCT47_INTR_SET | 0x40288BD4 | FULL | Interrupt set |
| DW0_CH_STRUCT47_INTR_MASK | 0x40288BD8 | FULL | Interrupt mask |
| DW0_CH_STRUCT47_INTR_MASKED | 0x40288BDC | FULL | Interrupt masked |
| DW0_CH_STRUCT47_SRAM_DATA0 | 0x40288BE0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT47_SRAM_DATA1 | 0x40288BE4 | FULL | SRAM data 1 |
| DW0_CH_STRUCT47_TR_CMD | 0x40288BE8 | FULL | Channel software trigger |

### 8.1.1.49 CH_STRUCT 48

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT48_CH_CTL | 0x40288C00 | FULL | Channel control |
| DW0_CH_STRUCT48_CH_STATUS | 0x40288C04 | FULL | Channel status |
| DW0_CH_STRUCT48_CH_IDX | 0x40288C08 | FULL | Channel current indices |
| DW0_CH_STRUCT48_CH_CURR_PTR | 0x40288C0C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT48_INTR | 0x40288C10 | FULL | Interrupt |
| DW0_CH_STRUCT48_INTR_SET | 0x40288C14 | FULL | Interrupt set |
| DW0_CH_STRUCT48_INTR_MASK | 0x40288C18 | FULL | Interrupt mask |
| DW0_CH_STRUCT48_INTR_MASKED | 0x40288C1C | FULL | Interrupt masked |
| DW0_CH_STRUCT48_SRAM_DATA0 | 0x40288C20 | FULL | SRAM data 0 |
| DW0_CH_STRUCT48_SRAM_DATA1 | 0x40288C24 | FULL | SRAM data 1 |
| DW0_CH_STRUCT48_TR_CMD | 0x40288C28 | FULL | Channel software trigger |

### 8.1.1.50 CH_STRUCT 49

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT49_CH_CTL | 0x40288C40 | FULL | Channel control |
| DW0_CH_STRUCT49_CH_STATUS | 0x40288C44 | FULL | Channel status |
| DW0_CH_STRUCT49_CH_IDX | 0x40288C48 | FULL | Channel current indices |
| DW0_CH_STRUCT49_CH_CURR_PTR | 0x40288C4C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT49_INTR | 0x40288C50 | FULL | Interrupt |
| DW0_CH_STRUCT49_INTR_SET | 0x40288C54 | FULL | Interrupt set |
| DW0_CH_STRUCT49_INTR_MASK | 0x40288C58 | FULL | Interrupt mask |
| DW0_CH_STRUCT49_INTR_MASKED | 0x40288C5C | FULL | Interrupt masked |
| DW0_CH_STRUCT49_SRAM_DATA0 | 0x40288C60 | FULL | SRAM data 0 |
| DW0_CH_STRUCT49_SRAM_DATA1 | 0x40288C64 | FULL | SRAM data 1 |
| DW0_CH_STRUCT49_TR_CMD | 0x40288C68 | FULL | Channel software trigger |

### 8.1.1.51 CH_STRUCT 50

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT50_CH_CTL | 0x40288C80 | FULL | Channel control |
| DW0_CH_STRUCT50_CH_STATUS | 0x40288C84 | FULL | Channel status |
| DW0_CH_STRUCT50_CH_IDX | 0x40288C88 | FULL | Channel current indices |
| DW0_CH_STRUCT50_CH_CURR_PTR | 0x40288C8C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT50_INTR | 0x40288C90 | FULL | Interrupt |
| DW0_CH_STRUCT50_INTR_SET | 0x40288C94 | FULL | Interrupt set |
| DW0_CH_STRUCT50_INTR_MASK | 0x40288C98 | FULL | Interrupt mask |
| DW0_CH_STRUCT50_INTR_MASKED | 0x40288C9C | FULL | Interrupt masked |
| DW0_CH_STRUCT50_SRAM_DATA0 | 0x40288CA0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT50_SRAM_DATA1 | 0x40288CA4 | FULL | SRAM data 1 |
| DW0_CH_STRUCT50_TR_CMD | 0x40288CA8 | FULL | Channel software trigger |

### 8.1.1.52 CH_STRUCT 51

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT51_CH_CTL | 0x40288CC0 | FULL | Channel control |
| DW0_CH_STRUCT51_CH_STATUS | 0x40288CC4 | FULL | Channel status |
| DW0_CH_STRUCT51_CH_IDX | 0x40288CC8 | FULL | Channel current indices |
| DW0_CH_STRUCT51_CH_CURR_PTR | 0x40288CCC | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT51_INTR | 0x40288CD0 | FULL | Interrupt |
| DW0_CH_STRUCT51_INTR_SET | 0x40288CD4 | FULL | Interrupt set |
| DW0_CH_STRUCT51_INTR_MASK | 0x40288CD8 | FULL | Interrupt mask |
| DW0_CH_STRUCT51_INTR_MASKED | 0x40288CDC | FULL | Interrupt masked |
| DW0_CH_STRUCT51_SRAM_DATA0 | 0x40288CE0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT51_SRAM_DATA1 | 0x40288CE4 | FULL | SRAM data 1 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT51_TR_CMD | 0x40288CE8 | FULL | Channel software trigger |

### 8.1.1.53 CH_STRUCT 52

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT52_CH_CTL | 0x40288D00 | FULL | Channel control |
| DW0_CH_STRUCT52_CH_STATUS | 0x40288D04 | FULL | Channel status |
| DW0_CH_STRUCT52_CH_IDX | 0x40288D08 | FULL | Channel current indices |
| DW0_CH_STRUCT52_CH_CURR_PTR | 0x40288D0C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT52_INTR | 0x40288D10 | FULL | Interrupt |
| DW0_CH_STRUCT52_INTR_SET | 0x40288D14 | FULL | Interrupt set |
| DW0_CH_STRUCT52_INTR_MASK | 0x40288D18 | FULL | Interrupt mask |
| DW0_CH_STRUCT52_INTR_MASKED | 0x40288D1C | FULL | Interrupt masked |
| DW0_CH_STRUCT52_SRAM_DATA0 | 0x40288D20 | FULL | SRAM data 0 |
| DW0_CH_STRUCT52_SRAM_DATA1 | 0x40288D24 | FULL | SRAM data 1 |
| DW0_CH_STRUCT52_TR_CMD | 0x40288D28 | FULL | Channel software trigger |

### 8.1.1.54 CH_STRUCT 53

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT53_CH_CTL | 0x40288D40 | FULL | Channel control |
| DW0_CH_STRUCT53_CH_STATUS | 0x40288D44 | FULL | Channel status |
| DW0_CH_STRUCT53_CH_IDX | 0x40288D48 | FULL | Channel current indices |
| DW0_CH_STRUCT53_CH_CURR_PTR | 0x40288D4C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT53_INTR | 0x40288D50 | FULL | Interrupt |
| DW0_CH_STRUCT53_INTR_SET | 0x40288D54 | FULL | Interrupt set |
| DW0_CH_STRUCT53_INTR_MASK | 0x40288D58 | FULL | Interrupt mask |
| DW0_CH_STRUCT53_INTR_MASKED | 0x40288D5C | FULL | Interrupt masked |
| DW0_CH_STRUCT53_SRAM_DATA0 | 0x40288D60 | FULL | SRAM data 0 |
| DW0_CH_STRUCT53_SRAM_DATA1 | 0x40288D64 | FULL | SRAM data 1 |
| DW0_CH_STRUCT53_TR_CMD | 0x40288D68 | FULL | Channel software trigger |

### 8.1.1.55 CH_STRUCT 54

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT54_CH_CTL | 0x40288D80 | FULL | Channel control |
| DW0_CH_STRUCT54_CH_STATUS | 0x40288D84 | FULL | Channel status |
| DW0_CH_STRUCT54_CH_IDX | 0x40288D88 | FULL | Channel current indices |
| DW0_CH_STRUCT54_CH_CURR_PTR | 0x40288D8C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT54_INTR | 0x40288D90 | FULL | Interrupt |
| DW0_CH_STRUCT54_INTR_SET | 0x40288D94 | FULL | Interrupt set |
| DW0_CH_STRUCT54_INTR_MASK | 0x40288D98 | FULL | Interrupt mask |
| DW0_CH_STRUCT54_INTR_MASKED | 0x40288D9C | FULL | Interrupt masked |
| DW0_CH_STRUCT54_SRAM_DATA0 | 0x40288DA0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT54_SRAM_DATA1 | 0x40288DA4 | FULL | SRAM data 1 |
| DW0_CH_STRUCT54_TR_CMD | 0x40288DA8 | FULL | Channel software trigger |

### 8.1.1.56 CH_STRUCT 55

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT55_CH_CTL | 0x40288DC0 | FULL | Channel control |
| DW0_CH_STRUCT55_CH_STATUS | 0x40288DC4 | FULL | Channel status |
| DW0_CH_STRUCT55_CH_IDX | 0x40288DC8 | FULL | Channel current indices |
| DW0_CH_STRUCT55_CH_CURR_PTR | 0x40288DCC | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT55_INTR | 0x40288DD0 | FULL | Interrupt |
| DW0_CH_STRUCT55_INTR_SET | 0x40288DD4 | FULL | Interrupt set |
| DW0_CH_STRUCT55_INTR_MASK | 0x40288DD8 | FULL | Interrupt mask |
| DW0_CH_STRUCT55_INTR_MASKED | 0x40288DDC | FULL | Interrupt masked |
| DW0_CH_STRUCT55_SRAM_DATA0 | 0x40288DE0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT55_SRAM_DATA1 | 0x40288DE4 | FULL | SRAM data 1 |
| DW0_CH_STRUCT55_TR_CMD | 0x40288DE8 | FULL | Channel software trigger |

### 8.1.1.57 CH_STRUCT 56

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT56_CH_CTL | 0x40288E00 | FULL | Channel control |
| DW0_CH_STRUCT56_CH_STATUS | 0x40288E04 | FULL | Channel status |
| DW0_CH_STRUCT56_CH_IDX | 0x40288E08 | FULL | Channel current indices |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT56_CH_CURR_PTR | 0x40288E0C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT56_INTR | 0x40288E10 | FULL | Interrupt |
| DW0_CH_STRUCT56_INTR_SET | 0x40288E14 | FULL | Interrupt set |
| DW0_CH_STRUCT56_INTR_MASK | 0x40288E18 | FULL | Interrupt mask |
| DW0_CH_STRUCT56_INTR_MASKED | 0x40288E1C | FULL | Interrupt masked |
| DW0_CH_STRUCT56_SRAM_DATA0 | 0x40288E20 | FULL | SRAM data 0 |
| DW0_CH_STRUCT56_SRAM_DATA1 | 0x40288E24 | FULL | SRAM data 1 |
| DW0_CH_STRUCT56_TR_CMD | 0x40288E28 | FULL | Channel software trigger |

### 8.1.1.58 CH_STRUCT 57

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT57_CH_CTL | 0x40288E40 | FULL | Channel control |
| DW0_CH_STRUCT57_CH_STATUS | 0x40288E44 | FULL | Channel status |
| DW0_CH_STRUCT57_CH_IDX | 0x40288E48 | FULL | Channel current indices |
| DW0_CH_STRUCT57_CH_CURR_PTR | 0x40288E4C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT57_INTR | 0x40288E50 | FULL | Interrupt |
| DW0_CH_STRUCT57_INTR_SET | 0x40288E54 | FULL | Interrupt set |
| DW0_CH_STRUCT57_INTR_MASK | 0x40288E58 | FULL | Interrupt mask |
| DW0_CH_STRUCT57_INTR_MASKED | 0x40288E5C | FULL | Interrupt masked |
| DW0_CH_STRUCT57_SRAM_DATA0 | 0x40288E60 | FULL | SRAM data 0 |
| DW0_CH_STRUCT57_SRAM_DATA1 | 0x40288E64 | FULL | SRAM data 1 |
| DW0_CH_STRUCT57_TR_CMD | 0x40288E68 | FULL | Channel software trigger |

### 8.1.1.59 CH_STRUCT 58

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT58_CH_CTL | 0x40288E80 | FULL | Channel control |
| DW0_CH_STRUCT58_CH_STATUS | 0x40288E84 | FULL | Channel status |
| DW0_CH_STRUCT58_CH_IDX | 0x40288E88 | FULL | Channel current indices |
| DW0_CH_STRUCT58_CH_CURR_PTR | 0x40288E8C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT58_INTR | 0x40288E90 | FULL | Interrupt |
| DW0_CH_STRUCT58_INTR_SET | 0x40288E94 | FULL | Interrupt set |
| DW0_CH_STRUCT58_INTR_MASK | 0x40288E98 | FULL | Interrupt mask |
| DW0_CH_STRUCT58_INTR_MASKED | 0x40288E9C | FULL | Interrupt masked |
| DW0_CH_STRUCT58_SRAM_DATA0 | 0x40288EA0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT58_SRAM_DATA1 | 0x40288EA4 | FULL | SRAM data 1 |
| DW0_CH_STRUCT58_TR_CMD | 0x40288EA8 | FULL | Channel software trigger |

### 8.1.1.60 CH_STRUCT 59

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT59_CH_CTL | 0x40288EC0 | FULL | Channel control |
| DW0_CH_STRUCT59_CH_STATUS | 0x40288EC4 | FULL | Channel status |
| DW0_CH_STRUCT59_CH_IDX | 0x40288EC8 | FULL | Channel current indices |
| DW0_CH_STRUCT59_CH_CURR_PTR | 0x40288ECC | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT59_INTR | 0x40288ED0 | FULL | Interrupt |
| DW0_CH_STRUCT59_INTR_SET | 0x40288ED4 | FULL | Interrupt set |
| DW0_CH_STRUCT59_INTR_MASK | 0x40288ED8 | FULL | Interrupt mask |
| DW0_CH_STRUCT59_INTR_MASKED | 0x40288EDC | FULL | Interrupt masked |
| DW0_CH_STRUCT59_SRAM_DATA0 | 0x40288EE0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT59_SRAM_DATA1 | 0x40288EE4 | FULL | SRAM data 1 |
| DW0_CH_STRUCT59_TR_CMD | 0x40288EE8 | FULL | Channel software trigger |

### 8.1.1.61 CH_STRUCT 60

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT60_CH_CTL | 0x40288F00 | FULL | Channel control |
| DW0_CH_STRUCT60_CH_STATUS | 0x40288F04 | FULL | Channel status |
| DW0_CH_STRUCT60_CH_IDX | 0x40288F08 | FULL | Channel current indices |
| DW0_CH_STRUCT60_CH_CURR_PTR | 0x40288F0C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT60_INTR | 0x40288F10 | FULL | Interrupt |
| DW0_CH_STRUCT60_INTR_SET | 0x40288F14 | FULL | Interrupt set |
| DW0_CH_STRUCT60_INTR_MASK | 0x40288F18 | FULL | Interrupt mask |
| DW0_CH_STRUCT60_INTR_MASKED | 0x40288F1C | FULL | Interrupt masked |
| DW0_CH_STRUCT60_SRAM_DATA0 | 0x40288F20 | FULL | SRAM data 0 |
| DW0_CH_STRUCT60_SRAM_DATA1 | 0x40288F24 | FULL | SRAM data 1 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT60_TR_CMD | 0x40288F28 | FULL | Channel software trigger |

### 8.1.1.62 CH_STRUCT 61

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT61_CH_CTL | 0x40288F40 | FULL | Channel control |
| DW0_CH_STRUCT61_CH_STATUS | 0x40288F44 | FULL | Channel status |
| DW0_CH_STRUCT61_CH_IDX | 0x40288F48 | FULL | Channel current indices |
| DW0_CH_STRUCT61_CH_CURR_PTR | 0x40288F4C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT61_INTR | 0x40288F50 | FULL | Interrupt |
| DW0_CH_STRUCT61_INTR_SET | 0x40288F54 | FULL | Interrupt set |
| DW0_CH_STRUCT61_INTR_MASK | 0x40288F58 | FULL | Interrupt mask |
| DW0_CH_STRUCT61_INTR_MASKED | 0x40288F5C | FULL | Interrupt masked |
| DW0_CH_STRUCT61_SRAM_DATA0 | 0x40288F60 | FULL | SRAM data 0 |
| DW0_CH_STRUCT61_SRAM_DATA1 | 0x40288F64 | FULL | SRAM data 1 |
| DW0_CH_STRUCT61_TR_CMD | 0x40288F68 | FULL | Channel software trigger |

### 8.1.1.63 CH_STRUCT 62

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT62_CH_CTL | 0x40288F80 | FULL | Channel control |
| DW0_CH_STRUCT62_CH_STATUS | 0x40288F84 | FULL | Channel status |
| DW0_CH_STRUCT62_CH_IDX | 0x40288F88 | FULL | Channel current indices |
| DW0_CH_STRUCT62_CH_CURR_PTR | 0x40288F8C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT62_INTR | 0x40288F90 | FULL | Interrupt |
| DW0_CH_STRUCT62_INTR_SET | 0x40288F94 | FULL | Interrupt set |
| DW0_CH_STRUCT62_INTR_MASK | 0x40288F98 | FULL | Interrupt mask |
| DW0_CH_STRUCT62_INTR_MASKED | 0x40288F9C | FULL | Interrupt masked |
| DW0_CH_STRUCT62_SRAM_DATA0 | 0x40288FA0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT62_SRAM_DATA1 | 0x40288FA4 | FULL | SRAM data 1 |
| DW0_CH_STRUCT62_TR_CMD | 0x40288FA8 | FULL | Channel software trigger |

### 8.1.1.64 CH_STRUCT 63

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT63_CH_CTL | 0x40288FC0 | FULL | Channel control |
| DW0_CH_STRUCT63_CH_STATUS | 0x40288FC4 | FULL | Channel status |
| DW0_CH_STRUCT63_CH_IDX | 0x40288FC8 | FULL | Channel current indices |
| DW0_CH_STRUCT63_CH_CURR_PTR | 0x40288FCC | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT63_INTR | 0x40288FD0 | FULL | Interrupt |
| DW0_CH_STRUCT63_INTR_SET | 0x40288FD4 | FULL | Interrupt set |
| DW0_CH_STRUCT63_INTR_MASK | 0x40288FD8 | FULL | Interrupt mask |
| DW0_CH_STRUCT63_INTR_MASKED | 0x40288FDC | FULL | Interrupt masked |
| DW0_CH_STRUCT63_SRAM_DATA0 | 0x40288FE0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT63_SRAM_DATA1 | 0x40288FE4 | FULL | SRAM data 1 |
| DW0_CH_STRUCT63_TR_CMD | 0x40288FE8 | FULL | Channel software trigger |

### 8.1.1.65 CH_STRUCT 64

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT64_CH_CTL | 0x40289000 | FULL | Channel control |
| DW0_CH_STRUCT64_CH_STATUS | 0x40289004 | FULL | Channel status |
| DW0_CH_STRUCT64_CH_IDX | 0x40289008 | FULL | Channel current indices |
| DW0_CH_STRUCT64_CH_CURR_PTR | 0x4028900C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT64_INTR | 0x40289010 | FULL | Interrupt |
| DW0_CH_STRUCT64_INTR_SET | 0x40289014 | FULL | Interrupt set |
| DW0_CH_STRUCT64_INTR_MASK | 0x40289018 | FULL | Interrupt mask |
| DW0_CH_STRUCT64_INTR_MASKED | 0x4028901C | FULL | Interrupt masked |
| DW0_CH_STRUCT64_SRAM_DATA0 | 0x40289020 | FULL | SRAM data 0 |
| DW0_CH_STRUCT64_SRAM_DATA1 | 0x40289024 | FULL | SRAM data 1 |
| DW0_CH_STRUCT64_TR_CMD | 0x40289028 | FULL | Channel software trigger |

### 8.1.1.66 CH_STRUCT 65

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT65_CH_CTL | 0x40289040 | FULL | Channel control |
| DW0_CH_STRUCT65_CH_STATUS | 0x40289044 | FULL | Channel status |
| DW0_CH_STRUCT65_CH_IDX | 0x40289048 | FULL | Channel current indices |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT65_CH_CURR_PTR | 0x4028904C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT65_INTR | 0x40289050 | FULL | Interrupt |
| DW0_CH_STRUCT65_INTR_SET | 0x40289054 | FULL | Interrupt set |
| DW0_CH_STRUCT65_INTR_MASK | 0x40289058 | FULL | Interrupt mask |
| DW0_CH_STRUCT65_INTR_MASKED | 0x4028905C | FULL | Interrupt masked |
| DW0_CH_STRUCT65_SRAM_DATA0 | 0x40289060 | FULL | SRAM data 0 |
| DW0_CH_STRUCT65_SRAM_DATA1 | 0x40289064 | FULL | SRAM data 1 |
| DW0_CH_STRUCT65_TR_CMD | 0x40289068 | FULL | Channel software trigger |

### 8.1.1.67 CH_STRUCT 66

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT66_CH_CTL | 0x40289080 | FULL | Channel control |
| DW0_CH_STRUCT66_CH_STATUS | 0x40289084 | FULL | Channel status |
| DW0_CH_STRUCT66_CH_IDX | 0x40289088 | FULL | Channel current indices |
| DW0_CH_STRUCT66_CH_CURR_PTR | 0x4028908C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT66_INTR | 0x40289090 | FULL | Interrupt |
| DW0_CH_STRUCT66_INTR_SET | 0x40289094 | FULL | Interrupt set |
| DW0_CH_STRUCT66_INTR_MASK | 0x40289098 | FULL | Interrupt mask |
| DW0_CH_STRUCT66_INTR_MASKED | 0x4028909C | FULL | Interrupt masked |
| DW0_CH_STRUCT66_SRAM_DATA0 | 0x402890A0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT66_SRAM_DATA1 | 0x402890A4 | FULL | SRAM data 1 |
| DW0_CH_STRUCT66_TR_CMD | 0x402890A8 | FULL | Channel software trigger |

### 8.1.1.68 CH_STRUCT 67

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT67_CH_CTL | 0x402890C0 | FULL | Channel control |
| DW0_CH_STRUCT67_CH_STATUS | 0x402890C4 | FULL | Channel status |
| DW0_CH_STRUCT67_CH_IDX | 0x402890C8 | FULL | Channel current indices |
| DW0_CH_STRUCT67_CH_CURR_PTR | 0x402890CC | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT67_INTR | 0x402890D0 | FULL | Interrupt |
| DW0_CH_STRUCT67_INTR_SET | 0x402890D4 | FULL | Interrupt set |
| DW0_CH_STRUCT67_INTR_MASK | 0x402890D8 | FULL | Interrupt mask |
| DW0_CH_STRUCT67_INTR_MASKED | 0x402890DC | FULL | Interrupt masked |
| DW0_CH_STRUCT67_SRAM_DATA0 | 0x402890E0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT67_SRAM_DATA1 | 0x402890E4 | FULL | SRAM data 1 |
| DW0_CH_STRUCT67_TR_CMD | 0x402890E8 | FULL | Channel software trigger |

### 8.1.1.69 CH_STRUCT 68

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT68_CH_CTL | 0x40289100 | FULL | Channel control |
| DW0_CH_STRUCT68_CH_STATUS | 0x40289104 | FULL | Channel status |
| DW0_CH_STRUCT68_CH_IDX | 0x40289108 | FULL | Channel current indices |
| DW0_CH_STRUCT68_CH_CURR_PTR | 0x4028910C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT68_INTR | 0x40289110 | FULL | Interrupt |
| DW0_CH_STRUCT68_INTR_SET | 0x40289114 | FULL | Interrupt set |
| DW0_CH_STRUCT68_INTR_MASK | 0x40289118 | FULL | Interrupt mask |
| DW0_CH_STRUCT68_INTR_MASKED | 0x4028911C | FULL | Interrupt masked |
| DW0_CH_STRUCT68_SRAM_DATA0 | 0x40289120 | FULL | SRAM data 0 |
| DW0_CH_STRUCT68_SRAM_DATA1 | 0x40289124 | FULL | SRAM data 1 |
| DW0_CH_STRUCT68_TR_CMD | 0x40289128 | FULL | Channel software trigger |

### 8.1.1.70 CH_STRUCT 69

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT69_CH_CTL | 0x40289140 | FULL | Channel control |
| DW0_CH_STRUCT69_CH_STATUS | 0x40289144 | FULL | Channel status |
| DW0_CH_STRUCT69_CH_IDX | 0x40289148 | FULL | Channel current indices |
| DW0_CH_STRUCT69_CH_CURR_PTR | 0x4028914C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT69_INTR | 0x40289150 | FULL | Interrupt |
| DW0_CH_STRUCT69_INTR_SET | 0x40289154 | FULL | Interrupt set |
| DW0_CH_STRUCT69_INTR_MASK | 0x40289158 | FULL | Interrupt mask |
| DW0_CH_STRUCT69_INTR_MASKED | 0x4028915C | FULL | Interrupt masked |
| DW0_CH_STRUCT69_SRAM_DATA0 | 0x40289160 | FULL | SRAM data 0 |
| DW0_CH_STRUCT69_SRAM_DATA1 | 0x40289164 | FULL | SRAM data 1 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT69_TR_CMD | 0x40289168 | FULL | Channel software trigger |

### 8.1.1.71 CH_STRUCT 70

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT70_CH_CTL | 0x40289180 | FULL | Channel control |
| DW0_CH_STRUCT70_CH_STATUS | 0x40289184 | FULL | Channel status |
| DW0_CH_STRUCT70_CH_IDX | 0x40289188 | FULL | Channel current indices |
| DW0_CH_STRUCT70_CH_CURR_PTR | 0x4028918C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT70_INTR | 0x40289190 | FULL | Interrupt |
| DW0_CH_STRUCT70_INTR_SET | 0x40289194 | FULL | Interrupt set |
| DW0_CH_STRUCT70_INTR_MASK | 0x40289198 | FULL | Interrupt mask |
| DW0_CH_STRUCT70_INTR_MASKED | 0x4028919C | FULL | Interrupt masked |
| DW0_CH_STRUCT70_SRAM_DATA0 | 0x402891A0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT70_SRAM_DATA1 | 0x402891A4 | FULL | SRAM data 1 |
| DW0_CH_STRUCT70_TR_CMD | 0x402891A8 | FULL | Channel software trigger |

### 8.1.1.72 CH_STRUCT 71

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT71_CH_CTL | 0x402891C0 | FULL | Channel control |
| DW0_CH_STRUCT71_CH_STATUS | 0x402891C4 | FULL | Channel status |
| DW0_CH_STRUCT71_CH_IDX | 0x402891C8 | FULL | Channel current indices |
| DW0_CH_STRUCT71_CH_CURR_PTR | 0x402891CC | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT71_INTR | 0x402891D0 | FULL | Interrupt |
| DW0_CH_STRUCT71_INTR_SET | 0x402891D4 | FULL | Interrupt set |
| DW0_CH_STRUCT71_INTR_MASK | 0x402891D8 | FULL | Interrupt mask |
| DW0_CH_STRUCT71_INTR_MASKED | 0x402891DC | FULL | Interrupt masked |
| DW0_CH_STRUCT71_SRAM_DATA0 | 0x402891E0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT71_SRAM_DATA1 | 0x402891E4 | FULL | SRAM data 1 |
| DW0_CH_STRUCT71_TR_CMD | 0x402891E8 | FULL | Channel software trigger |

### 8.1.1.73 CH_STRUCT 72

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT72_CH_CTL | 0x40289200 | FULL | Channel control |
| DW0_CH_STRUCT72_CH_STATUS | 0x40289204 | FULL | Channel status |
| DW0_CH_STRUCT72_CH_IDX | 0x40289208 | FULL | Channel current indices |
| DW0_CH_STRUCT72_CH_CURR_PTR | 0x4028920C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT72_INTR | 0x40289210 | FULL | Interrupt |
| DW0_CH_STRUCT72_INTR_SET | 0x40289214 | FULL | Interrupt set |
| DW0_CH_STRUCT72_INTR_MASK | 0x40289218 | FULL | Interrupt mask |
| DW0_CH_STRUCT72_INTR_MASKED | 0x4028921C | FULL | Interrupt masked |
| DW0_CH_STRUCT72_SRAM_DATA0 | 0x40289220 | FULL | SRAM data 0 |
| DW0_CH_STRUCT72_SRAM_DATA1 | 0x40289224 | FULL | SRAM data 1 |
| DW0_CH_STRUCT72_TR_CMD | 0x40289228 | FULL | Channel software trigger |

### 8.1.1.74 CH_STRUCT 73

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT73_CH_CTL | 0x40289240 | FULL | Channel control |
| DW0_CH_STRUCT73_CH_STATUS | 0x40289244 | FULL | Channel status |
| DW0_CH_STRUCT73_CH_IDX | 0x40289248 | FULL | Channel current indices |
| DW0_CH_STRUCT73_CH_CURR_PTR | 0x4028924C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT73_INTR | 0x40289250 | FULL | Interrupt |
| DW0_CH_STRUCT73_INTR_SET | 0x40289254 | FULL | Interrupt set |
| DW0_CH_STRUCT73_INTR_MASK | 0x40289258 | FULL | Interrupt mask |
| DW0_CH_STRUCT73_INTR_MASKED | 0x4028925C | FULL | Interrupt masked |
| DW0_CH_STRUCT73_SRAM_DATA0 | 0x40289260 | FULL | SRAM data 0 |
| DW0_CH_STRUCT73_SRAM_DATA1 | 0x40289264 | FULL | SRAM data 1 |
| DW0_CH_STRUCT73_TR_CMD | 0x40289268 | FULL | Channel software trigger |

### 8.1.1.75 CH_STRUCT 74

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT74_CH_CTL | 0x40289280 | FULL | Channel control |
| DW0_CH_STRUCT74_CH_STATUS | 0x40289284 | FULL | Channel status |
| DW0_CH_STRUCT74_CH_IDX | 0x40289288 | FULL | Channel current indices |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT74_CH_CURR_PTR | 0x4028928C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT74_INTR | 0x40289290 | FULL | Interrupt |
| DW0_CH_STRUCT74_INTR_SET | 0x40289294 | FULL | Interrupt set |
| DW0_CH_STRUCT74_INTR_MASK | 0x40289298 | FULL | Interrupt mask |
| DW0_CH_STRUCT74_INTR_MASKED | 0x4028929C | FULL | Interrupt masked |
| DW0_CH_STRUCT74_SRAM_DATA0 | 0x402892A0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT74_SRAM_DATA1 | 0x402892A4 | FULL | SRAM data 1 |
| DW0_CH_STRUCT74_TR_CMD | 0x402892A8 | FULL | Channel software trigger |

### 8.1.1.76 CH_STRUCT 75

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT75_CH_CTL | 0x402892C0 | FULL | Channel control |
| DW0_CH_STRUCT75_CH_STATUS | 0x402892C4 | FULL | Channel status |
| DW0_CH_STRUCT75_CH_IDX | 0x402892C8 | FULL | Channel current indices |
| DW0_CH_STRUCT75_CH_CURR_PTR | 0x402892CC | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT75_INTR | 0x402892D0 | FULL | Interrupt |
| DW0_CH_STRUCT75_INTR_SET | 0x402892D4 | FULL | Interrupt set |
| DW0_CH_STRUCT75_INTR_MASK | 0x402892D8 | FULL | Interrupt mask |
| DW0_CH_STRUCT75_INTR_MASKED | 0x402892DC | FULL | Interrupt masked |
| DW0_CH_STRUCT75_SRAM_DATA0 | 0x402892E0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT75_SRAM_DATA1 | 0x402892E4 | FULL | SRAM data 1 |
| DW0_CH_STRUCT75_TR_CMD | 0x402892E8 | FULL | Channel software trigger |

### 8.1.1.77 CH_STRUCT 76

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT76_CH_CTL | 0x40289300 | FULL | Channel control |
| DW0_CH_STRUCT76_CH_STATUS | 0x40289304 | FULL | Channel status |
| DW0_CH_STRUCT76_CH_IDX | 0x40289308 | FULL | Channel current indices |
| DW0_CH_STRUCT76_CH_CURR_PTR | 0x4028930C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT76_INTR | 0x40289310 | FULL | Interrupt |
| DW0_CH_STRUCT76_INTR_SET | 0x40289314 | FULL | Interrupt set |
| DW0_CH_STRUCT76_INTR_MASK | 0x40289318 | FULL | Interrupt mask |
| DW0_CH_STRUCT76_INTR_MASKED | 0x4028931C | FULL | Interrupt masked |
| DW0_CH_STRUCT76_SRAM_DATA0 | 0x40289320 | FULL | SRAM data 0 |
| DW0_CH_STRUCT76_SRAM_DATA1 | 0x40289324 | FULL | SRAM data 1 |
| DW0_CH_STRUCT76_TR_CMD | 0x40289328 | FULL | Channel software trigger |

### 8.1.1.78 CH_STRUCT 77

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT77_CH_CTL | 0x40289340 | FULL | Channel control |
| DW0_CH_STRUCT77_CH_STATUS | 0x40289344 | FULL | Channel status |
| DW0_CH_STRUCT77_CH_IDX | 0x40289348 | FULL | Channel current indices |
| DW0_CH_STRUCT77_CH_CURR_PTR | 0x4028934C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT77_INTR | 0x40289350 | FULL | Interrupt |
| DW0_CH_STRUCT77_INTR_SET | 0x40289354 | FULL | Interrupt set |
| DW0_CH_STRUCT77_INTR_MASK | 0x40289358 | FULL | Interrupt mask |
| DW0_CH_STRUCT77_INTR_MASKED | 0x4028935C | FULL | Interrupt masked |
| DW0_CH_STRUCT77_SRAM_DATA0 | 0x40289360 | FULL | SRAM data 0 |
| DW0_CH_STRUCT77_SRAM_DATA1 | 0x40289364 | FULL | SRAM data 1 |
| DW0_CH_STRUCT77_TR_CMD | 0x40289368 | FULL | Channel software trigger |

### 8.1.1.79 CH_STRUCT 78

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT78_CH_CTL | 0x40289380 | FULL | Channel control |
| DW0_CH_STRUCT78_CH_STATUS | 0x40289384 | FULL | Channel status |
| DW0_CH_STRUCT78_CH_IDX | 0x40289388 | FULL | Channel current indices |
| DW0_CH_STRUCT78_CH_CURR_PTR | 0x4028938C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT78_INTR | 0x40289390 | FULL | Interrupt |
| DW0_CH_STRUCT78_INTR_SET | 0x40289394 | FULL | Interrupt set |
| DW0_CH_STRUCT78_INTR_MASK | 0x40289398 | FULL | Interrupt mask |
| DW0_CH_STRUCT78_INTR_MASKED | 0x4028939C | FULL | Interrupt masked |
| DW0_CH_STRUCT78_SRAM_DATA0 | 0x402893A0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT78_SRAM_DATA1 | 0x402893A4 | FULL | SRAM data 1 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT78_TR_CMD | 0x402893A8 | FULL | Channel software trigger |

### 8.1.1.80 CH_STRUCT 79

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT79_CH_CTL | 0x402893C0 | FULL | Channel control |
| DW0_CH_STRUCT79_CH_STATUS | 0x402893C4 | FULL | Channel status |
| DW0_CH_STRUCT79_CH_IDX | 0x402893C8 | FULL | Channel current indices |
| DW0_CH_STRUCT79_CH_CURR_PTR | 0x402893CC | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT79_INTR | 0x402893D0 | FULL | Interrupt |
| DW0_CH_STRUCT79_INTR_SET | 0x402893D4 | FULL | Interrupt set |
| DW0_CH_STRUCT79_INTR_MASK | 0x402893D8 | FULL | Interrupt mask |
| DW0_CH_STRUCT79_INTR_MASKED | 0x402893DC | FULL | Interrupt masked |
| DW0_CH_STRUCT79_SRAM_DATA0 | 0x402893E0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT79_SRAM_DATA1 | 0x402893E4 | FULL | SRAM data 1 |
| DW0_CH_STRUCT79_TR_CMD | 0x402893E8 | FULL | Channel software trigger |

### 8.1.1.81 CH_STRUCT 80

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT80_CH_CTL | 0x40289400 | FULL | Channel control |
| DW0_CH_STRUCT80_CH_STATUS | 0x40289404 | FULL | Channel status |
| DW0_CH_STRUCT80_CH_IDX | 0x40289408 | FULL | Channel current indices |
| DW0_CH_STRUCT80_CH_CURR_PTR | 0x4028940C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT80_INTR | 0x40289410 | FULL | Interrupt |
| DW0_CH_STRUCT80_INTR_SET | 0x40289414 | FULL | Interrupt set |
| DW0_CH_STRUCT80_INTR_MASK | 0x40289418 | FULL | Interrupt mask |
| DW0_CH_STRUCT80_INTR_MASKED | 0x4028941C | FULL | Interrupt masked |
| DW0_CH_STRUCT80_SRAM_DATA0 | 0x40289420 | FULL | SRAM data 0 |
| DW0_CH_STRUCT80_SRAM_DATA1 | 0x40289424 | FULL | SRAM data 1 |
| DW0_CH_STRUCT80_TR_CMD | 0x40289428 | FULL | Channel software trigger |

### 8.1.1.82 CH_STRUCT 81

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT81_CH_CTL | 0x40289440 | FULL | Channel control |
| DW0_CH_STRUCT81_CH_STATUS | 0x40289444 | FULL | Channel status |
| DW0_CH_STRUCT81_CH_IDX | 0x40289448 | FULL | Channel current indices |
| DW0_CH_STRUCT81_CH_CURR_PTR | 0x4028944C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT81_INTR | 0x40289450 | FULL | Interrupt |
| DW0_CH_STRUCT81_INTR_SET | 0x40289454 | FULL | Interrupt set |
| DW0_CH_STRUCT81_INTR_MASK | 0x40289458 | FULL | Interrupt mask |
| DW0_CH_STRUCT81_INTR_MASKED | 0x4028945C | FULL | Interrupt masked |
| DW0_CH_STRUCT81_SRAM_DATA0 | 0x40289460 | FULL | SRAM data 0 |
| DW0_CH_STRUCT81_SRAM_DATA1 | 0x40289464 | FULL | SRAM data 1 |
| DW0_CH_STRUCT81_TR_CMD | 0x40289468 | FULL | Channel software trigger |

### 8.1.1.83 CH_STRUCT 82

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT82_CH_CTL | 0x40289480 | FULL | Channel control |
| DW0_CH_STRUCT82_CH_STATUS | 0x40289484 | FULL | Channel status |
| DW0_CH_STRUCT82_CH_IDX | 0x40289488 | FULL | Channel current indices |
| DW0_CH_STRUCT82_CH_CURR_PTR | 0x4028948C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT82_INTR | 0x40289490 | FULL | Interrupt |
| DW0_CH_STRUCT82_INTR_SET | 0x40289494 | FULL | Interrupt set |
| DW0_CH_STRUCT82_INTR_MASK | 0x40289498 | FULL | Interrupt mask |
| DW0_CH_STRUCT82_INTR_MASKED | 0x4028949C | FULL | Interrupt masked |
| DW0_CH_STRUCT82_SRAM_DATA0 | 0x402894A0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT82_SRAM_DATA1 | 0x402894A4 | FULL | SRAM data 1 |
| DW0_CH_STRUCT82_TR_CMD | 0x402894A8 | FULL | Channel software trigger |

### 8.1.1.84 CH_STRUCT 83

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT83_CH_CTL | 0x402894C0 | FULL | Channel control |
| DW0_CH_STRUCT83_CH_STATUS | 0x402894C4 | FULL | Channel status |
| DW0_CH_STRUCT83_CH_IDX | 0x402894C8 | FULL | Channel current indices |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT83_CH_CURR_PTR | 0x402894CC | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT83_INTR | 0x402894D0 | FULL | Interrupt |
| DW0_CH_STRUCT83_INTR_SET | 0x402894D4 | FULL | Interrupt set |
| DW0_CH_STRUCT83_INTR_MASK | 0x402894D8 | FULL | Interrupt mask |
| DW0_CH_STRUCT83_INTR_MASKED | 0x402894DC | FULL | Interrupt masked |
| DW0_CH_STRUCT83_SRAM_DATA0 | 0x402894E0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT83_SRAM_DATA1 | 0x402894E4 | FULL | SRAM data 1 |
| DW0_CH_STRUCT83_TR_CMD | 0x402894E8 | FULL | Channel software trigger |

### 8.1.1.85 CH_STRUCT 84

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT84_CH_CTL | 0x40289500 | FULL | Channel control |
| DW0_CH_STRUCT84_CH_STATUS | 0x40289504 | FULL | Channel status |
| DW0_CH_STRUCT84_CH_IDX | 0x40289508 | FULL | Channel current indices |
| DW0_CH_STRUCT84_CH_CURR_PTR | 0x4028950C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT84_INTR | 0x40289510 | FULL | Interrupt |
| DW0_CH_STRUCT84_INTR_SET | 0x40289514 | FULL | Interrupt set |
| DW0_CH_STRUCT84_INTR_MASK | 0x40289518 | FULL | Interrupt mask |
| DW0_CH_STRUCT84_INTR_MASKED | 0x4028951C | FULL | Interrupt masked |
| DW0_CH_STRUCT84_SRAM_DATA0 | 0x40289520 | FULL | SRAM data 0 |
| DW0_CH_STRUCT84_SRAM_DATA1 | 0x40289524 | FULL | SRAM data 1 |
| DW0_CH_STRUCT84_TR_CMD | 0x40289528 | FULL | Channel software trigger |

### 8.1.1.86 CH_STRUCT 85

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT85_CH_CTL | 0x40289540 | FULL | Channel control |
| DW0_CH_STRUCT85_CH_STATUS | 0x40289544 | FULL | Channel status |
| DW0_CH_STRUCT85_CH_IDX | 0x40289548 | FULL | Channel current indices |
| DW0_CH_STRUCT85_CH_CURR_PTR | 0x4028954C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT85_INTR | 0x40289550 | FULL | Interrupt |
| DW0_CH_STRUCT85_INTR_SET | 0x40289554 | FULL | Interrupt set |
| DW0_CH_STRUCT85_INTR_MASK | 0x40289558 | FULL | Interrupt mask |
| DW0_CH_STRUCT85_INTR_MASKED | 0x4028955C | FULL | Interrupt masked |
| DW0_CH_STRUCT85_SRAM_DATA0 | 0x40289560 | FULL | SRAM data 0 |
| DW0_CH_STRUCT85_SRAM_DATA1 | 0x40289564 | FULL | SRAM data 1 |
| DW0_CH_STRUCT85_TR_CMD | 0x40289568 | FULL | Channel software trigger |

### 8.1.1.87 CH_STRUCT 86

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT86_CH_CTL | 0x40289580 | FULL | Channel control |
| DW0_CH_STRUCT86_CH_STATUS | 0x40289584 | FULL | Channel status |
| DW0_CH_STRUCT86_CH_IDX | 0x40289588 | FULL | Channel current indices |
| DW0_CH_STRUCT86_CH_CURR_PTR | 0x4028958C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT86_INTR | 0x40289590 | FULL | Interrupt |
| DW0_CH_STRUCT86_INTR_SET | 0x40289594 | FULL | Interrupt set |
| DW0_CH_STRUCT86_INTR_MASK | 0x40289598 | FULL | Interrupt mask |
| DW0_CH_STRUCT86_INTR_MASKED | 0x4028959C | FULL | Interrupt masked |
| DW0_CH_STRUCT86_SRAM_DATA0 | 0x402895A0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT86_SRAM_DATA1 | 0x402895A4 | FULL | SRAM data 1 |
| DW0_CH_STRUCT86_TR_CMD | 0x402895A8 | FULL | Channel software trigger |

### 8.1.1.88 CH_STRUCT 87

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT87_CH_CTL | 0x402895C0 | FULL | Channel control |
| DW0_CH_STRUCT87_CH_STATUS | 0x402895C4 | FULL | Channel status |
| DW0_CH_STRUCT87_CH_IDX | 0x402895C8 | FULL | Channel current indices |
| DW0_CH_STRUCT87_CH_CURR_PTR | 0x402895CC | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT87_INTR | 0x402895D0 | FULL | Interrupt |
| DW0_CH_STRUCT87_INTR_SET | 0x402895D4 | FULL | Interrupt set |
| DW0_CH_STRUCT87_INTR_MASK | 0x402895D8 | FULL | Interrupt mask |
| DW0_CH_STRUCT87_INTR_MASKED | 0x402895DC | FULL | Interrupt masked |
| DW0_CH_STRUCT87_SRAM_DATA0 | 0x402895E0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT87_SRAM_DATA1 | 0x402895E4 | FULL | SRAM data 1 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT87_TR_CMD | 0x402895E8 | FULL | Channel software trigger |

### 8.1.1.89 CH_STRUCT 88

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT88_CH_CTL | 0x40289600 | FULL | Channel control |
| DW0_CH_STRUCT88_CH_STATUS | 0x40289604 | FULL | Channel status |
| DW0_CH_STRUCT88_CH_IDX | 0x40289608 | FULL | Channel current indices |
| DW0_CH_STRUCT88_CH_CURR_PTR | 0x4028960C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT88_INTR | 0x40289610 | FULL | Interrupt |
| DW0_CH_STRUCT88_INTR_SET | 0x40289614 | FULL | Interrupt set |
| DW0_CH_STRUCT88_INTR_MASK | 0x40289618 | FULL | Interrupt mask |
| DW0_CH_STRUCT88_INTR_MASKED | 0x4028961C | FULL | Interrupt masked |
| DW0_CH_STRUCT88_SRAM_DATA0 | 0x40289620 | FULL | SRAM data 0 |
| DW0_CH_STRUCT88_SRAM_DATA1 | 0x40289624 | FULL | SRAM data 1 |
| DW0_CH_STRUCT88_TR_CMD | 0x40289628 | FULL | Channel software trigger |

### 8.1.1.90 CH_STRUCT 89

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT89_CH_CTL | 0x40289640 | FULL | Channel control |
| DW0_CH_STRUCT89_CH_STATUS | 0x40289644 | FULL | Channel status |
| DW0_CH_STRUCT89_CH_IDX | 0x40289648 | FULL | Channel current indices |
| DW0_CH_STRUCT89_CH_CURR_PTR | 0x4028964C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT89_INTR | 0x40289650 | FULL | Interrupt |
| DW0_CH_STRUCT89_INTR_SET | 0x40289654 | FULL | Interrupt set |
| DW0_CH_STRUCT89_INTR_MASK | 0x40289658 | FULL | Interrupt mask |
| DW0_CH_STRUCT89_INTR_MASKED | 0x4028965C | FULL | Interrupt masked |
| DW0_CH_STRUCT89_SRAM_DATA0 | 0x40289660 | FULL | SRAM data 0 |
| DW0_CH_STRUCT89_SRAM_DATA1 | 0x40289664 | FULL | SRAM data 1 |
| DW0_CH_STRUCT89_TR_CMD | 0x40289668 | FULL | Channel software trigger |

### 8.1.1.91 CH_STRUCT 90

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT90_CH_CTL | 0x40289680 | FULL | Channel control |
| DW0_CH_STRUCT90_CH_STATUS | 0x40289684 | FULL | Channel status |
| DW0_CH_STRUCT90_CH_IDX | 0x40289688 | FULL | Channel current indices |
| DW0_CH_STRUCT90_CH_CURR_PTR | 0x4028968C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT90_INTR | 0x40289690 | FULL | Interrupt |
| DW0_CH_STRUCT90_INTR_SET | 0x40289694 | FULL | Interrupt set |
| DW0_CH_STRUCT90_INTR_MASK | 0x40289698 | FULL | Interrupt mask |
| DW0_CH_STRUCT90_INTR_MASKED | 0x4028969C | FULL | Interrupt masked |
| DW0_CH_STRUCT90_SRAM_DATA0 | 0x402896A0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT90_SRAM_DATA1 | 0x402896A4 | FULL | SRAM data 1 |
| DW0_CH_STRUCT90_TR_CMD | 0x402896A8 | FULL | Channel software trigger |

### 8.1.1.92 CH_STRUCT 91

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT91_CH_CTL | 0x402896C0 | FULL | Channel control |
| DW0_CH_STRUCT91_CH_STATUS | 0x402896C4 | FULL | Channel status |
| DW0_CH_STRUCT91_CH_IDX | 0x402896C8 | FULL | Channel current indices |
| DW0_CH_STRUCT91_CH_CURR_PTR | 0x402896CC | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT91_INTR | 0x402896D0 | FULL | Interrupt |
| DW0_CH_STRUCT91_INTR_SET | 0x402896D4 | FULL | Interrupt set |
| DW0_CH_STRUCT91_INTR_MASK | 0x402896D8 | FULL | Interrupt mask |
| DW0_CH_STRUCT91_INTR_MASKED | 0x402896DC | FULL | Interrupt masked |
| DW0_CH_STRUCT91_SRAM_DATA0 | 0x402896E0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT91_SRAM_DATA1 | 0x402896E4 | FULL | SRAM data 1 |
| DW0_CH_STRUCT91_TR_CMD | 0x402896E8 | FULL | Channel software trigger |

### 8.1.1.93 CH_STRUCT 92

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT92_CH_CTL | 0x40289700 | FULL | Channel control |
| DW0_CH_STRUCT92_CH_STATUS | 0x40289704 | FULL | Channel status |
| DW0_CH_STRUCT92_CH_IDX | 0x40289708 | FULL | Channel current indices |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT92_CH_CURR_PTR | 0x4028970C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT92_INTR | 0x40289710 | FULL | Interrupt |
| DW0_CH_STRUCT92_INTR_SET | 0x40289714 | FULL | Interrupt set |
| DW0_CH_STRUCT92_INTR_MASK | 0x40289718 | FULL | Interrupt mask |
| DW0_CH_STRUCT92_INTR_MASKED | 0x4028971C | FULL | Interrupt masked |
| DW0_CH_STRUCT92_SRAM_DATA0 | 0x40289720 | FULL | SRAM data 0 |
| DW0_CH_STRUCT92_SRAM_DATA1 | 0x40289724 | FULL | SRAM data 1 |
| DW0_CH_STRUCT92_TR_CMD | 0x40289728 | FULL | Channel software trigger |

### 8.1.1.94 CH_STRUCT 93

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT93_CH_CTL | 0x40289740 | FULL | Channel control |
| DW0_CH_STRUCT93_CH_STATUS | 0x40289744 | FULL | Channel status |
| DW0_CH_STRUCT93_CH_IDX | 0x40289748 | FULL | Channel current indices |
| DW0_CH_STRUCT93_CH_CURR_PTR | 0x4028974C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT93_INTR | 0x40289750 | FULL | Interrupt |
| DW0_CH_STRUCT93_INTR_SET | 0x40289754 | FULL | Interrupt set |
| DW0_CH_STRUCT93_INTR_MASK | 0x40289758 | FULL | Interrupt mask |
| DW0_CH_STRUCT93_INTR_MASKED | 0x4028975C | FULL | Interrupt masked |
| DW0_CH_STRUCT93_SRAM_DATA0 | 0x40289760 | FULL | SRAM data 0 |
| DW0_CH_STRUCT93_SRAM_DATA1 | 0x40289764 | FULL | SRAM data 1 |
| DW0_CH_STRUCT93_TR_CMD | 0x40289768 | FULL | Channel software trigger |

### 8.1.1.95 CH_STRUCT 94

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT94_CH_CTL | 0x40289780 | FULL | Channel control |
| DW0_CH_STRUCT94_CH_STATUS | 0x40289784 | FULL | Channel status |
| DW0_CH_STRUCT94_CH_IDX | 0x40289788 | FULL | Channel current indices |
| DW0_CH_STRUCT94_CH_CURR_PTR | 0x4028978C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT94_INTR | 0x40289790 | FULL | Interrupt |
| DW0_CH_STRUCT94_INTR_SET | 0x40289794 | FULL | Interrupt set |
| DW0_CH_STRUCT94_INTR_MASK | 0x40289798 | FULL | Interrupt mask |
| DW0_CH_STRUCT94_INTR_MASKED | 0x4028979C | FULL | Interrupt masked |
| DW0_CH_STRUCT94_SRAM_DATA0 | 0x402897A0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT94_SRAM_DATA1 | 0x402897A4 | FULL | SRAM data 1 |
| DW0_CH_STRUCT94_TR_CMD | 0x402897A8 | FULL | Channel software trigger |

### 8.1.1.96 CH_STRUCT 95

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT95_CH_CTL | 0x402897C0 | FULL | Channel control |
| DW0_CH_STRUCT95_CH_STATUS | 0x402897C4 | FULL | Channel status |
| DW0_CH_STRUCT95_CH_IDX | 0x402897C8 | FULL | Channel current indices |
| DW0_CH_STRUCT95_CH_CURR_PTR | 0x402897CC | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT95_INTR | 0x402897D0 | FULL | Interrupt |
| DW0_CH_STRUCT95_INTR_SET | 0x402897D4 | FULL | Interrupt set |
| DW0_CH_STRUCT95_INTR_MASK | 0x402897D8 | FULL | Interrupt mask |
| DW0_CH_STRUCT95_INTR_MASKED | 0x402897DC | FULL | Interrupt masked |
| DW0_CH_STRUCT95_SRAM_DATA0 | 0x402897E0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT95_SRAM_DATA1 | 0x402897E4 | FULL | SRAM data 1 |
| DW0_CH_STRUCT95_TR_CMD | 0x402897E8 | FULL | Channel software trigger |

### 8.1.1.97 CH_STRUCT 96

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT96_CH_CTL | 0x40289800 | FULL | Channel control |
| DW0_CH_STRUCT96_CH_STATUS | 0x40289804 | FULL | Channel status |
| DW0_CH_STRUCT96_CH_IDX | 0x40289808 | FULL | Channel current indices |
| DW0_CH_STRUCT96_CH_CURR_PTR | 0x4028980C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT96_INTR | 0x40289810 | FULL | Interrupt |
| DW0_CH_STRUCT96_INTR_SET | 0x40289814 | FULL | Interrupt set |
| DW0_CH_STRUCT96_INTR_MASK | 0x40289818 | FULL | Interrupt mask |
| DW0_CH_STRUCT96_INTR_MASKED | 0x4028981C | FULL | Interrupt masked |
| DW0_CH_STRUCT96_SRAM_DATA0 | 0x40289820 | FULL | SRAM data 0 |
| DW0_CH_STRUCT96_SRAM_DATA1 | 0x40289824 | FULL | SRAM data 1 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT96_TR_CMD | 0x40289828 | FULL | Channel software trigger |

### 8.1.1.98 CH_STRUCT 97

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT97_CH_CTL | 0x40289840 | FULL | Channel control |
| DW0_CH_STRUCT97_CH_STATUS | 0x40289844 | FULL | Channel status |
| DW0_CH_STRUCT97_CH_IDX | 0x40289848 | FULL | Channel current indices |
| DW0_CH_STRUCT97_CH_CURR_PTR | 0x4028984C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT97_INTR | 0x40289850 | FULL | Interrupt |
| DW0_CH_STRUCT97_INTR_SET | 0x40289854 | FULL | Interrupt set |
| DW0_CH_STRUCT97_INTR_MASK | 0x40289858 | FULL | Interrupt mask |
| DW0_CH_STRUCT97_INTR_MASKED | 0x4028985C | FULL | Interrupt masked |
| DW0_CH_STRUCT97_SRAM_DATA0 | 0x40289860 | FULL | SRAM data 0 |
| DW0_CH_STRUCT97_SRAM_DATA1 | 0x40289864 | FULL | SRAM data 1 |
| DW0_CH_STRUCT97_TR_CMD | 0x40289868 | FULL | Channel software trigger |

### 8.1.1.99 CH_STRUCT 98

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT98_CH_CTL | 0x40289880 | FULL | Channel control |
| DW0_CH_STRUCT98_CH_STATUS | 0x40289884 | FULL | Channel status |
| DW0_CH_STRUCT98_CH_IDX | 0x40289888 | FULL | Channel current indices |
| DW0_CH_STRUCT98_CH_CURR_PTR | 0x4028988C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT98_INTR | 0x40289890 | FULL | Interrupt |
| DW0_CH_STRUCT98_INTR_SET | 0x40289894 | FULL | Interrupt set |
| DW0_CH_STRUCT98_INTR_MASK | 0x40289898 | FULL | Interrupt mask |
| DW0_CH_STRUCT98_INTR_MASKED | 0x4028989C | FULL | Interrupt masked |
| DW0_CH_STRUCT98_SRAM_DATA0 | 0x402898A0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT98_SRAM_DATA1 | 0x402898A4 | FULL | SRAM data 1 |
| DW0_CH_STRUCT98_TR_CMD | 0x402898A8 | FULL | Channel software trigger |

### 8.1.1.100 CH_STRUCT 99

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT99_CH_CTL | 0x402898C0 | FULL | Channel control |
| DW0_CH_STRUCT99_CH_STATUS | 0x402898C4 | FULL | Channel status |
| DW0_CH_STRUCT99_CH_IDX | 0x402898C8 | FULL | Channel current indices |
| DW0_CH_STRUCT99_CH_CURR_PTR | 0x402898CC | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT99_INTR | 0x402898D0 | FULL | Interrupt |
| DW0_CH_STRUCT99_INTR_SET | 0x402898D4 | FULL | Interrupt set |
| DW0_CH_STRUCT99_INTR_MASK | 0x402898D8 | FULL | Interrupt mask |
| DW0_CH_STRUCT99_INTR_MASKED | 0x402898DC | FULL | Interrupt masked |
| DW0_CH_STRUCT99_SRAM_DATA0 | 0x402898E0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT99_SRAM_DATA1 | 0x402898E4 | FULL | SRAM data 1 |
| DW0_CH_STRUCT99_TR_CMD | 0x402898E8 | FULL | Channel software trigger |

### 8.1.1.101 CH_STRUCT 100

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT100_CH_CTL | 0x40289900 | FULL | Channel control |
| DW0_CH_STRUCT100_CH_STATUS | 0x40289904 | FULL | Channel status |
| DW0_CH_STRUCT100_CH_IDX | 0x40289908 | FULL | Channel current indices |
| DW0_CH_STRUCT100_CH_CURR_PTR | 0x4028990C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT100_INTR | 0x40289910 | FULL | Interrupt |
| DW0_CH_STRUCT100_INTR_SET | 0x40289914 | FULL | Interrupt set |
| DW0_CH_STRUCT100_INTR_MASK | 0x40289918 | FULL | Interrupt mask |
| DW0_CH_STRUCT100_INTR_MASKED | 0x4028991C | FULL | Interrupt masked |
| DW0_CH_STRUCT100_SRAM_DATA0 | 0x40289920 | FULL | SRAM data 0 |
| DW0_CH_STRUCT100_SRAM_DATA1 | 0x40289924 | FULL | SRAM data 1 |
| DW0_CH_STRUCT100_TR_CMD | 0x40289928 | FULL | Channel software trigger |

### 8.1.1.102 CH_STRUCT 101

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT101_CH_CTL | 0x40289940 | FULL | Channel control |
| DW0_CH_STRUCT101_CH_STATUS | 0x40289944 | FULL | Channel status |
| DW0_CH_STRUCT101_CH_IDX | 0x40289948 | FULL | Channel current indices |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT101_CH_CURR_PTR | 0x4028994C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT101_INTR | 0x40289950 | FULL | Interrupt |
| DW0_CH_STRUCT101_INTR_SET | 0x40289954 | FULL | Interrupt set |
| DW0_CH_STRUCT101_INTR_MASK | 0x40289958 | FULL | Interrupt mask |
| DW0_CH_STRUCT101_INTR_MASKED | 0x4028995C | FULL | Interrupt masked |
| DW0_CH_STRUCT101_SRAM_DATA0 | 0x40289960 | FULL | SRAM data 0 |
| DW0_CH_STRUCT101_SRAM_DATA1 | 0x40289964 | FULL | SRAM data 1 |
| DW0_CH_STRUCT101_TR_CMD | 0x40289968 | FULL | Channel software trigger |

### 8.1.1.103 CH_STRUCT 102

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT102_CH_CTL | 0x40289980 | FULL | Channel control |
| DW0_CH_STRUCT102_CH_STATUS | 0x40289984 | FULL | Channel status |
| DW0_CH_STRUCT102_CH_IDX | 0x40289988 | FULL | Channel current indices |
| DW0_CH_STRUCT102_CH_CURR_PTR | 0x4028998C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT102_INTR | 0x40289990 | FULL | Interrupt |
| DW0_CH_STRUCT102_INTR_SET | 0x40289994 | FULL | Interrupt set |
| DW0_CH_STRUCT102_INTR_MASK | 0x40289998 | FULL | Interrupt mask |
| DW0_CH_STRUCT102_INTR_MASKED | 0x4028999C | FULL | Interrupt masked |
| DW0_CH_STRUCT102_SRAM_DATA0 | 0x402899A0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT102_SRAM_DATA1 | 0x402899A4 | FULL | SRAM data 1 |
| DW0_CH_STRUCT102_TR_CMD | 0x402899A8 | FULL | Channel software trigger |

### 8.1.1.104 CH_STRUCT 103

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT103_CH_CTL | 0x402899C0 | FULL | Channel control |
| DW0_CH_STRUCT103_CH_STATUS | 0x402899C4 | FULL | Channel status |
| DW0_CH_STRUCT103_CH_IDX | 0x402899C8 | FULL | Channel current indices |
| DW0_CH_STRUCT103_CH_CURR_PTR | 0x402899CC | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT103_INTR | 0x402899D0 | FULL | Interrupt |
| DW0_CH_STRUCT103_INTR_SET | 0x402899D4 | FULL | Interrupt set |
| DW0_CH_STRUCT103_INTR_MASK | 0x402899D8 | FULL | Interrupt mask |
| DW0_CH_STRUCT103_INTR_MASKED | 0x402899DC | FULL | Interrupt masked |
| DW0_CH_STRUCT103_SRAM_DATA0 | 0x402899E0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT103_SRAM_DATA1 | 0x402899E4 | FULL | SRAM data 1 |
| DW0_CH_STRUCT103_TR_CMD | 0x402899E8 | FULL | Channel software trigger |

### 8.1.1.105 CH_STRUCT 104

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT104_CH_CTL | 0x40289A00 | FULL | Channel control |
| DW0_CH_STRUCT104_CH_STATUS | 0x40289A04 | FULL | Channel status |
| DW0_CH_STRUCT104_CH_IDX | 0x40289A08 | FULL | Channel current indices |
| DW0_CH_STRUCT104_CH_CURR_PTR | 0x40289A0C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT104_INTR | 0x40289A10 | FULL | Interrupt |
| DW0_CH_STRUCT104_INTR_SET | 0x40289A14 | FULL | Interrupt set |
| DW0_CH_STRUCT104_INTR_MASK | 0x40289A18 | FULL | Interrupt mask |
| DW0_CH_STRUCT104_INTR_MASKED | 0x40289A1C | FULL | Interrupt masked |
| DW0_CH_STRUCT104_SRAM_DATA0 | 0x40289A20 | FULL | SRAM data 0 |
| DW0_CH_STRUCT104_SRAM_DATA1 | 0x40289A24 | FULL | SRAM data 1 |
| DW0_CH_STRUCT104_TR_CMD | 0x40289A28 | FULL | Channel software trigger |

### 8.1.1.106 CH_STRUCT 105

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT105_CH_CTL | 0x40289A40 | FULL | Channel control |
| DW0_CH_STRUCT105_CH_STATUS | 0x40289A44 | FULL | Channel status |
| DW0_CH_STRUCT105_CH_IDX | 0x40289A48 | FULL | Channel current indices |
| DW0_CH_STRUCT105_CH_CURR_PTR | 0x40289A4C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT105_INTR | 0x40289A50 | FULL | Interrupt |
| DW0_CH_STRUCT105_INTR_SET | 0x40289A54 | FULL | Interrupt set |
| DW0_CH_STRUCT105_INTR_MASK | 0x40289A58 | FULL | Interrupt mask |
| DW0_CH_STRUCT105_INTR_MASKED | 0x40289A5C | FULL | Interrupt masked |
| DW0_CH_STRUCT105_SRAM_DATA0 | 0x40289A60 | FULL | SRAM data 0 |
| DW0_CH_STRUCT105_SRAM_DATA1 | 0x40289A64 | FULL | SRAM data 1 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT105_TR_CMD | 0x40289A68 | FULL | Channel software trigger |

### 8.1.1.107 CH_STRUCT 106

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT106_CH_CTL | 0x40289A80 | FULL | Channel control |
| DW0_CH_STRUCT106_CH_STATUS | 0x40289A84 | FULL | Channel status |
| DW0_CH_STRUCT106_CH_IDX | 0x40289A88 | FULL | Channel current indices |
| DW0_CH_STRUCT106_CH_CURR_PTR | 0x40289A8C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT106_INTR | 0x40289A90 | FULL | Interrupt |
| DW0_CH_STRUCT106_INTR_SET | 0x40289A94 | FULL | Interrupt set |
| DW0_CH_STRUCT106_INTR_MASK | 0x40289A98 | FULL | Interrupt mask |
| DW0_CH_STRUCT106_INTR_MASKED | 0x40289A9C | FULL | Interrupt masked |
| DW0_CH_STRUCT106_SRAM_DATA0 | 0x40289AA0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT106_SRAM_DATA1 | 0x40289AA4 | FULL | SRAM data 1 |
| DW0_CH_STRUCT106_TR_CMD | 0x40289AA8 | FULL | Channel software trigger |

### 8.1.1.108 CH_STRUCT 107

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT107_CH_CTL | 0x40289AC0 | FULL | Channel control |
| DW0_CH_STRUCT107_CH_STATUS | 0x40289AC4 | FULL | Channel status |
| DW0_CH_STRUCT107_CH_IDX | 0x40289AC8 | FULL | Channel current indices |
| DW0_CH_STRUCT107_CH_CURR_PTR | 0x40289ACC | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT107_INTR | 0x40289AD0 | FULL | Interrupt |
| DW0_CH_STRUCT107_INTR_SET | 0x40289AD4 | FULL | Interrupt set |
| DW0_CH_STRUCT107_INTR_MASK | 0x40289AD8 | FULL | Interrupt mask |
| DW0_CH_STRUCT107_INTR_MASKED | 0x40289ADC | FULL | Interrupt masked |
| DW0_CH_STRUCT107_SRAM_DATA0 | 0x40289AE0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT107_SRAM_DATA1 | 0x40289AE4 | FULL | SRAM data 1 |
| DW0_CH_STRUCT107_TR_CMD | 0x40289AE8 | FULL | Channel software trigger |

### 8.1.1.109 CH_STRUCT 108

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT108_CH_CTL | 0x40289B00 | FULL | Channel control |
| DW0_CH_STRUCT108_CH_STATUS | 0x40289B04 | FULL | Channel status |
| DW0_CH_STRUCT108_CH_IDX | 0x40289B08 | FULL | Channel current indices |
| DW0_CH_STRUCT108_CH_CURR_PTR | 0x40289B0C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT108_INTR | 0x40289B10 | FULL | Interrupt |
| DW0_CH_STRUCT108_INTR_SET | 0x40289B14 | FULL | Interrupt set |
| DW0_CH_STRUCT108_INTR_MASK | 0x40289B18 | FULL | Interrupt mask |
| DW0_CH_STRUCT108_INTR_MASKED | 0x40289B1C | FULL | Interrupt masked |
| DW0_CH_STRUCT108_SRAM_DATA0 | 0x40289B20 | FULL | SRAM data 0 |
| DW0_CH_STRUCT108_SRAM_DATA1 | 0x40289B24 | FULL | SRAM data 1 |
| DW0_CH_STRUCT108_TR_CMD | 0x40289B28 | FULL | Channel software trigger |

### 8.1.1.110 CH_STRUCT 109

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT109_CH_CTL | 0x40289B40 | FULL | Channel control |
| DW0_CH_STRUCT109_CH_STATUS | 0x40289B44 | FULL | Channel status |
| DW0_CH_STRUCT109_CH_IDX | 0x40289B48 | FULL | Channel current indices |
| DW0_CH_STRUCT109_CH_CURR_PTR | 0x40289B4C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT109_INTR | 0x40289B50 | FULL | Interrupt |
| DW0_CH_STRUCT109_INTR_SET | 0x40289B54 | FULL | Interrupt set |
| DW0_CH_STRUCT109_INTR_MASK | 0x40289B58 | FULL | Interrupt mask |
| DW0_CH_STRUCT109_INTR_MASKED | 0x40289B5C | FULL | Interrupt masked |
| DW0_CH_STRUCT109_SRAM_DATA0 | 0x40289B60 | FULL | SRAM data 0 |
| DW0_CH_STRUCT109_SRAM_DATA1 | 0x40289B64 | FULL | SRAM data 1 |
| DW0_CH_STRUCT109_TR_CMD | 0x40289B68 | FULL | Channel software trigger |

### 8.1.1.111 CH_STRUCT 110

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT110_CH_CTL | 0x40289B80 | FULL | Channel control |
| DW0_CH_STRUCT110_CH_STATUS | 0x40289B84 | FULL | Channel status |
| DW0_CH_STRUCT110_CH_IDX | 0x40289B88 | FULL | Channel current indices |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT110_CH_CURR_PTR | 0x40289B8C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT110_INTR | 0x40289B90 | FULL | Interrupt |
| DW0_CH_STRUCT110_INTR_SET | 0x40289B94 | FULL | Interrupt set |
| DW0_CH_STRUCT110_INTR_MASK | 0x40289B98 | FULL | Interrupt mask |
| DW0_CH_STRUCT110_INTR_MASKED | 0x40289B9C | FULL | Interrupt masked |
| DW0_CH_STRUCT110_SRAM_DATA0 | 0x40289BA0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT110_SRAM_DATA1 | 0x40289BA4 | FULL | SRAM data 1 |
| DW0_CH_STRUCT110_TR_CMD | 0x40289BA8 | FULL | Channel software trigger |

### 8.1.1.112 CH_STRUCT 111

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT111_CH_CTL | 0x40289BC0 | FULL | Channel control |
| DW0_CH_STRUCT111_CH_STATUS | 0x40289BC4 | FULL | Channel status |
| DW0_CH_STRUCT111_CH_IDX | 0x40289BC8 | FULL | Channel current indices |
| DW0_CH_STRUCT111_CH_CURR_PTR | 0x40289BCC | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT111_INTR | 0x40289BD0 | FULL | Interrupt |
| DW0_CH_STRUCT111_INTR_SET | 0x40289BD4 | FULL | Interrupt set |
| DW0_CH_STRUCT111_INTR_MASK | 0x40289BD8 | FULL | Interrupt mask |
| DW0_CH_STRUCT111_INTR_MASKED | 0x40289BDC | FULL | Interrupt masked |
| DW0_CH_STRUCT111_SRAM_DATA0 | 0x40289BE0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT111_SRAM_DATA1 | 0x40289BE4 | FULL | SRAM data 1 |
| DW0_CH_STRUCT111_TR_CMD | 0x40289BE8 | FULL | Channel software trigger |

### 8.1.1.113 CH_STRUCT 112

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT112_CH_CTL | 0x40289C00 | FULL | Channel control |
| DW0_CH_STRUCT112_CH_STATUS | 0x40289C04 | FULL | Channel status |
| DW0_CH_STRUCT112_CH_IDX | 0x40289C08 | FULL | Channel current indices |
| DW0_CH_STRUCT112_CH_CURR_PTR | 0x40289C0C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT112_INTR | 0x40289C10 | FULL | Interrupt |
| DW0_CH_STRUCT112_INTR_SET | 0x40289C14 | FULL | Interrupt set |
| DW0_CH_STRUCT112_INTR_MASK | 0x40289C18 | FULL | Interrupt mask |
| DW0_CH_STRUCT112_INTR_MASKED | 0x40289C1C | FULL | Interrupt masked |
| DW0_CH_STRUCT112_SRAM_DATA0 | 0x40289C20 | FULL | SRAM data 0 |
| DW0_CH_STRUCT112_SRAM_DATA1 | 0x40289C24 | FULL | SRAM data 1 |
| DW0_CH_STRUCT112_TR_CMD | 0x40289C28 | FULL | Channel software trigger |

### 8.1.1.114 CH_STRUCT 113

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT113_CH_CTL | 0x40289C40 | FULL | Channel control |
| DW0_CH_STRUCT113_CH_STATUS | 0x40289C44 | FULL | Channel status |
| DW0_CH_STRUCT113_CH_IDX | 0x40289C48 | FULL | Channel current indices |
| DW0_CH_STRUCT113_CH_CURR_PTR | 0x40289C4C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT113_INTR | 0x40289C50 | FULL | Interrupt |
| DW0_CH_STRUCT113_INTR_SET | 0x40289C54 | FULL | Interrupt set |
| DW0_CH_STRUCT113_INTR_MASK | 0x40289C58 | FULL | Interrupt mask |
| DW0_CH_STRUCT113_INTR_MASKED | 0x40289C5C | FULL | Interrupt masked |
| DW0_CH_STRUCT113_SRAM_DATA0 | 0x40289C60 | FULL | SRAM data 0 |
| DW0_CH_STRUCT113_SRAM_DATA1 | 0x40289C64 | FULL | SRAM data 1 |
| DW0_CH_STRUCT113_TR_CMD | 0x40289C68 | FULL | Channel software trigger |

### 8.1.1.115 CH_STRUCT 114

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT114_CH_CTL | 0x40289C80 | FULL | Channel control |
| DW0_CH_STRUCT114_CH_STATUS | 0x40289C84 | FULL | Channel status |
| DW0_CH_STRUCT114_CH_IDX | 0x40289C88 | FULL | Channel current indices |
| DW0_CH_STRUCT114_CH_CURR_PTR | 0x40289C8C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT114_INTR | 0x40289C90 | FULL | Interrupt |
| DW0_CH_STRUCT114_INTR_SET | 0x40289C94 | FULL | Interrupt set |
| DW0_CH_STRUCT114_INTR_MASK | 0x40289C98 | FULL | Interrupt mask |
| DW0_CH_STRUCT114_INTR_MASKED | 0x40289C9C | FULL | Interrupt masked |
| DW0_CH_STRUCT114_SRAM_DATA0 | 0x40289CA0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT114_SRAM_DATA1 | 0x40289CA4 | FULL | SRAM data 1 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT114_TR_CMD | 0x40289CA8 | FULL | Channel software trigger |

### 8.1.1.116 CH_STRUCT 115

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT115_CH_CTL | 0x40289CC0 | FULL | Channel control |
| DW0_CH_STRUCT115_CH_STATUS | 0x40289CC4 | FULL | Channel status |
| DW0_CH_STRUCT115_CH_IDX | 0x40289CC8 | FULL | Channel current indices |
| DW0_CH_STRUCT115_CH_CURR_PTR | 0x40289CCC | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT115_INTR | 0x40289CD0 | FULL | Interrupt |
| DW0_CH_STRUCT115_INTR_SET | 0x40289CD4 | FULL | Interrupt set |
| DW0_CH_STRUCT115_INTR_MASK | 0x40289CD8 | FULL | Interrupt mask |
| DW0_CH_STRUCT115_INTR_MASKED | 0x40289CDC | FULL | Interrupt masked |
| DW0_CH_STRUCT115_SRAM_DATA0 | 0x40289CE0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT115_SRAM_DATA1 | 0x40289CE4 | FULL | SRAM data 1 |
| DW0_CH_STRUCT115_TR_CMD | 0x40289CE8 | FULL | Channel software trigger |

### 8.1.1.117 CH_STRUCT 116

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT116_CH_CTL | 0x40289D00 | FULL | Channel control |
| DW0_CH_STRUCT116_CH_STATUS | 0x40289D04 | FULL | Channel status |
| DW0_CH_STRUCT116_CH_IDX | 0x40289D08 | FULL | Channel current indices |
| DW0_CH_STRUCT116_CH_CURR_PTR | 0x40289D0C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT116_INTR | 0x40289D10 | FULL | Interrupt |
| DW0_CH_STRUCT116_INTR_SET | 0x40289D14 | FULL | Interrupt set |
| DW0_CH_STRUCT116_INTR_MASK | 0x40289D18 | FULL | Interrupt mask |
| DW0_CH_STRUCT116_INTR_MASKED | 0x40289D1C | FULL | Interrupt masked |
| DW0_CH_STRUCT116_SRAM_DATA0 | 0x40289D20 | FULL | SRAM data 0 |
| DW0_CH_STRUCT116_SRAM_DATA1 | 0x40289D24 | FULL | SRAM data 1 |
| DW0_CH_STRUCT116_TR_CMD | 0x40289D28 | FULL | Channel software trigger |

### 8.1.1.118 CH_STRUCT 117

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT117_CH_CTL | 0x40289D40 | FULL | Channel control |
| DW0_CH_STRUCT117_CH_STATUS | 0x40289D44 | FULL | Channel status |
| DW0_CH_STRUCT117_CH_IDX | 0x40289D48 | FULL | Channel current indices |
| DW0_CH_STRUCT117_CH_CURR_PTR | 0x40289D4C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT117_INTR | 0x40289D50 | FULL | Interrupt |
| DW0_CH_STRUCT117_INTR_SET | 0x40289D54 | FULL | Interrupt set |
| DW0_CH_STRUCT117_INTR_MASK | 0x40289D58 | FULL | Interrupt mask |
| DW0_CH_STRUCT117_INTR_MASKED | 0x40289D5C | FULL | Interrupt masked |
| DW0_CH_STRUCT117_SRAM_DATA0 | 0x40289D60 | FULL | SRAM data 0 |
| DW0_CH_STRUCT117_SRAM_DATA1 | 0x40289D64 | FULL | SRAM data 1 |
| DW0_CH_STRUCT117_TR_CMD | 0x40289D68 | FULL | Channel software trigger |

### 8.1.1.119 CH_STRUCT 118

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT118_CH_CTL | 0x40289D80 | FULL | Channel control |
| DW0_CH_STRUCT118_CH_STATUS | 0x40289D84 | FULL | Channel status |
| DW0_CH_STRUCT118_CH_IDX | 0x40289D88 | FULL | Channel current indices |
| DW0_CH_STRUCT118_CH_CURR_PTR | 0x40289D8C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT118_INTR | 0x40289D90 | FULL | Interrupt |
| DW0_CH_STRUCT118_INTR_SET | 0x40289D94 | FULL | Interrupt set |
| DW0_CH_STRUCT118_INTR_MASK | 0x40289D98 | FULL | Interrupt mask |
| DW0_CH_STRUCT118_INTR_MASKED | 0x40289D9C | FULL | Interrupt masked |
| DW0_CH_STRUCT118_SRAM_DATA0 | 0x40289DA0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT118_SRAM_DATA1 | 0x40289DA4 | FULL | SRAM data 1 |
| DW0_CH_STRUCT118_TR_CMD | 0x40289DA8 | FULL | Channel software trigger |

### 8.1.1.120 CH_STRUCT 119

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT119_CH_CTL | 0x40289DC0 | FULL | Channel control |
| DW0_CH_STRUCT119_CH_STATUS | 0x40289DC4 | FULL | Channel status |
| DW0_CH_STRUCT119_CH_IDX | 0x40289DC8 | FULL | Channel current indices |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT119_CH_CURR_PTR | 0x40289DCC | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT119_INTR | 0x40289DD0 | FULL | Interrupt |
| DW0_CH_STRUCT119_INTR_SET | 0x40289DD4 | FULL | Interrupt set |
| DW0_CH_STRUCT119_INTR_MASK | 0x40289DD8 | FULL | Interrupt mask |
| DW0_CH_STRUCT119_INTR_MASKED | 0x40289DDC | FULL | Interrupt masked |
| DW0_CH_STRUCT119_SRAM_DATA0 | 0x40289DE0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT119_SRAM_DATA1 | 0x40289DE4 | FULL | SRAM data 1 |
| DW0_CH_STRUCT119_TR_CMD | 0x40289DE8 | FULL | Channel software trigger |

### 8.1.1.121 CH_STRUCT 120

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT120_CH_CTL | 0x40289E00 | FULL | Channel control |
| DW0_CH_STRUCT120_CH_STATUS | 0x40289E04 | FULL | Channel status |
| DW0_CH_STRUCT120_CH_IDX | 0x40289E08 | FULL | Channel current indices |
| DW0_CH_STRUCT120_CH_CURR_PTR | 0x40289E0C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT120_INTR | 0x40289E10 | FULL | Interrupt |
| DW0_CH_STRUCT120_INTR_SET | 0x40289E14 | FULL | Interrupt set |
| DW0_CH_STRUCT120_INTR_MASK | 0x40289E18 | FULL | Interrupt mask |
| DW0_CH_STRUCT120_INTR_MASKED | 0x40289E1C | FULL | Interrupt masked |
| DW0_CH_STRUCT120_SRAM_DATA0 | 0x40289E20 | FULL | SRAM data 0 |
| DW0_CH_STRUCT120_SRAM_DATA1 | 0x40289E24 | FULL | SRAM data 1 |
| DW0_CH_STRUCT120_TR_CMD | 0x40289E28 | FULL | Channel software trigger |

### 8.1.1.122 CH_STRUCT 121

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT121_CH_CTL | 0x40289E40 | FULL | Channel control |
| DW0_CH_STRUCT121_CH_STATUS | 0x40289E44 | FULL | Channel status |
| DW0_CH_STRUCT121_CH_IDX | 0x40289E48 | FULL | Channel current indices |
| DW0_CH_STRUCT121_CH_CURR_PTR | 0x40289E4C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT121_INTR | 0x40289E50 | FULL | Interrupt |
| DW0_CH_STRUCT121_INTR_SET | 0x40289E54 | FULL | Interrupt set |
| DW0_CH_STRUCT121_INTR_MASK | 0x40289E58 | FULL | Interrupt mask |
| DW0_CH_STRUCT121_INTR_MASKED | 0x40289E5C | FULL | Interrupt masked |
| DW0_CH_STRUCT121_SRAM_DATA0 | 0x40289E60 | FULL | SRAM data 0 |
| DW0_CH_STRUCT121_SRAM_DATA1 | 0x40289E64 | FULL | SRAM data 1 |
| DW0_CH_STRUCT121_TR_CMD | 0x40289E68 | FULL | Channel software trigger |

### 8.1.1.123 CH_STRUCT 122

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT122_CH_CTL | 0x40289E80 | FULL | Channel control |
| DW0_CH_STRUCT122_CH_STATUS | 0x40289E84 | FULL | Channel status |
| DW0_CH_STRUCT122_CH_IDX | 0x40289E88 | FULL | Channel current indices |
| DW0_CH_STRUCT122_CH_CURR_PTR | 0x40289E8C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT122_INTR | 0x40289E90 | FULL | Interrupt |
| DW0_CH_STRUCT122_INTR_SET | 0x40289E94 | FULL | Interrupt set |
| DW0_CH_STRUCT122_INTR_MASK | 0x40289E98 | FULL | Interrupt mask |
| DW0_CH_STRUCT122_INTR_MASKED | 0x40289E9C | FULL | Interrupt masked |
| DW0_CH_STRUCT122_SRAM_DATA0 | 0x40289EA0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT122_SRAM_DATA1 | 0x40289EA4 | FULL | SRAM data 1 |
| DW0_CH_STRUCT122_TR_CMD | 0x40289EA8 | FULL | Channel software trigger |

### 8.1.1.124 CH_STRUCT 123

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT123_CH_CTL | 0x40289EC0 | FULL | Channel control |
| DW0_CH_STRUCT123_CH_STATUS | 0x40289EC4 | FULL | Channel status |
| DW0_CH_STRUCT123_CH_IDX | 0x40289EC8 | FULL | Channel current indices |
| DW0_CH_STRUCT123_CH_CURR_PTR | 0x40289ECC | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT123_INTR | 0x40289ED0 | FULL | Interrupt |
| DW0_CH_STRUCT123_INTR_SET | 0x40289ED4 | FULL | Interrupt set |
| DW0_CH_STRUCT123_INTR_MASK | 0x40289ED8 | FULL | Interrupt mask |
| DW0_CH_STRUCT123_INTR_MASKED | 0x40289EDC | FULL | Interrupt masked |
| DW0_CH_STRUCT123_SRAM_DATA0 | 0x40289EE0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT123_SRAM_DATA1 | 0x40289EE4 | FULL | SRAM data 1 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT123_TR_CMD | 0x40289EE8 | FULL | Channel software trigger |

### 8.1.1.125 CH_STRUCT 124

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT124_CH_CTL | 0x40289F00 | FULL | Channel control |
| DW0_CH_STRUCT124_CH_STATUS | 0x40289F04 | FULL | Channel status |
| DW0_CH_STRUCT124_CH_IDX | 0x40289F08 | FULL | Channel current indices |
| DW0_CH_STRUCT124_CH_CURR_PTR | 0x40289F0C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT124_INTR | 0x40289F10 | FULL | Interrupt |
| DW0_CH_STRUCT124_INTR_SET | 0x40289F14 | FULL | Interrupt set |
| DW0_CH_STRUCT124_INTR_MASK | 0x40289F18 | FULL | Interrupt mask |
| DW0_CH_STRUCT124_INTR_MASKED | 0x40289F1C | FULL | Interrupt masked |
| DW0_CH_STRUCT124_SRAM_DATA0 | 0x40289F20 | FULL | SRAM data 0 |
| DW0_CH_STRUCT124_SRAM_DATA1 | 0x40289F24 | FULL | SRAM data 1 |
| DW0_CH_STRUCT124_TR_CMD | 0x40289F28 | FULL | Channel software trigger |

### 8.1.1.126 CH_STRUCT 125

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT125_CH_CTL | 0x40289F40 | FULL | Channel control |
| DW0_CH_STRUCT125_CH_STATUS | 0x40289F44 | FULL | Channel status |
| DW0_CH_STRUCT125_CH_IDX | 0x40289F48 | FULL | Channel current indices |
| DW0_CH_STRUCT125_CH_CURR_PTR | 0x40289F4C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT125_INTR | 0x40289F50 | FULL | Interrupt |
| DW0_CH_STRUCT125_INTR_SET | 0x40289F54 | FULL | Interrupt set |
| DW0_CH_STRUCT125_INTR_MASK | 0x40289F58 | FULL | Interrupt mask |
| DW0_CH_STRUCT125_INTR_MASKED | 0x40289F5C | FULL | Interrupt masked |
| DW0_CH_STRUCT125_SRAM_DATA0 | 0x40289F60 | FULL | SRAM data 0 |
| DW0_CH_STRUCT125_SRAM_DATA1 | 0x40289F64 | FULL | SRAM data 1 |
| DW0_CH_STRUCT125_TR_CMD | 0x40289F68 | FULL | Channel software trigger |

### 8.1.1.127 CH_STRUCT 126

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT126_CH_CTL | 0x40289F80 | FULL | Channel control |
| DW0_CH_STRUCT126_CH_STATUS | 0x40289F84 | FULL | Channel status |
| DW0_CH_STRUCT126_CH_IDX | 0x40289F88 | FULL | Channel current indices |
| DW0_CH_STRUCT126_CH_CURR_PTR | 0x40289F8C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT126_INTR | 0x40289F90 | FULL | Interrupt |
| DW0_CH_STRUCT126_INTR_SET | 0x40289F94 | FULL | Interrupt set |
| DW0_CH_STRUCT126_INTR_MASK | 0x40289F98 | FULL | Interrupt mask |
| DW0_CH_STRUCT126_INTR_MASKED | 0x40289F9C | FULL | Interrupt masked |
| DW0_CH_STRUCT126_SRAM_DATA0 | 0x40289FA0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT126_SRAM_DATA1 | 0x40289FA4 | FULL | SRAM data 1 |
| DW0_CH_STRUCT126_TR_CMD | 0x40289FA8 | FULL | Channel software trigger |

### 8.1.1.128 CH_STRUCT 127

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT127_CH_CTL | 0x40289FC0 | FULL | Channel control |
| DW0_CH_STRUCT127_CH_STATUS | 0x40289FC4 | FULL | Channel status |
| DW0_CH_STRUCT127_CH_IDX | 0x40289FC8 | FULL | Channel current indices |
| DW0_CH_STRUCT127_CH_CURR_PTR | 0x40289FCC | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT127_INTR | 0x40289FD0 | FULL | Interrupt |
| DW0_CH_STRUCT127_INTR_SET | 0x40289FD4 | FULL | Interrupt set |
| DW0_CH_STRUCT127_INTR_MASK | 0x40289FD8 | FULL | Interrupt mask |
| DW0_CH_STRUCT127_INTR_MASKED | 0x40289FDC | FULL | Interrupt masked |
| DW0_CH_STRUCT127_SRAM_DATA0 | 0x40289FE0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT127_SRAM_DATA1 | 0x40289FE4 | FULL | SRAM data 1 |
| DW0_CH_STRUCT127_TR_CMD | 0x40289FE8 | FULL | Channel software trigger |

### 8.1.1.129 CH_STRUCT 128

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT128_CH_CTL | 0x4028A000 | FULL | Channel control |
| DW0_CH_STRUCT128_CH_STATUS | 0x4028A004 | FULL | Channel status |
| DW0_CH_STRUCT128_CH_IDX | 0x4028A008 | FULL | Channel current indices |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT128_CH_CURR_PTR | 0x4028A00C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT128_INTR | 0x4028A010 | FULL | Interrupt |
| DW0_CH_STRUCT128_INTR_SET | 0x4028A014 | FULL | Interrupt set |
| DW0_CH_STRUCT128_INTR_MASK | 0x4028A018 | FULL | Interrupt mask |
| DW0_CH_STRUCT128_INTR_MASKED | 0x4028A01C | FULL | Interrupt masked |
| DW0_CH_STRUCT128_SRAM_DATA0 | 0x4028A020 | FULL | SRAM data 0 |
| DW0_CH_STRUCT128_SRAM_DATA1 | 0x4028A024 | FULL | SRAM data 1 |
| DW0_CH_STRUCT128_TR_CMD | 0x4028A028 | FULL | Channel software trigger |

### 8.1.1.130 CH_STRUCT 129

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT129_CH_CTL | 0x4028A040 | FULL | Channel control |
| DW0_CH_STRUCT129_CH_STATUS | 0x4028A044 | FULL | Channel status |
| DW0_CH_STRUCT129_CH_IDX | 0x4028A048 | FULL | Channel current indices |
| DW0_CH_STRUCT129_CH_CURR_PTR | 0x4028A04C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT129_INTR | 0x4028A050 | FULL | Interrupt |
| DW0_CH_STRUCT129_INTR_SET | 0x4028A054 | FULL | Interrupt set |
| DW0_CH_STRUCT129_INTR_MASK | 0x4028A058 | FULL | Interrupt mask |
| DW0_CH_STRUCT129_INTR_MASKED | 0x4028A05C | FULL | Interrupt masked |
| DW0_CH_STRUCT129_SRAM_DATA0 | 0x4028A060 | FULL | SRAM data 0 |
| DW0_CH_STRUCT129_SRAM_DATA1 | 0x4028A064 | FULL | SRAM data 1 |
| DW0_CH_STRUCT129_TR_CMD | 0x4028A068 | FULL | Channel software trigger |

### 8.1.1.131 CH_STRUCT 130

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT130_CH_CTL | 0x4028A080 | FULL | Channel control |
| DW0_CH_STRUCT130_CH_STATUS | 0x4028A084 | FULL | Channel status |
| DW0_CH_STRUCT130_CH_IDX | 0x4028A088 | FULL | Channel current indices |
| DW0_CH_STRUCT130_CH_CURR_PTR | 0x4028A08C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT130_INTR | 0x4028A090 | FULL | Interrupt |
| DW0_CH_STRUCT130_INTR_SET | 0x4028A094 | FULL | Interrupt set |
| DW0_CH_STRUCT130_INTR_MASK | 0x4028A098 | FULL | Interrupt mask |
| DW0_CH_STRUCT130_INTR_MASKED | 0x4028A09C | FULL | Interrupt masked |
| DW0_CH_STRUCT130_SRAM_DATA0 | 0x4028A0A0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT130_SRAM_DATA1 | 0x4028A0A4 | FULL | SRAM data 1 |
| DW0_CH_STRUCT130_TR_CMD | 0x4028A0A8 | FULL | Channel software trigger |

### 8.1.1.132 CH_STRUCT 131

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT131_CH_CTL | 0x4028A0C0 | FULL | Channel control |
| DW0_CH_STRUCT131_CH_STATUS | 0x4028A0C4 | FULL | Channel status |
| DW0_CH_STRUCT131_CH_IDX | 0x4028A0C8 | FULL | Channel current indices |
| DW0_CH_STRUCT131_CH_CURR_PTR | 0x4028A0CC | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT131_INTR | 0x4028A0D0 | FULL | Interrupt |
| DW0_CH_STRUCT131_INTR_SET | 0x4028A0D4 | FULL | Interrupt set |
| DW0_CH_STRUCT131_INTR_MASK | 0x4028A0D8 | FULL | Interrupt mask |
| DW0_CH_STRUCT131_INTR_MASKED | 0x4028A0DC | FULL | Interrupt masked |
| DW0_CH_STRUCT131_SRAM_DATA0 | 0x4028A0E0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT131_SRAM_DATA1 | 0x4028A0E4 | FULL | SRAM data 1 |
| DW0_CH_STRUCT131_TR_CMD | 0x4028A0E8 | FULL | Channel software trigger |

### 8.1.1.133 CH_STRUCT 132

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT132_CH_CTL | 0x4028A100 | FULL | Channel control |
| DW0_CH_STRUCT132_CH_STATUS | 0x4028A104 | FULL | Channel status |
| DW0_CH_STRUCT132_CH_IDX | 0x4028A108 | FULL | Channel current indices |
| DW0_CH_STRUCT132_CH_CURR_PTR | 0x4028A10C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT132_INTR | 0x4028A110 | FULL | Interrupt |
| DW0_CH_STRUCT132_INTR_SET | 0x4028A114 | FULL | Interrupt set |
| DW0_CH_STRUCT132_INTR_MASK | 0x4028A118 | FULL | Interrupt mask |
| DW0_CH_STRUCT132_INTR_MASKED | 0x4028A11C | FULL | Interrupt masked |
| DW0_CH_STRUCT132_SRAM_DATA0 | 0x4028A120 | FULL | SRAM data 0 |
| DW0_CH_STRUCT132_SRAM_DATA1 | 0x4028A124 | FULL | SRAM data 1 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT132_TR_CMD | 0x4028A128 | FULL | Channel software trigger |

### 8.1.1.134 CH_STRUCT 133

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT133_CH_CTL | 0x4028A140 | FULL | Channel control |
| DW0_CH_STRUCT133_CH_STATUS | 0x4028A144 | FULL | Channel status |
| DW0_CH_STRUCT133_CH_IDX | 0x4028A148 | FULL | Channel current indices |
| DW0_CH_STRUCT133_CH_CURR_PTR | 0x4028A14C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT133_INTR | 0x4028A150 | FULL | Interrupt |
| DW0_CH_STRUCT133_INTR_SET | 0x4028A154 | FULL | Interrupt set |
| DW0_CH_STRUCT133_INTR_MASK | 0x4028A158 | FULL | Interrupt mask |
| DW0_CH_STRUCT133_INTR_MASKED | 0x4028A15C | FULL | Interrupt masked |
| DW0_CH_STRUCT133_SRAM_DATA0 | 0x4028A160 | FULL | SRAM data 0 |
| DW0_CH_STRUCT133_SRAM_DATA1 | 0x4028A164 | FULL | SRAM data 1 |
| DW0_CH_STRUCT133_TR_CMD | 0x4028A168 | FULL | Channel software trigger |

### 8.1.1.135 CH_STRUCT 134

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT134_CH_CTL | 0x4028A180 | FULL | Channel control |
| DW0_CH_STRUCT134_CH_STATUS | 0x4028A184 | FULL | Channel status |
| DW0_CH_STRUCT134_CH_IDX | 0x4028A188 | FULL | Channel current indices |
| DW0_CH_STRUCT134_CH_CURR_PTR | 0x4028A18C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT134_INTR | 0x4028A190 | FULL | Interrupt |
| DW0_CH_STRUCT134_INTR_SET | 0x4028A194 | FULL | Interrupt set |
| DW0_CH_STRUCT134_INTR_MASK | 0x4028A198 | FULL | Interrupt mask |
| DW0_CH_STRUCT134_INTR_MASKED | 0x4028A19C | FULL | Interrupt masked |
| DW0_CH_STRUCT134_SRAM_DATA0 | 0x4028A1A0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT134_SRAM_DATA1 | 0x4028A1A4 | FULL | SRAM data 1 |
| DW0_CH_STRUCT134_TR_CMD | 0x4028A1A8 | FULL | Channel software trigger |

### 8.1.1.136 CH_STRUCT 135

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT135_CH_CTL | 0x4028A1C0 | FULL | Channel control |
| DW0_CH_STRUCT135_CH_STATUS | 0x4028A1C4 | FULL | Channel status |
| DW0_CH_STRUCT135_CH_IDX | 0x4028A1C8 | FULL | Channel current indices |
| DW0_CH_STRUCT135_CH_CURR_PTR | 0x4028A1CC | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT135_INTR | 0x4028A1D0 | FULL | Interrupt |
| DW0_CH_STRUCT135_INTR_SET | 0x4028A1D4 | FULL | Interrupt set |
| DW0_CH_STRUCT135_INTR_MASK | 0x4028A1D8 | FULL | Interrupt mask |
| DW0_CH_STRUCT135_INTR_MASKED | 0x4028A1DC | FULL | Interrupt masked |
| DW0_CH_STRUCT135_SRAM_DATA0 | 0x4028A1E0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT135_SRAM_DATA1 | 0x4028A1E4 | FULL | SRAM data 1 |
| DW0_CH_STRUCT135_TR_CMD | 0x4028A1E8 | FULL | Channel software trigger |

### 8.1.1.137 CH_STRUCT 136

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT136_CH_CTL | 0x4028A200 | FULL | Channel control |
| DW0_CH_STRUCT136_CH_STATUS | 0x4028A204 | FULL | Channel status |
| DW0_CH_STRUCT136_CH_IDX | 0x4028A208 | FULL | Channel current indices |
| DW0_CH_STRUCT136_CH_CURR_PTR | 0x4028A20C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT136_INTR | 0x4028A210 | FULL | Interrupt |
| DW0_CH_STRUCT136_INTR_SET | 0x4028A214 | FULL | Interrupt set |
| DW0_CH_STRUCT136_INTR_MASK | 0x4028A218 | FULL | Interrupt mask |
| DW0_CH_STRUCT136_INTR_MASKED | 0x4028A21C | FULL | Interrupt masked |
| DW0_CH_STRUCT136_SRAM_DATA0 | 0x4028A220 | FULL | SRAM data 0 |
| DW0_CH_STRUCT136_SRAM_DATA1 | 0x4028A224 | FULL | SRAM data 1 |
| DW0_CH_STRUCT136_TR_CMD | 0x4028A228 | FULL | Channel software trigger |

### 8.1.1.138 CH_STRUCT 137

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT137_CH_CTL | 0x4028A240 | FULL | Channel control |
| DW0_CH_STRUCT137_CH_STATUS | 0x4028A244 | FULL | Channel status |
| DW0_CH_STRUCT137_CH_IDX | 0x4028A248 | FULL | Channel current indices |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT137_CH_CURR_PTR | 0x4028A24C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT137_INTR | 0x4028A250 | FULL | Interrupt |
| DW0_CH_STRUCT137_INTR_SET | 0x4028A254 | FULL | Interrupt set |
| DW0_CH_STRUCT137_INTR_MASK | 0x4028A258 | FULL | Interrupt mask |
| DW0_CH_STRUCT137_INTR_MASKED | 0x4028A25C | FULL | Interrupt masked |
| DW0_CH_STRUCT137_SRAM_DATA0 | 0x4028A260 | FULL | SRAM data 0 |
| DW0_CH_STRUCT137_SRAM_DATA1 | 0x4028A264 | FULL | SRAM data 1 |
| DW0_CH_STRUCT137_TR_CMD | 0x4028A268 | FULL | Channel software trigger |

### 8.1.1.139 CH_STRUCT 138

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT138_CH_CTL | 0x4028A280 | FULL | Channel control |
| DW0_CH_STRUCT138_CH_STATUS | 0x4028A284 | FULL | Channel status |
| DW0_CH_STRUCT138_CH_IDX | 0x4028A288 | FULL | Channel current indices |
| DW0_CH_STRUCT138_CH_CURR_PTR | 0x4028A28C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT138_INTR | 0x4028A290 | FULL | Interrupt |
| DW0_CH_STRUCT138_INTR_SET | 0x4028A294 | FULL | Interrupt set |
| DW0_CH_STRUCT138_INTR_MASK | 0x4028A298 | FULL | Interrupt mask |
| DW0_CH_STRUCT138_INTR_MASKED | 0x4028A29C | FULL | Interrupt masked |
| DW0_CH_STRUCT138_SRAM_DATA0 | 0x4028A2A0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT138_SRAM_DATA1 | 0x4028A2A4 | FULL | SRAM data 1 |
| DW0_CH_STRUCT138_TR_CMD | 0x4028A2A8 | FULL | Channel software trigger |

### 8.1.1.140 CH_STRUCT 139

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT139_CH_CTL | 0x4028A2C0 | FULL | Channel control |
| DW0_CH_STRUCT139_CH_STATUS | 0x4028A2C4 | FULL | Channel status |
| DW0_CH_STRUCT139_CH_IDX | 0x4028A2C8 | FULL | Channel current indices |
| DW0_CH_STRUCT139_CH_CURR_PTR | 0x4028A2CC | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT139_INTR | 0x4028A2D0 | FULL | Interrupt |
| DW0_CH_STRUCT139_INTR_SET | 0x4028A2D4 | FULL | Interrupt set |
| DW0_CH_STRUCT139_INTR_MASK | 0x4028A2D8 | FULL | Interrupt mask |
| DW0_CH_STRUCT139_INTR_MASKED | 0x4028A2DC | FULL | Interrupt masked |
| DW0_CH_STRUCT139_SRAM_DATA0 | 0x4028A2E0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT139_SRAM_DATA1 | 0x4028A2E4 | FULL | SRAM data 1 |
| DW0_CH_STRUCT139_TR_CMD | 0x4028A2E8 | FULL | Channel software trigger |

### 8.1.1.141 CH_STRUCT 140

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT140_CH_CTL | 0x4028A300 | FULL | Channel control |
| DW0_CH_STRUCT140_CH_STATUS | 0x4028A304 | FULL | Channel status |
| DW0_CH_STRUCT140_CH_IDX | 0x4028A308 | FULL | Channel current indices |
| DW0_CH_STRUCT140_CH_CURR_PTR | 0x4028A30C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT140_INTR | 0x4028A310 | FULL | Interrupt |
| DW0_CH_STRUCT140_INTR_SET | 0x4028A314 | FULL | Interrupt set |
| DW0_CH_STRUCT140_INTR_MASK | 0x4028A318 | FULL | Interrupt mask |
| DW0_CH_STRUCT140_INTR_MASKED | 0x4028A31C | FULL | Interrupt masked |
| DW0_CH_STRUCT140_SRAM_DATA0 | 0x4028A320 | FULL | SRAM data 0 |
| DW0_CH_STRUCT140_SRAM_DATA1 | 0x4028A324 | FULL | SRAM data 1 |
| DW0_CH_STRUCT140_TR_CMD | 0x4028A328 | FULL | Channel software trigger |

### 8.1.1.142 CH_STRUCT 141

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT141_CH_CTL | 0x4028A340 | FULL | Channel control |
| DW0_CH_STRUCT141_CH_STATUS | 0x4028A344 | FULL | Channel status |
| DW0_CH_STRUCT141_CH_IDX | 0x4028A348 | FULL | Channel current indices |
| DW0_CH_STRUCT141_CH_CURR_PTR | 0x4028A34C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT141_INTR | 0x4028A350 | FULL | Interrupt |
| DW0_CH_STRUCT141_INTR_SET | 0x4028A354 | FULL | Interrupt set |
| DW0_CH_STRUCT141_INTR_MASK | 0x4028A358 | FULL | Interrupt mask |
| DW0_CH_STRUCT141_INTR_MASKED | 0x4028A35C | FULL | Interrupt masked |
| DW0_CH_STRUCT141_SRAM_DATA0 | 0x4028A360 | FULL | SRAM data 0 |
| DW0_CH_STRUCT141_SRAM_DATA1 | 0x4028A364 | FULL | SRAM data 1 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT141_TR_CMD | 0x4028A368 | FULL | Channel software trigger |

#### 8.1.1.143 CH_STRUCT 142

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW0_CH_STRUCT142_CH_CTL | 0x4028A380 | FULL | Channel control |
| DW0_CH_STRUCT142_CH_STATUS | 0x4028A384 | FULL | Channel status |
| DW0_CH_STRUCT142_CH_IDX | 0x4028A388 | FULL | Channel current indices |
| DW0_CH_STRUCT142_CH_CURR_PTR | 0x4028A38C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT142_INTR | 0x4028A390 | FULL | Interrupt |
| DW0_CH_STRUCT142_INTR_SET | 0x4028A394 | FULL | Interrupt set |
| DW0_CH_STRUCT142_INTR_MASK | 0x4028A398 | FULL | Interrupt mask |
| DW0_CH_STRUCT142_INTR_MASKED | 0x4028A39C | FULL | Interrupt masked |
| DW0_CH_STRUCT142_SRAM_DATA0 | 0x4028A3A0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT142_SRAM_DATA1 | 0x4028A3A4 | FULL | SRAM data 1 |
| DW0_CH_STRUCT142_TR_CMD | 0x4028A3A8 | FULL | Channel software trigger |

## 8.2 DW 1

**Description** Datawire Controller
**Base Address** 0x40290000
**Size** 0x10000
**Slave Num** MMIO2 - 8

### 8.2.1 0

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW1_CTL0 | 0x40290000 | FULL | Control |
| DW1_STATUS0 | 0x40290004 | FULL | Status |
| DW1_ACT_DESCR_CTL0 | 0x40290020 | FULL | Active descriptor control |
| DW1_ACT_DESCR_SRC0 | 0x40290024 | FULL | Active descriptor source |
| DW1_ACT_DESCR_DST0 | 0x40290028 | FULL | Active descriptor destination |
| DW1_ACT_DESCR_X_CTL0 | 0x40290030 | FULL | Active descriptor X loop control |
| DW1_ACT_DESCR_Y_CTL0 | 0x40290034 | FULL | Active descriptor Y loop control |
| DW1_ACT_DESCR_NEXT_PTR0 | 0x40290038 | FULL | Active descriptor next pointer |
| DW1_ACT_SRC0 | 0x40290040 | FULL | Active source |
| DW1_ACT_DST0 | 0x40290044 | FULL | Active destination |
| DW1_ECC_CTL0 | 0x40290080 | FULL | ECC control |
| DW1_CRC_CTL0 | 0x40290100 | FULL | CRC control |
| DW1_CRC_DATA_CTL0 | 0x40290110 | FULL | CRC data control |
| DW1_CRC_POL_CTL0 | 0x40290120 | FULL | CRC polynomial control |
| DW1_CRC_LFSR_CTL0 | 0x40290130 | FULL | CRC LFSR control |
| DW1_CRC_REM_CTL0 | 0x40290140 | FULL | CRC remainder control |
| DW1_CRC_REM_RESULT0 | 0x40290148 | FULL | CRC remainder result |

#### 8.2.1.1 CH_STRUCT 0

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW1_CH_STRUCT0_CH_CTL | 0x40298000 | FULL | Channel control |
| DW1_CH_STRUCT0_CH_STATUS | 0x40298004 | FULL | Channel status |
| DW1_CH_STRUCT0_CH_IDX | 0x40298008 | FULL | Channel current indices |
| DW1_CH_STRUCT0_CH_CURR_PTR | 0x4029800C | FULL | Channel current descriptor pointer |
| DW1_CH_STRUCT0_INTR | 0x40298010 | FULL | Interrupt |
| DW1_CH_STRUCT0_INTR_SET | 0x40298014 | FULL | Interrupt set |
| DW1_CH_STRUCT0_INTR_MASK | 0x40298018 | FULL | Interrupt mask |
| DW1_CH_STRUCT0_INTR_MASKED | 0x4029801C | FULL | Interrupt masked |
| DW1_CH_STRUCT0_SRAM_DATA0 | 0x40298020 | FULL | SRAM data 0 |
| DW1_CH_STRUCT0_SRAM_DATA1 | 0x40298024 | FULL | SRAM data 1 |
| DW1_CH_STRUCT0_TR_CMD | 0x40298028 | FULL | Channel software trigger |

#### 8.2.1.2 CH_STRUCT 1

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW1_CH_STRUCT1_CH_CTL | 0x40298040 | FULL | Channel control |
| DW1_CH_STRUCT1_CH_STATUS | 0x40298044 | FULL | Channel status |
| DW1_CH_STRUCT1_CH_IDX | 0x40298048 | FULL | Channel current indices |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW1_CH_STRUCT1_CH_CURR_PTR | 0x4029804C | FULL | Channel current descriptor pointer |
| DW1_CH_STRUCT1_INTR | 0x40298050 | FULL | Interrupt |
| DW1_CH_STRUCT1_INTR_SET | 0x40298054 | FULL | Interrupt set |
| DW1_CH_STRUCT1_INTR_MASK | 0x40298058 | FULL | Interrupt mask |
| DW1_CH_STRUCT1_INTR_MASKED | 0x4029805C | FULL | Interrupt masked |
| DW1_CH_STRUCT1_SRAM_DATA0 | 0x40298060 | FULL | SRAM data 0 |
| DW1_CH_STRUCT1_SRAM_DATA1 | 0x40298064 | FULL | SRAM data 1 |
| DW1_CH_STRUCT1_TR_CMD | 0x40298068 | FULL | Channel software trigger |

### 8.2.1.3 CH_STRUCT 2

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW1_CH_STRUCT2_CH_CTL | 0x40298080 | FULL | Channel control |
| DW1_CH_STRUCT2_CH_STATUS | 0x40298084 | FULL | Channel status |
| DW1_CH_STRUCT2_CH_IDX | 0x40298088 | FULL | Channel current indices |
| DW1_CH_STRUCT2_CH_CURR_PTR | 0x4029808C | FULL | Channel current descriptor pointer |
| DW1_CH_STRUCT2_INTR | 0x40298090 | FULL | Interrupt |
| DW1_CH_STRUCT2_INTR_SET | 0x40298094 | FULL | Interrupt set |
| DW1_CH_STRUCT2_INTR_MASK | 0x40298098 | FULL | Interrupt mask |
| DW1_CH_STRUCT2_INTR_MASKED | 0x4029809C | FULL | Interrupt masked |
| DW1_CH_STRUCT2_SRAM_DATA0 | 0x402980A0 | FULL | SRAM data 0 |
| DW1_CH_STRUCT2_SRAM_DATA1 | 0x402980A4 | FULL | SRAM data 1 |
| DW1_CH_STRUCT2_TR_CMD | 0x402980A8 | FULL | Channel software trigger |

### 8.2.1.4 CH_STRUCT 3

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW1_CH_STRUCT3_CH_CTL | 0x402980C0 | FULL | Channel control |
| DW1_CH_STRUCT3_CH_STATUS | 0x402980C4 | FULL | Channel status |
| DW1_CH_STRUCT3_CH_IDX | 0x402980C8 | FULL | Channel current indices |
| DW1_CH_STRUCT3_CH_CURR_PTR | 0x402980CC | FULL | Channel current descriptor pointer |
| DW1_CH_STRUCT3_INTR | 0x402980D0 | FULL | Interrupt |
| DW1_CH_STRUCT3_INTR_SET | 0x402980D4 | FULL | Interrupt set |
| DW1_CH_STRUCT3_INTR_MASK | 0x402980D8 | FULL | Interrupt mask |
| DW1_CH_STRUCT3_INTR_MASKED | 0x402980DC | FULL | Interrupt masked |
| DW1_CH_STRUCT3_SRAM_DATA0 | 0x402980E0 | FULL | SRAM data 0 |
| DW1_CH_STRUCT3_SRAM_DATA1 | 0x402980E4 | FULL | SRAM data 1 |
| DW1_CH_STRUCT3_TR_CMD | 0x402980E8 | FULL | Channel software trigger |

### 8.2.1.5 CH_STRUCT 4

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW1_CH_STRUCT4_CH_CTL | 0x40298100 | FULL | Channel control |
| DW1_CH_STRUCT4_CH_STATUS | 0x40298104 | FULL | Channel status |
| DW1_CH_STRUCT4_CH_IDX | 0x40298108 | FULL | Channel current indices |
| DW1_CH_STRUCT4_CH_CURR_PTR | 0x4029810C | FULL | Channel current descriptor pointer |
| DW1_CH_STRUCT4_INTR | 0x40298110 | FULL | Interrupt |
| DW1_CH_STRUCT4_INTR_SET | 0x40298114 | FULL | Interrupt set |
| DW1_CH_STRUCT4_INTR_MASK | 0x40298118 | FULL | Interrupt mask |
| DW1_CH_STRUCT4_INTR_MASKED | 0x4029811C | FULL | Interrupt masked |
| DW1_CH_STRUCT4_SRAM_DATA0 | 0x40298120 | FULL | SRAM data 0 |
| DW1_CH_STRUCT4_SRAM_DATA1 | 0x40298124 | FULL | SRAM data 1 |
| DW1_CH_STRUCT4_TR_CMD | 0x40298128 | FULL | Channel software trigger |

### 8.2.1.6 CH_STRUCT 5

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW1_CH_STRUCT5_CH_CTL | 0x40298140 | FULL | Channel control |
| DW1_CH_STRUCT5_CH_STATUS | 0x40298144 | FULL | Channel status |
| DW1_CH_STRUCT5_CH_IDX | 0x40298148 | FULL | Channel current indices |
| DW1_CH_STRUCT5_CH_CURR_PTR | 0x4029814C | FULL | Channel current descriptor pointer |
| DW1_CH_STRUCT5_INTR | 0x40298150 | FULL | Interrupt |
| DW1_CH_STRUCT5_INTR_SET | 0x40298154 | FULL | Interrupt set |
| DW1_CH_STRUCT5_INTR_MASK | 0x40298158 | FULL | Interrupt mask |
| DW1_CH_STRUCT5_INTR_MASKED | 0x4029815C | FULL | Interrupt masked |
| DW1_CH_STRUCT5_SRAM_DATA0 | 0x40298160 | FULL | SRAM data 0 |
| DW1_CH_STRUCT5_SRAM_DATA1 | 0x40298164 | FULL | SRAM data 1 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW1_CH_STRUCT5_TR_CMD | 0x40298168 | FULL | Channel software trigger |

### 8.2.1.7 CH_STRUCT 6

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW1_CH_STRUCT6_CH_CTL | 0x40298180 | FULL | Channel control |
| DW1_CH_STRUCT6_CH_STATUS | 0x40298184 | FULL | Channel status |
| DW1_CH_STRUCT6_CH_IDX | 0x40298188 | FULL | Channel current indices |
| DW1_CH_STRUCT6_CH_CURR_PTR | 0x4029818C | FULL | Channel current descriptor pointer |
| DW1_CH_STRUCT6_INTR | 0x40298190 | FULL | Interrupt |
| DW1_CH_STRUCT6_INTR_SET | 0x40298194 | FULL | Interrupt set |
| DW1_CH_STRUCT6_INTR_MASK | 0x40298198 | FULL | Interrupt mask |
| DW1_CH_STRUCT6_INTR_MASKED | 0x4029819C | FULL | Interrupt masked |
| DW1_CH_STRUCT6_SRAM_DATA0 | 0x402981A0 | FULL | SRAM data 0 |
| DW1_CH_STRUCT6_SRAM_DATA1 | 0x402981A4 | FULL | SRAM data 1 |
| DW1_CH_STRUCT6_TR_CMD | 0x402981A8 | FULL | Channel software trigger |

### 8.2.1.8 CH_STRUCT 7

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW1_CH_STRUCT7_CH_CTL | 0x402981C0 | FULL | Channel control |
| DW1_CH_STRUCT7_CH_STATUS | 0x402981C4 | FULL | Channel status |
| DW1_CH_STRUCT7_CH_IDX | 0x402981C8 | FULL | Channel current indices |
| DW1_CH_STRUCT7_CH_CURR_PTR | 0x402981CC | FULL | Channel current descriptor pointer |
| DW1_CH_STRUCT7_INTR | 0x402981D0 | FULL | Interrupt |
| DW1_CH_STRUCT7_INTR_SET | 0x402981D4 | FULL | Interrupt set |
| DW1_CH_STRUCT7_INTR_MASK | 0x402981D8 | FULL | Interrupt mask |
| DW1_CH_STRUCT7_INTR_MASKED | 0x402981DC | FULL | Interrupt masked |
| DW1_CH_STRUCT7_SRAM_DATA0 | 0x402981E0 | FULL | SRAM data 0 |
| DW1_CH_STRUCT7_SRAM_DATA1 | 0x402981E4 | FULL | SRAM data 1 |
| DW1_CH_STRUCT7_TR_CMD | 0x402981E8 | FULL | Channel software trigger |

### 8.2.1.9 CH_STRUCT 8

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW1_CH_STRUCT8_CH_CTL | 0x40298200 | FULL | Channel control |
| DW1_CH_STRUCT8_CH_STATUS | 0x40298204 | FULL | Channel status |
| DW1_CH_STRUCT8_CH_IDX | 0x40298208 | FULL | Channel current indices |
| DW1_CH_STRUCT8_CH_CURR_PTR | 0x4029820C | FULL | Channel current descriptor pointer |
| DW1_CH_STRUCT8_INTR | 0x40298210 | FULL | Interrupt |
| DW1_CH_STRUCT8_INTR_SET | 0x40298214 | FULL | Interrupt set |
| DW1_CH_STRUCT8_INTR_MASK | 0x40298218 | FULL | Interrupt mask |
| DW1_CH_STRUCT8_INTR_MASKED | 0x4029821C | FULL | Interrupt masked |
| DW1_CH_STRUCT8_SRAM_DATA0 | 0x40298220 | FULL | SRAM data 0 |
| DW1_CH_STRUCT8_SRAM_DATA1 | 0x40298224 | FULL | SRAM data 1 |
| DW1_CH_STRUCT8_TR_CMD | 0x40298228 | FULL | Channel software trigger |

### 8.2.1.10 CH_STRUCT 9

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW1_CH_STRUCT9_CH_CTL | 0x40298240 | FULL | Channel control |
| DW1_CH_STRUCT9_CH_STATUS | 0x40298244 | FULL | Channel status |
| DW1_CH_STRUCT9_CH_IDX | 0x40298248 | FULL | Channel current indices |
| DW1_CH_STRUCT9_CH_CURR_PTR | 0x4029824C | FULL | Channel current descriptor pointer |
| DW1_CH_STRUCT9_INTR | 0x40298250 | FULL | Interrupt |
| DW1_CH_STRUCT9_INTR_SET | 0x40298254 | FULL | Interrupt set |
| DW1_CH_STRUCT9_INTR_MASK | 0x40298258 | FULL | Interrupt mask |
| DW1_CH_STRUCT9_INTR_MASKED | 0x4029825C | FULL | Interrupt masked |
| DW1_CH_STRUCT9_SRAM_DATA0 | 0x40298260 | FULL | SRAM data 0 |
| DW1_CH_STRUCT9_SRAM_DATA1 | 0x40298264 | FULL | SRAM data 1 |
| DW1_CH_STRUCT9_TR_CMD | 0x40298268 | FULL | Channel software trigger |

### 8.2.1.11 CH_STRUCT 10

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW1_CH_STRUCT10_CH_CTL | 0x40298280 | FULL | Channel control |
| DW1_CH_STRUCT10_CH_STATUS | 0x40298284 | FULL | Channel status |
| DW1_CH_STRUCT10_CH_IDX | 0x40298288 | FULL | Channel current indices |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW1_CH_STRUCT10_CH_CURR_PTR | 0x4029828C | FULL | Channel current descriptor pointer |
| DW1_CH_STRUCT10_INTR | 0x40298290 | FULL | Interrupt |
| DW1_CH_STRUCT10_INTR_SET | 0x40298294 | FULL | Interrupt set |
| DW1_CH_STRUCT10_INTR_MASK | 0x40298298 | FULL | Interrupt mask |
| DW1_CH_STRUCT10_INTR_MASKED | 0x4029829C | FULL | Interrupt masked |
| DW1_CH_STRUCT10_SRAM_DATA0 | 0x402982A0 | FULL | SRAM data 0 |
| DW1_CH_STRUCT10_SRAM_DATA1 | 0x402982A4 | FULL | SRAM data 1 |
| DW1_CH_STRUCT10_TR_CMD | 0x402982A8 | FULL | Channel software trigger |

### 8.2.1.12 CH_STRUCT 11

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW1_CH_STRUCT11_CH_CTL | 0x402982C0 | FULL | Channel control |
| DW1_CH_STRUCT11_CH_STATUS | 0x402982C4 | FULL | Channel status |
| DW1_CH_STRUCT11_CH_IDX | 0x402982C8 | FULL | Channel current indices |
| DW1_CH_STRUCT11_CH_CURR_PTR | 0x402982CC | FULL | Channel current descriptor pointer |
| DW1_CH_STRUCT11_INTR | 0x402982D0 | FULL | Interrupt |
| DW1_CH_STRUCT11_INTR_SET | 0x402982D4 | FULL | Interrupt set |
| DW1_CH_STRUCT11_INTR_MASK | 0x402982D8 | FULL | Interrupt mask |
| DW1_CH_STRUCT11_INTR_MASKED | 0x402982DC | FULL | Interrupt masked |
| DW1_CH_STRUCT11_SRAM_DATA0 | 0x402982E0 | FULL | SRAM data 0 |
| DW1_CH_STRUCT11_SRAM_DATA1 | 0x402982E4 | FULL | SRAM data 1 |
| DW1_CH_STRUCT11_TR_CMD | 0x402982E8 | FULL | Channel software trigger |

### 8.2.1.13 CH_STRUCT 12

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW1_CH_STRUCT12_CH_CTL | 0x40298300 | FULL | Channel control |
| DW1_CH_STRUCT12_CH_STATUS | 0x40298304 | FULL | Channel status |
| DW1_CH_STRUCT12_CH_IDX | 0x40298308 | FULL | Channel current indices |
| DW1_CH_STRUCT12_CH_CURR_PTR | 0x4029830C | FULL | Channel current descriptor pointer |
| DW1_CH_STRUCT12_INTR | 0x40298310 | FULL | Interrupt |
| DW1_CH_STRUCT12_INTR_SET | 0x40298314 | FULL | Interrupt set |
| DW1_CH_STRUCT12_INTR_MASK | 0x40298318 | FULL | Interrupt mask |
| DW1_CH_STRUCT12_INTR_MASKED | 0x4029831C | FULL | Interrupt masked |
| DW1_CH_STRUCT12_SRAM_DATA0 | 0x40298320 | FULL | SRAM data 0 |
| DW1_CH_STRUCT12_SRAM_DATA1 | 0x40298324 | FULL | SRAM data 1 |
| DW1_CH_STRUCT12_TR_CMD | 0x40298328 | FULL | Channel software trigger |

### 8.2.1.14 CH_STRUCT 13

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW1_CH_STRUCT13_CH_CTL | 0x40298340 | FULL | Channel control |
| DW1_CH_STRUCT13_CH_STATUS | 0x40298344 | FULL | Channel status |
| DW1_CH_STRUCT13_CH_IDX | 0x40298348 | FULL | Channel current indices |
| DW1_CH_STRUCT13_CH_CURR_PTR | 0x4029834C | FULL | Channel current descriptor pointer |
| DW1_CH_STRUCT13_INTR | 0x40298350 | FULL | Interrupt |
| DW1_CH_STRUCT13_INTR_SET | 0x40298354 | FULL | Interrupt set |
| DW1_CH_STRUCT13_INTR_MASK | 0x40298358 | FULL | Interrupt mask |
| DW1_CH_STRUCT13_INTR_MASKED | 0x4029835C | FULL | Interrupt masked |
| DW1_CH_STRUCT13_SRAM_DATA0 | 0x40298360 | FULL | SRAM data 0 |
| DW1_CH_STRUCT13_SRAM_DATA1 | 0x40298364 | FULL | SRAM data 1 |
| DW1_CH_STRUCT13_TR_CMD | 0x40298368 | FULL | Channel software trigger |

### 8.2.1.15 CH_STRUCT 14

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW1_CH_STRUCT14_CH_CTL | 0x40298380 | FULL | Channel control |
| DW1_CH_STRUCT14_CH_STATUS | 0x40298384 | FULL | Channel status |
| DW1_CH_STRUCT14_CH_IDX | 0x40298388 | FULL | Channel current indices |
| DW1_CH_STRUCT14_CH_CURR_PTR | 0x4029838C | FULL | Channel current descriptor pointer |
| DW1_CH_STRUCT14_INTR | 0x40298390 | FULL | Interrupt |
| DW1_CH_STRUCT14_INTR_SET | 0x40298394 | FULL | Interrupt set |
| DW1_CH_STRUCT14_INTR_MASK | 0x40298398 | FULL | Interrupt mask |
| DW1_CH_STRUCT14_INTR_MASKED | 0x4029839C | FULL | Interrupt masked |
| DW1_CH_STRUCT14_SRAM_DATA0 | 0x402983A0 | FULL | SRAM data 0 |
| DW1_CH_STRUCT14_SRAM_DATA1 | 0x402983A4 | FULL | SRAM data 1 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW1_CH_STRUCT14_TR_CMD | 0x402983A8 | FULL | Channel software trigger |

### 8.2.1.16 CH_STRUCT 15

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW1_CH_STRUCT15_CH_CTL | 0x402983C0 | FULL | Channel control |
| DW1_CH_STRUCT15_CH_STATUS | 0x402983C4 | FULL | Channel status |
| DW1_CH_STRUCT15_CH_IDX | 0x402983C8 | FULL | Channel current indices |
| DW1_CH_STRUCT15_CH_CURR_PTR | 0x402983CC | FULL | Channel current descriptor pointer |
| DW1_CH_STRUCT15_INTR | 0x402983D0 | FULL | Interrupt |
| DW1_CH_STRUCT15_INTR_SET | 0x402983D4 | FULL | Interrupt set |
| DW1_CH_STRUCT15_INTR_MASK | 0x402983D8 | FULL | Interrupt mask |
| DW1_CH_STRUCT15_INTR_MASKED | 0x402983DC | FULL | Interrupt masked |
| DW1_CH_STRUCT15_SRAM_DATA0 | 0x402983E0 | FULL | SRAM data 0 |
| DW1_CH_STRUCT15_SRAM_DATA1 | 0x402983E4 | FULL | SRAM data 1 |
| DW1_CH_STRUCT15_TR_CMD | 0x402983E8 | FULL | Channel software trigger |

### 8.2.1.17 CH_STRUCT 16

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW1_CH_STRUCT16_CH_CTL | 0x40298400 | FULL | Channel control |
| DW1_CH_STRUCT16_CH_STATUS | 0x40298404 | FULL | Channel status |
| DW1_CH_STRUCT16_CH_IDX | 0x40298408 | FULL | Channel current indices |
| DW1_CH_STRUCT16_CH_CURR_PTR | 0x4029840C | FULL | Channel current descriptor pointer |
| DW1_CH_STRUCT16_INTR | 0x40298410 | FULL | Interrupt |
| DW1_CH_STRUCT16_INTR_SET | 0x40298414 | FULL | Interrupt set |
| DW1_CH_STRUCT16_INTR_MASK | 0x40298418 | FULL | Interrupt mask |
| DW1_CH_STRUCT16_INTR_MASKED | 0x4029841C | FULL | Interrupt masked |
| DW1_CH_STRUCT16_SRAM_DATA0 | 0x40298420 | FULL | SRAM data 0 |
| DW1_CH_STRUCT16_SRAM_DATA1 | 0x40298424 | FULL | SRAM data 1 |
| DW1_CH_STRUCT16_TR_CMD | 0x40298428 | FULL | Channel software trigger |

### 8.2.1.18 CH_STRUCT 17

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW1_CH_STRUCT17_CH_CTL | 0x40298440 | FULL | Channel control |
| DW1_CH_STRUCT17_CH_STATUS | 0x40298444 | FULL | Channel status |
| DW1_CH_STRUCT17_CH_IDX | 0x40298448 | FULL | Channel current indices |
| DW1_CH_STRUCT17_CH_CURR_PTR | 0x4029844C | FULL | Channel current descriptor pointer |
| DW1_CH_STRUCT17_INTR | 0x40298450 | FULL | Interrupt |
| DW1_CH_STRUCT17_INTR_SET | 0x40298454 | FULL | Interrupt set |
| DW1_CH_STRUCT17_INTR_MASK | 0x40298458 | FULL | Interrupt mask |
| DW1_CH_STRUCT17_INTR_MASKED | 0x4029845C | FULL | Interrupt masked |
| DW1_CH_STRUCT17_SRAM_DATA0 | 0x40298460 | FULL | SRAM data 0 |
| DW1_CH_STRUCT17_SRAM_DATA1 | 0x40298464 | FULL | SRAM data 1 |
| DW1_CH_STRUCT17_TR_CMD | 0x40298468 | FULL | Channel software trigger |

### 8.2.1.19 CH_STRUCT 18

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW1_CH_STRUCT18_CH_CTL | 0x40298480 | FULL | Channel control |
| DW1_CH_STRUCT18_CH_STATUS | 0x40298484 | FULL | Channel status |
| DW1_CH_STRUCT18_CH_IDX | 0x40298488 | FULL | Channel current indices |
| DW1_CH_STRUCT18_CH_CURR_PTR | 0x4029848C | FULL | Channel current descriptor pointer |
| DW1_CH_STRUCT18_INTR | 0x40298490 | FULL | Interrupt |
| DW1_CH_STRUCT18_INTR_SET | 0x40298494 | FULL | Interrupt set |
| DW1_CH_STRUCT18_INTR_MASK | 0x40298498 | FULL | Interrupt mask |
| DW1_CH_STRUCT18_INTR_MASKED | 0x4029849C | FULL | Interrupt masked |
| DW1_CH_STRUCT18_SRAM_DATA0 | 0x402984A0 | FULL | SRAM data 0 |
| DW1_CH_STRUCT18_SRAM_DATA1 | 0x402984A4 | FULL | SRAM data 1 |
| DW1_CH_STRUCT18_TR_CMD | 0x402984A8 | FULL | Channel software trigger |

### 8.2.1.20 CH_STRUCT 19

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW1_CH_STRUCT19_CH_CTL | 0x402984C0 | FULL | Channel control |
| DW1_CH_STRUCT19_CH_STATUS | 0x402984C4 | FULL | Channel status |
| DW1_CH_STRUCT19_CH_IDX | 0x402984C8 | FULL | Channel current indices |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW1_CH_STRUCT19_CH_CURR_PTR | 0x402984CC | FULL | Channel current descriptor pointer |
| DW1_CH_STRUCT19_INTR | 0x402984D0 | FULL | Interrupt |
| DW1_CH_STRUCT19_INTR_SET | 0x402984D4 | FULL | Interrupt set |
| DW1_CH_STRUCT19_INTR_MASK | 0x402984D8 | FULL | Interrupt mask |
| DW1_CH_STRUCT19_INTR_MASKED | 0x402984DC | FULL | Interrupt masked |
| DW1_CH_STRUCT19_SRAM_DATA0 | 0x402984E0 | FULL | SRAM data 0 |
| DW1_CH_STRUCT19_SRAM_DATA1 | 0x402984E4 | FULL | SRAM data 1 |
| DW1_CH_STRUCT19_TR_CMD | 0x402984E8 | FULL | Channel software trigger |

### 8.2.1.21 CH_STRUCT 20

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW1_CH_STRUCT20_CH_CTL | 0x40298500 | FULL | Channel control |
| DW1_CH_STRUCT20_CH_STATUS | 0x40298504 | FULL | Channel status |
| DW1_CH_STRUCT20_CH_IDX | 0x40298508 | FULL | Channel current indices |
| DW1_CH_STRUCT20_CH_CURR_PTR | 0x4029850C | FULL | Channel current descriptor pointer |
| DW1_CH_STRUCT20_INTR | 0x40298510 | FULL | Interrupt |
| DW1_CH_STRUCT20_INTR_SET | 0x40298514 | FULL | Interrupt set |
| DW1_CH_STRUCT20_INTR_MASK | 0x40298518 | FULL | Interrupt mask |
| DW1_CH_STRUCT20_INTR_MASKED | 0x4029851C | FULL | Interrupt masked |
| DW1_CH_STRUCT20_SRAM_DATA0 | 0x40298520 | FULL | SRAM data 0 |
| DW1_CH_STRUCT20_SRAM_DATA1 | 0x40298524 | FULL | SRAM data 1 |
| DW1_CH_STRUCT20_TR_CMD | 0x40298528 | FULL | Channel software trigger |

### 8.2.1.22 CH_STRUCT 21

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW1_CH_STRUCT21_CH_CTL | 0x40298540 | FULL | Channel control |
| DW1_CH_STRUCT21_CH_STATUS | 0x40298544 | FULL | Channel status |
| DW1_CH_STRUCT21_CH_IDX | 0x40298548 | FULL | Channel current indices |
| DW1_CH_STRUCT21_CH_CURR_PTR | 0x4029854C | FULL | Channel current descriptor pointer |
| DW1_CH_STRUCT21_INTR | 0x40298550 | FULL | Interrupt |
| DW1_CH_STRUCT21_INTR_SET | 0x40298554 | FULL | Interrupt set |
| DW1_CH_STRUCT21_INTR_MASK | 0x40298558 | FULL | Interrupt mask |
| DW1_CH_STRUCT21_INTR_MASKED | 0x4029855C | FULL | Interrupt masked |
| DW1_CH_STRUCT21_SRAM_DATA0 | 0x40298560 | FULL | SRAM data 0 |
| DW1_CH_STRUCT21_SRAM_DATA1 | 0x40298564 | FULL | SRAM data 1 |
| DW1_CH_STRUCT21_TR_CMD | 0x40298568 | FULL | Channel software trigger |

### 8.2.1.23 CH_STRUCT 22

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW1_CH_STRUCT22_CH_CTL | 0x40298580 | FULL | Channel control |
| DW1_CH_STRUCT22_CH_STATUS | 0x40298584 | FULL | Channel status |
| DW1_CH_STRUCT22_CH_IDX | 0x40298588 | FULL | Channel current indices |
| DW1_CH_STRUCT22_CH_CURR_PTR | 0x4029858C | FULL | Channel current descriptor pointer |
| DW1_CH_STRUCT22_INTR | 0x40298590 | FULL | Interrupt |
| DW1_CH_STRUCT22_INTR_SET | 0x40298594 | FULL | Interrupt set |
| DW1_CH_STRUCT22_INTR_MASK | 0x40298598 | FULL | Interrupt mask |
| DW1_CH_STRUCT22_INTR_MASKED | 0x4029859C | FULL | Interrupt masked |
| DW1_CH_STRUCT22_SRAM_DATA0 | 0x402985A0 | FULL | SRAM data 0 |
| DW1_CH_STRUCT22_SRAM_DATA1 | 0x402985A4 | FULL | SRAM data 1 |
| DW1_CH_STRUCT22_TR_CMD | 0x402985A8 | FULL | Channel software trigger |

### 8.2.1.24 CH_STRUCT 23

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW1_CH_STRUCT23_CH_CTL | 0x402985C0 | FULL | Channel control |
| DW1_CH_STRUCT23_CH_STATUS | 0x402985C4 | FULL | Channel status |
| DW1_CH_STRUCT23_CH_IDX | 0x402985C8 | FULL | Channel current indices |
| DW1_CH_STRUCT23_CH_CURR_PTR | 0x402985CC | FULL | Channel current descriptor pointer |
| DW1_CH_STRUCT23_INTR | 0x402985D0 | FULL | Interrupt |
| DW1_CH_STRUCT23_INTR_SET | 0x402985D4 | FULL | Interrupt set |
| DW1_CH_STRUCT23_INTR_MASK | 0x402985D8 | FULL | Interrupt mask |
| DW1_CH_STRUCT23_INTR_MASKED | 0x402985DC | FULL | Interrupt masked |
| DW1_CH_STRUCT23_SRAM_DATA0 | 0x402985E0 | FULL | SRAM data 0 |
| DW1_CH_STRUCT23_SRAM_DATA1 | 0x402985E4 | FULL | SRAM data 1 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW1_CH_STRUCT23_TR_CMD | 0x402985E8 | FULL | Channel software trigger |

### 8.2.1.25 CH_STRUCT 24

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW1_CH_STRUCT24_CH_CTL | 0x40298600 | FULL | Channel control |
| DW1_CH_STRUCT24_CH_STATUS | 0x40298604 | FULL | Channel status |
| DW1_CH_STRUCT24_CH_IDX | 0x40298608 | FULL | Channel current indices |
| DW1_CH_STRUCT24_CH_CURR_PTR | 0x4029860C | FULL | Channel current descriptor pointer |
| DW1_CH_STRUCT24_INTR | 0x40298610 | FULL | Interrupt |
| DW1_CH_STRUCT24_INTR_SET | 0x40298614 | FULL | Interrupt set |
| DW1_CH_STRUCT24_INTR_MASK | 0x40298618 | FULL | Interrupt mask |
| DW1_CH_STRUCT24_INTR_MASKED | 0x4029861C | FULL | Interrupt masked |
| DW1_CH_STRUCT24_SRAM_DATA0 | 0x40298620 | FULL | SRAM data 0 |
| DW1_CH_STRUCT24_SRAM_DATA1 | 0x40298624 | FULL | SRAM data 1 |
| DW1_CH_STRUCT24_TR_CMD | 0x40298628 | FULL | Channel software trigger |

### 8.2.1.26 CH_STRUCT 25

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW1_CH_STRUCT25_CH_CTL | 0x40298640 | FULL | Channel control |
| DW1_CH_STRUCT25_CH_STATUS | 0x40298644 | FULL | Channel status |
| DW1_CH_STRUCT25_CH_IDX | 0x40298648 | FULL | Channel current indices |
| DW1_CH_STRUCT25_CH_CURR_PTR | 0x4029864C | FULL | Channel current descriptor pointer |
| DW1_CH_STRUCT25_INTR | 0x40298650 | FULL | Interrupt |
| DW1_CH_STRUCT25_INTR_SET | 0x40298654 | FULL | Interrupt set |
| DW1_CH_STRUCT25_INTR_MASK | 0x40298658 | FULL | Interrupt mask |
| DW1_CH_STRUCT25_INTR_MASKED | 0x4029865C | FULL | Interrupt masked |
| DW1_CH_STRUCT25_SRAM_DATA0 | 0x40298660 | FULL | SRAM data 0 |
| DW1_CH_STRUCT25_SRAM_DATA1 | 0x40298664 | FULL | SRAM data 1 |
| DW1_CH_STRUCT25_TR_CMD | 0x40298668 | FULL | Channel software trigger |

### 8.2.1.27 CH_STRUCT 26

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW1_CH_STRUCT26_CH_CTL | 0x40298680 | FULL | Channel control |
| DW1_CH_STRUCT26_CH_STATUS | 0x40298684 | FULL | Channel status |
| DW1_CH_STRUCT26_CH_IDX | 0x40298688 | FULL | Channel current indices |
| DW1_CH_STRUCT26_CH_CURR_PTR | 0x4029868C | FULL | Channel current descriptor pointer |
| DW1_CH_STRUCT26_INTR | 0x40298690 | FULL | Interrupt |
| DW1_CH_STRUCT26_INTR_SET | 0x40298694 | FULL | Interrupt set |
| DW1_CH_STRUCT26_INTR_MASK | 0x40298698 | FULL | Interrupt mask |
| DW1_CH_STRUCT26_INTR_MASKED | 0x4029869C | FULL | Interrupt masked |
| DW1_CH_STRUCT26_SRAM_DATA0 | 0x402986A0 | FULL | SRAM data 0 |
| DW1_CH_STRUCT26_SRAM_DATA1 | 0x402986A4 | FULL | SRAM data 1 |
| DW1_CH_STRUCT26_TR_CMD | 0x402986A8 | FULL | Channel software trigger |

### 8.2.1.28 CH_STRUCT 27

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW1_CH_STRUCT27_CH_CTL | 0x402986C0 | FULL | Channel control |
| DW1_CH_STRUCT27_CH_STATUS | 0x402986C4 | FULL | Channel status |
| DW1_CH_STRUCT27_CH_IDX | 0x402986C8 | FULL | Channel current indices |
| DW1_CH_STRUCT27_CH_CURR_PTR | 0x402986CC | FULL | Channel current descriptor pointer |
| DW1_CH_STRUCT27_INTR | 0x402986D0 | FULL | Interrupt |
| DW1_CH_STRUCT27_INTR_SET | 0x402986D4 | FULL | Interrupt set |
| DW1_CH_STRUCT27_INTR_MASK | 0x402986D8 | FULL | Interrupt mask |
| DW1_CH_STRUCT27_INTR_MASKED | 0x402986DC | FULL | Interrupt masked |
| DW1_CH_STRUCT27_SRAM_DATA0 | 0x402986E0 | FULL | SRAM data 0 |
| DW1_CH_STRUCT27_SRAM_DATA1 | 0x402986E4 | FULL | SRAM data 1 |
| DW1_CH_STRUCT27_TR_CMD | 0x402986E8 | FULL | Channel software trigger |

### 8.2.1.29 CH_STRUCT 28

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW1_CH_STRUCT28_CH_CTL | 0x40298700 | FULL | Channel control |
| DW1_CH_STRUCT28_CH_STATUS | 0x40298704 | FULL | Channel status |
| DW1_CH_STRUCT28_CH_IDX | 0x40298708 | FULL | Channel current indices |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW1_CH_STRUCT28_CH_CURR_PTR | 0x4029870C | FULL | Channel current descriptor pointer |
| DW1_CH_STRUCT28_INTR | 0x40298710 | FULL | Interrupt |
| DW1_CH_STRUCT28_INTR_SET | 0x40298714 | FULL | Interrupt set |
| DW1_CH_STRUCT28_INTR_MASK | 0x40298718 | FULL | Interrupt mask |
| DW1_CH_STRUCT28_INTR_MASKED | 0x4029871C | FULL | Interrupt masked |
| DW1_CH_STRUCT28_SRAM_DATA0 | 0x40298720 | FULL | SRAM data 0 |
| DW1_CH_STRUCT28_SRAM_DATA1 | 0x40298724 | FULL | SRAM data 1 |
| DW1_CH_STRUCT28_TR_CMD | 0x40298728 | FULL | Channel software trigger |

### 8.2.1.30 CH_STRUCT 29

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW1_CH_STRUCT29_CH_CTL | 0x40298740 | FULL | Channel control |
| DW1_CH_STRUCT29_CH_STATUS | 0x40298744 | FULL | Channel status |
| DW1_CH_STRUCT29_CH_IDX | 0x40298748 | FULL | Channel current indices |
| DW1_CH_STRUCT29_CH_CURR_PTR | 0x4029874C | FULL | Channel current descriptor pointer |
| DW1_CH_STRUCT29_INTR | 0x40298750 | FULL | Interrupt |
| DW1_CH_STRUCT29_INTR_SET | 0x40298754 | FULL | Interrupt set |
| DW1_CH_STRUCT29_INTR_MASK | 0x40298758 | FULL | Interrupt mask |
| DW1_CH_STRUCT29_INTR_MASKED | 0x4029875C | FULL | Interrupt masked |
| DW1_CH_STRUCT29_SRAM_DATA0 | 0x40298760 | FULL | SRAM data 0 |
| DW1_CH_STRUCT29_SRAM_DATA1 | 0x40298764 | FULL | SRAM data 1 |
| DW1_CH_STRUCT29_TR_CMD | 0x40298768 | FULL | Channel software trigger |

### 8.2.1.31 CH_STRUCT 30

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW1_CH_STRUCT30_CH_CTL | 0x40298780 | FULL | Channel control |
| DW1_CH_STRUCT30_CH_STATUS | 0x40298784 | FULL | Channel status |
| DW1_CH_STRUCT30_CH_IDX | 0x40298788 | FULL | Channel current indices |
| DW1_CH_STRUCT30_CH_CURR_PTR | 0x4029878C | FULL | Channel current descriptor pointer |
| DW1_CH_STRUCT30_INTR | 0x40298790 | FULL | Interrupt |
| DW1_CH_STRUCT30_INTR_SET | 0x40298794 | FULL | Interrupt set |
| DW1_CH_STRUCT30_INTR_MASK | 0x40298798 | FULL | Interrupt mask |
| DW1_CH_STRUCT30_INTR_MASKED | 0x4029879C | FULL | Interrupt masked |
| DW1_CH_STRUCT30_SRAM_DATA0 | 0x402987A0 | FULL | SRAM data 0 |
| DW1_CH_STRUCT30_SRAM_DATA1 | 0x402987A4 | FULL | SRAM data 1 |
| DW1_CH_STRUCT30_TR_CMD | 0x402987A8 | FULL | Channel software trigger |

### 8.2.1.32 CH_STRUCT 31

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW1_CH_STRUCT31_CH_CTL | 0x402987C0 | FULL | Channel control |
| DW1_CH_STRUCT31_CH_STATUS | 0x402987C4 | FULL | Channel status |
| DW1_CH_STRUCT31_CH_IDX | 0x402987C8 | FULL | Channel current indices |
| DW1_CH_STRUCT31_CH_CURR_PTR | 0x402987CC | FULL | Channel current descriptor pointer |
| DW1_CH_STRUCT31_INTR | 0x402987D0 | FULL | Interrupt |
| DW1_CH_STRUCT31_INTR_SET | 0x402987D4 | FULL | Interrupt set |
| DW1_CH_STRUCT31_INTR_MASK | 0x402987D8 | FULL | Interrupt mask |
| DW1_CH_STRUCT31_INTR_MASKED | 0x402987DC | FULL | Interrupt masked |
| DW1_CH_STRUCT31_SRAM_DATA0 | 0x402987E0 | FULL | SRAM data 0 |
| DW1_CH_STRUCT31_SRAM_DATA1 | 0x402987E4 | FULL | SRAM data 1 |
| DW1_CH_STRUCT31_TR_CMD | 0x402987E8 | FULL | Channel software trigger |

### 8.2.1.33 CH_STRUCT 32

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW1_CH_STRUCT32_CH_CTL | 0x40298800 | FULL | Channel control |
| DW1_CH_STRUCT32_CH_STATUS | 0x40298804 | FULL | Channel status |
| DW1_CH_STRUCT32_CH_IDX | 0x40298808 | FULL | Channel current indices |
| DW1_CH_STRUCT32_CH_CURR_PTR | 0x4029880C | FULL | Channel current descriptor pointer |
| DW1_CH_STRUCT32_INTR | 0x40298810 | FULL | Interrupt |
| DW1_CH_STRUCT32_INTR_SET | 0x40298814 | FULL | Interrupt set |
| DW1_CH_STRUCT32_INTR_MASK | 0x40298818 | FULL | Interrupt mask |
| DW1_CH_STRUCT32_INTR_MASKED | 0x4029881C | FULL | Interrupt masked |
| DW1_CH_STRUCT32_SRAM_DATA0 | 0x40298820 | FULL | SRAM data 0 |
| DW1_CH_STRUCT32_SRAM_DATA1 | 0x40298824 | FULL | SRAM data 1 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW1_CH_STRUCT32_TR_CMD | 0x40298828 | FULL | Channel software trigger |

### 8.2.1.34 CH_STRUCT 33

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW1_CH_STRUCT33_CH_CTL | 0x40298840 | FULL | Channel control |
| DW1_CH_STRUCT33_CH_STATUS | 0x40298844 | FULL | Channel status |
| DW1_CH_STRUCT33_CH_IDX | 0x40298848 | FULL | Channel current indices |
| DW1_CH_STRUCT33_CH_CURR_PTR | 0x4029884C | FULL | Channel current descriptor pointer |
| DW1_CH_STRUCT33_INTR | 0x40298850 | FULL | Interrupt |
| DW1_CH_STRUCT33_INTR_SET | 0x40298854 | FULL | Interrupt set |
| DW1_CH_STRUCT33_INTR_MASK | 0x40298858 | FULL | Interrupt mask |
| DW1_CH_STRUCT33_INTR_MASKED | 0x4029885C | FULL | Interrupt masked |
| DW1_CH_STRUCT33_SRAM_DATA0 | 0x40298860 | FULL | SRAM data 0 |
| DW1_CH_STRUCT33_SRAM_DATA1 | 0x40298864 | FULL | SRAM data 1 |
| DW1_CH_STRUCT33_TR_CMD | 0x40298868 | FULL | Channel software trigger |

### 8.2.1.35 CH_STRUCT 34

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW1_CH_STRUCT34_CH_CTL | 0x40298880 | FULL | Channel control |
| DW1_CH_STRUCT34_CH_STATUS | 0x40298884 | FULL | Channel status |
| DW1_CH_STRUCT34_CH_IDX | 0x40298888 | FULL | Channel current indices |
| DW1_CH_STRUCT34_CH_CURR_PTR | 0x4029888C | FULL | Channel current descriptor pointer |
| DW1_CH_STRUCT34_INTR | 0x40298890 | FULL | Interrupt |
| DW1_CH_STRUCT34_INTR_SET | 0x40298894 | FULL | Interrupt set |
| DW1_CH_STRUCT34_INTR_MASK | 0x40298898 | FULL | Interrupt mask |
| DW1_CH_STRUCT34_INTR_MASKED | 0x4029889C | FULL | Interrupt masked |
| DW1_CH_STRUCT34_SRAM_DATA0 | 0x402988A0 | FULL | SRAM data 0 |
| DW1_CH_STRUCT34_SRAM_DATA1 | 0x402988A4 | FULL | SRAM data 1 |
| DW1_CH_STRUCT34_TR_CMD | 0x402988A8 | FULL | Channel software trigger |

### 8.2.1.36 CH_STRUCT 35

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW1_CH_STRUCT35_CH_CTL | 0x402988C0 | FULL | Channel control |
| DW1_CH_STRUCT35_CH_STATUS | 0x402988C4 | FULL | Channel status |
| DW1_CH_STRUCT35_CH_IDX | 0x402988C8 | FULL | Channel current indices |
| DW1_CH_STRUCT35_CH_CURR_PTR | 0x402988CC | FULL | Channel current descriptor pointer |
| DW1_CH_STRUCT35_INTR | 0x402988D0 | FULL | Interrupt |
| DW1_CH_STRUCT35_INTR_SET | 0x402988D4 | FULL | Interrupt set |
| DW1_CH_STRUCT35_INTR_MASK | 0x402988D8 | FULL | Interrupt mask |
| DW1_CH_STRUCT35_INTR_MASKED | 0x402988DC | FULL | Interrupt masked |
| DW1_CH_STRUCT35_SRAM_DATA0 | 0x402988E0 | FULL | SRAM data 0 |
| DW1_CH_STRUCT35_SRAM_DATA1 | 0x402988E4 | FULL | SRAM data 1 |
| DW1_CH_STRUCT35_TR_CMD | 0x402988E8 | FULL | Channel software trigger |

### 8.2.1.37 CH_STRUCT 36

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW1_CH_STRUCT36_CH_CTL | 0x40298900 | FULL | Channel control |
| DW1_CH_STRUCT36_CH_STATUS | 0x40298904 | FULL | Channel status |
| DW1_CH_STRUCT36_CH_IDX | 0x40298908 | FULL | Channel current indices |
| DW1_CH_STRUCT36_CH_CURR_PTR | 0x4029890C | FULL | Channel current descriptor pointer |
| DW1_CH_STRUCT36_INTR | 0x40298910 | FULL | Interrupt |
| DW1_CH_STRUCT36_INTR_SET | 0x40298914 | FULL | Interrupt set |
| DW1_CH_STRUCT36_INTR_MASK | 0x40298918 | FULL | Interrupt mask |
| DW1_CH_STRUCT36_INTR_MASKED | 0x4029891C | FULL | Interrupt masked |
| DW1_CH_STRUCT36_SRAM_DATA0 | 0x40298920 | FULL | SRAM data 0 |
| DW1_CH_STRUCT36_SRAM_DATA1 | 0x40298924 | FULL | SRAM data 1 |
| DW1_CH_STRUCT36_TR_CMD | 0x40298928 | FULL | Channel software trigger |

### 8.2.1.38 CH_STRUCT 37

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW1_CH_STRUCT37_CH_CTL | 0x40298940 | FULL | Channel control |
| DW1_CH_STRUCT37_CH_STATUS | 0x40298944 | FULL | Channel status |
| DW1_CH_STRUCT37_CH_IDX | 0x40298948 | FULL | Channel current indices |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW1_CH_STRUCT37_CH_CURR_PTR | 0x4029894C | FULL | Channel current descriptor pointer |
| DW1_CH_STRUCT37_INTR | 0x40298950 | FULL | Interrupt |
| DW1_CH_STRUCT37_INTR_SET | 0x40298954 | FULL | Interrupt set |
| DW1_CH_STRUCT37_INTR_MASK | 0x40298958 | FULL | Interrupt mask |
| DW1_CH_STRUCT37_INTR_MASKED | 0x4029895C | FULL | Interrupt masked |
| DW1_CH_STRUCT37_SRAM_DATA0 | 0x40298960 | FULL | SRAM data 0 |
| DW1_CH_STRUCT37_SRAM_DATA1 | 0x40298964 | FULL | SRAM data 1 |
| DW1_CH_STRUCT37_TR_CMD | 0x40298968 | FULL | Channel software trigger |

### 8.2.1.39 CH_STRUCT 38

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW1_CH_STRUCT38_CH_CTL | 0x40298980 | FULL | Channel control |
| DW1_CH_STRUCT38_CH_STATUS | 0x40298984 | FULL | Channel status |
| DW1_CH_STRUCT38_CH_IDX | 0x40298988 | FULL | Channel current indices |
| DW1_CH_STRUCT38_CH_CURR_PTR | 0x4029898C | FULL | Channel current descriptor pointer |
| DW1_CH_STRUCT38_INTR | 0x40298990 | FULL | Interrupt |
| DW1_CH_STRUCT38_INTR_SET | 0x40298994 | FULL | Interrupt set |
| DW1_CH_STRUCT38_INTR_MASK | 0x40298998 | FULL | Interrupt mask |
| DW1_CH_STRUCT38_INTR_MASKED | 0x4029899C | FULL | Interrupt masked |
| DW1_CH_STRUCT38_SRAM_DATA0 | 0x402989A0 | FULL | SRAM data 0 |
| DW1_CH_STRUCT38_SRAM_DATA1 | 0x402989A4 | FULL | SRAM data 1 |
| DW1_CH_STRUCT38_TR_CMD | 0x402989A8 | FULL | Channel software trigger |

### 8.2.1.40 CH_STRUCT 39

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW1_CH_STRUCT39_CH_CTL | 0x402989C0 | FULL | Channel control |
| DW1_CH_STRUCT39_CH_STATUS | 0x402989C4 | FULL | Channel status |
| DW1_CH_STRUCT39_CH_IDX | 0x402989C8 | FULL | Channel current indices |
| DW1_CH_STRUCT39_CH_CURR_PTR | 0x402989CC | FULL | Channel current descriptor pointer |
| DW1_CH_STRUCT39_INTR | 0x402989D0 | FULL | Interrupt |
| DW1_CH_STRUCT39_INTR_SET | 0x402989D4 | FULL | Interrupt set |
| DW1_CH_STRUCT39_INTR_MASK | 0x402989D8 | FULL | Interrupt mask |
| DW1_CH_STRUCT39_INTR_MASKED | 0x402989DC | FULL | Interrupt masked |
| DW1_CH_STRUCT39_SRAM_DATA0 | 0x402989E0 | FULL | SRAM data 0 |
| DW1_CH_STRUCT39_SRAM_DATA1 | 0x402989E4 | FULL | SRAM data 1 |
| DW1_CH_STRUCT39_TR_CMD | 0x402989E8 | FULL | Channel software trigger |

### 8.2.1.41 CH_STRUCT 40

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW1_CH_STRUCT40_CH_CTL | 0x40298A00 | FULL | Channel control |
| DW1_CH_STRUCT40_CH_STATUS | 0x40298A04 | FULL | Channel status |
| DW1_CH_STRUCT40_CH_IDX | 0x40298A08 | FULL | Channel current indices |
| DW1_CH_STRUCT40_CH_CURR_PTR | 0x40298A0C | FULL | Channel current descriptor pointer |
| DW1_CH_STRUCT40_INTR | 0x40298A10 | FULL | Interrupt |
| DW1_CH_STRUCT40_INTR_SET | 0x40298A14 | FULL | Interrupt set |
| DW1_CH_STRUCT40_INTR_MASK | 0x40298A18 | FULL | Interrupt mask |
| DW1_CH_STRUCT40_INTR_MASKED | 0x40298A1C | FULL | Interrupt masked |
| DW1_CH_STRUCT40_SRAM_DATA0 | 0x40298A20 | FULL | SRAM data 0 |
| DW1_CH_STRUCT40_SRAM_DATA1 | 0x40298A24 | FULL | SRAM data 1 |
| DW1_CH_STRUCT40_TR_CMD | 0x40298A28 | FULL | Channel software trigger |

### 8.2.1.42 CH_STRUCT 41

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW1_CH_STRUCT41_CH_CTL | 0x40298A40 | FULL | Channel control |
| DW1_CH_STRUCT41_CH_STATUS | 0x40298A44 | FULL | Channel status |
| DW1_CH_STRUCT41_CH_IDX | 0x40298A48 | FULL | Channel current indices |
| DW1_CH_STRUCT41_CH_CURR_PTR | 0x40298A4C | FULL | Channel current descriptor pointer |
| DW1_CH_STRUCT41_INTR | 0x40298A50 | FULL | Interrupt |
| DW1_CH_STRUCT41_INTR_SET | 0x40298A54 | FULL | Interrupt set |
| DW1_CH_STRUCT41_INTR_MASK | 0x40298A58 | FULL | Interrupt mask |
| DW1_CH_STRUCT41_INTR_MASKED | 0x40298A5C | FULL | Interrupt masked |
| DW1_CH_STRUCT41_SRAM_DATA0 | 0x40298A60 | FULL | SRAM data 0 |
| DW1_CH_STRUCT41_SRAM_DATA1 | 0x40298A64 | FULL | SRAM data 1 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW1_CH_STRUCT41_TR_CMD | 0x40298A68 | FULL | Channel software trigger |

### 8.2.1.43 CH_STRUCT 42

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW1_CH_STRUCT42_CH_CTL | 0x40298A80 | FULL | Channel control |
| DW1_CH_STRUCT42_CH_STATUS | 0x40298A84 | FULL | Channel status |
| DW1_CH_STRUCT42_CH_IDX | 0x40298A88 | FULL | Channel current indices |
| DW1_CH_STRUCT42_CH_CURR_PTR | 0x40298A8C | FULL | Channel current descriptor pointer |
| DW1_CH_STRUCT42_INTR | 0x40298A90 | FULL | Interrupt |
| DW1_CH_STRUCT42_INTR_SET | 0x40298A94 | FULL | Interrupt set |
| DW1_CH_STRUCT42_INTR_MASK | 0x40298A98 | FULL | Interrupt mask |
| DW1_CH_STRUCT42_INTR_MASKED | 0x40298A9C | FULL | Interrupt masked |
| DW1_CH_STRUCT42_SRAM_DATA0 | 0x40298AA0 | FULL | SRAM data 0 |
| DW1_CH_STRUCT42_SRAM_DATA1 | 0x40298AA4 | FULL | SRAM data 1 |
| DW1_CH_STRUCT42_TR_CMD | 0x40298AA8 | FULL | Channel software trigger |

### 8.2.1.44 CH_STRUCT 43

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW1_CH_STRUCT43_CH_CTL | 0x40298AC0 | FULL | Channel control |
| DW1_CH_STRUCT43_CH_STATUS | 0x40298AC4 | FULL | Channel status |
| DW1_CH_STRUCT43_CH_IDX | 0x40298AC8 | FULL | Channel current indices |
| DW1_CH_STRUCT43_CH_CURR_PTR | 0x40298ACC | FULL | Channel current descriptor pointer |
| DW1_CH_STRUCT43_INTR | 0x40298AD0 | FULL | Interrupt |
| DW1_CH_STRUCT43_INTR_SET | 0x40298AD4 | FULL | Interrupt set |
| DW1_CH_STRUCT43_INTR_MASK | 0x40298AD8 | FULL | Interrupt mask |
| DW1_CH_STRUCT43_INTR_MASKED | 0x40298ADC | FULL | Interrupt masked |
| DW1_CH_STRUCT43_SRAM_DATA0 | 0x40298AE0 | FULL | SRAM data 0 |
| DW1_CH_STRUCT43_SRAM_DATA1 | 0x40298AE4 | FULL | SRAM data 1 |
| DW1_CH_STRUCT43_TR_CMD | 0x40298AE8 | FULL | Channel software trigger |

### 8.2.1.45 CH_STRUCT 44

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW1_CH_STRUCT44_CH_CTL | 0x40298B00 | FULL | Channel control |
| DW1_CH_STRUCT44_CH_STATUS | 0x40298B04 | FULL | Channel status |
| DW1_CH_STRUCT44_CH_IDX | 0x40298B08 | FULL | Channel current indices |
| DW1_CH_STRUCT44_CH_CURR_PTR | 0x40298B0C | FULL | Channel current descriptor pointer |
| DW1_CH_STRUCT44_INTR | 0x40298B10 | FULL | Interrupt |
| DW1_CH_STRUCT44_INTR_SET | 0x40298B14 | FULL | Interrupt set |
| DW1_CH_STRUCT44_INTR_MASK | 0x40298B18 | FULL | Interrupt mask |
| DW1_CH_STRUCT44_INTR_MASKED | 0x40298B1C | FULL | Interrupt masked |
| DW1_CH_STRUCT44_SRAM_DATA0 | 0x40298B20 | FULL | SRAM data 0 |
| DW1_CH_STRUCT44_SRAM_DATA1 | 0x40298B24 | FULL | SRAM data 1 |
| DW1_CH_STRUCT44_TR_CMD | 0x40298B28 | FULL | Channel software trigger |

### 8.2.1.46 CH_STRUCT 45

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW1_CH_STRUCT45_CH_CTL | 0x40298B40 | FULL | Channel control |
| DW1_CH_STRUCT45_CH_STATUS | 0x40298B44 | FULL | Channel status |
| DW1_CH_STRUCT45_CH_IDX | 0x40298B48 | FULL | Channel current indices |
| DW1_CH_STRUCT45_CH_CURR_PTR | 0x40298B4C | FULL | Channel current descriptor pointer |
| DW1_CH_STRUCT45_INTR | 0x40298B50 | FULL | Interrupt |
| DW1_CH_STRUCT45_INTR_SET | 0x40298B54 | FULL | Interrupt set |
| DW1_CH_STRUCT45_INTR_MASK | 0x40298B58 | FULL | Interrupt mask |
| DW1_CH_STRUCT45_INTR_MASKED | 0x40298B5C | FULL | Interrupt masked |
| DW1_CH_STRUCT45_SRAM_DATA0 | 0x40298B60 | FULL | SRAM data 0 |
| DW1_CH_STRUCT45_SRAM_DATA1 | 0x40298B64 | FULL | SRAM data 1 |
| DW1_CH_STRUCT45_TR_CMD | 0x40298B68 | FULL | Channel software trigger |

### 8.2.1.47 CH_STRUCT 46

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW1_CH_STRUCT46_CH_CTL | 0x40298B80 | FULL | Channel control |
| DW1_CH_STRUCT46_CH_STATUS | 0x40298B84 | FULL | Channel status |
| DW1_CH_STRUCT46_CH_IDX | 0x40298B88 | FULL | Channel current indices |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW1_CH_STRUCT46_CH_CURR_PTR | 0x40298B8C | FULL | Channel current descriptor pointer |
| DW1_CH_STRUCT46_INTR | 0x40298B90 | FULL | Interrupt |
| DW1_CH_STRUCT46_INTR_SET | 0x40298B94 | FULL | Interrupt set |
| DW1_CH_STRUCT46_INTR_MASK | 0x40298B98 | FULL | Interrupt mask |
| DW1_CH_STRUCT46_INTR_MASKED | 0x40298B9C | FULL | Interrupt masked |
| DW1_CH_STRUCT46_SRAM_DATA0 | 0x40298BA0 | FULL | SRAM data 0 |
| DW1_CH_STRUCT46_SRAM_DATA1 | 0x40298BA4 | FULL | SRAM data 1 |
| DW1_CH_STRUCT46_TR_CMD | 0x40298BA8 | FULL | Channel software trigger |

### 8.2.1.48 CH_STRUCT 47

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW1_CH_STRUCT47_CH_CTL | 0x40298BC0 | FULL | Channel control |
| DW1_CH_STRUCT47_CH_STATUS | 0x40298BC4 | FULL | Channel status |
| DW1_CH_STRUCT47_CH_IDX | 0x40298BC8 | FULL | Channel current indices |
| DW1_CH_STRUCT47_CH_CURR_PTR | 0x40298BCC | FULL | Channel current descriptor pointer |
| DW1_CH_STRUCT47_INTR | 0x40298BD0 | FULL | Interrupt |
| DW1_CH_STRUCT47_INTR_SET | 0x40298BD4 | FULL | Interrupt set |
| DW1_CH_STRUCT47_INTR_MASK | 0x40298BD8 | FULL | Interrupt mask |
| DW1_CH_STRUCT47_INTR_MASKED | 0x40298BDC | FULL | Interrupt masked |
| DW1_CH_STRUCT47_SRAM_DATA0 | 0x40298BE0 | FULL | SRAM data 0 |
| DW1_CH_STRUCT47_SRAM_DATA1 | 0x40298BE4 | FULL | SRAM data 1 |
| DW1_CH_STRUCT47_TR_CMD | 0x40298BE8 | FULL | Channel software trigger |

### 8.2.1.49 CH_STRUCT 48

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW1_CH_STRUCT48_CH_CTL | 0x40298C00 | FULL | Channel control |
| DW1_CH_STRUCT48_CH_STATUS | 0x40298C04 | FULL | Channel status |
| DW1_CH_STRUCT48_CH_IDX | 0x40298C08 | FULL | Channel current indices |
| DW1_CH_STRUCT48_CH_CURR_PTR | 0x40298C0C | FULL | Channel current descriptor pointer |
| DW1_CH_STRUCT48_INTR | 0x40298C10 | FULL | Interrupt |
| DW1_CH_STRUCT48_INTR_SET | 0x40298C14 | FULL | Interrupt set |
| DW1_CH_STRUCT48_INTR_MASK | 0x40298C18 | FULL | Interrupt mask |
| DW1_CH_STRUCT48_INTR_MASKED | 0x40298C1C | FULL | Interrupt masked |
| DW1_CH_STRUCT48_SRAM_DATA0 | 0x40298C20 | FULL | SRAM data 0 |
| DW1_CH_STRUCT48_SRAM_DATA1 | 0x40298C24 | FULL | SRAM data 1 |
| DW1_CH_STRUCT48_TR_CMD | 0x40298C28 | FULL | Channel software trigger |

### 8.2.1.50 CH_STRUCT 49

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW1_CH_STRUCT49_CH_CTL | 0x40298C40 | FULL | Channel control |
| DW1_CH_STRUCT49_CH_STATUS | 0x40298C44 | FULL | Channel status |
| DW1_CH_STRUCT49_CH_IDX | 0x40298C48 | FULL | Channel current indices |
| DW1_CH_STRUCT49_CH_CURR_PTR | 0x40298C4C | FULL | Channel current descriptor pointer |
| DW1_CH_STRUCT49_INTR | 0x40298C50 | FULL | Interrupt |
| DW1_CH_STRUCT49_INTR_SET | 0x40298C54 | FULL | Interrupt set |
| DW1_CH_STRUCT49_INTR_MASK | 0x40298C58 | FULL | Interrupt mask |
| DW1_CH_STRUCT49_INTR_MASKED | 0x40298C5C | FULL | Interrupt masked |
| DW1_CH_STRUCT49_SRAM_DATA0 | 0x40298C60 | FULL | SRAM data 0 |
| DW1_CH_STRUCT49_SRAM_DATA1 | 0x40298C64 | FULL | SRAM data 1 |
| DW1_CH_STRUCT49_TR_CMD | 0x40298C68 | FULL | Channel software trigger |

### 8.2.1.51 CH_STRUCT 50

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW1_CH_STRUCT50_CH_CTL | 0x40298C80 | FULL | Channel control |
| DW1_CH_STRUCT50_CH_STATUS | 0x40298C84 | FULL | Channel status |
| DW1_CH_STRUCT50_CH_IDX | 0x40298C88 | FULL | Channel current indices |
| DW1_CH_STRUCT50_CH_CURR_PTR | 0x40298C8C | FULL | Channel current descriptor pointer |
| DW1_CH_STRUCT50_INTR | 0x40298C90 | FULL | Interrupt |
| DW1_CH_STRUCT50_INTR_SET | 0x40298C94 | FULL | Interrupt set |
| DW1_CH_STRUCT50_INTR_MASK | 0x40298C98 | FULL | Interrupt mask |
| DW1_CH_STRUCT50_INTR_MASKED | 0x40298C9C | FULL | Interrupt masked |
| DW1_CH_STRUCT50_SRAM_DATA0 | 0x40298CA0 | FULL | SRAM data 0 |
| DW1_CH_STRUCT50_SRAM_DATA1 | 0x40298CA4 | FULL | SRAM data 1 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW1_CH_STRUCT50_TR_CMD | 0x40298CA8 | FULL | Channel software trigger |

### 8.2.1.52 CH_STRUCT 51

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW1_CH_STRUCT51_CH_CTL | 0x40298CC0 | FULL | Channel control |
| DW1_CH_STRUCT51_CH_STATUS | 0x40298CC4 | FULL | Channel status |
| DW1_CH_STRUCT51_CH_IDX | 0x40298CC8 | FULL | Channel current indices |
| DW1_CH_STRUCT51_CH_CURR_PTR | 0x40298CCC | FULL | Channel current descriptor pointer |
| DW1_CH_STRUCT51_INTR | 0x40298CD0 | FULL | Interrupt |
| DW1_CH_STRUCT51_INTR_SET | 0x40298CD4 | FULL | Interrupt set |
| DW1_CH_STRUCT51_INTR_MASK | 0x40298CD8 | FULL | Interrupt mask |
| DW1_CH_STRUCT51_INTR_MASKED | 0x40298CDC | FULL | Interrupt masked |
| DW1_CH_STRUCT51_SRAM_DATA0 | 0x40298CE0 | FULL | SRAM data 0 |
| DW1_CH_STRUCT51_SRAM_DATA1 | 0x40298CE4 | FULL | SRAM data 1 |
| DW1_CH_STRUCT51_TR_CMD | 0x40298CE8 | FULL | Channel software trigger |

### 8.2.1.53 CH_STRUCT 52

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW1_CH_STRUCT52_CH_CTL | 0x40298D00 | FULL | Channel control |
| DW1_CH_STRUCT52_CH_STATUS | 0x40298D04 | FULL | Channel status |
| DW1_CH_STRUCT52_CH_IDX | 0x40298D08 | FULL | Channel current indices |
| DW1_CH_STRUCT52_CH_CURR_PTR | 0x40298D0C | FULL | Channel current descriptor pointer |
| DW1_CH_STRUCT52_INTR | 0x40298D10 | FULL | Interrupt |
| DW1_CH_STRUCT52_INTR_SET | 0x40298D14 | FULL | Interrupt set |
| DW1_CH_STRUCT52_INTR_MASK | 0x40298D18 | FULL | Interrupt mask |
| DW1_CH_STRUCT52_INTR_MASKED | 0x40298D1C | FULL | Interrupt masked |
| DW1_CH_STRUCT52_SRAM_DATA0 | 0x40298D20 | FULL | SRAM data 0 |
| DW1_CH_STRUCT52_SRAM_DATA1 | 0x40298D24 | FULL | SRAM data 1 |
| DW1_CH_STRUCT52_TR_CMD | 0x40298D28 | FULL | Channel software trigger |

### 8.2.1.54 CH_STRUCT 53

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW1_CH_STRUCT53_CH_CTL | 0x40298D40 | FULL | Channel control |
| DW1_CH_STRUCT53_CH_STATUS | 0x40298D44 | FULL | Channel status |
| DW1_CH_STRUCT53_CH_IDX | 0x40298D48 | FULL | Channel current indices |
| DW1_CH_STRUCT53_CH_CURR_PTR | 0x40298D4C | FULL | Channel current descriptor pointer |
| DW1_CH_STRUCT53_INTR | 0x40298D50 | FULL | Interrupt |
| DW1_CH_STRUCT53_INTR_SET | 0x40298D54 | FULL | Interrupt set |
| DW1_CH_STRUCT53_INTR_MASK | 0x40298D58 | FULL | Interrupt mask |
| DW1_CH_STRUCT53_INTR_MASKED | 0x40298D5C | FULL | Interrupt masked |
| DW1_CH_STRUCT53_SRAM_DATA0 | 0x40298D60 | FULL | SRAM data 0 |
| DW1_CH_STRUCT53_SRAM_DATA1 | 0x40298D64 | FULL | SRAM data 1 |
| DW1_CH_STRUCT53_TR_CMD | 0x40298D68 | FULL | Channel software trigger |

### 8.2.1.55 CH_STRUCT 54

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW1_CH_STRUCT54_CH_CTL | 0x40298D80 | FULL | Channel control |
| DW1_CH_STRUCT54_CH_STATUS | 0x40298D84 | FULL | Channel status |
| DW1_CH_STRUCT54_CH_IDX | 0x40298D88 | FULL | Channel current indices |
| DW1_CH_STRUCT54_CH_CURR_PTR | 0x40298D8C | FULL | Channel current descriptor pointer |
| DW1_CH_STRUCT54_INTR | 0x40298D90 | FULL | Interrupt |
| DW1_CH_STRUCT54_INTR_SET | 0x40298D94 | FULL | Interrupt set |
| DW1_CH_STRUCT54_INTR_MASK | 0x40298D98 | FULL | Interrupt mask |
| DW1_CH_STRUCT54_INTR_MASKED | 0x40298D9C | FULL | Interrupt masked |
| DW1_CH_STRUCT54_SRAM_DATA0 | 0x40298DA0 | FULL | SRAM data 0 |
| DW1_CH_STRUCT54_SRAM_DATA1 | 0x40298DA4 | FULL | SRAM data 1 |
| DW1_CH_STRUCT54_TR_CMD | 0x40298DA8 | FULL | Channel software trigger |

### 8.2.1.56 CH_STRUCT 55

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW1_CH_STRUCT55_CH_CTL | 0x40298DC0 | FULL | Channel control |
| DW1_CH_STRUCT55_CH_STATUS | 0x40298DC4 | FULL | Channel status |
| DW1_CH_STRUCT55_CH_IDX | 0x40298DC8 | FULL | Channel current indices |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW1_CH_STRUCT55_CH_CURR_PTR | 0x40298DCC | FULL | Channel current descriptor pointer |
| DW1_CH_STRUCT55_INTR | 0x40298DD0 | FULL | Interrupt |
| DW1_CH_STRUCT55_INTR_SET | 0x40298DD4 | FULL | Interrupt set |
| DW1_CH_STRUCT55_INTR_MASK | 0x40298DD8 | FULL | Interrupt mask |
| DW1_CH_STRUCT55_INTR_MASKED | 0x40298DDC | FULL | Interrupt masked |
| DW1_CH_STRUCT55_SRAM_DATA0 | 0x40298DE0 | FULL | SRAM data 0 |
| DW1_CH_STRUCT55_SRAM_DATA1 | 0x40298DE4 | FULL | SRAM data 1 |
| DW1_CH_STRUCT55_TR_CMD | 0x40298DE8 | FULL | Channel software trigger |

### 8.2.1.57 CH_STRUCT 56

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW1_CH_STRUCT56_CH_CTL | 0x40298E00 | FULL | Channel control |
| DW1_CH_STRUCT56_CH_STATUS | 0x40298E04 | FULL | Channel status |
| DW1_CH_STRUCT56_CH_IDX | 0x40298E08 | FULL | Channel current indices |
| DW1_CH_STRUCT56_CH_CURR_PTR | 0x40298E0C | FULL | Channel current descriptor pointer |
| DW1_CH_STRUCT56_INTR | 0x40298E10 | FULL | Interrupt |
| DW1_CH_STRUCT56_INTR_SET | 0x40298E14 | FULL | Interrupt set |
| DW1_CH_STRUCT56_INTR_MASK | 0x40298E18 | FULL | Interrupt mask |
| DW1_CH_STRUCT56_INTR_MASKED | 0x40298E1C | FULL | Interrupt masked |
| DW1_CH_STRUCT56_SRAM_DATA0 | 0x40298E20 | FULL | SRAM data 0 |
| DW1_CH_STRUCT56_SRAM_DATA1 | 0x40298E24 | FULL | SRAM data 1 |
| DW1_CH_STRUCT56_TR_CMD | 0x40298E28 | FULL | Channel software trigger |

### 8.2.1.58 CH_STRUCT 57

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW1_CH_STRUCT57_CH_CTL | 0x40298E40 | FULL | Channel control |
| DW1_CH_STRUCT57_CH_STATUS | 0x40298E44 | FULL | Channel status |
| DW1_CH_STRUCT57_CH_IDX | 0x40298E48 | FULL | Channel current indices |
| DW1_CH_STRUCT57_CH_CURR_PTR | 0x40298E4C | FULL | Channel current descriptor pointer |
| DW1_CH_STRUCT57_INTR | 0x40298E50 | FULL | Interrupt |
| DW1_CH_STRUCT57_INTR_SET | 0x40298E54 | FULL | Interrupt set |
| DW1_CH_STRUCT57_INTR_MASK | 0x40298E58 | FULL | Interrupt mask |
| DW1_CH_STRUCT57_INTR_MASKED | 0x40298E5C | FULL | Interrupt masked |
| DW1_CH_STRUCT57_SRAM_DATA0 | 0x40298E60 | FULL | SRAM data 0 |
| DW1_CH_STRUCT57_SRAM_DATA1 | 0x40298E64 | FULL | SRAM data 1 |
| DW1_CH_STRUCT57_TR_CMD | 0x40298E68 | FULL | Channel software trigger |

### 8.2.1.59 CH_STRUCT 58

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW1_CH_STRUCT58_CH_CTL | 0x40298E80 | FULL | Channel control |
| DW1_CH_STRUCT58_CH_STATUS | 0x40298E84 | FULL | Channel status |
| DW1_CH_STRUCT58_CH_IDX | 0x40298E88 | FULL | Channel current indices |
| DW1_CH_STRUCT58_CH_CURR_PTR | 0x40298E8C | FULL | Channel current descriptor pointer |
| DW1_CH_STRUCT58_INTR | 0x40298E90 | FULL | Interrupt |
| DW1_CH_STRUCT58_INTR_SET | 0x40298E94 | FULL | Interrupt set |
| DW1_CH_STRUCT58_INTR_MASK | 0x40298E98 | FULL | Interrupt mask |
| DW1_CH_STRUCT58_INTR_MASKED | 0x40298E9C | FULL | Interrupt masked |
| DW1_CH_STRUCT58_SRAM_DATA0 | 0x40298EA0 | FULL | SRAM data 0 |
| DW1_CH_STRUCT58_SRAM_DATA1 | 0x40298EA4 | FULL | SRAM data 1 |
| DW1_CH_STRUCT58_TR_CMD | 0x40298EA8 | FULL | Channel software trigger |

### 8.2.1.60 CH_STRUCT 59

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW1_CH_STRUCT59_CH_CTL | 0x40298EC0 | FULL | Channel control |
| DW1_CH_STRUCT59_CH_STATUS | 0x40298EC4 | FULL | Channel status |
| DW1_CH_STRUCT59_CH_IDX | 0x40298EC8 | FULL | Channel current indices |
| DW1_CH_STRUCT59_CH_CURR_PTR | 0x40298ECC | FULL | Channel current descriptor pointer |
| DW1_CH_STRUCT59_INTR | 0x40298ED0 | FULL | Interrupt |
| DW1_CH_STRUCT59_INTR_SET | 0x40298ED4 | FULL | Interrupt set |
| DW1_CH_STRUCT59_INTR_MASK | 0x40298ED8 | FULL | Interrupt mask |
| DW1_CH_STRUCT59_INTR_MASKED | 0x40298EDC | FULL | Interrupt masked |
| DW1_CH_STRUCT59_SRAM_DATA0 | 0x40298EE0 | FULL | SRAM data 0 |
| DW1_CH_STRUCT59_SRAM_DATA1 | 0x40298EE4 | FULL | SRAM data 1 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW1_CH_STRUCT59_TR_CMD | 0x40298EE8 | FULL | Channel software trigger |

### 8.2.1.61 CH_STRUCT 60

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW1_CH_STRUCT60_CH_CTL | 0x40298F00 | FULL | Channel control |
| DW1_CH_STRUCT60_CH_STATUS | 0x40298F04 | FULL | Channel status |
| DW1_CH_STRUCT60_CH_IDX | 0x40298F08 | FULL | Channel current indices |
| DW1_CH_STRUCT60_CH_CURR_PTR | 0x40298F0C | FULL | Channel current descriptor pointer |
| DW1_CH_STRUCT60_INTR | 0x40298F10 | FULL | Interrupt |
| DW1_CH_STRUCT60_INTR_SET | 0x40298F14 | FULL | Interrupt set |
| DW1_CH_STRUCT60_INTR_MASK | 0x40298F18 | FULL | Interrupt mask |
| DW1_CH_STRUCT60_INTR_MASKED | 0x40298F1C | FULL | Interrupt masked |
| DW1_CH_STRUCT60_SRAM_DATA0 | 0x40298F20 | FULL | SRAM data 0 |
| DW1_CH_STRUCT60_SRAM_DATA1 | 0x40298F24 | FULL | SRAM data 1 |
| DW1_CH_STRUCT60_TR_CMD | 0x40298F28 | FULL | Channel software trigger |

### 8.2.1.62 CH_STRUCT 61

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW1_CH_STRUCT61_CH_CTL | 0x40298F40 | FULL | Channel control |
| DW1_CH_STRUCT61_CH_STATUS | 0x40298F44 | FULL | Channel status |
| DW1_CH_STRUCT61_CH_IDX | 0x40298F48 | FULL | Channel current indices |
| DW1_CH_STRUCT61_CH_CURR_PTR | 0x40298F4C | FULL | Channel current descriptor pointer |
| DW1_CH_STRUCT61_INTR | 0x40298F50 | FULL | Interrupt |
| DW1_CH_STRUCT61_INTR_SET | 0x40298F54 | FULL | Interrupt set |
| DW1_CH_STRUCT61_INTR_MASK | 0x40298F58 | FULL | Interrupt mask |
| DW1_CH_STRUCT61_INTR_MASKED | 0x40298F5C | FULL | Interrupt masked |
| DW1_CH_STRUCT61_SRAM_DATA0 | 0x40298F60 | FULL | SRAM data 0 |
| DW1_CH_STRUCT61_SRAM_DATA1 | 0x40298F64 | FULL | SRAM data 1 |
| DW1_CH_STRUCT61_TR_CMD | 0x40298F68 | FULL | Channel software trigger |

### 8.2.1.63 CH_STRUCT 62

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW1_CH_STRUCT62_CH_CTL | 0x40298F80 | FULL | Channel control |
| DW1_CH_STRUCT62_CH_STATUS | 0x40298F84 | FULL | Channel status |
| DW1_CH_STRUCT62_CH_IDX | 0x40298F88 | FULL | Channel current indices |
| DW1_CH_STRUCT62_CH_CURR_PTR | 0x40298F8C | FULL | Channel current descriptor pointer |
| DW1_CH_STRUCT62_INTR | 0x40298F90 | FULL | Interrupt |
| DW1_CH_STRUCT62_INTR_SET | 0x40298F94 | FULL | Interrupt set |
| DW1_CH_STRUCT62_INTR_MASK | 0x40298F98 | FULL | Interrupt mask |
| DW1_CH_STRUCT62_INTR_MASKED | 0x40298F9C | FULL | Interrupt masked |
| DW1_CH_STRUCT62_SRAM_DATA0 | 0x40298FA0 | FULL | SRAM data 0 |
| DW1_CH_STRUCT62_SRAM_DATA1 | 0x40298FA4 | FULL | SRAM data 1 |
| DW1_CH_STRUCT62_TR_CMD | 0x40298FA8 | FULL | Channel software trigger |

### 8.2.1.64 CH_STRUCT 63

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW1_CH_STRUCT63_CH_CTL | 0x40298FC0 | FULL | Channel control |
| DW1_CH_STRUCT63_CH_STATUS | 0x40298FC4 | FULL | Channel status |
| DW1_CH_STRUCT63_CH_IDX | 0x40298FC8 | FULL | Channel current indices |
| DW1_CH_STRUCT63_CH_CURR_PTR | 0x40298FCC | FULL | Channel current descriptor pointer |
| DW1_CH_STRUCT63_INTR | 0x40298FD0 | FULL | Interrupt |
| DW1_CH_STRUCT63_INTR_SET | 0x40298FD4 | FULL | Interrupt set |
| DW1_CH_STRUCT63_INTR_MASK | 0x40298FD8 | FULL | Interrupt mask |
| DW1_CH_STRUCT63_INTR_MASKED | 0x40298FDC | FULL | Interrupt masked |
| DW1_CH_STRUCT63_SRAM_DATA0 | 0x40298FE0 | FULL | SRAM data 0 |
| DW1_CH_STRUCT63_SRAM_DATA1 | 0x40298FE4 | FULL | SRAM data 1 |
| DW1_CH_STRUCT63_TR_CMD | 0x40298FE8 | FULL | Channel software trigger |

### 8.2.1.65 CH_STRUCT 64

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW1_CH_STRUCT64_CH_CTL | 0x40299000 | FULL | Channel control |
| DW1_CH_STRUCT64_CH_STATUS | 0x40299004 | FULL | Channel status |
| DW1_CH_STRUCT64_CH_IDX | 0x40299008 | FULL | Channel current indices |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| DW1_CH_STRUCT64_CH_CURR_PTR | 0x4029900C | FULL | Channel current descriptor pointer |
| DW1_CH_STRUCT64_INTR | 0x40299010 | FULL | Interrupt |
| DW1_CH_STRUCT64_INTR_SET | 0x40299014 | FULL | Interrupt set |
| DW1_CH_STRUCT64_INTR_MASK | 0x40299018 | FULL | Interrupt mask |
| DW1_CH_STRUCT64_INTR_MASKED | 0x4029901C | FULL | Interrupt masked |
| DW1_CH_STRUCT64_SRAM_DATA0 | 0x40299020 | FULL | SRAM data 0 |
| DW1_CH_STRUCT64_SRAM_DATA1 | 0x40299024 | FULL | SRAM data 1 |
| DW1_CH_STRUCT64_TR_CMD | 0x40299028 | FULL | Channel software trigger |

## 8.3 Register Details

### 8.3.1 DW_CTL

**Description:** Control
**Address:** 0x40280000
**Offset:** 0x0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x1

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:2] | | | | | | ECC_INJ_EN [1:1] | ECC_EN [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | ENABLED [31:31] | None [30:24] | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | ECC_EN | RW | R | 1 | Enable ECC checking:<br>'0': Disabled.<br>'1': Enabled. |
| 1 | ECC_INJ_EN | RW | R | 0 | Enable parity injection for SRAM.<br>When '1', the parity (ECC_CTL.PARITY) is used when a full 32-bit write is done to the ECC_CTL.WORD_ADDR word address of the SRAM. |
| 31 | ENABLED | RW | R | 0 | IP enable:<br>'0': Disabled. Disabling the IP activates the IP's Active logic reset: Active logic and non-retention MMIO registers are reset (retention MMIO registers are not affected).<br>'1': Enabled. |

### 8.3.2 DW_STATUS

**Description:** Status
**Address:** 0x40280004
**Offset:** 0x4
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | PC [7:4] | | | | None [3:3] | B [2:2] | NS [1:1] | P [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:12] | | | | PREEMPTABLE [11:11] | None [10:10] | PRIO [9:8] | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | CH_IDX [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | ACTIVE [31:31] | STATE [30:28] | | | None [27:25] | | | CH_IDX [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | P | R | RW | Undefined | Active channel, user/privileged access control:<br>'0': user mode.<br>'1': privileged mode. |
| 1 | NS | R | RW | Undefined | Active channel, secure/non-secure access control:<br>'0': secure.<br>'1': non-secure. |
| 2 | B | R | RW | Undefined | Active channel, non-bufferable/bufferable access control:<br>'0': non-bufferable<br>'1': bufferable. |
| 4:7 | PC | R | RW | Undefined | Active channel protection context. |
| 8:9 | PRIO | R | W | Undefined | Active channel priority. |
| 11 | PREEMPTABLE | R | W | Undefined | Active channel preemptable. |
| 16:24 | CH_IDX | R | W | Undefined | Active channel index. |
| 28:30 | STATE | R | W | 0 | State of the DW controller.<br>'0': Default/inactive state.<br>'1': Loading descriptor.<br>'2': Loading data element from source location.<br>'3': Storing data element to destination location.<br>'4': CRC functionality (only used for CRC transfer descriptor type).<br>'5': Update of active control information (e.g. source and destination addresses) and wait for trigger de-activation.<br>'6': Error. |
| 31 | ACTIVE | R | W | 0 | Active channel present:<br>'0': No.<br>'1': Yes. |

### 8.3.3 DW_ACT_DESCR_CTL

**Description:** Active descriptor control
**Address:** 0x40280020
**Offset:** 0x20
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | DATA | R | W | Undefined | Copy of DESCR_CTL of the currently active descriptor.<br><br>[1:0] WAIT_FOR_DEACT<br>Specifies whether the controller should wait for the input trigger to be deactivated; i.e. the selected system trigger is not active. This field is used to synchronize the controller with the agent that generated the trigger. This field is ONLY used at the completion of the transfer as specified by TR_IN. E.g., a TX FIFO indicates that it is empty and it needs a new data sample. The agent removes the trigger ONLY when the data sample has been written by the controller AND received by the agent. Furthermore, the agent's trigger may be delayed by a few cycles before it reaches the controller. This field is used for level sensitive trigger, which reflect state (pulse sensitive triggers should have this field set to '0'). The wait cycles incurred by this field reduce DW controller performance.<br>'0': Do not wait for trigger de-activation (for pulse sensitive triggers).<br>'1': Wait for up to 4 cycles.<br>'2': Wait for up to 16 cycles.<br>'3': Wait indefinitely. This option may result in controller lockup if the trigger is not de-activated.<br><br>[3:2] INTR_TYPE<br>Specifies the input trigger type (not to be confused with the descriptor type):<br>'0': A trigger results in the execution of a single transfer. The descriptor type can be single, 1D or 2D. '1': A trigger results in the execution of a single 1D transfer.<br>- If the descriptor type is 'single', the trigger results inthe execution of a single transfer.<br>- If the descriptor type is '1D' or '2D', the trigger resultsin the execution of a 1D transfer.<br>'2': A trigger results in the execution of the current descriptor.<br>'3': A trigger results in the execution of the current descriptor and continues (without requiring another input trigger) with the execution of the next descriptor using the next descriptor's information.<br><br>[5:4] TR_OUT_TYPE<br>Specifies when an output trigger is generated:<br>'0': An output trigger is generated after a single transfer.<br>'1': An output trigger is generated after a single 1D transfer.<br>- If the descriptor type is 'single', the output trigger is generated after a single transfer.<br>- If the descriptor type is '1D', 'CRC' or '2D', the outputtrigger is generated after the execution of a 1D transfer.<br>'2': An output trigger is generated after the execution of the current descriptor.<br>'3': An output trigger is generated after the execution of a descriptor list: after the execution of the current descriptor AND the current descriptor DESCR_NEXT_PTR.ADDR is '0'.<br><br>[7:6] TR_IN_TYPE<br>Specifies the input trigger type (not to be confused with the descriptor type):<br>'0': A trigger results in the execution of a single transfer. The descriptor type can be single, 1D or 2D. '1': A trigger results in the execution of a single 1D transfer. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| | | | | | (Continuation)<br>- If the descriptor type is 'single', the trigger results inthe execution of a single transfer.<br>- If the descriptor type is '1D' or '2D', the trigger resultsin the execution of a 1D transfer.<br>'2': A trigger results in the execution of the current descriptor.<br>'3': A trigger results in the execution of the current descriptor and continues (without requiring another input trigger) with the execution of the next descriptor using the next descriptor's information.<br><br>[24] CH_DISABLE<br>Specifies whether the channel is disabled or not after completion of the current descriptor (independent of the value of the DESCR_NEXT_PTR value):<br>'0': Channel is not disabled.<br>'1': Channel is disabled.<br><br>Note: a disabled channel will ignore its input trigger.<br><br>[26] SRC_TRANSFER_SIZE<br>Specifies the bus transfer size to the source location: '0': As specified by DATA_SIZE.<br>'1': Word (32 bits).<br>Distinguishing bus transfer size from data element size allows for source components with data elements that are smaller than their 32-bit bus interface width. E.g., an ADC source has a 32-bit bus transfer size, but only provides a 16-bit data element.<br><br>[27] DST_TRANSFER_SIZE<br>Specifies the bus transfer size to the destination location:<br>'0': As specified by DATA_SIZE.<br>'1': Word (32 bits).<br>Distinguishing bus transfer size from data element size allows for destination components with data elements that are smaller than their 32-bit bus interface width.<br>E.g., a DAC destination has a 32-bit bus transfer size, but only requires a 16-bit data element.<br><br>[29:28] DATA_SIZE<br>Specifies the data element size:<br>'0': Byte (8 bits).<br>'1': Halfword (16 bits).<br>'2': Word (32 bits).<br>DATA_SIZE, SRC_TRANSFER_SIZE and DST_TRANSFER_SIZE together determine how data elements are transferred. The following are the 9 legal settings:<br>- DATA is 8 bit, SRC is 8 bit, DST is 8 bit.<br>- DATA is 8 bit, SRC is 32 bit (higher 24 bits are dropped), DST is 8 bit.<br>- DATA is 8 bit, SRC is 8 bit, DST is 32 bit (higher 24bits are made '0').<br>- DATA is 8 bit, SRC is 32 bit (higher 24 bits are dropped), DST is 32 bit (higher 24 bits are made '0'). - DATA is 16 bit, SRC is 16 bit, DST is 16 bit.<br>- DATA is 16 bit, SRC is 32 bit (higher 16 bits are dropped), DST is 16 bit.<br>- DATA is 16 bit, SRC is 16 bit, DST is 32 bit (higher16 bits are made '0').<br>- DATA is 16 bit, SRC is 32 bit (higher 16 bits are dropped), DST is 32 bit (higher 16 bits are made '0').<br>- DATA is 32 bit, SRC is 32 bit, DST is 32 bit.<br><br>[31:30] DESCR_TYPE<br>Specifies the descriptor type (not to be confused with the trigger type):<br>'0': Single transfer. The DESCR_X_CTL and DESCR_Y_CTL registers are not present and DESCR_NEXT_PTR is at offset 0x0c. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| | | | | | (Continuation)<br>'1': 1D transfer. The DESCR_X_CTL register is present, the DESCR_Y_CTL is not present and DESCR_NEXT_PTR is at offset 0x10. A 1D transfer consists out of DESCR_X_CTL.X_COUNT single transfers.<br>'2': 2D transfer. The DESCR_X_CTL and DESCR_Y_CTL registers are present and DESCR_NEXT_PTR is at offset 0x14. A 2D transfer consists of DESCR_X_CTL.X_COUNT*DESCR_Y_CTL.Y_COUNT single transfers.<br>'3': CRC transfer. The DESCR_X_CTL register is present, theDESCR_Y_CTL is not present and DESCR_NEXT_PTR is at offset 0x10. A CRC transfer consists out of DESCR_X_CTL.X_COUNT single transfers.<br><br>After the execution of the current descriptor, the DESCR_NEXT_PTR address is copied to the channel's CH_CURR_PTR address and CH_STATUS.X_IDX and CH_STATUS.Y_IDX are set to '0'. |

### 8.3.4 DW_ACT_DESCR_SRC

**Description:** Active descriptor source
**Address:** 0x40280024
**Offset:** 0x24
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | DATA | R | W | Undefined | Copy of DESCR_SRC of the currently active descriptor.<br><br>Base address of source location. |

### 8.3.5 DW_ACT_DESCR_DST

**Description:** Active descriptor destination
**Address:** 0x40280028
**Offset:** 0x28
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | DATA | R | W | Undefined | Copy of DESCR_DST of the currently active descriptor.<br><br>Base address of destination location.<br><br>Note: For a CRC transfer descriptor, this field should be programmed with the address of the CRC_LFSR_CTL register. The calculated CRC LFSR state is written to this address (through the CRYPTO AHB-Lite master interface) when the input trigger is processed. The write transfer will be submitted to the CPUSS and PERI protection schemes. |

### 8.3.6 DW_ACT_DESCR_X_CTL

**Description:** Active descriptor X loop control
**Address:** 0x40280030
**Offset:** 0x30
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** If the currently active descriptor has not X_CTL register, this MMIO register provides undefined information.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | DATA | R | W | Undefined | Copy of DESCR_X_CTL of the currently active descriptor.<br><br>[11:0] SRC_X_INCR<br>Specifies increment of source address for each X loop iteration (in multiples of SRC_TRANSFER_SIZE). This field is a signed number in the range [-2048, 2047]. If this field is '0', the source address is not incremented. This is useful for reading from RX FIFO structures.<br><br>[23:12] DST_X_INCR<br>Specifies increment of destination address for each X loop iteration (in multiples of DST_TRANSFER_SIZE). This field is a signed number in the range [-2048, 2047]. If this field is '0', the destination address is not incremented. This is useful for writing to TX FIFO structures.<br><br>Note: this field is not used for CRC transfer descriptors and must be set to '0'.<br><br>[31:24] X_COUNT<br>Number of iterations (minus 1) of the 'X loop' (X_COUNT+1 is the number of single transfers in a 1D transfer). This field is an unsigned number in the range [0, 255], representing 1 through 256 iterations.<br><br>For a single transfer descriptor type, descriptor will not have X_CTL. |

### 8.3.7 DW_ACT_DESCR_Y_CTL

**Description:** Active descriptor Y loop control
**Address:** 0x40280034
**Offset:** 0x34
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** If the currently active descriptor has not Y_CTL register, this MMIO register provides undefined information.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | DATA | R | W | Undefined | Copy of DESCR_Y_CTL of the currently active descriptor.<br><br>[11:0] SRC_Y_INCR<br>Specifies increment of source address for each Y loop iteration (in multiples of SRC_TRANSFER_SIZE). This field is a signed number in the range [-2048, 2047].<br><br>[23:12] DST_Y_INCR<br>Specifies increment of destination address for each Y loop iteration (in multiples of DST_TRANSFER_SIZE). This field is a signed number in the range [-2048, 2047].<br><br>[31:24] Y_COUNT<br>Number of iterations (minus 1) of the 'Y loop' (X_COUNT+1)*(Y_COUNT+1) is the number of single transfers in a 2D transfer). This field is an unsigned number in the range [0, 255], representing 1 through 256 iterations.<br><br>For single, 1D and CRC transfer descriptor types, descriptor will not have Y_CTL. |

### 8.3.8 DW_ACT_DESCR_NEXT_PTR

**Description:** Active descriptor next pointer
**Address:** 0x40280038
**Offset:** 0x38
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDR [7:2] | | | | | | None [1:0] | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDR [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDR [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDR [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 2:31 | ADDR | R | W | Undefined | Copy of DESCR_NEXT_PTR of the currently active descriptor.<br><br>[31:2] ADDR<br>Address of next descriptor in descriptor list. When this field is '0', this is the last descriptor in the descriptor list. |

### 8.3.9 DW_ACT_SRC

**Description:** Active source
**Address:** 0x40280040
**Offset:** 0x40
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | SRC_ADDR [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | SRC_ADDR [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | SRC_ADDR [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | SRC_ADDR [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | SRC_ADDR | R | W | Undefined | Current address of source location. |

### 8.3.10 DW_ACT_DST

**Description:** Active destination
**Address:** 0x40280044
**Offset:** 0x44
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DST_ADDR [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | DST_ADDR [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | DST_ADDR [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | DST_ADDR [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | DST_ADDR | R | W | Undefined | Current address of destination location. |

### 8.3.11 DW_ECC_CTL

**Description:** ECC control
**Address:** 0x40280080
**Offset:** 0x80
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | WORD_ADDR [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:10] | | | | | | WORD_ADDR [9:8] | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | PARITY [31:25] | | | | | | | None [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:9 | WORD_ADDR | RW | R | 0 | Specifies the word address where an error will be injected.<br>- On a write transfer to this SRAM word address and when CTL.ECC_INJ_EN bit is '1', the parity (PARITY) is injected. |
| 25:31 | PARITY | RW | R | 0 | ECC parity to use for ECC error injection at address WORD_ADDR. |

### 8.3.12 DW_CRC_CTL

**Description:** CRC control
**Address:** 0x40280100
**Offset:** 0x100
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:1] | | | | | | | DATA_REVERSE [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:9] | | | | | | | REM_REVERSE [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | DATA_REVERSE | RW | R | 0 | Specifies the bit order in which a data Byte is processed (reversal is performed after XORing):<br>'0': Most significant bit (bit 1) first.<br>'1': Least significant bit (bit 0) first. |
| 8 | REM_REVERSE | RW | R | 0 | Specifies whether the remainder is bit reversed (reversal is performed after XORing):<br>'0': No.<br>'1': Yes. |

### 8.3.13 DW_CRC_DATA_CTL

**Description:** CRC data control
**Address:** 0x40280110
**Offset:** 0x110
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA_XOR [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | DATA_XOR | RW | R | 0 | Specifies a byte mask with which each data byte is XOR'd. The XOR is performed before data reversal. |

### 8.3.14 DW_CRC_POL_CTL

**Description:** CRC polynomial control
**Address:** 0x40280120
**Offset:** 0x120
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | POLYNOMIAL [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | POLYNOMIAL [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | POLYNOMIAL [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | POLYNOMIAL [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | POLYNOMIAL | RW | R | 0 | CRC polynomial. The polynomial is represented WITHOUT the high order bit (this bit is always assumed '1'). The polynomial should be aligned/shifted such that the more significant bits (bit 31 and down) contain the polynomial and the less significant bits (bit 0 and up) contain padding '0's. Some frequently used polynomials:<br>- CRC32: POLYNOMIAL is 0x04c11db7 (x^32 + x^26 + x^23 + x^22 + x^16 + x^12 + x^11 + x^10 + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1).<br>- CRC16: POLYNOMIAL is 0x80050000 (x^16 + x^15 + x^2 + 1, shifted by 16 bit positions).<br>- CRC16 CCITT: POLYNOMIAL is 0x10210000 (x^16 + x^12 + x^5 + 1, shifted by 16 bit positions). |

### 8.3.15 DW_CRC_LFSR_CTL

**Description:** CRC LFSR control
**Address:** 0x40280130
**Offset:** 0x130
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | LFSR32 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | LFSR32 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | LFSR32 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | LFSR32 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | LFSR32 | RW | RW | 0 | State of a 32-bit Linear Feedback Shift Registers (LFSR) that is used to implement CRC. This register needs to be initialized by SW to provide the CRC seed value.<br><br>The seed value should be aligned such that the more significant bits (bit 31 and down) contain the seed value and the less significant bits (bit 0 and up) contain padding '0's.<br><br>Note that SW can write this field. This functionality can be used prevent information leakage (through either CRC_LFSR_CTL or CRC_REM_RESULT). |

### 8.3.16 DW_CRC_REM_CTL

**Description:** CRC remainder control
**Address:** 0x40280140
**Offset:** 0x140
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | REM_XOR [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | REM_XOR [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | REM_XOR [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | REM_XOR [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | REM_XOR | RW | R | 0 | Specifies a mask with which the CRC_LFSR_CTL.LFSR32 register is XOR'd to produce a remainder. The XOR is performed before remainder reversal. |

### 8.3.17 DW_CRC_REM_RESULT

**Description:** CRC remainder result
**Address:** 0x40280148
**Offset:** 0x148
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | REM [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | REM [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | REM [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | REM [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | REM | R | W | 0 | Remainder value. The alignment of the remainder depends on CRC_REM_CTL0.REM_REVERSE:<br>'0': the more significant bits (bit 31 and down) contain the remainder.<br>'1': the less significant bits (bit 0 and up) contain the remainder.<br><br>Note: This field is combinatorially derived from CRC_LFSR_CTL.LFSR32, CRC_CTL.REM_REVERSE and CRC_REM_CTL.REM_XOR. |

### 8.3.18 CH_STRUCT

#### 8.3.18.1 DW_CH_STRUCT_CH_CTL

**Description:** Channel control
**Address:** 0x40288000
**Offset:** 0x0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** Undefined as one or more bit fields have a default value that is undefined

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | PC [7:4] | | | | None [3:3] | B [2:2] | NS [1:1] | P [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:12] | | | | PREEMPTABLE [11:11] | None [10:10] | PRIO [9:8] | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | ENABLED [31:31] | None [30:24] | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | P | RW | R | Undefined | User/privileged access control:<br>'0': user mode.<br>'1': privileged mode.<br><br>This field is set with the user/privileged access control of the transaction that writes this register; i.e. the 'write data' is ignored and instead the access control is inherited from the write transaction (note the field attributes should be HW:RW, SW:R).<br><br>All transactions for this channel use the P field for the user/privileged access control ('hprot[1]'). |
| 1 | NS | RW | R | Undefined | Secure/on-secure access control:<br>'0': secure.<br>'1': non-secure.<br><br>This field is set with the secure/non-secure access control of the transaction that writes this register; i.e. the 'write data' is ignored and instead the access control is inherited from the write transaction (note the field attributes should be HW:RW, SW:R).<br><br>All transactions for this channel use the NS field for the secure/non-secure access control ('hprot[4]'). |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 2 | B | RW | R | Undefined | Non-bufferable/bufferable access control:<br>'0': non-bufferable.<br>'1': bufferable.<br><br>This field is used to indicate to an AMBA bridge that a write transaction can complete without waiting for the destination to accept the write transaction data.<br><br>All transactions for this channel uses the B field for the non-bufferable/bufferable access control ('hprot[2]'). |
| 4:7 | PC | RW | R | Undefined | Protection context.<br><br>This field is set with the protection context of the transaction that writes this register; i.e. the 'write data' is ignored and instead the context is inherited from the write transaction (note the field attributes should be HW:RW, SW:R).<br><br>All transactions for this channel uses the PC field for the protection context. |
| 8:9 | PRIO | RW | R | 0 | Channel priority:<br>'0': highest priority.<br>'1'<br>'2'<br>'3': lowest priority.<br><br>Channels with the same priority constitute a priority group. Priority decoding determines the highest priority pending channel. This channel is determined as follows. First, the highest priority group with pending channels is identified. Second, within this priority group, round robin arbitration is applied. Round robin arbitration (within a priority group) gives the highest priority to the lower channel indices (within the priority group). |
| 11 | PREEMPTABLE | RW | R | Undefined | Specifies if the channel is preemptable.<br>'0': Not preemptable.<br>'1': Preemptable. This field allows higher priority pending channels (from a higher priority group; i.e. an active channel can NOT be preempted by a pending channel in the same priority group) to preempt the active channel in between 'single transfers' (a 1D transfer consists out of X_COUNT single transfers; a 2D transfer consists out of X_COUNT*Y_COUNT single transfers). Preemption will NOT affect the pending status of channel. As a result, after completion of a higher priority activated channel, the current channel may be reactivated. |
| 31 | ENABLED | RW | RW1C | 0 | Channel enable:<br>'0': Disabled. The channel's trigger is ignored and the channel cannot be made pending and therefore cannot be made active. If a pending channel is disabled, the channel is made non pending. If the activate channel is disabled, the channel is de-activated (bus transactions are completed).<br>'1': Enabled.<br><br>SW sets this field to '1' to enable a specific channel.<br><br>HW sets this field to '0' on an error interrupt cause (the specific error is specified by CH_STATUS.INTR_CAUSE). |

### 8.3.18.2 DW_CH_STRUCT_CH_STATUS

**Description:** Channel status
**Address:** 0x40288004
**Offset:** 0x4
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** Undefined as one or more bit fields have a default value that is undefined

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:4] | | | | INTR_CAUSE [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | PENDING [31:31] | None [30:24] | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | INTR_CAUSE | R | W | Undefined | Specifies the source of the interrupt cause:<br>'0': No interrupt generated<br>'1': Interrupt based on transfer complettion configuration based on INTR_TYPE<br>'2': Source transfer bus error<br>'3': Destination transfer bus error<br>'4': Source address misalignment<br>'5': Destination address misalignment<br>'6': Current descriptor pointer is null<br>'7': Active channel is disabled<br>'8': Descriptor bus error<br>'9'-'15': Not used.<br><br>For error related interrupt causes (INTR_CAUSE is '2', '3', ..., '8'), the channel is disabled (HW sets CH_CTL.ENABLED to '0'). |
| 31 | PENDING | R | W | 0 | Specifies pending DW channels; i.e. enabled channels whose trigger got activated. This field includes all channels that are in the pending state (not scheduled) or active state (scheduled and performing data transfer(s)). |

### 8.3.18.3 DW_CH_STRUCT_CH_IDX

**Description:** Channel current indices
**Address:** 0x40288008
**Offset:** 0x8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Note that this register is retained during DeepSleep system power mode.
**Default:** Undefined as one or more bit fields have a default value that is undefined

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | X_IDX [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | Y_IDX [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | X_IDX | RW | RW | Undefined | Specifies the X loop index. In the range of [0, X_COUNT], with X_COUNT taken from the current descriptor.<br><br>Note: HW sets this field to '0' when it updates the current descriptor pointer CH_CURR_PTR with DESCR_NEXT_PTR after execution of the current descriptor.<br><br>Note: SW should set this field to '0' when it updates CH_CURR_PTR. |
| 8:15 | Y_IDX | RW | RW | Undefined | Specifies the Y loop index, with X_COUNT taken from the current descriptor.<br><br>Note: HW sets this field to '0' when it updates the current descriptor pointer CH_CURR_PTR with DESCR_NEXT_PTR after execution of the current descriptor.<br><br>Note: SW should set this field to '0' when it updates CH_CURR_PTR. |

### 8.3.18.4 DW_CH_STRUCT_CH_CURR_PTR

**Description:** Channel current descriptor pointer
**Address:** 0x4028800C
**Offset:** 0xC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** Undefined as one or more bit fields have a default value that is undefined

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDR [7:2] | | | | | | None [1:0] | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDR [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDR [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDR [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 2:31 | ADDR | RW | RW | Undefined | Address of current descriptor. When this field is '0', there is no valid descriptor.<br><br>Note: HW updates the current descriptor pointer CH_CURR_PTR with DESCR_NEXT_PTR after execution of the current descriptor.<br><br>Note: Typically, when SW updates the current descriptor pointer CH_CURR_PTR, it also sets CH_IDX.X_IDX and CH_IDX.Y_IDX to '0'. |

### 8.3.18.5 DW_CH_STRUCT_INTR

**Description:** Interrupt
**Address:** 0x40288010
**Offset:** 0x10
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** The register fields are not retained. This is to ensure that they come up as '0' after coming out of DeepSleep system power mode.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:1] | | | | | | | CH [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | CH | RW1C | RW1S | 0 | Set to '1', when event (as specified by CH_STATUS.INTR_CAUSE) is detected. Write INTR.CH field with '1', to clear bit. Write INTR_SET.CH field with '1', to set bit. |

### 8.3.18.6 DW_CH_STRUCT_INTR_SET

**Description:** Interrupt set
**Address:** 0x40288014
**Offset:** 0x14
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** When read, this register reflects the INTR register.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:1] | | | | | | | CH [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | CH | RW1S | A | 0 | Write INTR_SET field with '1' to set corresponding INTR.CH field (a write of '0' has no effect). |

### 8.3.18.7 DW_CH_STRUCT_INTR_MASK

**Description:** Interrupt mask
**Address:** 0x40288018
**Offset:** 0x18
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:1] | | | | | | | CH [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | CH | RW | R | 0 | Mask for corresponding field in INTR register. |

### 8.3.18.8 DW_CH_STRUCT_INTR_MASKED

**Description:** Interrupt masked
**Address:** 0x4028801C
**Offset:** 0x1C
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** When read, this register reflects a bitwise AND between the INTR and INTR_MASK registers. This register allows SW to read the status of all mask enabled interrupt causes with a single load operation, rather than two load operations: one for INTR and one for INTR_MASK. This simplifies Firmware development. The associated interrupt is active ('1'), when INTR_MASKED != 0.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:1] | | | | | | | CH [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | CH | R | W | 0 | Logical and of corresponding INTR and INTR_MASK fields. |

### 8.3.18.9 DW_CH_STRUCT_SRAM_DATA0

**Description:** SRAM data 0
**Address:** 0x40288020
**Offset:** 0x20
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** SRAM_DATA0 and SRAM_DATA1 are provided for ECC fault injection functionality. These register should NOT be used to control regular functionality (except that they can be used for initialization of DW SRAMs).

Some of the CH_CTL, CH_STATUS, CH_IDX and CH_CURR_PTR fields are implemented using SRAM storage. Each channel uses two 32-bit SRAM data words. The fields of a register that are implemented using SRAM storage are mapped on a subset of either of the two 32-bit SRAM data words. Specifically, the first 32-bit SRAM data word implements CH_CTL.P, CH_CTL.NS, CH_CTL.B, CH_CTL.PC, CH_CTL.PREEMPTABLE, CH_IDX.X_IDX and CH_IDX.Y_IDX fields and the second 32-bit SRAM data word implements the CH_CURR_PTR.ADDR field. As a result, CH_CTL, CH_IDX and CH_CURR_PTR writes only update a subset of a 32-bit SRAM data word.

For ECC fault injection, it is required to update a complete 32-bit SRAM data word with a user provided ECC parity (specified by ECC_CTL.PARITY) at a specific SRAM location (specified by ECC_CTL.WORD_ADDR). Therefore, SRAM_DATA0 and SRAM_DATA1 provide access to specific SRAM locations. For a channel i, SRAM_DATA0 provides access to SRAM word address 2*i and SRAM_DATA1 provides access to SRAM word address 2*i + 1. E.g., to inject a fault at SRAM word address '13', CTL.ECC_INJ_EN is set to '1', ECC_CTL.WORD_ADDR is set to '13', and ECC_CTL.PARITY is set to the faulting parity. Next, the SW performs a 32-bit write to SRAM_DATA1 of channel 6 (2*6 + 1 = 13). The write data and the faulting parity is written to SRAM word address '13'.
**Default:** Undefined as one or more bit fields have a default value that is undefined

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | DATA | RW | RW | Undefined | N/A |

### 8.3.18.10 DW_CH_STRUCT_SRAM_DATA1

**Description:** SRAM data 1
**Address:** 0x40288024
**Offset:** 0x24
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** Undefined as one or more bit fields have a default value that is undefined

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | DATA | RW | RW | Undefined | N/A |

### 8.3.18.11 DW_CH_STRUCT_TR_CMD

**Description:** Channel software trigger
**Address:** 0x40288028
**Offset:** 0x28
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:1] | | | | | | | ACTIVATE [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | ACTIVATE | RW1S | A | 0 | Software trigger. When written with '1', a trigger is generated which sets 'trigger pending' (only if the channel is enabled). A read always returns a 0. |

# 9 EFUSE

**Description** EFUSE MXS40 registers
**Base Address** 0x402C0000
**Size** 0x200
**Slave Num** MMIO2 - 10

# 10 EFUSE_DATA

**Description** eFUSE memory
**Base Address** 0x402C0800
**Size** 0x200
**Slave Num** MMIO2 - 10

| Register Name | Address | Permission | Description |
|---|---|---|---|
| EFUSE_DATA_CUSTOMER_DATA0 | 0x402C0868 | NO-ACCESS | Available EFUSE bits for customer usage.They can be programmed in NORMAL protection state via CMx/DAP and in SECURE protection state via CMx. |
| EFUSE_DATA_CUSTOMER_DATA1 | 0x402C086C | NO-ACCESS | Available EFUSE bits for customer usage.They can be programmed in NORMAL protection state via CMx/DAP and in SECURE protection state via CMx. |
| EFUSE_DATA_CUSTOMER_DATA2 | 0x402C0870 | NO-ACCESS | Available EFUSE bits for customer usage.They can be programmed in NORMAL protection state via CMx/DAP and in SECURE protection state via CMx. |
| EFUSE_DATA_CUSTOMER_DATA3 | 0x402C0874 | NO-ACCESS | Available EFUSE bits for customer usage.They can be programmed in NORMAL protection state via CMx/DAP and in SECURE protection state via CMx. |
| EFUSE_DATA_CUSTOMER_DATA4 | 0x402C0878 | NO-ACCESS | Available EFUSE bits for customer usage.They can be programmed in NORMAL protection state via CMx/DAP and in SECURE protection state via CMx. |
| EFUSE_DATA_CUSTOMER_DATA5 | 0x402C087C | NO-ACCESS | Available EFUSE bits for customer usage.They can be programmed in NORMAL protection state via CMx/DAP and in SECURE protection state via CMx. |

## 10.1 Register Details

### 10.1.1 EFUSE_DATA_CUSTOMER_DATA

**Description:** Available EFUSE bits for customer usage.They can be programmed in NORMAL protection state via CMx/DAP and in SECURE protection state via CMx.
**Address:** 0x402C0868
**Offset:** 0x68
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** The eFUSE memory consists of an array of eFUSE macros. The memory can only be read with AHB-Lite Byte read transfers. A non-Byte AHB-Lite read transfer results in an AHB-Lite bus error. An AHB-Lite write transfer results in an AHB-Lite bus error. Furthermore, an AHB-Lite read transfer while a program operation is in progress (CMD.START is '1') results in an AHB-Lite bus error.

The number of eFUSE memory Bytes is determined by the EFUSE_NR configuration parameter. This parameter specifies the number of instantiated eFUSE macros. Each macro has 16 Bytes. E.g., if EFUSE_NR is 8, the eFUSE memory has 8*16 Bytes = 128 Bytes.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA_BYTE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA_BYTE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA_BYTE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA_BYTE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | DATA_BYTE | RW | R | 0 | Available EFUSE bits for customer usage.They can be programmed in NORMAL protection state via CMx/DAP and in SECURE protection state via CMx. |

# 11 ETH

## 11.1 ETH 0

**Description** Ethernet Interface
**Base Address** 0x40480000
**Size** 0x10000
**Slave Num** MMIO4 - 2

| Register Name | Address | Permission | Description |
|---|---|---|---|
| ETH0_CTL | 0x40480000 | FULL | MXETH Control Register |
| ETH0_STATUS | 0x40480004 | FULL | MXETH Status Register |
| ETH0_NETWORK_CONTROL | 0x40481000 | FULL | The network control register contains general MAC control functions for both receiver and transmitter. |
| ETH0_NETWORK_CONFIG | 0x40481004 | FULL | The network configuration register contains functions for setting the mode of operation for the Gigabit Ethernet MAC. |
| ETH0_NETWORK_STATUS | 0x40481008 | FULL | The network status register returns status information with respect to the PHY management interface. |
| ETH0_USER_IO_REGISTER | 0x4048100C | FULL | Not presents. Access to the register will return AHB error. |
| ETH0_DMA_CONFIG | 0x40481010 | FULL | DMA Configuration Register |
| ETH0_TRANSMIT_STATUS | 0x40481014 | FULL | This register, when read, provides details of the status of a transmit. Once read, individual bits may be cleared by writing 1 to them. It is not possible to set a bit to 1 by writing to the register. |
| ETH0_RECEIVE_Q_PTR | 0x40481018 | FULL | This register holds the start address of the receive buffer queue (receive buffers descriptor list). The receive buffer queue base address must be initialized before receive is enabled through bit 2 of the network control register. Once reception is enabled, any write to the receive buffer queue base address register is ignored. Reading this register returns the location of the descriptor currently being accessed. This value increments as buffers are used. Software should not use this register for determining where to remove received frames from the queue as it constantly changes as new frames are received. Software should instead work its way through the buffer descriptor queue checking the used bits. In terms of AMBA (AXI) operation, the receive descriptors are read from memory using a single 32bit AXI access. When the datapath is configured at 64bit, the receive descriptors should be aligned at 64-bit boundaries and each pair of 32-bit descriptors is written to using a single 64bit AXI access. |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| ETH0_TRANSMIT_Q_PTR | 0x4048101C | FULL | This register holds the start address of the transmit buffer queue (transmit buffers descriptor list). The transmit buffer queue base address register must be initialized before transmit is started through bit 9 of the network control register. Once transmission has started, any write to the transmit buffer queue base address register is illegal and therefore ignored. Note that due to clock boundary synchronization, it takes a maximum of four pclk cycles from the writing of the transmit start bit before the transmitter is active. Writing to the transmit buffer queue base address register during this time may produce unpredictable results. Reading this register returns the location of the descriptor currently being accessed. Because the DMA can store data for multiple frames at once, this may not necessarily be pointing to the current frame being transmitted. In terms of AMBA AXI operation, the transmit descriptors are written to memory using a single 32bit AHB access. When the datapath is configured as 64bit, the transmit descriptors should be aligned at 64-bit boundaries and each pair of 32-bit descriptors is read from memory using a single AXI access. |
| ETH0_RECEIVE_STATUS | 0x40481020 | FULL | This register, when read provides details of the status of a receive. Once read, individual bits may be cleared by writing 1 to them. It is not possible to set a bit to 1 by writing to the register. |
| ETH0_INT_STATUS | 0x40481024 | FULL | If not configured for priority queueing, the GEM generates a single interrupt. This register indicates the source of this interrupt. The corresponding bit in the mask register must be clear for a bit to be set. If any bit is set in this register the ethernet_int signal will be asserted. For test purposes each bit can be set or reset by writing to the interrupt mask register. The default configuration is shown below whereby all bits are reset to zero on read. Changing the validity of the `gem_irq_read_clear define will instead require a one to be written to the appropriate bit in order to clear it. In this mode reading has no affect on the status of the bit. |
| ETH0_INT_ENABLE | 0x40481028 | FULL | At reset all interrupts are disabled. Writing a one to the relevant bit location enables the required interrupt. This register is write only and when read will return zero. |
| ETH0_INT_DISABLE | 0x4048102C | FULL | Writing a 1 to the relevant bit location disables that particular interrupt. This register is write only and when read will return zero. |
| ETH0_INT_MASK | 0x40481030 | FULL | The interrupt mask register is a read only register indicating which interrupts are masked. All bits are set at reset and can be reset individually by writing to the interrupt enable register or set individually by writing to the interrupt disable register. Having separate address locations for enable and disable saves the need for performing a read modify write when updating the interrupt mask register. For test purposes there is a write-only function to this register that allows the bits in the interrupt status register to be set or cleared, regardless of the state of the mask register. |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| ETH0_PHY_MANAGEMENT | 0x40481034 | FULL | The PHY maintenance register is implemented as a shift register. Writing to the register starts a shift operation which is signalled as complete when bit-2 is set in the network status register. It takes about 2000 pclk cycles to complete, when MDC is set for pclk divide by 32 in the network configuration register. An interrupt is generated upon completion. During this time, the MSB of the register is output on the MDIO pin and the LSB updated from the MDIO pin with each MDC cycle. This causes transmission of a PHY management frame on MDIO. See Section 22.2.4.5 of the IEEE 802.3 standard. Reading during the shift operation will return the current contents of the shift register. At the end of management operation, the bits will have shifted back to their original locations. For a read operation, the data bits will be updated with data read from the PHY. It is important to write the correct values to the register to ensure a valid PHY management frame is produced. The MDIO interface can read IEEE 802.3 clause 45 PHYs as well as clause 22 PHYs. To read clause 45 PHYs, bit 30 should be written with a 0 rather than a 1. For a description of MDC generation, see Network Configuration Register. |
| ETH0_PAUSE_TIME | 0x40481038 | FULL | Received Pause Quantum Register |
| ETH0_TX_PAUSE_QUANTUM | 0x4048103C | FULL | Transmit Pause Quantum Register |
| ETH0_PBUF_TXCUTTHRU | 0x40481040 | FULL | Partial store and forward is only applicable when using the DMA configured in SRAM based packet buffer mode. It is also not available when using multi buffer frames. TX Partial Store and Forward |
| ETH0_PBUF_RXCUTTHRU | 0x40481044 | FULL | RX Partial Store and Forward |
| ETH0_JUMBO_MAX_LENGTH | 0x40481048 | FULL | Maximum Jumbo Frame Size. |
| ETH0_EXTERNAL_FIFO_INTERFACE | 0x4048104C | FULL | Not presents. |
| ETH0_AXI_MAX_PIPELINE | 0x40481054 | FULL | Used to set the maximum amount of outstanding transactions on the AXI bus between AR / R channels and AW / W channels. Cannot be more than the depth of the configured AXI pipeline FIFO (defined in verilog defs.v) |
| ETH0_RSC_CONTROL | 0x40481058 | FULL | Not presents. Access to the register will return AHB error. |
| ETH0_INT_MODERATION | 0x4048105C | FULL | Used to moderate the number of transmit and receive complete interrupts issued. With interrupt moderation enabled receive and transmit interrupts are not generated immediately a frame is transmitted or received. Instead when a receive or transmit event occurs a timer is started and the interrupt is asserted after it times out. This limits the frequency with which the CPU receives interrupts. When interrupt moderation is enabled interrupt status bit one is always used for receive and bit 7 is always used for transmit even when priority queuing is enabled. With interrupt moderation 800ns periods are counted. GEM determines what constitutes an 800ns period by looking at the tbi (bit 11), gigabit bit (10) and speed (bit 0) bits in the network configuration register and counting tx_clk cycles. Bit 0 needs to be set to 1 for 100M operation. |
| ETH0_SYS_WAKE_TIME | 0x40481060 | FULL | Used to pause transmission after deassertion of tx_lpi_en. Each unit in this register corresponds to 64ns in gigabit mode, 320ns in 100M mode and 3200ns at 10M. After tx_lpi_en is deasserted transmission will pause for the set time. |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| ETH0_HASH_BOTTOM | 0x40481080 | FULL | The unicast hash enable and the multicast hash enable bits in the network configuration register enable the reception of hash matched frames. Hash Register Bottom (31 to 0 bits) |
| ETH0_HASH_TOP | 0x40481084 | FULL | Hash Register Top (63 to 32 bits) |
| ETH0_SPEC_ADD1_BOTTOM | 0x40481088 | FULL | The addresses stored in the specific address registers are deactivated at reset or when their corresponding specific address register bottom is written. They are activated when specific address register top is written. |
| ETH0_SPEC_ADD1_TOP | 0x4048108C | FULL | Specific Address Top |
| ETH0_SPEC_ADD2_BOTTOM | 0x40481090 | FULL | The addresses stored in the specific address registers are deactivated at reset or when their corresponding specific address register bottom is written. They are activated when specific address register top is written. |
| ETH0_SPEC_ADD2_TOP | 0x40481094 | FULL | Specific Address Top |
| ETH0_SPEC_ADD3_BOTTOM | 0x40481098 | FULL | The addresses stored in the specific address registers are deactivated at reset or when their corresponding specific address register bottom is written. They are activated when specific address register top is written. |
| ETH0_SPEC_ADD3_TOP | 0x4048109C | FULL | Specific Address Top |
| ETH0_SPEC_ADD4_BOTTOM | 0x404810A0 | FULL | The addresses stored in the specific address registers are deactivated at reset or when their corresponding specific address register bottom is written. They are activated when specific address register top is written. |
| ETH0_SPEC_ADD4_TOP | 0x404810A4 | FULL | Specific Address Top |
| ETH0_SPEC_TYPE1 | 0x404810A8 | FULL | Type ID Match 1 |
| ETH0_SPEC_TYPE2 | 0x404810AC | FULL | Type ID Match 2 |
| ETH0_SPEC_TYPE3 | 0x404810B0 | FULL | Type ID Match 3 |
| ETH0_SPEC_TYPE4 | 0x404810B4 | FULL | Type ID Match 4 |
| ETH0_WOL_REGISTER | 0x404810B8 | FULL | Wake on LAN Register. Presents in design, but feature is not supported. |
| ETH0_STRETCH_RATIO | 0x404810BC | FULL | IPG stretch register |
| ETH0_STACKED_VLAN | 0x404810C0 | FULL | Stacked VLAN Register |
| ETH0_TX_PFC_PAUSE | 0x404810C4 | FULL | Transmit PFC Pause Register |
| ETH0_MASK_ADD1_BOTTOM | 0x404810C8 | FULL | Specific Address Mask 1 Bottom (31 to 0 bits) |
| ETH0_MASK_ADD1_TOP | 0x404810CC | FULL | Specific Address Mask 1 Top (47 to 32 bits) |
| ETH0_DMA_ADDR_OR_MASK | 0x404810D0 | FULL | Receive DMA Data Buffer Address Mask |
| ETH0_RX_PTP_UNICAST | 0x404810D4 | FULL | PTP RX unicast IP destination address |
| ETH0_TX_PTP_UNICAST | 0x404810D8 | FULL | PTP TX unicast IP destination address |
| ETH0_TSU_NSEC_CMP | 0x404810DC | FULL | TSU timer comparison value nanoseconds |
| ETH0_TSU_SEC_CMP | 0x404810E0 | FULL | TSU timer comparison value seconds (31 to 0 bits) |
| ETH0_TSU_MSB_SEC_CMP | 0x404810E4 | FULL | TSU timer comparison value seconds (47 to 32 bits) |
| ETH0_TSU_PTP_TX_MSB_SEC | 0x404810E8 | FULL | PTP Event Frame Transmitted Seconds Register (47 to 32 bits) |
| ETH0_TSU_PTP_RX_MSB_SEC | 0x404810EC | FULL | PTP Event Frame Received Seconds Register (47 to 32 bits) |
| ETH0_TSU_PEER_TX_MSB_SEC | 0x404810F0 | FULL | PTP Peer Event Frame Transmitted Seconds Register (47 to 32 bits) |
| ETH0_TSU_PEER_RX_MSB_SEC | 0x404810F4 | FULL | PTP Peer Event Frame Received Seconds Register (47 to 32 bits) |
| ETH0_DPRAM_FILL_DBG | 0x404810F8 | FULL | The fill levels for the TX & RX packet buffers can be read using this register, including the fill level for each queue in the TX direction. |
| ETH0_REVISION_REG | 0x404810FC | FULL | This register indicates a Cadence module identification number and module revision. The value of this register is read only as defined by `gem_revision_reg_value |
| ETH0_OCTETS_TXED_BOTTOM | 0x40481100 | FULL | Octets Transmitted lower bits (31 to 0 bits) |
| ETH0_OCTETS_TXED_TOP | 0x40481104 | FULL | Octets Transmitted higher bits (47 to 32 bits) |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| ETH0_FRAMES_TXED_OK | 0x40481108 | FULL | Frames Transmitted |
| ETH0_BROADCAST_TXED | 0x4048110C | FULL | Broadcast Frames Transmitted |
| ETH0_MULTICAST_TXED | 0x40481110 | FULL | Multicast Frames Transmitted |
| ETH0_PAUSE_FRAMES_TXED | 0x40481114 | FULL | Pause Frames Transmitted |
| ETH0_FRAMES_TXED_64 | 0x40481118 | FULL | 64 Byte Frames Transmitted |
| ETH0_FRAMES_TXED_65 | 0x4048111C | FULL | 65 to 127 Byte Frames Transmitted |
| ETH0_FRAMES_TXED_128 | 0x40481120 | FULL | 128 to 255 Byte Frames Transmitted |
| ETH0_FRAMES_TXED_256 | 0x40481124 | FULL | 256 to 511 Byte Frames Transmitted |
| ETH0_FRAMES_TXED_512 | 0x40481128 | FULL | 512 to 1023 Byte Frames Transmitted |
| ETH0_FRAMES_TXED_1024 | 0x4048112C | FULL | 1024 to 1518 Byte Frames Transmitted |
| ETH0_FRAMES_TXED_1519 | 0x40481130 | FULL | Greater Than 1518 Byte Frames Transmitted |
| ETH0_TX_UNDERRUNS | 0x40481134 | FULL | Transmit Under Runs |
| ETH0_SINGLE_COLLISIONS | 0x40481138 | FULL | Single Collision Frames. Presents in design but not support. |
| ETH0_MULTIPLE_COLLISIONS | 0x4048113C | FULL | Multiple Collision Frames. Presents in design but not support. |
| ETH0_EXCESSIVE_COLLISIONS | 0x40481140 | FULL | Excessive Collisions. Presents in design but not support. |
| ETH0_LATE_COLLISIONS | 0x40481144 | FULL | Late Collisions. Presents in design but not support. |
| ETH0_DEFERRED_FRAMES | 0x40481148 | FULL | Deferred Transmission Frames. Presents in design but not support. |
| ETH0_CRS_ERRORS | 0x4048114C | FULL | Carrier Sense Errors. Presents in design but not support. |
| ETH0_OCTETS_RXED_BOTTOM | 0x40481150 | FULL | Octets Received (31 to 0 bits) |
| ETH0_OCTETS_RXED_TOP | 0x40481154 | FULL | Octets Received (47 to 32 bits) |
| ETH0_FRAMES_RXED_OK | 0x40481158 | FULL | Frames Received |
| ETH0_BROADCAST_RXED | 0x4048115C | FULL | Broadcast Frames Received |
| ETH0_MULTICAST_RXED | 0x40481160 | FULL | Multicast Frames Received |
| ETH0_PAUSE_FRAMES_RXED | 0x40481164 | FULL | Pause Frames Received |
| ETH0_FRAMES_RXED_64 | 0x40481168 | FULL | 64 Byte Frames Received |
| ETH0_FRAMES_RXED_65 | 0x4048116C | FULL | 65 to 127 Byte Frames Received |
| ETH0_FRAMES_RXED_128 | 0x40481170 | FULL | 128 to 255 Byte Frames Received |
| ETH0_FRAMES_RXED_256 | 0x40481174 | FULL | 256 to 511 Byte Frames Received |
| ETH0_FRAMES_RXED_512 | 0x40481178 | FULL | 512 to 1023 Byte Frames Received |
| ETH0_FRAMES_RXED_1024 | 0x4048117C | FULL | 1024 to 1518 Byte Frames Received |
| ETH0_FRAMES_RXED_1519 | 0x40481180 | FULL | 1519 to maximum Byte Frames Received |
| ETH0_UNDERSIZE_FRAMES | 0x40481184 | FULL | Undersized Frames Received |
| ETH0_EXCESSIVE_RX_LENGTH | 0x40481188 | FULL | Oversize Frames Received |
| ETH0_RX_JABBERS | 0x4048118C | FULL | Jabbers Received |
| ETH0_FCS_ERRORS | 0x40481190 | FULL | Frame Check Sequence Errors |
| ETH0_RX_LENGTH_ERRORS | 0x40481194 | FULL | Length Field Frame Errors |
| ETH0_RX_SYMBOL_ERRORS | 0x40481198 | FULL | Receive Symbol Errors |
| ETH0_ALIGNMENT_ERRORS | 0x4048119C | FULL | Alignment Errors |
| ETH0_RX_RESOURCE_ERRORS | 0x404811A0 | FULL | Receive Resource Errors |
| ETH0_RX_OVERRUNS | 0x404811A4 | FULL | Receive Overruns |
| ETH0_RX_IP_CK_ERRORS | 0x404811A8 | FULL | IP Header Checksum Errors |
| ETH0_RX_TCP_CK_ERRORS | 0x404811AC | FULL | TCP Checksum Errors |
| ETH0_RX_UDP_CK_ERRORS | 0x404811B0 | FULL | UDP Checksum Errors |
| ETH0_AUTO_FLUSHED_PKTS | 0x404811B4 | FULL | Receive DMA Flushed Packets |
| ETH0_TSU_TIMER_INCR_SUB_NSEC | 0x404811BC | FULL | 1588 Timer Increment Register sub nsec |
| ETH0_TSU_TIMER_MSB_SEC | 0x404811C0 | FULL | 1588 Timer Seconds Register (47 to 32 bits) |
| ETH0_TSU_STROBE_MSB_SEC | 0x404811C4 | FULL | 1588 Timer Sync Strobe Seconds Register (47 to 32 bits) |
| ETH0_TSU_STROBE_SEC | 0x404811C8 | FULL | 1588 Timer Sync Strobe Seconds Register (31 to 0 bits) |
| ETH0_TSU_STROBE_NSEC | 0x404811CC | FULL | 1588 Timer Sync Strobe Nanoseconds Register |
| ETH0_TSU_TIMER_SEC | 0x404811D0 | FULL | 1588 Timer Seconds Register (31 to 0 bits) |
| ETH0_TSU_TIMER_NSEC | 0x404811D4 | FULL | 1588 Timer Nanoseconds Register |
| ETH0_TSU_TIMER_ADJUST | 0x404811D8 | FULL | This register is used to adjust the value of the timer in the TSU. It allows an integral number of nanoseconds to be added or subtracted from the timer in a one-off operation. This register returns all zeroes when read. |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| ETH0_TSU_TIMER_INCR | 0x404811DC | FULL | 1588 Timer Increment Register |
| ETH0_TSU_PTP_TX_SEC | 0x404811E0 | FULL | PTP Event Frame Transmitted Seconds Register (31 to 0 bits) |
| ETH0_TSU_PTP_TX_NSEC | 0x404811E4 | FULL | PTP Event Frame Transmitted Nanoseconds Register |
| ETH0_TSU_PTP_RX_SEC | 0x404811E8 | FULL | PTP Event Frame Received Seconds Register (31 to 0 bits) |
| ETH0_TSU_PTP_RX_NSEC | 0x404811EC | FULL | PTP Event Frame Received Nanoseconds Register |
| ETH0_TSU_PEER_TX_SEC | 0x404811F0 | FULL | PTP Peer Event Frame Transmitted Seconds Register (31 to 0 bits) |
| ETH0_TSU_PEER_TX_NSEC | 0x404811F4 | FULL | PTP Peer Event Frame Transmitted Nanoseconds Register |
| ETH0_TSU_PEER_RX_SEC | 0x404811F8 | FULL | PTP Peer Event Frame Received Seconds Register (31 to 0 bits) |
| ETH0_TSU_PEER_RX_NSEC | 0x404811FC | FULL | PTP Peer Event Frame Received Nanoseconds Register |
| ETH0_PCS_CONTROL | 0x40481200 | FULL | Not presents. Access to the register returns AHB error. |
| ETH0_PCS_STATUS | 0x40481204 | FULL | Not presents. Access to the register returns AHB error. |
| ETH0_PCS_AN_ADV | 0x40481210 | FULL | Not presents. Access to the register returns AHB error. |
| ETH0_PCS_AN_LP_BASE | 0x40481214 | FULL | Not presents. Access to the register returns AHB error. |
| ETH0_PCS_AN_EXP | 0x40481218 | FULL | Not presents. Access to the register returns AHB error. |
| ETH0_PCS_AN_NP_TX | 0x4048121C | FULL | Not presents. Access to the register returns AHB error. |
| ETH0_PCS_AN_LP_NP | 0x40481220 | FULL | Not presents. Access to the register returns AHB error. |
| ETH0_PCS_AN_EXT_STATUS | 0x4048123C | FULL | Not presents. Access to the register returns AHB error. |
| ETH0_TX_PAUSE_QUANTUM1 | 0x40481260 | FULL | Transmit Pause Quantum Register 1 |
| ETH0_TX_PAUSE_QUANTUM2 | 0x40481264 | FULL | Transmit Pause Quantum Register 2 |
| ETH0_TX_PAUSE_QUANTUM3 | 0x40481268 | FULL | Transmit Pause Quantum Register 3 |
| ETH0_RX_LPI | 0x40481270 | FULL | Received LPI transitions |
| ETH0_RX_LPI_TIME | 0x40481274 | FULL | Received LPI time |
| ETH0_TX_LPI | 0x40481278 | FULL | Transmit LPI transitions |
| ETH0_TX_LPI_TIME | 0x4048127C | FULL | Transmit LPI time |
| ETH0_DESIGNCFG_DEBUG1 | 0x40481280 | FULL | The GEM_GXL(3PIP) has many parameterisation options to configure the IP during compilation stage. This is achieved using Verilog define compiler directives in an include file called mxeth_defs.v. |
| ETH0_DESIGNCFG_DEBUG2 | 0x40481284 | FULL | Design Configuration Register 2 |
| ETH0_DESIGNCFG_DEBUG3 | 0x40481288 | FULL | Design Configuration Register 3 |
| ETH0_DESIGNCFG_DEBUG4 | 0x4048128C | FULL | Design Configuration Register 4 |
| ETH0_DESIGNCFG_DEBUG5 | 0x40481290 | FULL | Design Configuration Register 5 |
| ETH0_DESIGNCFG_DEBUG6 | 0x40481294 | FULL | Design Configuration Register 6 |
| ETH0_DESIGNCFG_DEBUG7 | 0x40481298 | FULL | Design Configuration Register 7 |
| ETH0_DESIGNCFG_DEBUG8 | 0x4048129C | FULL | Design Configuration Register 8 |
| ETH0_DESIGNCFG_DEBUG9 | 0x404812A0 | FULL | Design Configuration Register 9 |
| ETH0_DESIGNCFG_DEBUG10 | 0x404812A4 | FULL | Design Configuration Register 10 |
| ETH0_SPEC_ADD5_BOTTOM | 0x40481300 | FULL | Specific address registers 5 ~ 36 doesn't present. Access to the register returns AHB error. |
| ETH0_SPEC_ADD5_TOP | 0x40481304 | FULL | Specific address registers 5 ~ 36 doesn't present. Access to the register returns AHB error. |
| ETH0_SPEC_ADD36_BOTTOM | 0x404813F8 | FULL | Not presents. |
| ETH0_SPEC_ADD36_TOP | 0x404813FC | FULL | Not presents. |
| ETH0_INT_Q1_STATUS | 0x40481400 | FULL | Priority queue Interrupt Status Register |
| ETH0_INT_Q2_STATUS | 0x40481404 | FULL | Priority queue Interrupt Status Register |
| ETH0_INT_Q3_STATUS | 0x40481408 | FULL | int_q3_status to int_q15_status doesn't present. Access to the register returns AHB error. |
| ETH0_INT_Q15_STATUS | 0x40481438 | FULL | Not presents. |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| ETH0_TRANSMIT_Q1_PTR | 0x40481440 | FULL | This register holds the start address of the transmit buffer queue (transmit buffers descriptor list). The transmit buffer queue base address register must be initialized before transmit is started through bit 9 of the network control register. Once transmission has started, any write to the transmit buffer queue base address register is illegal and therefore ignored. Note that due to clock boundary synchronization, it takes a maximum of four pclk cycles from the writing of the transmit start bit before the transmitter is active. Writing to the transmit buffer queue base address register during this time may produce unpredictable results. Reading this register returns the location of the descriptor currently being accessed. Because the DMA can store data for multiple frames at once, this may not necessarily be pointing to the current frame being transmitted. In terms of AMBA AXI operation, the transmit descriptors are written to memory using a single 32bit AHB access. When the datapath is configured as 64bit , the transmit descriptors should be aligned at 64-bit boundaries and each pair of 32-bit descriptors is read from memory using a single AXI access. |
| ETH0_TRANSMIT_Q2_PTR | 0x40481444 | FULL | This register holds the start address of the transmit buffer queue (transmit buffers descriptor list). The transmit buffer queue base address register must be initialized before transmit is started through bit 9 of the network control register. Once transmission has started, any write to the transmit buffer queue base address register is illegal and therefore ignored. Note that due to clock boundary synchronization, it takes a maximum of four pclk cycles from the writing of the transmit start bit before the transmitter is active. Writing to the transmit buffer queue base address register during this time may produce unpredictable results. Reading this register returns the location of the descriptor currently being accessed. Because the DMA can store data for multiple frames at once, this may not necessarily be pointing to the current frame being transmitted. In terms of AMBA AXI operation, the transmit descriptors are written to memory using a single 32bit AHB access. When the datapath is configured as 64bit , the transmit descriptors should be aligned at 64-bit boundaries and each pair of 32-bit descriptors is read from memory using a single AXI access. |
| ETH0_TRANSMIT_Q3_PTR | 0x40481448 | FULL | transmit_q3_ptr to transmit_q15_ptr doesn't present. Access to the register returns AHB error. |
| ETH0_TRANSMIT_Q15_PTR | 0x40481478 | FULL | Not presents. |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| ETH0_RECEIVE_Q1_PTR | 0x40481480 | FULL | This register holds the start address of the transmit buffer queue (transmit buffers descriptor list). The transmit buffer queue base address register must be initialized before transmit is started through bit 9 of the network control register. Once transmission has started, any write to the transmit buffer queue base address register is illegal and therefore ignored. Note that due to clock boundary synchronization, it takes a maximum of four pclk cycles from the writing of the transmit start bit before the transmitter is active. Writing to the transmit buffer queue base address register during this time may produce unpredictable results. Reading this register returns the location of the descriptor currently being accessed. Because the DMA can store data for multiple frames at once, this may not necessarily be pointing to the current frame being transmitted. In terms of AMBA AXI operation, the transmit descriptors are written to memory using a single 32bit AHB access. When the datapath is configured as 64bit , the transmit descriptors should be aligned at 64-bit boundaries and each pair of 32-bit descriptors is read from memory using a single AXI access. |
| ETH0_RECEIVE_Q2_PTR | 0x40481484 | FULL | This register holds the start address of the transmit buffer queue (transmit buffers descriptor list). The transmit buffer queue base address register must be initialized before transmit is started through bit 9 of the network control register. Once transmission has started, any write to the transmit buffer queue base address register is illegal and therefore ignored. Note that due to clock boundary synchronization, it takes a maximum of four pclk cycles from the writing of the transmit start bit before the transmitter is active. Writing to the transmit buffer queue base address register during this time may produce unpredictable results. Reading this register returns the location of the descriptor currently being accessed. Because the DMA can store data for multiple frames at once, this may not necessarily be pointing to the current frame being transmitted. In terms of AMBA AXI operation, the transmit descriptors are written to memory using a single 32bit AHB access. When the datapath is configured as 64bit , the transmit descriptors should be aligned at 64-bit boundaries and each pair of 32-bit descriptors is read from memory using a single AXI access. |
| ETH0_RECEIVE_Q3_PTR | 0x40481488 | FULL | Not presents. Start address register doesn't present for queue3 ~ queue7. |
| ETH0_RECEIVE_Q7_PTR | 0x40481498 | FULL | Not presents. |
| ETH0_DMA_RXBUF_SIZE_Q1 | 0x404814A0 | FULL | Receive Buffer queue 1 Size |
| ETH0_DMA_RXBUF_SIZE_Q2 | 0x404814A4 | FULL | Receive Buffer queue 2 Size |
| ETH0_DMA_RXBUF_SIZE_Q3 | 0x404814A8 | FULL | dma_rxbuf_size_q3 to dma_rxbuf_size_q7 doesn't present. |
| ETH0_DMA_RXBUF_SIZE_Q7 | 0x404814B8 | FULL | Not presents. |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| ETH0_CBS_CONTROL | 0x404814BC | FULL | The IdleSlope value is defined as the rate of change of credit when a packet is waiting to be sent. This must not exceed the portTransmitRate which is dependent on the speed of operation, eg, portTranmsitRate. 1Gb/s = 32'h07735940 (125 Mbytes/s), 100Mb/sec = 32'h017D7840 (25 Mnibbles/s), 10Mb/sec = 32'h002625A0 (2.5 Mnibbles/s). If 50 percent of bandwidth was to be allocated to a particular queue in 1Gb/sec mode then the IdleSlope value for that queue would be calculated as 32'h07735940/2. Note that Credit-Based Shaping should be disabled prior to updating the IdleSlope values. As another example, for a 1722 audio packet with a payload of 6 samples per channel, the packet size would be 7 (preamble) + 1 (SFD) + 50 (packet header) + 6x4x2(payload) + 4 (CRC) = 110 bytes. For a rate of 8000 packets per second, the desired rate would 110 x 8000 bytes per second, so the programmed idleSlope value would be 880000 for a 1Gb/s connection, or 1760000 for a 100Mb/s or 10Mbs connection. See Figure 6.3 in the IEEE 1722 standard. In practice, the actual transmission rate will be vary slightly from that calculated. In this case, the idleSlope value should be recalibrated based on the variance between the measured and expected rate, and in this case very accurate transmission rates can be achieved. |
| ETH0_CBS_IDLESLOPE_Q_A | 0x404814C0 | FULL | queue A is the highest priority queue. This would be queue 8 in an 8 queue configuration. |
| ETH0_CBS_IDLESLOPE_Q_B | 0x404814C4 | FULL | queue B is the 2nd highest priority queue. This would be queue 7 in an 8 queue configuration. |
| ETH0_UPPER_TX_Q_BASE_ADDR | 0x404814C8 | FULL | Upper 32 bits of transmit buffer descriptor queue base address. |
| ETH0_TX_BD_CONTROL | 0x404814CC | FULL | TX BD control register |
| ETH0_RX_BD_CONTROL | 0x404814D0 | FULL | RX BD control register |
| ETH0_UPPER_RX_Q_BASE_ADDR | 0x404814D4 | FULL | Upper 32 bits of receive buffer descriptor queue base address. |
| ETH0_HIDDEN_REG0 | 0x404814E0 | FULL | Hidden registers defined in edma_defs.v \`define gem_cbs_port_tx_rate_10m 12'h4e0 // 10M Port TX Rate *** HIDDEN Register ***'. Default value of cbs related hidden registers (0x14E0~0x14E8) are depicted in cbs_control register. |
| ETH0_HIDDEN_REG1 | 0x404814E4 | FULL | Hidden registers defined in edma_defs.v \`define gem_cbs_port_tx_rate_100m 12'h4e4 // 100M Port TX Rate *** HIDDEN Register ***' |
| ETH0_HIDDEN_REG2 | 0x404814E8 | FULL | Hidden registers defined in edma_defs.v \`define gem_cbs_port_tx_rate_1g 12'h4e8 // 1G Port TX Rate *** HIDDEN Register ***' |
| ETH0_HIDDEN_REG3 | 0x404814EC | FULL | Hidden registers defined in edma_defs.v \`define gem_wd_counter 12'h4ec // *** HIDDEN Register ***'. |
| ETH0_HIDDEN_REG4 | 0x404814F8 | FULL | Hidden registers defined in edma_defs.v \`define gem_axi_tx_full_threshold0 12'h4f8 // AXI full threshold setting *** HIDDEN Register ***'. Note. When using AXI mode with a single port ram ( gem_spram == 1) mode and a 32b dma bus width ( gem_dma_bus_width == 32 or bits 22 to 21 of the network_config register are set to 0) the AXI hidden registers (0x14F8 and 0x14FC) need to be updated (these registers are used for fine tuning AXI dma bursts and normally should not be touched). |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| ETH0_HIDDEN_REG5 | 0x404814FC | FULL | Hidden registers defined in edma_defs.v `define gem_axi_tx_full_threshold1 12'h4fc // AXI full threshold setting *** HIDDEN Register ***'. |
| ETH0_SCREENING_TYPE_1_REGISTER_0 | 0x40481500 | FULL | Screening type 1 registers are used to allocate up to 16 priority queues to received frames based on certain IP or UDP fields of incoming frames. Firstly, when DS/TC match enable is set (bit 28), the DS (Differentiated Services) field of the received IPv4 header or TCfield (traffic class) of IPv6 headers are matched against bits 11 to 4. Secondly, when UDP port match enable is set (bit 29), the UDP Destination Port of the received UDP frame is matched against bits 27 to 12. Both UDP and DS/TC matching can be enabled simultaneously or individually. If a match is successful, then the queue value programmed in bits 2 to 0 is allocated to the frame. The required number of Type 1 screening registers is configured in the gem defines file. Up to 16 type 1 screening registers have been allocated APB address space between 0x500 and 0x53C. |
| ETH0_SCREENING_TYPE_1_REGISTER_1 | 0x40481504 | FULL | screening type 1 register 1, same as screening_type_1_register_0 |
| ETH0_SCREENING_TYPE_1_REGISTER_2 | 0x40481508 | FULL | screening type 1 register 2, same as screening_type_1_register_0 |
| ETH0_SCREENING_TYPE_1_REGISTER_3 | 0x4048150C | FULL | screening type 1 register 3, same as screening_type_1_register_0 |
| ETH0_SCREENING_TYPE_1_REGISTER_4 | 0x40481510 | FULL | screening type 1 register 4, same as screening_type_1_register_0 |
| ETH0_SCREENING_TYPE_1_REGISTER_5 | 0x40481514 | FULL | screening type 1 register 5, same as screening_type_1_register_0 |
| ETH0_SCREENING_TYPE_1_REGISTER_6 | 0x40481518 | FULL | screening type 1 register 6, same as screening_type_1_register_0 |
| ETH0_SCREENING_TYPE_1_REGISTER_7 | 0x4048151C | FULL | screening type 1 register 7, same as screening_type_1_register_0 |
| ETH0_SCREENING_TYPE_1_REGISTER_8 | 0x40481520 | FULL | screening type 1 register 8, same as screening_type_1_register_0 |
| ETH0_SCREENING_TYPE_1_REGISTER_9 | 0x40481524 | FULL | screening type 1 register 9, same as screening_type_1_register_0 |
| ETH0_SCREENING_TYPE_1_REGISTER_10 | 0x40481528 | FULL | screening type 1 register 10, same as screening_type_1_register_0 |
| ETH0_SCREENING_TYPE_1_REGISTER_11 | 0x4048152C | FULL | screening type 1 register 11, same as screening_type_1_register_0 |
| ETH0_SCREENING_TYPE_1_REGISTER_12 | 0x40481530 | FULL | screening type 1 register 12, same as screening_type_1_register_0 |
| ETH0_SCREENING_TYPE_1_REGISTER_13 | 0x40481534 | FULL | screening type 1 register 13, same as screening_type_1_register_0 |
| ETH0_SCREENING_TYPE_1_REGISTER_14 | 0x40481538 | FULL | screening type 1 register 14, same as screening_type_1_register_0 |
| ETH0_SCREENING_TYPE_1_REGISTER_15 | 0x4048153C | FULL | screening type 1 register 15, same as screening_type_1_register_0 |
| ETH0_SCREENING_TYPE_2_REGISTER_0 | 0x40481540 | FULL | Screener Type 2 match registers operate independently of screener type 1 registers and offer additional match capabilities, extending the capabilities into vendor specific protocols. |
| ETH0_SCREENING_TYPE_2_REGISTER_1 | 0x40481544 | FULL | screening type 2 register 1, same as screening_type_2_register_0 |
| ETH0_SCREENING_TYPE_2_REGISTER_2 | 0x40481548 | FULL | screening type 2 register 2, same as screening_type_2_register_0 |
| ETH0_SCREENING_TYPE_2_REGISTER_3 | 0x4048154C | FULL | screening type 2 register 3, same as screening_type_2_register_0 |
| ETH0_SCREENING_TYPE_2_REGISTER_4 | 0x40481550 | FULL | screening type 2 register 4, same as screening_type_2_register_0 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| ETH0_SCREENING_TYPE_2_REGISTER_5 | 0x40481554 | FULL | screening type 2 register 5, same as screening_type_2_register_0 |
| ETH0_SCREENING_TYPE_2_REGISTER_6 | 0x40481558 | FULL | screening type 2 register 6, same as screening_type_2_register_0 |
| ETH0_SCREENING_TYPE_2_REGISTER_7 | 0x4048155C | FULL | screening type 2 register 7, same as screening_type_2_register_0 |
| ETH0_SCREENING_TYPE_2_REGISTER_8 | 0x40481560 | FULL | screening type 2 register 8, same as screening_type_2_register_0 |
| ETH0_SCREENING_TYPE_2_REGISTER_9 | 0x40481564 | FULL | screening type 2 register 9, same as screening_type_2_register_0 |
| ETH0_SCREENING_TYPE_2_REGISTER_10 | 0x40481568 | FULL | screening type 2 register 10, same as screening_type_2_register_0 |
| ETH0_SCREENING_TYPE_2_REGISTER_11 | 0x4048156C | FULL | screening type 2 register 11, same as screening_type_2_register_0 |
| ETH0_SCREENING_TYPE_2_REGISTER_12 | 0x40481570 | FULL | screening type 2 register 12, same as screening_type_2_register_0 |
| ETH0_SCREENING_TYPE_2_REGISTER_13 | 0x40481574 | FULL | screening type 2 register 13, same as screening_type_2_register_0 |
| ETH0_SCREENING_TYPE_2_REGISTER_14 | 0x40481578 | FULL | screening type 2 register 14, same as screening_type_2_register_0 |
| ETH0_SCREENING_TYPE_2_REGISTER_15 | 0x4048157C | FULL | screening type 2 register 15, same as screening_type_2_register_0 |
| ETH0_TX_SCHED_CTRL | 0x40481580 | FULL | This register controls the transmit scheduling algorithm the user can select for each active transmit queue. By default all queues are initialized to fixed priority, with the top indexed queue having overall priority |
| ETH0_BW_RATE_LIMIT_Q0TO3 | 0x40481590 | FULL | This register holds the DWRR weighting value or the ETS bandwidth percentage value used by the transmit scheduler for queues 0 to 3. |
| ETH0_BW_RATE_LIMIT_Q4TO7 | 0x40481594 | FULL | Not presents. MXETH has only 3 queues. Access to the register returns AHB error. |
| ETH0_BW_RATE_LIMIT_Q8TO11 | 0x40481598 | FULL | Not presents. MXETH has only 3 queues. Access to the register returns AHB error. |
| ETH0_BW_RATE_LIMIT_Q12TO15 | 0x4048159C | FULL | Not presents. MXETH has only 3 queues. Access to the register returns AHB error. |
| ETH0_TX_Q_SEG_ALLOC_Q0TO7 | 0x404815A0 | FULL | This register allows the user to distribute the Transmit SRAM used by the DMA across the priority queues, for queues 0 to 7. The SRAM itself is split into a number of evenly sized segments (this is defined in the verilog configuration defs file - for the configuration used to generate this register description, the total number of segments was set to '16'). Those segments can then be freely distributed across the active queues, in powers of 2. I.e. a value of 0 would mean 1 segment has been allocated to the queue. A value of 1 would mean 2 segments, a value of 2 means 4 segments and so on. The reset values of these registers are defined in the configuration defs file. |
| ETH0_TX_Q_SEG_ALLOC_Q8TO15 | 0x404815A4 | FULL | Not presents. Access to the register returns AHB error. |
| ETH0_RECEIVE_Q8_PTR | 0x404815C0 | FULL | receive_q8_ptr to receive_q15_ptr doesn't present. Access to the register returns AHB error. |
| ETH0_RECEIVE_Q15_PTR | 0x404815DC | FULL | Not presents. |
| ETH0_DMA_RXBUF_SIZE_Q8 | 0x404815E0 | FULL | dma_rxbuf_size_q8 to dma_rxbuf_size_q15 doesn't present. Access to the register returns AHB error. |
| ETH0_DMA_RXBUF_SIZE_Q15 | 0x404815FC | FULL | Not presents. |
| ETH0_INT_Q1_ENABLE | 0x40481600 | FULL | At reset all interrupts are disabled. Writing a one to the relevant bit location enables the required interrupt. This register is write only and when read will return zero. |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| ETH0_INT_Q2_ENABLE | 0x40481604 | FULL | At reset all interrupts are disabled. Writing a one to the relevant bit location enables the required interrupt. This register is write only and when read will return zero. |
| ETH0_INT_Q3_ENABLE | 0x40481608 | FULL | int_q3_enable to int_q7_enable doesn't present. Access to the register returns AHB error. |
| ETH0_INT_Q7_ENABLE | 0x40481618 | FULL | Not presents. |
| ETH0_INT_Q1_DISABLE | 0x40481620 | FULL | Writing a 1 to the relevant bit location disables that particular interrupt. This register is write only and when read will return zero. |
| ETH0_INT_Q2_DISABLE | 0x40481624 | FULL | Writing a 1 to the relevant bit location disables that particular interrupt. This register is write only and when read will return zero. |
| ETH0_INT_Q3_DISABLE | 0x40481628 | FULL | int_q3_disable to int_q7_disable doesn't present. Access to the register returns AHB error. |
| ETH0_INT_Q7_DISABLE | 0x40481638 | FULL | Not presents. |
| ETH0_INT_Q1_MASK | 0x40481640 | FULL | The interrupt mask register is a read only register indicating which interrupts are masked. All bits are set at reset and can be reset individually by writing to the interrupt enable register or set individually by writing to the interrupt disable register. Having separate address locations for enable and disable saves the need for performing a read modify write when updating the interrupt mask register. For test purposes there is a write-only function to this register that allows the bits in the interrupt status register to be set or cleared, regardless of the state of the mask register. |
| ETH0_INT_Q2_MASK | 0x40481644 | FULL | The interrupt mask register is a read only register indicating which interrupts are masked. All bits are set at reset and can be reset individually by writing to the interrupt enable register or set individually by writing to the interrupt disable register. Having separate address locations for enable and disable saves the need for performing a read modify write when updating the interrupt mask register. For test purposes there is a write-only function to this register that allows the bits in the interrupt status register to be set or cleared, regardless of the state of the mask register. |
| ETH0_INT_Q3_MASK | 0x40481648 | FULL | int_q3_mask to int_q7_mask doesn't present. Access to the register returns AHB error. |
| ETH0_INT_Q7_MASK | 0x40481658 | FULL | Not presents. |
| ETH0_INT_Q8_ENABLE | 0x40481660 | FULL | int_q8_enable to int_q15_enable doesn't present. Access to the register returns AHB error. |
| ETH0_INT_Q15_ENABLE | 0x4048167C | FULL | Not presents. |
| ETH0_INT_Q8_DISABLE | 0x40481680 | FULL | int_q8_disable to int_q15_disable doesn't present. Access to the register returns AHB error. |
| ETH0_INT_Q15_DISABLE | 0x4048169C | FULL | Not presents. |
| ETH0_INT_Q8_MASK | 0x404816A0 | FULL | int_q8_mask to int_q15_mask doesn't present. Access to the register returns AHB error. |
| ETH0_INT_Q15_MASK | 0x404816BC | FULL | Not presents. |
| ETH0_SCREENING_TYPE_2_ETHERTYPE_REG_0 | 0x404816E0 | FULL | Ethertype Register |
| ETH0_SCREENING_TYPE_2_ETHERTYPE_REG_1 | 0x404816E4 | FULL | Ethertype Register |
| ETH0_SCREENING_TYPE_2_ETHERTYPE_REG_2 | 0x404816E8 | FULL | Ethertype Register |
| ETH0_SCREENING_TYPE_2_ETHERTYPE_REG_3 | 0x404816EC | FULL | Ethertype Register |
| ETH0_SCREENING_TYPE_2_ETHERTYPE_REG_4 | 0x404816F0 | FULL | Ethertype Register |
| ETH0_SCREENING_TYPE_2_ETHERTYPE_REG_5 | 0x404816F4 | FULL | Ethertype Register |
| ETH0_SCREENING_TYPE_2_ETHERTYPE_REG_6 | 0x404816F8 | FULL | Ethertype Register |
| ETH0_SCREENING_TYPE_2_ETHERTYPE_REG_7 | 0x404816FC | FULL | Ethertype Register |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| ETH0_TYPE2_COMPARE_0_WORD_0 | 0x40481700 | FULL | 'Compare A, B and C fields of the screener type 2 match register are pointers to a pool of up to 32 compare registers. If enabled the compare is true if the data at the OFFSET into the frame, ANDed with the MASK Value if the mask is enabled, is equal to the COMPARE Value. Either a 16 bit comparison or a 32 bit comparison is done. This selection is made via the associated compare word1 register bit 9. If a 16 bit comparison is selected, then a 16 bit mask is also available to the user to select which bits should be compared. If the 32 bit compare option is selected, then no mask is available. The byte at the OFFSET number of bytes from the index start is compared thru bits 7 to 0 of the configured VALUE. The byte at the OFFSET number of bytes + 1 from the index start is compared thru bits 15 to 8 of the configured VALUE and so on. The OFFSET can be configured to be from 0 to 127 bytes from either the start of the frame, the byte following the therType field (last EtherType in the header if the frame is VLAN tagged), the byte following the IP header (IPv4 or IPv6) or from the byte following the start of the TCP/UDP header. The required number of Type 2 screening registers up to a maximum of 32 is configurable in the gem defines file and have been allocated APB address space between 0x700 and 0x7fc. Note. when using RX Partial Store and Forward mode and priority queues, the frame offset must be less than the Partial Store and Forward watermark. If the offset is higher than the watermark value it's not possible to identify the priority queue before the frame is sent to the AMBA interface, and an incorrect priority queue may be used. ' |
| ETH0_TYPE2_COMPARE_0_WORD_1 | 0x40481704 | FULL | 'Type2 Compare Word 1' |
| ETH0_TYPE2_COMPARE_1_WORD_0 | 0x40481708 | FULL | same as type2_compare_0_word_0 |
| ETH0_TYPE2_COMPARE_1_WORD_1 | 0x4048170C | FULL | same as type2_compare_0_word_1 |
| ETH0_TYPE2_COMPARE_2_WORD_0 | 0x40481710 | FULL | same as type2_compare_0_word_0 |
| ETH0_TYPE2_COMPARE_2_WORD_1 | 0x40481714 | FULL | same as type2_compare_0_word_1 |
| ETH0_TYPE2_COMPARE_3_WORD_0 | 0x40481718 | FULL | same as type2_compare_0_word_0 |
| ETH0_TYPE2_COMPARE_3_WORD_1 | 0x4048171C | FULL | same as type2_compare_0_word_1 |
| ETH0_TYPE2_COMPARE_4_WORD_0 | 0x40481720 | FULL | same as type2_compare_0_word_0 |
| ETH0_TYPE2_COMPARE_4_WORD_1 | 0x40481724 | FULL | same as type2_compare_0_word_1 |
| ETH0_TYPE2_COMPARE_5_WORD_0 | 0x40481728 | FULL | same as type2_compare_0_word_0 |
| ETH0_TYPE2_COMPARE_5_WORD_1 | 0x4048172C | FULL | same as type2_compare_0_word_1 |
| ETH0_TYPE2_COMPARE_6_WORD_0 | 0x40481730 | FULL | same as type2_compare_0_word_0 |
| ETH0_TYPE2_COMPARE_6_WORD_1 | 0x40481734 | FULL | same as type2_compare_0_word_1 |
| ETH0_TYPE2_COMPARE_7_WORD_0 | 0x40481738 | FULL | same as type2_compare_0_word_0 |
| ETH0_TYPE2_COMPARE_7_WORD_1 | 0x4048173C | FULL | same as type2_compare_0_word_1 |
| ETH0_TYPE2_COMPARE_8_WORD_0 | 0x40481740 | FULL | same as type2_compare_0_word_0 |
| ETH0_TYPE2_COMPARE_8_WORD_1 | 0x40481744 | FULL | same as type2_compare_0_word_1 |
| ETH0_TYPE2_COMPARE_9_WORD_0 | 0x40481748 | FULL | same as type2_compare_0_word_0 |
| ETH0_TYPE2_COMPARE_9_WORD_1 | 0x4048174C | FULL | same as type2_compare_0_word_1 |
| ETH0_TYPE2_COMPARE_10_WORD_0 | 0x40481750 | FULL | same as type2_compare_0_word_0 |
| ETH0_TYPE2_COMPARE_10_WORD_1 | 0x40481754 | FULL | same as type2_compare_0_word_1 |
| ETH0_TYPE2_COMPARE_11_WORD_0 | 0x40481758 | FULL | same as type2_compare_0_word_0 |
| ETH0_TYPE2_COMPARE_11_WORD_1 | 0x4048175C | FULL | same as type2_compare_0_word_1 |
| ETH0_TYPE2_COMPARE_12_WORD_0 | 0x40481760 | FULL | same as type2_compare_0_word_0 |
| ETH0_TYPE2_COMPARE_12_WORD_1 | 0x40481764 | FULL | same as type2_compare_0_word_1 |
| ETH0_TYPE2_COMPARE_13_WORD_0 | 0x40481768 | FULL | same as type2_compare_0_word_0 |
| ETH0_TYPE2_COMPARE_13_WORD_1 | 0x4048176C | FULL | same as type2_compare_0_word_1 |
| ETH0_TYPE2_COMPARE_14_WORD_0 | 0x40481770 | FULL | same as type2_compare_0_word_0 |
| ETH0_TYPE2_COMPARE_14_WORD_1 | 0x40481774 | FULL | same as type2_compare_0_word_1 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| ETH0_TYPE2_COMPARE_15_WORD_0 | 0x40481778 | FULL | same as type2_compare_0_word_0 |
| ETH0_TYPE2_COMPARE_15_WORD_1 | 0x4048177C | FULL | same as type2_compare_0_word_1 |
| ETH0_TYPE2_COMPARE_16_WORD_0 | 0x40481780 | FULL | same as type2_compare_0_word_0 |
| ETH0_TYPE2_COMPARE_16_WORD_1 | 0x40481784 | FULL | same as type2_compare_0_word_1 |
| ETH0_TYPE2_COMPARE_17_WORD_0 | 0x40481788 | FULL | same as type2_compare_0_word_0 |
| ETH0_TYPE2_COMPARE_17_WORD_1 | 0x4048178C | FULL | same as type2_compare_0_word_1 |
| ETH0_TYPE2_COMPARE_18_WORD_0 | 0x40481790 | FULL | same as type2_compare_0_word_0 |
| ETH0_TYPE2_COMPARE_18_WORD_1 | 0x40481794 | FULL | same as type2_compare_0_word_1 |
| ETH0_TYPE2_COMPARE_19_WORD_0 | 0x40481798 | FULL | same as type2_compare_0_word_0 |
| ETH0_TYPE2_COMPARE_19_WORD_1 | 0x4048179C | FULL | same as type2_compare_0_word_1 |
| ETH0_TYPE2_COMPARE_20_WORD_0 | 0x404817A0 | FULL | same as type2_compare_0_word_0 |
| ETH0_TYPE2_COMPARE_20_WORD_1 | 0x404817A4 | FULL | same as type2_compare_0_word_1 |
| ETH0_TYPE2_COMPARE_21_WORD_0 | 0x404817A8 | FULL | same as type2_compare_0_word_0 |
| ETH0_TYPE2_COMPARE_21_WORD_1 | 0x404817AC | FULL | same as type2_compare_0_word_1 |
| ETH0_TYPE2_COMPARE_22_WORD_0 | 0x404817B0 | FULL | same as type2_compare_0_word_0 |
| ETH0_TYPE2_COMPARE_22_WORD_1 | 0x404817B4 | FULL | same as type2_compare_0_word_1 |
| ETH0_TYPE2_COMPARE_23_WORD_0 | 0x404817B8 | FULL | same as type2_compare_0_word_0 |
| ETH0_TYPE2_COMPARE_23_WORD_1 | 0x404817BC | FULL | same as type2_compare_0_word_1 |
| ETH0_TYPE2_COMPARE_24_WORD_0 | 0x404817C0 | FULL | same as type2_compare_0_word_0 |
| ETH0_TYPE2_COMPARE_24_WORD_1 | 0x404817C4 | FULL | same as type2_compare_0_word_1 |
| ETH0_TYPE2_COMPARE_25_WORD_0 | 0x404817C8 | FULL | same as type2_compare_0_word_0 |
| ETH0_TYPE2_COMPARE_25_WORD_1 | 0x404817CC | FULL | same as type2_compare_0_word_1 |
| ETH0_TYPE2_COMPARE_26_WORD_0 | 0x404817D0 | FULL | same as type2_compare_0_word_0 |
| ETH0_TYPE2_COMPARE_26_WORD_1 | 0x404817D4 | FULL | same as type2_compare_0_word_1 |
| ETH0_TYPE2_COMPARE_27_WORD_0 | 0x404817D8 | FULL | same as type2_compare_0_word_0 |
| ETH0_TYPE2_COMPARE_27_WORD_1 | 0x404817DC | FULL | same as type2_compare_0_word_1 |
| ETH0_TYPE2_COMPARE_28_WORD_0 | 0x404817E0 | FULL | same as type2_compare_0_word_0 |
| ETH0_TYPE2_COMPARE_28_WORD_1 | 0x404817E4 | FULL | same as type2_compare_0_word_1 |
| ETH0_TYPE2_COMPARE_29_WORD_0 | 0x404817E8 | FULL | same as type2_compare_0_word_0 |
| ETH0_TYPE2_COMPARE_29_WORD_1 | 0x404817EC | FULL | same as type2_compare_0_word_1 |
| ETH0_TYPE2_COMPARE_30_WORD_0 | 0x404817F0 | FULL | same as type2_compare_0_word_0 |
| ETH0_TYPE2_COMPARE_30_WORD_1 | 0x404817F4 | FULL | same as type2_compare_0_word_1 |
| ETH0_TYPE2_COMPARE_31_WORD_0 | 0x404817F8 | FULL | same as type2_compare_0_word_0 |
| ETH0_TYPE2_COMPARE_31_WORD_1 | 0x404817FC | FULL | same as type2_compare_0_word_1 |

## 11.2 ETH 1

**Description** Ethernet Interface
**Base Address** 0x40490000
**Size** 0x10000
**Slave Num** MMIO4 - 3

| Register Name | Address | Permission | Description |
|---|---|---|---|
| ETH1_CTL | 0x40490000 | FULL | MXETH Control Register |
| ETH1_STATUS | 0x40490004 | FULL | MXETH Status Register |
| ETH1_NETWORK_CONTROL | 0x40491000 | FULL | The network control register contains general MAC control functions for both receiver and transmitter. |
| ETH1_NETWORK_CONFIG | 0x40491004 | FULL | The network configuration register contains functions for setting the mode of operation for the Gigabit Ethernet MAC. |
| ETH1_NETWORK_STATUS | 0x40491008 | FULL | The network status register returns status information with respect to the PHY management interface. |
| ETH1_USER_IO_REGISTER | 0x4049100C | FULL | Not presents. Access to the register will return AHB error. |
| ETH1_DMA_CONFIG | 0x40491010 | FULL | DMA Configuration Register |
| ETH1_TRANSMIT_STATUS | 0x40491014 | FULL | This register, when read, provides details of the status of a transmit. Once read, individual bits may be cleared by writing 1 to them. It is not possible to set a bit to 1 by writing to the register. |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| ETH1_RECEIVE_Q_PTR | 0x40491018 | FULL | This register holds the start address of the receive buffer queue (receive buffers descriptor list). The receive buffer queue base address must be initialized before receive is enabled through bit 2 of the network control register. Once reception is enabled, any write to the receive buffer queue base address register is ignored. Reading this register returns the location of the descriptor currently being accessed. This value increments as buffers are used. Software should not use this register for determining where to remove received frames from the queue as it constantly changes as new frames are received. Software should instead work its way through the buffer descriptor queue checking the used bits. In terms of AMBA (AXI) operation, the receive descriptors are read from memory using a single 32bit AXI access. When the datapath is configured at 64bit, the receive descriptors should be aligned at 64-bit boundaries and each pair of 32-bit descriptors is written to using a single 64bit AXI access. |
| ETH1_TRANSMIT_Q_PTR | 0x4049101C | FULL | This register holds the start address of the transmit buffer queue (transmit buffers descriptor list). The transmit buffer queue base address register must be initialized before transmit is started through bit 9 of the network control register. Once transmission has started, any write to the transmit buffer queue base address register is illegal and therefore ignored. Note that due to clock boundary synchronization, it takes a maximum of four pclk cycles from the writing of the transmit start bit before the transmitter is active. Writing to the transmit buffer queue base address register during this time may produce unpredictable results. Reading this register returns the location of the descriptor currently being accessed. Because the DMA can store data for multiple frames at once, this may not necessarily be pointing to the current frame being transmitted. In terms of AMBA AXI operation, the transmit descriptors are written to memory using a single 32bit AHB access. When the datapath is configured as 64bit, the transmit descriptors should be aligned at 64-bit boundaries and each pair of 32-bit descriptors is read from memory using a single AXI access. |
| ETH1_RECEIVE_STATUS | 0x40491020 | FULL | This register, when read provides details of the status of a receive. Once read, individual bits may be cleared by writing 1 to them. It is not possible to set a bit to 1 by writing to the register. |
| ETH1_INT_STATUS | 0x40491024 | FULL | If not configured for priority queueing, the GEM generates a single interrupt. This register indicates the source of this interrupt. The corresponding bit in the mask register must be clear for a bit to be set. If any bit is set in this register the ethernet_int signal will be asserted. For test purposes each bit can be set or reset by writing to the interrupt mask register. The default configuration is shown below whereby all bits are reset to zero on read. Changing the validity of the `gem_irq_read_clear define will instead require a one to be written to the appropriate bit in order to clear it. In this mode reading has no affect on the status of the bit. |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| ETH1_INT_ENABLE | 0x40491028 | FULL | At reset all interrupts are disabled. Writing a one to the relevant bit location enables the required interrupt. This register is write only and when read will return zero. |
| ETH1_INT_DISABLE | 0x4049102C | FULL | Writing a 1 to the relevant bit location disables that particular interrupt. This register is write only and when read will return zero. |
| ETH1_INT_MASK | 0x40491030 | FULL | The interrupt mask register is a read only register indicating which interrupts are masked. All bits are set at reset and can be reset individually by writing to the interrupt enable register or set individually by writing to the interrupt disable register. Having separate address locations for enable and disable saves the need for performing a read modify write when updating the interrupt mask register. For test purposes there is a write-only function to this register that allows the bits in the interrupt status register to be set or cleared, regardless of the state of the mask register. |
| ETH1_PHY_MANAGEMENT | 0x40491034 | FULL | The PHY maintenance register is implemented as a shift register. Writing to the register starts a shift operation which is signalled as complete when bit-2 is set in the network status register. It takes about 2000 pclk cycles to complete, when MDC is set for pclk divide by 32 in the network configuration register. An interrupt is generated upon completion. During this time, the MSB of the register is output on the MDIO pin and the LSB updated from the MDIO pin with each MDC cycle. This causes transmission of a PHY management frame on MDIO. See Section 22.2.4.5 of the IEEE 802.3 standard. Reading during the shift operation will return the current contents of the shift register. At the end of management operation, the bits will have shifted back to their original locations. For a read operation, the data bits will be updated with data read from the PHY. It is important to write the correct values to the register to ensure a valid PHY management frame is produced. The MDIO interface can read IEEE 802.3 clause 45 PHYs as well as clause 22 PHYs. To read clause 45 PHYs, bit 30 should be written with a 0 rather than a 1. For a description of MDC generation, see Network Configuration Register. |
| ETH1_PAUSE_TIME | 0x40491038 | FULL | Received Pause Quantum Register |
| ETH1_TX_PAUSE_QUANTUM | 0x4049103C | FULL | Transmit Pause Quantum Register |
| ETH1_PBUF_TXCUTTHRU | 0x40491040 | FULL | Partial store and forward is only applicable when using the DMA configured in SRAM based packet buffer mode. It is also not available when using multi buffer frames. TX Partial Store and Forward |
| ETH1_PBUF_RXCUTTHRU | 0x40491044 | FULL | RX Partial Store and Forward |
| ETH1_JUMBO_MAX_LENGTH | 0x40491048 | FULL | Maximum Jumbo Frame Size. |
| ETH1_EXTERNAL_FIFO_INTERFACE | 0x4049104C | FULL | Not presents. |
| ETH1_AXI_MAX_PIPELINE | 0x40491054 | FULL | Used to set the maximum amount of outstanding transactions on the AXI bus between AR / R channels and AW / W channels. Cannot be more than the depth of the configured AXI pipeline FIFO (defined in verilog defs.v) |
| ETH1_RSC_CONTROL | 0x40491058 | FULL | Not presents. Access to the register will return AHB error. |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| ETH1_INT_MODERATION | 0x4049105C | FULL | Used to moderate the number of transmit and receive complete interrupts issued. With interrupt moderation enabled receive and transmit interrupts are not generated immediately a frame is transmitted or received. Instead when a receive or transmit event occurs a timer is started and the interrupt is asserted after it times out. This limits the frequency with which the CPU receives interrupts. When interrupt moderation is enabled interrupt status bit one is always used for receive and bit 7 is always used for transmit even when priority queuing is enabled. With interrupt moderation 800ns periods are counted. GEM determines what constitutes an 800ns period by looking at the tbi (bit 11), gigabit bit (10) and speed (bit 0) bits in the network configuration register and counting tx_clk cycles. Bit 0 needs to be set to 1 for 100M operation. |
| ETH1_SYS_WAKE_TIME | 0x40491060 | FULL | Used to pause transmission after deassertion of tx_lpi_en. Each unit in this register corresponds to 64ns in gigabit mode, 320ns in 100M mode and 3200ns at 10M. After tx_lpi_en is deasserted transmission will pause for the set time. |
| ETH1_HASH_BOTTOM | 0x40491080 | FULL | The unicast hash enable and the multicast hash enable bits in the network configuration register enable the reception of hash matched frames. Hash Register Bottom (31 to 0 bits) |
| ETH1_HASH_TOP | 0x40491084 | FULL | Hash Register Top (63 to 32 bits) |
| ETH1_SPEC_ADD1_BOTTOM | 0x40491088 | FULL | The addresses stored in the specific address registers are deactivated at reset or when their corresponding specific address register bottom is written. They are activated when specific address register top is written. |
| ETH1_SPEC_ADD1_TOP | 0x4049108C | FULL | Specific Address Top |
| ETH1_SPEC_ADD2_BOTTOM | 0x40491090 | FULL | The addresses stored in the specific address registers are deactivated at reset or when their corresponding specific address register bottom is written. They are activated when specific address register top is written. |
| ETH1_SPEC_ADD2_TOP | 0x40491094 | FULL | Specific Address Top |
| ETH1_SPEC_ADD3_BOTTOM | 0x40491098 | FULL | The addresses stored in the specific address registers are deactivated at reset or when their corresponding specific address register bottom is written. They are activated when specific address register top is written. |
| ETH1_SPEC_ADD3_TOP | 0x4049109C | FULL | Specific Address Top |
| ETH1_SPEC_ADD4_BOTTOM | 0x404910A0 | FULL | The addresses stored in the specific address registers are deactivated at reset or when their corresponding specific address register bottom is written. They are activated when specific address register top is written. |
| ETH1_SPEC_ADD4_TOP | 0x404910A4 | FULL | Specific Address Top |
| ETH1_SPEC_TYPE1 | 0x404910A8 | FULL | Type ID Match 1 |
| ETH1_SPEC_TYPE2 | 0x404910AC | FULL | Type ID Match 2 |
| ETH1_SPEC_TYPE3 | 0x404910B0 | FULL | Type ID Match 3 |
| ETH1_SPEC_TYPE4 | 0x404910B4 | FULL | Type ID Match 4 |
| ETH1_WOL_REGISTER | 0x404910B8 | FULL | Wake on LAN Register. Presents in design, but feature is not supported. |
| ETH1_STRETCH_RATIO | 0x404910BC | FULL | IPG stretch register |
| ETH1_STACKED_VLAN | 0x404910C0 | FULL | Stacked VLAN Register |
| ETH1_TX_PFC_PAUSE | 0x404910C4 | FULL | Transmit PFC Pause Register |
| ETH1_MASK_ADD1_BOTTOM | 0x404910C8 | FULL | Specific Address Mask 1 Bottom (31 to 0 bits) |
| ETH1_MASK_ADD1_TOP | 0x404910CC | FULL | Specific Address Mask 1 Top (47 to 32 bits) |
| ETH1_DMA_ADDR_OR_MASK | 0x404910D0 | FULL | Receive DMA Data Buffer Address Mask |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| ETH1_RX_PTP_UNICAST | 0x404910D4 | FULL | PTP RX unicast IP destination address |
| ETH1_TX_PTP_UNICAST | 0x404910D8 | FULL | PTP TX unicast IP destination address |
| ETH1_TSU_NSEC_CMP | 0x404910DC | FULL | TSU timer comparison value nanoseconds |
| ETH1_TSU_SEC_CMP | 0x404910E0 | FULL | TSU timer comparison value seconds (31 to 0 bits) |
| ETH1_TSU_MSB_SEC_CMP | 0x404910E4 | FULL | TSU timer comparison value seconds (47 to 32 bits) |
| ETH1_TSU_PTP_TX_MSB_SEC | 0x404910E8 | FULL | PTP Event Frame Transmitted Seconds Register (47 to 32 bits) |
| ETH1_TSU_PTP_RX_MSB_SEC | 0x404910EC | FULL | PTP Event Frame Received Seconds Register (47 to 32 bits) |
| ETH1_TSU_PEER_TX_MSB_SEC | 0x404910F0 | FULL | PTP Peer Event Frame Transmitted Seconds Register (47 to 32 bits) |
| ETH1_TSU_PEER_RX_MSB_SEC | 0x404910F4 | FULL | PTP Peer Event Frame Received Seconds Register (47 to 32 bits) |
| ETH1_DPRAM_FILL_DBG | 0x404910F8 | FULL | The fill levels for the TX & RX packet buffers can be read using this register, including the fill level for each queue in the TX direction. |
| ETH1_REVISION_REG | 0x404910FC | FULL | This register indicates a Cadence module identification number and module revision. The value of this register is read only as defined by `gem_revision_reg_value |
| ETH1_OCTETS_TXED_BOTTOM | 0x40491100 | FULL | Octets Transmitted lower bits (31 to 0 bits) |
| ETH1_OCTETS_TXED_TOP | 0x40491104 | FULL | Octets Transmitted higher bits (47 to 32 bits) |
| ETH1_FRAMES_TXED_OK | 0x40491108 | FULL | Frames Transmitted |
| ETH1_BROADCAST_TXED | 0x4049110C | FULL | Broadcast Frames Transmitted |
| ETH1_MULTICAST_TXED | 0x40491110 | FULL | Multicast Frames Transmitted |
| ETH1_PAUSE_FRAMES_TXED | 0x40491114 | FULL | Pause Frames Transmitted |
| ETH1_FRAMES_TXED_64 | 0x40491118 | FULL | 64 Byte Frames Transmitted |
| ETH1_FRAMES_TXED_65 | 0x4049111C | FULL | 65 to 127 Byte Frames Transmitted |
| ETH1_FRAMES_TXED_128 | 0x40491120 | FULL | 128 to 255 Byte Frames Transmitted |
| ETH1_FRAMES_TXED_256 | 0x40491124 | FULL | 256 to 511 Byte Frames Transmitted |
| ETH1_FRAMES_TXED_512 | 0x40491128 | FULL | 512 to 1023 Byte Frames Transmitted |
| ETH1_FRAMES_TXED_1024 | 0x4049112C | FULL | 1024 to 1518 Byte Frames Transmitted |
| ETH1_FRAMES_TXED_1519 | 0x40491130 | FULL | Greater Than 1518 Byte Frames Transmitted |
| ETH1_TX_UNDERRUNS | 0x40491134 | FULL | Transmit Under Runs |
| ETH1_SINGLE_COLLISIONS | 0x40491138 | FULL | Single Collision Frames. Presents in design but not support. |
| ETH1_MULTIPLE_COLLISIONS | 0x4049113C | FULL | Multiple Collision Frames. Presents in design but not support. |
| ETH1_EXCESSIVE_COLLISIONS | 0x40491140 | FULL | Excessive Collisions. Presents in design but not support. |
| ETH1_LATE_COLLISIONS | 0x40491144 | FULL | Late Collisions. Presents in design but not support. |
| ETH1_DEFERRED_FRAMES | 0x40491148 | FULL | Deferred Transmission Frames. Presents in design but not support. |
| ETH1_CRS_ERRORS | 0x4049114C | FULL | Carrier Sense Errors. Presents in design but not support. |
| ETH1_OCTETS_RXED_BOTTOM | 0x40491150 | FULL | Octets Received (31 to 0 bits) |
| ETH1_OCTETS_RXED_TOP | 0x40491154 | FULL | Octets Received (47 to 32 bits) |
| ETH1_FRAMES_RXED_OK | 0x40491158 | FULL | Frames Received |
| ETH1_BROADCAST_RXED | 0x4049115C | FULL | Broadcast Frames Received |
| ETH1_MULTICAST_RXED | 0x40491160 | FULL | Multicast Frames Received |
| ETH1_PAUSE_FRAMES_RXED | 0x40491164 | FULL | Pause Frames Received |
| ETH1_FRAMES_RXED_64 | 0x40491168 | FULL | 64 Byte Frames Received |
| ETH1_FRAMES_RXED_65 | 0x4049116C | FULL | 65 to 127 Byte Frames Received |
| ETH1_FRAMES_RXED_128 | 0x40491170 | FULL | 128 to 255 Byte Frames Received |
| ETH1_FRAMES_RXED_256 | 0x40491174 | FULL | 256 to 511 Byte Frames Received |
| ETH1_FRAMES_RXED_512 | 0x40491178 | FULL | 512 to 1023 Byte Frames Received |
| ETH1_FRAMES_RXED_1024 | 0x4049117C | FULL | 1024 to 1518 Byte Frames Received |
| ETH1_FRAMES_RXED_1519 | 0x40491180 | FULL | 1519 to maximum Byte Frames Received |
| ETH1_UNDERSIZE_FRAMES | 0x40491184 | FULL | Undersized Frames Received |
| ETH1_EXCESSIVE_RX_LENGTH | 0x40491188 | FULL | Oversize Frames Received |
| ETH1_RX_JABBERS | 0x4049118C | FULL | Jabbers Received |
| ETH1_FCS_ERRORS | 0x40491190 | FULL | Frame Check Sequence Errors |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| ETH1_RX_LENGTH_ERRORS | 0x40491194 | FULL | Length Field Frame Errors |
| ETH1_RX_SYMBOL_ERRORS | 0x40491198 | FULL | Receive Symbol Errors |
| ETH1_ALIGNMENT_ERRORS | 0x4049119C | FULL | Alignment Errors |
| ETH1_RX_RESOURCE_ERRORS | 0x404911A0 | FULL | Receive Resource Errors |
| ETH1_RX_OVERRUNS | 0x404911A4 | FULL | Receive Overruns |
| ETH1_RX_IP_CK_ERRORS | 0x404911A8 | FULL | IP Header Checksum Errors |
| ETH1_RX_TCP_CK_ERRORS | 0x404911AC | FULL | TCP Checksum Errors |
| ETH1_RX_UDP_CK_ERRORS | 0x404911B0 | FULL | UDP Checksum Errors |
| ETH1_AUTO_FLUSHED_PKTS | 0x404911B4 | FULL | Receive DMA Flushed Packets |
| ETH1_TSU_TIMER_INCR_SUB_NSEC | 0x404911BC | FULL | 1588 Timer Increment Register sub nsec |
| ETH1_TSU_TIMER_MSB_SEC | 0x404911C0 | FULL | 1588 Timer Seconds Register (47 to 32 bits) |
| ETH1_TSU_STROBE_MSB_SEC | 0x404911C4 | FULL | 1588 Timer Sync Strobe Seconds Register (47 to 32 bits) |
| ETH1_TSU_STROBE_SEC | 0x404911C8 | FULL | 1588 Timer Sync Strobe Seconds Register (31 to 0 bits) |
| ETH1_TSU_STROBE_NSEC | 0x404911CC | FULL | 1588 Timer Sync Strobe Nanoseconds Register |
| ETH1_TSU_TIMER_SEC | 0x404911D0 | FULL | 1588 Timer Seconds Register (31 to 0 bits) |
| ETH1_TSU_TIMER_NSEC | 0x404911D4 | FULL | 1588 Timer Nanoseconds Register |
| ETH1_TSU_TIMER_ADJUST | 0x404911D8 | FULL | This register is used to adjust the value of the timer in the TSU. It allows an integral number of nanoseconds to be added or subtracted from the timer in a one-off operation. This register returns all zeroes when read. |
| ETH1_TSU_TIMER_INCR | 0x404911DC | FULL | 1588 Timer Increment Register |
| ETH1_TSU_PTP_TX_SEC | 0x404911E0 | FULL | PTP Event Frame Transmitted Seconds Register (31 to 0 bits) |
| ETH1_TSU_PTP_TX_NSEC | 0x404911E4 | FULL | PTP Event Frame Transmitted Nanoseconds Register |
| ETH1_TSU_PTP_RX_SEC | 0x404911E8 | FULL | PTP Event Frame Received Seconds Register (31 to 0 bits) |
| ETH1_TSU_PTP_RX_NSEC | 0x404911EC | FULL | PTP Event Frame Received Nanoseconds Register |
| ETH1_TSU_PEER_TX_SEC | 0x404911F0 | FULL | PTP Peer Event Frame Transmitted Seconds Register (31 to 0 bits) |
| ETH1_TSU_PEER_TX_NSEC | 0x404911F4 | FULL | PTP Peer Event Frame Transmitted Nanoseconds Register |
| ETH1_TSU_PEER_RX_SEC | 0x404911F8 | FULL | PTP Peer Event Frame Received Seconds Register (31 to 0 bits) |
| ETH1_TSU_PEER_RX_NSEC | 0x404911FC | FULL | PTP Peer Event Frame Received Nanoseconds Register |
| ETH1_PCS_CONTROL | 0x40491200 | FULL | Not presents. Access to the register returns AHB error. |
| ETH1_PCS_STATUS | 0x40491204 | FULL | Not presents. Access to the register returns AHB error. |
| ETH1_PCS_AN_ADV | 0x40491210 | FULL | Not presents. Access to the register returns AHB error. |
| ETH1_PCS_AN_LP_BASE | 0x40491214 | FULL | Not presents. Access to the register returns AHB error. |
| ETH1_PCS_AN_EXP | 0x40491218 | FULL | Not presents. Access to the register returns AHB error. |
| ETH1_PCS_AN_NP_TX | 0x4049121C | FULL | Not presents. Access to the register returns AHB error. |
| ETH1_PCS_AN_LP_NP | 0x40491220 | FULL | Not presents. Access to the register returns AHB error. |
| ETH1_PCS_AN_EXT_STATUS | 0x4049123C | FULL | Not presents. Access to the register returns AHB error. |
| ETH1_TX_PAUSE_QUANTUM1 | 0x40491260 | FULL | Transmit Pause Quantum Register 1 |
| ETH1_TX_PAUSE_QUANTUM2 | 0x40491264 | FULL | Transmit Pause Quantum Register 2 |
| ETH1_TX_PAUSE_QUANTUM3 | 0x40491268 | FULL | Transmit Pause Quantum Register 3 |
| ETH1_RX_LPI | 0x40491270 | FULL | Received LPI transitions |
| ETH1_RX_LPI_TIME | 0x40491274 | FULL | Received LPI time |
| ETH1_TX_LPI | 0x40491278 | FULL | Transmit LPI transitions |
| ETH1_TX_LPI_TIME | 0x4049127C | FULL | Transmit LPI time |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| ETH1_DESIGNCFG_DEBUG1 | 0x40491280 | FULL | The GEM_GXL(3PIP) has many parameterisation options to configure the IP during compilation stage. This is achieved using Verilog define compiler directives in an include file called mxeth_defs.v. |
| ETH1_DESIGNCFG_DEBUG2 | 0x40491284 | FULL | Design Configuration Register 2 |
| ETH1_DESIGNCFG_DEBUG3 | 0x40491288 | FULL | Design Configuration Register 3 |
| ETH1_DESIGNCFG_DEBUG4 | 0x4049128C | FULL | Design Configuration Register 4 |
| ETH1_DESIGNCFG_DEBUG5 | 0x40491290 | FULL | Design Configuration Register 5 |
| ETH1_DESIGNCFG_DEBUG6 | 0x40491294 | FULL | Design Configuration Register 6 |
| ETH1_DESIGNCFG_DEBUG7 | 0x40491298 | FULL | Design Configuration Register 7 |
| ETH1_DESIGNCFG_DEBUG8 | 0x4049129C | FULL | Design Configuration Register 8 |
| ETH1_DESIGNCFG_DEBUG9 | 0x404912A0 | FULL | Design Configuration Register 9 |
| ETH1_DESIGNCFG_DEBUG10 | 0x404912A4 | FULL | Design Configuration Register 10 |
| ETH1_SPEC_ADD5_BOTTOM | 0x40491300 | FULL | Specific address registers 5 ~ 36 doesn't present. Access to the register returns AHB error. |
| ETH1_SPEC_ADD5_TOP | 0x40491304 | FULL | Specific address registers 5 ~ 36 doesn't present. Access to the register returns AHB error. |
| ETH1_SPEC_ADD36_BOTTOM | 0x404913F8 | FULL | Not presents. |
| ETH1_SPEC_ADD36_TOP | 0x404913FC | FULL | Not presents. |
| ETH1_INT_Q1_STATUS | 0x40491400 | FULL | Priority queue Interrupt Status Register |
| ETH1_INT_Q2_STATUS | 0x40491404 | FULL | Priority queue Interrupt Status Register |
| ETH1_INT_Q3_STATUS | 0x40491408 | FULL | int_q3_status to int_q15_status doesn't present. Access to the register returns AHB error. |
| ETH1_INT_Q15_STATUS | 0x40491438 | FULL | Not presents. |
| ETH1_TRANSMIT_Q1_PTR | 0x40491440 | FULL | This register holds the start address of the transmit buffer queue (transmit buffers descriptor list). The transmit buffer queue base address register must be initialized before transmit is started through bit 9 of the network control register. Once transmission has started, any write to the transmit buffer queue base address register is illegal and therefore ignored. Note that due to clock boundary synchronization, it takes a maximum of four pclk cycles from the writing of the transmit start bit before the transmitter is active. Writing to the transmit buffer queue base address register during this time may produce unpredictable results. Reading this register returns the location of the descriptor currently being accessed. Because the DMA can store data for multiple frames at once, this may not necessarily be pointing to the current frame being transmitted. In terms of AMBA AXI operation, the transmit descriptors are written to memory using a single 32bit AHB access. When the datapath is configured as 64bit , the transmit descriptors should be aligned at 64-bit boundaries and each pair of 32-bit descriptors is read from memory using a single AXI access. |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| ETH1_TRANSMIT_Q2_PTR | 0x40491444 | FULL | This register holds the start address of the transmit buffer queue (transmit buffers descriptor list). The transmit buffer queue base address register must be initialized before transmit is started through bit 9 of the network control register. Once transmission has started, any write to the transmit buffer queue base address register is illegal and therefore ignored. Note that due to clock boundary synchronization, it takes a maximum of four pclk cycles from the writing of the transmit start bit before the transmitter is active. Writing to the transmit buffer queue base address register during this time may produce unpredictable results. Reading this register returns the location of the descriptor currently being accessed. Because the DMA can store data for multiple frames at once, this may not necessarily be pointing to the current frame being transmitted. In terms of AMBA AXI operation, the transmit descriptors are written to memory using a single 32bit AHB access. When the datapath is configured as 64bit , the transmit descriptors should be aligned at 64-bit boundaries and each pair of 32-bit descriptors is read from memory using a single AXI access. |
| ETH1_TRANSMIT_Q3_PTR | 0x40491448 | FULL | transmit_q3_ptr to transmit_q15_ptr doesn't present. Access to the register returns AHB error. |
| ETH1_TRANSMIT_Q15_PTR | 0x40491478 | FULL | Not presents. |
| ETH1_RECEIVE_Q1_PTR | 0x40491480 | FULL | This register holds the start address of the transmit buffer queue (transmit buffers descriptor list). The transmit buffer queue base address register must be initialized before transmit is started through bit 9 of the network control register. Once transmission has started, any write to the transmit buffer queue base address register is illegal and therefore ignored. Note that due to clock boundary synchronization, it takes a maximum of four pclk cycles from the writing of the transmit start bit before the transmitter is active. Writing to the transmit buffer queue base address register during this time may produce unpredictable results. Reading this register returns the location of the descriptor currently being accessed. Because the DMA can store data for multiple frames at once, this may not necessarily be pointing to the current frame being transmitted. In terms of AMBA AXI operation, the transmit descriptors are written to memory using a single 32bit AHB access. When the datapath is configured as 64bit , the transmit descriptors should be aligned at 64-bit boundaries and each pair of 32-bit descriptors is read from memory using a single AXI access. |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| ETH1_RECEIVE_Q2_PTR | 0x40491484 | FULL | This register holds the start address of the transmit buffer queue (transmit buffers descriptor list). The transmit buffer queue base address register must be initialized before transmit is started through bit 9 of the network control register. Once transmission has started, any write to the transmit buffer queue base address register is illegal and therefore ignored. Note that due to clock boundary synchronization, it takes a maximum of four pclk cycles from the writing of the transmit start bit before the transmitter is active. Writing to the transmit buffer queue base address register during this time may produce unpredictable results. Reading this register returns the location of the descriptor currently being accessed. Because the DMA can store data for multiple frames at once, this may not necessarily be pointing to the current frame being transmitted. In terms of AMBA AXI operation, the transmit descriptors are written to memory using a single 32bit AHB access. When the datapath is configured as 64bit , the transmit descriptors should be aligned at 64-bit boundaries and each pair of 32-bit descriptors is read from memory using a single AXI access. |
| ETH1_RECEIVE_Q3_PTR | 0x40491488 | FULL | Not presents. Start address register doesn't present for queue3 ~ queue7. |
| ETH1_RECEIVE_Q7_PTR | 0x40491498 | FULL | Not presents. |
| ETH1_DMA_RXBUF_SIZE_Q1 | 0x404914A0 | FULL | Receive Buffer queue 1 Size |
| ETH1_DMA_RXBUF_SIZE_Q2 | 0x404914A4 | FULL | Receive Buffer queue 2 Size |
| ETH1_DMA_RXBUF_SIZE_Q3 | 0x404914A8 | FULL | dma_rxbuf_size_q3 to dma_rxbuf_size_q7 doesn't present. |
| ETH1_DMA_RXBUF_SIZE_Q7 | 0x404914B8 | FULL | Not presents. |
| ETH1_CBS_CONTROL | 0x404914BC | FULL | The IdleSlope value is defined as the rate of change of credit when a packet is waiting to be sent. This must not exceed the portTransmitRate which is dependent on the speed of operation, eg, portTranmsitRate. 1Gb/s = 32'h07735940 (125 Mbytes/s), 100Mb/sec = 32'h017D7840 (25 Mnibbles/s), 10Mb/sec = 32'h002625A0 (2.5 Mnibbles/s). If 50 percent of bandwidth was to be allocated to a particular queue in 1Gb/sec mode then the IdleSlope value for that queue would be calculated as 32'h07735940/2. Note that Credit-Based Shaping should be disabled prior to updating the IdleSlope values. As another example, for a 1722 audio packet with a payload of 6 samples per channel, the packet size would be 7 (preamble) + 1 (SFD) + 50 (packet header) + 6x4x2(payload) + 4 (CRC) = 110 bytes. For a rate of 8000 packets per second, the desired rate would 110 x 8000 bytes per second, so the programmed idleSlope value would be 880000 for a 1Gb/s connection, or 1760000 for a 100Mb/s or 10Mbs connection. See Figure 6.3 in the IEEE 1722 standard. In practice, the actual transmission rate will be vary slightly from that calculated. In this case, the idleSlope value should be recalibrated based on the variance between the measured and expected rate, and in this case very accurate transmission rates can be achieved. |
| ETH1_CBS_IDLESLOPE_Q_A | 0x404914C0 | FULL | queue A is the highest priority queue. This would be queue 8 in an 8 queue configuration. |
| ETH1_CBS_IDLESLOPE_Q_B | 0x404914C4 | FULL | queue B is the 2nd highest priority queue. This would be queue 7 in an 8 queue configuration. |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| ETH1_UPPER_TX_Q_BASE_ADDR | 0x404914C8 | FULL | Upper 32 bits of transmit buffer descriptor queue base address. |
| ETH1_TX_BD_CONTROL | 0x404914CC | FULL | TX BD control register |
| ETH1_RX_BD_CONTROL | 0x404914D0 | FULL | RX BD control register |
| ETH1_UPPER_RX_Q_BASE_ADDR | 0x404914D4 | FULL | Upper 32 bits of receive buffer descriptor queue base address. |
| ETH1_HIDDEN_REG0 | 0x404914E0 | FULL | Hidden registers defined in edma_defs.v `define gem_cbs_port_tx_rate_10m 12'h4e0 // 10M Port TX Rate *** HIDDEN Register ***'. Default value of cbs related hidden registers (0x14E0~0x14E8) are depicted in cbs_control register. |
| ETH1_HIDDEN_REG1 | 0x404914E4 | FULL | Hidden registers defined in edma_defs.v `define gem_cbs_port_tx_rate_100m 12'h4e4 // 100M Port TX Rate *** HIDDEN Register ***' |
| ETH1_HIDDEN_REG2 | 0x404914E8 | FULL | Hidden registers defined in edma_defs.v `define gem_cbs_port_tx_rate_1g 12'h4e8 // 1G Port TX Rate *** HIDDEN Register ***' |
| ETH1_HIDDEN_REG3 | 0x404914EC | FULL | Hidden registers defined in edma_defs.v `define gem_wd_counter 12'h4ec // *** HIDDEN Register ***'. |
| ETH1_HIDDEN_REG4 | 0x404914F8 | FULL | Hidden registers defined in edma_defs.v `define gem_axi_tx_full_threshold0 12'h4f8 // AXI full threshold setting *** HIDDEN Register ***'. Note. When using AXI mode with a single port ram ( gem_spram == 1) mode and a 32b dma bus width ( gem_dma_bus_width == 32 or bits 22 to 21 of the network_config register are set to 0) the AXI hidden registers (0x14F8 and 0x14FC) need to be updated (these registers are used for fine tuning AXI dma bursts and normally should not be touched). |
| ETH1_HIDDEN_REG5 | 0x404914FC | FULL | Hidden registers defined in edma_defs.v `define gem_axi_tx_full_threshold1 12'h4fc // AXI full threshold setting *** HIDDEN Register ***'. |
| ETH1_SCREENING_TYPE_1_REGISTER_0 | 0x40491500 | FULL | Screening type 1 registers are used to allocate up to 16 priority queues to received frames based on certain IP or UDP fields of incoming frames. Firstly, when DS/TC match enable is set (bit 28), the DS (Differentiated Services) field of the received IPv4 header or TCfield (traffic class) of IPv6 headers are matched against bits 11 to 4. Secondly, when UDP port match enable is set (bit 29), the UDP Destination Port of the received UDP frame is matched against bits 27 to 12. Both UDP and DS/TC matching can be enabled simultaneously or individually. If a match is successful, then the queue value programmed in bits 2 to 0 is allocated to the frame. The required number of Type 1 screening registers is configured in the gem defines file. Up to 16 type 1 screening registers have been allocated APB address space between 0x500 and 0x53C. |
| ETH1_SCREENING_TYPE_1_REGISTER_1 | 0x40491504 | FULL | screening type 1 register 1, same as screening_type_1_register_0 |
| ETH1_SCREENING_TYPE_1_REGISTER_2 | 0x40491508 | FULL | screening type 1 register 2, same as screening_type_1_register_0 |
| ETH1_SCREENING_TYPE_1_REGISTER_3 | 0x4049150C | FULL | screening type 1 register 3, same as screening_type_1_register_0 |
| ETH1_SCREENING_TYPE_1_REGISTER_4 | 0x40491510 | FULL | screening type 1 register 4, same as screening_type_1_register_0 |
| ETH1_SCREENING_TYPE_1_REGISTER_5 | 0x40491514 | FULL | screening type 1 register 5, same as screening_type_1_register_0 |
| ETH1_SCREENING_TYPE_1_REGISTER_6 | 0x40491518 | FULL | screening type 1 register 6, same as screening_type_1_register_0 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| ETH1_SCREENING_TYPE_1_REGISTER_7 | 0x4049151C | FULL | screening type 1 register 7, same as screening_type_1_register_0 |
| ETH1_SCREENING_TYPE_1_REGISTER_8 | 0x40491520 | FULL | screening type 1 register 8, same as screening_type_1_register_0 |
| ETH1_SCREENING_TYPE_1_REGISTER_9 | 0x40491524 | FULL | screening type 1 register 9, same as screening_type_1_register_0 |
| ETH1_SCREENING_TYPE_1_REGISTER_10 | 0x40491528 | FULL | screening type 1 register 10, same as screening_type_1_register_0 |
| ETH1_SCREENING_TYPE_1_REGISTER_11 | 0x4049152C | FULL | screening type 1 register 11, same as screening_type_1_register_0 |
| ETH1_SCREENING_TYPE_1_REGISTER_12 | 0x40491530 | FULL | screening type 1 register 12, same as screening_type_1_register_0 |
| ETH1_SCREENING_TYPE_1_REGISTER_13 | 0x40491534 | FULL | screening type 1 register 13, same as screening_type_1_register_0 |
| ETH1_SCREENING_TYPE_1_REGISTER_14 | 0x40491538 | FULL | screening type 1 register 14, same as screening_type_1_register_0 |
| ETH1_SCREENING_TYPE_1_REGISTER_15 | 0x4049153C | FULL | screening type 1 register 15, same as screening_type_1_register_0 |
| ETH1_SCREENING_TYPE_2_REGISTER_0 | 0x40491540 | FULL | Screener Type 2 match registers operate independently of screener type 1 registers and offer additional match capabilities, extending the capabilities into vendor specific protocols. |
| ETH1_SCREENING_TYPE_2_REGISTER_1 | 0x40491544 | FULL | screening type 2 register 1, same as screening_type_2_register_0 |
| ETH1_SCREENING_TYPE_2_REGISTER_2 | 0x40491548 | FULL | screening type 2 register 2, same as screening_type_2_register_0 |
| ETH1_SCREENING_TYPE_2_REGISTER_3 | 0x4049154C | FULL | screening type 2 register 3, same as screening_type_2_register_0 |
| ETH1_SCREENING_TYPE_2_REGISTER_4 | 0x40491550 | FULL | screening type 2 register 4, same as screening_type_2_register_0 |
| ETH1_SCREENING_TYPE_2_REGISTER_5 | 0x40491554 | FULL | screening type 2 register 5, same as screening_type_2_register_0 |
| ETH1_SCREENING_TYPE_2_REGISTER_6 | 0x40491558 | FULL | screening type 2 register 6, same as screening_type_2_register_0 |
| ETH1_SCREENING_TYPE_2_REGISTER_7 | 0x4049155C | FULL | screening type 2 register 7, same as screening_type_2_register_0 |
| ETH1_SCREENING_TYPE_2_REGISTER_8 | 0x40491560 | FULL | screening type 2 register 8, same as screening_type_2_register_0 |
| ETH1_SCREENING_TYPE_2_REGISTER_9 | 0x40491564 | FULL | screening type 2 register 9, same as screening_type_2_register_0 |
| ETH1_SCREENING_TYPE_2_REGISTER_10 | 0x40491568 | FULL | screening type 2 register 10, same as screening_type_2_register_0 |
| ETH1_SCREENING_TYPE_2_REGISTER_11 | 0x4049156C | FULL | screening type 2 register 11, same as screening_type_2_register_0 |
| ETH1_SCREENING_TYPE_2_REGISTER_12 | 0x40491570 | FULL | screening type 2 register 12, same as screening_type_2_register_0 |
| ETH1_SCREENING_TYPE_2_REGISTER_13 | 0x40491574 | FULL | screening type 2 register 13, same as screening_type_2_register_0 |
| ETH1_SCREENING_TYPE_2_REGISTER_14 | 0x40491578 | FULL | screening type 2 register 14, same as screening_type_2_register_0 |
| ETH1_SCREENING_TYPE_2_REGISTER_15 | 0x4049157C | FULL | screening type 2 register 15, same as screening_type_2_register_0 |
| ETH1_TX_SCHED_CTRL | 0x40491580 | FULL | This register controls the transmit scheduling algorithm the user can select for each active transmit queue. By default all queues are initialized to fixed priority, with the top indexed queue having overall priority |
| ETH1_BW_RATE_LIMIT_Q0TO3 | 0x40491590 | FULL | This register holds the DWRR weighting value or the ETS bandwidth percentage value used by the transmit scheduler for queues 0 to 3. |
| ETH1_BW_RATE_LIMIT_Q4TO7 | 0x40491594 | FULL | Not presents. MXETH has only 3 queues. Access to the register returns AHB error. |
| ETH1_BW_RATE_LIMIT_Q8TO11 | 0x40491598 | FULL | Not presents. MXETH has only 3 queues. Access to the register returns AHB error. |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| ETH1_BW_RATE_LIMIT_Q12TO15 | 0x4049159C | FULL | Not presents. MXETH has only 3 queues. Access to the register returns AHB error. |
| ETH1_TX_Q_SEG_ALLOC_Q0TO7 | 0x404915A0 | FULL | This register allows the user to distribute the Transmit SRAM used by the DMA across the priority queues, for queues 0 to 7. The SRAM itself is split into a number of evenly sized segments (this is defined in the verilog configuration defs file - for the configuration used to generate this register description, the total number of segments was set to '16'). Those segments can then be freely distributed across the active queues, in powers of 2. I.e. a value of 0 would mean 1 segment has been allocated to the queue. A value of 1 would mean 2 segments, a value of 2 means 4 segments and so on. The reset values of these registers are defined in the configuration defs file. |
| ETH1_TX_Q_SEG_ALLOC_Q8TO15 | 0x404915A4 | FULL | Not presents. Access to the register returns AHB error. |
| ETH1_RECEIVE_Q8_PTR | 0x404915C0 | FULL | receive_q8_ptr to receive_q15_ptr doesn't present. Access to the register returns AHB error. |
| ETH1_RECEIVE_Q15_PTR | 0x404915DC | FULL | Not presents. |
| ETH1_DMA_RXBUF_SIZE_Q8 | 0x404915E0 | FULL | dma_rxbuf_size_q8 to dma_rxbuf_size_q15 doesn't present. Access to the register returns AHB error. |
| ETH1_DMA_RXBUF_SIZE_Q15 | 0x404915FC | FULL | Not presents. |
| ETH1_INT_Q1_ENABLE | 0x40491600 | FULL | At reset all interrupts are disabled. Writing a one to the relevant bit location enables the required interrupt. This register is write only and when read will return zero. |
| ETH1_INT_Q2_ENABLE | 0x40491604 | FULL | At reset all interrupts are disabled. Writing a one to the relevant bit location enables the required interrupt. This register is write only and when read will return zero. |
| ETH1_INT_Q3_ENABLE | 0x40491608 | FULL | int_q3_enable to int_q7_enable doesn't present. Access to the register returns AHB error. |
| ETH1_INT_Q7_ENABLE | 0x40491618 | FULL | Not presents. |
| ETH1_INT_Q1_DISABLE | 0x40491620 | FULL | Writing a 1 to the relevant bit location disables that particular interrupt. This register is write only and when read will return zero. |
| ETH1_INT_Q2_DISABLE | 0x40491624 | FULL | Writing a 1 to the relevant bit location disables that particular interrupt. This register is write only and when read will return zero. |
| ETH1_INT_Q3_DISABLE | 0x40491628 | FULL | int_q3_disable to int_q7_disable doesn't present. Access to the register returns AHB error. |
| ETH1_INT_Q7_DISABLE | 0x40491638 | FULL | Not presents. |
| ETH1_INT_Q1_MASK | 0x40491640 | FULL | The interrupt mask register is a read only register indicating which interrupts are masked. All bits are set at reset and can be reset individually by writing to the interrupt enable register or set individually by writing to the interrupt disable register. Having separate address locations for enable and disable saves the need for performing a read modify write when updating the interrupt mask register. For test purposes there is a write-only function to this register that allows the bits in the interrupt status register to be set or cleared, regardless of the state of the mask register. |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| ETH1_INT_Q2_MASK | 0x40491644 | FULL | The interrupt mask register is a read only register indicating which interrupts are masked. All bits are set at reset and can be reset individually by writing to the interrupt enable register or set individually by writing to the interrupt disable register. Having separate address locations for enable and disable saves the need for performing a read modify write when updating the interrupt mask register. For test purposes there is a write-only function to this register that allows the bits in the interrupt status register to be set or cleared, regardless of the state of the mask register. |
| ETH1_INT_Q3_MASK | 0x40491648 | FULL | int_q3_mask to int_q7_mask doesn't present. Access to the register returns AHB error. |
| ETH1_INT_Q7_MASK | 0x40491658 | FULL | Not presents. |
| ETH1_INT_Q8_ENABLE | 0x40491660 | FULL | int_q8_enable to int_q15_enable doesn't present. Access to the register returns AHB error. |
| ETH1_INT_Q15_ENABLE | 0x4049167C | FULL | Not presents. |
| ETH1_INT_Q8_DISABLE | 0x40491680 | FULL | int_q8_disable to int_q15_disable doesn't present. Access to the register returns AHB error. |
| ETH1_INT_Q15_DISABLE | 0x4049169C | FULL | Not presents. |
| ETH1_INT_Q8_MASK | 0x404916A0 | FULL | int_q8_mask to int_q15_mask doesn't present. Access to the register returns AHB error. |
| ETH1_INT_Q15_MASK | 0x404916BC | FULL | Not presents. |
| ETH1_SCREENING_TYPE_2_ETHERTYPE_REG_0 | 0x404916E0 | FULL | Ethertype Register |
| ETH1_SCREENING_TYPE_2_ETHERTYPE_REG_1 | 0x404916E4 | FULL | Ethertype Register |
| ETH1_SCREENING_TYPE_2_ETHERTYPE_REG_2 | 0x404916E8 | FULL | Ethertype Register |
| ETH1_SCREENING_TYPE_2_ETHERTYPE_REG_3 | 0x404916EC | FULL | Ethertype Register |
| ETH1_SCREENING_TYPE_2_ETHERTYPE_REG_4 | 0x404916F0 | FULL | Ethertype Register |
| ETH1_SCREENING_TYPE_2_ETHERTYPE_REG_5 | 0x404916F4 | FULL | Ethertype Register |
| ETH1_SCREENING_TYPE_2_ETHERTYPE_REG_6 | 0x404916F8 | FULL | Ethertype Register |
| ETH1_SCREENING_TYPE_2_ETHERTYPE_REG_7 | 0x404916FC | FULL | Ethertype Register |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| ETH1_TYPE2_COMPARE_0_WORD_0 | 0x40491700 | FULL | 'Compare A, B and C fields of the screener type 2 match register are pointers to a pool of up to 32 compare registers. If enabled the compare is true if the data at the OFFSET into the frame, ANDed with the MASK Value if the mask is enabled, is equal to the COMPARE Value. Either a 16 bit comparison or a 32 bit comparison is done. This selection is made via the associated compare word1 register bit 9. If a 16 bit comparison is selected, then a 16 bit mask is also available to the user to select which bits should be compared. If the 32 bit compare option is selected, then no mask is available. The byte at the OFFSET number of bytes from the index start is compared thru bits 7 to 0 of the configured VALUE. The byte at the OFFSET number of bytes + 1 from the index start is compared thru bits 15 to 8 of the configured VALUE and so on. The OFFSET can be configured to be from 0 to 127 bytes from either the start of the frame, the byte following the therType field (last EtherType in the header if the frame is VLAN tagged), the byte following the IP header (IPv4 or IPv6) or from the byte following the start of the TCP/UDP header. The required number of Type 2 screening registers up to a maximum of 32 is configurable in the gem defines file and have been allocated APB address space between 0x700 and 0x7fc. Note. when using RX Partial Store and Forward mode and priority queues, the frame offset must be less than the Partial Store and Forward watermark. If the offset is higher than the watermark value it's not possible to identify the priority queue before the frame is sent to the AMBA interface, and an incorrect priority queue may be used. ' |
| ETH1_TYPE2_COMPARE_0_WORD_1 | 0x40491704 | FULL | 'Type2 Compare Word 1' |
| ETH1_TYPE2_COMPARE_1_WORD_0 | 0x40491708 | FULL | same as type2_compare_0_word_0 |
| ETH1_TYPE2_COMPARE_1_WORD_1 | 0x4049170C | FULL | same as type2_compare_0_word_1 |
| ETH1_TYPE2_COMPARE_2_WORD_0 | 0x40491710 | FULL | same as type2_compare_0_word_0 |
| ETH1_TYPE2_COMPARE_2_WORD_1 | 0x40491714 | FULL | same as type2_compare_0_word_1 |
| ETH1_TYPE2_COMPARE_3_WORD_0 | 0x40491718 | FULL | same as type2_compare_0_word_0 |
| ETH1_TYPE2_COMPARE_3_WORD_1 | 0x4049171C | FULL | same as type2_compare_0_word_1 |
| ETH1_TYPE2_COMPARE_4_WORD_0 | 0x40491720 | FULL | same as type2_compare_0_word_0 |
| ETH1_TYPE2_COMPARE_4_WORD_1 | 0x40491724 | FULL | same as type2_compare_0_word_1 |
| ETH1_TYPE2_COMPARE_5_WORD_0 | 0x40491728 | FULL | same as type2_compare_0_word_0 |
| ETH1_TYPE2_COMPARE_5_WORD_1 | 0x4049172C | FULL | same as type2_compare_0_word_1 |
| ETH1_TYPE2_COMPARE_6_WORD_0 | 0x40491730 | FULL | same as type2_compare_0_word_0 |
| ETH1_TYPE2_COMPARE_6_WORD_1 | 0x40491734 | FULL | same as type2_compare_0_word_1 |
| ETH1_TYPE2_COMPARE_7_WORD_0 | 0x40491738 | FULL | same as type2_compare_0_word_0 |
| ETH1_TYPE2_COMPARE_7_WORD_1 | 0x4049173C | FULL | same as type2_compare_0_word_1 |
| ETH1_TYPE2_COMPARE_8_WORD_0 | 0x40491740 | FULL | same as type2_compare_0_word_0 |
| ETH1_TYPE2_COMPARE_8_WORD_1 | 0x40491744 | FULL | same as type2_compare_0_word_1 |
| ETH1_TYPE2_COMPARE_9_WORD_0 | 0x40491748 | FULL | same as type2_compare_0_word_0 |
| ETH1_TYPE2_COMPARE_9_WORD_1 | 0x4049174C | FULL | same as type2_compare_0_word_1 |
| ETH1_TYPE2_COMPARE_10_WORD_0 | 0x40491750 | FULL | same as type2_compare_0_word_0 |
| ETH1_TYPE2_COMPARE_10_WORD_1 | 0x40491754 | FULL | same as type2_compare_0_word_1 |
| ETH1_TYPE2_COMPARE_11_WORD_0 | 0x40491758 | FULL | same as type2_compare_0_word_0 |
| ETH1_TYPE2_COMPARE_11_WORD_1 | 0x4049175C | FULL | same as type2_compare_0_word_1 |
| ETH1_TYPE2_COMPARE_12_WORD_0 | 0x40491760 | FULL | same as type2_compare_0_word_0 |
| ETH1_TYPE2_COMPARE_12_WORD_1 | 0x40491764 | FULL | same as type2_compare_0_word_1 |
| ETH1_TYPE2_COMPARE_13_WORD_0 | 0x40491768 | FULL | same as type2_compare_0_word_0 |
| ETH1_TYPE2_COMPARE_13_WORD_1 | 0x4049176C | FULL | same as type2_compare_0_word_1 |
| ETH1_TYPE2_COMPARE_14_WORD_0 | 0x40491770 | FULL | same as type2_compare_0_word_0 |
| ETH1_TYPE2_COMPARE_14_WORD_1 | 0x40491774 | FULL | same as type2_compare_0_word_1 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| ETH1_TYPE2_COMPARE_15_WORD_0 | 0x40491778 | FULL | same as type2_compare_0_word_0 |
| ETH1_TYPE2_COMPARE_15_WORD_1 | 0x4049177C | FULL | same as type2_compare_0_word_1 |
| ETH1_TYPE2_COMPARE_16_WORD_0 | 0x40491780 | FULL | same as type2_compare_0_word_0 |
| ETH1_TYPE2_COMPARE_16_WORD_1 | 0x40491784 | FULL | same as type2_compare_0_word_1 |
| ETH1_TYPE2_COMPARE_17_WORD_0 | 0x40491788 | FULL | same as type2_compare_0_word_0 |
| ETH1_TYPE2_COMPARE_17_WORD_1 | 0x4049178C | FULL | same as type2_compare_0_word_1 |
| ETH1_TYPE2_COMPARE_18_WORD_0 | 0x40491790 | FULL | same as type2_compare_0_word_0 |
| ETH1_TYPE2_COMPARE_18_WORD_1 | 0x40491794 | FULL | same as type2_compare_0_word_1 |
| ETH1_TYPE2_COMPARE_19_WORD_0 | 0x40491798 | FULL | same as type2_compare_0_word_0 |
| ETH1_TYPE2_COMPARE_19_WORD_1 | 0x4049179C | FULL | same as type2_compare_0_word_1 |
| ETH1_TYPE2_COMPARE_20_WORD_0 | 0x404917A0 | FULL | same as type2_compare_0_word_0 |
| ETH1_TYPE2_COMPARE_20_WORD_1 | 0x404917A4 | FULL | same as type2_compare_0_word_1 |
| ETH1_TYPE2_COMPARE_21_WORD_0 | 0x404917A8 | FULL | same as type2_compare_0_word_0 |
| ETH1_TYPE2_COMPARE_21_WORD_1 | 0x404917AC | FULL | same as type2_compare_0_word_1 |
| ETH1_TYPE2_COMPARE_22_WORD_0 | 0x404917B0 | FULL | same as type2_compare_0_word_0 |
| ETH1_TYPE2_COMPARE_22_WORD_1 | 0x404917B4 | FULL | same as type2_compare_0_word_1 |
| ETH1_TYPE2_COMPARE_23_WORD_0 | 0x404917B8 | FULL | same as type2_compare_0_word_0 |
| ETH1_TYPE2_COMPARE_23_WORD_1 | 0x404917BC | FULL | same as type2_compare_0_word_1 |
| ETH1_TYPE2_COMPARE_24_WORD_0 | 0x404917C0 | FULL | same as type2_compare_0_word_0 |
| ETH1_TYPE2_COMPARE_24_WORD_1 | 0x404917C4 | FULL | same as type2_compare_0_word_1 |
| ETH1_TYPE2_COMPARE_25_WORD_0 | 0x404917C8 | FULL | same as type2_compare_0_word_0 |
| ETH1_TYPE2_COMPARE_25_WORD_1 | 0x404917CC | FULL | same as type2_compare_0_word_1 |
| ETH1_TYPE2_COMPARE_26_WORD_0 | 0x404917D0 | FULL | same as type2_compare_0_word_0 |
| ETH1_TYPE2_COMPARE_26_WORD_1 | 0x404917D4 | FULL | same as type2_compare_0_word_1 |
| ETH1_TYPE2_COMPARE_27_WORD_0 | 0x404917D8 | FULL | same as type2_compare_0_word_0 |
| ETH1_TYPE2_COMPARE_27_WORD_1 | 0x404917DC | FULL | same as type2_compare_0_word_1 |
| ETH1_TYPE2_COMPARE_28_WORD_0 | 0x404917E0 | FULL | same as type2_compare_0_word_0 |
| ETH1_TYPE2_COMPARE_28_WORD_1 | 0x404917E4 | FULL | same as type2_compare_0_word_1 |
| ETH1_TYPE2_COMPARE_29_WORD_0 | 0x404917E8 | FULL | same as type2_compare_0_word_0 |
| ETH1_TYPE2_COMPARE_29_WORD_1 | 0x404917EC | FULL | same as type2_compare_0_word_1 |
| ETH1_TYPE2_COMPARE_30_WORD_0 | 0x404917F0 | FULL | same as type2_compare_0_word_0 |
| ETH1_TYPE2_COMPARE_30_WORD_1 | 0x404917F4 | FULL | same as type2_compare_0_word_1 |
| ETH1_TYPE2_COMPARE_31_WORD_0 | 0x404917F8 | FULL | same as type2_compare_0_word_0 |
| ETH1_TYPE2_COMPARE_31_WORD_1 | 0x404917FC | FULL | same as type2_compare_0_word_1 |

## 11.3 Register Details

### 11.3.1 ETH_CTL

**Description:** MXETH Control Register
**Address:** 0x40480000
**Offset:** 0x0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** The field ETH_MODE and REFCLK_SRC will select clock source for MAC transmit and receive logic in different Eth mode, it should NOT be changed while ENABLED is '1'.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:3] | | | | | REFCLK_SRC_SEL [2:2] | ETH_MODE [1:0] | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | REFCLK_DIV [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | ENABLED [31:31] | None [30:24] | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:1 | ETH_MODE | RW | R | 0 | Set ethernet mode. The speed of 10M/100M/1G is selected by programming network_config after IP is enabled.<br>The field also specifies the clock source of internal tx_clk and rx_clk domain. |
| | MII | | | 0 | MII mode (10/100MHz speed is determined by network_config[0]). |
| | GMII | | | 1 | GMII mode (network_config[10] must be set to enable 1G operation). |
| | RGMII | | | 2 | RGMII mode (10M/100M/1G speed is determined by network_config[10] and network_config[0]). |
| | RMII | | | 3 | RMII mode (10M/100M speed is determined by network_config[0]). |
| 2 | REFCLK_SRC_SEL | RW | R | 0 | Select the source for ref_clk.<br>0: Ref_clk comes from REF_CLK_IN input port (HSIO).<br>1: Ref_clk comes from REF_CLK_INT_IN input port (PLL). |
| 8:15 | REFCLK_DIV | RW | R | 0 | Specify the ref_clk divider. Integer division by (1+REFCLK_DIV). Allows for integer divisions in the range [1, 256]. |
| 31 | ENABLED | RW | R | 0 | MXETH enable:<br>'0': Disabled.<br>'1': Enabled. |

### 11.3.2 ETH_STATUS

**Description:** MXETH Status Register
**Address:** 0x40480004
**Offset:** 0x4
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:1] | | | | | | | PFC_NEGOTIATE [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | RX_PFC_PAUSED [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | PFC_NEGOTIATE | R | W | 0 | Identifies that PFC priority based pause flow control has been negotiated.<br>0 - No PFC priority based pause frames have yet been received, flow control is being handled using classic 802.3 pause frames.<br>1 - At least one PFC priority based pause frames has been received. All subsequent 802.3 pause frames will be dropped. |
| 8:15 | RX_PFC_PAUSED | R | W | 0 | Each bit corresponds to a priority indicated within the PFC priority based pause frame.<br>Each bit is set when a PFC priority based pause frame has been received, and the associated priority pause time quantum is non-zero. Each bit is cleared when the associated pause time identified by the received pause time quantum has elapsed. |

### 11.3.3 ETH_NETWORK_CONTROL

**Description:** The network control register contains general MAC control functions for both receiver and transmitter.
**Address:** 0x40481000
**Offset:** 0x1000
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | STATS_WRITE_EN [7:7] | INC_ALL_STATS_REGS [6:6] | CLEAR_ALL_STATS_REGS [5:5] | MAN_PORT_EN [4:4] | ENABLE_TRANSMIT [3:3] | ENABLE_RECEIVE [2:2] | LOOPBACK_LOCAL [1:1] | LOOPBACK [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | STORE_RX_TS [15:15] | REMOVED_14 [14:14] | REMOVED_13 [13:13] | TX_PAUSE_FRAME_ZERO [12:12] | TX_PAUSE_FRAME_REQ [11:11] | TX_HALT_PCLK [10:10] | TX_START_PCLK [9:9] | BACK_PRESSURE [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | EXT_TSU_PORT_ENABLE [23:23] | STORE_UDP_OFFSET [22:22] | ALT_SGMII_MODE [21:21] | PTP_UNICAST_ENA [20:20] | TX_LPI_EN [19:19] | FLUSH_RX_PKT_PCLK [18:18] | TRANSMIT_PFC_PRIORITY_BASED_PAUSE_FRAME [17:17] | PFC_ENABLE [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | EXT_RXQ_RESERVED_31 [31:31] | IFG_EATS_QAV_CREDIT [30:30] | TWO_PT_FIVE_GIG [29:29] | SEL_MII_ON_RGMII [28:28] | OSS_CORRECTION_FIELD [27:27] | EXT_RXQ_SEL_EN [26:26] | PFC_CTRL [25:25] | ONE_STEP_SYNC_MODE [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | LOOPBACK | RW | R | 0 | Loopback - controls the loopback output pin. |
| 1 | LOOPBACK_LOCAL | RW | R | 0 | Loopback local - asserts the loopback_local signal to the system clock generator. Also connects txd to rxd, tx_en to rx_dv and forces full duplex mode. Bit 11 of the network configuration register must be set low to disable TBI mode when in internal loopback. rx_clk and tx_clk may malfunction as the GEM is switched into and out of internal loopback. It is important that receive and transmit circuits have already been disabled when making the switch into and out of internal loopback. Local loopback functionality is optional and may not be supported by some instantiations of the GEM. |
| 2 | ENABLE_RECEIVE | RW | R | 0 | Receive enable - when set, it enables the GEM to receive data. When reset frame reception will stop immediately and the receive pipeline will be cleared. The receive queue pointer register is unaffected. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 3 | ENABLE_TRANSMIT | RW | R | 0 | Transmit enable - when set, it enables the GEM transmitter to send data. When reset transmission will stop immediately, the transmit pipeline and control registers will be cleared and the transmit queue pointer register will reset to point to the start of the transmit descriptor list. |
| 4 | MAN_PORT_EN | RW | R | 0 | Management port enable - set to one to enable the management port. When zero forces mdio to high impedance state and mdc low. |
| 5 | CLEAR_ALL_STATS _REGS | W | R | 0 | Clear statistics registers - this bit is write only. Writing a one clears the statistics registers. Self clearing register. |
| 6 | INC_ALL_STATS_REGS | W | R | 0 | Incremental statistics registers - this bit is write only. Writing a one increments all the statistics registers by one for test purposes. Self clearing register. |
| 7 | STATS_WRITE_EN | RW | R | 0 | Write enable for statistics registers - setting this bit to one means the statistics registers can be written for functional test purposes. |
| 8 | BACK_PRESSURE | RW | R | 0 | Back pressure if set in 10M or 100M half duplex mode will force collisions on all received frames. Ignored in gigabit half duplex mode. |
| 9 | TX_START_PCLK | W | R | 0 | Start transmission - writing one to this bit starts transmission. |
| 10 | TX_HALT_PCLK | W | R | 0 | Transmit halt - writing one to this bit halts transmission as soon as any ongoing frame transmission ends. |
| 11 | TX_PAUSE_FRAME _REQ | W | R | 0 | Transmit pause frame - writing one to this bit causes a pause frame to be transmitted. Self clearing register. |
| 12 | TX_PAUSE_FRAME _ZERO | W | R | 0 | Transmit zero quantum pause frame - writing one to this bit causes a pause frame with zero quantum to be transmitted. |
| 13 | REMOVED_13 | R | R | 0 | Write ignore, read 0 |
| 14 | REMOVED_14 | R | R | 0 | Write ignore, read 0 |
| 15 | STORE_RX_TS | RW | R | 0 | Store receive time stamp to memory. Setting this bit to one will cause the CRC of every received frame to be replaced with the value of the nanoseconds field of the 1588 timer that was captured as the receive frame passed the message time stamp point. Set to zero for normal operation. |
| 16 | PFC_ENABLE | RW | R | 0 | Enable PFC Priority Based Pause Reception capabilities. Setting this bit will enable PFC negotiation and recognition of priority based pause frames. |
| 17 | TRANSMIT_PFC_PRIORI TY_BASED_PAUSE _FRAME | W | R | 0 | Write a one to transmit PFC priority based pause frame. Takes the values stored in the Transmit PFC Pause Register. Self clearing register. |
| 18 | FLUSH_RX_PKT_PCLK | W | R | 0 | Flush the next packet from the external RX DPRAM. Writing one to this bit will only have an effect if the DMA is not currently writing a packet already stored in the DPRAM to memory. Self clearing register. |
| 19 | TX_LPI_EN | RW | R | 0 | Enable LPI transmission when set LPI (low power idle) is immediately transmitted. LPI is transmitted even if bit 3 transmit enable is disabled. Setting this bit also sends a pause signal to the transmit datapath. |
| 20 | PTP_UNICAST_ENA | RW | R | 0 | Enable detection of unicast PTP unicast frames. |
| 21 | ALT_SGMII_MODE | RW | R | 0 | Alternative sgmii mode. If asserted with sgmii_mode in the network control register the ACK bit is driven before ability detect during transfer of status information from the PHY to the MAC. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 22 | STORE_UDP_OFFSET | RW | R | 0 | Store UDP / TCP offset to memory. Setting this bit to one will cause the upper 16-bits of the CRC of every received frame to be replaced with the offset from start of frame to the beginning of the UDP or TCP header. The lower 16-bits of the CRC are replaced with zero and reserved for future use. The offset is measured in units of 2 bytes. Set to zero for normal operation. |
| 23 | EXT_TSU_PORT _ENABLE | R | R | 0 | Write ignore, read 0 |
| 24 | ONE_STEP_SYNC _MODE | RW | R | 0 | 1588 One Step Sync Mode. Write 1 to enable. Replace timestamp field in the 1588 header for TX Sync Frames with current TSU timer value. |
| 25 | PFC_CTRL | RW | R | 0 | 'Enable multiple PFC pause quantums, one per pause priority' |
| 26 | EXT_RXQ_SEL_EN | RW | R | 0 | Enable external selection of receive queue. When this bit is high the ext_match1, ext_match2, ext_match3 and ext_match4 inputs will determine which receive queue a frame is routed to. This will be the case regardless of the state of the external address match enable bit 9 of the network config register. Note that receive frames will be dropped unless they are matched by the internal frame filtering functionality. If the external address match enable bit 9 in the network config register is set frames may be matched by an external address match filter as long as one of the ext_match1, ext_match2, ext_match3 and ext_match4 inputs is asserted early enough. When set ext_rxq_sel_en takes precedence over the existing screener functionality. This bit is only relevant if priority queuing is configured. |
| 27 | OSS_CORRECTION _FIELD | RW | R | 0 | 1588 One Step Correction Field Update. Set this bit high to enable updating the correction field of PTP 1588 version 2 sync frames by adding current TSU timer value. |
| 28 | SEL_MII_ON_RGMII | RW | R | 0 | If the RGMII interface being used set this bit high to configure the interface for MII operation. |
| 29 | TWO_PT_FIVE_GIG | RW | R | 0 | 2.5G operation selected - setting this bit high drives the speed_mode[3] top level output pin high and also adjusts the link timer in the PCS auto-negotiation block to ensure it delivers 10ms for 2500BASE-X and 1.6ms in SGMII mode, and also ensures int_moderation counts 800ns periods with the speeded up MAC clocks. |
| 30 | IFG_EATS_QAV_CREDIT | RW | R | 0 | Setting this bit high modifies the CBS algorithm so the IFG/IPG associated with a transmit frame counts towards its 802.1Qav credit. |
| 31 | EXT_RXQ_RESERVED _31 | R | R | 0 | Reserved, read as 0, ignored on write. |

### 11.3.4 ETH_NETWORK_CONFIG

**Description:** The network configuration register contains functions for setting the mode of operation for the Gigabit Ethernet MAC.
**Address:** 0x40481004
**Offset:** 0x1004
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x2C0000

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | UNICAST_HASH_ENABLE [7:7] | MULTICAST_HASH_ENABLE [6:6] | NO_BROADCAST [5:5] | COPY_ALL_FRAMES [4:4] | JUMBO_FRAMES [3:3] | DISCARD_NON_VLAN_FRAMES [2:2] | FULL_DUPLEX [1:1] | SPEED [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | RECEIVE_BUFFER_OFFSET [15:14] | | PAUSE_ENABLE [13:13] | RETRY_TEST [12:12] | PCS_SELECT [11:11] | GIGABIT_MODE_ENABLE [10:10] | EXTERNAL_ADDRESS_MATCH_ENABLE [9:9] | RECEIVE_1536_BYTE_FRAMES [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | DISABLE_COPY_OF_PAUSE_FRAMES [23:23] | DATA_BUS_WIDTH [22:21] | | MDC_CLOCK_DIVISION [20:18] | | | FCS_REMOVE [17:17] | LENGTH_FIELD_ERROR_FRAME_DISCARD [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31 [31:31] | IGNORE_IPG_RX_ER [30:30] | NSP_CHANGE [29:29] | IPG_STRETCH_ENABLE [28:28] | SGMII_MODE_ENABLE [27:27] | IGNORE_RX_FCS [26:26] | EN_HALF_DUPLEX_RX [25:25] | RECEIVE_CHECKSUM_OFFLOAD_ENABLE [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | SPEED | RW | R | 0 | Speed - set to logic one to indicate 100Mbps operation, logic zero for 10Mbps. |
| 1 | FULL_DUPLEX | RW | R | 0 | Full duplex - if set to logic one, the transmit block ignores the state of collision and carrier sense and allows receive while transmitting. Also controls the half_duplex pin. |
| 2 | DISCARD_NON_VLAN_FRAMES | RW | R | 0 | Discard non-VLAN frames - when set only VLAN tagged frames will be passed to the address matching logic. |
| 3 | JUMBO_FRAMES | RW | R | 0 | Jumbo frames - set to one to enable jumbo frames up to `gem_jumbo_max_length bytes to be accepted. The default length is 10,240 bytes. |
| 4 | COPY_ALL_FRAMES | RW | R | 0 | Copy all frames - when set to logic one, all valid frames will be accepted. |
| 5 | NO_BROADCAST | RW | R | 0 | No broadcast - when set to logic one, frames addressed to the broadcast address of all ones will not be accepted. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 6 | MULTICAST_HASH _ENABLE | RW | R | 0 | Multicast hash enable - when set, multicast frames will be accepted when the 6 bit hash function of the destination address points to a bit that is set in the hash register. |
| 7 | UNICAST_HASH _ENABLE | RW | R | 0 | Unicast hash enable - when set, unicast frames will be accepted when the 6 bit hash function of the destination address points to a bit that is set in the hash register. |
| 8 | RECEIVE_1536_BYTE_F RAMES | RW | R | 0 | Receive 1536 byte frames - setting this bit means the GEM will accept frames up to 1536 bytes in length. Normally the GEM would reject any frame above 1518 bytes. |
| 9 | EXTERNAL_ADDRESS _MATCH_ENABLE | RW | R | 0 | External address match enable - when set the external address match interface can be used to copy frames to memory. |
| 10 | GIGABIT_MODE _ENABLE | RW | R | 0 | Gigabit mode enable - setting this bit configures the GEM for 1000 Mbps operation.<br>0: 10/100 operation using MII interface<br>1: Gigabit operation using GMI interface |
| 11 | PCS_SELECT | RW | R | 0 | PCS select - selects between MII/GMII and TBI |
| 12 | RETRY_TEST | RW | R | 0 | Retry test - must be set to zero for normal operation. If set to one the backoff between collisions will always be one slot time. Setting this bit to one helps test the too many retries condition. Also used in the pause frame tests to reduce the pause counter's decrement time from 512 bit times, to every rx_clk cycle. |
| 13 | PAUSE_ENABLE | RW | R | 0 | Pause enable - when set, transmission will pause if a non zero 802.3 classic pause frame is received and PFC has not been negotiated. |
| 14:15 | RECEIVE_BUFFER _OFFSET | RW | R | 0 | Receive buffer offset - indicates the number of bytes by which the received data is offset from the start of the receive buffer. |
| 16 | LENGTH_FIELD_ERROR _FRAME_DISCARD | RW | R | 0 | Length field error frame discard - setting this bit causes frames with a measured length shorter than the extracted length field (as indicated by bytes 13 and 14 in a non-VLAN tagged frame) to be discarded. This only applies to frames with a length field less than 0x0600. |
| 17 | FCS_REMOVE | RW | R | 0 | FCS remove - setting this bit will cause received frames to be written to memory without their frame check sequence (last 4 bytes). The frame length indicated will be reduced by four bytes in this mode. |
| 18:20 | MDC_CLOCK_DIVISION | RW | R | 3 | MDC clock division - set according to pclk speed. These three bits determine the number pclk will be divided by to generate MDC. For conformance with the 802.3 specification, MDC must not exceed 2.5 MHz (MDC is only active during MDIO read and write operations). The reset value for this can be changed by defining a new value for gem_mdc_clock_div in gem_defs.v<br>000: divide pclk by 8 (pclk up to 20 MHz)<br>001: divide pclk by 16 (pclk up to 40 MHz)<br>010: divide pclk by 32 (pclk up to 80 MHz)<br>011: divide pclk by 48 (pclk up to 120MHz)<br>100: divide pclk by 64 (pclk up to 160 MHz)<br>101: divide pclk by 96 (pclk up to 240 MHz)<br>110: divide pclk by 128 (pclk up to 320 MHz)<br>111: divide pclk by 224 (pclk up to 540 MHz).<br>Note. The reset value of this field is equal to the gem_mdc_clock_div define, which is user configurable. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 21:22 | DATA_BUS_WIDTH | RW | R | 1 | Data bus width - set according to AMBA (AXI) or external FIFO data bus width. The reset value for this can be changed by defining a new value for gem_dma_bus_width_def in gem_defs. Only valid bus widths may be written if the system is configured to a maximum width less than 128-bits.<br>00: 32 bit data bus width 01: 64 bit AMBA (AXI) data bus width<br>10: 128 bit AMBA (AXI) data bus width<br>11: 128 bit AMBA (AXI) data bus width.<br>Note. The reset value of this field is equal to the gem_dma_bus_width_def define, which is user configurable.<br>MXETH only supports 64b DMA data bus width, so must set it 1. |
| 23 | DISABLE_COPY_OF_PAUSE_FRAMES | RW | R | 0 | Disable copy of pause frames - set to one to prevent pause frames being copied to memory. When set, neither control frames with type id 8808, nor pause frames with destination address 010000c28001 are copied to memory, this functionality was enhanced in release 1p09 (mxeth uses 1p09). Note that valid pause frames received will still increment pause statistics and pause the transmission of frames as required. |
| 24 | RECEIVE_CHECKSUM_OFFLOAD_ENABLE | RW | R | 0 | Receive checksum offload enable - when set, the receive checksum engine is enabled. Frames with bad IP, TCP or UDP checksums are discarded. |
| 25 | EN_HALF_DUPLEX_RX | RW | R | 0 | Enable frames to be received in half-duplex mode while transmitting. |
| 26 | IGNORE_RX_FCS | RW | R | 0 | Ignore RX FCS - when set frames with FCS/CRC errors will not be rejected. FCS error statistics will still be collected for frames with bad FCS and FCS status will be recorded in frame's DMA descriptor. For normal operation this bit must be set to zero. |
| 27 | SGMII_MODE_ENABLE | RW | R | 0 | SGMII mode enable - changes behaviour of the auto-negotiation advertisement and link partner ability registers to meet the requirements of SGMII and reduces the duration of the link timer from 10 ms to 1.6 ms. |
| 28 | IPG_STRETCH_ENABLE | RW | R | 0 | IPG stretch enable - when set the transmit IPG can be increased above 96 bit times depending on the previous frame length using the IPG stretch register. |
| 29 | NSP_CHANGE | RW | R | 0 | Receive bad preamble. When set frames with non-standard preamble are not rejected. |
| 30 | IGNORE_IPG_RX_ER | RW | R | 0 | Ignore IPG rx_er. When set rx_er has no effect on the GEMs operation when rx_dv is low. Set this when using the RGMII wrapper in half-duplex mode. |
| 31 | RESERVED_31 | RW | R | 0 | Reserved. Writeable register. Ignore on read. |

### 11.3.5 ETH_NETWORK_STATUS

**Description:** The network status register returns status information with respect to the PHY management interface.
**Address:** 0x40481008
**Offset:** 0x1008
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x6

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | LPI_INDICATE_PCLK [7:7] | PFC_NEGOTIATE_PCLK [6:6] | REMOVED_5_4 [5:4] | | MAC_FULL_DUPLEX [3:3] | MAN_DONE [2:2] | MDIO_IN [1:1] | PCS_LINK_STATE [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | PCS_LINK_STATE | R | W | 0 | Returns status of PCS link state. If auto-negotiation is disabled this returns the synchronisation status. If auto-negotiation is enabled it is set in the LINK_OK state as long as a compatible duplex mode is resolved. |
| 1 | MDIO_IN | R | W | 1 | Returns status of the mdio_in pin. |
| 2 | MAN_DONE | R | W | 1 | The PHY management logic is idle (i.e. has completed). |
| 3 | MAC_FULL_DUPLEX | R | W | 0 | PCS auto-negotiation duplex resolution. Set to one if the resolution function determines that both devices are capable of full duplex operation. If zero half-duplex operation is possible as long as bit 0 (PCS link state) is also one. |
| 4:5 | REMOVED_5_4 | R | W | 0 | Reserved, read as 0, ignored on write. |
| 6 | PFC_NEGOTIATE_PCLK | R | W | 0 | Set when PFC Priority Based Pause has been negotiated. |
| 7 | LPI_INDICATE_PCLK | R | W | 0 | LPI Indication - Low power idle has been detected on receive. This bit is set when LPI is detected and reset when normal idle is detected. An interrupt is generated when the state of this bit changes. |

### 11.3.6 ETH_USER_IO_REGISTER

**Description:** Not presents. Access to the register will return AHB error.
**Address:** 0x4048100C
**Offset:** 0x100C
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_0 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_0 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_0 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_0 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | RESERVED_31_0 | R | R | 0 | Write ignore, read 0 |

### 11.3.7 ETH_DMA_CONFIG

**Description:** DMA Configuration Register
**Address:** 0x40481010
**Offset:** 0x1010
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x180704

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | ENDIAN_SWAP_PACKET [7:7] | ENDIAN_SWAP_MANAGEMENT [6:6] | HDR_DATA_SPLITTING_EN [5:5] | AMBA_BURST_LENGTH [4:0] | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:14] | | CRC_ERROR_REPORT [13:13] | INFINITE_LAST_DBUF_SIZE_EN [12:12] | TX_PBUF_TCP_EN [11:11] | TX_PBUF_SIZE [10:10] | RX_PBUF_SIZE [9:8] | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | RX_BUF_SIZE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:31] | DMA_ADDR_BUS_WIDTH_1 [30:30] | TX_BD_EXTENDED_MODE_EN [29:29] | RX_BD_EXTENDED_MODE_EN [28:28] | None [27:27] | FORCE_MAX_AMBA_BURST_TX [26:26] | FORCE_MAX_AMBA_BURST_RX [25:25] | FORCE_DISCARD_ON_ERR [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:4 | AMBA_BURST_LENGTH | RW | R | 4 | Selects the burst length to use on the AMBA (AHB/AXI) when transferring frame data. Not used for DMA management operations and only used where space and data size allow and respecting AXI/AHB burst boundary rules. One-hot priority encoding enforced automatically on register writes as follows, where x represents don't care:<br>1xxxx: Attempt to use bursts of up to 16.<br>01xxx: Attempt to use bursts of up to 8.<br>001xx: Attempt to use bursts of up to 4.<br>0001x: Always use SINGLE bursts.<br>00001: Always use SINGLE bursts.<br>00000: Attempt to use bursts of up to 256.<br>Note: MXETH only supports burst length up to 16. |
| 5 | HDR_DATA_SPLITTING_EN | RW | R | 0 | Enable header data Splitting. When set, receive frames will be forwarded to main memory using a minimum of two DMA data buffers. The first X data buffers will contain the frame header, consisting of the Ethernet,VLAN,(IPv4 or IPv6),(TCP or UDP). X= (frame header size divided by rx_buf_size as defined in bits 23:16 of this register). The last Y data buffers will contain the frame payload. Y= (frame payload size divided by rx_buf_size). Note that for non VLAN/IP/TCP/UDP frames, the header will always be 14 bytes. When this feature is disabled, the frame is forwarded to main memory in blocks of rx_buf_size. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 6 | ENDIAN_SWAP _MANAGEMENT | RW | R | 0 | endian swap mode enable for management descriptor accesses. When set, selects swapped endianism for AMBA (AXI) transfers. When clear, selects little endian mode. Note, the default value of this bit equals to `gem_endian_swap_def, which is design time configuration. |
| 7 | ENDIAN_SWAP _PACKET | RW | R | 0 | endian swap mode enable for packet data accesses. When set, selects swapped endianism for AMBA (AXI) transfers. When clear, selects little endian mode. Note, the default value of this bit equals to `gem_endian_swap_def, which is design time configuration. |
| 8:9 | RX_PBUF_SIZE | RW | R | 3 | Receiver packet buffer memory size select. Having these bits at less than 11 reduces the amount of memory used for the receive packet buffer. This reduces the amount of memory used by the GEM. It is important to set these bits both to one if the full configured physical memory is available. The value in brackets below represents the size that would result for the default maximum configured memory size of 8 Kbytes.<br>11: Use full configured addressable space (8 Kb)<br>10: Do not use top address bit (4 Kb)<br>01: Do not use top two address bits (2 Kb)<br>00: Do not use top three address bits (1 Kb)<br>If the GEM is not configured to use the DMA packet buffer, these bits are not implemented and will be treated as reserved, read as 0, ignored on write. Note. The reset value of this field is equal to the gem_rx_pbuf_size_def define, which is user configurable. |
| 10 | TX_PBUF_SIZE | RW | R | 1 | Transmitter packet buffer memory size select. Having this bit at zero halves the amount of memory used for the transmit packet buffer. This reduces the amount of memory used by the GEM. It is important to set this bit to one if the full configured physical memory is available. The value in brackets below represents the size that would result for the default maximum configured memory size of 4 Kbytes.<br>1: Use full configured addressable space (4 Kb)<br>0: Do not use top address bit (2 Kb)<br>If the GEM is not configured to use the DMA packet buffer, this bit is not implemented and will be treated as reserved, read as 0, ignored on write. Note. The reset value of this field is equal to the gem_tx_pbuf_size_def define, which is user configurable. |
| 11 | TX_PBUF_TCP_EN | RW | R | 0 | Transmitter IP, TCP and UDP checksum generation offload enable (not supported when in TX Partial Store and Forward mode). When set, the transmitter checksum generation engine is enabled, to calculate and substitute checksums for transmit frames. When clear, frame data is unaffected. If the GEM is not configured to use the DMA packet buffer, this bit is not implemented and will be treated as reserved, read as 0, ignored on write. |
| 12 | INFINITE_LAST_DBUF_ SIZE_EN | RW | R | 0 | Forces the DMA to consider the data buffer pointed to by last descriptor in the descriptor list to be of infinite size. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 13 | CRC_ERROR_REPORT | RW | R | 0 | When the bit is set, bit 16 of the receive buffer descriptor will represent FCS/CRC error (only if frames with FCS are copied to memory as enabled by bit 26 in the network config register). When this bit is clear, bit 16 of the receive buffer descriptor will represent the Canonical format indicator (CFI) bit as extracted from the receive frame (if the receive buffer descriptor is pointing to the last data buffer of the receive frame and the received frame was VLAN tagged). |
| 16:23 | RX_BUF_SIZE | RW | R | 24 | DMA receive buffer size in external AMBA (AXI) system memory. The value defined by these bits determines the size of buffer to use in main system memory when writing received data. The value is defined in multiples of 64 bytes.<br>0x01 corresponds to buffers of 64 bytes<br>0x02 corresponds to 128 bytes etc.<br>For example:<br>0x02: 128 byte.<br>0x18: 1536 byte (1*max length frame/buffer)<br>0xA0: 10240 byte (1*10K jumbo frame/buffer)<br>Note that this value should never be written as zero.<br>Note. The reset value of this field is equal to the gem_rx_buffer_length_def define, which is user configurable. |
| 24 | FORCE_DISCARD_ON_ERR | RW | R | 0 | Auto Discard RX pkts during lack of resource. When set, the GEM DMA will automatically discard receive packets from the receiver packet buffer memory when no AMBA (AXI) resource is available. When low, then received packets will remain to be stored in the SRAM based packet buffer until AMBA (AXI) buffer resource next becomes available. A write to this bit is ignored if the DMA is not configured in the packet buffer full store and forward mode. |
| 25 | FORCE_MAX_AMBA_BURST_RX | RW | R | 0 | Force max length bursts on RX. Force the RX DMA to always issue max length bursts on EOP(end of packet) or EOB(end of buffer)transfers, even if there is less than max burst real packet data required to write. Any extra bytes of pad data is set to 0x00. Does not apply on bursts that break 1k boundary rule. |
| 26 | FORCE_MAX_AMBA_BURST_TX | RW | R | 0 | Force max length bursts on TX. Force the TX DMA to always issue max length bursts on EOP(end of packet) or EOB(end of buffer) transfers as defined by bits 4:0 of this register, even when there is less that max burst data bytes to read. Residual data read is ignored. Does not apply on bursts that break 1k boundary rule. |
| 28 | RX_BD_EXTENDED_MODE_EN | RW | R | 0 | Enable RX extended BD mode. See RX BD control register definition for description of feature. |
| 29 | TX_BD_EXTENDED_MODE_EN | RW | R | 0 | Enable TX extended BD mode. See TX BD control register definition for description of feature. |
| 30 | DMA_ADDR_BUS_WIDTH_1 | RW | R | 0 | DMA address bus width. 0 = 32b, 1 = 64b. MXETH only supports 32b DMA address bus width, so must set it 0. |

### 11.3.8 ETH_TRANSMIT_STATUS

**Description:** This register, when read, provides details of the status of a transmit. Once read, individual bits may be cleared by writing 1 to them. It is not possible to set a bit to 1 by writing to the register.
**Address:** 0x40481014
**Offset:** 0x1014
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | LATE_COLLISION_OCCURRED [7:7] | TRANSMIT_UNDER_RUN123 [6:6] | TRANSMIT_COMPLETE123 [5:5] | AMBA_ERROR123 [4:4] | TRANSMIT_GO [3:3] | RETRY_LIMIT_EXCEEDED [2:2] | COLLISION_OCCURRED [1:1] | USED_BIT_READ [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:9] | | | | | | | RESP_NOT_OK123 [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | USED_BIT_READ | RW1C | RW1S | 0 | Used bit read - set when a transmit buffer descriptor is read with its used bit set. Cleared by writing a one to this bit. |
| 1 | COLLISION_OCCURRED | RW1C | RW1S | 0 | Collision occurred - set by the assertion of collision. Cleared by writing a one to this bit. When operating in 10/100 mode, this status indicates either a collision or a late collision. In gigabit mode, this status is not set for a late collision. |
| 2 | RETRY_LIMIT_EXCEEDED | RW1C | RW1S | 0 | Retry limit exceeded - cleared by writing a one to this bit. |
| 3 | TRANSMIT_GO | R | W | 0 | Transmit go - if high transmit is active. When using the exposed FIFO interface, this bit represents bit 3 of the network control register. When using the DMA interface this bit represents the tx_go variable as specified in the transmit buffer description. |
| 4 | AMBA_ERROR123 | RW1C | RW1S | 0 | Transmit frame corruption due to AMBA (AXI) errors. Set if an error occurs whilst midway through reading transmit frame from external memory including RRESP or BRESP errors and buffers exhausted mid frame (if the buffers run out during transmission of a frame then transmission stops, FCS shall be bad and tx_er asserted). Also set in DMA packet buffer mode if single frame is too large for configured packet buffer memory size. Cleared by writing a one to this bit. |
| 5 | TRANSMIT_COMPLETE123 | RW1C | RW1S | 0 | Transmit complete - set when a frame has been transmitted. Cleared by writing a one to this bit. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 6 | TRANSMIT_UNDER_RUN123 | RW1C | RW1S | 0 | Transmit under run - this bit is set if the transmitter was forced to terminate a frame that it had already began transmitting due to further data being unavailable. This bit is set if a transmitter status write back has not completed when another status write back is attempted. When using the DMA interface configured for packet buffer mode, this bit will never be set. Cleared by writing a 1. |
| 7 | LATE_COLLISION_OCCURRED | RW1C | RW1S | 0 | Late collision occurred - only set if the condition occurs in gigabit mode, as retry is not attempted. Cleared by writing a one to this bit. |
| 8 | RESP_NOT_OK123 | RW1C | RW1S | 0 | bresp/hresp not OK - set when the DMA block sees bresp/hresp not OK. Cleared by writing a one to this bit. |

### 11.3.9 ETH_RECEIVE_Q_PTR

**Description:** This register holds the start address of the receive buffer queue (receive buffers descriptor list). The receive buffer queue base address must be initialized before receive is enabled through bit 2 of the network control register. Once reception is enabled, any write to the receive buffer queue base address register is ignored. Reading this register returns the location of the descriptor currently being accessed. This value increments as buffers are used. Software should not use this register for determining where to remove received frames from the queue as it constantly changes as new frames are received. Software should instead work its way through the buffer descriptor queue checking the used bits. In terms of AMBA (AXI) operation, the receive descriptors are read from memory using a single 32bit AXI access. When the datapath is configured at 64bit, the receive descriptors should be aligned at 64-bit boundaries and each pair of 32-bit descriptors is written to using a single 64bit AXI access.

**Address:** 0x40481018
**Offset:** 0x1018
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DMA_RX_Q_PTR [7:2] | | | | | | None [1:1] | DMA_RX_DIS_Q [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | DMA_RX_Q_PTR [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | DMA_RX_Q_PTR [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | DMA_RX_Q_PTR [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | DMA_RX_DIS_Q | RW | R | 0 | Disable queue if set to 1. This can be used to reduce the number of active queues and should only be changed while receive is not enabled. |
| 2:31 | DMA_RX_Q_PTR | RW | R | 0 | Receive buffer queue base address - written with the address of the start of the receive queue. |

### 11.3.10 ETH_TRANSMIT_Q_PTR

**Description:** This register holds the start address of the transmit buffer queue (transmit buffers descriptor list). The transmit buffer queue base address register must be initialized before transmit is started through bit 9 of the network control register. Once transmission has started, any write to the transmit buffer queue base address register is illegal and therefore ignored. Note that due to clock boundary synchronization, it takes a maximum of four pclk cycles from the writing of the transmit start bit before the transmitter is active. Writing to the transmit buffer queue base address register during this time may produce unpredictable results. Reading this register returns the location of the descriptor currently being accessed. Because the DMA can store data for multiple frames at once, this may not necessarily be pointing to the current frame being transmitted. In terms of AMBA AXI operation, the transmit descriptors are written to memory using a single 32bit AHB access. When the datapath is configured as 64bit, the transmit descriptors should be aligned at 64-bit boundaries and each pair of 32-bit descriptors is read from memory using a single AXI access.

**Address:** 0x4048101C
**Offset:** 0x101C
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DMA_TX_Q_PTR [7:2] | | | | | | None [1:1] | DMA_TX_DIS_Q [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | DMA_TX_Q_PTR [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | DMA_TX_Q_PTR [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | DMA_TX_Q_PTR [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | DMA_TX_DIS_Q | RW | R | 0 | Disable queue if set to 1. This can be used to reduce the number of active queues and should only be changed while transmit is not enabled. |
| 2:31 | DMA_TX_Q_PTR | RW | R | 0 | Transmit buffer queue base address - written with the address of the start of the transmit queue. |

### 11.3.11 ETH_RECEIVE_STATUS

**Description:** This register, when read provides details of the status of a receive. Once read, individual bits may be cleared by writing 1 to them. It is not possible to set a bit to 1 by writing to the register.
**Address:** 0x40481020
**Offset:** 0x1020
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:4] | | | | RESP_NOT_OK1234 [3:3] | RECEIVE_OVERRUN123 [2:2] | FRAME_RECEIVED [1:1] | BUFFER_NOT_AVAILABLE [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | BUFFER_NOT_AVAILABLE | RW1C | RW1S | 0 | Buffer not available - an attempt was made to get a new buffer and the pointer indicated that it was owned by the processor. The DMA will reread the pointer each time an end of frame is received until a valid pointer is found. This bit is set following each descriptor read attempt that fails, even if consecutive pointers are unsuccessful and software has in the mean time cleared the status flag. Cleared by writing a one to this bit. |
| 1 | FRAME_RECEIVED | RW1C | RW1S | 0 | Frame received - one or more frames have been received and placed in memory. Cleared by writing a one to this bit. |
| 2 | RECEIVE_OVERRUN123 | RW1C | RW1S | 0 | Receive overrun - this bit is set if either the gem_dma RX FIFO or external RX FIFO were unable to store the receive frame due to a FIFO overflow, or if the receive status, reported by the gem_rx module to the gem_dma was not taken at end of frame. This bit is also set in DMA packet buffer mode if the packet buffer overflows. For DMA operation the buffer will be recovered if an overrun occurs. This bit is cleared by writing a one to it. |
| 3 | RESP_NOT_OK1234 | RW1C | RW1S | 0 | bresp not OK - set when the DMA block sees bresp/hresp not OK. Cleared by writing a one to this bit. |

### 11.3.12 ETH_INT_STATUS

**Description:** If not configured for priority queueing, the GEM generates a single interrupt. This register indicates the source of this interrupt. The corresponding bit in the mask register must be clear for a bit to be set. If any bit is set in this register the ethernet_int signal will be asserted. For test purposes each bit can be set or reset by writing to the interrupt mask register. The default configuration is shown below whereby all bits are reset to zero on read. Changing the validity of the `gem_irq_read_clear define will instead require a one to be written to the appropriate bit in order to clear it. In this mode reading has no affect on the status of the bit.

**Address:** 0x40481024
**Offset:** 0x1024
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | TRANSMIT_COMPLETE [7:7] | AMBA_ERROR [6:6] | RETRY_LIMIT_EXCEEDED_OR_LATE_COLLISION [5:5] | TRANSMIT_UNDER_RUN [4:4] | TX_USED_BIT_READ [3:3] | RX_USED_BIT_READ [2:2] | RECEIVE_COMPLETE [1:1] | MANAGEMENT_FRAME_SENT [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_15 [15:15] | PAUSE_FRAME_TRANSMITTED [14:14] | PAUSE_TIME_ELAPSED [13:13] | PAUSE_FRAME_WITH_NON_ZERO_PAUSE_QUANTUM_RECEIVED [12:12] | RESP_NOT_OK [11:11] | RECEIVE_OVERRUN [10:10] | REMOVED_9 [9:9] | None [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | PTP_PDELAY_RESP_FRAME_RECEIVED [23:23] | PTP_PDELAY_REQ_FRAME_RECEIVED [22:22] | PTP_SYNC_FRAME_TRANSMITTED [21:21] | PTP_DELAY_REQ_FRAME_TRANSMITTED [20:20] | PTP_SYNC_FRAME_RECEIVED [19:19] | PTP_DELAY_REQ_FRAME_RECEIVED [18:18] | REMOVED_17 [17:17] | REMOVED_16 [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:30] | | TSU_TIMER_COMPARISON_INTERRUPT [29:29] | REMOVED_28 [28:28] | RECEIVE_LPI_INDICATION_STATUS_BIT_CHANGE [27:27] | TSU_SECONDS_REGISTER_INCREMENT [26:26] | PTP_PDELAY_RESP_FRAME_TRANSMITTED [25:25] | PTP_PDELAY_REQ_FRAME_TRANSMITTED [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | MANAGEMENT_FRAME_SENT | RW1C | RW1S | 0 | Management frame sent - the PHY maintenance register has completed its operation. |
| 1 | RECEIVE_COMPLETE | RW1C | RW1S | 0 | Receive complete - a frame has been stored in memory. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 2 | RX_USED_BIT_READ | RW1C | RW1S | 0 | RX used bit read - set when a receive buffer descriptor is read with its used bit set. |
| 3 | TX_USED_BIT_READ | RW1C | RW1S | 0 | TX used bit read - set when a transmit buffer descriptor is read with its used bit set. |
| 4 | TRANSMIT_UNDER_RUN | RW1C | RW1S | 0 | Transmit under run - this interrupt is set if the transmitter was forced to terminate a frame that it has already began transmitting due to further data being unavailable. If an under run occurs, the transmitter will force bad crc and tx_er high. This interrupt is set if a transmitter status write back has not completed when another status write back is attempted. When using the DMA interface configured for internal FIFO mode, this interrupt is also set when the transmit DMA has written the SOP data into the FIFO and either the AHB bus was not granted in time for further data, or because an AHB/AXI error response was returned by the connected slave, or because a used bit was read. When using the DMA interface configured for packet buffer mode, this bit will never be set. When using the external FIFO interface, this interrupt is also set when the tx_r_underflow input was asserted during a frame transfer. |
| 5 | RETRY_LIMIT_EXCEEDED_OR_LATE_COLLISION | RW1C | RW1S | 0 | Retry limit exceeded or late collision - transmit error. Late collision will only cause this status bit to be set in gigabit mode (as a retry is not attempted). |
| 6 | AMBA_ERROR | RW1C | RW1S | 0 | Transmit frame corruption due to AMBA (AXI) error. Set if an error occurs whilst midway through reading transmit frame from external system memory, including RRESP or BRESP(AXI) errors and buffers exhausted mid frame (if the buffers run out during transmission of a frame then transmission stops, FCS shall be bad and tx_er asserted). Also set in DMA packet buffer mode if single frame is too large for configured packet buffer memory size. |
| 7 | TRANSMIT_COMPLETE | RW1C | RW1S | 0 | Transmit complete - set when a frame has been transmitted. |
| 9 | REMOVED_9 | R | R | 0 | Write ignore, read 0 |
| 10 | RECEIVE_OVERRUN | RW1C | RW1S | 0 | Receive overrun - set when the receive overrun status bit gets set. |
| 11 | RESP_NOT_OK | RW1C | RW1S | 0 | bresp not OK - set when the DMA block sees bresp not OK. |
| 12 | PAUSE_FRAME_WITH_NON_ZERO_PAUSE_QUANTUM_RECEIVED | RW1C | RW1S | 0 | Pause frame with non-zero pause quantum received - indicates a valid pause has been received that has a non-zero pause quantum field. |
| 13 | PAUSE_TIME_ELAPSED | RW1C | RW1S | 0 | Pause Time elapsed. set when either the pause time register at address 0x38 decrements to zero, or when a valid pause frame is received with a zero pause quantum field. |
| 14 | PAUSE_FRAME_TRANSMITTED | RW1C | RW1S | 0 | Pause frame transmitted - indicates a pause frame has been successfully transmitted after being initiated from the network control register or from the tx_pause control pin. |
| 15 | REMOVED_15 | R | R | 0 | Write ignore, read 0 |
| 16 | REMOVED_16 | R | R | 0 | Write ignore, read 0 |
| 17 | REMOVED_17 | R | R | 0 | Write ignore, read 0 |
| 18 | PTP_DELAY_REQ_FRAME_RECEIVED | RW1C | RW1S | 0 | PTP delay_req frame received indicates a PTP delay_req frame has been received. |
| 19 | PTP_SYNC_FRAME_RECEIVED | RW1C | RW1S | 0 | PTP sync frame received indicates a PTP sync frame has been received. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 20 | PTP_DELAY_REQ _FRAME_TRANSMITTED | RW1C | RW1S | 0 | PTP delay_req frame transmitted indicates a PTP delay_req frame has been transmitted. |
| 21 | PTP_SYNC_FRAME _TRANSMITTED | RW1C | RW1S | 0 | PTP sync frame transmitted indicates a PTP sync frame has been transmitted. |
| 22 | PTP_PDELAY_REQ _FRAME_RECEIVED | RW1C | RW1S | 0 | PTP pdelay_req frame received indicates a PTP pdelay_req frame has been received. |
| 23 | PTP_PDELAY_RESP _FRAME_RECEIVED | RW1C | RW1S | 0 | PTP pdelay_resp frame received indicates a PTP pdelay_resp frame has been received. |
| 24 | PTP_PDELAY_REQ _FRAME_TRANSMITTED | RW1C | RW1S | 0 | PTP pdelay_req frame transmitted indicates a PTP pdelay_req frame has been transmitted. |
| 25 | PTP_PDELAY_RESP _FRAME_TRANSMITTED | RW1C | RW1S | 0 | PTP pdelay_resp frame transmitted indicates a PTP pdelay_resp frame has been transmitted. |
| 26 | TSU_SECONDS _REGISTER_INCREMEN T | RW1C | RW1S | 0 | TSU seconds register increment indicates the register has incremented. |
| 27 | RECEIVE_LPI_INDICAT ION_STATUS_BIT _CHANGE | RW1C | RW1S | 0 | Receive LPI indication status bit change |
| 28 | REMOVED_28 | R | R | 0 | Write ignore, read 0 |
| 29 | TSU_TIMER _COMPARISON _INTERRUPT | RW1C | RW1S | 0 | TSU timer comparison interrupt. Indicates when TSU timer count value is equal to programmed value. |

### 11.3.13 ETH_INT_ENABLE

**Description:** At reset all interrupts are disabled. Writing a one to the relevant bit location enables the required interrupt. This register is write only and when read will return zero.
**Address:** 0x40481028
**Offset:** 0x1028
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | ENABLE_TRANSMIT_COMPLETE_INTERRUPT [7:7] | ENABLE_TRANSMIT_FRAME_CORRUPTION_DUE_TO_AMBA_ERROR_INTERRUPT [6:6] | ENABLE_RETRY_LIMIT_EXCEEDED_OR_LATE_COLLISION_INTERRUPT [5:5] | ENABLE_TRANSMIT_BUFFER_UNDER_RUN_INTERRUPT [4:4] | ENABLE_TRANSMIT_USED_BIT_READ_INTERRUPT [3:3] | ENABLE_RECEIVE_USED_BIT_READ_INTERRUPT [2:2] | ENABLE_RECEIVE_COMPLETE_INTERRUPT [1:1] | ENABLE_MANAGEMENT_DONE_INTERRUPT [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | UNUSED_15 [15:15] | ENABLE_PAUSE_FRAME_TRANSMITTED_INTERRUPT [14:14] | ENABLE_PAUSE_TIME_ZERO_INTERRUPT [13:13] | ENABLE_PAUSE_FRAME_WITH_NON_ZERO_PAUSE_QUANTUM_INTERRUPT [12:12] | ENABLE_RESP_NOT_OK_INTERRUPT [11:11] | ENABLE_RECEIVE_OVERRUN_INTERRUPT [10:10] | UNUSED_9 [9:9] | UNUSED_8 [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | ENABLE_PTP_PDELAY_RESP_FRAME_RECEIVED [23:23] | ENABLE_PTP_PDELAY_REQ_FRAME_RECEIVED [22:22] | ENABLE_PTP_SYNC_FRAME_TRANSMITTED [21:21] | ENABLE_PTP_DELAY_REQ_FRAME_TRANSMITTED [20:20] | ENABLE_PTP_SYNC_FRAME_RECEIVED [19:19] | ENABLE_PTP_DELAY_REQ_FRAME_RECEIVED [18:18] | UNUSED_17 [17:17] | UNUSED_16 [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:30] | | ENABLE_TSU_TIMER_COMPARISON_INTERRUPT [29:29] | UNUSED_28 [28:28] | ENABLE_RX_LPI_INDICATION_INTERRUPT [27:27] | ENABLE_TSU_SECONDS_REGISTER_INCREMENT [26:26] | ENABLE_PTP_PDELAY_RESP_FRAME_TRANSMITTED [25:25] | ENABLE_PTP_PDELAY_REQ_FRAME_TRANSMITTED [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | ENABLE_MANAGEMENT_DONE_INTERRUPT | W | R | 0 | Enable management done interrupt |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 1 | ENABLE_RECEIVE_COMPLETE_INTERRUPT | W | R | 0 | Enable receive complete interrupt |
| 2 | ENABLE_RECEIVE_USED_BIT_READ_INTERRUPT | W | R | 0 | Enable receive used bit read interrupt |
| 3 | ENABLE_TRANSMIT_USED_BIT_READ_INTERRUPT | W | R | 0 | Enable transmit used bit read interrupt |
| 4 | ENABLE_TRANSMIT_BUFFER_UNDER_RUN_INTERRUPT | W | R | 0 | Enable transmit buffer under run interrupt |
| 5 | ENABLE_RETRY_LIMIT_EXCEEDED_OR_LATE_COLLISION_INTERRUPT | W | R | 0 | Enable retry limit exceeded or late collision interrupt |
| 6 | ENABLE_TRANSMIT_FRAME_CORRUPTION_DUE_TO_AMBA_ERROR_INTERRUPT | W | R | 0 | Enable transmit frame corruption due to AMBA (AXI) error interrupt |
| 7 | ENABLE_TRANSMIT_COMPLETE_INTERRUPT | W | R | 0 | Enable transmit complete interrupt |
| 8 | UNUSED_8 | W | R | 0 | Not used |
| 9 | UNUSED_9 | W | R | 0 | Not used |
| 10 | ENABLE_RECEIVE_OVERRUN_INTERRUPT | W | R | 0 | Enable receive overrun interrupt |
| 11 | ENABLE_RESP_NOT_OK_INTERRUPT | W | R | 0 | Enable bresp not OK interrupt |
| 12 | ENABLE_PAUSE_FRAME_WITH_NON_ZERO_PAUSE_QUANTUM_INTERRUPT | W | R | 0 | Enable pause frame with non-zero pause quantum interrupt |
| 13 | ENABLE_PAUSE_TIME_ZERO_INTERRUPT | W | R | 0 | Enable pause time zero interrupt |
| 14 | ENABLE_PAUSE_FRAME_TRANSMITTED_INTERRUPT | W | R | 0 | Enable pause frame transmitted interrupt |
| 15 | UNUSED_15 | W | R | 0 | Not used |
| 16 | UNUSED_16 | W | R | 0 | Not used |
| 17 | UNUSED_17 | W | R | 0 | Not used |
| 18 | ENABLE_PTP_DELAY_REQ_FRAME_RECEIVED | W | R | 0 | Enable PTP delay_req frame received |
| 19 | ENABLE_PTP_SYNC_FRAME_RECEIVED | W | R | 0 | Enable PTP sync frame received |
| 20 | ENABLE_PTP_DELAY_REQ_FRAME_TRANSMITTED | W | R | 0 | Enable PTP delay_req frame transmitted |
| 21 | ENABLE_PTP_SYNC_FRAME_TRANSMITTED | W | R | 0 | Enable PTP sync frame transmitted |
| 22 | ENABLE_PTP_PDELAY_REQ_FRAME_RECEIVED | W | R | 0 | Enable PTP pdelay_req frame received |
| 23 | ENABLE_PTP_PDELAY_RESP_FRAME_RECEIVED | W | R | 0 | Enable PTP pdelay_resp frame received |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 24 | ENABLE_PTP_PDELAY_REQ_FRAME_TRANSMITTED | W | R | 0 | Enable PTP pdelay_req frame transmitted |
| 25 | ENABLE_PTP_PDELAY_RESP_FRAME_TRANSMITTED | W | R | 0 | Enable PTP pdelay_resp frame transmitted |
| 26 | ENABLE_TSU_SECONDS_REGISTER_INCREMENT | W | R | 0 | Enable TSU seconds register increment |
| 27 | ENABLE_RX_LPI_INDICATION_INTERRUPT | W | R | 0 | Enable RX LPI indication interrupt |
| 28 | UNUSED_28 | W | R | 0 | Not used |
| 29 | ENABLE_TSU_TIMER_COMPARISON_INTERRUPT | W | R | 0 | Enable TSU timer comparison interrupt. |

### 11.3.14 ETH_INT_DISABLE

**Description:** Writing a 1 to the relevant bit location disables that particular interrupt. This register is write only and when read will return zero.
**Address:** 0x4048102C
**Offset:** 0x102C
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DISABLE_TRANSMIT_COMPLETE_INTERRUPT [7:7] | DISABLE_TRANSMIT_FRAME_CORRUPTION_DUE_TO_AMBA_ERROR_INTERRUPT [6:6] | DISABLE_RETRY_LIMIT_EXCEEDED_OR_LATE_COLLISION_INTERRUPT [5:5] | DISABLE_TRANSMIT_BUFFER_UNDER_RUN_INTERRUPT [4:4] | DISABLE_TRANSMIT_USED_BIT_READ_INTERRUPT [3:3] | DISABLE_RECEIVE_USED_BIT_READ_INTERRUPT [2:2] | DISABLE_RECEIVE_COMPLETE_INTERRUPT [1:1] | DISABLE_MANAGEMENT_DONE_INTERRUPT [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | UNUSED_15 [15:15] | DISABLE_PAUSE_FRAME_TRANSMITTED_INTERRUPT [14:14] | DISABLE_PAUSE_TIME_ZERO_INTERRUPT [13:13] | DISABLE_PAUSE_FRAME_WITH_NON_ZERO_PAUSE_QUANTUM_INTERRUPT [12:12] | DISABLE_RESP_NOT_OK_INTERRUPT [11:11] | DISABLE_RECEIVE_OVERRUN_INTERRUPT [10:10] | UNUSED_9 [9:9] | UNUSED_8 [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | DISABLE_PTP_PDELAY_RESP_FRAME_RECEIVED [23:23] | DISABLE_PTP_PDELAY_REQ_FRAME_RECEIVED [22:22] | DISABLE_PTP_SYNC_FRAME_TRANSMITTED [21:21] | DISABLE_PTP_DELAY_REQ_FRAME_TRANSMITTED [20:20] | DISABLE_PTP_SYNC_FRAME_RECEIVED [19:19] | DISABLE_PTP_DELAY_REQ_FRAME_RECEIVED [18:18] | UNUSED_17 [17:17] | UNUSED_16 [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_31 [31:31] | RESERVED_30_30 [30:30] | DISABLE_TSU_TIMER_COMPARISON_INTERRUPT [29:29] | UNUSED_28 [28:28] | DISABLE_RX_LPI_INDICATION_INTERRUPT [27:27] | DISABLE_TSU_SECONDS_REGISTER_INCREMENT [26:26] | DISABLE_PTP_PDELAY_RESP_FRAME_TRANSMITTED [25:25] | DISABLE_PTP_PDELAY_REQ_FRAME_TRANSMITTED [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | DISABLE_MANAGEMENT_DONE_INTERRUPT | W | R | 0 | 'Disable management done interrupt' |
| 1 | DISABLE_RECEIVE_COMPLETE_INTERRUPT | W | R | 0 | 'Disable receive complete interrupt' |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 2 | DISABLE_RECEIVE_USED_BIT_READ_INTERRUPT | W | R | 0 | 'Disable receive used bit read interrupt' |
| 3 | DISABLE_TRANSMIT_USED_BIT_READ_INTERRUPT | W | R | 0 | 'Disable transmit used bit read interrupt' |
| 4 | DISABLE_TRANSMIT_BUFFER_UNDER_RUN_INTERRUPT | W | R | 0 | 'Disable transmit buffer under run interrupt' |
| 5 | DISABLE_RETRY_LIMIT_EXCEEDED_OR_LATE_COLLISION_INTERRUPT | W | R | 0 | 'Disable retry limit exceeded or late collision interrupt' |
| 6 | DISABLE_TRANSMIT_FRAME_CORRUPTION_DUE_TO_AMBA_ERROR_INTERRUPT | W | R | 0 | 'Disable transmit frame corruption due to AMBA (AHB/AXI) error interrupt' |
| 7 | DISABLE_TRANSMIT_COMPLETE_INTERRUPT | W | R | 0 | 'Disable transmit complete interrupt' |
| 8 | UNUSED_8 | W | R | 0 | Not used |
| 9 | UNUSED_9 | W | R | 0 | Not used |
| 10 | DISABLE_RECEIVE_OVERRUN_INTERRUPT | W | R | 0 | 'Disable receive overrun interrupt' |
| 11 | DISABLE_RESP_NOT_OK_INTERRUPT | W | R | 0 | 'Disable bresp/hresp not OK interrupt' |
| 12 | DISABLE_PAUSE_FRAME_WITH_NON_ZERO_PAUSE_QUANTUM_INTERRUPT | W | R | 0 | 'Disable pause frame with non-zero pause quantum interrupt' |
| 13 | DISABLE_PAUSE_TIME_ZERO_INTERRUPT | W | R | 0 | 'Disable pause time zero interrupt' |
| 14 | DISABLE_PAUSE_FRAME_TRANSMITTED_INTERRUPT | W | R | 0 | 'Disable pause frame transmitted interrupt' |
| 15 | UNUSED_15 | W | R | 0 | Not used |
| 16 | UNUSED_16 | W | R | 0 | Not used |
| 17 | UNUSED_17 | W | R | 0 | Not used |
| 18 | DISABLE_PTP_DELAY_REQ_FRAME_RECEIVED | W | R | 0 | 'Disable PTP delay_req frame received' |
| 19 | DISABLE_PTP_SYNC_FRAME_RECEIVED | W | R | 0 | 'Disable PTP sync frame received' |
| 20 | DISABLE_PTP_DELAY_REQ_FRAME_TRANSMITTED | W | R | 0 | 'Disable PTP delay_req frame transmitted ' |
| 21 | DISABLE_PTP_SYNC_FRAME_TRANSMITTED | W | R | 0 | 'Disable PTP sync frame transmitted ' |
| 22 | DISABLE_PTP_PDELAY_REQ_FRAME_RECEIVED | W | R | 0 | 'Disable PTP pdelay_req frame received' |
| 23 | DISABLE_PTP_PDELAY_RESP_FRAME_RECEIVED | W | R | 0 | 'Disable PTP pdelay_resp frame received' |
| 24 | DISABLE_PTP_PDELAY_REQ_FRAME_TRANSMITTED | W | R | 0 | 'Disable PTP pdelay_req frame transmitted' |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 25 | DISABLE_PTP_PDELAY_RESP_FRAME_TRANSMITTED | W | R | 0 | 'Disable PTP pdelay_resp frame transmitted' |
| 26 | DISABLE_TSU_SECONDS_REGISTER_INCREMENT | W | R | 0 | 'Disable TSU seconds register increment' |
| 27 | DISABLE_RX_LPI_INDICATION_INTERRUPT | W | R | 0 | 'Disable RX LPI indication interrupt' |
| 28 | UNUSED_28 | W | R | 0 | Not used |
| 29 | DISABLE_TSU_TIMER_COMPARISON_INTERRUPT | W | R | 0 | 'Disable TSU timer comparison interrupt.' |
| 30 | RESERVED_30_30 | R | R | 0 | 'Reserved, read as 0, ignored on write.' |
| 31 | RESERVED_31_31 | R | R | 0 | 'Reserved, read as 0, ignored on write.' |

### 11.3.15 ETH_INT_MASK

**Description:** The interrupt mask register is a read only register indicating which interrupts are masked. All bits are set at reset and can be reset individually by writing to the interrupt enable register or set individually by writing to the interrupt disable register. Having separate address locations for enable and disable saves the need for performing a read modify write when updating the interrupt mask register. For test purposes there is a write-only function to this register that allows the bits in the interrupt status register to be set or cleared, regardless of the state of the mask register.

**Address:** 0x40481030
**Offset:** 0x1030
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x3FFFFFFF

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | TRANSMIT_COMPLETE_INTERRUPT_MASK [7:7] | AMBA_ERROR_INTERRUPT_MASK [6:6] | RETRY_LIMIT_EXCEEDED_OR_LATE_COLLISION_MASK [5:5] | TRANSMIT_BUFFER_UNDER_RUN_INTERRUPT_MASK [4:4] | TRANSMIT_USED_BIT_READ_INTERRUPT_MASK [3:3] | RECEIVE_USED_BIT_READ_INTERRUPT_MASK [2:2] | RECEIVE_COMPLETE_INTERRUPT_MASK [1:1] | MANAGEMENT_DONE_INTERRUPT_MASK [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | UNUSED_15 [15:15] | PAUSE_FRAME_TRANSMITTED_INTERRUPT_MASK [14:14] | PAUSE_TIME_ZERO_INTERRUPT_MASK [13:13] | PAUSE_FRAME_WITH_NON_ZERO_PAUSE_QUANTUM_INTERRUPT_MASK [12:12] | RESP_NOT_OK_INTERRUPT_MASK [11:11] | RECEIVE_OVERRUN_INTERRUPT_MASK [10:10] | UNUSED_9 [9:9] | UNUSED_8 [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | PTP_PDELAY_RESP_FRAME_RECEIVED_MASK [23:23] | PTP_PDELAY_REQ_FRAME_RECEIVED_MASK [22:22] | PTP_SYNC_FRAME_TRANSMITTED_MASK [21:21] | PTP_DELAY_REQ_FRAME_TRANSMITTED_MASK [20:20] | PTP_SYNC_FRAME_RECEIVED_MASK [19:19] | PTP_DELAY_REQ_FRAME_RECEIVED_MASK [18:18] | UNUSED_17 [17:17] | UNUSED_16 [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:30] | | TSU_TIMER_COMPARISON_MASK [29:29] | UNUSED_28 [28:28] | RX_LPI_INDICATION_MASK [27:27] | TSU_SECONDS_REGISTER_INCREMENT_MASK [26:26] | PTP_PDELAY_RESP_FRAME_TRANSMITTED_MASK [25:25] | PTP_PDELAY_REQ_FRAME_TRANSMITTED_MASK [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | MANAGEMENT_DONE_INTERRUPT_MASK | R | W | 1 | management done interrupt mask.<br>0: Interrupt is enabled.<br>1: Interrupt is disabled.<br>A write to this register directly affects the state of the corresponding bit in the interrupt status register, causing an interrupt to be generated if a 1 is written. |
| 1 | RECEIVE_COMPLETE_INTERRUPT_MASK | R | W | 1 | receive complete interrupt mask.<br>0: Interrupt is enabled.<br>1: Interrupt is disabled.<br>A write to this register directly affects the state of the corresponding bit in the interrupt status register, causing an interrupt to be generated if a 1 is written. |
| 2 | RECEIVE_USED_BIT_READ_INTERRUPT_MASK | R | W | 1 | receive used bit read interrupt mask.<br>0: Interrupt is enabled.<br>1: Interrupt is disabled.<br>A write to this register directly affects the state of the corresponding bit in the interrupt status register, causing an interrupt to be generated if a 1 is written. |
| 3 | TRANSMIT_USED_BIT_READ_INTERRUPT_MASK | R | W | 1 | transmit used bit read interrupt mask.<br>0: Interrupt is enabled.<br>1: Interrupt is disabled.<br>A write to this register directly affects the state of the corresponding bit in the interrupt status register, causing an interrupt to be generated if a 1 is written. |
| 4 | TRANSMIT_BUFFER_UNDER_RUN_INTERRUPT_MASK | R | W | 1 | transmit buffer under run interrupt mask.<br>0: Interrupt is enabled.<br>1: Interrupt is disabled.<br>A write to this register directly affects the state of the corresponding bit in the interrupt status register, causing an interrupt to be generated if a 1 is written. |
| 5 | RETRY_LIMIT_EXCEEDED_OR_LATE_COLLISION_MASK | R | W | 1 | A read of this register returns the value of the retry limit exceeded or late collision (gigabit mode only) interrupt mask.<br>0: Interrupt is enabled.<br>1: Interrupt is disabled.<br>A write to this register directly affects the state of the corresponding bit in the interrupt status register, causing an interrupt to be generated if a 1 is written. |
| 6 | AMBA_ERROR_INTERRUPT_MASK | R | W | 1 | transmit frame corruption due to AMBA (AXI) error interrupt mask.<br>0: Interrupt is enabled.<br>1: Interrupt is disabled.<br>A write to this register directly affects the state of the corresponding bit in the interrupt status register, causing an interrupt to be generated if a 1 is written. |
| 7 | TRANSMIT_COMPLETE_INTERRUPT_MASK | R | W | 1 | transmit complete interrupt mask.<br>0: Interrupt is enabled.<br>1: Interrupt is disabled.<br>A write to this register directly affects the state of the corresponding bit in the interrupt status register, causing an interrupt to be generated if a 1 is written. |
| 8 | UNUSED_8 | R | W | 1 | Not used |
| 9 | UNUSED_9 | R | W | 1 | Not used |
| 10 | RECEIVE_OVERRUN_INTERRUPT_MASK | R | W | 1 | receive overrun interrupt mask.<br>0: Interrupt is enabled.<br>1: Interrupt is disabled.<br>A write to this register directly affects the state of the corresponding bit in the interrupt status register, causing an interrupt to be generated if a 1 is written. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 11 | RESP_NOT_OK _INTERRUPT_MASK | R | W | 1 | bresp not OK interrupt mask.<br>0: Interrupt is enabled.<br>1: Interrupt is disabled.<br>A write to this register directly affects the state of the corresponding bit in the interrupt status register, causing an interrupt to be generated if a 1 is written. |
| 12 | PAUSE_FRAME_WITH _NON_ZERO_PAUSE _QUANTUM _INTERRUPT_MASK | R | W | 1 | pause frame with non-zero pause quantum interrupt mask.<br>0: Interrupt is enabled.<br>1: Interrupt is disabled.<br>A write to this register directly affects the state of the corresponding bit in the interrupt status register, causing an interrupt to be generated if a 1 is written. |
| 13 | PAUSE_TIME_ZERO _INTERRUPT_MASK | R | W | 1 | pause time zero interrupt mask.<br>0: Interrupt is enabled.<br>1: Interrupt is disabled.<br>A write to this register directly affects the state of the corresponding bit in the interrupt status register, causing an interrupt to be generated if a 1 is written. |
| 14 | PAUSE_FRAME _TRANSMITTED_INTER RUPT_MASK | R | W | 1 | pause frame transmitted interrupt mask.<br>0: Interrupt is enabled.<br>1: Interrupt is disabled.<br>A write to this register directly affects the state of the corresponding bit in the interrupt status register, causing an interrupt to be generated if a 1 is written. |
| 15 | UNUSED_15 | R | W | 1 | Not used |
| 16 | UNUSED_16 | R | W | 1 | Not used |
| 17 | UNUSED_17 | R | W | 1 | Not used |
| 18 | PTP_DELAY_REQ _FRAME_RECEIVED_ MASK | R | W | 1 | A read of this register returns the value of the PTP delay_req frame received mask.<br>0: Interrupt is enabled.<br>1: Interrupt is disabled.<br>A write to this register directly affects the state of the corresponding bit in the interrupt status register, causing an interrupt to be generated if a 1 is written. |
| 19 | PTP_SYNC_FRAME _RECEIVED_MASK | R | W | 1 | A read of this register returns the value of the PTP sync frame received mask.<br>0: Interrupt is enabled.<br>1: Interrupt is disabled.<br>A write to this register directly affects the state of the corresponding bit in the interrupt status register, causing an interrupt to be generated if a 1 is written. |
| 20 | PTP_DELAY_REQ _FRAME_TRANSMITTED _MASK | R | W | 1 | A read of this register returns the value of the PTP delay_req frame transmitted mask.<br>0: Interrupt is enabled.<br>1: Interrupt is disabled.<br>A write to this register directly affects the state of the corresponding bit in the interrupt status register, causing an interrupt to be generated if a 1 is written. |
| 21 | PTP_SYNC_FRAME _TRANSMITTED_MASK | R | W | 1 | A read of this register returns the value of the PTP sync frame transmitted mask.<br>0: Interrupt is enabled.<br>1: Interrupt is disabled.<br>A write to this register directly affects the state of the corresponding bit in the interrupt status register, causing an interrupt to be generated if a 1 is written. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 22 | PTP_PDELAY_REQ _FRAME_RECEIVED _MASK | R | W | 1 | A read of this register returns the value of the PTP pdelay_req frame received mask.<br>0: Interrupt is enabled.<br>1: Interrupt is disabled.<br>A write to this register directly affects the state of the corresponding bit in the interrupt status register, causing an interrupt to be generated if a 1 is written. |
| 23 | PTP_PDELAY_RESP _FRAME_RECEIVED _MASK | R | W | 1 | A read of this register returns the value of the PTP pdelay_resp frame received mask.<br>0: Interrupt is enabled.<br>1: Interrupt is disabled.<br>A write to this register directly affects the state of the corresponding bit in the interrupt status register, causing an interrupt to be generated if a 1 is written. |
| 24 | PTP_PDELAY_REQ _FRAME_TRANSMITTED _MASK | R | W | 1 | A read of this register returns the value of the PTP pdelay_req frame transmitted mask.<br>0: Interrupt is enabled.<br>1: Interrupt is disabled.<br>A write to this register directly affects the state of the corresponding bit in the interrupt status register, causing an interrupt to be generated if a 1 is written. |
| 25 | PTP_PDELAY_RESP _FRAME_TRANSMITTED _MASK | R | W | 1 | A read of this register returns the value of the PTP pdelay_resp frame transmitted mask.<br>0: Interrupt is enabled.<br>1: Interrupt is disabled.<br>A write to this register directly affects the state of the corresponding bit in the interrupt status register, causing an interrupt to be generated if a 1 is written. |
| 26 | TSU_SECONDS _REGISTER_INCREMEN T_MASK | R | W | 1 | A read of this register returns the value of the TSU seconds register increment mask.<br>0: Interrupt is enabled.<br>1: Interrupt is disabled.<br>A write to this register directly affects the state of the corresponding bit in the interrupt status register, causing an interrupt to be generated if a 1 is written. |
| 27 | RX_LPI_INDICATION_M ASK | R | W | 1 | A read of this register returns the value of the RX LPI indication mask.<br>0: Interrupt is enabled.<br>1: Interrupt is disabled.<br>A write to this register directly affects the state of the corresponding bit in the interrupt status register, causing an interrupt to be generated if a 1 is written |
| 28 | UNUSED_28 | R | W | 1 | unused |
| 29 | TSU_TIMER _COMPARISON_MASK | R | W | 1 | Enable TSU timer comparison interrupt mask. |

### 11.3.16 ETH_PHY_MANAGEMENT

**Description:** The PHY maintenance register is implemented as a shift register. Writing to the register starts a shift operation which is signalled as complete when bit-2 is set in the network status register. It takes about 2000 pclk cycles to complete, when MDC is set for pclk divide by 32 in the network configuration register. An interrupt is generated upon completion. During this time, the MSB of the register is output on the MDIO pin and the LSB updated from the MDIO pin with each MDC cycle. This causes transmission of a PHY management frame on MDIO. See Section 22.2.4.5 of the IEEE 802.3 standard. Reading during the shift operation will return the current contents of the shift register. At the end of management operation, the bits will have shifted back to their original locations. For a read operation, the data bits will be updated with data read from the PHY. It is important to write the correct values to the register to ensure a valid PHY management frame is produced. The MDIO interface can read IEEE 802.3 clause 45 PHYs as well as clause 22 PHYs. To read clause 45 PHYs, bit 30 should be written with a 0 rather than a 1. For a description of MDC generation, see Network Configuration Register.

**Address:** 0x40481034
**Offset:** 0x1034
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | PHY_WRITE_READ_DATA [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | PHY_WRITE_READ_DATA [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | PHY _ADDRESS [23:23] | REGISTER_ADDRESS [22:18] | | | | | WRITE10 [17:16] | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | WRITE0 [31:31] | WRITE1 [30:30] | OPERATION [29:28] | | PHY_ADDRESS [27:24] | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | PHY_WRITE_READ _DATA | RW | RW | 0 | For a write operation this is written with the data to be written to the PHY. After a read operation this contains the data read from the PHY. |
| 16:17 | WRITE10 | RW | R | 0 | Must be written with 10. |
| 18:22 | REGISTER_ADDRESS | RW | R | 0 | Register address - specifies the register in the PHY to access. |
| 23:27 | PHY_ADDRESS | RW | R | 0 | PHY address. |
| 28:29 | OPERATION | RW | R | 0 | Operation. For a Clause 45 frame: 00 is an addr, 01 is a write, 10 is a post read increment, 11 is a read frame. For a Clause 22 frame: 10 is a read, 01 is a write. |
| 30 | WRITE1 | RW | R | 0 | Must be written to 1 for a valid Clause 22 frame and to 0 for a valid Clause 45 frame. |
| 31 | WRITE0 | RW | R | 0 | Must be written with 0. |

### 11.3.17 ETH_PAUSE_TIME

**Description:** Received Pause Quantum Register
**Address:** 0x40481038
**Offset:** 0x1038
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | QUANTUM [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | QUANTUM [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | QUANTUM | R | W | 0 | Received pause quantum - stores the current value of the received pause quantum register which is decremented every 512 bit times. |

### 11.3.18 ETH_TX_PAUSE_QUANTUM

**Description:** Transmit Pause Quantum Register
**Address:** 0x4048103C
**Offset:** 0x103C
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xFFFFFFFF

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | QUANTUM [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | QUANTUM [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | QUANTUM_P1 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | QUANTUM_P1 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | QUANTUM | RW | R | 65535 | Transmit pause quantum - written with the pause quantum value for pause frame transmission. |
| 16:31 | QUANTUM_P1 | RW | R | 65535 | Transmit pause quantum - written with the pause quantum value for pause frame transmission of priority 1. |

### 11.3.19 ETH_PBUF_TXCUTTHRU

**Description:** Partial store and forward is only applicable when using the DMA configured in SRAM based packet buffer mode. It is also not available when using multi buffer frames. TX Partial Store and Forward
**Address:** 0x40481040
**Offset:** 0x1040
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x1FF

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DMA_TX_CUTTHRU_THRESHOLD [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:9] | | | | | | | DMA_TX_CUTTHRU_THRESHOLD [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | DMA_TX_CUTTHRU [31:31] | None [30:24] | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:8 | DMA_TX_CUTTHRU_THRESHOLD | RW | R | 511 | Watermark value. This value must be >= 0x9. The reset value depends on the value of the configuration option `gem_tx_pbuf_addr, which is defined in the verilog defs configuration file. The value chosen for the generation of the userguide was `gem_tx_pbuf_addr = 9 |
| 31 | DMA_TX_CUTTHRU | RW | R | 0 | Enable TX partial store and forward operation |

### 11.3.20 ETH_PBUF_RXCUTTHRU

**Description:** RX Partial Store and Forward
**Address:** 0x40481044
**Offset:** 0x1044
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xFF

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DMA_RX_CUTTHRU_THRESHOLD [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | DMA_RX_CUTTHRU [31:31] | None [30:24] | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | DMA_RX_CUTTHRU_THRESHOLD | RW | R | 255 | Watermark value. The reset value depends on the value of the configuration option `gem_rx_pbuf_addr, which is defined in the verilog defs configuration file. The value chosen for the generation of the userguide was `gem_rx_pbuf_addr = 8. |
| 31 | DMA_RX_CUTTHRU | RW | R | 0 | Enable RX partial store and forward operation |

### 11.3.21 ETH_JUMBO_MAX_LENGTH

**Description:** Maximum Jumbo Frame Size.
**Address:** 0x40481048
**Offset:** 0x1048
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x600

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | JUMBO_MAX_LENGTH [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:14] | | JUMBO_MAX_LENGTH [13:8] | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:13 | JUMBO_MAX_LENGTH | RW | R | 1536 | Maximum Jumbo Frame Size - resets to the gem_jumbo_max_length define value. |

### 11.3.22 ETH_EXTERNAL_FIFO_INTERFACE

**Description:** Not presents.
**Address:** 0x4048104C
**Offset:** 0x104C
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | REMOVED_31_0 | R | R | 0 | Write ignore, read 0 |

### 11.3.23 ETH_AXI_MAX_PIPELINE

**Description:** Used to set the maximum amount of outstanding transactions on the AXI bus between AR / R channels and AW / W channels. Cannot be more than the depth of the configured AXI pipeline FIFO (defined in verilog defs.v)
**Address:** 0x40481054
**Offset:** 0x1054
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x101

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | AR2R_MAX_PIPELINE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | AW2W_MAX_PIPELINE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:17] | | | | | | | USE_AW2B_FILL [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | AR2R_MAX_PIPELINE | RW | R | 1 | Defines the maximum number of outstanding AXI read requests that can be issued by the DMA via the AR channel. |
| 8:15 | AW2W_MAX_PIPELINE | RW | R | 1 | Defines the maximum number of outstanding AXI write requests that can be issued by the DMA via the AW channel. |
| 16 | USE_AW2B_FILL | RW | R | 0 | For the write issuing capability as defined in bits 15:8 of this register, select whether the max number of transactions operates between the AW to W AXI channel or the AW to B channel. Set to 0 to operate between the AW and W channels. Set to 1 to operate between the AW and B channels. |

### 11.3.24 ETH_RSC_CONTROL

**Description:** Not presents. Access to the register will return AHB error.
**Address:** 0x40481058
**Offset:** 0x1058
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | REMOVED_31_0 | R | R | 0 | Write ignore, read 0 |

### 11.3.25 ETH_INT_MODERATION

**Description:** Used to moderate the number of transmit and receive complete interrupts issued. With interrupt moderation enabled receive and transmit interrupts are not generated immediately a frame is transmitted or received. Instead when a receive or transmit event occurs a timer is started and the interrupt is asserted after it times out. This limits the frequency with which the CPU receives interrupts. When interrupt moderation is enabled interrupt status bit one is always used for receive and bit 7 is always used for transmit even when priority queuing is enabled. With interrupt moderation 800ns periods are counted. GEM determines what constitutes an 800ns period by looking at the tbi (bit 11), gigabit bit (10) and speed (bit 0) bits in the network configuration register and counting tx_clk cycles. Bit 0 needs to be set to 1 for 100M operation.

**Address:** 0x4048105C
**Offset:** 0x105C
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | RX_INT_MODERATION [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | TX_INT_MODERATION [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | RX_INT_MODERATION | RW | R | 0 | Count of 800ns periods before bit 1 is set in the interrupt status register after a frame is received. A non-zero value indicates receive interrupt moderation will be performed. |
| 16:23 | TX_INT_MODERATION | RW | R | 0 | Count of 800ns periods before bit 7 is set in the interrupt status register after a frame is transmitted. A non-zero value indicates transmit interrupt moderation will be performed. |

### 11.3.26 ETH_SYS_WAKE_TIME

**Description:** Used to pause transmission after deassertion of tx_lpi_en. Each unit in this register corresponds to 64ns in gigabit mode, 320ns in 100M mode and 3200ns at 10M. After tx_lpi_en is deasserted transmission will pause for the set time.
**Address:** 0x40481060
**Offset:** 0x1060
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | SYS_WAKE_TIME [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | SYS_WAKE_TIME [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | SYS_WAKE_TIME | RW | R | 0 | Count of 64ns, 320ns or 3200ns intervals before transmission starts after deassertion of tx_lpi_en (each interval is equivalent to eight tx_clk periods and so varies with data rate). |

### 11.3.27 ETH_HASH_BOTTOM

**Description:** The unicast hash enable and the multicast hash enable bits in the network configuration register enable the reception of hash matched frames. Hash Register Bottom (31 to 0 bits)
**Address:** 0x40481080
**Offset:** 0x1080
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDRESS_HASH_B [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDRESS_HASH_B [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDRESS_HASH_B [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDRESS_HASH_B [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | ADDRESS_HASH_B | RW | R | 0 | The first 32 bits of the hash address register. |

### 11.3.28 ETH_HASH_TOP

**Description:** Hash Register Top (63 to 32 bits)
**Address:** 0x40481084
**Offset:** 0x1084
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDRESS_HASH_T [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDRESS_HASH_T [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDRESS_HASH_T [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDRESS_HASH_T [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | ADDRESS_HASH_T | RW | R | 0 | The remaining 32 bits of the hash address register. |

### 11.3.29 ETH_SPEC_ADD1_BOTTOM

**Description:** The addresses stored in the specific address registers are deactivated at reset or when their corresponding specific address register bottom is written. They are activated when specific address register top is written.
**Address:** 0x40481088
**Offset:** 0x1088
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDRESS_ADD1_B [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDRESS_ADD1_B [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDRESS_ADD1_B [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDRESS_ADD1_B [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | ADDRESS_ADD1_B | RW | R | 0 | 'Least significant 32 bits of the destination address, that is bits 31:0. Bit zero indicates whether the address is multicast or unicast and corresponds to the least significant bit of the first byte received.' |

### 11.3.30 ETH_SPEC_ADD1_TOP

**Description:** Specific Address Top
**Address:** 0x4048108C
**Offset:** 0x108C
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDRESS_TOP [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDRESS_TOP [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:17] | | | | | | | FILTER_TYPE [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | ADDRESS_TOP | RW | R | 0 | Specific address 1. The most significant bits of the destination/source address that is to be compared, that is bits 47:32. |
| 16 | FILTER_TYPE | RW | R | 0 | This control bit selects whether this filter should be comparing the MAC source address or the MAC destination address of the received Ethernet frame. When set to zero, the filter is a destination address filter. When set to one, the filter is a source address filter. Specific address 1. The most significant bits of the destination address, that is bits 47:32. |

### 11.3.31 ETH_SPEC_ADD2_BOTTOM

**Description:** The addresses stored in the specific address registers are deactivated at reset or when their corresponding specific address register bottom is written. They are activated when specific address register top is written.
**Address:** 0x40481090
**Offset:** 0x1090
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDRESS_BOTTOM [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDRESS_BOTTOM [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDRESS_BOTTOM [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDRESS_BOTTOM [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | ADDRESS_BOTTOM | RW | R | 0 | Least significant 32 bits of the destination address, that is bits 31:0. Bit zero indicates whether the address is multicast or unicast and corresponds to the least significant bit of the first byte received. |

### 11.3.32 ETH_SPEC_ADD2_TOP

**Description:** Specific Address Top
**Address:** 0x40481094
**Offset:** 0x1094
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDRESS_TOP [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDRESS_TOP [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:17] | | | | | | | FILTER_TYPE [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:30] | | FILTER_BYTE_MASK [29:24] | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | ADDRESS_TOP | RW | R | 0 | Specific address 1. The most significant bits of the destination/source address that is to be compared, that is bits 47:32. |
| 16 | FILTER_TYPE | RW | R | 0 | This control bit selects whether this filter should be comparing the MAC source address or the MAC destination address of the received Ethernet frame. When set to zero, the filter is a destination address filter. When set to one, the filter is a source address filter. Specific address 1. The most significant bits of the destination address, that is bits 47:32. |
| 24:29 | FILTER_BYTE_MASK | RW | R | 0 | When high, the associated byte of the specific address will not be compared. Bit 24 controls whether the first byte received should be compared. Bit 29 controls whether the last byte received should be compared. |

### 11.3.33 ETH_SPEC_ADD3_BOTTOM

**Description:** The addresses stored in the specific address registers are deactivated at reset or when their corresponding specific address register bottom is written. They are activated when specific address register top is written.
**Address:** 0x40481098
**Offset:** 0x1098
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDRESS_BOTTOM [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDRESS_BOTTOM [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDRESS_BOTTOM [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDRESS_BOTTOM [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | ADDRESS_BOTTOM | RW | R | 0 | Least significant 32 bits of the destination address, that is bits 31:0. Bit zero indicates whether the address is multicast or unicast and corresponds to the least significant bit of the first byte received. |

### 11.3.34 ETH_SPEC_ADD3_TOP

**Description:** Specific Address Top
**Address:** 0x4048109C
**Offset:** 0x109C
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDRESS_TOP [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDRESS_TOP [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:17] | | | | | | | FILTER_TYPE [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:30] | | FILTER_BYTE_MASK [29:24] | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | ADDRESS_TOP | RW | R | 0 | Specific address 1. The most significant bits of the destination/source address that is to be compared, that is bits 47:32. |
| 16 | FILTER_TYPE | RW | R | 0 | This control bit selects whether this filter should be comparing the MAC source address or the MAC destination address of the received Ethernet frame. When set to zero, the filter is a destination address filter. When set to one, the filter is a source address filter. Specific address 1. The most significant bits of the destination address, that is bits 47:32. |
| 24:29 | FILTER_BYTE_MASK | RW | R | 0 | When high, the associated byte of the specific address will not be compared. Bit 24 controls whether the first byte received should be compared. Bit 29 controls whether the last byte received should be compared. |

### 11.3.35 ETH_SPEC_ADD4_BOTTOM

**Description:** The addresses stored in the specific address registers are deactivated at reset or when their corresponding specific address register bottom is written. They are activated when specific address register top is written.
**Address:** 0x404810A0
**Offset:** 0x10A0
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDRESS_BOTTOM [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDRESS_BOTTOM [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDRESS_BOTTOM [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDRESS_BOTTOM [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | ADDRESS_BOTTOM | RW | R | 0 | Least significant 32 bits of the destination address, that is bits 31:0. Bit zero indicates whether the address is multicast or unicast and corresponds to the least significant bit of the first byte received. |

### 11.3.36 ETH_SPEC_ADD4_TOP

**Description:** Specific Address Top
**Address:** 0x404810A4
**Offset:** 0x10A4
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDRESS_TOP [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDRESS_TOP [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:17] | | | | | | | FILTER_TYPE [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:30] | | FILTER_BYTE_MASK [29:24] | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | ADDRESS_TOP | RW | R | 0 | Specific address 1. The most significant bits of the destination/source address that is to be compared, that is bits 47:32. |
| 16 | FILTER_TYPE | RW | R | 0 | This control bit selects whether this filter should be comparing the MAC source address or the MAC destination address of the received Ethernet frame. When set to zero, the filter is a destination address filter. When set to one, the filter is a source address filter. Specific address 1. The most significant bits of the destination address, that is bits 47:32. |
| 24:29 | FILTER_BYTE_MASK | RW | R | 0 | When high, the associated byte of the specific address will not be compared. Bit 24 controls whether the first byte received should be compared. Bit 29 controls whether the last byte received should be compared. |

### 11.3.37 ETH_SPEC_TYPE1

**Description:** Type ID Match 1
**Address:** 0x404810A8
**Offset:** 0x10A8
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | MATCH [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | MATCH [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | ENABLE_COPY [31:31] | None [30:24] | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | MATCH | RW | R | 0 | Type ID match 1. For use in comparisons with received frames type ID/length field. |
| 31 | ENABLE_COPY | RW | R | 0 | Enable copying of type ID match 1 matched frames. |

### 11.3.38 ETH_SPEC_TYPE2

**Description:** Type ID Match 2
**Address:** 0x404810AC
**Offset:** 0x10AC
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | MATCH [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | MATCH [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | ENABLE_COPY [31:31] | None [30:24] | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | MATCH | RW | R | 0 | Type ID match 2. For use in comparisons with received frames type ID/length field. |
| 31 | ENABLE_COPY | RW | R | 0 | Enable copying of type ID match 2 matched frames. |

### 11.3.39 ETH_SPEC_TYPE3

**Description:** Type ID Match 3
**Address:** 0x404810B0
**Offset:** 0x10B0
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | MATCH [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | MATCH [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | ENABLE_COPY [31:31] | None [30:24] | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | MATCH | RW | R | 0 | Type ID match 3. For use in comparisons with received frames type ID/length field. |
| 31 | ENABLE_COPY | RW | R | 0 | Enable copying of type ID match 3 matched frames. |

### 11.3.40 ETH_SPEC_TYPE4

**Description:** Type ID Match 4
**Address:** 0x404810B4
**Offset:** 0x10B4
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | MATCH [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | MATCH [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | ENABLE_COPY [31:31] | None [30:24] | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | MATCH | RW | R | 0 | Type ID match 4. For use in comparisons with received frames type ID/length field. |
| 31 | ENABLE_COPY | RW | R | 0 | Enable copying of type ID match 4 matched frames. |

### 11.3.41 ETH_WOL_REGISTER

**Description:** Wake on LAN Register. Presents in design, but feature is not supported.
**Address:** 0x404810B8
**Offset:** 0x10B8
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDR [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDR [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:20] | | | | WOL _MASK_3 [19:19] | WOL _MASK_2 [18:18] | WOL _MASK_1 [17:17] | WOL _MASK_0 [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | ADDR | RW | R | 0 | Wake on LAN ARP request IP address. Written to define the least significant 16 bits of the target IP address that is matched to generate a Wake on LAN event. A value of zero will not generate an event, even if this is matched by the received frame. |
| 16 | WOL_MASK_0 | RW | R | 0 | Wake on LAN magic packet event enable. When set magic packet events will cause the wol output to be asserted. |
| 17 | WOL_MASK_1 | RW | R | 0 | Wake on LAN ARP request event enable. When set ARP request events will cause the wol output to be asserted. |
| 18 | WOL_MASK_2 | RW | R | 0 | Wake on LAN specific address register 1 event enable. When set specific address 1 events will cause the wol output to be asserted. |
| 19 | WOL_MASK_3 | RW | R | 0 | Wake on LAN multicast hash event enable. When set multicast hash events will cause the wol output to be asserted. |

### 11.3.42 ETH_STRETCH_RATIO

**Description:** IPG stretch register
**Address:** 0x404810BC
**Offset:** 0x10BC
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | IPG_STRETCH [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | IPG_STRETCH [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | IPG_STRETCH | RW | R | 0 | IPG Stretch. Bits 7:0 are multiplied with the previously transmitted frame length (including preamble) bits 15:8 +1 divide the frame length. If the resulting number is greater than 96 and bit 28 is set in the network configuration register then the resulting number is used for the transmit inter-packet-gap. 1 is added to bits 15:8 to prevent a divide by zero. |

### 11.3.43 ETH_STACKED_VLAN

**Description:** Stacked VLAN Register
**Address:** 0x404810C0
**Offset:** 0x10C0
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | MATCH [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | MATCH [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | ENABLE_PROCESSING [31:31] | None [30:24] | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | MATCH | RW | R | 0 | User defined VLAN_TYPE field. When Stacked VLAN is enabled, the first VLAN tag in a received frame will only be accepted if the VLAN type field is equal to this user defined VLAN_TYPE OR equal to the standard VLAN type (0x8100). Note that the second VLAN tag of a Stacked VLAN packet will only be matched correctly if its VLAN_TYPE field equals 0x8100. |
| 31 | ENABLE_PROCESSING | RW | R | 0 | Enable stacked VLAN processing mode |

### 11.3.44 ETH_TX_PFC_PAUSE

**Description:** Transmit PFC Pause Register
**Address:** 0x404810C4
**Offset:** 0x10C4
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VECTOR_ENABLE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VECTOR [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | VECTOR_ENABLE | RW | R | 0 | Priority Vector Enable. If bit 17 of the network control register is written with a one then the priority enable vector of the PFC priority based pause frame will be set equal to the value stored in this register [7:0]. |
| 8:15 | VECTOR | RW | R | 0 | Priority Vector Pause Size. If bit 17 of the network control register is written with a one then for each entry equal to zero in the Transmit PFC Pause Register[15:8], the PFC pause frame's pause quantum field associated with that entry will be taken from the transmit pause quantum register. For each entry equal to one in the Transmit PFC Pause Register [15:8], the pause quantum associated with that entry will be zero. |

### 11.3.45 ETH_MASK_ADD1_BOTTOM

**Description:** Specific Address Mask 1 Bottom (31 to 0 bits)
**Address:** 0x404810C8
**Offset:** 0x10C8
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDRESS_MASK_BOTTOM [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDRESS_MASK_BOTTOM [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDRESS_MASK_BOTTOM [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDRESS_MASK_BOTTOM [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | ADDRESS_MASK_BOTTOM | RW | R | 0 | Specific Address Mask. Setting a bit to one masks the corresponding bit in the specific address 1 register (31 to 0 bits) |

### 11.3.46 ETH_MASK_ADD1_TOP

**Description:** Specific Address Mask 1 Top (47 to 32 bits)
**Address:** 0x404810CC
**Offset:** 0x10CC
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDRESS_MASK_TOP [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDRESS_MASK_TOP [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | ADDRESS_MASK_TOP | RW | R | 0 | Specific Address Mask. Setting a bit to one masks the corresponding bit in the specific address 1 register (47 to 32 bits). |

### 11.3.47 ETH_DMA_ADDR_OR_MASK

**Description:** Receive DMA Data Buffer Address Mask
**Address:** 0x404810D0
**Offset:** 0x10D0
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:4] | | | | MASK_ENABLE [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | MASK_VALUE_DA [31:28] | | | | None [27:24] | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | MASK_ENABLE | RW | R | 0 | Data Buffer Address Mask Enable. These bits are associated directly with bits[31:28].When bit 0 is set, the AXI address bit 28 used for accessing the receive data buffers will be forced to the value stored in bit 28 of this register. When bit 1 is set, the AXI address bit 29 used for accessing the receive data buffers will be forced to the value stored in bit 29 of this register. When bit 2 is set, the AXI address bit 30 used for accessing the receive data buffers will be forced to the value stored in bit 30 of this register. When bit 3 is set, the AXI address bit 31 used for accessing the receive data buffers will be forced to the value stored in bit 31 of this register. When these bits are clear, the associated value stored in bits 31:28 have no effect on the AXI address used for receive data buffer accesses. Any changes to this register will be ignored while the DMA is currently processing a receive packet. It will only affect the next full packet to be written to external memory. |
| 28:31 | MASK_VALUE_DA | RW | R | 0 | Data Buffer Address Mask Value. Values used to force bits 31:28 of the receive data buffer AHB address to a particular value when the associated enable bits stored in this register [3:0] are set. Any changes to this register will be ignored while the DMA is currently processing a receive packet. It will only affect the next full packet to be written to external system memory. |

### 11.3.48 ETH_RX_PTP_UNICAST

**Description:** PTP RX unicast IP destination address
**Address:** 0x404810D4
**Offset:** 0x10D4
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDRESS_UNICAST [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDRESS_UNICAST [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDRESS_UNICAST [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDRESS_UNICAST [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | ADDRESS_UNICAST | RW | R | 0 | Unicast IP destination address. Used for detection of PTP frames on receive path. |

### 11.3.49 ETH_TX_PTP_UNICAST

**Description:** PTP TX unicast IP destination address
**Address:** 0x404810D8
**Offset:** 0x10D8
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDRESS_UNICAST [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDRESS_UNICAST [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDRESS_UNICAST [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDRESS_UNICAST [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | ADDRESS_UNICAST | RW | R | 0 | Unicast IP destination address. Used for detection of PTP frames on transmit path. |

### 11.3.50 ETH_TSU_NSEC_CMP

**Description:** TSU timer comparison value nanoseconds
**Address:** 0x404810DC
**Offset:** 0x10DC
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARISON_NSEC [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARISON_NSEC [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:22] | | COMPARISON_NSEC [21:16] | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:21 | COMPARISON_NSEC | RW | R | 0 | TSU timer comparison value (ns). Value is compared to the bits[45:24] of the TSU timer count value (upper 22 bits of nanosecond value). |

### 11.3.51 ETH_TSU_SEC_CMP

**Description:** TSU timer comparison value seconds (31 to 0 bits)
**Address:** 0x404810E0
**Offset:** 0x10E0
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARISON_SEC [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARISON_SEC [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARISON_SEC [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARISON_SEC [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | COMPARISON_SEC | RW | R | 0 | TSU timer comparison value (s). Value is compared to seconds value bits [31:0] of the TSU timer count value. |

### 11.3.52 ETH_TSU_MSB_SEC_CMP

**Description:** TSU timer comparison value seconds (47 to 32 bits)
**Address:** 0x404810E4
**Offset:** 0x10E4
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARISON_MSB_SEC [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARISON_MSB_SEC [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | COMPARISON_MSB_SEC | RW | R | 0 | TSU timer comparison value (s). Value is compared to the top 16 bits (most significant 16-bits {47:32] of seconds value) of the TSU timer count value. |

### 11.3.53 ETH_TSU_PTP_TX_MSB_SEC

**Description:** PTP Event Frame Transmitted Seconds Register (47 to 32 bits)
**Address:** 0x404810E8
**Offset:** 0x10E8
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | TIMER_SECONDS [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | TIMER_SECONDS [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | TIMER_SECONDS | R | W | 0 | PTP Event Frame TX Seconds. The register is updated with the value that the 1588 timer seconds register held when the SFD of a PTP transmit primary event crosses the MII interface. The actual update occurs when the GEM recognizes the frame as a PTP sync or delay_req frame. An interrupt is issued when the register is updated. |

### 11.3.54 ETH_TSU_PTP_RX_MSB_SEC

**Description:** PTP Event Frame Received Seconds Register (47 to 32 bits)
**Address:** 0x404810EC
**Offset:** 0x10EC
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | TIMER_SECONDS [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | TIMER_SECONDS [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | TIMER_SECONDS | R | W | 0 | PTP Event Frame TX Seconds. The register is updated with the value that the 1588 timer seconds register held when the SFD of a PTP receive primary event crosses the MII interface. The actual update occurs when the GEM recognizes the frame as a PTP sync or delay_req frame. An interrupt is issued when the register is updated. |

### 11.3.55 ETH_TSU_PEER_TX_MSB_SEC

**Description:** PTP Peer Event Frame Transmitted Seconds Register (47 to 32 bits)
**Address:** 0x404810F0
**Offset:** 0x10F0
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | TIMER_SECONDS [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | TIMER_SECONDS [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | TIMER_SECONDS | R | W | 0 | PTP Peer Event Frame TX Seconds. The register is updated with the value that the 1588 timer seconds register held when the SFD of a PTP transmit peer event crosses the MII interface. The actual update occurs when the GEM recognizes the frame as a PTP pdelay_req or pdelay_resp frame. An interrupt is issued when the register is updated. |

### 11.3.56 ETH_TSU_PEER_RX_MSB_SEC

**Description:** PTP Peer Event Frame Received Seconds Register (47 to 32 bits)
**Address:** 0x404810F4
**Offset:** 0x10F4
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | TIMER_SECONDS [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | TIMER_SECONDS [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | TIMER_SECONDS | R | W | 0 | PTP Peer Event Frame RX Seconds. The register is updated with the value that the 1588 timer seconds register held when the SFD of a PTP receive peer event crosses the MII interface. The actual update occurs when the GEM recognizes the frame as a PTP pdelay_req or pdelay_resp frame. An interrupt is issued when the register is updated. |

### 11.3.57 ETH_DPRAM_FILL_DBG

**Description:** The fill levels for the TX & RX packet buffers can be read using this register, including the fill level for each queue in the TX direction.
**Address:** 0x404810F8
**Offset:** 0x10F8
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DMA_TX_Q_FILL_LEVEL_SELECT [7:4] | | | | None [3:1] | | | DMA_TX_RX_FILL_LEVEL_SELECT [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | DMA_TX_RX_FILL_LEVEL [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | DMA_TX_RX_FILL_LEVEL [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | DMA_TX_RX_FILL_LEVEL_SELECT | RW | R | 0 | TX/RX Fill Level select - report the fill level for the TX or RX packet buffer. |
| 4:7 | DMA_TX_Q_FILL_LEVEL_SELECT | RW | R | 0 | TX queue fill level select - select what TX queue to report fill levels for. |
| 16:31 | DMA_TX_RX_FILL_LEVEL | R | W | 0 | Fill Level - TX or RX packet buffer fill level, selected by the tx_q_fill_level_select and tx_rx_fill_level_select registers. Read this register to determine the fill level. |

### 11.3.58 ETH_REVISION_REG

**Description:** This register indicates a Cadence module identification number and module revision. The value of this register is read only as defined by `gem_revision_reg_value
**Address:** 0x404810FC
**Offset:** 0x10FC
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x70109

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | MODULE_REVISION [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | MODULE_REVISION [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | MODULE_IDENTIFICATION_NUMBER [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | FIX_NUMBER [31:28] | | | | MODULE_IDENTIFICATION_NUMBER [27:24] | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | MODULE_REVISION | R | W | 265 | Module revision - fixed value specific to the revision of the design which is incremented for each non-fix release of the IP. |
| 16:27 | MODULE_IDENTIFICATION_NUMBER | R | W | 7 | Module identification number - for the GEM, this value is fixed. |
| 28:31 | FIX_NUMBER | R | W | 0 | Fix number - incremented for fix releases. |

### 11.3.59 ETH_OCTETS_TXED_BOTTOM

**Description:** Octets Transmitted lower bits (31 to 0 bits)
**Address:** 0x40481100
**Offset:** 0x1100
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** These registers reset to zero on a read and stick at all ones when they count to their maximum value. They should be read frequently enough to prevent loss of data. In order to reduce overall design area, the statistics registers may be optionally removed in the configuration file if they are deemed unnecessary for a particular design. The receive statistics registers are only incremented when the receive enable bit is set in the network control register. The statistics registers optionally have a snapshot capability which, when exercised, will simultaneously store and clear the current values of all the statistics registers into a snapshot register set in order to allow a consistent set of statistics to be read by the processor. The snapshot is controlled using bit 13 of the network control register. The read snapshot control indicated by bit 14 of the network control register determines whether the processor reads the snapshot registers (logic 1) or the incrementing registers (logic 0). The default GEM configuration does not support the snapshot capability. See Parameterization section under Implementation Application Notes for an explanation of how to enable this function. All the statistics registers are read only. For test purposes they may be written by setting bit 7 (Write Enable) in the network control register. Setting bit 6 (increment statistics) in the network control register causes all the statistics registers to increment by one, again for test purposes. Once a statistics register has been read, it is automatically cleared. When reading the octets transmitted and octets received registers, bits 31:0 should be read prior to bits 47:32 to ensure reliable operation. The statistics register block contains the following registers. Octets Transmitted [31:0]
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_BOTTOM [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_BOTTOM [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_BOTTOM [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_BOTTOM [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | COUNT_BOTTOM | RC | W | 0 | Transmitted octets in frame without errors [31:0]. The number of octets transmitted in valid frames of any type. This counter is 48-bits, and is read through two registers. This count does not include octets from automatically generated pause frames. |

### 11.3.60 ETH_OCTETS_TXED_TOP

**Description:** Octets Transmitted higher bits (47 to 32 bits)
**Address:** 0x40481104
**Offset:** 0x1104
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_TOP [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_TOP [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | COUNT_TOP | RC | W | 0 | Transmitted octets in frame without errors [47:32]. The number of octets transmitted in valid frames of any type. This counter is 48-bits, and is read through two registers. This count does not include octets from automatically generated pause frames. |

### 11.3.61 ETH_FRAMES_TXED_OK

**Description:** Frames Transmitted
**Address:** 0x40481108
**Offset:** 0x1108
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_OK [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_OK [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_OK [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_OK [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | COUNT_OK | RC | W | 0 | Frames transmitted without error. A 32 bit register counting the number of frames successfully transmitted, i.e. no under run and not too many retries. Excludes pause frames. |

### 11.3.62 ETH_BROADCAST_TXED

**Description:** Broadcast Frames Transmitted
**Address:** 0x4048110C
**Offset:** 0x110C
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_BROADCAST [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_BROADCAST [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_BROADCAST [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_BROADCAST [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | COUNT_BROADCAST | RC | W | 0 | Broadcast frames transmitted without error. A 32 bit register counting the number of broadcast frames successfully transmitted without error, i.e. no under run and not too many retries. Excludes pause frames. |

### 11.3.63 ETH_MULTICAST_TXED

**Description:** Multicast Frames Transmitted
**Address:** 0x40481110
**Offset:** 0x1110
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_MULTICAST [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_MULTICAST [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_MULTICAST [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_MULTICAST [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | COUNT_MULTICAST | RC | W | 0 | Multicast frames transmitted without error. A 32 bit register counting the number of multicast frames successfully transmitted without error, i.e. no under run and not too many retries. Excludes pause frames. |

### 11.3.64 ETH_PAUSE_FRAMES_TXED

**Description:** Pause Frames Transmitted
**Address:** 0x40481114
**Offset:** 0x1114
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_PAUSE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_PAUSE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | COUNT_PAUSE | RC | W | 0 | Transmitted pause frames - a 16 bit register counting the number of pause frames transmitted. Only pause frames triggered by the register interface or through the external pause pins are counted as pause frames. Pause frames received through the external FIFO interface are counted in the frames transmitted counter. |

### 11.3.65 ETH_FRAMES_TXED_64

**Description:** 64 Byte Frames Transmitted
**Address:** 0x40481118
**Offset:** 0x1118
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_64 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_64 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_64 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_64 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | COUNT_64 | RC | W | 0 | 64 byte frames transmitted without error. A 32 bit register counting the number of 64 byte frames successfully transmitted without error, i.e. no under run and not too many retries. Excludes pause frames. |

### 11.3.66 ETH_FRAMES_TXED_65

**Description:** 65 to 127 Byte Frames Transmitted
**Address:** 0x4048111C
**Offset:** 0x111C
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_65 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_65 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_65 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_65 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | COUNT_65 | RC | W | 0 | 65 to127 byte frames transmitted without error. A 32 bit register counting the number of 65 to127 byte frames successfully transmitted without error, i.e. no under run and not too many retries. |

### 11.3.67 ETH_FRAMES_TXED_128

**Description:** 128 to 255 Byte Frames Transmitted
**Address:** 0x40481120
**Offset:** 0x1120
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_128 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_128 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_128 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_128 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | COUNT_128 | RC | W | 0 | 128 to 255 byte frames transmitted without error. A 32 bit register counting the number of 128 to 255 byte frames successfully transmitted without error, i.e. no under run and not too many retries. |

### 11.3.68 ETH_FRAMES_TXED_256

**Description:** 256 to 511 Byte Frames Transmitted
**Address:** 0x40481124
**Offset:** 0x1124
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_256 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_256 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_256 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_256 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | COUNT_256 | RC | W | 0 | 256 to 511 byte frames transmitted without error. A 32 bit register counting the number of 256 to 511 byte frames successfully transmitted without error, i.e. no under run and not too many retries. |

### 11.3.69 ETH_FRAMES_TXED_512

**Description:** 512 to 1023 Byte Frames Transmitted
**Address:** 0x40481128
**Offset:** 0x1128
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_512 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_512 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_512 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_512 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | COUNT_512 | RC | W | 0 | 512 to 1023 byte frames transmitted without error. A 32 bit register counting the number of 512 to 1023 byte frames successfully transmitted without error, i.e. no under run and not too many retries. |

### 11.3.70 ETH_FRAMES_TXED_1024

**Description:** 1024 to 1518 Byte Frames Transmitted
**Address:** 0x4048112C
**Offset:** 0x112C
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_1024 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_1024 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_1024 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_1024 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | COUNT_1024 | RC | W | 0 | 1024 to 1518 byte frames transmitted without error. A 32 bit register counting the number of 1024 to 1518 byte frames successfully transmitted without error, i.e. no under run and not too many retries. |

### 11.3.71 ETH_FRAMES_TXED_1519

**Description:** Greater Than 1518 Byte Frames Transmitted
**Address:** 0x40481130
**Offset:** 0x1130
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_1519 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_1519 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_1519 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_1519 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | COUNT_1519 | RC | W | 0 | Greater than 1518 byte frames transmitted without error. A 32 bit register counting the number of 1518 or above byte frames successfully transmitted without error, i.e. no under run and not too many retries. |

### 11.3.72 ETH_TX_UNDERRUNS

**Description:** Transmit Under Runs
**Address:** 0x40481134
**Offset:** 0x1134
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_UN [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:10] | | | | | | COUNT_UN [9:8] | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:9 | COUNT_UN | RC | W | 0 | Transmit under runs - a 10 bit register counting the number of frames not transmitted due to a transmit under run. If this register is incremented then no other statistics register is incremented. |

### 11.3.73 ETH_SINGLE_COLLISIONS

**Description:** Single Collision Frames. Presents in design but not support.
**Address:** 0x40481138
**Offset:** 0x1138
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT14 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT14 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:18] | | | | | | COUNT14 [17:16] | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:17 | COUNT14 | RC | W | 0 | Single collision frames - an 18 bit register counting the number of frames experiencing a single collision before being successfully transmitted, i.e. no under run. |

### 11.3.74 ETH_MULTIPLE_COLLISIONS

**Description:** Multiple Collision Frames. Presents in design but not support.
**Address:** 0x4048113C
**Offset:** 0x113C
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT15 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT15 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:18] | | | | | | COUNT15 [17:16] | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:17 | COUNT15 | RC | W | 0 | Multiple collision frames - an 18 bit register counting the number of frames experiencing between two and fifteen collisions prior to being successfully transmitted, i.e. no under run and not too many retries. |

### 11.3.75 ETH_EXCESSIVE_COLLISIONS

**Description:** Excessive Collisions. Presents in design but not support.
**Address:** 0x40481140
**Offset:** 0x1140
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT16 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:10] | | | | | | COUNT16 [9:8] | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:9 | COUNT16 | RC | W | 0 | Excessive collisions - a 10 bit register counting the number of frames that failed to be transmitted because they experienced 16 collisions. |

### 11.3.76 ETH_LATE_COLLISIONS

**Description:** Late Collisions. Presents in design but not support.
**Address:** 0x40481144
**Offset:** 0x1144
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT17 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:10] | | | | | | COUNT17 [9:8] | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:9 | COUNT17 | RC | W | 0 | Late collisions - a 10 bit register counting the number of late collision occurring after the slot time (512 bits) has expired. In 10/100 mode, late collisions are counted twice i.e. both as a collision and a late collision. In gigabit mode, a late collision causes the transmission to be aborted, thus the single and multi collision registers are not updated. |

### 11.3.77 ETH_DEFERRED_FRAMES

**Description:** Deferred Transmission Frames. Presents in design but not support.
**Address:** 0x40481148
**Offset:** 0x1148
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT18 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT18 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:18] | | | | | | COUNT18 [17:16] | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:17 | COUNT18 | RC | W | 0 | Deferred transmission frames - an 18 bit register counting the number of frames experiencing deferral due to carrier sense being active on their first attempt at transmission. Frames involved in any collision are not counted nor are frames that experienced a transmit under run. |

### 11.3.78 ETH_CRS_ERRORS

**Description:** Carrier Sense Errors. Presents in design but not support.
**Address:** 0x4048114C
**Offset:** 0x114C
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT19 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:10] | | | | | | COUNT19 [9:8] | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:9 | COUNT19 | RC | W | 0 | Carrier sense errors - a 10 bit register counting the number of frames transmitted where carrier sense was not seen during transmission or where carrier sense was deasserted after being asserted in a transmit frame without collision (no under run). Only incremented in half duplex mode. The only effect of a carrier sense error is to increment this register. The behaviour of the other statistics registers is unaffected by the detection of a carrier sense error. |

### 11.3.79 ETH_OCTETS_RXED_BOTTOM

**Description:** Octets Received (31 to 0 bits)
**Address:** 0x40481150
**Offset:** 0x1150
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_BOTTOM [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_BOTTOM [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_BOTTOM [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_BOTTOM [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | COUNT_BOTTOM | RC | W | 0 | Received octets in frame without errors [31:0]. The number of octets received in valid frames of any type. This counter is 48-bits and is read through two registers. This count does not include octets from pause frames, and is only incremented if the frame is successfully filtered. |

### 11.3.80 ETH_OCTETS_RXED_TOP

**Description:** Octets Received (47 to 32 bits)
**Address:** 0x40481154
**Offset:** 0x1154
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_TOP [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_TOP [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | COUNT_TOP | RC | W | 0 | Received octets in frame without errors [47:32]. The number of octets received in valid frames of any type. This counter is 48-bits and is read through two registers. This count does not include octets from pause frames, and is only incremented if the frame is successfully filtered. |

### 11.3.81 ETH_FRAMES_RXED_OK

**Description:** Frames Received
**Address:** 0x40481158
**Offset:** 0x1158
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_OK [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_OK [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_OK [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_OK [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | COUNT_OK | RC | W | 0 | Frames received without error. A 32 bit register counting the number of frames successfully received. Excludes pause frames, and is only incremented if the frame is successfully filtered. |

### 11.3.82 ETH_BROADCAST_RXED

**Description:** Broadcast Frames Received
**Address:** 0x4048115C
**Offset:** 0x115C
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_BROADCAST [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_BROADCAST [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_BROADCAST [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_BROADCAST [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | COUNT_BROADCAST | RC | W | 0 | Broadcast frames received without error. A 32 bit register counting the number of broadcast frames successfully received without error. Excludes pause frames, and is only incremented if the frame is successfully filtered. |

### 11.3.83 ETH_MULTICAST_RXED

**Description:** Multicast Frames Received
**Address:** 0x40481160
**Offset:** 0x1160
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_MULTICAST [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_MULTICAST [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_MULTICAST [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_MULTICAST [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | COUNT_MULTICAST | RC | W | 0 | Multicast frames received without error. A 32 bit register counting the number of multicast frames successfully received without error. Excludes pause frames, and is only incremented if the frame is successfully filtered. |

### 11.3.84 ETH_PAUSE_FRAMES_RXED

**Description:** Pause Frames Received
**Address:** 0x40481164
**Offset:** 0x1164
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_PAUSE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_PAUSE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | COUNT_PAUSE | RC | W | 0 | Received pause frames - a 16 bit register counting the number of pause frames received without error. |

### 11.3.85 ETH_FRAMES_RXED_64

**Description:** 64 Byte Frames Received
**Address:** 0x40481168
**Offset:** 0x1168
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_64 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_64 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_64 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_64 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | COUNT_64 | RC | W | 0 | 64 byte frames received without error. A 32 bit register counting the number of 64 byte frames successfully received without error. Excludes pause frames, and is only incremented if the frame is successfully filtered. |

### 11.3.86 ETH_FRAMES_RXED_65

**Description:** 65 to 127 Byte Frames Received
**Address:** 0x4048116C
**Offset:** 0x116C
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_65 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_65 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_65 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_65 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | COUNT_65 | RC | W | 0 | 65 to 127 byte frames received without error. A 32 bit register counting the number of 65 to 127 byte frames successfully received without error. Excludes pause frames, and is only incremented if the frame is successfully filtered. |

### 11.3.87 ETH_FRAMES_RXED_128

**Description:** 128 to 255 Byte Frames Received
**Address:** 0x40481170
**Offset:** 0x1170
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_128 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_128 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_128 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_128 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | COUNT_128 | RC | W | 0 | 128 to 255 byte frames received without error. A 32 bit register counting the number of 128 to 255 byte frames successfully received without error. Excludes pause frames, and is only incremented if the frame is successfully filtered. |

### 11.3.88 ETH_FRAMES_RXED_256

**Description:** 256 to 511 Byte Frames Received
**Address:** 0x40481174
**Offset:** 0x1174
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_256 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_256 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_256 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_256 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | COUNT_256 | RC | W | 0 | 256 to 511 byte frames received without error. A 32 bit register counting the number of 256 to 511 byte frames successfully transmitted without error. Excludes pause frames, and is only incremented if the frame is successfully filtered. |

### 11.3.89 ETH_FRAMES_RXED_512

**Description:** 512 to 1023 Byte Frames Received
**Address:** 0x40481178
**Offset:** 0x1178
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_512 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_512 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_512 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_512 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | COUNT_512 | RC | W | 0 | 512 to 1023 byte frames received without error. A 32 bit register counting the number of 512 to 1023 byte frames successfully received without error. Excludes pause frames, and is only incremented if the frame is successfully filtered. |

### 11.3.90 ETH_FRAMES_RXED_1024

**Description:** 1024 to 1518 Byte Frames Received
**Address:** 0x4048117C
**Offset:** 0x117C
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_1024 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_1024 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_1024 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_1024 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | COUNT_1024 | RC | W | 0 | 1024 to 1518 byte frames received without error. A 32 bit register counting the number of 1024 to 1518 byte frames successfully received without error. Excludes pause frames, and is only incremented if the frame is successfully filtered. |

### 11.3.91 ETH_FRAMES_RXED_1519

**Description:** 1519 to maximum Byte Frames Received
**Address:** 0x40481180
**Offset:** 0x1180
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_1519 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_1519 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_1519 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_1519 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | COUNT_1519 | RC | W | 0 | 1519 to maximum byte frames received without error. A 32 bit register counting the number of 1519 byte or above frames successfully received without error. Maximum frame size is determined by the network configuration register bit 8 (1536 maximum frame size) or bit 3 (jumbo frame size). Excludes pause frames, and is only incremented if the frame is successfully filtered. |

### 11.3.92 ETH_UNDERSIZE_FRAMES

**Description:** Undersized Frames Received
**Address:** 0x40481184
**Offset:** 0x1184
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_UNDERSIZE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:10] | | | | | | COUNT_UNDERSIZE [9:8] | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:9 | COUNT_UNDERSIZE | RC | W | 0 | Undersize frames received - a 10 bit register counting the number of frames received less than 64 bytes in length (10/100 mode or gigabit mode, full duplex) that do not have either a CRC error or an alignment error. In gigabit mode, half duplex, this register counts either frames not conforming to the minimum slot time of 512 bytes or frames not conforming to the minimum frame size once bursting is active. |

### 11.3.93 ETH_EXCESSIVE_RX_LENGTH

**Description:** Oversize Frames Received
**Address:** 0x40481188
**Offset:** 0x1188
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_OVERSIZE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:10] | | | | | | COUNT_OVERSIZE [9:8] | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:9 | COUNT_OVERSIZE | RC | W | 0 | Oversize frames received - a 10 bit register counting the number of frames received exceeding 1518 bytes (1536 bytes if bit 8 is set in network configuration register, 10,240 bytes if bit 3 is set in the network configuration register) in length but do not have either a CRC error, an alignment error nor a receive symbol error. |

### 11.3.94 ETH_RX_JABBERS

**Description:** Jabbers Received
**Address:** 0x4048118C
**Offset:** 0x118C
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_JABBERS [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:10] | | | | | | COUNT_JABBERS [9:8] | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:9 | COUNT_JABBERS | RC | W | 0 | Jabbers received - a 10 bit register counting the number of frames received exceeding 1518 bytes (1536 if bit 8 set in network configuration register, 10,240 bytes if bit 3 is set in the network configuration register) in length and have either a CRC error, an alignment error or a receive symbol error. |

### 11.3.95 ETH_FCS_ERRORS

**Description:** Frame Check Sequence Errors
**Address:** 0x40481190
**Offset:** 0x1190
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_FCS_ERR [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:10] | | | | | | COUNT_FCS_ERR [9:8] | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:9 | COUNT_FCS_ERR | RC | W | 0 | Frame check sequence errors - a 10 bit register counting frames that are an integral number of bytes, have bad CRC and are between 64 and 1518 bytes in length (1536 if bit 8 set in network configuration register, 10,240 bytes if bit 3 is set in the network configuration register). This register is also incremented if a symbol error is detected and the frame is of valid length and has an integral number of bytes. This register is incremented for a frame with bad FCS, regardless of whether it is copied to memory due to ignore FCS mode being enabled in bit 26 of the network configuration register. |

### 11.3.96 ETH_RX_LENGTH_ERRORS

**Description:** Length Field Frame Errors
**Address:** 0x40481194
**Offset:** 0x1194
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_LENGTH_ERR [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:10] | | | | | | COUNT_LENGTH_ERR [9:8] | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:9 | COUNT_LENGTH_ERR | RC | W | 0 | Length field frame errors - this 10-bit register counts the number of frames received that have a measured length shorter than that extracted from the length field (bytes 13 and 14). This condition is only counted if the value of the length field is less than 0x0600, the frame is not of excessive length and checking is enabled through bit 16 of the network configuration register. |

### 11.3.97 ETH_RX_SYMBOL_ERRORS

**Description:** Receive Symbol Errors
**Address:** 0x40481198
**Offset:** 0x1198
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_SYMBOL_ERR [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:10] | | | | | | COUNT_SYMBOL_ERR [9:8] | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:9 | COUNT_SYMBOL_ERR | RC | W | 0 | Receive symbol errors - a 10-bit register counting the number of frames that had rx_er asserted during reception. For 10/100 mode symbol errors are counted regardless of frame length checks. For gigabit mode the frame must satisfy slot time requirements in order to count a symbol error. Additionally, in gigabit half duplex mode, carrier extension errors are also recorded. Receive symbol errors will also be counted as an FCS or alignment error if the frame is between 64 and 1518 bytes (1536 bytes if bit 8 is set in the network configuration register, 10240 bytes if bit 3 is set in the network configuration register). If the frame is larger it will be recorded as a jabber error. |

### 11.3.98 ETH_ALIGNMENT_ERRORS

**Description:** Alignment Errors
**Address:** 0x4048119C
**Offset:** 0x119C
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_ALIGNMENT_ERROR [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:10] | | | | | | COUNT_ALIGNMENT _ERROR [9:8] | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:9 | COUNT_ALIGNMENT _ERROR | RC | W | 0 | Alignment errors - a 10 bit register counting frames that are not an integral number of bytes long and have bad CRC when their length is truncated to an integral number of bytes and are between 64 and 1518 bytes in length (1536 if bit 8 set in network configuration register, 10,240 bytes if bit 3 is set in the network configuration register). This register is also incremented if a symbol error is detected and the frame is of valid length and does not have an integral number of bytes. |

### 11.3.99 ETH_RX_RESOURCE_ERRORS

**Description:** Receive Resource Errors
**Address:** 0x404811A0
**Offset:** 0x11A0
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_RESOURCE_ERR [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_RESOURCE_ERR [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:18] | | | | | | COUNT_RESOURCE_ERR [17:16] | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:17 | COUNT_RESOURCE_ERR | RC | W | 0 | Receive resource errors - an 18 bit register counting the number of frames that were successfully received by the MAC (correct address matched frame and adequate slot time) but could not be copied to memory because no receive buffer was available. This occurs when the GEM reads a buffer descriptor with its ownership (or used) bit set. |

### 11.3.100 ETH_RX_OVERRUNS

**Description:** Receive Overruns
**Address:** 0x404811A4
**Offset:** 0x11A4
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_OVERRUN [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:10] | | | | | | COUNT_OVERRUN [9:8] | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:9 | COUNT_OVERRUN | RC | W | 0 | Receive overruns - a 10 bit register counting the number of frames that are address recognized but were not copied to memory due to a receive overrun. |

### 11.3.101 ETH_RX_IP_CK_ERRORS

**Description:** IP Header Checksum Errors
**Address:** 0x404811A8
**Offset:** 0x11A8
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_IPCK_ERR [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | COUNT_IPCK_ERR | RC | W | 0 | IP header checksum errors - an 8-bit register counting the number of frames discarded due to an incorrect IP header checksum, but are between 64 and 1518 bytes (1536 bytes if bit 8 is set in the network configuration register or 10240 bytes if bit 3 is in the network configuration register) and do not have a CRC error, an alignment error, nor a symbol error. |

### 11.3.102 ETH_RX_TCP_CK_ERRORS

**Description:** TCP Checksum Errors
**Address:** 0x404811AC
**Offset:** 0x11AC
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_TCPCK_ERR [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | COUNT_TCPCK_ERR | RC | W | 0 | TCP checksum errors - an 8-bit register counting the number of frames discarded due to an incorrect TCP checksum, but are between 64 and 1518 bytes (1536 bytes if bit 8 is set in the network configuration register or 10240 bytes if bit 3 is in the network configuration register) and do not have a CRC error, an alignment error, nor a symbol error. |

### 11.3.103 ETH_RX_UDP_CK_ERRORS

**Description:** UDP Checksum Errors
**Address:** 0x404811B0
**Offset:** 0x11B0
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_UDPCK_ERR [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | COUNT_UDPCK_ERR | RC | W | 0 | UDP checksum errors - an 8-bit register counting the number of frames discarded due to an incorrect UDP checksum, but are between 64 and 1518 bytes (1536 bytes if bit 8 is set in the network configuration register or 10240 bytes if bit 3 is in the network configuration register) and do not have a CRC error, an alignment error, nor a symbol error. |

### 11.3.104 ETH_AUTO_FLUSHED_PKTS

**Description:** Receive DMA Flushed Packets
**Address:** 0x404811B4
**Offset:** 0x11B4
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_FLUSHED [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_FLUSHED [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | COUNT_FLUSHED | RC | W | 0 | Flushed RX packets counter. A 16 bit register counting the number of frames that have been flushed from the receive SRAM based packet buffer due to one of the following reasons .1. When partial store and forward mode is enabled or bit 24 of the DMA configuration register is enabled, a packet is received while there is no AMBA (AXI) resource. 2. When partial store and forward mode is enabled and an AMBA (AXI) error is encountered while writing the packet data to external memory. When bit 18 of the network control register(software action to flush a packet from the head of the PBUF queue) is pulsed and the GEM DMA is not currently busy. |

### 11.3.105 ETH_TSU_TIMER_INCR_SUB_NSEC

**Description:** 1588 Timer Increment Register sub nsec
**Address:** 0x404811BC
**Offset:** 0x11BC
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | SUB_NS_INCR [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | SUB_NS_INCR [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | SUB_NS_INCR_LSB [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | SUB_NS_INCR | RW | R | 0 | These are the most significant bits [23:8] of the sub-ns value by which the 1588 timer will be incremented each clock cycle. 24 bits of sub nanosecond precision gives resolution of approximately 5.86E-17 seconds (16 bits gives 15.2 femtoseconds). |
| 24:31 | SUB_NS_INCR_LSB | RW | R | 0 | These are the least significant bits [7:0] of the sub-ns value by which the 1588 timer will be incremented each clock cycle. |

### 11.3.106 ETH_TSU_TIMER_MSB_SEC

**Description:** 1588 Timer Seconds Register (47 to 32 bits)
**Address:** 0x404811C0
**Offset:** 0x11C0
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | TIMER_MSB_SEC [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | TIMER_MSB_SEC [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | TIMER_MSB_SEC | RW | RW | 0 | TSU timer value (s). Most significant 16 bits of seconds timer count. The register is writeable. The 48-bit counter increments by one when the 1588 nanoseconds counter counts to one second. It may also be incremented or decremented when the timer adjust register is written (if decremented from zero the 48-bit combined count would roll back to 0xFFFFFFFFFFFF). Note: The value of this register is used only when the lower 32 bit register is written to. This is to ensure a single update of the 48 bit seconds value |

### 11.3.107 ETH_TSU_STROBE_MSB_SEC

**Description:** 1588 Timer Sync Strobe Seconds Register (47 to 32 bits)
**Address:** 0x404811C4
**Offset:** 0x11C4
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | STROBE_MSB_SEC [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | STROBE_MSB_SEC [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | STROBE_MSB_SEC | R | W | 0 | 1588 Timer Sync Strobe Seconds. The most significant 16-bit value of the Timer Seconds register captured when gem_tsu_ms and gem_tsu_inc_ctrl are zero. |

### 11.3.108 ETH_TSU_STROBE_SEC

**Description:** 1588 Timer Sync Strobe Seconds Register (31 to 0 bits)
**Address:** 0x404811C8
**Offset:** 0x11C8
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | STROBE_SEC [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | STROBE_SEC [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | STROBE_SEC [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | STROBE_SEC [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | STROBE_SEC | R | W | 0 | 1588 Timer Sync Strobe Seconds. The lowest significant 32-bit value of the Timer Seconds register captured when gem_tsu_ms and gem_tsu_inc_ctrl are zero. |

### 11.3.109 ETH_TSU_STROBE_NSEC

**Description:** 1588 Timer Sync Strobe Nanoseconds Register
**Address:** 0x404811CC
**Offset:** 0x11CC
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | STROBE_NSEC [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | STROBE_NSEC [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | STROBE_NSEC [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:30] | | STROBE_NSEC [29:24] | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:29 | STROBE_NSEC | R | W | 0 | 1588 Timer Sync Strobe Nanoseconds. The value of the Timer Nanoseconds register captured when gem_tsu_ms and gem_tsu_inc_ctrl are zero. |

### 11.3.110 ETH_TSU_TIMER_SEC

**Description:** 1588 Timer Seconds Register (31 to 0 bits)
**Address:** 0x404811D0
**Offset:** 0x11D0
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | TIMER_SEC [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | TIMER_SEC [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | TIMER_SEC [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | TIMER_SEC [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | TIMER_SEC | RW | RW | 0 | 1588 Timer Seconds Register. TSU timer value (s). Least significant 32 bits of seconds timer count. This register is writeable. The 48-bit counter increments by one when the 1588 nanoseconds counter counts to one second. It may also be incremented or decremented when the timer adjust register is written (if decremented from zero the 48-bit combined count would roll back to 0xFFFFFFFFFFFF). |

### 11.3.111 ETH_TSU_TIMER_NSEC

**Description:** 1588 Timer Nanoseconds Register
**Address:** 0x404811D4
**Offset:** 0x11D4
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | TIMER_NSEC [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | TIMER_NSEC [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | TIMER_NSEC [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:30] | | TIMER_NSEC [29:24] | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:29 | TIMER_NSEC | RW | RW | 0 | Timer count in nanoseconds. This register is writeable. It can also be adjusted by writes to the 1588 timer adjust register. It increments by the value of the 1588 timer increment register each clock cycle (if this register is close to zero and a write to the timer adjust register causes a decrement the seconds register will be decremented if necessary and the nanoseconds register will roll back to 9999999xx(decimal)). |

### 11.3.112 ETH_TSU_TIMER_ADJUST

**Description:** This register is used to adjust the value of the timer in the TSU. It allows an integral number of nanoseconds to be added or subtracted from the timer in a one-off operation. This register returns all zeroes when read.
**Address:** 0x404811D8
**Offset:** 0x11D8
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | INCREMENT_VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | INCREMENT_VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | INCREMENT_VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | ADD _SUBTR ACT [31:31] | None [30:30] | INCREMENT_VALUE [29:24] | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:29 | INCREMENT_VALUE | W | R | 0 | Timer increment value. The number of nanoseconds to increment or decrement the 1588 timer nanoseconds register. If necessary the 1588 seconds register will be incremented or decremented. |
| 31 | ADD_SUBTRACT | W | R | 0 | Write as one to subtract from the 1588 timer. Write as zero to add to it. |

### 11.3.113 ETH_TSU_TIMER_INCR

**Description:** 1588 Timer Increment Register
**Address:** 0x404811DC
**Offset:** 0x11DC
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | NS_INCREMENT [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | ALT_NS_INCR [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | NUM_INCS [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | NS_INCREMENT | RW | R | 0 | A count of nanoseconds by which the 1588 timer nanoseconds register will be incremented each clock cycle. These are the most significant 8 bits of the 32 bit timer_increment counter. The tsu_timer_incr_sub_nsec register holds the least significant 24 bits of the increment. |
| 8:15 | ALT_NS_INCR | RW | R | 0 | Alternative nanoseconds count. Alternative count of nanoseconds by which the 1588 timer nanoseconds register will be incremented each clock cycle. |
| 16:23 | NUM_INCS | RW | R | 0 | Number of incs before alt inc. The number of increments after which the alternative increment is used. |

### 11.3.114 ETH_TSU_PTP_TX_SEC

**Description:** PTP Event Frame Transmitted Seconds Register (31 to 0 bits)
**Address:** 0x404811E0
**Offset:** 0x11E0
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | TIMER_PTP_SEC [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | TIMER_PTP_SEC [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | TIMER_PTP_SEC [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | TIMER_PTP_SEC [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | TIMER_PTP_SEC | R | W | 0 | PTP Event Frame Transmitted Seconds. The register is updated with the value that the 1588 timer seconds register held when the SFD of a PTP transmit primary event crosses the MII interface. The actual update occurs when the GEM recognizes the frame as a PTP sync or delay_req frame. An interrupt is issued when the register is updated. |

### 11.3.115 ETH_TSU_PTP_TX_NSEC

**Description:** PTP Event Frame Transmitted Nanoseconds Register
**Address:** 0x404811E4
**Offset:** 0x11E4
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | TIMER_PTP_NSEC [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | TIMER_PTP_NSEC [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | TIMER_PTP_NSEC [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:30] | | TIMER_PTP_NSEC [29:24] | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:29 | TIMER_PTP_NSEC | R | W | 0 | PTP Event Frame Transmitted Nanoseconds. The register is updated with the value that the 1588 timer nanoseconds register held when the SFD of a PTP transmit primary event crosses the MII interface. The actual update occurs when the GEM recognizes the frame as a PTP sync or delay_req frame. An interrupt is issued when the register is updated. |

### 11.3.116 ETH_TSU_PTP_RX_SEC

**Description:** PTP Event Frame Received Seconds Register (31 to 0 bits)
**Address:** 0x404811E8
**Offset:** 0x11E8
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | TIMER_PTP_SEC [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | TIMER_PTP_SEC [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | TIMER_PTP_SEC [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | TIMER_PTP_SEC [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | TIMER_PTP_SEC | R | W | 0 | PTP Event Frame Received Seconds. The register is updated with the value that the 1588 timer seconds register held when the SFD of a PTP receive primary event crosses the MII interface. The actual update occurs when the GEM recognizes the frame as a PTP sync or delay_req frame. An interrupt is issued when the register is updated. |

### 11.3.117 ETH_TSU_PTP_RX_NSEC

**Description:** PTP Event Frame Received Nanoseconds Register
**Address:** 0x404811EC
**Offset:** 0x11EC
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | TIMER_PTP_NSEC [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | TIMER_PTP_NSEC [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | TIMER_PTP_NSEC [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:30] | | TIMER_PTP_NSEC [29:24] | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:29 | TIMER_PTP_NSEC | R | W | 0 | PTP Event Frame Received Nanoseconds. The register is updated with the value that the 1588 timer nanoseconds register held when the SFD of a PTP receive primary event crosses the MII interface. The actual update occurs when the GEM recognizes the frame as a PTP sync or delay_req frame. An interrupt is issued when the register is updated. |

### 11.3.118 ETH_TSU_PEER_TX_SEC

**Description:** PTP Peer Event Frame Transmitted Seconds Register (31 to 0 bits)
**Address:** 0x404811F0
**Offset:** 0x11F0
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | TIMER_PEER_SEC [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | TIMER_PEER_SEC [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | TIMER_PEER_SEC [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | TIMER_PEER_SEC [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | TIMER_PEER_SEC | R | W | 0 | PTP Peer Event Frame Received Seconds. The register is updated with the value that the 1588 timer seconds register held when the SFD of a PTP transmit peer event crosses the MII interface. The actual update occurs when the GEM recognizes the frame as a PTP pdelay_req or pdelay_resp frame. An interrupt is issued when the register is updated. |

### 11.3.119 ETH_TSU_PEER_TX_NSEC

**Description:** PTP Peer Event Frame Transmitted Nanoseconds Register
**Address:** 0x404811F4
**Offset:** 0x11F4
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | TIMER_PEER_NSEC [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | TIMER_PEER_NSEC [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | TIMER_PEER_NSEC [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:30] | | TIMER_PEER_NSEC [29:24] | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:29 | TIMER_PEER_NSEC | R | W | 0 | PTP Peer Event Frame Transmitted Nanoseconds. The register is updated with the value that the 1588 timer nanoseconds register held when the SFD of a PTP transmit peer event crosses the MII interface. The actual update occurs when the GEM recognizes the frame as a PTP pdelay_req or pdelay_resp frame. An interrupt is issued when the register is updated. |

### 11.3.120 ETH_TSU_PEER_RX_SEC

**Description:** PTP Peer Event Frame Received Seconds Register (31 to 0 bits)
**Address:** 0x404811F8
**Offset:** 0x11F8
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | TIMER_PEER_SEC [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | TIMER_PEER_SEC [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | TIMER_PEER_SEC [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | TIMER_PEER_SEC [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | TIMER_PEER_SEC | R | W | 0 | PTP Peer Event Frame Received Seconds. The register is updated with the value that the 1588 timer seconds register held when the SFD of a PTP receive peer event crosses the MII interface. The actual update occurs when the GEM recognizes the frame as a PTP pdelay_req or pdelay_resp frame. An interrupt is issued when the register is updated. |

### 11.3.121 ETH_TSU_PEER_RX_NSEC

**Description:** PTP Peer Event Frame Received Nanoseconds Register
**Address:** 0x404811FC
**Offset:** 0x11FC
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | TIMER_PEER_NSEC [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | TIMER_PEER_NSEC [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | TIMER_PEER_NSEC [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:30] | | TIMER_PEER_NSEC [29:24] | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:29 | TIMER_PEER_NSEC | R | W | 0 | PTP Peer Event Frame Received Nanoseconds. The register is updated with the value that the 1588 timer nanoseconds register held when the SFD of a PTP receive peer event crosses the MII interface. The actual update occurs when the GEM recognizes the frame as a PTP pdelay_req or pdelay_resp frame. An interrupt is issued when the register is updated. |

### 11.3.122 ETH_PCS_CONTROL

**Description:** Not presents. Access to the register returns AHB error.
**Address:** 0x40481200
**Offset:** 0x1200
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | REMOVED_31_0 | R | R | 0 | Write ignore, read 0 |

### 11.3.123 ETH_PCS_STATUS

**Description:** Not presents. Access to the register returns AHB error.
**Address:** 0x40481204
**Offset:** 0x1204
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | REMOVED_31_0 | R | R | 0 | Write ignore, read 0 |

### 11.3.124 ETH_PCS_AN_ADV

**Description:** Not presents. Access to the register returns AHB error.
**Address:** 0x40481210
**Offset:** 0x1210
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | REMOVED_31_0 | R | R | 0 | Write ignore, read 0 |

### 11.3.125 ETH_PCS_AN_LP_BASE

**Description:** Not presents. Access to the register returns AHB error.
**Address:** 0x40481214
**Offset:** 0x1214
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | REMOVED_31_0 | R | R | 0 | Write ignore, read 0 |

### 11.3.126 ETH_PCS_AN_EXP

**Description:** Not presents. Access to the register returns AHB error.
**Address:** 0x40481218
**Offset:** 0x1218
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | REMOVED_31_0 | R | R | 0 | Write ignore, read 0 |

### 11.3.127 ETH_PCS_AN_NP_TX

**Description:** Not presents. Access to the register returns AHB error.
**Address:** 0x4048121C
**Offset:** 0x121C
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | REMOVED_31_0 | R | R | 0 | Write ignore, read 0 |

### 11.3.128 ETH_PCS_AN_LP_NP

**Description:** Not presents. Access to the register returns AHB error.
**Address:** 0x40481220
**Offset:** 0x1220
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | REMOVED_31_0 | R | R | 0 | Write ignore, read 0 |

### 11.3.129 ETH_PCS_AN_EXT_STATUS

**Description:** Not presents. Access to the register returns AHB error.
**Address:** 0x4048123C
**Offset:** 0x123C
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | REMOVED_31_0 | R | R | 0 | Write ignore, read 0 |

### 11.3.130 ETH_TX_PAUSE_QUANTUM1

**Description:** Transmit Pause Quantum Register 1
**Address:** 0x40481260
**Offset:** 0x1260
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xFFFFFFFF

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | QUANTUM_P2 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | QUANTUM_P2 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | QUANTUM_P3 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | QUANTUM_P3 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | QUANTUM_P2 | RW | R | 65535 | Transmit pause quantum - written with the pause quantum value for pause frame transmission of priority 2. |
| 16:31 | QUANTUM_P3 | RW | R | 65535 | Transmit pause quantum - written with the pause quantum value for pause frame transmission of priority 3. |

### 11.3.131 ETH_TX_PAUSE_QUANTUM2

**Description:** Transmit Pause Quantum Register 2
**Address:** 0x40481264
**Offset:** 0x1264
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xFFFFFFFF

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | QUANTUM_P4 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | QUANTUM_P4 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | QUANTUM_P5 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | QUANTUM_P5 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | QUANTUM_P4 | RW | R | 65535 | Transmit pause quantum - written with the pause quantum value for pause frame transmission of priority 4. |
| 16:31 | QUANTUM_P5 | RW | R | 65535 | Transmit pause quantum - written with the pause quantum value for pause frame transmission of priority 5. |

### 11.3.132 ETH_TX_PAUSE_QUANTUM3

**Description:** Transmit Pause Quantum Register 3
**Address:** 0x40481268
**Offset:** 0x1268
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xFFFFFFFF

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | QUANTUM_P6 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | QUANTUM_P6 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | QUANTUM_P7 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | QUANTUM_P7 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | QUANTUM_P6 | RW | R | 65535 | Transmit pause quantum - written with the pause quantum value for pause frame transmission of priority 6. |
| 16:31 | QUANTUM_P7 | RW | R | 65535 | Transmit pause quantum - written with the pause quantum value for pause frame transmission of priority 7. |

### 11.3.133 ETH_RX_LPI

**Description:** Received LPI transitions
**Address:** 0x40481270
**Offset:** 0x1270
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_LPI [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_LPI [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | COUNT_LPI | RC | RW | 0 | Count of RX LPI transitions. A count of the number of times there is a transition from receiving normal idle to receiving low power idle. Cleared on read. |

### 11.3.134 ETH_RX_LPI_TIME

**Description:** Received LPI time
**Address:** 0x40481274
**Offset:** 0x1274
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | LPI_TIME [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | LPI_TIME [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | LPI_TIME [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:23 | LPI_TIME | RC | RW | 0 | Time in LPI. This register increments once every 16 pclk cycles when the LPI indication bit 20 is set in the receive configuration register. Cleared on read. |

### 11.3.135 ETH_TX_LPI

**Description:** Transmit LPI transitions
**Address:** 0x40481278
**Offset:** 0x1278
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_LPI [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT_LPI [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | COUNT_LPI | RC | RW | 0 | Count of LPI transmissions. A count of the number of times the enable LPI transmission bit 20 goes from low to high in the transmit control register. |

### 11.3.136 ETH_TX_LPI_TIME

**Description:** Transmit LPI time
**Address:** 0x4048127C
**Offset:** 0x127C
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | LPI_TIME [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | LPI_TIME [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | LPI_TIME [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:23 | LPI_TIME | RC | RW | 0 | Time in LPI. This register increments once every 16 pclk cycles when the enable LPI transmission bit 20 is set in the transmit control register. Cleared on read. |

### 11.3.137 ETH_DESIGNCFG_DEBUG1

**Description:** The GEM_GXL(3PIP) has many parameterisation options to configure the IP during compilation stage. This is achieved using Verilog define compiler directives in an include file called mxeth_defs.v.
**Address:** 0x40481280
**Offset:** 0x1280
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x2508503

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_7 [7:7] | EXT_FIFO_INTERFACE [6:6] | RESERVED_5 [5:5] | INT_LOOPBACK [4:4] | RESERVED_2 [3:2] | | EXCLUDE_QBV [1:1] | NO_PCS [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | USER_IN_WIDTH [15:15] | USER_OUT_WIDTH [14:10] | | | | | USER_IO [9:9] | RESERVED_8 [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | IRQ_READ_CLEAR [23:23] | NO_SNAPSHOT [22:22] | NO_STATS [21:21] | RESERVED_20 [20:20] | USER_IN_WIDTH [19:16] | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | AXI_CACHE_VALUE [31:28] | | | | DMA_BUS_WIDTH [27:25] | | | EXCLUDE_CBS [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | NO_PCS | R | W | 1 | Takes the value of the `gem_no_pcs DEFINE |
| 1 | EXCLUDE_QBV | R | W | 1 | Takes the value of the `gem_exclude_qbv DEFINE |
| 2:3 | RESERVED_2 | R | W | 0 | Reserved, read as 0, ignored on write. |
| 4 | INT_LOOPBACK | R | W | 0 | Takes the value of the `gem_int_loopback DEFINE |
| 5 | RESERVED_5 | R | W | 0 | Reserved, read as 0, ignored on write |
| 6 | EXT_FIFO_INTERFACE | R | W | 0 | Takes the value of the `gem_ext_fifo_interface DEFINE |
| 7 | RESERVED_7 | R | W | 0 | Reserved, read as 0, ignored on write |
| 8 | RESERVED_8 | R | W | 1 | Reserved, read as 1, ignored on write |
| 9 | USER_IO | R | W | 0 | Takes the value of the `gem_user_io DEFINE |
| 10:14 | USER_OUT_WIDTH | R | W | 1 | Takes the value of the `gem_user_out_width DEFINE if `gem_user_io is set.<br>If 'gem_user_io is not set, the value is 0x01 |
| 15:19 | USER_IN_WIDTH | R | W | 1 | Takes the value of the `gem_user_in_width DEFINE `gem_user_io.<br>If 'gem_user_io is not set, the value is 0x01 |
| 20 | RESERVED_20 | R | W | 1 | Reserved, read as 1, ignored on write |
| 21 | NO_STATS | R | W | 0 | Takes the value of the `gem_no_stats DEFINE |
| 22 | NO_SNAPSHOT | R | W | 1 | Takes the value of the `gem_no_snapshot DEFINE |
| 23 | IRQ_READ_CLEAR | R | W | 0 | Takes the value of the `gem_irq_read_clear DEFINE |
| 24 | EXCLUDE_CBS | R | W | 0 | Takes the value of the `gem_exclude_cbs DEFINE |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 25:27 | DMA_BUS_WIDTH | R | W | 1 | Takes the value of bits 7:5 of the `gem_dma_bus_width DEFINE. So if the define is set to decimal 64 this will return binary 010. |
| 28:31 | AXI_CACHE_VALUE | R | W | 0 | Takes the value of the `gem_axi_awcache_value DEFINE |

### 11.3.138 ETH_DESIGNCFG_DEBUG2

**Description:** Design Configuration Register 2
**Address:** 0x40481284
**Offset:** 0x1284
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xE6310600

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | JUMBO_MAX_LENGTH [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:14] | | JUMBO_MAX_LENGTH [13:8] | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | RX_PBUF_ADDR [23:22] | | TX_PKT _BUFFER [21:21] | RX_PKT _BUFFER [20:20] | HPROT_VALUE [19:16] | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | SPRAM [31:31] | AXI [30:30] | TX_PBUF_ADDR [29:26] | | | | RX_PBUF_ADDR [25:24] | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:13 | JUMBO_MAX_LENGTH | R | W | 1536 | Takes the value of the `gem_jumbo_max_length DEFINE |
| 16:19 | HPROT_VALUE | R | W | 1 | Takes the value of the `gem_hprot_value DEFINE |
| 20 | RX_PKT_BUFFER | R | W | 1 | Takes the value of the `gem_rx_pkt_buffer DEFINE |
| 21 | TX_PKT_BUFFER | R | W | 1 | Takes the value of the `gem_tx_pkt_buffer DEFINE |
| 22:25 | RX_PBUF_ADDR | R | W | 8 | Takes the value of the `gem_rx_pbuf_addr DEFINE |
| 26:29 | TX_PBUF_ADDR | R | W | 9 | Takes the value of the `gem_tx_pbuf_addr DEFINE |
| 30 | AXI | R | W | 1 | Takes the value of the `gem_axi DEFINE |
| 31 | SPRAM | R | W | 1 | Takes the value of the `gem_spram DEFINE |

### 11.3.139 ETH_DESIGNCFG_DEBUG3

**Description:** Design Configuration Register 3
**Address:** 0x40481288
**Offset:** 0x1288
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x4000000

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:30] | | NUM_SPEC_ADD_FILTERS [29:24] | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 24:29 | NUM_SPEC_ADD_FILTERS | R | W | 4 | Takes the value of the `num_spec_add_filters DEFINE |

### 11.3.140 ETH_DESIGNCFG_DEBUG4

**Description:** Design Configuration Register 4
**Address:** 0x4048128C
**Offset:** 0x128C
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_0 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_0 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_0 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_0 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | RESERVED_31_0 | R | W | 0 | Unused, read zero - reserved for `gem_tx_fifo_size DEFINE in internal FIFO mode |

### 11.3.141 ETH_DESIGNCFG_DEBUG5

**Description:** Design Configuration Register 5
**Address:** 0x40481290
**Offset:** 0x1290
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x518E3744

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | TX_FIFO_CNT_WIDTH [7:4] | | | | RX_FIFO_CNT_WIDTH [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | ENDIAN_SWAP_DEF [15:15] | MDC_CLOCK_DIV [14:12] | | | DMA_BUS_WIDTH_DEF [11:10] | | PHY_IDENT [9:9] | TSU [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | RX_BUFFER_LENGTH_DEF [23:20] | | | | TX_PBUF_SIZE_DEF [19:19] | RX_PBUF_SIZE_DEF [18:17] | | ENDIAN_SWAP_DEF [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | AXI_PROT_VALUE [31:29] | | | TSU_CLK [28:28] | RX_BUFFER_LENGTH_DEF [27:24] | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | RX_FIFO_CNT_WIDTH | R | W | 4 | Takes the value of the `gem_rx_fifo_cnt_width DEFINE |
| 4:7 | TX_FIFO_CNT_WIDTH | R | W | 4 | Takes the value of the `gem_tx_fifo_cnt_width DEFINE |
| 8 | TSU | R | W | 1 | Takes the value of the `gem_tsu DEFINE |
| 9 | PHY_IDENT | R | W | 1 | Takes the value of the `gem_phy_ident DEFINE |
| 10:11 | DMA_BUS_WIDTH_DEF | R | W | 1 | Takes the value of the `gem_dma_bus_width_def DEFINE |
| 12:14 | MDC_CLOCK_DIV | R | W | 3 | Takes the value of the `gem_mdc_clock_div DEFINE |
| 15:16 | ENDIAN_SWAP_DEF | R | W | 0 | Takes the value of the `gem_endian_swap_def DEFINE |
| 17:18 | RX_PBUF_SIZE_DEF | R | W | 3 | Takes the value of the `gem_rx_pbuf_size_def DEFINE |
| 19 | TX_PBUF_SIZE_DEF | R | W | 1 | Takes the value of the `gem_tx_pbuf_size_def DEFINE |
| 20:27 | RX_BUFFER_LENGTH_DEF | R | W | 24 | Takes the value of the `gem_rx_buffer_length_def DEFINE |
| 28 | TSU_CLK | R | W | 1 | Takes the value of the `gem_tsu_clk DEFINE |
| 29:31 | AXI_PROT_VALUE | R | W | 2 | Takes the value of the `gem_axi_prot_value DEFINE |

### 11.3.142 ETH_DESIGNCFG_DEBUG6

**Description:** Design Configuration Register 6
**Address:** 0x40481294
**Offset:** 0x1294
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x3020006

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DMA_PRIORITY_QUEUE7 [7:7] | DMA_PRIORITY_QUEUE6 [6:6] | DMA_PRIORITY_QUEUE5 [5:5] | DMA_PRIORITY_QUEUE4 [4:4] | DMA_PRIORITY_QUEUE3 [3:3] | DMA_PRIORITY_QUEUE2 [2:2] | DMA_PRIORITY_QUEUE1 [1:1] | None [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | DMA_PRIORITY_QUEUE15 [15:15] | DMA_PRIORITY_QUEUE14 [14:14] | DMA_PRIORITY_QUEUE13 [13:13] | DMA_PRIORITY_QUEUE12 [12:12] | DMA_PRIORITY_QUEUE11 [11:11] | DMA_PRIORITY_QUEUE10 [10:10] | DMA_PRIORITY_QUEUE9 [9:9] | DMA_PRIORITY_QUEUE8 [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | DMA_ADDR_WIDTH_IS_64B [23:23] | HOST_IF_SOFT_SELECT [22:22] | TX_ADD_FIFO_IF [21:21] | EXT_TSU_TIMER [20:20] | TX_PBUF_QUEUE_SEGMENT_SIZE [19:16] | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:28] | | | | PBUF_LSO [27:27] | PBUF_RSC [26:26] | PBUF_CUTTHRU [25:25] | PFC_MULTI_QUANTUM [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 1 | DMA_PRIORITY_QUEUE1 | R | W | 1 | Takes the value of the `dma_priority_queue1 DEFINE |
| 2 | DMA_PRIORITY_QUEUE2 | R | W | 1 | Takes the value of the `dma_priority_queue2 DEFINE |
| 3 | DMA_PRIORITY_QUEUE3 | R | W | 0 | Takes the value of the `dma_priority_queue3 DEFINE |
| 4 | DMA_PRIORITY_QUEUE4 | R | W | 0 | Takes the value of the `dma_priority_queue4 DEFINE |
| 5 | DMA_PRIORITY_QUEUE5 | R | W | 0 | Takes the value of the `dma_priority_queue5 DEFINE |
| 6 | DMA_PRIORITY_QUEUE6 | R | W | 0 | Takes the value of the `dma_priority_queue6 DEFINE |
| 7 | DMA_PRIORITY_QUEUE7 | R | W | 0 | Takes the value of the `dma_priority_queue7 DEFINE |
| 8 | DMA_PRIORITY_QUEUE8 | R | W | 0 | Takes the value of the `dma_priority_queue8 DEFINE |
| 9 | DMA_PRIORITY_QUEUE9 | R | W | 0 | Takes the value of the `dma_priority_queue9 DEFINE |
| 10 | DMA_PRIORITY_QUEUE10 | R | W | 0 | Takes the value of the `dma_priority_queue10 DEFINE |
| 11 | DMA_PRIORITY_QUEUE11 | R | W | 0 | Takes the value of the `dma_priority_queue11 DEFINE |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 12 | DMA_PRIORITY _QUEUE12 | R | W | 0 | Takes the value of the `dma_priority_queue12 DEFINE |
| 13 | DMA_PRIORITY _QUEUE13 | R | W | 0 | Takes the value of the `dma_priority_queue13 DEFINE |
| 14 | DMA_PRIORITY _QUEUE14 | R | W | 0 | Takes the value of the `dma_priority_queue14 DEFINE |
| 15 | DMA_PRIORITY _QUEUE15 | R | W | 0 | Takes the value of the `dma_priority_queue15 DEFINE |
| 16:19 | TX_PBUF_QUEUE _SEGMENT_SIZE | R | W | 2 | Takes the value of the `gem_tx_pbuf_queue_segment_size DEFINE |
| 20 | EXT_TSU_TIMER | R | W | 0 | Takes the value of the `gem_ext_tsu_timer DEFINE |
| 21 | TX_ADD_FIFO_IF | R | W | 0 | Takes the value of the `gem_tx_add_fifo_if DEFINE |
| 22 | HOST_IF_SOFT _SELECT | R | W | 0 | Takes the value of the `gem_host_if_soft_select DEFINE |
| 23 | DMA_ADDR_WIDTH_IS _64B | R | W | 0 | Takes the value of the `gem_dma_addr_width_is_64b DEFINE |
| 24 | PFC_MULTI_QUANTUM | R | W | 1 | Takes the value of the `gem_pfc_multi_quantum DEFINE |
| 25 | PBUF_CUTTHRU | R | W | 1 | Takes the value of the `gem_pbuf_cutthru DEFINE |
| 26 | PBUF_RSC | R | W | 0 | Takes the value of the `gem_pbuf_rsc DEFINE |
| 27 | PBUF_LSO | R | W | 0 | Takes the value of the `gem_pbuf_lso DEFINE |

### 11.3.143 ETH_DESIGNCFG_DEBUG7

**Description:** Design Configuration Register 7
**Address:** 0x40481298
**Offset:** 0x1298
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x1

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | X_PBUF_NUM_SEGMENTS_Q1 [7:4] | | | | X_PBUF_NUM_SEGMENTS_Q0 [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | X_PBUF_NUM_SEGMENTS_Q3 [15:12] | | | | X_PBUF_NUM_SEGMENTS_Q2 [11:8] | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | X_PBUF_NUM_SEGMENTS_Q5 [23:20] | | | | X_PBUF_NUM_SEGMENTS_Q4 [19:16] | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | X_PBUF_NUM_SEGMENTS_Q7 [31:28] | | | | X_PBUF_NUM_SEGMENTS_Q6 [27:24] | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | X_PBUF_NUM_SEGMENTS_Q0 | R | W | 1 | Takes the value of the `gem_tx_pbuf_num_segments_q0 DEFINE |
| 4:7 | X_PBUF_NUM_SEGMENTS_Q1 | R | W | 0 | Takes the value of the `gem_tx_pbuf_num_segments_q1 DEFINE |
| 8:11 | X_PBUF_NUM_SEGMENTS_Q2 | R | W | 0 | Takes the value of the `gem_tx_pbuf_num_segments_q2 DEFINE |
| 12:15 | X_PBUF_NUM_SEGMENTS_Q3 | R | W | 0 | Takes the value of the `gem_tx_pbuf_num_segments_q3 DEFINE |
| 16:19 | X_PBUF_NUM_SEGMENTS_Q4 | R | W | 0 | Takes the value of the `gem_tx_pbuf_num_segments_q4 DEFINE |
| 20:23 | X_PBUF_NUM_SEGMENTS_Q5 | R | W | 0 | Takes the value of the `gem_tx_pbuf_num_segments_q5 DEFINE |
| 24:27 | X_PBUF_NUM_SEGMENTS_Q6 | R | W | 0 | Takes the value of the `gem_tx_pbuf_num_segments_q6 DEFINE |
| 28:31 | X_PBUF_NUM_SEGMENTS_Q7 | R | W | 0 | Takes the value of the `gem_tx_pbuf_num_segments_q7 DEFINE |

### 11.3.144 ETH_DESIGNCFG_DEBUG8

**Description:** Design Configuration Register 8
**Address:** 0x4048129C
**Offset:** 0x129C
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x10100820

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | NUM_SCR2_COMPARE_REGS [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | NUM_SCR2_ETHTYPE_REGS [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | NUM_TYPE2_SCREENERS [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | NUM_TYPE1_SCREENERS [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | NUM_SCR2_COMPARE_REGS | R | W | 32 | Takes the value of the `num_scr2_compare_regs DEFINE |
| 8:15 | NUM_SCR2_ETHTYPE_REGS | R | W | 8 | Takes the value of the `num_scr2_ethtype_regs DEFINE |
| 16:23 | NUM_TYPE2_SCREENERS | R | W | 16 | Takes the value of the `num_type2_screeners DEFINE |
| 24:31 | NUM_TYPE1_SCREENERS | R | W | 16 | Takes the value of the `num_type1_screeners DEFINE |

### 11.3.145 ETH_DESIGNCFG_DEBUG9

**Description:** Design Configuration Register 9
**Address:** 0x404812A0
**Offset:** 0x12A0
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | TX_PBUF_NUM_SEGMENTS_Q9 [7:4] | | | | TX_PBUF_NUM_SEGMENTS_Q8 [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | TX_PBUF_NUM_SEGMENTS_Q11 [15:12] | | | | TX_PBUF_NUM_SEGMENTS_Q10 [11:8] | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | TX_PBUF_NUM_SEGMENTS_Q13 [23:20] | | | | TX_PBUF_NUM_SEGMENTS_Q12 [19:16] | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | TX_PBUF_NUM_SEGMENTS_Q15 [31:28] | | | | TX_PBUF_NUM_SEGMENTS_Q14 [27:24] | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | TX_PBUF_NUM_SEGMENTS_Q8 | R | W | 0 | Takes the value of the `gem_tx_pbuf_num_segments_q8 DEFINE |
| 4:7 | TX_PBUF_NUM_SEGMENTS_Q9 | R | W | 0 | Takes the value of the `gem_tx_pbuf_num_segments_q9 DEFINE |
| 8:11 | TX_PBUF_NUM_SEGMENTS_Q10 | R | W | 0 | Takes the value of the `gem_tx_pbuf_num_segments_q10 DEFINE |
| 12:15 | TX_PBUF_NUM_SEGMENTS_Q11 | R | W | 0 | Takes the value of the `gem_tx_pbuf_num_segments_q11 DEFINE |
| 16:19 | TX_PBUF_NUM_SEGMENTS_Q12 | R | W | 0 | Takes the value of the `gem_tx_pbuf_num_segments_q12 DEFINE |
| 20:23 | TX_PBUF_NUM_SEGMENTS_Q13 | R | W | 0 | Takes the value of the `gem_tx_pbuf_num_segments_q13 DEFINE |
| 24:27 | TX_PBUF_NUM_SEGMENTS_Q14 | R | W | 0 | Takes the value of the `gem_tx_pbuf_num_segments_q14 DEFINE |
| 28:31 | TX_PBUF_NUM_SEGMENTS_Q15 | R | W | 0 | Takes the value of the `gem_tx_pbuf_num_segments_q15 DEFINE |

### 11.3.146 ETH_DESIGNCFG_DEBUG10

**Description:** Design Configuration Register 10
**Address:** 0x404812A4
**Offset:** 0x12A4
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x14411111

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | AXI_TX_DESCR_WR_BUFF_BITS [7:4] | | | | AXI_RX_DESCR_WR_BUFF_BITS [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | AXI_TX_DESCR_RD_BUFF_BITS [15:12] | | | | AXI_RX_DESCR_RD_BUFF_BITS [11:8] | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | RX_PBUF_DATA [23:20] | | | | AXI_ACCESS_PIPELINE_BITS [19:16] | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | EMAC_BUS_WIDTH [31:28] | | | | TX_PBUF_DATA [27:24] | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | AXI_RX_DESCR_WR_BUFF_BITS | R | W | 1 | Takes the value of the `gem_axi_rx_descr_wr_buff_bits DEFINE |
| 4:7 | AXI_TX_DESCR_WR_BUFF_BITS | R | W | 1 | Takes the value of the `gem_axi_tx_descr_wr_buff_bits DEFINE |
| 8:11 | AXI_RX_DESCR_RD_BUFF_BITS | R | W | 1 | Takes the value of the `gem_axi_rx_descr_rd_buff_bits DEFINE |
| 12:15 | AXI_TX_DESCR_RD_BUFF_BITS | R | W | 1 | Takes the value of the `gem_axi_tx_descr_rd_buff_bits DEFINE |
| 16:19 | AXI_ACCESS_PIPELINE_BITS | R | W | 1 | Takes the value of the `gem_axi_access_pipeline_bits DEFINE |
| 20:23 | RX_PBUF_DATA | R | W | 4 | Takes the value of the `gem_rx_pbuf_data DEFINE. 1 - The RX DPRAM has a datawidth of 32bits. 2 - The RX DPRAM has a datawidth of 64bits. 4 - RX The DPRAM has a datawidth of 128bits |
| 24:27 | TX_PBUF_DATA | R | W | 4 | Takes the value of the `gem_tx_pbuf_data DEFINE. 1 - The TX DPRAM has a datawidth of 32bits. 2 - The TX DPRAM has a datawidth of 64bits. 4 - The TX DPRAM has a datawidth of 128bits |
| 28:31 | EMAC_BUS_WIDTH | R | W | 1 | Takes the value of the `gem_emac_bus_width DEFINE. 1 - The MAC has a datawidth of 32bits. 2 - The MAC has a datawidth of 64bits. 4 - The MAC has a datawidth of 128bits |

### 11.3.147 ETH_SPEC_ADD5_BOTTOM

**Description:** Specific address registers 5 ~ 36 doesn't present. Access to the register returns AHB error.
**Address:** 0x40481300
**Offset:** 0x1300
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_0 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_0 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_0 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_0 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | RESERVED_31_0 | R | R | 0 | Write ignore, read 0 |

### 11.3.148 ETH_SPEC_ADD5_TOP

**Description:** Specific address registers 5 ~ 36 doesn't present. Access to the register returns AHB error.
**Address:** 0x40481304
**Offset:** 0x1304
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_0 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_0 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_0 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_0 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | RESERVED_31_0 | R | R | 0 | Write ignore, read 0 |

### 11.3.149 ETH_SPEC_ADD36_BOTTOM

**Description:** Not presents.
**Address:** 0x404813F8
**Offset:** 0x13F8
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_0 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_0 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_0 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_0 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | RESERVED_31_0 | R | R | 0 | Write ignore, read 0 |

### 11.3.150 ETH_SPEC_ADD36_TOP

**Description:** Not presents.
**Address:** 0x404813FC
**Offset:** 0x13FC
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_0 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_0 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_0 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_0 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | RESERVED_31_0 | R | R | 0 | Write ignore, read 0 |

### 11.3.151 ETH_INT_Q1_STATUS

**Description:** Priority queue Interrupt Status Register
**Address:** 0x40481400
**Offset:** 0x1400
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | TRANSMIT_COMPLETE [7:7] | AMBA_ERROR [6:6] | RETRY_LIMIT_EXCEEDED_OR_LATE_COLLISION [5:5] | None [4:3] | | RX_USED_BIT_READ [2:2] | RECEIVE_COMPLETE [1:1] | None [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:12] | | | | RESP_NOT_OK [11:11] | None [10:8] | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 1 | RECEIVE_COMPLETE | RW1C | W | 0 | Receive complete |
| 2 | RX_USED_BIT_READ | RW1C | W | 0 | RX used bit read |
| 5 | RETRY_LIMIT_EXCEEDED_OR_LATE_COLLISION | RW1C | W | 0 | Retry limit exceeded or late collision |
| 6 | AMBA_ERROR | RW1C | W | 0 | Transmit frame corruption due to AMBA (AXI) error set if an error occurs whilst midway through reading transmit frame from the external memory, including RRESP and BRESP errors (AXI) and buffers exhausted mid frame |
| 7 | TRANSMIT_COMPLETE | RW1C | W | 0 | Transmit complete |
| 11 | RESP_NOT_OK | RW1C | W | 0 | bresp not OK |

### 11.3.152 ETH_INT_Q2_STATUS

**Description:** Priority queue Interrupt Status Register
**Address:** 0x40481404
**Offset:** 0x1404
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | TRANSMIT_COMPLETE [7:7] | AMBA_ERROR [6:6] | RETRY_LIMIT_EXCEEDED_OR_LATE_COLLISION [5:5] | None [4:3] | | RX_USED_BIT_READ [2:2] | RECEIVE_COMPLETE [1:1] | None [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:12] | | | | RESP_NOT_OK [11:11] | None [10:8] | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 1 | RECEIVE_COMPLETE | RW1C | W | 0 | Receive complete |
| 2 | RX_USED_BIT_READ | RW1C | W | 0 | RX used bit read |
| 5 | RETRY_LIMIT_EXCEEDED_OR_LATE_COLLISION | RW1C | W | 0 | Retry limit exceeded or late collision |
| 6 | AMBA_ERROR | RW1C | W | 0 | Transmit frame corruption due to AMBA (AXI) error set if an error occurs whilst midway through reading transmit frame from the external memory, including RRESP and BRESP errors (AXI) and buffers exhausted mid frame |
| 7 | TRANSMIT_COMPLETE | RW1C | W | 0 | Transmit complete |
| 11 | RESP_NOT_OK | RW1C | W | 0 | bresp not OK |

### 11.3.153 ETH_INT_Q3_STATUS

**Description:** int_q3_status to int_q15_status doesn't present. Access to the register returns AHB error.
**Address:** 0x40481408
**Offset:** 0x1408
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | REMOVED_31_0 | R | W | 0 | Write ignore, read 0 |

### 11.3.154 ETH_INT_Q15_STATUS

**Description:** Not presents.
**Address:** 0x40481438
**Offset:** 0x1438
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | REMOVED_31_0 | R | R | 0 | Write ignore, read 0 |

### 11.3.155 ETH_TRANSMIT_Q1_PTR

**Description:** This register holds the start address of the transmit buffer queue (transmit buffers descriptor list). The transmit buffer queue base address register must be initialized before transmit is started through bit 9 of the network control register. Once transmission has started, any write to the transmit buffer queue base address register is illegal and therefore ignored. Note that due to clock boundary synchronization, it takes a maximum of four pclk cycles from the writing of the transmit start bit before the transmitter is active. Writing to the transmit buffer queue base address register during this time may produce unpredictable results. Reading this register returns the location of the descriptor currently being accessed. Because the DMA can store data for multiple frames at once, this may not necessarily be pointing to the current frame being transmitted. In terms of AMBA AXI operation, the transmit descriptors are written to memory using a single 32bit AHB access. When the datapath is configured as 64bit , the transmit descriptors should be aligned at 64-bit boundaries and each pair of 32-bit descriptors is read from memory using a single AXI access.

**Address:** 0x40481440
**Offset:** 0x1440
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DMA_TX_Q_PTR [7:2] | | | | | | None [1:1] | DMA_TX_DIS_Q [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | DMA_TX_Q_PTR [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | DMA_TX_Q_PTR [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | DMA_TX_Q_PTR [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | DMA_TX_DIS_Q | RW | R | 0 | Disable queue if set to 1. This can be used to reduce the number of active queues and should only be changed while transmit is not enabled. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 2:31 | DMA_TX_Q_PTR | RW | R | 0 | This register holds the start address of the transmit buffer queue (transmit buffers descriptor list). The transmit buffer queue base address register must be initialized before transmit is started through bit 9 of the network control register. Once transmission has started, any write to the transmit buffer queue base address register is illegal and therefore ignored. Note that due to clock boundary synchronization, it takes a maximum of four pclk cycles from the writing of the transmit start bit before the transmitter is active. Writing to the transmit buffer queue base address register during this time may produce unpredictable results. Reading this register returns the location of the descriptor currently being accessed. Because the DMA can store data for multiple frames at once, this may not necessarily be pointing to the current frame being transmitted. In terms of AMBA AHB/AXI operation, the transmit descriptors are written to memory using a single 32bit AHB access. When the datapath is configured as 64bit or 128bit, the transmit descriptors should be aligned at 64-bit boundaries and each pair of 32-bit descriptors is read from memory using a single AHB/AXI access. For 32bit datapaths, the descriptors should be aligned at 32-bit boundaries and the descriptors are read from memory using two individual 32-bit non sequential accesses. |

### 11.3.156 ETH_TRANSMIT_Q2_PTR

**Description:** This register holds the start address of the transmit buffer queue (transmit buffers descriptor list). The transmit buffer queue base address register must be initialized before transmit is started through bit 9 of the network control register. Once transmission has started, any write to the transmit buffer queue base address register is illegal and therefore ignored. Note that due to clock boundary synchronization, it takes a maximum of four pclk cycles from the writing of the transmit start bit before the transmitter is active. Writing to the transmit buffer queue base address register during this time may produce unpredictable results. Reading this register returns the location of the descriptor currently being accessed. Because the DMA can store data for multiple frames at once, this may not necessarily be pointing to the current frame being transmitted. In terms of AMBA AXI operation, the transmit descriptors are written to memory using a single 32bit AHB access. When the datapath is configured as 64bit , the transmit descriptors should be aligned at 64-bit boundaries and each pair of 32-bit descriptors is read from memory using a single AXI access.

**Address:** 0x40481444
**Offset:** 0x1444
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DMA_TX_Q_PTR [7:2] | | | | | | None [1:1] | DMA_TX_DIS_Q [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | DMA_TX_Q_PTR [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | DMA_TX_Q_PTR [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | DMA_TX_Q_PTR [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | DMA_TX_DIS_Q | RW | R | 0 | Disable queue if set to 1. This can be used to reduce the number of active queues and should only be changed while transmit is not enabled. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 2:31 | DMA_TX_Q_PTR | RW | R | 0 | This register holds the start address of the transmit buffer queue (transmit buffers descriptor list). The transmit buffer queue base address register must be initialized before transmit is started through bit 9 of the network control register. Once transmission has started, any write to the transmit buffer queue base address register is illegal and therefore ignored. Note that due to clock boundary synchronization, it takes a maximum of four pclk cycles from the writing of the transmit start bit before the transmitter is active. Writing to the transmit buffer queue base address register during this time may produce unpredictable results. Reading this register returns the location of the descriptor currently being accessed. Because the DMA can store data for multiple frames at once, this may not necessarily be pointing to the current frame being transmitted. In terms of AMBA AHB/AXI operation, the transmit descriptors are written to memory using a single 32bit AHB access. When the datapath is configured as 64bit or 128bit, the transmit descriptors should be aligned at 64-bit boundaries and each pair of 32-bit descriptors is read from memory using a single AHB/AXI access. For 32bit datapaths, the descriptors should be aligned at 32-bit boundaries and the descriptors are read from memory using two individual 32-bit non sequential accesses |

### 11.3.157 ETH_TRANSMIT_Q3_PTR

**Description:** transmit_q3_ptr to transmit_q15_ptr doesn't present. Access to the register returns AHB error.
**Address:** 0x40481448
**Offset:** 0x1448
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | REMOVED_31_0 | R | R | 0 | Disable queue if set to 1. This can be used to reduce the number of active queues and should only be changed while transmit is not enabled. |

### 11.3.158 ETH_TRANSMIT_Q15_PTR

**Description:** Not presents.
**Address:** 0x40481478
**Offset:** 0x1478
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | REMOVED_31_0 | R | R | 0 | Write ignore, read 0 |

### 11.3.159 ETH_RECEIVE_Q1_PTR

**Description:** This register holds the start address of the transmit buffer queue (transmit buffers descriptor list). The transmit buffer queue base address register must be initialized before transmit is started through bit 9 of the network control register. Once transmission has started, any write to the transmit buffer queue base address register is illegal and therefore ignored. Note that due to clock boundary synchronization, it takes a maximum of four pclk cycles from the writing of the transmit start bit before the transmitter is active. Writing to the transmit buffer queue base address register during this time may produce unpredictable results. Reading this register returns the location of the descriptor currently being accessed. Because the DMA can store data for multiple frames at once, this may not necessarily be pointing to the current frame being transmitted. In terms of AMBA AXI operation, the transmit descriptors are written to memory using a single 32bit AHB access. When the datapath is configured as 64bit , the transmit descriptors should be aligned at 64-bit boundaries and each pair of 32-bit descriptors is read from memory using a single AXI access.

**Address:** 0x40481480
**Offset:** 0x1480
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DMA_RX_Q_PTR [7:2] | | | | | | None [1:1] | DMA_RX_DIS_Q [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | DMA_RX_Q_PTR [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | DMA_RX_Q_PTR [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | DMA_RX_Q_PTR [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | DMA_RX_DIS_Q | RW | R | 0 | Disable queue if set to 1. This can be used to reduce the number of active queues and should only be changed while receive is not enabled. |
| 2:31 | DMA_RX_Q_PTR | RW | R | 0 | Receive buffer queue base address - written with the address of the start of the receive queue. |

### 11.3.160 ETH_RECEIVE_Q2_PTR

**Description:** This register holds the start address of the transmit buffer queue (transmit buffers descriptor list). The transmit buffer queue base address register must be initialized before transmit is started through bit 9 of the network control register. Once transmission has started, any write to the transmit buffer queue base address register is illegal and therefore ignored. Note that due to clock boundary synchronization, it takes a maximum of four pclk cycles from the writing of the transmit start bit before the transmitter is active. Writing to the transmit buffer queue base address register during this time may produce unpredictable results. Reading this register returns the location of the descriptor currently being accessed. Because the DMA can store data for multiple frames at once, this may not necessarily be pointing to the current frame being transmitted. In terms of AMBA AXI operation, the transmit descriptors are written to memory using a single 32bit AHB access. When the datapath is configured as 64bit , the transmit descriptors should be aligned at 64-bit boundaries and each pair of 32-bit descriptors is read from memory using a single AXI access.

**Address:** 0x40481484
**Offset:** 0x1484
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DMA_RX_Q_PTR [7:2] | | | | | | None [1:1] | DMA_RX_DIS_Q [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | DMA_RX_Q_PTR [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | DMA_RX_Q_PTR [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | DMA_RX_Q_PTR [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | DMA_RX_DIS_Q | RW | R | 0 | Disable queue if set to 1. This can be used to reduce the number of active queues and should only be changed while receive is not enabled. |
| 2:31 | DMA_RX_Q_PTR | RW | R | 0 | Receive buffer queue base address - written with the address of the start of the receive queue. |

### 11.3.161 ETH_RECEIVE_Q3_PTR

**Description:** Not presents. Start address register doesn't present for queue3 ~ queue7.
**Address:** 0x40481488
**Offset:** 0x1488
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | REMOVED_31_0 | R | R | 0 | Write ignore, read 0 |

### 11.3.162 ETH_RECEIVE_Q7_PTR

**Description:** Not presents.
**Address:** 0x40481498
**Offset:** 0x1498
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | REMOVED_31_0 | R | R | 0 | Write ignore, read 0 |

### 11.3.163 ETH_DMA_RXBUF_SIZE_Q1

**Description:** Receive Buffer queue 1 Size
**Address:** 0x404814A0
**Offset:** 0x14A0
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x18

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DMA_RX_Q_BUF_SIZE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | DMA_RX_Q_BUF_SIZE | RW | R | 24 | DMA receive buffer size in system memory. The value defined by these bits determines the size of buffer to use in main system memory when writing received data. The value is defined in multiples of 64 bytes.<br>0x01 corresponds to buffers of 64 bytes.<br>0x02 corresponds to 128 bytes etc.<br>For example:<br>0x02: 128 byte<br>0x18: 1536 byte (1*max length frame/buffer)<br>0xA0: 10240 byte (1*10K jumbo frame/buffer)<br>Note that this value should never be written as zero.<br>Note. The reset value of this field is equal to the gem_rx_buffer_length_def define, which is user configurable. |

### 11.3.164 ETH_DMA_RXBUF_SIZE_Q2

**Description:** Receive Buffer queue 2 Size
**Address:** 0x404814A4
**Offset:** 0x14A4
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x18

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DMA_RX_Q_BUF_SIZE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | DMA_RX_Q_BUF_SIZE | RW | R | 24 | DMA receive buffer size in system memory. The value defined by these bits determines the size of buffer to use in main system memory when writing received data. The value is defined in multiples of 64 bytes.<br>0x01 corresponds to buffers of 64 bytes.<br>0x02 corresponds to 128 bytes etc.<br>For example:<br>0x02: 128 byte<br>0x18: 1536 byte (1*max length frame/buffer)<br>0xA0: 10240 byte (1*10K jumbo frame/buffer)<br>Note that this value should never be written as zero.<br>Note. The reset value of this field is equal to the gem_rx_buffer_length_def define, which is user configurable. |

### 11.3.165 ETH_DMA_RXBUF_SIZE_Q3

**Description:** dma_rxbuf_size_q3 to dma_rxbuf_size_q7 doesn't present.
**Address:** 0x404814A8
**Offset:** 0x14A8
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | REMOVED_31_0 | R | R | 0 | DMA receive buffer size in system memory. The value defined by these bits determines the size of buffer to use in main system memory when writing received data. The value is defined in multiples of 64 bytes.<br>0x01 corresponds to buffers of 64 bytes.<br>0x02 corresponds to 128 bytes etc.<br>For example:<br>0x02: 128 byte<br>0x18: 1536 byte (1*max length frame/buffer)<br>0xA0: 10240 byte (1*10K jumbo frame/buffer)<br>Note that this value should never be written as zero.<br>Note. The reset value of this field is equal to the gem_rx_buffer_length_def define, which is user configurable. |

### 11.3.166 ETH_DMA_RXBUF_SIZE_Q7

**Description:** Not presents.
**Address:** 0x404814B8
**Offset:** 0x14B8
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | REMOVED_31_0 | R | R | 0 | Write ignore, read 0 |

### 11.3.167 ETH_CBS_CONTROL

**Description:** The IdleSlope value is defined as the rate of change of credit when a packet is waiting to be sent. This must not exceed the portTransmitRate which is dependent on the speed of operation, eg, portTranmsitRate. 1Gb/s = 32'h07735940 (125 Mbytes/s), 100Mb/sec = 32'h017D7840 (25 Mnibbles/s), 10Mb/sec = 32'h002625A0 (2.5 Mnibbles/s). If 50 percent of bandwidth was to be allocated to a particular queue in 1Gb/sec mode then the IdleSlope value for that queue would be calculated as 32'h07735940/2. Note that Credit-Based Shaping should be disabled prior to updating the IdleSlope values. As another example, for a 1722 audio packet with a payload of 6 samples per channel, the packet size would be 7 (preamble) + 1 (SFD) + 50 (packet header) + 6x4x2(payload) + 4 (CRC) = 110 bytes. For a rate of 8000 packets per second, the desired rate would 110 x 8000 bytes per second, so the programmed idleSlope value would be 880000 for a 1Gb/s connection, or 1760000 for a 100Mb/s or 10Mbs connection. See Figure 6.3 in the IEEE 1722 standard. In practice, the actual transmission rate will be vary slightly from that calculated. In this case, the idleSlope value should be recalibrated based on the variance between the measured and expected rate, and in this case very accurate transmission rates can be achieved.

**Address:** 0x404814BC
**Offset:** 0x14BC
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:2] | | | | | | CBS_ENABLE_QUEUE_B [1:1] | CBS_ENABLE_QUEUE_A [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | CBS_ENABLE_QUEUE_A | RW | R | 0 | Enable Credit-Based Shaping on the highest priority queue (queue A). Write 1 to enable |
| 1 | CBS_ENABLE_QUEUE_B | RW | R | 0 | Enable Credit-Based shaping on the 2nd highest priority queue (queue B). Write 1 to enable |

### 11.3.168 ETH_CBS_IDLESLOPE_Q_A

**Description:** queue A is the highest priority queue. This would be queue 8 in an 8 queue configuration.
**Address:** 0x404814C0
**Offset:** 0x14C0
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | IDLESLOPE_A [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | IDLESLOPE_A [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | IDLESLOPE_A [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | IDLESLOPE_A [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | IDLESLOPE_A | RW | R | 0 | IdleSlope value for queue A in bytes/sec for gigabit operation and nibbles/sec for 10/100 operation |

### 11.3.169 ETH_CBS_IDLESLOPE_Q_B

**Description:** queue B is the 2nd highest priority queue. This would be queue 7 in an 8 queue configuration.
**Address:** 0x404814C4
**Offset:** 0x14C4
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | IDLESLOPE_B [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | IDLESLOPE_B [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | IDLESLOPE_B [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | IDLESLOPE_B [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | IDLESLOPE_B | RW | R | 0 | IdleSlope value for queue B in bytes/sec for gigabit operation and nibbles/sec for 10/100 operation |

### 11.3.170 ETH_UPPER_TX_Q_BASE_ADDR

**Description:** Upper 32 bits of transmit buffer descriptor queue base address.
**Address:** 0x404814C8
**Offset:** 0x14C8
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | UPPER_TX_Q_BASE_ADDR [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | UPPER_TX_Q_BASE_ADDR [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | UPPER_TX_Q_BASE_ADDR [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | UPPER_TX_Q_BASE_ADDR [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | UPPER_TX_Q_BASE_ADDR | RW | R | 0 | Upper 32 bits of transmit buffer descriptor queue base address. Used when 64 bit addressing is enabled. (In releases earlier to 1p06f2 this register also affected the receive descriptor queue.) |

### 11.3.171 ETH_TX_BD_CONTROL

**Description:** TX BD control register
**Address:** 0x404814CC
**Offset:** 0x14CC
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:6] | | TX_BD_TS_MODE [5:4] | | None [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 4:5 | TX_BD_TS_MODE | RW | R | 0 | TX Descriptor Timestamp Insertion mode, 00: TS insertion disable, 01: TS inserted for PTP Event Frames only, 10: TS inserted for All PTP Frames only, 11: TS insertion for All Frames |

### 11.3.172 ETH_RX_BD_CONTROL

**Description:** RX BD control register
**Address:** 0x404814D0
**Offset:** 0x14D0
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:6] | | RX_BD_TS_MODE [5:4] | | None [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 4:5 | RX_BD_TS_MODE | RW | R | 0 | RX Descriptor Timestamp Insertion mode, 00: TS insertion disable, 01: TS inserted for PTP Event Frames only, 10: TS inserted for All PTP Frames only, 11: TS insertion for All Frames |

### 11.3.173 ETH_UPPER_RX_Q_BASE_ADDR

**Description:** Upper 32 bits of receive buffer descriptor queue base address.
**Address:** 0x404814D4
**Offset:** 0x14D4
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | UPPER_RX_Q_BASE_ADDR [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | UPPER_RX_Q_BASE_ADDR [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | UPPER_RX_Q_BASE_ADDR [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | UPPER_RX_Q_BASE_ADDR [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | UPPER_RX_Q_BASE_ADDR | RW | R | 0 | Upper 32 bits of receive buffer descriptor queue base address. Used when 64 bit addressing is enabled. |

### 11.3.174 ETH_HIDDEN_REG0

**Description:** Hidden registers defined in edma_defs.v \`define gem_cbs_port_tx_rate_10m 12'h4e0 // 10M Port TX Rate *** HIDDEN Register ***'. Default value of cbs related hidden registers (0x14E0~0x14E8) are depicted in cbs_control register.
**Address:** 0x404814E0
**Offset:** 0x14E0
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x2625A0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | HIDDEN0_FIELD [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | HIDDEN0_FIELD [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | HIDDEN0_FIELD [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | HIDDEN0_FIELD [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | HIDDEN0_FIELD | RW | R | 2500000 | default value is defined per description of register cbs_control. |

### 11.3.175 ETH_HIDDEN_REG1

**Description:** Hidden registers defined in edma_defs.v \`define gem_cbs_port_tx_rate_100m 12'h4e4 // 100M Port TX Rate *** HIDDEN Register ***'
**Address:** 0x404814E4
**Offset:** 0x14E4
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x17D7840

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | HIDDEN1_FIELD [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | HIDDEN1_FIELD [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | HIDDEN1_FIELD [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | HIDDEN1_FIELD [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | HIDDEN1_FIELD | RW | R | 25000000 | default value is defined per description of register cbs_control. |

### 11.3.176 ETH_HIDDEN_REG2

**Description:** Hidden registers defined in edma_defs.v `define gem_cbs_port_tx_rate_1g 12'h4e8 // 1G Port TX Rate *** HIDDEN Register ***'
**Address:** 0x404814E8
**Offset:** 0x14E8
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x7735940

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | HIDDEN2_FIELD [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | HIDDEN2_FIELD [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | HIDDEN2_FIELD [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | HIDDEN2_FIELD [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | HIDDEN2_FIELD | RW | R | 125000000 | default value is defined per description of register cbs_control. |

### 11.3.177 ETH_HIDDEN_REG3

**Description:** Hidden registers defined in edma_defs.v `define gem_wd_counter 12'h4ec // *** HIDDEN Register ***'.
**Address:** 0x404814EC
**Offset:** 0x14EC
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x7

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:4] | | | | HIDDEN3_FIELD [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | HIDDEN3_FIELD | RW | R | 7 | default value is defined per description of register cbs_control. |

### 11.3.178 ETH_HIDDEN_REG4

**Description:** Hidden registers defined in edma_defs.v '`define gem_axi_tx_full_threshold0 12'h4f8 // AXI full threshold setting *** HIDDEN Register ***'. Note. When using AXI mode with a single port ram ( gem_spram == 1) mode and a 32b dma bus width ( gem_dma_bus_width == 32 or bits 22 to 21 of the network_config register are set to 0) the AXI hidden registers (0x14F8 and 0x14FC) need to be updated (these registers are used for fine tuning AXI dma bursts and normally should not be touched).
**Address:** 0x404814F8
**Offset:** 0x14F8
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x60008

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | HIDDEN4_FIELD_L [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:9] | | | | | | | HIDDEN4_FIELD_L [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | HIDDEN4_FIELD_H [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:25] | | | | | | | HIDDEN4_FIELD_H [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:8 | HIDDEN4_FIELD_L | RW | R | 8 | The valid bits is defined by `gem_tx_pbuf_addr. |
| 16:24 | HIDDEN4_FIELD_H | RW | R | 6 | The valid bits is defined by `gem_tx_pbuf_addr. |

### 11.3.179 ETH_HIDDEN_REG5

**Description:** Hidden registers defined in edma_defs.v '`define gem_axi_tx_full_threshold1 12'h4fc // AXI full threshold setting *** HIDDEN Register ***'.
**Address:** 0x404814FC
**Offset:** 0x14FC
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | HIDDEN5_FIELD_L [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:9] | | | | | | | HIDDEN5_FIELD_L [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | HIDDEN5_FIELD_H [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:25] | | | | | | | HIDDEN5_FIELD_H [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:8 | HIDDEN5_FIELD_L | RW | R | 0 | The valid bits is defined by `gem_tx_pbuf_addr. |
| 16:24 | HIDDEN5_FIELD_H | RW | R | 0 | The valid bits is defined by `gem_tx_pbuf_addr. |

### 11.3.180 ETH_SCREENING_TYPE_1_REGISTER_0

**Description:** Screening type 1 registers are used to allocate up to 16 priority queues to received frames based on certain IP or UDP fields of incoming frames. Firstly, when DS/TC match enable is set (bit 28), the DS (Differentiated Services) field of the received IPv4 header or TCfield (traffic class) of IPv6 headers are matched against bits 11 to 4. Secondly, when UDP port match enable is set (bit 29), the UDP Destination Port of the received UDP frame is matched against bits 27 to 12. Both UDP and DS/TC matching can be enabled simultaneously or individually. If a match is successful, then the queue value programmed in bits 2 to 0 is allocated to the frame. The required number of Type 1 screening registers is configured in the gem defines file. Up to 16 type 1 screening registers have been allocated APB address space between 0x500 and 0x53C.

**Address:** 0x40481500

**Offset:** 0x1500

**Retention:** Not Retained

**IsDeepSleep:** No

**Comment:**

**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DSTC_MATCH [7:4] | | | | QUEUE_NUMBER [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | UDP_PORT_MATCH [15:12] | | | | DSTC_MATCH [11:8] | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | UDP_PORT_MATCH [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:30] | | UDP_PORT_MATCH_ENABLE [29:29] | DSTC_ENABLE [28:28] | UDP_PORT_MATCH [27:24] | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | QUEUE_NUMBER | RW | R | 0 | Queue Number (0 to 15) |
| 4:11 | DSTC_MATCH | RW | R | 0 | DS/TC Match |
| 12:27 | UDP_PORT_MATCH | RW | R | 0 | UDP Port Match |
| 28 | DSTC_ENABLE | RW | R | 0 | DS/TC Enable |
| 29 | UDP_PORT_MATCH_ENABLE | RW | R | 0 | UDP port match enable |

### 11.3.181 ETH_SCREENING_TYPE_1_REGISTER_1

**Description:** screening type 1 register 1, same as screening_type_1_register_0
**Address:** 0x40481504
**Offset:** 0x1504
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DSTC_MATCH [7:4] | | | | QUEUE_NUMBER [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | UDP_PORT_MATCH [15:12] | | | | DSTC_MATCH [11:8] | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | UDP_PORT_MATCH [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:30] | | UDP_PORT_MATCH_ENABLE [29:29] | DSTC_ENABLE [28:28] | UDP_PORT_MATCH [27:24] | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | QUEUE_NUMBER | RW | R | 0 | Queue Number (0 to 15) |
| 4:11 | DSTC_MATCH | RW | R | 0 | DS/TC Match |
| 12:27 | UDP_PORT_MATCH | RW | R | 0 | UDP Port Match |
| 28 | DSTC_ENABLE | RW | R | 0 | DS/TC Enable |
| 29 | UDP_PORT_MATCH_ENABLE | RW | R | 0 | UDP port match enable |

### 11.3.182 ETH_SCREENING_TYPE_1_REGISTER_2

**Description:** screening type 1 register 2, same as screening_type_1_register_0
**Address:** 0x40481508
**Offset:** 0x1508
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DSTC_MATCH [7:4] | | | | QUEUE_NUMBER [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | UDP_PORT_MATCH [15:12] | | | | DSTC_MATCH [11:8] | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | UDP_PORT_MATCH [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:30] | | UDP_PORT_MATCH_ENABLE [29:29] | DSTC_ENABLE [28:28] | UDP_PORT_MATCH [27:24] | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | QUEUE_NUMBER | RW | R | 0 | Queue Number (0 to 15) |
| 4:11 | DSTC_MATCH | RW | R | 0 | DS/TC Match |
| 12:27 | UDP_PORT_MATCH | RW | R | 0 | UDP Port Match |
| 28 | DSTC_ENABLE | RW | R | 0 | DS/TC Enable |
| 29 | UDP_PORT_MATCH_ENABLE | RW | R | 0 | UDP port match enable |

### 11.3.183 ETH_SCREENING_TYPE_1_REGISTER_3

**Description:** screening type 1 register 3, same as screening_type_1_register_0
**Address:** 0x4048150C
**Offset:** 0x150C
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DSTC_MATCH [7:4] | | | | QUEUE_NUMBER [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | UDP_PORT_MATCH [15:12] | | | | DSTC_MATCH [11:8] | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | UDP_PORT_MATCH [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:30] | | UDP_PORT_MATCH_ENABLE [29:29] | DSTC_ENABLE [28:28] | UDP_PORT_MATCH [27:24] | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | QUEUE_NUMBER | RW | R | 0 | Queue Number (0 to 15) |
| 4:11 | DSTC_MATCH | RW | R | 0 | DS/TC Match |
| 12:27 | UDP_PORT_MATCH | RW | R | 0 | UDP Port Match |
| 28 | DSTC_ENABLE | RW | R | 0 | DS/TC Enable |
| 29 | UDP_PORT_MATCH_ENABLE | RW | R | 0 | UDP port match enable |

### 11.3.184 ETH_SCREENING_TYPE_1_REGISTER_4

**Description:** screening type 1 register 4, same as screening_type_1_register_0
**Address:** 0x40481510
**Offset:** 0x1510
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DSTC_MATCH [7:4] | | | | QUEUE_NUMBER [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | UDP_PORT_MATCH [15:12] | | | | DSTC_MATCH [11:8] | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | UDP_PORT_MATCH [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:30] | | UDP_PORT_MATCH_ENABLE [29:29] | DSTC_ENABLE [28:28] | UDP_PORT_MATCH [27:24] | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | QUEUE_NUMBER | RW | R | 0 | Queue Number (0 to 15) |
| 4:11 | DSTC_MATCH | RW | R | 0 | DS/TC Match |
| 12:27 | UDP_PORT_MATCH | RW | R | 0 | UDP Port Match |
| 28 | DSTC_ENABLE | RW | R | 0 | DS/TC Enable |
| 29 | UDP_PORT_MATCH_ENABLE | RW | R | 0 | UDP port match enable |

### 11.3.185 ETH_SCREENING_TYPE_1_REGISTER_5

**Description:** screening type 1 register 5, same as screening_type_1_register_0
**Address:** 0x40481514
**Offset:** 0x1514
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DSTC_MATCH [7:4] | | | | QUEUE_NUMBER [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | UDP_PORT_MATCH [15:12] | | | | DSTC_MATCH [11:8] | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | UDP_PORT_MATCH [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:30] | | UDP_PORT_MATCH_ENABLE [29:29] | DSTC_ENABLE [28:28] | UDP_PORT_MATCH [27:24] | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | QUEUE_NUMBER | RW | R | 0 | Queue Number (0 to 15) |
| 4:11 | DSTC_MATCH | RW | R | 0 | DS/TC Match |
| 12:27 | UDP_PORT_MATCH | RW | R | 0 | UDP Port Match |
| 28 | DSTC_ENABLE | RW | R | 0 | DS/TC Enable |
| 29 | UDP_PORT_MATCH_ENABLE | RW | R | 0 | UDP port match enable |

### 11.3.186 ETH_SCREENING_TYPE_1_REGISTER_6

**Description:** screening type 1 register 6, same as screening_type_1_register_0
**Address:** 0x40481518
**Offset:** 0x1518
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DSTC_MATCH [7:4] | | | | QUEUE_NUMBER [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | UDP_PORT_MATCH [15:12] | | | | DSTC_MATCH [11:8] | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | UDP_PORT_MATCH [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:30] | | UDP_PORT_MATCH_ENABLE [29:29] | DSTC_ENABLE [28:28] | UDP_PORT_MATCH [27:24] | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | QUEUE_NUMBER | RW | R | 0 | Queue Number (0 to 15) |
| 4:11 | DSTC_MATCH | RW | R | 0 | DS/TC Match |
| 12:27 | UDP_PORT_MATCH | RW | R | 0 | UDP Port Match |
| 28 | DSTC_ENABLE | RW | R | 0 | DS/TC Enable |
| 29 | UDP_PORT_MATCH_ENABLE | RW | R | 0 | UDP port match enable |

### 11.3.187 ETH_SCREENING_TYPE_1_REGISTER_7

**Description:** screening type 1 register 7, same as screening_type_1_register_0
**Address:** 0x4048151C
**Offset:** 0x151C
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DSTC_MATCH [7:4] | | | | QUEUE_NUMBER [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | UDP_PORT_MATCH [15:12] | | | | DSTC_MATCH [11:8] | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | UDP_PORT_MATCH [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:30] | | UDP_PORT_MATCH_ENABLE [29:29] | DSTC_ENABLE [28:28] | UDP_PORT_MATCH [27:24] | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | QUEUE_NUMBER | RW | R | 0 | Queue Number (0 to 15) |
| 4:11 | DSTC_MATCH | RW | R | 0 | DS/TC Match |
| 12:27 | UDP_PORT_MATCH | RW | R | 0 | UDP Port Match |
| 28 | DSTC_ENABLE | RW | R | 0 | DS/TC Enable |
| 29 | UDP_PORT_MATCH_ENABLE | RW | R | 0 | UDP port match enable |

### 11.3.188 ETH_SCREENING_TYPE_1_REGISTER_8

**Description:** screening type 1 register 8, same as screening_type_1_register_0
**Address:** 0x40481520
**Offset:** 0x1520
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DSTC_MATCH [7:4] | | | | QUEUE_NUMBER [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | UDP_PORT_MATCH [15:12] | | | | DSTC_MATCH [11:8] | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | UDP_PORT_MATCH [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:30] | | UDP_PORT_MATCH_ENABLE [29:29] | DSTC_ENABLE [28:28] | UDP_PORT_MATCH [27:24] | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | QUEUE_NUMBER | RW | R | 0 | Queue Number (0 to 15) |
| 4:11 | DSTC_MATCH | RW | R | 0 | DS/TC Match |
| 12:27 | UDP_PORT_MATCH | RW | R | 0 | UDP Port Match |
| 28 | DSTC_ENABLE | RW | R | 0 | DS/TC Enable |
| 29 | UDP_PORT_MATCH_ENABLE | RW | R | 0 | UDP port match enable |

### 11.3.189 ETH_SCREENING_TYPE_1_REGISTER_9

**Description:** screening type 1 register 9, same as screening_type_1_register_0
**Address:** 0x40481524
**Offset:** 0x1524
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DSTC_MATCH [7:4] | | | | QUEUE_NUMBER [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | UDP_PORT_MATCH [15:12] | | | | DSTC_MATCH [11:8] | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | UDP_PORT_MATCH [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:30] | | UDP_PORT_MATCH_ENABLE [29:29] | DSTC_ENABLE [28:28] | UDP_PORT_MATCH [27:24] | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | QUEUE_NUMBER | RW | R | 0 | Queue Number (0 to 15) |
| 4:11 | DSTC_MATCH | RW | R | 0 | DS/TC Match |
| 12:27 | UDP_PORT_MATCH | RW | R | 0 | UDP Port Match |
| 28 | DSTC_ENABLE | RW | R | 0 | DS/TC Enable |
| 29 | UDP_PORT_MATCH_ENABLE | RW | R | 0 | UDP port match enable |

### 11.3.190 ETH_SCREENING_TYPE_1_REGISTER_10

**Description:** screening type 1 register 10, same as screening_type_1_register_0
**Address:** 0x40481528
**Offset:** 0x1528
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DSTC_MATCH [7:4] | | | | QUEUE_NUMBER [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | UDP_PORT_MATCH [15:12] | | | | DSTC_MATCH [11:8] | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | UDP_PORT_MATCH [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:30] | | UDP_PORT_MATCH_ENABLE [29:29] | DSTC_ENABLE [28:28] | UDP_PORT_MATCH [27:24] | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | QUEUE_NUMBER | RW | R | 0 | Queue Number (0 to 15) |
| 4:11 | DSTC_MATCH | RW | R | 0 | DS/TC Match |
| 12:27 | UDP_PORT_MATCH | RW | R | 0 | UDP Port Match |
| 28 | DSTC_ENABLE | RW | R | 0 | DS/TC Enable |
| 29 | UDP_PORT_MATCH_ENABLE | RW | R | 0 | UDP port match enable |

### 11.3.191 ETH_SCREENING_TYPE_1_REGISTER_11

**Description:** screening type 1 register 11, same as screening_type_1_register_0
**Address:** 0x4048152C
**Offset:** 0x152C
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DSTC_MATCH [7:4] | | | | QUEUE_NUMBER [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | UDP_PORT_MATCH [15:12] | | | | DSTC_MATCH [11:8] | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | UDP_PORT_MATCH [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:30] | | UDP_PORT_MATCH_ENABLE [29:29] | DSTC_ENABLE [28:28] | UDP_PORT_MATCH [27:24] | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | QUEUE_NUMBER | RW | R | 0 | Queue Number (0 to 15) |
| 4:11 | DSTC_MATCH | RW | R | 0 | DS/TC Match |
| 12:27 | UDP_PORT_MATCH | RW | R | 0 | UDP Port Match |
| 28 | DSTC_ENABLE | RW | R | 0 | DS/TC Enable |
| 29 | UDP_PORT_MATCH_ENABLE | RW | R | 0 | UDP port match enable |

### 11.3.192 ETH_SCREENING_TYPE_1_REGISTER_12

**Description:** screening type 1 register 12, same as screening_type_1_register_0
**Address:** 0x40481530
**Offset:** 0x1530
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DSTC_MATCH [7:4] | | | | QUEUE_NUMBER [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | UDP_PORT_MATCH [15:12] | | | | DSTC_MATCH [11:8] | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | UDP_PORT_MATCH [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:30] | | UDP_PORT_MATCH_ENABLE [29:29] | DSTC_ENABLE [28:28] | UDP_PORT_MATCH [27:24] | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | QUEUE_NUMBER | RW | R | 0 | Queue Number (0 to 15) |
| 4:11 | DSTC_MATCH | RW | R | 0 | DS/TC Match |
| 12:27 | UDP_PORT_MATCH | RW | R | 0 | UDP Port Match |
| 28 | DSTC_ENABLE | RW | R | 0 | DS/TC Enable |
| 29 | UDP_PORT_MATCH_ENABLE | RW | R | 0 | UDP port match enable |

### 11.3.193 ETH_SCREENING_TYPE_1_REGISTER_13

**Description:** screening type 1 register 13, same as screening_type_1_register_0
**Address:** 0x40481534
**Offset:** 0x1534
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DSTC_MATCH [7:4] | | | | QUEUE_NUMBER [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | UDP_PORT_MATCH [15:12] | | | | DSTC_MATCH [11:8] | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | UDP_PORT_MATCH [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:30] | | UDP_PORT_MATCH_ENABLE [29:29] | DSTC_ENABLE [28:28] | UDP_PORT_MATCH [27:24] | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | QUEUE_NUMBER | RW | R | 0 | Queue Number (0 to 15) |
| 4:11 | DSTC_MATCH | RW | R | 0 | DS/TC Match |
| 12:27 | UDP_PORT_MATCH | RW | R | 0 | UDP Port Match |
| 28 | DSTC_ENABLE | RW | R | 0 | DS/TC Enable |
| 29 | UDP_PORT_MATCH_ENABLE | RW | R | 0 | UDP port match enable |

### 11.3.194 ETH_SCREENING_TYPE_1_REGISTER_14

**Description:** screening type 1 register 14, same as screening_type_1_register_0
**Address:** 0x40481538
**Offset:** 0x1538
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DSTC_MATCH [7:4] | | | | QUEUE_NUMBER [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | UDP_PORT_MATCH [15:12] | | | | DSTC_MATCH [11:8] | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | UDP_PORT_MATCH [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:30] | | UDP_PORT_MATCH_ENABLE [29:29] | DSTC_ENABLE [28:28] | UDP_PORT_MATCH [27:24] | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | QUEUE_NUMBER | RW | R | 0 | Queue Number (0 to 15) |
| 4:11 | DSTC_MATCH | RW | R | 0 | DS/TC Match |
| 12:27 | UDP_PORT_MATCH | RW | R | 0 | UDP Port Match |
| 28 | DSTC_ENABLE | RW | R | 0 | DS/TC Enable |
| 29 | UDP_PORT_MATCH_ENABLE | RW | R | 0 | UDP port match enable |

### 11.3.195 ETH_SCREENING_TYPE_1_REGISTER_15

**Description:** screening type 1 register 15, same as screening_type_1_register_0
**Address:** 0x4048153C
**Offset:** 0x153C
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DSTC_MATCH [7:4] | | | | QUEUE_NUMBER [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | UDP_PORT_MATCH [15:12] | | | | DSTC_MATCH [11:8] | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | UDP_PORT_MATCH [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:30] | | UDP_PORT_MATCH_ENABLE [29:29] | DSTC_ENABLE [28:28] | UDP_PORT_MATCH [27:24] | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | QUEUE_NUMBER | RW | R | 0 | Queue Number (0 to 15) |
| 4:11 | DSTC_MATCH | RW | R | 0 | DS/TC Match |
| 12:27 | UDP_PORT_MATCH | RW | R | 0 | UDP Port Match |
| 28 | DSTC_ENABLE | RW | R | 0 | DS/TC Enable |
| 29 | UDP_PORT_MATCH_ENABLE | RW | R | 0 | UDP port match enable |

### 11.3.196 ETH_SCREENING_TYPE_2_REGISTER_0

**Description:** Screener Type 2 match registers operate independently of screener type 1 registers and offer additional match capabilities, extending the capabilities into vendor specific protocols.
**Address:** 0x40481540
**Offset:** 0x1540
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** 'Screener Type 2 match registers allow a screen to be configured that is the combination of all or any of the following comparisons:
1) An enabled VLAN Priority. A VLAN Priority match will be performed if the VLAN priority enable is set. The extracted priority field in the VLAN header is compared against 3 bits within the screener type 2 register itself.
2) An enabled EtherType.
3) An enabled Field Compare A.
4) An enabled Field Compare B.
5) An enabled Field Compare C.
The required number of Type 2 screening registers is configured in the gem defines file. Up to 16 type 2 screening registers have been allocated APB address space between 0x540 and 0x57C. The bit mappings for these registers is as follows:'
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_7 [7:7] | VLAN_PRIORITY [6:4] | | | QUEUE_NUMBER [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_A [15:13] | | | ETHERTYPE_ENABLE [12:12] | INDEX [11:9] | | | VLAN_ENABLE [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_B [23:19] | | | | | COMPARE_A_ENABLE [18:18] | COMPARE_A [17:16] | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31 [31:31] | COMPARE_C_ENABLE [30:30] | COMPARE_C [29:25] | | | | | COMPARE_B_ENABLE [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | QUEUE_NUMBER | RW | R | 0 | 'Queue Number (0 to 15)' |
| 4:6 | VLAN_PRIORITY | RW | R | 0 | 'VLAN Priority' |
| 7 | RESERVED_7 | RW | R | 0 | 'Reserved and implemented as RW' |
| 8 | VLAN_ENABLE | RW | R | 0 | 'VLAN Enable' |
| 9:11 | INDEX | RW | R | 0 | 'Index to screener type 2 EtherType register' |
| 12 | ETHERTYPE_ENABLE | RW | R | 0 | 'EtherType Enable' |
| 13:17 | COMPARE_A | RW | R | 0 | 'Compare A - Index to screener type 2 Compare register ' |
| 18 | COMPARE_A_ENABLE | RW | R | 0 | 'Compare A Enable' |
| 19:23 | COMPARE_B | RW | R | 0 | 'Compare B - Index to screener type 2 Compare register' |
| 24 | COMPARE_B_ENABLE | RW | R | 0 | 'Compare B Enable' |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 25:29 | COMPARE_C | RW | R | 0 | 'Compare C - Index to screener type 2 Compare register' |
| 30 | COMPARE_C_ENABLE | RW | R | 0 | 'Compare C Enable' |
| 31 | RESERVED_31 | R | R | 0 | 'Reserved, read as 0, ignored on write.' |

### 11.3.197 ETH_SCREENING_TYPE_2_REGISTER_1

**Description:** screening type 2 register 1, same as screening_type_2_register_0
**Address:** 0x40481544
**Offset:** 0x1544
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_7 [7:7] | VLAN_PRIORITY [6:4] | | | QUEUE_NUMBER [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_A [15:13] | | | ETHERTYPE_ENABLE [12:12] | INDEX [11:9] | | | VLAN_ENABLE [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_B [23:19] | | | | | COMPARE_A_ENABLE [18:18] | COMPARE_A [17:16] | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31 [31:31] | COMPARE_C_ENABLE [30:30] | COMPARE_C [29:25] | | | | | COMPARE_B_ENABLE [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | QUEUE_NUMBER | RW | R | 0 | 'Queue Number (0 to 15)' |
| 4:6 | VLAN_PRIORITY | RW | R | 0 | 'VLAN Priority' |
| 7 | RESERVED_7 | RW | R | 0 | 'Reserved and implemented as RW' |
| 8 | VLAN_ENABLE | RW | R | 0 | 'VLAN Enable' |
| 9:11 | INDEX | RW | R | 0 | 'Index to screener type 2 EtherType register' |
| 12 | ETHERTYPE_ENABLE | RW | R | 0 | 'EtherType Enable' |
| 13:17 | COMPARE_A | RW | R | 0 | 'Compare A - Index to screener type 2 Compare register ' |
| 18 | COMPARE_A_ENABLE | RW | R | 0 | 'Compare A Enable' |
| 19:23 | COMPARE_B | RW | R | 0 | 'Compare B - Index to screener type 2 Compare register' |
| 24 | COMPARE_B_ENABLE | RW | R | 0 | 'Compare B Enable' |
| 25:29 | COMPARE_C | RW | R | 0 | 'Compare C - Index to screener type 2 Compare register' |
| 30 | COMPARE_C_ENABLE | RW | R | 0 | 'Compare C Enable' |
| 31 | RESERVED_31 | R | R | 0 | 'Reserved, read as 0, ignored on write.' |

### 11.3.198 ETH_SCREENING_TYPE_2_REGISTER_2

**Description:** screening type 2 register 2, same as screening_type_2_register_0
**Address:** 0x40481548
**Offset:** 0x1548
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_7 [7:7] | VLAN_PRIORITY [6:4] | | | QUEUE_NUMBER [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_A [15:13] | | | ETHERTYPE_ENABLE [12:12] | INDEX [11:9] | | | VLAN_ENABLE [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_B [23:19] | | | | | COMPARE_A_ENABLE [18:18] | COMPARE_A [17:16] | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31 [31:31] | COMPARE_C_ENABLE [30:30] | COMPARE_C [29:25] | | | | | COMPARE_B_ENABLE [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | QUEUE_NUMBER | RW | R | 0 | 'Queue Number (0 to 15)' |
| 4:6 | VLAN_PRIORITY | RW | R | 0 | 'VLAN Priority' |
| 7 | RESERVED_7 | RW | R | 0 | 'Reserved and implemented as RW' |
| 8 | VLAN_ENABLE | RW | R | 0 | 'VLAN Enable' |
| 9:11 | INDEX | RW | R | 0 | 'Index to screener type 2 EtherType register' |
| 12 | ETHERTYPE_ENABLE | RW | R | 0 | 'EtherType Enable' |
| 13:17 | COMPARE_A | RW | R | 0 | 'Compare A - Index to screener type 2 Compare register ' |
| 18 | COMPARE_A_ENABLE | RW | R | 0 | 'Compare A Enable' |
| 19:23 | COMPARE_B | RW | R | 0 | 'Compare B - Index to screener type 2 Compare register' |
| 24 | COMPARE_B_ENABLE | RW | R | 0 | 'Compare B Enable' |
| 25:29 | COMPARE_C | RW | R | 0 | 'Compare C - Index to screener type 2 Compare register' |
| 30 | COMPARE_C_ENABLE | RW | R | 0 | 'Compare C Enable' |
| 31 | RESERVED_31 | R | R | 0 | 'Reserved, read as 0, ignored on write.' |

### 11.3.199 ETH_SCREENING_TYPE_2_REGISTER_3

**Description:** screening type 2 register 3, same as screening_type_2_register_0
**Address:** 0x4048154C
**Offset:** 0x154C
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_7 [7:7] | VLAN_PRIORITY [6:4] | | | QUEUE_NUMBER [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_A [15:13] | | | ETHERTYPE_ENABLE [12:12] | INDEX [11:9] | | | VLAN_ENABLE [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_B [23:19] | | | | | COMPARE_A_ENABLE [18:18] | COMPARE_A [17:16] | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31 [31:31] | COMPARE_C_ENABLE [30:30] | COMPARE_C [29:25] | | | | | COMPARE_B_ENABLE [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | QUEUE_NUMBER | RW | R | 0 | 'Queue Number (0 to 15)' |
| 4:6 | VLAN_PRIORITY | RW | R | 0 | 'VLAN Priority' |
| 7 | RESERVED_7 | RW | R | 0 | 'Reserved and implemented as RW' |
| 8 | VLAN_ENABLE | RW | R | 0 | 'VLAN Enable' |
| 9:11 | INDEX | RW | R | 0 | 'Index to screener type 2 EtherType register' |
| 12 | ETHERTYPE_ENABLE | RW | R | 0 | 'EtherType Enable' |
| 13:17 | COMPARE_A | RW | R | 0 | 'Compare A - Index to screener type 2 Compare register ' |
| 18 | COMPARE_A_ENABLE | RW | R | 0 | 'Compare A Enable' |
| 19:23 | COMPARE_B | RW | R | 0 | 'Compare B - Index to screener type 2 Compare register' |
| 24 | COMPARE_B_ENABLE | RW | R | 0 | 'Compare B Enable' |
| 25:29 | COMPARE_C | RW | R | 0 | 'Compare C - Index to screener type 2 Compare register' |
| 30 | COMPARE_C_ENABLE | RW | R | 0 | 'Compare C Enable' |
| 31 | RESERVED_31 | R | R | 0 | 'Reserved, read as 0, ignored on write.' |

### 11.3.200 ETH_SCREENING_TYPE_2_REGISTER_4

**Description:** screening type 2 register 4, same as screening_type_2_register_0
**Address:** 0x40481550
**Offset:** 0x1550
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_7 [7:7] | VLAN_PRIORITY [6:4] | | | QUEUE_NUMBER [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_A [15:13] | | | ETHERTYPE_ENABLE [12:12] | INDEX [11:9] | | | VLAN_ENABLE [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_B [23:19] | | | | | COMPARE_A_ENABLE [18:18] | COMPARE_A [17:16] | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31 [31:31] | COMPARE_C_ENABLE [30:30] | COMPARE_C [29:25] | | | | | COMPARE_B_ENABLE [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | QUEUE_NUMBER | RW | R | 0 | 'Queue Number (0 to 15)' |
| 4:6 | VLAN_PRIORITY | RW | R | 0 | 'VLAN Priority' |
| 7 | RESERVED_7 | RW | R | 0 | 'Reserved and implemented as RW' |
| 8 | VLAN_ENABLE | RW | R | 0 | 'VLAN Enable' |
| 9:11 | INDEX | RW | R | 0 | 'Index to screener type 2 EtherType register' |
| 12 | ETHERTYPE_ENABLE | RW | R | 0 | 'EtherType Enable' |
| 13:17 | COMPARE_A | RW | R | 0 | 'Compare A - Index to screener type 2 Compare register ' |
| 18 | COMPARE_A_ENABLE | RW | R | 0 | 'Compare A Enable' |
| 19:23 | COMPARE_B | RW | R | 0 | 'Compare B - Index to screener type 2 Compare register' |
| 24 | COMPARE_B_ENABLE | RW | R | 0 | 'Compare B Enable' |
| 25:29 | COMPARE_C | RW | R | 0 | 'Compare C - Index to screener type 2 Compare register' |
| 30 | COMPARE_C_ENABLE | RW | R | 0 | 'Compare C Enable' |
| 31 | RESERVED_31 | R | R | 0 | 'Reserved, read as 0, ignored on write.' |

### 11.3.201 ETH_SCREENING_TYPE_2_REGISTER_5

**Description:** screening type 2 register 5, same as screening_type_2_register_0
**Address:** 0x40481554
**Offset:** 0x1554
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_7 [7:7] | VLAN_PRIORITY [6:4] | | | QUEUE_NUMBER [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_A [15:13] | | | ETHERTYPE_ENABLE [12:12] | INDEX [11:9] | | | VLAN_ENABLE [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_B [23:19] | | | | | COMPARE_A_ENABLE [18:18] | COMPARE_A [17:16] | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31 [31:31] | COMPARE_C_ENABLE [30:30] | COMPARE_C [29:25] | | | | | COMPARE_B_ENABLE [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | QUEUE_NUMBER | RW | R | 0 | 'Queue Number (0 to 15)' |
| 4:6 | VLAN_PRIORITY | RW | R | 0 | 'VLAN Priority' |
| 7 | RESERVED_7 | RW | R | 0 | 'Reserved and implemented as RW' |
| 8 | VLAN_ENABLE | RW | R | 0 | 'VLAN Enable' |
| 9:11 | INDEX | RW | R | 0 | 'Index to screener type 2 EtherType register' |
| 12 | ETHERTYPE_ENABLE | RW | R | 0 | 'EtherType Enable' |
| 13:17 | COMPARE_A | RW | R | 0 | 'Compare A - Index to screener type 2 Compare register ' |
| 18 | COMPARE_A_ENABLE | RW | R | 0 | 'Compare A Enable' |
| 19:23 | COMPARE_B | RW | R | 0 | 'Compare B - Index to screener type 2 Compare register' |
| 24 | COMPARE_B_ENABLE | RW | R | 0 | 'Compare B Enable' |
| 25:29 | COMPARE_C | RW | R | 0 | 'Compare C - Index to screener type 2 Compare register' |
| 30 | COMPARE_C_ENABLE | RW | R | 0 | 'Compare C Enable' |
| 31 | RESERVED_31 | R | R | 0 | 'Reserved, read as 0, ignored on write.' |

### 11.3.202 ETH_SCREENING_TYPE_2_REGISTER_6

**Description:** screening type 2 register 6, same as screening_type_2_register_0
**Address:** 0x40481558
**Offset:** 0x1558
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_7 [7:7] | VLAN_PRIORITY [6:4] | | | QUEUE_NUMBER [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_A [15:13] | | | ETHERTYPE_ENABLE [12:12] | INDEX [11:9] | | | VLAN_ENABLE [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_B [23:19] | | | | | COMPARE_A_ENABLE [18:18] | COMPARE_A [17:16] | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31 [31:31] | COMPARE_C_ENABLE [30:30] | COMPARE_C [29:25] | | | | | COMPARE_B_ENABLE [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | QUEUE_NUMBER | RW | R | 0 | 'Queue Number (0 to 15)' |
| 4:6 | VLAN_PRIORITY | RW | R | 0 | 'VLAN Priority' |
| 7 | RESERVED_7 | RW | R | 0 | 'Reserved and implemented as RW' |
| 8 | VLAN_ENABLE | RW | R | 0 | 'VLAN Enable' |
| 9:11 | INDEX | RW | R | 0 | 'Index to screener type 2 EtherType register' |
| 12 | ETHERTYPE_ENABLE | RW | R | 0 | 'EtherType Enable' |
| 13:17 | COMPARE_A | RW | R | 0 | 'Compare A - Index to screener type 2 Compare register ' |
| 18 | COMPARE_A_ENABLE | RW | R | 0 | 'Compare A Enable' |
| 19:23 | COMPARE_B | RW | R | 0 | 'Compare B - Index to screener type 2 Compare register' |
| 24 | COMPARE_B_ENABLE | RW | R | 0 | 'Compare B Enable' |
| 25:29 | COMPARE_C | RW | R | 0 | 'Compare C - Index to screener type 2 Compare register' |
| 30 | COMPARE_C_ENABLE | RW | R | 0 | 'Compare C Enable' |
| 31 | RESERVED_31 | R | R | 0 | 'Reserved, read as 0, ignored on write.' |

### 11.3.203 ETH_SCREENING_TYPE_2_REGISTER_7

**Description:** screening type 2 register 7, same as screening_type_2_register_0
**Address:** 0x4048155C
**Offset:** 0x155C
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_7 [7:7] | VLAN_PRIORITY [6:4] | | | QUEUE_NUMBER [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_A [15:13] | | | ETHERTYPE_ENABLE [12:12] | INDEX [11:9] | | | VLAN_ENABLE [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_B [23:19] | | | | | COMPARE_A_ENABLE [18:18] | COMPARE_A [17:16] | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31 [31:31] | COMPARE_C_ENABLE [30:30] | COMPARE_C [29:25] | | | | | COMPARE_B_ENABLE [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | QUEUE_NUMBER | RW | R | 0 | 'Queue Number (0 to 15)' |
| 4:6 | VLAN_PRIORITY | RW | R | 0 | 'VLAN Priority' |
| 7 | RESERVED_7 | RW | R | 0 | 'Reserved and implemented as RW' |
| 8 | VLAN_ENABLE | RW | R | 0 | 'VLAN Enable' |
| 9:11 | INDEX | RW | R | 0 | 'Index to screener type 2 EtherType register' |
| 12 | ETHERTYPE_ENABLE | RW | R | 0 | 'EtherType Enable' |
| 13:17 | COMPARE_A | RW | R | 0 | 'Compare A - Index to screener type 2 Compare register ' |
| 18 | COMPARE_A_ENABLE | RW | R | 0 | 'Compare A Enable' |
| 19:23 | COMPARE_B | RW | R | 0 | 'Compare B - Index to screener type 2 Compare register' |
| 24 | COMPARE_B_ENABLE | RW | R | 0 | 'Compare B Enable' |
| 25:29 | COMPARE_C | RW | R | 0 | 'Compare C - Index to screener type 2 Compare register' |
| 30 | COMPARE_C_ENABLE | RW | R | 0 | 'Compare C Enable' |
| 31 | RESERVED_31 | R | R | 0 | 'Reserved, read as 0, ignored on write.' |

### 11.3.204 ETH_SCREENING_TYPE_2_REGISTER_8

**Description:** screening type 2 register 8, same as screening_type_2_register_0
**Address:** 0x40481560
**Offset:** 0x1560
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_7 [7:7] | VLAN_PRIORITY [6:4] | | | QUEUE_NUMBER [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_A [15:13] | | | ETHERTYPE_ENABLE [12:12] | INDEX [11:9] | | | VLAN_ENABLE [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_B [23:19] | | | | | COMPARE_A_ENABLE [18:18] | COMPARE_A [17:16] | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31 [31:31] | COMPARE_C_ENABLE [30:30] | COMPARE_C [29:25] | | | | | COMPARE_B_ENABLE [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | QUEUE_NUMBER | RW | R | 0 | 'Queue Number (0 to 15)' |
| 4:6 | VLAN_PRIORITY | RW | R | 0 | 'VLAN Priority' |
| 7 | RESERVED_7 | RW | R | 0 | 'Reserved and implemented as RW' |
| 8 | VLAN_ENABLE | RW | R | 0 | 'VLAN Enable' |
| 9:11 | INDEX | RW | R | 0 | 'Index to screener type 2 EtherType register' |
| 12 | ETHERTYPE_ENABLE | RW | R | 0 | 'EtherType Enable' |
| 13:17 | COMPARE_A | RW | R | 0 | 'Compare A - Index to screener type 2 Compare register ' |
| 18 | COMPARE_A_ENABLE | RW | R | 0 | 'Compare A Enable' |
| 19:23 | COMPARE_B | RW | R | 0 | 'Compare B - Index to screener type 2 Compare register' |
| 24 | COMPARE_B_ENABLE | RW | R | 0 | 'Compare B Enable' |
| 25:29 | COMPARE_C | RW | R | 0 | 'Compare C - Index to screener type 2 Compare register' |
| 30 | COMPARE_C_ENABLE | RW | R | 0 | 'Compare C Enable' |
| 31 | RESERVED_31 | R | R | 0 | 'Reserved, read as 0, ignored on write.' |

### 11.3.205 ETH_SCREENING_TYPE_2_REGISTER_9

**Description:** screening type 2 register 9, same as screening_type_2_register_0
**Address:** 0x40481564
**Offset:** 0x1564
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_7 [7:7] | VLAN_PRIORITY [6:4] | | | QUEUE_NUMBER [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_A [15:13] | | | ETHERTYPE_ENABLE [12:12] | INDEX [11:9] | | | VLAN_ENABLE [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_B [23:19] | | | | | COMPARE_A_ENABLE [18:18] | COMPARE_A [17:16] | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31 [31:31] | COMPARE_C_ENABLE [30:30] | COMPARE_C [29:25] | | | | | COMPARE_B_ENABLE [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | QUEUE_NUMBER | RW | R | 0 | 'Queue Number (0 to 15)' |
| 4:6 | VLAN_PRIORITY | RW | R | 0 | 'VLAN Priority' |
| 7 | RESERVED_7 | RW | R | 0 | 'Reserved and implemented as RW' |
| 8 | VLAN_ENABLE | RW | R | 0 | 'VLAN Enable' |
| 9:11 | INDEX | RW | R | 0 | 'Index to screener type 2 EtherType register' |
| 12 | ETHERTYPE_ENABLE | RW | R | 0 | 'EtherType Enable' |
| 13:17 | COMPARE_A | RW | R | 0 | 'Compare A - Index to screener type 2 Compare register ' |
| 18 | COMPARE_A_ENABLE | RW | R | 0 | 'Compare A Enable' |
| 19:23 | COMPARE_B | RW | R | 0 | 'Compare B - Index to screener type 2 Compare register' |
| 24 | COMPARE_B_ENABLE | RW | R | 0 | 'Compare B Enable' |
| 25:29 | COMPARE_C | RW | R | 0 | 'Compare C - Index to screener type 2 Compare register' |
| 30 | COMPARE_C_ENABLE | RW | R | 0 | 'Compare C Enable' |
| 31 | RESERVED_31 | R | R | 0 | 'Reserved, read as 0, ignored on write.' |

### 11.3.206 ETH_SCREENING_TYPE_2_REGISTER_10

**Description:** screening type 2 register 10, same as screening_type_2_register_0
**Address:** 0x40481568
**Offset:** 0x1568
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_7 [7:7] | VLAN_PRIORITY [6:4] | | | QUEUE_NUMBER [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_A [15:13] | | | ETHERTYPE_ENABLE [12:12] | INDEX [11:9] | | | VLAN_ENABLE [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_B [23:19] | | | | | COMPARE_A_ENABLE [18:18] | COMPARE_A [17:16] | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31 [31:31] | COMPARE_C_ENABLE [30:30] | COMPARE_C [29:25] | | | | | COMPARE_B_ENABLE [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | QUEUE_NUMBER | RW | R | 0 | 'Queue Number (0 to 15)' |
| 4:6 | VLAN_PRIORITY | RW | R | 0 | 'VLAN Priority' |
| 7 | RESERVED_7 | RW | R | 0 | 'Reserved and implemented as RW' |
| 8 | VLAN_ENABLE | RW | R | 0 | 'VLAN Enable' |
| 9:11 | INDEX | RW | R | 0 | 'Index to screener type 2 EtherType register' |
| 12 | ETHERTYPE_ENABLE | RW | R | 0 | 'EtherType Enable' |
| 13:17 | COMPARE_A | RW | R | 0 | 'Compare A - Index to screener type 2 Compare register ' |
| 18 | COMPARE_A_ENABLE | RW | R | 0 | 'Compare A Enable' |
| 19:23 | COMPARE_B | RW | R | 0 | 'Compare B - Index to screener type 2 Compare register' |
| 24 | COMPARE_B_ENABLE | RW | R | 0 | 'Compare B Enable' |
| 25:29 | COMPARE_C | RW | R | 0 | 'Compare C - Index to screener type 2 Compare register' |
| 30 | COMPARE_C_ENABLE | RW | R | 0 | 'Compare C Enable' |
| 31 | RESERVED_31 | R | R | 0 | 'Reserved, read as 0, ignored on write.' |

### 11.3.207 ETH_SCREENING_TYPE_2_REGISTER_11

**Description:** screening type 2 register 11, same as screening_type_2_register_0
**Address:** 0x4048156C
**Offset:** 0x156C
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_7 [7:7] | VLAN_PRIORITY [6:4] | | | QUEUE_NUMBER [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_A [15:13] | | | ETHERTYPE_ENABLE [12:12] | INDEX [11:9] | | | VLAN_ENABLE [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_B [23:19] | | | | | COMPARE_A_ENABLE [18:18] | COMPARE_A [17:16] | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31 [31:31] | COMPARE_C_ENABLE [30:30] | COMPARE_C [29:25] | | | | | COMPARE_B_ENABLE [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | QUEUE_NUMBER | RW | R | 0 | 'Queue Number (0 to 15)' |
| 4:6 | VLAN_PRIORITY | RW | R | 0 | 'VLAN Priority' |
| 7 | RESERVED_7 | RW | R | 0 | 'Reserved and implemented as RW' |
| 8 | VLAN_ENABLE | RW | R | 0 | 'VLAN Enable' |
| 9:11 | INDEX | RW | R | 0 | 'Index to screener type 2 EtherType register' |
| 12 | ETHERTYPE_ENABLE | RW | R | 0 | 'EtherType Enable' |
| 13:17 | COMPARE_A | RW | R | 0 | 'Compare A - Index to screener type 2 Compare register ' |
| 18 | COMPARE_A_ENABLE | RW | R | 0 | 'Compare A Enable' |
| 19:23 | COMPARE_B | RW | R | 0 | 'Compare B - Index to screener type 2 Compare register' |
| 24 | COMPARE_B_ENABLE | RW | R | 0 | 'Compare B Enable' |
| 25:29 | COMPARE_C | RW | R | 0 | 'Compare C - Index to screener type 2 Compare register' |
| 30 | COMPARE_C_ENABLE | RW | R | 0 | 'Compare C Enable' |
| 31 | RESERVED_31 | R | R | 0 | 'Reserved, read as 0, ignored on write.' |

### 11.3.208 ETH_SCREENING_TYPE_2_REGISTER_12

**Description:** screening type 2 register 12, same as screening_type_2_register_0
**Address:** 0x40481570
**Offset:** 0x1570
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_7 [7:7] | VLAN_PRIORITY [6:4] | | | QUEUE_NUMBER [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_A [15:13] | | | ETHERTYPE_ENABLE [12:12] | INDEX [11:9] | | | VLAN_ENABLE [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_B [23:19] | | | | | COMPARE_A_ENABLE [18:18] | COMPARE_A [17:16] | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31 [31:31] | COMPARE_C_ENABLE [30:30] | COMPARE_C [29:25] | | | | | COMPARE_B_ENABLE [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | QUEUE_NUMBER | RW | R | 0 | 'Queue Number (0 to 15)' |
| 4:6 | VLAN_PRIORITY | RW | R | 0 | 'VLAN Priority' |
| 7 | RESERVED_7 | RW | R | 0 | 'Reserved and implemented as RW' |
| 8 | VLAN_ENABLE | RW | R | 0 | 'VLAN Enable' |
| 9:11 | INDEX | RW | R | 0 | 'Index to screener type 2 EtherType register' |
| 12 | ETHERTYPE_ENABLE | RW | R | 0 | 'EtherType Enable' |
| 13:17 | COMPARE_A | RW | R | 0 | 'Compare A - Index to screener type 2 Compare register ' |
| 18 | COMPARE_A_ENABLE | RW | R | 0 | 'Compare A Enable' |
| 19:23 | COMPARE_B | RW | R | 0 | 'Compare B - Index to screener type 2 Compare register' |
| 24 | COMPARE_B_ENABLE | RW | R | 0 | 'Compare B Enable' |
| 25:29 | COMPARE_C | RW | R | 0 | 'Compare C - Index to screener type 2 Compare register' |
| 30 | COMPARE_C_ENABLE | RW | R | 0 | 'Compare C Enable' |
| 31 | RESERVED_31 | R | R | 0 | 'Reserved, read as 0, ignored on write.' |

### 11.3.209 ETH_SCREENING_TYPE_2_REGISTER_13

**Description:** screening type 2 register 13, same as screening_type_2_register_0
**Address:** 0x40481574
**Offset:** 0x1574
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_7 [7:7] | VLAN_PRIORITY [6:4] | | | QUEUE_NUMBER [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_A [15:13] | | | ETHERTYPE_ENABLE [12:12] | INDEX [11:9] | | | VLAN_ENABLE [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_B [23:19] | | | | | COMPARE_A_ENABLE [18:18] | COMPARE_A [17:16] | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31 [31:31] | COMPARE_C_ENABLE [30:30] | COMPARE_C [29:25] | | | | | COMPARE_B_ENABLE [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | QUEUE_NUMBER | RW | R | 0 | 'Queue Number (0 to 15)' |
| 4:6 | VLAN_PRIORITY | RW | R | 0 | 'VLAN Priority' |
| 7 | RESERVED_7 | RW | R | 0 | 'Reserved and implemented as RW' |
| 8 | VLAN_ENABLE | RW | R | 0 | 'VLAN Enable' |
| 9:11 | INDEX | RW | R | 0 | 'Index to screener type 2 EtherType register' |
| 12 | ETHERTYPE_ENABLE | RW | R | 0 | 'EtherType Enable' |
| 13:17 | COMPARE_A | RW | R | 0 | 'Compare A - Index to screener type 2 Compare register ' |
| 18 | COMPARE_A_ENABLE | RW | R | 0 | 'Compare A Enable' |
| 19:23 | COMPARE_B | RW | R | 0 | 'Compare B - Index to screener type 2 Compare register' |
| 24 | COMPARE_B_ENABLE | RW | R | 0 | 'Compare B Enable' |
| 25:29 | COMPARE_C | RW | R | 0 | 'Compare C - Index to screener type 2 Compare register' |
| 30 | COMPARE_C_ENABLE | RW | R | 0 | 'Compare C Enable' |
| 31 | RESERVED_31 | R | R | 0 | 'Reserved, read as 0, ignored on write.' |

### 11.3.210 ETH_SCREENING_TYPE_2_REGISTER_14

**Description:** screening type 2 register 14, same as screening_type_2_register_0
**Address:** 0x40481578
**Offset:** 0x1578
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_7 [7:7] | VLAN_PRIORITY [6:4] | | | QUEUE_NUMBER [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_A [15:13] | | | ETHERTYPE_ENABLE [12:12] | INDEX [11:9] | | | VLAN_ENABLE [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_B [23:19] | | | | | COMPARE_A_ENABLE [18:18] | COMPARE_A [17:16] | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31 [31:31] | COMPARE_C_ENABLE [30:30] | COMPARE_C [29:25] | | | | | COMPARE_B_ENABLE [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | QUEUE_NUMBER | RW | R | 0 | 'Queue Number (0 to 15)' |
| 4:6 | VLAN_PRIORITY | RW | R | 0 | 'VLAN Priority' |
| 7 | RESERVED_7 | RW | R | 0 | 'Reserved and implemented as RW' |
| 8 | VLAN_ENABLE | RW | R | 0 | 'VLAN Enable' |
| 9:11 | INDEX | RW | R | 0 | 'Index to screener type 2 EtherType register' |
| 12 | ETHERTYPE_ENABLE | RW | R | 0 | 'EtherType Enable' |
| 13:17 | COMPARE_A | RW | R | 0 | 'Compare A - Index to screener type 2 Compare register ' |
| 18 | COMPARE_A_ENABLE | RW | R | 0 | 'Compare A Enable' |
| 19:23 | COMPARE_B | RW | R | 0 | 'Compare B - Index to screener type 2 Compare register' |
| 24 | COMPARE_B_ENABLE | RW | R | 0 | 'Compare B Enable' |
| 25:29 | COMPARE_C | RW | R | 0 | 'Compare C - Index to screener type 2 Compare register' |
| 30 | COMPARE_C_ENABLE | RW | R | 0 | 'Compare C Enable' |
| 31 | RESERVED_31 | R | R | 0 | 'Reserved, read as 0, ignored on write.' |

### 11.3.211 ETH_SCREENING_TYPE_2_REGISTER_15

**Description:** screening type 2 register 15, same as screening_type_2_register_0
**Address:** 0x4048157C
**Offset:** 0x157C
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_7 [7:7] | VLAN_PRIORITY [6:4] | | | QUEUE_NUMBER [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_A [15:13] | | | ETHERTYPE_ENABLE [12:12] | INDEX [11:9] | | | VLAN_ENABLE [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_B [23:19] | | | | | COMPARE_A_ENABLE [18:18] | COMPARE_A [17:16] | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31 [31:31] | COMPARE_C_ENABLE [30:30] | COMPARE_C [29:25] | | | | | COMPARE_B_ENABLE [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | QUEUE_NUMBER | RW | R | 0 | 'Queue Number (0 to 15)' |
| 4:6 | VLAN_PRIORITY | RW | R | 0 | 'VLAN Priority' |
| 7 | RESERVED_7 | RW | R | 0 | 'Reserved and implemented as RW' |
| 8 | VLAN_ENABLE | RW | R | 0 | 'VLAN Enable' |
| 9:11 | INDEX | RW | R | 0 | 'Index to screener type 2 EtherType register' |
| 12 | ETHERTYPE_ENABLE | RW | R | 0 | 'EtherType Enable' |
| 13:17 | COMPARE_A | RW | R | 0 | 'Compare A - Index to screener type 2 Compare register ' |
| 18 | COMPARE_A_ENABLE | RW | R | 0 | 'Compare A Enable' |
| 19:23 | COMPARE_B | RW | R | 0 | 'Compare B - Index to screener type 2 Compare register' |
| 24 | COMPARE_B_ENABLE | RW | R | 0 | 'Compare B Enable' |
| 25:29 | COMPARE_C | RW | R | 0 | 'Compare C - Index to screener type 2 Compare register' |
| 30 | COMPARE_C_ENABLE | RW | R | 0 | 'Compare C Enable' |
| 31 | RESERVED_31 | R | R | 0 | 'Reserved, read as 0, ignored on write.' |

### 11.3.212 ETH_TX_SCHED_CTRL

**Description:** This register controls the transmit scheduling algorithm the user can select for each active transmit queue. By default all queues are initialized to fixed priority, with the top indexed queue having overall priority
**Address:** 0x40481580
**Offset:** 0x1580
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | TX_SCHED_Q3 [7:6] | | TX_SCHED_Q2 [5:4] | | TX_SCHED_Q1 [3:2] | | TX_SCHED_Q0 [1:0] | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_8 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_8 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_8 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:1 | TX_SCHED_Q0 | RW | | 0 | 'Queue 0 selection.<br>00 : Fixed Priority<br>01 : CBS Enabled only valid for top two enabled queues and if CBS capability selected.<br>10 : DWRR Enabled<br>11 : ETS Enabled' |
| 2:3 | TX_SCHED_Q1 | RW | | 0 | 'Queue 1 selection.<br>00 : Fixed Priority<br>01 : CBS Enabled only valid for top two enabled queues and if CBS capability selected.<br>10 : DWRR Enabled<br>11 : ETS Enabled' |
| 4:5 | TX_SCHED_Q2 | RW | | 0 | 'Queue 2 selection.<br>00 : Fixed Priority<br>01 : CBS Enabled only valid for top two enabled queues and if CBS capability selected.<br>10 : DWRR Enabled<br>11 : ETS Enabled |
| 6:7 | TX_SCHED_Q3 | R | | 0 | Write ignore, read 0 |
| 8:31 | REMOVED_31_8 | R | | 0 | Write ignore, read 0 |

### 11.3.213 ETH_BW_RATE_LIMIT_Q0TO3

**Description:** This register holds the DWRR weighting value or the ETS bandwidth percentage value used by the transmit scheduler for queues 0 to 3.
**Address:** 0x40481590
**Offset:** 0x1590
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DWRR_ETS_WEIGHT_Q0 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | DWRR_ETS_WEIGHT_Q1 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | DWRR_ETS_WEIGHT_Q2 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | DWRR_ETS_WEIGHT_Q3 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | DWRR_ETS_WEIGHT_Q0 | RW | | 0 | 'DWRR Weighting / ETS Bandwidth Allocation for queue 0' |
| 8:15 | DWRR_ETS_WEIGHT_Q1 | RW | | 0 | 'DWRR Weighting / ETS Bandwidth Allocation for queue 1' |
| 16:23 | DWRR_ETS_WEIGHT_Q2 | RW | | 0 | 'DWRR Weighting / ETS Bandwidth Allocation for queue 2' |
| 24:31 | DWRR_ETS_WEIGHT_Q3 | R | | 0 | Write ignore, read 0 |

### 11.3.214 ETH_BW_RATE_LIMIT_Q4TO7

**Description:** Not presents. MXETH has only 3 queues. Access to the register returns AHB error.
**Address:** 0x40481594
**Offset:** 0x1594
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | REMOVED_31_0 | RW | | 0 | 'DWRR Weighting / ETS Bandwidth Allocation for queue 0' |

### 11.3.215 ETH_BW_RATE_LIMIT_Q8TO11

**Description:** Not presents. MXETH has only 3 queues. Access to the register returns AHB error.
**Address:** 0x40481598
**Offset:** 0x1598
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | REMOVED_31_0 | R | R | 0 | Write ignore, read 0 |

### 11.3.216 ETH_BW_RATE_LIMIT_Q12TO15

**Description:** Not presents. MXETH has only 3 queues. Access to the register returns AHB error.
**Address:** 0x4048159C
**Offset:** 0x159C
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | REMOVED_31_0 | R | R | 0 | Write ignore, read 0 |

### 11.3.217 ETH_TX_Q_SEG_ALLOC_Q0TO7

**Description:** This register allows the user to distribute the Transmit SRAM used by the DMA across the priority queues, for queues 0 to 7. The SRAM itself is split into a number of evenly sized segments (this is defined in the verilog configuration defs file - for the configuration used to generate this register description, the total number of segments was set to '16'). Those segments can then be freely distributed across the active queues, in powers of 2. I.e. a value of 0 would mean 1 segment has been allocated to the queue. A value of 1 would mean 2 segments, a value of 2 means 4 segments and so on. The reset values of these registers are defined in the configuration defs file.

**Address:** 0x404815A0
**Offset:** 0x15A0
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x1

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_7_7 [7:7] | SEGMENT_ALLOC_Q1 [6:4] | | | RESERVED_3_3 [3:3] | SEGMENT_ALLOC_Q0 [2:0] | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_15_15 [15:15] | REMOVED_14_12 [14:12] | | | RESERVED_11_11 [11:11] | SEGMENT_ALLOC_Q2 [10:8] | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_23 [23:23] | REMOVED_22_20 [22:20] | | | RESERVED_19_19 [19:19] | REMOVED_18_16 [18:16] | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_31 [31:31] | REMOVED_30_28 [30:28] | | | RESERVED_27_27 [27:27] | REMOVED_26_24 [26:24] | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:2 | SEGMENT_ALLOC_Q0 | RW | R | 1 | Number of segments allocated to q0. This should be entered as a log 2, for example entering a value of 2 would grant 4 segments. A maximum of 32 segments can be granted. The default value is determined by `gem_tx_pbuf_num_segments_q0 |
| 3 | RESERVED_3_3 | R | R | 0 | Reserved, read as 0, ignored on write. |
| 4:6 | SEGMENT_ALLOC_Q1 | RW | R | 0 | Number of segments allocated to q1. This should be entered as a log 2, for example entering a value of 2 would grant 4 segments. A maximum of 32 segments can be granted |
| 7 | RESERVED_7_7 | R | R | 0 | Reserved, read as 0, ignored on write. |
| 8:10 | SEGMENT_ALLOC_Q2 | RW | R | 0 | Number of segments allocated to q2. This should be entered as a log 2, for example entering a value of 2 would grant 4 segments. A maximum of 32 segments can be granted |
| 11 | RESERVED_11_11 | R | R | 0 | Write ignore, read 0 |
| 12:14 | REMOVED_14_12 | R | R | 0 | Write ignore, read 0 |
| 15 | RESERVED_15_15 | R | R | 0 | Write ignore, read 0 |
| 16:18 | REMOVED_18_16 | R | R | 0 | Write ignore, read 0 |
| 19 | RESERVED_19_19 | R | R | 0 | Write ignore, read 0 |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 20:22 | REMOVED_22_20 | R | R | 0 | Write ignore, read 0 |
| 23 | RESERVED_23 | R | R | 0 | Write ignore, read 0 |
| 24:26 | REMOVED_26_24 | R | R | 0 | Write ignore, read 0 |
| 27 | RESERVED_27_27 | R | R | 0 | Write ignore, read 0 |
| 28:30 | REMOVED_30_28 | R | R | 0 | Write ignore, read 0 |
| 31 | RESERVED_31_31 | R | R | 0 | Write ignore, read 0 |

### 11.3.218 ETH_TX_Q_SEG_ALLOC_Q8TO15

**Description:** Not presents. Access to the register returns AHB error.
**Address:** 0x404815A4
**Offset:** 0x15A4
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | REMOVED_31_0 | R | R | 0 | Write ignore, read 0 |

### 11.3.219 ETH_RECEIVE_Q8_PTR

**Description:** receive_q8_ptr to receive_q15_ptr doesn't present. Access to the register returns AHB error.
**Address:** 0x404815C0
**Offset:** 0x15C0
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | REMOVED_31_0 | R | R | 0 | Write ignore, read 0 |

### 11.3.220 ETH_RECEIVE_Q15_PTR

**Description:** Not presents.
**Address:** 0x404815DC
**Offset:** 0x15DC
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | REMOVED_31_0 | R | R | 0 | Write ignore, read 0 |

### 11.3.221 ETH_DMA_RXBUF_SIZE_Q8

**Description:** dma_rxbuf_size_q8 to dma_rxbuf_size_q15 doesn't present. Access to the register returns AHB error.
**Address:** 0x404815E0
**Offset:** 0x15E0
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | REMOVED_31_0 | R | R | 0 | Write ignore, read 0 |

### 11.3.222 ETH_DMA_RXBUF_SIZE_Q15

**Description:** Not presents.
**Address:** 0x404815FC
**Offset:** 0x15FC
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | REMOVED_31_0 | R | R | 0 | Write ignore, read 0 |

### 11.3.223 ETH_INT_Q1_ENABLE

**Description:** At reset all interrupts are disabled. Writing a one to the relevant bit location enables the required interrupt. This register is write only and when read will return zero.
**Address:** 0x40481600
**Offset:** 0x1600
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | ENABLE_TRANSMIT_COMPLETE_INTERRUPT [7:7] | ENABLE_TRANSMIT_FRAME_CORRUPTION_DUE_TO_AMBA_ERROR_INTERRUPT [6:6] | ENABLE_RETRY_LIMIT_EXCEEDED_OR_LATE_COLLISION_INTERRUPT [5:5] | None [4:3] | | ENABLE_RX_USED_BIT_READ_INTERRUPT [2:2] | ENABLE_RECEIVE_COMPLETE_INTERRUPT [1:1] | None [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:12] | | | | ENABLE_RESP_NOT_OK_INTERRUPT [11:11] | None [10:8] | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 1 | ENABLE_RECEIVE_COMPLETE_INTERRUPT | W | R | 0 | Enable Receive complete interrupt |
| 2 | ENABLE_RX_USED_BIT_READ_INTERRUPT | W | R | 0 | Enable RX used bit read interrupt |
| 5 | ENABLE_RETRY_LIMIT_EXCEEDED_OR_LATE_COLLISION_INTERRUPT | W | R | 0 | Enable Retry limit exceeded or late collision interrupt |
| 6 | ENABLE_TRANSMIT_FRAME_CORRUPTION_DUE_TO_AMBA_ERROR_INTERRUPT | W | R | 0 | Enable Transmit frame corruption due to AMBA (AXI) error interrupt |
| 7 | ENABLE_TRANSMIT_COMPLETE_INTERRUPT | W | R | 0 | Enable Transmit complete interrupt |
| 11 | ENABLE_RESP_NOT_OK_INTERRUPT | W | R | 0 | Enable bresp not OK interrupt |

### 11.3.224 ETH_INT_Q2_ENABLE

**Description:** At reset all interrupts are disabled. Writing a one to the relevant bit location enables the required interrupt. This register is write only and when read will return zero.
**Address:** 0x40481604
**Offset:** 0x1604
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | ENABLE_TRANSMIT_COMPLETE_INTERRUPT [7:7] | ENABLE_TRANSMIT_FRAME_CORRUPTION_DUE_TO_AMBA_ERROR_INTERRUPT [6:6] | ENABLE_RETRY_LIMIT_EXCEEDED_OR_LATE_COLLISION_INTERRUPT [5:5] | None [4:3] | | ENABLE_RX_USED_BIT_READ_INTERRUPT [2:2] | ENABLE_RECEIVE_COMPLETE_INTERRUPT [1:1] | None [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:12] | | | | ENABLE_RESP_NOT_OK_INTERRUPT [11:11] | None [10:8] | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 1 | ENABLE_RECEIVE_COMPLETE_INTERRUPT | W | R | 0 | Enable Receive complete interrupt |
| 2 | ENABLE_RX_USED_BIT_READ_INTERRUPT | W | R | 0 | Enable RX used bit read interrupt |
| 5 | ENABLE_RETRY_LIMIT_EXCEEDED_OR_LATE_COLLISION_INTERRUPT | W | R | 0 | Enable Retry limit exceeded or late collision interrupt |
| 6 | ENABLE_TRANSMIT_FRAME_CORRUPTION_DUE_TO_AMBA_ERROR_INTERRUPT | W | R | 0 | Enable Transmit frame corruption due to AMBA (AXI) error interrupt |
| 7 | ENABLE_TRANSMIT_COMPLETE_INTERRUPT | W | R | 0 | Enable Transmit complete interrupt |
| 11 | ENABLE_RESP_NOT_OK_INTERRUPT | W | R | 0 | Enable bresp not OK interrupt |

### 11.3.225 ETH_INT_Q3_ENABLE

**Description:** int_q3_enable to int_q7_enable doesn't present. Access to the register returns AHB error.
**Address:** 0x40481608
**Offset:** 0x1608
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | REMOVED_31_0 | R | R | 0 | Write ignore, read 0 |

### 11.3.226 ETH_INT_Q7_ENABLE

**Description:** Not presents.
**Address:** 0x40481618
**Offset:** 0x1618
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | REMOVED_31_0 | R | R | 0 | Write ignore, read 0 |

### 11.3.227 ETH_INT_Q1_DISABLE

**Description:** Writing a 1 to the relevant bit location disables that particular interrupt. This register is write only and when read will return zero.
**Address:** 0x40481620
**Offset:** 0x1620
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DISABLE_TRANSMIT_COMPLETE_INTERRUPT [7:7] | DISABLE_TRANSMIT_FRAME_CORRUPTION_DUE_TO_AMBA_ERROR_INTERRUPT [6:6] | DISABLE_RETRY_LIMIT_EXCEEDED_OR_LATE_COLLISION_INTERRUPT [5:5] | None [4:3] | | DISABLE_RX_USED_BIT_READ_INTERRUPT [2:2] | DISABLE_RECEIVE_COMPLETE_INTERRUPT [1:1] | None [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:12] | | | | DISABLE_RESP_NOT_OK_INTERRUPT [11:11] | None [10:8] | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 1 | DISABLE_RECEIVE_COMPLETE_INTERRUPT | W | R | 0 | Disable Receive complete interrupt |
| 2 | DISABLE_RX_USED_BIT_READ_INTERRUPT | W | R | 0 | Disable RX used bit read interrupt |
| 5 | DISABLE_RETRY_LIMIT_EXCEEDED_OR_LATE_COLLISION_INTERRUPT | W | R | 0 | Disable Retry limit exceeded or late collision interrupt |
| 6 | DISABLE_TRANSMIT_FRAME_CORRUPTION_DUE_TO_AMBA_ERROR_INTERRUPT | W | R | 0 | Disable Transmit frame corruption due to AMBA (AXI) error interrupt |
| 7 | DISABLE_TRANSMIT_COMPLETE_INTERRUPT | W | R | 0 | Disable Transmit complete interrupt |
| 11 | DISABLE_RESP_NOT_OK_INTERRUPT | W | R | 0 | Disable bresp not OK interrupt |

### 11.3.228 ETH_INT_Q2_DISABLE

**Description:** Writing a 1 to the relevant bit location disables that particular interrupt. This register is write only and when read will return zero.
**Address:** 0x40481624
**Offset:** 0x1624
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DISABLE_TRANSMIT_COMPLETE_INTERRUPT [7:7] | DISABLE_TRANSMIT_FRAME_CORRUPTION_DUE_TO_AMBA_ERROR_INTERRUPT [6:6] | DISABLE_RETRY_LIMIT_EXCEEDED_OR_LATE_COLLISION_INTERRUPT [5:5] | None [4:3] | | DISABLE_RX_USED_BIT_READ_INTERRUPT [2:2] | DISABLE_RECEIVE_COMPLETE_INTERRUPT [1:1] | None [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:12] | | | | DISABLE_RESP_NOT_OK_INTERRUPT [11:11] | None [10:8] | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 1 | DISABLE_RECEIVE_COMPLETE_INTERRUPT | W | R | 0 | Disable Receive complete interrupt |
| 2 | DISABLE_RX_USED_BIT_READ_INTERRUPT | W | R | 0 | Disable RX used bit read interrupt |
| 5 | DISABLE_RETRY_LIMIT_EXCEEDED_OR_LATE_COLLISION_INTERRUPT | W | R | 0 | Disable Retry limit exceeded or late collision interrupt |
| 6 | DISABLE_TRANSMIT_FRAME_CORRUPTION_DUE_TO_AMBA_ERROR_INTERRUPT | W | R | 0 | Disable Transmit frame corruption due to AMBA (AXI) error interrupt |
| 7 | DISABLE_TRANSMIT_COMPLETE_INTERRUPT | W | R | 0 | Disable Transmit complete interrupt |
| 11 | DISABLE_RESP_NOT_OK_INTERRUPT | W | R | 0 | Disable bresp not OK interrupt |

### 11.3.229 ETH_INT_Q3_DISABLE

**Description:** int_q3_disable to int_q7_disable doesn't present. Access to the register returns AHB error.
**Address:** 0x40481628
**Offset:** 0x1628
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | REMOVED_31_0 | R | R | 0 | Write ignore, read 0 |

### 11.3.230 ETH_INT_Q7_DISABLE

**Description:** Not presents.
**Address:** 0x40481638
**Offset:** 0x1638
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | REMOVED_31_0 | R | R | 0 | Write ignore, read 0 |

### 11.3.231 ETH_INT_Q1_MASK

**Description:** The interrupt mask register is a read only register indicating which interrupts are masked. All bits are set at reset and can be reset individually by writing to the interrupt enable register or set individually by writing to the interrupt disable register. Having separate address locations for enable and disable saves the need for performing a read modify write when updating the interrupt mask register. For test purposes there is a write-only function to this register that allows the bits in the interrupt status register to be set or cleared, regardless of the state of the mask register.

**Address:** 0x40481640
**Offset:** 0x1640
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x8E6

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | TRANSMIT_COMPLETE_INTERRUPT_MASK [7:7] | AMBA_ERROR_INTERRUPT_MASK [6:6] | RETRY_LIMIT_EXCEEDED_OR_LATE_COLLISION_INTERRUPT_MASK [5:5] | None [4:3] | | RX_USED_INTERRUPT_MASK [2:2] | RECEIVE_COMPLETE_INTERRUPT_MASK [1:1] | None [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:12] | | | | RESP_NOT_OK_INTERRUPT_MASK [11:11] | None [10:8] | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 1 | RECEIVE_COMPLETE_INTERRUPT_MASK | R | W | 1 | receive complete interrupt mask.<br>0: Interrupt is enabled.<br>1: Interrupt is disabled.<br>A write to this register directly affects the state of the corresponding bit in the interrupt status register, causing an interrupt to be generated if a 1 is written. |
| 2 | RX_USED_INTERRUPT_MASK | R | W | 1 | A read of this register returns the value of the RX Used interrupt mask.<br>0: Interrupt is enabled.<br>1: Interrupt is disabled.<br>A write to this register directly affects the state of the corresponding bit in the interrupt status register, causing an interrupt to be generated if a 1 is written. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 5 | RETRY_LIMIT _EXCEEDED_OR_LATE_ COLLISION_INTERRUPT _MASK | R | W | 1 | retry limit exceeded or late collision interrupt mask.<br>0: Interrupt is enabled.<br>1: Interrupt is disabled.<br>A write to this register directly affects the state of the corresponding bit in the interrupt status register, causing an interrupt to be generated if a 1 is written. |
| 6 | AMBA_ERROR _INTERRUPT_MASK | R | W | 1 | A read of this register returns the value of the AMBA (AXI) error interrupt mask.<br>0: Interrupt is enabled.<br>1: Interrupt is disabled.<br>A write to this register directly affects the state of the corresponding bit in the interrupt status register, causing an interrupt to be generated if a 1 is written. |
| 7 | TRANSMIT_COMPLETE _INTERRUPT_MASK | R | W | 1 | transmit complete interrupt mask.<br>0: Interrupt is enabled.<br>1: Interrupt is disabled.<br>A write to this register directly affects the state of the corresponding bit in the interrupt status register, causing an interrupt to be generated if a 1 is written. |
| 11 | RESP_NOT_OK _INTERRUPT_MASK | R | W | 1 | bresp not OK interrupt mask.<br>0: Interrupt is enabled.<br>1: Interrupt is disabled.<br>A write to this register directly affects the state of the corresponding bit in the interrupt status register, causing an interrupt to be generated if a 1 is written. |

### 11.3.232 ETH_INT_Q2_MASK

**Description:** The interrupt mask register is a read only register indicating which interrupts are masked. All bits are set at reset and can be reset individually by writing to the interrupt enable register or set individually by writing to the interrupt disable register. Having separate address locations for enable and disable saves the need for performing a read modify write when updating the interrupt mask register. For test purposes there is a write-only function to this register that allows the bits in the interrupt status register to be set or cleared, regardless of the state of the mask register.

**Address:** 0x40481644
**Offset:** 0x1644
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x8E6

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | TRANSMIT_COMPLETE_INTERRUPT_MASK [7:7] | AMBA_ERROR_INTERRUPT_MASK [6:6] | RETRY_LIMIT_EXCEEDED_OR_LATE_COLLISION_INTERRUPT_MASK [5:5] | None [4:3] | | RX_USED_INTERRUPT_MASK [2:2] | RECEIVE_COMPLETE_INTERRUPT_MASK [1:1] | None [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:12] | | | | RESP_NOT_OK_INTERRUPT_MASK [11:11] | None [10:8] | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 1 | RECEIVE_COMPLETE_INTERRUPT_MASK | R | W | 1 | receive complete interrupt mask.<br>0: Interrupt is enabled.<br>1: Interrupt is disabled.<br>A write to this register directly affects the state of the corresponding bit in the interrupt status register, causing an interrupt to be generated if a 1 is written. |
| 2 | RX_USED_INTERRUPT_MASK | R | W | 1 | A read of this register returns the value of the RX Used interrupt mask.<br>0: Interrupt is enabled.<br>1: Interrupt is disabled.<br>A write to this register directly affects the state of the corresponding bit in the interrupt status register, causing an interrupt to be generated if a 1 is written. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 5 | RETRY_LIMIT _EXCEEDED_OR_LATE_ COLLISION_INTERRUPT _MASK | R | W | 1 | retry limit exceeded or late collision interrupt mask.<br>0: Interrupt is enabled.<br>1: Interrupt is disabled.<br>A write to this register directly affects the state of the corresponding bit in the interrupt status register, causing an interrupt to be generated if a 1 is written. |
| 6 | AMBA_ERROR _INTERRUPT_MASK | R | W | 1 | A read of this register returns the value of the AMBA (AXI) error interrupt mask.<br>0: Interrupt is enabled.<br>1: Interrupt is disabled.<br>A write to this register directly affects the state of the corresponding bit in the interrupt status register, causing an interrupt to be generated if a 1 is written. |
| 7 | TRANSMIT_COMPLETE _INTERRUPT_MASK | R | W | 1 | transmit complete interrupt mask.<br>0: Interrupt is enabled.<br>1: Interrupt is disabled.<br>A write to this register directly affects the state of the corresponding bit in the interrupt status register, causing an interrupt to be generated if a 1 is written. |
| 11 | RESP_NOT_OK _INTERRUPT_MASK | R | W | 1 | bresp not OK interrupt mask.<br>0: Interrupt is enabled.<br>1: Interrupt is disabled.<br>A write to this register directly affects the state of the corresponding bit in the interrupt status register, causing an interrupt to be generated if a 1 is written. |

### 11.3.233 ETH_INT_Q3_MASK

**Description:** int_q3_mask to int_q7_mask doesn't present. Access to the register returns AHB error.
**Address:** 0x40481648
**Offset:** 0x1648
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | REMOVED_31_0 | R | R | 0 | Write ignore, read 0 |

### 11.3.234 ETH_INT_Q7_MASK

**Description:** Not presents.
**Address:** 0x40481658
**Offset:** 0x1658
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | REMOVED_31_0 | R | R | 0 | Write ignore, read 0 |

### 11.3.235 ETH_INT_Q8_ENABLE

**Description:** int_q8_enable to int_q15_enable doesn't present. Access to the register returns AHB error.
**Address:** 0x40481660
**Offset:** 0x1660
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | REMOVED_31_0 | R | R | 0 | Write ignore, read 0 |

### 11.3.236 ETH_INT_Q15_ENABLE

**Description:** Not presents.
**Address:** 0x4048167C
**Offset:** 0x167C
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | REMOVED_31_0 | R | R | 0 | Write ignore, read 0 |

### 11.3.237 ETH_INT_Q8_DISABLE

**Description:** int_q8_disable to int_q15_disable doesn't present. Access to the register returns AHB error.
**Address:** 0x40481680
**Offset:** 0x1680
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | REMOVED_31_0 | R | R | 0 | Write ignore, read 0 |

### 11.3.238 ETH_INT_Q15_DISABLE

**Description:** Not presents.
**Address:** 0x4048169C
**Offset:** 0x169C
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | REMOVED_31_0 | R | R | 0 | Write ignore, read 0 |

### 11.3.239 ETH_INT_Q8_MASK

**Description:** int_q8_mask to int_q15_mask doesn't present. Access to the register returns AHB error.
**Address:** 0x404816A0
**Offset:** 0x16A0
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | REMOVED_31_0 | R | R | 0 | Write ignore, read 0 |

### 11.3.240 ETH_INT_Q15_MASK

**Description:** Not presents.
**Address:** 0x404816BC
**Offset:** 0x16BC
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | REMOVED_31_0 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | REMOVED_31_0 | R | R | 0 | Write ignore, read 0 |

### 11.3.241 ETH_SCREENING_TYPE_2_ETHERTYPE_REG_0

**Description:** Ethertype Register
**Address:** 0x404816E0
**Offset:** 0x16E0
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_16 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_16 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | COMPARE_VALUE | RW | R | 0 | 'EtherType compare value' |
| 16:31 | RESERVED_31_16 | R | R | 0 | 'Reserved, read as 0, ignored on write ' |

### 11.3.242 ETH_SCREENING_TYPE_2_ETHERTYPE_REG_1

**Description:** Ethertype Register
**Address:** 0x404816E4
**Offset:** 0x16E4
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_16 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_16 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | COMPARE_VALUE | RW | R | 0 | 'EtherType compare value' |
| 16:31 | RESERVED_31_16 | R | R | 0 | 'Reserved, read as 0, ignored on write ' |

### 11.3.243 ETH_SCREENING_TYPE_2_ETHERTYPE_REG_2

**Description:** Ethertype Register
**Address:** 0x404816E8
**Offset:** 0x16E8
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_16 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_16 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | COMPARE_VALUE | RW | R | 0 | 'EtherType compare value' |
| 16:31 | RESERVED_31_16 | R | R | 0 | 'Reserved, read as 0, ignored on write ' |

### 11.3.244 ETH_SCREENING_TYPE_2_ETHERTYPE_REG_3

**Description:** Ethertype Register
**Address:** 0x404816EC
**Offset:** 0x16EC
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_16 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_16 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | COMPARE_VALUE | RW | R | 0 | 'EtherType compare value' |
| 16:31 | RESERVED_31_16 | R | R | 0 | 'Reserved, read as 0, ignored on write ' |

### 11.3.245 ETH_SCREENING_TYPE_2_ETHERTYPE_REG_4

**Description:** Ethertype Register
**Address:** 0x404816F0
**Offset:** 0x16F0
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_16 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_16 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | COMPARE_VALUE | RW | R | 0 | 'EtherType compare value' |
| 16:31 | RESERVED_31_16 | R | R | 0 | 'Reserved, read as 0, ignored on write ' |

### 11.3.246 ETH_SCREENING_TYPE_2_ETHERTYPE_REG_5

**Description:** Ethertype Register
**Address:** 0x404816F4
**Offset:** 0x16F4
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_16 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_16 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | COMPARE_VALUE | RW | R | 0 | 'EtherType compare value' |
| 16:31 | RESERVED_31_16 | R | R | 0 | 'Reserved, read as 0, ignored on write ' |

### 11.3.247 ETH_SCREENING_TYPE_2_ETHERTYPE_REG_6

**Description:** Ethertype Register
**Address:** 0x404816F8
**Offset:** 0x16F8
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_16 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_16 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | COMPARE_VALUE | RW | R | 0 | 'EtherType compare value' |
| 16:31 | RESERVED_31_16 | R | R | 0 | 'Reserved, read as 0, ignored on write ' |

### 11.3.248 ETH_SCREENING_TYPE_2_ETHERTYPE_REG_7

**Description:** Ethertype Register
**Address:** 0x404816FC
**Offset:** 0x16FC
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_16 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_16 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | COMPARE_VALUE | RW | R | 0 | 'EtherType compare value' |
| 16:31 | RESERVED_31_16 | R | R | 0 | 'Reserved, read as 0, ignored on write ' |

### 11.3.249 ETH_TYPE2_COMPARE_0_WORD_0

**Description:** 'Compare A, B and C fields of the screener type 2 match register are pointers to a pool of up to 32 compare registers. If enabled the compare is true if the data at the OFFSET into the frame, ANDed with the MASK Value if the mask is enabled, is equal to the COMPARE Value. Either a 16 bit comparison or a 32 bit comparison is done. This selection is made via the associated compare word1 register bit 9. If a 16 bit comparison is selected, then a 16 bit mask is also available to the user to select which bits should be compared. If the 32 bit compare option is selected, then no mask is available. The byte at the OFFSET number of bytes from the index start is compared thru bits 7 to 0 of the configured VALUE. The byte at the OFFSET number of bytes + 1 from the index start is compared thru bits 15 to 8 of the configured VALUE and so on. The OFFSET can be configured to be from 0 to 127 bytes from either the start of the frame, the byte following the therType field (last EtherType in the header if the frame is VLAN tagged), the byte following the IP header (IPv4 or IPv6) or from the byte following the start of the TCP/UDP header. The required number of Type 2 screening registers up to a maximum of 32 is configurable in the gem defines file and have been allocated APB address space between 0x700 and 0x7fc. Note. when using RX Partial Store and Forward mode and priority queues, the frame offset must be less than the Partial Store and Forward watermark. If the offset is higher than the watermark value it's not possible to identify the priority queue before the frame is sent to the AMBA interface, and an incorrect priority queue may be used. '

**Address:** 0x40481700

**Offset:** 0x1700

**Retention:** Not Retained

**IsDeepSleep:** No

**Comment:**

**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | MASK_VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | MASK_VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_VALUE_TYPE2 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_VALUE_TYPE2 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | MASK_VALUE | RW | R | 0 | These bits can be either a 2 byte mask field or an additional 2 byte Compare Value.<br>If bit 9 of the associated compare_word1 register is set, then the byte stored in bits [7:0] is compared against the byte in the received frame from the selected offset+0 and the byte stored in bits [15:8] is compared against the byte in the received frame from the selected offset+1.<br>If bit 9 of the associated compare_word1 register is clear, these bits become a direct 2-byte mask for the 2-byte compare register in bits [31:16]. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 16:31 | COMPARE_VALUE_TYPE2 | RW | R | 0 | 2 byte Compare Value.<br>If bit 9 of the associated compare_word1 register is set, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+2 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+3.<br>If bit 9 of the associated compare_word1 register is clear, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+0 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+1. |

### 11.3.250 ETH_TYPE2_COMPARE_0_WORD_1

**Description:** 'Type2 Compare Word 1'
**Address:** 0x40481704
**Offset:** 0x1704
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_OFFSET [7:7] | OFFSET_VALUE [6:0] | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_10 [15:10] | | | | | | DISABLE_MASK [9:9] | COMPARE_OFFSET [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_10 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_10 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:6 | OFFSET_VALUE | RW | R | 0 | 'Offset value in bytes' |
| 7:8 | COMPARE_OFFSET | RW | R | 0 | 'Compare byte offset.<br>00 : Offset from beginning of the frame.<br>01 : Offset from byte after Ether Type.<br>10 : Offset from byte following end of IP header.<br>11 : Offset from byte following end of TCP/UDP header'<br><br>If bit 9 of the associated compare_word1 register is set, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+2 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+3.<br>If bit 9 of the associated compare_word1 register is clear, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+0 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+1. |
| 9 | DISABLE_MASK | RW | R | 0 | 'This bit is used to control whether the compare register word_0 contains a 4-byte compare value, or a 2-byte compare value with a 2-byte mask value.<br>1 - 4-byte compare value<br>0 - 2-byte compare, 2-byte mask ' |
| 10:31 | RESERVED_31_10 | R | R | 0 | 'Reserved, read as 0, ignored on write.' |

### 11.3.251 ETH_TYPE2_COMPARE_1_WORD_0

**Description:** same as type2_compare_0_word_0
**Address:** 0x40481708
**Offset:** 0x1708
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | MASK_VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | MASK_VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_VALUE_TYPE2 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_VALUE_TYPE2 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | MASK_VALUE | RW | R | 0 | These bits can be either a 2 byte mask field or an additional 2 byte Compare Value.<br>If bit 9 of the associated compare_word1 register is set, then the byte stored in bits [7:0] is compared against the byte in the received frame from the selected offset+0 and the byte stored in bits [15:8] is compared against the byte in the received frame from the selected offset+1.<br>If bit 9 of the associated compare_word1 register is clear, these bits become a direct 2-byte mask for the 2-byte compare register in bits [31:16]. |
| 16:31 | COMPARE_VALUE_TYPE2 | RW | R | 0 | 2 byte Compare Value.<br>If bit 9 of the associated compare_word1 register is set, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+2 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+3.<br>If bit 9 of the associated compare_word1 register is clear, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+0 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+1. |

### 11.3.252 ETH_TYPE2_COMPARE_1_WORD_1

**Description:** same as type2_compare_0_word_1
**Address:** 0x4048170C
**Offset:** 0x170C
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_OFFSET [7:7] | OFFSET_VALUE [6:0] | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_10 [15:10] | | | | | | DISABLE_MASK [9:9] | COMPARE_OFFSET [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_10 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_10 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:6 | OFFSET_VALUE | RW | R | 0 | 'Offset value in bytes' |
| 7:8 | COMPARE_OFFSET | RW | R | 0 | 'Compare byte offset.<br>00 : Offset from beginning of the frame.<br>01 : Offset from byte after Ether Type.<br>10 : Offset from byte following end of IP header.<br>11 : Offset from byte following end of TCP/UDP header'<br><br>If bit 9 of the associated compare_word1 register is set, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+2 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+3.<br>If bit 9 of the associated compare_word1 register is clear, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+0 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+1. |
| 9 | DISABLE_MASK | RW | R | 0 | 'This bit is used to control whether the compare register word_0 contains a 4-byte compare value, or a 2-byte compare value with a 2-byte mask value.<br>1 - 4-byte compare value<br>0 - 2-byte compare, 2-byte mask ' |
| 10:31 | RESERVED_31_10 | R | R | 0 | 'Reserved, read as 0, ignored on write.' |

### 11.3.253 ETH_TYPE2_COMPARE_2_WORD_0

**Description:** same as type2_compare_0_word_0
**Address:** 0x40481710
**Offset:** 0x1710
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | MASK_VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | MASK_VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_VALUE_TYPE2 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_VALUE_TYPE2 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | MASK_VALUE | RW | R | 0 | These bits can be either a 2 byte mask field or an additional 2 byte Compare Value.<br>If bit 9 of the associated compare_word1 register is set, then the byte stored in bits [7:0] is compared against the byte in the received frame from the selected offset+0 and the byte stored in bits [15:8] is compared against the byte in the received frame from the selected offset+1.<br>If bit 9 of the associated compare_word1 register is clear, these bits become a direct 2-byte mask for the 2-byte compare register in bits [31:16]. |
| 16:31 | COMPARE_VALUE_TYPE2 | RW | R | 0 | 2 byte Compare Value.<br>If bit 9 of the associated compare_word1 register is set, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+2 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+3.<br>If bit 9 of the associated compare_word1 register is clear, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+0 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+1. |

### 11.3.254 ETH_TYPE2_COMPARE_2_WORD_1

**Description:** same as type2_compare_0_word_1
**Address:** 0x40481714
**Offset:** 0x1714
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_OFFSET [7:7] | OFFSET_VALUE [6:0] | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_10 [15:10] | | | | | | DISABLE_MASK [9:9] | COMPARE_OFFSET [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_10 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_10 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:6 | OFFSET_VALUE | RW | R | 0 | 'Offset value in bytes' |
| 7:8 | COMPARE_OFFSET | RW | R | 0 | 'Compare byte offset.<br>00 : Offset from beginning of the frame.<br>01 : Offset from byte after Ether Type.<br>10 : Offset from byte following end of IP header.<br>11 : Offset from byte following end of TCP/UDP header'<br><br>If bit 9 of the associated compare_word1 register is set, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+2 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+3.<br>If bit 9 of the associated compare_word1 register is clear, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+0 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+1. |
| 9 | DISABLE_MASK | RW | R | 0 | 'This bit is used to control whether the compare register word_0 contains a 4-byte compare value, or a 2-byte compare value with a 2-byte mask value.<br>1 - 4-byte compare value<br>0 - 2-byte compare, 2-byte mask ' |
| 10:31 | RESERVED_31_10 | R | R | 0 | 'Reserved, read as 0, ignored on write.' |

### 11.3.255 ETH_TYPE2_COMPARE_3_WORD_0

**Description:** same as type2_compare_0_word_0
**Address:** 0x40481718
**Offset:** 0x1718
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | MASK_VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | MASK_VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_VALUE_TYPE2 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_VALUE_TYPE2 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | MASK_VALUE | RW | R | 0 | These bits can be either a 2 byte mask field or an additional 2 byte Compare Value.<br>If bit 9 of the associated compare_word1 register is set, then the byte stored in bits [7:0] is compared against the byte in the received frame from the selected offset+0 and the byte stored in bits [15:8] is compared against the byte in the received frame from the selected offset+1.<br>If bit 9 of the associated compare_word1 register is clear, these bits become a direct 2-byte mask for the 2-byte compare register in bits [31:16]. |
| 16:31 | COMPARE_VALUE_TYPE2 | RW | R | 0 | 2 byte Compare Value.<br>If bit 9 of the associated compare_word1 register is set, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+2 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+3.<br>If bit 9 of the associated compare_word1 register is clear, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+0 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+1. |

### 11.3.256 ETH_TYPE2_COMPARE_3_WORD_1

**Description:** same as type2_compare_0_word_1
**Address:** 0x4048171C
**Offset:** 0x171C
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_OFFSET [7:7] | OFFSET_VALUE [6:0] | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_10 [15:10] | | | | | | DISABLE_MASK [9:9] | COMPARE_OFFSET [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_10 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_10 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:6 | OFFSET_VALUE | RW | R | 0 | 'Offset value in bytes' |
| 7:8 | COMPARE_OFFSET | RW | R | 0 | 'Compare byte offset.<br>00 : Offset from beginning of the frame.<br>01 : Offset from byte after Ether Type.<br>10 : Offset from byte following end of IP header.<br>11 : Offset from byte following end of TCP/UDP header'<br><br>If bit 9 of the associated compare_word1 register is set, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+2 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+3.<br>If bit 9 of the associated compare_word1 register is clear, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+0 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+1. |
| 9 | DISABLE_MASK | RW | R | 0 | 'This bit is used to control whether the compare register word_0 contains a 4-byte compare value, or a 2-byte compare value with a 2-byte mask value.<br>1 - 4-byte compare value<br>0 - 2-byte compare, 2-byte mask ' |
| 10:31 | RESERVED_31_10 | R | R | 0 | 'Reserved, read as 0, ignored on write.' |

### 11.3.257 ETH_TYPE2_COMPARE_4_WORD_0

**Description:** same as type2_compare_0_word_0
**Address:** 0x40481720
**Offset:** 0x1720
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | MASK_VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | MASK_VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_VALUE_TYPE2 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_VALUE_TYPE2 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | MASK_VALUE | RW | R | 0 | These bits can be either a 2 byte mask field or an additional 2 byte Compare Value.<br>If bit 9 of the associated compare_word1 register is set, then the byte stored in bits [7:0] is compared against the byte in the received frame from the selected offset+0 and the byte stored in bits [15:8] is compared against the byte in the received frame from the selected offset+1.<br>If bit 9 of the associated compare_word1 register is clear, these bits become a direct 2-byte mask for the 2-byte compare register in bits [31:16]. |
| 16:31 | COMPARE_VALUE _TYPE2 | RW | R | 0 | 2 byte Compare Value.<br>If bit 9 of the associated compare_word1 register is set, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+2 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+3.<br>If bit 9 of the associated compare_word1 register is clear, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+0 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+1. |

### 11.3.258 ETH_TYPE2_COMPARE_4_WORD_1

**Description:** same as type2_compare_0_word_1
**Address:** 0x40481724
**Offset:** 0x1724
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_OFFSET [7:7] | OFFSET_VALUE [6:0] | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_10 [15:10] | | | | | | DISABLE_MASK [9:9] | COMPARE_OFFSET [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_10 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_10 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:6 | OFFSET_VALUE | RW | R | 0 | 'Offset value in bytes' |
| 7:8 | COMPARE_OFFSET | RW | R | 0 | 'Compare byte offset.<br>00 : Offset from beginning of the frame.<br>01 : Offset from byte after Ether Type.<br>10 : Offset from byte following end of IP header.<br>11 : Offset from byte following end of TCP/UDP header'<br><br>If bit 9 of the associated compare_word1 register is set, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+2 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+3.<br>If bit 9 of the associated compare_word1 register is clear, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+0 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+1. |
| 9 | DISABLE_MASK | RW | R | 0 | 'This bit is used to control whether the compare register word_0 contains a 4-byte compare value, or a 2-byte compare value with a 2-byte mask value.<br>1 - 4-byte compare value<br>0 - 2-byte compare, 2-byte mask ' |
| 10:31 | RESERVED_31_10 | R | R | 0 | 'Reserved, read as 0, ignored on write.' |

### 11.3.259 ETH_TYPE2_COMPARE_5_WORD_0

**Description:** same as type2_compare_0_word_0
**Address:** 0x40481728
**Offset:** 0x1728
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | MASK_VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | MASK_VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_VALUE_TYPE2 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_VALUE_TYPE2 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | MASK_VALUE | RW | R | 0 | These bits can be either a 2 byte mask field or an additional 2 byte Compare Value.<br>If bit 9 of the associated compare_word1 register is set, then the byte stored in bits [7:0] is compared against the byte in the received frame from the selected offset+0 and the byte stored in bits [15:8] is compared against the byte in the received frame from the selected offset+1.<br>If bit 9 of the associated compare_word1 register is clear, these bits become a direct 2-byte mask for the 2-byte compare register in bits [31:16]. |
| 16:31 | COMPARE_VALUE_TYPE2 | RW | R | 0 | 2 byte Compare Value.<br>If bit 9 of the associated compare_word1 register is set, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+2 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+3.<br>If bit 9 of the associated compare_word1 register is clear, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+0 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+1. |

### 11.3.260 ETH_TYPE2_COMPARE_5_WORD_1

**Description:** same as type2_compare_0_word_1
**Address:** 0x4048172C
**Offset:** 0x172C
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_OFFSET [7:7] | OFFSET_VALUE [6:0] | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_10 [15:10] | | | | | | DISABLE_MASK [9:9] | COMPARE_OFFSET [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_10 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_10 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:6 | OFFSET_VALUE | RW | R | 0 | 'Offset value in bytes' |
| 7:8 | COMPARE_OFFSET | RW | R | 0 | 'Compare byte offset.<br>00 : Offset from beginning of the frame.<br>01 : Offset from byte after Ether Type.<br>10 : Offset from byte following end of IP header.<br>11 : Offset from byte following end of TCP/UDP header'<br><br>If bit 9 of the associated compare_word1 register is set, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+2 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+3.<br>If bit 9 of the associated compare_word1 register is clear, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+0 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+1. |
| 9 | DISABLE_MASK | RW | R | 0 | 'This bit is used to control whether the compare register word_0 contains a 4-byte compare value, or a 2-byte compare value with a 2-byte mask value.<br>1 - 4-byte compare value<br>0 - 2-byte compare, 2-byte mask ' |
| 10:31 | RESERVED_31_10 | R | R | 0 | 'Reserved, read as 0, ignored on write.' |

### 11.3.261 ETH_TYPE2_COMPARE_6_WORD_0

**Description:** same as type2_compare_0_word_0
**Address:** 0x40481730
**Offset:** 0x1730
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | MASK_VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | MASK_VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_VALUE_TYPE2 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_VALUE_TYPE2 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | MASK_VALUE | RW | R | 0 | These bits can be either a 2 byte mask field or an additional 2 byte Compare Value.<br>If bit 9 of the associated compare_word1 register is set, then the byte stored in bits [7:0] is compared against the byte in the received frame from the selected offset+0 and the byte stored in bits [15:8] is compared against the byte in the received frame from the selected offset+1.<br>If bit 9 of the associated compare_word1 register is clear, these bits become a direct 2-byte mask for the 2-byte compare register in bits [31:16]. |
| 16:31 | COMPARE_VALUE_TYPE2 | RW | R | 0 | 2 byte Compare Value.<br>If bit 9 of the associated compare_word1 register is set, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+2 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+3.<br>If bit 9 of the associated compare_word1 register is clear, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+0 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+1. |

### 11.3.262 ETH_TYPE2_COMPARE_6_WORD_1

**Description:** same as type2_compare_0_word_1
**Address:** 0x40481734
**Offset:** 0x1734
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_OFFSET [7:7] | OFFSET_VALUE [6:0] | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_10 [15:10] | | | | | | DISABLE_MASK [9:9] | COMPARE_OFFSET [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_10 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_10 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:6 | OFFSET_VALUE | RW | R | 0 | 'Offset value in bytes' |
| 7:8 | COMPARE_OFFSET | RW | R | 0 | 'Compare byte offset.<br>00 : Offset from beginning of the frame.<br>01 : Offset from byte after Ether Type.<br>10 : Offset from byte following end of IP header.<br>11 : Offset from byte following end of TCP/UDP header'<br><br>If bit 9 of the associated compare_word1 register is set, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+2 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+3.<br>If bit 9 of the associated compare_word1 register is clear, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+0 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+1. |
| 9 | DISABLE_MASK | RW | R | 0 | 'This bit is used to control whether the compare register word_0 contains a 4-byte compare value, or a 2-byte compare value with a 2-byte mask value.<br>1 - 4-byte compare value<br>0 - 2-byte compare, 2-byte mask ' |
| 10:31 | RESERVED_31_10 | R | R | 0 | 'Reserved, read as 0, ignored on write.' |

### 11.3.263 ETH_TYPE2_COMPARE_7_WORD_0

**Description:** same as type2_compare_0_word_0
**Address:** 0x40481738
**Offset:** 0x1738
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | MASK_VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | MASK_VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_VALUE_TYPE2 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_VALUE_TYPE2 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | MASK_VALUE | RW | R | 0 | These bits can be either a 2 byte mask field or an additional 2 byte Compare Value.<br>If bit 9 of the associated compare_word1 register is set, then the byte stored in bits [7:0] is compared against the byte in the received frame from the selected offset+0 and the byte stored in bits [15:8] is compared against the byte in the received frame from the selected offset+1.<br>If bit 9 of the associated compare_word1 register is clear, these bits become a direct 2-byte mask for the 2-byte compare register in bits [31:16]. |
| 16:31 | COMPARE_VALUE_TYPE2 | RW | R | 0 | 2 byte Compare Value.<br>If bit 9 of the associated compare_word1 register is set, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+2 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+3.<br>If bit 9 of the associated compare_word1 register is clear, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+0 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+1. |

### 11.3.264 ETH_TYPE2_COMPARE_7_WORD_1

**Description:** same as type2_compare_0_word_1
**Address:** 0x4048173C
**Offset:** 0x173C
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_OFFSET [7:7] | OFFSET_VALUE [6:0] | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_10 [15:10] | | | | | | DISABLE_MASK [9:9] | COMPARE_OFFSET [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_10 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_10 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:6 | OFFSET_VALUE | RW | R | 0 | 'Offset value in bytes' |
| 7:8 | COMPARE_OFFSET | RW | R | 0 | 'Compare byte offset.<br>00 : Offset from beginning of the frame.<br>01 : Offset from byte after Ether Type.<br>10 : Offset from byte following end of IP header.<br>11 : Offset from byte following end of TCP/UDP header'<br><br>If bit 9 of the associated compare_word1 register is set, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+2 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+3.<br>If bit 9 of the associated compare_word1 register is clear, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+0 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+1. |
| 9 | DISABLE_MASK | RW | R | 0 | 'This bit is used to control whether the compare register word_0 contains a 4-byte compare value, or a 2-byte compare value with a 2-byte mask value.<br>1 - 4-byte compare value<br>0 - 2-byte compare, 2-byte mask ' |
| 10:31 | RESERVED_31_10 | R | R | 0 | 'Reserved, read as 0, ignored on write.' |

### 11.3.265 ETH_TYPE2_COMPARE_8_WORD_0

**Description:** same as type2_compare_0_word_0
**Address:** 0x40481740
**Offset:** 0x1740
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | MASK_VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | MASK_VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_VALUE_TYPE2 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_VALUE_TYPE2 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | MASK_VALUE | RW | R | 0 | These bits can be either a 2 byte mask field or an additional 2 byte Compare Value.<br>If bit 9 of the associated compare_word1 register is set, then the byte stored in bits [7:0] is compared against the byte in the received frame from the selected offset+0 and the byte stored in bits [15:8] is compared against the byte in the received frame from the selected offset+1.<br>If bit 9 of the associated compare_word1 register is clear, these bits become a direct 2-byte mask for the 2-byte compare register in bits [31:16]. |
| 16:31 | COMPARE_VALUE_TYPE2 | RW | R | 0 | 2 byte Compare Value.<br>If bit 9 of the associated compare_word1 register is set, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+2 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+3.<br>If bit 9 of the associated compare_word1 register is clear, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+0 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+1. |

### 11.3.266 ETH_TYPE2_COMPARE_8_WORD_1

**Description:** same as type2_compare_0_word_1
**Address:** 0x40481744
**Offset:** 0x1744
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_OFFSET [7:7] | OFFSET_VALUE [6:0] | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_10 [15:10] | | | | | | DISABLE_MASK [9:9] | COMPARE_OFFSET [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_10 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_10 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:6 | OFFSET_VALUE | RW | R | 0 | 'Offset value in bytes' |
| 7:8 | COMPARE_OFFSET | RW | R | 0 | 'Compare byte offset.<br>00 : Offset from beginning of the frame.<br>01 : Offset from byte after Ether Type.<br>10 : Offset from byte following end of IP header.<br>11 : Offset from byte following end of TCP/UDP header'<br><br>If bit 9 of the associated compare_word1 register is set, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+2 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+3.<br>If bit 9 of the associated compare_word1 register is clear, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+0 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+1. |
| 9 | DISABLE_MASK | RW | R | 0 | 'This bit is used to control whether the compare register word_0 contains a 4-byte compare value, or a 2-byte compare value with a 2-byte mask value.<br>1 - 4-byte compare value<br>0 - 2-byte compare, 2-byte mask ' |
| 10:31 | RESERVED_31_10 | R | R | 0 | 'Reserved, read as 0, ignored on write.' |

### 11.3.267 ETH_TYPE2_COMPARE_9_WORD_0

**Description:** same as type2_compare_0_word_0
**Address:** 0x40481748
**Offset:** 0x1748
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | MASK_VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | MASK_VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_VALUE_TYPE2 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_VALUE_TYPE2 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | MASK_VALUE | RW | R | 0 | These bits can be either a 2 byte mask field or an additional 2 byte Compare Value.<br>If bit 9 of the associated compare_word1 register is set, then the byte stored in bits [7:0] is compared against the byte in the received frame from the selected offset+0 and the byte stored in bits [15:8] is compared against the byte in the received frame from the selected offset+1.<br>If bit 9 of the associated compare_word1 register is clear, these bits become a direct 2-byte mask for the 2-byte compare register in bits [31:16]. |
| 16:31 | COMPARE_VALUE_TYPE2 | RW | R | 0 | 2 byte Compare Value.<br>If bit 9 of the associated compare_word1 register is set, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+2 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+3.<br>If bit 9 of the associated compare_word1 register is clear, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+0 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+1. |

### 11.3.268 ETH_TYPE2_COMPARE_9_WORD_1

**Description:** same as type2_compare_0_word_1
**Address:** 0x4048174C
**Offset:** 0x174C
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_OFFSET [7:7] | OFFSET_VALUE [6:0] | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_10 [15:10] | | | | | | DISABLE_MASK [9:9] | COMPARE_OFFSET [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_10 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_10 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:6 | OFFSET_VALUE | RW | R | 0 | 'Offset value in bytes' |
| 7:8 | COMPARE_OFFSET | RW | R | 0 | 'Compare byte offset.<br>00 : Offset from beginning of the frame.<br>01 : Offset from byte after Ether Type.<br>10 : Offset from byte following end of IP header.<br>11 : Offset from byte following end of TCP/UDP header'<br><br>If bit 9 of the associated compare_word1 register is set, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+2 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+3.<br>If bit 9 of the associated compare_word1 register is clear, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+0 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+1. |
| 9 | DISABLE_MASK | RW | R | 0 | 'This bit is used to control whether the compare register word_0 contains a 4-byte compare value, or a 2-byte compare value with a 2-byte mask value.<br>1 - 4-byte compare value<br>0 - 2-byte compare, 2-byte mask ' |
| 10:31 | RESERVED_31_10 | R | R | 0 | 'Reserved, read as 0, ignored on write.' |

### 11.3.269 ETH_TYPE2_COMPARE_10_WORD_0

**Description:** same as type2_compare_0_word_0
**Address:** 0x40481750
**Offset:** 0x1750
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | MASK_VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | MASK_VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_VALUE_TYPE2 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_VALUE_TYPE2 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | MASK_VALUE | RW | R | 0 | These bits can be either a 2 byte mask field or an additional 2 byte Compare Value.<br>If bit 9 of the associated compare_word1 register is set, then the byte stored in bits [7:0] is compared against the byte in the received frame from the selected offset+0 and the byte stored in bits [15:8] is compared against the byte in the received frame from the selected offset+1.<br>If bit 9 of the associated compare_word1 register is clear, these bits become a direct 2-byte mask for the 2-byte compare register in bits [31:16]. |
| 16:31 | COMPARE_VALUE_TYPE2 | RW | R | 0 | 2 byte Compare Value.<br>If bit 9 of the associated compare_word1 register is set, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+2 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+3.<br>If bit 9 of the associated compare_word1 register is clear, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+0 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+1. |

### 11.3.270 ETH_TYPE2_COMPARE_10_WORD_1

**Description:** same as type2_compare_0_word_1
**Address:** 0x40481754
**Offset:** 0x1754
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_OFFSET [7:7] | OFFSET_VALUE [6:0] | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_10 [15:10] | | | | | | DISABLE_MASK [9:9] | COMPARE_OFFSET [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_10 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_10 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:6 | OFFSET_VALUE | RW | R | 0 | 'Offset value in bytes' |
| 7:8 | COMPARE_OFFSET | RW | R | 0 | 'Compare byte offset.<br>00 : Offset from beginning of the frame.<br>01 : Offset from byte after Ether Type.<br>10 : Offset from byte following end of IP header.<br>11 : Offset from byte following end of TCP/UDP header'<br><br>If bit 9 of the associated compare_word1 register is set, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+2 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+3.<br>If bit 9 of the associated compare_word1 register is clear, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+0 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+1. |
| 9 | DISABLE_MASK | RW | R | 0 | 'This bit is used to control whether the compare register word_0 contains a 4-byte compare value, or a 2-byte compare value with a 2-byte mask value.<br>1 - 4-byte compare value<br>0 - 2-byte compare, 2-byte mask ' |
| 10:31 | RESERVED_31_10 | R | R | 0 | 'Reserved, read as 0, ignored on write.' |

### 11.3.271 ETH_TYPE2_COMPARE_11_WORD_0

**Description:** same as type2_compare_0_word_0
**Address:** 0x40481758
**Offset:** 0x1758
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | MASK_VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | MASK_VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_VALUE_TYPE2 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_VALUE_TYPE2 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | MASK_VALUE | RW | R | 0 | These bits can be either a 2 byte mask field or an additional 2 byte Compare Value.<br>If bit 9 of the associated compare_word1 register is set, then the byte stored in bits [7:0] is compared against the byte in the received frame from the selected offset+0 and the byte stored in bits [15:8] is compared against the byte in the received frame from the selected offset+1.<br>If bit 9 of the associated compare_word1 register is clear, these bits become a direct 2-byte mask for the 2-byte compare register in bits [31:16]. |
| 16:31 | COMPARE_VALUE _TYPE2 | RW | R | 0 | 2 byte Compare Value.<br>If bit 9 of the associated compare_word1 register is set, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+2 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+3.<br>If bit 9 of the associated compare_word1 register is clear, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+0 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+1. |

### 11.3.272 ETH_TYPE2_COMPARE_11_WORD_1

**Description:** same as type2_compare_0_word_1
**Address:** 0x4048175C
**Offset:** 0x175C
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_OFFSET [7:7] | OFFSET_VALUE [6:0] | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_10 [15:10] | | | | | | DISABLE_MASK [9:9] | COMPARE_OFFSET [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_10 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_10 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:6 | OFFSET_VALUE | RW | R | 0 | 'Offset value in bytes' |
| 7:8 | COMPARE_OFFSET | RW | R | 0 | 'Compare byte offset.<br>00 : Offset from beginning of the frame.<br>01 : Offset from byte after Ether Type.<br>10 : Offset from byte following end of IP header.<br>11 : Offset from byte following end of TCP/UDP header'<br><br>If bit 9 of the associated compare_word1 register is set, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+2 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+3.<br>If bit 9 of the associated compare_word1 register is clear, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+0 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+1. |
| 9 | DISABLE_MASK | RW | R | 0 | 'This bit is used to control whether the compare register word_0 contains a 4-byte compare value, or a 2-byte compare value with a 2-byte mask value.<br>1 - 4-byte compare value<br>0 - 2-byte compare, 2-byte mask ' |
| 10:31 | RESERVED_31_10 | R | R | 0 | 'Reserved, read as 0, ignored on write.' |

### 11.3.273 ETH_TYPE2_COMPARE_12_WORD_0

**Description:** same as type2_compare_0_word_0
**Address:** 0x40481760
**Offset:** 0x1760
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | MASK_VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | MASK_VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_VALUE_TYPE2 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_VALUE_TYPE2 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | MASK_VALUE | RW | R | 0 | These bits can be either a 2 byte mask field or an additional 2 byte Compare Value.<br>If bit 9 of the associated compare_word1 register is set, then the byte stored in bits [7:0] is compared against the byte in the received frame from the selected offset+0 and the byte stored in bits [15:8] is compared against the byte in the received frame from the selected offset+1.<br>If bit 9 of the associated compare_word1 register is clear, these bits become a direct 2-byte mask for the 2-byte compare register in bits [31:16]. |
| 16:31 | COMPARE_VALUE_TYPE2 | RW | R | 0 | 2 byte Compare Value.<br>If bit 9 of the associated compare_word1 register is set, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+2 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+3.<br>If bit 9 of the associated compare_word1 register is clear, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+0 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+1. |

### 11.3.274 ETH_TYPE2_COMPARE_12_WORD_1

**Description:** same as type2_compare_0_word_1
**Address:** 0x40481764
**Offset:** 0x1764
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_OFFSET [7:7] | OFFSET_VALUE [6:0] | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_10 [15:10] | | | | | | DISABLE_MASK [9:9] | COMPARE_OFFSET [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_10 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_10 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:6 | OFFSET_VALUE | RW | R | 0 | 'Offset value in bytes' |
| 7:8 | COMPARE_OFFSET | RW | R | 0 | 'Compare byte offset.<br>00 : Offset from beginning of the frame.<br>01 : Offset from byte after Ether Type.<br>10 : Offset from byte following end of IP header.<br>11 : Offset from byte following end of TCP/UDP header'<br><br>If bit 9 of the associated compare_word1 register is set, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+2 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+3.<br>If bit 9 of the associated compare_word1 register is clear, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+0 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+1. |
| 9 | DISABLE_MASK | RW | R | 0 | 'This bit is used to control whether the compare register word_0 contains a 4-byte compare value, or a 2-byte compare value with a 2-byte mask value.<br>1 - 4-byte compare value<br>0 - 2-byte compare, 2-byte mask ' |
| 10:31 | RESERVED_31_10 | R | R | 0 | 'Reserved, read as 0, ignored on write.' |

### 11.3.275 ETH_TYPE2_COMPARE_13_WORD_0

**Description:** same as type2_compare_0_word_0
**Address:** 0x40481768
**Offset:** 0x1768
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | MASK_VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | MASK_VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_VALUE_TYPE2 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_VALUE_TYPE2 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | MASK_VALUE | RW | R | 0 | These bits can be either a 2 byte mask field or an additional 2 byte Compare Value.<br>If bit 9 of the associated compare_word1 register is set, then the byte stored in bits [7:0] is compared against the byte in the received frame from the selected offset+0 and the byte stored in bits [15:8] is compared against the byte in the received frame from the selected offset+1.<br>If bit 9 of the associated compare_word1 register is clear, these bits become a direct 2-byte mask for the 2-byte compare register in bits [31:16]. |
| 16:31 | COMPARE_VALUE _TYPE2 | RW | R | 0 | 2 byte Compare Value.<br>If bit 9 of the associated compare_word1 register is set, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+2 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+3.<br>If bit 9 of the associated compare_word1 register is clear, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+0 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+1. |

### 11.3.276 ETH_TYPE2_COMPARE_13_WORD_1

**Description:** same as type2_compare_0_word_1
**Address:** 0x4048176C
**Offset:** 0x176C
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_OFFSET [7:7] | OFFSET_VALUE [6:0] | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_10 [15:10] | | | | | | DISABLE_MASK [9:9] | COMPARE_OFFSET [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_10 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_10 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:6 | OFFSET_VALUE | RW | R | 0 | 'Offset value in bytes' |
| 7:8 | COMPARE_OFFSET | RW | R | 0 | 'Compare byte offset.<br>00 : Offset from beginning of the frame.<br>01 : Offset from byte after Ether Type.<br>10 : Offset from byte following end of IP header.<br>11 : Offset from byte following end of TCP/UDP header'<br><br>If bit 9 of the associated compare_word1 register is set, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+2 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+3.<br>If bit 9 of the associated compare_word1 register is clear, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+0 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+1. |
| 9 | DISABLE_MASK | RW | R | 0 | 'This bit is used to control whether the compare register word_0 contains a 4-byte compare value, or a 2-byte compare value with a 2-byte mask value.<br>1 - 4-byte compare value<br>0 - 2-byte compare, 2-byte mask ' |
| 10:31 | RESERVED_31_10 | R | R | 0 | 'Reserved, read as 0, ignored on write.' |

### 11.3.277 ETH_TYPE2_COMPARE_14_WORD_0

**Description:** same as type2_compare_0_word_0
**Address:** 0x40481770
**Offset:** 0x1770
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | MASK_VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | MASK_VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_VALUE_TYPE2 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_VALUE_TYPE2 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | MASK_VALUE | RW | R | 0 | These bits can be either a 2 byte mask field or an additional 2 byte Compare Value.<br>If bit 9 of the associated compare_word1 register is set, then the byte stored in bits [7:0] is compared against the byte in the received frame from the selected offset+0 and the byte stored in bits [15:8] is compared against the byte in the received frame from the selected offset+1.<br>If bit 9 of the associated compare_word1 register is clear, these bits become a direct 2-byte mask for the 2-byte compare register in bits [31:16]. |
| 16:31 | COMPARE_VALUE _TYPE2 | RW | R | 0 | 2 byte Compare Value.<br>If bit 9 of the associated compare_word1 register is set, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+2 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+3.<br>If bit 9 of the associated compare_word1 register is clear, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+0 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+1. |

### 11.3.278 ETH_TYPE2_COMPARE_14_WORD_1

**Description:** same as type2_compare_0_word_1
**Address:** 0x40481774
**Offset:** 0x1774
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_OFFSET [7:7] | OFFSET_VALUE [6:0] | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_10 [15:10] | | | | | | DISABLE_MASK [9:9] | COMPARE_OFFSET [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_10 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_10 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:6 | OFFSET_VALUE | RW | R | 0 | 'Offset value in bytes' |
| 7:8 | COMPARE_OFFSET | RW | R | 0 | 'Compare byte offset.<br>00 : Offset from beginning of the frame.<br>01 : Offset from byte after Ether Type.<br>10 : Offset from byte following end of IP header.<br>11 : Offset from byte following end of TCP/UDP header'<br><br>If bit 9 of the associated compare_word1 register is set, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+2 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+3.<br>If bit 9 of the associated compare_word1 register is clear, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+0 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+1. |
| 9 | DISABLE_MASK | RW | R | 0 | 'This bit is used to control whether the compare register word_0 contains a 4-byte compare value, or a 2-byte compare value with a 2-byte mask value.<br>1 - 4-byte compare value<br>0 - 2-byte compare, 2-byte mask ' |
| 10:31 | RESERVED_31_10 | R | R | 0 | 'Reserved, read as 0, ignored on write.' |

### 11.3.279 ETH_TYPE2_COMPARE_15_WORD_0

**Description:** same as type2_compare_0_word_0
**Address:** 0x40481778
**Offset:** 0x1778
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | MASK_VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | MASK_VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_VALUE_TYPE2 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_VALUE_TYPE2 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | MASK_VALUE | RW | R | 0 | These bits can be either a 2 byte mask field or an additional 2 byte Compare Value.<br>If bit 9 of the associated compare_word1 register is set, then the byte stored in bits [7:0] is compared against the byte in the received frame from the selected offset+0 and the byte stored in bits [15:8] is compared against the byte in the received frame from the selected offset+1.<br>If bit 9 of the associated compare_word1 register is clear, these bits become a direct 2-byte mask for the 2-byte compare register in bits [31:16]. |
| 16:31 | COMPARE_VALUE_TYPE2 | RW | R | 0 | 2 byte Compare Value.<br>If bit 9 of the associated compare_word1 register is set, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+2 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+3.<br>If bit 9 of the associated compare_word1 register is clear, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+0 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+1. |

### 11.3.280 ETH_TYPE2_COMPARE_15_WORD_1

**Description:** same as type2_compare_0_word_1
**Address:** 0x4048177C
**Offset:** 0x177C
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_OFFSET [7:7] | OFFSET_VALUE [6:0] | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_10 [15:10] | | | | | | DISABLE_MASK [9:9] | COMPARE_OFFSET [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_10 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_10 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:6 | OFFSET_VALUE | RW | R | 0 | 'Offset value in bytes' |
| 7:8 | COMPARE_OFFSET | RW | R | 0 | 'Compare byte offset.<br>00 : Offset from beginning of the frame.<br>01 : Offset from byte after Ether Type.<br>10 : Offset from byte following end of IP header.<br>11 : Offset from byte following end of TCP/UDP header'<br><br>If bit 9 of the associated compare_word1 register is set, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+2 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+3.<br>If bit 9 of the associated compare_word1 register is clear, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+0 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+1. |
| 9 | DISABLE_MASK | RW | R | 0 | 'This bit is used to control whether the compare register word_0 contains a 4-byte compare value, or a 2-byte compare value with a 2-byte mask value.<br>1 - 4-byte compare value<br>0 - 2-byte compare, 2-byte mask ' |
| 10:31 | RESERVED_31_10 | R | R | 0 | 'Reserved, read as 0, ignored on write.' |

### 11.3.281 ETH_TYPE2_COMPARE_16_WORD_0

**Description:** same as type2_compare_0_word_0
**Address:** 0x40481780
**Offset:** 0x1780
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | MASK_VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | MASK_VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_VALUE_TYPE2 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_VALUE_TYPE2 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | MASK_VALUE | RW | R | 0 | These bits can be either a 2 byte mask field or an additional 2 byte Compare Value.<br>If bit 9 of the associated compare_word1 register is set, then the byte stored in bits [7:0] is compared against the byte in the received frame from the selected offset+0 and the byte stored in bits [15:8] is compared against the byte in the received frame from the selected offset+1.<br>If bit 9 of the associated compare_word1 register is clear, these bits become a direct 2-byte mask for the 2-byte compare register in bits [31:16]. |
| 16:31 | COMPARE_VALUE _TYPE2 | RW | R | 0 | 2 byte Compare Value.<br>If bit 9 of the associated compare_word1 register is set, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+2 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+3.<br>If bit 9 of the associated compare_word1 register is clear, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+0 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+1. |

### 11.3.282 ETH_TYPE2_COMPARE_16_WORD_1

**Description:** same as type2_compare_0_word_1
**Address:** 0x40481784
**Offset:** 0x1784
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_OFFSET [7:7] | OFFSET_VALUE [6:0] | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_10 [15:10] | | | | | | DISABLE_MASK [9:9] | COMPARE_OFFSET [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_10 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_10 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:6 | OFFSET_VALUE | RW | R | 0 | 'Offset value in bytes' |
| 7:8 | COMPARE_OFFSET | RW | R | 0 | 'Compare byte offset.<br>00 : Offset from beginning of the frame.<br>01 : Offset from byte after Ether Type.<br>10 : Offset from byte following end of IP header.<br>11 : Offset from byte following end of TCP/UDP header'<br><br>If bit 9 of the associated compare_word1 register is set, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+2 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+3.<br>If bit 9 of the associated compare_word1 register is clear, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+0 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+1. |
| 9 | DISABLE_MASK | RW | R | 0 | 'This bit is used to control whether the compare register word_0 contains a 4-byte compare value, or a 2-byte compare value with a 2-byte mask value.<br>1 - 4-byte compare value<br>0 - 2-byte compare, 2-byte mask ' |
| 10:31 | RESERVED_31_10 | R | R | 0 | 'Reserved, read as 0, ignored on write.' |

### 11.3.283 ETH_TYPE2_COMPARE_17_WORD_0

**Description:** same as type2_compare_0_word_0
**Address:** 0x40481788
**Offset:** 0x1788
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | MASK_VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | MASK_VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_VALUE_TYPE2 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_VALUE_TYPE2 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | MASK_VALUE | RW | R | 0 | These bits can be either a 2 byte mask field or an additional 2 byte Compare Value.<br>If bit 9 of the associated compare_word1 register is set, then the byte stored in bits [7:0] is compared against the byte in the received frame from the selected offset+0 and the byte stored in bits [15:8] is compared against the byte in the received frame from the selected offset+1.<br>If bit 9 of the associated compare_word1 register is clear, these bits become a direct 2-byte mask for the 2-byte compare register in bits [31:16]. |
| 16:31 | COMPARE_VALUE_TYPE2 | RW | R | 0 | 2 byte Compare Value.<br>If bit 9 of the associated compare_word1 register is set, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+2 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+3.<br>If bit 9 of the associated compare_word1 register is clear, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+0 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+1. |

### 11.3.284 ETH_TYPE2_COMPARE_17_WORD_1

**Description:** same as type2_compare_0_word_1
**Address:** 0x4048178C
**Offset:** 0x178C
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_OFFSET [7:7] | OFFSET_VALUE [6:0] | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_10 [15:10] | | | | | | DISABLE_MASK [9:9] | COMPARE_OFFSET [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_10 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_10 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:6 | OFFSET_VALUE | RW | R | 0 | 'Offset value in bytes' |
| 7:8 | COMPARE_OFFSET | RW | R | 0 | 'Compare byte offset.<br>00 : Offset from beginning of the frame.<br>01 : Offset from byte after Ether Type.<br>10 : Offset from byte following end of IP header.<br>11 : Offset from byte following end of TCP/UDP header'<br><br>If bit 9 of the associated compare_word1 register is set, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+2 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+3.<br>If bit 9 of the associated compare_word1 register is clear, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+0 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+1. |
| 9 | DISABLE_MASK | RW | R | 0 | 'This bit is used to control whether the compare register word_0 contains a 4-byte compare value, or a 2-byte compare value with a 2-byte mask value.<br>1 - 4-byte compare value<br>0 - 2-byte compare, 2-byte mask ' |
| 10:31 | RESERVED_31_10 | R | R | 0 | 'Reserved, read as 0, ignored on write.' |

### 11.3.285 ETH_TYPE2_COMPARE_18_WORD_0

**Description:** same as type2_compare_0_word_0
**Address:** 0x40481790
**Offset:** 0x1790
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | MASK_VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | MASK_VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_VALUE_TYPE2 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_VALUE_TYPE2 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | MASK_VALUE | RW | R | 0 | These bits can be either a 2 byte mask field or an additional 2 byte Compare Value.<br>If bit 9 of the associated compare_word1 register is set, then the byte stored in bits [7:0] is compared against the byte in the received frame from the selected offset+0 and the byte stored in bits [15:8] is compared against the byte in the received frame from the selected offset+1.<br>If bit 9 of the associated compare_word1 register is clear, these bits become a direct 2-byte mask for the 2-byte compare register in bits [31:16]. |
| 16:31 | COMPARE_VALUE _TYPE2 | RW | R | 0 | 2 byte Compare Value.<br>If bit 9 of the associated compare_word1 register is set, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+2 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+3.<br>If bit 9 of the associated compare_word1 register is clear, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+0 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+1. |

### 11.3.286 ETH_TYPE2_COMPARE_18_WORD_1

**Description:** same as type2_compare_0_word_1
**Address:** 0x40481794
**Offset:** 0x1794
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_OFFSET [7:7] | OFFSET_VALUE [6:0] | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_10 [15:10] | | | | | | DISABLE_MASK [9:9] | COMPARE_OFFSET [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_10 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_10 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:6 | OFFSET_VALUE | RW | R | 0 | 'Offset value in bytes' |
| 7:8 | COMPARE_OFFSET | RW | R | 0 | 'Compare byte offset.<br>00 : Offset from beginning of the frame.<br>01 : Offset from byte after Ether Type.<br>10 : Offset from byte following end of IP header.<br>11 : Offset from byte following end of TCP/UDP header'<br><br>If bit 9 of the associated compare_word1 register is set, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+2 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+3.<br>If bit 9 of the associated compare_word1 register is clear, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+0 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+1. |
| 9 | DISABLE_MASK | RW | R | 0 | 'This bit is used to control whether the compare register word_0 contains a 4-byte compare value, or a 2-byte compare value with a 2-byte mask value.<br>1 - 4-byte compare value<br>0 - 2-byte compare, 2-byte mask ' |
| 10:31 | RESERVED_31_10 | R | R | 0 | 'Reserved, read as 0, ignored on write.' |

### 11.3.287 ETH_TYPE2_COMPARE_19_WORD_0

**Description:** same as type2_compare_0_word_0
**Address:** 0x40481798
**Offset:** 0x1798
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | MASK_VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | MASK_VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_VALUE_TYPE2 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_VALUE_TYPE2 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | MASK_VALUE | RW | R | 0 | These bits can be either a 2 byte mask field or an additional 2 byte Compare Value.<br>If bit 9 of the associated compare_word1 register is set, then the byte stored in bits [7:0] is compared against the byte in the received frame from the selected offset+0 and the byte stored in bits [15:8] is compared against the byte in the received frame from the selected offset+1.<br>If bit 9 of the associated compare_word1 register is clear, these bits become a direct 2-byte mask for the 2-byte compare register in bits [31:16]. |
| 16:31 | COMPARE_VALUE_TYPE2 | RW | R | 0 | 2 byte Compare Value.<br>If bit 9 of the associated compare_word1 register is set, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+2 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+3.<br>If bit 9 of the associated compare_word1 register is clear, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+0 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+1. |

### 11.3.288 ETH_TYPE2_COMPARE_19_WORD_1

**Description:** same as type2_compare_0_word_1
**Address:** 0x4048179C
**Offset:** 0x179C
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_OFFSET [7:7] | OFFSET_VALUE [6:0] | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_10 [15:10] | | | | | | DISABLE_MASK [9:9] | COMPARE_OFFSET [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_10 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_10 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:6 | OFFSET_VALUE | RW | R | 0 | 'Offset value in bytes' |
| 7:8 | COMPARE_OFFSET | RW | R | 0 | 'Compare byte offset.<br>00 : Offset from beginning of the frame.<br>01 : Offset from byte after Ether Type.<br>10 : Offset from byte following end of IP header.<br>11 : Offset from byte following end of TCP/UDP header'<br><br>If bit 9 of the associated compare_word1 register is set, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+2 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+3.<br>If bit 9 of the associated compare_word1 register is clear, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+0 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+1. |
| 9 | DISABLE_MASK | RW | R | 0 | 'This bit is used to control whether the compare register word_0 contains a 4-byte compare value, or a 2-byte compare value with a 2-byte mask value.<br>1 - 4-byte compare value<br>0 - 2-byte compare, 2-byte mask ' |
| 10:31 | RESERVED_31_10 | R | R | 0 | 'Reserved, read as 0, ignored on write.' |

### 11.3.289 ETH_TYPE2_COMPARE_20_WORD_0

**Description:** same as type2_compare_0_word_0
**Address:** 0x404817A0
**Offset:** 0x17A0
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | MASK_VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | MASK_VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_VALUE_TYPE2 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_VALUE_TYPE2 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | MASK_VALUE | RW | R | 0 | These bits can be either a 2 byte mask field or an additional 2 byte Compare Value.<br>If bit 9 of the associated compare_word1 register is set, then the byte stored in bits [7:0] is compared against the byte in the received frame from the selected offset+0 and the byte stored in bits [15:8] is compared against the byte in the received frame from the selected offset+1.<br>If bit 9 of the associated compare_word1 register is clear, these bits become a direct 2-byte mask for the 2-byte compare register in bits [31:16]. |
| 16:31 | COMPARE_VALUE_TYPE2 | RW | R | 0 | 2 byte Compare Value.<br>If bit 9 of the associated compare_word1 register is set, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+2 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+3.<br>If bit 9 of the associated compare_word1 register is clear, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+0 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+1. |

### 11.3.290 ETH_TYPE2_COMPARE_20_WORD_1

**Description:** same as type2_compare_0_word_1
**Address:** 0x404817A4
**Offset:** 0x17A4
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_OFFSET [7:7] | OFFSET_VALUE [6:0] | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_10 [15:10] | | | | | | DISABLE_MASK [9:9] | COMPARE_OFFSET [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_10 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_10 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:6 | OFFSET_VALUE | RW | R | 0 | 'Offset value in bytes' |
| 7:8 | COMPARE_OFFSET | RW | R | 0 | 'Compare byte offset.<br>00 : Offset from beginning of the frame.<br>01 : Offset from byte after Ether Type.<br>10 : Offset from byte following end of IP header.<br>11 : Offset from byte following end of TCP/UDP header'<br><br>If bit 9 of the associated compare_word1 register is set, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+2 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+3.<br>If bit 9 of the associated compare_word1 register is clear, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+0 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+1. |
| 9 | DISABLE_MASK | RW | R | 0 | 'This bit is used to control whether the compare register word_0 contains a 4-byte compare value, or a 2-byte compare value with a 2-byte mask value.<br>1 - 4-byte compare value<br>0 - 2-byte compare, 2-byte mask ' |
| 10:31 | RESERVED_31_10 | R | R | 0 | 'Reserved, read as 0, ignored on write.' |

### 11.3.291 ETH_TYPE2_COMPARE_21_WORD_0

**Description:** same as type2_compare_0_word_0
**Address:** 0x404817A8
**Offset:** 0x17A8
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | MASK_VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | MASK_VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_VALUE_TYPE2 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_VALUE_TYPE2 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | MASK_VALUE | RW | R | 0 | These bits can be either a 2 byte mask field or an additional 2 byte Compare Value.<br>If bit 9 of the associated compare_word1 register is set, then the byte stored in bits [7:0] is compared against the byte in the received frame from the selected offset+0 and the byte stored in bits [15:8] is compared against the byte in the received frame from the selected offset+1.<br>If bit 9 of the associated compare_word1 register is clear, these bits become a direct 2-byte mask for the 2-byte compare register in bits [31:16]. |
| 16:31 | COMPARE_VALUE _TYPE2 | RW | R | 0 | 2 byte Compare Value.<br>If bit 9 of the associated compare_word1 register is set, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+2 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+3.<br>If bit 9 of the associated compare_word1 register is clear, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+0 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+1. |

### 11.3.292 ETH_TYPE2_COMPARE_21_WORD_1

**Description:** same as type2_compare_0_word_1
**Address:** 0x404817AC
**Offset:** 0x17AC
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_OFFSET [7:7] | OFFSET_VALUE [6:0] | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_10 [15:10] | | | | | | DISABLE_MASK [9:9] | COMPARE_OFFSET [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_10 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_10 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:6 | OFFSET_VALUE | RW | R | 0 | 'Offset value in bytes' |
| 7:8 | COMPARE_OFFSET | RW | R | 0 | 'Compare byte offset.<br>00 : Offset from beginning of the frame.<br>01 : Offset from byte after Ether Type.<br>10 : Offset from byte following end of IP header.<br>11 : Offset from byte following end of TCP/UDP header'<br><br>If bit 9 of the associated compare_word1 register is set, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+2 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+3.<br>If bit 9 of the associated compare_word1 register is clear, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+0 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+1. |
| 9 | DISABLE_MASK | RW | R | 0 | 'This bit is used to control whether the compare register word_0 contains a 4-byte compare value, or a 2-byte compare value with a 2-byte mask value.<br>1 - 4-byte compare value<br>0 - 2-byte compare, 2-byte mask ' |
| 10:31 | RESERVED_31_10 | R | R | 0 | 'Reserved, read as 0, ignored on write.' |

### 11.3.293 ETH_TYPE2_COMPARE_22_WORD_0

**Description:** same as type2_compare_0_word_0
**Address:** 0x404817B0
**Offset:** 0x17B0
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | MASK_VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | MASK_VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_VALUE_TYPE2 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_VALUE_TYPE2 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | MASK_VALUE | RW | R | 0 | These bits can be either a 2 byte mask field or an additional 2 byte Compare Value.<br>If bit 9 of the associated compare_word1 register is set, then the byte stored in bits [7:0] is compared against the byte in the received frame from the selected offset+0 and the byte stored in bits [15:8] is compared against the byte in the received frame from the selected offset+1.<br>If bit 9 of the associated compare_word1 register is clear, these bits become a direct 2-byte mask for the 2-byte compare register in bits [31:16]. |
| 16:31 | COMPARE_VALUE_TYPE2 | RW | R | 0 | 2 byte Compare Value.<br>If bit 9 of the associated compare_word1 register is set, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+2 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+3.<br>If bit 9 of the associated compare_word1 register is clear, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+0 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+1. |

### 11.3.294 ETH_TYPE2_COMPARE_22_WORD_1

**Description:** same as type2_compare_0_word_1
**Address:** 0x404817B4
**Offset:** 0x17B4
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_OFFSET [7:7] | OFFSET_VALUE [6:0] | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_10 [15:10] | | | | | | DISABLE_MASK [9:9] | COMPARE_OFFSET [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_10 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_10 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:6 | OFFSET_VALUE | RW | R | 0 | 'Offset value in bytes' |
| 7:8 | COMPARE_OFFSET | RW | R | 0 | 'Compare byte offset.<br>00 : Offset from beginning of the frame.<br>01 : Offset from byte after Ether Type.<br>10 : Offset from byte following end of IP header.<br>11 : Offset from byte following end of TCP/UDP header'<br><br>If bit 9 of the associated compare_word1 register is set, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+2 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+3.<br>If bit 9 of the associated compare_word1 register is clear, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+0 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+1. |
| 9 | DISABLE_MASK | RW | R | 0 | 'This bit is used to control whether the compare register word_0 contains a 4-byte compare value, or a 2-byte compare value with a 2-byte mask value.<br>1 - 4-byte compare value<br>0 - 2-byte compare, 2-byte mask ' |
| 10:31 | RESERVED_31_10 | R | R | 0 | 'Reserved, read as 0, ignored on write.' |

### 11.3.295 ETH_TYPE2_COMPARE_23_WORD_0

**Description:** same as type2_compare_0_word_0
**Address:** 0x404817B8
**Offset:** 0x17B8
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | MASK_VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | MASK_VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_VALUE_TYPE2 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_VALUE_TYPE2 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | MASK_VALUE | RW | R | 0 | These bits can be either a 2 byte mask field or an additional 2 byte Compare Value.<br>If bit 9 of the associated compare_word1 register is set, then the byte stored in bits [7:0] is compared against the byte in the received frame from the selected offset+0 and the byte stored in bits [15:8] is compared against the byte in the received frame from the selected offset+1.<br>If bit 9 of the associated compare_word1 register is clear, these bits become a direct 2-byte mask for the 2-byte compare register in bits [31:16]. |
| 16:31 | COMPARE_VALUE_TYPE2 | RW | R | 0 | 2 byte Compare Value.<br>If bit 9 of the associated compare_word1 register is set, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+2 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+3.<br>If bit 9 of the associated compare_word1 register is clear, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+0 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+1. |

### 11.3.296 ETH_TYPE2_COMPARE_23_WORD_1

**Description:** same as type2_compare_0_word_1
**Address:** 0x404817BC
**Offset:** 0x17BC
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_OFFSET [7:7] | OFFSET_VALUE [6:0] | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_10 [15:10] | | | | | | DISABLE_MASK [9:9] | COMPARE_OFFSET [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_10 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_10 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:6 | OFFSET_VALUE | RW | R | 0 | 'Offset value in bytes' |
| 7:8 | COMPARE_OFFSET | RW | R | 0 | 'Compare byte offset.<br>00 : Offset from beginning of the frame.<br>01 : Offset from byte after Ether Type.<br>10 : Offset from byte following end of IP header.<br>11 : Offset from byte following end of TCP/UDP header'<br><br>If bit 9 of the associated compare_word1 register is set, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+2 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+3.<br>If bit 9 of the associated compare_word1 register is clear, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+0 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+1. |
| 9 | DISABLE_MASK | RW | R | 0 | 'This bit is used to control whether the compare register word_0 contains a 4-byte compare value, or a 2-byte compare value with a 2-byte mask value.<br>1 - 4-byte compare value<br>0 - 2-byte compare, 2-byte mask ' |
| 10:31 | RESERVED_31_10 | R | R | 0 | 'Reserved, read as 0, ignored on write.' |

### 11.3.297 ETH_TYPE2_COMPARE_24_WORD_0

**Description:** same as type2_compare_0_word_0
**Address:** 0x404817C0
**Offset:** 0x17C0
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | MASK_VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | MASK_VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_VALUE_TYPE2 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_VALUE_TYPE2 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | MASK_VALUE | RW | R | 0 | These bits can be either a 2 byte mask field or an additional 2 byte Compare Value.<br>If bit 9 of the associated compare_word1 register is set, then the byte stored in bits [7:0] is compared against the byte in the received frame from the selected offset+0 and the byte stored in bits [15:8] is compared against the byte in the received frame from the selected offset+1.<br>If bit 9 of the associated compare_word1 register is clear, these bits become a direct 2-byte mask for the 2-byte compare register in bits [31:16]. |
| 16:31 | COMPARE_VALUE_TYPE2 | RW | R | 0 | 2 byte Compare Value.<br>If bit 9 of the associated compare_word1 register is set, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+2 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+3.<br>If bit 9 of the associated compare_word1 register is clear, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+0 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+1. |

### 11.3.298 ETH_TYPE2_COMPARE_24_WORD_1

**Description:** same as type2_compare_0_word_1
**Address:** 0x404817C4
**Offset:** 0x17C4
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_OFFSET [7:7] | OFFSET_VALUE [6:0] | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_10 [15:10] | | | | | | DISABLE_MASK [9:9] | COMPARE_OFFSET [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_10 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_10 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:6 | OFFSET_VALUE | RW | R | 0 | 'Offset value in bytes' |
| 7:8 | COMPARE_OFFSET | RW | R | 0 | 'Compare byte offset.<br>00 : Offset from beginning of the frame.<br>01 : Offset from byte after Ether Type.<br>10 : Offset from byte following end of IP header.<br>11 : Offset from byte following end of TCP/UDP header'<br><br>If bit 9 of the associated compare_word1 register is set, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+2 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+3.<br>If bit 9 of the associated compare_word1 register is clear, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+0 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+1. |
| 9 | DISABLE_MASK | RW | R | 0 | 'This bit is used to control whether the compare register word_0 contains a 4-byte compare value, or a 2-byte compare value with a 2-byte mask value.<br>1 - 4-byte compare value<br>0 - 2-byte compare, 2-byte mask ' |
| 10:31 | RESERVED_31_10 | R | R | 0 | 'Reserved, read as 0, ignored on write.' |

### 11.3.299 ETH_TYPE2_COMPARE_25_WORD_0

**Description:** same as type2_compare_0_word_0
**Address:** 0x404817C8
**Offset:** 0x17C8
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | MASK_VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | MASK_VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_VALUE_TYPE2 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_VALUE_TYPE2 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | MASK_VALUE | RW | R | 0 | These bits can be either a 2 byte mask field or an additional 2 byte Compare Value.<br>If bit 9 of the associated compare_word1 register is set, then the byte stored in bits [7:0] is compared against the byte in the received frame from the selected offset+0 and the byte stored in bits [15:8] is compared against the byte in the received frame from the selected offset+1.<br>If bit 9 of the associated compare_word1 register is clear, these bits become a direct 2-byte mask for the 2-byte compare register in bits [31:16]. |
| 16:31 | COMPARE_VALUE_TYPE2 | RW | R | 0 | 2 byte Compare Value.<br>If bit 9 of the associated compare_word1 register is set, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+2 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+3.<br>If bit 9 of the associated compare_word1 register is clear, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+0 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+1. |

### 11.3.300 ETH_TYPE2_COMPARE_25_WORD_1

**Description:** same as type2_compare_0_word_1
**Address:** 0x404817CC
**Offset:** 0x17CC
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_OFFSET [7:7] | OFFSET_VALUE [6:0] | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_10 [15:10] | | | | | | DISABLE_MASK [9:9] | COMPARE_OFFSET [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_10 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_10 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:6 | OFFSET_VALUE | RW | R | 0 | 'Offset value in bytes' |
| 7:8 | COMPARE_OFFSET | RW | R | 0 | 'Compare byte offset.<br>00 : Offset from beginning of the frame.<br>01 : Offset from byte after Ether Type.<br>10 : Offset from byte following end of IP header.<br>11 : Offset from byte following end of TCP/UDP header'<br><br>If bit 9 of the associated compare_word1 register is set, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+2 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+3.<br>If bit 9 of the associated compare_word1 register is clear, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+0 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+1. |
| 9 | DISABLE_MASK | RW | R | 0 | 'This bit is used to control whether the compare register word_0 contains a 4-byte compare value, or a 2-byte compare value with a 2-byte mask value.<br>1 - 4-byte compare value<br>0 - 2-byte compare, 2-byte mask ' |
| 10:31 | RESERVED_31_10 | R | R | 0 | 'Reserved, read as 0, ignored on write.' |

### 11.3.301 ETH_TYPE2_COMPARE_26_WORD_0

**Description:** same as type2_compare_0_word_0
**Address:** 0x404817D0
**Offset:** 0x17D0
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | MASK_VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | MASK_VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_VALUE_TYPE2 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_VALUE_TYPE2 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | MASK_VALUE | RW | R | 0 | These bits can be either a 2 byte mask field or an additional 2 byte Compare Value.<br>If bit 9 of the associated compare_word1 register is set, then the byte stored in bits [7:0] is compared against the byte in the received frame from the selected offset+0 and the byte stored in bits [15:8] is compared against the byte in the received frame from the selected offset+1.<br>If bit 9 of the associated compare_word1 register is clear, these bits become a direct 2-byte mask for the 2-byte compare register in bits [31:16]. |
| 16:31 | COMPARE_VALUE_TYPE2 | RW | R | 0 | 2 byte Compare Value.<br>If bit 9 of the associated compare_word1 register is set, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+2 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+3.<br>If bit 9 of the associated compare_word1 register is clear, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+0 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+1. |

### 11.3.302 ETH_TYPE2_COMPARE_26_WORD_1

**Description:** same as type2_compare_0_word_1
**Address:** 0x404817D4
**Offset:** 0x17D4
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_OFFSET [7:7] | OFFSET_VALUE [6:0] | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_10 [15:10] | | | | | | DISABLE_MASK [9:9] | COMPARE_OFFSET [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_10 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_10 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:6 | OFFSET_VALUE | RW | R | 0 | 'Offset value in bytes' |
| 7:8 | COMPARE_OFFSET | RW | R | 0 | 'Compare byte offset.<br>00 : Offset from beginning of the frame.<br>01 : Offset from byte after Ether Type.<br>10 : Offset from byte following end of IP header.<br>11 : Offset from byte following end of TCP/UDP header'<br><br>If bit 9 of the associated compare_word1 register is set, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+2 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+3.<br>If bit 9 of the associated compare_word1 register is clear, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+0 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+1. |
| 9 | DISABLE_MASK | RW | R | 0 | 'This bit is used to control whether the compare register word_0 contains a 4-byte compare value, or a 2-byte compare value with a 2-byte mask value.<br>1 - 4-byte compare value<br>0 - 2-byte compare, 2-byte mask ' |
| 10:31 | RESERVED_31_10 | R | R | 0 | 'Reserved, read as 0, ignored on write.' |

### 11.3.303 ETH_TYPE2_COMPARE_27_WORD_0

**Description:** same as type2_compare_0_word_0
**Address:** 0x404817D8
**Offset:** 0x17D8
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | MASK_VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | MASK_VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_VALUE_TYPE2 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_VALUE_TYPE2 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | MASK_VALUE | RW | R | 0 | These bits can be either a 2 byte mask field or an additional 2 byte Compare Value.<br>If bit 9 of the associated compare_word1 register is set, then the byte stored in bits [7:0] is compared against the byte in the received frame from the selected offset+0 and the byte stored in bits [15:8] is compared against the byte in the received frame from the selected offset+1.<br>If bit 9 of the associated compare_word1 register is clear, these bits become a direct 2-byte mask for the 2-byte compare register in bits [31:16]. |
| 16:31 | COMPARE_VALUE_TYPE2 | RW | R | 0 | 2 byte Compare Value.<br>If bit 9 of the associated compare_word1 register is set, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+2 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+3.<br>If bit 9 of the associated compare_word1 register is clear, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+0 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+1. |

### 11.3.304 ETH_TYPE2_COMPARE_27_WORD_1

**Description:** same as type2_compare_0_word_1
**Address:** 0x404817DC
**Offset:** 0x17DC
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_OFFSET [7:7] | OFFSET_VALUE [6:0] | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_10 [15:10] | | | | | | DISABLE_MASK [9:9] | COMPARE_OFFSET [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_10 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_10 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:6 | OFFSET_VALUE | RW | R | 0 | 'Offset value in bytes' |
| 7:8 | COMPARE_OFFSET | RW | R | 0 | 'Compare byte offset.<br>00 : Offset from beginning of the frame.<br>01 : Offset from byte after Ether Type.<br>10 : Offset from byte following end of IP header.<br>11 : Offset from byte following end of TCP/UDP header'<br><br>If bit 9 of the associated compare_word1 register is set, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+2 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+3.<br>If bit 9 of the associated compare_word1 register is clear, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+0 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+1. |
| 9 | DISABLE_MASK | RW | R | 0 | 'This bit is used to control whether the compare register word_0 contains a 4-byte compare value, or a 2-byte compare value with a 2-byte mask value.<br>1 - 4-byte compare value<br>0 - 2-byte compare, 2-byte mask ' |
| 10:31 | RESERVED_31_10 | R | R | 0 | 'Reserved, read as 0, ignored on write.' |

### 11.3.305 ETH_TYPE2_COMPARE_28_WORD_0

**Description:** same as type2_compare_0_word_0
**Address:** 0x404817E0
**Offset:** 0x17E0
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | MASK_VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | MASK_VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_VALUE_TYPE2 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_VALUE_TYPE2 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | MASK_VALUE | RW | R | 0 | These bits can be either a 2 byte mask field or an additional 2 byte Compare Value.<br>If bit 9 of the associated compare_word1 register is set, then the byte stored in bits [7:0] is compared against the byte in the received frame from the selected offset+0 and the byte stored in bits [15:8] is compared against the byte in the received frame from the selected offset+1.<br>If bit 9 of the associated compare_word1 register is clear, these bits become a direct 2-byte mask for the 2-byte compare register in bits [31:16]. |
| 16:31 | COMPARE_VALUE_TYPE2 | RW | R | 0 | 2 byte Compare Value.<br>If bit 9 of the associated compare_word1 register is set, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+2 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+3.<br>If bit 9 of the associated compare_word1 register is clear, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+0 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+1. |

### 11.3.306 ETH_TYPE2_COMPARE_28_WORD_1

**Description:** same as type2_compare_0_word_1
**Address:** 0x404817E4
**Offset:** 0x17E4
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_OFFSET [7:7] | OFFSET_VALUE [6:0] | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_10 [15:10] | | | | | | DISABLE_MASK [9:9] | COMPARE_OFFSET [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_10 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_10 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:6 | OFFSET_VALUE | RW | R | 0 | 'Offset value in bytes' |
| 7:8 | COMPARE_OFFSET | RW | R | 0 | 'Compare byte offset.<br>00 : Offset from beginning of the frame.<br>01 : Offset from byte after Ether Type.<br>10 : Offset from byte following end of IP header.<br>11 : Offset from byte following end of TCP/UDP header'<br><br>If bit 9 of the associated compare_word1 register is set, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+2 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+3.<br>If bit 9 of the associated compare_word1 register is clear, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+0 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+1. |
| 9 | DISABLE_MASK | RW | R | 0 | 'This bit is used to control whether the compare register word_0 contains a 4-byte compare value, or a 2-byte compare value with a 2-byte mask value.<br>1 - 4-byte compare value<br>0 - 2-byte compare, 2-byte mask ' |
| 10:31 | RESERVED_31_10 | R | R | 0 | 'Reserved, read as 0, ignored on write.' |

### 11.3.307 ETH_TYPE2_COMPARE_29_WORD_0

**Description:** same as type2_compare_0_word_0
**Address:** 0x404817E8
**Offset:** 0x17E8
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | MASK_VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | MASK_VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_VALUE_TYPE2 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_VALUE_TYPE2 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | MASK_VALUE | RW | R | 0 | These bits can be either a 2 byte mask field or an additional 2 byte Compare Value.<br>If bit 9 of the associated compare_word1 register is set, then the byte stored in bits [7:0] is compared against the byte in the received frame from the selected offset+0 and the byte stored in bits [15:8] is compared against the byte in the received frame from the selected offset+1.<br>If bit 9 of the associated compare_word1 register is clear, these bits become a direct 2-byte mask for the 2-byte compare register in bits [31:16]. |
| 16:31 | COMPARE_VALUE_TYPE2 | RW | R | 0 | 2 byte Compare Value.<br>If bit 9 of the associated compare_word1 register is set, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+2 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+3.<br>If bit 9 of the associated compare_word1 register is clear, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+0 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+1. |

### 11.3.308 ETH_TYPE2_COMPARE_29_WORD_1

**Description:** same as type2_compare_0_word_1
**Address:** 0x404817EC
**Offset:** 0x17EC
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_OFFSET [7:7] | OFFSET_VALUE [6:0] | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_10 [15:10] | | | | | | DISABLE_MASK [9:9] | COMPARE_OFFSET [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_10 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_10 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:6 | OFFSET_VALUE | RW | R | 0 | 'Offset value in bytes' |
| 7:8 | COMPARE_OFFSET | RW | R | 0 | 'Compare byte offset.<br>00 : Offset from beginning of the frame.<br>01 : Offset from byte after Ether Type.<br>10 : Offset from byte following end of IP header.<br>11 : Offset from byte following end of TCP/UDP header'<br><br>If bit 9 of the associated compare_word1 register is set, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+2 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+3.<br>If bit 9 of the associated compare_word1 register is clear, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+0 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+1. |
| 9 | DISABLE_MASK | RW | R | 0 | 'This bit is used to control whether the compare register word_0 contains a 4-byte compare value, or a 2-byte compare value with a 2-byte mask value.<br>1 - 4-byte compare value<br>0 - 2-byte compare, 2-byte mask ' |
| 10:31 | RESERVED_31_10 | R | R | 0 | 'Reserved, read as 0, ignored on write.' |

### 11.3.309 ETH_TYPE2_COMPARE_30_WORD_0

**Description:** same as type2_compare_0_word_0
**Address:** 0x404817F0
**Offset:** 0x17F0
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | MASK_VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | MASK_VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_VALUE_TYPE2 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_VALUE_TYPE2 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | MASK_VALUE | RW | R | 0 | These bits can be either a 2 byte mask field or an additional 2 byte Compare Value.<br>If bit 9 of the associated compare_word1 register is set, then the byte stored in bits [7:0] is compared against the byte in the received frame from the selected offset+0 and the byte stored in bits [15:8] is compared against the byte in the received frame from the selected offset+1.<br>If bit 9 of the associated compare_word1 register is clear, these bits become a direct 2-byte mask for the 2-byte compare register in bits [31:16]. |
| 16:31 | COMPARE_VALUE_TYPE2 | RW | R | 0 | 2 byte Compare Value.<br>If bit 9 of the associated compare_word1 register is set, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+2 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+3.<br>If bit 9 of the associated compare_word1 register is clear, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+0 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+1. |

### 11.3.310 ETH_TYPE2_COMPARE_30_WORD_1

**Description:** same as type2_compare_0_word_1
**Address:** 0x404817F4
**Offset:** 0x17F4
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_OFFSET [7:7] | OFFSET_VALUE [6:0] | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_10 [15:10] | | | | | | DISABLE_MASK [9:9] | COMPARE_OFFSET [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_10 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_10 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:6 | OFFSET_VALUE | RW | R | 0 | 'Offset value in bytes' |
| 7:8 | COMPARE_OFFSET | RW | R | 0 | 'Compare byte offset.<br>00 : Offset from beginning of the frame.<br>01 : Offset from byte after Ether Type.<br>10 : Offset from byte following end of IP header.<br>11 : Offset from byte following end of TCP/UDP header'<br><br>If bit 9 of the associated compare_word1 register is set, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+2 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+3.<br>If bit 9 of the associated compare_word1 register is clear, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+0 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+1. |
| 9 | DISABLE_MASK | RW | R | 0 | 'This bit is used to control whether the compare register word_0 contains a 4-byte compare value, or a 2-byte compare value with a 2-byte mask value.<br>1 - 4-byte compare value<br>0 - 2-byte compare, 2-byte mask ' |
| 10:31 | RESERVED_31_10 | R | R | 0 | 'Reserved, read as 0, ignored on write.' |

### 11.3.311 ETH_TYPE2_COMPARE_31_WORD_0

**Description:** same as type2_compare_0_word_0
**Address:** 0x404817F8
**Offset:** 0x17F8
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | MASK_VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | MASK_VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_VALUE_TYPE2 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_VALUE_TYPE2 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | MASK_VALUE | RW | R | 0 | These bits can be either a 2 byte mask field or an additional 2 byte Compare Value.<br>If bit 9 of the associated compare_word1 register is set, then the byte stored in bits [7:0] is compared against the byte in the received frame from the selected offset+0 and the byte stored in bits [15:8] is compared against the byte in the received frame from the selected offset+1.<br>If bit 9 of the associated compare_word1 register is clear, these bits become a direct 2-byte mask for the 2-byte compare register in bits [31:16]. |
| 16:31 | COMPARE_VALUE_TYPE2 | RW | R | 0 | 2 byte Compare Value.<br>If bit 9 of the associated compare_word1 register is set, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+2 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+3.<br>If bit 9 of the associated compare_word1 register is clear, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+0 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+1. |

### 11.3.312 ETH_TYPE2_COMPARE_31_WORD_1

**Description:** same as type2_compare_0_word_1
**Address:** 0x404817FC
**Offset:** 0x17FC
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | COMPARE_OFFSET [7:7] | OFFSET_VALUE [6:0] | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_10 [15:10] | | | | | | DISABLE_MASK [9:9] | COMPARE_OFFSET [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_10 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | RESERVED_31_10 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:6 | OFFSET_VALUE | RW | R | 0 | 'Offset value in bytes' |
| 7:8 | COMPARE_OFFSET | RW | R | 0 | 'Compare byte offset.<br>00 : Offset from beginning of the frame.<br>01 : Offset from byte after Ether Type.<br>10 : Offset from byte following end of IP header.<br>11 : Offset from byte following end of TCP/UDP header'<br><br>If bit 9 of the associated compare_word1 register is set, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+2 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+3.<br>If bit 9 of the associated compare_word1 register is clear, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+0 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+1. |
| 9 | DISABLE_MASK | RW | R | 0 | 'This bit is used to control whether the compare register word_0 contains a 4-byte compare value, or a 2-byte compare value with a 2-byte mask value.<br>1 - 4-byte compare value<br>0 - 2-byte compare, 2-byte mask ' |
| 10:31 | RESERVED_31_10 | R | R | 0 | 'Reserved, read as 0, ignored on write.' |

# 12 EVTGEN

**Description** Event generator
**Base Address** 0x403F0000
**Size** 0x1000
**Slave Num** MMIO3 - 4

| Register Name | Address | Permission | Description |
|---|---|---|---|
| EVTGEN0_CTL | 0x403F0000 | FULL | Control |
| EVTGEN0_COMP0_STATUS | 0x403F0004 | FULL | Comparator structures comparator 0 status |
| EVTGEN0_COMP1_STATUS | 0x403F0008 | FULL | Comparator structures comparator 1 status |
| EVTGEN0_COUNTER_STATUS | 0x403F0010 | FULL | Counter status |
| EVTGEN0_COUNTER | 0x403F0014 | FULL | Counter |
| EVTGEN0_RATIO_CTL | 0x403F0020 | FULL | Ratio control |
| EVTGEN0_RATIO | 0x403F0024 | FULL | Ratio |
| EVTGEN0_REF_CLOCK_CTL | 0x403F0030 | FULL | Reference clock control |
| EVTGEN0_INTR | 0x403F0700 | FULL | Interrupt |
| EVTGEN0_INTR_SET | 0x403F0704 | FULL | Interrupt set |
| EVTGEN0_INTR_MASK | 0x403F0708 | FULL | Interrupt mask |
| EVTGEN0_INTR_MASKED | 0x403F070C | FULL | Interrupt masked |
| EVTGEN0_INTR_DPSLP | 0x403F0710 | FULL | DeepSleep interrupt |
| EVTGEN0_INTR_DPSLP_SET | 0x403F0714 | FULL | DeepSleep interrupt set |
| EVTGEN0_INTR_DPSLP_MASK | 0x403F0718 | FULL | DeepSleep interrupt mask |
| EVTGEN0_INTR_DPSLP_MASKED | 0x403F071C | FULL | DeepSleep interrupt masked |

## 12.1 COMP_STRUCT 0

| Register Name | Address | Permission | Description |
|---|---|---|---|
| EVTGEN0_COMP_STRUCT0_COMP_CTL | 0x403F0800 | FULL | Comparator control |
| EVTGEN0_COMP_STRUCT0_COMP0 | 0x403F0804 | FULL | Comparator 0 (Active functionality) |
| EVTGEN0_COMP_STRUCT0_COMP1 | 0x403F0808 | FULL | Comparator 1 (DeepSleep functionality) |

## 12.2 COMP_STRUCT 1

| Register Name | Address | Permission | Description |
|---|---|---|---|
| EVTGEN0_COMP_STRUCT1_COMP_CTL | 0x403F0820 | FULL | Comparator control |
| EVTGEN0_COMP_STRUCT1_COMP0 | 0x403F0824 | FULL | Comparator 0 (Active functionality) |
| EVTGEN0_COMP_STRUCT1_COMP1 | 0x403F0828 | FULL | Comparator 1 (DeepSleep functionality) |

## 12.3 COMP_STRUCT 2

| Register Name | Address | Permission | Description |
|---|---|---|---|
| EVTGEN0_COMP_STRUCT2_COMP_CTL | 0x403F0840 | FULL | Comparator control |
| EVTGEN0_COMP_STRUCT2_COMP0 | 0x403F0844 | FULL | Comparator 0 (Active functionality) |
| EVTGEN0_COMP_STRUCT2_COMP1 | 0x403F0848 | FULL | Comparator 1 (DeepSleep functionality) |

## 12.4 COMP_STRUCT 3

| Register Name | Address | Permission | Description |
|---|---|---|---|
| EVTGEN0_COMP_STRUCT3_COMP_CTL | 0x403F0860 | FULL | Comparator control |
| EVTGEN0_COMP_STRUCT3_COMP0 | 0x403F0864 | FULL | Comparator 0 (Active functionality) |
| EVTGEN0_COMP_STRUCT3_COMP1 | 0x403F0868 | FULL | Comparator 1 (DeepSleep functionality) |

## 12.5 COMP_STRUCT 4

| Register Name | Address | Permission | Description |
|---|---|---|---|
| EVTGEN0_COMP_STRUCT4_COMP_CTL | 0x403F0880 | FULL | Comparator control |
| EVTGEN0_COMP_STRUCT4_COMP0 | 0x403F0884 | FULL | Comparator 0 (Active functionality) |
| EVTGEN0_COMP_STRUCT4_COMP1 | 0x403F0888 | FULL | Comparator 1 (DeepSleep functionality) |

## 12.6 COMP_STRUCT 5

| Register Name | Address | Permission | Description |
|---|---|---|---|
| EVTGEN0_COMP_STRUCT5_COMP_CTL | 0x403F08A0 | FULL | Comparator control |
| EVTGEN0_COMP_STRUCT5_COMP0 | 0x403F08A4 | FULL | Comparator 0 (Active functionality) |
| EVTGEN0_COMP_STRUCT5_COMP1 | 0x403F08A8 | FULL | Comparator 1 (DeepSleep functionality) |

## 12.7 COMP_STRUCT 6

| Register Name | Address | Permission | Description |
|---|---|---|---|
| EVTGEN0_COMP_STRUCT6_COMP_CTL | 0x403F08C0 | FULL | Comparator control |
| EVTGEN0_COMP_STRUCT6_COMP0 | 0x403F08C4 | FULL | Comparator 0 (Active functionality) |
| EVTGEN0_COMP_STRUCT6_COMP1 | 0x403F08C8 | FULL | Comparator 1 (DeepSleep functionality) |

## 12.8 COMP_STRUCT 7

| Register Name | Address | Permission | Description |
|---|---|---|---|
| EVTGEN0_COMP_STRUCT7_COMP_CTL | 0x403F08E0 | FULL | Comparator control |
| EVTGEN0_COMP_STRUCT7_COMP0 | 0x403F08E4 | FULL | Comparator 0 (Active functionality) |
| EVTGEN0_COMP_STRUCT7_COMP1 | 0x403F08E8 | FULL | Comparator 1 (DeepSleep functionality) |

## 12.9 COMP_STRUCT 8

| Register Name | Address | Permission | Description |
|---|---|---|---|
| EVTGEN0_COMP_STRUCT8_COMP_CTL | 0x403F0900 | FULL | Comparator control |
| EVTGEN0_COMP_STRUCT8_COMP0 | 0x403F0904 | FULL | Comparator 0 (Active functionality) |
| EVTGEN0_COMP_STRUCT8_COMP1 | 0x403F0908 | FULL | Comparator 1 (DeepSleep functionality) |

## 12.10 COMP_STRUCT 9

| Register Name | Address | Permission | Description |
|---|---|---|---|
| EVTGEN0_COMP_STRUCT9_COMP_CTL | 0x403F0920 | FULL | Comparator control |
| EVTGEN0_COMP_STRUCT9_COMP0 | 0x403F0924 | FULL | Comparator 0 (Active functionality) |
| EVTGEN0_COMP_STRUCT9_COMP1 | 0x403F0928 | FULL | Comparator 1 (DeepSleep functionality) |

## 12.11 COMP_STRUCT 10

| Register Name | Address | Permission | Description |
|---|---|---|---|
| EVTGEN0_COMP_STRUCT10_COMP_CTL | 0x403F0940 | FULL | Comparator control |
| EVTGEN0_COMP_STRUCT10_COMP0 | 0x403F0944 | FULL | Comparator 0 (Active functionality) |
| EVTGEN0_COMP_STRUCT10_COMP1 | 0x403F0948 | FULL | Comparator 1 (DeepSleep functionality) |

## 12.12 COMP_STRUCT 11

| Register Name | Address | Permission | Description |
|---|---|---|---|
| EVTGEN0_COMP_STRUCT11_COMP_CTL | 0x403F0960 | FULL | Comparator control |
| EVTGEN0_COMP_STRUCT11_COMP0 | 0x403F0964 | FULL | Comparator 0 (Active functionality) |
| EVTGEN0_COMP_STRUCT11_COMP1 | 0x403F0968 | FULL | Comparator 1 (DeepSleep functionality) |

## 12.13 COMP_STRUCT 12

| Register Name | Address | Permission | Description |
|---|---|---|---|
| EVTGEN0_COMP_STRUCT12_COMP_CTL | 0x403F0980 | FULL | Comparator control |
| EVTGEN0_COMP_STRUCT12_COMP0 | 0x403F0984 | FULL | Comparator 0 (Active functionality) |
| EVTGEN0_COMP_STRUCT12_COMP1 | 0x403F0988 | FULL | Comparator 1 (DeepSleep functionality) |

## 12.14 COMP_STRUCT 13

| Register Name | Address | Permission | Description |
|---|---|---|---|
| EVTGEN0_COMP_STRUCT13_COMP_CTL | 0x403F09A0 | FULL | Comparator control |
| EVTGEN0_COMP_STRUCT13_COMP0 | 0x403F09A4 | FULL | Comparator 0 (Active functionality) |
| EVTGEN0_COMP_STRUCT13_COMP1 | 0x403F09A8 | FULL | Comparator 1 (DeepSleep functionality) |

## 12.15 COMP_STRUCT 14

| Register Name | Address | Permission | Description |
|---|---|---|---|
| EVTGEN0_COMP_STRUCT14_COMP_CTL | 0x403F09C0 | FULL | Comparator control |
| EVTGEN0_COMP_STRUCT14_COMP0 | 0x403F09C4 | FULL | Comparator 0 (Active functionality) |
| EVTGEN0_COMP_STRUCT14_COMP1 | 0x403F09C8 | FULL | Comparator 1 (DeepSleep functionality) |

## 12.16 COMP_STRUCT 15

| Register Name | Address | Permission | Description |
|---|---|---|---|
| EVTGEN0_COMP_STRUCT15_COMP_CTL | 0x403F09E0 | FULL | Comparator control |
| EVTGEN0_COMP_STRUCT15_COMP0 | 0x403F09E4 | FULL | Comparator 0 (Active functionality) |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| EVTGEN0_COMP_STRUCT15_COMP1 | 0x403F09E8 | FULL | Comparator 1 (DeepSleep functionality) |

## 12.17 Register Details

### 12.17.1 EVTGEN_CTL

**Description:** Control
**Address:** 0x403F0000
**Offset:** 0x0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | ENABLED [31:31] | None [30:24] | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 31 | ENABLED | RW | R | 0 | IP enable:<br>'0': Disabled. All non-retention registers (command and status registers) are reset to their default value when the IP is disabled. All retention registers retain their value when the IP is disabled.<br>'1': Enabled. |
| | DISABLED | | | 0 | N/A |
| | ENABLED | | | 1 | N/A |

### 12.17.2 EVTGEN_COMP0_STATUS

**Description:** Comparator structures comparator 0 status
**Address:** 0x403F0004
**Offset:** 0x4
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | COMP0_OUT [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | COMP0_OUT [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | COMP0_OUT | R | W | 0 | Active comparator 'comp0_out[]' outputs. |

### 12.17.3 EVTGEN_COMP1_STATUS

**Description:** Comparator structures comparator 1 status
**Address:** 0x403F0008
**Offset:** 0x8
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | COMP1_OUT [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | COMP1_OUT [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | COMP1_OUT | R | W | 0 | DeepSleep comparator 'comp1_out_lf[]' outputs (synchronized from clk_lf to the IP clock). |

### 12.17.4 EVTGEN_COUNTER_STATUS

**Description:** Counter status
**Address:** 0x403F0010
**Offset:** 0x10
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALID [31:31] | None [30:24] | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 31 | VALID | R | W | 0 | Active counter validity:<br>'0': Invalid.<br>'1': Valid.<br><br>The COUNTER register field INT32 is only valid when VALID is '1'.<br><br>The COUNTER_STATUS and COUNTER registers are non-retention registers; i.e. the COUNTER_STATUS and COUNTER registers are reset during DeepSleep power mode. After entering the Active power mode, the Active counter is initialized with the DeepSleep counter. This initialization may take up to 1 clk_lf cycle. |

### 12.17.5 EVTGEN_COUNTER

**Description:** Counter
**Address:** 0x403F0014
**Offset:** 0x14
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** Undefined as one or more bit fields have a default value that is undefined

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | INT32 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | INT32 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | INT32 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | INT32 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | INT32 | R | W | Undefined | Active counter 'counter_int[31:0]' on clk_ref_div. |

### 12.17.6 EVTGEN_RATIO_CTL

**Description:** Ratio control
**Address:** 0x403F0020
**Offset:** 0x20
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:19] | | | | | DYNAMIC_MODE [18:16] | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALID [31:31] | DYNAMIC [30:30] | None [29:24] | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 16:18 | DYNAMIC_MODE | RW | R | 0 | Weighted average calculation (only used when DYNAMIC is '1'):<br>'0': new RATIO value = (RATIO + measurement + 1) / 2.<br>'1': new RATIO value = (3*RATIO + measurement + 2) / 4.<br>'2': new RATIO value = (7*RATIO + measurement + 4) / 8.<br>'3': new RATIO value = (15*RATIO + measurement + 8) / 16.<br>'4': new RATIO value = (31*RATIO + measurement + 16) / 32.<br>'5': new RATIO value = (63*RATIO + measurement + 32) / 64.<br>'6': new RATIO value = (127*RATIO + measurement + 64) / 128.<br>'7': new RATIO value = (255*RATIO + measurement + 128) / 256.<br><br>Note: 'measurement' (integer component only) is defined as: 256 * 'number of measured clk_ref_div cycles per clk_lf cycle'. The RATIO value (integer and fractional component) is defined as: 256*RATIO.INT16 + RATIO.FRAC8 (RATIO.INT16 = RATIO >> 8 and RATIO.FRAC8 = RATIO percent 256). |
| 30 | DYNAMIC | RW | R | 0 | Specifies if RATIO_CTL.VALID and RATIO are under SW or HW control:<br>'0': SW control.<br>'1: HW control. Auto calibration is used to derive the RATIO value. HW measures the number of clk_ref_div cycles per clk_lf cycle. This measurement is combined with the current ratio value to calculate a new ratio value. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 31 | VALID | RW | RW1S | 0 | Ratio value valid:<br>'0': Invalid.<br>'1': Valid.<br><br>The RATIO register fields INT16 and FRAC8 are only valid when VALID is '1'. |

### 12.17.7 EVTGEN_RATIO

**Description:** Ratio
**Address:** 0x403F0024
**Offset:** 0x24
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register contains a ratio value expressing the relative frequency of the DeepSleep clock clk_lf wrt. the Active clock clk_ref_div. Specifically, this registers contains the average number of clk_ref_div cycles per clk_lf cycle.
**Default:** Undefined as one or more bit fields have a default value that is undefined

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | FRAC8 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | INT16 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | INT16 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 8:15 | FRAC8 | RW | RW | Undefined | Fractional component of ratio value. |
| 16:31 | INT16 | RW | RW | Undefined | Integer component of ratio value. |

### 12.17.8 EVTGEN_REF_CLOCK_CTL

**Description:** Reference clock control
**Address:** 0x403F0030
**Offset:** 0x30
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | INT_DIV [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | INT_DIV | RW | R | 0 | Divider control for clk_ref_div:<br>'0': Divide by 1.<br>...<br>'255': Divide by '256'.<br><br>Fclk_ref_div = Fclk_ref / (INT_DIV + 1) |

### 12.17.9 EVTGEN_INTR

**Description:** Interrupt
**Address:** 0x403F0700
**Offset:** 0x700
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | COMP0 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | COMP0 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | COMP0 | RW1C | RW1S | 0 | This interrupt cause field is activated (HW sets the field to '1') when a comparator 0 event is generated (Active counter 'counter_int[31:0]' becomes greater or equal to COMP0.INT[31:0]). |

### 12.17.10 EVTGEN_INTR_SET

**Description:** Interrupt set
**Address:** 0x403F0704
**Offset:** 0x704
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** When read, this register reflects the INTR register. For debug purposes, SW can write a '1' to activate a specific interrupt cause (this allows for debug of the SW ISR, without relying on HW to activate the interrupt cause).

The interrupt causes are deactivated when the IP is disabled (CTL.ENABLED is '0').
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | COMP0 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | COMP0 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | COMP0 | RW1S | A | 0 | SW writes a '1' to this field to set the corresponding field in the INTR register. |

### 12.17.11 EVTGEN_INTR_MASK

**Description:** Interrupt mask
**Address:** 0x403F0708
**Offset:** 0x708
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | COMP0 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | COMP0 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | COMP0 | RW | R | 0 | Mask bit for corresponding field in the INTR register. |

### 12.17.12 EVTGEN_INTR_MASKED

**Description:** Interrupt masked
**Address:** 0x403F070C
**Offset:** 0x70C
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** When read, this register reflects 'a bitwise AND' between the INTR and INTR_MASK registers.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | COMP0 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | COMP0 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | COMP0 | R | W | 0 | Logical and of corresponding INTR and INTR_MASK fields. |

### 12.17.13 EVTGEN_INTR_DPSLP

**Description:** DeepSleep interrupt
**Address:** 0x403F0710
**Offset:** 0x710
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** The interrupt causes are deactivated when the IP is disabled (CTL.ENABLED is '0').
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | COMP1 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | COMP1 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | COMP1 | RW1C | A | 0 | This interrupt cause field is activated (HW sets the field to '1') when a comparator 1 event is generated (DeepSleep counter 'counter_int_lf[31:0]' becomes greater or equal to COMP1.INT[31:0]). |

### 12.17.14 EVTGEN_INTR_DPSLP_SET

**Description:** DeepSleep interrupt set
**Address:** 0x403F0714
**Offset:** 0x714
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** When read, this register reflects the INTR register. For debug purposes, SW can write a '1' to activate a specific interrupt cause (this allows for debug of the SW ISR, without relying on HW to activate the interrupt cause).
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | COMP1 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | COMP1 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | COMP1 | RW1S | A | 0 | SW writes a '1' to this field to set the corresponding field in the INTR register. |

### 12.17.15 EVTGEN_INTR_DPSLP_MASK

**Description:** DeepSleep interrupt mask
**Address:** 0x403F0718
**Offset:** 0x718
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | COMP1 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | COMP1 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | COMP1 | RW | R | 0 | Mask bit for corresponding field in the INTR register. |

### 12.17.16 EVTGEN_INTR_DPSLP_MASKED

**Description:** DeepSleep interrupt masked
**Address:** 0x403F071C
**Offset:** 0x71C
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** When read, this register reflects 'a bitwise AND' between the INTR and INTR_MASK registers.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | COMP1 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | COMP1 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | COMP1 | R | W | 0 | Logical and of corresponding INTR and INTR_MASK fields. |

### 12.17.17 COMP_STRUCT

#### 12.17.17.1 EVTGEN_COMP_STRUCT_COMP_CTL

**Description:** Comparator control
**Address:** 0x403F0800
**Offset:** 0x0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:2] | | | | | | COMP1_EN [1:1] | COMP0_EN [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:17] | | | | | | | TR_OUT_EDGE [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | ENABLED [31:31] | None [30:24] | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | COMP0_EN | RW | R | 0 | Active comparator (COMP0) enable:<br>'0': Disabled. The comparator output 'comp0_out' is '0'.<br>'1': Enabled. |
| 1 | COMP1_EN | RW | R | 0 | DeepSleep comparator (COMP1) enable:<br>'0': Disabled. The comparator output 'comp1_out_lf' is '0'.<br>'1': Enabled. |
| 16 | TR_OUT_EDGE | RW | R | 0 | Specifies the 'tr_out' output trigger:<br>'0': The trigger is a level sensitive trigger. The Active comparator output ('comp0_out') is reflected on 'tr_out'.<br>'1': The trigger is an edge sensitive trigger. Activation of the Active comparator output (rising edge on 'comp0_out') results in a two cycle '1'/high pulse on 'tr_out'. |
| 31 | ENABLED | RW | R | 0 | Comparator structure enable:<br>'0': Disabled.<br>'1': Enabled. |

### 12.17.17.2 EVTGEN_COMP_STRUCT_COMP0

**Description:** Comparator 0 (Active functionality)
**Address:** 0x403F0804
**Offset:** 0x4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** Undefined as one or more bit fields have a default value that is undefined

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | INT32 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | INT32 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | INT32 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | INT32 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | INT32 | RW | R | Undefined | This value is a 32-bit unsigned integer in the range [0, 2^32-1]. The comparator 'comp0_out' output is activated when the Active counter 'counter_int[31:0]' becomes greater or equal to COMP0.<br><br>Note: SW must ensure that COMP_CTL.COMP_EN[0] is '0' when COMP0 is written. |

### 12.17.17.3 EVTGEN_COMP_STRUCT_COMP1

**Description:** Comparator 1 (DeepSleep functionality)
**Address:** 0x403F0808
**Offset:** 0x8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** Undefined as one or more bit fields have a default value that is undefined

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | INT32 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | INT32 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | INT32 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | INT32 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | INT32 | RW | R | Undefined | This value is a 32-bit unsigned integer in the range [0, 2^32-1]. The comparator 'comp1_out_lf' output is activated when the DeepSleep counter 'counter_int_lf[31:0]' becomes greater or equal to COMP1.<br><br>Note: SW must ensure that COMP_CTL.COMP_EN[1] is '0' when COMP1 is written. |

# 13 FAULT

**Description** Fault structures
**Base Address** 0x40210000
**Size** 0x10000
**Slave Num** MMIO2 - 1

## 13.1 STRUCT 0

| Register Name | Address | Permission | Description |
|---|---|---|---|
| FAULT_STRUCT0_CTL | 0x40210000 | FULL | Fault control |
| FAULT_STRUCT0_STATUS | 0x4021000C | FULL | Fault status |
| FAULT_STRUCT0_DATA0 | 0x40210010 | FULL | Fault data |
| FAULT_STRUCT0_DATA1 | 0x40210014 | FULL | Fault data |
| FAULT_STRUCT0_DATA2 | 0x40210018 | FULL | Fault data |
| FAULT_STRUCT0_DATA3 | 0x4021001C | FULL | Fault data |
| FAULT_STRUCT0_PENDING0 | 0x40210040 | FULL | Fault pending 0 |
| FAULT_STRUCT0_PENDING1 | 0x40210044 | FULL | Fault pending 1 |
| FAULT_STRUCT0_PENDING2 | 0x40210048 | FULL | Fault pending 2 |
| FAULT_STRUCT0_MASK0 | 0x40210050 | FULL | Fault mask 0 |
| FAULT_STRUCT0_MASK1 | 0x40210054 | FULL | Fault mask 1 |
| FAULT_STRUCT0_MASK2 | 0x40210058 | FULL | Fault mask 2 |
| FAULT_STRUCT0_INTR | 0x402100C0 | FULL | Interrupt |
| FAULT_STRUCT0_INTR_SET | 0x402100C4 | FULL | Interrupt set |
| FAULT_STRUCT0_INTR_MASK | 0x402100C8 | FULL | Interrupt mask |
| FAULT_STRUCT0_INTR_MASKED | 0x402100CC | FULL | Interrupt masked |

## 13.2 STRUCT 1

| Register Name | Address | Permission | Description |
|---|---|---|---|
| FAULT_STRUCT1_CTL | 0x40210100 | FULL | Fault control |
| FAULT_STRUCT1_STATUS | 0x4021010C | FULL | Fault status |
| FAULT_STRUCT1_DATA0 | 0x40210110 | FULL | Fault data |
| FAULT_STRUCT1_DATA1 | 0x40210114 | FULL | Fault data |
| FAULT_STRUCT1_DATA2 | 0x40210118 | FULL | Fault data |
| FAULT_STRUCT1_DATA3 | 0x4021011C | FULL | Fault data |
| FAULT_STRUCT1_PENDING0 | 0x40210140 | FULL | Fault pending 0 |
| FAULT_STRUCT1_PENDING1 | 0x40210144 | FULL | Fault pending 1 |
| FAULT_STRUCT1_PENDING2 | 0x40210148 | FULL | Fault pending 2 |
| FAULT_STRUCT1_MASK0 | 0x40210150 | FULL | Fault mask 0 |
| FAULT_STRUCT1_MASK1 | 0x40210154 | FULL | Fault mask 1 |
| FAULT_STRUCT1_MASK2 | 0x40210158 | FULL | Fault mask 2 |
| FAULT_STRUCT1_INTR | 0x402101C0 | FULL | Interrupt |
| FAULT_STRUCT1_INTR_SET | 0x402101C4 | FULL | Interrupt set |
| FAULT_STRUCT1_INTR_MASK | 0x402101C8 | FULL | Interrupt mask |
| FAULT_STRUCT1_INTR_MASKED | 0x402101CC | FULL | Interrupt masked |

## 13.3 STRUCT 2

| Register Name | Address | Permission | Description |
|---|---|---|---|
| FAULT_STRUCT2_CTL | 0x40210200 | FULL | Fault control |
| FAULT_STRUCT2_STATUS | 0x4021020C | FULL | Fault status |
| FAULT_STRUCT2_DATA0 | 0x40210210 | FULL | Fault data |
| FAULT_STRUCT2_DATA1 | 0x40210214 | FULL | Fault data |
| FAULT_STRUCT2_DATA2 | 0x40210218 | FULL | Fault data |
| FAULT_STRUCT2_DATA3 | 0x4021021C | FULL | Fault data |
| FAULT_STRUCT2_PENDING0 | 0x40210240 | FULL | Fault pending 0 |
| FAULT_STRUCT2_PENDING1 | 0x40210244 | FULL | Fault pending 1 |
| FAULT_STRUCT2_PENDING2 | 0x40210248 | FULL | Fault pending 2 |
| FAULT_STRUCT2_MASK0 | 0x40210250 | FULL | Fault mask 0 |
| FAULT_STRUCT2_MASK1 | 0x40210254 | FULL | Fault mask 1 |
| FAULT_STRUCT2_MASK2 | 0x40210258 | FULL | Fault mask 2 |
| FAULT_STRUCT2_INTR | 0x402102C0 | FULL | Interrupt |
| FAULT_STRUCT2_INTR_SET | 0x402102C4 | FULL | Interrupt set |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| FAULT_STRUCT2_INTR_MASK | 0x402102C8 | FULL | Interrupt mask |
| FAULT_STRUCT2_INTR_MASKED | 0x402102CC | FULL | Interrupt masked |

## 13.4 STRUCT 3

| Register Name | Address | Permission | Description |
|---|---|---|---|
| FAULT_STRUCT3_CTL | 0x40210300 | FULL | Fault control |
| FAULT_STRUCT3_STATUS | 0x4021030C | FULL | Fault status |
| FAULT_STRUCT3_DATA0 | 0x40210310 | FULL | Fault data |
| FAULT_STRUCT3_DATA1 | 0x40210314 | FULL | Fault data |
| FAULT_STRUCT3_DATA2 | 0x40210318 | FULL | Fault data |
| FAULT_STRUCT3_DATA3 | 0x4021031C | FULL | Fault data |
| FAULT_STRUCT3_PENDING0 | 0x40210340 | FULL | Fault pending 0 |
| FAULT_STRUCT3_PENDING1 | 0x40210344 | FULL | Fault pending 1 |
| FAULT_STRUCT3_PENDING2 | 0x40210348 | FULL | Fault pending 2 |
| FAULT_STRUCT3_MASK0 | 0x40210350 | FULL | Fault mask 0 |
| FAULT_STRUCT3_MASK1 | 0x40210354 | FULL | Fault mask 1 |
| FAULT_STRUCT3_MASK2 | 0x40210358 | FULL | Fault mask 2 |
| FAULT_STRUCT3_INTR | 0x402103C0 | FULL | Interrupt |
| FAULT_STRUCT3_INTR_SET | 0x402103C4 | FULL | Interrupt set |
| FAULT_STRUCT3_INTR_MASK | 0x402103C8 | FULL | Interrupt mask |
| FAULT_STRUCT3_INTR_MASKED | 0x402103CC | FULL | Interrupt masked |

## 13.5 Register Details

### 13.5.1 STRUCT

#### 13.5.1.1 FAULT_STRUCT_CTL

**Description:** Fault control
**Address:** 0x40210000
**Offset:** 0x0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register uses DeepSleep reset. Therefore, a DeepSleep reset (possibly as a result of CTL.RESET_EN) resets this register (including setting CTL.RESET_EN to '0').
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:3] | | | | | RESET_REQ_EN [2:2] | OUT_EN [1:1] | TR_EN [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | TR_EN | RW | R | 0 | Trigger output enable:<br>'0': Disabled. The trigger output 'tr_fault' is '0'.<br>'1': Enabled. The trigger output 'tr_fault' reflects STATUS.VALID. The trigger can be used to initiate a Datawire transfer of the FAULT data (FAULT_DATA0 through FAULT_DATA3). |
| 1 | OUT_EN | RW | R | 0 | IO output signal enable:<br>'0': Disabled. The IO output signal 'fault_out' is '0'. The IO output enable signal 'fault_out_en' is '0'.<br>'1': Enabled. The IO output signal 'fault_out' reflects STATUS.VALID. The IO output enable signal 'fault_out_en' is '1'. |
| 2 | RESET_REQ_EN | RW | R | 0 | Reset request enable:<br>'0': Disabled.<br>'1': Enabled. The output reset request signal 'fault_reset_req' reflects STATUS.VALID. This reset causes a warm/soft/core reset. This warm/soft/core reset does not affect the fault logic STATUS, DATA0, ..., DATA3 registers (allowing for post soft reset failure analysis).<br><br>The 'fault_reset_req' signals of the individual fault report structures are combined (logically OR'd) into a single SRSS 'fault_reset_req' signal. |

### 13.5.1.2 FAULT_STRUCT_STATUS

**Description:** Fault status
**Address:** 0x4021000C
**Offset:** 0xC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register uses cold reset (and is NOT affected by Active or DeepSleep reset). This allows for failure analysis after a warm reset (DeepSleep reset).
**Default:** Undefined as one or more bit fields have a default value that is undefined

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:7] | IDX [6:0] | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALID [31:31] | None [30:24] | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:6 | IDX | RW | W | Undefined | The fault source index for which fault information is captured in DATA0 through DATA3. The fault information is fault source specific and described below.<br><br>Note: this register field (and associated fault source data in DATA0 through DATA3) should only be considered valid, when VALID is '1'. |
| | MPU_0 | | | 0 | Bus master 0 MPU/SMPU.<br>DATA0[31:0]: Violating address.<br>DATA1[0]: User read.<br>DATA1[1]: User write.<br>DATA1[2]: User execute.<br>DATA1[3]: Privileged read.<br>DATA1[4]: Privileged write.<br>DATA1[5]: Privileged execute.<br>DATA1[6]: Non-secure.<br>DATA1[11:8]: Master identifier.<br>DATA1[15:12]: Protection context identifier.<br>DATA1[31]: '0' MPU violation; '1': SMPU violation. |
| | MPU_1 | | | 1 | Bus master 1 MPU. See MPU_0 description. |
| | MPU_2 | | | 2 | Bus master 2 MPU. See MPU_0 description. |
| | MPU_3 | | | 3 | Bus master 3 MPU. See MPU_0 description. |
| | MPU_4 | | | 4 | Bus master 4 MPU. See MPU_0 description. |
| | MPU_5 | | | 5 | Bus master 5 MPU. See MPU_0 description. |
| | MPU_6 | | | 6 | Bus master 6 MPU. See MPU_0 description. |
| | MPU_7 | | | 7 | Bus master 7 MPU. See MPU_0 description. |
| | MPU_8 | | | 8 | Bus master 8 MPU. See MPU_0 description. |
| | MPU_9 | | | 9 | Bus master 9 MPU. See MPU_0 description. |
| | MPU_10 | | | 10 | Bus master 10 MPU. See MPU_0 description. |
| | MPU_11 | | | 11 | Bus master 11 MPU. See MPU_0 description. |
| | MPU_12 | | | 12 | Bus master 12 MPU. See MPU_0 description. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| | MPU_13 | | | 13 | Bus master 13 MPU. See MPU_0 description. |
| | MPU_14 | | | 14 | Bus master 14 MPU. See MPU_0 description. |
| | MPU_15 | | | 15 | Bus master 15 MPU. See MPU_0 description. |
| | CM7_1_TCM_C_ECC | | | 16 | Correctable ECC error in CM7_1 TCM memory. See CM7_0_TCM_C_ECC description. |
| | CM7_1_TCM_NC_ECC | | | 17 | Non Correctable ECC error in CM7_1 TCM memory. See CM7_0_TCM_C_ECC description. |
| | CM7_0_CACHE_C_ECC | | | 18 | Correctable ECC error in CM7_0 Cache memories<br>DATA0[16:2]: location information: Tag/Data SRAM, Way, Index and line Offset, see CM7 UGRM IEBR0/DEBR0 description for details.<br>DATA0[31]: 0=Instruction cache, 1= Data cache |
| | CM7_0_CACHE_NC_ECC | | | 19 | Non Correctable ECC error in CM7_0 Cache memories. See CM7_0_CACHE_C_ECC description |
| | CM7_1_CACHE_C_ECC | | | 20 | Correctable ECC error in CM7_1 Cache memories. See CM7_0_CACHE_C_ECC description. |
| | CM7_1_CACHE_NC_ECC | | | 21 | Non Correctable ECC error in CM7_1 Cache memories. See CM7_0_CACHE_C_ECC description. |
| | MS_PPU_4 | | | 25 | Peripheral interconnect, master interface 4 PPU. See MS_PPU_0 description. |
| | PERI_ECC | | | 26 | Peripheral interconnect, protection structures SRAM, correctable ECC error:<br>DATA0[10:0]: Violating address.<br>DATA1[7:0]: Syndrome of SRAM word. |
| | PERI_NC_ECC | | | 27 | Peripheral interconnect, protection structures SRAM, non-correctable ECC error. |
| | MS_PPU_0 | | | 28 | Peripheral interconnect, master interface 0 PPU.<br>DATA0[31:0]: Violating address.<br>DATA1[0]: User read.<br>DATA1[1]: User write.<br>DATA1[2]: User execute.<br>DATA1[3]: Privileged read.<br>DATA1[4]: Privileged write.<br>DATA1[5]: Privileged execute.<br>DATA1[6]: Non-secure.<br>DATA1[11:8]: Master identifier.<br>DATA1[15:12]: Protection context identifier.<br>DATA1[31:28]: '0': master interface, PPU violation, '1': timeout detected, '2': bus error, other: undefined. |
| | MS_PPU_1 | | | 29 | Peripheral interconnect, master interface 1 PPU. See MS_PPU_0 description. |
| | MS_PPU_2 | | | 30 | Peripheral interconnect, master interface 2 PPU. See MS_PPU_0 description. |
| | MS_PPU_3 | | | 31 | Peripheral interconnect, master interface 3 PPU. See MS_PPU_0 description. |
| | GROUP_FAULT_0 | | | 32 | Peripheral group 0 fault detection.<br>DATA0[31:0]: Violating address.<br>DATA1[0]: User read.<br>DATA1[1]: User write.<br>DATA1[2]: User execute.<br>DATA1[3]: Privileged read.<br>DATA1[4]: Privileged write.<br>DATA1[5]: Privileged execute.<br>DATA1[6]: Non-secure.<br>DATA1[11:8]: Master identifier.<br>DATA1[15:12]: Protection context identifier.<br>DATA1[31:28]: '0': decoder or peripheral bus error, other: undefined. |
| | GROUP_FAULT_1 | | | 33 | Peripheral group 1 fault detection. See GROUP_FAULT_0 description. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| | GROUP_FAULT_2 | | | 34 | Peripheral group 2 fault detection. See GROUP_FAULT_0 description. |
| | GROUP_FAULT_3 | | | 35 | Peripheral group 3 fault detection. See GROUP_FAULT_0 description. |
| | GROUP_FAULT_4 | | | 36 | Peripheral group 4 fault detection. See GROUP_FAULT_0 description. |
| | GROUP_FAULT_5 | | | 37 | Peripheral group 5 fault detection. See GROUP_FAULT_0 description. |
| | GROUP_FAULT_6 | | | 38 | Peripheral group 6 fault detection. See GROUP_FAULT_0 description. |
| | GROUP_FAULT_7 | | | 39 | Peripheral group 7 fault detection. See GROUP_FAULT_0 description. |
| | GROUP_FAULT_8 | | | 40 | Peripheral group 8 fault detection. See GROUP_FAULT_0 description. |
| | GROUP_FAULT_9 | | | 41 | Peripheral group 9 fault detection. See GROUP_FAULT_0 description. |
| | GROUP_FAULT_10 | | | 42 | Peripheral group 10 fault detection. See GROUP_FAULT_0 description. |
| | GROUP_FAULT_11 | | | 43 | Peripheral group 11 fault detection. See GROUP_FAULT_0 description. |
| | GROUP_FAULT_12 | | | 44 | Peripheral group 12 fault detection. See GROUP_FAULT_0 description. |
| | GROUP_FAULT_13 | | | 45 | Peripheral group 13 fault detection. See GROUP_FAULT_0 description. |
| | GROUP_FAULT_14 | | | 46 | Peripheral group 14 fault detection. See GROUP_FAULT_0 description. |
| | GROUP_FAULT_15 | | | 47 | Peripheral group 15 fault detection. See GROUP_FAULT_0 description. |
| | FLASHC_MAIN_BUS_ERROR | | | 48 | Flash controller, main interface, bus error:<br>FAULT_DATA0[26:0]: Violating address. Append 5'b00010 as most significant bits to derive 32-bit system address.<br>FAULT_DATA1[11:8]: Master identifier. |
| | FLASHC_MAIN_C_ECC | | | 49 | Flash controller, main interface, correctable ECC error:<br>DATA[26:0]: Violating address. Append 5'b00010 as most significant bits to derive 32-bit system address.<br>DATA1[7:0]: Syndrome of 64-bit word (at address offset 0x00).<br>DATA1[15:8]: Syndrome of 64-bit word (at address offset 0x08).<br>DATA1[23:16]: Syndrome of 64-bit word (at address offset 0x10).<br>DATA1[31:24]: Syndrome of 64-bit word (at address offset 0x18). |
| | FLASHC_MAIN_NC_ECC | | | 50 | Flash controller, main interface, non-correctable ECC error. See FLASHC_MAIN_C_ECC description. |
| | FLASHC_WORK_BUS_ERROR | | | 51 | Flash controller, work interface, bus error. See FLASHC_MAIN_BUS_ERROR description. |
| | FLASHC_WORK_C_ECC | | | 52 | Flash controller, work interface, correctable ECC error:<br>DATA0[26:0]: Violating address. Append 5'b00010 as most significant bits to derive 32-bit system address.<br>DATA1[6:0]: Syndrome of 32-bit word. |
| | FLASHC_WORK_NC_ECC | | | 53 | Flash controller, work interface, non-correctable ECC error. See FLASHC_WORK_C_ECC description. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| | FLASHC_CM0_CA_C_ECC | | | 54 | Flash controller, CM0+ cache, correctable ECC error:<br>DATA0[26:0]: Violating address.<br>DATA1[6:0]: Syndrome of 32-bit SRAM word (at address offset 0x0).<br>DATA1[14:8]: Syndrome of 32-bit SRAM word (at address offset 0x4).<br>DATA1[22:16]: Syndrome of 32-bit SRAM word (at address offset 0x8).<br>DATA1[30:24]: Syndrome of 32-bit SRAM word (at address offset 0xc). |
| | FLASHC_CM0_CA_NC_ECC | | | 55 | Flash controller, CM0+ cache, non-correctable ECC error. See FLASHC_CM0_CA_C_ECC description. |
| | CM7_0_TCM_C_ECC | | | 56 | Correctable ECC error in CM7_0 TCM memory<br>DATA0[23:2]: Violating address.<br>DATA1[7:0]: Syndrome of code word (at address offset 0x0).<br>DATA1[31:30]: 0= ITCM, 2=D0TCM, 3=D1TCM |
| | CM7_0_TCM_NC_ECC | | | 57 | Non Correctable ECC error in CM7_0 TCM memory. See CM7_0_TCM_C_ECC description. |
| | RAMC0_C_ECC | | | 58 | System SRAM 0 correctable ECC error:<br>DATA0[31:0]: Violating address.<br>DATA1[6:0]: Syndrome of 32-bit SRAM code word. |
| | RAMC0_NC_ECC | | | 59 | System SRAM 0 non-correctable ECC error. See RAMC0_C_ECC description. |
| | RAMC1_C_ECC | | | 60 | System SRAM 1 correctable ECC error. See RAMC0_C_ECC description. |
| | RAMC1_NC_ECC | | | 61 | System SRAM 1 non-correctable ECC error. See RAMC0_C_ECC description. |
| | RAMC2_C_ECC | | | 62 | System SRAM 2 correctable ECC error. See RAMC0_C_ECC description. |
| | RAMC2_NC_ECC | | | 63 | System SRAM 2 non-correctable ECC error. See RAMC0_C_ECC description. |
| | CRYPTO_C_ECC | | | 64 | Cryptography SRAM correctable ECC error.<br>DATA0[31:0]: Violating address.<br>DATA1[6:0]: Syndrome of Least Significant 32-bit SRAM.<br>DATA1[14:8]: Syndrome of Most Significant 32-bit SRAM. |
| | CRYPTO_NC_ECC | | | 65 | Cryptography SRAM non-correctable ECC error. See CRYPTO_C_ECC description. |
| | DW0_C_ECC | | | 70 | DataWire 0 SRAM 1 correctable ECC error:<br>DATA0[11:0]: Violating DW SRAM address (word address, assuming byte addressable).<br>DATA1[6:0]: Syndrome of 32-bit SRAM code word. |
| | DW0_NC_ECC | | | 71 | DataWire 0 SRAM 1 non-correctable ECC error. See DW0_C_ECC description. |
| | DW1_C_ECC | | | 72 | DataWire 1 SRAM 1 correctable ECC error. See DW0_C_ECC description. |
| | DW1_NC_ECC | | | 73 | DataWire 1 SRAM 1 non-correctable ECC error. See DW0_C_ECC description. |
| | FM_SRAM_C_ECC | | | 74 | eCT Flash SRAM (for embedded operations) correctable ECC error:<br>DATA0[15:0]: Address location in the eCT Flash SRAM.<br>DATA1[6:0]: Syndrome of 32-bit SRAM word. |
| | FM_SRAM_NC_ECC | | | 75 | eCT Flash SRAM non-correctable ECC error: See FM_SRAM_C_ECC description. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| | CAN0_C_ECC | | | 80 | CAN controller 0 MRAM correctable ECC error:<br>DATA0[15:0]: Violating address.<br>DATA0[22:16]: ECC violating data[38:32] from MRAM.<br>DATA0[27:24]: Master ID: 0-7 = CAN channel ID within mxttcanfd cluster, 8 = AHB I/F<br>DATA1[31:0]: ECC violating data[31:0] from MRAM. |
| | CAN0_NC_ECC | | | 81 | CAN controller 0 MRAM non-correctable ECC error:<br>DATA0[15:0]: Violating address.<br>DATA0[22:16]: ECC violating data[38:32] from MRAM (not for Address Error).<br>DATA0[27:24]: Master ID: 0-7 = CAN channel ID within mxttcanfd cluster, 8 = AHB I/F<br>DATA0[30]: Write access, only possible for Address Error<br>DATA0[31]: Address Error: a CAN channel did an MRAM access above MRAM_SIZE<br>DATA1[31:0]: ECC violating data[31:0] from MRAM (not for Address Error). |
| | CAN1_C_ECC | | | 82 | CAN controller 1 MRAM correctable ECC error. See CAN0_C_ECC description. |
| | CAN1_NC_ECC | | | 83 | CAN controller 1 MRAM non-correctable ECC error. See CAN0_NC_ECC description. |
| | VIDEOSS_VRPU0 | | | 84 | Video Ram Protection Unit 0 fault detection.<br>DATA0[31:0]: Violating address.<br>DATA1[0]: User read.<br>DATA1[1]: User write.<br>DATA1[2]: User execute.<br>DATA1[3]: Privileged read.<br>DATA1[4]: Privileged write.<br>DATA1[5]: Privileged execute.<br>DATA1[6]: Non-secure.<br>DATA1[11:8]: Master identifier.<br>DATA1[15:12]: Protection context identifier.<br>DATA1[31:28]: '0': decoder or peripheral bus error, other: undefined. |
| | VIDEOSS_VRPU1 | | | 85 | Video Ram Protection Unit 1 fault detection. See VIDEOSS_VRPU0 description. |
| | VIDEOSS_VRPU2 | | | 86 | Video Ram Protection Unit 2 fault detection. See VIDEOSS_VRPU0 description. |
| | VIDEOSS_VRPU3 | | | 87 | Video Ram Protection Unit 3 fault detection. See VIDEOSS_VRPU0 description. |
| | VIDEOSS_VRPU4 | | | 88 | Video Ram Protection Unit 4 fault detection. See VIDEOSS_VRPU0 description. |
| | VIDEOSS_VRPU5 | | | 89 | Video Ram Protection Unit 5 fault detection. See VIDEOSS_VRPU0 description. |
| | SRSS_CSV | | | 90 | SRSS Clock SuperVisor (CSV) violation detected. Multiple CSV can detect a violation at the same time.<br>DATA0[15:0]: clk_hf* root CSV violation flag, each bit representing a clk_hf, say bit 0 for clk_hf0, bit 1 for clk_hf1, etc.<br>DATA0[24]: clk_ref CSV violation flag (reference clock for clk_hf CSVs)<br>DATA0[25]: clk_lf CSV violation flag<br>DATA0[26]: clk_hvilo CSV violation flag |
| | SRSS_SSV | | | 91 | SRSS Clock SuperVisor (CSV) violation detected. Multiple CSV can detect a violation at the same time.<br>DATA0[0]: BOD on VDDA<br>DATA[1]: OVD on VDDA<br>DATA[16]: LVD/HVD #1<br>DATA0[17]: LVD/HVD #2 |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| | SRSS_MCWDT0 | | | 92 | SRSS Multi-Counter Watch Dog Timer (MCWDT) #0 violation detected. Multiple counters can detect a violation at the same time.<br>DATA0[0]: MCWDT subcounter 0 LOWER_LIMIT<br>DATA0[1]: MCWDT subcounter 0 UPPER_LIMIT<br>DATA0[2]: MCWDT subcounter 1 LOWER_LIMIT<br>DATA0[3]: MCWDT subcounter 1 UPPER_LIMIT |
| | SRSS_MCWDT1 | | | 93 | SRSS Multi-Counter Watch Dog Timer (MCWDT) #1 violation detected. See SRSS_MCWDT0 description. |
| | SRSS_MCWDT2 | | | 94 | SRSS Multi-Counter Watch Dog Timer (MCWDT) #2 violation detected. See SRSS_MCWDT0 description. |
| | SRSS_MCWDT3 | | | 95 | SRSS Multi-Counter Watch Dog Timer (MCWDT) #3 violation detected. See SRSS_MCWDT0 description. |
| 31 | VALID | RW | RW1S | 0 | Valid indication:<br>'0': Invalid.<br>'1': Valid. STATUS.IDX, DATA0, ..., DATA3 specify the fault.<br><br>Note: Typically, HW sets this field to '1' (on an activated HW fault source that is 'enabled' by the MASK registers) and SW clears this field to '0' (typically by boot code SW (after a warm system reset, when the fault is handled). In this typical use case scenario, the HW source fault data is simultaneously captured into DATA0, ..., DATA3 when the VALID field is set to '1'.<br><br>An exceptional SW use case scenario is identified as well. In this scenario, SW sets this field to '1' with a fault source index different to one of the defined HW fault sources. SW update is not restricted by the MASK registers). In both use case scenarios, the following holds:<br>- STATUS.IDX, DATA0, ..., DATA3 can only be written when STATUS.VALID is '0'; the fault structure is not in use yet. Writing STATUS.VALID to '1' effectively locks the fault structure (until SW clears STATUS.VALID to '0'). This restriction requires a SW update to sequentially update the DATA registers followed by an update of the STATUS register.<br><br>Note: For the exceptional SW use case, sequential updates to the DATA and STATUS registers may be 'interrupted' by a HW fault capture. In this case, the SW DATA register updates are overwritten by the HW update (and the STATUS.IDX field will reflect the HW capture) |

### 13.5.1.3 FAULT_STRUCT_DATA

**Description:** Fault data
**Address:** 0x40210010
**Offset:** 0x10
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** The DATA registers capture fault information.

These register use cold reset (and are NOT affected by Active or DeepSleep reset). This allows for failure analysis after a warm reset (DeepSleep reset).
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | DATA | RW | W | Undefined | Captured fault source data.<br><br>Note: the DATA registers can only be written when STATUS.VALID is '0'.<br><br>Note: the fault source index STATUS.IDX specifies the format of the DATA registers. |

### 13.5.1.4 FAULT_STRUCT_PENDING0

**Description:** Fault pending 0
**Address:** 0x40210040
**Offset:** 0x40
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** The PENDING0, PENDING1, PENDING2 registers specify pending (not captured) fault sources. The fault source for which data is captured in DATA0 through DATA3 and which is validated by STATUS.VALID and identified by STATUS.IDX is NOT included in this list of pending fault sources. When a fault source is captured, its corresponding bit field in PENDING0/1/2 is set to '0'.

Note that the pending fault sources are the same for ALL fault structures; i.e. these registers are NOT qualified by the fault structure specific MASK0, MASK1 and MASK2 registers.
**Default:** Undefined as one or more bit fields have a default value that is undefined

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | SOURCE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | SOURCE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | SOURCE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | SOURCE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | SOURCE | R | W | Undefined | This field specifies the following sources:<br>Bit 0: CM0 MPU.<br>Bit 1: CRYPTO MPU.<br>Bit 2: DW 0 MPU.<br>Bit 3: DW 1 MPU.<br>Bit 4: DMA controller MPU.<br>...<br>Bit 15: DAP MPU.<br>Bit 16: CM4 system bus MPU.<br>Bit 17: CM4 code bus MPU (for non FLASH controller accesses).<br>Bit 18: CM4 code bus MPU (for FLASH controller accesses). |

### 13.5.1.5 FAULT_STRUCT_PENDING1

**Description:** Fault pending 1
**Address:** 0x40210044
**Offset:** 0x44
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** Undefined as one or more bit fields have a default value that is undefined

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | SOURCE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | SOURCE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | SOURCE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | SOURCE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | SOURCE | R | W | Undefined | This field specifies the following sources:<br>Bit 0: Peripheral group 0 PPU.<br>Bit 1: Peripheral group 1 PPU.<br>Bit 2: Peripheral group 2 PPU.<br>Bit 3: Peripheral group 3 PPU.<br>Bit 4: Peripheral group 4 PPU.<br>Bit 5: Peripheral group 5 PPU.<br>Bit 6: Peripheral group 6 PPU.<br>Bit 7: Peripheral group 7 PPU.<br>...<br>Bit 15: Peripheral group 15 PPU.<br><br>Bit 16 - 31: See STATUS register. |

### 13.5.1.6 FAULT_STRUCT_PENDING2

**Description:** Fault pending 2
**Address:** 0x40210048
**Offset:** 0x48
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** Undefined as one or more bit fields have a default value that is undefined

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | SOURCE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | SOURCE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | SOURCE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | SOURCE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | SOURCE | R | W | Undefined | This field specifies the following sources:<br>Bit 0 - 31: See STATUS register. |

### 13.5.1.7 FAULT_STRUCT_MASK0

**Description:** Fault mask 0
**Address:** 0x40210050
**Offset:** 0x50
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** The MASK0, MASK1, MASK2 registers specify 'enables' for fault sources. Only 'enabled' fault sources will be captured by this fault structure (and result in STATUS.VALID and INTR.FAULT being set to '1'). When a fault source is captured, its corresponding bit field in PENDING0/1/2 is set to '0'.

When multiple fault structures are present and the mask fields of the fault structures overlap (the same source is 'enabled' for multiple fault structures), an overlapping enabled pending fault source is captured by a single fault structure that has not captured a fault (the fault structure with the lowest index has precedence).
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | SOURCE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | SOURCE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | SOURCE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | SOURCE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | SOURCE | RW | R | 0 | Fault source enables:<br>Bits 31-0: Fault sources 31 to 0. |

### 13.5.1.8 FAULT_STRUCT_MASK1

**Description:** Fault mask 1
**Address:** 0x40210054
**Offset:** 0x54
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | SOURCE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | SOURCE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | SOURCE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | SOURCE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | SOURCE | RW | R | 0 | Fault source enables:<br>Bits 31-0: Fault sources 63 to 32. |

### 13.5.1.9 FAULT_STRUCT_MASK2

**Description:** Fault mask 2
**Address:** 0x40210058
**Offset:** 0x58
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | SOURCE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | SOURCE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | SOURCE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | SOURCE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | SOURCE | RW | R | 0 | Fault source enables:<br>Bits 31-0: Fault sources 95 to 64. |

### 13.5.1.10 FAULT_STRUCT_INTR

**Description:** Interrupt
**Address:** 0x402100C0
**Offset:** 0xC0
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:1] | | | | | | | FAULT [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | FAULT | RW1C | RW1S | 0 | This interrupt cause field is activated (HW sets the field to '1') when an enabled (MASK0/MASK1/MASK2) pending fault source is captured:<br>- STATUS.VALID is set to '1'.<br>- STATUS.IDX specifies the fault source index.<br>- DATA0 through DATA3 captures the fault source data.<br><br>SW writes a '1' to this field to clear the interrupt cause to '0'. SW clear STATUS.VALID to '0' to enable capture of the next fault. Note that when there is an enabled pending fault source, the pending fault source is captured immediately and INTR.FAULT is immediately activated (set to '1'). |

### 13.5.1.11 FAULT_STRUCT_INTR_SET

**Description:** Interrupt set
**Address:** 0x402100C4
**Offset:** 0xC4
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** When read, this register reflects the INTR register. For debug purposes, SW can write a '1' to activate a specific interrupt cause (this allows for debug of the SW ISR, without relying on HW to activate the interrupt cause).
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:1] | | | | | | | FAULT [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | FAULT | RW1S | A | 0 | SW writes a '1' to this field to set the corresponding field in the INTR register. |

### 13.5.1.12 FAULT_STRUCT_INTR_MASK

**Description:** Interrupt mask
**Address:** 0x402100C8
**Offset:** 0xC8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:1] | | | | | | | FAULT [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | FAULT | RW | R | 0 | Mask bit for corresponding field in the INTR register. |

### 13.5.1.13 FAULT_STRUCT_INTR_MASKED

**Description:** Interrupt masked
**Address:** 0x402100CC
**Offset:** 0xCC
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** When read, this register reflects 'a bitwise AND' between the INTR and INTR_MASK registers.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:1] | | | | | | | FAULT [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | FAULT | R | W | 0 | Logical and of corresponding INTR and INTR_MASK fields. |

# 14 FLASHC

**Description** Flash controller
**Base Address** 0x40240000
**Size** 0x10000
**Slave Num** MMIO2 - 4

| Register Name | Address | Permission | Description |
|---|---|---|---|
| FLASHC_FLASH_CTL | 0x40240000 | FULL | Control |
| FLASHC_FLASH_PWR_CTL | 0x40240004 | FULL | Flash power control |
| FLASHC_FLASH_CMD | 0x40240008 | FULL | Command |
| FLASHC_ECC_CTL | 0x402402A0 | READ | ECC control |
| FLASHC_FM_SRAM_ECC_CTL0 | 0x402402B0 | READ | eCT Flash SRAM ECC control 0 |
| FLASHC_FM_SRAM_ECC_CTL1 | 0x402402B4 | READ | eCT Flash SRAM ECC control 1 |
| FLASHC_FM_SRAM_ECC_CTL2 | 0x402402B8 | READ | eCT Flash SRAM ECC control 2 |
| FLASHC_FM_SRAM_ECC_CTL3 | 0x402402BC | READ | eCT Flash SRAM ECC control 3 |
| FLASHC_CM0_CA_CTL0 | 0x40240400 | FULL | CM0+ cache control |
| FLASHC_CM0_CA_CTL1 | 0x40240404 | FULL | CM0+ cache control |
| FLASHC_CM0_CA_CTL2 | 0x40240408 | FULL | CM0+ cache control |
| FLASHC_CM0_CA_STATUS0 | 0x40240440 | FULL | CM0+ cache status 0 |
| FLASHC_CM0_CA_STATUS1 | 0x40240444 | FULL | CM0+ cache status 1 |
| FLASHC_CM0_CA_STATUS2 | 0x40240448 | FULL | CM0+ cache status 2 |
| FLASHC_CM0_STATUS | 0x40240460 | FULL | CM0+ interface status |
| FLASHC_CM7_0_STATUS | 0x402404E0 | FULL | CM7 #0 interface status |
| FLASHC_CM7_1_STATUS | 0x40240560 | FULL | CM7 #1 interface status |
| FLASHC_CRYPTO_BUFF_CTL | 0x40240580 | FULL | Cryptography buffer control |
| FLASHC_DW0_BUFF_CTL | 0x40240600 | FULL | Datawire 0 buffer control |
| FLASHC_DW1_BUFF_CTL | 0x40240680 | FULL | Datawire 1 buffer control |
| FLASHC_DMAC_BUFF_CTL | 0x40240700 | FULL | DMA controller buffer control |
| FLASHC_SLOW0_MS_BUFF_CTL | 0x40240780 | FULL | Slow external master 0 buffer control |

## 14.1 FM_CTL_ECT

| Register Name | Address | Permission | Description |
|---|---|---|---|
| FLASHC_FM_CTL | 0x4024F000 | NO-ACCESS | Flash Macro Control |
| FLASHC_FM_CODE_MARGIN | 0x4024F004 | NO-ACCESS | Flash Macro Margin Mode on Code Flash |
| FLASHC_FM_ADDR | 0x4024F008 | NO-ACCESS | Flash Macro Address |
| FLASHC_INTR | 0x4024F020 | NO-ACCESS | Interrupt |
| FLASHC_INTR_SET | 0x4024F024 | NO-ACCESS | Interrupt Set |
| FLASHC_INTR_MASK | 0x4024F028 | NO-ACCESS | Interrupt Mask |
| FLASHC_INTR_MASKED | 0x4024F02C | NO-ACCESS | Interrupt Masked |
| FLASHC_ECC_OVERRIDE | 0x4024F030 | NO-ACCESS | ECC Data In override information and control bits |
| FLASHC_FM_DATA | 0x4024F040 | NO-ACCESS | Flash macro data_in[31 to 0] both Code and Work Flash |
| FLASHC_BOOKMARK | 0x4024F064 | NO-ACCESS | Bookmark register - keeps the current FW HV seq |
| FLASHC_MAIN_FLASH_SAFETY | 0x4024F400 | FULL | Main (Code) Flash Security enable |
| FLASHC_STATUS | 0x4024F404 | FULL | Status read from Flash Macro |
| FLASHC_WORK_FLASH_SAFETY | 0x4024F500 | FULL | Work Flash Security enable |

## 14.2 Register Details

### 14.2.1 FLASHC_FLASH_CTL

**Description:** Control
**Address:** 0x40240000
**Offset:** 0x0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x1000000

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:4] | | | | WS [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:14] | | WORK_BANK_MODE [13:13] | MAIN_BANK_MODE [12:12] | None [11:10] | | WORK_MAP [9:9] | MAIN_MAP [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:23] | WORK_ERR_SILENT [22:22] | WORK_ECC_INJ_EN [21:21] | WORK_ECC_EN [20:20] | None [19:19] | MAIN_ERR_SILENT [18:18] | MAIN_ECC_INJ_EN [17:17] | MAIN_ECC_EN [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:25] | | | | | | | WORK_SEQ_RD_EN [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | WS | RW | R | 0 | FLASH macro wait states (same for main and work interfaces):<br>'0': 0 wait states.<br>...<br>'15': 15 wait states |
| 8 | MAIN_MAP | RW | R | 0 | Specifies mapping of FLASH macro main array.<br>0: Mapping A.<br>1: Mapping B.<br><br>This field is only used when MAIN_BANK_MODE is '1' (dual bank mode). |
| 9 | WORK_MAP | RW | R | 0 | Specifies mapping of FLASH macro work array.<br>0: Mapping A.<br>1: Mapping B.<br><br>This field is only used when WORK_BANK_MODE is '1' (dual bank mode). |
| 12 | MAIN_BANK_MODE | RW | R | 0 | Specifies bank mode of FLASH macro main array.<br>0: Single bank mode.<br>1: Dual bank mode. |
| 13 | WORK_BANK_MODE | RW | R | 0 | Specifies bank mode of FLASH macro work array.<br>0: Single bank mode.<br>1: Dual bank mode. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 16 | MAIN_ECC_EN | RW | R | 0 | Enable ECC checking for FLASH main interface:<br>0: Disabled. ECC checking/reporting on FLASH main interface is disabled. No correctable or non-correctable faults are reported.<br>1: Enabled. |
| 17 | MAIN_ECC_INJ_EN | RW | R | 0 | Enable error injection for FLASH main interface. When'1', the parity (ECC_CTL.PARITY[7:0]) is used for a load from the ECC_CTL.WORD_ADDR[23:0] word address. |
| 18 | MAIN_ERR_SILENT | RW | R | 0 | Specifies bus transfer behavior for a non-recoverable error on the FLASH macro main interface (either a non-correctable ECC error or a FLASH macro main interface internal error):<br>0: Bus transfer has a bus error.<br>1: Bus transfer does NOT have a bus error; i.e. the error is 'silent'<br>In either case, the erroneous FLASH macro data is returned by the bus master interface. The erroneous data is NOT placed in a bus master interface's cache and/or buffer.<br><br>This field is ONLY used by CPU (or debug i.e. SYS_AP/CM0_AP/CM7_0/1_AP) bus transfers. Non-CPU bus transfers always have a bus transfer with a bus error, in case of a non-recoverable error.<br><br>Note: All CPU bus masters have dedicated status registers (CM0_STATUS, CM7_0_STATUS and CM7_1_STATUS) to register the occurrence of FLASH macro main interface internal errors (non-correctable ECC errors are NOT registered).<br><br>Note: fault reporting can be used to identify the error that occurred:<br>- FLASH macro main interface internal error.<br>- FLASH macro main interface non-recoverable ECC error.<br>- FLASH macro main interface recoverable ECC error. |
| 20 | WORK_ECC_EN | RW | R | 0 | N/A |
| 21 | WORK_ECC_INJ_EN | RW | R | 0 | N/A |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 22 | WORK_ERR_SILENT | RW | R | 0 | Specifies bus transfer behavior for a non-recoverable error on the FLASH macro work interface (either a non-correctable ECC error or a FLASH macro work interface internal error):<br>0: Bus transfer has a bus error.<br>1: Bus transfer does NOT have a bus error; i.e. the error is 'silent'<br>In either case, the erroneous FLASH macro data is returned by the bus master interface. The erroneous data is NOT placed in a bus master interface's cache and/or buffer.<br><br>This field is ONLY used by CPU (or debug i.e. SYS_AP/CM0_AP/CM7_0/1_AP) bus transfers. Non-CPU bus transfers always have a bus transfer with a bus error, in case of a non-recoverable error.<br><br>Note: All CPU bus masters have dedicated status registers (CM0_STATUS, CM7_0_STATUS and CM7_1_STATUS) to register the occurrence of FLASH macro work interface internal errors (non-correctable ECC errors are NOT registered).<br><br>Note: fault reporting can be used to identify the error that occurred:<br>- FLASH macro work interface internal error.<br>- FLASH macro work interface non-recoverable ECC error.<br>- FLASH macro work interface recoverable ECC error. |
| 24 | WORK_SEQ_RD_EN | RW | R | 1 | Enable sequential read mode for Work Flash for read accesses on the AXI port.<br>0: Sequential read mode for Work Flash is disabled.<br>1: Sequential read mode for Work Flash is enabled. This speeds up subsequent AXI read accesses to the same page (64 bytes) of the Work Flash.<br><br>Setting this field to '1' has a side effect on the round-robin arbitration of the Work Flash macro between the different ports. When this field is set to '1', then as soon as the arbitration of the Work Flash is given to the AXI port, it is not released before the current AXI read burst either has been completed or leaves the current Work Flash page (64 bytes). This means that AHB masters accessing the Work Flash that have the same priority as the AXI port will not get their fair share of the Work Flash bandwidth. While an AHB master can perform one Work Flash access per round-robin cycle (4 bytes), an AXI master can read a whole AXI burst, or up to the next Work Flash page boundary. So if this field is set to '1', and an AHB master requires a high Work Flash bandwidth, then it should have a higher priority than the AXI masters accessing the Work Flash. |

### 14.2.2 FLASHC_FLASH_PWR_CTL

**Description:** Flash power control
**Address:** 0x40240004
**Offset:** 0x4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register controls Flash memory power control input pins 'enable' and 'enable_hv'. Flash memory can turned OFF through SW in LPACTIVE power mode by making ENABLE=0 and ENABLE_HV=0. The wakeup time of the Flash memory is 10us (Twake1). So, SW has to wait for 10us to read from Flash after turning the Flash memory ON though this register.
**Default:** 0x3

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:2] | | | | | | ENABLE_HV [1:1] | ENABLE [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | ENABLE | RW | R | 1 | Controls 'enable' pin of the Flash memory. |
| 1 | ENABLE_HV | RW | R | 1 | Controls 'enable_hv' pin of the Flash memory. |

### 14.2.3 FLASHC_FLASH_CMD

**Description:** Command
**Address:** 0x40240008
**Offset:** 0x8
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:2] | | | | | | BUFF_INV [1:1] | INV [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | INV | RW1S | RW1C | 0 | Invalidation of ALL caches (for CM0+) and ALL buffers. SW writes a '1' to clear the caches. HW sets this field to '0' when the operation is completed. The operation takes a maximum of three clock cycles on the slowest of the clk_slow and clk_fast clocks. The caches LRU structures are also reset to their default state. |
| 1 | BUFF_INV | RW1S | RW1C | 0 | Invalidation of ALL buffers (does not invalidate the caches). SW writes a '1' to clear the buffers. HW sets this field to '0' when the operation is completed. The operation takes a maximum of three clock cycles on the slowest of the clk_slow and clk_fast clocks.<br><br>Note: the caches only capture FLASH macro main array data. Therefore, invalidating just the buffers (BUFF_INV) does not invalidate captures main array data in the caches. |

### 14.2.4 FLASHC_ECC_CTL

**Description:** ECC control
**Address:** 0x402402A0
**Offset:** 0x2A0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | WORD_ADDR [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | WORD_ADDR [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | WORD_ADDR [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | PARITY [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:23 | WORD_ADDR | RW | R | 0 | N/A |
| 24:31 | PARITY | RW | R | 0 | N/A |

### 14.2.5 FLASHC_FM_SRAM_ECC_CTL0

**Description:** eCT Flash SRAM ECC control 0
**Address:** 0x402402B0
**Offset:** 0x2B0
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | ECC_INJ_DATA [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | ECC_INJ_DATA [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | ECC_INJ_DATA [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | ECC_INJ_DATA [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | ECC_INJ_DATA | RW | R | 0 | 32-bit data for ECC error injection test of eCT Flash SRAM ECC logic. |

### 14.2.6 FLASHC_FM_SRAM_ECC_CTL1

**Description:** eCT Flash SRAM ECC control 1
**Address:** 0x402402B4
**Offset:** 0x2B4
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:7] | ECC_INJ_PARITY [6:0] | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:6 | ECC_INJ_PARITY | RW | R | 0 | 7-bit parity for ECC error injection test of eCT Flash SRAM ECC logic. |

### 14.2.7 FLASHC_FM_SRAM_ECC_CTL2

**Description:** eCT Flash SRAM ECC control 2
**Address:** 0x402402B8
**Offset:** 0x2B8
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | CORRECTED_DATA [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | CORRECTED_DATA [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | CORRECTED_DATA [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | CORRECTED_DATA [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | CORRECTED_DATA | R | W | 0 | 32-bit corrected data output of the ECC syndrome logic. |

### 14.2.8 FLASHC_FM_SRAM_ECC_CTL3

**Description:** eCT Flash SRAM ECC control 3
**Address:** 0x402402BC
**Offset:** 0x2BC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x1

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:5] | | | ECC_INJ_EN [4:4] | None [3:1] | | | ECC_ENABLE [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:9] | | | | | | | ECC_TEST_FAIL [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | ECC_ENABLE | RW | R | 1 | ECC generation/check enable for eCT Flash SRAM memory. |
| 4 | ECC_INJ_EN | RW | RW1C | 0 | eCT Flash SRAM ECC error injection test enable.<br>Follow the steps below for ECC logic test:<br>1. Write corrupted or uncorrupted 39-bit data to FM_SRAM_ECC_CTL0/1 registers.<br>2. Set the ECC_INJ_EN bit to '1'.<br>3. Confirm that the bit ECC_TEST_FAIL is '0'. If this is not the case, start over at item 1 because the eCT Flash was not idle.<br>4. Check the corrected data in FM_SRAM_ECC_CTL2.<br>5. Confirm that fault was reported to fault structure, and check syndrome (only applicable if corrupted data was written in step 1).<br>6. If not finished, start over at 1 with different data. |
| 8 | ECC_TEST_FAIL | R | W | 0 | Status of ECC test.<br>1: ECC test failed because eCT Flash macro is busy and using the SRAM.<br>0: ECC was performed. |

### 14.2.9 FLASHC_CM0_CA_CTL0

**Description:** CM0+ cache control
**Address:** 0x40240400
**Offset:** 0x400
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xC0000001

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:2] | | | | | | RAM_ECC_INJ_EN [1:1] | RAM_ECC_EN [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:18] | | | | | | WAY [17:16] | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | CA_EN [31:31] | PREF_EN [30:30] | None [29:27] | | | SET_ADDR [26:24] | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | RAM_ECC_EN | RW | R | 1 | Enable ECC checking for cache accesses:<br>0: Disabled.<br>1: Enabled. |
| 1 | RAM_ECC_INJ_EN | RW | R | 0 | Enable error injection for cache.<br>When '1', the parity (ECC_CTL.PARITY[6:0]) is used when a refill is done from the FLASH macro to the ECC_CTL.WORD_ADDR[24:0] word address. |
| 16:17 | WAY | RW | R | 0 | Specifies the cache way for which cache information is provided in CM0_CA_STATUS0/1/2. |
| 24:26 | SET_ADDR | RW | R | 0 | Specifies the cache set for which cache information is provided in CM0_CA_STATUS0/1/2. |
| 30 | PREF_EN | RW | R | 1 | Prefetch enable:<br>0: Disabled.<br>1: Enabled.<br><br>Prefetching requires the cache to be enabled; i.e. ENABLED is '1'. |
| 31 | CA_EN | RW | R | 1 | Cache enable:<br>0: Disabled. The cache tag valid bits are reset to '0's and the cache LRU information is set to '1's (making way 0 the LRU way and way 3 the MRU way).<br>1: Enabled.G269 |

### 14.2.10 FLASHC_CM0_CA_CTL1

**Description:** CM0+ cache control
**Address:** 0x40240404
**Offset:** 0x404
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register controls the CM0 Cache SRAM power states. CM0 Cache SRAM consists of a single power partition.
**Default:** 0xFA050003

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:2] | | | | | | PWR_MODE [1:0] | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VECTKEYSTAT [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VECTKEYSTAT [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:1 | PWR_MODE | RW | R | 3 | Specifies power mode for CM0 cache.<br>The following sequnece should be followed for truning OFF/ON the cache SRAM.<br>Turn OFF sequence:<br>a) Write CM0_CA_CTL0 to disable cache.<br>b) Write CM0_CA_CTL1 to turn OFF cache SRAM.<br>Turn ON sequence:<br>a) Write CM0_CA_CTL1 to turn ON cache SRAM.<br>b) Delay to allow power up of cache SRAM. Delay should be at a minimum of CM0_CA_CTL2.PWRUP_DELAY CLK_SLOW clock cycles.<br>c) Write CM0_CA_CTL0 to enable cache. |
| | OFF | | | 0 | Power OFF the CM0 cache SRAM. |
| | RESERVED | | | 1 | Undefined |
| | RETAINED | | | 2 | Put CM0 cache SRAM in retained mode. |
| | ENABLED | | | 3 | Enable/Turn ON the CM0 cache SRAM. |
| 16:31 | VECTKEYSTAT | R | | 64005 | Register key (to prevent accidental writes).<br>- Should be written with a 0x05fa key value for the write to take effect.<br>- Always reads as 0xfa05.<br>Note: Although the SW attribute for this field says "R', SW need to write the key 0x05fa in this field for this register write to happen. This is a built in protection provided to prevent accidental writes from SW. |

### 14.2.11 FLASHC_CM0_CA_CTL2

**Description:** CM0+ cache control
**Address:** 0x40240408
**Offset:** 0x408
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x12C

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | PWRUP_DELAY [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:10] | | | | | | PWRUP_DELAY [9:8] | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:9 | PWRUP_DELAY | RW | R | 300 | Number clock cycles delay needed after power domain power up |

### 14.2.12 FLASHC_CM0_CA_STATUS0

**Description:** CM0+ cache status 0
**Address:** 0x40240440
**Offset:** 0x440
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALID32 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALID32 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALID32 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALID32 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALID32 | R | W | 0 | Sixteen valid bits of the cache line specified by CM0_CA_CTL.WAY and CM0_CA_CTL.SET_ADDR. |

### 14.2.13 FLASHC_CM0_CA_STATUS1

**Description:** CM0+ cache status 1
**Address:** 0x40240444
**Offset:** 0x444
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** Undefined as one or more bit fields have a default value that is undefined

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | TAG [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | TAG [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | TAG [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | TAG [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | TAG | R | W | Undefined | Cache line address of the cache line specified by CM0_CA_CTL.WAY and CM0_CA_CTL.SET_ADDR. |

### 14.2.14 FLASHC_CM0_CA_STATUS2

**Description:** CM0+ cache status 2
**Address:** 0x40240448
**Offset:** 0x448
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** Undefined as one or more bit fields have a default value that is undefined

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:6] | | LRU [5:0] | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:5 | LRU | R | W | Undefined | Six bit LRU representation of the cache set specified by CM0_CA_CTL.SET_ADDR. The encoding of the field is as follows ('X_LRU_Y' indicates that way X is Less Recently Used than way Y):<br>Bit 5: 0_LRU_1: way 0 less recently used than way 1.<br>Bit 4: 0_LRU_2.<br>Bit 3: 0_LRU_3.<br>Bit 2: 1_LRU_2.<br>Bit 1: 1_LRU_3.<br>Bit 0: 2_LRU_3. |

### 14.2.15 FLASHC_CM0_STATUS

**Description:** CM0+ interface status
**Address:** 0x40240460
**Offset:** 0x460
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:2] | | | | | | WORK_INTERNAL_ERR [1:1] | MAIN_INTERNAL_ERR [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | MAIN_INTERNAL_ERR | RW1C | W1S | 0 | Specifies/registers the occurrence of a FLASH macro main interface internal error (typically the result of a read access while a program erase operation is ongoing) as a result of a CM0+ (or debug access via SYS_AP/CM0_AP) access.<br><br>SW clears this field to '0'. HW sets this field to '1' on a FLASH macro main interface internal error. Typically, SW reads this field after a code section to detect the occurrence of an error.<br><br>Note: this field is independent of FLASH_CTL.MAIN_ERR_SILENT. |
| 1 | WORK_INTERNAL_ERR | RW1C | W1S | 0 | See CM0_STATUS.MAIN_INTERNAL_ERROR. |

### 14.2.16 FLASHC_CM7_0_STATUS

**Description:** CM7 #0 interface status
**Address:** 0x402404E0
**Offset:** 0x4E0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:2] | | | | | | WORK_INTERNAL_ERR [1:1] | MAIN_INTERNAL_ERR [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | MAIN_INTERNAL_ERR | RW1C | W1S | 0 | Specifies/registers the occurrence of a FLASH macro main interface internal error (typically the result of a read access while a program erase operation is ongoing) as a result of a CM7_0 (or debug access via SYS_AP/CM7_0_AP) access.<br><br>SW clears this field to '0'. HW sets this field to '1' on a FLASH macro main interface internal error. Typically, SW reads this field after a code section to detect the occurrence of an error.<br><br>Note: this field is independent of FLASH_CTL.MAIN_ERR_SILENT. |
| 1 | WORK_INTERNAL_ERR | RW1C | W1S | 0 | See CM7_0_STATUS.MAIN_INTERNAL_ERROR. |

### 14.2.17 FLASHC_CM7_1_STATUS

**Description:** CM7 #1 interface status
**Address:** 0x40240560
**Offset:** 0x560
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:2] | | | | | | WORK_INTERNAL_ERR [1:1] | MAIN_INTERNAL_ERR [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | MAIN_INTERNAL_ERR | RW1C | W1S | 0 | Specifies/registers the occurrence of a FLASH macro main interface internal error (typically the result of a read access while a program erase operation is ongoing) as a result of a CM7_1 (or debug access via SYS_AP/CM7_1_AP) access.<br><br>SW clears this field to '0'. HW sets this field to '1' on a FLASH macro main interface internal error. Typically, SW reads this field after a code section to detect the occurrence of an error.<br><br>Note: this field is independent of FLASH_CTL.MAIN_ERR_SILENT. |
| 1 | WORK_INTERNAL_ERR | RW1C | W1S | 0 | See CM7_1_STATUS.MAIN_INTERNAL_ERROR. |

### 14.2.18 FLASHC_CRYPTO_BUFF_CTL

**Description:** Cryptography buffer control
**Address:** 0x40240580
**Offset:** 0x580
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x40000000

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:31] | PREF_EN [30:30] | None [29:24] | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 30 | PREF_EN | RW | R | 1 | Prefetch enable:<br>0: Disabled.<br>1: Enabled. |

### 14.2.19 FLASHC_DW0_BUFF_CTL

**Description:** Datawire 0 buffer control
**Address:** 0x40240600
**Offset:** 0x600
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x40000000

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:31] | PREF_EN [30:30] | None [29:24] | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 30 | PREF_EN | RW | R | 1 | See CRYPTO_BUFF_CTL. |

### 14.2.20 FLASHC_DW1_BUFF_CTL

**Description:** Datawire 1 buffer control
**Address:** 0x40240680
**Offset:** 0x680
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x40000000

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:31] | PREF_EN [30:30] | None [29:24] | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 30 | PREF_EN | RW | R | 1 | See CRYPTO_BUFF_CTL. |

### 14.2.21 FLASHC_DMAC_BUFF_CTL

**Description:** DMA controller buffer control
**Address:** 0x40240700
**Offset:** 0x700
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x40000000

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:31] | PREF_EN [30:30] | None [29:24] | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 30 | PREF_EN | RW | R | 1 | See CRYPTO_BUFF_CTL. |

### 14.2.22 FLASHC_SLOW0_MS_BUFF_CTL

**Description:** Slow external master 0 buffer control
**Address:** 0x40240780
**Offset:** 0x780
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x40000000

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:31] | PREF_EN [30:30] | None [29:24] | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 30 | PREF_EN | RW | R | 1 | See CRYPTO_BUFF_CTL. |

### 14.2.23 FM_CTL_ECT

#### 14.2.23.1 FLASHC_FM_CTL

**Description:** Flash Macro Control
**Address:** 0x4024F000
**Offset:** 0x0
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** The register fields are related to C interface functionality
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:5] | | | FM_MODE [4:0] | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | EMB_START [31:31] | None [30:24] | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:4 | FM_MODE | RW | R | 0 | Flash macro mode selection:<br>d0: Read/Idle - Normal mode, read array enabled<br>d1: Not Used - the 1st analog POR is done by enable/enable_hv<br>d2 - POR FUR Download - Downloads critical Flash initialization data from OTP (BG, rd, redu, etc....)<br>d3 - POR IRAM MMR Download - Downloads from OTP region the MMR / IRAM into to the 8051 RDL shadows<br>d4 - POR SW Download - Downloads from OTP region the SW code into to the 8051 MCU SRAM<br>d5 - POR Code_Work Prepare - Loads the Code and Work Flash MG's to be ready for user mode operation<br>d6 - Not Used<br>d7 - Program 32b (WORK) - Used as program confirm command for 32 (Work) bits program<br>d8 - Program 64b (CODE) - Used as program confirm command for 64 (Code) bits program<br>d9 - Program 256b (CODE) - Used as program confirm command for 256 (Code) bits program<br>d10: Program Page (CODE) - Used as program confirm command for page program for Code flash<br>d11: Not Used<br>d12 - Sector Erase - Erase for all kinds of sectors (Code/Work/SMS)<br>d13 - Blank check Entry (UBC)<br>d14 - Blank Check Read 32bit (WORK) - Blank check mode<br>d15 - Blank check Exit<br>d16 - Not Used<br>d17 - Erase Suspend - Suspend command to the Erase operation<br>d18 - Erase Resume - Resume command to Erase suspended operation<br>d19 - Not Used<br>d20- Not Used<br>d21- Not Used<br>d22- Not Used<br>d23- Not Used<br>d24- Not Used<br>d25- Not Used<br>d26- Not Used<br>d27- Not Used<br>d28- Not Used<br>d29- Not Used<br>d30: Not Used<br>d31: Not Used |
| 31 | EMB_START | RW | R | 0 | '0': not active<br>'1': starts the actual embedded operation |

### 14.2.23.2 FLASHC_FM_CODE_MARGIN

**Description:** Flash Macro Margin Mode on Code Flash
**Address:** 0x4024F004
**Offset:** 0x4
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** This register shell be used when Margin read is applied to the s40ect Flash IP. One should set the DCS trim that serves as the reference current to the area between 4-8uA (around the 6uA normal static ref current) and set the enable. After that one should wait ~10uSec before starting to read any data in the Code Flash. Once Finished the MARGIN_MODE_EN should be reset. Again, user should wait ~10uSec before continue to work with the Flash normally.
**Default:** 0x3943

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | MARGIN_DCS_TRIM [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | MARGIN_RDREG_TRIM [15:10] | | | | | | MARGIN_DCS_TRIM_EN [9:9] | MARGIN_DCS_TRIM [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | MARGIN_MODE_EN [31:31] | MARGIN_MODE_RDREG_CHNG_EN [30:30] | MARGIN_PGM_ERS_B [29:29] | None [28:24] | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:8 | MARGIN_DCS_TRIM | RW | R | 323 | see above table to set the DCS reference current value to be used during Margin mode. (default set to 5uS = 0x143) which gives a Margin to the Erase side. 7uA would probably be used for Margin to the PGM side |
| 9 | MARGIN_DCS_TRIM_EN | RW | R | 0 | 0: internal device defaults used from Margin reads reference current<br>1: MARGIN_DCS_TRIM configuration is used during Margin read |
| 10:15 | MARGIN_RDREG_TRIM | RW | R | 14 | rdreg_c trim to be used in Margin mode if enabled by MARGIN_MODE_RDREG_CHNG_EN |
| 29 | MARGIN_PGM_ERS_B | RW | R | 0 | 0: ERS Margin is checked<br>1: PGM Margin is checked |
| 30 | MARGIN_MODE_RDREG_CHNG_EN | RW | R | 0 | when set will also use the MARGIN_RDREG_TRIM from above. Default is not to use |
| 31 | MARGIN_MODE_EN | RW | R | 0 | when set puts the s40ect Flash IP In Margin mode |

### 14.2.23.3 FLASHC_FM_ADDR

**Description:** Flash Macro Address
**Address:** 0x4024F008
**Offset:** 0x8
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** This register specifies the flash memory address till the byte resolution. This register defines the address space for both Code and Work Flash and it works according to the address scheme tables defined below (also used as the address definition for R-bus ( code_r_addr and work_r_addr)
This FM_ADDR should be used whenever a user mode embedded operation is done on the Flash i.e. PGM/ERS
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | FM_ADDR [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | FM_ADDR [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | FM_ADDR [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | FM_ADDR [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | FM_ADDR | W | R | 0 | Code or Work Flash Address to be used during write operations (PGM/ERS) |

### 14.2.23.4 FLASHC_INTR

**Description:** Interrupt
**Address:** 0x4024F020
**Offset:** 0x20
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:1] | | | | | | | INTR [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | INTR | RW1C | RW1S | 0 | Set to '1', when event is detected. Write INTR field with '1', to clear bit. Write INTR_SET field with '1', to set bit. |

### 14.2.23.5 FLASHC_INTR_SET

**Description:** Interrupt Set
**Address:** 0x4024F024
**Offset:** 0x24
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:1] | | | | | | | INTR_SET [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | INTR_SET | RW1S | A | 0 | Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect). |

### 14.2.23.6 FLASHC_INTR_MASK

**Description:** Interrupt Mask
**Address:** 0x4024F028
**Offset:** 0x28
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:1] | | | | | | | INTR_MASK [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | INTR_MASK | RW | R | 0 | Mask for corresponding field in the INTR register |

### 14.2.23.7 FLASHC_INTR_MASKED

**Description:** Interrupt Masked
**Address:** 0x4024F02C
**Offset:** 0x2C
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:1] | | | | | | | INTR_MASKED [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | INTR_MASKED | R | W | 0 | Logical and of corresponding request and mask fields. |

### 14.2.23.8 FLASHC_ECC_OVERRIDE

**Description:** ECC Data In override information and control bits
**Address:** 0x4024F030
**Offset:** 0x30
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** The replacement can be either to the Code syndrome or the work flash syndrome. It knows to replace only 8 bits (per 64) in code flash OR 7 bits (per 32) in work flash, therefore this option is valid only for pgm64 command (Code) or pgm32 command (Work)
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | ECC_OVERRIDE_SYNDROME [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | ECC_OVERRIDE_CODE [31:31] | ECC_OVERRIDE_WORK [30:30] | None [29:24] | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | ECC_OVERRIDE_SYNDROME | W | R | 0 | The override syndrome itself to be used in case one of the enables are set. It will take [7:0] in the case of Code flash and [6:0] in the case of work flash, to bypass the internal generated syndrome |
| 30 | ECC_OVERRIDE_WORK | W | R | 0 | 0: no override. Using internal ECC engine to calculate the ECC of the Work Flash |
| 31 | ECC_OVERRIDE_CODE | W | R | 0 | 0: no override. Using internal ECC engine to calculate the ECC of the Code Flash |

### 14.2.23.9 FLASHC_FM_DATA

**Description:** Flash macro data_in[31 to 0] both Code and Work Flash
**Address:** 0x4024F040
**Offset:** 0x40
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** These registers support aligned 32-bit accesses. The usage of this register should follow the PGM sequence defined (and implemented by API). It has restrictions on the FM_ADDR and # of writes that can be done per pgm command (64,256,page for Code or 32 to work flash) and therefore the sequence must be correct. These register are related to C interface functionality.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | FM_DATA [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | FM_DATA [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | FM_DATA [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | FM_DATA [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | FM_DATA | W | RW | 0 | Pgm command data in going to the internal write buffer (WBUF). |

### 14.2.23.10 FLASHC_BOOKMARK

**Description:** Bookmark register - keeps the current FW HV seq
**Address:** 0x4024F064
**Offset:** 0x64
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | BOOKMARK [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | BOOKMARK [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | BOOKMARK [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | BOOKMARK [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | BOOKMARK | RW | R | 0 | Used by FW. Keeps the Current HV cycle sequence |

### 14.2.23.11 FLASHC_MAIN_FLASH_SAFETY

**Description:** Main (Code) Flash Security enable
**Address:** 0x4024F400
**Offset:** 0x400
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:1] | | | | | | | MAINFLASH WRITEENABLE [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | MAINFLASH WRITEENABLE | RW | R | 0 | '0': Main Flash embedded operations are blocked<br>'1': Main Flash embedded operations are enabled |

### 14.2.23.12 FLASHC_STATUS

**Description:** Status read from Flash Macro
**Address:** 0x4024F404
**Offset:** 0x404
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** Read out by the CPUSS to understand the Flash Macro status
**Default:** 0x80000000

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:7] | BLANK _CHCEK _PASS [6:6] | BLANK _CHECK _WORK [5:5] | ERS _SUSPEND [4:4] | ERASE _WORK [3:3] | ERASE _CODE [2:2] | PGM _WORK [1:1] | PGM _CODE [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | BUSY [31:31] | HANG [30:30] | NATIVE _POR [29:29] | POR_2B _ECC _ERROR [28:28] | POR_1B _ECC _CORRECTE D [27:27] | None [26:24] | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | PGM_CODE | R | W | 0 | Indicates if active PGM operation to the Code flash is taking place<br>0: not running<br>1: running |
| 1 | PGM_WORK | R | W | 0 | Indicates if active PGM operation to the Work flash is taking place<br>0: not running<br>1: running |
| 2 | ERASE_CODE | R | W | 0 | Indicates if active Erase operation to the Code flash is taking place<br>0: not running<br>1: running |
| 3 | ERASE_WORK | R | W | 0 | Indicates if active Erase operation to the Work flash is taking place<br>0: not running<br>1: running |
| 4 | ERS_SUSPEND | R | W | 0 | Indicates if Erase operation (Code/Work) is currently being suspended<br>0: not suspended<br>1: suspended |
| 5 | BLANK_CHECK_WORK | R | W | 0 | Indicates if Blank Check mode is currently running on the work flash<br>0: not running<br>1: running |
| 6 | BLANK_CHCEK_PASS | R | W | 0 | Indicates the Blank check command result is PASS (Blank)<br>0: Not Blank<br>1: Blank (PASS) |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 27 | POR_1B_ECC _CORRECTED | R | W | 0 | Indicates internal ECC found 1b error while downloading info in POR from NVM to VM and fixed it. Valid after 2nd, 3rd and 4th POR phases (FUR, IREM & MMR, SW DOWNLOAD). If Set it is not cleaned till additional POR (rst_hf_ac_t)<br>0: No error<br>1: 1b ECC Error corrected in POR |
| 28 | POR_2B_ECC_ERROR | R | W | 0 | Indicates an internal ECC error of 2b while downloading info in POR from NVM to VM.<br>Valid after 2nd, 3rd and 4th POR phases (FUR, IREM & MMR, SW DOWNLOAD). If Set it is not cleaned till additional POR (rst_hf_ac_t)<br>0: No error<br>1: ECC 2b Error in POR |
| 29 | NATIVE_POR | R | W | 0 | Indicates a Native Flash state (UV) or sorted one. Valid only after 2nd phase of POR (FUR DOWNLOAD).<br>Comment: not a retained flop, therefore reset (rst_hf_act_n) puts it back to 0. If Set it is not cleaned till additional POR (rst_hf_ac_t)<br>0: SORTED DEVICE (Non - Native)<br>1: NATIVE |
| 30 | HANG | R | W | 0 | After embedded operation (pgm/erase) this flag will tell if it was successful or failed<br>0: PASS<br>1: FAIL |
| 31 | BUSY | R | W | 1 | Whenever the device is in embedded mode the RDY goes low. Should be the same as c_interrupt pin of the IP (but inverted)<br>1: busy in embedded<br>0: rdy (high also in erase suspend) |

### 14.2.23.13 FLASHC_WORK_FLASH_SAFETY

**Description:** Work Flash Security enable
**Address:** 0x4024F500
**Offset:** 0x500
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:1] | | | | | | | WORKFLASH WRITEENABLE [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | WORKFLASH WRITEENABLE | RW | R | 0 | 0: Work Flash embedded operations are blocked<br>1: Work Flash embedded operations are enabled |

# 15 FLEXRAY

**Description** FlexRay Bus Interface
**Base Address** 0x40560000
**Size** 0x1000
**Slave Num** MMIO5 - 3

This instance is not available in the following part numbers:
CYT4BF8CES, CYT4BF8CEE, CYT4A0M1BE, CYT4BF8DES, CYT4BF8DEE, CYT4BFBCJS, CYT4BFBCJE, CYT4A0M1AE, CYT4BFBDJS, CYT4BFBDJE, CYT4BFCCJS, CYT4BFCCJE, CYT4BFCDJS, CYT4BFCDJE, CYT4A0100S.

| Register Name | Address | Permission | Description |
|---|---|---|---|
| FLEXRAY0_CTL | 0x40560000 | FULL | Control Register |
| FLEXRAY0_DMA_CTL | 0x40560004 | FULL | DMA Control Register |
| FLEXRAY0_TEST1 | 0x40560010 | FULL | Test Register 1 |
| FLEXRAY0_TEST2 | 0x40560014 | FULL | Test Register 2 |
| FLEXRAY0_LCK | 0x4056001C | FULL | Lock Register |
| FLEXRAY0_EIR | 0x40560020 | FULL | Error Interrupt Register |
| FLEXRAY0_SIR | 0x40560024 | FULL | Status Interrupt Register |
| FLEXRAY0_EILS | 0x40560028 | FULL | Error Interrupt Line Select |
| FLEXRAY0_SILS | 0x4056002C | FULL | Status Interrupt Line Select |
| FLEXRAY0_EIES | 0x40560030 | FULL | Error Interrupt Enable Set |
| FLEXRAY0_EIER | 0x40560034 | FULL | Error Interrupt Enable Reset |
| FLEXRAY0_SIES | 0x40560038 | FULL | Status Interrupt Enable Set |
| FLEXRAY0_SIER | 0x4056003C | FULL | Status Interrupt Enable Reset |
| FLEXRAY0_ILE | 0x40560040 | FULL | Interrupt Line Enable |
| FLEXRAY0_T0C | 0x40560044 | FULL | Timer 0 Configuration |
| FLEXRAY0_T1C | 0x40560048 | FULL | Timer 1 Configuration |
| FLEXRAY0_STPW1 | 0x4056004C | FULL | Stop Watch Register 1 |
| FLEXRAY0_STPW2 | 0x40560050 | FULL | Stop Watch Register 2 |
| FLEXRAY0_SUCC1 | 0x40560080 | FULL | SUC Configuration Register 1 |
| FLEXRAY0_SUCC2 | 0x40560084 | FULL | SUC Configuration Register 2 |
| FLEXRAY0_SUCC3 | 0x40560088 | FULL | SUC Configuration Register 3 |
| FLEXRAY0_NEMC | 0x4056008C | FULL | NEM Configuration Register |
| FLEXRAY0_PRTC1 | 0x40560090 | FULL | PRT Configuration Register 1 |
| FLEXRAY0_PRTC2 | 0x40560094 | FULL | PRT Configuration Register 2 |
| FLEXRAY0_MHDC | 0x40560098 | FULL | MHD Configuration Register |
| FLEXRAY0_GTUC1 | 0x405600A0 | FULL | GTU Configuration Register 1 |
| FLEXRAY0_GTUC2 | 0x405600A4 | FULL | GTU Configuration Register 2 |
| FLEXRAY0_GTUC3 | 0x405600A8 | FULL | GTU Configuration Register 3 |
| FLEXRAY0_GTUC4 | 0x405600AC | FULL | GTU Configuration Register 4 |
| FLEXRAY0_GTUC5 | 0x405600B0 | FULL | GTU Configuration Register 5 |
| FLEXRAY0_GTUC6 | 0x405600B4 | FULL | GTU Configuration Register 6 |
| FLEXRAY0_GTUC7 | 0x405600B8 | FULL | GTU Configuration Register 7 |
| FLEXRAY0_GTUC8 | 0x405600BC | FULL | GTU Configuration Register 8 |
| FLEXRAY0_GTUC9 | 0x405600C0 | FULL | GTU Configuration Register 9 |
| FLEXRAY0_GTUC10 | 0x405600C4 | FULL | GTU Configuration Register 10 |
| FLEXRAY0_GTUC11 | 0x405600C8 | FULL | GTU Configuration Register 11 |
| FLEXRAY0_CCSV | 0x40560100 | FULL | CC Status Vector |
| FLEXRAY0_CCEV | 0x40560104 | FULL | CC Error Vector |
| FLEXRAY0_SCV | 0x40560110 | FULL | Slot Counter Value |
| FLEXRAY0_MTCCV | 0x40560114 | FULL | Macrotick and Cycle Counter Value |
| FLEXRAY0_RCV | 0x40560118 | FULL | Rate Correction Value |
| FLEXRAY0_OCV | 0x4056011C | FULL | Offset Correction Value |
| FLEXRAY0_SFS | 0x40560120 | FULL | Sync Frame Status |
| FLEXRAY0_SWNIT | 0x40560124 | FULL | Symbol Window and NIT Status |
| FLEXRAY0_ACS | 0x40560128 | FULL | Aggregated Channel Status |
| FLEXRAY0_ESID0 | 0x40560130 | FULL | Even Sync ID [1...15] |
| FLEXRAY0_ESID1 | 0x40560134 | FULL | Even Sync ID [1...15] |
| FLEXRAY0_ESID2 | 0x40560138 | FULL | Even Sync ID [1...15] |
| FLEXRAY0_ESID3 | 0x4056013C | FULL | Even Sync ID [1...15] |
| FLEXRAY0_ESID4 | 0x40560140 | FULL | Even Sync ID [1...15] |
| FLEXRAY0_ESID5 | 0x40560144 | FULL | Even Sync ID [1...15] |
| FLEXRAY0_ESID6 | 0x40560148 | FULL | Even Sync ID [1...15] |
| FLEXRAY0_ESID7 | 0x4056014C | FULL | Even Sync ID [1...15] |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| FLEXRAY0_ESID8 | 0x40560150 | FULL | Even Sync ID [1...15] |
| FLEXRAY0_ESID9 | 0x40560154 | FULL | Even Sync ID [1...15] |
| FLEXRAY0_ESID10 | 0x40560158 | FULL | Even Sync ID [1...15] |
| FLEXRAY0_ESID11 | 0x4056015C | FULL | Even Sync ID [1...15] |
| FLEXRAY0_ESID12 | 0x40560160 | FULL | Even Sync ID [1...15] |
| FLEXRAY0_ESID13 | 0x40560164 | FULL | Even Sync ID [1...15] |
| FLEXRAY0_ESID14 | 0x40560168 | FULL | Even Sync ID [1...15] |
| FLEXRAY0_OSID0 | 0x40560170 | FULL | Odd Sync ID [1...15] |
| FLEXRAY0_OSID1 | 0x40560174 | FULL | Odd Sync ID [1...15] |
| FLEXRAY0_OSID2 | 0x40560178 | FULL | Odd Sync ID [1...15] |
| FLEXRAY0_OSID3 | 0x4056017C | FULL | Odd Sync ID [1...15] |
| FLEXRAY0_OSID4 | 0x40560180 | FULL | Odd Sync ID [1...15] |
| FLEXRAY0_OSID5 | 0x40560184 | FULL | Odd Sync ID [1...15] |
| FLEXRAY0_OSID6 | 0x40560188 | FULL | Odd Sync ID [1...15] |
| FLEXRAY0_OSID7 | 0x4056018C | FULL | Odd Sync ID [1...15] |
| FLEXRAY0_OSID8 | 0x40560190 | FULL | Odd Sync ID [1...15] |
| FLEXRAY0_OSID9 | 0x40560194 | FULL | Odd Sync ID [1...15] |
| FLEXRAY0_OSID10 | 0x40560198 | FULL | Odd Sync ID [1...15] |
| FLEXRAY0_OSID11 | 0x4056019C | FULL | Odd Sync ID [1...15] |
| FLEXRAY0_OSID12 | 0x405601A0 | FULL | Odd Sync ID [1...15] |
| FLEXRAY0_OSID13 | 0x405601A4 | FULL | Odd Sync ID [1...15] |
| FLEXRAY0_OSID14 | 0x405601A8 | FULL | Odd Sync ID [1...15] |
| FLEXRAY0_NMV1 | 0x405601B0 | FULL | Network Management Vector 1 |
| FLEXRAY0_NMV2 | 0x405601B4 | FULL | Network Management Vector 2 |
| FLEXRAY0_NMV3 | 0x405601B8 | FULL | Network Management Vector 3 |
| FLEXRAY0_MRC | 0x40560300 | FULL | Message RAM Configuration |
| FLEXRAY0_FRF | 0x40560304 | FULL | FIFO Rejection Filter |
| FLEXRAY0_FRFM | 0x40560308 | FULL | FIFO Rejection Filter Mask |
| FLEXRAY0_FCL | 0x4056030C | FULL | FIFO Critical Level |
| FLEXRAY0_MHDS | 0x40560310 | FULL | Message Handler Status |
| FLEXRAY0_LDTS | 0x40560314 | FULL | Last Dynamic Transmit Slot |
| FLEXRAY0_FSR | 0x40560318 | FULL | FIFO Status Register |
| FLEXRAY0_MHDF | 0x4056031C | FULL | Message Handler Constraints Flags |
| FLEXRAY0_TXRQ1 | 0x40560320 | FULL | Transmission Request 1 |
| FLEXRAY0_TXRQ2 | 0x40560324 | FULL | Transmission Request 2 |
| FLEXRAY0_TXRQ3 | 0x40560328 | FULL | Transmission Request 3 |
| FLEXRAY0_TXRQ4 | 0x4056032C | FULL | Transmission Request 4 |
| FLEXRAY0_NDAT1 | 0x40560330 | FULL | New Data 1 |
| FLEXRAY0_NDAT2 | 0x40560334 | FULL | New Data 2 |
| FLEXRAY0_NDAT3 | 0x40560338 | FULL | New Data 3 |
| FLEXRAY0_NDAT4 | 0x4056033C | FULL | New Data 4 |
| FLEXRAY0_MBSC1 | 0x40560340 | FULL | Message Buffer Status Changed 1 |
| FLEXRAY0_MBSC2 | 0x40560344 | FULL | Message Buffer Status Changed 2 |
| FLEXRAY0_MBSC3 | 0x40560348 | FULL | Message Buffer Status Changed 3 |
| FLEXRAY0_MBSC4 | 0x4056034C | FULL | Message Buffer Status Changed 4 |
| FLEXRAY0_CREL | 0x405603F0 | FULL | Core Release Register |
| FLEXRAY0_ENDN | 0x405603F4 | FULL | Endian Register |
| FLEXRAY0_WRDS0 | 0x40560400 | FULL | Write Data Section [1...64] |
| FLEXRAY0_WRDS1 | 0x40560404 | FULL | Write Data Section [1...64] |
| FLEXRAY0_WRDS2 | 0x40560408 | FULL | Write Data Section [1...64] |
| FLEXRAY0_WRDS3 | 0x4056040C | FULL | Write Data Section [1...64] |
| FLEXRAY0_WRDS4 | 0x40560410 | FULL | Write Data Section [1...64] |
| FLEXRAY0_WRDS5 | 0x40560414 | FULL | Write Data Section [1...64] |
| FLEXRAY0_WRDS6 | 0x40560418 | FULL | Write Data Section [1...64] |
| FLEXRAY0_WRDS7 | 0x4056041C | FULL | Write Data Section [1...64] |
| FLEXRAY0_WRDS8 | 0x40560420 | FULL | Write Data Section [1...64] |
| FLEXRAY0_WRDS9 | 0x40560424 | FULL | Write Data Section [1...64] |
| FLEXRAY0_WRDS10 | 0x40560428 | FULL | Write Data Section [1...64] |
| FLEXRAY0_WRDS11 | 0x4056042C | FULL | Write Data Section [1...64] |
| FLEXRAY0_WRDS12 | 0x40560430 | FULL | Write Data Section [1...64] |
| FLEXRAY0_WRDS13 | 0x40560434 | FULL | Write Data Section [1...64] |
| FLEXRAY0_WRDS14 | 0x40560438 | FULL | Write Data Section [1...64] |
| FLEXRAY0_WRDS15 | 0x4056043C | FULL | Write Data Section [1...64] |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| FLEXRAY0_WRDS16 | 0x40560440 | FULL | Write Data Section [1...64] |
| FLEXRAY0_WRDS17 | 0x40560444 | FULL | Write Data Section [1...64] |
| FLEXRAY0_WRDS18 | 0x40560448 | FULL | Write Data Section [1...64] |
| FLEXRAY0_WRDS19 | 0x4056044C | FULL | Write Data Section [1...64] |
| FLEXRAY0_WRDS20 | 0x40560450 | FULL | Write Data Section [1...64] |
| FLEXRAY0_WRDS21 | 0x40560454 | FULL | Write Data Section [1...64] |
| FLEXRAY0_WRDS22 | 0x40560458 | FULL | Write Data Section [1...64] |
| FLEXRAY0_WRDS23 | 0x4056045C | FULL | Write Data Section [1...64] |
| FLEXRAY0_WRDS24 | 0x40560460 | FULL | Write Data Section [1...64] |
| FLEXRAY0_WRDS25 | 0x40560464 | FULL | Write Data Section [1...64] |
| FLEXRAY0_WRDS26 | 0x40560468 | FULL | Write Data Section [1...64] |
| FLEXRAY0_WRDS27 | 0x4056046C | FULL | Write Data Section [1...64] |
| FLEXRAY0_WRDS28 | 0x40560470 | FULL | Write Data Section [1...64] |
| FLEXRAY0_WRDS29 | 0x40560474 | FULL | Write Data Section [1...64] |
| FLEXRAY0_WRDS30 | 0x40560478 | FULL | Write Data Section [1...64] |
| FLEXRAY0_WRDS31 | 0x4056047C | FULL | Write Data Section [1...64] |
| FLEXRAY0_WRDS32 | 0x40560480 | FULL | Write Data Section [1...64] |
| FLEXRAY0_WRDS33 | 0x40560484 | FULL | Write Data Section [1...64] |
| FLEXRAY0_WRDS34 | 0x40560488 | FULL | Write Data Section [1...64] |
| FLEXRAY0_WRDS35 | 0x4056048C | FULL | Write Data Section [1...64] |
| FLEXRAY0_WRDS36 | 0x40560490 | FULL | Write Data Section [1...64] |
| FLEXRAY0_WRDS37 | 0x40560494 | FULL | Write Data Section [1...64] |
| FLEXRAY0_WRDS38 | 0x40560498 | FULL | Write Data Section [1...64] |
| FLEXRAY0_WRDS39 | 0x4056049C | FULL | Write Data Section [1...64] |
| FLEXRAY0_WRDS40 | 0x405604A0 | FULL | Write Data Section [1...64] |
| FLEXRAY0_WRDS41 | 0x405604A4 | FULL | Write Data Section [1...64] |
| FLEXRAY0_WRDS42 | 0x405604A8 | FULL | Write Data Section [1...64] |
| FLEXRAY0_WRDS43 | 0x405604AC | FULL | Write Data Section [1...64] |
| FLEXRAY0_WRDS44 | 0x405604B0 | FULL | Write Data Section [1...64] |
| FLEXRAY0_WRDS45 | 0x405604B4 | FULL | Write Data Section [1...64] |
| FLEXRAY0_WRDS46 | 0x405604B8 | FULL | Write Data Section [1...64] |
| FLEXRAY0_WRDS47 | 0x405604BC | FULL | Write Data Section [1...64] |
| FLEXRAY0_WRDS48 | 0x405604C0 | FULL | Write Data Section [1...64] |
| FLEXRAY0_WRDS49 | 0x405604C4 | FULL | Write Data Section [1...64] |
| FLEXRAY0_WRDS50 | 0x405604C8 | FULL | Write Data Section [1...64] |
| FLEXRAY0_WRDS51 | 0x405604CC | FULL | Write Data Section [1...64] |
| FLEXRAY0_WRDS52 | 0x405604D0 | FULL | Write Data Section [1...64] |
| FLEXRAY0_WRDS53 | 0x405604D4 | FULL | Write Data Section [1...64] |
| FLEXRAY0_WRDS54 | 0x405604D8 | FULL | Write Data Section [1...64] |
| FLEXRAY0_WRDS55 | 0x405604DC | FULL | Write Data Section [1...64] |
| FLEXRAY0_WRDS56 | 0x405604E0 | FULL | Write Data Section [1...64] |
| FLEXRAY0_WRDS57 | 0x405604E4 | FULL | Write Data Section [1...64] |
| FLEXRAY0_WRDS58 | 0x405604E8 | FULL | Write Data Section [1...64] |
| FLEXRAY0_WRDS59 | 0x405604EC | FULL | Write Data Section [1...64] |
| FLEXRAY0_WRDS60 | 0x405604F0 | FULL | Write Data Section [1...64] |
| FLEXRAY0_WRDS61 | 0x405604F4 | FULL | Write Data Section [1...64] |
| FLEXRAY0_WRDS62 | 0x405604F8 | FULL | Write Data Section [1...64] |
| FLEXRAY0_WRDS63 | 0x405604FC | FULL | Write Data Section [1...64] |
| FLEXRAY0_WRHS1 | 0x40560500 | FULL | Write Header Section 1 |
| FLEXRAY0_WRHS2 | 0x40560504 | FULL | Write Header Section 2 |
| FLEXRAY0_WRHS3 | 0x40560508 | FULL | Write Header Section 3 |
| FLEXRAY0_IBCM | 0x40560510 | FULL | Input Buffer Command Mask |
| FLEXRAY0_IBCR | 0x40560514 | FULL | Input Buffer Command Request |
| FLEXRAY0_RDDS0 | 0x40560600 | FULL | Read Data Section [1...64] |
| FLEXRAY0_RDDS1 | 0x40560604 | FULL | Read Data Section [1...64] |
| FLEXRAY0_RDDS2 | 0x40560608 | FULL | Read Data Section [1...64] |
| FLEXRAY0_RDDS3 | 0x4056060C | FULL | Read Data Section [1...64] |
| FLEXRAY0_RDDS4 | 0x40560610 | FULL | Read Data Section [1...64] |
| FLEXRAY0_RDDS5 | 0x40560614 | FULL | Read Data Section [1...64] |
| FLEXRAY0_RDDS6 | 0x40560618 | FULL | Read Data Section [1...64] |
| FLEXRAY0_RDDS7 | 0x4056061C | FULL | Read Data Section [1...64] |
| FLEXRAY0_RDDS8 | 0x40560620 | FULL | Read Data Section [1...64] |
| FLEXRAY0_RDDS9 | 0x40560624 | FULL | Read Data Section [1...64] |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| FLEXRAY0_RDDS10 | 0x40560628 | FULL | Read Data Section [1...64] |
| FLEXRAY0_RDDS11 | 0x4056062C | FULL | Read Data Section [1...64] |
| FLEXRAY0_RDDS12 | 0x40560630 | FULL | Read Data Section [1...64] |
| FLEXRAY0_RDDS13 | 0x40560634 | FULL | Read Data Section [1...64] |
| FLEXRAY0_RDDS14 | 0x40560638 | FULL | Read Data Section [1...64] |
| FLEXRAY0_RDDS15 | 0x4056063C | FULL | Read Data Section [1...64] |
| FLEXRAY0_RDDS16 | 0x40560640 | FULL | Read Data Section [1...64] |
| FLEXRAY0_RDDS17 | 0x40560644 | FULL | Read Data Section [1...64] |
| FLEXRAY0_RDDS18 | 0x40560648 | FULL | Read Data Section [1...64] |
| FLEXRAY0_RDDS19 | 0x4056064C | FULL | Read Data Section [1...64] |
| FLEXRAY0_RDDS20 | 0x40560650 | FULL | Read Data Section [1...64] |
| FLEXRAY0_RDDS21 | 0x40560654 | FULL | Read Data Section [1...64] |
| FLEXRAY0_RDDS22 | 0x40560658 | FULL | Read Data Section [1...64] |
| FLEXRAY0_RDDS23 | 0x4056065C | FULL | Read Data Section [1...64] |
| FLEXRAY0_RDDS24 | 0x40560660 | FULL | Read Data Section [1...64] |
| FLEXRAY0_RDDS25 | 0x40560664 | FULL | Read Data Section [1...64] |
| FLEXRAY0_RDDS26 | 0x40560668 | FULL | Read Data Section [1...64] |
| FLEXRAY0_RDDS27 | 0x4056066C | FULL | Read Data Section [1...64] |
| FLEXRAY0_RDDS28 | 0x40560670 | FULL | Read Data Section [1...64] |
| FLEXRAY0_RDDS29 | 0x40560674 | FULL | Read Data Section [1...64] |
| FLEXRAY0_RDDS30 | 0x40560678 | FULL | Read Data Section [1...64] |
| FLEXRAY0_RDDS31 | 0x4056067C | FULL | Read Data Section [1...64] |
| FLEXRAY0_RDDS32 | 0x40560680 | FULL | Read Data Section [1...64] |
| FLEXRAY0_RDDS33 | 0x40560684 | FULL | Read Data Section [1...64] |
| FLEXRAY0_RDDS34 | 0x40560688 | FULL | Read Data Section [1...64] |
| FLEXRAY0_RDDS35 | 0x4056068C | FULL | Read Data Section [1...64] |
| FLEXRAY0_RDDS36 | 0x40560690 | FULL | Read Data Section [1...64] |
| FLEXRAY0_RDDS37 | 0x40560694 | FULL | Read Data Section [1...64] |
| FLEXRAY0_RDDS38 | 0x40560698 | FULL | Read Data Section [1...64] |
| FLEXRAY0_RDDS39 | 0x4056069C | FULL | Read Data Section [1...64] |
| FLEXRAY0_RDDS40 | 0x405606A0 | FULL | Read Data Section [1...64] |
| FLEXRAY0_RDDS41 | 0x405606A4 | FULL | Read Data Section [1...64] |
| FLEXRAY0_RDDS42 | 0x405606A8 | FULL | Read Data Section [1...64] |
| FLEXRAY0_RDDS43 | 0x405606AC | FULL | Read Data Section [1...64] |
| FLEXRAY0_RDDS44 | 0x405606B0 | FULL | Read Data Section [1...64] |
| FLEXRAY0_RDDS45 | 0x405606B4 | FULL | Read Data Section [1...64] |
| FLEXRAY0_RDDS46 | 0x405606B8 | FULL | Read Data Section [1...64] |
| FLEXRAY0_RDDS47 | 0x405606BC | FULL | Read Data Section [1...64] |
| FLEXRAY0_RDDS48 | 0x405606C0 | FULL | Read Data Section [1...64] |
| FLEXRAY0_RDDS49 | 0x405606C4 | FULL | Read Data Section [1...64] |
| FLEXRAY0_RDDS50 | 0x405606C8 | FULL | Read Data Section [1...64] |
| FLEXRAY0_RDDS51 | 0x405606CC | FULL | Read Data Section [1...64] |
| FLEXRAY0_RDDS52 | 0x405606D0 | FULL | Read Data Section [1...64] |
| FLEXRAY0_RDDS53 | 0x405606D4 | FULL | Read Data Section [1...64] |
| FLEXRAY0_RDDS54 | 0x405606D8 | FULL | Read Data Section [1...64] |
| FLEXRAY0_RDDS55 | 0x405606DC | FULL | Read Data Section [1...64] |
| FLEXRAY0_RDDS56 | 0x405606E0 | FULL | Read Data Section [1...64] |
| FLEXRAY0_RDDS57 | 0x405606E4 | FULL | Read Data Section [1...64] |
| FLEXRAY0_RDDS58 | 0x405606E8 | FULL | Read Data Section [1...64] |
| FLEXRAY0_RDDS59 | 0x405606EC | FULL | Read Data Section [1...64] |
| FLEXRAY0_RDDS60 | 0x405606F0 | FULL | Read Data Section [1...64] |
| FLEXRAY0_RDDS61 | 0x405606F4 | FULL | Read Data Section [1...64] |
| FLEXRAY0_RDDS62 | 0x405606F8 | FULL | Read Data Section [1...64] |
| FLEXRAY0_RDDS63 | 0x405606FC | FULL | Read Data Section [1...64] |
| FLEXRAY0_RDHS1 | 0x40560700 | FULL | Read Header Section 1 |
| FLEXRAY0_RDHS2 | 0x40560704 | FULL | Read Header Section 2 |
| FLEXRAY0_RDHS3 | 0x40560708 | FULL | Read Header Section 3 |
| FLEXRAY0_MBS | 0x4056070C | FULL | Message Buffer Status |
| FLEXRAY0_OBCM | 0x40560710 | FULL | Output Buffer Command Mask |
| FLEXRAY0_OBCR | 0x40560714 | FULL | Output Buffer Command Request |
| FLEXRAY0_WRHS1_MIR2 | 0x40560BF0 | FULL | Write Header Section 1 (2nd mirror) |
| FLEXRAY0_WRHS2_MIR2 | 0x40560BF4 | FULL | Write Header Section 2 (2nd mirror) |
| FLEXRAY0_WRHS3_MIR2 | 0x40560BF8 | FULL | Write Header Section 3 (2nd mirror) |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| FLEXRAY0_WRDS_MIR0 | 0x40560C00 | FULL | Write Data Section [1...64] (mirror) |
| FLEXRAY0_WRDS_MIR1 | 0x40560C04 | FULL | Write Data Section [1...64] (mirror) |
| FLEXRAY0_WRDS_MIR2 | 0x40560C08 | FULL | Write Data Section [1...64] (mirror) |
| FLEXRAY0_WRDS_MIR3 | 0x40560C0C | FULL | Write Data Section [1...64] (mirror) |
| FLEXRAY0_WRDS_MIR4 | 0x40560C10 | FULL | Write Data Section [1...64] (mirror) |
| FLEXRAY0_WRDS_MIR5 | 0x40560C14 | FULL | Write Data Section [1...64] (mirror) |
| FLEXRAY0_WRDS_MIR6 | 0x40560C18 | FULL | Write Data Section [1...64] (mirror) |
| FLEXRAY0_WRDS_MIR7 | 0x40560C1C | FULL | Write Data Section [1...64] (mirror) |
| FLEXRAY0_WRDS_MIR8 | 0x40560C20 | FULL | Write Data Section [1...64] (mirror) |
| FLEXRAY0_WRDS_MIR9 | 0x40560C24 | FULL | Write Data Section [1...64] (mirror) |
| FLEXRAY0_WRDS_MIR10 | 0x40560C28 | FULL | Write Data Section [1...64] (mirror) |
| FLEXRAY0_WRDS_MIR11 | 0x40560C2C | FULL | Write Data Section [1...64] (mirror) |
| FLEXRAY0_WRDS_MIR12 | 0x40560C30 | FULL | Write Data Section [1...64] (mirror) |
| FLEXRAY0_WRDS_MIR13 | 0x40560C34 | FULL | Write Data Section [1...64] (mirror) |
| FLEXRAY0_WRDS_MIR14 | 0x40560C38 | FULL | Write Data Section [1...64] (mirror) |
| FLEXRAY0_WRDS_MIR15 | 0x40560C3C | FULL | Write Data Section [1...64] (mirror) |
| FLEXRAY0_WRDS_MIR16 | 0x40560C40 | FULL | Write Data Section [1...64] (mirror) |
| FLEXRAY0_WRDS_MIR17 | 0x40560C44 | FULL | Write Data Section [1...64] (mirror) |
| FLEXRAY0_WRDS_MIR18 | 0x40560C48 | FULL | Write Data Section [1...64] (mirror) |
| FLEXRAY0_WRDS_MIR19 | 0x40560C4C | FULL | Write Data Section [1...64] (mirror) |
| FLEXRAY0_WRDS_MIR20 | 0x40560C50 | FULL | Write Data Section [1...64] (mirror) |
| FLEXRAY0_WRDS_MIR21 | 0x40560C54 | FULL | Write Data Section [1...64] (mirror) |
| FLEXRAY0_WRDS_MIR22 | 0x40560C58 | FULL | Write Data Section [1...64] (mirror) |
| FLEXRAY0_WRDS_MIR23 | 0x40560C5C | FULL | Write Data Section [1...64] (mirror) |
| FLEXRAY0_WRDS_MIR24 | 0x40560C60 | FULL | Write Data Section [1...64] (mirror) |
| FLEXRAY0_WRDS_MIR25 | 0x40560C64 | FULL | Write Data Section [1...64] (mirror) |
| FLEXRAY0_WRDS_MIR26 | 0x40560C68 | FULL | Write Data Section [1...64] (mirror) |
| FLEXRAY0_WRDS_MIR27 | 0x40560C6C | FULL | Write Data Section [1...64] (mirror) |
| FLEXRAY0_WRDS_MIR28 | 0x40560C70 | FULL | Write Data Section [1...64] (mirror) |
| FLEXRAY0_WRDS_MIR29 | 0x40560C74 | FULL | Write Data Section [1...64] (mirror) |
| FLEXRAY0_WRDS_MIR30 | 0x40560C78 | FULL | Write Data Section [1...64] (mirror) |
| FLEXRAY0_WRDS_MIR31 | 0x40560C7C | FULL | Write Data Section [1...64] (mirror) |
| FLEXRAY0_WRDS_MIR32 | 0x40560C80 | FULL | Write Data Section [1...64] (mirror) |
| FLEXRAY0_WRDS_MIR33 | 0x40560C84 | FULL | Write Data Section [1...64] (mirror) |
| FLEXRAY0_WRDS_MIR34 | 0x40560C88 | FULL | Write Data Section [1...64] (mirror) |
| FLEXRAY0_WRDS_MIR35 | 0x40560C8C | FULL | Write Data Section [1...64] (mirror) |
| FLEXRAY0_WRDS_MIR36 | 0x40560C90 | FULL | Write Data Section [1...64] (mirror) |
| FLEXRAY0_WRDS_MIR37 | 0x40560C94 | FULL | Write Data Section [1...64] (mirror) |
| FLEXRAY0_WRDS_MIR38 | 0x40560C98 | FULL | Write Data Section [1...64] (mirror) |
| FLEXRAY0_WRDS_MIR39 | 0x40560C9C | FULL | Write Data Section [1...64] (mirror) |
| FLEXRAY0_WRDS_MIR40 | 0x40560CA0 | FULL | Write Data Section [1...64] (mirror) |
| FLEXRAY0_WRDS_MIR41 | 0x40560CA4 | FULL | Write Data Section [1...64] (mirror) |
| FLEXRAY0_WRDS_MIR42 | 0x40560CA8 | FULL | Write Data Section [1...64] (mirror) |
| FLEXRAY0_WRDS_MIR43 | 0x40560CAC | FULL | Write Data Section [1...64] (mirror) |
| FLEXRAY0_WRDS_MIR44 | 0x40560CB0 | FULL | Write Data Section [1...64] (mirror) |
| FLEXRAY0_WRDS_MIR45 | 0x40560CB4 | FULL | Write Data Section [1...64] (mirror) |
| FLEXRAY0_WRDS_MIR46 | 0x40560CB8 | FULL | Write Data Section [1...64] (mirror) |
| FLEXRAY0_WRDS_MIR47 | 0x40560CBC | FULL | Write Data Section [1...64] (mirror) |
| FLEXRAY0_WRDS_MIR48 | 0x40560CC0 | FULL | Write Data Section [1...64] (mirror) |
| FLEXRAY0_WRDS_MIR49 | 0x40560CC4 | FULL | Write Data Section [1...64] (mirror) |
| FLEXRAY0_WRDS_MIR50 | 0x40560CC8 | FULL | Write Data Section [1...64] (mirror) |
| FLEXRAY0_WRDS_MIR51 | 0x40560CCC | FULL | Write Data Section [1...64] (mirror) |
| FLEXRAY0_WRDS_MIR52 | 0x40560CD0 | FULL | Write Data Section [1...64] (mirror) |
| FLEXRAY0_WRDS_MIR53 | 0x40560CD4 | FULL | Write Data Section [1...64] (mirror) |
| FLEXRAY0_WRDS_MIR54 | 0x40560CD8 | FULL | Write Data Section [1...64] (mirror) |
| FLEXRAY0_WRDS_MIR55 | 0x40560CDC | FULL | Write Data Section [1...64] (mirror) |
| FLEXRAY0_WRDS_MIR56 | 0x40560CE0 | FULL | Write Data Section [1...64] (mirror) |
| FLEXRAY0_WRDS_MIR57 | 0x40560CE4 | FULL | Write Data Section [1...64] (mirror) |
| FLEXRAY0_WRDS_MIR58 | 0x40560CE8 | FULL | Write Data Section [1...64] (mirror) |
| FLEXRAY0_WRDS_MIR59 | 0x40560CEC | FULL | Write Data Section [1...64] (mirror) |
| FLEXRAY0_WRDS_MIR60 | 0x40560CF0 | FULL | Write Data Section [1...64] (mirror) |
| FLEXRAY0_WRDS_MIR61 | 0x40560CF4 | FULL | Write Data Section [1...64] (mirror) |
| FLEXRAY0_WRDS_MIR62 | 0x40560CF8 | FULL | Write Data Section [1...64] (mirror) |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| FLEXRAY0_WRDS_MIR63 | 0x40560CFC | FULL | Write Data Section [1...64] (mirror) |
| FLEXRAY0_WRHS1_MIR | 0x40560D00 | FULL | Write Header Section 1 (mirror) |
| FLEXRAY0_WRHS2_MIR | 0x40560D04 | FULL | Write Header Section 2 (mirror) |
| FLEXRAY0_WRHS3_MIR | 0x40560D08 | FULL | Write Header Section 3 (mirror) |
| FLEXRAY0_IBCM_MIR | 0x40560D10 | FULL | Input Buffer Command Mask (mirror) |
| FLEXRAY0_IBCR_MIR | 0x40560D14 | FULL | Input Buffer Command Request (mirror) |
| FLEXRAY0_RDHS1_MIR2 | 0x40560DF0 | FULL | Read Header Section 1 (2nd mirror) |
| FLEXRAY0_RDHS2_MIR2 | 0x40560DF4 | FULL | Read Header Section 2 (2nd mirror) |
| FLEXRAY0_RDHS3_MIR2 | 0x40560DF8 | FULL | Read Header Section 3 (2nd mirror) |
| FLEXRAY0_MBS_MIR2 | 0x40560DFC | FULL | Message Buffer Status (2nd mirror) |
| FLEXRAY0_RDDS_MIR0 | 0x40560E00 | FULL | Read Data Section [1...64] (mirror) |
| FLEXRAY0_RDDS_MIR1 | 0x40560E04 | FULL | Read Data Section [1...64] (mirror) |
| FLEXRAY0_RDDS_MIR2 | 0x40560E08 | FULL | Read Data Section [1...64] (mirror) |
| FLEXRAY0_RDDS_MIR3 | 0x40560E0C | FULL | Read Data Section [1...64] (mirror) |
| FLEXRAY0_RDDS_MIR4 | 0x40560E10 | FULL | Read Data Section [1...64] (mirror) |
| FLEXRAY0_RDDS_MIR5 | 0x40560E14 | FULL | Read Data Section [1...64] (mirror) |
| FLEXRAY0_RDDS_MIR6 | 0x40560E18 | FULL | Read Data Section [1...64] (mirror) |
| FLEXRAY0_RDDS_MIR7 | 0x40560E1C | FULL | Read Data Section [1...64] (mirror) |
| FLEXRAY0_RDDS_MIR8 | 0x40560E20 | FULL | Read Data Section [1...64] (mirror) |
| FLEXRAY0_RDDS_MIR9 | 0x40560E24 | FULL | Read Data Section [1...64] (mirror) |
| FLEXRAY0_RDDS_MIR10 | 0x40560E28 | FULL | Read Data Section [1...64] (mirror) |
| FLEXRAY0_RDDS_MIR11 | 0x40560E2C | FULL | Read Data Section [1...64] (mirror) |
| FLEXRAY0_RDDS_MIR12 | 0x40560E30 | FULL | Read Data Section [1...64] (mirror) |
| FLEXRAY0_RDDS_MIR13 | 0x40560E34 | FULL | Read Data Section [1...64] (mirror) |
| FLEXRAY0_RDDS_MIR14 | 0x40560E38 | FULL | Read Data Section [1...64] (mirror) |
| FLEXRAY0_RDDS_MIR15 | 0x40560E3C | FULL | Read Data Section [1...64] (mirror) |
| FLEXRAY0_RDDS_MIR16 | 0x40560E40 | FULL | Read Data Section [1...64] (mirror) |
| FLEXRAY0_RDDS_MIR17 | 0x40560E44 | FULL | Read Data Section [1...64] (mirror) |
| FLEXRAY0_RDDS_MIR18 | 0x40560E48 | FULL | Read Data Section [1...64] (mirror) |
| FLEXRAY0_RDDS_MIR19 | 0x40560E4C | FULL | Read Data Section [1...64] (mirror) |
| FLEXRAY0_RDDS_MIR20 | 0x40560E50 | FULL | Read Data Section [1...64] (mirror) |
| FLEXRAY0_RDDS_MIR21 | 0x40560E54 | FULL | Read Data Section [1...64] (mirror) |
| FLEXRAY0_RDDS_MIR22 | 0x40560E58 | FULL | Read Data Section [1...64] (mirror) |
| FLEXRAY0_RDDS_MIR23 | 0x40560E5C | FULL | Read Data Section [1...64] (mirror) |
| FLEXRAY0_RDDS_MIR24 | 0x40560E60 | FULL | Read Data Section [1...64] (mirror) |
| FLEXRAY0_RDDS_MIR25 | 0x40560E64 | FULL | Read Data Section [1...64] (mirror) |
| FLEXRAY0_RDDS_MIR26 | 0x40560E68 | FULL | Read Data Section [1...64] (mirror) |
| FLEXRAY0_RDDS_MIR27 | 0x40560E6C | FULL | Read Data Section [1...64] (mirror) |
| FLEXRAY0_RDDS_MIR28 | 0x40560E70 | FULL | Read Data Section [1...64] (mirror) |
| FLEXRAY0_RDDS_MIR29 | 0x40560E74 | FULL | Read Data Section [1...64] (mirror) |
| FLEXRAY0_RDDS_MIR30 | 0x40560E78 | FULL | Read Data Section [1...64] (mirror) |
| FLEXRAY0_RDDS_MIR31 | 0x40560E7C | FULL | Read Data Section [1...64] (mirror) |
| FLEXRAY0_RDDS_MIR32 | 0x40560E80 | FULL | Read Data Section [1...64] (mirror) |
| FLEXRAY0_RDDS_MIR33 | 0x40560E84 | FULL | Read Data Section [1...64] (mirror) |
| FLEXRAY0_RDDS_MIR34 | 0x40560E88 | FULL | Read Data Section [1...64] (mirror) |
| FLEXRAY0_RDDS_MIR35 | 0x40560E8C | FULL | Read Data Section [1...64] (mirror) |
| FLEXRAY0_RDDS_MIR36 | 0x40560E90 | FULL | Read Data Section [1...64] (mirror) |
| FLEXRAY0_RDDS_MIR37 | 0x40560E94 | FULL | Read Data Section [1...64] (mirror) |
| FLEXRAY0_RDDS_MIR38 | 0x40560E98 | FULL | Read Data Section [1...64] (mirror) |
| FLEXRAY0_RDDS_MIR39 | 0x40560E9C | FULL | Read Data Section [1...64] (mirror) |
| FLEXRAY0_RDDS_MIR40 | 0x40560EA0 | FULL | Read Data Section [1...64] (mirror) |
| FLEXRAY0_RDDS_MIR41 | 0x40560EA4 | FULL | Read Data Section [1...64] (mirror) |
| FLEXRAY0_RDDS_MIR42 | 0x40560EA8 | FULL | Read Data Section [1...64] (mirror) |
| FLEXRAY0_RDDS_MIR43 | 0x40560EAC | FULL | Read Data Section [1...64] (mirror) |
| FLEXRAY0_RDDS_MIR44 | 0x40560EB0 | FULL | Read Data Section [1...64] (mirror) |
| FLEXRAY0_RDDS_MIR45 | 0x40560EB4 | FULL | Read Data Section [1...64] (mirror) |
| FLEXRAY0_RDDS_MIR46 | 0x40560EB8 | FULL | Read Data Section [1...64] (mirror) |
| FLEXRAY0_RDDS_MIR47 | 0x40560EBC | FULL | Read Data Section [1...64] (mirror) |
| FLEXRAY0_RDDS_MIR48 | 0x40560EC0 | FULL | Read Data Section [1...64] (mirror) |
| FLEXRAY0_RDDS_MIR49 | 0x40560EC4 | FULL | Read Data Section [1...64] (mirror) |
| FLEXRAY0_RDDS_MIR50 | 0x40560EC8 | FULL | Read Data Section [1...64] (mirror) |
| FLEXRAY0_RDDS_MIR51 | 0x40560ECC | FULL | Read Data Section [1...64] (mirror) |
| FLEXRAY0_RDDS_MIR52 | 0x40560ED0 | FULL | Read Data Section [1...64] (mirror) |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| FLEXRAY0_RDDS_MIR53 | 0x40560ED4 | FULL | Read Data Section [1...64] (mirror) |
| FLEXRAY0_RDDS_MIR54 | 0x40560ED8 | FULL | Read Data Section [1...64] (mirror) |
| FLEXRAY0_RDDS_MIR55 | 0x40560EDC | FULL | Read Data Section [1...64] (mirror) |
| FLEXRAY0_RDDS_MIR56 | 0x40560EE0 | FULL | Read Data Section [1...64] (mirror) |
| FLEXRAY0_RDDS_MIR57 | 0x40560EE4 | FULL | Read Data Section [1...64] (mirror) |
| FLEXRAY0_RDDS_MIR58 | 0x40560EE8 | FULL | Read Data Section [1...64] (mirror) |
| FLEXRAY0_RDDS_MIR59 | 0x40560EEC | FULL | Read Data Section [1...64] (mirror) |
| FLEXRAY0_RDDS_MIR60 | 0x40560EF0 | FULL | Read Data Section [1...64] (mirror) |
| FLEXRAY0_RDDS_MIR61 | 0x40560EF4 | FULL | Read Data Section [1...64] (mirror) |
| FLEXRAY0_RDDS_MIR62 | 0x40560EF8 | FULL | Read Data Section [1...64] (mirror) |
| FLEXRAY0_RDDS_MIR63 | 0x40560EFC | FULL | Read Data Section [1...64] (mirror) |
| FLEXRAY0_RDHS1_MIR | 0x40560F00 | FULL | Read Header Section 1 (mirror) |
| FLEXRAY0_RDHS2_MIR | 0x40560F04 | FULL | Read Header Section 2 (mirror) |
| FLEXRAY0_RDHS3_MIR | 0x40560F08 | FULL | Read Header Section 3 (mirror) |
| FLEXRAY0_MBS_MIR | 0x40560F0C | FULL | Message Buffer Status (mirror) |
| FLEXRAY0_OBCM_MIR | 0x40560F10 | FULL | Output Buffer Command Mask (mirror) |
| FLEXRAY0_OBCR_MIR | 0x40560F14 | FULL | Output Buffer Command Request (mirror) |

## 15.1 Register Details

### 15.1.1 FLEXRAY_CTL

**Description:** Control Register
**Address:** 0x40560000
**Offset:** 0x0
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** IP enable
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | ENABLED [31:31] | None [30:24] | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 31 | ENABLED | RW | R | 0 | This bit enables the operation of this IP.<br>'0' : Disable. Registers FLEXRAY.CTL and FLEXRAY.DMA_CTL can be accessed normally. Access to all other registers within FLEXRAY results in a bus error response.<br>'1' : Enable |
| | DISABLE | | | 0 | N/A |
| | ENABLE | | | 1 | N/A |

### 15.1.2 FLEXRAY_DMA_CTL

**Description:** DMA Control Register
**Address:** 0x40560004
**Offset:** 0x4
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** DMA Control Register
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:3] | | | | | ODMAFFE [2:2] | ODMATOE [1:1] | IDMATOE [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | IDMATOE | RW | R | 0 | IBF DMA trigger output enable<br>'0' : Disable: tr_ibf_out = '0'.<br>'1' : Enable: tr_ibf_out is asserted after the detection of tr_ibf_in, postponed until IBF is not busy. |
| | DISABLE | | | 0 | N/A |
| | ENABLE | | | 1 | N/A |
| 1 | ODMATOE | RW | R | 0 | OBF DMA trigger output enable<br>'0' : Disable: tr_obf_out = '0'.<br>'1' : Enable: tr_obf_out is asserted after detection of tr_obf_in according to the setting of ODMAFFE. |
| | DISABLE | | | 0 | N/A |
| | ENABLE | | | 1 | N/A |
| 2 | ODMAFFE | RW | R | 0 | OBF DMA FIFO enable<br>'0' : Disable: tr_obf_out is postponed until OBF is not busy.<br>'1' : Enable: tr_obf_out is postponed until OBF is not busy AND the receive FIFO is not empty. |
| | DISABLE | | | 0 | N/A |
| | ENABLE | | | 1 | N/A |

### 15.1.3 FLEXRAY_TEST1

**Description:** Test Register 1
**Address:** 0x40560010
**Offset:** 0x10
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** Test Register 1
**Default:** 0x300

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:6] | | TMC [5:4] | | None [3:2] | | ELBE [1:1] | WRTEN [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:10] | | | | | | AOB [9:9] | AOA [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:22] | | TXENB [21:21] | TXENA [20:20] | TXB [19:19] | TXA [18:18] | RXB [17:17] | RXA [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | CERB [31:28] | | | | CERA [27:24] | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | WRTEN | RW | R | 0 | Write Test Register Enable<br>Enables write access to the test registers. To set the bit from '0' to '1' the test mode key has to be written as defined in [01]Section 4.3.3 Lock Register (LCK). The unlock sequence is not required when WRTEN is kept at '1' while other bits of the register are changed. The bit can be reset to '0' at any time.<br>1 = Write access to test registers enabled<br>0 = Write access to test registers disabled |
| | TEST_REG_WR_DISABLED | | | 0 | N/A |
| | TEST_REG_WR_ENABLED | | | 1 | N/A |
| 1 | ELBE | RW | R | 0 | External Loop Back Enable<br>There are two possibilities to perform a Loop Back test. External Loop Back via physical layer or internal Loop Back for in-system self-test (default). In case of an internal Loop Back pins eray_txen1,2_n are in their inactive state, pins eray_txd1,2 are set to HIGH, pins eray_rxd1,2 are not evaluated. Bit ELBE is evaluated only when POC is in Loop Back Mode and test multiplexer control is in non-multiplexing mode TMC[1:0] = '00'.<br>1 = External Loop Back<br>0 = Internal Loop Back (default) |
| | INTERNAL_LOOP_BACK | | | 0 | N/A |
| | EXTERNAL_LOOP_BACK | | | 1 | N/A |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 4:5 | TMC | RW | R | 0 | Test Multiplexer Control<br>00, 11= Normal signal path (default)<br>01 = RAM Test Mode - Internal busses are multiplexed to make all RAM blocks of the ERay module directly accessible by the Host. This mode is intended to enable testing of the embedded RAM blocks during production testing.<br>10 = I/O Test Mode - Output pins eray_txd1, eray_txd2, eray_txen1_n, eray_txen2_n, are driven to the values defined by bits TXA, TXB, TXENA, TXENB. The values applied to the input pins eray_rxd1, eray_rxd2 can be read from register bits RXA, RXB. |
| | NORMAL_SIGNAL_PATH | | | 0 | N/A |
| | NORMAL_SIGNAL_PATH_MIRROR | | | 3 | N/A |
| | RAM_TEST_MODE | | | 1 | N/A |
| | IO_TEST_MODE | | | 2 | N/A |
| 8 | AOA | R | RW | 1 | Activity on A<br>AOA is set when there is activity on channel A. It is reset when 11 consecutive '1' bits are detected or if the POC state is DEFAULT_CONFIG or CONFIG. During STARTUP, NORMAL_ACTIVE, or NORMAL_PASSIVE the function of AOA is the inverse of zChannelIdle as specified in the FlexRay protocol spec v2.1, chapter 3, BITSTRB process. AOA should be ignored in all other POC states.<br>1 = Activity detected, channel A not idle<br>0 = No activity detected, channel A idle |
| | NOACT_DETECT_CH_A_IDLE | | | 0 | N/A |
| | ACT_DETECT_CH_A_NOT_IDLE | | | 1 | N/A |
| 9 | AOB | R | RW | 1 | Activity on B<br>AOB is set when there is activity on channel B. It is reset when 11 consecutive '1' bits are detected or if the POC state is DEFAULT_CONFIG or CONFIG. During STARTUP, NORMAL_ACTIVE, or NORMAL_PASSIVE the function of AOB is the inverse of zChannel-Idle as specified in the FlexRay protocol spec v2.1, chapter 3, BITSTRB process. AOB should be ignored in all other POC states.<br>1 = Activity detected, channel B not idle<br>0 = No activity detected, channel B idle |
| | NOACT_DETECT_CH_B_IDLE | | | 0 | N/A |
| | ACT_DETECT_CH_B_NOT_IDLE | | | 1 | N/A |
| 16 | RXA | R | RW | 0 | Monitor Channel A Receive Pin<br>This is used to test the interface to the physical layer (connectivity test) by reading the pin.<br>0 = eray_rxd1 = '0'<br>1 = eray_rxd1 = '1' |
| | ERAY_RXD1_0 | | | 0 | N/A |
| | ERAY_RXD1_1 | | | 1 | N/A |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 17 | RXB | R | RW | 0 | Monitor Channel B Receive Pin<br>This is used to test the interface to the physical layer (connectivity test) by reading the pin.<br>0 = eray_rxd2 = '0'<br>1 = eray_rxd2 = '1' |
| | ERAY_RXD2_0 | | | 0 | N/A |
| | ERAY_RXD2_1 | | | 1 | N/A |
| 18 | TXA | RW | R | 0 | Control of Channel A Transmit Pin<br>This is used to test the interface to the physical layer (connectivity test) by driving the pin.<br>0 = eray_txd1 pin drives a '0'<br>1 = eray_txd1 pin drives a '1' |
| | ERAY_TXD1_0 | | | 0 | N/A |
| | ERAY_TXD1_1 | | | 1 | N/A |
| 19 | TXB | RW | R | 0 | Control of Channel B Transmit Pin<br>This is used to test the interface to the physical layer (connectivity test) by driving the pin.<br>0 = eray_txd2 pin drives a '0'<br>1 = eray_txd2 pin drives a '1' |
| | ERAY_TXD2_0 | | | 0 | N/A |
| | ERAY_TXD2_1 | | | 1 | N/A |
| 20 | TXENA | RW | R | 0 | Control of Channel A Transmit Enable Pin<br>This is used to test the interface to the physical layer (connectivity test) by driving the pin.<br>0 = eray_txen1_n pin drives a '0'<br>1 = eray_txen1_n pin drives a '1' |
| | ERAY_TXEN1_N_0 | | | 0 | N/A |
| | ERAY_TXEN1_N_1 | | | 1 | N/A |
| 21 | TXENB | RW | R | 0 | Control of Channel B Transmit Enable Pin<br>This is used to test the interface to the physical layer (connectivity test) by driving the pin.<br>0 = eray_txen2_n pin drives a '0'<br>1 = eray_txen2_n pin drives a '1' |
| | ERAY_TXEN2_N_0 | | | 0 | N/A |
| | ERAY_TXEN2_N_1 | | | 1 | N/A |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 24:27 | CERA | R | RW | 0 | Coding Error Report Channel A<br>Set when a coding error is detected on channel A. Reset to zero when register TEST1 is read or written. Once the CERA[3:0] is set it will remain unchanged until TEST1 register is accessed.<br>0000 = No coding error detected<br>0001 = Header CRC error detected<br>0010 = Frame CRC error detected<br>0011 = Frame Start Sequence FSS too long<br>0100 = First bit of Byte Start Sequence BSS seen LOW<br>0101 = Second bit of Byte Start Sequence BSS seen HIGH<br>0110 = First bit of Frame End Sequence FES seen HIGH<br>0111 = Second bit of Frame End Sequence FES seen LOW<br>1000 = CAS / MTS symbol seen too short<br>1001 = CAS / MTS symbol seen too long<br>1010...1111 =reserved<br>Note: Coding errors are signalled in all states where frame decoding is possible. CERA[3:0] and CERB[3:0] should be ignored in all other states.<br>The error codes regarding CAS / MTS symbols concern only the monitored bit pattern, irrelevant whether those bit patterns are seen in the symbol window or elsewhere. |
| | NO_CODING_ERR | | | 0 | N/A |
| | HEADER_CRC_ERR | | | 1 | N/A |
| | FRAME_CRC_ERR | | | 2 | N/A |
| | FRAME_START_SEQ_FSS_LONG | | | 3 | N/A |
| | FIRST_BIT_OF_BSS_LOW | | | 4 | N/A |
| | SECOND_BIT_OF_BSS_HIGH | | | 5 | N/A |
| | FIRST_BIT_OF_FES_HIGH | | | 6 | N/A |
| | SECOND_BIT_OF_FES_LOW | | | 7 | N/A |
| | CAS_MTS_SYMBOL_SHORT | | | 8 | N/A |
| | CAS_MTS_SYMBOL_LONG | | | 9 | N/A |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 28:31 | CERB | R | RW | 0 | Coding Error Report Channel B<br>Set when a coding error is detected on channel B. Reset to zero when register TEST1 is read or written. Once the CERB[3:0] is set it will remain unchanged until TEST1 register is accessed.<br>0000 = No coding error detected<br>0001 = Header CRC error detected<br>0010 = Frame CRC error detected<br>0011 = Frame Start Sequence FSS too long<br>0100 = First bit of Byte Start Sequence BSS seen LOW<br>0101 = Second bit of Byte Start Sequence BSS seen HIGH<br>0110 = First bit of Frame End Sequence FES seen HIGH<br>0111 = Second bit of Frame End Sequence FES seen LOW<br>1000 = CAS / MTS symbol seen too short<br>1001 = CAS / MTS symbol seen too long<br>1010...1111 =reserved<br>Note: Coding errors are signalled in all states where frame decoding is possible. CERA[3:0] and CERB[3:0] should be ignored in all other states.<br>The error codes regarding CAS / MTS symbols concern only the monitored bit pattern, irrelevant whether those bit patterns are seen in the symbol window or elsewhere. |
| | NO_CODING_ERR | | | 0 | N/A |
| | HEADER_CRC_ERR | | | 1 | N/A |
| | FRAME_CRC_ERR | | | 2 | N/A |
| | FRAME_START_SEQ_FSS_LONG | | | 3 | N/A |
| | FIRST_BIT_OF_BSS_LOW | | | 4 | N/A |
| | SECOND_BIT_OF_BSS_HIGH | | | 5 | N/A |
| | FIRST_BIT_OF_FES_HIGH | | | 6 | N/A |
| | SECOND_BIT_OF_FES_LOW | | | 7 | N/A |
| | CAS_MTS_SYMBOL_SHORT | | | 8 | N/A |
| | CAS_MTS_SYMBOL_LONG | | | 9 | N/A |

### 15.1.4 FLEXRAY_TEST2

**Description:** Test Register 2
**Address:** 0x40560014
**Offset:** 0x14
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** Test Register 2
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:7] | SSEL [6:4] | | | None [3:3] | RS [2:0] | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | RDPB [15:15] | WRPB [14:14] | None [13:8] | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:2 | RS | RW | R | 0 | RAM Select<br>In RAM Test mode the RAM blocks selected by RS[2:0] are mapped to module address 0x400 to 7FF (1024 byte addresses).<br>000 = Input Buffer RAM 1 (IBF1)<br>001 = Input Buffer RAM 2 (IBF2)<br>010 = Output Buffer RAM 1 (OBF1)<br>011 = Output Buffer RAM 2 (OBF2)<br>100 = Transient Buffer RAM A (TBF1)<br>101 = Transient Buffer RAM B (TBF2)<br>110 = Message RAM (MBF)<br>111 = unused |
| | IBF1 | | | 0 | N/A |
| | IBF2 | | | 1 | N/A |
| | OBF1 | | | 2 | N/A |
| | OBF2 | | | 3 | N/A |
| | TBF1 | | | 4 | N/A |
| | TBF2 | | | 5 | N/A |
| | MBF | | | 6 | N/A |
| 4:6 | SSEL | RW | R | 0 | Segment Select<br>To enable access to the complete Message RAM (8192 byte addresses) the Message RAM is segmented.<br>000 = access to RAM bytes 0000h to 03FFh enabled<br>001 = access to RAM bytes 0400h to 07FFh enabled<br>010 = access to RAM bytes 0800h to 0BFFh enabled<br>011 = access to RAM bytes 0C00h to 0FFFh enabled<br>100 = access to RAM bytes 1000h to 13FFh enabled<br>101 = access to RAM bytes 1400h to 17FFh enabled<br>110 = access to RAM bytes 1800h to 1BFFh enabled<br>111 = access to RAM bytes 1C00h to 1FFFh enabled |
| | ADDR_0000_TO_03FF_ENABLED | | | 0 | N/A |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| | ADDR_0400_TO_07FF_ENABLED | | | 1 | N/A |
| | ADDR_0800_TO_0BFF_ENABLED | | | 2 | N/A |
| | ADDR_0C00_TO_0FFF_ENABLED | | | 3 | N/A |
| | ADDR_1000_TO_13FF_ENABLED | | | 4 | N/A |
| | ADDR_1400_TO_17FF_ENABLED | | | 5 | N/A |
| | ADDR_1800_TO_1BFF_ENABLED | | | 6 | N/A |
| | ADDR_1C00_TO_1FFF_ENABLED | | | 7 | N/A |
| 14 | WRPB | RW | R | 0 | Write Parity Bit<br>Value of parity bit to be written to bit 32 of the addressed RAM word. |
| 15 | RDPB | R | RW | 0 | Read Parity Bit<br>Value of parity bit read from bit 32 of the addressed RAM word. |

### 15.1.5 FLEXRAY_LCK

**Description:** Lock Register
**Address:** 0x4056001C
**Offset:** 0x1C
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** Write Only, Read returns 0
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | CLK [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | TMK [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | CLK | W | R | 0 | Configuration Lock Key<br>To leave CONFIG state by writing SUCC1.CMD[3:0] (commands READY,<br>MONITOR_MODE, ATM, LOOP_BACK), the write operation has to be directly preceded by<br>two write accesses to the Configuration Lock Key (unlock sequence). If the write sequence<br>below is interrupted by other write accesses between the second write to the Configuration Lock<br>Key and the write access to the SUCC1 register, the CC remains in CONFIG state and the<br>sequence has to be repeated.<br>First write: LCK.CLK[7:0] = '1100 1110' (0xCE)<br>Second write: LCK.CLK[7:0] = '0011 0001' (0x31)<br>Third write: SUCC1.CMD[3:0] |
| 8:15 | TMK | W | R | 0 | Test Mode Key<br>To write bit TEST1.WRTEN, the write operation has to be directly preceded by two consecutive<br>write accesses to the Test Mode Key (unlock sequence). If the write sequence below is<br>interrupted by other write accesses between the second write to the Test Mode Key and the write<br>access to the TEST1 register, TEST1.WRTEN is not set to '1' and the sequence has to be<br>repeated.<br>First write: LCK.TMK[7:0] = '0111 0101' (0x75)<br>Second write: LCK.TMK[7:0] = '1000 1010' (0x8A)<br>Third write: TEST1.WRTEN = '1' |

### 15.1.6 FLEXRAY_EIR

**Description:** Error Interrupt Register
**Address:** 0x40560020
**Offset:** 0x20
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | RFO [7:7] | PERR [6:6] | CCL [5:5] | CCF [4:4] | SFO [3:3] | SFBM [2:2] | CNA [1:1] | PEMC [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:12] | | | | MHF [11:11] | IOBA [10:10] | IIBA [9:9] | EFA [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:19] | | | | | TABA [18:18] | LTVA [17:17] | EDA [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:27] | | | | | TABB [26:26] | LTVB [25:25] | EDB [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | PEMC | RW1C | RW | 0 | POC Error Mode Changed<br>This flag is set whenever the error mode signalled by CCEV.ERRM[1:0] has changed.<br>1 = Error mode has changed<br>0 = Error mode has not changed |
| | POC_ERR_MODE_UNCHANGED | | | 0 | N/A |
| | POC_ERR_MODE_CHANGED | | | 1 | N/A |
| 1 | CNA | RW1C | RW | 0 | Command Not Accepted<br>The flag signals that the write access to the CHI command vector SUCC1.CMD[3:0] was not successful because the requested command was not valid in the actual POC state, or because the CHI command was locked (CCL = '1').<br>1 = CHI command not accepted<br>0 = CHI command accepted |
| | CHI_CMD_ACCEPTED | | | 0 | N/A |
| | CHI_CMD_NOT_ACCEPTED | | | 1 | N/A |
| 2 | SFBM | RW1C | RW | 0 | Sync Frames Below Minimum<br>This flag signals that the number of sync frames received during the last communication cycle was below the limit required by the FlexRay protocol. May be set during startup and therefore should be cleared by the Host after the CC entered NORMAL_ACTIVE state.<br>1 = Less than the required minimum of sync frames received<br>0 = Sync node: 1 or more sync frames received, non-sync node: 2 or more sync frames received |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| | SYNC_FRAMES_NOT_BELOW_MIN | | | 0 | N/A |
| | SYNC_FRAMES_BELOW_MIN | | | 1 | N/A |
| 3 | SFO | RW1C | RW | 0 | Sync Frame Overflow<br>Set when either the number of sync frames received during the last communication cycle or the total number of different sync frame IDs received during the last double cycle exceeds the maximum number of sync frames as defined by GTUC2.SNM[3:0].<br>1 = More sync frames received than configured by GTUC2.SNM[3:0]<br>0 = Number of received sync frames <= GTUC2.SNM[3:0] |
| | NO_SYNC_FRAME_OVERFLOW | | | 0 | N/A |
| | SYNC_FRAME_OVERFLOW | | | 1 | N/A |
| 4 | CCF | RW1C | RW | 0 | Clock Correction Failure<br>This flag is set at the end of the cycle whenever one of the following errors occurred:<br>Missing offset and / or rate correction<br>Clock correction limit reached<br>The clock correction status is monitored in registers CCEV and SFS. A failure may occur during startup, therefore bit CCF should be cleared by the Host after the CC entered NORMAL_ACTIVE state.<br>1 = Clock correction failed<br>0 = No clock correction error |
| | NO_CLK_CORRECTION_ERR | | | 0 | N/A |
| | CLK_CORRECTION_ERR | | | 1 | N/A |
| 5 | CCL | RW1C | RW | 0 | CHI Command Locked<br>The flag signals that the write access to the CHI command vector SUCC1.CMD[3:0] was not successful because the execution of the previous CHI command has not yet completed. In this case bit CNA is also set to '1'.<br>1 = CHI command not accepted<br>0 = CHI command accepted |
| | CHI_CMD_ACCEPTED | | | 0 | N/A |
| | CHI_CMD_NOT_ACCEPTED | | | 1 | N/A |
| 6 | PERR | RW1C | RW | 0 | Parity Error<br>The flag signals a parity error to the Host. It is set whenever one of the flags MHDS.PIBF, MHDS.POBF, MHDS.PMR, MHDS.PTBF1, MHDS.PTBF2 changes from '0' to '1'.<br>1 = Parity error detected<br>0 = No parity error detected |
| | NO_PARITY_ERR | | | 0 | N/A |
| | PARITY_ERR | | | 1 | N/A |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 7 | RFO | RW1C | RW | 0 | Receive FIFO Overrun<br>The flag is set by the CC when a receive FIFO overrun is detected. When a receive FIFO overrun occurs, the oldest message is overwritten with the actual received message. The actual state of the FIFO is monitored in register FSR.<br>1 = A receive FIFO overrun has been detected<br>0 = No receive FIFO overrun detected |
| | NO_RECEIVE_FIFO_OVERRUN | | | 0 | N/A |
| | RECEIVE_FIFO_OVERRUN | | | 1 | N/A |
| 8 | EFA | RW1C | RW | 0 | Empty FIFO Access<br>This flag is set by the CC when the Host requests the transfer of a message from the receive FIFO via Output Buffer while the receive FIFO is empty.<br>1 = Host access to empty FIFO occurred<br>0 = No Host access to empty FIFO occurred |
| | NO_EMPTY_FIFO_ACCESS | | | 0 | N/A |
| | EMPTY_FIFO_ACCESS | | | 1 | N/A |
| 9 | IIBA | RW1C | RW | 0 | Illegal Input Buffer Access<br>This flag is set by the CC when the Host wants to modify a message buffer via Input Buffer and one of the following conditions applies:<br>1) The CC is not in CONFIG or DEFAULT_CONFIG state and the Host writes to the Input Buffer Command Request register to modify the Header section of message buffer 0, 1 if configured for transmission in key slot<br>Header section of static message buffers with buffer number < MRC.FDB[7:0] while MRC.SEC[1:0] = '01'<br>Header section of any static or dynamic message buffer while MRC.SEC[1:0] = '1x'<br>Header and / or data section of any message buffer belonging to the receive FIFO<br>2) The Host writes to any register of the Input Buffer while IBCR.IBSYH is set to '1'.<br>1 = Illegal Host access to Input Buffer occurred<br>0 = No illegal Host access to Input Buffer occurred |
| | NO_ILLEGAL_IBF_ACCESS | | | 0 | N/A |
| | ILLEGAL_IBF_ACCESS | | | 1 | N/A |
| 10 | IOBA | RW1C | RW | 0 | Illegal Output buffer Access<br>This flag is set by the CC when the Host requests the transfer of a message buffer from the Message RAM to the Output Buffer while OBCR.OBSYS is set to '1'.<br>1 = Illegal Host access to Output Buffer occurred<br>0 = No illegal Host access to Output Buffer occurred |
| | NO_ILLEGAL_OBF_ACCESS | | | 0 | N/A |
| | ILLEGAL_OBF_ACCESS | | | 1 | N/A |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 11 | MHF | RW1C | RW | 0 | Message Handler Constraints Flag<br>The flag signals a Message Handler constraints violation condition. It is set whenever one of the flags MHDF.SNUA, MHDF.SNUB, MHDF.FNFA, MHDF.FNFB, MHDF.TBFA,<br>MHDF.TBFB, MHDF.WAHP changes from '0' to '1'.<br>1 = Message Handler failure detected<br>0 = No Message Handler failure detected |
| | NO_MSG_HANDLER_FAIL_DETECT | | | 0 | N/A |
| | MSG_HANDLER_FAIL_DETECT | | | 1 | N/A |
| 16 | EDA | RW1C | RW | 0 | Error Detected on Channel A<br>This bit is set whenever one of the flags ACS.SEDA, ACS.CEDA, ACS.CIA, ACS.SBVA<br>changes from '0' to '1'.<br>1 = Error detected on channel A<br>0 = No error detected on channel A |
| | NO_CH_A_ERR_DETECTED | | | 0 | N/A |
| | CH_A_ERR_DETECTED | | | 1 | N/A |
| 17 | LTVA | RW1C | RW | 0 | Latest Transmit Violation Channel A<br>The flag signals a latest transmit violation on channel A to the Host.<br>1 = Latest transmit violation detected on channel A<br>0 = No latest transmit violation detected on channel A |
| | NO_CH_A_LATEST_TX_VIOLATION_DETECTED | | | 0 | N/A |
| | CH_A_LATEST_TX_VIOLATION_DETECTED | | | 1 | N/A |
| 18 | TABA | RW1C | RW | 0 | Transmission Across Boundary Channel A<br>The flag signals to the Host that a transmission across a slot boundary occurred for channel A.<br>1 = Transmission across slot boundary detected on channel A<br>0 = No transmission across slot boundary detected on channel A |
| | NO_CH_A_TX_ACROSS_SLOT_BOUND_DETECTED | | | 0 | N/A |
| | CH_A_TX_ACROSS_SLOT_BOUND_DETECTED | | | 1 | N/A |
| 24 | EDB | RW1C | RW | 0 | Error Detected on Channel B<br>This bit is set whenever one of the flags ACS.SEDB, ACS.CEDB, ACS.CIB, ACS.SBVB<br>changes from '0' to '1'.<br>1 = Error detected on channel B<br>0 = No error detected on channel B |
| | NO_CH_B_ERR_DETECTED | | | 0 | N/A |
| | CH_B_ERR_DETECTED | | | 1 | N/A |
| 25 | LTVB | RW1C | RW | 0 | Latest Transmit Violation Channel B<br>The flag signals a latest transmit violation on channel B to the Host.<br>1 = Latest transmit violation detected on channel B<br>0 = No latest transmit violation detected on channel B |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| | NO_CH_B_LATEST_TX_VIOLATION_DETECTED | | | 0 | N/A |
| | CH_B_LATEST_TX_VIOLATION_DETECTED | | | 1 | N/A |
| 26 | TABB | RW1C | RW | 0 | Transmission Across Boundary Channel B<br>The flag signals to the Host that a transmission across a slot boundary occurred for channel B.<br>1 = Transmission across slot boundary detected on channel B<br>0 = No transmission across slot boundary detected on channel B |
| | NO_CH_B_TX_ACROSS_SLOT_BOUND_DETECTED | | | 0 | N/A |
| | CH_B_TX_ACROSS_SLOT_BOUND_DETECTED | | | 1 | N/A |

### 15.1.7 FLEXRAY_SIR

**Description:** Status Interrupt Register
**Address:** 0x40560024
**Offset:** 0x24
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | NMVC [7:7] | RFCL [6:6] | RFNE [5:5] | RXI [4:4] | TXI [3:3] | CYCS [2:2] | CAS [1:1] | WST [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | SDS [15:15] | MBSI [14:14] | SUCS [13:13] | SWE [12:12] | TOBC [11:11] | TIBC [10:10] | TI1 [9:9] | TI0 [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:18] | | | | | | MTSA [17:17] | WUPA [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:26] | | | | | | MTSB [25:25] | WUPB [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | WST | RW1C | RW | 0 | Wakeup Status<br>This flag is set when CCSV.WSV[2:0] changes to a value other than UNDEFINED.<br>1 = Wakeup status changed<br>0 = Wakeup status unchanged |
| | WAKEUP_STATUS_UNCHANGED | | | 0 | N/A |
| | WAKEUP_STATUS_CHANGED | | | 1 | N/A |
| 1 | CAS | RW1C | RW | 0 | Collision Avoidance Symbol<br>This flag is set by the CC during STARTUP state when a CAS or a potential CAS was received.<br>1 = Bit pattern matching the CAS symbol received<br>0 = No bit pattern matching the CAS symbol received |
| | NO_CAS_BIT_PATTERN_MATCH | | | 0 | N/A |
| | CAS_BIT_PATTERN_MATCH | | | 1 | N/A |
| 2 | CYCS | RW1C | RW | 0 | Cycle Start Interrupt<br>This flag is set by the CC when a communication cycle starts.<br>1 = Communication cycle started<br>0 = No communication cycle started |
| | NO_COMM_CYCLE_STARTED | | | 0 | N/A |
| | COMM_CYCLE_STARTED | | | 1 | N/A |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 3 | TXI | RW1C | RW | 0 | Transmit Interrupt<br>This flag is set by the CC at the end of frame transmission if bit MBI in the respective message buffer is set to '1' (see Table 17).<br>1 = At least one frame was transmitted from a transmit buffer with MBI = '1'<br>0 = No frame transmitted from a transmit buffer with MBI = '1' |
| | NO_FRAME_TXED_FROM_TX_MBI_BUFF | | | 0 | N/A |
| | FRAME_TXED_FROM_TX_MBI_BUFF | | | 1 | N/A |
| 4 | RXI | RW1C | RW | 0 | Receive Interrupt<br>This flag is set by the CC whenever the set condition of a message buffers ND flag is fulfilled<br>see 4.8.6 New Data 1/2/3/4 (NDAT1/2/3/4)), and if bit MBI of that message buffer is set to '1'<br>see Table 17).<br>1 = At least one ND flag of a receive buffer with MBI = '1' has been set to '1'<br>0 = No ND flag of a receive buffer with MBI = '1' has been set to '1' |
| | NO_ND_FLAG_OF_RX_MBI_BUFF_SET | | | 0 | N/A |
| | ND_FLAG_OF_RX_MBI_BUFF_SET | | | 1 | N/A |
| 5 | RFNE | RW1C | RW | 0 | Receive FIFO Not Empty<br>This flag is set by the CC when a received valid frame was stored into the empty receive FIFO.<br>The actual state of the receive FIFO is monitored in register FSR.<br>1 = Receive FIFO is not empty<br>0 = Receive FIFO is empty |
| | RX_FIFO_EMPTY | | | 0 | N/A |
| | RX_FIFO_NOT_EMPTY | | | 1 | N/A |
| 6 | RFCL | RW1C | RW | 0 | Receive FIFO Critical Level<br>This flag is set when the receive FIFO fill level FSR.RFFL[7:0] is equal or greater than the critical level as configured by FCL.CL[7:0].<br>1 = Receive FIFO critical level reached<br>0 = Receive FIFO below critical level |
| | RX_FIFO_BELOW_CRITICAL_LEVEL | | | 0 | N/A |
| | RX_FIFO_NOT_BELOW_CRITICAL_LEVEL | | | 1 | N/A |
| 7 | NMVC | RW1C | RW | 0 | Network Management Vector Changed<br>This interrupt flag signals a change in the Network Management Vector visible to the Host.<br>1 = Network management vector changed<br>0 = No change in the network management vector |
| | NTWK_MGMT_VECTOR_UNCHANGED | | | 0 | N/A |
| | NTWK_MGMT_VECTOR_CHANGED | | | 1 | N/A |
| 8 | TI0 | RW1C | RW | 0 | Timer Interrupt 0<br>This flag is set whenever timer 0 matches the conditions configured in register T0C. A Timer Interrupt 0 is also signalled on pin eray_tint0.<br>1 = Timer Interrupt 0 occurred<br>0 = No Timer Interrupt 0 |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| | NO_TIMER_INTERRUPT_0 | | | 0 | N/A |
| | TIMER_INTERRUPT_0_OCCURED | | | 1 | N/A |
| 9 | TI1 | RW1C | RW | 0 | Timer Interrupt 1<br>This flag is set whenever timer 1 matches the conditions configured in register T1C. A Timer Interrupt 1 is also signalled on pin eray_tint1.<br>1 = Timer Interrupt 1 occurred<br>0 = No Timer Interrupt 1 |
| | NO_TIMER_INTERRUPT_1 | | | 0 | N/A |
| | TIMER_INTERRUPT_1_OCCURED | | | 1 | N/A |
| 10 | TIBC | RW1C | RW | 0 | Transfer Input Buffer Completed<br>This flag is set whenever a transfer from Input Buffer to the Message RAM has completed and IBCR.IBSYS has been reset by the Message Handler.<br>1 = Transfer between Input Buffer and Message RAM completed<br>0 = No transfer completed |
| | NO_TRANSFER_COMPLETED | | | 0 | N/A |
| | IBF_TO_MSGRAM_TRANSFER_COMPLETED | | | 1 | N/A |
| 11 | TOBC | RW1C | RW | 0 | Transfer Output Buffer Completed<br>This flag is set whenever a transfer from the Message RAM to the Output Buffer has completed and OBCR.OBSYS has been reset by the Message Handler.<br>1 = Transfer between Message RAM and Output Buffer completed<br>0 = No transfer completed |
| | NO_TRANSFER_COMPLETED | | | 0 | N/A |
| | MSGRAM_TO_OBF_TRANSFER_COMPLETED | | | 1 | N/A |
| 12 | SWE | RW1C | RW | 0 | Stop Watch Event<br>This flag is set after a stop watch activation when the actual cycle counter and macrotick value are stored in the Stop Watch register (see [01]Section 4.4.10 Stop Watch Register 1 (STPW1)).<br>1 = Stop Watch Event occurred<br>0 = No Stop Watch Event |
| | NO_STOP_WATCH_EVENT | | | 0 | N/A |
| | STOP_WATCH_EVENT_OCCURRED | | | 1 | N/A |
| 13 | SUCS | RW1C | RW | 0 | Startup Completed Successfully<br>This flag is set whenever a startup completed successfully and the CC entered NORMAL_ACTIVE state.<br>1 = Startup completed successfully<br>0 = No startup completed successfully |
| | NO_STARTUP_COMPLETED | | | 0 | N/A |
| | STARTUP_COMPLETED | | | 1 | N/A |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 14 | MBSI | RW1C | RW | 0 | Message Buffer Status Interrupt<br>This flag is set by the CC when the message buffer status MBS has changed and if bit MBI of that message buffer is set (see Table 17).<br>1 = Message buffer status of at least one message buffer with MBI = '1' has changed<br>0 = No message buffer status change of message buffer with MBI = '1' |
| | NO_MSG_BUFF_STATUS_CHANGED | | | 0 | N/A |
| | MSG_BUFF_STATUS_CHANGED | | | 1 | N/A |
| 15 | SDS | RW1C | RW | 0 | Start of Dynamic Segment<br>This flag is set by the CC when the dynamic segment starts.<br>1 = Dynamic segment started<br>0 = Dynamic segment not yet started |
| | DYNAMIC_SEGMENT_NOT_STARTED | | | 0 | N/A |
| | DYNAMIC_SEGMENT_STARTED | | | 1 | N/A |
| 16 | WUPA | RW1C | RW | 0 | Wakeup Pattern Channel A<br>This flag is set by the CC when a wakeup pattern was received on channel A. Only set when the CC is in WAKEUP, READY, or STARTUP state, or when in Monitor mode.<br>1 = Wakeup pattern received on channel A<br>0 = No wakeup pattern received on channel A |
| | NO_WAKEUP_PATTERN_RXD_ON_CH_A | | | 0 | N/A |
| | WAKEUP_PATTERN_RXD_ON_CH_A | | | 1 | N/A |
| 17 | MTSA | RW1C | RW | 0 | MTS Received on Channel A (vSS!ValidMTSA)<br>Media Access Test symbol received on channel A during the preceding symbol window.<br>Updated by the CC for each channel at the end of the symbol window.<br>1 = MTS symbol received on channel A<br>0 = No MTS symbol received on channel A |
| | NO_MTS_SYMBOL_RXD_ON_CH_A | | | 0 | N/A |
| | MTS_SYMBOL_RXD_ON_CH_A | | | 1 | N/A |
| 24 | WUPB | RW1C | RW | 0 | Wakeup Pattern Channel B<br>This flag is set by the CC when a wakeup pattern was received on channel B. Only set when the CC is in WAKEUP, READY, or STARTUP state, or when in Monitor mode.<br>1 = Wakeup pattern received on channel B<br>0 = No wakeup pattern received on channel B |
| | NO_WAKEUP_PATTERN_RXD_ON_CH_B | | | 0 | N/A |
| | WAKEUP_PATTERN_RXD_ON_CH_B | | | 1 | N/A |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 25 | MTSB | RW1C | RW | 0 | MTS Received on Channel B (vSS!ValidMTSB)<br>Media Access Test symbol received on channel B during the preceding symbol window.<br>Updated by the CC for each channel at the end of the symbol window.<br>1 = MTS symbol received on channel B<br>0 = No MTS symbol received on channel B |
| | NO_MTS_SYMBOL_RXD_ON_CH_B | | | 0 | N/A |
| | MTS_SYMBOL_RXD_ON_CH_B | | | 1 | N/A |

### 15.1.8 FLEXRAY_EILS

**Description:** Error Interrupt Line Select
**Address:** 0x40560028
**Offset:** 0x28
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** The Error Interrupt Line Select register assigns an interrupt generated by a specific error interrupt flag
from register EIR to one of the two module interrupt lines:
1 = Interrupt assigned to interrupt line eray_int1
0 = Interrupt assigned to interrupt line eray_int0
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | RFOL [7:7] | PERRL [6:6] | CCLL [5:5] | CCFL [4:4] | SFOL [3:3] | SFBML [2:2] | CNAL [1:1] | PEMCL [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:12] | | | | MHFL [11:11] | IOBAL [10:10] | IIBAL [9:9] | EFAL [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:19] | | | | | TABAL [18:18] | LTVAL [17:17] | EDAL [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:27] | | | | | TABBL [26:26] | LTVBL [25:25] | EDBL [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | PEMCL | RW | R | 0 | POC Error Mode Changed Interrupt Line |
| 1 | CNAL | RW | R | 0 | Command Not Accepted Interrupt Line |
| 2 | SFBML | RW | R | 0 | Sync Frames Below Minimum Interrupt Line |
| 3 | SFOL | RW | R | 0 | Sync Frame Overflow Interrupt Line |
| 4 | CCFL | RW | R | 0 | Clock Correction Failure Interrupt Line |
| 5 | CCLL | RW | R | 0 | CHI Command Locked Interrupt Line |
| 6 | PERRL | RW | R | 0 | Parity Error Interrupt Line |
| 7 | RFOL | RW | R | 0 | Receive FIFO Overrun Interrupt Line |
| 8 | EFAL | RW | R | 0 | Empty FIFO Access Interrupt Line |
| 9 | IIBAL | RW | R | 0 | Illegal Input Buffer Access Interrupt Line |
| 10 | IOBAL | RW | R | 0 | Illegal Output Buffer Access Interrupt Line |
| 11 | MHFL | RW | R | 0 | Message Handler Constraints Flag Interrupt Line |
| 16 | EDAL | RW | R | 0 | Error Detected on Channel A Interrupt Line |
| 17 | LTVAL | RW | R | 0 | Latest Transmit Violation Channel A Interrupt Line |
| 18 | TABAL | RW | R | 0 | Transmission Across Boundary Channel A Interrupt Line |
| 24 | EDBL | RW | R | 0 | Error Detected on Channel B Interrupt Line |
| 25 | LTVBL | RW | R | 0 | Latest Transmit Violation Channel B Interrupt Line |
| 26 | TABBL | RW | R | 0 | Transmission Across Boundary Channel B Interrupt Line |

### 15.1.9 FLEXRAY_SILS

**Description:** Status Interrupt Line Select
**Address:** 0x4056002C
**Offset:** 0x2C
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** The Error Interrupt Line Select register assigns an interrupt generated by a specific error interrupt flag
from register EIR to one of the two module interrupt lines:
1 = Interrupt assigned to interrupt line eray_int1
0 = Interrupt assigned to interrupt line eray_int0
**Default:** 0x303FFFF

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | NMVCL [7:7] | RFCLL [6:6] | RFNEL [5:5] | RXIL [4:4] | TXIL [3:3] | CYCSL [2:2] | CASL [1:1] | WSTL [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | SDSL [15:15] | MBSIL [14:14] | SUCSL [13:13] | SWEL [12:12] | TOBCL [11:11] | TIBCL [10:10] | TI1L [9:9] | TI0L [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:18] | | | | | | MTSAL [17:17] | WUPAL [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:26] | | | | | | MTSBL [25:25] | WUPBL [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | WSTL | RW | R | 1 | Wakeup Status Interrupt Line |
| 1 | CASL | RW | R | 1 | Collision Avoidance Symbol Interrupt Line |
| 2 | CYCSL | RW | R | 1 | Cycle Start Interrupt Line |
| 3 | TXIL | RW | R | 1 | Transmit Interrupt Line |
| 4 | RXIL | RW | R | 1 | Receive Interrupt Line |
| 5 | RFNEL | RW | R | 1 | Receive FIFO Not Empty Interrupt Line |
| 6 | RFCLL | RW | R | 1 | Receive FIFO Critical Level Interrupt Line |
| 7 | NMVCL | RW | R | 1 | Network Management Vector Changed Interrupt Line |
| 8 | TI0L | RW | R | 1 | Timer Interrupt 0 Line |
| 9 | TI1L | RW | R | 1 | Timer Interrupt 1 Line |
| 10 | TIBCL | RW | R | 1 | Transfer Input Buffer Completed Interrupt Line |
| 11 | TOBCL | RW | R | 1 | Transfer Output Buffer Completed Interrupt Line |
| 12 | SWEL | RW | R | 1 | Stop Watch Event Interrupt Line |
| 13 | SUCSL | RW | R | 1 | Startup Completed Successfully Interrupt Line |
| 14 | MBSIL | RW | R | 1 | Message Buffer Status Interrupt Line |
| 15 | SDSL | RW | R | 1 | Start of Dynamic Segment Interrupt Line |
| 16 | WUPAL | RW | R | 1 | Wakeup Pattern Channel A Interrupt Line |
| 17 | MTSAL | RW | R | 1 | Media Access Test Symbol Channel A Interrupt Line |
| 24 | WUPBL | RW | R | 1 | Wakeup Pattern Channel B Interrupt Line |
| 25 | MTSBL | RW | R | 1 | Media Access Test Symbol Channel B Interrupt Line |

### 15.1.10 FLEXRAY_EIES

**Description:** Error Interrupt Enable Set
**Address:** 0x40560030
**Offset:** 0x30
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** Set
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | RFOE [7:7] | PERRE [6:6] | CCLE [5:5] | CCFE [4:4] | SFOE [3:3] | SFBME [2:2] | CNAE [1:1] | PEMCE [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:12] | | | | MHFE [11:11] | IOBAE [10:10] | IIBAE [9:9] | EFAE [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:19] | | | | | TABAE [18:18] | LTVAE [17:17] | EDAE [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:27] | | | | | TABBE [26:26] | LTVBE [25:25] | EDBE [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | PEMCE | RW1S | RW | 0 | POC Error Mode Changed Interrupt Enable |
| 1 | CNAE | RW1S | RW | 0 | Command Not Accepted Interrupt Enable |
| 2 | SFBME | RW1S | RW | 0 | Sync Frames Below Minimum Interrupt Enable |
| 3 | SFOE | RW1S | RW | 0 | Sync Frame Overflow Interrupt Enable |
| 4 | CCFE | RW1S | RW | 0 | Clock Correction Failure Interrupt Enable |
| 5 | CCLE | RW1S | RW | 0 | CHI Command Locked Interrupt Enable |
| 6 | PERRE | RW1S | RW | 0 | Parity Error Interrupt Enable |
| 7 | RFOE | RW1S | RW | 0 | Receive FIFO Overrun Interrupt Enable |
| 8 | EFAE | RW1S | RW | 0 | Empty FIFO Access Interrupt Enable |
| 9 | IIBAE | RW1S | RW | 0 | Illegal Input Buffer Access Interrupt Enable |
| 10 | IOBAE | RW1S | RW | 0 | Illegal Output Buffer Access Interrupt Enable |
| 11 | MHFE | RW1S | RW | 0 | Message Handler Constraints Flag Interrupt Enable |
| 16 | EDAE | RW1S | RW | 0 | Error Detected on Channel A Interrupt Enable |
| 17 | LTVAE | RW1S | RW | 0 | Latest Transmit Violation Channel A Interrupt Enable |
| 18 | TABAE | RW1S | RW | 0 | Transmission Across Boundary Channel A Interrupt Enable |
| 24 | EDBE | RW1S | RW | 0 | Error Detected on Channel B Interrupt Enable |
| 25 | LTVBE | RW1S | RW | 0 | Latest Transmit Violation Channel B Interrupt Enable |
| 26 | TABBE | RW1S | RW | 0 | Transmission Across Boundary Channel B Interrupt Enable |

### 15.1.11 FLEXRAY_EIER

**Description:** Error Interrupt Enable Reset
**Address:** 0x40560034
**Offset:** 0x34
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** Reset
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | RFOE [7:7] | PERRE [6:6] | CCLE [5:5] | CCFE [4:4] | SFOE [3:3] | SFBME [2:2] | CNAE [1:1] | PEMCE [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:12] | | | | MHFE [11:11] | IOBAE [10:10] | IIBAE [9:9] | EFAE [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:19] | | | | | TABAE [18:18] | LTVAE [17:17] | EDAE [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:27] | | | | | TABBE [26:26] | LTVBE [25:25] | EDBE [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | PEMCE | RW1C | RW | 0 | POC Error Mode Changed Interrupt Enable |
| 1 | CNAE | RW1C | RW | 0 | Command Not Accepted Interrupt Enable |
| 2 | SFBME | RW1C | RW | 0 | Sync Frames Below Minimum Interrupt Enable |
| 3 | SFOE | RW1C | RW | 0 | Sync Frame Overflow Interrupt Enable |
| 4 | CCFE | RW1C | RW | 0 | Clock Correction Failure Interrupt Enable |
| 5 | CCLE | RW1C | RW | 0 | CHI Command Locked Interrupt Enable |
| 6 | PERRE | RW1C | RW | 0 | Parity Error Interrupt Enable |
| 7 | RFOE | RW1C | RW | 0 | Receive FIFO Overrun Interrupt Enable |
| 8 | EFAE | RW1C | RW | 0 | Empty FIFO Access Interrupt Enable |
| 9 | IIBAE | RW1C | RW | 0 | Illegal Input Buffer Access Interrupt Enable |
| 10 | IOBAE | RW1C | RW | 0 | Illegal Output Buffer Access Interrupt Enable |
| 11 | MHFE | RW1C | RW | 0 | Message Handler Constraints Flag Interrupt Enable |
| 16 | EDAE | RW1C | RW | 0 | Error Detected on Channel A Interrupt Enable |
| 17 | LTVAE | RW1C | RW | 0 | Latest Transmit Violation Channel A Interrupt Enable |
| 18 | TABAE | RW1C | RW | 0 | Transmission Across Boundary Channel A Interrupt Enable |
| 24 | EDBE | RW1C | RW | 0 | Error Detected on Channel B Interrupt Enable |
| 25 | LTVBE | RW1C | RW | 0 | Latest Transmit Violation Channel B Interrupt Enable |
| 26 | TABBE | RW1C | RW | 0 | Transmission Across Boundary Channel B Interrupt Enable |

### 15.1.12 FLEXRAY_SIES

**Description:** Status Interrupt Enable Set
**Address:** 0x40560038
**Offset:** 0x38
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** Set
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | NMVCE [7:7] | RFCLE [6:6] | RFNEE [5:5] | RXIE [4:4] | TXIE [3:3] | CYCSE [2:2] | CASE [1:1] | WSTE [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | SDSE [15:15] | MBSIE [14:14] | SUCSE [13:13] | SWEE [12:12] | TOBCE [11:11] | TIBCE [10:10] | TI1E [9:9] | TI0E [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:18] | | | | | | MTSAE [17:17] | WUPAE [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:26] | | | | | | MTSBE [25:25] | WUPBE [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | WSTE | RW1S | RW | 0 | Wakeup Status Interrupt Enable |
| 1 | CASE | RW1S | RW | 0 | Collision Avoidance Symbol Interrupt Enable |
| 2 | CYCSE | RW1S | RW | 0 | Cycle Start Interrupt Enable |
| 3 | TXIE | RW1S | RW | 0 | Transmit Interrupt Enable |
| 4 | RXIE | RW1S | RW | 0 | Receive Interrupt Enable |
| 5 | RFNEE | RW1S | RW | 0 | Receive FIFO Not Empty Interrupt Enable |
| 6 | RFCLE | RW1S | RW | 0 | Receive FIFO Critical Level Interrupt Enable |
| 7 | NMVCE | RW1S | RW | 0 | Network Management Vector Changed Interrupt Enable |
| 8 | TI0E | RW1S | RW | 0 | Timer Interrupt 0 Enable |
| 9 | TI1E | RW1S | RW | 0 | Timer Interrupt 1 Enable |
| 10 | TIBCE | RW1S | RW | 0 | Transfer Input Buffer Completed Interrupt Enable |
| 11 | TOBCE | RW1S | RW | 0 | Transfer Output Buffer Completed Interrupt Enable |
| 12 | SWEE | RW1S | RW | 0 | Stop Watch Event Interrupt Enable |
| 13 | SUCSE | RW1S | RW | 0 | Startup Completed Successfully Interrupt Enable |
| 14 | MBSIE | RW1S | RW | 0 | Message Buffer Status Interrupt Enable |
| 15 | SDSE | RW1S | RW | 0 | Start of Dynamic Segment Interrupt Enable |
| 16 | WUPAE | RW1S | RW | 0 | Wakeup Pattern Channel A Interrupt Enable |
| 17 | MTSAE | RW1S | RW | 0 | MTS Received on Channel A Interrupt Enable |
| 24 | WUPBE | RW1S | RW | 0 | Wakeup Pattern Channel B Interrupt Enable |
| 25 | MTSBE | RW1S | RW | 0 | MTS Received on Channel B Interrupt Enable |

### 15.1.13 FLEXRAY_SIER

**Description:** Status Interrupt Enable Reset
**Address:** 0x4056003C
**Offset:** 0x3C
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** Reset
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | NMVCE [7:7] | RFCLE [6:6] | RFNEE [5:5] | RXIE [4:4] | TXIE [3:3] | CYCSE [2:2] | CASE [1:1] | WSTE [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | SDSE [15:15] | MBSIE [14:14] | SUCSE [13:13] | SWEE [12:12] | TOBCE [11:11] | TIBCE [10:10] | TI1E [9:9] | TI0E [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:18] | | | | | | MTSAE [17:17] | WUPAE [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:26] | | | | | | MTSBE [25:25] | WUPBE [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | WSTE | RW1C | RW | 0 | Wakeup Status Interrupt Enable |
| 1 | CASE | RW1C | RW | 0 | Collision Avoidance Symbol Interrupt Enable |
| 2 | CYCSE | RW1C | RW | 0 | Cycle Start Interrupt Enable |
| 3 | TXIE | RW1C | RW | 0 | Transmit Interrupt Enable |
| 4 | RXIE | RW1C | RW | 0 | Receive Interrupt Enable |
| 5 | RFNEE | RW1C | RW | 0 | Receive FIFO Not Empty Interrupt Enable |
| 6 | RFCLE | RW1C | RW | 0 | Receive FIFO Critical Level Interrupt Enable |
| 7 | NMVCE | RW1C | RW | 0 | Network Management Vector Changed Interrupt Enable |
| 8 | TI0E | RW1C | RW | 0 | Timer Interrupt 0 Enable |
| 9 | TI1E | RW1C | RW | 0 | Timer Interrupt 1 Enable |
| 10 | TIBCE | RW1C | RW | 0 | Transfer Input Buffer Completed Interrupt Enable |
| 11 | TOBCE | RW1C | RW | 0 | Transfer Output Buffer Completed Interrupt Enable |
| 12 | SWEE | RW1C | RW | 0 | Stop Watch Event Interrupt Enable |
| 13 | SUCSE | RW1C | RW | 0 | Startup Completed Successfully Interrupt Enable |
| 14 | MBSIE | RW1C | RW | 0 | Message Buffer Status Interrupt Enable |
| 15 | SDSE | RW1C | RW | 0 | Start of Dynamic Segment Interrupt Enable |
| 16 | WUPAE | RW1C | RW | 0 | Wakeup Pattern Channel A Interrupt Enable |
| 17 | MTSAE | RW1C | RW | 0 | MTS Received on Channel A Interrupt Enable |
| 24 | WUPBE | RW1C | RW | 0 | Wakeup Pattern Channel B Interrupt Enable |
| 25 | MTSBE | RW1C | RW | 0 | MTS Received on Channel B Interrupt Enable |

### 15.1.14 FLEXRAY_ILE

**Description:** Interrupt Line Enable
**Address:** 0x40560040
**Offset:** 0x40
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:2] | | | | | | EINT1_ [1:1] | EINT0_ [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | EINT0_ | RW | R | 0 | Enable Interrupt Line 0<br>1 = Interrupt line eray_int0 enabled<br>0 = Interrupt line eray_int0 disabled |
| | ERAY_INT0_DISABLED | | | 0 | N/A |
| | ERAY_INT0_ENABLED | | | 1 | N/A |
| 1 | EINT1_ | RW | R | 0 | Enable Interrupt Line 1<br>1 = Interrupt line eray_int1 enabled<br>0 = Interrupt line eray_int1 disabled |
| | ERAY_INT1_DISABLED | | | 0 | N/A |
| | ERAY_INT1_ENABLED | | | 1 | N/A |

### 15.1.15 FLEXRAY_T0C

**Description:** Timer 0 Configuration
**Address:** 0x40560044
**Offset:** 0x44
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:2] | | | | | | T0MS [1:1] | T0RC [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:15] | T0CC [14:8] | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | T0MO [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:30] | | T0MO [29:24] | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | T0RC | RW | R | 0 | Timer 0 Run Control<br>1 = Timer 0 running<br>0 = Timer 0 halted |
| | TIMER_0_HALTED | | | 0 | N/A |
| | TIMER_0_RUNNING | | | 1 | N/A |
| 1 | T0MS | RW | R | 0 | Timer 0 Mode Select<br>1 = Continuous mode<br>0 = Single-shot mode |
| | TIMER_0_SINGLE_SHOT_MODE | | | 0 | N/A |
| | TIMER_0_CONTINUOUS_MODE | | | 1 | N/A |
| 8:14 | T0CC | RW | R | 0 | Timer 0 Cycle Code<br>The 7-bit timer 0 cycle code determines the cycle set used for generation of the timer 0 interrupt.<br>For details about the configuration of the cycle code see [01]Section 5.7.2 Cycle Counter Filtering. |
| 16:29 | T0MO | RW | R | 0 | Timer 0 Macrotick Offset<br>Configures the macrotick offset from the beginning of the cycle where the interrupt is to occur.<br>The Timer 0 Interrupt occurs at this offset for each cycle of the cycle set. |

### 15.1.16 FLEXRAY_T1C

**Description:** Timer 1 Configuration
**Address:** 0x40560048
**Offset:** 0x48
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x20000

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:2] | | | | | | T1MS [1:1] | T1RC [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | T1MC [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:30] | | T1MC [29:24] | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | T1RC | RW | R | 0 | Timer 1 Run Control<br>1 = Timer 1 running<br>0 = Timer 1 halted |
| | TIMER_1_HALTED | | | 0 | N/A |
| | TIMER_1_RUNNING | | | 1 | N/A |
| 1 | T1MS | RW | R | 0 | Timer 1 Mode Select<br>1 = Continuous mode<br>0 = Single-shot mode |
| | TIMER_1_SINGLE_SHOT_MODE | | | 0 | N/A |
| | TIMER_1_CONTINUOUS_MODE | | | 1 | N/A |
| 16:29 | T1MC | RW | R | 2 | Timer 1 Macrotick Count<br>When the configured macrotick count is reached the timer 1 interrupt is generated.<br>Valid values are: 2 to 16383 MT in continuous mode<br>1 to 16383 MT in single-shot mode |
| | MIN | | | 1 | N/A |
| | MAX | | | 16383 | N/A |

### 15.1.17 FLEXRAY_STPW1

**Description:** Stop Watch Register 1
**Address:** 0x4056004C
**Offset:** 0x4C
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:7] | EINT1 [6:6] | EINT0 [5:5] | EETP [4:4] | SSWT [3:3] | EDGE [2:2] | SWMS [1:1] | ESWT [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:14] | | SCCV [13:8] | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | SMTV [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:30] | | SMTV [29:24] | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | ESWT | RW | R | 0 | Enable Stop Watch Trigger<br>If enabled an edge on input eray_stpwt or an interrupt 0,1 event (rising edge on pin eray_int0 or eray_int1) activates the stop watch. In single-shot mode this bit is reset to '0' after the actual cycle counter and macrotick value are stored in the Stop Watch register.<br>1 = Stop watch trigger enabled<br>0 = Stop watch trigger disabled |
| | STOP_WATCH_TRIGGER_DISABLED | | | 0 | N/A |
| | STOP_WATCH_TRIGGER_ENABLED | | | 1 | N/A |
| 1 | SWMS | RW | R | 0 | Stop Watch Mode Select<br>1 = Continuous mode<br>0 = Single-shot mode |
| | STOP_WATCH_SINGLE_SHOT_MODE | | | 0 | N/A |
| | STOP_WATCH_CONTINUOUS_MODE | | | 1 | N/A |
| 2 | EDGE | RW | R | 0 | Stop Watch Trigger Edge Select<br>1 = Rising edge<br>0 = Falling edge |
| | STOP_WATCH_FALLING_EDGE | | | 0 | N/A |
| | STOP_WATCH_RISING_EDGE | | | 1 | N/A |
| 3 | SSWT | RW | R | 0 | Software Stop Watch Trigger<br>When the Host writes this bit to '1' the stop watch is activated. After the actual cycle counter and macrotick value are stored in the Stop Watch register this bit is reset to '0'. The bit is only writeable while ESWT = '0'.<br>1 = Stop watch activated by software trigger<br>0 = Software trigger reset |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| | STOP_WATCH_SOFTWARE_TRIGGER_RESET | | | 0 | N/A |
| | STOP_WATCH_SOFTWARE_TRIGGER_ACTIVATED | | | 1 | N/A |
| 4 | EETP | RW | R | 0 | Enable External Trigger Pin<br>Enables stop watch trigger event via pin eray_stpwt if ESWT = '1'.<br>1 = Edge on pin eray_stpwt triggers stop watch<br>0 = Stop watch trigger via pin eray_stpwt disabled |
| | ESTPWT_DISABLED | | | 0 | N/A |
| | ESTPWT_ENABLED | | | 1 | N/A |
| 5 | EINT0 | RW | R | 0 | Enable Interrupt 0 Trigger<br>Enables stop watch trigger by interrupt 0 event if ESWT = '1'.<br>1 = Interrupt 0 event triggers stop watch<br>0 = Stop watch trigger by interrupt 0 disabled |
| | STPWT_TRIGGER_BY_INT0_DISABLED | | | 0 | N/A |
| | STPWT_TRIGGER_BY_INT0_ENABLED | | | 1 | N/A |
| 6 | EINT1 | RW | R | 0 | Enable Interrupt 1 Trigger<br>Enables stop watch trigger by interrupt 1event if ESWT = '1'.<br>1 = Interrupt 1 event triggers stop watch<br>0 = Stop watch trigger by interrupt 1 disabled |
| | STPWT_TRIGGER_BY_INT1_DISABLED | | | 0 | N/A |
| | STPWT_TRIGGER_BY_INT1_ENABLED | | | 1 | N/A |
| 8:13 | SCCV | R | RW | 0 | Stop Watch Captured Cycle Counter Value<br>State of the cycle counter when the stop watch event occurred. Valid values are 0 to 63. |
| 16:29 | SMTV | R | RW | 0 | Stop Watch Captured Macrotick Value<br>State of the macrotick counter when the stop watch event occurred. Valid values are 0 to 15999. |
| | MAX | | | 15999 | N/A |

### 15.1.18 FLEXRAY_STPW2

**Description:** Stop Watch Register 2
**Address:** 0x40560050
**Offset:** 0x50
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | SSCVA [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:11] | | | | | SSCVA [10:8] | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | SSCVB [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:27] | | | | | SSCVB [26:24] | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:10 | SSCVA | R | RW | 0 | Stop Watch Captured Slot Counter Value Channel A State of the slot counter for channel A when the stop watch event occurred. Valid values are 0 to 2047. |
| 16:26 | SSCVB | R | RW | 0 | Stop Watch Captured Slot Counter Value Channel B State of the slot counter for channel B when the stop watch event occurred. Valid values are 0 to 2047. |

### 15.1.19 FLEXRAY_SUCC1

**Description:** SUC Configuration Register 1
**Address:** 0x40560080
**Offset:** 0x80
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** Most bits except CMD are write protected, see LCK register
**Default:** 0xC401080

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | PBSY [7:7] | None [6:4] | | | CMD [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | CSA [15:11] | | | | | None [10:10] | TXSY [9:9] | TXST [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | HCSE [23:23] | TSM [22:22] | WUCS [21:21] | PTA [20:16] | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:28] | | | | CCHB [27:27] | CCHA [26:26] | MTSB_ [25:25] | MTSA_ [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | CMD | RW | RW | 0 | CHI Command Vector<br>The Host may write any CHI command at any time, but certain commands are enabled only in certain POC states. If a command is not enabled, it will not be executed, the CHI command vector CMD[3:0] will be reset to '0000' = command_not_accepted, and flag EIR.CNA will be set to '1'. In case the previous CHI command has not yet completed, EIR.CCL is set to '1' together with EIR.CNA; the CHI command needs to be repeated. Except for HALT state, a POC state change command applied while the CC is already in the requested POC state neither causes a state change nor will EIR.CNA be set.<br>0000 = command_not_accepted<br>0001 = CONFIG<br>0010 = READY<br>0011 = WAKEUP<br>0100 = RUN<br>0101 = ALL_SLOTS<br>0110 = HALT<br>0111 = FREEZE<br>1000 = SEND_MTS<br>1001 = ALLOW_COLDSTART<br>1010 = RESET_STATUS_INDICATORS<br>1011 = MONITOR_MODE<br>1100 = CLEAR_RAMS<br>1101 = reserved<br>1110 = reserved<br>1111 = reserved |
| | CMD_NOT_ACCEPTED | | | 0 | N/A |
| | CONFIG | | | 1 | N/A |
| | READY | | | 2 | N/A |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| | WAKEUP | | | 3 | N/A |
| | RUN | | | 4 | N/A |
| | ALL_SLOTS | | | 5 | N/A |
| | HALT | | | 6 | N/A |
| | FREEZE | | | 7 | N/A |
| | SEND_MTS | | | 8 | N/A |
| | ALLOW_COLDSTART | | | 9 | N/A |
| | RESET_STATUS_INDICATORS | | | 10 | N/A |
| | MONITOR_MODE | | | 11 | N/A |
| | CLEAR_RAMS | | | 12 | N/A |
| 7 | PBSY | R | RW | 1 | POC Busy<br>Signals that the POC is busy and cannot accept a command from the Host. CMD[3:0] is locked against write accesses. Set to '1' after hard reset during initialization of internal RAM blocks.<br>1 = POC is busy, CMD[3:0] locked<br>0 = POC not busy, CMD[3:0] writeable |
| | POC_NOT_BUSY | | | 0 | N/A |
| | POC_BUSY | | | 1 | N/A |
| 8 | TXST | RW | R | 0 | Transmit Startup Frame in Key Slot (pKeySlotUsedForStartup)<br>Defines whether the key slot is used to transmit startup frames. The bit can be modified in DEFAULT_CONFIG or CONFIG state only.<br>1 = Key slot used to transmit startup frame, node is leading or following coldstarter<br>0 = No startup frame transmission in key slot, node is non-coldstarter |
| | NO_STARTUP_FRAME_TXMN | | | 0 | N/A |
| | STARTUP_FRAME_TXMN | | | 1 | N/A |
| 9 | TXSY | RW | R | 0 | Transmit Sync Frame in Key Slot (pKeySlotUsedForSync)<br>Defines whether the key slot is used to transmit sync frames. The bit can be modified in DEFAULT_CONFIG or CONFIG state only.<br>1 = Key slot used to transmit sync frame, node is sync node<br>0 = No sync frame transmission in key slot, node is neither sync nor coldstart node |
| | NO_SYNC_FRAME_TXMN | | | 0 | N/A |
| | SYNC_FRAME_TXMN | | | 1 | N/A |
| 11:15 | CSA | RW | R | 2 | Cold Start Attempts (gColdStartAttempts)<br>Configures the maximum number of attempts that a cold starting node is permitted to try to start up the network without receiving any valid response from another node. It can be modified in DEFAULT_CONFIG or CONFIG state only. Must be identical in all nodes of a cluster. Valid values are 2 to 31. |
| | MIN | | | 2 | N/A |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 16:20 | PTA | RW | R | 0 | Passive to Active (pAllowPassiveToActive)<br>Defines the number of consecutive even / odd cycle pairs that must have valid clock correction terms before the CC is allowed to transit from NORMAL_PASSIVE to NORMAL_ACTIVE state. If set to '00000' the CC is not allowed to transit from NORMAL_PASSIVE to NORMAL_ACTIVE state. It can be modified in DEFAULT_CONFIG or CONFIG state only.<br>Valid values are 0 to 31 even / odd cycle pairs. |
| 21 | WUCS | RW | R | 0 | Wakeup Channel Select (pWakeupChannel)<br>With this bit the Host selects the channel on which the CC sends the Wakeup pattern. The CC ignores any attempt to change the status of this bit when not in DEFAULT_CONFIG or CONFIG state.<br>1 = Send wakeup pattern on channel B<br>0 = Send wakeup pattern on channel A |
| | SEND_WKUP_PATTERN_ON_CH_A | | | 0 | N/A |
| | SEND_WKUP_PATTERN_ON_CH_B | | | 1 | N/A |
| 22 | TSM | RW | R | 1 | Transmission Slot Mode (pSingleSlotEnabled)<br>Selects the initial transmission slot mode. In SINGLE slot mode the CC may only transmit in the preconfigured key slot. The key slot ID is configured in the header section of message buffer 0 respectively message buffers 0 and 1 depending on bit MRC.SPLM. In case TSM = '1', message buffer 0 respectively message buffers 0,1 can be (re)configured in DEFAULT_CONFIG or CONFIG state only. In ALL slot mode the CC may transmit in all slots. TSM is a configuration bit which can only be set / reset by the Host. The bit can be written in DEFAULT_CONFIG or CONFIG state only. The CC changes to ALL slot mode when the Host successfully applied the ALL_SLOTS command by writing CMD[3:0] = '0101' in POC states NORMAL_ACTIVE or NORMAL_PASSIVE. The actual slot mode is monitored by CCSV.SLM[1:0].<br>1 = SINGLE Slot Mode (default after hard reset)<br>0 = ALL Slot Mode |
| | ALL_SLOT_MODE | | | 0 | N/A |
| | SINGLE_SLOT_MODE | | | 1 | N/A |
| 23 | HCSE | RW | R | 0 | Halt due to Clock Sync Error (pAllowHaltDueToClock)<br>Controls the transition to HALT state due to a clock synchronization error. The bit can be modified in DEFAULT_CONFIG or CONFIG state only.<br>1 = CC will enter HALT state<br>0 = CC will enter / remain in NORMAL_PASSIVE |
| | CC_TO_ENTER_NORMAL_PASSIVE | | | 0 | N/A |
| | CC_TO_ENTER_HALT | | | 1 | N/A |
| 24 | MTSA_ | RW | R | 0 | Select Channel A for MTS Transmission<br>The bit selects channel A for MTS symbol transmission. The flag is reset by default and may be modified only in DEFAULT_CONFIG or CONFIG state.<br>1 = Channel A selected for MTS transmission<br>0 = Channel A disabled for MTS transmission |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| | CH_A_DISABLED_FOR_MTS_TXMN | | | 0 | N/A |
| | CH_A_SELECTED_FOR_MTS_TXMN | | | 1 | N/A |
| 25 | MTSB_ | RW | R | 0 | Select Channel B for MTS Transmission<br>The bit selects channel B for MTS symbol transmission. The flag is reset by default and may be modified only in DEFAULT_CONFIG or CONFIG state.<br>1 = Channel B selected for MTS transmission<br>0 = Channel B disabled for MTS transmission |
| | CH_B_DISABLED_FOR_MTS_TXMN | | | 0 | N/A |
| | CH_B_SELECTED_FOR_MTS_TXMN | | | 1 | N/A |
| 26 | CCHA | RW | R | 1 | Connected to Channel A (pChannels)<br>Configures whether the node is connected to channel A.<br>1 = Node connected to channel A (default after hard reset)<br>0 = Not connected to channel A |
| | CH_A_NOT_CONNECTED | | | 0 | N/A |
| | CH_A_CONNECTED | | | 1 | N/A |
| 27 | CCHB | RW | R | 1 | Connected to Channel B (pChannels)<br>Configures whether the node is connected to channel B.<br>1 = Node connected to channel B (default after hard reset)<br>0 = Not connected to channel B |
| | CH_B_NOT_CONNECTED | | | 0 | N/A |
| | CH_B_CONNECTED | | | 1 | N/A |

### 15.1.20 FLEXRAY_SUCC2

**Description:** SUC Configuration Register 2
**Address:** 0x40560084
**Offset:** 0x84
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** Protected write, see LCK register
**Default:** 0x1000504

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | LT [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | LT [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:21] | | | LT [20:16] | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:28] | | | | LTN [27:24] | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:20 | LT | RW | R | 1284 | Listen Timeout (pdListenTimeout)<br>Configures wakeup / startup listen timeout in uT. The range for pdListenTimeout is 1284 to 1283846 uT. |
| | MIN | | | 1284 | N/A |
| | MAX | | | 1283846 | N/A |
| 24:27 | LTN | RW | R | 1 | Listen Timeout Noise (gListenNoise - 1)<br>Configures the upper limit for startup and wakeup listen timeout in the presence of noise expressed as a multiple of pdListenTimeout. The range for gListenNoise is 2 to 16. LTN[3:0] must be configured identical in all nodes of a cluster. |
| | MIN | | | 1 | N/A |

### 15.1.21 FLEXRAY_SUCC3

**Description:** SUC Configuration Register 3
**Address:** 0x40560088
**Offset:** 0x88
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** Protected write, see LCK register
**Default:** 0x11

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | WCF [7:4] | | | | WCP [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | WCP | RW | R | 1 | Maximum Without Clock Correction Passive (gMaxWithoutClockCorrectionPassive)<br>Defines the number of consecutive even / odd cycle pairs with missing clock correction terms<br>that will cause a transition from NORMAL_ACTIVE to NORMAL_PASSIVE state. Must be<br>identical in all nodes of a cluster. Valid values are 1 to 15 cycle pairs. |
| | MIN | | | 1 | N/A |
| 4:7 | WCF | RW | R | 1 | Maximum Without Clock Correction Fatal (gMaxWithoutClockCorrectionFatal)<br>Defines the number of consecutive even / odd cycle pairs with missing clock correction terms<br>that will cause a transition from NORMAL_ACTIVE or NORMAL_PASSIVE to HALT state.<br>Must be identical in all nodes of a cluster. Valid values are 1 to 15 cycle pairs. |
| | MIN | | | 1 | N/A |

### 15.1.22 FLEXRAY_NEMC

**Description:** NEM Configuration Register
**Address:** 0x4056008C
**Offset:** 0x8C
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** Protected write, see LCK register
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:4] | | | | NML [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | NML | RW | R | 0 | Network Management Vector Length (gNetworkManagementVectorLength)<br>These bits configure the length of the NM vector. The configured length must be identical in all nodes of a cluster. Valid values are 0 to 12 bytes. |
| | MAX | | | 12 | N/A |

### 15.1.23 FLEXRAY_PRTC1

**Description:** PRT Configuration Register 1
**Address:** 0x40560090
**Offset:** 0x90
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** Protected write, see LCK register
**Default:** 0x84C0633

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | CASM [7:4] | | | | TSST [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | BRP [15:14] | | SPP [13:12] | | None [11:11] | CASM6 [10:10] | CASM [9:8] | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | RXW [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | RWP [31:26] | | | | | | None [25:25] | RXW [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | TSST | RW | R | 3 | Transmission Start Sequence Transmitter (gdTSSTransmitter)<br>Configures the duration of the Transmission Start Sequence (TSS) in terms of bit times (1 bit time = 4 uT = 100ns@10Mbps). Must be identical in all nodes of a cluster. Valid values are 3 to 15 bit times. |
| | MIN | | | 3 | N/A |
| | MAX | | | 15 | N/A |
| 4:9 | CASM | RW | R | 35 | Collision Avoidance Symbol Max (gdCASRxLowMax)<br>Configures the upper limit of the acceptance window for a collision avoidance symbol (CAS).<br>CASM6 is fixed to '1'. Valid values are 67 to 99 bit times, corresponding to a CASM range (without CASM6) of 3 to 35. |
| | MIN | | | 3 | N/A |
| | MAX | | | 35 | N/A |
| 10 | CASM6 | R | R | 1 | Part of CASM[6:0], but fixed to 1 |
| 12:13 | SPP | RW | R | 0 | Strobe Point Position<br>Defines the sample count value for strobing. The strobed bit value is set to the voted value when the sample count is incremented to the value configured by SPP[1:0].<br>00, 11= Sample 5 (default)<br>01 = Sample 4<br>10 = Sample 6 |
| | SAMPLE_5 | | | 0 | N/A |
| | SAMPLE_5_MIRROR | | | 3 | N/A |
| | SAMPLE_4 | | | 1 | N/A |
| | SAMPLE_6 | | | 2 | N/A |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 14:15 | BRP | RW | R | 0 | Baud Rate Prescaler (gdSampleClockPeriod, pSamplesPerMicrotick)<br>The Baud Rate Prescaler configures the baud rate on the FlexRay bus. The baud rates listed<br>below are valid with a sample clock eray_sclk = 80 MHz. One bit time always consists of 8<br>samples independent of the configured baud rate.<br>00 = 10 MBit/s (default)<br>gdSampleClockPeriod = 12.5 ns = 1 - eray_sclk<br>pSamplesPerMicrotick = 2 (1 uT = 25 ns)<br>01 = 5 MBit/s<br>gdSampleClockPeriod = 25 ns = 2 - eray_sclk<br>pSamplesPerMicrotick = 1 (1 uT = 25 ns)<br>10, 11 = 2.5 MBit/s<br>gdSampleClockPeriod = 50 ns = 4 - eray_sclk<br>pSamplesPerMicrotick = 1 (1 uT = 50 ns) |
| | BAUD_10_MBPS | | | 0 | N/A |
| | BAUD_5_MBPS | | | 1 | N/A |
| | BAUD_2P5_MBPS | | | 2 | N/A |
| | BAUD_2P5_MBPS _MIRROR | | | 3 | N/A |
| 16:24 | RXW | RW | R | 76 | Wakeup Symbol Receive Window Length (gdWakeupSymbolRxWindow)<br>Configures the number of bit times used by the node to test the duration of the received wakeup<br>pattern. Must be identical in all nodes of a cluster.<br>Valid values are 76 to 301 bit times. |
| | MIN | | | 76 | N/A |
| | MAX | | | 301 | N/A |
| 26:31 | RWP | RW | R | 2 | Repetitions of Tx Wakeup Pattern (pWakeupPattern)<br>Configures the number of repetitions (sequences) of the Tx wakeup symbol. Valid values are 2<br>to 63. |
| | MIN | | | 2 | N/A |

### 15.1.24 FLEXRAY_PRTC2

**Description:** PRT Configuration Register 2
**Address:** 0x40560094
**Offset:** 0x94
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** Protected write, see LCK register
**Default:** 0xF2D0A0E

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:6] | | RXI_ [5:0] | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:14] | | RXL [13:8] | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | TXI_ [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:30] | | TXL [29:24] | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:5 | RXI_ | RW | R | 14 | Wakeup Symbol Receive Idle (gdWakeupSymbolRxIdle)<br>Configures the number of bit times used by the node to test the duration of the idle phase of the received wakeup symbol. Must be identical in all nodes of a cluster. Valid values are 14 to 59 bit times. |
| | MIN | | | 14 | N/A |
| | MAX | | | 59 | N/A |
| 8:13 | RXL | RW | R | 10 | Wakeup Symbol Receive Low (gdWakeupSymbolRxLow)<br>Configures the number of bit times used by the node to test the duration of the low phase of the received wakeup symbol. Must be identical in all nodes of a cluster. Valid values are 10 to 55 bit times. |
| | MIN | | | 10 | N/A |
| | MAX | | | 55 | N/A |
| 16:23 | TXI_ | RW | R | 45 | Wakeup Symbol Transmit Idle (gdWakeupSymbolTxIdle)<br>Configures the number of bit times used by the node to transmit the idle phase of the wakeup symbol. Must be identical in all nodes of a cluster. Valid values are 45 to 180 bit times. |
| | MIN | | | 45 | N/A |
| | MAX | | | 180 | N/A |
| 24:29 | TXL | RW | R | 15 | Wakeup Symbol Transmit Low (gdWakeupSymbolTxLow)<br>Configures the number of bit times used by the node to transmit the low phase of the wakeup symbol. Must be identical in all nodes of a cluster. Valid values are 15 to 60 bit times. |
| | MIN | | | 15 | N/A |
| | MAX | | | 60 | N/A |

### 15.1.25 FLEXRAY_MHDC

**Description:** MHD Configuration Register
**Address:** 0x40560098
**Offset:** 0x98
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** Protected write, see LCK register
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:7] | SFDL [6:0] | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | SLT [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:29] | | | SLT [28:24] | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:6 | SFDL | RW | R | 0 | Static Frame Data Length (gPayloadLengthStatic)<br>Configures the cluster-wide payload length for all frames sent in the static segment in double bytes. The payload length must be identical in all nodes of a cluster. Valid values are 0 to 127. |
| 16:28 | SLT | RW | R | 0 | Start of Latest Transmit (pLatestTx)<br>Configures the maximum minislot value allowed before inhibiting frame transmission in the dynamic segment of the cycle. There is no transmission in dynamic segment if SLT[12:0] is set to zero. Valid values are 0 to 7981 minislots. |
| | MAX | | | 7981 | N/A |

### 15.1.26 FLEXRAY_GTUC1

**Description:** GTU Configuration Register 1
**Address:** 0x405600A0
**Offset:** 0xA0
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** Protected write, see LCK register
**Default:** 0x280

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | UT [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | UT [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:20] | | | | UT [19:16] | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:19 | UT | RW | R | 640 | Microtick per Cycle (pMicroPerCycle)<br>Configures the duration of the communication cycle in microticks. Valid values are 640 to 640000 uT. |
| | MIN | | | 640 | N/A |
| | MAX | | | 640000 | N/A |

### 15.1.27 FLEXRAY_GTUC2

**Description:** GTU Configuration Register 2
**Address:** 0x405600A4
**Offset:** 0xA4
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** Protected write, see LCK register
**Default:** 0x2000A

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | MPC [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:14] | | MPC [13:8] | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:20] | | | | SNM [19:16] | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:13 | MPC | RW | R | 10 | Macrotick Per Cycle (gMacroPerCycle)<br>Configures the duration of one communication cycle in macroticks. The cycle length must be<br>identical in all nodes of a cluster. Valid values are 10 to 16000 MT. |
| | MIN | | | 10 | N/A |
| | MAX | | | 16000 | N/A |
| 16:19 | SNM | RW | R | 2 | Sync Node Max (gSyncNodeMax)<br>Maximum number of frames within a cluster with sync frame indicator bit SYN set to '1'. Must<br>be identical in all nodes of a cluster. Valid values are 2 to 15. |
| | MIN | | | 2 | N/A |
| | MAX | | | 15 | N/A |

### 15.1.28 FLEXRAY_GTUC3

**Description:** GTU Configuration Register 3
**Address:** 0x405600A8
**Offset:** 0xA8
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** Protected write, see LCK register
**Default:** 0x2020000

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | UIOA [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | UIOB [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:23] | MIOA [22:16] | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:31] | MIOB [30:24] | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | UIOA | RW | R | 0 | Microtick Initial Offset Channel A (pMicroInitialOffset[A]) Configures the number of microticks between the actual time reference point on channel A and the subsequent macrotick boundary of the secondary time reference point. The parameter depends on pDelayCompensation[A] and therefore has to be set for each channel independently. Valid values are 0 to 240 uT. |
| | MAX | | | 240 | N/A |
| 8:15 | UIOB | RW | R | 0 | Microtick Initial Offset Channel B (pMicroInitialOffset[B]) Configures the number of microticks between the actual time reference point on channel B and the subsequent macrotick boundary of the secondary time reference point. The parameter depends on pDelayCompensation[B] and therefore has to be set for each channel independently. Valid values are 0 to 240 uT. |
| | MAX | | | 240 | N/A |
| 16:22 | MIOA | RW | R | 2 | Macrotick Initial Offset Channel A (pMacroInitialOffset[A]) Configures the number of macroticks between the static slot boundary and the subsequent macrotick boundary of the secondary time reference point based on the nominal macrotick duration. Must be identical in all nodes of a cluster. Valid values are 2 to 72 MT. |
| | MIN | | | 2 | N/A |
| | MAX | | | 72 | N/A |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 24:30 | MIOB | RW | R | 2 | Macrotick Initial Offset Channel B (pMacroInitialOffset[B])<br>Configures the number of macroticks between the static slot boundary and the subsequent macrotick boundary of the secondary time reference point based on the nominal macrotick duration.<br>Must be identical in all nodes of a cluster. Valid values are 2 to 72 MT. |
| | MIN | | | 2 | N/A |
| | MAX | | | 72 | N/A |

### 15.1.29 FLEXRAY_GTUC4

**Description:** GTU Configuration Register 4
**Address:** 0x405600AC
**Offset:** 0xAC
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** Protected write, see LCK register
**Default:** 0x80007

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | NIT [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:14] | | NIT [13:8] | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | OCS [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:30] | | OCS [29:24] | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:13 | NIT | RW | R | 7 | Network Idle Time Start (gMacroPerCycle - gdNIT - 1)<br>Configures the starting point of the Network Idle Time NIT at the end of the communication<br>cycle expressed in terms of macroticks from the beginning of the cycle. The start of NIT is recognized if Macrotick = gMacroPerCycle - gdNIT -1 and the increment pulse of Macrotick is set.<br>Must be identical in all nodes of a cluster. Valid values are 7 to 15997 MT. |
| | MIN | | | 7 | N/A |
| | MAX | | | 15997 | N/A |
| 16:29 | OCS | RW | R | 8 | Offset Correction Start (gOffsetCorrectionStart - 1)<br>Determines the start of the offset correction within the NIT phase, calculated from start of cycle.<br>Must be identical in all nodes of a cluster. For cluster consisting of E-Ray implementations only,<br>it is sufficient to program OCS = NIT + 1. Valid values are 8 to 15998 MT. |
| | MIN | | | 8 | N/A |
| | MAX | | | 15998 | N/A |

### 15.1.30 FLEXRAY_GTUC5

**Description:** GTU Configuration Register 5
**Address:** 0x405600B0
**Offset:** 0xB0
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** Protected write, see LCK register
**Default:** 0xE000000

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DCA [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | DCB [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:21] | | | CDD [20:16] | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | DEC [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | DCA | RW | R | 0 | Delay Compensation Channel A (pDelayCompensation[A]) Used to compensate for reception delays on the indicated channel. This covers assumed propagation delay up to cPropagationDelayMax for microticks in the range of 0.0125 to 0.05us. In practice, the minimum of the propagation delays of all sync nodes should be applied. Valid values are 0 to 200 uT. |
| | MAX | | | 200 | N/A |
| 8:15 | DCB | RW | R | 0 | Delay Compensation Channel B (pDelayCompensation[B]) Used to compensate for reception delays on the indicated channel. This covers assumed propagation delay up to cPropagationDelayMax for microticks in the range of 0.0125 to 0.05us. In practice, the minimum of the propagation delays of all sync nodes should be applied. Valid values are 0 to 200 uT. |
| | MAX | | | 200 | N/A |
| 16:20 | CDD | RW | R | 0 | Cluster Drift Damping (pClusterDriftDamping) Configures the cluster drift damping value used in clock synchronization to minimize accumulation of rounding errors. Valid values are 0 to 20 uT. |
| | MAX | | | 20 | N/A |
| 24:31 | DEC | RW | R | 14 | Decoding Correction (pDecodingCorrection) Configures the decoding correction value used to determine the primary time reference point. Valid values are 14 to 143 uT. |
| | MIN | | | 14 | N/A |
| | MAX | | | 143 | N/A |

### 15.1.31 FLEXRAY_GTUC6

**Description:** GTU Configuration Register 6
**Address:** 0x405600B4
**Offset:** 0xB4
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** Protected write, see LCK register
**Default:** 0x20000

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | ASR [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:11] | | | | | ASR [10:8] | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | MOD [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:27] | | | | | MOD [26:24] | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:10 | ASR | RW | R | 0 | Accepted Startup Range (pdAcceptedStartupRange)<br>Number of microticks constituting the expanded range of measured deviation for startup frames during integration. Valid values are 0 to 1875 uT. |
| | MAX | | | 1875 | N/A |
| 16:26 | MOD | RW | R | 2 | Maximum Oscillator Drift (pdMaxDrift)<br>Maximum drift offset between two nodes that operate with unsynchronized clocks over one communication cycle in uT. Valid values are 2 to 1923 uT. |
| | MIN | | | 2 | N/A |
| | MAX | | | 1923 | N/A |

### 15.1.32 FLEXRAY_GTUC7

**Description:** GTU Configuration Register 7
**Address:** 0x405600B8
**Offset:** 0xB8
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** Protected write, see LCK register
**Default:** 0x20004

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | SSL [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:10] | | | | | | SSL [9:8] | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | NSS [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:26] | | | | | | NSS [25:24] | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:9 | SSL | RW | R | 4 | Static Slot Length (gdStaticSlot)<br>Configures the duration of a static slot in macroticks. The static slot length must be identical in all nodes of a cluster. Valid values are 4 to 659 MT. |
| | MIN | | | 4 | N/A |
| | MAX | | | 659 | N/A |
| 16:25 | NSS | RW | R | 2 | Number of Static Slots (gNumberOfStaticSlots)<br>Configures the number of static slots in a cycle. At least 2 coldstart nodes must be configured to startup a FlexRay network. The number of static slots must be identical in all nodes of a cluster.<br>Valid values are 2 to 1023. |
| | MIN | | | 2 | N/A |
| | MAX | | | 1023 | N/A |

### 15.1.33 FLEXRAY_GTUC8

**Description:** GTU Configuration Register 8
**Address:** 0x405600BC
**Offset:** 0xBC
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** Protected write, see LCK register
**Default:** 0x2

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:6] | | MSL [5:0] | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | NMS [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:29] | | | NMS [28:24] | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:5 | MSL | RW | R | 2 | Minislot Length (gdMinislot)<br>Configures the duration of a minislot in macroticks. The minislot length must be identical in all nodes of a cluster. Valid values are 2 to 63 MT. |
| | MIN | | | 2 | N/A |
| | MAX | | | 63 | N/A |
| 16:28 | NMS | RW | R | 0 | Number of Minislots (gNumberOfMinislots)<br>Configures the number of minislots within the dynamic segment of a cycle. The number of minislots must be identical in all nodes of a cluster. Valid values are 0 to 7986. |
| | MAX | | | 7986 | N/A |

### 15.1.34 FLEXRAY_GTUC9

**Description:** GTU Configuration Register 9
**Address:** 0x405600C0
**Offset:** 0xC0
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** Protected write, see LCK register
**Default:** 0x101

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:6] | | APO [5:0] | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:13] | | | MAPO [12:8] | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:18] | | | | | | DSI [17:16] | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:5 | APO | RW | R | 1 | Action Point Offset (gdActionPointOffset)<br>Configures the action point offset in macroticks within static slots and symbol window. Must be identical in all nodes of a cluster. Valid values are 1 to 63 MT. |
| | MIN | | | 1 | N/A |
| 8:12 | MAPO | RW | R | 1 | Minislot Action Point Offset (gdMinislotActionPointOffset)<br>Configures the action point offset in macroticks within the minislots of the dynamic segment.<br>Must be identical in all nodes of a cluster. Valid values are 1 to 31 MT. |
| | MIN | | | 1 | N/A |
| 16:17 | DSI | RW | R | 0 | Dynamic Slot Idle Phase (gdDynamicSlotIdlePhase)<br>The duration of the dynamic slot idle phase has to be greater or equal than the idle detection time. Must be identical in all nodes of a cluster. Valid values are 0 to 2 Minislot. |
| | MAX | | | 2 | N/A |

### 15.1.35 FLEXRAY_GTUC10

**Description:** GTU Configuration Register 10
**Address:** 0x405600C4
**Offset:** 0xC4
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** Protected write, see LCK register
**Default:** 0x20005

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | MOC [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:14] | | MOC [13:8] | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | MRC [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:27] | | | | | MRC [26:24] | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:13 | MOC | RW | R | 5 | Maximum Offset Correction (pOffsetCorrectionOut) Holds the maximum permitted offset correction value to be applied by the internal clock synchronization algorithm (absolute value). The CC checks only the internal offset correction value against the maximum offset correction value. Valid values are 5 to 15266 uT. |
| | MIN | | | 5 | N/A |
| | MAX | | | 15266 | N/A |
| 16:26 | MRC | RW | R | 2 | Maximum Rate Correction (pRateCorrectionOut) Holds the maximum permitted rate correction value to be applied by the internal clock synchronization algorithm. The CC checks only the internal rate correction value against the maximum rate correction value (absolute value). Valid values are 2 to 1923 uT. |
| | MIN | | | 2 | N/A |
| | MAX | | | 1923 | N/A |

### 15.1.36 FLEXRAY_GTUC11

**Description:** GTU Configuration Register 11
**Address:** 0x405600C8
**Offset:** 0xC8
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** Upper half word is wirte Protected, see LCK register
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:2] | | | | | | EOCC [1:0] | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:10] | | | | | | ERCC [9:8] | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:19] | | | | | EOC [18:16] | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:27] | | | | | ERC [26:24] | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:1 | EOCC | RW | R | 0 | External Offset Correction Control (vExternOffsetControl)<br>By writing to EOCC[1:0] the external offset correction is enabled as specified below. Should be modified only outside NIT.<br>00, 01 = No external offset correction<br>10 = External offset correction value subtracted from calculated offset correction value<br>11 = External offset correction value added to calculated offset correction value |
| | NO_EXT_OFFSET_CORRECTION | | | 0 | N/A |
| | NO_EXT_OFFSET_CORRECTION_MIRROR | | | 1 | N/A |
| | EXT_OFFSET_CORRECTION_SUBTRACTED | | | 2 | N/A |
| | EXT_OFFSET_CORRECTION_ADDED | | | 3 | N/A |
| 8:9 | ERCC | RW | R | 0 | External Rate Correction Control (vExternRateControl)<br>By writing to ERCC[1:0] the external rate correction is enabled as specified below. Should be modified only outside NIT.<br>00, 01 = No external rate correction<br>10 = External rate correction value subtracted from calculated rate correction value<br>11 = External rate correction value added to calculated rate correction value |
| | NO_EXT_RATE_CORRECTION | | | 0 | N/A |
| | NO_EXT_RATE_CORRECTION_MIRROR | | | 1 | N/A |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| | EXT_RATE_ CORRECTION _SUBTRACTED | | | 2 | N/A |
| | EXT_RATE_ CORRECTION_ADDED | | | 3 | N/A |
| 16:18 | EOC | RW | R | 0 | External Offset Correction (pExternOffsetCorrection) Holds the external offset correction value in microticks to be applied by the internal clock synchronization algorithm. The value is subtracted / added from / to the calculated offset correction value. The value is applied during NIT. May be modified in DEFAULT_CONFIG or CONFIG state only. Valid values are 0 to 7 uT. |
| 24:26 | ERC | RW | R | 0 | External Rate Correction (pExternRateCorrection) Holds the external rate correction value in microticks to be applied by the internal clock synchronization algorithm. The value is subtracted / added from / to the calculated rate correction value. The value is applied during NIT. May be modified in DEFAULT_CONFIG or CONFIG state only. Valid values are 0 to 7 uT. |

### 15.1.37 FLEXRAY_CCSV

**Description:** CC Status Vector
**Address:** 0x40560100
**Offset:** 0x100
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x104000

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | HRQ [7:7] | FSI [6:6] | POCS [5:0] | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:15] | CSI [14:14] | CSAI [13:13] | CSNI [12:12] | None [11:10] | | SLM [9:8] | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | RCA [23:19] | | | | | WSV [18:16] | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:30] | | PSL [29:24] | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:5 | POCS | R | RW | 0 | Protocol Operation Control Status<br>Indicates the actual state of operation of the CC Protocol Operation Control<br>00 0000 = DEFAULT_CONFIG state<br>00 0001 = READY state<br>00 0010 = NORMAL_ACTIVE state<br>00 0011 = NORMAL_PASSIVE state<br>00 0100 = HALT state<br>00 0101 = MONITOR_MODE state<br>00 0110 ... 00 1110 = reserved<br>00 1111 = CONFIG state<br>Indicates the actual state of operation of the POC in the wakeup path<br>01 0000 = WAKEUP_STANDBY state<br>01 0001 = WAKEUP_LISTEN state<br>01 0010 = WAKEUP_SEND state<br>01 0011 = WAKEUP_DETECT state<br>01 0100 ... 01 1111 = reserved<br>Indicates the actual state of operation of the POC in the startup path<br>10 0000 = STARTUP_PREPARE state<br>10 0001 = COLDSTART_LISTEN state<br>10 0010 = COLDSTART_COLLISION_RESOLUTION state<br>10 0011 = COLDSTART_CONSISTENCY_CHECK state<br>10 0100 = COLDSTART_GAP state<br>10 0101 = COLDSTART_JOIN State<br>10 0110 = INTEGRATION_COLDSTART_CHECK state<br>10 0111 = INTEGRATION_LISTEN state<br>10 1000 = INTEGRATION_CONSISTENCY_CHECK state<br>10 1001 = INITIALIZE_SCHEDULE state<br>10 1010 = ABORT_STARTUP state<br>10 1011 = STARTUP_SUCCESS state<br>10 1100 ... 11 1111 = reserved |
| | DEFAULT_CONFIG | | | 0 | N/A |
| | READY | | | 1 | N/A |
| | NORMAL_ACTIVE | | | 2 | N/A |
| | NORMAL_PASSIVE | | | 3 | N/A |
| | HALT | | | 4 | N/A |
| | MONITOR_MODE | | | 5 | N/A |
| | CONFIG | | | 15 | N/A |
| | WAKEUP_STANDBY | | | 16 | N/A |
| | WAKEUP_LISTEN | | | 17 | N/A |
| | WAKEUP_SEND | | | 18 | N/A |
| | WAKEUP_DETECT | | | 19 | N/A |
| | STARTUP_PREPARE | | | 32 | N/A |
| | COLDSTART_LISTEN | | | 33 | N/A |
| | COLDSTART_COLLISION_RESOLUTION | | | 34 | N/A |
| | COLDSTART_CONSISTENCY_CHECK | | | 35 | N/A |
| | COLDSTART_GAP | | | 36 | N/A |
| | COLDSTART_JOIN | | | 37 | N/A |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| | INTEGRATION _COLDSTART_CHECK | | | 38 | N/A |
| | INTEGRATION_LISTEN | | | 39 | N/A |
| | INTEGRATION _CONSISTENCY _CHECK | | | 40 | N/A |
| | INITIALIZE_SCHEDULE | | | 41 | N/A |
| | ABORT_STARTUP | | | 42 | N/A |
| | STARTUP_SUCCESS | | | 43 | N/A |
| 6 | FSI | R | RW | 0 | Freeze Status Indicator (vPOC!Freeze)<br>Indicates that the POC has entered the HALT state due to CHI command FREEZE or due to an error condition requiring an immediate POC halt. Reset by transition from HALT to DEFAULT_CONFIG state. |
| 7 | HRQ | R | RW | 0 | Halt Request (vPOC!CHIHaltRequest)<br>Indicates that a request from the Host has been received to halt the POC at the end of the communication cycle. Reset by transition from HALT to DEFAULT_CONFIG state or when entering READY state. |
| 8:9 | SLM | R | RW | 0 | Slot Mode (vPOC!SlotMode)<br>Indicates the actual slot mode of the POC in states READY, WAKEUP, STARTUP, NORMAL_ACTIVE, and NORMAL_PASSIVE. Default is SINGLE. Changes to ALL, depending on SUCC1.TSM. In NORMAL_ACTIVE or NORMAL_PASSIVE state the CHI command ALL_SLOTS will change the slot mode from SINGLE over ALL_PENDING to ALL. Set to SINGLE in all other states.<br>00 = SINGLE<br>01 = reserved<br>10 = ALL_PENDING<br>11 = ALL |
| | SINGLE | | | 0 | N/A |
| | ALL_PENDING | | | 2 | N/A |
| | ALL | | | 3 | N/A |
| 12 | CSNI | R | RW | 0 | Coldstart Noise Indicator (vPOC!ColdstartNoise)<br>Indicates that the cold start procedure occurred under noisy conditions. Reset by CHI command RESET_STATUS_INDICATORS or by transition from HALT to DEFAULT_CONFIG state or from READY to STARTUP state. |
| 13 | CSAI | R | RW | 0 | Coldstart Abort Indicator<br>Coldstart aborted. Reset by CHI command RESET_STATUS_INDICATORS or by transition from HALT to DEFAULT_CONFIG state or from READY to STARTUP state. |
| 14 | CSI | R | RW | 1 | Cold Start Inhibit (vColdStartInhibit)<br>Indicates that the node is disabled from cold starting. The flag is set whenever the POC enters READY state due to CHI command READY. The flag has to be reset under control of the Host by CHI command ALLOW_COLDSTART (SUCC1.CMD[3:0] = '1001').<br>1 = Cold starting of node disabled<br>0 = Cold starting of node enabled |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| | NODE_COLD_START_ENABLED | | | 0 | N/A |
| | NODE_COLD_START_DISABLED | | | 1 | N/A |
| 16:18 | WSV | R | RW | 0 | Wakeup Status (vPOC!WakeupStatus)<br>Indicates the status of the current wakeup attempt. Reset when entering Wakeup state, by CHI command RESET_STATUS_INDICATORS, or by transition from DEFAULT_CONFIG to CONFIG state.<br>000 = UNDEFINED. Wakeup not yet executed by the CC.<br>001 = RECEIVED_HEADER. Set when the CC finishes wakeup due to the reception of a frame header without coding violation on either channel in WAKEUP_LISTEN state.<br>010 = RECEIVED_WUP. Set when the CC finishes wakeup due to the reception of a valid wakeup pattern on the configured wakeup channel in WAKEUP_LISTEN state.<br>011 = COLLISION_HEADER. Set when the CC stops wakeup due to a detected collision during wakeup pattern transmission by receiving a valid header on either channel.<br>100 = COLLISION_WUP. Set when the CC stops wakeup due to a detected collision during wakeup pattern transmission by receiving a valid wakeup pattern on the configured wakeup channel.<br>101 = COLLISION_UNKNOWN. Set when the CC stops wakeup by leaving WAKEUP_DETECT state after expiration of the wakeup timer without receiving a valid wakeup pattern or a valid frame header.<br>110 = TRANSMITTED. Set when the CC has successfully completed the transmission of the wakeup pattern.<br>111 = reserved |
| | UNDEFINED | | | 0 | N/A |
| | RECEIVED_HEADER | | | 1 | N/A |
| | RECEIVED_WUP | | | 2 | N/A |
| | COLLISION_HEADER | | | 3 | N/A |
| | COLLISION_WUP | | | 4 | N/A |
| | COLLISION_UNKNOWN | | | 5 | N/A |
| | TRANSMITTED | | | 6 | N/A |
| 19:23 | RCA | R | RW | 2 | Remaining Coldstart Attempts (vRemainingColdstartAttempts)<br>Indicates the number of remaining coldstart attempts. The RUN command resets this counter to the maximum number of coldstart attempts as configured by SUCC1.CSA[4:0]. The initial value of RCA[4:0] during CONFIG and DEFAULT_CONFIG state is also SUCC1.CSA[4:0]. |
| 24:29 | PSL | R | RW | 0 | POC Status Log<br>Status of POCS[5:0] immediately before entering HALT state. Set when entering HALT state.<br>Set to HALT when FREEZE command is applied during HALT state and FSI is not already set i.e. the HALT state was not reached by FREEZE command. Reset to '00 0000' when leaving HALT state. |

### 15.1.38 FLEXRAY_CCEV

**Description:** CC Error Vector
**Address:** 0x40560104
**Offset:** 0x104
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | ERRM [7:6] | | None [5:4] | | CCFC [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:13] | | | PTAC [12:8] | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | CCFC | R | RW | 0 | Clock Correction Failed Counter (vClockCorrectionFailed)<br>The Clock Correction Failed Counter is incremented by one at the end of any odd communication<br>cycle where either the missing offset correction error or missing rate correction error are<br>active. The Clock Correction Failed Counter is reset to '0' at the end of an odd communication<br>cycle if neither the offset correction failed nor the rate correction failed errors are active. The<br>Clock Correction Failed Counter stops at 15. |
| 6:7 | ERRM | R | RW | 0 | Error Mode (vPOC!ErrorMode)<br>Indicates the actual error mode of the POC.<br>00 = ACTIVE (green)<br>01 = PASSIVE (yellow)<br>10 = COMM_HALT (red)<br>11 = reserved |
| | ACTIVE | | | 0 | N/A |
| | PASSIVE | | | 1 | N/A |
| | COMM_HALT | | | 2 | N/A |
| 8:12 | PTAC | R | RW | 0 | Passive to Active Count (vAllowPassiveToActive)<br>Indicates the number of consecutive even / odd cycle pairs that have passed with valid rate and<br>offset correction terms, while the node is waiting to transit from NORMAL_PASSIVE state to<br>NORMAL_ACTIVE state. The transition takes place when PTAC[4:0] equals<br>SUCC1.PTA[4:0] -1. |

### 15.1.39 FLEXRAY_SCV

**Description:** Slot Counter Value
**Address:** 0x40560110
**Offset:** 0x110
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | SCCA [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:11] | | | | | SCCA [10:8] | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | SCCB [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:27] | | | | | SCCB [26:24] | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:10 | SCCA | R | RW | 0 | Slot Counter Channel A (vSlotCounter[A])<br>Current slot counter value on channel A. The value is incremented by the CC and reset at the start of a communication cycle. Valid values are 0 to 2047. |
| 16:26 | SCCB | R | RW | 0 | Slot Counter Channel B (vSlotCounter[B])<br>Current slot counter value on channel B. The value is incremented by the CC and reset at the start of a communication cycle. Valid values are 0 to 2047. |

### 15.1.40 FLEXRAY_MTCCV

**Description:** Macrotick and Cycle Counter Value
**Address:** 0x40560114
**Offset:** 0x114
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | MTV [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:14] | | MTV [13:8] | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:22] | | CCV [21:16] | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:13 | MTV | R | RW | 0 | Macrotick Value (vMacrotick)<br>Current macrotick value. The value is incremented by the CC and reset at the start of a communication cycle. Valid values are 0 to 15999. |
| | MAX | | | 15999 | N/A |
| 16:21 | CCV | R | RW | 0 | Cycle Counter Value (vCycleCounter)<br>Current cycle counter value. The value is incremented by the CC at the start of a communication cycle. Valid values are 0 to 63. |

### 15.1.41 FLEXRAY_RCV

**Description:** Rate Correction Value
**Address:** 0x40560118
**Offset:** 0x118
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | RCV [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:12] | | | | RCV [11:8] | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:11 | RCV | R | RW | 0 | Rate Correction Value (vRateCorrection)<br>Rate correction value (two's complement). Calculated internal rate correction value before limitation.<br>If the RCV value exceeds the limits defined by GTUC10.MRC[10:0], flag SFS.RCLR<br>is set to '1'. |

### 15.1.42 FLEXRAY_OCV

**Description:** Offset Correction Value
**Address:** 0x4056011C
**Offset:** 0x11C
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | OCV [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | OCV [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:19] | | | | | OCV [18:16] | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:18 | OCV | R | RW | 0 | Offset Correction Value (vOffsetCorrection)<br>Offset correction value (two's complement). Calculated internal offset correction value before<br>limitation. If the OCV value exceeds the limits defined by GTUC10.MOC[13:0], flag<br>SFS.OCLR is set to '1'. |

### 15.1.43 FLEXRAY_SFS

**Description:** Sync Frame Status
**Address:** 0x40560120
**Offset:** 0x120
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VSAO [7:4] | | | | VSAE [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VSBO [15:12] | | | | VSBE [11:8] | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:20] | | | | RCLR [19:19] | MRCS [18:18] | OCLR [17:17] | MOCS [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | VSAE | R | RW | 0 | Valid Sync Frames Channel A, even communication cycle<br>Holds the number of valid sync frames received on channel A in the even communication cycle.<br>If transmission of sync frames is enabled by SUCC1.TXSY the value is incremented by one.<br>The value is updated during the NIT of each even communication cycle. |
| 4:7 | VSAO | R | RW | 0 | Valid Sync Frames Channel A, odd communication cycle<br>Holds the number of valid sync frames received on channel A in the odd communication cycle.<br>If transmission of sync frames is enabled by SUCC1.TXSY the value is incremented by one.<br>The value is updated during the NIT of each odd communication cycle. |
| 8:11 | VSBE | R | RW | 0 | Valid Sync Frames Channel B, even communication cycle<br>Holds the number of valid sync frames received on channel B in the even communication cycle.<br>If transmission of sync frames is enabled by SUCC1.TXSY the value is incremented by one.<br>The value is updated during the NIT of each even communication cycle. |
| 12:15 | VSBO | R | RW | 0 | Valid Sync Frames Channel B, odd communication cycle<br>Holds the number of valid sync frames received on channel B in the odd communication cycle.<br>If transmission of sync frames is enabled by SUCC1.TXSY the value is incremented by one.<br>The value is updated during the NIT of each odd communication cycle. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 16 | MOCS | R | RW | 0 | Missing Offset Correction Signal<br>The Missing Offset Correction flag signals to the Host, that no offset correction calculation can be performed because no sync frames were received. The flag is updated by the CC at start of offset correction phase.<br>1 = Missing offset correction signal<br>0 = Offset correction signal valid |
| | OFFSET_CORRECTION_SIGNAL_VALID | | | 0 | N/A |
| | OFFSET_CORRECTION_SIGNAL_INVALID | | | 1 | N/A |
| 17 | OCLR | R | RW | 0 | Offset Correction Limit Reached<br>The Offset Correction Limit Reached flag signals to the Host, that the offset correction value has exceeded its limit as defined by GTUC10.MOC[13:0]. The flag is updated by the CC at start of offset correction phase.<br>1 = Offset correction limit reached<br>0 = Offset correction below limit |
| | OFFSET_CORRECTION_BELOW_LIMIT | | | 0 | N/A |
| | OFFSET_CORRECTION_LIMIT_REACHED | | | 1 | N/A |
| 18 | MRCS | R | RW | 0 | Missing Rate Correction Signal<br>The Missing Rate Correction flag signals to the Host, that no rate correction calculation can be performed because no pairs of even / odd sync frames were received. The flag is updated by the CC at start of offset correction phase.<br>1 = Missing rate correction signal<br>0 = Rate correction signal valid |
| | RATE_CORRECTION_SIGNAL_VALID | | | 0 | N/A |
| | RATE_CORRECTION_SIGNAL_INVALID | | | 1 | N/A |
| 19 | RCLR | R | RW | 0 | Rate Correction Limit Reached<br>The Rate Correction Limit Reached flag signals to the Host, that the rate correction value has exceeded its limit as defined by GTUC10.MRC[10:0]. The flag is updated by the CC at start of offset correction phase.<br>1 = Rate correction limit reached<br>0 = Rate correction below limit |
| | RATE_CORRECTION_BELOW_LIMIT | | | 0 | N/A |
| | RATE_CORRECTION_LIMIT_REACHED | | | 1 | N/A |

### 15.1.44 FLEXRAY_SWNIT

**Description:** Symbol Window and NIT Status
**Address:** 0x40560124
**Offset:** 0x124
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | MTSB__ [7:7] | MTSA__ [6:6] | TCSB [5:5] | SBSB [4:4] | SESB [3:3] | TCSA [2:2] | SBSA [1:1] | SESA [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:12] | | | | SBNB [11:11] | SENB [10:10] | SBNA [9:9] | SENA [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | SESA | R | RW | 0 | Syntax Error in Symbol Window Channel A (vSS!SyntaxErrorA)<br>1 = Syntax error during symbol window detected on channel A<br>0 = No syntax error detected |
| | NO_SYNTAX_ERROR_IN_CH_A | | | 0 | N/A |
| | SYNTAX_ERR_IN_CH_A | | | 1 | N/A |
| 1 | SBSA | R | RW | 0 | Slot Boundary Violation in Symbol Window Channel A (vSS!BViolationA)<br>1 = Slot boundary violation during symbol window detected on channel A<br>0 = No slot boundary violation detected |
| | NO_BNDRY_VIOLATION_ERROR_IN_CH_A | | | 0 | N/A |
| | BNDRY_VIOLATION_ERROR_IN_CH_A | | | 1 | N/A |
| 2 | TCSA | R | RW | 0 | Transmission Conflict in Symbol Window Channel A (vSS!TxConflictA)<br>1 = Transmission conflict in symbol window detected on channel A<br>0 = No transmission conflict detected |
| | NO_TXMN_CONFLICT_IN_CH_A | | | 0 | N/A |
| | TXMN_CONFLICT_IN_CH_A | | | 1 | N/A |
| 3 | SESB | R | RW | 0 | Syntax Error in Symbol Window Channel B (vSS!SyntaxErrorB)<br>1 = Syntax error during symbol window detected on channel B<br>0 = No syntax error detected |
| | NO_SYNTAX_ERROR_IN_CH_B | | | 0 | N/A |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| | SYNTAX_ERR_IN_CH_B | | | 1 | N/A |
| 4 | SBSB | R | RW | 0 | Slot Boundary Violation in Symbol Window Channel B (vSS!BViolationB)<br>1 = Slot boundary violation during symbol window detected on channel B<br>0 = No slot boundary violation detected |
| | NO_BNDRY_VIOLATION_ERROR_IN_CH_B | | | 0 | N/A |
| | BNDRY_VIOLATION_ERROR_IN_CH_B | | | 1 | N/A |
| 5 | TCSB | R | RW | 0 | Transmission Conflict in Symbol Window Channel B (vSS!TxConflictB)<br>1 = Transmission conflict in symbol window detected on channel B<br>0 = No transmission conflict detected |
| | NO_TXMN_CONFLICT_IN_CH_B | | | 0 | N/A |
| | TXMN_CONFLICT_IN_CH_B | | | 1 | N/A |
| 6 | MTSA__ | R | RW | 0 | MTS Received on Channel A (vSS!ValidMTSA)<br>Media Access Test symbol received on channel A during the preceding symbol window.<br>Updated by the CC for each channel at the end of the symbol window. When this bit is set to '1', also interrupt flag SIR.MTSA is set to '1'.<br>1 = MTS symbol received on channel A<br>0 = No MTS symbol received on channel A |
| | NO_MTS_SYMBOL_RXD_IN_CH_A | | | 0 | N/A |
| | MTS_SYMBOL_RXD_IN_CH_A | | | 1 | N/A |
| 7 | MTSB__ | R | RW | 0 | MTS Received on Channel B (vSS!ValidMTSB)<br>Media Access Test symbol received on channel B during the preceding symbol window.<br>Updated by the CC for each channel at the end of the symbol window. When this bit is set to '1', also interrupt flag SIR.MTSB is set to '1'.<br>1 = MTS symbol received on channel B<br>0 = No MTS symbol received on channel B<br>NIT related status information. Updated by the CC at the end of the NIT for each channel: |
| | NO_MTS_SYMBOL_RXD_IN_CH_B | | | 0 | N/A |
| | MTS_SYMBOL_RXD_IN_CH_B | | | 1 | N/A |
| 8 | SENA | R | RW | 0 | Syntax Error during NIT Channel A (vSS!SyntaxErrorA)<br>1 = Syntax error during NIT detected on channel A<br>0 = No syntax error detected |
| | NO_SYNTAX_ERROR_DETECTED_ON_CH_A | | | 0 | N/A |
| | SYNTAX_ERROR_DETECTED_ON_CH_A | | | 1 | N/A |
| 9 | SBNA | R | RW | 0 | Slot Boundary Violation during NIT Channel A (vSS!BViolationA)<br>1 = Slot boundary violation during NIT detected on channel A<br>0 = No slot boundary violation detected |
| | NO_BNDRY_VIOLATION_ERROR_IN_CH_A | | | 0 | N/A |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| | BNDRY_VIOLATION _ERROR_IN_CH_A | | | 1 | N/A |
| 10 | SENB | R | RW | 0 | Syntax Error during NIT Channel B (vSS!SyntaxErrorB)<br>1 = Syntax error during NIT detected on channel B<br>0 = No syntax error detected |
| | NO_SYNTAX_ERROR _DETECTED_ON_CH_B | | | 0 | N/A |
| | SYNTAX_ERROR _DETECTED_ON_CH_B | | | 1 | N/A |
| 11 | SBNB | R | RW | 0 | Slot Boundary Violation during NIT Channel B (vSS!BViolationB)<br>1 = Slot boundary violation during NIT detected on channel B<br>0 = No slot boundary violation detected |
| | NO_BNDRY_VIOLATION _ERROR_IN_CH_B | | | 0 | N/A |
| | BNDRY_VIOLATION _ERROR_IN_CH_B | | | 1 | N/A |

### 15.1.45 FLEXRAY_ACS

**Description:** Aggregated Channel Status
**Address:** 0x40560128
**Offset:** 0x128
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:5] | | | SBVA [4:4] | CIA [3:3] | CEDA [2:2] | SEDA [1:1] | VFRA_ [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:13] | | | SBVB [12:12] | CIB [11:11] | CEDB [10:10] | SEDB [9:9] | VFRB_ [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | VFRA_ | RW1C | RW | 0 | Valid Frame Received on Channel A (vSS!ValidFrameA)<br>One or more valid frames were received on channel A in any static or dynamic slot during the observation period.<br>1 = Valid frame(s) received on channel A<br>0 = No valid frame received |
| | NO_VALID_FRAME_RXD_ON_CH_A | | | 0 | N/A |
| | VALID_FRAME_RXD_ON_CH_A | | | 1 | N/A |
| 1 | SEDA | RW1C | RW | 0 | Syntax Error Detected on Channel A (vSS!SyntaxErrorA)<br>One or more syntax errors in static or dynamic slots, symbol window, and NIT were observed on channel A.<br>1 = Syntax error(s) observed on channel A<br>0 = No syntax error observed |
| | NO_SYNTAX_ERR_OBSVD_ON_CH_A | | | 0 | N/A |
| | SYNTAX_ERR_OBSVD_ON_CH_A | | | 1 | N/A |
| 2 | CEDA | RW1C | RW | 0 | Content Error Detected on Channel A (vSS!ContentErrorA)<br>One or more frames with a content error were received on channel A in any static or dynamic slot during the observation period.<br>1 = Frame(s) with content error received on channel A<br>0 = No frame with content error received |
| | NO_FRAME_WITH_CONTENT_ERR_ON_CH_A | | | 0 | N/A |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| | FRAME_WITH _CONTENT_ERR_RXD _ON_CH_A | | | 1 | N/A |
| 3 | CIA | RW1C | RW | 0 | Communication Indicator Channel A<br>One or more valid frames were received on channel A in slots that also contained any additional communication during the observation period, i.e. one or more slots received a valid frame<br>AND had any combination of either syntax error OR content error OR slot boundary violation.<br>1 = Valid frame(s) received on channel A in slots containing any additional communication<br>0 = No valid frame(s) received in slots containing any additional communication |
| | NO_VALID_FRAME_RXD _ON_CH_A_IN_SLOTS | | | 0 | N/A |
| | VALID_FRAME_RXD_ON _CH_A_IN_SLOTS | | | 1 | N/A |
| 4 | SBVA | RW1C | RW | 0 | Slot Boundary Violation on Channel A (vSS!BViolationA)<br>One or more slot boundary violations were observed on channel A at any time during the observation period (static or dynamic slots, symbol window, and NIT).<br>1 = Slot boundary violation(s) observed on channel A<br>0 = No slot boundary violation observed |
| | NO_BNDRY_VIOLATION _ERROR_IN_CH_A | | | 0 | N/A |
| | BNDRY_VIOLATION _ERROR_IN_CH_A | | | 1 | N/A |
| 8 | VFRB_ | RW1C | RW | 0 | Valid Frame Received on Channel B (vSS!ValidFrameB)<br>One or more valid frames were received on channel B in any static or dynamic slot during the observation period. Reset under control of the Host.<br>1 = Valid frame(s) received on channel B<br>0 = No valid frame received |
| | NO_VALID_FRAME_RXD _ON_CH_B | | | 0 | N/A |
| | VALID_FRAME_RXD_ON _CH_B | | | 1 | N/A |
| 9 | SEDB | RW1C | RW | 0 | Syntax Error Detected on Channel B (vSS!SyntaxErrorB)<br>One or more syntax errors in static or dynamic slots, symbol window, and NIT were observed on channel B.<br>1 = Syntax error(s) observed on channel B<br>0 = No syntax error observed |
| | NO_SYNTAX_ERR _OBSVD_ON_CH_B | | | 0 | N/A |
| | SYNTAX_ERR_OBSVD _ON_CH_B | | | 1 | N/A |
| 10 | CEDB | RW1C | RW | 0 | Content Error Detected on Channel B (vSS!ContentErrorB)<br>One or more frames with a content error were received on channel B in any static or dynamic slot during the observation period.<br>1 = Frame(s) with content error received on channel B<br>0 = No frame with content error received |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| | NO_FRAME_WITH_CONTENT_ERR_ON_CH_B | | | 0 | N/A |
| | FRAME_WITH_CONTENT_ERR_RXD_ON_CH_B | | | 1 | N/A |
| 11 | CIB | RW1C | RW | 0 | Communication Indicator Channel B<br>One or more valid frames were received on channel B in slots that also contained any additional communication during the observation period, i.e. one or more slots received a valid frame<br>AND had any combination of either syntax error OR content error OR slot boundary violation.<br>1 = Valid frame(s) received on channel B in slots containing any additional communication<br>0 = No valid frame(s) received in slots containing any additional communication |
| | NO_VALID_FRAME_RXD_ON_CH_B_IN_SLOTS | | | 0 | N/A |
| | VALID_FRAME_RXD_ON_CH_B_IN_SLOTS | | | 1 | N/A |
| 12 | SBVB | RW1C | RW | 0 | Slot Boundary Violation on Channel B (vSS!BViolationB)<br>One or more slot boundary violations were observed on channel B at any time during the observation period (static or dynamic slots, symbol window, and NIT).<br>1 = Slot boundary violation(s) observed on channel B<br>0 = No slot boundary violation observed |
| | NO_BNDRY_VIOLATION_ERROR_IN_CH_B | | | 0 | N/A |
| | BNDRY_VIOLATION_ERROR_IN_CH_B | | | 1 | N/A |

### 15.1.46 FLEXRAY_ESID

**Description:** Even Sync ID [1...15]
**Address:** 0x40560130
**Offset:** 0x130
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** should be n=1...15
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | EID [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | RXEB [15:15] | RXEA [14:14] | None [13:10] | | | | EID [9:8] | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:9 | EID | R | RW | 0 | Even Sync ID (vsSyncIDListA,B even)<br>Sync frame ID even communication cycle. |
| 14 | RXEA | R | RW | 0 | Received / Configured Even Sync ID on Channel A<br>Signals that a sync frame corresponding to the stored even sync ID was received on channel A or<br>that the node is configured to be a sync node with key slot = EID[9:0] (ESID1 only).<br>1 = Sync frame received on channel A / node configured to transmit sync frames<br>0 = No sync frame received on channel A / node not configured to transmit sync frames |
| | NO_SYNC_FRAME_RXD_ON_CH_A | | | 0 | N/A |
| | SYNC_FRAME_RXD_ON_CH_A | | | 1 | N/A |
| 15 | RXEB | R | RW | 0 | Received / Configured Even Sync ID on Channel B<br>Signals that a sync frame corresponding to the stored even sync ID was received on channel B or<br>that the node is configured to be a sync node with key slot = EID[9:0] (ESID1 only).<br>1 = Sync frame received on channel B / node configured to transmit sync frames<br>0 = No sync frame received on channel B / node not configured to transmit sync frames |
| | NO_SYNC_FRAME_RXD_ON_CH_B | | | 0 | N/A |
| | SYNC_FRAME_RXD_ON_CH_B | | | 1 | N/A |

### 15.1.47 FLEXRAY_OSID

**Description:** Odd Sync ID [1...15]
**Address:** 0x40560170
**Offset:** 0x170
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** should be n=1...15
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | OID [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | RXOB [15:15] | RXOA [14:14] | None [13:10] | | | | OID [9:8] | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:9 | OID | R | RW | 0 | Odd Sync ID (vsSyncIDListA,B odd)<br>Sync frame ID odd communication cycle. |
| 14 | RXOA | R | RW | 0 | Received / Configured Odd Sync ID on Channel A<br>Signals that a sync frame corresponding to the stored odd sync ID was received on channel A or<br>that the node is configured to be a sync node with key slot = OID[9:0] (OSID1 only).<br>1 = Sync frame received on channel A / node configured to transmit sync frames<br>0 = No sync frame received on channel A / node not configured to transmit sync frames |
| | NO_SYNC_FRAME_RXD_ON_CH_A | | | 0 | N/A |
| | SYNC_FRAME_RXD_ON_CH_A | | | 1 | N/A |
| 15 | RXOB | R | RW | 0 | Received / Configured Odd Sync ID on Channel B<br>Signals that a sync frame corresponding to the stored odd sync ID was received on channel B or<br>that the node is configured to be a sync node with key slot = OID[9:0] (OSID1 only).<br>1 = Sync frame received on channel B / node configured to transmit sync frames<br>0 = No sync frame received on channel B / node not configured to transmit sync frames |
| | NO_SYNC_FRAME_RXD_ON_CH_B | | | 0 | N/A |
| | SYNC_FRAME_RXD_ON_CH_B | | | 1 | N/A |

### 15.1.48 FLEXRAY_NMV1

**Description:** Network Management Vector 1
**Address:** 0x405601B0
**Offset:** 0x1B0
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA0 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA1 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA2 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA3 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | DATA0 | R | RW | 0 | Data0 |
| 8:15 | DATA1 | R | RW | 0 | Data1 |
| 16:23 | DATA2 | R | RW | 0 | Data2 |
| 24:31 | DATA3 | R | RW | 0 | Data3 |

### 15.1.49 FLEXRAY_NMV2

**Description:** Network Management Vector 2
**Address:** 0x405601B4
**Offset:** 0x1B4
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA4 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA5 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA6 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA7 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | DATA4 | R | RW | 0 | Data4 |
| 8:15 | DATA5 | R | RW | 0 | Data5 |
| 16:23 | DATA6 | R | RW | 0 | Data6 |
| 24:31 | DATA7 | R | RW | 0 | Data7 |

### 15.1.50 FLEXRAY_NMV3

**Description:** Network Management Vector 3
**Address:** 0x405601B8
**Offset:** 0x1B8
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA8 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA9 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA10 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA11 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | DATA8 | R | RW | 0 | Data8 |
| 8:15 | DATA9 | R | RW | 0 | Data9 |
| 16:23 | DATA10 | R | RW | 0 | Data10 |
| 24:31 | DATA11 | R | RW | 0 | Data11 |

### 15.1.51 FLEXRAY_MRC

**Description:** Message RAM Configuration
**Address:** 0x40560300
**Offset:** 0x300
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** Protected write, see LCK register
**Default:** 0x1800000

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | FDB [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | FFB [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | LCB [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:27] | | | | | SPLM [26:26] | SEC [25:24] | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | FDB | RW | R | 0 | First Dynamic Buffer<br>0 = No group of message buffers exclusively for the static segment configured<br>1...127 = Message buffers 0 to FDB - 1 reserved for static segment<br>128 = No dynamic message buffers configured |
| | MAX | | | 128 | N/A |
| 8:15 | FFB | RW | R | 0 | First Buffer of FIFO<br>0 = All message buffers assigned to the FIFO<br>1...127 = Message buffers from FFB to LCB assigned to the FIFO<br>128 = No message buffer assigned to the FIFO |
| | MAX | | | 128 | N/A |
| 16:23 | LCB | RW | R | 128 | Last Configured Buffer<br>0...127 = Number of message buffers is LCB + 1<br>128 = No message buffer configured |
| | MAX | | | 128 | N/A |
| 24:25 | SEC | RW | R | 1 | Secure Buffers<br>Not evaluated when the CC is in DEFAULT_CONFIG or CONFIG state. For temporary unlocking see 5.12.4 Host Handling of Parity Errors.<br>00 = Reconfiguration of message buffers enabled with numbers < FFB enabled<br>Exception: In nodes configured for sync frame transmission or for single slot mode operation message buffer 0 (and if SPLM = '1', also message buffer 1) is always locked<br>01 = Reconfiguration of message buffers with numbers < FDB and with numbers >= FFB locked and transmission of message buffers for static segment with numbers >= FDB disabled<br>10 = Reconfiguration of all message buffers locked<br>11 = Reconfiguration of all message buffers locked and transmission of message buffers for static segment with numbers => FDB disabled |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| | MSG_BUFFERS_LT_FFB _ENABLED | | | 0 | N/A |
| | MSG_BUFFERS_LT_FDB _ENABLED_AND_GT _FFB_LOCKED | | | 1 | N/A |
| | ALL_MSG_BUFFERS _LOCKED | | | 2 | N/A |
| | ALL_MSG_BUFFERS _LOCKED_AND_TXMN _OF_GT_FDB_LOCKED | | | 3 | N/A |
| 26 | SPLM | RW | R | 0 | Sync Frame Payload Multiplex<br>This bit is only evaluated if the node is configured as sync node (SUCC1.TXSY = '1') or for<br>single slot mode operation (SUCC1.TSM = '1'). When this bit is set to '1' message buffers 0<br>and 1 are dedicated for sync frame transmission with different payload data on channel A and B.<br>When this bit is set to '0', sync frames are transmitted from message buffer 0 with the same payload<br>data on both channels. Note that the channel filter configuration for message buffer 0 resp.<br>message buffer 1 has to be chosen accordingly.<br>1 = Both message buffers 0 and 1 are locked against reconfiguration<br>0 = Only message buffer 0 locked against reconfiguration |
| | MSG_BUFFER_0 _LOCKED | | | 0 | N/A |
| | MSG_BUFFER_0_AND_1 _LOCKED | | | 1 | N/A |

### 15.1.52 FLEXRAY_FRF

**Description:** FIFO Rejection Filter
**Address:** 0x40560304
**Offset:** 0x304
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** Protected write, see LCK register
**Default:** 0x1800000

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | FID_ [7:2] | | | | | | CH [1:0] | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:13] | | | FID_ [12:8] | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | RSS [23:23] | CYF [22:16] | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:25] | | | | | | | RNF [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:1 | CH | RW | R | 0 | Channel Filter<br>11 = no reception<br>10 = receive only on channel A<br>01 = receive only on channel B<br>00 = receive on both channels |
| | RECEIVE_ON_BOTH_CHANNELS | | | 0 | N/A |
| | RECEIVE_ONLY_ON_CHANNEL_B | | | 1 | N/A |
| | RECEIVE_ONLY_ON_CHANNEL_A | | | 2 | N/A |
| | NO_RECEPTION | | | 3 | N/A |
| 2:12 | FID_ | RW | R | 0 | Frame ID Filter<br>Determines the frame ID to be rejected by the FIFO. With the additional configuration of register FRFM, the corresponding frame ID filter bits are ignored, which results in further rejected frame IDs. When FRFM.MFID[10:0] is zero, a frame ID filter value of zero means that no frame ID is rejected.<br>0...2047 = Frame ID filter values |
| 16:22 | CYF | RW | R | 0 | Cycle Counter Filter<br>The 7-bit cycle counter filter determines the cycle set to which frame ID and channel rejection filter are applied. In cycles not belonging to the cycle set specified by CYF[6:0], all frames are rejected. For details about the configuration of the cycle counter filter see [01]Section 5.7.2 Cycle Counter Filtering. |
| 23 | RSS | RW | R | 1 | Reject in Static Segment<br>If this bit is set, the FIFO is used only for the dynamic segment.<br>1 = Reject messages in static segment<br>0 = FIFO also used for static segment |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| | FIFO_STATIC _SEGMENT_STORAGE _ENABLED | | | 0 | N/A |
| | FIFO_STATIC _SEGMENT_STORAGE _DISABLED | | | 1 | N/A |
| 24 | RNF | RW | R | 1 | Reject Null Frames<br>If this bit is set, received null frames are not stored in the FIFO.<br>1 = Reject all null frames<br>0 = Null frames are stored in the FIFO |
| | NULL_FRAMES_FIFO _STORAGE_ENABLED | | | 0 | N/A |
| | NULL_FRAMES_FIFO _STORAGE_DISABLED | | | 1 | N/A |

### 15.1.53 FLEXRAY_FRFM

**Description:** FIFO Rejection Filter Mask
**Address:** 0x40560308
**Offset:** 0x308
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** Protected write, see LCK register
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | MFID [7:2] | | | | | | None [1:0] | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:13] | | | MFID [12:8] | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 2:12 | MFID | RW | R | 0 | Mask Frame ID Filter<br>1 = Ignore corresponding frame ID filter bit.<br>0 = Corresponding frame ID filter bit is used for rejection filtering |
| | FRAME_ID_FILTER_MASK_ENABLED | | | 0 | N/A |
| | FRAME_ID_FILTER_MASK_DISABLED | | | 1 | N/A |

### 15.1.54 FLEXRAY_FCL

**Description:** FIFO Critical Level
**Address:** 0x4056030C
**Offset:** 0x30C
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** Protected write, see LCK register
**Default:** 0x80

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | CL [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | CL | RW | R | 128 | Critical Level<br>When the receive FIFO fill level FSR.RFFL[7:0] is equal or greater than the critical level configured by CL[7:0], the receive FIFO critical level flag FSR.RFCL is set. If CL[7:0] is programmed to values > 128, bit FSR.RFCL is never set. When FSR.RFCL changes from '0' to 1' bit SIR.RFCL is set to '1', and if enabled, an interrupt is generated. |

### 15.1.55 FLEXRAY_MHDS

**Description:** Message Handler Status
**Address:** 0x40560310
**Offset:** 0x310
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x80

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | CRAM [7:7] | MFMB [6:6] | FMBD [5:5] | PTBF2 [4:4] | PTBF1 [3:3] | PMR [2:2] | POBF [1:1] | PIBF [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:15] | FMB [14:8] | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:23] | MBT [22:16] | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:31] | MBU [30:24] | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | PIBF | RW1C | RW | 0 | Parity Error Input Buffer RAM 1,2<br>1 = Parity error occurred when reading Input Buffer RAM 1,2<br>0 = No parity error |
| | NO_PARITY_ERROR | | | 0 | N/A |
| | PARITY_ERROR_IN_IBF_RAM_1_2 | | | 1 | N/A |
| 1 | POBF | RW1C | RW | 0 | Parity Error Output Buffer RAM 1,2<br>1 = Parity error occurred when reading Output Buffer RAM 1,2<br>0 = No parity error |
| | NO_PARITY_ERROR | | | 0 | N/A |
| | PARITY_ERROR_IN_OBF_RAM_1_2 | | | 1 | N/A |
| 2 | PMR | RW1C | RW | 0 | Parity Error Message RAM<br>1 = Parity error occurred when reading the Message RAM<br>0 = No parity error |
| | NO_PARITY_ERROR | | | 0 | N/A |
| | PARITY_ERROR_IN_MSG_RAM | | | 1 | N/A |
| 3 | PTBF1 | RW1C | RW | 0 | Parity Error Transient Buffer RAM A<br>1 = Parity error occurred when reading Transient Buffer RAM A<br>0 = No parity error |
| | NO_PARITY_ERROR | | | 0 | N/A |
| | PARITY_ERROR_IN_TRAN_BUF_RAM_A | | | 1 | N/A |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 4 | PTBF2 | RW1C | RW | 0 | Parity Error Transient Buffer RAM B<br>1 = Parity error occurred when reading Transient Buffer RAM B<br>0 = No parity error |
| | NO_PARITY_ERROR | | | 0 | N/A |
| | PARITY_ERROR_IN_TRAN_BUF_RAM_B | | | 1 | N/A |
| 5 | FMBD | RW1C | RW | 0 | Faulty Message Buffer Detected<br>1 = Message buffer referenced by FMB[6:0] holds faulty data due to a parity error<br>0 = No faulty message buffer |
| | NO_FAULTY_MSG_BUFFER | | | 0 | N/A |
| | FAULTY_MSG_BUFFER_ERROR | | | 1 | N/A |
| 6 | MFMB | RW1C | RW | 0 | Multiple Faulty Message Buffers detected<br>1 = Another faulty message buffer was detected while flag FMBD is set<br>0 = No additional faulty message buffer |
| | NO_ADDITIONAL_FAULTY_MSG_BUFFER | | | 0 | N/A |
| | ADDITIONAL_FAULTY_MSG_BUFFER_ERROR | | | 1 | N/A |
| 7 | CRAM | R | RW | 1 | Clear all internal RAM's<br>Signals that execution of the CHI command CLEAR_RAMS is ongoing (all bits of all internal RAM blocks are written to '0'). The bit is set by hard reset or by CHI command CLEAR_RAMS.<br>1 = Execution of the CHI command CLEAR_RAMS ongoing<br>0 = No execution of the CHI command CLEAR_RAMS |
| | CLEAR_RAMS_NOT_IN_PROGRESS | | | 0 | N/A |
| | CLEAR_RAMS_IN_PROGRESS | | | 1 | N/A |
| 8:14 | FMB | R | RW | 0 | Faulty Message Buffer<br>Parity error occurred when reading from the message buffer or when transferring data from Input Buffer or Transient Buffer 1,2 to the message buffer referenced by FMB[6:0]. Value only valid when one of the flags PIBF, PMR, PTBF1, PTBF2, and flag FMBD is set. Is not updated while flag FMBD is set. |
| 16:22 | MBT | R | RW | 0 | Message Buffer Transmitted<br>Number of last successfully transmitted message buffer. If the message buffer is configured for single-shot mode, the respective TXR flag in the TXRQ1/2/3/4 registers was reset. |
| 24:30 | MBU | R | RW | 0 | Message Buffer Updated<br>Number of message buffer that was updated last by the CC. For this message buffer the respective ND and / or MBC flag in the NDAT1/2/3/4 registers and the MBSC1/2/3/4 registers are also set. |

### 15.1.56 FLEXRAY_LDTS

**Description:** Last Dynamic Transmit Slot
**Address:** 0x40560314
**Offset:** 0x314
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | LDTA [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:11] | | | | | LDTA [10:8] | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | LDTB [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:27] | | | | | LDTB [26:24] | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:10 | LDTA | R | RW | 0 | Last Dynamic Transmission Channel A<br>Value of vSlotCounter[A] at the time of the last frame transmission on channel A in the dynamic segment of this node. It is updated at the end of the dynamic segment and is reset to zero if no frame was transmitted during the dynamic segment. |
| 16:26 | LDTB | R | RW | 0 | Last Dynamic Transmission Channel B<br>Value of vSlotCounter[B] at the time of the last frame transmission on channel B in the dynamic segment of this node. It is updated at the end of the dynamic segment and is reset to zero if no frame was transmitted during the dynamic segment. |

### 15.1.57 FLEXRAY_FSR

**Description:** FIFO Status Register
**Address:** 0x40560318
**Offset:** 0x318
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:3] | | | | | RFO_ [2:2] | RFCL_ [1:1] | RFNE_ [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | RFFL [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | RFNE_ | R | RW | 0 | Receive FIFO Not Empty<br>This flag is set by the CC when a received valid frame (data or null frame depending on rejection mask) was stored in the FIFO. In addition, interrupt flag SIR.RFNE is set. The bit is reset after the Host has read all message from the FIFO.<br>1 = Receive FIFO is not empty<br>0 = Receive FIFO is empty |
| | RX_FIFO_EMPTY | | | 0 | N/A |
| | RX_FIFO_NOT_EMPTY | | | 1 | N/A |
| 1 | RFCL_ | R | RW | 0 | Receive FIFO Critical Level<br>This flag is set when the receive FIFO fill level RFFL[7:0] is equal or greater than the critical level as configured by FCL.CL[7:0]. The flag is cleared by the CC as soon as RFFL[7:0] drops below FCL.CL[7:0]. When RFCL changes from '0' to '1' bit SIR.RFCL is set to '1', and if enabled, an interrupt is generated.<br>1 = Receive FIFO critical level reached<br>0 = Receive FIFO below critical level |
| | RX_FIFO_LT_CRITICAL_LEVEL | | | 0 | N/A |
| | RX_FIFO_CRITICAL_LEVEL | | | 1 | N/A |
| 2 | RFO_ | R | RW | 0 | Receive FIFO Overrun<br>The flag is set by the CC when a receive FIFO overrun is detected. When a receive FIFO overrun occurs, the oldest message is overwritten with the actual received message. In addition, interrupt flag EIR.RFO is set.The flag is cleared by the next FIFO read access issued by the Host.<br>1 = A receive FIFO overrun has been detected<br>0 = No receive FIFO overrun detected |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| | RX_FIFO_NO _OVERRUN | | | 0 | N/A |
| | RX_FIFO_OVERRUN | | | 1 | N/A |
| 8:15 | RFFL | R | RW | 0 | Receive FIFO Fill Level<br>Number of FIFO buffers filled with new data not yet read by the Host. Maximum value is 128. |
| | MAX | | | 128 | N/A |

### 15.1.58 FLEXRAY_MHDF

**Description:** Message Handler Constraints Flags
**Address:** 0x4056031C
**Offset:** 0x31C
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | TNSB [7:7] | TNSA [6:6] | TBFB [5:5] | TBFA [4:4] | FNFB [3:3] | FNFA [2:2] | SNUB [1:1] | SNUA [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:9] | | | | | | | WAHP [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | SNUA | RW | R | 0 | Status Not Updated Channel A<br>This flag is set by the CC when the Message Handler, due to overload condition, was not able to update a message buffer's status MBS with respect to channel A.<br>1 = MBS for channel A not updated<br>0 = No overload condition occurred when updating MBS for channel A |
| | MBS_FOR_CH_A_UPDATED | | | 0 | N/A |
| | MBS_FOR_CH_A_NOT_UPDATED | | | 1 | N/A |
| 1 | SNUB | RW | R | 0 | Status Not Updated Channel B<br>This flag is set by the CC when the Message Handler, due to overload condition, was not able to update a message buffer's status MBS with respect to channel B.<br>1 = MBS for channel B not updated<br>0 = No overload condition occurred when updating MBS for channel B |
| | MBS_FOR_CH_B_UPDATED | | | 0 | N/A |
| | MBS_FOR_CH_B_NOT_UPDATED | | | 1 | N/A |
| 2 | FNFA | RW | R | 0 | Find Sequence Not Finished Channel A<br>This flag is set by the CC when the Message Handler, due to overload condition, was not able to finish a find sequence (scan of Message RAM for matching message buffer) with respect to channel A.<br>1 = Find sequence not finished for channel A<br>0 = No find sequence not finished for channel A |
| | NO_CH_A_FIND_SEQ_NOT_FINISHED | | | 0 | N/A |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| | CH_A_FIND_SEQ_NOT_FINISHED | | | 1 | N/A |
| 3 | FNFB | RW | R | 0 | Find Sequence Not Finished Channel B<br>This flag is set by the CC when the Message Handler, due to overload condition, was not able to finish a find sequence (scan of Message RAM for matching message buffer) with respect to channel B.<br>1 = Find sequence not finished for channel B<br>0 = No find sequence not finished for channel B |
| | NO_CH_B_FIND_SEQ_NOT_FINISHED | | | 0 | N/A |
| | CH_B_FIND_SEQ_NOT_FINISHED | | | 1 | N/A |
| 4 | TBFA | RW | R | 0 | Transient Buffer Access Failure A<br>This flag is set by the CC when a read or write access to TBF A requested by PRT A could not complete within the available time.<br>1 = TBF A access failure<br>0 = No TBF A access failure |
| | TBF_CH_A_ACCESS_NOT_FAILED | | | 0 | N/A |
| | TBF_CH_A_ACCESS_FAILED | | | 1 | N/A |
| 5 | TBFB | RW | R | 0 | Transient Buffer Access Failure B<br>This flag is set by the CC when a read or write access to TBF B requested by PRT B could not complete within the available time.<br>1 = TBF B access failure<br>0 = No TBF B access failure |
| | TBF_CH_B_ACCESS_NOT_FAILED | | | 0 | N/A |
| | TBF_CH_B_ACCESS_FAILED | | | 1 | N/A |
| 6 | TNSA | RW | R | 0 | Transmission Not Started Channel A<br>This flag is set by the CC when the Message Handler was not ready to start a scheduled transmission on channel A at the action point of the configured slot.<br>1 = Transmission not started on channel A<br>0 = No transmission not started on channel A |
| | NO_CH_A_TXMN_NOT_STARTED | | | 0 | N/A |
| | CH_A_TXMN_NOT_STARTED | | | 1 | N/A |
| 7 | TNSB | RW | R | 0 | Transmission Not Started Channel B<br>This flag is set by the CC when the Message Handler was not ready to start a scheduled transmission on channel B at the action point of the configured slot.<br>1 = Transmission not started on channel B<br>0 = No transmission not started on channel B |
| | NO_CH_B_TXMN_NOT_STARTED | | | 0 | N/A |
| | CH_B_TXMN_NOT_STARTED | | | 1 | N/A |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 8 | WAHP | RW | R | 0 | Write Attempt to Header Partition<br>Outside DEFAULT_CONFIG and CONFIG state this flag is set by the CC when the message handler tries to write message data into the header partition of the Message RAM due to faulty configuration of a message buffer. The write attempt is not executed, to protect the header partition from unintended write accesses.<br>1 = Write attempt to header partition<br>0 = No write attempt to header partition |
| | HEADER_PARTITION_NO_WRITE | | | 0 | N/A |
| | HEADER_PARTITION_WRITE | | | 1 | N/A |

### 15.1.59 FLEXRAY_TXRQ1

**Description:** Transmission Request 1
**Address:** 0x40560320
**Offset:** 0x320
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | TXR [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | TXR [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | TXR [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | TXR [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | TXR | R | RW | 0 | Transmission Request<br>TRX[31:0]<br>If the flag is set, the respective message buffer is ready for transmission respectively transmission of this message buffer is in progress. In single-shot mode the flags are reset after transmission has completed. |

### 15.1.60 FLEXRAY_TXRQ2

**Description:** Transmission Request 2
**Address:** 0x40560324
**Offset:** 0x324
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | TXR [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | TXR [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | TXR [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | TXR [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | TXR | R | RW | 0 | Transmission Request<br>TRX[63:32]<br>If the flag is set, the respective message buffer is ready for transmission respectively transmission of this message buffer is in progress. In single-shot mode the flags are reset after transmission has completed. |

### 15.1.61 FLEXRAY_TXRQ3

**Description:** Transmission Request 3
**Address:** 0x40560328
**Offset:** 0x328
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | TXR [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | TXR [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | TXR [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | TXR [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | TXR | R | RW | 0 | Transmission Request<br>TRX[95:64]<br>If the flag is set, the respective message buffer is ready for transmission respectively transmission of this message buffer is in progress. In single-shot mode the flags are reset after transmission has completed. |

### 15.1.62 FLEXRAY_TXRQ4

**Description:** Transmission Request 4
**Address:** 0x4056032C
**Offset:** 0x32C
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | TXR [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | TXR [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | TXR [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | TXR [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | TXR | R | RW | 0 | Transmission Request<br>TRX[127:96]<br>If the flag is set, the respective message buffer is ready for transmission respectively transmission of this message buffer is in progress. In single-shot mode the flags are reset after transmission has completed. |

### 15.1.63 FLEXRAY_NDAT1

**Description:** New Data 1
**Address:** 0x40560330
**Offset:** 0x330
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | ND [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | ND [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | ND [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | ND [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | ND | R | RW | 0 | New Data<br>ND[31:0]<br>The flags are set when a valid received data frame matches the message buffer's filter configuration, independent of the payload length received or the payload length configured for that message buffer. The flags are not set after reception of null frames except for message buffers belonging to the receive FIFO. An ND flag is reset when the header section of the corresponding message buffer is reconfigured or when the data section has been transferred to the Output Buffer. |

### 15.1.64 FLEXRAY_NDAT2

**Description:** New Data 2
**Address:** 0x40560334
**Offset:** 0x334
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | ND [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | ND [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | ND [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | ND [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | ND | R | RW | 0 | New Data<br>ND[63:32]<br>The flags are set when a valid received data frame matches the message buffer's filter configuration, independent of the payload length received or the payload length configured for that message buffer. The flags are not set after reception of null frames except for message buffers belonging to the receive FIFO. An ND flag is reset when the header section of the corresponding message buffer is reconfigured or when the data section has been transferred to the Output Buffer. |

### 15.1.65 FLEXRAY_NDAT3

**Description:** New Data 3
**Address:** 0x40560338
**Offset:** 0x338
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | ND [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | ND [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | ND [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | ND [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | ND | R | RW | 0 | New Data<br>ND[95:64]<br>The flags are set when a valid received data frame matches the message buffer's filter configuration, independent of the payload length received or the payload length configured for that message buffer. The flags are not set after reception of null frames except for message buffers belonging to the receive FIFO. An ND flag is reset when the header section of the corresponding message buffer is reconfigured or when the data section has been transferred to the Output Buffer. |

### 15.1.66 FLEXRAY_NDAT4

**Description:** New Data 4
**Address:** 0x4056033C
**Offset:** 0x33C
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | ND [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | ND [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | ND [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | ND [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | ND | R | RW | 0 | New Data<br>ND[127:96]<br>The flags are set when a valid received data frame matches the message buffer's filter configuration, independent of the payload length received or the payload length configured for that message buffer. The flags are not set after reception of null frames except for message buffers belonging to the receive FIFO. An ND flag is reset when the header section of the corresponding message buffer is reconfigured or when the data section has been transferred to the Output Buffer. |

### 15.1.67 FLEXRAY_MBSC1

**Description:** Message Buffer Status Changed 1
**Address:** 0x40560340
**Offset:** 0x340
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | MBC [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | MBC [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | MBC [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | MBC [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | MBC | R | RW | 0 | Message Buffer Status Changed<br>MBC[31:0]<br>An MBC flag is set whenever the Message Handler changes one of the status flags VFRA,<br>VFRB, SEOA, SEOB, CEOA, CEOB, SVOA, SVOB,<br>TCIA, TCIB, ESA, ESB, MLST,<br>FTA, FTB in the header section (see 4.11.5 Message Buffer Status (MBS) and 5.12.1 Header<br>Partition, header 4) of the respective message buffer.<br>An MBC flag is reset when the header section<br>of the corresponding message buffer is reconfigured or<br>when it has been transferred to the<br>Output Buffer. |

### 15.1.68 FLEXRAY_MBSC2

**Description:** Message Buffer Status Changed 2
**Address:** 0x40560344
**Offset:** 0x344
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | MBC [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | MBC [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | MBC [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | MBC [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | MBC | R | RW | 0 | Message Buffer Status Changed<br>MBC[63:32]<br>An MBC flag is set whenever the Message Handler changes one of the status flags VFRA,<br>VFRB, SEOA, SEOB, CEOA, CEOB, SVOA, SVOB,<br>TCIA, TCIB, ESA, ESB, MLST,<br>FTA, FTB in the header section (see 4.11.5 Message Buffer Status (MBS) and 5.12.1 Header<br>Partition, header 4) of the respective message buffer.<br>An MBC flag is reset when the header section<br>of the corresponding message buffer is reconfigured or<br>when it has been transferred to the<br>Output Buffer. |

### 15.1.69 FLEXRAY_MBSC3

**Description:** Message Buffer Status Changed 3
**Address:** 0x40560348
**Offset:** 0x348
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | MBC [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | MBC [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | MBC [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | MBC [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | MBC | R | RW | 0 | Message Buffer Status Changed<br>MBC[95:64]<br>An MBC flag is set whenever the Message Handler changes one of the status flags VFRA,<br>VFRB, SEOA, SEOB, CEOA, CEOB, SVOA, SVOB,<br>TCIA, TCIB, ESA, ESB, MLST,<br>FTA, FTB in the header section (see 4.11.5 Message Buffer Status (MBS) and 5.12.1 Header<br>Partition, header 4) of the respective message buffer.<br>An MBC flag is reset when the header section<br>of the corresponding message buffer is reconfigured or<br>when it has been transferred to the<br>Output Buffer. |

### 15.1.70 FLEXRAY_MBSC4

**Description:** Message Buffer Status Changed 4
**Address:** 0x4056034C
**Offset:** 0x34C
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | MBC [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | MBC [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | MBC [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | MBC [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | MBC | R | RW | 0 | Message Buffer Status Changed<br>MBC[127:96]<br>An MBC flag is set whenever the Message Handler changes one of the status flags VFRA,<br>VFRB, SEOA, SEOB, CEOA, CEOB, SVOA, SVOB,<br>TCIA, TCIB, ESA, ESB, MLST,<br>FTA, FTB in the header section (see 4.11.5 Message Buffer Status (MBS) and 5.12.1 Header<br>Partition, header 4) of the respective message buffer.<br>An MBC flag is reset when the header section<br>of the corresponding message buffer is reconfigured or<br>when it has been transferred to the<br>Output Buffer. |

### 15.1.71 FLEXRAY_CREL

**Description:** Core Release Register
**Address:** 0x405603F0
**Offset:** 0x3F0
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x10390206

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DAY [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | MON [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | STEP [23:20] | | | | YEAR [19:16] | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | REL [31:28] | | | | STEP [27:24] | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | DAY | R | R | 06 | Design Time Stamp, Day<br>Two digits, BCD-coded. |
| 8:15 | MON | R | R | 02 | Design Time Stamp, Month<br>Two digits, BCD-coded. |
| 16:19 | YEAR | R | R | 9 | Design Time Stamp, Year<br>One digit, BCD-coded. |
| 20:27 | STEP | R | R | 03 | Step of Core Release<br>Two digits, BCD-coded. |
| 28:31 | REL | R | R | 1 | Core Release<br>One digit, BCD-coded.<br>Table 5: Coding for releases |

### 15.1.72 FLEXRAY_ENDN

**Description:** Endian Register
**Address:** 0x405603F4
**Offset:** 0x3F4
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x87654321

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | ETV [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | ETV [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | ETV [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | ETV [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | ETV | R | R | 2271560481 | Endianness Test Value<br>The endianness test value is 0x87654321. |

### 15.1.73 FLEXRAY_WRDS

**Description:** Write Data Section [1...64]
**Address:** 0x40560400
**Offset:** 0x400
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** should be n=1...64
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | MD [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | MD [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | MD [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | MD [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | MD | RW | R | 0 | Message Data<br>MD[7:0] = DW2n-1, byte4n-4<br>MD[15:8] = DW2n-1, byte4n-3<br>MD[23:16] = DW2n, byte4n-2<br>MD[31:24] = DW2n, byte4n-1 |

### 15.1.74 FLEXRAY_WRHS1

**Description:** Write Header Section 1
**Address:** 0x40560500
**Offset:** 0x500
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | FID [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:11] | | | | | FID [10:8] | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:23] | CYC [22:16] | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:30] | | MBI [29:29] | TXM [28:28] | PPIT [27:27] | CFG [26:26] | CHB [25:25] | CHA [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:10 | FID | RW | R | 0 | Frame ID<br>Frame ID of the selected message buffer. The frame ID defines the slot number for transmission reception of the respective message. Message buffers with frame ID = '0' are considered as not valid. |
| 16:22 | CYC | RW | R | 0 | Cycle Code<br>The 7-bit cycle code determines the cycle set used for cycle counter filtering. For details about the configuration of the cycle code see [01]Section 5.7.2 Cycle Counter Filtering.<br>CHA, CHB Channel Filter Control<br>The 2-bit channel filtering field associated with each buffer serves as a filter for receive buffers, and as a control field for transmit buffers.<br>CHA CHB.<br>Transmit Buffer<br>transmit frame on<br>Receive Buffer<br>store frame received from<br>1 1 both channels<br>static segment only)<br>channel A or B<br>store first semantically valid frame,<br>static segment only)<br>1 0 channel A channel A<br>0 1 channel B channel B<br>0 0 no transmission ignore frame |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 24 | CHA | RW | R | 0 | Channel Filter Control A<br>The 2-bit channel filtering field associated with each buffer serves as a filter for receive buffers, and as a control field for transmit buffers.<br><br>Note: If a message buffer is configured for the dynamic segment and both bits of the channel filtering field are set to '1', no frames are transmitted resp. received frames are ignored (same function as CHA = CHB = '0') |
| | CH_A_DISABLED | | | 0 | N/A |
| | CH_A_ENABLED | | | 1 | N/A |
| 25 | CHB | RW | R | 0 | Channel Filter Control B<br>The 2-bit channel filtering field associated with each buffer serves as a filter for receive buffers, and as a control field for transmit buffers.<br><br>Note: If a message buffer is configured for the dynamic segment and both bits of the channel filtering field are set to '1', no frames are transmitted resp. received frames are ignored (same function as CHA = CHB = '0') |
| | CH_B_DISABLED | | | 0 | N/A |
| | CH_B_ENABLED | | | 1 | N/A |
| 26 | CFG | RW | R | 0 | Message Buffer Direction Configuration Bit<br>This bit is used to configure the corresponding buffer as transmit buffer or as receive buffer. For message buffers belonging to the receive FIFO the bit is not evaluated.<br>1 = The corresponding buffer is configured as Transmit Buffer<br>0 = The corresponding buffer is configured as Receive Buffer |
| | RX_BUFF | | | 0 | N/A |
| | TX_BUFF | | | 1 | N/A |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 27 | PPIT | RW | R | 0 | Payload Preamble Indicator Transmit<br>This bit is used to control the state of the Payload Preamble Indicator in transmit frames. If the bit is set in a static message buffer, the respective message buffer holds network management information. If the bit is set in a dynamic message buffer the first two bytes of the payload segment may be used for message ID filtering by the receiver. Message ID filtering of received FlexRay frames is not supported by the E-Ray module, but can be done by the Host.<br>1 = Payload Preamble Indicator set<br>0 = Payload Preamble Indicator not set |
| | PAYLOAD_PREAMBLE_NOT_SET | | | 0 | N/A |
| | PAYLOAD_PREAMBLE_SET | | | 1 | N/A |
| 28 | TXM | RW | R | 0 | Transmission Mode<br>This bit is used to select the transmission mode (see [01]Section 5.8.3 Transmit Buffers).<br>1 = Single-shot mode<br>0 = Continuous mode |
| | CONTINUOUS_MODE | | | 0 | N/A |
| | SINGLE_SHOT_MODE | | | 1 | N/A |
| 29 | MBI | RW | R | 0 | Message Buffer Interrupt<br>This bit enables the receive / transmit interrupt for the corresponding message buffer. After a dedicated receive buffer has been updated by the Message Handler, flag SIR.RXI and /or SIR.MBSI are set. After a transmission has completed flag SIR.TXI is set.<br>1 = The corresponding message buffer interrupt is enabled<br>0 = The corresponding message buffer interrupt is disabled |
| | MSG_BUFF_INTR_DISABLED | | | 0 | N/A |
| | MSG_BUFF_INTR_ENABLED | | | 1 | N/A |

### 15.1.75 FLEXRAY_WRHS2

**Description:** Write Header Section 2
**Address:** 0x40560504
**Offset:** 0x504
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | CRC [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:11] | | | | | CRC [10:8] | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:23] | PLC [22:16] | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:10 | CRC | RW | R | 0 | Header CRC (vRF!Header!HeaderCRC)<br>Receive Buffer: Configuration not required<br>Transmit Buffer: Header CRC calculated and configured by the Host<br>For calculation of the header CRC the payload length of the frame send on the bus has to be considered. In static segment the payload length of all frames is configured by MHDC.SFDL[6:0]. |
| 16:22 | PLC | RW | R | 0 | Payload Length Configured<br>Length of data section (number of 2-byte words) as configured by the Host. During static segment the static frame payload length as configured by MHDC.SFDL[6:0] defines the payload length for all static frames. If the payload length configured by PLC[6:0] is shorter than this value padding bytes are inserted to ensure that frames have proper physical length. The padding pattern is logical zero (see also Section 5.8.3 Transmit Buffers). |

### 15.1.76 FLEXRAY_WRHS3

**Description:** Write Header Section 3
**Address:** 0x40560508
**Offset:** 0x508
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DP [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:11] | | | | | DP [10:8] | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:10 | DP | RW | R | 0 | Data Pointer<br>Pointer to the first 32-bit word of the data section of the addressed message buffer in the Message RAM. |

### 15.1.77 FLEXRAY_IBCM

**Description:** Input Buffer Command Mask
**Address:** 0x40560510
**Offset:** 0x510
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:3] | | | | | STXRH [2:2] | LDSH [1:1] | LHSH [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:19] | | | | | STXRS [18:18] | LDSS [17:17] | LHSS [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | LHSH | RW | R | 0 | Load Header Section Host<br>1 = Header section selected for transfer from Input Buffer to the Message RAM<br>0 = Header section is not updated |
| | HEADER_SECTION_NOT_UPDATED | | | 0 | N/A |
| | HEADER_SECTION_UPDATED | | | 1 | N/A |
| 1 | LDSH | RW | R | 0 | Load Data Section Host<br>1 = Data section selected for transfer from Input Buffer to the Message RAM<br>0 = Data section is not updated |
| | DATA_SECTION_NOT_UPDATED | | | 0 | N/A |
| | DATA_SECTION_UPDATED | | | 1 | N/A |
| 2 | STXRH | RW | R | 0 | Set Transmission Request Host<br>If this bit is set to '1', the TXR flag for the selected message buffer is set in the TXRQ1/2/3/4 registers to release the message buffer for transmission. In single-shot mode the flag is cleared by the CC after transmission has completed. TXR is evaluated for transmit buffers only.<br>1 = Set TXR flag, transmit buffer released for transmission<br>0 = Reset TXR flag |
| | TXR_FLAG_RESET | | | 0 | N/A |
| | TXR_FLAG_SET | | | 1 | N/A |
| 16 | LHSS | R | RW | 0 | Load Header Section Shadow<br>1 = Header section selected for transfer from Input Buffer to the Message RAM<br>transfer ongoing or finished)<br>0 = Header section is not updated |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| | HEADER_SECTION_NOT_UPDATED | | | 0 | N/A |
| | HEADER_SECTION_UPDATED | | | 1 | N/A |
| 17 | LDSS | R | RW | 0 | Load Data Section Shadow<br>1 = Data section selected for transfer from Input Buffer to the Message RAM<br>transfer ongoing or finished)<br>0 = Data section is not updated |
| | DATA_SECTION_NOT_UPDATED | | | 0 | N/A |
| | DATA_SECTION_UPDATED | | | 1 | N/A |
| 18 | STXRS | R | RW | 0 | Set Transmission Request Shadow<br>1 = Set TXR flag, transmit buffer released for transmission (operation ongoing or finished)<br>0 = Reset TXR flag |
| | TXR_FLAG_RESET | | | 0 | N/A |
| | TXR_FLAG_SET | | | 1 | N/A |

### 15.1.78 FLEXRAY_IBCR

**Description:** Input Buffer Command Request
**Address:** 0x40560514
**Offset:** 0x514
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:7] | IBRH [6:0] | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | IBSYH [15:15] | None [14:8] | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:23] | IBRS [22:16] | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | IBSYS [31:31] | None [30:24] | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:6 | IBRH | RW | R | 0 | Input Buffer Request Host<br>Selects the target message buffer in the Message RAM for data transfer from Input Buffer.<br>Valid values are 0x00 to 0x7F (0...127). |
| 15 | IBSYH | R | RW | 0 | Input Buffer Busy Host<br>Set to '1' by writing IBRH[6:0] while IBSYS is still '1'. After the ongoing transfer between<br>IBF Shadow and the Message RAM has completed, the IBSYH is set back to '0'.<br>1 = Request while transfer between IBF Shadow and Message RAM in progress<br>0 = No request pending |
| | REQUEST_NOT_PENDING | | | 0 | N/A |
| | REQUEST_IN_PROGRESS | | | 1 | N/A |
| 16:22 | IBRS | R | RW | 0 | Input Buffer Request Shadow<br>Number of the target message buffer actually updated / lately updated.<br>Valid values are 0x00 to 0x7F (0...127). |
| 31 | IBSYS | R | RW | 0 | Input Buffer Busy Shadow<br>Set to '1' after writing IBRH[6:0]. When the transfer between IBF Shadow and the Message<br>RAM has completed, IBSYS is set back to '0'.<br>1 = Transfer between IBF Shadow and Message RAM in progress<br>0 = Transfer between IBF Shadow and Message RAM completed |
| | TXFR_IBF2MSRAM_COMPLETE | | | 0 | N/A |
| | TXFR_IBF2MSRAM_IN_PROGRESS | | | 1 | N/A |

### 15.1.79 FLEXRAY_RDDS

**Description:** Read Data Section [1...64]
**Address:** 0x40560600
**Offset:** 0x600
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** should be n=1...64
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | MD [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | MD [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | MD [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | MD [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | MD | R | RW | 0 | Message Data<br>MD[7:0] = DW2n-1, byte4n-4<br>MD[15:8] = DW2n-1, byte4n-3<br>MD[23:16] = DW2n, byte4n-2<br>MD[31:24] = DW2n, byte4n-1 |

### 15.1.80 FLEXRAY_RDHS1

**Description:** Read Header Section 1
**Address:** 0x40560700
**Offset:** 0x700
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | FID [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:11] | | | | | FID [10:8] | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:23] | CYC [22:16] | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:30] | | MBI [29:29] | TXM [28:28] | PPIT [27:27] | CFG [26:26] | CHB [25:25] | CHA [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:10 | FID | R | RW | 0 | Frame ID |
| 16:22 | CYC | R | RW | 0 | Cycle Code |
| 24 | CHA | R | RW | 0 | Channel Filter Control A |
| 25 | CHB | R | RW | 0 | Channel Filter Control B |
| 26 | CFG | R | RW | 0 | Message Buffer Direction Configuration Bit |
| 27 | PPIT | R | RW | 0 | Payload Preamble Indicator Transmit |
| 28 | TXM | R | RW | 0 | Transmission Mode |
| 29 | MBI | R | RW | 0 | Message Buffer Interrupt |

### 15.1.81 FLEXRAY_RDHS2

**Description:** Read Header Section 2
**Address:** 0x40560704
**Offset:** 0x704
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | CRC [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:11] | | | | | CRC [10:8] | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:23] | PLC [22:16] | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:31] | PLR [30:24] | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:10 | CRC | R | RW | 0 | Header CRC (vRF!Header!HeaderCRC)<br>Receive Buffer: Header CRC updated from received data frames<br>Transmit Buffer: Header CRC calculated and configured by the Host |
| 16:22 | PLC | R | RW | 0 | Payload Length Configured<br>Length of data section (number of 2-byte words) as configured by the Host. |
| 24:30 | PLR | R | RW | 0 | Payload Length Received (vRF!Header!Length)<br>Payload length value updated from received data frames (exception: if message buffer belongs to the receive FIFO PLR[6:0] is also updated from received null frames)<br>When a message is stored into a message buffer the following behaviour with respect to payload length received and payload length configured is implemented:<br>PLR[6:0] > PLC[6:0]: The payload data stored in the message buffer is truncated to the payload length configured if PLC[6:0] even or else truncated to PLC[6:0] + 1.<br>PLR[6:0] <= PLC[6:0]: The received payload data is stored into the message buffers data section. The remaining data bytes of the data section as configured by PLC[6:0] are filled with undefined data<br>PLR[6:0] = zero: The message buffer's data section is filled with undefined data<br>PLC[6:0] = zero: Message buffer has no data section configured. No data is stored into the message buffer's data section. |

### 15.1.82 FLEXRAY_RDHS3

**Description:** Read Header Section 3
**Address:** 0x40560708
**Offset:** 0x708
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DP [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:11] | | | | | DP [10:8] | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:22] | | RCC [21:16] | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:30] | | RES [29:29] | PPI [28:28] | NFI [27:27] | SYN [26:26] | SFI [25:25] | RCI [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:10 | DP | R | RW | 0 | Data Pointer<br>Pointer to the first 32-bit word of the data section of the addressed message buffer in the Message RAM. |
| 16:21 | RCC | R | RW | 0 | Receive Cycle Count (vRF!Header!CycleCount)<br>Cycle counter value updated from received data frame. |
| 24 | RCI | R | RW | 0 | Received on Channel Indicator (vSS!Channel)<br>Indicates the channel from which the received data frame was taken to update the respective receive buffer.<br>1 = Frame received on channel A<br>0 = Frame received on channel B |
| | CH_B_FRAME_RECEIVED | | | 0 | N/A |
| | CH_A_FRAME_RECEIVED | | | 1 | N/A |
| 25 | SFI | R | RW | 0 | Startup Frame Indicator (vRF!Header!SuFIndicator)<br>A startup frame is marked by the startup frame indicator.<br>1 = The received frame is a startup frame<br>0 = The received frame is not a startup frame |
| | RXD_FRAME_NOT_STARTUP_FRAME | | | 0 | N/A |
| | RXD_FRAME_STARTUP_FRAME | | | 1 | N/A |
| 26 | SYN | R | RW | 0 | Sync Frame Indicator (vRF!Header!SyFIndicator)<br>A sync frame is marked by the sync frame indicator.<br>1 = The received frame is a sync frame<br>0 = The received frame is not a sync frame |
| | RXD_FRAME_NOT_SYNC_FRAME | | | 0 | N/A |
| | RXD_FRAME_SYNC_FRAME | | | 1 | N/A |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 27 | NFI | R | RW | 0 | Null Frame Indicator (vRF!Header!NFIndicator)<br>Is set to '1' after storage of the first received data frame.<br>1 = At least one data frame has been stored into the respective message buffer<br>0 = Up to now no data frame has been stored into the respective message buffer |
| | DATA_FRAME_NOT_STORED | | | 0 | N/A |
| | DATA_FRAME_STORED | | | 1 | N/A |
| 28 | PPI | R | RW | 0 | Payload Preamble Indicator (vRF!Header!PPIndicator)<br>The payload preamble indicator defines whether a network management vector or message ID is contained within the payload segment of the received frame.<br>1 = Static segment: Network management vector in the first part of the payload<br>Dynamic segment:Message ID in the first part of the payload<br>0 = The payload segment of the received frame does not contain a network management vector<br>nor a message ID |
| | PAYLOAD_SEGMENT_HAS_NO_NMV_MID | | | 0 | N/A |
| | PAYLOAD_SEGMENT_WITH_NMV_MID | | | 1 | N/A |
| 29 | RES | R | RW | 0 | Reserved Bit (vRF!Header!Reserved)<br>Reflects the state of the received reserved bit. The reserved bit is transmitted as '0'. |

### 15.1.83 FLEXRAY_MBS

**Description:** Message Buffer Status
**Address:** 0x4056070C
**Offset:** 0x70C
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | SVOB [7:7] | SVOA [6:6] | CEOB [5:5] | CEOA [4:4] | SEOB [3:3] | SEOA [2:2] | VFRB [1:1] | VFRA [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | FTB [15:15] | FTA [14:14] | None [13:13] | MLST [12:12] | ESB [11:11] | ESA [10:10] | TCIB [9:9] | TCIA [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:22] | | CCS [21:16] | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:30] | | RESS [29:29] | PPIS [28:28] | NFIS [27:27] | SYNS [26:26] | SFIS [25:25] | RCIS [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | VFRA | R | RW | 0 | Valid Frame Received on Channel A (vSS!ValidFrameA)<br>A valid frame indication is set if a valid frame was received on channel A.<br>1 = Valid frame received on channel A<br>0 = No valid frame received on channel A |
| | CH_A_NO_VALID_FRAME | | | 0 | N/A |
| | CH_A_WITH_VALID_FRAME | | | 1 | N/A |
| 1 | VFRB | R | RW | 0 | Valid Frame Received on Channel B (vSS!ValidFrameB)<br>A valid frame indication is set if a valid frame was received on channel B.<br>1 = Valid frame received on channel B<br>0 = No valid frame received on channel B |
| | CH_B_NO_VALID_FRAME | | | 0 | N/A |
| | CH_B_WITH_VALID_FRAME | | | 1 | N/A |
| 2 | SEOA | R | RW | 0 | Syntax Error Observed on Channel A (vSS!SyntaxErrorA)<br>A syntax error was observed in the assigned slot on channel A.<br>1 = Syntax error observed on channel A<br>0 = No syntax error observed on channel A |
| | CH_A_NO_SYNTAX_ERROR | | | 0 | N/A |
| | CH_A_HAS_SYNTAX_ERROR | | | 1 | N/A |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 3 | SEOB | R | RW | 0 | Syntax Error Observed on Channel B (vSS!SyntaxErrorB)<br>A syntax error was observed in the assigned slot on channel B.<br>1 = Syntax error observed on channel B<br>0 = No syntax error observed on channel B |
| | CH_B_NO_SYNTAX_ERROR | | | 0 | N/A |
| | CH_B_HAS_SYNTAX_ERROR | | | 1 | N/A |
| 4 | CEOA | R | RW | 0 | Content Error Observed on Channel A (vSS!ContentErrorA)<br>A content error was observed in the assigned slot on channel A.<br>1 = Content error observed on channel A<br>0 = No content error observed on channel A |
| | CH_A_NO_CONTENT_ERROR | | | 0 | N/A |
| | CH_A_HAS_CONTENT_ERROR | | | 1 | N/A |
| 5 | CEOB | R | RW | 0 | Content Error Observed on Channel B (vSS!ContentErrorB)<br>A content error was observed in the assigned slot on channel B.<br>1 = Content error observed on channel B<br>0 = No content error observed on channel B |
| | CH_B_NO_CONTENT_ERROR | | | 0 | N/A |
| | CH_B_HAS_CONTENT_ERROR | | | 1 | N/A |
| 6 | SVOA | R | RW | 0 | Slot Boundary Violation Observed on Channel A (vSS!BViolationA)<br>A slot boundary violation (channel active at the start or at the end of the assigned slot) was observed on channel A.<br>1 = Slot boundary violation observed on channel A<br>0 = No slot boundary violation observed on channel A |
| | CH_A_NO_SLOT_BNDRY_VIOLATION | | | 0 | N/A |
| | CH_A_HAS_SLOT_BNDRY_VIOLATION | | | 1 | N/A |
| 7 | SVOB | R | RW | 0 | Slot Boundary Violation Observed on Channel B (vSS!BViolationB)<br>A slot boundary violation (channel active at the start or at the end of the assigned slot) was observed on channel B.<br>1 = Slot boundary violation observed on channel B<br>0 = No slot boundary violation observed on channel B |
| | CH_B_NO_SLOT_BNDRY_VIOLATION | | | 0 | N/A |
| | CH_B_HAS_SLOT_BNDRY_VIOLATION | | | 1 | N/A |
| 8 | TCIA | R | RW | 0 | Transmission Conflict Indication Channel A (vSS!TxConflictA)<br>A transmission conflict indication is set if a transmission conflict has occurred on channel A.<br>1 = Transmission conflict occurred on channel A<br>0 = No transmission conflict occurred on channel A |
| | CH_A_NO_TXMN_CONFLICT | | | 0 | N/A |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| | CH_A_HAS_TXMN _CONFLICT | | | 1 | N/A |
| 9 | TCIB | R | RW | 0 | Transmission Conflict Indication Channel B (vSS!TxConflictB)<br>A transmission conflict indication is set if a transmission conflict has occurred on channel B.<br>1 = Transmission conflict occurred on channel B<br>0 = No transmission conflict occurred on channel B |
| | CH_B_NO_TXMN _CONFLICT | | | 0 | N/A |
| | CH_B_HAS_TXMN _CONFLICT | | | 1 | N/A |
| 10 | ESA | R | RW | 0 | Empty Slot Channel A<br>In an empty slot there is no activity detected on the bus. The condition is checked in static and dynamic slots.<br>1 = No bus activity detected in the assigned slot on channel A<br>0 = Bus activity detected in the assigned slot on channel A |
| | CH_A_HAS_BUS_ACTIVI TY | | | 0 | N/A |
| | CH_A_NO_BUS_ACTIVIT Y | | | 1 | N/A |
| 11 | ESB | R | RW | 0 | Empty Slot Channel B<br>In an empty slot there is no activity detected on the bus. The condition is checked in static and dynamic slots.<br>1 = No bus activity detected in the assigned slot on channel B<br>0 = Bus activity detected in the assigned slot on channel B |
| | CH_B_HAS_BUS_ACTIVI TY | | | 0 | N/A |
| | CH_B_NO_BUS_ACTIVIT Y | | | 1 | N/A |
| 12 | MLST | R | RW | 0 | Message Lost<br>The flag is set in case the Host did not read the message before the message buffer was updated from a received data frame. Not affected by reception of null frames except for message buffers belonging to the receive FIFO. The flag is reset by a Host write to the message buffer via IBF or when a new message is stored into the message buffer after the message buffers ND flag was reset by reading out the message buffer via OBF.<br>1 = Unprocessed message was overwritten<br>0 = No message lost |
| | NO_MSG_LOST | | | 0 | N/A |
| | MSG_LOST | | | 1 | N/A |
| 14 | FTA | R | RW | 0 | Frame Transmitted on Channel A<br>Indicates that this node has transmitted a data frame in the configured slot on channel A.<br>1 = Data frame transmitted on channel A<br>0 = No data frame transmitted on channel A |
| | DATA_FRAME_NOT _TXD_ON_CH_A | | | 0 | N/A |
| | DATA_FRAME_TXD_ON _CH_A | | | 1 | N/A |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 15 | FTB | R | RW | 0 | Frame Transmitted on Channel B<br>Indicates that this node has transmitted a data frame in the configured slot on channel B.<br>1 = Data frame transmitted on channel B<br>0 = No data frame transmitted on channel B |
| | DATA_FRAME_NOT_TXD_ON_CH_B | | | 0 | N/A |
| | DATA_FRAME_TXD_ON_CH_B | | | 1 | N/A |
| 16:21 | CCS | R | RW | 0 | Cycle Count Status<br>Actual cycle count when status was updated.<br>For receive buffers (CFG = '0') the following status bits are updated from both valid data and null frames. If no valid frame was received, the previous value is maintained. For transmit buffers the flags have no meaning and should be ignored. |
| 24 | RCIS | R | RW | 0 | Received on Channel Indicator Status (vSS!Channel)<br>Indicates the channel on which the frame was received.<br>1 = Frame received on channel A<br>0 = Frame received on channel B |
| | CH_B_FRAME_RECEIVED | | | 0 | N/A |
| | CH_A_FRAME_RECEIVED | | | 1 | N/A |
| 25 | SFIS | R | RW | 0 | Startup Frame Indicator Status (vRF!Header!SuFIndicator)<br>A startup frame is marked by the startup frame indicator.<br>1 = The received frame is a startup frame<br>0 = No startup frame received |
| | NO_STARTUP_FRAME_RECEIVED | | | 0 | N/A |
| | STARTUP_FRAME_RECEIVED | | | 1 | N/A |
| 26 | SYNS | R | RW | 0 | Sync Frame Indicator Status (vRF!Header!SyFIndicator)<br>A sync frame is marked by the sync frame indicator.<br>1 = The received frame is a sync frame<br>0 = No sync frame received |
| | NO_SYNC_FRAME_RECEIVED | | | 0 | N/A |
| | SYNC_FRAME_RECEIVED | | | 1 | N/A |
| 27 | NFIS | R | RW | 0 | Null Frame Indicator Status (vRF!Header!NFIndicator)<br>If set to '0' the payload segment of the received frame contains no usable data.<br>1 = Received frame is not a null frame<br>0 = Received frame is a null frame |
| | NULL_FRAME_RECEIVED | | | 0 | N/A |
| | NO_NULL_FRAME_RECEIVED | | | 1 | N/A |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 28 | PPIS | R | RW | 0 | Payload Preamble Indicator Status (vRF!Header!PPIndicator)<br>The payload preamble indicator defines whether a network management vector or message ID is contained within the payload segment of the received frame.<br>1 = Static segment: Network management vector at the beginning of the payload<br>Dynamic segment: Message ID at the beginning of the payload<br>0 = The payload segment of the received frame does not contain a network management vector<br>or a message ID |
| | PAYLOAD_SEGMENT_HAS_NO_NMV_MID | | | 0 | N/A |
| | PAYLOAD_SEGMENT_WITH_NMV_MID | | | 1 | N/A |
| 29 | RESS | R | RW | 0 | Reserved Bit Status (vRF!Header!Reserved)<br>Reflects the state of the received reserved bit. The reserved bit is transmitted as '0'. |

### 15.1.84 FLEXRAY_OBCM

**Description:** Output Buffer Command Mask
**Address:** 0x40560710
**Offset:** 0x710
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:2] | | | | | | RDSS [1:1] | RHSS [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:18] | | | | | | RDSH [17:17] | RHSH [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | RHSS | RW | R | 0 | Read Header Section Shadow<br>1 = Header section selected for transfer from Message RAM to Output Buffer<br>0 = Header section is not read |
| | HEADER_SECTION_NOT_READ | | | 0 | N/A |
| | HEADER_SECTION_FOR_MSRAM2OBF_TXFR | | | 1 | N/A |
| 1 | RDSS | RW | R | 0 | Read Data Section Shadow<br>1 = Data section selected for transfer from Message RAM to Output Buffer<br>0 = Data section is not read |
| | DATA_SECTION_NOT_READ | | | 0 | N/A |
| | DATA_SECTION_FOR_MSRAM2OBF_TXFR | | | 1 | N/A |
| 16 | RHSH | R | RW | 0 | Read Header Section Host<br>1 = Header section selected for transfer from Message RAM to Output Buffer<br>0 = Header section is not read |
| | HEADER_SECTION_NOT_READ | | | 0 | N/A |
| | HEADER_SECTION_FOR_MSRAM2OBF_TXFR | | | 1 | N/A |
| 17 | RDSH | R | RW | 0 | Read Data Section Host<br>1 = Data section selected for transfer from Message RAM to Output Buffer<br>0 = Data section is not read |
| | DATA_SECTION_NOT_READ | | | 0 | N/A |
| | DATA_SECTION_FOR_MSRAM2OBF_TXFR | | | 1 | N/A |

### 15.1.85 FLEXRAY_OBCR

**Description:** Output Buffer Command Request
**Address:** 0x40560714
**Offset:** 0x714
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:7] | OBRS [6:0] | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | OBSYS [15:15] | None [14:10] | | | | | REQ [9:9] | VIEW [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:23] | OBRH [22:16] | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:6 | OBRS | RW | R | 0 | Output Buffer Request Shadow<br>Number of source message buffer to be transferred from the Message RAM to OBF Shadow.<br>Valid values are 0x00 to 0x7F (0...127). If the number of the first message buffer of the receive<br>FIFO is written to this register the Message Handler transfers the message buffer addressed by<br>the GET Index (GIDX, see [01]Section 5.10 FIFO Function) to OBF Shadow. |
| 8 | VIEW | RW | R | 0 | View Shadow Buffer<br>Toggles between OBF Shadow and OBF Host. Only writeable while OBSYS = '0'.<br>1 = Swap OBF Shadow and OBF Host<br>0 = No action |
| | NO_ACTION | | | 0 | N/A |
| | SWP_OBFS_AND_OBFH | | | 1 | N/A |
| 9 | REQ | RW | R | 0 | Request Message RAM Transfer<br>Requests transfer of message buffer addressed by OBRS[6:0] from Message RAM to OBF<br>Shadow. Only writeable while OBSYS = '0'.<br>1 = Transfer to OBF Shadow requested<br>0 = No request |
| | NO_REQUEST | | | 0 | N/A |
| | TXFR_TO_OBFS_REQ | | | 1 | N/A |
| 15 | OBSYS | R | RW | 0 | Output Buffer Busy Shadow<br>Set to '1' after setting bit REQ. When the transfer between the Message RAM and OBF<br>Shadow has completed, OBSYS is set back to '0'.<br>1 = Transfer between Message RAM and OBF Shadow in progress<br>0 = No transfer in progress |
| | NO_TXFR_IN_PROGRESS | | | 0 | N/A |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| | TXFR_BTW_MSRAM_AND_OBFS | | | 1 | N/A |
| 16:22 | OBRH | R | RW | 0 | Output Buffer Request Host<br>Number of message buffer currently accessible by the Host via RDHS[1...3], MBS, and RDDS[1...64]. By writing VIEW to '1' OBF Shadow and OBF Host are swapped and the transferred message buffer is accessible by the Host. Valid values are 0x00 to 0x7F (0...127). |

### 15.1.86 FLEXRAY_WRHS1_MIR2

**Description:** Write Header Section 1 (2nd mirror)
**Address:** 0x40560BF0
**Offset:** 0xBF0
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | FID [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:11] | | | | | FID [10:8] | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:23] | CYC [22:16] | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:30] | | MBI [29:29] | TXM [28:28] | PPIT [27:27] | CFG [26:26] | CHB [25:25] | CHA [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:10 | FID | RW | R | 0 | Frame ID<br>Frame ID of the selected message buffer. The frame ID defines the slot number for transmission reception of the respective message. Message buffers with frame ID = '0' are considered as not valid. |
| 16:22 | CYC | RW | R | 0 | Cycle Code<br>The 7-bit cycle code determines the cycle set used for cycle counter filtering. For details about the configuration of the cycle code see [01]Section 5.7.2 Cycle Counter Filtering.<br>CHA, CHB Channel Filter Control<br>The 2-bit channel filtering field associated with each buffer serves as a filter for receive buffers, and as a control field for transmit buffers.<br>CHA CHB.<br>Transmit Buffer<br>transmit frame on<br>Receive Buffer<br>store frame received from<br>1 1 both channels<br>static segment only)<br>channel A or B<br>store first semantically valid frame,<br>static segment only)<br>1 0 channel A channel A<br>0 1 channel B channel B<br>0 0 no transmission ignore frame |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 24 | CHA | RW | R | 0 | Channel Filter Control A<br>The 2-bit channel filtering field associated with each buffer serves as a filter for receive buffers, and as a control field for transmit buffers.<br><br>Note: If a message buffer is configured for the dynamic segment and both bits of the channel filtering field are set to '1', no frames are transmitted resp. received frames are ignored (same function as CHA = CHB = '0') |
| | CH_A_DISABLED | | | 0 | N/A |
| | CH_A_ENABLED | | | 1 | N/A |
| 25 | CHB | RW | R | 0 | Channel Filter Control B<br>The 2-bit channel filtering field associated with each buffer serves as a filter for receive buffers, and as a control field for transmit buffers.<br><br>Note: If a message buffer is configured for the dynamic segment and both bits of the channel filtering field are set to '1', no frames are transmitted resp. received frames are ignored (same function as CHA = CHB = '0') |
| | CH_B_DISABLED | | | 0 | N/A |
| | CH_B_ENABLED | | | 1 | N/A |
| 26 | CFG | RW | R | 0 | Message Buffer Direction Configuration Bit<br>This bit is used to configure the corresponding buffer as transmit buffer or as receive buffer. For message buffers belonging to the receive FIFO the bit is not evaluated.<br>1 = The corresponding buffer is configured as Transmit Buffer<br>0 = The corresponding buffer is configured as Receive Buffer |
| | RX_BUFF | | | 0 | N/A |
| | TX_BUFF | | | 1 | N/A |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 27 | PPIT | RW | R | 0 | Payload Preamble Indicator Transmit<br>This bit is used to control the state of the Payload Preamble Indicator in transmit frames. If the bit is set in a static message buffer, the respective message buffer holds network management information. If the bit is set in a dynamic message buffer the first two bytes of the payload segment may be used for message ID filtering by the receiver. Message ID filtering of received FlexRay frames is not supported by the E-Ray module, but can be done by the Host.<br>1 = Payload Preamble Indicator set<br>0 = Payload Preamble Indicator not set |
| | PAYLOAD_PREAMBLE_NOT_SET | | | 0 | N/A |
| | PAYLOAD_PREAMBLE_SET | | | 1 | N/A |
| 28 | TXM | RW | R | 0 | Transmission Mode<br>This bit is used to select the transmission mode (see [01]Section 5.8.3 Transmit Buffers).<br>1 = Single-shot mode<br>0 = Continuous mode |
| | CONTINUOUS_MODE | | | 0 | N/A |
| | SINGLE_SHOT_MODE | | | 1 | N/A |
| 29 | MBI | RW | R | 0 | Message Buffer Interrupt<br>This bit enables the receive / transmit interrupt for the corresponding message buffer. After a dedicated receive buffer has been updated by the Message Handler, flag SIR.RXI and /or SIR.MBSI are set. After a transmission has completed flag SIR.TXI is set.<br>1 = The corresponding message buffer interrupt is enabled<br>0 = The corresponding message buffer interrupt is disabled |
| | MSG_BUFF_INTR_DISABLED | | | 0 | N/A |
| | MSG_BUFF_INTR_ENABLED | | | 1 | N/A |

### 15.1.87 FLEXRAY_WRHS2_MIR2

**Description:** Write Header Section 2 (2nd mirror)
**Address:** 0x40560BF4
**Offset:** 0xBF4
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | CRC [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:11] | | | | | CRC [10:8] | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:23] | PLC [22:16] | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:10 | CRC | RW | R | 0 | Header CRC (vRF!Header!HeaderCRC)<br>Receive Buffer: Configuration not required<br>Transmit Buffer: Header CRC calculated and configured by the Host<br>For calculation of the header CRC the payload length of the frame send on the bus has to be considered. In static segment the payload length of all frames is configured by MHDC.SFDL[6:0]. |
| 16:22 | PLC | RW | R | 0 | Payload Length Configured<br>Length of data section (number of 2-byte words) as configured by the Host. During static segment the static frame payload length as configured by MHDC.SFDL[6:0] defines the payload length for all static frames. If the payload length configured by PLC[6:0] is shorter than this value padding bytes are inserted to ensure that frames have proper physical length. The padding pattern is logical zero (see also Section 5.8.3 Transmit Buffers). |

### 15.1.88 FLEXRAY_WRHS3_MIR2

**Description:** Write Header Section 3 (2nd mirror)
**Address:** 0x40560BF8
**Offset:** 0xBF8
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DP [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:11] | | | | | DP [10:8] | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:10 | DP | RW | R | 0 | Data Pointer<br>Pointer to the first 32-bit word of the data section of the addressed message buffer in the Message RAM. |

### 15.1.89 FLEXRAY_WRDS_MIR

**Description:** Write Data Section [1...64] (mirror)
**Address:** 0x40560C00
**Offset:** 0xC00
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** should be n=1...64
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | MD [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | MD [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | MD [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | MD [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | MD | RW | R | 0 | Message Data<br>MD[7:0] = DW2n-1, byte4n-4<br>MD[15:8] = DW2n-1, byte4n-3<br>MD[23:16] = DW2n, byte4n-2<br>MD[31:24] = DW2n, byte4n-1 |

### 15.1.90 FLEXRAY_WRHS1_MIR

**Description:** Write Header Section 1 (mirror)
**Address:** 0x40560D00
**Offset:** 0xD00
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | FID [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:11] | | | | | FID [10:8] | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:23] | CYC [22:16] | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:30] | | MBI [29:29] | TXM [28:28] | PPIT [27:27] | CFG [26:26] | CHB [25:25] | CHA [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:10 | FID | RW | R | 0 | Frame ID<br>Frame ID of the selected message buffer. The frame ID defines the slot number for transmission reception of the respective message. Message buffers with frame ID = '0' are considered as not valid. |
| 16:22 | CYC | RW | R | 0 | Cycle Code<br>The 7-bit cycle code determines the cycle set used for cycle counter filtering. For details about the configuration of the cycle code see [01]Section 5.7.2 Cycle Counter Filtering.<br>CHA, CHB Channel Filter Control<br>The 2-bit channel filtering field associated with each buffer serves as a filter for receive buffers, and as a control field for transmit buffers.<br>CHA CHB.<br>Transmit Buffer<br>transmit frame on<br>Receive Buffer<br>store frame received from<br>1 1 both channels<br>static segment only)<br>channel A or B<br>store first semantically valid frame,<br>static segment only)<br>1 0 channel A channel A<br>0 1 channel B channel B<br>0 0 no transmission ignore frame |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 24 | CHA | RW | R | 0 | Channel Filter Control A<br>The 2-bit channel filtering field associated with each buffer serves as a filter for receive buffers, and as a control field for transmit buffers.<br><br>Note: If a message buffer is configured for the dynamic segment and both bits of the channel filtering field are set to '1', no frames are transmitted resp. received frames are ignored (same function as CHA = CHB = '0') |
| | CH_A_DISABLED | | | 0 | N/A |
| | CH_A_ENABLED | | | 1 | N/A |
| 25 | CHB | RW | R | 0 | Channel Filter Control B<br>The 2-bit channel filtering field associated with each buffer serves as a filter for receive buffers, and as a control field for transmit buffers.<br><br>Note: If a message buffer is configured for the dynamic segment and both bits of the channel filtering field are set to '1', no frames are transmitted resp. received frames are ignored (same function as CHA = CHB = '0') |
| | CH_B_DISABLED | | | 0 | N/A |
| | CH_B_ENABLED | | | 1 | N/A |
| 26 | CFG | RW | R | 0 | Message Buffer Direction Configuration Bit<br>This bit is used to configure the corresponding buffer as transmit buffer or as receive buffer. For message buffers belonging to the receive FIFO the bit is not evaluated.<br>1 = The corresponding buffer is configured as Transmit Buffer<br>0 = The corresponding buffer is configured as Receive Buffer |
| | RX_BUFF | | | 0 | N/A |
| | TX_BUFF | | | 1 | N/A |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 27 | PPIT | RW | R | 0 | Payload Preamble Indicator Transmit<br>This bit is used to control the state of the Payload Preamble Indicator in transmit frames. If the bit is set in a static message buffer, the respective message buffer holds network management information. If the bit is set in a dynamic message buffer the first two bytes of the payload segment may be used for message ID filtering by the receiver. Message ID filtering of received FlexRay frames is not supported by the E-Ray module, but can be done by the Host.<br>1 = Payload Preamble Indicator set<br>0 = Payload Preamble Indicator not set |
| | PAYLOAD_PREAMBLE_NOT_SET | | | 0 | N/A |
| | PAYLOAD_PREAMBLE_SET | | | 1 | N/A |
| 28 | TXM | RW | R | 0 | Transmission Mode<br>This bit is used to select the transmission mode (see [01]Section 5.8.3 Transmit Buffers).<br>1 = Single-shot mode<br>0 = Continuous mode |
| | CONTINUOUS_MODE | | | 0 | N/A |
| | SINGLE_SHOT_MODE | | | 1 | N/A |
| 29 | MBI | RW | R | 0 | Message Buffer Interrupt<br>This bit enables the receive / transmit interrupt for the corresponding message buffer. After a dedicated receive buffer has been updated by the Message Handler, flag SIR.RXI and /or SIR.MBSI are set. After a transmission has completed flag SIR.TXI is set.<br>1 = The corresponding message buffer interrupt is enabled<br>0 = The corresponding message buffer interrupt is disabled |
| | MSG_BUFF_INTR_DISABLED | | | 0 | N/A |
| | MSG_BUFF_INTR_ENABLED | | | 1 | N/A |

### 15.1.91 FLEXRAY_WRHS2_MIR

**Description:** Write Header Section 2 (mirror)
**Address:** 0x40560D04
**Offset:** 0xD04
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | CRC [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:11] | | | | | CRC [10:8] | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:23] | PLC [22:16] | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:10 | CRC | RW | R | 0 | Header CRC (vRF!Header!HeaderCRC)<br>Receive Buffer: Configuration not required<br>Transmit Buffer: Header CRC calculated and configured by the Host<br>For calculation of the header CRC the payload length of the frame send on the bus has to be considered. In static segment the payload length of all frames is configured by MHDC.SFDL[6:0]. |
| 16:22 | PLC | RW | R | 0 | Payload Length Configured<br>Length of data section (number of 2-byte words) as configured by the Host. During static segment the static frame payload length as configured by MHDC.SFDL[6:0] defines the payload length for all static frames. If the payload length configured by PLC[6:0] is shorter than this value padding bytes are inserted to ensure that frames have proper physical length. The padding pattern is logical zero (see also Section 5.8.3 Transmit Buffers). |

### 15.1.92 FLEXRAY_WRHS3_MIR

**Description:** Write Header Section 3 (mirror)
**Address:** 0x40560D08
**Offset:** 0xD08
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DP [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:11] | | | | | DP [10:8] | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:10 | DP | RW | R | 0 | Data Pointer<br>Pointer to the first 32-bit word of the data section of the addressed message buffer in the Message RAM. |

### 15.1.93 FLEXRAY_IBCM_MIR

**Description:** Input Buffer Command Mask (mirror)
**Address:** 0x40560D10
**Offset:** 0xD10
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:3] | | | | | STXRH [2:2] | LDSH [1:1] | LHSH [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:19] | | | | | STXRS [18:18] | LDSS [17:17] | LHSS [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | LHSH | RW | R | 0 | Load Header Section Host<br>1 = Header section selected for transfer from Input Buffer to the Message RAM<br>0 = Header section is not updated |
| | HEADER_SECTION_NOT_UPDATED | | | 0 | N/A |
| | HEADER_SECTION_UPDATED | | | 1 | N/A |
| 1 | LDSH | RW | R | 0 | Load Data Section Host<br>1 = Data section selected for transfer from Input Buffer to the Message RAM<br>0 = Data section is not updated |
| | DATA_SECTION_NOT_UPDATED | | | 0 | N/A |
| | DATA_SECTION_UPDATED | | | 1 | N/A |
| 2 | STXRH | RW | R | 0 | Set Transmission Request Host<br>If this bit is set to '1', the TXR flag for the selected message buffer is set in the TXRQ1/2/3/4 registers to release the message buffer for transmission. In single-shot mode the flag is cleared by the CC after transmission has completed. TXR is evaluated for transmit buffers only.<br>1 = Set TXR flag, transmit buffer released for transmission<br>0 = Reset TXR flag |
| | TXR_FLAG_RESET | | | 0 | N/A |
| | TXR_FLAG_SET | | | 1 | N/A |
| 16 | LHSS | R | RW | 0 | Load Header Section Shadow<br>1 = Header section selected for transfer from Input Buffer to the Message RAM<br>transfer ongoing or finished)<br>0 = Header section is not updated |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| | HEADER_SECTION_NOT_UPDATED | | | 0 | N/A |
| | HEADER_SECTION_UPDATED | | | 1 | N/A |
| 17 | LDSS | R | RW | 0 | Load Data Section Shadow<br>1 = Data section selected for transfer from Input Buffer to the Message RAM<br>transfer ongoing or finished)<br>0 = Data section is not updated |
| | DATA_SECTION_NOT_UPDATED | | | 0 | N/A |
| | DATA_SECTION_UPDATED | | | 1 | N/A |
| 18 | STXRS | R | RW | 0 | Set Transmission Request Shadow<br>1 = Set TXR flag, transmit buffer released for transmission (operation ongoing or finished)<br>0 = Reset TXR flag |
| | TXR_FLAG_RESET | | | 0 | N/A |
| | TXR_FLAG_SET | | | 1 | N/A |

### 15.1.94 FLEXRAY_IBCR_MIR

**Description:** Input Buffer Command Request (mirror)
**Address:** 0x40560D14
**Offset:** 0xD14
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:7] | IBRH [6:0] | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | IBSYH [15:15] | None [14:8] | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:23] | IBRS [22:16] | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | IBSYS [31:31] | None [30:24] | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:6 | IBRH | RW | R | 0 | Input Buffer Request Host<br>Selects the target message buffer in the Message RAM for data transfer from Input Buffer.<br>Valid values are 0x00 to 0x7F (0...127). |
| 15 | IBSYH | R | RW | 0 | Input Buffer Busy Host<br>Set to '1' by writing IBRH[6:0] while IBSYS is still '1'. After the ongoing transfer between<br>IBF Shadow and the Message RAM has completed, the IBSYH is set back to '0'.<br>1 = Request while transfer between IBF Shadow and Message RAM in progress<br>0 = No request pending |
| | REQUEST_NOT_PENDING | | | 0 | N/A |
| | REQUEST_IN_PROGRESS | | | 1 | N/A |
| 16:22 | IBRS | R | RW | 0 | Input Buffer Request Shadow<br>Number of the target message buffer actually updated / lately updated.<br>Valid values are 0x00 to 0x7F (0...127). |
| 31 | IBSYS | R | RW | 0 | Input Buffer Busy Shadow<br>Set to '1' after writing IBRH[6:0]. When the transfer between IBF Shadow and the Message<br>RAM has completed, IBSYS is set back to '0'.<br>1 = Transfer between IBF Shadow and Message RAM in progress<br>0 = Transfer between IBF Shadow and Message RAM completed |
| | TXFR_IBF2MSRAM_COMPLETE | | | 0 | N/A |
| | TXFR_IBF2MSRAM_IN_PROGRESS | | | 1 | N/A |

### 15.1.95 FLEXRAY_RDHS1_MIR2

**Description:** Read Header Section 1 (2nd mirror)
**Address:** 0x40560DF0
**Offset:** 0xDF0
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | FID [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:11] | | | | | FID [10:8] | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:23] | CYC [22:16] | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:30] | | MBI [29:29] | TXM [28:28] | PPIT [27:27] | CFG [26:26] | CHB [25:25] | CHA [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:10 | FID | R | RW | 0 | Frame ID |
| 16:22 | CYC | R | RW | 0 | Cycle Code |
| 24 | CHA | R | RW | 0 | Channel Filter Control A |
| 25 | CHB | R | RW | 0 | Channel Filter Control B |
| 26 | CFG | R | RW | 0 | Message Buffer Direction Configuration Bit |
| 27 | PPIT | R | RW | 0 | Payload Preamble Indicator Transmit |
| 28 | TXM | R | RW | 0 | Transmission Mode |
| 29 | MBI | R | RW | 0 | Message Buffer Interrupt |

### 15.1.96 FLEXRAY_RDHS2_MIR2

**Description:** Read Header Section 2 (2nd mirror)
**Address:** 0x40560DF4
**Offset:** 0xDF4
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | CRC [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:11] | | | | | CRC [10:8] | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:23] | PLC [22:16] | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:31] | PLR [30:24] | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:10 | CRC | R | RW | 0 | Header CRC (vRF!Header!HeaderCRC)<br>Receive Buffer: Header CRC updated from received data frames<br>Transmit Buffer: Header CRC calculated and configured by the Host |
| 16:22 | PLC | R | RW | 0 | Payload Length Configured<br>Length of data section (number of 2-byte words) as configured by the Host. |
| 24:30 | PLR | R | RW | 0 | Payload Length Received (vRF!Header!Length)<br>Payload length value updated from received data frames (exception: if message buffer belongs to the receive FIFO PLR[6:0] is also updated from received null frames)<br>When a message is stored into a message buffer the following behaviour with respect to payload length received and payload length configured is implemented:<br>PLR[6:0] > PLC[6:0]: The payload data stored in the message buffer is truncated to the payload length configured if PLC[6:0] even or else truncated to PLC[6:0] + 1.<br>PLR[6:0] <= PLC[6:0]: The received payload data is stored into the message buffers data section. The remaining data bytes of the data section as configured by PLC[6:0] are filled with undefined data<br>PLR[6:0] = zero: The message buffer's data section is filled with undefined data<br>PLC[6:0] = zero: Message buffer has no data section configured. No data is stored into the message buffer's data section. |

### 15.1.97 FLEXRAY_RDHS3_MIR2

**Description:** Read Header Section 3 (2nd mirror)
**Address:** 0x40560DF8
**Offset:** 0xDF8
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DP [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:11] | | | | | DP [10:8] | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:22] | | RCC [21:16] | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:30] | | RES [29:29] | PPI [28:28] | NFI [27:27] | SYN [26:26] | SFI [25:25] | RCI [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:10 | DP | R | RW | 0 | Data Pointer<br>Pointer to the first 32-bit word of the data section of the addressed message buffer in the Message RAM. |
| 16:21 | RCC | R | RW | 0 | Receive Cycle Count (vRF!Header!CycleCount)<br>Cycle counter value updated from received data frame. |
| 24 | RCI | R | RW | 0 | Received on Channel Indicator (vSS!Channel)<br>Indicates the channel from which the received data frame was taken to update the respective receive buffer.<br>1 = Frame received on channel A<br>0 = Frame received on channel B |
| | CH_B_FRAME_RECEIVED | | | 0 | N/A |
| | CH_A_FRAME_RECEIVED | | | 1 | N/A |
| 25 | SFI | R | RW | 0 | Startup Frame Indicator (vRF!Header!SuFIndicator)<br>A startup frame is marked by the startup frame indicator.<br>1 = The received frame is a startup frame<br>0 = The received frame is not a startup frame |
| | RXD_FRAME_NOT_STARTUP_FRAME | | | 0 | N/A |
| | RXD_FRAME_STARTUP_FRAME | | | 1 | N/A |
| 26 | SYN | R | RW | 0 | Sync Frame Indicator (vRF!Header!SyFIndicator)<br>A sync frame is marked by the sync frame indicator.<br>1 = The received frame is a sync frame<br>0 = The received frame is not a sync frame |
| | RXD_FRAME_NOT_SYNC_FRAME | | | 0 | N/A |
| | RXD_FRAME_SYNC_FRAME | | | 1 | N/A |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 27 | NFI | R | RW | 0 | Null Frame Indicator (vRF!Header!NFIndicator)<br>Is set to '1' after storage of the first received data frame.<br>1 = At least one data frame has been stored into the respective message buffer<br>0 = Up to now no data frame has been stored into the respective message buffer |
| | DATA_FRAME_NOT_STORED | | | 0 | N/A |
| | DATA_FRAME_STORED | | | 1 | N/A |
| 28 | PPI | R | RW | 0 | Payload Preamble Indicator (vRF!Header!PPIndicator)<br>The payload preamble indicator defines whether a network management vector or message ID is contained within the payload segment of the received frame.<br>1 = Static segment: Network management vector in the first part of the payload<br>Dynamic segment:Message ID in the first part of the payload<br>0 = The payload segment of the received frame does not contain a network management vector<br>nor a message ID |
| | PAYLOAD_SEGMENT_HAS_NO_NMV_MID | | | 0 | N/A |
| | PAYLOAD_SEGMENT_WITH_NMV_MID | | | 1 | N/A |
| 29 | RES | R | RW | 0 | Reserved Bit (vRF!Header!Reserved)<br>Reflects the state of the received reserved bit. The reserved bit is transmitted as '0'. |

### 15.1.98 FLEXRAY_MBS_MIR2

**Description:** Message Buffer Status (2nd mirror)
**Address:** 0x40560DFC
**Offset:** 0xDFC
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | SVOB [7:7] | SVOA [6:6] | CEOB [5:5] | CEOA [4:4] | SEOB [3:3] | SEOA [2:2] | VFRB [1:1] | VFRA [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | FTB [15:15] | FTA [14:14] | None [13:13] | MLST [12:12] | ESB [11:11] | ESA [10:10] | TCIB [9:9] | TCIA [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:22] | | CCS [21:16] | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:30] | | RESS [29:29] | PPIS [28:28] | NFIS [27:27] | SYNS [26:26] | SFIS [25:25] | RCIS [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | VFRA | R | RW | 0 | Valid Frame Received on Channel A (vSS!ValidFrameA)<br>A valid frame indication is set if a valid frame was received on channel A.<br>1 = Valid frame received on channel A<br>0 = No valid frame received on channel A |
| | CH_A_NO_VALID_FRAME | | | 0 | N/A |
| | CH_A_WITH_VALID_FRAME | | | 1 | N/A |
| 1 | VFRB | R | RW | 0 | Valid Frame Received on Channel B (vSS!ValidFrameB)<br>A valid frame indication is set if a valid frame was received on channel B.<br>1 = Valid frame received on channel B<br>0 = No valid frame received on channel B |
| | CH_B_NO_VALID_FRAME | | | 0 | N/A |
| | CH_B_WITH_VALID_FRAME | | | 1 | N/A |
| 2 | SEOA | R | RW | 0 | Syntax Error Observed on Channel A (vSS!SyntaxErrorA)<br>A syntax error was observed in the assigned slot on channel A.<br>1 = Syntax error observed on channel A<br>0 = No syntax error observed on channel A |
| | CH_A_NO_SYNTAX_ERROR | | | 0 | N/A |
| | CH_A_HAS_SYNTAX_ERROR | | | 1 | N/A |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 3 | SEOB | R | RW | 0 | Syntax Error Observed on Channel B (vSS!SyntaxErrorB)<br>A syntax error was observed in the assigned slot on channel B.<br>1 = Syntax error observed on channel B<br>0 = No syntax error observed on channel B |
| | CH_B_NO_SYNTAX_ERROR | | | 0 | N/A |
| | CH_B_HAS_SYNTAX_ERROR | | | 1 | N/A |
| 4 | CEOA | R | RW | 0 | Content Error Observed on Channel A (vSS!ContentErrorA)<br>A content error was observed in the assigned slot on channel A.<br>1 = Content error observed on channel A<br>0 = No content error observed on channel A |
| | CH_A_NO_CONTENT_ERROR | | | 0 | N/A |
| | CH_A_HAS_CONTENT_ERROR | | | 1 | N/A |
| 5 | CEOB | R | RW | 0 | Content Error Observed on Channel B (vSS!ContentErrorB)<br>A content error was observed in the assigned slot on channel B.<br>1 = Content error observed on channel B<br>0 = No content error observed on channel B |
| | CH_B_NO_CONTENT_ERROR | | | 0 | N/A |
| | CH_B_HAS_CONTENT_ERROR | | | 1 | N/A |
| 6 | SVOA | R | RW | 0 | Slot Boundary Violation Observed on Channel A (vSS!BViolationA)<br>A slot boundary violation (channel active at the start or at the end of the assigned slot) was observed on channel A.<br>1 = Slot boundary violation observed on channel A<br>0 = No slot boundary violation observed on channel A |
| | CH_A_NO_SLOT_BNDRY_VIOLATION | | | 0 | N/A |
| | CH_A_HAS_SLOT_BNDRY_VIOLATION | | | 1 | N/A |
| 7 | SVOB | R | RW | 0 | Slot Boundary Violation Observed on Channel B (vSS!BViolationB)<br>A slot boundary violation (channel active at the start or at the end of the assigned slot) was observed on channel B.<br>1 = Slot boundary violation observed on channel B<br>0 = No slot boundary violation observed on channel B |
| | CH_B_NO_SLOT_BNDRY_VIOLATION | | | 0 | N/A |
| | CH_B_HAS_SLOT_BNDRY_VIOLATION | | | 1 | N/A |
| 8 | TCIA | R | RW | 0 | Transmission Conflict Indication Channel A (vSS!TxConflictA)<br>A transmission conflict indication is set if a transmission conflict has occurred on channel A.<br>1 = Transmission conflict occurred on channel A<br>0 = No transmission conflict occurred on channel A |
| | CH_A_NO_TXMN_CONFLICT | | | 0 | N/A |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| | CH_A_HAS_TXMN _CONFLICT | | | 1 | N/A |
| 9 | TCIB | R | RW | 0 | Transmission Conflict Indication Channel B (vSS!TxConflictB)<br>A transmission conflict indication is set if a transmission conflict has occurred on channel B.<br>1 = Transmission conflict occurred on channel B<br>0 = No transmission conflict occurred on channel B |
| | CH_B_NO_TXMN _CONFLICT | | | 0 | N/A |
| | CH_B_HAS_TXMN _CONFLICT | | | 1 | N/A |
| 10 | ESA | R | RW | 0 | Empty Slot Channel A<br>In an empty slot there is no activity detected on the bus. The condition is checked in static and dynamic slots.<br>1 = No bus activity detected in the assigned slot on channel A<br>0 = Bus activity detected in the assigned slot on channel A |
| | CH_A_HAS_BUS_ACTIVI TY | | | 0 | N/A |
| | CH_A_NO_BUS_ACTIVIT Y | | | 1 | N/A |
| 11 | ESB | R | RW | 0 | Empty Slot Channel B<br>In an empty slot there is no activity detected on the bus. The condition is checked in static and dynamic slots.<br>1 = No bus activity detected in the assigned slot on channel B<br>0 = Bus activity detected in the assigned slot on channel B |
| | CH_B_HAS_BUS_ACTIVI TY | | | 0 | N/A |
| | CH_B_NO_BUS_ACTIVIT Y | | | 1 | N/A |
| 12 | MLST | R | RW | 0 | Message Lost<br>The flag is set in case the Host did not read the message before the message buffer was updated from a received data frame. Not affected by reception of null frames except for message buffers belonging to the receive FIFO. The flag is reset by a Host write to the message buffer via IBF or when a new message is stored into the message buffer after the message buffers ND flag was reset by reading out the message buffer via OBF.<br>1 = Unprocessed message was overwritten<br>0 = No message lost |
| | NO_MSG_LOST | | | 0 | N/A |
| | MSG_LOST | | | 1 | N/A |
| 14 | FTA | R | RW | 0 | Frame Transmitted on Channel A<br>Indicates that this node has transmitted a data frame in the configured slot on channel A.<br>1 = Data frame transmitted on channel A<br>0 = No data frame transmitted on channel A |
| | DATA_FRAME_NOT _TXD_ON_CH_A | | | 0 | N/A |
| | DATA_FRAME_TXD_ON _CH_A | | | 1 | N/A |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 15 | FTB | R | RW | 0 | Frame Transmitted on Channel B<br>Indicates that this node has transmitted a data frame in the configured slot on channel B.<br>1 = Data frame transmitted on channel B<br>0 = No data frame transmitted on channel B |
| | DATA_FRAME_NOT_TXD_ON_CH_B | | | 0 | N/A |
| | DATA_FRAME_TXD_ON_CH_B | | | 1 | N/A |
| 16:21 | CCS | R | RW | 0 | Cycle Count Status<br>Actual cycle count when status was updated.<br>For receive buffers (CFG = '0') the following status bits are updated from both valid data and null frames. If no valid frame was received, the previous value is maintained. For transmit buffers the flags have no meaning and should be ignored. |
| 24 | RCIS | R | RW | 0 | Received on Channel Indicator Status (vSS!Channel)<br>Indicates the channel on which the frame was received.<br>1 = Frame received on channel A<br>0 = Frame received on channel B |
| | CH_B_FRAME_RECEIVED | | | 0 | N/A |
| | CH_A_FRAME_RECEIVED | | | 1 | N/A |
| 25 | SFIS | R | RW | 0 | Startup Frame Indicator Status (vRF!Header!SuFIndicator)<br>A startup frame is marked by the startup frame indicator.<br>1 = The received frame is a startup frame<br>0 = No startup frame received |
| | NO_STARTUP_FRAME_RECEIVED | | | 0 | N/A |
| | STARTUP_FRAME_RECEIVED | | | 1 | N/A |
| 26 | SYNS | R | RW | 0 | Sync Frame Indicator Status (vRF!Header!SyFIndicator)<br>A sync frame is marked by the sync frame indicator.<br>1 = The received frame is a sync frame<br>0 = No sync frame received |
| | NO_SYNC_FRAME_RECEIVED | | | 0 | N/A |
| | SYNC_FRAME_RECEIVED | | | 1 | N/A |
| 27 | NFIS | R | RW | 0 | Null Frame Indicator Status (vRF!Header!NFIndicator)<br>If set to '0' the payload segment of the received frame contains no usable data.<br>1 = Received frame is not a null frame<br>0 = Received frame is a null frame |
| | NULL_FRAME_RECEIVED | | | 0 | N/A |
| | NO_NULL_FRAME_RECEIVED | | | 1 | N/A |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 28 | PPIS | R | RW | 0 | Payload Preamble Indicator Status (vRF!Header!PPIndicator)<br>The payload preamble indicator defines whether a network management vector or message ID is contained within the payload segment of the received frame.<br>1 = Static segment: Network management vector at the beginning of the payload<br>Dynamic segment: Message ID at the beginning of the payload<br>0 = The payload segment of the received frame does not contain a network management vector<br>or a message ID |
| | PAYLOAD_SEGMENT_HAS_NO_NMV_MID | | | 0 | N/A |
| | PAYLOAD_SEGMENT_WITH_NMV_MID | | | 1 | N/A |
| 29 | RESS | R | RW | 0 | Reserved Bit Status (vRF!Header!Reserved)<br>Reflects the state of the received reserved bit. The reserved bit is transmitted as '0'. |

### 15.1.99 FLEXRAY_RDDS_MIR

**Description:** Read Data Section [1...64] (mirror)
**Address:** 0x40560E00
**Offset:** 0xE00
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** should be n=1...64
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | MD [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | MD [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | MD [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | MD [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | MD | R | RW | 0 | Message Data<br>MD[7:0] = DW2n-1, byte4n-4<br>MD[15:8] = DW2n-1, byte4n-3<br>MD[23:16] = DW2n, byte4n-2<br>MD[31:24] = DW2n, byte4n-1 |

### 15.1.100 FLEXRAY_RDHS1_MIR

**Description:** Read Header Section 1 (mirror)
**Address:** 0x40560F00
**Offset:** 0xF00
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | FID [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:11] | | | | | FID [10:8] | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:23] | CYC [22:16] | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:30] | | MBI [29:29] | TXM [28:28] | PPIT [27:27] | CFG [26:26] | CHB [25:25] | CHA [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:10 | FID | R | RW | 0 | Frame ID |
| 16:22 | CYC | R | RW | 0 | Cycle Code |
| 24 | CHA | R | RW | 0 | Channel Filter Control A |
| 25 | CHB | R | RW | 0 | Channel Filter Control B |
| 26 | CFG | R | RW | 0 | Message Buffer Direction Configuration Bit |
| 27 | PPIT | R | RW | 0 | Payload Preamble Indicator Transmit |
| 28 | TXM | R | RW | 0 | Transmission Mode |
| 29 | MBI | R | RW | 0 | Message Buffer Interrupt |

### 15.1.101 FLEXRAY_RDHS2_MIR

**Description:** Read Header Section 2 (mirror)
**Address:** 0x40560F04
**Offset:** 0xF04
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | CRC [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:11] | | | | | CRC [10:8] | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:23] | PLC [22:16] | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:31] | PLR [30:24] | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:10 | CRC | R | RW | 0 | Header CRC (vRF!Header!HeaderCRC)<br>Receive Buffer: Header CRC updated from received data frames<br>Transmit Buffer: Header CRC calculated and configured by the Host |
| 16:22 | PLC | R | RW | 0 | Payload Length Configured<br>Length of data section (number of 2-byte words) as configured by the Host. |
| 24:30 | PLR | R | RW | 0 | Payload Length Received (vRF!Header!Length)<br>Payload length value updated from received data frames (exception: if message buffer belongs to the receive FIFO PLR[6:0] is also updated from received null frames)<br>When a message is stored into a message buffer the following behaviour with respect to payload length received and payload length configured is implemented:<br>PLR[6:0] > PLC[6:0]: The payload data stored in the message buffer is truncated to the payload length configured if PLC[6:0] even or else truncated to PLC[6:0] + 1.<br>PLR[6:0] <= PLC[6:0]: The received payload data is stored into the message buffers data section. The remaining data bytes of the data section as configured by PLC[6:0] are filled with undefined data<br>PLR[6:0] = zero: The message buffer's data section is filled with undefined data<br>PLC[6:0] = zero: Message buffer has no data section configured. No data is stored into the message buffer's data section. |

### 15.1.102 FLEXRAY_RDHS3_MIR

**Description:** Read Header Section 3 (mirror)
**Address:** 0x40560F08
**Offset:** 0xF08
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DP [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:11] | | | | | DP [10:8] | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:22] | | RCC [21:16] | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:30] | | RES [29:29] | PPI [28:28] | NFI [27:27] | SYN [26:26] | SFI [25:25] | RCI [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:10 | DP | R | RW | 0 | Data Pointer<br>Pointer to the first 32-bit word of the data section of the addressed message buffer in the Message RAM. |
| 16:21 | RCC | R | RW | 0 | Receive Cycle Count (vRF!Header!CycleCount)<br>Cycle counter value updated from received data frame. |
| 24 | RCI | R | RW | 0 | Received on Channel Indicator (vSS!Channel)<br>Indicates the channel from which the received data frame was taken to update the respective receive buffer.<br>1 = Frame received on channel A<br>0 = Frame received on channel B |
| | CH_B_FRAME_RECEIVED | | | 0 | N/A |
| | CH_A_FRAME_RECEIVED | | | 1 | N/A |
| 25 | SFI | R | RW | 0 | Startup Frame Indicator (vRF!Header!SuFIndicator)<br>A startup frame is marked by the startup frame indicator.<br>1 = The received frame is a startup frame<br>0 = The received frame is not a startup frame |
| | RXD_FRAME_NOT_STARTUP_FRAME | | | 0 | N/A |
| | RXD_FRAME_STARTUP_FRAME | | | 1 | N/A |
| 26 | SYN | R | RW | 0 | Sync Frame Indicator (vRF!Header!SyFIndicator)<br>A sync frame is marked by the sync frame indicator.<br>1 = The received frame is a sync frame<br>0 = The received frame is not a sync frame |
| | RXD_FRAME_NOT_SYNC_FRAME | | | 0 | N/A |
| | RXD_FRAME_SYNC_FRAME | | | 1 | N/A |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 27 | NFI | R | RW | 0 | Null Frame Indicator (vRF!Header!NFIndicator)<br>Is set to '1' after storage of the first received data frame.<br>1 = At least one data frame has been stored into the respective message buffer<br>0 = Up to now no data frame has been stored into the respective message buffer |
| | DATA_FRAME_NOT_STORED | | | 0 | N/A |
| | DATA_FRAME_STORED | | | 1 | N/A |
| 28 | PPI | R | RW | 0 | Payload Preamble Indicator (vRF!Header!PPIndicator)<br>The payload preamble indicator defines whether a network management vector or message ID is contained within the payload segment of the received frame.<br>1 = Static segment: Network management vector in the first part of the payload<br>Dynamic segment:Message ID in the first part of the payload<br>0 = The payload segment of the received frame does not contain a network management vector<br>nor a message ID |
| | PAYLOAD_SEGMENT_HAS_NO_NMV_MID | | | 0 | N/A |
| | PAYLOAD_SEGMENT_WITH_NMV_MID | | | 1 | N/A |
| 29 | RES | R | RW | 0 | Reserved Bit (vRF!Header!Reserved)<br>Reflects the state of the received reserved bit. The reserved bit is transmitted as '0'. |

### 15.1.103 FLEXRAY_MBS_MIR

**Description:** Message Buffer Status (mirror)
**Address:** 0x40560F0C
**Offset:** 0xF0C
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | SVOB [7:7] | SVOA [6:6] | CEOB [5:5] | CEOA [4:4] | SEOB [3:3] | SEOA [2:2] | VFRB [1:1] | VFRA [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | FTB [15:15] | FTA [14:14] | None [13:13] | MLST [12:12] | ESB [11:11] | ESA [10:10] | TCIB [9:9] | TCIA [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:22] | | CCS [21:16] | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:30] | | RESS [29:29] | PPIS [28:28] | NFIS [27:27] | SYNS [26:26] | SFIS [25:25] | RCIS [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | VFRA | R | RW | 0 | Valid Frame Received on Channel A (vSS!ValidFrameA)<br>A valid frame indication is set if a valid frame was received on channel A.<br>1 = Valid frame received on channel A<br>0 = No valid frame received on channel A |
| | CH_A_NO_VALID_FRAME | | | 0 | N/A |
| | CH_A_WITH_VALID_FRAME | | | 1 | N/A |
| 1 | VFRB | R | RW | 0 | Valid Frame Received on Channel B (vSS!ValidFrameB)<br>A valid frame indication is set if a valid frame was received on channel B.<br>1 = Valid frame received on channel B<br>0 = No valid frame received on channel B |
| | CH_B_NO_VALID_FRAME | | | 0 | N/A |
| | CH_B_WITH_VALID_FRAME | | | 1 | N/A |
| 2 | SEOA | R | RW | 0 | Syntax Error Observed on Channel A (vSS!SyntaxErrorA)<br>A syntax error was observed in the assigned slot on channel A.<br>1 = Syntax error observed on channel A<br>0 = No syntax error observed on channel A |
| | CH_A_NO_SYNTAX_ERROR | | | 0 | N/A |
| | CH_A_HAS_SYNTAX_ERROR | | | 1 | N/A |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 3 | SEOB | R | RW | 0 | Syntax Error Observed on Channel B (vSS!SyntaxErrorB)<br>A syntax error was observed in the assigned slot on channel B.<br>1 = Syntax error observed on channel B<br>0 = No syntax error observed on channel B |
| | CH_B_NO_SYNTAX_ERROR | | | 0 | N/A |
| | CH_B_HAS_SYNTAX_ERROR | | | 1 | N/A |
| 4 | CEOA | R | RW | 0 | Content Error Observed on Channel A (vSS!ContentErrorA)<br>A content error was observed in the assigned slot on channel A.<br>1 = Content error observed on channel A<br>0 = No content error observed on channel A |
| | CH_A_NO_CONTENT_ERROR | | | 0 | N/A |
| | CH_A_HAS_CONTENT_ERROR | | | 1 | N/A |
| 5 | CEOB | R | RW | 0 | Content Error Observed on Channel B (vSS!ContentErrorB)<br>A content error was observed in the assigned slot on channel B.<br>1 = Content error observed on channel B<br>0 = No content error observed on channel B |
| | CH_B_NO_CONTENT_ERROR | | | 0 | N/A |
| | CH_B_HAS_CONTENT_ERROR | | | 1 | N/A |
| 6 | SVOA | R | RW | 0 | Slot Boundary Violation Observed on Channel A (vSS!BViolationA)<br>A slot boundary violation (channel active at the start or at the end of the assigned slot) was observed on channel A.<br>1 = Slot boundary violation observed on channel A<br>0 = No slot boundary violation observed on channel A |
| | CH_A_NO_SLOT_BNDRY_VIOLATION | | | 0 | N/A |
| | CH_A_HAS_SLOT_BNDRY_VIOLATION | | | 1 | N/A |
| 7 | SVOB | R | RW | 0 | Slot Boundary Violation Observed on Channel B (vSS!BViolationB)<br>A slot boundary violation (channel active at the start or at the end of the assigned slot) was observed on channel B.<br>1 = Slot boundary violation observed on channel B<br>0 = No slot boundary violation observed on channel B |
| | CH_B_NO_SLOT_BNDRY_VIOLATION | | | 0 | N/A |
| | CH_B_HAS_SLOT_BNDRY_VIOLATION | | | 1 | N/A |
| 8 | TCIA | R | RW | 0 | Transmission Conflict Indication Channel A (vSS!TxConflictA)<br>A transmission conflict indication is set if a transmission conflict has occurred on channel A.<br>1 = Transmission conflict occurred on channel A<br>0 = No transmission conflict occurred on channel A |
| | CH_A_NO_TXMN_CONFLICT | | | 0 | N/A |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| | CH_A_HAS_TXMN _CONFLICT | | | 1 | N/A |
| 9 | TCIB | R | RW | 0 | Transmission Conflict Indication Channel B (vSS!TxConflictB)<br>A transmission conflict indication is set if a transmission conflict has occurred on channel B.<br>1 = Transmission conflict occurred on channel B<br>0 = No transmission conflict occurred on channel B |
| | CH_B_NO_TXMN _CONFLICT | | | 0 | N/A |
| | CH_B_HAS_TXMN _CONFLICT | | | 1 | N/A |
| 10 | ESA | R | RW | 0 | Empty Slot Channel A<br>In an empty slot there is no activity detected on the bus. The condition is checked in static and dynamic slots.<br>1 = No bus activity detected in the assigned slot on channel A<br>0 = Bus activity detected in the assigned slot on channel A |
| | CH_A_HAS_BUS_ACTIVI TY | | | 0 | N/A |
| | CH_A_NO_BUS_ACTIVIT Y | | | 1 | N/A |
| 11 | ESB | R | RW | 0 | Empty Slot Channel B<br>In an empty slot there is no activity detected on the bus. The condition is checked in static and dynamic slots.<br>1 = No bus activity detected in the assigned slot on channel B<br>0 = Bus activity detected in the assigned slot on channel B |
| | CH_B_HAS_BUS_ACTIVI TY | | | 0 | N/A |
| | CH_B_NO_BUS_ACTIVIT Y | | | 1 | N/A |
| 12 | MLST | R | RW | 0 | Message Lost<br>The flag is set in case the Host did not read the message before the message buffer was updated from a received data frame. Not affected by reception of null frames except for message buffers belonging to the receive FIFO. The flag is reset by a Host write to the message buffer via IBF or when a new message is stored into the message buffer after the message buffers ND flag was reset by reading out the message buffer via OBF.<br>1 = Unprocessed message was overwritten<br>0 = No message lost |
| | NO_MSG_LOST | | | 0 | N/A |
| | MSG_LOST | | | 1 | N/A |
| 14 | FTA | R | RW | 0 | Frame Transmitted on Channel A<br>Indicates that this node has transmitted a data frame in the configured slot on channel A.<br>1 = Data frame transmitted on channel A<br>0 = No data frame transmitted on channel A |
| | DATA_FRAME_NOT _TXD_ON_CH_A | | | 0 | N/A |
| | DATA_FRAME_TXD_ON _CH_A | | | 1 | N/A |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 15 | FTB | R | RW | 0 | Frame Transmitted on Channel B<br>Indicates that this node has transmitted a data frame in the configured slot on channel B.<br>1 = Data frame transmitted on channel B<br>0 = No data frame transmitted on channel B |
| | DATA_FRAME_NOT_TXD_ON_CH_B | | | 0 | N/A |
| | DATA_FRAME_TXD_ON_CH_B | | | 1 | N/A |
| 16:21 | CCS | R | RW | 0 | Cycle Count Status<br>Actual cycle count when status was updated.<br>For receive buffers (CFG = '0') the following status bits are updated from both valid data and null frames. If no valid frame was received, the previous value is maintained. For transmit buffers the flags have no meaning and should be ignored. |
| 24 | RCIS | R | RW | 0 | Received on Channel Indicator Status (vSS!Channel)<br>Indicates the channel on which the frame was received.<br>1 = Frame received on channel A<br>0 = Frame received on channel B |
| | CH_B_FRAME_RECEIVED | | | 0 | N/A |
| | CH_A_FRAME_RECEIVED | | | 1 | N/A |
| 25 | SFIS | R | RW | 0 | Startup Frame Indicator Status (vRF!Header!SuFIndicator)<br>A startup frame is marked by the startup frame indicator.<br>1 = The received frame is a startup frame<br>0 = No startup frame received |
| | NO_STARTUP_FRAME_RECEIVED | | | 0 | N/A |
| | STARTUP_FRAME_RECEIVED | | | 1 | N/A |
| 26 | SYNS | R | RW | 0 | Sync Frame Indicator Status (vRF!Header!SyFIndicator)<br>A sync frame is marked by the sync frame indicator.<br>1 = The received frame is a sync frame<br>0 = No sync frame received |
| | NO_SYNC_FRAME_RECEIVED | | | 0 | N/A |
| | SYNC_FRAME_RECEIVED | | | 1 | N/A |
| 27 | NFIS | R | RW | 0 | Null Frame Indicator Status (vRF!Header!NFIndicator)<br>If set to '0' the payload segment of the received frame contains no usable data.<br>1 = Received frame is not a null frame<br>0 = Received frame is a null frame |
| | NULL_FRAME_RECEIVED | | | 0 | N/A |
| | NO_NULL_FRAME_RECEIVED | | | 1 | N/A |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 28 | PPIS | R | RW | 0 | Payload Preamble Indicator Status (vRF!Header!PPIndicator)<br>The payload preamble indicator defines whether a network management vector or message ID is contained within the payload segment of the received frame.<br>1 = Static segment: Network management vector at the beginning of the payload<br>Dynamic segment: Message ID at the beginning of the payload<br>0 = The payload segment of the received frame does not contain a network management vector<br>or a message ID |
| | PAYLOAD_SEGMENT_HAS_NO_NMV_MID | | | 0 | N/A |
| | PAYLOAD_SEGMENT_WITH_NMV_MID | | | 1 | N/A |
| 29 | RESS | R | RW | 0 | Reserved Bit Status (vRF!Header!Reserved)<br>Reflects the state of the received reserved bit. The reserved bit is transmitted as '0'. |

### 15.1.104 FLEXRAY_OBCM_MIR

**Description:** Output Buffer Command Mask (mirror)
**Address:** 0x40560F10
**Offset:** 0xF10
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:2] | | | | | | RDSS [1:1] | RHSS [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:18] | | | | | | RDSH [17:17] | RHSH [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | RHSS | RW | R | 0 | Read Header Section Shadow<br>1 = Header section selected for transfer from Message RAM to Output Buffer<br>0 = Header section is not read |
| | HEADER_SECTION_NOT_READ | | | 0 | N/A |
| | HEADER_SECTION_FOR_MSRAM2OBF_TXFR | | | 1 | N/A |
| 1 | RDSS | RW | R | 0 | Read Data Section Shadow<br>1 = Data section selected for transfer from Message RAM to Output Buffer<br>0 = Data section is not read |
| | DATA_SECTION_NOT_READ | | | 0 | N/A |
| | DATA_SECTION_FOR_MSRAM2OBF_TXFR | | | 1 | N/A |
| 16 | RHSH | R | RW | 0 | Read Header Section Host<br>1 = Header section selected for transfer from Message RAM to Output Buffer<br>0 = Header section is not read |
| | HEADER_SECTION_NOT_READ | | | 0 | N/A |
| | HEADER_SECTION_FOR_MSRAM2OBF_TXFR | | | 1 | N/A |
| 17 | RDSH | R | RW | 0 | Read Data Section Host<br>1 = Data section selected for transfer from Message RAM to Output Buffer<br>0 = Data section is not read |
| | DATA_SECTION_NOT_READ | | | 0 | N/A |
| | DATA_SECTION_FOR_MSRAM2OBF_TXFR | | | 1 | N/A |

### 15.1.105 FLEXRAY_OBCR_MIR

**Description:** Output Buffer Command Request (mirror)
**Address:** 0x40560F14
**Offset:** 0xF14
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:7] | OBRS [6:0] | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | OBSYS [15:15] | None [14:10] | | | | | REQ [9:9] | VIEW [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:23] | OBRH [22:16] | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:6 | OBRS | RW | R | 0 | Output Buffer Request Shadow<br>Number of source message buffer to be transferred from the Message RAM to OBF Shadow.<br>Valid values are 0x00 to 0x7F (0...127). If the number of the first message buffer of the receive<br>FIFO is written to this register the Message Handler transfers the message buffer addressed by<br>the GET Index (GIDX, see [01]Section 5.10 FIFO Function) to OBF Shadow. |
| 8 | VIEW | RW | R | 0 | View Shadow Buffer<br>Toggles between OBF Shadow and OBF Host. Only writeable while OBSYS = '0'.<br>1 = Swap OBF Shadow and OBF Host<br>0 = No action |
| | NO_ACTION | | | 0 | N/A |
| | SWP_OBFS_AND_OBFH | | | 1 | N/A |
| 9 | REQ | RW | R | 0 | Request Message RAM Transfer<br>Requests transfer of message buffer addressed by OBRS[6:0] from Message RAM to OBF<br>Shadow. Only writeable while OBSYS = '0'.<br>1 = Transfer to OBF Shadow requested<br>0 = No request |
| | NO_REQUEST | | | 0 | N/A |
| | TXFR_TO_OBFS_REQ | | | 1 | N/A |
| 15 | OBSYS | R | RW | 0 | Output Buffer Busy Shadow<br>Set to '1' after setting bit REQ. When the transfer between the Message RAM and OBF<br>Shadow has completed, OBSYS is set back to '0'.<br>1 = Transfer between Message RAM and OBF Shadow in progress<br>0 = No transfer in progress |
| | NO_TXFR_IN_PROGRESS | | | 0 | N/A |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| | TXFR_BTW_MSRAM _AND_OBFS | | | 1 | N/A |
| 16:22 | OBRH | R | RW | 0 | Output Buffer Request Host<br>Number of message buffer currently accessible by the Host via RDHS[1...3], MBS, and RDDS[1...64]. By writing VIEW to '1' OBF Shadow and OBF Host are swapped and the transferred message buffer is accessible by the Host. Valid values are 0x00 to 0x7F (0...127). |

# 16 GPIO

**Description** GPIO port control/configuration
**Base Address** 0x40310000
**Size** 0x10000
**Slave Num** MMIO3 - 1

| Register Name | Address | Permission | Description |
|---|---|---|---|
| GPIO_INTR_CAUSE0 | 0x40314000 | FULL | Interrupt port cause register 0 |
| GPIO_INTR_CAUSE1 | 0x40314004 | FULL | Interrupt port cause register 1 |
| GPIO_VDD_ACTIVE | 0x40314010 | FULL | Extern power supply detection register |
| GPIO_VDD_INTR | 0x40314014 | FULL | Supply detection interrupt register |
| GPIO_VDD_INTR_MASK | 0x40314018 | FULL | Supply detection interrupt mask register |
| GPIO_VDD_INTR_MASKED | 0x4031401C | FULL | Supply detection interrupt masked register |
| GPIO_VDD_INTR_SET | 0x40314020 | FULL | Supply detection interrupt set register |

## 16.1 PRT 0

| Register Name | Address | Permission | Description |
|---|---|---|---|
| GPIO_PRT0_OUT | 0x40310000 | FULL | Port output data register<br>Note:OUT4 OUT5 OUT6 OUT7 are not available for this register |
| GPIO_PRT0_OUT_CLR | 0x40310004 | FULL | Port output data clear register |
| GPIO_PRT0_OUT_SET | 0x40310008 | FULL | Port output data set register |
| GPIO_PRT0_OUT_INV | 0x4031000C | FULL | Port output data invert register |
| GPIO_PRT0_IN | 0x40310010 | FULL | Port input state register<br>Note:IN4 IN5 IN6 IN7 are not available for this register |
| GPIO_PRT0_INTR | 0x40310014 | FULL | Port interrupt status register<br>Note:EDGE4 EDGE5 EDGE6 EDGE7 IN_IN4 IN_IN5 IN_IN6 IN_IN7 are not available for this register |
| GPIO_PRT0_INTR_MASK | 0x40310018 | FULL | Port interrupt mask register<br>Note:EDGE4 EDGE5 EDGE6 EDGE7 are not available for this register |
| GPIO_PRT0_INTR_MASKED | 0x4031001C | FULL | Port interrupt masked status register<br>Note:EDGE4 EDGE5 EDGE6 EDGE7 are not available for this register |
| GPIO_PRT0_INTR_SET | 0x40310020 | FULL | Port interrupt set register<br>Note:EDGE4 EDGE5 EDGE6 EDGE7 are not available for this register |
| GPIO_PRT0_INTR_CFG | 0x40310040 | FULL | Port interrupt configuration register<br>Note:EDGE4_SEL EDGE5_SEL EDGE6_SEL EDGE7_SEL are not available for this register |
| GPIO_PRT0_CFG | 0x40310044 | FULL | Port configuration register<br>Note:IN_EN4 IN_EN5 IN_EN6 IN_EN7 are not available for this register |
| GPIO_PRT0_CFG_IN | 0x40310048 | FULL | Port input buffer configuration register<br>Note:VTRIP_SEL4_0 VTRIP_SEL5_0 VTRIP_SEL6_0 VTRIP_SEL7_0 are not available for this register |
| GPIO_PRT0_CFG_OUT | 0x4031004C | FULL | Port output buffer configuration register<br>Note:SLOW4 SLOW5 SLOW6 SLOW7 DRIVE_SEL4 DRIVE_SEL5 DRIVE_SEL6 DRIVE_SEL7 are not available for this register |
| GPIO_PRT0_CFG_IN_AUTOLVL | 0x40310058 | FULL | Port input buffer AUTOLVL configuration register<br>Note:VTRIP_SEL4_1 VTRIP_SEL5_1 VTRIP_SEL6_1 VTRIP_SEL7_1 are not available for this register |

## 16.2 PRT 1

| Register Name | Address | Permission | Description |
|---|---|---|---|
| GPIO_PRT1_OUT | 0x40310080 | FULL | Port output data register<br>Note:OUT7 is not available for this register |
| GPIO_PRT1_OUT_CLR | 0x40310084 | FULL | Port output data clear register |
| GPIO_PRT1_OUT_SET | 0x40310088 | FULL | Port output data set register |
| GPIO_PRT1_OUT_INV | 0x4031008C | FULL | Port output data invert register |
| GPIO_PRT1_IN | 0x40310090 | FULL | Port input state register<br>Note:IN7 is not available for this register |
| GPIO_PRT1_INTR | 0x40310094 | FULL | Port interrupt status register<br>Note:EDGE7 IN_IN7 are not available for this register |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| GPIO_PRT1_INTR_MASK | 0x40310098 | FULL | Port interrupt mask register<br>Note:EDGE7 is not available for this register |
| GPIO_PRT1_INTR_MASKED | 0x4031009C | FULL | Port interrupt masked status register<br>Note:EDGE7 is not available for this register |
| GPIO_PRT1_INTR_SET | 0x403100A0 | FULL | Port interrupt set register<br>Note:EDGE7 is not available for this register |
| GPIO_PRT1_INTR_CFG | 0x403100C0 | FULL | Port interrupt configuration register<br>Note:EDGE7_SEL is not available for this register |
| GPIO_PRT1_CFG | 0x403100C4 | FULL | Port configuration register<br>Note:IN_EN7 is not available for this register |
| GPIO_PRT1_CFG_IN | 0x403100C8 | FULL | Port input buffer configuration register<br>Note:VTRIP_SEL7_0 is not available for this register |
| GPIO_PRT1_CFG_OUT | 0x403100CC | FULL | Port output buffer configuration register<br>Note:SLOW0 SLOW1 SLOW2 SLOW3 SLOW4 SLOW5 SLOW6 SLOW7 DRIVE_SEL7 are not available for this register |
| GPIO_PRT1_CFG_IN_AUTOLVL | 0x403100D8 | FULL | Port input buffer AUTOLVL configuration register<br>Note:VTRIP_SEL7_1 is not available for this register |

## 16.3 PRT 2

| Register Name | Address | Permission | Description |
|---|---|---|---|
| GPIO_PRT2_OUT | 0x40310100 | FULL | Port output data register |
| GPIO_PRT2_OUT_CLR | 0x40310104 | FULL | Port output data clear register |
| GPIO_PRT2_OUT_SET | 0x40310108 | FULL | Port output data set register |
| GPIO_PRT2_OUT_INV | 0x4031010C | FULL | Port output data invert register |
| GPIO_PRT2_IN | 0x40310110 | FULL | Port input state register |
| GPIO_PRT2_INTR | 0x40310114 | FULL | Port interrupt status register |
| GPIO_PRT2_INTR_MASK | 0x40310118 | FULL | Port interrupt mask register |
| GPIO_PRT2_INTR_MASKED | 0x4031011C | FULL | Port interrupt masked status register |
| GPIO_PRT2_INTR_SET | 0x40310120 | FULL | Port interrupt set register |
| GPIO_PRT2_INTR_CFG | 0x40310140 | FULL | Port interrupt configuration register |
| GPIO_PRT2_CFG | 0x40310144 | FULL | Port configuration register |
| GPIO_PRT2_CFG_IN | 0x40310148 | FULL | Port input buffer configuration register |
| GPIO_PRT2_CFG_OUT | 0x4031014C | FULL | Port output buffer configuration register<br>Note:SLOW0 SLOW1 SLOW2 SLOW3 SLOW4 SLOW5 SLOW6 SLOW7 are not available for this register |
| GPIO_PRT2_CFG_IN_AUTOLVL | 0x40310158 | FULL | Port input buffer AUTOLVL configuration register |

## 16.4 PRT 3

| Register Name | Address | Permission | Description |
|---|---|---|---|
| GPIO_PRT3_OUT | 0x40310180 | FULL | Port output data register |
| GPIO_PRT3_OUT_CLR | 0x40310184 | FULL | Port output data clear register |
| GPIO_PRT3_OUT_SET | 0x40310188 | FULL | Port output data set register |
| GPIO_PRT3_OUT_INV | 0x4031018C | FULL | Port output data invert register |
| GPIO_PRT3_IN | 0x40310190 | FULL | Port input state register |
| GPIO_PRT3_INTR | 0x40310194 | FULL | Port interrupt status register |
| GPIO_PRT3_INTR_MASK | 0x40310198 | FULL | Port interrupt mask register |
| GPIO_PRT3_INTR_MASKED | 0x4031019C | FULL | Port interrupt masked status register |
| GPIO_PRT3_INTR_SET | 0x403101A0 | FULL | Port interrupt set register |
| GPIO_PRT3_INTR_CFG | 0x403101C0 | FULL | Port interrupt configuration register |
| GPIO_PRT3_CFG | 0x403101C4 | FULL | Port configuration register |
| GPIO_PRT3_CFG_IN | 0x403101C8 | FULL | Port input buffer configuration register |
| GPIO_PRT3_CFG_OUT | 0x403101CC | FULL | Port output buffer configuration register<br>Note:SLOW0 SLOW1 SLOW2 SLOW3 SLOW4 SLOW5 SLOW6 SLOW7 are not available for this register |
| GPIO_PRT3_CFG_IN_AUTOLVL | 0x403101D8 | FULL | Port input buffer AUTOLVL configuration register |

## 16.5 PRT 4

| Register Name | Address | Permission | Description |
|---|---|---|---|
| GPIO_PRT4_OUT | 0x40310200 | FULL | Port output data register<br>Note:OUT7 is not available for this register |
| GPIO_PRT4_OUT_CLR | 0x40310204 | FULL | Port output data clear register |
| GPIO_PRT4_OUT_SET | 0x40310208 | FULL | Port output data set register |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| GPIO_PRT4_OUT_INV | 0x4031020C | FULL | Port output data invert register |
| GPIO_PRT4_IN | 0x40310210 | FULL | Port input state register<br>Note:IN7 is not available for this register |
| GPIO_PRT4_INTR | 0x40310214 | FULL | Port interrupt status register<br>Note:EDGE7 IN_IN7 are not available for this register |
| GPIO_PRT4_INTR_MASK | 0x40310218 | FULL | Port interrupt mask register<br>Note:EDGE7 is not available for this register |
| GPIO_PRT4_INTR_MASKED | 0x4031021C | FULL | Port interrupt masked status register<br>Note:EDGE7 is not available for this register |
| GPIO_PRT4_INTR_SET | 0x40310220 | FULL | Port interrupt set register<br>Note:EDGE7 is not available for this register |
| GPIO_PRT4_INTR_CFG | 0x40310240 | FULL | Port interrupt configuration register<br>Note:EDGE7_SEL is not available for this register |
| GPIO_PRT4_CFG | 0x40310244 | FULL | Port configuration register<br>Note:IN_EN7 is not available for this register |
| GPIO_PRT4_CFG_IN | 0x40310248 | FULL | Port input buffer configuration register<br>Note:VTRIP_SEL7_0 is not available for this register |
| GPIO_PRT4_CFG_OUT | 0x4031024C | FULL | Port output buffer configuration register<br>Note:SLOW0 SLOW1 SLOW2 SLOW3 SLOW4 SLOW5 SLOW6 SLOW7 DRIVE_SEL7 are not available for this register |
| GPIO_PRT4_CFG_IN_AUTOLVL | 0x40310258 | FULL | Port input buffer AUTOLVL configuration register<br>Note:VTRIP_SEL7_1 is not available for this register |

## 16.6 PRT 5

| Register Name | Address | Permission | Description |
|---|---|---|---|
| GPIO_PRT5_OUT | 0x40310280 | FULL | Port output data register<br>Note:OUT6 OUT7 are not available for this register |
| GPIO_PRT5_OUT_CLR | 0x40310284 | FULL | Port output data clear register |
| GPIO_PRT5_OUT_SET | 0x40310288 | FULL | Port output data set register |
| GPIO_PRT5_OUT_INV | 0x4031028C | FULL | Port output data invert register |
| GPIO_PRT5_IN | 0x40310290 | FULL | Port input state register<br>Note:IN6 IN7 are not available for this register |
| GPIO_PRT5_INTR | 0x40310294 | FULL | Port interrupt status register<br>Note:EDGE6 EDGE7 IN_IN6 IN_IN7 are not available for this register |
| GPIO_PRT5_INTR_MASK | 0x40310298 | FULL | Port interrupt mask register<br>Note:EDGE6 EDGE7 are not available for this register |
| GPIO_PRT5_INTR_MASKED | 0x4031029C | FULL | Port interrupt masked status register<br>Note:EDGE6 EDGE7 are not available for this register |
| GPIO_PRT5_INTR_SET | 0x403102A0 | FULL | Port interrupt set register<br>Note:EDGE6 EDGE7 are not available for this register |
| GPIO_PRT5_INTR_CFG | 0x403102C0 | FULL | Port interrupt configuration register<br>Note:EDGE6_SEL EDGE7_SEL are not available for this register |
| GPIO_PRT5_CFG | 0x403102C4 | FULL | Port configuration register<br>Note:IN_EN6 IN_EN7 are not available for this register |
| GPIO_PRT5_CFG_IN | 0x403102C8 | FULL | Port input buffer configuration register<br>Note:VTRIP_SEL6_0 VTRIP_SEL7_0 are not available for this register |
| GPIO_PRT5_CFG_OUT | 0x403102CC | FULL | Port output buffer configuration register<br>Note:SLOW0 SLOW1 SLOW2 SLOW3 SLOW4 SLOW5 SLOW6 SLOW7 DRIVE_SEL6 DRIVE_SEL7 are not available for this register |
| GPIO_PRT5_CFG_IN_AUTOLVL | 0x403102D8 | FULL | Port input buffer AUTOLVL configuration register<br>Note:VTRIP_SEL6_1 VTRIP_SEL7_1 are not available for this register |

## 16.7 PRT 6

| Register Name | Address | Permission | Description |
|---|---|---|---|
| GPIO_PRT6_OUT | 0x40310300 | FULL | Port output data register |
| GPIO_PRT6_OUT_CLR | 0x40310304 | FULL | Port output data clear register |
| GPIO_PRT6_OUT_SET | 0x40310308 | FULL | Port output data set register |
| GPIO_PRT6_OUT_INV | 0x4031030C | FULL | Port output data invert register |
| GPIO_PRT6_IN | 0x40310310 | FULL | Port input state register |
| GPIO_PRT6_INTR | 0x40310314 | FULL | Port interrupt status register |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| GPIO_PRT6_INTR_MASK | 0x40310318 | FULL | Port interrupt mask register |
| GPIO_PRT6_INTR_MASKED | 0x4031031C | FULL | Port interrupt masked status register |
| GPIO_PRT6_INTR_SET | 0x40310320 | FULL | Port interrupt set register |
| GPIO_PRT6_INTR_CFG | 0x40310340 | FULL | Port interrupt configuration register |
| GPIO_PRT6_CFG | 0x40310344 | FULL | Port configuration register |
| GPIO_PRT6_CFG_IN | 0x40310348 | FULL | Port input buffer configuration register |
| GPIO_PRT6_CFG_OUT | 0x4031034C | FULL | Port output buffer configuration register<br>Note:SLOW0 SLOW1 SLOW2 SLOW3 SLOW4 SLOW5 SLOW6 SLOW7 are not available for this register |
| GPIO_PRT6_CFG_IN_AUTOLVL | 0x40310358 | FULL | Port input buffer AUTOLVL configuration register |

## 16.8 PRT 7

| Register Name | Address | Permission | Description |
|---|---|---|---|
| GPIO_PRT7_OUT | 0x40310380 | FULL | Port output data register |
| GPIO_PRT7_OUT_CLR | 0x40310384 | FULL | Port output data clear register |
| GPIO_PRT7_OUT_SET | 0x40310388 | FULL | Port output data set register |
| GPIO_PRT7_OUT_INV | 0x4031038C | FULL | Port output data invert register |
| GPIO_PRT7_IN | 0x40310390 | FULL | Port input state register |
| GPIO_PRT7_INTR | 0x40310394 | FULL | Port interrupt status register |
| GPIO_PRT7_INTR_MASK | 0x40310398 | FULL | Port interrupt mask register |
| GPIO_PRT7_INTR_MASKED | 0x4031039C | FULL | Port interrupt masked status register |
| GPIO_PRT7_INTR_SET | 0x403103A0 | FULL | Port interrupt set register |
| GPIO_PRT7_INTR_CFG | 0x403103C0 | FULL | Port interrupt configuration register |
| GPIO_PRT7_CFG | 0x403103C4 | FULL | Port configuration register |
| GPIO_PRT7_CFG_IN | 0x403103C8 | FULL | Port input buffer configuration register |
| GPIO_PRT7_CFG_OUT | 0x403103CC | FULL | Port output buffer configuration register<br>Note:SLOW0 SLOW1 SLOW2 SLOW3 SLOW4 SLOW5 SLOW6 SLOW7 are not available for this register |
| GPIO_PRT7_CFG_IN_AUTOLVL | 0x403103D8 | FULL | Port input buffer AUTOLVL configuration register |

## 16.9 PRT 8

| Register Name | Address | Permission | Description |
|---|---|---|---|
| GPIO_PRT8_OUT | 0x40310400 | FULL | Port output data register<br>Note:OUT5 OUT6 OUT7 are not available for this register |
| GPIO_PRT8_OUT_CLR | 0x40310404 | FULL | Port output data clear register |
| GPIO_PRT8_OUT_SET | 0x40310408 | FULL | Port output data set register |
| GPIO_PRT8_OUT_INV | 0x4031040C | FULL | Port output data invert register |
| GPIO_PRT8_IN | 0x40310410 | FULL | Port input state register<br>Note:IN5 IN6 IN7 are not available for this register |
| GPIO_PRT8_INTR | 0x40310414 | FULL | Port interrupt status register<br>Note:EDGE5 EDGE6 EDGE7 IN_IN5 IN_IN6 IN_IN7 are not available for this register |
| GPIO_PRT8_INTR_MASK | 0x40310418 | FULL | Port interrupt mask register<br>Note:EDGE5 EDGE6 EDGE7 are not available for this register |
| GPIO_PRT8_INTR_MASKED | 0x4031041C | FULL | Port interrupt masked status register<br>Note:EDGE5 EDGE6 EDGE7 are not available for this register |
| GPIO_PRT8_INTR_SET | 0x40310420 | FULL | Port interrupt set register<br>Note:EDGE5 EDGE6 EDGE7 are not available for this register |
| GPIO_PRT8_INTR_CFG | 0x40310440 | FULL | Port interrupt configuration register<br>Note:EDGE5_SEL EDGE6_SEL EDGE7_SEL are not available for this register |
| GPIO_PRT8_CFG | 0x40310444 | FULL | Port configuration register<br>Note:IN_EN5 IN_EN6 IN_EN7 are not available for this register |
| GPIO_PRT8_CFG_IN | 0x40310448 | FULL | Port input buffer configuration register<br>Note:VTRIP_SEL5_0 VTRIP_SEL6_0 VTRIP_SEL7_0 are not available for this register |
| GPIO_PRT8_CFG_OUT | 0x4031044C | FULL | Port output buffer configuration register<br>Note:SLOW0 SLOW1 SLOW2 SLOW3 SLOW4 SLOW5 SLOW6 SLOW7 DRIVE_SEL5 DRIVE_SEL6 DRIVE_SEL7 are not available for this register |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| GPIO_PRT8_CFG_IN_AUTOLVL | 0x40310458 | FULL | Port input buffer AUTOLVL configuration register<br>Note:VTRIP_SEL5_1 VTRIP_SEL6_1 VTRIP_SEL7_1 are not available for this register |

## 16.10 PRT 9

| Register Name | Address | Permission | Description |
|---|---|---|---|
| GPIO_PRT9_OUT | 0x40310480 | FULL | Port output data register<br>Note:OUT4 OUT5 OUT6 OUT7 are not available for this register |
| GPIO_PRT9_OUT_CLR | 0x40310484 | FULL | Port output data clear register |
| GPIO_PRT9_OUT_SET | 0x40310488 | FULL | Port output data set register |
| GPIO_PRT9_OUT_INV | 0x4031048C | FULL | Port output data invert register |
| GPIO_PRT9_IN | 0x40310490 | FULL | Port input state register<br>Note:IN4 IN5 IN6 IN7 are not available for this register |
| GPIO_PRT9_INTR | 0x40310494 | FULL | Port interrupt status register<br>Note:EDGE4 EDGE5 EDGE6 EDGE7 IN_IN4 IN_IN5 IN_IN6 IN_IN7 are not available for this register |
| GPIO_PRT9_INTR_MASK | 0x40310498 | FULL | Port interrupt mask register<br>Note:EDGE4 EDGE5 EDGE6 EDGE7 are not available for this register |
| GPIO_PRT9_INTR_MASKED | 0x4031049C | FULL | Port interrupt masked status register<br>Note:EDGE4 EDGE5 EDGE6 EDGE7 are not available for this register |
| GPIO_PRT9_INTR_SET | 0x403104A0 | FULL | Port interrupt set register<br>Note:EDGE4 EDGE5 EDGE6 EDGE7 are not available for this register |
| GPIO_PRT9_INTR_CFG | 0x403104C0 | FULL | Port interrupt configuration register<br>Note:EDGE4_SEL EDGE5_SEL EDGE6_SEL EDGE7_SEL are not available for this register |
| GPIO_PRT9_CFG | 0x403104C4 | FULL | Port configuration register<br>Note:IN_EN4 IN_EN5 IN_EN6 IN_EN7 are not available for this register |
| GPIO_PRT9_CFG_IN | 0x403104C8 | FULL | Port input buffer configuration register<br>Note:VTRIP_SEL4_0 VTRIP_SEL5_0 VTRIP_SEL6_0 VTRIP_SEL7_0 are not available for this register |
| GPIO_PRT9_CFG_OUT | 0x403104CC | FULL | Port output buffer configuration register<br>Note:SLOW0 SLOW1 SLOW2 SLOW3 SLOW4 SLOW5 SLOW6 SLOW7 DRIVE_SEL4 DRIVE_SEL5 DRIVE_SEL6 DRIVE_SEL7 are not available for this register |
| GPIO_PRT9_CFG_IN_AUTOLVL | 0x403104D8 | FULL | Port input buffer AUTOLVL configuration register<br>Note:VTRIP_SEL4_1 VTRIP_SEL5_1 VTRIP_SEL6_1 VTRIP_SEL7_1 are not available for this register |

## 16.11 PRT 10

| Register Name | Address | Permission | Description |
|---|---|---|---|
| GPIO_PRT10_OUT | 0x40310500 | FULL | Port output data register |
| GPIO_PRT10_OUT_CLR | 0x40310504 | FULL | Port output data clear register |
| GPIO_PRT10_OUT_SET | 0x40310508 | FULL | Port output data set register |
| GPIO_PRT10_OUT_INV | 0x4031050C | FULL | Port output data invert register |
| GPIO_PRT10_IN | 0x40310510 | FULL | Port input state register |
| GPIO_PRT10_INTR | 0x40310514 | FULL | Port interrupt status register |
| GPIO_PRT10_INTR_MASK | 0x40310518 | FULL | Port interrupt mask register |
| GPIO_PRT10_INTR_MASKED | 0x4031051C | FULL | Port interrupt masked status register |
| GPIO_PRT10_INTR_SET | 0x40310520 | FULL | Port interrupt set register |
| GPIO_PRT10_INTR_CFG | 0x40310540 | FULL | Port interrupt configuration register |
| GPIO_PRT10_CFG | 0x40310544 | FULL | Port configuration register |
| GPIO_PRT10_CFG_IN | 0x40310548 | FULL | Port input buffer configuration register |
| GPIO_PRT10_CFG_OUT | 0x4031054C | FULL | Port output buffer configuration register<br>Note:SLOW0 SLOW1 SLOW2 SLOW3 SLOW4 SLOW5 SLOW6 SLOW7 are not available for this register |
| GPIO_PRT10_CFG_IN_AUTOLVL | 0x40310558 | FULL | Port input buffer AUTOLVL configuration register |

## 16.12 PRT 11

| Register Name | Address | Permission | Description |
|---|---|---|---|
| GPIO_PRT11_OUT | 0x40310580 | FULL | Port output data register<br>Note:OUT3 OUT4 OUT5 OUT6 OUT7 are not available for this register |
| GPIO_PRT11_OUT_CLR | 0x40310584 | FULL | Port output data clear register |
| GPIO_PRT11_OUT_SET | 0x40310588 | FULL | Port output data set register |
| GPIO_PRT11_OUT_INV | 0x4031058C | FULL | Port output data invert register |
| GPIO_PRT11_IN | 0x40310590 | FULL | Port input state register<br>Note:IN3 IN4 IN5 IN6 IN7 are not available for this register |
| GPIO_PRT11_INTR | 0x40310594 | FULL | Port interrupt status register<br>Note:EDGE3 EDGE4 EDGE5 EDGE6 EDGE7 IN_IN3 IN_IN4 IN_IN5 IN_IN6 IN_IN7 are not available for this register |
| GPIO_PRT11_INTR_MASK | 0x40310598 | FULL | Port interrupt mask register<br>Note:EDGE3 EDGE4 EDGE5 EDGE6 EDGE7 are not available for this register |
| GPIO_PRT11_INTR_MASKED | 0x4031059C | FULL | Port interrupt masked status register<br>Note:EDGE3 EDGE4 EDGE5 EDGE6 EDGE7 are not available for this register |
| GPIO_PRT11_INTR_SET | 0x403105A0 | FULL | Port interrupt set register<br>Note:EDGE3 EDGE4 EDGE5 EDGE6 EDGE7 are not available for this register |
| GPIO_PRT11_INTR_CFG | 0x403105C0 | FULL | Port interrupt configuration register<br>Note:EDGE3_SEL EDGE4_SEL EDGE5_SEL EDGE6_SEL EDGE7_SEL are not available for this register |
| GPIO_PRT11_CFG | 0x403105C4 | FULL | Port configuration register<br>Note:IN_EN3 IN_EN4 IN_EN5 IN_EN6 IN_EN7 are not available for this register |
| GPIO_PRT11_CFG_IN | 0x403105C8 | FULL | Port input buffer configuration register<br>Note:VTRIP_SEL3_0 VTRIP_SEL4_0 VTRIP_SEL5_0 VTRIP_SEL6_0 VTRIP_SEL7_0 are not available for this register |
| GPIO_PRT11_CFG_OUT | 0x403105CC | FULL | Port output buffer configuration register<br>Note:SLOW0 SLOW1 SLOW2 SLOW3 SLOW4 SLOW5 SLOW6 SLOW7 DRIVE_SEL3 DRIVE_SEL4 DRIVE_SEL5 DRIVE_SEL6 DRIVE_SEL7 are not available for this register |
| GPIO_PRT11_CFG_IN_AUTOLVL | 0x403105D8 | FULL | Port input buffer AUTOLVL configuration register<br>Note:VTRIP_SEL3_1 VTRIP_SEL4_1 VTRIP_SEL5_1 VTRIP_SEL6_1 VTRIP_SEL7_1 are not available for this register |

## 16.13 PRT 12

| Register Name | Address | Permission | Description |
|---|---|---|---|
| GPIO_PRT12_OUT | 0x40310600 | FULL | Port output data register |
| GPIO_PRT12_OUT_CLR | 0x40310604 | FULL | Port output data clear register |
| GPIO_PRT12_OUT_SET | 0x40310608 | FULL | Port output data set register |
| GPIO_PRT12_OUT_INV | 0x4031060C | FULL | Port output data invert register |
| GPIO_PRT12_IN | 0x40310610 | FULL | Port input state register |
| GPIO_PRT12_INTR | 0x40310614 | FULL | Port interrupt status register |
| GPIO_PRT12_INTR_MASK | 0x40310618 | FULL | Port interrupt mask register |
| GPIO_PRT12_INTR_MASKED | 0x4031061C | FULL | Port interrupt masked status register |
| GPIO_PRT12_INTR_SET | 0x40310620 | FULL | Port interrupt set register |
| GPIO_PRT12_INTR_CFG | 0x40310640 | FULL | Port interrupt configuration register |
| GPIO_PRT12_CFG | 0x40310644 | FULL | Port configuration register |
| GPIO_PRT12_CFG_IN | 0x40310648 | FULL | Port input buffer configuration register |
| GPIO_PRT12_CFG_OUT | 0x4031064C | FULL | Port output buffer configuration register<br>Note:SLOW0 SLOW1 SLOW2 SLOW3 SLOW4 SLOW5 SLOW6 SLOW7 are not available for this register |
| GPIO_PRT12_CFG_IN_AUTOLVL | 0x40310658 | FULL | Port input buffer AUTOLVL configuration register |

## 16.14 PRT 13

| Register Name | Address | Permission | Description |
|---|---|---|---|
| GPIO_PRT13_OUT | 0x40310680 | FULL | Port output data register |
| GPIO_PRT13_OUT_CLR | 0x40310684 | FULL | Port output data clear register |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| GPIO_PRT13_OUT_SET | 0x40310688 | FULL | Port output data set register |
| GPIO_PRT13_OUT_INV | 0x4031068C | FULL | Port output data invert register |
| GPIO_PRT13_IN | 0x40310690 | FULL | Port input state register |
| GPIO_PRT13_INTR | 0x40310694 | FULL | Port interrupt status register |
| GPIO_PRT13_INTR_MASK | 0x40310698 | FULL | Port interrupt mask register |
| GPIO_PRT13_INTR_MASKED | 0x4031069C | FULL | Port interrupt masked status register |
| GPIO_PRT13_INTR_SET | 0x403106A0 | FULL | Port interrupt set register |
| GPIO_PRT13_INTR_CFG | 0x403106C0 | FULL | Port interrupt configuration register |
| GPIO_PRT13_CFG | 0x403106C4 | FULL | Port configuration register |
| GPIO_PRT13_CFG_IN | 0x403106C8 | FULL | Port input buffer configuration register |
| GPIO_PRT13_CFG_OUT | 0x403106CC | FULL | Port output buffer configuration register<br>Note:SLOW0 SLOW1 SLOW2 SLOW3 SLOW4 SLOW5 SLOW6 SLOW7 are not available for this register |
| GPIO_PRT13_CFG_IN_AUTOLVL | 0x403106D8 | FULL | Port input buffer AUTOLVL configuration register |

## 16.15 PRT 14

| Register Name | Address | Permission | Description |
|---|---|---|---|
| GPIO_PRT14_OUT | 0x40310700 | FULL | Port output data register |
| GPIO_PRT14_OUT_CLR | 0x40310704 | FULL | Port output data clear register |
| GPIO_PRT14_OUT_SET | 0x40310708 | FULL | Port output data set register |
| GPIO_PRT14_OUT_INV | 0x4031070C | FULL | Port output data invert register |
| GPIO_PRT14_IN | 0x40310710 | FULL | Port input state register |
| GPIO_PRT14_INTR | 0x40310714 | FULL | Port interrupt status register |
| GPIO_PRT14_INTR_MASK | 0x40310718 | FULL | Port interrupt mask register |
| GPIO_PRT14_INTR_MASKED | 0x4031071C | FULL | Port interrupt masked status register |
| GPIO_PRT14_INTR_SET | 0x40310720 | FULL | Port interrupt set register |
| GPIO_PRT14_INTR_CFG | 0x40310740 | FULL | Port interrupt configuration register |
| GPIO_PRT14_CFG | 0x40310744 | FULL | Port configuration register |
| GPIO_PRT14_CFG_IN | 0x40310748 | FULL | Port input buffer configuration register |
| GPIO_PRT14_CFG_OUT | 0x4031074C | FULL | Port output buffer configuration register<br>Note:SLOW0 SLOW1 SLOW2 SLOW3 SLOW4 SLOW5 SLOW6 SLOW7 are not available for this register |
| GPIO_PRT14_CFG_IN_AUTOLVL | 0x40310758 | FULL | Port input buffer AUTOLVL configuration register |

## 16.16 PRT 15

| Register Name | Address | Permission | Description |
|---|---|---|---|
| GPIO_PRT15_OUT | 0x40310780 | FULL | Port output data register<br>Note:OUT4 OUT5 OUT6 OUT7 are not available for this register |
| GPIO_PRT15_OUT_CLR | 0x40310784 | FULL | Port output data clear register |
| GPIO_PRT15_OUT_SET | 0x40310788 | FULL | Port output data set register |
| GPIO_PRT15_OUT_INV | 0x4031078C | FULL | Port output data invert register |
| GPIO_PRT15_IN | 0x40310790 | FULL | Port input state register<br>Note:IN4 IN5 IN6 IN7 are not available for this register |
| GPIO_PRT15_INTR | 0x40310794 | FULL | Port interrupt status register<br>Note:EDGE4 EDGE5 EDGE6 EDGE7 IN_IN4 IN_IN5 IN_IN6 IN_IN7 are not available for this register |
| GPIO_PRT15_INTR_MASK | 0x40310798 | FULL | Port interrupt mask register<br>Note:EDGE4 EDGE5 EDGE6 EDGE7 are not available for this register |
| GPIO_PRT15_INTR_MASKED | 0x4031079C | FULL | Port interrupt masked status register<br>Note:EDGE4 EDGE5 EDGE6 EDGE7 are not available for this register |
| GPIO_PRT15_INTR_SET | 0x403107A0 | FULL | Port interrupt set register<br>Note:EDGE4 EDGE5 EDGE6 EDGE7 are not available for this register |
| GPIO_PRT15_INTR_CFG | 0x403107C0 | FULL | Port interrupt configuration register<br>Note:EDGE4_SEL EDGE5_SEL EDGE6_SEL EDGE7_SEL are not available for this register |
| GPIO_PRT15_CFG | 0x403107C4 | FULL | Port configuration register<br>Note:IN_EN4 IN_EN5 IN_EN6 IN_EN7 are not available for this register |
| GPIO_PRT15_CFG_IN | 0x403107C8 | FULL | Port input buffer configuration register<br>Note:VTRIP_SEL4_0 VTRIP_SEL5_0 VTRIP_SEL6_0 VTRIP_SEL7_0 are not available for this register |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| GPIO_PRT15_CFG_OUT | 0x403107CC | FULL | Port output buffer configuration register<br>Note:SLOW0 SLOW1 SLOW2 SLOW3 SLOW4 SLOW5 SLOW6 SLOW7 DRIVE_SEL4 DRIVE_SEL5 DRIVE_SEL6 DRIVE_SEL7 are not available for this register |
| GPIO_PRT15_CFG_IN_AUTOLVL | 0x403107D8 | FULL | Port input buffer AUTOLVL configuration register<br>Note:VTRIP_SEL4_1 VTRIP_SEL5_1 VTRIP_SEL6_1 VTRIP_SEL7_1 are not available for this register |

## 16.17 PRT 16

| Register Name | Address | Permission | Description |
|---|---|---|---|
| GPIO_PRT16_OUT | 0x40310800 | FULL | Port output data register |
| GPIO_PRT16_OUT_CLR | 0x40310804 | FULL | Port output data clear register |
| GPIO_PRT16_OUT_SET | 0x40310808 | FULL | Port output data set register |
| GPIO_PRT16_OUT_INV | 0x4031080C | FULL | Port output data invert register |
| GPIO_PRT16_IN | 0x40310810 | FULL | Port input state register |
| GPIO_PRT16_INTR | 0x40310814 | FULL | Port interrupt status register |
| GPIO_PRT16_INTR_MASK | 0x40310818 | FULL | Port interrupt mask register |
| GPIO_PRT16_INTR_MASKED | 0x4031081C | FULL | Port interrupt masked status register |
| GPIO_PRT16_INTR_SET | 0x40310820 | FULL | Port interrupt set register |
| GPIO_PRT16_INTR_CFG | 0x40310840 | FULL | Port interrupt configuration register |
| GPIO_PRT16_CFG | 0x40310844 | FULL | Port configuration register |
| GPIO_PRT16_CFG_IN | 0x40310848 | FULL | Port input buffer configuration register |
| GPIO_PRT16_CFG_OUT | 0x4031084C | FULL | Port output buffer configuration register<br>Note:SLOW0 SLOW1 SLOW2 SLOW3 SLOW4 SLOW5 SLOW6 SLOW7 are not available for this register |
| GPIO_PRT16_CFG_IN_AUTOLVL | 0x40310858 | FULL | Port input buffer AUTOLVL configuration register |

## 16.18 PRT 17

| Register Name | Address | Permission | Description |
|---|---|---|---|
| GPIO_PRT17_OUT | 0x40310880 | FULL | Port output data register |
| GPIO_PRT17_OUT_CLR | 0x40310884 | FULL | Port output data clear register |
| GPIO_PRT17_OUT_SET | 0x40310888 | FULL | Port output data set register |
| GPIO_PRT17_OUT_INV | 0x4031088C | FULL | Port output data invert register |
| GPIO_PRT17_IN | 0x40310890 | FULL | Port input state register |
| GPIO_PRT17_INTR | 0x40310894 | FULL | Port interrupt status register |
| GPIO_PRT17_INTR_MASK | 0x40310898 | FULL | Port interrupt mask register |
| GPIO_PRT17_INTR_MASKED | 0x4031089C | FULL | Port interrupt masked status register |
| GPIO_PRT17_INTR_SET | 0x403108A0 | FULL | Port interrupt set register |
| GPIO_PRT17_INTR_CFG | 0x403108C0 | FULL | Port interrupt configuration register |
| GPIO_PRT17_CFG | 0x403108C4 | FULL | Port configuration register |
| GPIO_PRT17_CFG_IN | 0x403108C8 | FULL | Port input buffer configuration register |
| GPIO_PRT17_CFG_OUT | 0x403108CC | FULL | Port output buffer configuration register<br>Note:SLOW0 SLOW1 SLOW2 SLOW3 SLOW4 SLOW5 SLOW6 SLOW7 are not available for this register |
| GPIO_PRT17_CFG_IN_AUTOLVL | 0x403108D8 | FULL | Port input buffer AUTOLVL configuration register |

## 16.19 PRT 18

| Register Name | Address | Permission | Description |
|---|---|---|---|
| GPIO_PRT18_OUT | 0x40310900 | FULL | Port output data register |
| GPIO_PRT18_OUT_CLR | 0x40310904 | FULL | Port output data clear register |
| GPIO_PRT18_OUT_SET | 0x40310908 | FULL | Port output data set register |
| GPIO_PRT18_OUT_INV | 0x4031090C | FULL | Port output data invert register |
| GPIO_PRT18_IN | 0x40310910 | FULL | Port input state register |
| GPIO_PRT18_INTR | 0x40310914 | FULL | Port interrupt status register |
| GPIO_PRT18_INTR_MASK | 0x40310918 | FULL | Port interrupt mask register |
| GPIO_PRT18_INTR_MASKED | 0x4031091C | FULL | Port interrupt masked status register |
| GPIO_PRT18_INTR_SET | 0x40310920 | FULL | Port interrupt set register |
| GPIO_PRT18_INTR_CFG | 0x40310940 | FULL | Port interrupt configuration register |
| GPIO_PRT18_CFG | 0x40310944 | FULL | Port configuration register |
| GPIO_PRT18_CFG_IN | 0x40310948 | FULL | Port input buffer configuration register |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| GPIO_PRT18_CFG_OUT | 0x4031094C | FULL | Port output buffer configuration register<br>Note:SLOW0 SLOW1 SLOW2 SLOW3 SLOW4 SLOW5 SLOW6 SLOW7 are not available for this register |
| GPIO_PRT18_CFG_IN_AUTOLVL | 0x40310958 | FULL | Port input buffer AUTOLVL configuration register |

## 16.20 PRT 19

| Register Name | Address | Permission | Description |
|---|---|---|---|
| GPIO_PRT19_OUT | 0x40310980 | FULL | Port output data register<br>Note:OUT5 OUT6 OUT7 are not available for this register |
| GPIO_PRT19_OUT_CLR | 0x40310984 | FULL | Port output data clear register |
| GPIO_PRT19_OUT_SET | 0x40310988 | FULL | Port output data set register |
| GPIO_PRT19_OUT_INV | 0x4031098C | FULL | Port output data invert register |
| GPIO_PRT19_IN | 0x40310990 | FULL | Port input state register<br>Note:IN5 IN6 IN7 are not available for this register |
| GPIO_PRT19_INTR | 0x40310994 | FULL | Port interrupt status register<br>Note:EDGE5 EDGE6 EDGE7 IN_IN5 IN_IN6 IN_IN7 are not available for this register |
| GPIO_PRT19_INTR_MASK | 0x40310998 | FULL | Port interrupt mask register<br>Note:EDGE5 EDGE6 EDGE7 are not available for this register |
| GPIO_PRT19_INTR_MASKED | 0x4031099C | FULL | Port interrupt masked status register<br>Note:EDGE5 EDGE6 EDGE7 are not available for this register |
| GPIO_PRT19_INTR_SET | 0x403109A0 | FULL | Port interrupt set register<br>Note:EDGE5 EDGE6 EDGE7 are not available for this register |
| GPIO_PRT19_INTR_CFG | 0x403109C0 | FULL | Port interrupt configuration register<br>Note:EDGE5_SEL EDGE6_SEL EDGE7_SEL are not available for this register |
| GPIO_PRT19_CFG | 0x403109C4 | FULL | Port configuration register<br>Note:IN_EN5 IN_EN6 IN_EN7 are not available for this register |
| GPIO_PRT19_CFG_IN | 0x403109C8 | FULL | Port input buffer configuration register<br>Note:VTRIP_SEL5_0 VTRIP_SEL6_0 VTRIP_SEL7_0 are not available for this register |
| GPIO_PRT19_CFG_OUT | 0x403109CC | FULL | Port output buffer configuration register<br>Note:SLOW0 SLOW1 SLOW2 SLOW3 SLOW4 SLOW5 SLOW6 SLOW7 DRIVE_SEL5 DRIVE_SEL6 DRIVE_SEL7 are not available for this register |
| GPIO_PRT19_CFG_IN_AUTOLVL | 0x403109D8 | FULL | Port input buffer AUTOLVL configuration register<br>Note:VTRIP_SEL5_1 VTRIP_SEL6_1 VTRIP_SEL7_1 are not available for this register |

## 16.21 PRT 20

| Register Name | Address | Permission | Description |
|---|---|---|---|
| GPIO_PRT20_OUT | 0x40310A00 | FULL | Port output data register |
| GPIO_PRT20_OUT_CLR | 0x40310A04 | FULL | Port output data clear register |
| GPIO_PRT20_OUT_SET | 0x40310A08 | FULL | Port output data set register |
| GPIO_PRT20_OUT_INV | 0x40310A0C | FULL | Port output data invert register |
| GPIO_PRT20_IN | 0x40310A10 | FULL | Port input state register |
| GPIO_PRT20_INTR | 0x40310A14 | FULL | Port interrupt status register |
| GPIO_PRT20_INTR_MASK | 0x40310A18 | FULL | Port interrupt mask register |
| GPIO_PRT20_INTR_MASKED | 0x40310A1C | FULL | Port interrupt masked status register |
| GPIO_PRT20_INTR_SET | 0x40310A20 | FULL | Port interrupt set register |
| GPIO_PRT20_INTR_CFG | 0x40310A40 | FULL | Port interrupt configuration register |
| GPIO_PRT20_CFG | 0x40310A44 | FULL | Port configuration register |
| GPIO_PRT20_CFG_IN | 0x40310A48 | FULL | Port input buffer configuration register |
| GPIO_PRT20_CFG_OUT | 0x40310A4C | FULL | Port output buffer configuration register<br>Note:SLOW0 SLOW1 SLOW2 SLOW3 SLOW4 SLOW5 SLOW6 SLOW7 are not available for this register |
| GPIO_PRT20_CFG_IN_AUTOLVL | 0x40310A58 | FULL | Port input buffer AUTOLVL configuration register |

## 16.22 PRT 21

| Register Name | Address | Permission | Description |
|---|---|---|---|
| GPIO_PRT21_OUT | 0x40310A80 | FULL | Port output data register |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| GPIO_PRT21_OUT_CLR | 0x40310A84 | FULL | Port output data clear register |
| GPIO_PRT21_OUT_SET | 0x40310A88 | FULL | Port output data set register |
| GPIO_PRT21_OUT_INV | 0x40310A8C | FULL | Port output data invert register |
| GPIO_PRT21_IN | 0x40310A90 | FULL | Port input state register |
| GPIO_PRT21_INTR | 0x40310A94 | FULL | Port interrupt status register |
| GPIO_PRT21_INTR_MASK | 0x40310A98 | FULL | Port interrupt mask register |
| GPIO_PRT21_INTR_MASKED | 0x40310A9C | FULL | Port interrupt masked status register |
| GPIO_PRT21_INTR_SET | 0x40310AA0 | FULL | Port interrupt set register |
| GPIO_PRT21_INTR_CFG | 0x40310AC0 | FULL | Port interrupt configuration register |
| GPIO_PRT21_CFG | 0x40310AC4 | FULL | Port configuration register |
| GPIO_PRT21_CFG_IN | 0x40310AC8 | FULL | Port input buffer configuration register |
| GPIO_PRT21_CFG_OUT | 0x40310ACC | FULL | Port output buffer configuration register<br>Note:SLOW0 SLOW1 SLOW2 SLOW3 SLOW4 SLOW5 SLOW6 SLOW7 are not available for this register |
| GPIO_PRT21_CFG_IN_AUTOLVL | 0x40310AD8 | FULL | Port input buffer AUTOLVL configuration register |

## 16.23 PRT 22

| Register Name | Address | Permission | Description |
|---|---|---|---|
| GPIO_PRT22_OUT | 0x40310B00 | FULL | Port output data register |
| GPIO_PRT22_OUT_CLR | 0x40310B04 | FULL | Port output data clear register |
| GPIO_PRT22_OUT_SET | 0x40310B08 | FULL | Port output data set register |
| GPIO_PRT22_OUT_INV | 0x40310B0C | FULL | Port output data invert register |
| GPIO_PRT22_IN | 0x40310B10 | FULL | Port input state register |
| GPIO_PRT22_INTR | 0x40310B14 | FULL | Port interrupt status register |
| GPIO_PRT22_INTR_MASK | 0x40310B18 | FULL | Port interrupt mask register |
| GPIO_PRT22_INTR_MASKED | 0x40310B1C | FULL | Port interrupt masked status register |
| GPIO_PRT22_INTR_SET | 0x40310B20 | FULL | Port interrupt set register |
| GPIO_PRT22_INTR_CFG | 0x40310B40 | FULL | Port interrupt configuration register |
| GPIO_PRT22_CFG | 0x40310B44 | FULL | Port configuration register |
| GPIO_PRT22_CFG_IN | 0x40310B48 | FULL | Port input buffer configuration register |
| GPIO_PRT22_CFG_OUT | 0x40310B4C | FULL | Port output buffer configuration register<br>Note:SLOW0 SLOW1 SLOW2 SLOW3 SLOW4 SLOW5 SLOW6 SLOW7 are not available for this register |
| GPIO_PRT22_CFG_IN_AUTOLVL | 0x40310B58 | FULL | Port input buffer AUTOLVL configuration register |

## 16.24 PRT 23

| Register Name | Address | Permission | Description |
|---|---|---|---|
| GPIO_PRT23_OUT | 0x40310B80 | FULL | Port output data register |
| GPIO_PRT23_OUT_CLR | 0x40310B84 | FULL | Port output data clear register |
| GPIO_PRT23_OUT_SET | 0x40310B88 | FULL | Port output data set register |
| GPIO_PRT23_OUT_INV | 0x40310B8C | FULL | Port output data invert register |
| GPIO_PRT23_IN | 0x40310B90 | FULL | Port input state register |
| GPIO_PRT23_INTR | 0x40310B94 | FULL | Port interrupt status register |
| GPIO_PRT23_INTR_MASK | 0x40310B98 | FULL | Port interrupt mask register |
| GPIO_PRT23_INTR_MASKED | 0x40310B9C | FULL | Port interrupt masked status register |
| GPIO_PRT23_INTR_SET | 0x40310BA0 | FULL | Port interrupt set register |
| GPIO_PRT23_INTR_CFG | 0x40310BC0 | FULL | Port interrupt configuration register |
| GPIO_PRT23_CFG | 0x40310BC4 | FULL | Port configuration register |
| GPIO_PRT23_CFG_IN | 0x40310BC8 | FULL | Port input buffer configuration register |
| GPIO_PRT23_CFG_OUT | 0x40310BCC | FULL | Port output buffer configuration register<br>Note:SLOW0 SLOW1 SLOW2 SLOW3 SLOW4 SLOW5 SLOW6 SLOW7 are not available for this register |
| GPIO_PRT23_CFG_IN_AUTOLVL | 0x40310BD8 | FULL | Port input buffer AUTOLVL configuration register |

## 16.25 PRT 24

| Register Name | Address | Permission | Description |
|---|---|---|---|
| GPIO_PRT24_OUT | 0x40310C00 | FULL | Port output data register<br>Note:OUT5 OUT6 OUT7 are not available for this register |
| GPIO_PRT24_OUT_CLR | 0x40310C04 | FULL | Port output data clear register |
| GPIO_PRT24_OUT_SET | 0x40310C08 | FULL | Port output data set register |
| GPIO_PRT24_OUT_INV | 0x40310C0C | FULL | Port output data invert register |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| GPIO_PRT24_IN | 0x40310C10 | FULL | Port input state register<br>Note:IN5 IN6 IN7 are not available for this register |
| GPIO_PRT24_INTR | 0x40310C14 | FULL | Port interrupt status register<br>Note:EDGE5 EDGE6 EDGE7 IN_IN5 IN_IN6 IN_IN7 are not available for this register |
| GPIO_PRT24_INTR_MASK | 0x40310C18 | FULL | Port interrupt mask register<br>Note:EDGE5 EDGE6 EDGE7 are not available for this register |
| GPIO_PRT24_INTR_MASKED | 0x40310C1C | FULL | Port interrupt masked status register<br>Note:EDGE5 EDGE6 EDGE7 are not available for this register |
| GPIO_PRT24_INTR_SET | 0x40310C20 | FULL | Port interrupt set register<br>Note:EDGE5 EDGE6 EDGE7 are not available for this register |
| GPIO_PRT24_INTR_CFG | 0x40310C40 | FULL | Port interrupt configuration register<br>Note:EDGE5_SEL EDGE6_SEL EDGE7_SEL are not available for this register |
| GPIO_PRT24_CFG | 0x40310C44 | FULL | Port configuration register<br>Note:IN_EN5 IN_EN6 IN_EN7 are not available for this register |
| GPIO_PRT24_CFG_IN | 0x40310C48 | FULL | Port input buffer configuration register<br>Note:VTRIP_SEL5_0 VTRIP_SEL6_0 VTRIP_SEL7_0 are not available for this register |
| GPIO_PRT24_CFG_OUT | 0x40310C4C | FULL | Port output buffer configuration register<br>Note:SLOW0 SLOW1 SLOW2 SLOW3 SLOW4 SLOW5 SLOW6 SLOW7 DRIVE_SEL5 DRIVE_SEL6 DRIVE_SEL7 are not available for this register |
| GPIO_PRT24_CFG_IN_AUTOLVL | 0x40310C58 | FULL | Port input buffer AUTOLVL configuration register<br>Note:VTRIP_SEL5_1 VTRIP_SEL6_1 VTRIP_SEL7_1 are not available for this register |

## 16.26 PRT 25

| Register Name | Address | Permission | Description |
|---|---|---|---|
| GPIO_PRT25_OUT | 0x40310C80 | FULL | Port output data register |
| GPIO_PRT25_OUT_CLR | 0x40310C84 | FULL | Port output data clear register |
| GPIO_PRT25_OUT_SET | 0x40310C88 | FULL | Port output data set register |
| GPIO_PRT25_OUT_INV | 0x40310C8C | FULL | Port output data invert register |
| GPIO_PRT25_IN | 0x40310C90 | FULL | Port input state register |
| GPIO_PRT25_INTR | 0x40310C94 | FULL | Port interrupt status register |
| GPIO_PRT25_INTR_MASK | 0x40310C98 | FULL | Port interrupt mask register |
| GPIO_PRT25_INTR_MASKED | 0x40310C9C | FULL | Port interrupt masked status register |
| GPIO_PRT25_INTR_SET | 0x40310CA0 | FULL | Port interrupt set register |
| GPIO_PRT25_INTR_CFG | 0x40310CC0 | FULL | Port interrupt configuration register |
| GPIO_PRT25_CFG | 0x40310CC4 | FULL | Port configuration register |
| GPIO_PRT25_CFG_IN | 0x40310CC8 | FULL | Port input buffer configuration register |
| GPIO_PRT25_CFG_OUT | 0x40310CCC | FULL | Port output buffer configuration register<br>Note:SLOW0 SLOW1 SLOW2 SLOW3 SLOW4 SLOW5 SLOW6 SLOW7 are not available for this register |
| GPIO_PRT25_CFG_IN_AUTOLVL | 0x40310CD8 | FULL | Port input buffer AUTOLVL configuration register |

## 16.27 PRT 26

| Register Name | Address | Permission | Description |
|---|---|---|---|
| GPIO_PRT26_OUT | 0x40310D00 | FULL | Port output data register |
| GPIO_PRT26_OUT_CLR | 0x40310D04 | FULL | Port output data clear register |
| GPIO_PRT26_OUT_SET | 0x40310D08 | FULL | Port output data set register |
| GPIO_PRT26_OUT_INV | 0x40310D0C | FULL | Port output data invert register |
| GPIO_PRT26_IN | 0x40310D10 | FULL | Port input state register |
| GPIO_PRT26_INTR | 0x40310D14 | FULL | Port interrupt status register |
| GPIO_PRT26_INTR_MASK | 0x40310D18 | FULL | Port interrupt mask register |
| GPIO_PRT26_INTR_MASKED | 0x40310D1C | FULL | Port interrupt masked status register |
| GPIO_PRT26_INTR_SET | 0x40310D20 | FULL | Port interrupt set register |
| GPIO_PRT26_INTR_CFG | 0x40310D40 | FULL | Port interrupt configuration register |
| GPIO_PRT26_CFG | 0x40310D44 | FULL | Port configuration register |
| GPIO_PRT26_CFG_IN | 0x40310D48 | FULL | Port input buffer configuration register |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| GPIO_PRT26_CFG_OUT | 0x40310D4C | FULL | Port output buffer configuration register<br>Note:SLOW0 SLOW1 SLOW2 SLOW3 SLOW4 SLOW5 SLOW6 SLOW7 are not available for this register |
| GPIO_PRT26_CFG_IN_AUTOLVL | 0x40310D58 | FULL | Port input buffer AUTOLVL configuration register |

## 16.28 PRT 27

| Register Name | Address | Permission | Description |
|---|---|---|---|
| GPIO_PRT27_OUT | 0x40310D80 | FULL | Port output data register |
| GPIO_PRT27_OUT_CLR | 0x40310D84 | FULL | Port output data clear register |
| GPIO_PRT27_OUT_SET | 0x40310D88 | FULL | Port output data set register |
| GPIO_PRT27_OUT_INV | 0x40310D8C | FULL | Port output data invert register |
| GPIO_PRT27_IN | 0x40310D90 | FULL | Port input state register |
| GPIO_PRT27_INTR | 0x40310D94 | FULL | Port interrupt status register |
| GPIO_PRT27_INTR_MASK | 0x40310D98 | FULL | Port interrupt mask register |
| GPIO_PRT27_INTR_MASKED | 0x40310D9C | FULL | Port interrupt masked status register |
| GPIO_PRT27_INTR_SET | 0x40310DA0 | FULL | Port interrupt set register |
| GPIO_PRT27_INTR_CFG | 0x40310DC0 | FULL | Port interrupt configuration register |
| GPIO_PRT27_CFG | 0x40310DC4 | FULL | Port configuration register |
| GPIO_PRT27_CFG_IN | 0x40310DC8 | FULL | Port input buffer configuration register |
| GPIO_PRT27_CFG_OUT | 0x40310DCC | FULL | Port output buffer configuration register<br>Note:SLOW0 SLOW1 SLOW2 SLOW3 SLOW4 SLOW5 SLOW6 SLOW7 are not available for this register |
| GPIO_PRT27_CFG_IN_AUTOLVL | 0x40310DD8 | FULL | Port input buffer AUTOLVL configuration register |

## 16.29 PRT 28

| Register Name | Address | Permission | Description |
|---|---|---|---|
| GPIO_PRT28_OUT | 0x40310E00 | FULL | Port output data register |
| GPIO_PRT28_OUT_CLR | 0x40310E04 | FULL | Port output data clear register |
| GPIO_PRT28_OUT_SET | 0x40310E08 | FULL | Port output data set register |
| GPIO_PRT28_OUT_INV | 0x40310E0C | FULL | Port output data invert register |
| GPIO_PRT28_IN | 0x40310E10 | FULL | Port input state register |
| GPIO_PRT28_INTR | 0x40310E14 | FULL | Port interrupt status register |
| GPIO_PRT28_INTR_MASK | 0x40310E18 | FULL | Port interrupt mask register |
| GPIO_PRT28_INTR_MASKED | 0x40310E1C | FULL | Port interrupt masked status register |
| GPIO_PRT28_INTR_SET | 0x40310E20 | FULL | Port interrupt set register |
| GPIO_PRT28_INTR_CFG | 0x40310E40 | FULL | Port interrupt configuration register |
| GPIO_PRT28_CFG | 0x40310E44 | FULL | Port configuration register |
| GPIO_PRT28_CFG_IN | 0x40310E48 | FULL | Port input buffer configuration register |
| GPIO_PRT28_CFG_OUT | 0x40310E4C | FULL | Port output buffer configuration register<br>Note:SLOW0 SLOW1 SLOW2 SLOW3 SLOW4 SLOW5 SLOW6 SLOW7 are not available for this register |
| GPIO_PRT28_CFG_IN_AUTOLVL | 0x40310E58 | FULL | Port input buffer AUTOLVL configuration register |

## 16.30 PRT 29

| Register Name | Address | Permission | Description |
|---|---|---|---|
| GPIO_PRT29_OUT | 0x40310E80 | FULL | Port output data register |
| GPIO_PRT29_OUT_CLR | 0x40310E84 | FULL | Port output data clear register |
| GPIO_PRT29_OUT_SET | 0x40310E88 | FULL | Port output data set register |
| GPIO_PRT29_OUT_INV | 0x40310E8C | FULL | Port output data invert register |
| GPIO_PRT29_IN | 0x40310E90 | FULL | Port input state register |
| GPIO_PRT29_INTR | 0x40310E94 | FULL | Port interrupt status register |
| GPIO_PRT29_INTR_MASK | 0x40310E98 | FULL | Port interrupt mask register |
| GPIO_PRT29_INTR_MASKED | 0x40310E9C | FULL | Port interrupt masked status register |
| GPIO_PRT29_INTR_SET | 0x40310EA0 | FULL | Port interrupt set register |
| GPIO_PRT29_INTR_CFG | 0x40310EC0 | FULL | Port interrupt configuration register |
| GPIO_PRT29_CFG | 0x40310EC4 | FULL | Port configuration register |
| GPIO_PRT29_CFG_IN | 0x40310EC8 | FULL | Port input buffer configuration register |
| GPIO_PRT29_CFG_OUT | 0x40310ECC | FULL | Port output buffer configuration register<br>Note:SLOW0 SLOW1 SLOW2 SLOW3 SLOW4 SLOW5 SLOW6 SLOW7 are not available for this register |
| GPIO_PRT29_CFG_IN_AUTOLVL | 0x40310ED8 | FULL | Port input buffer AUTOLVL configuration register |

## 16.31 PRT 30

| Register Name | Address | Permission | Description |
|---|---|---|---|
| GPIO_PRT30_OUT | 0x40310F00 | FULL | Port output data register<br>Note:OUT4 OUT5 OUT6 OUT7 are not available for this register |
| GPIO_PRT30_OUT_CLR | 0x40310F04 | FULL | Port output data clear register |
| GPIO_PRT30_OUT_SET | 0x40310F08 | FULL | Port output data set register |
| GPIO_PRT30_OUT_INV | 0x40310F0C | FULL | Port output data invert register |
| GPIO_PRT30_IN | 0x40310F10 | FULL | Port input state register<br>Note:IN4 IN5 IN6 IN7 are not available for this register |
| GPIO_PRT30_INTR | 0x40310F14 | FULL | Port interrupt status register<br>Note:EDGE4 EDGE5 EDGE6 EDGE7 IN_IN4 IN_IN5 IN_IN6 IN_IN7 are not available for this register |
| GPIO_PRT30_INTR_MASK | 0x40310F18 | FULL | Port interrupt mask register<br>Note:EDGE4 EDGE5 EDGE6 EDGE7 are not available for this register |
| GPIO_PRT30_INTR_MASKED | 0x40310F1C | FULL | Port interrupt masked status register<br>Note:EDGE4 EDGE5 EDGE6 EDGE7 are not available for this register |
| GPIO_PRT30_INTR_SET | 0x40310F20 | FULL | Port interrupt set register<br>Note:EDGE4 EDGE5 EDGE6 EDGE7 are not available for this register |
| GPIO_PRT30_INTR_CFG | 0x40310F40 | FULL | Port interrupt configuration register<br>Note:EDGE4_SEL EDGE5_SEL EDGE6_SEL EDGE7_SEL are not available for this register |
| GPIO_PRT30_CFG | 0x40310F44 | FULL | Port configuration register<br>Note:IN_EN4 IN_EN5 IN_EN6 IN_EN7 are not available for this register |
| GPIO_PRT30_CFG_IN | 0x40310F48 | FULL | Port input buffer configuration register<br>Note:VTRIP_SEL4_0 VTRIP_SEL5_0 VTRIP_SEL6_0 VTRIP_SEL7_0 are not available for this register |
| GPIO_PRT30_CFG_OUT | 0x40310F4C | FULL | Port output buffer configuration register<br>Note:SLOW0 SLOW1 SLOW2 SLOW3 SLOW4 SLOW5 SLOW6 SLOW7 DRIVE_SEL4 DRIVE_SEL5 DRIVE_SEL6 DRIVE_SEL7 are not available for this register |
| GPIO_PRT30_CFG_IN_AUTOLVL | 0x40310F58 | FULL | Port input buffer AUTOLVL configuration register<br>Note:VTRIP_SEL4_1 VTRIP_SEL5_1 VTRIP_SEL6_1 VTRIP_SEL7_1 are not available for this register |

## 16.32 PRT 31

| Register Name | Address | Permission | Description |
|---|---|---|---|
| GPIO_PRT31_OUT | 0x40310F80 | FULL | Port output data register<br>Note:OUT3 OUT4 OUT5 OUT6 OUT7 are not available for this register |
| GPIO_PRT31_OUT_CLR | 0x40310F84 | FULL | Port output data clear register |
| GPIO_PRT31_OUT_SET | 0x40310F88 | FULL | Port output data set register |
| GPIO_PRT31_OUT_INV | 0x40310F8C | FULL | Port output data invert register |
| GPIO_PRT31_IN | 0x40310F90 | FULL | Port input state register<br>Note:IN3 IN4 IN5 IN6 IN7 are not available for this register |
| GPIO_PRT31_INTR | 0x40310F94 | FULL | Port interrupt status register<br>Note:EDGE3 EDGE4 EDGE5 EDGE6 EDGE7 IN_IN3 IN_IN4 IN_IN5 IN_IN6 IN_IN7 are not available for this register |
| GPIO_PRT31_INTR_MASK | 0x40310F98 | FULL | Port interrupt mask register<br>Note:EDGE3 EDGE4 EDGE5 EDGE6 EDGE7 are not available for this register |
| GPIO_PRT31_INTR_MASKED | 0x40310F9C | FULL | Port interrupt masked status register<br>Note:EDGE3 EDGE4 EDGE5 EDGE6 EDGE7 are not available for this register |
| GPIO_PRT31_INTR_SET | 0x40310FA0 | FULL | Port interrupt set register<br>Note:EDGE3 EDGE4 EDGE5 EDGE6 EDGE7 are not available for this register |
| GPIO_PRT31_INTR_CFG | 0x40310FC0 | FULL | Port interrupt configuration register<br>Note:EDGE3_SEL EDGE4_SEL EDGE5_SEL EDGE6_SEL EDGE7_SEL are not available for this register |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| GPIO_PRT31_CFG | 0x40310FC4 | FULL | Port configuration register<br>Note:IN_EN3 IN_EN4 IN_EN5 IN_EN6 IN_EN7 are not available for this register |
| GPIO_PRT31_CFG_IN | 0x40310FC8 | FULL | Port input buffer configuration register<br>Note:VTRIP_SEL3_0 VTRIP_SEL4_0 VTRIP_SEL5_0 VTRIP_SEL6_0 VTRIP_SEL7_0 are not available for this register |
| GPIO_PRT31_CFG_OUT | 0x40310FCC | FULL | Port output buffer configuration register<br>Note:SLOW0 SLOW1 SLOW2 SLOW3 SLOW4 SLOW5 SLOW6 SLOW7 DRIVE_SEL3 DRIVE_SEL4 DRIVE_SEL5 DRIVE_SEL6 DRIVE_SEL7 are not available for this register |
| GPIO_PRT31_CFG_IN_AUTOLVL | 0x40310FD8 | FULL | Port input buffer AUTOLVL configuration register<br>Note:VTRIP_SEL3_1 VTRIP_SEL4_1 VTRIP_SEL5_1 VTRIP_SEL6_1 VTRIP_SEL7_1 are not available for this register |

## 16.33 PRT 32

| Register Name | Address | Permission | Description |
|---|---|---|---|
| GPIO_PRT32_OUT | 0x40311000 | FULL | Port output data register |
| GPIO_PRT32_OUT_CLR | 0x40311004 | FULL | Port output data clear register |
| GPIO_PRT32_OUT_SET | 0x40311008 | FULL | Port output data set register |
| GPIO_PRT32_OUT_INV | 0x4031100C | FULL | Port output data invert register |
| GPIO_PRT32_IN | 0x40311010 | FULL | Port input state register |
| GPIO_PRT32_INTR | 0x40311014 | FULL | Port interrupt status register |
| GPIO_PRT32_INTR_MASK | 0x40311018 | FULL | Port interrupt mask register |
| GPIO_PRT32_INTR_MASKED | 0x4031101C | FULL | Port interrupt masked status register |
| GPIO_PRT32_INTR_SET | 0x40311020 | FULL | Port interrupt set register |
| GPIO_PRT32_INTR_CFG | 0x40311040 | FULL | Port interrupt configuration register |
| GPIO_PRT32_CFG | 0x40311044 | FULL | Port configuration register |
| GPIO_PRT32_CFG_IN | 0x40311048 | FULL | Port input buffer configuration register |
| GPIO_PRT32_CFG_OUT | 0x4031104C | FULL | Port output buffer configuration register<br>Note:SLOW0 SLOW1 SLOW2 SLOW3 SLOW4 SLOW5 SLOW6 SLOW7 are not available for this register |
| GPIO_PRT32_CFG_IN_AUTOLVL | 0x40311058 | FULL | Port input buffer AUTOLVL configuration register |

## 16.34 PRT 33

| Register Name | Address | Permission | Description |
|---|---|---|---|
| GPIO_PRT33_OUT | 0x40311080 | FULL | Port output data register |
| GPIO_PRT33_OUT_CLR | 0x40311084 | FULL | Port output data clear register |
| GPIO_PRT33_OUT_SET | 0x40311088 | FULL | Port output data set register |
| GPIO_PRT33_OUT_INV | 0x4031108C | FULL | Port output data invert register |
| GPIO_PRT33_IN | 0x40311090 | FULL | Port input state register |
| GPIO_PRT33_INTR | 0x40311094 | FULL | Port interrupt status register |
| GPIO_PRT33_INTR_MASK | 0x40311098 | FULL | Port interrupt mask register |
| GPIO_PRT33_INTR_MASKED | 0x4031109C | FULL | Port interrupt masked status register |
| GPIO_PRT33_INTR_SET | 0x403110A0 | FULL | Port interrupt set register |
| GPIO_PRT33_INTR_CFG | 0x403110C0 | FULL | Port interrupt configuration register |
| GPIO_PRT33_CFG | 0x403110C4 | FULL | Port configuration register |
| GPIO_PRT33_CFG_IN | 0x403110C8 | FULL | Port input buffer configuration register |
| GPIO_PRT33_CFG_OUT | 0x403110CC | FULL | Port output buffer configuration register<br>Note:SLOW0 SLOW1 SLOW2 SLOW3 SLOW4 SLOW5 SLOW6 SLOW7 are not available for this register |
| GPIO_PRT33_CFG_IN_AUTOLVL | 0x403110D8 | FULL | Port input buffer AUTOLVL configuration register |

## 16.35 PRT 34

| Register Name | Address | Permission | Description |
|---|---|---|---|
| GPIO_PRT34_OUT | 0x40311100 | FULL | Port output data register |
| GPIO_PRT34_OUT_CLR | 0x40311104 | FULL | Port output data clear register |
| GPIO_PRT34_OUT_SET | 0x40311108 | FULL | Port output data set register |
| GPIO_PRT34_OUT_INV | 0x4031110C | FULL | Port output data invert register |
| GPIO_PRT34_IN | 0x40311110 | FULL | Port input state register |
| GPIO_PRT34_INTR | 0x40311114 | FULL | Port interrupt status register |
| GPIO_PRT34_INTR_MASK | 0x40311118 | FULL | Port interrupt mask register |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| GPIO_PRT34_INTR_MASKED | 0x4031111C | FULL | Port interrupt masked status register |
| GPIO_PRT34_INTR_SET | 0x40311120 | FULL | Port interrupt set register |
| GPIO_PRT34_INTR_CFG | 0x40311140 | FULL | Port interrupt configuration register |
| GPIO_PRT34_CFG | 0x40311144 | FULL | Port configuration register |
| GPIO_PRT34_CFG_IN | 0x40311148 | FULL | Port input buffer configuration register |
| GPIO_PRT34_CFG_OUT | 0x4031114C | FULL | Port output buffer configuration register<br>Note:SLOW0 SLOW1 SLOW2 SLOW3 SLOW4 SLOW5 SLOW6 SLOW7 are not available for this register |
| GPIO_PRT34_CFG_IN_AUTOLVL | 0x40311158 | FULL | Port input buffer AUTOLVL configuration register |

## 16.36 Register Details

### 16.36.1 GPIO_INTR_CAUSE0

**Description:** Interrupt port cause register 0
**Address:** 0x40314000
**Offset:** 0x4000
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register provides interrupt status corresponding to ports 0 to 31
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | PORT_INT [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | PORT_INT [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | PORT_INT [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | PORT_INT [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | PORT_INT | R | W | 0 | Each IO port has an associated bit field in this register. The bit field reflects the IO port's interrupt line (bit field i reflects 'gpio_interrupts[i]' for IO port i). The register is used when the system uses a combined interrupt line 'gpio_interrupt'. The software ISR reads the register to determine which IO port(s) is responsible for the combined interrupt line. Once, the IO port(s) is determined, the IO port's GPIO_PRT_INTR register is read to determine the IO pin(s) in the IO port that caused the interrupt.<br>'0': Port has no pending interrupt<br>'1': Port has pending interrupt |

### 16.36.2 GPIO_INTR_CAUSE1

**Description:** Interrupt port cause register 1
**Address:** 0x40314004
**Offset:** 0x4004
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register provides interrupt status corresponding to ports 32 to 63
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:3] | | | | | PORT_INT [2:0] | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:2 | PORT_INT | R | W | 0 | Each IO port has an associated bit field in this register. The bit field reflects the IO port's interrupt line (bit field i reflects 'gpio_interrupts[i]' for IO port i). The register is used when the system uses a combined interrupt line 'gpio_interrupt'. The software ISR reads the register to determine which IO port(s) is responsible for the combined interrupt line. Once, the IO port(s) is determined, the IO port's GPIO_PORT_INTR register is read to determine the IO pin(s) in the IO port that caused the interrupt.<br>'0': Port has no pending interrupt<br>'1': Port has pending interrupt |

### 16.36.3 GPIO_VDD_ACTIVE

**Description:** Extern power supply detection register
**Address:** 0x40314010
**Offset:** 0x4010
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register provides external power supply status
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:4] | | | | VDDIO_ACTIVE [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VDDD _ACTIVE [31:31] | VDDA _ACTIVE [30:30] | None [29:24] | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | VDDIO_ACTIVE | R | W | 0 | Indicates presence or absence of VDDIO supplies (i.e. other than VDDD, VDDA) on the device (supplies are numbered 0..n-1). Note that VDDIO supplies have basic (crude) supply detectors only. If separate, robust, brown-out detection is desired on IO supplies, on-chip or off-chip analog resources need to provide it. For these bits to work reliable, the supply must be within valid spec range (per datasheet) or held at ground. Any in-between voltage has an undefined result.<br>'0': Supply is not present<br>'1': Supply is present<br><br>When multiple VDDIO supplies are present, they will be assigned in alphanumeric ascending order to these bits during implementation.<br>For example 'vddusb, vddio_0, vddio_a, vbackup, vddio_r, vddio_1' are present then they will be assigned to these bits as below:<br>0: vbackup,<br>1: vddio_0,<br>2: vddio_1,<br>3: vddio_a,<br>4: vddio_r,<br>5: vddusb' |
| 30 | VDDA_ACTIVE | R | W | 0 | Same as VDDIO_ACTIVE for the analog supply VDDA. |
| 31 | VDDD_ACTIVE | R | W | 0 | This bit indicates presence of the VDDD supply. This bit will always read-back 1. The VDDD supply has robust brown-out protection monitoring and it is not possible to read back this register without a valid supply. (This bit is used in certain test-modes to observe the brown-out detector status.) |

### 16.36.4 GPIO_VDD_INTR

**Description:** Supply detection interrupt register
**Address:** 0x40314014
**Offset:** 0x4014
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** An interrupt cause is cleared (set to '0') by writing a '1' to the corresponding bit field. It is not recommended to write 0xFF to clear all interrupt causes, as a new interrupt cause may have occurred between reading the register and clearing. Note that the interrupt cause fields and the associated interrupt provide DeepSleep functionality (interrupt causes can be set to '1' and cause the system to wake up from DeepSleep power mode). This register is set whenever a supply ramp up or ramp down is detected. Some bits may be set after system power-up, depending on power supply sequencing.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:4] | | | | VDDIO_ACTIVE [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VDDD_ACTIVE [31:31] | VDDA_ACTIVE [30:30] | None [29:24] | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | VDDIO_ACTIVE | RW1C | A | 0 | Supply state change detected.<br>'0': No change to supply detected<br>'1': Change to supply detected |
| 30 | VDDA_ACTIVE | RW1C | A | 0 | Same as VDDIO_ACTIVE for the analog supply VDDA. |
| 31 | VDDD_ACTIVE | RW1C | A | 0 | The VDDD supply is always present during operation so a supply transition can not occur. This bit will always read back '1'. |

### 16.36.5 GPIO_VDD_INTR_MASK

**Description:** Supply detection interrupt mask register
**Address:** 0x40314018
**Offset:** 0x4018
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register configures the supply detection interrupts for all supplies. This register only masks the forwarding of interrupts to the CPU(s), it does not enable/disable the logging of interrupts into the VDD_INTR register.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:4] | | | | VDDIO_ACTIVE [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VDDD _ACTIVE [31:31] | VDDA _ACTIVE [30:30] | None [29:24] | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | VDDIO_ACTIVE | RW | R | 0 | Masks supply interrupt on VDDIO.<br>'0': VDDIO interrupt forwarding disabled<br>'1': VDDIO interrupt forwarding enabled |
| 30 | VDDA_ACTIVE | RW | R | 0 | Same as VDDIO_ACTIVE for the analog supply VDDA. |
| 31 | VDDD_ACTIVE | RW | R | 0 | Same as VDDIO_ACTIVE for the digital supply VDDD. |

### 16.36.6 GPIO_VDD_INTR_MASKED

**Description:** Supply detection interrupt masked register
**Address:** 0x4031401C
**Offset:** 0x401C
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register contains the AND-ed values of VDD_INTR and VDD_INTR_MASK registers
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:4] | | | | VDDIO_ACTIVE [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VDDD_ACTIVE [31:31] | VDDA_ACTIVE [30:30] | None [29:24] | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | VDDIO_ACTIVE | R | W | 0 | Supply transition detected AND masked<br>'0': Interrupt was not forwarded to CPU<br>'1': Interrupt occurred and was forwarded to CPU |
| 30 | VDDA_ACTIVE | R | W | 0 | Same as VDDIO_ACTIVE for the analog supply VDDA. |
| 31 | VDDD_ACTIVE | R | W | 0 | Same as VDDIO_ACTIVE for the digital supply VDDD. |

### 16.36.7 GPIO_VDD_INTR_SET

**Description:** Supply detection interrupt set register
**Address:** 0x40314020
**Offset:** 0x4020
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Allows firmware or debugger to set interrupt bits in the VDD_INTR register by writing a '1' to the corresponding bit field. When read, returns the same value as the VDD_INTR register.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:4] | | | | VDDIO_ACTIVE [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VDDD _ACTIVE [31:31] | VDDA _ACTIVE [30:30] | None [29:24] | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | VDDIO_ACTIVE | RW1S | A | 0 | Sets supply interrupt.<br>'0': Interrupt state not affected<br>'1': Interrupt set |
| 30 | VDDA_ACTIVE | RW1S | A | 0 | Same as VDDIO_ACTIVE for the analog supply VDDA. |
| 31 | VDDD_ACTIVE | RW1S | A | 0 | Same as VDDIO_ACTIVE for the digital supply VDDD. |

## 16.36.8 PRT

### 16.36.8.1 GPIO_PRT_OUT

**Description:** Port output data register
**Address:** 0x40310000
**Offset:** 0x0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Used to read and write the output data for the IO pins in the port. A register write changes the output data to the written value. A register read reflects the output data (and not the current state of the input data for the IO pins). Using this register, Read-Modify-Write sequences are safely performed on a port with some IO pins configured as inputs.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | OUT7 [7:7] | OUT6 [6:6] | OUT5 [5:5] | OUT4 [4:4] | OUT3 [3:3] | OUT2 [2:2] | OUT1 [1:1] | OUT0 [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | OUT0 | RW | RW | 0 | IO output data for pin 0<br>'0': Output state set to '0'<br>'1': Output state set to '1' |
| 1 | OUT1 | RW | RW | 0 | IO output data for pin 1 |
| 2 | OUT2 | RW | RW | 0 | IO output data for pin 2 |
| 3 | OUT3 | RW | RW | 0 | IO output data for pin 3 |
| 4 | OUT4 | RW | RW | 0 | IO output data for pin 4 |
| 5 | OUT5 | RW | RW | 0 | IO output data for pin 5 |
| 6 | OUT6 | RW | RW | 0 | IO output data for pin 6 |
| 7 | OUT7 | RW | RW | 0 | IO output data for pin 7 |

### 16.36.8.2 GPIO_PRT_OUT_CLR

**Description:** Port output data clear register
**Address:** 0x40310004
**Offset:** 0x4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Used to clear output data of specific IO pins in the corresponding port to '0', without affecting the output data of the other IO pads in the port. A register read returns the same value as an OUT register read.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | OUT7 [7:7] | OUT6 [6:6] | OUT5 [5:5] | OUT4 [4:4] | OUT3 [3:3] | OUT2 [2:2] | OUT1 [1:1] | OUT0 [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | OUT0 | RW | A | 0 | IO clear output for pin 0:<br>'0': Output state not affected.<br>'1': Output state set to '0'. |
| 1 | OUT1 | RW | A | 0 | IO clear output for pin 1 |
| 2 | OUT2 | RW | A | 0 | IO clear output for pin 2 |
| 3 | OUT3 | RW | A | 0 | IO clear output for pin 3 |
| 4 | OUT4 | RW | A | 0 | IO clear output for pin 4 |
| 5 | OUT5 | RW | A | 0 | IO clear output for pin 5 |
| 6 | OUT6 | RW | A | 0 | IO clear output for pin 6 |
| 7 | OUT7 | RW | A | 0 | IO clear output for pin 7 |

### 16.36.8.3 GPIO_PRT_OUT_SET

**Description:** Port output data set register
**Address:** 0x40310008
**Offset:** 0x8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Used to set output data of specific IO pins in the corresponding port to '1', without affecting the output data of the other IO pads in the port. A register read returns the same value as an OUT register read.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | OUT7 [7:7] | OUT6 [6:6] | OUT5 [5:5] | OUT4 [4:4] | OUT3 [3:3] | OUT2 [2:2] | OUT1 [1:1] | OUT0 [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | OUT0 | RW | A | 0 | IO set output for pin 0:<br>'0': Output state not affected.<br>'1': Output state set to '1'. |
| 1 | OUT1 | RW | A | 0 | IO set output for pin 1 |
| 2 | OUT2 | RW | A | 0 | IO set output for pin 2 |
| 3 | OUT3 | RW | A | 0 | IO set output for pin 3 |
| 4 | OUT4 | RW | A | 0 | IO set output for pin 4 |
| 5 | OUT5 | RW | A | 0 | IO set output for pin 5 |
| 6 | OUT6 | RW | A | 0 | IO set output for pin 6 |
| 7 | OUT7 | RW | A | 0 | IO set output for pin 7 |

### 16.36.8.4 GPIO_PRT_OUT_INV

**Description:** Port output data invert register
**Address:** 0x4031000C
**Offset:** 0xC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Used to invert output data of specific IO pins in the corresponding port, without affecting the output data of the other IO pads in the port. A register read returns the same value as an OUT register read.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | OUT7 [7:7] | OUT6 [6:6] | OUT5 [5:5] | OUT4 [4:4] | OUT3 [3:3] | OUT2 [2:2] | OUT1 [1:1] | OUT0 [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | OUT0 | RW | A | 0 | IO invert output for pin 0:<br>'0': Output state not affected.<br>'1': Output state inverted ('0' => '1', '1' => '0'). |
| 1 | OUT1 | RW | A | 0 | IO invert output for pin 1 |
| 2 | OUT2 | RW | A | 0 | IO invert output for pin 2 |
| 3 | OUT3 | RW | A | 0 | IO invert output for pin 3 |
| 4 | OUT4 | RW | A | 0 | IO invert output for pin 4 |
| 5 | OUT5 | RW | A | 0 | IO invert output for pin 5 |
| 6 | OUT6 | RW | A | 0 | IO invert output for pin 6 |
| 7 | OUT7 | RW | A | 0 | IO invert output for pin 7 |

### 16.36.8.5 GPIO_PRT_IN

**Description:** Port input state register
**Address:** 0x40310010
**Offset:** 0x10
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** Used to read current pin status for IO pins that have their input buffer enabled (see CFG_IN).
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | IN7 [7:7] | IN6 [6:6] | IN5 [5:5] | IN4 [4:4] | IN3 [3:3] | IN2 [2:2] | IN1 [1:1] | IN0 [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:9] | | | | | | | FLT_IN [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | IN0 | R | W | 0 | IO pin state for pin 0<br>'0': Low logic level present on pin.<br>'1': High logic level present on pin.<br>On reset assertion , IN register will get reset. The Pad value takes 2 clock cycles to be reflected into IN Register. It's value then depends on the external pin value. |
| 1 | IN1 | R | W | 0 | IO pin state for pin 1 |
| 2 | IN2 | R | W | 0 | IO pin state for pin 2 |
| 3 | IN3 | R | W | 0 | IO pin state for pin 3 |
| 4 | IN4 | R | W | 0 | IO pin state for pin 4 |
| 5 | IN5 | R | W | 0 | IO pin state for pin 5 |
| 6 | IN6 | R | W | 0 | IO pin state for pin 6 |
| 7 | IN7 | R | W | 0 | IO pin state for pin 7 |
| 8 | FLT_IN | R | W | 0 | Reads of this register return the logical state of the filtered pin as selected in the INTR_CFG.FLT_SEL register. |

### 16.36.8.6 GPIO_PRT_INTR

**Description:** Port interrupt status register
**Address:** 0x40310014
**Offset:** 0x14
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** An interrupt cause is cleared (set to '0') by writing a '1' to the corresponding bit field. It is not recommended to write 0xFF to clear all interrupt causes, as a new interrupt cause may have occurred between reading the register and clearing. Note that the pin interrupt provide DeepSleep functionality (interrupt causes can be set to '1' and cause the system to wake up from DeepSleep power mode). The IN.IN fields reflect the logical IO pin states at the time of reading this register (same as the IN register).
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | EDGE7 [7:7] | EDGE6 [6:6] | EDGE5 [5:5] | EDGE4 [4:4] | EDGE3 [3:3] | EDGE2 [2:2] | EDGE1 [1:1] | EDGE0 [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:9] | | | | | | | FLT_EDGE [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | IN_IN7 [23:23] | IN_IN6 [22:22] | IN_IN5 [21:21] | IN_IN4 [20:20] | IN_IN3 [19:19] | IN_IN2 [18:18] | IN_IN1 [17:17] | IN_IN0 [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:25] | | | | | | | FLT_IN_IN [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | EDGE0 | RW1C | A | 0 | Edge detect for IO pin 0<br>'0': No edge was detected on pin.<br>'1': An edge was detected on pin. |
| 1 | EDGE1 | RW1C | A | 0 | Edge detect for IO pin 1 |
| 2 | EDGE2 | RW1C | A | 0 | Edge detect for IO pin 2 |
| 3 | EDGE3 | RW1C | A | 0 | Edge detect for IO pin 3 |
| 4 | EDGE4 | RW1C | A | 0 | Edge detect for IO pin 4 |
| 5 | EDGE5 | RW1C | A | 0 | Edge detect for IO pin 5 |
| 6 | EDGE6 | RW1C | A | 0 | Edge detect for IO pin 6 |
| 7 | EDGE7 | RW1C | A | 0 | Edge detect for IO pin 7 |
| 8 | FLT_EDGE | RW1C | A | 0 | Edge detected on filtered pin selected by INTR_CFG.FLT_SEL |
| 16 | IN_IN0 | R | W | 0 | IO pin state for pin 0 |
| 17 | IN_IN1 | R | W | 0 | IO pin state for pin 1 |
| 18 | IN_IN2 | R | W | 0 | IO pin state for pin 2 |
| 19 | IN_IN3 | R | W | 0 | IO pin state for pin 3 |
| 20 | IN_IN4 | R | W | 0 | IO pin state for pin 4 |
| 21 | IN_IN5 | R | W | 0 | IO pin state for pin 5 |
| 22 | IN_IN6 | R | W | 0 | IO pin state for pin 6 |
| 23 | IN_IN7 | R | W | 0 | IO pin state for pin 7 |
| 24 | FLT_IN_IN | R | W | 0 | Filtered pin state for pin selected by INTR_CFG.FLT_SEL |

### 16.36.8.7 GPIO_PRT_INTR_MASK

**Description:** Port interrupt mask register
**Address:** 0x40310018
**Offset:** 0x18
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register configures the edge detection interrupts for all pins in a port. This register only masks the forwarding of interrupts to the CPU(s) interrupt controller, it does not enable/disable the logging of interrupts into the INTR register.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | EDGE7 [7:7] | EDGE6 [6:6] | EDGE5 [5:5] | EDGE4 [4:4] | EDGE3 [3:3] | EDGE2 [2:2] | EDGE1 [1:1] | EDGE0 [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:9] | | | | | | | FLT_EDGE [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | EDGE0 | RW | R | 0 | Masks edge interrupt on IO pin 0<br>'0': Pin interrupt forwarding disabled<br>'1': Pin interrupt forwarding enabled |
| 1 | EDGE1 | RW | R | 0 | Masks edge interrupt on IO pin 1 |
| 2 | EDGE2 | RW | R | 0 | Masks edge interrupt on IO pin 2 |
| 3 | EDGE3 | RW | R | 0 | Masks edge interrupt on IO pin 3 |
| 4 | EDGE4 | RW | R | 0 | Masks edge interrupt on IO pin 4 |
| 5 | EDGE5 | RW | R | 0 | Masks edge interrupt on IO pin 5 |
| 6 | EDGE6 | RW | R | 0 | Masks edge interrupt on IO pin 6 |
| 7 | EDGE7 | RW | R | 0 | Masks edge interrupt on IO pin 7 |
| 8 | FLT_EDGE | RW | R | 0 | Masks edge interrupt on filtered pin selected by INTR_CFG.FLT_SEL |

### 16.36.8.8 GPIO_PRT_INTR_MASKED

**Description:** Port interrupt masked status register
**Address:** 0x4031001C
**Offset:** 0x1C
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register contains the AND-ed values of INTR and INTR_MASK registers forwarded to the CPU interrupt controller.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | EDGE7 [7:7] | EDGE6 [6:6] | EDGE5 [5:5] | EDGE4 [4:4] | EDGE3 [3:3] | EDGE2 [2:2] | EDGE1 [1:1] | EDGE0 [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:9] | | | | | | | FLT_EDGE [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | EDGE0 | R | W | 0 | Edge detected AND masked on IO pin 0<br>'0': Interrupt was not forwarded to CPU<br>'1': Interrupt occurred and was forwarded to CPU |
| 1 | EDGE1 | R | W | 0 | Edge detected and masked on IO pin 1 |
| 2 | EDGE2 | R | W | 0 | Edge detected and masked on IO pin 2 |
| 3 | EDGE3 | R | W | 0 | Edge detected and masked on IO pin 3 |
| 4 | EDGE4 | R | W | 0 | Edge detected and masked on IO pin 4 |
| 5 | EDGE5 | R | W | 0 | Edge detected and masked on IO pin 5 |
| 6 | EDGE6 | R | W | 0 | Edge detected and masked on IO pin 6 |
| 7 | EDGE7 | R | W | 0 | Edge detected and masked on IO pin 7 |
| 8 | FLT_EDGE | R | W | 0 | Edge detected and masked on filtered pin selected by INTR_CFG.FLT_SEL |

### 16.36.8.9 GPIO_PRT_INTR_SET

**Description:** Port interrupt set register
**Address:** 0x40310020
**Offset:** 0x20
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Allows firmware or debugger to set interrupt bits in the INTR register by writing a '1' to the corresponding bit field. When read, returns the same value as the INTR register.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | EDGE7 [7:7] | EDGE6 [6:6] | EDGE5 [5:5] | EDGE4 [4:4] | EDGE3 [3:3] | EDGE2 [2:2] | EDGE1 [1:1] | EDGE0 [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:9] | | | | | | | FLT_EDGE [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | EDGE0 | RW1S | A | 0 | Sets edge detect interrupt for IO pin 0<br>'0': Interrupt state not affected<br>'1': Interrupt set |
| 1 | EDGE1 | RW1S | A | 0 | Sets edge detect interrupt for IO pin 1 |
| 2 | EDGE2 | RW1S | A | 0 | Sets edge detect interrupt for IO pin 2 |
| 3 | EDGE3 | RW1S | A | 0 | Sets edge detect interrupt for IO pin 3 |
| 4 | EDGE4 | RW1S | A | 0 | Sets edge detect interrupt for IO pin 4 |
| 5 | EDGE5 | RW1S | A | 0 | Sets edge detect interrupt for IO pin 5 |
| 6 | EDGE6 | RW1S | A | 0 | Sets edge detect interrupt for IO pin 6 |
| 7 | EDGE7 | RW1S | A | 0 | Sets edge detect interrupt for IO pin 7 |
| 8 | FLT_EDGE | RW1S | A | 0 | Sets edge detect interrupt for filtered pin selected by INTR_CFG.FLT_SEL |

### 16.36.8.10 GPIO_PRT_INTR_CFG

**Description:** Port interrupt configuration register
**Address:** 0x40310040
**Offset:** 0x40
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register selects the edge detection type for each pin interrupt.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | EDGE3_SEL [7:6] | | EDGE2_SEL [5:4] | | EDGE1_SEL [3:2] | | EDGE0_SEL [1:0] | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | EDGE7_SEL [15:14] | | EDGE6_SEL [13:12] | | EDGE5_SEL [11:10] | | EDGE4_SEL [9:8] | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:21] | | | FLT_SEL [20:18] | | | FLT_EDGE_SEL [17:16] | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:1 | EDGE0_SEL | RW | R | 0 | Sets which edge will trigger an IRQ for IO pin 0 |
| | DISABLE | | | 0 | Disabled |
| | RISING | | | 1 | Rising edge |
| | FALLING | | | 2 | Falling edge |
| | BOTH | | | 3 | Both rising and falling edges |
| 2:3 | EDGE1_SEL | RW | R | 0 | Sets which edge will trigger an IRQ for IO pin 1 |
| 4:5 | EDGE2_SEL | RW | R | 0 | Sets which edge will trigger an IRQ for IO pin 2 |
| 6:7 | EDGE3_SEL | RW | R | 0 | Sets which edge will trigger an IRQ for IO pin 3 |
| 8:9 | EDGE4_SEL | RW | R | 0 | Sets which edge will trigger an IRQ for IO pin 4 |
| 10:11 | EDGE5_SEL | RW | R | 0 | Sets which edge will trigger an IRQ for IO pin 5 |
| 12:13 | EDGE6_SEL | RW | R | 0 | Sets which edge will trigger an IRQ for IO pin 6 |
| 14:15 | EDGE7_SEL | RW | R | 0 | Sets which edge will trigger an IRQ for IO pin 7 |
| 16:17 | FLT_EDGE_SEL | RW | R | 0 | Sets which edge will trigger an IRQ for the glitch filtered pin (selected by INTR_CFG.FLT_SEL |
| | DISABLE | | | 0 | Disabled |
| | RISING | | | 1 | Rising edge |
| | FALLING | | | 2 | Falling edge |
| | BOTH | | | 3 | Both rising and falling edges |
| 18:20 | FLT_SEL | RW | R | 0 | Selects which pin is routed through the 50ns glitch filter to provide a glitch-safe interrupt. |

### 16.36.8.11 GPIO_PRT_CFG

**Description:** Port configuration register
**Address:** 0x40310044
**Offset:** 0x44
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Configuration of drive mode and input buffer enable for each pin.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | IN_EN1 [7:7] | DRIVE_MODE1 [6:4] | | | IN_EN0 [3:3] | DRIVE_MODE0 [2:0] | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | IN_EN3 [15:15] | DRIVE_MODE3 [14:12] | | | IN_EN2 [11:11] | DRIVE_MODE2 [10:8] | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | IN_EN5 [23:23] | DRIVE_MODE5 [22:20] | | | IN_EN4 [19:19] | DRIVE_MODE4 [18:16] | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | IN_EN7 [31:31] | DRIVE_MODE7 [30:28] | | | IN_EN6 [27:27] | DRIVE_MODE6 [26:24] | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:2 | DRIVE_MODE0 | RW | R | 0 | The GPIO drive mode for IO pin 0. Resistive pull-up and pull-down is selected in the drive mode.<br>Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the peripheral and HSIOM (HSIOM_PRT_SELx) is properly configured before turning the IO on here to avoid producing glitches on the bus.<br>Note: that peripherals other than GPIO & UDB/DSI directly control both the output and output-enable of the output buffer (peripherals can drive strong 0 or strong 1 in any mode except OFF='0').<br>Note: D_OUT, D_OUT_EN are pins of GPIO cell. |
| | HIGHZ | | | 0 | Output buffer is off creating a high impedance input<br>D_OUT = '0': High Impedance<br>D_OUT = '1': High Impedance |
| | RESERVED | | | 1 | N/A |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| | PULLUP | | | 2 | Resistive pull up<br><br>For GPIO & UDB/DSI peripherals:<br>When D_OUT_EN = 1:<br>D_OUT = '0': Strong pull down<br>D_OUT = '1': Weak/resistive pull up<br>When D_OUT_EN = 0:<br>D_OUT = '0': High impedance<br>D_OUT = '1': High impedance<br><br>For peripherals other than GPIO & UDB/DSI:<br>When D_OUT_EN = 1:<br>D_OUT = '0': Strong pull down<br>D_OUT = '1': Strong pull up<br>When D_OUT_EN = 0:<br>D_OUT = '0': Weak/resistive pull up<br>D_OUT = '1': Weak/resistive pull up |
| | PULLDOWN | | | 3 | Resistive pull down<br><br>For GPIO & UDB/DSI peripherals:<br>When D_OUT_EN = 1:<br>D_OUT = '0': Weak/resistive pull down<br>D_OUT = '1': Strong pull up<br>When D_OUT_EN = 0:<br>D_OUT = '0': High impedance<br>D_OUT = '1': High impedance<br><br>For peripherals other than GPIO & UDB/DSI:<br>When D_OUT_EN = 1:<br>D_OUT = '0': Strong pull down<br>D_OUT = '1': Strong pull up<br>When D_OUT_EN = 0:<br>D_OUT = '0': Weak/resistive pull down<br>D_OUT = '1': Weak/resistive pull down |
| | OD_DRIVESLOW | | | 4 | Open drain, drives low<br><br>For GPIO & UDB/DSI peripherals:<br>When D_OUT_EN = 1:<br>D_OUT = '0': Strong pull down<br>D_OUT = '1': High Impedance<br>When D_OUT_EN = 0:<br>D_OUT = '0': High impedance<br>D_OUT = '1': High impedance<br><br>For peripherals other than GPIO & UDB/DSI:<br>When D_OUT_EN = 1:<br>D_OUT = '0': Strong pull down<br>D_OUT = '1': Strong pull up<br>When D_OUT_EN = 0:<br>D_OUT = '0': High Impedance<br>D_OUT = '1': High Impedance |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| | OD_DRIVESHIGH | | | 5 | Open drain, drives high<br><br>For GPIO & UDB/DSI peripherals:<br>When D_OUT_EN = 1:<br>D_OUT = '0': High Impedance<br>D_OUT = '1': Strong pull up<br>When D_OUT_EN = 0:<br>D_OUT = '0': High impedance<br>D_OUT = '1': High impedance<br><br>For peripherals other than GPIO & UDB/DSI:<br>When D_OUT_EN = 1:<br>D_OUT = '0': Strong pull down<br>D_OUT = '1': Strong pull up<br>When D_OUT_EN = 0:<br>D_OUT = '0': High Impedance<br>D_OUT = '1': High Impedance |
| | STRONG | | | 6 | Strong D_OUTput buffer<br><br>For GPIO & UDB/DSI peripherals:<br>When D_OUT_EN = 1:<br>D_OUT = '0': Strong pull down<br>D_OUT = '1': Strong pull up<br>When D_OUT_EN = 0:<br>D_OUT = '0': High impedance<br>D_OUT = '1': High impedance<br><br>For peripherals other than GPIO & UDB/DSI:<br>When D_OUT_EN = 1:<br>D_OUT = '0': Strong pull down<br>D_OUT = '1': Strong pull up<br>When D_OUT_EN = 0:<br>D_OUT = '0': High Impedance<br>D_OUT = '1': High Impedance |
| | PULLUP_DOWN | | | 7 | Pull up or pull down<br><br>For GPIO & UDB/DSI peripherals:<br>When D_OUT_EN = '0':<br>GPIO_DSI_OUT = '0': Weak/resistive pull down<br>GPIO_DSI_OUT = '1': Weak/resistive pull up<br>where 'GPIO_DSI_OUT' is a function of PORT_SEL, OUT & DSI_DATA_OUT.<br><br>For peripherals other than GPIO & UDB/DSI:<br>When D_OUT_EN = 1:<br>D_OUT = '0': Strong pull down<br>D_OUT = '1': Strong pull up<br>When D_OUT_EN = 0:<br>D_OUT = '0': Weak/resistive pull down<br>D_OUT = '1': Weak/resistive pull up |
| 3 | IN_EN0 | RW | R | 0 | Enables the input buffer for IO pin 0. This bit should be cleared when analog signals are present on the pin to avoid crowbar currents. The output buffer can be used to drive analog signals high or low without issue.<br>'0': Input buffer disabled<br>'1': Input buffer enabled |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 4:6 | DRIVE_MODE1 | RW | R | 0 | The GPIO drive mode for IO pin 1. Resistive pull-up and pull-down is selected in the drive mode.<br>Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the peripheral and HSIOM (HSIOM_PRT_SELx) is properly configured before turning the IO on here to avoid producing glitches on the bus.<br>Note: that peripherals other than GPIO & UDB/DSI directly control both the output and output-enable of the output buffer (peripherals can drive strong 0 or strong 1 in any mode except OFF='0').<br>Note: D_OUT, D_OUT_EN are pins of GPIO cell. |
| | HIGHZ | | | 0 | Output buffer is off creating a high impedance input<br>D_OUT = '0': High Impedance<br>D_OUT = '1': High Impedance |
| | RESERVED | | | 1 | N/A |
| | PULLUP | | | 2 | Resistive pull up<br><br>For GPIO & UDB/DSI peripherals:<br>When D_OUT_EN = 1:<br>D_OUT = '0': Strong pull down<br>D_OUT = '1': Weak/resistive pull up<br>When D_OUT_EN = 0:<br>D_OUT = '0': High impedance<br>D_OUT = '1': High impedance<br><br>For peripherals other than GPIO & UDB/DSI:<br>When D_OUT_EN = 1:<br>D_OUT = '0': Strong pull down<br>D_OUT = '1': Strong pull up<br>When D_OUT_EN = 0:<br>D_OUT = '0': Weak/resistive pull up<br>D_OUT = '1': Weak/resistive pull up |
| | PULLDOWN | | | 3 | Resistive pull down<br><br>For GPIO & UDB/DSI peripherals:<br>When D_OUT_EN = 1:<br>D_OUT = '0': Weak/resistive pull down<br>D_OUT = '1': Strong pull up<br>When D_OUT_EN = 0:<br>D_OUT = '0': High impedance<br>D_OUT = '1': High impedance<br><br>For peripherals other than GPIO & UDB/DSI:<br>When D_OUT_EN = 1:<br>D_OUT = '0': Strong pull down<br>D_OUT = '1': Strong pull up<br>When D_OUT_EN = 0:<br>D_OUT = '0': Weak/resistive pull down<br>D_OUT = '1': Weak/resistive pull down |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| | OD_DRIVESLOW | | | 4 | Open drain, drives low<br><br>For GPIO & UDB/DSI peripherals:<br>When D_OUT_EN = 1:<br>D_OUT = '0': Strong pull down<br>D_OUT = '1': High Impedance<br>When D_OUT_EN = 0:<br>D_OUT = '0': High impedance<br>D_OUT = '1': High impedance<br><br>For peripherals other than GPIO & UDB/DSI:<br>When D_OUT_EN = 1:<br>D_OUT = '0': Strong pull down<br>D_OUT = '1': Strong pull up<br>When D_OUT_EN = 0:<br>D_OUT = '0': High Impedance<br>D_OUT = '1': High Impedance |
| | OD_DRIVESHIGH | | | 5 | Open drain, drives high<br><br>For GPIO & UDB/DSI peripherals:<br>When D_OUT_EN = 1:<br>D_OUT = '0': High Impedance<br>D_OUT = '1': Strong pull up<br>When D_OUT_EN = 0:<br>D_OUT = '0': High impedance<br>D_OUT = '1': High impedance<br><br>For peripherals other than GPIO & UDB/DSI:<br>When D_OUT_EN = 1:<br>D_OUT = '0': Strong pull down<br>D_OUT = '1': Strong pull up<br>When D_OUT_EN = 0:<br>D_OUT = '0': High Impedance<br>D_OUT = '1': High Impedance |
| | STRONG | | | 6 | Strong D_OUTput buffer<br><br>For GPIO & UDB/DSI peripherals:<br>When D_OUT_EN = 1:<br>D_OUT = '0': Strong pull down<br>D_OUT = '1': Strong pull up<br>When D_OUT_EN = 0:<br>D_OUT = '0': High impedance<br>D_OUT = '1': High impedance<br><br>For peripherals other than GPIO & UDB/DSI:<br>When D_OUT_EN = 1:<br>D_OUT = '0': Strong pull down<br>D_OUT = '1': Strong pull up<br>When D_OUT_EN = 0:<br>D_OUT = '0': High Impedance<br>D_OUT = '1': High Impedance |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| | PULLUP_DOWN | | | 7 | Pull up or pull down<br><br>For GPIO & UDB/DSI peripherals:<br>When D_OUT_EN = '0':<br>GPIO_DSI_OUT = '0': Weak/resistive pull down<br>GPIO_DSI_OUT = '1': Weak/resistive pull up<br>where 'GPIO_DSI_OUT' is a function of PORT_SEL, OUT & DSI_DATA_OUT.<br><br>For peripherals other than GPIO & UDB/DSI:<br>When D_OUT_EN = 1:<br>D_OUT = '0': Strong pull down<br>D_OUT = '1': Strong pull up<br>When D_OUT_EN = 0:<br>D_OUT = '0': Weak/resistive pull down<br>D_OUT = '1': Weak/resistive pull up |
| 7 | IN_EN1 | RW | R | 0 | Enables the input buffer for IO pin 1 |
| 8:10 | DRIVE_MODE2 | RW | R | 0 | The GPIO drive mode for IO pin 2. Resistive pull-up and pull-down is selected in the drive mode.<br>Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the peripheral and HSIOM (HSIOM_PRT_SELx) is properly configured before turning the IO on here to avoid producing glitches on the bus.<br>Note: that peripherals other than GPIO & UDB/DSI directly control both the output and output-enable of the output buffer (peripherals can drive strong 0 or strong 1 in any mode except OFF='0').<br>Note: D_OUT, D_OUT_EN are pins of GPIO cell. |
| | HIGHZ | | | 0 | Output buffer is off creating a high impedance input<br>D_OUT = '0': High Impedance<br>D_OUT = '1': High Impedance |
| | RESERVED | | | 1 | N/A |
| | PULLUP | | | 2 | Resistive pull up<br><br>For GPIO & UDB/DSI peripherals:<br>When D_OUT_EN = 1:<br>D_OUT = '0': Strong pull down<br>D_OUT = '1': Weak/resistive pull up<br>When D_OUT_EN = 0:<br>D_OUT = '0': High impedance<br>D_OUT = '1': High impedance<br><br>For peripherals other than GPIO & UDB/DSI:<br>When D_OUT_EN = 1:<br>D_OUT = '0': Strong pull down<br>D_OUT = '1': Strong pull up<br>When D_OUT_EN = 0:<br>D_OUT = '0': Weak/resistive pull up<br>D_OUT = '1': Weak/resistive pull up |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| | PULLDOWN | | | 3 | Resistive pull down<br><br>For GPIO & UDB/DSI peripherals:<br>When D_OUT_EN = 1:<br>D_OUT = '0': Weak/resistive pull down<br>D_OUT = '1': Strong pull up<br>When D_OUT_EN = 0:<br>D_OUT = '0': High impedance<br>D_OUT = '1': High impedance<br><br>For peripherals other than GPIO & UDB/DSI:<br>When D_OUT_EN = 1:<br>D_OUT = '0': Strong pull down<br>D_OUT = '1': Strong pull up<br>When D_OUT_EN = 0:<br>D_OUT = '0': Weak/resistive pull down<br>D_OUT = '1': Weak/resistive pull down |
| | OD_DRIVESLOW | | | 4 | Open drain, drives low<br><br>For GPIO & UDB/DSI peripherals:<br>When D_OUT_EN = 1:<br>D_OUT = '0': Strong pull down<br>D_OUT = '1': High Impedance<br>When D_OUT_EN = 0:<br>D_OUT = '0': High impedance<br>D_OUT = '1': High impedance<br><br>For peripherals other than GPIO & UDB/DSI:<br>When D_OUT_EN = 1:<br>D_OUT = '0': Strong pull down<br>D_OUT = '1': Strong pull up<br>When D_OUT_EN = 0:<br>D_OUT = '0': High Impedance<br>D_OUT = '1': High Impedance |
| | OD_DRIVESHIGH | | | 5 | Open drain, drives high<br><br>For GPIO & UDB/DSI peripherals:<br>When D_OUT_EN = 1:<br>D_OUT = '0': High Impedance<br>D_OUT = '1': Strong pull up<br>When D_OUT_EN = 0:<br>D_OUT = '0': High impedance<br>D_OUT = '1': High impedance<br><br>For peripherals other than GPIO & UDB/DSI:<br>When D_OUT_EN = 1:<br>D_OUT = '0': Strong pull down<br>D_OUT = '1': Strong pull up<br>When D_OUT_EN = 0:<br>D_OUT = '0': High Impedance<br>D_OUT = '1': High Impedance |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| | STRONG | | | 6 | Strong D_OUTput buffer<br><br>For GPIO & UDB/DSI peripherals:<br>When D_OUT_EN = 1:<br>D_OUT = '0': Strong pull down<br>D_OUT = '1': Strong pull up<br>When D_OUT_EN = 0:<br>D_OUT = '0': High impedance<br>D_OUT = '1': High impedance<br><br>For peripherals other than GPIO & UDB/DSI:<br>When D_OUT_EN = 1:<br>D_OUT = '0': Strong pull down<br>D_OUT = '1': Strong pull up<br>When D_OUT_EN = 0:<br>D_OUT = '0': High Impedance<br>D_OUT = '1': High Impedance |
| | PULLUP_DOWN | | | 7 | Pull up or pull down<br><br>For GPIO & UDB/DSI peripherals:<br>When D_OUT_EN = '0':<br>GPIO_DSI_OUT = '0': Weak/resistive pull down<br>GPIO_DSI_OUT = '1': Weak/resistive pull up<br>where 'GPIO_DSI_OUT' is a function of PORT_SEL, OUT & DSI_DATA_OUT.<br><br>For peripherals other than GPIO & UDB/DSI:<br>When D_OUT_EN = 1:<br>D_OUT = '0': Strong pull down<br>D_OUT = '1': Strong pull up<br>When D_OUT_EN = 0:<br>D_OUT = '0': Weak/resistive pull down<br>D_OUT = '1': Weak/resistive pull up |
| 11 | IN_EN2 | RW | R | 0 | Enables the input buffer for IO pin 2 |
| 12:14 | DRIVE_MODE3 | RW | R | 0 | The GPIO drive mode for IO pin 3. Resistive pull-up and pull-down is selected in the drive mode.<br>Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the peripheral and HSIOM (HSIOM_PRT_SELx) is properly configured before turning the IO on here to avoid producing glitches on the bus.<br>Note: that peripherals other than GPIO & UDB/DSI directly control both the output and output-enable of the output buffer (peripherals can drive strong 0 or strong 1 in any mode except OFF='0').<br>Note: D_OUT, D_OUT_EN are pins of GPIO cell. |
| | HIGHZ | | | 0 | Output buffer is off creating a high impedance input<br>D_OUT = '0': High Impedance<br>D_OUT = '1': High Impedance |
| | RESERVED | | | 1 | N/A |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| | PULLUP | | | 2 | Resistive pull up<br><br>For GPIO & UDB/DSI peripherals:<br>When D_OUT_EN = 1:<br>D_OUT = '0': Strong pull down<br>D_OUT = '1': Weak/resistive pull up<br>When D_OUT_EN = 0:<br>D_OUT = '0': High impedance<br>D_OUT = '1': High impedance<br><br>For peripherals other than GPIO & UDB/DSI:<br>When D_OUT_EN = 1:<br>D_OUT = '0': Strong pull down<br>D_OUT = '1': Strong pull up<br>When D_OUT_EN = 0:<br>D_OUT = '0': Weak/resistive pull up<br>D_OUT = '1': Weak/resistive pull up |
| | PULLDOWN | | | 3 | Resistive pull down<br><br>For GPIO & UDB/DSI peripherals:<br>When D_OUT_EN = 1:<br>D_OUT = '0': Weak/resistive pull down<br>D_OUT = '1': Strong pull up<br>When D_OUT_EN = 0:<br>D_OUT = '0': High impedance<br>D_OUT = '1': High impedance<br><br>For peripherals other than GPIO & UDB/DSI:<br>When D_OUT_EN = 1:<br>D_OUT = '0': Strong pull down<br>D_OUT = '1': Strong pull up<br>When D_OUT_EN = 0:<br>D_OUT = '0': Weak/resistive pull down<br>D_OUT = '1': Weak/resistive pull down |
| | OD_DRIVESLOW | | | 4 | Open drain, drives low<br><br>For GPIO & UDB/DSI peripherals:<br>When D_OUT_EN = 1:<br>D_OUT = '0': Strong pull down<br>D_OUT = '1': High Impedance<br>When D_OUT_EN = 0:<br>D_OUT = '0': High impedance<br>D_OUT = '1': High impedance<br><br>For peripherals other than GPIO & UDB/DSI:<br>When D_OUT_EN = 1:<br>D_OUT = '0': Strong pull down<br>D_OUT = '1': Strong pull up<br>When D_OUT_EN = 0:<br>D_OUT = '0': High Impedance<br>D_OUT = '1': High Impedance |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| | OD_DRIVESHIGH | | | 5 | Open drain, drives high<br><br>For GPIO & UDB/DSI peripherals:<br>When D_OUT_EN = 1:<br>D_OUT = '0': High Impedance<br>D_OUT = '1': Strong pull up<br>When D_OUT_EN = 0:<br>D_OUT = '0': High impedance<br>D_OUT = '1': High impedance<br><br>For peripherals other than GPIO & UDB/DSI:<br>When D_OUT_EN = 1:<br>D_OUT = '0': Strong pull down<br>D_OUT = '1': Strong pull up<br>When D_OUT_EN = 0:<br>D_OUT = '0': High Impedance<br>D_OUT = '1': High Impedance |
| | STRONG | | | 6 | Strong D_OUTput buffer<br><br>For GPIO & UDB/DSI peripherals:<br>When D_OUT_EN = 1:<br>D_OUT = '0': Strong pull down<br>D_OUT = '1': Strong pull up<br>When D_OUT_EN = 0:<br>D_OUT = '0': High impedance<br>D_OUT = '1': High impedance<br><br>For peripherals other than GPIO & UDB/DSI:<br>When D_OUT_EN = 1:<br>D_OUT = '0': Strong pull down<br>D_OUT = '1': Strong pull up<br>When D_OUT_EN = 0:<br>D_OUT = '0': High Impedance<br>D_OUT = '1': High Impedance |
| | PULLUP_DOWN | | | 7 | Pull up or pull down<br><br>For GPIO & UDB/DSI peripherals:<br>When D_OUT_EN = '0':<br>GPIO_DSI_OUT = '0': Weak/resistive pull down<br>GPIO_DSI_OUT = '1': Weak/resistive pull up<br>where 'GPIO_DSI_OUT' is a function of PORT_SEL, OUT & DSI_DATA_OUT.<br><br>For peripherals other than GPIO & UDB/DSI:<br>When D_OUT_EN = 1:<br>D_OUT = '0': Strong pull down<br>D_OUT = '1': Strong pull up<br>When D_OUT_EN = 0:<br>D_OUT = '0': Weak/resistive pull down<br>D_OUT = '1': Weak/resistive pull up |
| 15 | IN_EN3 | RW | R | 0 | Enables the input buffer for IO pin 3 |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 16:18 | DRIVE_MODE4 | RW | R | 0 | The GPIO drive mode for IO pin 4. Resistive pull-up and pull-down is selected in the drive mode.<br>Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the peripheral and HSIOM (HSIOM_PRT_SELx) is properly configured before turning the IO on here to avoid producing glitches on the bus.<br>Note: that peripherals other than GPIO & UDB/DSI directly control both the output and output-enable of the output buffer (peripherals can drive strong 0 or strong 1 in any mode except OFF='0').<br>Note: D_OUT, D_OUT_EN are pins of GPIO cell. |
| | HIGHZ | | | 0 | Output buffer is off creating a high impedance input<br>D_OUT = '0': High Impedance<br>D_OUT = '1': High Impedance |
| | RESERVED | | | 1 | N/A |
| | PULLUP | | | 2 | Resistive pull up<br><br>For GPIO & UDB/DSI peripherals:<br>When D_OUT_EN = 1:<br>D_OUT = '0': Strong pull down<br>D_OUT = '1': Weak/resistive pull up<br>When D_OUT_EN = 0:<br>D_OUT = '0': High impedance<br>D_OUT = '1': High impedance<br><br>For peripherals other than GPIO & UDB/DSI:<br>When D_OUT_EN = 1:<br>D_OUT = '0': Strong pull down<br>D_OUT = '1': Strong pull up<br>When D_OUT_EN = 0:<br>D_OUT = '0': Weak/resistive pull up<br>D_OUT = '1': Weak/resistive pull up |
| | PULLDOWN | | | 3 | Resistive pull down<br><br>For GPIO & UDB/DSI peripherals:<br>When D_OUT_EN = 1:<br>D_OUT = '0': Weak/resistive pull down<br>D_OUT = '1': Strong pull up<br>When D_OUT_EN = 0:<br>D_OUT = '0': High impedance<br>D_OUT = '1': High impedance<br><br>For peripherals other than GPIO & UDB/DSI:<br>When D_OUT_EN = 1:<br>D_OUT = '0': Strong pull down<br>D_OUT = '1': Strong pull up<br>When D_OUT_EN = 0:<br>D_OUT = '0': Weak/resistive pull down<br>D_OUT = '1': Weak/resistive pull down |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| | OD_DRIVESLOW | | | 4 | Open drain, drives low<br><br>For GPIO & UDB/DSI peripherals:<br>When D_OUT_EN = 1:<br>D_OUT = '0': Strong pull down<br>D_OUT = '1': High Impedance<br>When D_OUT_EN = 0:<br>D_OUT = '0': High impedance<br>D_OUT = '1': High impedance<br><br>For peripherals other than GPIO & UDB/DSI:<br>When D_OUT_EN = 1:<br>D_OUT = '0': Strong pull down<br>D_OUT = '1': Strong pull up<br>When D_OUT_EN = 0:<br>D_OUT = '0': High Impedance<br>D_OUT = '1': High Impedance |
| | OD_DRIVESHIGH | | | 5 | Open drain, drives high<br><br>For GPIO & UDB/DSI peripherals:<br>When D_OUT_EN = 1:<br>D_OUT = '0': High Impedance<br>D_OUT = '1': Strong pull up<br>When D_OUT_EN = 0:<br>D_OUT = '0': High impedance<br>D_OUT = '1': High impedance<br><br>For peripherals other than GPIO & UDB/DSI:<br>When D_OUT_EN = 1:<br>D_OUT = '0': Strong pull down<br>D_OUT = '1': Strong pull up<br>When D_OUT_EN = 0:<br>D_OUT = '0': High Impedance<br>D_OUT = '1': High Impedance |
| | STRONG | | | 6 | Strong D_OUTput buffer<br><br>For GPIO & UDB/DSI peripherals:<br>When D_OUT_EN = 1:<br>D_OUT = '0': Strong pull down<br>D_OUT = '1': Strong pull up<br>When D_OUT_EN = 0:<br>D_OUT = '0': High impedance<br>D_OUT = '1': High impedance<br><br>For peripherals other than GPIO & UDB/DSI:<br>When D_OUT_EN = 1:<br>D_OUT = '0': Strong pull down<br>D_OUT = '1': Strong pull up<br>When D_OUT_EN = 0:<br>D_OUT = '0': High Impedance<br>D_OUT = '1': High Impedance |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| | PULLUP_DOWN | | | 7 | Pull up or pull down<br><br>For GPIO & UDB/DSI peripherals:<br>When D_OUT_EN = '0':<br>GPIO_DSI_OUT = '0': Weak/resistive pull down<br>GPIO_DSI_OUT = '1': Weak/resistive pull up<br>where 'GPIO_DSI_OUT' is a function of PORT_SEL, OUT & DSI_DATA_OUT.<br><br>For peripherals other than GPIO & UDB/DSI:<br>When D_OUT_EN = 1:<br>D_OUT = '0': Strong pull down<br>D_OUT = '1': Strong pull up<br>When D_OUT_EN = 0:<br>D_OUT = '0': Weak/resistive pull down<br>D_OUT = '1': Weak/resistive pull up |
| 19 | IN_EN4 | RW | R | 0 | Enables the input buffer for IO pin 4 |
| 20:22 | DRIVE_MODE5 | RW | R | 0 | The GPIO drive mode for IO pin 5. Resistive pull-up and pull-down is selected in the drive mode.<br>Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the peripheral and HSIOM (HSIOM_PRT_SELx) is properly configured before turning the IO on here to avoid producing glitches on the bus.<br>Note: that peripherals other than GPIO & UDB/DSI directly control both the output and output-enable of the output buffer (peripherals can drive strong 0 or strong 1 in any mode except OFF='0').<br>Note: D_OUT, D_OUT_EN are pins of GPIO cell. |
| | HIGHZ | | | 0 | Output buffer is off creating a high impedance input<br>D_OUT = '0': High Impedance<br>D_OUT = '1': High Impedance |
| | RESERVED | | | 1 | N/A |
| | PULLUP | | | 2 | Resistive pull up<br><br>For GPIO & UDB/DSI peripherals:<br>When D_OUT_EN = 1:<br>D_OUT = '0': Strong pull down<br>D_OUT = '1': Weak/resistive pull up<br>When D_OUT_EN = 0:<br>D_OUT = '0': High impedance<br>D_OUT = '1': High impedance<br><br>For peripherals other than GPIO & UDB/DSI:<br>When D_OUT_EN = 1:<br>D_OUT = '0': Strong pull down<br>D_OUT = '1': Strong pull up<br>When D_OUT_EN = 0:<br>D_OUT = '0': Weak/resistive pull up<br>D_OUT = '1': Weak/resistive pull up |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| | PULLDOWN | | | 3 | Resistive pull down<br><br>For GPIO & UDB/DSI peripherals:<br>When D_OUT_EN = 1:<br>D_OUT = '0': Weak/resistive pull down<br>D_OUT = '1': Strong pull up<br>When D_OUT_EN = 0:<br>D_OUT = '0': High impedance<br>D_OUT = '1': High impedance<br><br>For peripherals other than GPIO & UDB/DSI:<br>When D_OUT_EN = 1:<br>D_OUT = '0': Strong pull down<br>D_OUT = '1': Strong pull up<br>When D_OUT_EN = 0:<br>D_OUT = '0': Weak/resistive pull down<br>D_OUT = '1': Weak/resistive pull down |
| | OD_DRIVESLOW | | | 4 | Open drain, drives low<br><br>For GPIO & UDB/DSI peripherals:<br>When D_OUT_EN = 1:<br>D_OUT = '0': Strong pull down<br>D_OUT = '1': High Impedance<br>When D_OUT_EN = 0:<br>D_OUT = '0': High impedance<br>D_OUT = '1': High impedance<br><br>For peripherals other than GPIO & UDB/DSI:<br>When D_OUT_EN = 1:<br>D_OUT = '0': Strong pull down<br>D_OUT = '1': Strong pull up<br>When D_OUT_EN = 0:<br>D_OUT = '0': High Impedance<br>D_OUT = '1': High Impedance |
| | OD_DRIVESHIGH | | | 5 | Open drain, drives high<br><br>For GPIO & UDB/DSI peripherals:<br>When D_OUT_EN = 1:<br>D_OUT = '0': High Impedance<br>D_OUT = '1': Strong pull up<br>When D_OUT_EN = 0:<br>D_OUT = '0': High impedance<br>D_OUT = '1': High impedance<br><br>For peripherals other than GPIO & UDB/DSI:<br>When D_OUT_EN = 1:<br>D_OUT = '0': Strong pull down<br>D_OUT = '1': Strong pull up<br>When D_OUT_EN = 0:<br>D_OUT = '0': High Impedance<br>D_OUT = '1': High Impedance |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| | STRONG | | | 6 | Strong D_OUTput buffer<br><br>For GPIO & UDB/DSI peripherals:<br>When D_OUT_EN = 1:<br>D_OUT = '0': Strong pull down<br>D_OUT = '1': Strong pull up<br>When D_OUT_EN = 0:<br>D_OUT = '0': High impedance<br>D_OUT = '1': High impedance<br><br>For peripherals other than GPIO & UDB/DSI:<br>When D_OUT_EN = 1:<br>D_OUT = '0': Strong pull down<br>D_OUT = '1': Strong pull up<br>When D_OUT_EN = 0:<br>D_OUT = '0': High Impedance<br>D_OUT = '1': High Impedance |
| | PULLUP_DOWN | | | 7 | Pull up or pull down<br><br>For GPIO & UDB/DSI peripherals:<br>When D_OUT_EN = '0':<br>GPIO_DSI_OUT = '0': Weak/resistive pull down<br>GPIO_DSI_OUT = '1': Weak/resistive pull up<br>where 'GPIO_DSI_OUT' is a function of PORT_SEL, OUT & DSI_DATA_OUT.<br><br>For peripherals other than GPIO & UDB/DSI:<br>When D_OUT_EN = 1:<br>D_OUT = '0': Strong pull down<br>D_OUT = '1': Strong pull up<br>When D_OUT_EN = 0:<br>D_OUT = '0': Weak/resistive pull down<br>D_OUT = '1': Weak/resistive pull up |
| 23 | IN_EN5 | RW | R | 0 | Enables the input buffer for IO pin 5 |
| 24:26 | DRIVE_MODE6 | RW | R | 0 | The GPIO drive mode for IO pin 6. Resistive pull-up and pull-down is selected in the drive mode.<br>Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the peripheral and HSIOM (HSIOM_PRT_SELx) is properly configured before turning the IO on here to avoid producing glitches on the bus.<br>Note: that peripherals other than GPIO & UDB/DSI directly control both the output and output-enable of the output buffer (peripherals can drive strong 0 or strong 1 in any mode except OFF='0').<br>Note: D_OUT, D_OUT_EN are pins of GPIO cell. |
| | HIGHZ | | | 0 | Output buffer is off creating a high impedance input<br>D_OUT = '0': High Impedance<br>D_OUT = '1': High Impedance |
| | RESERVED | | | 1 | N/A |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| | PULLUP | | | 2 | Resistive pull up<br><br>For GPIO & UDB/DSI peripherals:<br>When D_OUT_EN = 1:<br>D_OUT = '0': Strong pull down<br>D_OUT = '1': Weak/resistive pull up<br>When D_OUT_EN = 0:<br>D_OUT = '0': High impedance<br>D_OUT = '1': High impedance<br><br>For peripherals other than GPIO & UDB/DSI:<br>When D_OUT_EN = 1:<br>D_OUT = '0': Strong pull down<br>D_OUT = '1': Strong pull up<br>When D_OUT_EN = 0:<br>D_OUT = '0': Weak/resistive pull up<br>D_OUT = '1': Weak/resistive pull up |
| | PULLDOWN | | | 3 | Resistive pull down<br><br>For GPIO & UDB/DSI peripherals:<br>When D_OUT_EN = 1:<br>D_OUT = '0': Weak/resistive pull down<br>D_OUT = '1': Strong pull up<br>When D_OUT_EN = 0:<br>D_OUT = '0': High impedance<br>D_OUT = '1': High impedance<br><br>For peripherals other than GPIO & UDB/DSI:<br>When D_OUT_EN = 1:<br>D_OUT = '0': Strong pull down<br>D_OUT = '1': Strong pull up<br>When D_OUT_EN = 0:<br>D_OUT = '0': Weak/resistive pull down<br>D_OUT = '1': Weak/resistive pull down |
| | OD_DRIVESLOW | | | 4 | Open drain, drives low<br><br>For GPIO & UDB/DSI peripherals:<br>When D_OUT_EN = 1:<br>D_OUT = '0': Strong pull down<br>D_OUT = '1': High Impedance<br>When D_OUT_EN = 0:<br>D_OUT = '0': High impedance<br>D_OUT = '1': High impedance<br><br>For peripherals other than GPIO & UDB/DSI:<br>When D_OUT_EN = 1:<br>D_OUT = '0': Strong pull down<br>D_OUT = '1': Strong pull up<br>When D_OUT_EN = 0:<br>D_OUT = '0': High Impedance<br>D_OUT = '1': High Impedance |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| | OD_DRIVESHIGH | | | 5 | Open drain, drives high<br><br>For GPIO & UDB/DSI peripherals:<br>When D_OUT_EN = 1:<br>D_OUT = '0': High Impedance<br>D_OUT = '1': Strong pull up<br>When D_OUT_EN = 0:<br>D_OUT = '0': High impedance<br>D_OUT = '1': High impedance<br><br>For peripherals other than GPIO & UDB/DSI:<br>When D_OUT_EN = 1:<br>D_OUT = '0': Strong pull down<br>D_OUT = '1': Strong pull up<br>When D_OUT_EN = 0:<br>D_OUT = '0': High Impedance<br>D_OUT = '1': High Impedance |
| | STRONG | | | 6 | Strong D_OUTput buffer<br><br>For GPIO & UDB/DSI peripherals:<br>When D_OUT_EN = 1:<br>D_OUT = '0': Strong pull down<br>D_OUT = '1': Strong pull up<br>When D_OUT_EN = 0:<br>D_OUT = '0': High impedance<br>D_OUT = '1': High impedance<br><br>For peripherals other than GPIO & UDB/DSI:<br>When D_OUT_EN = 1:<br>D_OUT = '0': Strong pull down<br>D_OUT = '1': Strong pull up<br>When D_OUT_EN = 0:<br>D_OUT = '0': High Impedance<br>D_OUT = '1': High Impedance |
| | PULLUP_DOWN | | | 7 | Pull up or pull down<br><br>For GPIO & UDB/DSI peripherals:<br>When D_OUT_EN = '0':<br>GPIO_DSI_OUT = '0': Weak/resistive pull down<br>GPIO_DSI_OUT = '1': Weak/resistive pull up<br>where 'GPIO_DSI_OUT' is a function of PORT_SEL, OUT & DSI_DATA_OUT.<br><br>For peripherals other than GPIO & UDB/DSI:<br>When D_OUT_EN = 1:<br>D_OUT = '0': Strong pull down<br>D_OUT = '1': Strong pull up<br>When D_OUT_EN = 0:<br>D_OUT = '0': Weak/resistive pull down<br>D_OUT = '1': Weak/resistive pull up |
| 27 | IN_EN6 | RW | R | 0 | Enables the input buffer for IO pin 6 |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 28:30 | DRIVE_MODE7 | RW | R | 0 | The GPIO drive mode for IO pin 7. Resistive pull-up and pull-down is selected in the drive mode.<br>Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the peripheral and HSIOM (HSIOM_PRT_SELx) is properly configured before turning the IO on here to avoid producing glitches on the bus.<br>Note: that peripherals other than GPIO & UDB/DSI directly control both the output and output-enable of the output buffer (peripherals can drive strong 0 or strong 1 in any mode except OFF='0').<br>Note: D_OUT, D_OUT_EN are pins of GPIO cell. |
| | HIGHZ | | | 0 | Output buffer is off creating a high impedance input<br>D_OUT = '0': High Impedance<br>D_OUT = '1': High Impedance |
| | RESERVED | | | 1 | N/A |
| | PULLUP | | | 2 | Resistive pull up<br><br>For GPIO & UDB/DSI peripherals:<br>When D_OUT_EN = 1:<br>D_OUT = '0': Strong pull down<br>D_OUT = '1': Weak/resistive pull up<br>When D_OUT_EN = 0:<br>D_OUT = '0': High impedance<br>D_OUT = '1': High impedance<br><br>For peripherals other than GPIO & UDB/DSI:<br>When D_OUT_EN = 1:<br>D_OUT = '0': Strong pull down<br>D_OUT = '1': Strong pull up<br>When D_OUT_EN = 0:<br>D_OUT = '0': Weak/resistive pull up<br>D_OUT = '1': Weak/resistive pull up |
| | PULLDOWN | | | 3 | Resistive pull down<br><br>For GPIO & UDB/DSI peripherals:<br>When D_OUT_EN = 1:<br>D_OUT = '0': Weak/resistive pull down<br>D_OUT = '1': Strong pull up<br>When D_OUT_EN = 0:<br>D_OUT = '0': High impedance<br>D_OUT = '1': High impedance<br><br>For peripherals other than GPIO & UDB/DSI:<br>When D_OUT_EN = 1:<br>D_OUT = '0': Strong pull down<br>D_OUT = '1': Strong pull up<br>When D_OUT_EN = 0:<br>D_OUT = '0': Weak/resistive pull down<br>D_OUT = '1': Weak/resistive pull down |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| | OD_DRIVESLOW | | | 4 | Open drain, drives low<br><br>For GPIO & UDB/DSI peripherals:<br>When D_OUT_EN = 1:<br>D_OUT = '0': Strong pull down<br>D_OUT = '1': High Impedance<br>When D_OUT_EN = 0:<br>D_OUT = '0': High impedance<br>D_OUT = '1': High impedance<br><br>For peripherals other than GPIO & UDB/DSI:<br>When D_OUT_EN = 1:<br>D_OUT = '0': Strong pull down<br>D_OUT = '1': Strong pull up<br>When D_OUT_EN = 0:<br>D_OUT = '0': High Impedance<br>D_OUT = '1': High Impedance |
| | OD_DRIVESHIGH | | | 5 | Open drain, drives high<br><br>For GPIO & UDB/DSI peripherals:<br>When D_OUT_EN = 1:<br>D_OUT = '0': High Impedance<br>D_OUT = '1': Strong pull up<br>When D_OUT_EN = 0:<br>D_OUT = '0': High impedance<br>D_OUT = '1': High impedance<br><br>For peripherals other than GPIO & UDB/DSI:<br>When D_OUT_EN = 1:<br>D_OUT = '0': Strong pull down<br>D_OUT = '1': Strong pull up<br>When D_OUT_EN = 0:<br>D_OUT = '0': High Impedance<br>D_OUT = '1': High Impedance |
| | STRONG | | | 6 | Strong D_OUTput buffer<br><br>For GPIO & UDB/DSI peripherals:<br>When D_OUT_EN = 1:<br>D_OUT = '0': Strong pull down<br>D_OUT = '1': Strong pull up<br>When D_OUT_EN = 0:<br>D_OUT = '0': High impedance<br>D_OUT = '1': High impedance<br><br>For peripherals other than GPIO & UDB/DSI:<br>When D_OUT_EN = 1:<br>D_OUT = '0': Strong pull down<br>D_OUT = '1': Strong pull up<br>When D_OUT_EN = 0:<br>D_OUT = '0': High Impedance<br>D_OUT = '1': High Impedance |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| | PULLUP_DOWN | | | 7 | Pull up or pull down<br><br>For GPIO & UDB/DSI peripherals:<br>When D_OUT_EN = '0':<br>GPIO_DSI_OUT = '0': Weak/resistive pull down<br>GPIO_DSI_OUT = '1': Weak/resistive pull up<br>where 'GPIO_DSI_OUT' is a function of PORT_SEL, OUT & DSI_DATA_OUT.<br><br>For peripherals other than GPIO & UDB/DSI:<br>When D_OUT_EN = 1:<br>D_OUT = '0': Strong pull down<br>D_OUT = '1': Strong pull up<br>When D_OUT_EN = 0:<br>D_OUT = '0': Weak/resistive pull down<br>D_OUT = '1': Weak/resistive pull up |
| 31 | IN_EN7 | RW | R | 0 | Enables the input buffer for IO pin 7 |

### 16.36.8.12 GPIO_PRT_CFG_IN

**Description:** Port input buffer configuration register
**Address:** 0x40310048
**Offset:** 0x48
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Configures the input buffer for each pin and this register is common for PSoC6: & Traveo II: GPIO pins. For Traveo II: GPIO pin, this register control the lower bit i.e. VTRIP_SEL[0].
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VTRIP_SEL 7_0 [7:7] | VTRIP_SEL 6_0 [6:6] | VTRIP_SEL 5_0 [5:5] | VTRIP_SEL 4_0 [4:4] | VTRIP_SEL 3_0 [3:3] | VTRIP_SEL 2_0 [2:2] | VTRIP_SEL 1_0 [1:1] | VTRIP_SEL 0_0 [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | VTRIP_SEL0_0 | RW | R | 0 | Configures the pin 0 input buffer mode (trip points and hysteresis) |
| | CMOS | | | 0 | PSoC6:: Input buffer compatible with CMOS and I2C interfaces<br>Traveo II: full encoding is shown in CFG_IN_AUTOLVL.VTRIP_SEL0_1 |
| | TTL | | | 1 | PSoC6:: Input buffer compatible with TTL and MediaLB interfaces<br>Traveo II: full encoding is shown in CFG_IN_AUTOLVL.VTRIP_SEL0_1 |
| 1 | VTRIP_SEL1_0 | RW | R | 0 | Configures the pin 1 input buffer mode (trip points and hysteresis) |
| 2 | VTRIP_SEL2_0 | RW | R | 0 | Configures the pin 2 input buffer mode (trip points and hysteresis) |
| 3 | VTRIP_SEL3_0 | RW | R | 0 | Configures the pin 3 input buffer mode (trip points and hysteresis) |
| 4 | VTRIP_SEL4_0 | RW | R | 0 | Configures the pin 4 input buffer mode (trip points and hysteresis) |
| 5 | VTRIP_SEL5_0 | RW | R | 0 | Configures the pin 5 input buffer mode (trip points and hysteresis) |
| 6 | VTRIP_SEL6_0 | RW | R | 0 | Configures the pin 6 input buffer mode (trip points and hysteresis) |
| 7 | VTRIP_SEL7_0 | RW | R | 0 | Configures the pin 7 input buffer mode (trip points and hysteresis) |

### 16.36.8.13 GPIO_PRT_CFG_OUT

**Description:** Port output buffer configuration register
**Address:** 0x4031004C
**Offset:** 0x4C
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Configures the output driver for each pin.
Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the peripheral and HSIOM (HSIOM_PRT_SELx) is properly configured before setting the IO drive mode to avoid producing glitches on the bus.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:4] | | | | SLOW3 [3:3] | SLOW2 [2:2] | SLOW1 [1:1] | SLOW0 [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | DRIVE_SEL3 [23:22] | | DRIVE_SEL2 [21:20] | | DRIVE_SEL1 [19:18] | | DRIVE_SEL0 [17:16] | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | DRIVE_SEL7 [31:30] | | DRIVE_SEL6 [29:28] | | DRIVE_SEL5 [27:26] | | DRIVE_SEL4 [25:24] | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | SLOW0 | RW | R | 0 | Enables slow slew rate for IO pin 0<br>'0': Fast slew rate<br>'1': Slow slew rate |
| 1 | SLOW1 | RW | R | 0 | Enables slow slew rate for IO pin 1 |
| 2 | SLOW2 | RW | R | 0 | Enables slow slew rate for IO pin 2 |
| 3 | SLOW3 | RW | R | 0 | Enables slow slew rate for IO pin 3 |
| 16:17 | DRIVE_SEL0 | RW | R | 0 | Sets the GPIO drive strength for IO pin 0 |
| | DRIVE_SEL_ZERO | | | 0 | Please refer to architecture TRM section I/O System |
| | DRIVE_SEL_ONE | | | 1 | Please refer to architecture TRM section I/O System |
| | DRIVE_SEL_TWO | | | 2 | Please refer to architecture TRM section I/O System |
| | DRIVE_SEL_THREE | | | 3 | Please refer to architecture TRM section I/O System |
| 18:19 | DRIVE_SEL1 | RW | R | 0 | Sets the GPIO drive strength for IO pin 1 |
| 20:21 | DRIVE_SEL2 | RW | R | 0 | Sets the GPIO drive strength for IO pin 2 |
| 22:23 | DRIVE_SEL3 | RW | R | 0 | Sets the GPIO drive strength for IO pin 3 |
| 24:25 | DRIVE_SEL4 | RW | R | 0 | Sets the GPIO drive strength for IO pin 4 |
| 26:27 | DRIVE_SEL5 | RW | R | 0 | Sets the GPIO drive strength for IO pin 5 |
| 28:29 | DRIVE_SEL6 | RW | R | 0 | Sets the GPIO drive strength for IO pin 6 |
| 30:31 | DRIVE_SEL7 | RW | R | 0 | Sets the GPIO drive strength for IO pin 7 |

### 16.36.8.14 GPIO_PRT_CFG_IN_AUTOLVL

**Description:** Port input buffer AUTOLVL configuration register
**Address:** 0x40310058
**Offset:** 0x58
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Configures the GPIO input buffer upper bit i.e. VTRIP_SEL[1] for each pin.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VTRIP_SEL 7_1 [7:7] | VTRIP_SEL 6_1 [6:6] | VTRIP_SEL 5_1 [5:5] | VTRIP_SEL 4_1 [4:4] | VTRIP_SEL 3_1 [3:3] | VTRIP_SEL 2_1 [2:2] | VTRIP_SEL 1_1 [1:1] | VTRIP_SEL 0_1 [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | VTRIP_SEL0_1 | RW | R | 0 | Configures the input buffer mode (trip points and hysteresis) for GPIO upper bit. Lower bit is still selected by CFG_IN.VTRIP_SEL0_0 field. This field is used along with CFG_IN.VTRIP_SEL0_0 field as below:<br>{CFG_IN_AUTOLVL.VTRIP_SEL0_1,CFG_IN.VTRIP_SEL0_0}:<br><br>0,0: CMOS<br>0,1: TTL<br>1,0: input buffer is compatible with automotive.<br>1,1: input buffer is compatible with automotive. |
| | CMOS_OR_TTL | | | 0 | Input buffer compatible with CMOS/TTL interfaces as described in CFG_IN.VTRIP_SEL0_0. |
| | AUTO | | | 1 | Input buffer compatible with AUTO (elevated Vil) interfaces when used along with CFG_IN.VTRIP_SEL0_0. |
| 1 | VTRIP_SEL1_1 | RW | R | 0 | Input buffer compatible with automotive (elevated Vil) interfaces. |
| 2 | VTRIP_SEL2_1 | RW | R | 0 | Input buffer compatible with automotive (elevated Vil) interfaces. |
| 3 | VTRIP_SEL3_1 | RW | R | 0 | Input buffer compatible with automotive (elevated Vil) interfaces. |
| 4 | VTRIP_SEL4_1 | RW | R | 0 | Input buffer compatible with automotive (elevated Vil) interfaces. |
| 5 | VTRIP_SEL5_1 | RW | R | 0 | Input buffer compatible with automotive (elevated Vil) interfaces. |
| 6 | VTRIP_SEL6_1 | RW | R | 0 | Input buffer compatible with automotive (elevated Vil) interfaces. |
| 7 | VTRIP_SEL7_1 | RW | R | 0 | Input buffer compatible with automotive (elevated Vil) interfaces. |

# 17 HSIOM

**Description** High Speed IO Matrix (HSIOM)
**Base Address** 0x40300000
**Size** 0x4000
**Slave Num** MMIO3 - 0

| Register Name | Address | Permission | Description |
|---|---|---|---|
| HSIOM_AMUX_SPLIT_CTL0 | 0x40302000 | FULL | AMUX splitter cell control |
| HSIOM_AMUX_SPLIT_CTL1 | 0x40302004 | FULL | AMUX splitter cell control |
| HSIOM_AMUX_SPLIT_CTL2 | 0x40302008 | FULL | AMUX splitter cell control |
| HSIOM_AMUX_SPLIT_CTL3 | 0x4030200C | FULL | AMUX splitter cell control |
| HSIOM_MONITOR_CTL_0 | 0x40302200 | FULL | Power/Ground Monitor cell control 0 |
| HSIOM_ALT_JTAG_EN | 0x40302240 | FULL | Alternate JTAG IF selection register |

## 17.1 PRT 0

| Register Name | Address | Permission | Description |
|---|---|---|---|
| HSIOM_PRT0_PORT_SEL0 | 0x40300000 | FULL | Port selection 0 |

## 17.2 PRT 1

| Register Name | Address | Permission | Description |
|---|---|---|---|
| HSIOM_PRT1_PORT_SEL0 | 0x40300010 | FULL | Port selection 0 |
| HSIOM_PRT1_PORT_SEL1 | 0x40300014 | FULL | Port selection 1<br>Note:IO7_SEL is not available for this register |

## 17.3 PRT 2

| Register Name | Address | Permission | Description |
|---|---|---|---|
| HSIOM_PRT2_PORT_SEL0 | 0x40300020 | FULL | Port selection 0 |
| HSIOM_PRT2_PORT_SEL1 | 0x40300024 | FULL | Port selection 1 |

## 17.4 PRT 3

| Register Name | Address | Permission | Description |
|---|---|---|---|
| HSIOM_PRT3_PORT_SEL0 | 0x40300030 | FULL | Port selection 0 |
| HSIOM_PRT3_PORT_SEL1 | 0x40300034 | FULL | Port selection 1 |

## 17.5 PRT 4

| Register Name | Address | Permission | Description |
|---|---|---|---|
| HSIOM_PRT4_PORT_SEL0 | 0x40300040 | FULL | Port selection 0 |
| HSIOM_PRT4_PORT_SEL1 | 0x40300044 | FULL | Port selection 1<br>Note:IO7_SEL is not available for this register |

## 17.6 PRT 5

| Register Name | Address | Permission | Description |
|---|---|---|---|
| HSIOM_PRT5_PORT_SEL0 | 0x40300050 | FULL | Port selection 0 |
| HSIOM_PRT5_PORT_SEL1 | 0x40300054 | FULL | Port selection 1<br>Note:IO6_SEL IO7_SEL are not available for this register |

## 17.7 PRT 6

| Register Name | Address | Permission | Description |
|---|---|---|---|
| HSIOM_PRT6_PORT_SEL0 | 0x40300060 | FULL | Port selection 0 |
| HSIOM_PRT6_PORT_SEL1 | 0x40300064 | FULL | Port selection 1 |

## 17.8 PRT 7

| Register Name | Address | Permission | Description |
|---|---|---|---|
| HSIOM_PRT7_PORT_SEL0 | 0x40300070 | FULL | Port selection 0 |
| HSIOM_PRT7_PORT_SEL1 | 0x40300074 | FULL | Port selection 1 |

## 17.9 PRT 8

| Register Name | Address | Permission | Description |
|---|---|---|---|
| HSIOM_PRT8_PORT_SEL0 | 0x40300080 | FULL | Port selection 0 |
| HSIOM_PRT8_PORT_SEL1 | 0x40300084 | FULL | Port selection 1<br>Note:IO5_SEL IO6_SEL IO7_SEL are not available for this register |

## 17.10 PRT 9

| Register Name | Address | Permission | Description |
|---|---|---|---|
| HSIOM_PRT9_PORT_SEL0 | 0x40300090 | FULL | Port selection 0 |

## 17.11 PRT 10

| Register Name | Address | Permission | Description |
|---|---|---|---|
| HSIOM_PRT10_PORT_SEL0 | 0x403000A0 | FULL | Port selection 0 |
| HSIOM_PRT10_PORT_SEL1 | 0x403000A4 | FULL | Port selection 1 |

## 17.12 PRT 11

| Register Name | Address | Permission | Description |
|---|---|---|---|
| HSIOM_PRT11_PORT_SEL0 | 0x403000B0 | FULL | Port selection 0<br>Note:IO3_SEL is not available for this register |

## 17.13 PRT 12

| Register Name | Address | Permission | Description |
|---|---|---|---|
| HSIOM_PRT12_PORT_SEL0 | 0x403000C0 | FULL | Port selection 0 |
| HSIOM_PRT12_PORT_SEL1 | 0x403000C4 | FULL | Port selection 1 |

## 17.14 PRT 13

| Register Name | Address | Permission | Description |
|---|---|---|---|
| HSIOM_PRT13_PORT_SEL0 | 0x403000D0 | FULL | Port selection 0 |
| HSIOM_PRT13_PORT_SEL1 | 0x403000D4 | FULL | Port selection 1 |

## 17.15 PRT 14

| Register Name | Address | Permission | Description |
|---|---|---|---|
| HSIOM_PRT14_PORT_SEL0 | 0x403000E0 | FULL | Port selection 0 |
| HSIOM_PRT14_PORT_SEL1 | 0x403000E4 | FULL | Port selection 1 |

## 17.16 PRT 15

| Register Name | Address | Permission | Description |
|---|---|---|---|
| HSIOM_PRT15_PORT_SEL0 | 0x403000F0 | FULL | Port selection 0 |

## 17.17 PRT 16

| Register Name | Address | Permission | Description |
|---|---|---|---|
| HSIOM_PRT16_PORT_SEL0 | 0x40300100 | FULL | Port selection 0 |
| HSIOM_PRT16_PORT_SEL1 | 0x40300104 | FULL | Port selection 1 |

## 17.18 PRT 17

| Register Name | Address | Permission | Description |
|---|---|---|---|
| HSIOM_PRT17_PORT_SEL0 | 0x40300110 | FULL | Port selection 0 |
| HSIOM_PRT17_PORT_SEL1 | 0x40300114 | FULL | Port selection 1 |

## 17.19 PRT 18

| Register Name | Address | Permission | Description |
|---|---|---|---|
| HSIOM_PRT18_PORT_SEL0 | 0x40300120 | FULL | Port selection 0 |
| HSIOM_PRT18_PORT_SEL1 | 0x40300124 | FULL | Port selection 1 |

## 17.20 PRT 19

| Register Name | Address | Permission | Description |
|---|---|---|---|
| HSIOM_PRT19_PORT_SEL0 | 0x40300130 | FULL | Port selection 0 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| HSIOM_PRT19_PORT_SEL1 | 0x40300134 | FULL | Port selection 1<br>Note:IO5_SEL IO6_SEL IO7_SEL are not available for this register |

## 17.21 PRT 20

| Register Name | Address | Permission | Description |
|---|---|---|---|
| HSIOM_PRT20_PORT_SEL0 | 0x40300140 | FULL | Port selection 0 |
| HSIOM_PRT20_PORT_SEL1 | 0x40300144 | FULL | Port selection 1 |

## 17.22 PRT 21

| Register Name | Address | Permission | Description |
|---|---|---|---|
| HSIOM_PRT21_PORT_SEL0 | 0x40300150 | FULL | Port selection 0 |
| HSIOM_PRT21_PORT_SEL1 | 0x40300154 | FULL | Port selection 1 |

## 17.23 PRT 22

| Register Name | Address | Permission | Description |
|---|---|---|---|
| HSIOM_PRT22_PORT_SEL0 | 0x40300160 | FULL | Port selection 0 |
| HSIOM_PRT22_PORT_SEL1 | 0x40300164 | FULL | Port selection 1 |

## 17.24 PRT 23

| Register Name | Address | Permission | Description |
|---|---|---|---|
| HSIOM_PRT23_PORT_SEL0 | 0x40300170 | FULL | Port selection 0 |
| HSIOM_PRT23_PORT_SEL1 | 0x40300174 | FULL | Port selection 1 |

## 17.25 PRT 24

| Register Name | Address | Permission | Description |
|---|---|---|---|
| HSIOM_PRT24_PORT_SEL0 | 0x40300180 | FULL | Port selection 0 |
| HSIOM_PRT24_PORT_SEL1 | 0x40300184 | FULL | Port selection 1<br>Note:IO5_SEL IO6_SEL IO7_SEL are not available for this register |

## 17.26 PRT 25

| Register Name | Address | Permission | Description |
|---|---|---|---|
| HSIOM_PRT25_PORT_SEL0 | 0x40300190 | FULL | Port selection 0 |
| HSIOM_PRT25_PORT_SEL1 | 0x40300194 | FULL | Port selection 1 |

## 17.27 PRT 26

| Register Name | Address | Permission | Description |
|---|---|---|---|
| HSIOM_PRT26_PORT_SEL0 | 0x403001A0 | FULL | Port selection 0 |
| HSIOM_PRT26_PORT_SEL1 | 0x403001A4 | FULL | Port selection 1 |

## 17.28 PRT 27

| Register Name | Address | Permission | Description |
|---|---|---|---|
| HSIOM_PRT27_PORT_SEL0 | 0x403001B0 | FULL | Port selection 0 |
| HSIOM_PRT27_PORT_SEL1 | 0x403001B4 | FULL | Port selection 1 |

## 17.29 PRT 28

| Register Name | Address | Permission | Description |
|---|---|---|---|
| HSIOM_PRT28_PORT_SEL0 | 0x403001C0 | FULL | Port selection 0 |
| HSIOM_PRT28_PORT_SEL1 | 0x403001C4 | FULL | Port selection 1 |

## 17.30 PRT 29

| Register Name | Address | Permission | Description |
|---|---|---|---|
| HSIOM_PRT29_PORT_SEL0 | 0x403001D0 | FULL | Port selection 0 |
| HSIOM_PRT29_PORT_SEL1 | 0x403001D4 | FULL | Port selection 1 |

## 17.31 PRT 30

| Register Name | Address | Permission | Description |
|---|---|---|---|
| HSIOM_PRT30_PORT_SEL0 | 0x403001E0 | FULL | Port selection 0 |

## 17.32 PRT 31

| Register Name | Address | Permission | Description |
|---|---|---|---|
| HSIOM_PRT31_PORT_SEL0 | 0x403001F0 | FULL | Port selection 0<br>Note:IO3_SEL is not available for this register |

## 17.33 PRT 32

| Register Name | Address | Permission | Description |
|---|---|---|---|
| HSIOM_PRT32_PORT_SEL0 | 0x40300200 | FULL | Port selection 0 |
| HSIOM_PRT32_PORT_SEL1 | 0x40300204 | FULL | Port selection 1 |

## 17.34 PRT 33

| Register Name | Address | Permission | Description |
|---|---|---|---|
| HSIOM_PRT33_PORT_SEL0 | 0x40300210 | FULL | Port selection 0 |
| HSIOM_PRT33_PORT_SEL1 | 0x40300214 | FULL | Port selection 1 |

## 17.35 PRT 34

| Register Name | Address | Permission | Description |
|---|---|---|---|
| HSIOM_PRT34_PORT_SEL0 | 0x40300220 | FULL | Port selection 0 |
| HSIOM_PRT34_PORT_SEL1 | 0x40300224 | FULL | Port selection 1 |

## 17.36 Register Details

### 17.36.1 HSIOM_AMUX_SPLIT_CTL

**Description:** AMUX splitter cell control
**Address:** 0x40302000
**Offset:** 0x2000
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register controls the breaking of AMUX buses A and B into multiple segments. It allows for grounding, disconnecting and feeding through. Feeding through is be done straight (from Left segment AMUXBUSA/AMUXBUSB to Right segment AMUXBUSA/AMUXBUSB).
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:7] | SWITCH_BB_S0 [6:6] | SWITCH_BB_SR [5:5] | SWITCH_BB_SL [4:4] | None [3:3] | SWITCH_AA_S0 [2:2] | SWITCH_AA_SR [1:1] | SWITCH_AA_SL [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | SWITCH_AA_SL | RW | R | 0 | T-switch control for Left AMUXBUSA switch:<br>'0': switch open.<br>'1': switch closed. |
| 1 | SWITCH_AA_SR | RW | R | 0 | T-switch control for Right AMUXBUSA switch:<br>'0': switch open.<br>'1': switch closed. |
| 2 | SWITCH_AA_S0 | RW | R | 0 | T-switch control for AMUXBUSA vssa/ground switch:<br>'0': switch open.<br>'1': switch closed. |
| 4 | SWITCH_BB_SL | RW | R | 0 | T-switch control for Left AMUXBUSB switch. |
| 5 | SWITCH_BB_SR | RW | R | 0 | T-switch control for Right AMUXBUSB switch. |
| 6 | SWITCH_BB_S0 | RW | R | 0 | T-switch control for AMUXBUSB vssa/ground switch. |

### 17.36.2 HSIOM_MONITOR_CTL_0

**Description:** Power/Ground Monitor cell control 0
**Address:** 0x40302200
**Offset:** 0x2200
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register controls the connectivity of PWR/GND monitor cells to either AMUX bus A or B respectively.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | MONITOR_EN [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | MONITOR_EN [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | MONITOR_EN [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:26] | | | | | | MONITOR_EN [25:24] | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:25 | MONITOR_EN | RW | R | 0 | control for switch, which connects the power/ground supply to AMUXBUS_A/B respectively when switch is closed:<br>'0': switch open.<br>'1': switch closed. |

### 17.36.3 HSIOM_ALT_JTAG_EN

**Description:** Alternate JTAG IF selection register
**Address:** 0x40302240
**Offset:** 0x2240
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register provides the alternate JTAG interface selection
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | ENABLE [31:31] | None [30:24] | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 31 | ENABLE | RW | R | 0 | Provides the selection for alternate JTAG IF connectivity.<br>0: Primary JTAG interface is selected<br>1: Secondary (alternate) JTAG interface is selected.<br><br>This connectivity works ONLY in ACTIVE mode. |

## 17.36.4 PRT

### 17.36.4.1 HSIOM_PRT_PORT_SEL0

**Description:** Port selection 0
**Address:** 0x40300000
**Offset:** 0x0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** The High Speed IO Mux (HSIOM) selects the hardware peripheral connection to an IO pin. The default setting of 'GPIO' leaves the pin under CPU control through firmware. Pin specific connections for the 'DS_x' and 'ACT_x' settings are listed in the pinout section of the device datasheet.
Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the peripheral and HSIOM is properly configured (HSIOM_PRT_SELx) before turning the IO on (GPIO_PRT_CFG.DRIVE_MODEx) to avoid producing glitches on the bus.
Note: peripherals other than GPIO & UDB/DSI directly control both the output and output-enable of the output buffer (peripherals can drive strong 0 or strong 1 in any mode except OFF='0').
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:5] | | | IO0_SEL [4:0] | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:13] | | | IO1_SEL [12:8] | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:21] | | | IO2_SEL [20:16] | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:29] | | | IO3_SEL [28:24] | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:4 | IO0_SEL | RW | RW | 0 | Selects the peripheral connections of Pin 0. Note that available connectivity options vary depending on the device, port and the pin. See the device Datasheet for a list of peripheral connections available at each pin. |
| | GPIO | | | 0 | GPIO controls 'out' |
| | GPIO_DSI | | | 1 | GPIO controls 'out', DSI controls 'output enable' |
| | DSI_DSI | | | 2 | DSI controls 'out' and 'output enable' |
| | DSI_GPIO | | | 3 | DSI controls 'out', GPIO controls 'output enable' |
| | AMUXA | | | 4 | AMUXBUS A |
| | AMUXB | | | 5 | AMUXBUS B |
| | AMUXA_DSI | | | 6 | Analog mux bus A, DSI control |
| | AMUXB_DSI | | | 7 | Analog mux bus B, DSI control |
| | ACT_0 | | | 8 | Active peripheral 0 |
| | ACT_1 | | | 9 | Active peripheral 1 |
| | ACT_2 | | | 10 | Active peripheral 2 |
| | ACT_3 | | | 11 | Active peripheral 3 |
| | DS_0 | | | 12 | Deep Sleep peripheral 0 |
| | DS_1 | | | 13 | Deep Sleep peripheral 1 |
| | DS_2 | | | 14 | Deep Sleep peripheral 2 |
| | DS_3 | | | 15 | Deep Sleep peripheral 3 |
| | ACT_4 | | | 16 | Active peripheral 4 |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| | ACT_5 | | | 17 | Active peripheral 5 |
| | ACT_6 | | | 18 | Active peripheral 6 |
| | ACT_7 | | | 19 | Active peripheral 7 |
| | ACT_8 | | | 20 | Active peripheral 8 |
| | ACT_9 | | | 21 | Active peripheral 9 |
| | ACT_10 | | | 22 | Active peripheral 10 |
| | ACT_11 | | | 23 | Active peripheral 11 |
| | ACT_12 | | | 24 | Active peripheral 12 |
| | ACT_13 | | | 25 | Active peripheral 13 |
| | ACT_14 | | | 26 | Active peripheral 14 |
| | ACT_15 | | | 27 | Active peripheral 15 |
| | DS_4 | | | 28 | Deep Sleep peripheral 4 |
| | DS_5 | | | 29 | Deep Sleep peripheral 5 |
| | DS_6 | | | 30 | Deep Sleep peripheral 6 |
| | DS_7 | | | 31 | Deep Sleep peripheral 7 |
| 8:12 | IO1_SEL | RW | RW | 0 | Selects the peripheral connections of Pin 1. |
| 16:20 | IO2_SEL | RW | RW | 0 | Selects the peripheral connections of Pin 2. |
| 24:28 | IO3_SEL | RW | RW | 0 | Selects the peripheral connections of Pin 3. |

### 17.36.4.2 HSIOM_PRT_PORT_SEL1

**Description:** Port selection 1
**Address:** 0x40300004
**Offset:** 0x4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** See PORT_SEL0 for details
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:5] | | | IO4_SEL [4:0] | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:13] | | | IO5_SEL [12:8] | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:21] | | | IO6_SEL [20:16] | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:29] | | | IO7_SEL [28:24] | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:4 | IO4_SEL | RW | RW | 0 | Selects the peripheral connections of Pin 4. See PORT_SEL0 for connection details. |
| 8:12 | IO5_SEL | RW | RW | 0 | Selects the peripheral connections of Pin 4. |
| 16:20 | IO6_SEL | RW | RW | 0 | Selects the peripheral connections of Pin 5. |
| 24:28 | IO7_SEL | RW | RW | 0 | Selects the peripheral connections of Pin 6. |

# 18 I2S

## 18.1 I2S 0

**Description** I2S registers
**Base Address** 0x40800000
**Size** 0x1000
**Slave Num** MMIO8 - 0

| Register Name | Address | Permission | Description |
|---|---|---|---|
| I2S0_CTL | 0x40800000 | FULL | Control |
| I2S0_CLOCK_CTL | 0x40800010 | FULL | Clock control |
| I2S0_CLOCK_STAT | 0x40800014 | FULL | Clock Status |
| I2S0_CMD | 0x40800020 | FULL | Command |
| I2S0_TR_CTL | 0x40800040 | FULL | Trigger control |
| I2S0_TX_CTL | 0x40800080 | FULL | Transmitter control |
| I2S0_TX_WATCHDOG | 0x40800084 | FULL | Transmitter watchdog |
| I2S0_RX_CTL | 0x408000A0 | FULL | Receiver control |
| I2S0_RX_WATCHDOG | 0x408000A4 | FULL | Receiver watchdog |
| I2S0_TX_FIFO_CTL | 0x40800200 | FULL | TX FIFO control |
| I2S0_TX_FIFO_STATUS | 0x40800204 | FULL | TX FIFO status |
| I2S0_TX_FIFO_WR | 0x40800208 | FULL | TX FIFO write |
| I2S0_RX_FIFO_CTL | 0x40800300 | FULL | RX FIFO control |
| I2S0_RX_FIFO_STATUS | 0x40800304 | FULL | RX FIFO status |
| I2S0_RX_FIFO_RD | 0x40800308 | FULL | RX FIFO read |
| I2S0_RX_FIFO_RD_SILENT | 0x4080030C | FULL | RX FIFO silent read |
| I2S0_INTR | 0x40800F00 | FULL | Interrupt register |
| I2S0_INTR_SET | 0x40800F04 | FULL | Interrupt set register |
| I2S0_INTR_MASK | 0x40800F08 | FULL | Interrupt mask register |
| I2S0_INTR_MASKED | 0x40800F0C | FULL | Interrupt masked register |

## 18.2 I2S 1

**Description** I2S registers
**Base Address** 0x40801000
**Size** 0x1000
**Slave Num** MMIO8 - 1

| Register Name | Address | Permission | Description |
|---|---|---|---|
| I2S1_CTL | 0x40801000 | FULL | Control |
| I2S1_CLOCK_CTL | 0x40801010 | FULL | Clock control |
| I2S1_CLOCK_STAT | 0x40801014 | FULL | Clock Status |
| I2S1_CMD | 0x40801020 | FULL | Command |
| I2S1_TR_CTL | 0x40801040 | FULL | Trigger control |
| I2S1_TX_CTL | 0x40801080 | FULL | Transmitter control |
| I2S1_TX_WATCHDOG | 0x40801084 | FULL | Transmitter watchdog |
| I2S1_RX_CTL | 0x408010A0 | FULL | Receiver control |
| I2S1_RX_WATCHDOG | 0x408010A4 | FULL | Receiver watchdog |
| I2S1_TX_FIFO_CTL | 0x40801200 | FULL | TX FIFO control |
| I2S1_TX_FIFO_STATUS | 0x40801204 | FULL | TX FIFO status |
| I2S1_TX_FIFO_WR | 0x40801208 | FULL | TX FIFO write |
| I2S1_RX_FIFO_CTL | 0x40801300 | FULL | RX FIFO control |
| I2S1_RX_FIFO_STATUS | 0x40801304 | FULL | RX FIFO status |
| I2S1_RX_FIFO_RD | 0x40801308 | FULL | RX FIFO read |
| I2S1_RX_FIFO_RD_SILENT | 0x4080130C | FULL | RX FIFO silent read |
| I2S1_INTR | 0x40801F00 | FULL | Interrupt register |
| I2S1_INTR_SET | 0x40801F04 | FULL | Interrupt set register |
| I2S1_INTR_MASK | 0x40801F08 | FULL | Interrupt mask register |
| I2S1_INTR_MASKED | 0x40801F0C | FULL | Interrupt masked register |

## 18.3 I2S 2

**Description** I2S registers
**Base Address** 0x40802000

**Size** 0x1000
**Slave Num** MMIO8 - 2

| Register Name | Address | Permission | Description |
|---|---|---|---|
| I2S2_CTL | 0x40802000 | FULL | Control |
| I2S2_CLOCK_CTL | 0x40802010 | FULL | Clock control |
| I2S2_CLOCK_STAT | 0x40802014 | FULL | Clock Status |
| I2S2_CMD | 0x40802020 | FULL | Command |
| I2S2_TR_CTL | 0x40802040 | FULL | Trigger control |
| I2S2_TX_CTL | 0x40802080 | FULL | Transmitter control |
| I2S2_TX_WATCHDOG | 0x40802084 | FULL | Transmitter watchdog |
| I2S2_RX_CTL | 0x408020A0 | FULL | Receiver control |
| I2S2_RX_WATCHDOG | 0x408020A4 | FULL | Receiver watchdog |
| I2S2_TX_FIFO_CTL | 0x40802200 | FULL | TX FIFO control |
| I2S2_TX_FIFO_STATUS | 0x40802204 | FULL | TX FIFO status |
| I2S2_TX_FIFO_WR | 0x40802208 | FULL | TX FIFO write |
| I2S2_RX_FIFO_CTL | 0x40802300 | FULL | RX FIFO control |
| I2S2_RX_FIFO_STATUS | 0x40802304 | FULL | RX FIFO status |
| I2S2_RX_FIFO_RD | 0x40802308 | FULL | RX FIFO read |
| I2S2_RX_FIFO_RD_SILENT | 0x4080230C | FULL | RX FIFO silent read |
| I2S2_INTR | 0x40802F00 | FULL | Interrupt register |
| I2S2_INTR_SET | 0x40802F04 | FULL | Interrupt set register |
| I2S2_INTR_MASK | 0x40802F08 | FULL | Interrupt mask register |
| I2S2_INTR_MASKED | 0x40802F0C | FULL | Interrupt masked register |

## 18.4 Register Details

### 18.4.1 I2S_CTL

**Description:** Control
**Address:** 0x40800000
**Offset:** 0x0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register is used to control I2S block.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | RX_ENABLED [31:31] | TX_ENABLED [30:30] | None [29:24] | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 30 | TX_ENABLED | RW | R | 0 | Enables the I2S TX component:<br>'0': Disabled.<br>'1': Enabled. |
| 31 | RX_ENABLED | RW | R | 0 | Enables the I2S RX component:<br>'0': Disabled.<br>'1': Enabled. |

### 18.4.2 I2S_CLOCK_CTL

**Description:** Clock control
**Address:** 0x40800010
**Offset:** 0x10
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register can configure frequencies for I2S block and master clock. This register should NOT be changed during communication.
**Default:** 0x3000

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:6] | | CLOCK_DIV [5:0] | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:14] | | MCLK_DIV [13:12] | | None [11:9] | | | CLOCK _SEL [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:17] | | | | | | | MCLK_EN [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:5 | CLOCK_DIV | RW | R | 0 | Frequency divisor for generating I2S clock frequency. The selected clock with CLOCK_SEL is divided by this.<br>'0': Bypass<br>'1': 2 x<br>'2': 3 x<br>'3': 4 x<br>...<br>'62': 63 x<br>'63': 64 x |
| 8 | CLOCK_SEL | RW | R | 0 | Selects clock to be used by I2S:<br>'0': Internal clock ('clk_audio_i2s')<br>'1': External clock ('clk_i2s_if') |
| 12:13 | MCLK_DIV | RW | R | 3 | Selects clock divider for MCLK_OUT. CTL.TX_ENABLED=1 or CTL.RX_ENABLED=1 and and CLOCK_CTL.CLOCK_SEL=0 to enable the clock. |
| | DIV1 | | | 0 | Divide clk_audio_i2s by 1 (Bypass) |
| | DIV2 | | | 1 | Divide clk_audio_i2s by 2 |
| | DIV4 | | | 2 | Divide clk_audio_i2s by 4 |
| | DIV8 | | | 3 | Divide clk-audio_i2s by 8 |
| 16 | MCLK_EN | RW | R | 0 | Enable MCLK - enables MCLK divider operation Upon assertion allows MCLK Divider to begin operation.<br>Upon de-assertion, i.e. 1-0 transition, allows MCLK divider to reach the all 0s state (reset state) then freezes the divider. This permits a controlled power-on/power-off sequence that may be used prior to going to DeepSleep/IP Disable and avoids glitching the MCLK. |

### 18.4.3 I2S_CLOCK_STAT

**Description:** Clock Status
**Address:** 0x40800014
**Offset:** 0x14
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** This register indicates the status of the MCLK Divider and is used to allow a controlled shutdown of the clock.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:1] | | | | | | | MCLK_DIV_OFF [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | MCLK_DIV_OFF | R | RW | 0 | MCLK Divider OFF<br>0: Indicates MCLK Divider not a reset state<br>1: Indicates MCLK Divider at reset state. This is ONLY set when IP is enabled (CTL.RX_ENABLED=1 or CTL.TX_ENABLED=1), CLOCK_CTL.MCLK_EN=0, and MCLK_DIV reaches it's reset state.<br><br>The intent is that this bit indicates successful shutdown of the MCLK_DIVIDER after CLOCK_CTL.MCLK_EN transitions from 1 to 0. |

### 18.4.4 I2S_CMD

**Description:** Command
**Address:** 0x40800020
**Offset:** 0x20
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** This register can control I2S functions.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:1] | | | | | | | TX_START [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:9] | | | | | | | TX_PAUSE [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:17] | | | | | | | RX_START [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | TX_START | RW | R | 0 | Transmitter enable:<br>'0': Disabled.<br>'1': Enabled. |
| 8 | TX_PAUSE | RW | R | 0 | Pause enable:<br>'0': Disabled (TX FIFO data is sent over I2S).<br>'1': Enabled ('0' data is sent over I2S, instead of TX FIFO data). |
| 16 | RX_START | RW | R | 0 | Receiver enable:<br>'0': Disabled.<br>'1': Enabled. |

### 18.4.5 I2S_TR_CTL

**Description:** Trigger control
**Address:** 0x40800040
**Offset:** 0x40
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register can enable DMA for I2S. This register should NOT be changed during communication.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:1] | | | | | | | TX_REQ_EN [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:17] | | | | | | | RX_REQ_EN [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | TX_REQ_EN | RW | R | 0 | Trigger output ('tr_i2s_tx_req') enable for requests of DMA transfer in transmission<br>'0': Disabled.<br>'1': Enabled. |
| 16 | RX_REQ_EN | RW | R | 0 | Trigger output ('tr_i2s_rx_req') enable for requests of DMA transfer in reception<br>'0': Disabled.<br>'1': Enabled. |

### 18.4.6 I2S_TX_CTL

**Description:** Transmitter control
**Address:** 0x40800080
**Offset:** 0x80
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register can configure transmitter for I2S functions. This register should NOT be changed during communication.
**Default:** 0x440510

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | MS [7:7] | CH_NR [6:4] | | | B_CLOCK_INV [3:3] | None [2:0] | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:14] | | WD_EN [13:13] | OVHDATA [12:12] | None [11:11] | WS_PULSE [10:10] | I2S_MODE [9:8] | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:23] | WORD_LEN [22:20] | | | None [19:19] | CH_LEN [18:16] | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:26] | | | | | | SCKI_POL [25:25] | SCKO_POL [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 3 | B_CLOCK_INV | RW | R | 0 | Serial data transmission is advanced by 0.5 SCK cycles. This bit is valid only in TX slave mode. When set to '1', the serial data will be transmitted 0.5 SCK cycles earlier than when set to '0'.<br><br>1) TX_CTL.SCKI_POL=0 and TX_CTL.B_CLOCK_INV=0: Serial data will be transmitted off the SCK falling edge<br>2) TX_CTL.SCKI_POL=0 and TX_CTL.B_CLOCK_INV=1: Serial data will be transmitted off the SCK rising edge that is 0.5 SCK cycles before the SCK falling edge in 1)<br>3) TX_CTL.SCKI_POL=1 and TX_CTL.B_CLOCK_INV=0: Serial data will be transmitted off the SCK rising edge<br>4) TX_CTL.SCKI_POL=1 and TX_CTL.B_CLOCK_INV=1: Serial data will be transmitted off the SCK falling edge that is 0.5 SCK cycles before the SCK rising edge in 3)<br><br>(Note that this is only the appearance w.r.t. SCK edge, the actual timing is generated by an internal clock that runs 8x the SCK frequency). The word sync (TX_WS) signal is not affected by this bit setting.<br>Note: When Master mode, must be '0'. |
| | FALLING_EDGE_TX | | | 0 | SDO transmitted at SCK falling edge when TX_CTL.SCKI_POL=0 |
| | RISING_EDGE_TX | | | 1 | SDO transmitted at SCK rising edge when TX_CTL.SCKI_POL=0 |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 4:6 | CH_NR | RW | R | 1 | Specifies number of channels per frame:<br><br>Note: only '2channels' is supported during Left Justfied or I2S mode. Hence software must set '1' to this field in the modes. |
| | CH_NUM1 | | | 0 | 1 channel |
| | CH_NUM2 | | | 1 | 2 channels |
| | CH_NUM3 | | | 2 | 3 channels |
| | CH_NUM4 | | | 3 | 4 channels |
| | CH_NUM5 | | | 4 | 5 channels |
| | CH_NUM6 | | | 5 | 6 channels |
| | CH_NUM7 | | | 6 | 7 channels |
| | CH_NUM8 | | | 7 | 8 channels |
| 7 | MS | RW | R | 0 | Set interface in master or slave mode: |
| | SLAVE | | | 0 | Slave |
| | MASTER | | | 1 | Master |
| 8:9 | I2S_MODE | RW | R | 1 | Select I2S, left-justified or TDM: |
| | LEFT_JUSTIFIED | | | 0 | Left Justified |
| | I2S | | | 1 | I2S mode |
| | TDM_A | | | 2 | TDM mode A, the 1st Channel align to WSO Rising Edge |
| | TDM_B | | | 3 | TDM mode B, the 1st Channel align to WSO Rising edge with1 SCK Delay |
| 10 | WS_PULSE | RW | R | 1 | Set WS pulse width in TDM mode:<br><br>Note: When not TDM mode, must be '1'. |
| | SCK_PERIOD | | | 0 | Pulse width is 1 SCK period |
| | CH_LENGTH | | | 1 | Pulse width is 1 channel length |
| 12 | OVHDATA | RW | R | 0 | Set overhead value:<br>'0': Set to '0'<br>'1': Set to '1' |
| 13 | WD_EN | RW | R | 0 | Set watchdog for 'tx_ws_in':<br>'0': Disabled.<br>'1': Enabled. |
| 16:18 | CH_LEN | RW | R | 4 | Channel length in number of bits:<br><br>Note:<br>- When this field is configured to '6' or '7', the length is set to 32-bit (same as '5').<br>- When TDM mode, must be 32-bit length to this field. |
| | BIT_LEN8 | | | 0 | 8-bit |
| | BIT_LEN16 | | | 1 | 16-bit |
| | BIT_LEN18 | | | 2 | 18-bit |
| | BIT_LEN20 | | | 3 | 20-bit |
| | BIT_LEN24 | | | 4 | 24-bit |
| | BIT_LEN32 | | | 5 | 32-bit |
| 20:22 | WORD_LEN | RW | R | 4 | Word length in number of bits:<br><br>Note:<br>- When this field is configured to '6' or '7', the length is set to 32-bit (same as '5').<br>- Don't configure this field as beyond Channel length. |
| | BIT_LEN8 | | | 0 | 8-bit |
| | BIT_LEN16 | | | 1 | 16-bit |
| | BIT_LEN18 | | | 2 | 18-bit |
| | BIT_LEN20 | | | 3 | 20-bit |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| | BIT_LEN24 | | | 4 | 24-bit |
| | BIT_LEN32 | | | 5 | 32-bit |
| 24 | SCKO_POL | RW | R | 0 | TX master bit clock polarity.<br>When this bit is 1, the outgoing tx_sck signal is inverted after it has been transmitted from the I2S transceiver core. This bit does not affect the internal serial data transmission timing. The word sync (TX_WS) signal is not affected by this bit setting.<br>'0': When transmitter is in master mode, serial data is transmitted from the falling bit clock edge<br>'1': When transmitter is in master mode, serial data is transmitted from the rising bit clock edge |
| 25 | SCKI_POL | RW | R | 0 | TX slave bit clock polarity.<br>When this bit is 1, the incoming tx_sck signal is inverted before it is received by the I2S transceiver core. This bit does not affect the internal serial data transmission timing. The word sync (TX_WS) signal is not affected by this bit setting. See TX_CTL.B_CLOCK_INV for more details. |

### 18.4.7 I2S_TX_WATCHDOG

**Description:** Transmitter watchdog
**Address:** 0x40800084
**Offset:** 0x84
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register can configure counter value for the Tx watchdog. This register should NOT be changed during the operation.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | WD_COUNTER [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | WD_COUNTER [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | WD_COUNTER [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | WD_COUNTER [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | WD_COUNTER | RW | R | 0 | Start value of the TX watchdog. With the reset value of 0x0000:0000 the counter is disabled. This is clocked by the AHB-Lite system clock 'clk_sys'. |

### 18.4.8 I2S_RX_CTL

**Description:** Receiver control
**Address:** 0x408000A0
**Offset:** 0xA0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register should NOT be changed during communication.
**Default:** 0x440510

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | MS [7:7] | CH_NR [6:4] | | | B_CLOCK_INV [3:3] | None [2:0] | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:14] | | WD_EN [13:13] | None [12:11] | | WS_PULSE [10:10] | I2S_MODE [9:8] | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | BIT_EXTENSION [23:23] | WORD_LEN [22:20] | | | None [19:19] | CH_LEN [18:16] | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:26] | | | | | | SCKI_POL [25:25] | SCKO_POL [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 3 | B_CLOCK_INV | RW | R | 0 | Serial data capture is delayed by 0.5 SCK cycles. This bit is valid only in RX master mode.<br>When set to '1', the serial data will be captured 0.5 SCK cycles later than when set to '0'.<br><br>1) RX_CTL.SCKO_POL=0 and RX_CTL.B_CLOCK_INV=0: Serial data will be captured by the SCK rising edge<br>2) RX_CTL.SCKO_POL=0 and RX_CTL.B_CLOCK_INV=1: Serial data will be captured by the SCK falling edge that is 0.5 SCK cycles after the SCK rising edge in 1)<br>3) RX_CTL.SCKO_POL=1 and RX_CTL.B_CLOCK_INV=0: Serial data will be captured by the SCK falling edge<br>4) RX_CTL.SCKO_POL=1 and RX_CTL.B_CLOCK_INV=1: Serial data will be captured by the SCK rising edge that is 0.5 SCK cycles after the SCK falling edge in 3)<br><br>(Note that this is only the appearance w.r.t. SCK edge, the actual capture timing is derived from an internal clock that runs 8x the SCK frequency). The word sync (RX_WS) signal is not affected by this bit setting.<br>Note: When Slave mode, must be '0'. |
| | RISING_EDGE_RX | | | 0 | SDI received at SCK rising edge when RX_CTL.SCKO_POL=0 |
| | FALLING_EDGE_RX | | | 1 | SDI received at SCK falling edge when RX_CTL.SCKO_POL=0 |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 4:6 | CH_NR | RW | R | 1 | Specifies number of channels per frame:<br><br>Note: only '2channels' is supported during Left Justfied or I2S mode. Hence software must set '1' to this field in the modes. |
| | CH_NUM1 | | | 0 | 1 channel |
| | CH_NUM2 | | | 1 | 2 channels |
| | CH_NUM3 | | | 2 | 3 channels |
| | CH_NUM4 | | | 3 | 4 channels |
| | CH_NUM5 | | | 4 | 5 channels |
| | CH_NUM6 | | | 5 | 6 channels |
| | CH_NUM7 | | | 6 | 7 channels |
| | CH_NUM8 | | | 7 | 8 channels |
| 7 | MS | RW | R | 0 | Set interface in master or slave mode: |
| | SLAVE | | | 0 | Slave |
| | MASTER | | | 1 | Master |
| 8:9 | I2S_MODE | RW | R | 1 | Select I2S, left-justified or TDM: |
| | LEFT_JUSTIFIED | | | 0 | Left Justified |
| | I2S | | | 1 | I2S mode |
| | TDM_A | | | 2 | TDM mode A, the 1st Channel align to WSO Rising Edge |
| | TDM_B | | | 3 | TDM mode B, the 1st Channel align to WSO Rising edge with1 SCK Delay |
| 10 | WS_PULSE | RW | R | 1 | Set WS pulse width in TDM mode:<br>Note: When not TDM mode, must be '1'. |
| | SCK_PERIOD | | | 0 | Pulse width is 1 SCK period |
| | CH_LENGTH | | | 1 | Pulse width is 1 channel length |
| 13 | WD_EN | RW | R | 0 | Set watchdog for 'rx_ws_in'<br>'0': Disabled.<br>'1': Enabled. |
| 16:18 | CH_LEN | RW | R | 4 | Channel length in number of bits:<br><br>Note:<br>- When this field is configured to '6' or '7', the length is set to 32-bit (same as '5').<br>- When TDM mode, must be 32-bit length to this field. |
| | BIT_LEN8 | | | 0 | 8-bit |
| | BIT_LEN16 | | | 1 | 16-bit |
| | BIT_LEN18 | | | 2 | 18-bit |
| | BIT_LEN20 | | | 3 | 20-bit |
| | BIT_LEN24 | | | 4 | 24-bit |
| | BIT_LEN32 | | | 5 | 32-bit |
| 20:22 | WORD_LEN | RW | R | 4 | Word length in number of bits:<br><br>Note:<br>- When this field is configured to '6' or '7', the length is set to 32-bit (same as '5').<br>- Don't configure this field as beyond Channel length. |
| | BIT_LEN8 | | | 0 | 8-bit |
| | BIT_LEN16 | | | 1 | 16-bit |
| | BIT_LEN18 | | | 2 | 18-bit |
| | BIT_LEN20 | | | 3 | 20-bit |
| | BIT_LEN24 | | | 4 | 24-bit |
| | BIT_LEN32 | | | 5 | 32-bit |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 23 | BIT_EXTENSION | RW | R | 0 | When reception word length is shorter than the word length of RX_FIFO_RD, extension mode of upper bit should be set.<br>'0': Extended by '0'<br>'1': Extended by sign bit (if MSB word is '1', then it is extended by '1', if MSB is '0' then it is extended by '0') |
| 24 | SCKO_POL | RW | R | 0 | RX master bit clock polarity.<br>When this bit is 1, the outgoing rx_sck signal is inverted after it has been transmitted from the I2S receiver core. This bit does not affect the internal serial data capture timing. The word sync (RX_WS) signal is not affected by this bit setting.See RX_CTL.B_CLOCK_INV for more details. |
| 25 | SCKI_POL | RW | R | 0 | RX slave bit clock polarity.<br>When this bit is 1, the incoming rx_sck signal is inverted before it is received by the I2S receiver core. This bit does not affect the internal serial data capture timing. The word sync (RX_WS) signal is not affected by this bit setting.<br>'0': When receiver is in slave mode, serial data is sampled on the rising bit clock edge<br>'1': When receiver is in slave mode, serial data is sampled on the falling bit clock edge |

### 18.4.9 I2S_RX_WATCHDOG

**Description:** Receiver watchdog
**Address:** 0x408000A4
**Offset:** 0xA4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register should NOT be changed during the operation.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | WD_COUNTER [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | WD_COUNTER [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | WD_COUNTER [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | WD_COUNTER [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | WD_COUNTER | RW | R | 0 | Start value of the RX watchdog. With the reset value of 0x0000:0000 the counter is disabled. This is clocked by the AHB-Lite system clock 'clk_sys'. |

### 18.4.10 I2S_TX_FIFO_CTL

**Description:** TX FIFO control
**Address:** 0x40800200
**Offset:** 0x200
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** This register can configure FIFO for I2S .
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | TRIGGER_LEVEL [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:18] | | | | | | FREEZE [17:17] | CLEAR [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | TRIGGER_LEVEL | RW | R | 0 | Trigger level. When the TX FIFO has less entries than the number of this field, a transmitter trigger event is generated. |
| 16 | CLEAR | RW | R | 0 | When '1', the TX FIFO and TX_BUF are cleared/invalidated. Invalidation will last for as long as this field is '1'. If a quick clear/invalidation is required, the field should be set to '1' and be followed by a set to '0'. If a clear/invalidation is required for an extended time period, the field should be set to '1' during the complete time period. |
| 17 | FREEZE | RW | R | 0 | When '1', hardware reads from the TX FIFO do not remove FIFO entries. Freeze will not advance the TX FIFO read pointer. This field is used only for debugging purposes. |

### 18.4.11 I2S_TX_FIFO_STATUS

**Description:** TX FIFO status
**Address:** 0x40800204
**Offset:** 0x204
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** This register displays the statuses of FIFO for I2S.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | USED [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:9] | | | | | | | USED [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | RD_PTR [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | WR_PTR [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:8 | USED | R | W | 0 | Number of entries in the TX FIFO. The field value is in the range [0, 256]. |
| 16:23 | RD_PTR | R | W | 0 | TX FIFO read pointer: FIFO location from which a data frame is read by the hardware.This field is used only for debugging purposes. |
| 24:31 | WR_PTR | R | W | 0 | TX FIFO write pointer: FIFO location at which a new data frame is written by the host. This field is used only for debugging purposes. |

### 18.4.12 I2S_TX_FIFO_WR

**Description:** TX FIFO write
**Address:** 0x40800208
**Offset:** 0x208
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** This register stores transmission data for I2S transfer.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | DATA | W | R | 0 | Data written into the TX FIFO. Behavior is similar to that of a PUSH operation.<br>Note: Don't access to this register while TX_FIFO_CTL.CLEAR is '1'. |

### 18.4.13 I2S_RX_FIFO_CTL

**Description:** RX FIFO control
**Address:** 0x40800300
**Offset:** 0x300
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | TRIGGER_LEVEL [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:18] | | | | | | FREEZE [17:17] | CLEAR [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | TRIGGER_LEVEL | RW | R | 0 | Trigger level. When the RX FIFO has more entries than the number of this field, a receiver trigger event is generated.<br>Note: software can configure up to 253 in I2S mode or Left Justified (RX_CTL.I2S_MODE = '0' or '1'). In TDM mode (RX_CTL.I2S_MODE = '2' or '3'), it can configure up to [256 - (RX_CTL.CH_NR+2)]. |
| 16 | CLEAR | RW | R | 0 | When '1', the RX FIFO and RX_BUF are cleared/invalidated. Invalidation will last for as long as this field is '1'. If a quick clear/invalidation is required, the field should be set to '1' and be followed by a set to '0'. If a clear/invalidation is required for an extended time period, the field should be set to '1' during the complete time period. |
| 17 | FREEZE | RW | R | 0 | When '1', hardware writes to the RX FIFO have no effect. Freeze will not advance the RX FIFO write pointer. This field is used only for debugging purposee. |

### 18.4.14 I2S_RX_FIFO_STATUS

**Description:** RX FIFO status
**Address:** 0x40800304
**Offset:** 0x304
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | USED [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:9] | | | | | | | USED [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | RD_PTR [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | WR_PTR [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:8 | USED | R | W | 0 | Number of entries in the RX FIFO. The field value is in the range [0, 256]. |
| 16:23 | RD_PTR | R | W | 0 | RX FIFO read pointer: FIFO location from which a data frame is read by the host. This field is used only for debugging purposes. |
| 24:31 | WR_PTR | R | W | 0 | RX FIFO write pointer: FIFO location at which a new data frame is written by the hardware. This field is used only for debugging purposes. |

### 18.4.15 I2S_RX_FIFO_RD

**Description:** RX FIFO read
**Address:** 0x40800308
**Offset:** 0x308
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** When the IP is disabled (CTRL.RX_ENABLED is '0'), a read from this register returns 0xffff:ffff.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | DATA | R | W | 0 | Data read from the RX FIFO. Reading a data frame will remove the data frame from the RX FIFO; i.e. behavior is similar to that of a POP operation.<br>Notes:<br>- Don't access to this register while RX_FIFO_CTL.CLEAR is '1'.<br>- Two stored data may be not valid after CMD.RX_START is set '1'. Therefore we recommend software discard those data. |

### 18.4.16 I2S_RX_FIFO_RD_SILENT

**Description:** RX FIFO silent read
**Address:** 0x4080030C
**Offset:** 0x30C
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** This register stores received data for I2S transfer. When the IP is disabled (CTRL.RX_ENABLED is '0'), a read from this register returns 0xffff:ffff.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | DATA | R | W | 0 | Data read from the RX FIFO. Reading a data frame will NOT remove the data frame from the RX FIFO; i.e. behavior is similar to that of a PEEK operation. This field is used only for debugging purposes.<br>Notes:<br>- Don't access to this register while RX_FIFO_CTL.CLEAR is '1'.<br>- Two stored data may be not valid after CMD.RX_START is set '1'. Therefore we recommend software discard those data. |

### 18.4.17 I2S_INTR

**Description:** Interrupt register
**Address:** 0x40800F00
**Offset:** 0xF00
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** This register displays the interrupt status.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:7] | TX_UNDERFLOW [6:6] | TX_OVERFLOW [5:5] | TX_EMPTY [4:4] | None [3:2] | | TX_NOT_FULL [1:1] | TX_TRIGGER [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:9] | | | | | | | TX_WD [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:23] | RX_UNDERFLOW [22:22] | RX_OVERFLOW [21:21] | None [20:20] | RX_FULL [19:19] | RX_NOT_EMPTY [18:18] | None [17:17] | RX_TRIGGER [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:25] | | | | | | | RX_WD [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | TX_TRIGGER | RW1C | RW1S | 0 | Less entries in the TX FIFO than the value specified by TRIGGER_LEVEL in TX_FIFO_CTRL. |
| 1 | TX_NOT_FULL | RW1C | RW1S | 0 | TX FIFO is not full. |
| 4 | TX_EMPTY | RW1C | RW1S | 0 | TX FIFO is empty; i.e. it has 0 entries. |
| 5 | TX_OVERFLOW | RW1C | RW1S | 0 | Attempt to write to a full TX FIFO. |
| 6 | TX_UNDERFLOW | RW1C | RW1S | 0 | Attempt to read from an empty TX FIFO. This happens when the IP is ready to transfer data and TX_EMPTY is '1'. |
| 8 | TX_WD | RW1C | RW1S | 0 | Triggers (sets to '1') when the Tx watchdog event occurs. |
| 16 | RX_TRIGGER | RW1C | RW1S | 0 | More entries in the RX FIFO than the value specified by TRIGGER_LEVEL in RX_FIFO_CTRL. |
| 18 | RX_NOT_EMPTY | RW1C | RW1S | 0 | RX FIFO is not empty. |
| 19 | RX_FULL | RW1C | RW1S | 0 | RX FIFO is full. |
| 21 | RX_OVERFLOW | RW1C | RW1S | 0 | Attempt to write to a full RX FIFO. |
| 22 | RX_UNDERFLOW | RW1C | RW1S | 0 | Attempt to read from an empty RX FIFO. |
| 24 | RX_WD | RW1C | RW1S | 0 | Triggers (sets to '1') when the Rx watchdog event occurs. |

### 18.4.18 I2S_INTR_SET

**Description:** Interrupt set register
**Address:** 0x40800F04
**Offset:** 0xF04
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:7] | TX_UNDERFLOW [6:6] | TX_OVERFLOW [5:5] | TX_EMPTY [4:4] | None [3:2] | | TX_NOT_FULL [1:1] | TX_TRIGGER [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:9] | | | | | | | TX_WD [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:23] | RX_UNDERFLOW [22:22] | RX_OVERFLOW [21:21] | None [20:20] | RX_FULL [19:19] | RX_NOT_EMPTY [18:18] | None [17:17] | RX_TRIGGER [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:25] | | | | | | | RX_WD [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | TX_TRIGGER | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt request register. |
| 1 | TX_NOT_FULL | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt request register. |
| 4 | TX_EMPTY | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt request register. |
| 5 | TX_OVERFLOW | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt request register. |
| 6 | TX_UNDERFLOW | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt request register. |
| 8 | TX_WD | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt request register. |
| 16 | RX_TRIGGER | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt request register. |
| 18 | RX_NOT_EMPTY | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt request register. |
| 19 | RX_FULL | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt request register. |
| 21 | RX_OVERFLOW | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt request register. |
| 22 | RX_UNDERFLOW | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt request register. |
| 24 | RX_WD | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt request register. |

### 18.4.19 I2S_INTR_MASK

**Description:** Interrupt mask register
**Address:** 0x40800F08
**Offset:** 0xF08
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:7] | TX_UNDERFLOW [6:6] | TX_OVERFLOW [5:5] | TX_EMPTY [4:4] | None [3:2] | | TX_NOT_FULL [1:1] | TX_TRIGGER [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:9] | | | | | | | TX_WD [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:23] | RX_UNDERFLOW [22:22] | RX_OVERFLOW [21:21] | None [20:20] | RX_FULL [19:19] | RX_NOT_EMPTY [18:18] | None [17:17] | RX_TRIGGER [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:25] | | | | | | | RX_WD [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | TX_TRIGGER | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |
| 1 | TX_NOT_FULL | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |
| 4 | TX_EMPTY | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |
| 5 | TX_OVERFLOW | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |
| 6 | TX_UNDERFLOW | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |
| 8 | TX_WD | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |
| 16 | RX_TRIGGER | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |
| 18 | RX_NOT_EMPTY | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |
| 19 | RX_FULL | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |
| 21 | RX_OVERFLOW | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |
| 22 | RX_UNDERFLOW | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |
| 24 | RX_WD | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |

### 18.4.20 I2S_INTR_MASKED

**Description:** Interrupt masked register
**Address:** 0x40800F0C
**Offset:** 0xF0C
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:7] | TX_UNDERFLOW [6:6] | TX_OVERFLOW [5:5] | TX_EMPTY [4:4] | None [3:2] | | TX_NOT_FULL [1:1] | TX_TRIGGER [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:9] | | | | | | | TX_WD [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:23] | RX_UNDERFLOW [22:22] | RX_OVERFLOW [21:21] | None [20:20] | RX_FULL [19:19] | RX_NOT_EMPTY [18:18] | None [17:17] | RX_TRIGGER [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:25] | | | | | | | RX_WD [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | TX_TRIGGER | R | W | 0 | Logical and of corresponding request and mask bits. |
| 1 | TX_NOT_FULL | R | W | 0 | Logical and of corresponding request and mask bits. |
| 4 | TX_EMPTY | R | W | 0 | Logical and of corresponding request and mask bits. |
| 5 | TX_OVERFLOW | R | W | 0 | Logical and of corresponding request and mask bits. |
| 6 | TX_UNDERFLOW | R | W | 0 | Logical and of corresponding request and mask bits. |
| 8 | TX_WD | R | W | 0 | Logical and of corresponding request and mask bits. |
| 16 | RX_TRIGGER | R | W | 0 | Logical and of corresponding request and mask bits. |
| 18 | RX_NOT_EMPTY | R | W | 0 | Logical and of corresponding request and mask bits. |
| 19 | RX_FULL | R | W | 0 | Logical and of corresponding request and mask bits. |
| 21 | RX_OVERFLOW | R | W | 0 | Logical and of corresponding request and mask bits. |
| 22 | RX_UNDERFLOW | R | W | 0 | Logical and of corresponding request and mask bits. |
| 24 | RX_WD | R | W | 0 | Logical and of corresponding request and mask bits. |

# 19 IPC

**Description** IPC
**Base Address** 0x40220000
**Size** 0x10000
**Slave Num** MMIO2 - 2

## 19.1 STRUCT 0

| Register Name | Address | Permission | Description |
|---|---|---|---|
| IPC_STRUCT0_ACQUIRE | 0x40220000 | FULL | IPC acquire |
| IPC_STRUCT0_RELEASE | 0x40220004 | FULL | IPC release |
| IPC_STRUCT0_NOTIFY | 0x40220008 | FULL | IPC notification |
| IPC_STRUCT0_DATA0 | 0x4022000C | FULL | IPC data 0 |
| IPC_STRUCT0_DATA1 | 0x40220010 | FULL | IPC data 1 |
| IPC_STRUCT0_LOCK_STATUS | 0x4022001C | FULL | IPC lock status |

## 19.2 STRUCT 1

| Register Name | Address | Permission | Description |
|---|---|---|---|
| IPC_STRUCT1_ACQUIRE | 0x40220020 | FULL | IPC acquire |
| IPC_STRUCT1_RELEASE | 0x40220024 | FULL | IPC release |
| IPC_STRUCT1_NOTIFY | 0x40220028 | FULL | IPC notification |
| IPC_STRUCT1_DATA0 | 0x4022002C | FULL | IPC data 0 |
| IPC_STRUCT1_DATA1 | 0x40220030 | FULL | IPC data 1 |
| IPC_STRUCT1_LOCK_STATUS | 0x4022003C | FULL | IPC lock status |

## 19.3 STRUCT 2

| Register Name | Address | Permission | Description |
|---|---|---|---|
| IPC_STRUCT2_ACQUIRE | 0x40220040 | FULL | IPC acquire |
| IPC_STRUCT2_RELEASE | 0x40220044 | FULL | IPC release |
| IPC_STRUCT2_NOTIFY | 0x40220048 | FULL | IPC notification |
| IPC_STRUCT2_DATA0 | 0x4022004C | FULL | IPC data 0 |
| IPC_STRUCT2_DATA1 | 0x40220050 | FULL | IPC data 1 |
| IPC_STRUCT2_LOCK_STATUS | 0x4022005C | FULL | IPC lock status |

## 19.4 STRUCT 3

| Register Name | Address | Permission | Description |
|---|---|---|---|
| IPC_STRUCT3_ACQUIRE | 0x40220060 | FULL | IPC acquire |
| IPC_STRUCT3_RELEASE | 0x40220064 | FULL | IPC release |
| IPC_STRUCT3_NOTIFY | 0x40220068 | FULL | IPC notification |
| IPC_STRUCT3_DATA0 | 0x4022006C | FULL | IPC data 0 |
| IPC_STRUCT3_DATA1 | 0x40220070 | FULL | IPC data 1 |
| IPC_STRUCT3_LOCK_STATUS | 0x4022007C | FULL | IPC lock status |

## 19.5 STRUCT 4

| Register Name | Address | Permission | Description |
|---|---|---|---|
| IPC_STRUCT4_ACQUIRE | 0x40220080 | FULL | IPC acquire |
| IPC_STRUCT4_RELEASE | 0x40220084 | FULL | IPC release |
| IPC_STRUCT4_NOTIFY | 0x40220088 | FULL | IPC notification |
| IPC_STRUCT4_DATA0 | 0x4022008C | FULL | IPC data 0 |
| IPC_STRUCT4_DATA1 | 0x40220090 | FULL | IPC data 1 |
| IPC_STRUCT4_LOCK_STATUS | 0x4022009C | FULL | IPC lock status |

## 19.6 STRUCT 5

| Register Name | Address | Permission | Description |
|---|---|---|---|
| IPC_STRUCT5_ACQUIRE | 0x402200A0 | FULL | IPC acquire |
| IPC_STRUCT5_RELEASE | 0x402200A4 | FULL | IPC release |
| IPC_STRUCT5_NOTIFY | 0x402200A8 | FULL | IPC notification |
| IPC_STRUCT5_DATA0 | 0x402200AC | FULL | IPC data 0 |
| IPC_STRUCT5_DATA1 | 0x402200B0 | FULL | IPC data 1 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| IPC_STRUCT5_LOCK_STATUS | 0x402200BC | FULL | IPC lock status |

## 19.7 STRUCT 6

| Register Name | Address | Permission | Description |
|---|---|---|---|
| IPC_STRUCT6_ACQUIRE | 0x402200C0 | FULL | IPC acquire |
| IPC_STRUCT6_RELEASE | 0x402200C4 | FULL | IPC release |
| IPC_STRUCT6_NOTIFY | 0x402200C8 | FULL | IPC notification |
| IPC_STRUCT6_DATA0 | 0x402200CC | FULL | IPC data 0 |
| IPC_STRUCT6_DATA1 | 0x402200D0 | FULL | IPC data 1 |
| IPC_STRUCT6_LOCK_STATUS | 0x402200DC | FULL | IPC lock status |

## 19.8 STRUCT 7

| Register Name | Address | Permission | Description |
|---|---|---|---|
| IPC_STRUCT7_ACQUIRE | 0x402200E0 | FULL | IPC acquire |
| IPC_STRUCT7_RELEASE | 0x402200E4 | FULL | IPC release |
| IPC_STRUCT7_NOTIFY | 0x402200E8 | FULL | IPC notification |
| IPC_STRUCT7_DATA0 | 0x402200EC | FULL | IPC data 0 |
| IPC_STRUCT7_DATA1 | 0x402200F0 | FULL | IPC data 1 |
| IPC_STRUCT7_LOCK_STATUS | 0x402200FC | FULL | IPC lock status |

## 19.9 INTR_STRUCT 0

| Register Name | Address | Permission | Description |
|---|---|---|---|
| IPC_INTR_STRUCT0_INTR | 0x40221000 | FULL | Interrupt |
| IPC_INTR_STRUCT0_INTR_SET | 0x40221004 | FULL | Interrupt set |
| IPC_INTR_STRUCT0_INTR_MASK | 0x40221008 | FULL | Interrupt mask |
| IPC_INTR_STRUCT0_INTR_MASKED | 0x4022100C | FULL | Interrupt masked |

## 19.10 INTR_STRUCT 1

| Register Name | Address | Permission | Description |
|---|---|---|---|
| IPC_INTR_STRUCT1_INTR | 0x40221020 | FULL | Interrupt |
| IPC_INTR_STRUCT1_INTR_SET | 0x40221024 | FULL | Interrupt set |
| IPC_INTR_STRUCT1_INTR_MASK | 0x40221028 | FULL | Interrupt mask |
| IPC_INTR_STRUCT1_INTR_MASKED | 0x4022102C | FULL | Interrupt masked |

## 19.11 INTR_STRUCT 2

| Register Name | Address | Permission | Description |
|---|---|---|---|
| IPC_INTR_STRUCT2_INTR | 0x40221040 | FULL | Interrupt |
| IPC_INTR_STRUCT2_INTR_SET | 0x40221044 | FULL | Interrupt set |
| IPC_INTR_STRUCT2_INTR_MASK | 0x40221048 | FULL | Interrupt mask |
| IPC_INTR_STRUCT2_INTR_MASKED | 0x4022104C | FULL | Interrupt masked |

## 19.12 INTR_STRUCT 3

| Register Name | Address | Permission | Description |
|---|---|---|---|
| IPC_INTR_STRUCT3_INTR | 0x40221060 | FULL | Interrupt |
| IPC_INTR_STRUCT3_INTR_SET | 0x40221064 | FULL | Interrupt set |
| IPC_INTR_STRUCT3_INTR_MASK | 0x40221068 | FULL | Interrupt mask |
| IPC_INTR_STRUCT3_INTR_MASKED | 0x4022106C | FULL | Interrupt masked |

## 19.13 INTR_STRUCT 4

| Register Name | Address | Permission | Description |
|---|---|---|---|
| IPC_INTR_STRUCT4_INTR | 0x40221080 | FULL | Interrupt |
| IPC_INTR_STRUCT4_INTR_SET | 0x40221084 | FULL | Interrupt set |
| IPC_INTR_STRUCT4_INTR_MASK | 0x40221088 | FULL | Interrupt mask |
| IPC_INTR_STRUCT4_INTR_MASKED | 0x4022108C | FULL | Interrupt masked |

## 19.14 INTR_STRUCT 5

| Register Name | Address | Permission | Description |
|---|---|---|---|
| IPC_INTR_STRUCT5_INTR | 0x402210A0 | FULL | Interrupt |
| IPC_INTR_STRUCT5_INTR_SET | 0x402210A4 | FULL | Interrupt set |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| IPC_INTR_STRUCT5_INTR_MASK | 0x402210A8 | FULL | Interrupt mask |
| IPC_INTR_STRUCT5_INTR_MASKED | 0x402210AC | FULL | Interrupt masked |

## 19.15 INTR_STRUCT 6

| Register Name | Address | Permission | Description |
|---|---|---|---|
| IPC_INTR_STRUCT6_INTR | 0x402210C0 | FULL | Interrupt |
| IPC_INTR_STRUCT6_INTR_SET | 0x402210C4 | FULL | Interrupt set |
| IPC_INTR_STRUCT6_INTR_MASK | 0x402210C8 | FULL | Interrupt mask |
| IPC_INTR_STRUCT6_INTR_MASKED | 0x402210CC | FULL | Interrupt masked |

## 19.16 INTR_STRUCT 7

| Register Name | Address | Permission | Description |
|---|---|---|---|
| IPC_INTR_STRUCT7_INTR | 0x402210E0 | FULL | Interrupt |
| IPC_INTR_STRUCT7_INTR_SET | 0x402210E4 | FULL | Interrupt set |
| IPC_INTR_STRUCT7_INTR_MASK | 0x402210E8 | FULL | Interrupt mask |
| IPC_INTR_STRUCT7_INTR_MASKED | 0x402210EC | FULL | Interrupt masked |

## 19.17 Register Details

### 19.17.1 STRUCT

#### 19.17.1.1 IPC_STRUCT_ACQUIRE

**Description:** IPC acquire
**Address:** 0x40220000
**Offset:** 0x0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register is used to acquire a lock.

A non test controller (the master identifer of the access is NOT '15') read access attempts to acquire a lock. This read access will return the result of the attempt as well as parameters of the master which successfully acquired the lock.
A test controller (the master identifer of the access is '15') read access returns value of LOCK_STATUS. A test controller write access attempts to acquire a lock (the write data value is ignored and does not matter). A separate LOCK_STATUS read access is required to return the result of the attempt.

**Default:** Undefined as one or more bit fields have a default value that is undefined

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | PC [7:4] | | | | None [3:2] | | NS [1:1] | P [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:12] | | | | MS [11:8] | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | SUCCESS [31:31] | None [30:24] | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | P | R | W | Undefined | User/privileged access control:<br>'0': user mode.<br>'1': privileged mode.<br><br>This field is set with the user/privileged access control of the access that successfully acquired the lock. |
| 1 | NS | R | W | Undefined | Secure/non-secure access control:<br>'0': secure.<br>'1': non-secure.<br><br>This field is set with the secure/non-secure access control of the access that successfully acquired the lock. |
| 4:7 | PC | R | W | Undefined | This field specifies the protection context that successfully acquired the lock. |
| 8:11 | MS | R | W | Undefined | This field specifies the bus master identifier that successfully acquired the lock. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 31 | SUCCESS | R | RW | 0 | Specifies if the lock is successfully acquired or not (reading the ACQUIRE register can have affect on SUCCESS and LOCK_STATUS.ACQUIRED):<br>'0': Not successfully acquired; i.e. the lock was already acquired by another read transaction and not released. The P, NS, PC and MS fields reflect the access attributes of the transaction that previously successfully acuired the lock; the fields are NOT affected by the current access.<br>'1': Successfully acquired. The P, NS, PC and MS fields reflect the access attributes of the current access.<br><br>Note that this field is NOT SW writable. A lock is released by writing to the associated RELEASE register (irrespective of the write value). |

### 19.17.1.2 IPC_STRUCT_RELEASE

**Description:** IPC release
**Address:** 0x40220004
**Offset:** 0x4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register is used to release a lock.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | INTR_RELEASE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | INTR_RELEASE | W | | 0 | Writing this field releases a lock and allows for the generation of release events to the IPC interrupt structures, but only when the lock is acquired (LOCK_STATUS.ACQUIRED is '1'). The IPC release cause fields associated with this IPC structure are set to '1', but only for those IPC interrupt structures for which the corresponding bit field in INTR_RELEASE[] is set to '1'.<br><br>SW writes a '1' to the bit fields to generate a release event. Due to the transient nature of this event, SW always reads a '0' from this field. |

### 19.17.1.3 IPC_STRUCT_NOTIFY

**Description:** IPC notification
**Address:** 0x40220008
**Offset:** 0x8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | INTR_NOTIFY [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | INTR_NOTIFY | W | | 0 | This field allows for the generation of notification events to the IPC interrupt structures. The IPC notification cause fields associated with this IPC structure are set to '1', but only for those IPC interrupt structures for which the corresponding bit field in INTR_NOTIFY[] is set to '1'.<br><br>SW writes a '1' to the bit fields to generate a notify event. Due to the transient nature of this event, SW always reads a '0' from this field. |

### 19.17.1.4 IPC_STRUCT_DATA0

**Description:** IPC data 0
**Address:** 0x4022000C
**Offset:** 0xC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** Undefined as one or more bit fields have a default value that is undefined

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | DATA | RW | | Undefined | This field holds a 32-bit data element that is associated with the IPC structure. |

### 19.17.1.5 IPC_STRUCT_DATA1

**Description:** IPC data 1
**Address:** 0x40220010
**Offset:** 0x10
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** Undefined as one or more bit fields have a default value that is undefined

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | DATA | RW | | Undefined | This field holds a 32-bit data element that is associated with the IPC structure. |

### 19.17.1.6 IPC_STRUCT_LOCK_STATUS

**Description:** IPC lock status
**Address:** 0x4022001C
**Offset:** 0x1C
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** Undefined as one or more bit fields have a default value that is undefined

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | PC [7:4] | | | | None [3:2] | | NS [1:1] | P [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:12] | | | | MS [11:8] | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | ACQUIRED [31:31] | None [30:24] | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | P | R | W | Undefined | This field specifies the user/privileged access control:<br>'0': user mode.<br>'1': privileged mode. |
| 1 | NS | R | W | Undefined | This field specifies the secure/non-secure access control:<br>'0': secure.<br>'1': non-secure. |
| 4:7 | PC | R | W | Undefined | This field specifies the protection context that successfully acquired the lock. |
| 8:11 | MS | R | W | Undefined | This field specifies the bus master identifier that successfully acquired the lock. |
| 31 | ACQUIRED | R | R | 0 | Specifies if the lock is acquired. This field is set to '1', if a ACQUIRE read transfer successfully acquires the lock (the ACQUIRE read transfer returns ACQUIRE.SUCCESS as '1'). If zero, P, NS, PC, and MS are not valid. |

### 19.17.2 INTR_STRUCT

#### 19.17.2.1 IPC_INTR_STRUCT_INTR

**Description:** Interrupt
**Address:** 0x40221000
**Offset:** 0x0
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | RELEASE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | NOTIFY [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | RELEASE | RW1C | RW1S | 0 | These interrupt cause fields are activated (HW sets the field to '1') when a IPC release event is detected. One bit field for each master. SW writes a '1' to these field to clear the interrupt cause. |
| 16:23 | NOTIFY | RW1C | RW1S | 0 | These interrupt cause fields are activated (HW sets the field to '1') when a IPC notification event is detected. One bit field for each master. SW writes a '1' to these field to clear the interrupt cause. |

### 19.17.2.2 IPC_INTR_STRUCT_INTR_SET

**Description:** Interrupt set
**Address:** 0x40221004
**Offset:** 0x4
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** When read, this register reflects the INTR register. For debug purposes, SW can write a '1' to activate a specific interrupt cause (this allows for debug of the SW ISR, without relying on HW to activate the interrupt cause).
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | RELEASE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | NOTIFY [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | RELEASE | RW1S | A | 0 | SW writes a '1' to this field to set the corresponding field in the INTR register. |
| 16:23 | NOTIFY | RW1S | A | 0 | SW writes a '1' to this field to set the corresponding field in the INTR register. |

### 19.17.2.3 IPC_INTR_STRUCT_INTR_MASK

**Description:** Interrupt mask
**Address:** 0x40221008
**Offset:** 0x8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | RELEASE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | NOTIFY [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | RELEASE | RW | R | 0 | Mask bit for corresponding field in the INTR register. |
| 16:23 | NOTIFY | RW | R | 0 | Mask bit for corresponding field in the INTR register. |

### 19.17.2.4 IPC_INTR_STRUCT_INTR_MASKED

**Description:** Interrupt masked
**Address:** 0x4022100C
**Offset:** 0xC
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** When read, this register reflects 'a bitwise AND' between the INTR and INTR_MASK registers.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | RELEASE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | NOTIFY [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | RELEASE | R | W | 0 | Logical and of corresponding request and mask bits. |
| 16:23 | NOTIFY | R | W | 0 | Logical and of corresponding INTR and INTR_MASK fields. |

# 20 LIN

**Description** LIN
**Base Address** 0x40500000
**Size** 0x10000
**Slave Num** MMIO5 - 0

| Register Name | Address | Permission | Description |
|---|---|---|---|
| LIN0_ERROR_CTL | 0x40500000 | FULL | Error control |
| LIN0_TEST_CTL | 0x40500004 | FULL | Test control |

## 20.1 CH 0

| Register Name | Address | Permission | Description |
|---|---|---|---|
| LIN0_CH0_CTL0 | 0x40508000 | FULL | Control 0 |
| LIN0_CH0_CTL1 | 0x40508004 | FULL | Control 1 |
| LIN0_CH0_STATUS | 0x40508008 | FULL | Status |
| LIN0_CH0_CMD | 0x40508010 | FULL | Command |
| LIN0_CH0_TX_RX_STATUS | 0x40508060 | FULL | TX/RX status |
| LIN0_CH0_PID_CHECKSUM | 0x40508080 | FULL | PID and checksum |
| LIN0_CH0_DATA0 | 0x40508084 | FULL | Response data 0 |
| LIN0_CH0_DATA1 | 0x40508088 | FULL | Response data 1 |
| LIN0_CH0_INTR | 0x405080C0 | FULL | Interrupt |
| LIN0_CH0_INTR_SET | 0x405080C4 | FULL | Interrupt set |
| LIN0_CH0_INTR_MASK | 0x405080C8 | FULL | Interrupt mask |
| LIN0_CH0_INTR_MASKED | 0x405080CC | FULL | Interrupt masked |

## 20.2 CH 1

| Register Name | Address | Permission | Description |
|---|---|---|---|
| LIN0_CH1_CTL0 | 0x40508100 | FULL | Control 0 |
| LIN0_CH1_CTL1 | 0x40508104 | FULL | Control 1 |
| LIN0_CH1_STATUS | 0x40508108 | FULL | Status |
| LIN0_CH1_CMD | 0x40508110 | FULL | Command |
| LIN0_CH1_TX_RX_STATUS | 0x40508160 | FULL | TX/RX status |
| LIN0_CH1_PID_CHECKSUM | 0x40508180 | FULL | PID and checksum |
| LIN0_CH1_DATA0 | 0x40508184 | FULL | Response data 0 |
| LIN0_CH1_DATA1 | 0x40508188 | FULL | Response data 1 |
| LIN0_CH1_INTR | 0x405081C0 | FULL | Interrupt |
| LIN0_CH1_INTR_SET | 0x405081C4 | FULL | Interrupt set |
| LIN0_CH1_INTR_MASK | 0x405081C8 | FULL | Interrupt mask |
| LIN0_CH1_INTR_MASKED | 0x405081CC | FULL | Interrupt masked |

## 20.3 CH 2

| Register Name | Address | Permission | Description |
|---|---|---|---|
| LIN0_CH2_CTL0 | 0x40508200 | FULL | Control 0 |
| LIN0_CH2_CTL1 | 0x40508204 | FULL | Control 1 |
| LIN0_CH2_STATUS | 0x40508208 | FULL | Status |
| LIN0_CH2_CMD | 0x40508210 | FULL | Command |
| LIN0_CH2_TX_RX_STATUS | 0x40508260 | FULL | TX/RX status |
| LIN0_CH2_PID_CHECKSUM | 0x40508280 | FULL | PID and checksum |
| LIN0_CH2_DATA0 | 0x40508284 | FULL | Response data 0 |
| LIN0_CH2_DATA1 | 0x40508288 | FULL | Response data 1 |
| LIN0_CH2_INTR | 0x405082C0 | FULL | Interrupt |
| LIN0_CH2_INTR_SET | 0x405082C4 | FULL | Interrupt set |
| LIN0_CH2_INTR_MASK | 0x405082C8 | FULL | Interrupt mask |
| LIN0_CH2_INTR_MASKED | 0x405082CC | FULL | Interrupt masked |

## 20.4 CH 3

| Register Name | Address | Permission | Description |
|---|---|---|---|
| LIN0_CH3_CTL0 | 0x40508300 | FULL | Control 0 |
| LIN0_CH3_CTL1 | 0x40508304 | FULL | Control 1 |
| LIN0_CH3_STATUS | 0x40508308 | FULL | Status |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| LIN0_CH3_CMD | 0x40508310 | FULL | Command |
| LIN0_CH3_TX_RX_STATUS | 0x40508360 | FULL | TX/RX status |
| LIN0_CH3_PID_CHECKSUM | 0x40508380 | FULL | PID and checksum |
| LIN0_CH3_DATA0 | 0x40508384 | FULL | Response data 0 |
| LIN0_CH3_DATA1 | 0x40508388 | FULL | Response data 1 |
| LIN0_CH3_INTR | 0x405083C0 | FULL | Interrupt |
| LIN0_CH3_INTR_SET | 0x405083C4 | FULL | Interrupt set |
| LIN0_CH3_INTR_MASK | 0x405083C8 | FULL | Interrupt mask |
| LIN0_CH3_INTR_MASKED | 0x405083CC | FULL | Interrupt masked |

## 20.5 CH 4

| Register Name | Address | Permission | Description |
|---|---|---|---|
| LIN0_CH4_CTL0 | 0x40508400 | FULL | Control 0 |
| LIN0_CH4_CTL1 | 0x40508404 | FULL | Control 1 |
| LIN0_CH4_STATUS | 0x40508408 | FULL | Status |
| LIN0_CH4_CMD | 0x40508410 | FULL | Command |
| LIN0_CH4_TX_RX_STATUS | 0x40508460 | FULL | TX/RX status |
| LIN0_CH4_PID_CHECKSUM | 0x40508480 | FULL | PID and checksum |
| LIN0_CH4_DATA0 | 0x40508484 | FULL | Response data 0 |
| LIN0_CH4_DATA1 | 0x40508488 | FULL | Response data 1 |
| LIN0_CH4_INTR | 0x405084C0 | FULL | Interrupt |
| LIN0_CH4_INTR_SET | 0x405084C4 | FULL | Interrupt set |
| LIN0_CH4_INTR_MASK | 0x405084C8 | FULL | Interrupt mask |
| LIN0_CH4_INTR_MASKED | 0x405084CC | FULL | Interrupt masked |

## 20.6 CH 5

| Register Name | Address | Permission | Description |
|---|---|---|---|
| LIN0_CH5_CTL0 | 0x40508500 | FULL | Control 0 |
| LIN0_CH5_CTL1 | 0x40508504 | FULL | Control 1 |
| LIN0_CH5_STATUS | 0x40508508 | FULL | Status |
| LIN0_CH5_CMD | 0x40508510 | FULL | Command |
| LIN0_CH5_TX_RX_STATUS | 0x40508560 | FULL | TX/RX status |
| LIN0_CH5_PID_CHECKSUM | 0x40508580 | FULL | PID and checksum |
| LIN0_CH5_DATA0 | 0x40508584 | FULL | Response data 0 |
| LIN0_CH5_DATA1 | 0x40508588 | FULL | Response data 1 |
| LIN0_CH5_INTR | 0x405085C0 | FULL | Interrupt |
| LIN0_CH5_INTR_SET | 0x405085C4 | FULL | Interrupt set |
| LIN0_CH5_INTR_MASK | 0x405085C8 | FULL | Interrupt mask |
| LIN0_CH5_INTR_MASKED | 0x405085CC | FULL | Interrupt masked |

## 20.7 CH 6

| Register Name | Address | Permission | Description |
|---|---|---|---|
| LIN0_CH6_CTL0 | 0x40508600 | FULL | Control 0 |
| LIN0_CH6_CTL1 | 0x40508604 | FULL | Control 1 |
| LIN0_CH6_STATUS | 0x40508608 | FULL | Status |
| LIN0_CH6_CMD | 0x40508610 | FULL | Command |
| LIN0_CH6_TX_RX_STATUS | 0x40508660 | FULL | TX/RX status |
| LIN0_CH6_PID_CHECKSUM | 0x40508680 | FULL | PID and checksum |
| LIN0_CH6_DATA0 | 0x40508684 | FULL | Response data 0 |
| LIN0_CH6_DATA1 | 0x40508688 | FULL | Response data 1 |
| LIN0_CH6_INTR | 0x405086C0 | FULL | Interrupt |
| LIN0_CH6_INTR_SET | 0x405086C4 | FULL | Interrupt set |
| LIN0_CH6_INTR_MASK | 0x405086C8 | FULL | Interrupt mask |
| LIN0_CH6_INTR_MASKED | 0x405086CC | FULL | Interrupt masked |

## 20.8 CH 7

| Register Name | Address | Permission | Description |
|---|---|---|---|
| LIN0_CH7_CTL0 | 0x40508700 | FULL | Control 0 |
| LIN0_CH7_CTL1 | 0x40508704 | FULL | Control 1 |
| LIN0_CH7_STATUS | 0x40508708 | FULL | Status |
| LIN0_CH7_CMD | 0x40508710 | FULL | Command |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| LIN0_CH7_TX_RX_STATUS | 0x40508760 | FULL | TX/RX status |
| LIN0_CH7_PID_CHECKSUM | 0x40508780 | FULL | PID and checksum |
| LIN0_CH7_DATA0 | 0x40508784 | FULL | Response data 0 |
| LIN0_CH7_DATA1 | 0x40508788 | FULL | Response data 1 |
| LIN0_CH7_INTR | 0x405087C0 | FULL | Interrupt |
| LIN0_CH7_INTR_SET | 0x405087C4 | FULL | Interrupt set |
| LIN0_CH7_INTR_MASK | 0x405087C8 | FULL | Interrupt mask |
| LIN0_CH7_INTR_MASKED | 0x405087CC | FULL | Interrupt masked |

## 20.9 CH 8

| Register Name | Address | Permission | Description |
|---|---|---|---|
| LIN0_CH8_CTL0 | 0x40508800 | FULL | Control 0 |
| LIN0_CH8_CTL1 | 0x40508804 | FULL | Control 1 |
| LIN0_CH8_STATUS | 0x40508808 | FULL | Status |
| LIN0_CH8_CMD | 0x40508810 | FULL | Command |
| LIN0_CH8_TX_RX_STATUS | 0x40508860 | FULL | TX/RX status |
| LIN0_CH8_PID_CHECKSUM | 0x40508880 | FULL | PID and checksum |
| LIN0_CH8_DATA0 | 0x40508884 | FULL | Response data 0 |
| LIN0_CH8_DATA1 | 0x40508888 | FULL | Response data 1 |
| LIN0_CH8_INTR | 0x405088C0 | FULL | Interrupt |
| LIN0_CH8_INTR_SET | 0x405088C4 | FULL | Interrupt set |
| LIN0_CH8_INTR_MASK | 0x405088C8 | FULL | Interrupt mask |
| LIN0_CH8_INTR_MASKED | 0x405088CC | FULL | Interrupt masked |

## 20.10 CH 9

| Register Name | Address | Permission | Description |
|---|---|---|---|
| LIN0_CH9_CTL0 | 0x40508900 | FULL | Control 0 |
| LIN0_CH9_CTL1 | 0x40508904 | FULL | Control 1 |
| LIN0_CH9_STATUS | 0x40508908 | FULL | Status |
| LIN0_CH9_CMD | 0x40508910 | FULL | Command |
| LIN0_CH9_TX_RX_STATUS | 0x40508960 | FULL | TX/RX status |
| LIN0_CH9_PID_CHECKSUM | 0x40508980 | FULL | PID and checksum |
| LIN0_CH9_DATA0 | 0x40508984 | FULL | Response data 0 |
| LIN0_CH9_DATA1 | 0x40508988 | FULL | Response data 1 |
| LIN0_CH9_INTR | 0x405089C0 | FULL | Interrupt |
| LIN0_CH9_INTR_SET | 0x405089C4 | FULL | Interrupt set |
| LIN0_CH9_INTR_MASK | 0x405089C8 | FULL | Interrupt mask |
| LIN0_CH9_INTR_MASKED | 0x405089CC | FULL | Interrupt masked |

## 20.11 CH 10

| Register Name | Address | Permission | Description |
|---|---|---|---|
| LIN0_CH10_CTL0 | 0x40508A00 | FULL | Control 0 |
| LIN0_CH10_CTL1 | 0x40508A04 | FULL | Control 1 |
| LIN0_CH10_STATUS | 0x40508A08 | FULL | Status |
| LIN0_CH10_CMD | 0x40508A10 | FULL | Command |
| LIN0_CH10_TX_RX_STATUS | 0x40508A60 | FULL | TX/RX status |
| LIN0_CH10_PID_CHECKSUM | 0x40508A80 | FULL | PID and checksum |
| LIN0_CH10_DATA0 | 0x40508A84 | FULL | Response data 0 |
| LIN0_CH10_DATA1 | 0x40508A88 | FULL | Response data 1 |
| LIN0_CH10_INTR | 0x40508AC0 | FULL | Interrupt |
| LIN0_CH10_INTR_SET | 0x40508AC4 | FULL | Interrupt set |
| LIN0_CH10_INTR_MASK | 0x40508AC8 | FULL | Interrupt mask |
| LIN0_CH10_INTR_MASKED | 0x40508ACC | FULL | Interrupt masked |

## 20.12 CH 11

| Register Name | Address | Permission | Description |
|---|---|---|---|
| LIN0_CH11_CTL0 | 0x40508B00 | FULL | Control 0 |
| LIN0_CH11_CTL1 | 0x40508B04 | FULL | Control 1 |
| LIN0_CH11_STATUS | 0x40508B08 | FULL | Status |
| LIN0_CH11_CMD | 0x40508B10 | FULL | Command |
| LIN0_CH11_TX_RX_STATUS | 0x40508B60 | FULL | TX/RX status |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| LIN0_CH11_PID_CHECKSUM | 0x40508B80 | FULL | PID and checksum |
| LIN0_CH11_DATA0 | 0x40508B84 | FULL | Response data 0 |
| LIN0_CH11_DATA1 | 0x40508B88 | FULL | Response data 1 |
| LIN0_CH11_INTR | 0x40508BC0 | FULL | Interrupt |
| LIN0_CH11_INTR_SET | 0x40508BC4 | FULL | Interrupt set |
| LIN0_CH11_INTR_MASK | 0x40508BC8 | FULL | Interrupt mask |
| LIN0_CH11_INTR_MASKED | 0x40508BCC | FULL | Interrupt masked |

## 20.13 CH 12

| Register Name | Address | Permission | Description |
|---|---|---|---|
| LIN0_CH12_CTL0 | 0x40508C00 | FULL | Control 0 |
| LIN0_CH12_CTL1 | 0x40508C04 | FULL | Control 1 |
| LIN0_CH12_STATUS | 0x40508C08 | FULL | Status |
| LIN0_CH12_CMD | 0x40508C10 | FULL | Command |
| LIN0_CH12_TX_RX_STATUS | 0x40508C60 | FULL | TX/RX status |
| LIN0_CH12_PID_CHECKSUM | 0x40508C80 | FULL | PID and checksum |
| LIN0_CH12_DATA0 | 0x40508C84 | FULL | Response data 0 |
| LIN0_CH12_DATA1 | 0x40508C88 | FULL | Response data 1 |
| LIN0_CH12_INTR | 0x40508CC0 | FULL | Interrupt |
| LIN0_CH12_INTR_SET | 0x40508CC4 | FULL | Interrupt set |
| LIN0_CH12_INTR_MASK | 0x40508CC8 | FULL | Interrupt mask |
| LIN0_CH12_INTR_MASKED | 0x40508CCC | FULL | Interrupt masked |

## 20.14 CH 13

| Register Name | Address | Permission | Description |
|---|---|---|---|
| LIN0_CH13_CTL0 | 0x40508D00 | FULL | Control 0 |
| LIN0_CH13_CTL1 | 0x40508D04 | FULL | Control 1 |
| LIN0_CH13_STATUS | 0x40508D08 | FULL | Status |
| LIN0_CH13_CMD | 0x40508D10 | FULL | Command |
| LIN0_CH13_TX_RX_STATUS | 0x40508D60 | FULL | TX/RX status |
| LIN0_CH13_PID_CHECKSUM | 0x40508D80 | FULL | PID and checksum |
| LIN0_CH13_DATA0 | 0x40508D84 | FULL | Response data 0 |
| LIN0_CH13_DATA1 | 0x40508D88 | FULL | Response data 1 |
| LIN0_CH13_INTR | 0x40508DC0 | FULL | Interrupt |
| LIN0_CH13_INTR_SET | 0x40508DC4 | FULL | Interrupt set |
| LIN0_CH13_INTR_MASK | 0x40508DC8 | FULL | Interrupt mask |
| LIN0_CH13_INTR_MASKED | 0x40508DCC | FULL | Interrupt masked |

## 20.15 CH 14

| Register Name | Address | Permission | Description |
|---|---|---|---|
| LIN0_CH14_CTL0 | 0x40508E00 | FULL | Control 0 |
| LIN0_CH14_CTL1 | 0x40508E04 | FULL | Control 1 |
| LIN0_CH14_STATUS | 0x40508E08 | FULL | Status |
| LIN0_CH14_CMD | 0x40508E10 | FULL | Command |
| LIN0_CH14_TX_RX_STATUS | 0x40508E60 | FULL | TX/RX status |
| LIN0_CH14_PID_CHECKSUM | 0x40508E80 | FULL | PID and checksum |
| LIN0_CH14_DATA0 | 0x40508E84 | FULL | Response data 0 |
| LIN0_CH14_DATA1 | 0x40508E88 | FULL | Response data 1 |
| LIN0_CH14_INTR | 0x40508EC0 | FULL | Interrupt |
| LIN0_CH14_INTR_SET | 0x40508EC4 | FULL | Interrupt set |
| LIN0_CH14_INTR_MASK | 0x40508EC8 | FULL | Interrupt mask |
| LIN0_CH14_INTR_MASKED | 0x40508ECC | FULL | Interrupt masked |

## 20.16 CH 15

| Register Name | Address | Permission | Description |
|---|---|---|---|
| LIN0_CH15_CTL0 | 0x40508F00 | FULL | Control 0 |
| LIN0_CH15_CTL1 | 0x40508F04 | FULL | Control 1 |
| LIN0_CH15_STATUS | 0x40508F08 | FULL | Status |
| LIN0_CH15_CMD | 0x40508F10 | FULL | Command |
| LIN0_CH15_TX_RX_STATUS | 0x40508F60 | FULL | TX/RX status |
| LIN0_CH15_PID_CHECKSUM | 0x40508F80 | FULL | PID and checksum |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| LIN0_CH15_DATA0 | 0x40508F84 | FULL | Response data 0 |
| LIN0_CH15_DATA1 | 0x40508F88 | FULL | Response data 1 |
| LIN0_CH15_INTR | 0x40508FC0 | FULL | Interrupt |
| LIN0_CH15_INTR_SET | 0x40508FC4 | FULL | Interrupt set |
| LIN0_CH15_INTR_MASK | 0x40508FC8 | FULL | Interrupt mask |
| LIN0_CH15_INTR_MASKED | 0x40508FCC | FULL | Interrupt masked |

## 20.17 CH 16

| Register Name | Address | Permission | Description |
|---|---|---|---|
| LIN0_CH16_CTL0 | 0x40509000 | FULL | Control 0 |
| LIN0_CH16_CTL1 | 0x40509004 | FULL | Control 1 |
| LIN0_CH16_STATUS | 0x40509008 | FULL | Status |
| LIN0_CH16_CMD | 0x40509010 | FULL | Command |
| LIN0_CH16_TX_RX_STATUS | 0x40509060 | FULL | TX/RX status |
| LIN0_CH16_PID_CHECKSUM | 0x40509080 | FULL | PID and checksum |
| LIN0_CH16_DATA0 | 0x40509084 | FULL | Response data 0 |
| LIN0_CH16_DATA1 | 0x40509088 | FULL | Response data 1 |
| LIN0_CH16_INTR | 0x405090C0 | FULL | Interrupt |
| LIN0_CH16_INTR_SET | 0x405090C4 | FULL | Interrupt set |
| LIN0_CH16_INTR_MASK | 0x405090C8 | FULL | Interrupt mask |
| LIN0_CH16_INTR_MASKED | 0x405090CC | FULL | Interrupt masked |

## 20.18 CH 17

This instance is not available in the following part numbers:
CYT4BF8CES, CYT4BF8CEE, CYT4A0M1BE, CYT4BF8DES, CYT4BF8DEE, CYT4BF8CDS, CYT4A0M14S, CYT4BF8CDE, CYT4A0M14E, CYT4BF8CXE, CYT4BF8DDS, CYT4BF8DDE, CYT4A0100S.

| Register Name | Address | Permission | Description |
|---|---|---|---|
| LIN0_CH17_CTL0 | 0x40509100 | FULL | Control 0 |
| LIN0_CH17_CTL1 | 0x40509104 | FULL | Control 1 |
| LIN0_CH17_STATUS | 0x40509108 | FULL | Status |
| LIN0_CH17_CMD | 0x40509110 | FULL | Command |
| LIN0_CH17_TX_RX_STATUS | 0x40509160 | FULL | TX/RX status |
| LIN0_CH17_PID_CHECKSUM | 0x40509180 | FULL | PID and checksum |
| LIN0_CH17_DATA0 | 0x40509184 | FULL | Response data 0 |
| LIN0_CH17_DATA1 | 0x40509188 | FULL | Response data 1 |
| LIN0_CH17_INTR | 0x405091C0 | FULL | Interrupt |
| LIN0_CH17_INTR_SET | 0x405091C4 | FULL | Interrupt set |
| LIN0_CH17_INTR_MASK | 0x405091C8 | FULL | Interrupt mask |
| LIN0_CH17_INTR_MASKED | 0x405091CC | FULL | Interrupt masked |

## 20.19 CH 18

This instance is not available in the following part numbers:
CYT4BF8CES, CYT4BF8CEE, CYT4A0M1BE, CYT4BF8DES, CYT4BF8DEE, CYT4BF8CDS, CYT4A0M14S, CYT4BF8CDE, CYT4A0M14E, CYT4BF8CXE, CYT4BF8DDS, CYT4BF8DDE, CYT4A0100S.

| Register Name | Address | Permission | Description |
|---|---|---|---|
| LIN0_CH18_CTL0 | 0x40509200 | FULL | Control 0 |
| LIN0_CH18_CTL1 | 0x40509204 | FULL | Control 1 |
| LIN0_CH18_STATUS | 0x40509208 | FULL | Status |
| LIN0_CH18_CMD | 0x40509210 | FULL | Command |
| LIN0_CH18_TX_RX_STATUS | 0x40509260 | FULL | TX/RX status |
| LIN0_CH18_PID_CHECKSUM | 0x40509280 | FULL | PID and checksum |
| LIN0_CH18_DATA0 | 0x40509284 | FULL | Response data 0 |
| LIN0_CH18_DATA1 | 0x40509288 | FULL | Response data 1 |
| LIN0_CH18_INTR | 0x405092C0 | FULL | Interrupt |
| LIN0_CH18_INTR_SET | 0x405092C4 | FULL | Interrupt set |
| LIN0_CH18_INTR_MASK | 0x405092C8 | FULL | Interrupt mask |
| LIN0_CH18_INTR_MASKED | 0x405092CC | FULL | Interrupt masked |

## 20.20 CH 19

This instance is not available in the following part numbers:

CYT4BF8CES, CYT4BF8CEE, CYT4A0M1BE, CYT4BF8DES, CYT4BF8DEE, CYT4BF8CDS, CYT4A0M14S, CYT4BF8CDE, CYT4A0M14E, CYT4BF8CXE, CYT4BF8DDS, CYT4BF8DDE, CYT4A0100S.

| Register Name | Address | Permission | Description |
|---|---|---|---|
| LIN0_CH19_CTL0 | 0x40509300 | FULL | Control 0 |
| LIN0_CH19_CTL1 | 0x40509304 | FULL | Control 1 |
| LIN0_CH19_STATUS | 0x40509308 | FULL | Status |
| LIN0_CH19_CMD | 0x40509310 | FULL | Command |
| LIN0_CH19_TX_RX_STATUS | 0x40509360 | FULL | TX/RX status |
| LIN0_CH19_PID_CHECKSUM | 0x40509380 | FULL | PID and checksum |
| LIN0_CH19_DATA0 | 0x40509384 | FULL | Response data 0 |
| LIN0_CH19_DATA1 | 0x40509388 | FULL | Response data 1 |
| LIN0_CH19_INTR | 0x405093C0 | FULL | Interrupt |
| LIN0_CH19_INTR_SET | 0x405093C4 | FULL | Interrupt set |
| LIN0_CH19_INTR_MASK | 0x405093C8 | FULL | Interrupt mask |
| LIN0_CH19_INTR_MASKED | 0x405093CC | FULL | Interrupt masked |

## 20.21 Register Details

### 20.21.1 LIN_ERROR_CTL

**Description:** Error control
**Address:** 0x40500000
**Offset:** 0x0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register supports error functionality: it enables HW injected channel transmitter errors. The receiver should detect these errors and report these errors through activation of corresponding interrupt causes.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:5] | | | CH_IDX [4:0] | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | TX_CHECKSUM_STOP_ERROR [23:23] | TX_CHECKSUM_ERROR [22:22] | TX_DATA_STOP_ERROR [21:21] | None [20:20] | TX_PID_STOP_ERROR [19:19] | TX_PARITY_ERROR [18:18] | TX_SYNC_STOP_ERROR [17:17] | TX_SYNC_ERROR [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | ENABLED [31:31] | None [30:24] | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:4 | CH_IDX | RW | R | 0 | Specifies the channel index of the channel to which HW injected channel transmitter errors applies. |
| 16 | TX_SYNC_ERROR | RW | R | 0 | The synchronization field is changed from 0x55 to 0x00.<br><br>At the receiver, this should result in INTR.RX_HEADER_SYNC_ERROR activation. |
| 17 | TX_SYNC_STOP_ERROR | RW | R | 0 | The synchronization field STOP bits are inverted to '0'.<br><br>At the receiver, this should result in INTR.RX_HEADER_SYNC_ERROR or INTR.RX_HEADER_FRAME_ERROR activation. |
| 18 | TX_PARITY_ERROR | RW | R | 0 | In LIN mode, the PID parity bit P[1] is inverted from !(ID[5] ^ ID[4] ^ ID[3] ^ ID[1]) to (ID[5] ^ ID[4] ^ ID[3] ^ ID[1]).<br><br>At the receiver, this should result in INTR.RX_HEADER_PARITY_ERROR activation.<br><br>In UART mode, a data field's parity bit is inverted. |
| 19 | TX_PID_STOP_ERROR | RW | R | 0 | The PID field STOP bits are inverted to '0'.<br><br>At the receiver, this should result in INTR.RX_HEADER_FRAME_ERROR activation. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 21 | TX_DATA_STOP _ERROR | RW | R | 0 | The data field STOP bits are inverted to '0'.<br><br>At the receiver, this should result in INTR.RX_RESPONSE_FRAME_ERROR activation.<br><br>Note: Used in UART mode. |
| 22 | TX_CHECKSUM_ERROR | RW | R | 0 | The checksum field is inverted.<br><br>At the receiver, this should result in INTR.RX_RESPONSE_CHECKSUM_ERROR activation. |
| 23 | TX_CHECKSUM_STOP _ERROR | RW | R | 0 | The checksum field STOP bits are inverted to '0'.<br><br>At the receiver, this should result in INTR.RX_RESPONSE_FRAME_ERROR activation. |
| 31 | ENABLED | RW | R | 0 | Error injection enable:<br>'0': Disabled.<br>'1': Enabled. |

### 20.21.2 LIN_TEST_CTL

**Description:** Test control
**Address:** 0x40500004
**Offset:** 0x4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register support test functionality.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:5] | | | CH_IDX [4:0] | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:17] | | | | | | | MODE [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | ENABLED [31:31] | None [30:24] | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:4 | CH_IDX | RW | R | 0 | Specifies the channel index of the channel to which test applies. The channel IO signals of channel indices CH_IDX and CH_NR-1 are connected as specified by MODE. CH_IDX should be in the range [0, CH_NR-2], as channel index CH_NR-1 is always involved in test and cannot be connected to itself. The test mode allows BOTH of the two connected channels to be tested.<br><br>Note: this testing functionality simplifies SW development, but may also be used in the field to verify correct channel functionality. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 16 | MODE | RW | R | 0 | Test mode:<br>'0': Partial disconnect from IOSS. This mode's isolation allows for device test without relying on an external LIN transceiver. The IOSS 'tx' IO cell can be used to observe messages outside of the device.<br>- tx_in[CH_IDX] = IOSS lin_tx_in[CH_IDX].<br>- tx_in[CH_NR-1] = IOSS lin_tx_in[CH_IDX].<br>- rx_in[CH_IDX] = IOSS lin_tx_in[CH_IDX].<br>- rx_in[CH_NR-1] = IOSS lin_tx_in[CH_IDX].<br>- lin_tx_out[CH_IDX] = tx_out[CH_IDX] & tx_out[CH_NR-1].<br>- lin_tx_out[CH_NR-1] = tx_out[CH_IDX] & tx_out[CH_NR-1].<br><br>'1': Full disconnect from IOSS (the IOSS/HSIOM should disconnect 'tx_out' from the 'tx' IO cell). This mode's isolation allows for device test without effecting an operational LIN cluster.<br>- tx_in[CH_IDX] = lin_tx_out[CH_IDX].<br>- tx_in[CH_NR-1] = lin_tx_out[CH_IDX].<br>- rx_in[CH_IDX] = lin_tx_out[CH_IDX].<br>- rx_in[CH_NR-1] = lin_tx_out[CH_IDX].<br>- lin_tx_out[CH_IDX] = tx_out[CH_IDX] & tx_out[CH_NR-1].<br>- lin_tx_out[CH_NR-1] = tx_out[CH_IDX] & tx_out[CH_NR-1]. |
| 31 | ENABLED | RW | R | 0 | Test enable:<br>'0': Disabled. Functional mode.<br>- tx_in[CH_IDX] = IOSS lin_tx_in[CH_IDX].<br>- tx_in[CH_NR-1] = IOSS lin_tx_in[CH_NR-1].<br>- rx_in[CH_IDX] = IOSS lin_rx_in[CH_IDX].<br>- rx_in[CH_NR-1] = IOSS lin_rx_in[CH_NR-1].<br>- lin_tx_out[CH_IDX] = tx_out[CH_IDX].<br>- lin_tx_out[CH_NR-1] = tx_out[CH_NR-1].<br>'1': Enabled. Test mode, specific test mode is specified by MODE. |

### 20.21.3 CH

#### 20.21.3.1 LIN_CH_CTL0

**Description:** Control 0
**Address:** 0x40508000
**Offset:** 0x0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x400C0101

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:5] | | | AUTO_EN [4:4] | None [3:2] | | STOP_BITS [1:0] | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:10] | | | | | | BREAK_DELIMITER_LENGTH [9:8] | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:21] | | | BREAK_WAKEUP_LENGTH [20:16] | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | ENABLED [31:31] | FILTER_EN [30:30] | PARITY_EN [29:29] | PARITY [28:28] | BIT_ERROR_IGNORE [27:27] | None [26:25] | | MODE [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:1 | STOP_BITS | RW | R | 1 | STOP bit periods:<br>'0': 1/2 bit period.<br>'1': 1 bit period.<br>'2': 1 1/2 bit period.<br>'3': 2 bit periods.<br><br>In LIN mode, this field should be set to '1' (the default value) .<br><br>In UART mode, this field can be programmed as desired.<br><br>Note: receiver STOP bit frame errors can only be detected if the number of STOP bit periods is 1 or more bit period. |
| 4 | AUTO_EN | RW | R | 0 | LIN transceiver auto enable:<br>'0': Disabled.<br>'1': Enabled. The TX_RX_STATUS.EN_OUT field is controlled by HW. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 8:9 | BREAK_DELIMITER_LENGTH | RW | R | 1 | In LIN mode, this field specifies the break delimiter length:<br>(used in header transmission, not used in header reception).<br>'0': 1 bit period.<br>'1': 2 bit periods (default value).<br>'2': 3 bit periods.<br>'3': 4 bit periods.<br><br>In UART mode, this field specifies the data field size:<br>'0': 5 bit data field.<br>'1': 6 bit data field.<br>'2': 7 bit data field.<br>'3': 8 bit data field.<br>When the data field size is less than 8 bits, the most significant (unused) bits of the DATAx.DATAy[7:0] fields should be set to '0' for the transmitter. |
| 16:20 | BREAK_WAKEUP_LENGTH | RW | R | 12 | Break/wakeup length (minus 1) in bit periods:<br>'0': 1 bit period.<br>...<br>'10': 11 bit periods (break length for slave nodes)<br>...<br>'12': 13 bit periods (break length for master nodes)<br>...<br>'30': 31 bit periods.<br>'31': Illegal (should NOT be used!!!)<br><br>This field is used for transmission/reception of BOTH break and wakeup signals. Note that these functions are mutually exclusive:<br>- When CMD.TX_HEADER is '1', the field specifies the transmitted break field.<br>- When CMD.TX_WAKEUP is '1', the field specifies the transmitted wakeup field.<br>- When CMD.RX_HEADER is '1', the field specifies the to be received break field.<br>- Otherwise, the field specifies the to be received wakeup field.<br><br>Per the standard, the master wakeup duration is between 250 us and 5 ms. To support uncalibrated slaves, a slave has a detection threshold of 150 us (3 bit periods at 20 kbps). After transmission of a break or wakeup signal, the INTR.TX_BREAK_WAKEUP_DONE interrupt cause is activated. After reception of a wakeup signal, the INTR.RX_BREAK_WAKEUP_DONE interrupt cause is activated.<br><br>To specify longer wakeup signals in terms of absolute time (us/ms rather than bit periods), the associated PERI clock divider value can be (temporarily) increased to make the LIN bit period longer.<br><br>Note: entering bus sleep mode is achieved with the 'go-to-sleep' command. |
| 24 | MODE | RW | R | 0 | Mode of operation:<br>'0': LIN mode.<br>'1': UART mode. |
| | LIN | | | 0 | LIN mode. |
| | UART | | | 1 | UART mode. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 27 | BIT_ERROR_IGNORE | RW | R | 0 | Specifies behavior on a detected bit error during header or response transmission:<br>'0': Message transfer is aborted.<br>'1': Message transfer is NOT aborted.<br><br>Note: this field does NOT effect the reporting of the bit error through INTR/STATUS.TX_HEADER/RESPONSE_BIT_ERROR; i.e. bit errors are always reported. |
| 28 | PARITY | RW | R | 0 | Parity mode:<br>'0': Even parity: even number of '1' bits (including parity).<br>'1': Odd parity.<br><br>Note: Used in UART mode only. |
| 29 | PARITY_EN | RW | R | 0 | Parity generation enable:<br>'0': Disabled. No parity bit is transferred.<br>'1': Enabled. The parity bit is transferred after the last (most significant) data field bit.<br><br>Note: Used in UART mode only. |
| 30 | FILTER_EN | RW | R | 1 | RX filter (for 'lin_rx_in'):<br>'0': No filter.<br>'1': Median 3 (default value) operates on the last three 'lin_rx_in' values. The sequences '000', '001', '010' and '100' result in a filtered value '0'. The sequences '111', '110', '101' and '011' result in a filtered value '1'. |
| 31 | ENABLED | RW | R | 0 | Channel enable:<br>'0': Disabled. If a channel is disabled, all non-retained MMIO registers (e.g. the TX_RX_STATUS, and INTR registers) have their fields reset to their default value.<br>'1': Enabled. |

### 20.21.3.2 LIN_CH_CTL1

**Description:** Control 1
**Address:** 0x40508004
**Offset:** 0x4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** A master node is aware of a message's checksum mode and number of data fields. Therefore, a master node can set the CHECKSUM_ENHANCED and DATA_NR fields accordingly, BEFORE the message header transmission.

A slave node needs to derive a message's checksum mode and number of data fields from the received PID field, AFTER the message header reception. The INTR.RX_HEADER_DONE interrupt cause indicates that the message header is received and PID_CHECKSUM.PID contains the received PID field. Slave node SW can use this PID field information to set CHECKSUM_ENHANCED and DATA_NR fields accordingly. A minimum message response consists of at least 1 data field, and the CHECKSUM_ENHANCED and DATA_NR fields need to be set BEFORE the receipt of the STOP bit(s) of the first data field; i.e. SW effectively has a data field transfer duration to set the fields.

**Default:** Undefined as one or more bit fields have a default value that is undefined

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:3] | | | | | DATA_NR [2:0] | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:9] | | | | | | | CHECKSUM_ENHANCED [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | FRAME_TIMEOUT [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:26] | | | | | | FRAME_TIMEOUT_SEL [25:24] | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:2 | DATA_NR | RW | R | Undefined | Number of data fields (minus 1) in the response (not including the checksum):<br>'0': 1 data field.<br>'1': 2 data fields.<br>...<br>'7': 8 data fields.<br><br>Note: master and slave nodes need to agree upon the number of data fields before message transfer.<br>In RX_RESPONSE case, When PID (header) is received, firmware has the time of one response data byte, to modify CTL1.DATA_NR. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 8 | CHECKSUM_ ENHANCED | RW | R | Undefined | Checksum mode:<br>'0': Classic mode. PID field is NOT included in the checksum calculation.<br>'1': Enhanced mode. PID field is included in the checksum calculation. This mode requires special attention when the master node transmits the header and a (different) slave node transmits the response: the slave node will use the calculated partial checksum over the received PID field as a starting point for the calculation over the to be transmitted data fields.<br><br>Note: If the frame identifier ID[5:0] is 0x3c or 0x3d, the classic mode will ALWAYS be used for transmission and assumed for reception, independent of the CHECKSUM_ENHANCED value. |
| 16:23 | FRAME_TIMEOUT | RW | R | Undefined | Specifies the maximum allowed length (timeout value) for a frame, frame header or frame response in bit periods. The LIN specification prescribes to set the maximum length to 1.4x the nominal length (Theader_max = 1.4 x Theader_nom and Tresponse_max = 1.4 x Tresponse_nom). The nominal header length Theader_nom is 34 bit periods and the nominal response length Tresponse_nom is 10 * (data_nr + 1) bit periods (data_nr is the number of data fields)<br><br>Note: the LIN specification specifies the following: 'Tools and tests shall check the Tframe_max (= Theader_max + Tresponse_max). Nodes shall not check this time. The receiving node of the frame shall accept the frame up to the next frame slot (i.e. next break field), even if it is longer then Tframe_max).' |
| 24:25 | FRAME_TIMEOUT_SEL | RW | R | 0 | Specifies the frame timeout mode:<br>'0': No timeout functionality (default value).<br>'1': Frame mode: detects timeout from the start of break field to checksum field STOP bits (inclusive). The minimum FRAME_TIMEOUT value is 34+20 bit periods (header and a response with 1 data field).<br>'2': Frame header mode: detects timeout from the start of break field to PID field STOP bits (inclusive). The minimum FRAME_TIMEOUT value is 34 bit periods (header).<br>'3': Frame response mode: detects timeout from the PID field STOP bits (exclusive) to checksum field STOP bits (the response space is included in the frame response). The minimum FRAME_TIMEOUT value is 20 bit periods (response with 1 data field). |

### 20.21.3.3 LIN_CH_STATUS

**Description:** Status
**Address:** 0x40508008
**Offset:** 0x8
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** The register fields are not retained. This is to ensure that they come up as '0' after coming out of DeepSleep system power mode.

This is a non-retained register; setting CTL.ENABLED to '0' clears all status fields to '0'.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:6] | | RX_DATA0_FRAME_ERROR [5:5] | HEADER_RESPONSE [4:4] | DATA_IDX [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:14] | | RX_DONE [13:13] | TX_DONE [12:12] | None [11:10] | | RX_BUSY [9:9] | TX_BUSY [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:18] | | | | | | TX_RESPONSE_BIT_ERROR [17:17] | TX_HEADER_BIT_ERROR [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:29] | | | RX_RESPONSE_CHECKSUM_ERROR [28:28] | RX_RESPONSE_FRAME_ERROR [27:27] | RX_HEADER_PARITY_ERROR [26:26] | RX_HEADER_SYNC_ERROR [25:25] | RX_HEADER_FRAME_ERROR [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | DATA_IDX | R | W | 0 | Number of transferred data and checksum fields in the response (also acts as an index/address into response data field and checksum field registers (DATA0, DATA1, PID_CHECKSUM)) :<br>'0': No data fields transferred.<br>'1': Data field 1 transferred.<br>...<br>'7': Data fields 1, 2, 3, ... and 7 transferred.<br>'8': Data fields 1, 2, 3, ... and 8 transferred.<br>'9': Data fields 1, 2, 3, ..., 8 and checksum field transferred.<br>'10'-'15': Unused.<br><br>Set to '0' on the start of a TX_HEADER or RX_HEADER command. |
| 4 | HEADER_RESPONSE | R | W | 0 | Frame header / response identifier (only valid when TX_BUSY or RX_BUSY is '1'):<br>'0': Frame header being transferred.<br>'1': Frame response being transferred. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 5 | RX_DATA0_FRAME_ERROR | R | W | 0 | Frame response, first data field frame error. HW sets this field to '1' when the received STOP bits of the first response data field have an unexpected value (only after a RX_HEADER command), and this data byte is 0x00. HW clears this field to '0' at the falling edge of SYNC start bit (after INTR.RX_HEADER_BREAK_WAKEUP_DONE). This field is used together with INTR.RX_RESPONSE_FRAME_ERROR to distinguish 'no response', 'error response' and 'correct response' scenarios.<br><br>Note: The ongoing message transfer is NOT aborted. |
| 8 | TX_BUSY | R | W | 0 | Transmitter busy.<br>- Set to '1' on the start of the following commands: TX_HEADER, TX_RESPONSE, TX_WAKEUP.<br>- Set to '0' on successful completion of previous commands or when an error is detected. In the successful completion case, TX_BUSY is updated one cycle after TX_DONE.<br>In 'TX_HEADER, RX_RESPONSE' case, set to '0' at the start bit falling edge in the first response data byte, after header transmission |
| 9 | RX_BUSY | R | W | 0 | Receiver busy.<br>- Set to '1' on the start of the following commands: RX_HEADER, RX_RESPONSE.<br>in RX_HEADER case, set at Break filed rising edge.<br>in RX_RESPONSE case, set at the start bit falling edge in the first response data byte.<br><br>- Set to '0' on successful completion of previous commands or when an error is detected. In the successful completion case, RX_BUSY is updated one cycle after RX_DONE. |
| 12 | TX_DONE | R | W | 0 | Transmitter done:<br>- Set to '0' on the start of a new command.<br>- Set to '1' on successful completion of the following command sequences (if CTL.AUTO_EN is '1', this includes the 4-bit period external transceiver disable post-amble):<br>- TX_HEADER.<br>- TX_HEADER, TX_RESPONSE.<br>- RX_HEADER, TX_RESPONSE.<br>- TX_WAKEUP. |
| 13 | RX_DONE | R | W | 0 | Receiver done:<br>- Set to '0' on the start of a new command.<br>- Set to '1' on successful completion of the following command sequences (if CTL.AUTO_EN is '1', this includes the 4-bit period external transceiver disable post-amble):<br>- RX_HEADER, RX_RESPONSE.<br>- TX_HEADER, RX_RESPONSE. |
| 16 | TX_HEADER_BIT_ERROR | R | W | 0 | Copy of INTR.TX_HEADER_BIT_ERROR. |
| 17 | TX_RESPONSE_BIT_ERROR | R | W | 0 | Copy of INTR.TX_RESPONSE_BIT_ERROR. |
| 24 | RX_HEADER_FRAME_ERROR | R | W | 0 | Copy of INTR.RX_HEADER_FRAME_ERROR. |
| 25 | RX_HEADER_SYNC_ERROR | R | W | 0 | Copy of INTR.RX_HEADER_SYNC_ERROR. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 26 | RX_HEADER_PARITY_ERROR | R | W | 0 | Copy of INTR.RX_HEADER_PARITY_ERROR. |
| 27 | RX_RESPONSE_FRAME_ERROR | R | W | 0 | Copy of INTR.RX_RESPONSE_FRAME_ERROR. |
| 28 | RX_RESPONSE_CHECKSUM_ERROR | R | W | 0 | Copy of INTR.RX_RESPONSE_CHECKSUM_ERROR. |

### 20.21.3.4 LIN_CH_CMD

**Description:** Command
**Address:** 0x40508010
**Offset:** 0x10
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** The register fields are retained. When a LIN channel is disabled (CTL.ENABLED is set to '0'), HW sets all the register fields to '0'.

The following restrictions apply when programming the commands:
- TX_HEADER and RX_HEADER are mutually exclusive; i.e. cannot both be set to '1'.
- TX_WAKEUP is mutually exclusive with all other commands.
- TX_RESPONSE and RX_RESPONSE are NOT mutually exclusive, but are evaluated in the following order (of decreasing priority): TX_RESPONSE, RX_RESPONSE.

The CMD.TX_HEADER register field description provides all legal command sequences. The break or wakeup detection is always enabled, regardless of CMD register setting.

Note: LIN mode supports all commands, UART mode supports the TX_HEADER and RX_HEADER commands only.

**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:3] | | | | | TX_WAKEUP [2:2] | TX_RESPONSE [1:1] | TX_HEADER [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:10] | | | | | | RX_RESPONSE [9:9] | RX_HEADER [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | TX_HEADER | RW1S | RW | 0 | SW sets this field to '1' to transmit a header. HW sets this field to '0' on successful completion of ANY of the following legal command sequences (also set to '0' when an error is detected):<br>- TX_HEADER<br>- TX_HEADER, TX_RESPONSE.<br>- TX_HEADER, RX_RESPONSE.<br>- RX_HEADER, TX_RESPONSE.<br>- RX_HEADER, RX_RESPONSE.<br>- TX_WAKEUP.<br><br>The header is transmitted when the PID field STOP bits are transmitted (INTR.TX_HEADER_DONE).<br><br>HW sets this field to '1', when the 'tr_cmd_tx_header' input trigger is activated. This allows for time triggered LIN message transfer. HW driven time triggered transfer eliminates the jitter that is typically associated with SW driven transfer.<br><br>In UART mode, a single data field (DATA0.DATA1) is transmitted. |
| 1 | TX_RESPONSE | RW1S | RW1C | 0 | SW sets this field to '1' to transmit a response. HW sets this field to '0' on successful completion of ANY of the legal command sequences (also set to '0' when an error is detected).<br><br>The response is transmitted when the checksum field STOP bits are transmitted (INTR.TX_RESPONSE_DONE). |
| 2 | TX_WAKEUP | RW1S | RW1C | 0 | SW sets this field to '1' to transmit a wakeup signal. HW sets this field to '0' on successful completion of ANY of the legal command sequences (also set to '0' when an error is detected).<br><br>The command generates CTL.BREAK_WAKEUP_LENGTH bit periods in the dominant state (low/'0') and transitions to the recessive state (high/'1') (INTR.TX_WAKEUP_DONE). |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 8 | RX_HEADER | RW1S | RW1C | 0 | SW sets this field to '1' to receive a header. HW sets this field to '0' on successful completion of the ANY of the legal command sequences (NOT set to '0' when an error is detected in LIN mode).<br><br>The header is received when the PID field STOP bits are received (INTR.RX_HEADER_DONE).<br><br>Typically, a slave node SW sets both RX_HEADER and RX_RESPONSE to '1', anticipating a transfer of a response from the master node to this slave node. After receipt of the header PID field (INTR.RX_HEADER_PID_DONE is activated), the slave node may decide to set TX_RESPONSE to '1' (which has a higher priority than RX_RESPONSE) to transmit a response.<br><br>the Break detection is performed regardless of CMD.RX_HEADER.<br>INTR.RX_BREAK_WAKEUP_DONE will trigger at LIN_RX rising edge, when the low pulse meet CTL0.BREAK_WAKEUP_LENGTH. when Break is detected, HW check CMD.RX_HEADER before entering SYNC byte processing state. when RX_HEADER is cleared, SW has at least 11 bit times to set RX_HEADER again, before next Break is detected (RX_BREAK_WAKEUP_DONE). in this case, there is no gap, Break will never be missed.<br><br>In UART mode, a single data field in received (in DATA0.DATA1). HW set this field to '0' when the data field is received, or when an error is detected. |
| 9 | RX_RESPONSE | RW1S | RW1C | 0 | SW sets this field to '1' to receive a response. HW sets this field to '0' on successful completion of ANY of the legal command sequences (NOT set to '0' when an error is detected).<br><br>The response is received when the checksum field STOP bits are received (INTR.RX_RESPONSE_DONE). |

### 20.21.3.5 LIN_CH_TX_RX_STATUS

**Description:** TX/RX status
**Address:** 0x40508060
**Offset:** 0x60
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** Undefined as one or more bit fields have a default value that is undefined

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | SYNC_COUNTER [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:18] | | | | | | RX_IN [17:17] | TX_IN [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:27] | | | | | EN_OUT [26:26] | None [25:25] | TX_OUT [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | SYNC_COUNTER | R | W | Undefined | Synchronization counter in LIN channel clock periods. After the receipt of a synchronization field, this fields reflects the duration of the synchronization field. Ideally, SYNC_COUNTER = 8*16 = 128 (the synchronization fields consists of eight bit period of 16 LIN channel clock periods each).<br>- If SYNC_COUNTER is less than 128, the LIN channel clock is too slow and the PERI/PCLK divider value should be decreased.<br>- If SYNC_COUNTER is greater than 128, the LIN channel clock is too fast and the PERI/PCLK divider value should be increased.<br><br>The biggest master-slave clock discrepancy occurs when the master is slow and the slave is fast or vice versa. At a 0.5 percent master inaccuracy and a 14 percent slave inaccuracy, this results in the extreme synchronization values of (.86 * 128) / 1.005 = 109.5 and (1.14 *128) / 0.995 = 146.6. We add a little margin for a valid range of [106, 152].<br><br>Note: Only slave nodes with imprecise clocks require clock resynchronization. Master and slave nodes with precise clocks do NOT require clock resynchronization. |
| 16 | TX_IN | R | W | Undefined | LIN transmitter input ('tx_in', 'lin_tx_in' in functional mode). TX_IN and RX_IN can be used to determine a wakeup source. Note that wakeup source detection relies on the external transceiver functionality. |
| 17 | RX_IN | R | W | Undefined | LIN receiver input ('rx_in', 'lin_rx_in' in functional mode). |
| 24 | TX_OUT | R | W | 1 | LIN transmitter output ('tx_out', 'lin_tx_out'). |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 26 | EN_OUT | RW | RW | 1 | LIN transceiver enable ('en_out', 'lin_en_out'). This field controls the enable (or low active sleep enable) of the external transceiver:<br>'0': Disabled.<br>'1': Enabled.<br><br>If CTL.AUTO_EN is '0', SW controls this field to enable the external transceiver. If CTL.AUTO_EN is '1', HW controls this field to enable the external transceiver:<br>- Before a legal command sequence, HW sets this field to '1', if it is '0'. The start of the command sequence is effectively postponed by a 4-bit period preamble.<br>- After a legal command sequence, HW clears this field to '0'. The end of the command sequence is effectively postponed by a 4-bit period postamble.<br><br>Note: external transceivers require a 'power up' or 'power down' period of 1 or 2 bit periods, so a 4-bit period suffices for all known transceivers. |

### 20.21.3.6 LIN_CH_PID_CHECKSUM

**Description:** PID and checksum
**Address:** 0x40508080
**Offset:** 0x80
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register supports 8-bit, 16-bit and 32-bit accesses.

A LIN header has a single PID field. This field is SW accessible through this register. The field is used in BOTH transmit and receive modes.

A LIN response has a single checksum field. This field is SW accessible through this register. The field is used in BOTH transmit and receive modes.

**Default:** Undefined as one or more bit fields have a default value that is undefined

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | PID [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | CHECKSUM [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | PID | RW | RW | Undefined | Header protected identifier (PID).<br>- Bits 5 down to 0: frame identifier ID[5:0].<br>Frame identifier 0x3c is for a 'master request' frame, 0x3d is for a 'slave response' frame, 0x3e and 0x3f are for future LIN enhancements. Frame identifier ID[5:4] is optionally used for length control; i.e. specifies the number of response data fields.<br>- Bits 1 down to 0: parity bits P[1] and P[0].<br>- P[1] = ! (ID[5] ^ ID[4] ^ ID[3] ^ ID[1])<br>- P[0] = (ID[4] ^ ID[2] ^ ID[1] ^ ID[0])<br><br>Transmission: To be transmitted PID field. SW needs to calculate the PID field parity bits P[1] and P[0].<br><br>Reception: Received PID field. Slave node SW uses the PID field to determine how to handle the response for a received frame header: TX_RESPONSE or RX_RESPONSE. |
| 8:15 | CHECKSUM | R | RW | Undefined | Checksum.<br><br>Transmission: HW calculated checksum (SW does not need to calculate the checksum) over the transmitted PID field (optional per CTL.CHECKSUM_ENHANCED) and data fields.<br><br>Reception: Received checksum. Note that in case of a RX_CHECKSUM_ERROR, SW can use the received PID field and the received data fields to calculate the correct checksum value. |

### 20.21.3.7 LIN_CH_DATA0

**Description:** Response data 0
**Address:** 0x40508084
**Offset:** 0x84
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register supports 8-bit, 16-bit and 32-bit accesses. This allows for a single 32-bit access to write or read four data fields.

A LIN response has a maximum of eight data fields. These data fields are SW accessible through the DATA0 and DATA1 registers. These register are used in BOTH transmit and receive modes. If the LIN response is both transmitted and received, the to be transmitted data fields (provided by SW) in this register are overwritten by the received data fields (provided by HW).

Data field DATA1 is the first response data field (first to be transmitted/received). The number of transmitted/received data fields is specified by CTL.DATA_NR.
**Default:** Undefined as one or more bit fields have a default value that is undefined

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA1 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA2 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA3 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA4 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | DATA1 | RW | RW | Undefined | Data field 1.<br><br>Transmission: To be transmitted data field. SW provides data field.<br><br>Reception: Received data field. SW uses the data field. |
| 8:15 | DATA2 | RW | RW | Undefined | Data field 2. |
| 16:23 | DATA3 | RW | RW | Undefined | Data field 3. |
| 24:31 | DATA4 | RW | RW | Undefined | Data field 4. |

### 20.21.3.8 LIN_CH_DATA1

**Description:** Response data 1
**Address:** 0x40508088
**Offset:** 0x88
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register supports 8-bit, 16-bit and 32-bit accesses. This allows for a single 32-bit access to write or read four data fields.
**Default:** Undefined as one or more bit fields have a default value that is undefined

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA5 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA6 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA7 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA8 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | DATA5 | RW | RW | Undefined | Data field 5. |
| 8:15 | DATA6 | RW | RW | Undefined | Data field 6. |
| 16:23 | DATA7 | RW | RW | Undefined | Data field 7. |
| 24:31 | DATA8 | RW | RW | Undefined | Data field 8. |

### 20.21.3.9 LIN_CH_INTR

**Description:** Interrupt
**Address:** 0x405080C0
**Offset:** 0xC0
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** The register fields are not retained. This is to ensure that they come up as '0' after coming out of DeepSleep system power mode.

This is a non-retained register; setting CTL.ENABLED to '0' clears all command fields to '0'.

An activated error interrupt cause aborts an ongoing frame transfer (except for bit errors when CTL.BIT_ERROR_IGNORE is '1').

Note: LIN mode supports all interrupt causes. UART mode supports the RX_NOISE_DETECT, TX_HEADER_BIT_ERROR, RX_HEADER_FRAME_ERROR and RX_HEADER_PARITY_ERROR interrupt causes only.

**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:3] | | | | | TX_WAKEUP_DONE [2:2] | TX_RESPONSE_DONE [1:1] | TX_HEADER_DONE [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:15] | TIMEOUT [14:14] | RX_NOISE_DETECT [13:13] | None [12:12] | RX_HEADER_SYNC_DONE [11:11] | RX_BREAK_WAKEUP_DONE [10:10] | RX_RESPONSE_DONE [9:9] | RX_HEADER_DONE [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:18] | | | | | | TX_RESPONSE_BIT_ERROR [17:17] | TX_HEADER_BIT_ERROR [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:29] | | | RX_RESPONSE_CHECKSUM_ERROR [28:28] | RX_RESPONSE_FRAME_ERROR [27:27] | RX_HEADER_PARITY_ERROR [26:26] | RX_HEADER_SYNC_ERROR [25:25] | RX_HEADER_FRAME_ERROR [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | TX_HEADER_DONE | RW1C | RW1S | 0 | HW sets this field to '1', when a frame header (break field, synchronization field and PID field) is transmitted (the CMD.TX_HEADER is completed). Specifically:<br>- When followed by CMD.TX_RESPONSE or CMD.RX_RESPONSE, this field is set to '1' after completion of the frame header transfer.<br>- When not followed by a response command, this field is set to '1' after completion of the frame header transfer. If CTL.AUTO_EN is '1', this includes the 4-bit period external transceiver disable post-amble.<br><br>Note: used in UART mode. |
| 1 | TX_RESPONSE_DONE | RW1C | RW1S | 0 | HW sets this field to '1', when a frame response (data fields and checksum field) is transmitted (the CMD.TX_RESPONSE is completed). If CTL.AUTO_EN is '1', this includes the 4-bit period external transceiver disable post-amble. |
| 2 | TX_WAKEUP_DONE | RW1C | RW1S | 0 | HW sets this field to '1', when a wakeup signal is transmitted (per CTL.BREAK_WAKEUP_LENGTH). This cause is activated on a transition from dominant/'0' state to recessive/'1' state; i.e. at the end of the wakeup signal. |
| 8 | RX_HEADER_DONE | RW1C | RW1S | 0 | HW sets this field to '1', when a frame header (break field, synchronization field and PID field) is received (the CMD.RX_HEADER is completed). Specifically:<br>- When followed by CMD.TX_RESPONSE or CMD.RX_RESPONSE, this field is set to '1' after completion of the frame header transfer.<br>- When not followed by a response command, this field is set to '1' after completion of the frame header transfer. If CTL.AUTO_EN is '1', this includes the 4-bit period external transceiver disable post-amble.<br><br>Note: used in UART mode. |
| 9 | RX_RESPONSE_DONE | RW1C | RW1S | 0 | HW sets this field to '1', when a frame response (data fields and checksum field) is received (the CMD.RX_RESPONSE is completed). If CTL.AUTO_EN is '1', this includes the 4-bit period external transceiver disable post-amble.<br><br>Note: activation implies that RX_RESPONSE_FRAME_ERROR and RX_RESPONSE_CHECKSUM_ERROR are not activated during response reception |
| 10 | RX_BREAK_WAKEUP_DONE | RW1C | RW1S | 0 | HW sets this field to '1', when a break or wakeup signal is received (per CTL.BREAK_WAKEUP_LENGTH). This cause is activated on a transition from dominant/'0' state to recessive/'1' state; i.e. at the end of the wakeup signal.<br><br>The break or wakeup detection is always enabled, regardless of CMD register setting. |
| 11 | RX_HEADER_SYNC_DONE | RW1C | RW1S | 0 | HW sets this field to '1', when a synchronization field is received (including trailing STOP bits). |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 13 | RX_NOISE_DETECT | RW1C | RW1S | 0 | HW sets this field to '1', when isolated '0' or '1' 'in_rx_in' values are observed or when during sampling the last three 'lin_rx_in' values do NOT all have the same value. This mismatch is an indication of noise on the LIN line.<br><br>Note: The ongoing frame transfer is NOT aborted.<br><br>Note: Used in UART mode. |
| 14 | TIMEOUT | RW1C | RW1S | 0 | HW sets this field to '1', when a frame, frame header or frame response timeout is detected (per CTL.FRAME_TIMEOUT_SEL).<br><br>Note: The ongoing frame transfer is NOT aborted. |
| 16 | TX_HEADER_BIT _ERROR | RW1C | RW1S | 0 | HW sets this field to '1', when a transmitted 'lin_tx_out' value does NOT match a received 'lin_rx_in' value (during header transmission). This specific test allows for delay through the external transceiver. This mismatch is an indication of bus collisions on the LIN line.<br><br>The match is performed for the Wakeup, Break, SYNC and the PID fields (for the START bit, data Byte and STOP bit).<br><br>Note: When CTL.BIT_ERROR_IGNORE is '0', the ongoing message transfer is aborted (INTR.TX_HEADER_DONE is NOT activated) and the TX_HEADER, TX_RESPONSE and TX_WAKEUP commands are set to '0'.<br><br>Note: Used in UART mode. |
| 17 | TX_RESPONSE_BIT _ERROR | RW1C | RW1S | 0 | HW sets this field to '1', when a transmitted 'lin_tx_out' value does NOT match a received 'lin_rx_in' value (during response transmission).<br><br>The match is performed for the data fields and the checksum field (for the START bit, data Byte and STOP bit).<br><br>Note: When CTL.BIT_ERROR_IGNORE is '0', the ongoing message transfer is aborted (INTR.TX_RESPONSE_DONE is NOT activated) and the TX_HEADER, TX_RESPONSE and TX_WAKEUP commands are set to '0'. |
| 24 | RX_HEADER_FRAME _ERROR | RW1C | RW1S | 0 | HW sets this field to '1', when the received START or STOP bits have an unexpected value (during header reception).<br><br>Note: The ongoing message transfer is aborted (INTR.RX_HEADER_DONE is NOT activated) and the TX_HEADER, TX_RESPONSE and TX_WAKEUP commands are set to '0'.<br><br>Note: Used in UART mode. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 25 | RX_HEADER_SYNC _ERROR | RW1C | RW1S | 0 | HW sets this field to '1', when the received synchronization field is not received within the synchronization counter range [106, 152] (see TX_RX_STATUS.SYNC_COUNTER).<br><br>Note: The ongoing message transfer is aborted (INTR.RX_HEADER_SYNC_DONE is NOT activated) and the TX_HEADER, TX_RESPONSE and TX_WAKEUP commands are set to '0'. |
| 26 | RX_HEADER_PARITY _ERROR | RW1C | RW1S | 0 | HW sets this field to '1', when the received PID field has a parity error.<br><br>Note: The ongoing message transfer is aborted (INTR.RX_PID_DONE is NOT activated) and the TX_HEADER, TX_RESPONSE and TX_WAKEUP commands are set to '0'.<br><br>+G119 HW sets this field to '1', when the received data field has a parity error (when CTL0.PARITY_EN is '1'). |
| 27 | RX_RESPONSE_FRAME _ERROR | RW1C | RW1S | 0 | HW sets this field to '1', when the received START or STOP bits have an unexpected value (during response reception). HW does NOT use this field for the STOP bits of the first data field after a RX_HEADER command, if the received data byte is 0x00. (STATUS.RX_DATA0_FRAME_ERROR is used instead).<br><br>Note: The ongoing message transfer is aborted (INTR.RX_RESPONSE_DONE is NOT activated) and the TX_HEADER, TX_RESPONSE and TX_WAKEUP commands are set to '0'. |
| 28 | RX_RESPONSE _CHECKSUM_ERROR | RW1C | RW1S | 0 | HW sets this field to '1', when the calculated checksum over the received PID and data fields is not the same as the received checksum.<br><br>Note: The ongoing message transfer is aborted (INTR.RX_RESPONSE_DONE is NOT activated) and the TX_HEADER, TX_RESPONSE and TX_WAKEUP commands are set to '0'. |

### 20.21.3.10 LIN_CH_INTR_SET

**Description:** Interrupt set
**Address:** 0x405080C4
**Offset:** 0xC4
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** When read, this register reflects the INTR register.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:3] | | | | | TX_WAKEUP_DONE [2:2] | TX_RESPONSE_DONE [1:1] | TX_HEADER_DONE [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:15] | TIMEOUT [14:14] | RX_NOISE_DETECT [13:13] | None [12:12] | RX_HEADER_SYNC_DONE [11:11] | RX_BREAK_WAKEUP_DONE [10:10] | RX_RESPONSE_DONE [9:9] | RX_HEADER_DONE [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:18] | | | | | | TX_RESPONSE_BIT_ERROR [17:17] | TX_HEADER_BIT_ERROR [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:29] | | | RX_RESPONSE_CHECKSUM_ERROR [28:28] | RX_RESPONSE_FRAME_ERROR [27:27] | RX_HEADER_PARITY_ERROR [26:26] | RX_HEADER_SYNC_ERROR [25:25] | RX_HEADER_FRAME_ERROR [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | TX_HEADER_DONE | RW1S | A | 0 | Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect). |
| 1 | TX_RESPONSE_DONE | RW1S | A | 0 | Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect). |
| 2 | TX_WAKEUP_DONE | RW1S | A | 0 | Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect). |
| 8 | RX_HEADER_DONE | RW1S | A | 0 | Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect). |
| 9 | RX_RESPONSE_DONE | RW1S | A | 0 | Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect). |
| 10 | RX_BREAK_WAKEUP_DONE | RW1S | A | 0 | Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect). |
| 11 | RX_HEADER_SYNC_DONE | RW1S | A | 0 | Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect). |
| 13 | RX_NOISE_DETECT | RW1S | A | 0 | Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect). |
| 14 | TIMEOUT | RW1S | A | 0 | Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect). |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 16 | TX_HEADER_BIT _ERROR | RW1S | A | 0 | Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect). |
| 17 | TX_RESPONSE_BIT _ERROR | RW1S | A | 0 | Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect). |
| 24 | RX_HEADER_FRAME _ERROR | RW1S | A | 0 | Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect). |
| 25 | RX_HEADER_SYNC _ERROR | RW1S | A | 0 | Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect). |
| 26 | RX_HEADER_PARITY _ERROR | RW1S | A | 0 | Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect). |
| 27 | RX_RESPONSE_FRAME _ERROR | RW1S | A | 0 | Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect). |
| 28 | RX_RESPONSE _CHECKSUM_ERROR | RW1S | A | 0 | Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect). |

### 20.21.3.11 LIN_CH_INTR_MASK

**Description:** Interrupt mask
**Address:** 0x405080C8
**Offset:** 0xC8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:3] | | | | | TX_WAKEUP_DONE [2:2] | TX_RESPONSE_DONE [1:1] | TX_HEADER_DONE [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:15] | TIMEOUT [14:14] | RX_NOISE_DETECT [13:13] | None [12:12] | RX_HEADER_SYNC_DONE [11:11] | RX_BREAK_WAKEUP_DONE [10:10] | RX_RESPONSE_DONE [9:9] | RX_HEADER_DONE [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:18] | | | | | | TX_RESPONSE_BIT_ERROR [17:17] | TX_HEADER_BIT_ERROR [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:29] | | | RX_RESPONSE_CHECKSUM_ERROR [28:28] | RX_RESPONSE_FRAME_ERROR [27:27] | RX_HEADER_PARITY_ERROR [26:26] | RX_HEADER_SYNC_ERROR [25:25] | RX_HEADER_FRAME_ERROR [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | TX_HEADER_DONE | RW | R | 0 | Mask for corresponding field in INTR register. |
| 1 | TX_RESPONSE_DONE | RW | R | 0 | Mask for corresponding field in INTR register. |
| 2 | TX_WAKEUP_DONE | RW | R | 0 | Mask for corresponding field in INTR register. |
| 8 | RX_HEADER_DONE | RW | R | 0 | Mask for corresponding field in INTR register. |
| 9 | RX_RESPONSE_DONE | RW | R | 0 | Mask for corresponding field in INTR register. |
| 10 | RX_BREAK_WAKEUP_DONE | RW | R | 0 | Mask for corresponding field in INTR register. |
| 11 | RX_HEADER_SYNC_DONE | RW | R | 0 | Mask for corresponding field in INTR register. |
| 13 | RX_NOISE_DETECT | RW | R | 0 | Mask for corresponding field in INTR register. |
| 14 | TIMEOUT | RW | R | 0 | Mask for corresponding field in INTR register. |
| 16 | TX_HEADER_BIT_ERROR | RW | R | 0 | Mask for corresponding field in INTR register. |
| 17 | TX_RESPONSE_BIT_ERROR | RW | R | 0 | Mask for corresponding field in INTR register. |
| 24 | RX_HEADER_FRAME_ERROR | RW | R | 0 | Mask for corresponding field in INTR register. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 25 | RX_HEADER_SYNC _ERROR | RW | R | 0 | Mask for corresponding field in INTR register. |
| 26 | RX_HEADER_PARITY _ERROR | RW | R | 0 | Mask for corresponding field in INTR register. |
| 27 | RX_RESPONSE_FRAME _ERROR | RW | R | 0 | Mask for corresponding field in INTR register. |
| 28 | RX_RESPONSE _CHECKSUM_ERROR | RW | R | 0 | Mask for corresponding field in INTR register. |

### 20.21.3.12 LIN_CH_INTR_MASKED

**Description:** Interrupt masked
**Address:** 0x405080CC
**Offset:** 0xCC
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** When read, this register reflects a bitwise AND between the INTR and INTR_MASK registers. This register allows SW to read the status of all mask enabled interrupt causes with a single load operation, rather than two load operations: one for INTR and one for INTR_MASK. This simplifies Firmware development. The associated interrupt is active ('1'), when INTR_MASKED != 0.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:3] | | | | | TX_WAKEUP_DONE [2:2] | TX_RESPONSE_DONE [1:1] | TX_HEADER_DONE [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:15] | TIMEOUT [14:14] | RX_NOISE_DETECT [13:13] | None [12:12] | RX_HEADER_SYNC_DONE [11:11] | RX_BREAK_WAKEUP_DONE [10:10] | RX_RESPONSE_DONE [9:9] | RX_HEADER_DONE [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:18] | | | | | | TX_RESPONSE_BIT_ERROR [17:17] | TX_HEADER_BIT_ERROR [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:29] | | | RX_RESPONSE_CHECKSUM_ERROR [28:28] | RX_RESPONSE_FRAME_ERROR [27:27] | RX_HEADER_PARITY_ERROR [26:26] | RX_HEADER_SYNC_ERROR [25:25] | RX_HEADER_FRAME_ERROR [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | TX_HEADER_DONE | R | W | 0 | Logical AND of corresponding INTR and INTR_MASK fields. |
| 1 | TX_RESPONSE_DONE | R | W | 0 | Logical AND of corresponding INTR and INTR_MASK fields. |
| 2 | TX_WAKEUP_DONE | R | W | 0 | Logical AND of corresponding INTR and INTR_MASK fields. |
| 8 | RX_HEADER_DONE | R | W | 0 | Logical AND of corresponding INTR and INTR_MASK fields. |
| 9 | RX_RESPONSE_DONE | R | W | 0 | Logical AND of corresponding INTR and INTR_MASK fields. |
| 10 | RX_BREAK_WAKEUP_DONE | R | W | 0 | Logical AND of corresponding INTR and INTR_MASK fields. |
| 11 | RX_HEADER_SYNC_DONE | R | W | 0 | Logical AND of corresponding INTR and INTR_MASK fields. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 13 | RX_NOISE_DETECT | R | W | 0 | Logical AND of corresponding INTR and INTR_MASK fields. |
| 14 | TIMEOUT | R | W | 0 | Logical AND of corresponding INTR and INTR_MASK fields. |
| 16 | TX_HEADER_BIT _ERROR | R | W | 0 | Logical AND of corresponding INTR and INTR_MASK fields. |
| 17 | TX_RESPONSE_BIT _ERROR | R | W | 0 | Logical AND of corresponding INTR and INTR_MASK fields. |
| 24 | RX_HEADER_FRAME _ERROR | R | W | 0 | Logical AND of corresponding INTR and INTR_MASK fields. |
| 25 | RX_HEADER_SYNC _ERROR | R | W | 0 | Logical AND of corresponding INTR and INTR_MASK fields. |
| 26 | RX_HEADER_PARITY _ERROR | R | W | 0 | Logical AND of corresponding INTR and INTR_MASK fields. |
| 27 | RX_RESPONSE_FRAME _ERROR | R | W | 0 | Logical AND of corresponding INTR and INTR_MASK fields. |
| 28 | RX_RESPONSE _CHECKSUM_ERROR | R | W | 0 | Logical AND of corresponding INTR and INTR_MASK fields. |

# 21 PASS

**Description** Programmable Analog Subsystem for S40E
**Base Address** 0x40900000
**Size** 0x100000
**Slave Num** MMIO9 - 0

## 21.1 SAR 0

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR0_CTL | 0x40900000 | FULL | Analog control register. |
| PASS0_SAR0_DIAG_CTL | 0x40900004 | FULL | Diagnostic Reference control register. |
| PASS0_SAR0_PRECOND_CTL | 0x40900010 | FULL | Preconditioning control register. |
| PASS0_SAR0_ANA_CAL | 0x40900080 | FULL | Current analog calibration values |
| PASS0_SAR0_DIG_CAL | 0x40900084 | FULL | Current digital calibration values |
| PASS0_SAR0_ANA_CAL_ALT | 0x40900090 | FULL | Alternate analog calibration values |
| PASS0_SAR0_DIG_CAL_ALT | 0x40900094 | FULL | Alternate digital calibration values |
| PASS0_SAR0_CAL_UPD_CMD | 0x40900098 | FULL | Calibration update command |
| PASS0_SAR0_TR_PEND | 0x40900100 | FULL | Trigger pending status |
| PASS0_SAR0_WORK_VALID | 0x40900180 | FULL | Channel working data register 'valid' bits |
| PASS0_SAR0_WORK_RANGE | 0x40900184 | FULL | Range detected |
| PASS0_SAR0_WORK_RANGE_HI | 0x40900188 | FULL | Range detect above Hi flag |
| PASS0_SAR0_WORK_PULSE | 0x4090018C | FULL | Pulse detected |
| PASS0_SAR0_RESULT_VALID | 0x409001A0 | FULL | Channel result data register 'valid' bits |
| PASS0_SAR0_RESULT_RANGE_HI | 0x409001A4 | FULL | Channel Range above Hi flags |
| PASS0_SAR0_STATUS | 0x40900200 | FULL | Current status of internal SAR registers (mostly for debug) |
| PASS0_SAR0_AVG_STAT | 0x40900204 | FULL | Current averaging status (for debug) |

### 21.1.1 CH 0

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR0_CH0_TR_CTL | 0x40900800 | FULL | Trigger control. |
| PASS0_SAR0_CH0_SAMPLE_CTL | 0x40900804 | FULL | Sample control. |
| PASS0_SAR0_CH0_POST_CTL | 0x40900808 | FULL | Post processing control |
| PASS0_SAR0_CH0_RANGE_CTL | 0x4090080C | FULL | Range thresholds |
| PASS0_SAR0_CH0_INTR | 0x40900810 | FULL | Interrupt request register. |
| PASS0_SAR0_CH0_INTR_SET | 0x40900814 | FULL | Interrupt set request register |
| PASS0_SAR0_CH0_INTR_MASK | 0x40900818 | FULL | Interrupt mask register. |
| PASS0_SAR0_CH0_INTR_MASKED | 0x4090081C | FULL | Interrupt masked request register |
| PASS0_SAR0_CH0_WORK | 0x40900820 | FULL | Working data register |
| PASS0_SAR0_CH0_RESULT | 0x40900824 | FULL | Result data register |
| PASS0_SAR0_CH0_GRP_STAT | 0x40900828 | FULL | Group status register |
| PASS0_SAR0_CH0_ENABLE | 0x40900838 | FULL | Enable register |
| PASS0_SAR0_CH0_TR_CMD | 0x4090083C | FULL | Software triggers |

### 21.1.2 CH 1

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR0_CH1_TR_CTL | 0x40900840 | FULL | Trigger control. |
| PASS0_SAR0_CH1_SAMPLE_CTL | 0x40900844 | FULL | Sample control. |
| PASS0_SAR0_CH1_POST_CTL | 0x40900848 | FULL | Post processing control |
| PASS0_SAR0_CH1_RANGE_CTL | 0x4090084C | FULL | Range thresholds |
| PASS0_SAR0_CH1_INTR | 0x40900850 | FULL | Interrupt request register. |
| PASS0_SAR0_CH1_INTR_SET | 0x40900854 | FULL | Interrupt set request register |
| PASS0_SAR0_CH1_INTR_MASK | 0x40900858 | FULL | Interrupt mask register. |
| PASS0_SAR0_CH1_INTR_MASKED | 0x4090085C | FULL | Interrupt masked request register |
| PASS0_SAR0_CH1_WORK | 0x40900860 | FULL | Working data register |
| PASS0_SAR0_CH1_RESULT | 0x40900864 | FULL | Result data register |
| PASS0_SAR0_CH1_GRP_STAT | 0x40900868 | FULL | Group status register |
| PASS0_SAR0_CH1_ENABLE | 0x40900878 | FULL | Enable register |
| PASS0_SAR0_CH1_TR_CMD | 0x4090087C | FULL | Software triggers |

### 21.1.3 CH 2

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR0_CH2_TR_CTL | 0x40900880 | FULL | Trigger control. |
| PASS0_SAR0_CH2_SAMPLE_CTL | 0x40900884 | FULL | Sample control. |
| PASS0_SAR0_CH2_POST_CTL | 0x40900888 | FULL | Post processing control |
| PASS0_SAR0_CH2_RANGE_CTL | 0x4090088C | FULL | Range thresholds |
| PASS0_SAR0_CH2_INTR | 0x40900890 | FULL | Interrupt request register. |
| PASS0_SAR0_CH2_INTR_SET | 0x40900894 | FULL | Interrupt set request register |
| PASS0_SAR0_CH2_INTR_MASK | 0x40900898 | FULL | Interrupt mask register. |
| PASS0_SAR0_CH2_INTR_MASKED | 0x4090089C | FULL | Interrupt masked request register |
| PASS0_SAR0_CH2_WORK | 0x409008A0 | FULL | Working data register |
| PASS0_SAR0_CH2_RESULT | 0x409008A4 | FULL | Result data register |
| PASS0_SAR0_CH2_GRP_STAT | 0x409008A8 | FULL | Group status register |
| PASS0_SAR0_CH2_ENABLE | 0x409008B8 | FULL | Enable register |
| PASS0_SAR0_CH2_TR_CMD | 0x409008BC | FULL | Software triggers |

### 21.1.4 CH 3

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR0_CH3_TR_CTL | 0x409008C0 | FULL | Trigger control. |
| PASS0_SAR0_CH3_SAMPLE_CTL | 0x409008C4 | FULL | Sample control. |
| PASS0_SAR0_CH3_POST_CTL | 0x409008C8 | FULL | Post processing control |
| PASS0_SAR0_CH3_RANGE_CTL | 0x409008CC | FULL | Range thresholds |
| PASS0_SAR0_CH3_INTR | 0x409008D0 | FULL | Interrupt request register. |
| PASS0_SAR0_CH3_INTR_SET | 0x409008D4 | FULL | Interrupt set request register |
| PASS0_SAR0_CH3_INTR_MASK | 0x409008D8 | FULL | Interrupt mask register. |
| PASS0_SAR0_CH3_INTR_MASKED | 0x409008DC | FULL | Interrupt masked request register |
| PASS0_SAR0_CH3_WORK | 0x409008E0 | FULL | Working data register |
| PASS0_SAR0_CH3_RESULT | 0x409008E4 | FULL | Result data register |
| PASS0_SAR0_CH3_GRP_STAT | 0x409008E8 | FULL | Group status register |
| PASS0_SAR0_CH3_ENABLE | 0x409008F8 | FULL | Enable register |
| PASS0_SAR0_CH3_TR_CMD | 0x409008FC | FULL | Software triggers |

### 21.1.5 CH 4

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR0_CH4_TR_CTL | 0x40900900 | FULL | Trigger control. |
| PASS0_SAR0_CH4_SAMPLE_CTL | 0x40900904 | FULL | Sample control. |
| PASS0_SAR0_CH4_POST_CTL | 0x40900908 | FULL | Post processing control |
| PASS0_SAR0_CH4_RANGE_CTL | 0x4090090C | FULL | Range thresholds |
| PASS0_SAR0_CH4_INTR | 0x40900910 | FULL | Interrupt request register. |
| PASS0_SAR0_CH4_INTR_SET | 0x40900914 | FULL | Interrupt set request register |
| PASS0_SAR0_CH4_INTR_MASK | 0x40900918 | FULL | Interrupt mask register. |
| PASS0_SAR0_CH4_INTR_MASKED | 0x4090091C | FULL | Interrupt masked request register |
| PASS0_SAR0_CH4_WORK | 0x40900920 | FULL | Working data register |
| PASS0_SAR0_CH4_RESULT | 0x40900924 | FULL | Result data register |
| PASS0_SAR0_CH4_GRP_STAT | 0x40900928 | FULL | Group status register |
| PASS0_SAR0_CH4_ENABLE | 0x40900938 | FULL | Enable register |
| PASS0_SAR0_CH4_TR_CMD | 0x4090093C | FULL | Software triggers |

### 21.1.6 CH 5

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR0_CH5_TR_CTL | 0x40900940 | FULL | Trigger control. |
| PASS0_SAR0_CH5_SAMPLE_CTL | 0x40900944 | FULL | Sample control. |
| PASS0_SAR0_CH5_POST_CTL | 0x40900948 | FULL | Post processing control |
| PASS0_SAR0_CH5_RANGE_CTL | 0x4090094C | FULL | Range thresholds |
| PASS0_SAR0_CH5_INTR | 0x40900950 | FULL | Interrupt request register. |
| PASS0_SAR0_CH5_INTR_SET | 0x40900954 | FULL | Interrupt set request register |
| PASS0_SAR0_CH5_INTR_MASK | 0x40900958 | FULL | Interrupt mask register. |
| PASS0_SAR0_CH5_INTR_MASKED | 0x4090095C | FULL | Interrupt masked request register |
| PASS0_SAR0_CH5_WORK | 0x40900960 | FULL | Working data register |
| PASS0_SAR0_CH5_RESULT | 0x40900964 | FULL | Result data register |
| PASS0_SAR0_CH5_GRP_STAT | 0x40900968 | FULL | Group status register |
| PASS0_SAR0_CH5_ENABLE | 0x40900978 | FULL | Enable register |
| PASS0_SAR0_CH5_TR_CMD | 0x4090097C | FULL | Software triggers |

### 21.1.7 CH 6

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR0_CH6_TR_CTL | 0x40900980 | FULL | Trigger control. |
| PASS0_SAR0_CH6_SAMPLE_CTL | 0x40900984 | FULL | Sample control. |
| PASS0_SAR0_CH6_POST_CTL | 0x40900988 | FULL | Post processing control |
| PASS0_SAR0_CH6_RANGE_CTL | 0x4090098C | FULL | Range thresholds |
| PASS0_SAR0_CH6_INTR | 0x40900990 | FULL | Interrupt request register. |
| PASS0_SAR0_CH6_INTR_SET | 0x40900994 | FULL | Interrupt set request register |
| PASS0_SAR0_CH6_INTR_MASK | 0x40900998 | FULL | Interrupt mask register. |
| PASS0_SAR0_CH6_INTR_MASKED | 0x4090099C | FULL | Interrupt masked request register |
| PASS0_SAR0_CH6_WORK | 0x409009A0 | FULL | Working data register |
| PASS0_SAR0_CH6_RESULT | 0x409009A4 | FULL | Result data register |
| PASS0_SAR0_CH6_GRP_STAT | 0x409009A8 | FULL | Group status register |
| PASS0_SAR0_CH6_ENABLE | 0x409009B8 | FULL | Enable register |
| PASS0_SAR0_CH6_TR_CMD | 0x409009BC | FULL | Software triggers |

### 21.1.8 CH 7

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR0_CH7_TR_CTL | 0x409009C0 | FULL | Trigger control. |
| PASS0_SAR0_CH7_SAMPLE_CTL | 0x409009C4 | FULL | Sample control. |
| PASS0_SAR0_CH7_POST_CTL | 0x409009C8 | FULL | Post processing control |
| PASS0_SAR0_CH7_RANGE_CTL | 0x409009CC | FULL | Range thresholds |
| PASS0_SAR0_CH7_INTR | 0x409009D0 | FULL | Interrupt request register. |
| PASS0_SAR0_CH7_INTR_SET | 0x409009D4 | FULL | Interrupt set request register |
| PASS0_SAR0_CH7_INTR_MASK | 0x409009D8 | FULL | Interrupt mask register. |
| PASS0_SAR0_CH7_INTR_MASKED | 0x409009DC | FULL | Interrupt masked request register |
| PASS0_SAR0_CH7_WORK | 0x409009E0 | FULL | Working data register |
| PASS0_SAR0_CH7_RESULT | 0x409009E4 | FULL | Result data register |
| PASS0_SAR0_CH7_GRP_STAT | 0x409009E8 | FULL | Group status register |
| PASS0_SAR0_CH7_ENABLE | 0x409009F8 | FULL | Enable register |
| PASS0_SAR0_CH7_TR_CMD | 0x409009FC | FULL | Software triggers |

### 21.1.9 CH 8

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR0_CH8_TR_CTL | 0x40900A00 | FULL | Trigger control. |
| PASS0_SAR0_CH8_SAMPLE_CTL | 0x40900A04 | FULL | Sample control. |
| PASS0_SAR0_CH8_POST_CTL | 0x40900A08 | FULL | Post processing control |
| PASS0_SAR0_CH8_RANGE_CTL | 0x40900A0C | FULL | Range thresholds |
| PASS0_SAR0_CH8_INTR | 0x40900A10 | FULL | Interrupt request register. |
| PASS0_SAR0_CH8_INTR_SET | 0x40900A14 | FULL | Interrupt set request register |
| PASS0_SAR0_CH8_INTR_MASK | 0x40900A18 | FULL | Interrupt mask register. |
| PASS0_SAR0_CH8_INTR_MASKED | 0x40900A1C | FULL | Interrupt masked request register |
| PASS0_SAR0_CH8_WORK | 0x40900A20 | FULL | Working data register |
| PASS0_SAR0_CH8_RESULT | 0x40900A24 | FULL | Result data register |
| PASS0_SAR0_CH8_GRP_STAT | 0x40900A28 | FULL | Group status register |
| PASS0_SAR0_CH8_ENABLE | 0x40900A38 | FULL | Enable register |
| PASS0_SAR0_CH8_TR_CMD | 0x40900A3C | FULL | Software triggers |

### 21.1.10 CH 9

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR0_CH9_TR_CTL | 0x40900A40 | FULL | Trigger control. |
| PASS0_SAR0_CH9_SAMPLE_CTL | 0x40900A44 | FULL | Sample control. |
| PASS0_SAR0_CH9_POST_CTL | 0x40900A48 | FULL | Post processing control |
| PASS0_SAR0_CH9_RANGE_CTL | 0x40900A4C | FULL | Range thresholds |
| PASS0_SAR0_CH9_INTR | 0x40900A50 | FULL | Interrupt request register. |
| PASS0_SAR0_CH9_INTR_SET | 0x40900A54 | FULL | Interrupt set request register |
| PASS0_SAR0_CH9_INTR_MASK | 0x40900A58 | FULL | Interrupt mask register. |
| PASS0_SAR0_CH9_INTR_MASKED | 0x40900A5C | FULL | Interrupt masked request register |
| PASS0_SAR0_CH9_WORK | 0x40900A60 | FULL | Working data register |
| PASS0_SAR0_CH9_RESULT | 0x40900A64 | FULL | Result data register |
| PASS0_SAR0_CH9_GRP_STAT | 0x40900A68 | FULL | Group status register |
| PASS0_SAR0_CH9_ENABLE | 0x40900A78 | FULL | Enable register |
| PASS0_SAR0_CH9_TR_CMD | 0x40900A7C | FULL | Software triggers |

### 21.1.11 CH 10

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR0_CH10_TR_CTL | 0x40900A80 | FULL | Trigger control. |
| PASS0_SAR0_CH10_SAMPLE_CTL | 0x40900A84 | FULL | Sample control. |
| PASS0_SAR0_CH10_POST_CTL | 0x40900A88 | FULL | Post processing control |
| PASS0_SAR0_CH10_RANGE_CTL | 0x40900A8C | FULL | Range thresholds |
| PASS0_SAR0_CH10_INTR | 0x40900A90 | FULL | Interrupt request register. |
| PASS0_SAR0_CH10_INTR_SET | 0x40900A94 | FULL | Interrupt set request register |
| PASS0_SAR0_CH10_INTR_MASK | 0x40900A98 | FULL | Interrupt mask register. |
| PASS0_SAR0_CH10_INTR_MASKED | 0x40900A9C | FULL | Interrupt masked request register |
| PASS0_SAR0_CH10_WORK | 0x40900AA0 | FULL | Working data register |
| PASS0_SAR0_CH10_RESULT | 0x40900AA4 | FULL | Result data register |
| PASS0_SAR0_CH10_GRP_STAT | 0x40900AA8 | FULL | Group status register |
| PASS0_SAR0_CH10_ENABLE | 0x40900AB8 | FULL | Enable register |
| PASS0_SAR0_CH10_TR_CMD | 0x40900ABC | FULL | Software triggers |

### 21.1.12 CH 11

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR0_CH11_TR_CTL | 0x40900AC0 | FULL | Trigger control. |
| PASS0_SAR0_CH11_SAMPLE_CTL | 0x40900AC4 | FULL | Sample control. |
| PASS0_SAR0_CH11_POST_CTL | 0x40900AC8 | FULL | Post processing control |
| PASS0_SAR0_CH11_RANGE_CTL | 0x40900ACC | FULL | Range thresholds |
| PASS0_SAR0_CH11_INTR | 0x40900AD0 | FULL | Interrupt request register. |
| PASS0_SAR0_CH11_INTR_SET | 0x40900AD4 | FULL | Interrupt set request register |
| PASS0_SAR0_CH11_INTR_MASK | 0x40900AD8 | FULL | Interrupt mask register. |
| PASS0_SAR0_CH11_INTR_MASKED | 0x40900ADC | FULL | Interrupt masked request register |
| PASS0_SAR0_CH11_WORK | 0x40900AE0 | FULL | Working data register |
| PASS0_SAR0_CH11_RESULT | 0x40900AE4 | FULL | Result data register |
| PASS0_SAR0_CH11_GRP_STAT | 0x40900AE8 | FULL | Group status register |
| PASS0_SAR0_CH11_ENABLE | 0x40900AF8 | FULL | Enable register |
| PASS0_SAR0_CH11_TR_CMD | 0x40900AFC | FULL | Software triggers |

### 21.1.13 CH 12

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR0_CH12_TR_CTL | 0x40900B00 | FULL | Trigger control. |
| PASS0_SAR0_CH12_SAMPLE_CTL | 0x40900B04 | FULL | Sample control. |
| PASS0_SAR0_CH12_POST_CTL | 0x40900B08 | FULL | Post processing control |
| PASS0_SAR0_CH12_RANGE_CTL | 0x40900B0C | FULL | Range thresholds |
| PASS0_SAR0_CH12_INTR | 0x40900B10 | FULL | Interrupt request register. |
| PASS0_SAR0_CH12_INTR_SET | 0x40900B14 | FULL | Interrupt set request register |
| PASS0_SAR0_CH12_INTR_MASK | 0x40900B18 | FULL | Interrupt mask register. |
| PASS0_SAR0_CH12_INTR_MASKED | 0x40900B1C | FULL | Interrupt masked request register |
| PASS0_SAR0_CH12_WORK | 0x40900B20 | FULL | Working data register |
| PASS0_SAR0_CH12_RESULT | 0x40900B24 | FULL | Result data register |
| PASS0_SAR0_CH12_GRP_STAT | 0x40900B28 | FULL | Group status register |
| PASS0_SAR0_CH12_ENABLE | 0x40900B38 | FULL | Enable register |
| PASS0_SAR0_CH12_TR_CMD | 0x40900B3C | FULL | Software triggers |

### 21.1.14 CH 13

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR0_CH13_TR_CTL | 0x40900B40 | FULL | Trigger control. |
| PASS0_SAR0_CH13_SAMPLE_CTL | 0x40900B44 | FULL | Sample control. |
| PASS0_SAR0_CH13_POST_CTL | 0x40900B48 | FULL | Post processing control |
| PASS0_SAR0_CH13_RANGE_CTL | 0x40900B4C | FULL | Range thresholds |
| PASS0_SAR0_CH13_INTR | 0x40900B50 | FULL | Interrupt request register. |
| PASS0_SAR0_CH13_INTR_SET | 0x40900B54 | FULL | Interrupt set request register |
| PASS0_SAR0_CH13_INTR_MASK | 0x40900B58 | FULL | Interrupt mask register. |
| PASS0_SAR0_CH13_INTR_MASKED | 0x40900B5C | FULL | Interrupt masked request register |
| PASS0_SAR0_CH13_WORK | 0x40900B60 | FULL | Working data register |
| PASS0_SAR0_CH13_RESULT | 0x40900B64 | FULL | Result data register |
| PASS0_SAR0_CH13_GRP_STAT | 0x40900B68 | FULL | Group status register |
| PASS0_SAR0_CH13_ENABLE | 0x40900B78 | FULL | Enable register |
| PASS0_SAR0_CH13_TR_CMD | 0x40900B7C | FULL | Software triggers |

### 21.1.15 CH 14

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR0_CH14_TR_CTL | 0x40900B80 | FULL | Trigger control. |
| PASS0_SAR0_CH14_SAMPLE_CTL | 0x40900B84 | FULL | Sample control. |
| PASS0_SAR0_CH14_POST_CTL | 0x40900B88 | FULL | Post processing control |
| PASS0_SAR0_CH14_RANGE_CTL | 0x40900B8C | FULL | Range thresholds |
| PASS0_SAR0_CH14_INTR | 0x40900B90 | FULL | Interrupt request register. |
| PASS0_SAR0_CH14_INTR_SET | 0x40900B94 | FULL | Interrupt set request register |
| PASS0_SAR0_CH14_INTR_MASK | 0x40900B98 | FULL | Interrupt mask register. |
| PASS0_SAR0_CH14_INTR_MASKED | 0x40900B9C | FULL | Interrupt masked request register |
| PASS0_SAR0_CH14_WORK | 0x40900BA0 | FULL | Working data register |
| PASS0_SAR0_CH14_RESULT | 0x40900BA4 | FULL | Result data register |
| PASS0_SAR0_CH14_GRP_STAT | 0x40900BA8 | FULL | Group status register |
| PASS0_SAR0_CH14_ENABLE | 0x40900BB8 | FULL | Enable register |
| PASS0_SAR0_CH14_TR_CMD | 0x40900BBC | FULL | Software triggers |

### 21.1.16 CH 15

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR0_CH15_TR_CTL | 0x40900BC0 | FULL | Trigger control. |
| PASS0_SAR0_CH15_SAMPLE_CTL | 0x40900BC4 | FULL | Sample control. |
| PASS0_SAR0_CH15_POST_CTL | 0x40900BC8 | FULL | Post processing control |
| PASS0_SAR0_CH15_RANGE_CTL | 0x40900BCC | FULL | Range thresholds |
| PASS0_SAR0_CH15_INTR | 0x40900BD0 | FULL | Interrupt request register. |
| PASS0_SAR0_CH15_INTR_SET | 0x40900BD4 | FULL | Interrupt set request register |
| PASS0_SAR0_CH15_INTR_MASK | 0x40900BD8 | FULL | Interrupt mask register. |
| PASS0_SAR0_CH15_INTR_MASKED | 0x40900BDC | FULL | Interrupt masked request register |
| PASS0_SAR0_CH15_WORK | 0x40900BE0 | FULL | Working data register |
| PASS0_SAR0_CH15_RESULT | 0x40900BE4 | FULL | Result data register |
| PASS0_SAR0_CH15_GRP_STAT | 0x40900BE8 | FULL | Group status register |
| PASS0_SAR0_CH15_ENABLE | 0x40900BF8 | FULL | Enable register |
| PASS0_SAR0_CH15_TR_CMD | 0x40900BFC | FULL | Software triggers |

### 21.1.17 CH 16

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR0_CH16_TR_CTL | 0x40900C00 | FULL | Trigger control. |
| PASS0_SAR0_CH16_SAMPLE_CTL | 0x40900C04 | FULL | Sample control. |
| PASS0_SAR0_CH16_POST_CTL | 0x40900C08 | FULL | Post processing control |
| PASS0_SAR0_CH16_RANGE_CTL | 0x40900C0C | FULL | Range thresholds |
| PASS0_SAR0_CH16_INTR | 0x40900C10 | FULL | Interrupt request register. |
| PASS0_SAR0_CH16_INTR_SET | 0x40900C14 | FULL | Interrupt set request register |
| PASS0_SAR0_CH16_INTR_MASK | 0x40900C18 | FULL | Interrupt mask register. |
| PASS0_SAR0_CH16_INTR_MASKED | 0x40900C1C | FULL | Interrupt masked request register |
| PASS0_SAR0_CH16_WORK | 0x40900C20 | FULL | Working data register |
| PASS0_SAR0_CH16_RESULT | 0x40900C24 | FULL | Result data register |
| PASS0_SAR0_CH16_GRP_STAT | 0x40900C28 | FULL | Group status register |
| PASS0_SAR0_CH16_ENABLE | 0x40900C38 | FULL | Enable register |
| PASS0_SAR0_CH16_TR_CMD | 0x40900C3C | FULL | Software triggers |

### 21.1.18 CH 17

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR0_CH17_TR_CTL | 0x40900C40 | FULL | Trigger control. |
| PASS0_SAR0_CH17_SAMPLE_CTL | 0x40900C44 | FULL | Sample control. |
| PASS0_SAR0_CH17_POST_CTL | 0x40900C48 | FULL | Post processing control |
| PASS0_SAR0_CH17_RANGE_CTL | 0x40900C4C | FULL | Range thresholds |
| PASS0_SAR0_CH17_INTR | 0x40900C50 | FULL | Interrupt request register. |
| PASS0_SAR0_CH17_INTR_SET | 0x40900C54 | FULL | Interrupt set request register |
| PASS0_SAR0_CH17_INTR_MASK | 0x40900C58 | FULL | Interrupt mask register. |
| PASS0_SAR0_CH17_INTR_MASKED | 0x40900C5C | FULL | Interrupt masked request register |
| PASS0_SAR0_CH17_WORK | 0x40900C60 | FULL | Working data register |
| PASS0_SAR0_CH17_RESULT | 0x40900C64 | FULL | Result data register |
| PASS0_SAR0_CH17_GRP_STAT | 0x40900C68 | FULL | Group status register |
| PASS0_SAR0_CH17_ENABLE | 0x40900C78 | FULL | Enable register |
| PASS0_SAR0_CH17_TR_CMD | 0x40900C7C | FULL | Software triggers |

### 21.1.19 CH 18

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR0_CH18_TR_CTL | 0x40900C80 | FULL | Trigger control. |
| PASS0_SAR0_CH18_SAMPLE_CTL | 0x40900C84 | FULL | Sample control. |
| PASS0_SAR0_CH18_POST_CTL | 0x40900C88 | FULL | Post processing control |
| PASS0_SAR0_CH18_RANGE_CTL | 0x40900C8C | FULL | Range thresholds |
| PASS0_SAR0_CH18_INTR | 0x40900C90 | FULL | Interrupt request register. |
| PASS0_SAR0_CH18_INTR_SET | 0x40900C94 | FULL | Interrupt set request register |
| PASS0_SAR0_CH18_INTR_MASK | 0x40900C98 | FULL | Interrupt mask register. |
| PASS0_SAR0_CH18_INTR_MASKED | 0x40900C9C | FULL | Interrupt masked request register |
| PASS0_SAR0_CH18_WORK | 0x40900CA0 | FULL | Working data register |
| PASS0_SAR0_CH18_RESULT | 0x40900CA4 | FULL | Result data register |
| PASS0_SAR0_CH18_GRP_STAT | 0x40900CA8 | FULL | Group status register |
| PASS0_SAR0_CH18_ENABLE | 0x40900CB8 | FULL | Enable register |
| PASS0_SAR0_CH18_TR_CMD | 0x40900CBC | FULL | Software triggers |

### 21.1.20 CH 19

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR0_CH19_TR_CTL | 0x40900CC0 | FULL | Trigger control. |
| PASS0_SAR0_CH19_SAMPLE_CTL | 0x40900CC4 | FULL | Sample control. |
| PASS0_SAR0_CH19_POST_CTL | 0x40900CC8 | FULL | Post processing control |
| PASS0_SAR0_CH19_RANGE_CTL | 0x40900CCC | FULL | Range thresholds |
| PASS0_SAR0_CH19_INTR | 0x40900CD0 | FULL | Interrupt request register. |
| PASS0_SAR0_CH19_INTR_SET | 0x40900CD4 | FULL | Interrupt set request register |
| PASS0_SAR0_CH19_INTR_MASK | 0x40900CD8 | FULL | Interrupt mask register. |
| PASS0_SAR0_CH19_INTR_MASKED | 0x40900CDC | FULL | Interrupt masked request register |
| PASS0_SAR0_CH19_WORK | 0x40900CE0 | FULL | Working data register |
| PASS0_SAR0_CH19_RESULT | 0x40900CE4 | FULL | Result data register |
| PASS0_SAR0_CH19_GRP_STAT | 0x40900CE8 | FULL | Group status register |
| PASS0_SAR0_CH19_ENABLE | 0x40900CF8 | FULL | Enable register |
| PASS0_SAR0_CH19_TR_CMD | 0x40900CFC | FULL | Software triggers |

### 21.1.21 CH 20

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR0_CH20_TR_CTL | 0x40900D00 | FULL | Trigger control. |
| PASS0_SAR0_CH20_SAMPLE_CTL | 0x40900D04 | FULL | Sample control. |
| PASS0_SAR0_CH20_POST_CTL | 0x40900D08 | FULL | Post processing control |
| PASS0_SAR0_CH20_RANGE_CTL | 0x40900D0C | FULL | Range thresholds |
| PASS0_SAR0_CH20_INTR | 0x40900D10 | FULL | Interrupt request register. |
| PASS0_SAR0_CH20_INTR_SET | 0x40900D14 | FULL | Interrupt set request register |
| PASS0_SAR0_CH20_INTR_MASK | 0x40900D18 | FULL | Interrupt mask register. |
| PASS0_SAR0_CH20_INTR_MASKED | 0x40900D1C | FULL | Interrupt masked request register |
| PASS0_SAR0_CH20_WORK | 0x40900D20 | FULL | Working data register |
| PASS0_SAR0_CH20_RESULT | 0x40900D24 | FULL | Result data register |
| PASS0_SAR0_CH20_GRP_STAT | 0x40900D28 | FULL | Group status register |
| PASS0_SAR0_CH20_ENABLE | 0x40900D38 | FULL | Enable register |
| PASS0_SAR0_CH20_TR_CMD | 0x40900D3C | FULL | Software triggers |

### 21.1.22 CH 21

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR0_CH21_TR_CTL | 0x40900D40 | FULL | Trigger control. |
| PASS0_SAR0_CH21_SAMPLE_CTL | 0x40900D44 | FULL | Sample control. |
| PASS0_SAR0_CH21_POST_CTL | 0x40900D48 | FULL | Post processing control |
| PASS0_SAR0_CH21_RANGE_CTL | 0x40900D4C | FULL | Range thresholds |
| PASS0_SAR0_CH21_INTR | 0x40900D50 | FULL | Interrupt request register. |
| PASS0_SAR0_CH21_INTR_SET | 0x40900D54 | FULL | Interrupt set request register |
| PASS0_SAR0_CH21_INTR_MASK | 0x40900D58 | FULL | Interrupt mask register. |
| PASS0_SAR0_CH21_INTR_MASKED | 0x40900D5C | FULL | Interrupt masked request register |
| PASS0_SAR0_CH21_WORK | 0x40900D60 | FULL | Working data register |
| PASS0_SAR0_CH21_RESULT | 0x40900D64 | FULL | Result data register |
| PASS0_SAR0_CH21_GRP_STAT | 0x40900D68 | FULL | Group status register |
| PASS0_SAR0_CH21_ENABLE | 0x40900D78 | FULL | Enable register |
| PASS0_SAR0_CH21_TR_CMD | 0x40900D7C | FULL | Software triggers |

### 21.1.23 CH 22

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR0_CH22_TR_CTL | 0x40900D80 | FULL | Trigger control. |
| PASS0_SAR0_CH22_SAMPLE_CTL | 0x40900D84 | FULL | Sample control. |
| PASS0_SAR0_CH22_POST_CTL | 0x40900D88 | FULL | Post processing control |
| PASS0_SAR0_CH22_RANGE_CTL | 0x40900D8C | FULL | Range thresholds |
| PASS0_SAR0_CH22_INTR | 0x40900D90 | FULL | Interrupt request register. |
| PASS0_SAR0_CH22_INTR_SET | 0x40900D94 | FULL | Interrupt set request register |
| PASS0_SAR0_CH22_INTR_MASK | 0x40900D98 | FULL | Interrupt mask register. |
| PASS0_SAR0_CH22_INTR_MASKED | 0x40900D9C | FULL | Interrupt masked request register |
| PASS0_SAR0_CH22_WORK | 0x40900DA0 | FULL | Working data register |
| PASS0_SAR0_CH22_RESULT | 0x40900DA4 | FULL | Result data register |
| PASS0_SAR0_CH22_GRP_STAT | 0x40900DA8 | FULL | Group status register |
| PASS0_SAR0_CH22_ENABLE | 0x40900DB8 | FULL | Enable register |
| PASS0_SAR0_CH22_TR_CMD | 0x40900DBC | FULL | Software triggers |

### 21.1.24 CH 23

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR0_CH23_TR_CTL | 0x40900DC0 | FULL | Trigger control. |
| PASS0_SAR0_CH23_SAMPLE_CTL | 0x40900DC4 | FULL | Sample control. |
| PASS0_SAR0_CH23_POST_CTL | 0x40900DC8 | FULL | Post processing control |
| PASS0_SAR0_CH23_RANGE_CTL | 0x40900DCC | FULL | Range thresholds |
| PASS0_SAR0_CH23_INTR | 0x40900DD0 | FULL | Interrupt request register. |
| PASS0_SAR0_CH23_INTR_SET | 0x40900DD4 | FULL | Interrupt set request register |
| PASS0_SAR0_CH23_INTR_MASK | 0x40900DD8 | FULL | Interrupt mask register. |
| PASS0_SAR0_CH23_INTR_MASKED | 0x40900DDC | FULL | Interrupt masked request register |
| PASS0_SAR0_CH23_WORK | 0x40900DE0 | FULL | Working data register |
| PASS0_SAR0_CH23_RESULT | 0x40900DE4 | FULL | Result data register |
| PASS0_SAR0_CH23_GRP_STAT | 0x40900DE8 | FULL | Group status register |
| PASS0_SAR0_CH23_ENABLE | 0x40900DF8 | FULL | Enable register |
| PASS0_SAR0_CH23_TR_CMD | 0x40900DFC | FULL | Software triggers |

### 21.1.25 CH 24

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR0_CH24_TR_CTL | 0x40900E00 | FULL | Trigger control. |
| PASS0_SAR0_CH24_SAMPLE_CTL | 0x40900E04 | FULL | Sample control. |
| PASS0_SAR0_CH24_POST_CTL | 0x40900E08 | FULL | Post processing control |
| PASS0_SAR0_CH24_RANGE_CTL | 0x40900E0C | FULL | Range thresholds |
| PASS0_SAR0_CH24_INTR | 0x40900E10 | FULL | Interrupt request register. |
| PASS0_SAR0_CH24_INTR_SET | 0x40900E14 | FULL | Interrupt set request register |
| PASS0_SAR0_CH24_INTR_MASK | 0x40900E18 | FULL | Interrupt mask register. |
| PASS0_SAR0_CH24_INTR_MASKED | 0x40900E1C | FULL | Interrupt masked request register |
| PASS0_SAR0_CH24_WORK | 0x40900E20 | FULL | Working data register |
| PASS0_SAR0_CH24_RESULT | 0x40900E24 | FULL | Result data register |
| PASS0_SAR0_CH24_GRP_STAT | 0x40900E28 | FULL | Group status register |
| PASS0_SAR0_CH24_ENABLE | 0x40900E38 | FULL | Enable register |
| PASS0_SAR0_CH24_TR_CMD | 0x40900E3C | FULL | Software triggers |

### 21.1.26 CH 25

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR0_CH25_TR_CTL | 0x40900E40 | FULL | Trigger control. |
| PASS0_SAR0_CH25_SAMPLE_CTL | 0x40900E44 | FULL | Sample control. |
| PASS0_SAR0_CH25_POST_CTL | 0x40900E48 | FULL | Post processing control |
| PASS0_SAR0_CH25_RANGE_CTL | 0x40900E4C | FULL | Range thresholds |
| PASS0_SAR0_CH25_INTR | 0x40900E50 | FULL | Interrupt request register. |
| PASS0_SAR0_CH25_INTR_SET | 0x40900E54 | FULL | Interrupt set request register |
| PASS0_SAR0_CH25_INTR_MASK | 0x40900E58 | FULL | Interrupt mask register. |
| PASS0_SAR0_CH25_INTR_MASKED | 0x40900E5C | FULL | Interrupt masked request register |
| PASS0_SAR0_CH25_WORK | 0x40900E60 | FULL | Working data register |
| PASS0_SAR0_CH25_RESULT | 0x40900E64 | FULL | Result data register |
| PASS0_SAR0_CH25_GRP_STAT | 0x40900E68 | FULL | Group status register |
| PASS0_SAR0_CH25_ENABLE | 0x40900E78 | FULL | Enable register |
| PASS0_SAR0_CH25_TR_CMD | 0x40900E7C | FULL | Software triggers |

### 21.1.27 CH 26

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR0_CH26_TR_CTL | 0x40900E80 | FULL | Trigger control. |
| PASS0_SAR0_CH26_SAMPLE_CTL | 0x40900E84 | FULL | Sample control. |
| PASS0_SAR0_CH26_POST_CTL | 0x40900E88 | FULL | Post processing control |
| PASS0_SAR0_CH26_RANGE_CTL | 0x40900E8C | FULL | Range thresholds |
| PASS0_SAR0_CH26_INTR | 0x40900E90 | FULL | Interrupt request register. |
| PASS0_SAR0_CH26_INTR_SET | 0x40900E94 | FULL | Interrupt set request register |
| PASS0_SAR0_CH26_INTR_MASK | 0x40900E98 | FULL | Interrupt mask register. |
| PASS0_SAR0_CH26_INTR_MASKED | 0x40900E9C | FULL | Interrupt masked request register |
| PASS0_SAR0_CH26_WORK | 0x40900EA0 | FULL | Working data register |
| PASS0_SAR0_CH26_RESULT | 0x40900EA4 | FULL | Result data register |
| PASS0_SAR0_CH26_GRP_STAT | 0x40900EA8 | FULL | Group status register |
| PASS0_SAR0_CH26_ENABLE | 0x40900EB8 | FULL | Enable register |
| PASS0_SAR0_CH26_TR_CMD | 0x40900EBC | FULL | Software triggers |

### 21.1.28 CH 27

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR0_CH27_TR_CTL | 0x40900EC0 | FULL | Trigger control. |
| PASS0_SAR0_CH27_SAMPLE_CTL | 0x40900EC4 | FULL | Sample control. |
| PASS0_SAR0_CH27_POST_CTL | 0x40900EC8 | FULL | Post processing control |
| PASS0_SAR0_CH27_RANGE_CTL | 0x40900ECC | FULL | Range thresholds |
| PASS0_SAR0_CH27_INTR | 0x40900ED0 | FULL | Interrupt request register. |
| PASS0_SAR0_CH27_INTR_SET | 0x40900ED4 | FULL | Interrupt set request register |
| PASS0_SAR0_CH27_INTR_MASK | 0x40900ED8 | FULL | Interrupt mask register. |
| PASS0_SAR0_CH27_INTR_MASKED | 0x40900EDC | FULL | Interrupt masked request register |
| PASS0_SAR0_CH27_WORK | 0x40900EE0 | FULL | Working data register |
| PASS0_SAR0_CH27_RESULT | 0x40900EE4 | FULL | Result data register |
| PASS0_SAR0_CH27_GRP_STAT | 0x40900EE8 | FULL | Group status register |
| PASS0_SAR0_CH27_ENABLE | 0x40900EF8 | FULL | Enable register |
| PASS0_SAR0_CH27_TR_CMD | 0x40900EFC | FULL | Software triggers |

### 21.1.29 CH 28

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR0_CH28_TR_CTL | 0x40900F00 | FULL | Trigger control. |
| PASS0_SAR0_CH28_SAMPLE_CTL | 0x40900F04 | FULL | Sample control. |
| PASS0_SAR0_CH28_POST_CTL | 0x40900F08 | FULL | Post processing control |
| PASS0_SAR0_CH28_RANGE_CTL | 0x40900F0C | FULL | Range thresholds |
| PASS0_SAR0_CH28_INTR | 0x40900F10 | FULL | Interrupt request register. |
| PASS0_SAR0_CH28_INTR_SET | 0x40900F14 | FULL | Interrupt set request register |
| PASS0_SAR0_CH28_INTR_MASK | 0x40900F18 | FULL | Interrupt mask register. |
| PASS0_SAR0_CH28_INTR_MASKED | 0x40900F1C | FULL | Interrupt masked request register |
| PASS0_SAR0_CH28_WORK | 0x40900F20 | FULL | Working data register |
| PASS0_SAR0_CH28_RESULT | 0x40900F24 | FULL | Result data register |
| PASS0_SAR0_CH28_GRP_STAT | 0x40900F28 | FULL | Group status register |
| PASS0_SAR0_CH28_ENABLE | 0x40900F38 | FULL | Enable register |
| PASS0_SAR0_CH28_TR_CMD | 0x40900F3C | FULL | Software triggers |

### 21.1.30 CH 29

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR0_CH29_TR_CTL | 0x40900F40 | FULL | Trigger control. |
| PASS0_SAR0_CH29_SAMPLE_CTL | 0x40900F44 | FULL | Sample control. |
| PASS0_SAR0_CH29_POST_CTL | 0x40900F48 | FULL | Post processing control |
| PASS0_SAR0_CH29_RANGE_CTL | 0x40900F4C | FULL | Range thresholds |
| PASS0_SAR0_CH29_INTR | 0x40900F50 | FULL | Interrupt request register. |
| PASS0_SAR0_CH29_INTR_SET | 0x40900F54 | FULL | Interrupt set request register |
| PASS0_SAR0_CH29_INTR_MASK | 0x40900F58 | FULL | Interrupt mask register. |
| PASS0_SAR0_CH29_INTR_MASKED | 0x40900F5C | FULL | Interrupt masked request register |
| PASS0_SAR0_CH29_WORK | 0x40900F60 | FULL | Working data register |
| PASS0_SAR0_CH29_RESULT | 0x40900F64 | FULL | Result data register |
| PASS0_SAR0_CH29_GRP_STAT | 0x40900F68 | FULL | Group status register |
| PASS0_SAR0_CH29_ENABLE | 0x40900F78 | FULL | Enable register |
| PASS0_SAR0_CH29_TR_CMD | 0x40900F7C | FULL | Software triggers |

### 21.1.31 CH 30

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR0_CH30_TR_CTL | 0x40900F80 | FULL | Trigger control. |
| PASS0_SAR0_CH30_SAMPLE_CTL | 0x40900F84 | FULL | Sample control. |
| PASS0_SAR0_CH30_POST_CTL | 0x40900F88 | FULL | Post processing control |
| PASS0_SAR0_CH30_RANGE_CTL | 0x40900F8C | FULL | Range thresholds |
| PASS0_SAR0_CH30_INTR | 0x40900F90 | FULL | Interrupt request register. |
| PASS0_SAR0_CH30_INTR_SET | 0x40900F94 | FULL | Interrupt set request register |
| PASS0_SAR0_CH30_INTR_MASK | 0x40900F98 | FULL | Interrupt mask register. |
| PASS0_SAR0_CH30_INTR_MASKED | 0x40900F9C | FULL | Interrupt masked request register |
| PASS0_SAR0_CH30_WORK | 0x40900FA0 | FULL | Working data register |
| PASS0_SAR0_CH30_RESULT | 0x40900FA4 | FULL | Result data register |
| PASS0_SAR0_CH30_GRP_STAT | 0x40900FA8 | FULL | Group status register |
| PASS0_SAR0_CH30_ENABLE | 0x40900FB8 | FULL | Enable register |
| PASS0_SAR0_CH30_TR_CMD | 0x40900FBC | FULL | Software triggers |

### 21.1.32 CH 31

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR0_CH31_TR_CTL | 0x40900FC0 | FULL | Trigger control. |
| PASS0_SAR0_CH31_SAMPLE_CTL | 0x40900FC4 | FULL | Sample control. |
| PASS0_SAR0_CH31_POST_CTL | 0x40900FC8 | FULL | Post processing control |
| PASS0_SAR0_CH31_RANGE_CTL | 0x40900FCC | FULL | Range thresholds |
| PASS0_SAR0_CH31_INTR | 0x40900FD0 | FULL | Interrupt request register. |
| PASS0_SAR0_CH31_INTR_SET | 0x40900FD4 | FULL | Interrupt set request register |
| PASS0_SAR0_CH31_INTR_MASK | 0x40900FD8 | FULL | Interrupt mask register. |
| PASS0_SAR0_CH31_INTR_MASKED | 0x40900FDC | FULL | Interrupt masked request register |
| PASS0_SAR0_CH31_WORK | 0x40900FE0 | FULL | Working data register |
| PASS0_SAR0_CH31_RESULT | 0x40900FE4 | FULL | Result data register |
| PASS0_SAR0_CH31_GRP_STAT | 0x40900FE8 | FULL | Group status register |
| PASS0_SAR0_CH31_ENABLE | 0x40900FF8 | FULL | Enable register |
| PASS0_SAR0_CH31_TR_CMD | 0x40900FFC | FULL | Software triggers |

## 21.2 SAR 1

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR1_CTL | 0x40901000 | FULL | Analog control register. |
| PASS0_SAR1_DIAG_CTL | 0x40901004 | FULL | Diagnostic Reference control register. |
| PASS0_SAR1_PRECOND_CTL | 0x40901010 | FULL | Preconditioning control register. |
| PASS0_SAR1_ANA_CAL | 0x40901080 | FULL | Current analog calibration values |
| PASS0_SAR1_DIG_CAL | 0x40901084 | FULL | Current digital calibration values |
| PASS0_SAR1_ANA_CAL_ALT | 0x40901090 | FULL | Alternate analog calibration values |
| PASS0_SAR1_DIG_CAL_ALT | 0x40901094 | FULL | Alternate digital calibration values |
| PASS0_SAR1_CAL_UPD_CMD | 0x40901098 | FULL | Calibration update command |
| PASS0_SAR1_TR_PEND | 0x40901100 | FULL | Trigger pending status |
| PASS0_SAR1_WORK_VALID | 0x40901180 | FULL | Channel working data register 'valid' bits |
| PASS0_SAR1_WORK_RANGE | 0x40901184 | FULL | Range detected |
| PASS0_SAR1_WORK_RANGE_HI | 0x40901188 | FULL | Range detect above Hi flag |
| PASS0_SAR1_WORK_PULSE | 0x4090118C | FULL | Pulse detected |
| PASS0_SAR1_RESULT_VALID | 0x409011A0 | FULL | Channel result data register 'valid' bits |
| PASS0_SAR1_RESULT_RANGE_HI | 0x409011A4 | FULL | Channel Range above Hi flags |
| PASS0_SAR1_STATUS | 0x40901200 | FULL | Current status of internal SAR registers (mostly for debug) |
| PASS0_SAR1_AVG_STAT | 0x40901204 | FULL | Current averaging status (for debug) |

### 21.2.1 CH 0

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR1_CH0_TR_CTL | 0x40901800 | FULL | Trigger control. |
| PASS0_SAR1_CH0_SAMPLE_CTL | 0x40901804 | FULL | Sample control. |
| PASS0_SAR1_CH0_POST_CTL | 0x40901808 | FULL | Post processing control |
| PASS0_SAR1_CH0_RANGE_CTL | 0x4090180C | FULL | Range thresholds |
| PASS0_SAR1_CH0_INTR | 0x40901810 | FULL | Interrupt request register. |
| PASS0_SAR1_CH0_INTR_SET | 0x40901814 | FULL | Interrupt set request register |
| PASS0_SAR1_CH0_INTR_MASK | 0x40901818 | FULL | Interrupt mask register. |
| PASS0_SAR1_CH0_INTR_MASKED | 0x4090181C | FULL | Interrupt masked request register |
| PASS0_SAR1_CH0_WORK | 0x40901820 | FULL | Working data register |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR1_CH0_RESULT | 0x40901824 | FULL | Result data register |
| PASS0_SAR1_CH0_GRP_STAT | 0x40901828 | FULL | Group status register |
| PASS0_SAR1_CH0_ENABLE | 0x40901838 | FULL | Enable register |
| PASS0_SAR1_CH0_TR_CMD | 0x4090183C | FULL | Software triggers |

### 21.2.2 CH 1

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR1_CH1_TR_CTL | 0x40901840 | FULL | Trigger control. |
| PASS0_SAR1_CH1_SAMPLE_CTL | 0x40901844 | FULL | Sample control. |
| PASS0_SAR1_CH1_POST_CTL | 0x40901848 | FULL | Post processing control |
| PASS0_SAR1_CH1_RANGE_CTL | 0x4090184C | FULL | Range thresholds |
| PASS0_SAR1_CH1_INTR | 0x40901850 | FULL | Interrupt request register. |
| PASS0_SAR1_CH1_INTR_SET | 0x40901854 | FULL | Interrupt set request register |
| PASS0_SAR1_CH1_INTR_MASK | 0x40901858 | FULL | Interrupt mask register. |
| PASS0_SAR1_CH1_INTR_MASKED | 0x4090185C | FULL | Interrupt masked request register |
| PASS0_SAR1_CH1_WORK | 0x40901860 | FULL | Working data register |
| PASS0_SAR1_CH1_RESULT | 0x40901864 | FULL | Result data register |
| PASS0_SAR1_CH1_GRP_STAT | 0x40901868 | FULL | Group status register |
| PASS0_SAR1_CH1_ENABLE | 0x40901878 | FULL | Enable register |
| PASS0_SAR1_CH1_TR_CMD | 0x4090187C | FULL | Software triggers |

### 21.2.3 CH 2

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR1_CH2_TR_CTL | 0x40901880 | FULL | Trigger control. |
| PASS0_SAR1_CH2_SAMPLE_CTL | 0x40901884 | FULL | Sample control. |
| PASS0_SAR1_CH2_POST_CTL | 0x40901888 | FULL | Post processing control |
| PASS0_SAR1_CH2_RANGE_CTL | 0x4090188C | FULL | Range thresholds |
| PASS0_SAR1_CH2_INTR | 0x40901890 | FULL | Interrupt request register. |
| PASS0_SAR1_CH2_INTR_SET | 0x40901894 | FULL | Interrupt set request register |
| PASS0_SAR1_CH2_INTR_MASK | 0x40901898 | FULL | Interrupt mask register. |
| PASS0_SAR1_CH2_INTR_MASKED | 0x4090189C | FULL | Interrupt masked request register |
| PASS0_SAR1_CH2_WORK | 0x409018A0 | FULL | Working data register |
| PASS0_SAR1_CH2_RESULT | 0x409018A4 | FULL | Result data register |
| PASS0_SAR1_CH2_GRP_STAT | 0x409018A8 | FULL | Group status register |
| PASS0_SAR1_CH2_ENABLE | 0x409018B8 | FULL | Enable register |
| PASS0_SAR1_CH2_TR_CMD | 0x409018BC | FULL | Software triggers |

### 21.2.4 CH 3

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR1_CH3_TR_CTL | 0x409018C0 | FULL | Trigger control. |
| PASS0_SAR1_CH3_SAMPLE_CTL | 0x409018C4 | FULL | Sample control. |
| PASS0_SAR1_CH3_POST_CTL | 0x409018C8 | FULL | Post processing control |
| PASS0_SAR1_CH3_RANGE_CTL | 0x409018CC | FULL | Range thresholds |
| PASS0_SAR1_CH3_INTR | 0x409018D0 | FULL | Interrupt request register. |
| PASS0_SAR1_CH3_INTR_SET | 0x409018D4 | FULL | Interrupt set request register |
| PASS0_SAR1_CH3_INTR_MASK | 0x409018D8 | FULL | Interrupt mask register. |
| PASS0_SAR1_CH3_INTR_MASKED | 0x409018DC | FULL | Interrupt masked request register |
| PASS0_SAR1_CH3_WORK | 0x409018E0 | FULL | Working data register |
| PASS0_SAR1_CH3_RESULT | 0x409018E4 | FULL | Result data register |
| PASS0_SAR1_CH3_GRP_STAT | 0x409018E8 | FULL | Group status register |
| PASS0_SAR1_CH3_ENABLE | 0x409018F8 | FULL | Enable register |
| PASS0_SAR1_CH3_TR_CMD | 0x409018FC | FULL | Software triggers |

### 21.2.5 CH 4

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR1_CH4_TR_CTL | 0x40901900 | FULL | Trigger control. |
| PASS0_SAR1_CH4_SAMPLE_CTL | 0x40901904 | FULL | Sample control. |
| PASS0_SAR1_CH4_POST_CTL | 0x40901908 | FULL | Post processing control |
| PASS0_SAR1_CH4_RANGE_CTL | 0x4090190C | FULL | Range thresholds |
| PASS0_SAR1_CH4_INTR | 0x40901910 | FULL | Interrupt request register. |
| PASS0_SAR1_CH4_INTR_SET | 0x40901914 | FULL | Interrupt set request register |
| PASS0_SAR1_CH4_INTR_MASK | 0x40901918 | FULL | Interrupt mask register. |
| PASS0_SAR1_CH4_INTR_MASKED | 0x4090191C | FULL | Interrupt masked request register |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR1_CH4_WORK | 0x40901920 | FULL | Working data register |
| PASS0_SAR1_CH4_RESULT | 0x40901924 | FULL | Result data register |
| PASS0_SAR1_CH4_GRP_STAT | 0x40901928 | FULL | Group status register |
| PASS0_SAR1_CH4_ENABLE | 0x40901938 | FULL | Enable register |
| PASS0_SAR1_CH4_TR_CMD | 0x4090193C | FULL | Software triggers |

### 21.2.6 CH 5

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR1_CH5_TR_CTL | 0x40901940 | FULL | Trigger control. |
| PASS0_SAR1_CH5_SAMPLE_CTL | 0x40901944 | FULL | Sample control. |
| PASS0_SAR1_CH5_POST_CTL | 0x40901948 | FULL | Post processing control |
| PASS0_SAR1_CH5_RANGE_CTL | 0x4090194C | FULL | Range thresholds |
| PASS0_SAR1_CH5_INTR | 0x40901950 | FULL | Interrupt request register. |
| PASS0_SAR1_CH5_INTR_SET | 0x40901954 | FULL | Interrupt set request register |
| PASS0_SAR1_CH5_INTR_MASK | 0x40901958 | FULL | Interrupt mask register. |
| PASS0_SAR1_CH5_INTR_MASKED | 0x4090195C | FULL | Interrupt masked request register |
| PASS0_SAR1_CH5_WORK | 0x40901960 | FULL | Working data register |
| PASS0_SAR1_CH5_RESULT | 0x40901964 | FULL | Result data register |
| PASS0_SAR1_CH5_GRP_STAT | 0x40901968 | FULL | Group status register |
| PASS0_SAR1_CH5_ENABLE | 0x40901978 | FULL | Enable register |
| PASS0_SAR1_CH5_TR_CMD | 0x4090197C | FULL | Software triggers |

### 21.2.7 CH 6

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR1_CH6_TR_CTL | 0x40901980 | FULL | Trigger control. |
| PASS0_SAR1_CH6_SAMPLE_CTL | 0x40901984 | FULL | Sample control. |
| PASS0_SAR1_CH6_POST_CTL | 0x40901988 | FULL | Post processing control |
| PASS0_SAR1_CH6_RANGE_CTL | 0x4090198C | FULL | Range thresholds |
| PASS0_SAR1_CH6_INTR | 0x40901990 | FULL | Interrupt request register. |
| PASS0_SAR1_CH6_INTR_SET | 0x40901994 | FULL | Interrupt set request register |
| PASS0_SAR1_CH6_INTR_MASK | 0x40901998 | FULL | Interrupt mask register. |
| PASS0_SAR1_CH6_INTR_MASKED | 0x4090199C | FULL | Interrupt masked request register |
| PASS0_SAR1_CH6_WORK | 0x409019A0 | FULL | Working data register |
| PASS0_SAR1_CH6_RESULT | 0x409019A4 | FULL | Result data register |
| PASS0_SAR1_CH6_GRP_STAT | 0x409019A8 | FULL | Group status register |
| PASS0_SAR1_CH6_ENABLE | 0x409019B8 | FULL | Enable register |
| PASS0_SAR1_CH6_TR_CMD | 0x409019BC | FULL | Software triggers |

### 21.2.8 CH 7

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR1_CH7_TR_CTL | 0x409019C0 | FULL | Trigger control. |
| PASS0_SAR1_CH7_SAMPLE_CTL | 0x409019C4 | FULL | Sample control. |
| PASS0_SAR1_CH7_POST_CTL | 0x409019C8 | FULL | Post processing control |
| PASS0_SAR1_CH7_RANGE_CTL | 0x409019CC | FULL | Range thresholds |
| PASS0_SAR1_CH7_INTR | 0x409019D0 | FULL | Interrupt request register. |
| PASS0_SAR1_CH7_INTR_SET | 0x409019D4 | FULL | Interrupt set request register |
| PASS0_SAR1_CH7_INTR_MASK | 0x409019D8 | FULL | Interrupt mask register. |
| PASS0_SAR1_CH7_INTR_MASKED | 0x409019DC | FULL | Interrupt masked request register |
| PASS0_SAR1_CH7_WORK | 0x409019E0 | FULL | Working data register |
| PASS0_SAR1_CH7_RESULT | 0x409019E4 | FULL | Result data register |
| PASS0_SAR1_CH7_GRP_STAT | 0x409019E8 | FULL | Group status register |
| PASS0_SAR1_CH7_ENABLE | 0x409019F8 | FULL | Enable register |
| PASS0_SAR1_CH7_TR_CMD | 0x409019FC | FULL | Software triggers |

### 21.2.9 CH 8

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR1_CH8_TR_CTL | 0x40901A00 | FULL | Trigger control. |
| PASS0_SAR1_CH8_SAMPLE_CTL | 0x40901A04 | FULL | Sample control. |
| PASS0_SAR1_CH8_POST_CTL | 0x40901A08 | FULL | Post processing control |
| PASS0_SAR1_CH8_RANGE_CTL | 0x40901A0C | FULL | Range thresholds |
| PASS0_SAR1_CH8_INTR | 0x40901A10 | FULL | Interrupt request register. |
| PASS0_SAR1_CH8_INTR_SET | 0x40901A14 | FULL | Interrupt set request register |
| PASS0_SAR1_CH8_INTR_MASK | 0x40901A18 | FULL | Interrupt mask register. |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR1_CH8_INTR_MASKED | 0x40901A1C | FULL | Interrupt masked request register |
| PASS0_SAR1_CH8_WORK | 0x40901A20 | FULL | Working data register |
| PASS0_SAR1_CH8_RESULT | 0x40901A24 | FULL | Result data register |
| PASS0_SAR1_CH8_GRP_STAT | 0x40901A28 | FULL | Group status register |
| PASS0_SAR1_CH8_ENABLE | 0x40901A38 | FULL | Enable register |
| PASS0_SAR1_CH8_TR_CMD | 0x40901A3C | FULL | Software triggers |

### 21.2.10 CH 9

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR1_CH9_TR_CTL | 0x40901A40 | FULL | Trigger control. |
| PASS0_SAR1_CH9_SAMPLE_CTL | 0x40901A44 | FULL | Sample control. |
| PASS0_SAR1_CH9_POST_CTL | 0x40901A48 | FULL | Post processing control |
| PASS0_SAR1_CH9_RANGE_CTL | 0x40901A4C | FULL | Range thresholds |
| PASS0_SAR1_CH9_INTR | 0x40901A50 | FULL | Interrupt request register. |
| PASS0_SAR1_CH9_INTR_SET | 0x40901A54 | FULL | Interrupt set request register |
| PASS0_SAR1_CH9_INTR_MASK | 0x40901A58 | FULL | Interrupt mask register. |
| PASS0_SAR1_CH9_INTR_MASKED | 0x40901A5C | FULL | Interrupt masked request register |
| PASS0_SAR1_CH9_WORK | 0x40901A60 | FULL | Working data register |
| PASS0_SAR1_CH9_RESULT | 0x40901A64 | FULL | Result data register |
| PASS0_SAR1_CH9_GRP_STAT | 0x40901A68 | FULL | Group status register |
| PASS0_SAR1_CH9_ENABLE | 0x40901A78 | FULL | Enable register |
| PASS0_SAR1_CH9_TR_CMD | 0x40901A7C | FULL | Software triggers |

### 21.2.11 CH 10

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR1_CH10_TR_CTL | 0x40901A80 | FULL | Trigger control. |
| PASS0_SAR1_CH10_SAMPLE_CTL | 0x40901A84 | FULL | Sample control. |
| PASS0_SAR1_CH10_POST_CTL | 0x40901A88 | FULL | Post processing control |
| PASS0_SAR1_CH10_RANGE_CTL | 0x40901A8C | FULL | Range thresholds |
| PASS0_SAR1_CH10_INTR | 0x40901A90 | FULL | Interrupt request register. |
| PASS0_SAR1_CH10_INTR_SET | 0x40901A94 | FULL | Interrupt set request register |
| PASS0_SAR1_CH10_INTR_MASK | 0x40901A98 | FULL | Interrupt mask register. |
| PASS0_SAR1_CH10_INTR_MASKED | 0x40901A9C | FULL | Interrupt masked request register |
| PASS0_SAR1_CH10_WORK | 0x40901AA0 | FULL | Working data register |
| PASS0_SAR1_CH10_RESULT | 0x40901AA4 | FULL | Result data register |
| PASS0_SAR1_CH10_GRP_STAT | 0x40901AA8 | FULL | Group status register |
| PASS0_SAR1_CH10_ENABLE | 0x40901AB8 | FULL | Enable register |
| PASS0_SAR1_CH10_TR_CMD | 0x40901ABC | FULL | Software triggers |

### 21.2.12 CH 11

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR1_CH11_TR_CTL | 0x40901AC0 | FULL | Trigger control. |
| PASS0_SAR1_CH11_SAMPLE_CTL | 0x40901AC4 | FULL | Sample control. |
| PASS0_SAR1_CH11_POST_CTL | 0x40901AC8 | FULL | Post processing control |
| PASS0_SAR1_CH11_RANGE_CTL | 0x40901ACC | FULL | Range thresholds |
| PASS0_SAR1_CH11_INTR | 0x40901AD0 | FULL | Interrupt request register. |
| PASS0_SAR1_CH11_INTR_SET | 0x40901AD4 | FULL | Interrupt set request register |
| PASS0_SAR1_CH11_INTR_MASK | 0x40901AD8 | FULL | Interrupt mask register. |
| PASS0_SAR1_CH11_INTR_MASKED | 0x40901ADC | FULL | Interrupt masked request register |
| PASS0_SAR1_CH11_WORK | 0x40901AE0 | FULL | Working data register |
| PASS0_SAR1_CH11_RESULT | 0x40901AE4 | FULL | Result data register |
| PASS0_SAR1_CH11_GRP_STAT | 0x40901AE8 | FULL | Group status register |
| PASS0_SAR1_CH11_ENABLE | 0x40901AF8 | FULL | Enable register |
| PASS0_SAR1_CH11_TR_CMD | 0x40901AFC | FULL | Software triggers |

### 21.2.13 CH 12

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR1_CH12_TR_CTL | 0x40901B00 | FULL | Trigger control. |
| PASS0_SAR1_CH12_SAMPLE_CTL | 0x40901B04 | FULL | Sample control. |
| PASS0_SAR1_CH12_POST_CTL | 0x40901B08 | FULL | Post processing control |
| PASS0_SAR1_CH12_RANGE_CTL | 0x40901B0C | FULL | Range thresholds |
| PASS0_SAR1_CH12_INTR | 0x40901B10 | FULL | Interrupt request register. |
| PASS0_SAR1_CH12_INTR_SET | 0x40901B14 | FULL | Interrupt set request register |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR1_CH12_INTR_MASK | 0x40901B18 | FULL | Interrupt mask register. |
| PASS0_SAR1_CH12_INTR_MASKED | 0x40901B1C | FULL | Interrupt masked request register |
| PASS0_SAR1_CH12_WORK | 0x40901B20 | FULL | Working data register |
| PASS0_SAR1_CH12_RESULT | 0x40901B24 | FULL | Result data register |
| PASS0_SAR1_CH12_GRP_STAT | 0x40901B28 | FULL | Group status register |
| PASS0_SAR1_CH12_ENABLE | 0x40901B38 | FULL | Enable register |
| PASS0_SAR1_CH12_TR_CMD | 0x40901B3C | FULL | Software triggers |

### 21.2.14 CH 13

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR1_CH13_TR_CTL | 0x40901B40 | FULL | Trigger control. |
| PASS0_SAR1_CH13_SAMPLE_CTL | 0x40901B44 | FULL | Sample control. |
| PASS0_SAR1_CH13_POST_CTL | 0x40901B48 | FULL | Post processing control |
| PASS0_SAR1_CH13_RANGE_CTL | 0x40901B4C | FULL | Range thresholds |
| PASS0_SAR1_CH13_INTR | 0x40901B50 | FULL | Interrupt request register. |
| PASS0_SAR1_CH13_INTR_SET | 0x40901B54 | FULL | Interrupt set request register |
| PASS0_SAR1_CH13_INTR_MASK | 0x40901B58 | FULL | Interrupt mask register. |
| PASS0_SAR1_CH13_INTR_MASKED | 0x40901B5C | FULL | Interrupt masked request register |
| PASS0_SAR1_CH13_WORK | 0x40901B60 | FULL | Working data register |
| PASS0_SAR1_CH13_RESULT | 0x40901B64 | FULL | Result data register |
| PASS0_SAR1_CH13_GRP_STAT | 0x40901B68 | FULL | Group status register |
| PASS0_SAR1_CH13_ENABLE | 0x40901B78 | FULL | Enable register |
| PASS0_SAR1_CH13_TR_CMD | 0x40901B7C | FULL | Software triggers |

### 21.2.15 CH 14

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR1_CH14_TR_CTL | 0x40901B80 | FULL | Trigger control. |
| PASS0_SAR1_CH14_SAMPLE_CTL | 0x40901B84 | FULL | Sample control. |
| PASS0_SAR1_CH14_POST_CTL | 0x40901B88 | FULL | Post processing control |
| PASS0_SAR1_CH14_RANGE_CTL | 0x40901B8C | FULL | Range thresholds |
| PASS0_SAR1_CH14_INTR | 0x40901B90 | FULL | Interrupt request register. |
| PASS0_SAR1_CH14_INTR_SET | 0x40901B94 | FULL | Interrupt set request register |
| PASS0_SAR1_CH14_INTR_MASK | 0x40901B98 | FULL | Interrupt mask register. |
| PASS0_SAR1_CH14_INTR_MASKED | 0x40901B9C | FULL | Interrupt masked request register |
| PASS0_SAR1_CH14_WORK | 0x40901BA0 | FULL | Working data register |
| PASS0_SAR1_CH14_RESULT | 0x40901BA4 | FULL | Result data register |
| PASS0_SAR1_CH14_GRP_STAT | 0x40901BA8 | FULL | Group status register |
| PASS0_SAR1_CH14_ENABLE | 0x40901BB8 | FULL | Enable register |
| PASS0_SAR1_CH14_TR_CMD | 0x40901BBC | FULL | Software triggers |

### 21.2.16 CH 15

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR1_CH15_TR_CTL | 0x40901BC0 | FULL | Trigger control. |
| PASS0_SAR1_CH15_SAMPLE_CTL | 0x40901BC4 | FULL | Sample control. |
| PASS0_SAR1_CH15_POST_CTL | 0x40901BC8 | FULL | Post processing control |
| PASS0_SAR1_CH15_RANGE_CTL | 0x40901BCC | FULL | Range thresholds |
| PASS0_SAR1_CH15_INTR | 0x40901BD0 | FULL | Interrupt request register. |
| PASS0_SAR1_CH15_INTR_SET | 0x40901BD4 | FULL | Interrupt set request register |
| PASS0_SAR1_CH15_INTR_MASK | 0x40901BD8 | FULL | Interrupt mask register. |
| PASS0_SAR1_CH15_INTR_MASKED | 0x40901BDC | FULL | Interrupt masked request register |
| PASS0_SAR1_CH15_WORK | 0x40901BE0 | FULL | Working data register |
| PASS0_SAR1_CH15_RESULT | 0x40901BE4 | FULL | Result data register |
| PASS0_SAR1_CH15_GRP_STAT | 0x40901BE8 | FULL | Group status register |
| PASS0_SAR1_CH15_ENABLE | 0x40901BF8 | FULL | Enable register |
| PASS0_SAR1_CH15_TR_CMD | 0x40901BFC | FULL | Software triggers |

### 21.2.17 CH 16

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR1_CH16_TR_CTL | 0x40901C00 | FULL | Trigger control. |
| PASS0_SAR1_CH16_SAMPLE_CTL | 0x40901C04 | FULL | Sample control. |
| PASS0_SAR1_CH16_POST_CTL | 0x40901C08 | FULL | Post processing control |
| PASS0_SAR1_CH16_RANGE_CTL | 0x40901C0C | FULL | Range thresholds |
| PASS0_SAR1_CH16_INTR | 0x40901C10 | FULL | Interrupt request register. |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR1_CH16_INTR_SET | 0x40901C14 | FULL | Interrupt set request register |
| PASS0_SAR1_CH16_INTR_MASK | 0x40901C18 | FULL | Interrupt mask register. |
| PASS0_SAR1_CH16_INTR_MASKED | 0x40901C1C | FULL | Interrupt masked request register |
| PASS0_SAR1_CH16_WORK | 0x40901C20 | FULL | Working data register |
| PASS0_SAR1_CH16_RESULT | 0x40901C24 | FULL | Result data register |
| PASS0_SAR1_CH16_GRP_STAT | 0x40901C28 | FULL | Group status register |
| PASS0_SAR1_CH16_ENABLE | 0x40901C38 | FULL | Enable register |
| PASS0_SAR1_CH16_TR_CMD | 0x40901C3C | FULL | Software triggers |

### 21.2.18 CH 17

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR1_CH17_TR_CTL | 0x40901C40 | FULL | Trigger control. |
| PASS0_SAR1_CH17_SAMPLE_CTL | 0x40901C44 | FULL | Sample control. |
| PASS0_SAR1_CH17_POST_CTL | 0x40901C48 | FULL | Post processing control |
| PASS0_SAR1_CH17_RANGE_CTL | 0x40901C4C | FULL | Range thresholds |
| PASS0_SAR1_CH17_INTR | 0x40901C50 | FULL | Interrupt request register. |
| PASS0_SAR1_CH17_INTR_SET | 0x40901C54 | FULL | Interrupt set request register |
| PASS0_SAR1_CH17_INTR_MASK | 0x40901C58 | FULL | Interrupt mask register. |
| PASS0_SAR1_CH17_INTR_MASKED | 0x40901C5C | FULL | Interrupt masked request register |
| PASS0_SAR1_CH17_WORK | 0x40901C60 | FULL | Working data register |
| PASS0_SAR1_CH17_RESULT | 0x40901C64 | FULL | Result data register |
| PASS0_SAR1_CH17_GRP_STAT | 0x40901C68 | FULL | Group status register |
| PASS0_SAR1_CH17_ENABLE | 0x40901C78 | FULL | Enable register |
| PASS0_SAR1_CH17_TR_CMD | 0x40901C7C | FULL | Software triggers |

### 21.2.19 CH 18

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR1_CH18_TR_CTL | 0x40901C80 | FULL | Trigger control. |
| PASS0_SAR1_CH18_SAMPLE_CTL | 0x40901C84 | FULL | Sample control. |
| PASS0_SAR1_CH18_POST_CTL | 0x40901C88 | FULL | Post processing control |
| PASS0_SAR1_CH18_RANGE_CTL | 0x40901C8C | FULL | Range thresholds |
| PASS0_SAR1_CH18_INTR | 0x40901C90 | FULL | Interrupt request register. |
| PASS0_SAR1_CH18_INTR_SET | 0x40901C94 | FULL | Interrupt set request register |
| PASS0_SAR1_CH18_INTR_MASK | 0x40901C98 | FULL | Interrupt mask register. |
| PASS0_SAR1_CH18_INTR_MASKED | 0x40901C9C | FULL | Interrupt masked request register |
| PASS0_SAR1_CH18_WORK | 0x40901CA0 | FULL | Working data register |
| PASS0_SAR1_CH18_RESULT | 0x40901CA4 | FULL | Result data register |
| PASS0_SAR1_CH18_GRP_STAT | 0x40901CA8 | FULL | Group status register |
| PASS0_SAR1_CH18_ENABLE | 0x40901CB8 | FULL | Enable register |
| PASS0_SAR1_CH18_TR_CMD | 0x40901CBC | FULL | Software triggers |

### 21.2.20 CH 19

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR1_CH19_TR_CTL | 0x40901CC0 | FULL | Trigger control. |
| PASS0_SAR1_CH19_SAMPLE_CTL | 0x40901CC4 | FULL | Sample control. |
| PASS0_SAR1_CH19_POST_CTL | 0x40901CC8 | FULL | Post processing control |
| PASS0_SAR1_CH19_RANGE_CTL | 0x40901CCC | FULL | Range thresholds |
| PASS0_SAR1_CH19_INTR | 0x40901CD0 | FULL | Interrupt request register. |
| PASS0_SAR1_CH19_INTR_SET | 0x40901CD4 | FULL | Interrupt set request register |
| PASS0_SAR1_CH19_INTR_MASK | 0x40901CD8 | FULL | Interrupt mask register. |
| PASS0_SAR1_CH19_INTR_MASKED | 0x40901CDC | FULL | Interrupt masked request register |
| PASS0_SAR1_CH19_WORK | 0x40901CE0 | FULL | Working data register |
| PASS0_SAR1_CH19_RESULT | 0x40901CE4 | FULL | Result data register |
| PASS0_SAR1_CH19_GRP_STAT | 0x40901CE8 | FULL | Group status register |
| PASS0_SAR1_CH19_ENABLE | 0x40901CF8 | FULL | Enable register |
| PASS0_SAR1_CH19_TR_CMD | 0x40901CFC | FULL | Software triggers |

### 21.2.21 CH 20

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR1_CH20_TR_CTL | 0x40901D00 | FULL | Trigger control. |
| PASS0_SAR1_CH20_SAMPLE_CTL | 0x40901D04 | FULL | Sample control. |
| PASS0_SAR1_CH20_POST_CTL | 0x40901D08 | FULL | Post processing control |
| PASS0_SAR1_CH20_RANGE_CTL | 0x40901D0C | FULL | Range thresholds |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR1_CH20_INTR | 0x40901D10 | FULL | Interrupt request register. |
| PASS0_SAR1_CH20_INTR_SET | 0x40901D14 | FULL | Interrupt set request register |
| PASS0_SAR1_CH20_INTR_MASK | 0x40901D18 | FULL | Interrupt mask register. |
| PASS0_SAR1_CH20_INTR_MASKED | 0x40901D1C | FULL | Interrupt masked request register |
| PASS0_SAR1_CH20_WORK | 0x40901D20 | FULL | Working data register |
| PASS0_SAR1_CH20_RESULT | 0x40901D24 | FULL | Result data register |
| PASS0_SAR1_CH20_GRP_STAT | 0x40901D28 | FULL | Group status register |
| PASS0_SAR1_CH20_ENABLE | 0x40901D38 | FULL | Enable register |
| PASS0_SAR1_CH20_TR_CMD | 0x40901D3C | FULL | Software triggers |

### 21.2.22 CH 21

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR1_CH21_TR_CTL | 0x40901D40 | FULL | Trigger control. |
| PASS0_SAR1_CH21_SAMPLE_CTL | 0x40901D44 | FULL | Sample control. |
| PASS0_SAR1_CH21_POST_CTL | 0x40901D48 | FULL | Post processing control |
| PASS0_SAR1_CH21_RANGE_CTL | 0x40901D4C | FULL | Range thresholds |
| PASS0_SAR1_CH21_INTR | 0x40901D50 | FULL | Interrupt request register. |
| PASS0_SAR1_CH21_INTR_SET | 0x40901D54 | FULL | Interrupt set request register |
| PASS0_SAR1_CH21_INTR_MASK | 0x40901D58 | FULL | Interrupt mask register. |
| PASS0_SAR1_CH21_INTR_MASKED | 0x40901D5C | FULL | Interrupt masked request register |
| PASS0_SAR1_CH21_WORK | 0x40901D60 | FULL | Working data register |
| PASS0_SAR1_CH21_RESULT | 0x40901D64 | FULL | Result data register |
| PASS0_SAR1_CH21_GRP_STAT | 0x40901D68 | FULL | Group status register |
| PASS0_SAR1_CH21_ENABLE | 0x40901D78 | FULL | Enable register |
| PASS0_SAR1_CH21_TR_CMD | 0x40901D7C | FULL | Software triggers |

### 21.2.23 CH 22

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR1_CH22_TR_CTL | 0x40901D80 | FULL | Trigger control. |
| PASS0_SAR1_CH22_SAMPLE_CTL | 0x40901D84 | FULL | Sample control. |
| PASS0_SAR1_CH22_POST_CTL | 0x40901D88 | FULL | Post processing control |
| PASS0_SAR1_CH22_RANGE_CTL | 0x40901D8C | FULL | Range thresholds |
| PASS0_SAR1_CH22_INTR | 0x40901D90 | FULL | Interrupt request register. |
| PASS0_SAR1_CH22_INTR_SET | 0x40901D94 | FULL | Interrupt set request register |
| PASS0_SAR1_CH22_INTR_MASK | 0x40901D98 | FULL | Interrupt mask register. |
| PASS0_SAR1_CH22_INTR_MASKED | 0x40901D9C | FULL | Interrupt masked request register |
| PASS0_SAR1_CH22_WORK | 0x40901DA0 | FULL | Working data register |
| PASS0_SAR1_CH22_RESULT | 0x40901DA4 | FULL | Result data register |
| PASS0_SAR1_CH22_GRP_STAT | 0x40901DA8 | FULL | Group status register |
| PASS0_SAR1_CH22_ENABLE | 0x40901DB8 | FULL | Enable register |
| PASS0_SAR1_CH22_TR_CMD | 0x40901DBC | FULL | Software triggers |

### 21.2.24 CH 23

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR1_CH23_TR_CTL | 0x40901DC0 | FULL | Trigger control. |
| PASS0_SAR1_CH23_SAMPLE_CTL | 0x40901DC4 | FULL | Sample control. |
| PASS0_SAR1_CH23_POST_CTL | 0x40901DC8 | FULL | Post processing control |
| PASS0_SAR1_CH23_RANGE_CTL | 0x40901DCC | FULL | Range thresholds |
| PASS0_SAR1_CH23_INTR | 0x40901DD0 | FULL | Interrupt request register. |
| PASS0_SAR1_CH23_INTR_SET | 0x40901DD4 | FULL | Interrupt set request register |
| PASS0_SAR1_CH23_INTR_MASK | 0x40901DD8 | FULL | Interrupt mask register. |
| PASS0_SAR1_CH23_INTR_MASKED | 0x40901DDC | FULL | Interrupt masked request register |
| PASS0_SAR1_CH23_WORK | 0x40901DE0 | FULL | Working data register |
| PASS0_SAR1_CH23_RESULT | 0x40901DE4 | FULL | Result data register |
| PASS0_SAR1_CH23_GRP_STAT | 0x40901DE8 | FULL | Group status register |
| PASS0_SAR1_CH23_ENABLE | 0x40901DF8 | FULL | Enable register |
| PASS0_SAR1_CH23_TR_CMD | 0x40901DFC | FULL | Software triggers |

### 21.2.25 CH 24

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR1_CH24_TR_CTL | 0x40901E00 | FULL | Trigger control. |
| PASS0_SAR1_CH24_SAMPLE_CTL | 0x40901E04 | FULL | Sample control. |
| PASS0_SAR1_CH24_POST_CTL | 0x40901E08 | FULL | Post processing control |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR1_CH24_RANGE_CTL | 0x40901E0C | FULL | Range thresholds |
| PASS0_SAR1_CH24_INTR | 0x40901E10 | FULL | Interrupt request register. |
| PASS0_SAR1_CH24_INTR_SET | 0x40901E14 | FULL | Interrupt set request register |
| PASS0_SAR1_CH24_INTR_MASK | 0x40901E18 | FULL | Interrupt mask register. |
| PASS0_SAR1_CH24_INTR_MASKED | 0x40901E1C | FULL | Interrupt masked request register |
| PASS0_SAR1_CH24_WORK | 0x40901E20 | FULL | Working data register |
| PASS0_SAR1_CH24_RESULT | 0x40901E24 | FULL | Result data register |
| PASS0_SAR1_CH24_GRP_STAT | 0x40901E28 | FULL | Group status register |
| PASS0_SAR1_CH24_ENABLE | 0x40901E38 | FULL | Enable register |
| PASS0_SAR1_CH24_TR_CMD | 0x40901E3C | FULL | Software triggers |

### 21.2.26 CH 25

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR1_CH25_TR_CTL | 0x40901E40 | FULL | Trigger control. |
| PASS0_SAR1_CH25_SAMPLE_CTL | 0x40901E44 | FULL | Sample control. |
| PASS0_SAR1_CH25_POST_CTL | 0x40901E48 | FULL | Post processing control |
| PASS0_SAR1_CH25_RANGE_CTL | 0x40901E4C | FULL | Range thresholds |
| PASS0_SAR1_CH25_INTR | 0x40901E50 | FULL | Interrupt request register. |
| PASS0_SAR1_CH25_INTR_SET | 0x40901E54 | FULL | Interrupt set request register |
| PASS0_SAR1_CH25_INTR_MASK | 0x40901E58 | FULL | Interrupt mask register. |
| PASS0_SAR1_CH25_INTR_MASKED | 0x40901E5C | FULL | Interrupt masked request register |
| PASS0_SAR1_CH25_WORK | 0x40901E60 | FULL | Working data register |
| PASS0_SAR1_CH25_RESULT | 0x40901E64 | FULL | Result data register |
| PASS0_SAR1_CH25_GRP_STAT | 0x40901E68 | FULL | Group status register |
| PASS0_SAR1_CH25_ENABLE | 0x40901E78 | FULL | Enable register |
| PASS0_SAR1_CH25_TR_CMD | 0x40901E7C | FULL | Software triggers |

### 21.2.27 CH 26

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR1_CH26_TR_CTL | 0x40901E80 | FULL | Trigger control. |
| PASS0_SAR1_CH26_SAMPLE_CTL | 0x40901E84 | FULL | Sample control. |
| PASS0_SAR1_CH26_POST_CTL | 0x40901E88 | FULL | Post processing control |
| PASS0_SAR1_CH26_RANGE_CTL | 0x40901E8C | FULL | Range thresholds |
| PASS0_SAR1_CH26_INTR | 0x40901E90 | FULL | Interrupt request register. |
| PASS0_SAR1_CH26_INTR_SET | 0x40901E94 | FULL | Interrupt set request register |
| PASS0_SAR1_CH26_INTR_MASK | 0x40901E98 | FULL | Interrupt mask register. |
| PASS0_SAR1_CH26_INTR_MASKED | 0x40901E9C | FULL | Interrupt masked request register |
| PASS0_SAR1_CH26_WORK | 0x40901EA0 | FULL | Working data register |
| PASS0_SAR1_CH26_RESULT | 0x40901EA4 | FULL | Result data register |
| PASS0_SAR1_CH26_GRP_STAT | 0x40901EA8 | FULL | Group status register |
| PASS0_SAR1_CH26_ENABLE | 0x40901EB8 | FULL | Enable register |
| PASS0_SAR1_CH26_TR_CMD | 0x40901EBC | FULL | Software triggers |

### 21.2.28 CH 27

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR1_CH27_TR_CTL | 0x40901EC0 | FULL | Trigger control. |
| PASS0_SAR1_CH27_SAMPLE_CTL | 0x40901EC4 | FULL | Sample control. |
| PASS0_SAR1_CH27_POST_CTL | 0x40901EC8 | FULL | Post processing control |
| PASS0_SAR1_CH27_RANGE_CTL | 0x40901ECC | FULL | Range thresholds |
| PASS0_SAR1_CH27_INTR | 0x40901ED0 | FULL | Interrupt request register. |
| PASS0_SAR1_CH27_INTR_SET | 0x40901ED4 | FULL | Interrupt set request register |
| PASS0_SAR1_CH27_INTR_MASK | 0x40901ED8 | FULL | Interrupt mask register. |
| PASS0_SAR1_CH27_INTR_MASKED | 0x40901EDC | FULL | Interrupt masked request register |
| PASS0_SAR1_CH27_WORK | 0x40901EE0 | FULL | Working data register |
| PASS0_SAR1_CH27_RESULT | 0x40901EE4 | FULL | Result data register |
| PASS0_SAR1_CH27_GRP_STAT | 0x40901EE8 | FULL | Group status register |
| PASS0_SAR1_CH27_ENABLE | 0x40901EF8 | FULL | Enable register |
| PASS0_SAR1_CH27_TR_CMD | 0x40901EFC | FULL | Software triggers |

### 21.2.29 CH 28

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR1_CH28_TR_CTL | 0x40901F00 | FULL | Trigger control. |
| PASS0_SAR1_CH28_SAMPLE_CTL | 0x40901F04 | FULL | Sample control. |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR1_CH28_POST_CTL | 0x40901F08 | FULL | Post processing control |
| PASS0_SAR1_CH28_RANGE_CTL | 0x40901F0C | FULL | Range thresholds |
| PASS0_SAR1_CH28_INTR | 0x40901F10 | FULL | Interrupt request register. |
| PASS0_SAR1_CH28_INTR_SET | 0x40901F14 | FULL | Interrupt set request register |
| PASS0_SAR1_CH28_INTR_MASK | 0x40901F18 | FULL | Interrupt mask register. |
| PASS0_SAR1_CH28_INTR_MASKED | 0x40901F1C | FULL | Interrupt masked request register |
| PASS0_SAR1_CH28_WORK | 0x40901F20 | FULL | Working data register |
| PASS0_SAR1_CH28_RESULT | 0x40901F24 | FULL | Result data register |
| PASS0_SAR1_CH28_GRP_STAT | 0x40901F28 | FULL | Group status register |
| PASS0_SAR1_CH28_ENABLE | 0x40901F38 | FULL | Enable register |
| PASS0_SAR1_CH28_TR_CMD | 0x40901F3C | FULL | Software triggers |

### 21.2.30 CH 29

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR1_CH29_TR_CTL | 0x40901F40 | FULL | Trigger control. |
| PASS0_SAR1_CH29_SAMPLE_CTL | 0x40901F44 | FULL | Sample control. |
| PASS0_SAR1_CH29_POST_CTL | 0x40901F48 | FULL | Post processing control |
| PASS0_SAR1_CH29_RANGE_CTL | 0x40901F4C | FULL | Range thresholds |
| PASS0_SAR1_CH29_INTR | 0x40901F50 | FULL | Interrupt request register. |
| PASS0_SAR1_CH29_INTR_SET | 0x40901F54 | FULL | Interrupt set request register |
| PASS0_SAR1_CH29_INTR_MASK | 0x40901F58 | FULL | Interrupt mask register. |
| PASS0_SAR1_CH29_INTR_MASKED | 0x40901F5C | FULL | Interrupt masked request register |
| PASS0_SAR1_CH29_WORK | 0x40901F60 | FULL | Working data register |
| PASS0_SAR1_CH29_RESULT | 0x40901F64 | FULL | Result data register |
| PASS0_SAR1_CH29_GRP_STAT | 0x40901F68 | FULL | Group status register |
| PASS0_SAR1_CH29_ENABLE | 0x40901F78 | FULL | Enable register |
| PASS0_SAR1_CH29_TR_CMD | 0x40901F7C | FULL | Software triggers |

### 21.2.31 CH 30

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR1_CH30_TR_CTL | 0x40901F80 | FULL | Trigger control. |
| PASS0_SAR1_CH30_SAMPLE_CTL | 0x40901F84 | FULL | Sample control. |
| PASS0_SAR1_CH30_POST_CTL | 0x40901F88 | FULL | Post processing control |
| PASS0_SAR1_CH30_RANGE_CTL | 0x40901F8C | FULL | Range thresholds |
| PASS0_SAR1_CH30_INTR | 0x40901F90 | FULL | Interrupt request register. |
| PASS0_SAR1_CH30_INTR_SET | 0x40901F94 | FULL | Interrupt set request register |
| PASS0_SAR1_CH30_INTR_MASK | 0x40901F98 | FULL | Interrupt mask register. |
| PASS0_SAR1_CH30_INTR_MASKED | 0x40901F9C | FULL | Interrupt masked request register |
| PASS0_SAR1_CH30_WORK | 0x40901FA0 | FULL | Working data register |
| PASS0_SAR1_CH30_RESULT | 0x40901FA4 | FULL | Result data register |
| PASS0_SAR1_CH30_GRP_STAT | 0x40901FA8 | FULL | Group status register |
| PASS0_SAR1_CH30_ENABLE | 0x40901FB8 | FULL | Enable register |
| PASS0_SAR1_CH30_TR_CMD | 0x40901FBC | FULL | Software triggers |

### 21.2.32 CH 31

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR1_CH31_TR_CTL | 0x40901FC0 | FULL | Trigger control. |
| PASS0_SAR1_CH31_SAMPLE_CTL | 0x40901FC4 | FULL | Sample control. |
| PASS0_SAR1_CH31_POST_CTL | 0x40901FC8 | FULL | Post processing control |
| PASS0_SAR1_CH31_RANGE_CTL | 0x40901FCC | FULL | Range thresholds |
| PASS0_SAR1_CH31_INTR | 0x40901FD0 | FULL | Interrupt request register. |
| PASS0_SAR1_CH31_INTR_SET | 0x40901FD4 | FULL | Interrupt set request register |
| PASS0_SAR1_CH31_INTR_MASK | 0x40901FD8 | FULL | Interrupt mask register. |
| PASS0_SAR1_CH31_INTR_MASKED | 0x40901FDC | FULL | Interrupt masked request register |
| PASS0_SAR1_CH31_WORK | 0x40901FE0 | FULL | Working data register |
| PASS0_SAR1_CH31_RESULT | 0x40901FE4 | FULL | Result data register |
| PASS0_SAR1_CH31_GRP_STAT | 0x40901FE8 | FULL | Group status register |
| PASS0_SAR1_CH31_ENABLE | 0x40901FF8 | FULL | Enable register |
| PASS0_SAR1_CH31_TR_CMD | 0x40901FFC | FULL | Software triggers |

## 21.3 SAR 2

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR2_CTL | 0x40902000 | FULL | Analog control register. |
| PASS0_SAR2_DIAG_CTL | 0x40902004 | FULL | Diagnostic Reference control register. |
| PASS0_SAR2_PRECOND_CTL | 0x40902010 | FULL | Preconditioning control register. |
| PASS0_SAR2_ANA_CAL | 0x40902080 | FULL | Current analog calibration values |
| PASS0_SAR2_DIG_CAL | 0x40902084 | FULL | Current digital calibration values |
| PASS0_SAR2_ANA_CAL_ALT | 0x40902090 | FULL | Alternate analog calibration values |
| PASS0_SAR2_DIG_CAL_ALT | 0x40902094 | FULL | Alternate digital calibration values |
| PASS0_SAR2_CAL_UPD_CMD | 0x40902098 | FULL | Calibration update command |
| PASS0_SAR2_TR_PEND | 0x40902100 | FULL | Trigger pending status |
| PASS0_SAR2_WORK_VALID | 0x40902180 | FULL | Channel working data register 'valid' bits |
| PASS0_SAR2_WORK_RANGE | 0x40902184 | FULL | Range detected |
| PASS0_SAR2_WORK_RANGE_HI | 0x40902188 | FULL | Range detect above Hi flag |
| PASS0_SAR2_WORK_PULSE | 0x4090218C | FULL | Pulse detected |
| PASS0_SAR2_RESULT_VALID | 0x409021A0 | FULL | Channel result data register 'valid' bits |
| PASS0_SAR2_RESULT_RANGE_HI | 0x409021A4 | FULL | Channel Range above Hi flags |
| PASS0_SAR2_STATUS | 0x40902200 | FULL | Current status of internal SAR registers (mostly for debug) |
| PASS0_SAR2_AVG_STAT | 0x40902204 | FULL | Current averaging status (for debug) |

### 21.3.1 CH 0

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR2_CH0_TR_CTL | 0x40902800 | FULL | Trigger control. |
| PASS0_SAR2_CH0_SAMPLE_CTL | 0x40902804 | FULL | Sample control. |
| PASS0_SAR2_CH0_POST_CTL | 0x40902808 | FULL | Post processing control |
| PASS0_SAR2_CH0_RANGE_CTL | 0x4090280C | FULL | Range thresholds |
| PASS0_SAR2_CH0_INTR | 0x40902810 | FULL | Interrupt request register. |
| PASS0_SAR2_CH0_INTR_SET | 0x40902814 | FULL | Interrupt set request register |
| PASS0_SAR2_CH0_INTR_MASK | 0x40902818 | FULL | Interrupt mask register. |
| PASS0_SAR2_CH0_INTR_MASKED | 0x4090281C | FULL | Interrupt masked request register |
| PASS0_SAR2_CH0_WORK | 0x40902820 | FULL | Working data register |
| PASS0_SAR2_CH0_RESULT | 0x40902824 | FULL | Result data register |
| PASS0_SAR2_CH0_GRP_STAT | 0x40902828 | FULL | Group status register |
| PASS0_SAR2_CH0_ENABLE | 0x40902838 | FULL | Enable register |
| PASS0_SAR2_CH0_TR_CMD | 0x4090283C | FULL | Software triggers |

### 21.3.2 CH 1

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR2_CH1_TR_CTL | 0x40902840 | FULL | Trigger control. |
| PASS0_SAR2_CH1_SAMPLE_CTL | 0x40902844 | FULL | Sample control. |
| PASS0_SAR2_CH1_POST_CTL | 0x40902848 | FULL | Post processing control |
| PASS0_SAR2_CH1_RANGE_CTL | 0x4090284C | FULL | Range thresholds |
| PASS0_SAR2_CH1_INTR | 0x40902850 | FULL | Interrupt request register. |
| PASS0_SAR2_CH1_INTR_SET | 0x40902854 | FULL | Interrupt set request register |
| PASS0_SAR2_CH1_INTR_MASK | 0x40902858 | FULL | Interrupt mask register. |
| PASS0_SAR2_CH1_INTR_MASKED | 0x4090285C | FULL | Interrupt masked request register |
| PASS0_SAR2_CH1_WORK | 0x40902860 | FULL | Working data register |
| PASS0_SAR2_CH1_RESULT | 0x40902864 | FULL | Result data register |
| PASS0_SAR2_CH1_GRP_STAT | 0x40902868 | FULL | Group status register |
| PASS0_SAR2_CH1_ENABLE | 0x40902878 | FULL | Enable register |
| PASS0_SAR2_CH1_TR_CMD | 0x4090287C | FULL | Software triggers |

### 21.3.3 CH 2

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR2_CH2_TR_CTL | 0x40902880 | FULL | Trigger control. |
| PASS0_SAR2_CH2_SAMPLE_CTL | 0x40902884 | FULL | Sample control. |
| PASS0_SAR2_CH2_POST_CTL | 0x40902888 | FULL | Post processing control |
| PASS0_SAR2_CH2_RANGE_CTL | 0x4090288C | FULL | Range thresholds |
| PASS0_SAR2_CH2_INTR | 0x40902890 | FULL | Interrupt request register. |
| PASS0_SAR2_CH2_INTR_SET | 0x40902894 | FULL | Interrupt set request register |
| PASS0_SAR2_CH2_INTR_MASK | 0x40902898 | FULL | Interrupt mask register. |
| PASS0_SAR2_CH2_INTR_MASKED | 0x4090289C | FULL | Interrupt masked request register |
| PASS0_SAR2_CH2_WORK | 0x409028A0 | FULL | Working data register |
| PASS0_SAR2_CH2_RESULT | 0x409028A4 | FULL | Result data register |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR2_CH2_GRP_STAT | 0x409028A8 | FULL | Group status register |
| PASS0_SAR2_CH2_ENABLE | 0x409028B8 | FULL | Enable register |
| PASS0_SAR2_CH2_TR_CMD | 0x409028BC | FULL | Software triggers |

### 21.3.4 CH 3

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR2_CH3_TR_CTL | 0x409028C0 | FULL | Trigger control. |
| PASS0_SAR2_CH3_SAMPLE_CTL | 0x409028C4 | FULL | Sample control. |
| PASS0_SAR2_CH3_POST_CTL | 0x409028C8 | FULL | Post processing control |
| PASS0_SAR2_CH3_RANGE_CTL | 0x409028CC | FULL | Range thresholds |
| PASS0_SAR2_CH3_INTR | 0x409028D0 | FULL | Interrupt request register. |
| PASS0_SAR2_CH3_INTR_SET | 0x409028D4 | FULL | Interrupt set request register |
| PASS0_SAR2_CH3_INTR_MASK | 0x409028D8 | FULL | Interrupt mask register. |
| PASS0_SAR2_CH3_INTR_MASKED | 0x409028DC | FULL | Interrupt masked request register |
| PASS0_SAR2_CH3_WORK | 0x409028E0 | FULL | Working data register |
| PASS0_SAR2_CH3_RESULT | 0x409028E4 | FULL | Result data register |
| PASS0_SAR2_CH3_GRP_STAT | 0x409028E8 | FULL | Group status register |
| PASS0_SAR2_CH3_ENABLE | 0x409028F8 | FULL | Enable register |
| PASS0_SAR2_CH3_TR_CMD | 0x409028FC | FULL | Software triggers |

### 21.3.5 CH 4

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR2_CH4_TR_CTL | 0x40902900 | FULL | Trigger control. |
| PASS0_SAR2_CH4_SAMPLE_CTL | 0x40902904 | FULL | Sample control. |
| PASS0_SAR2_CH4_POST_CTL | 0x40902908 | FULL | Post processing control |
| PASS0_SAR2_CH4_RANGE_CTL | 0x4090290C | FULL | Range thresholds |
| PASS0_SAR2_CH4_INTR | 0x40902910 | FULL | Interrupt request register. |
| PASS0_SAR2_CH4_INTR_SET | 0x40902914 | FULL | Interrupt set request register |
| PASS0_SAR2_CH4_INTR_MASK | 0x40902918 | FULL | Interrupt mask register. |
| PASS0_SAR2_CH4_INTR_MASKED | 0x4090291C | FULL | Interrupt masked request register |
| PASS0_SAR2_CH4_WORK | 0x40902920 | FULL | Working data register |
| PASS0_SAR2_CH4_RESULT | 0x40902924 | FULL | Result data register |
| PASS0_SAR2_CH4_GRP_STAT | 0x40902928 | FULL | Group status register |
| PASS0_SAR2_CH4_ENABLE | 0x40902938 | FULL | Enable register |
| PASS0_SAR2_CH4_TR_CMD | 0x4090293C | FULL | Software triggers |

### 21.3.6 CH 5

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR2_CH5_TR_CTL | 0x40902940 | FULL | Trigger control. |
| PASS0_SAR2_CH5_SAMPLE_CTL | 0x40902944 | FULL | Sample control. |
| PASS0_SAR2_CH5_POST_CTL | 0x40902948 | FULL | Post processing control |
| PASS0_SAR2_CH5_RANGE_CTL | 0x4090294C | FULL | Range thresholds |
| PASS0_SAR2_CH5_INTR | 0x40902950 | FULL | Interrupt request register. |
| PASS0_SAR2_CH5_INTR_SET | 0x40902954 | FULL | Interrupt set request register |
| PASS0_SAR2_CH5_INTR_MASK | 0x40902958 | FULL | Interrupt mask register. |
| PASS0_SAR2_CH5_INTR_MASKED | 0x4090295C | FULL | Interrupt masked request register |
| PASS0_SAR2_CH5_WORK | 0x40902960 | FULL | Working data register |
| PASS0_SAR2_CH5_RESULT | 0x40902964 | FULL | Result data register |
| PASS0_SAR2_CH5_GRP_STAT | 0x40902968 | FULL | Group status register |
| PASS0_SAR2_CH5_ENABLE | 0x40902978 | FULL | Enable register |
| PASS0_SAR2_CH5_TR_CMD | 0x4090297C | FULL | Software triggers |

### 21.3.7 CH 6

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR2_CH6_TR_CTL | 0x40902980 | FULL | Trigger control. |
| PASS0_SAR2_CH6_SAMPLE_CTL | 0x40902984 | FULL | Sample control. |
| PASS0_SAR2_CH6_POST_CTL | 0x40902988 | FULL | Post processing control |
| PASS0_SAR2_CH6_RANGE_CTL | 0x4090298C | FULL | Range thresholds |
| PASS0_SAR2_CH6_INTR | 0x40902990 | FULL | Interrupt request register. |
| PASS0_SAR2_CH6_INTR_SET | 0x40902994 | FULL | Interrupt set request register |
| PASS0_SAR2_CH6_INTR_MASK | 0x40902998 | FULL | Interrupt mask register. |
| PASS0_SAR2_CH6_INTR_MASKED | 0x4090299C | FULL | Interrupt masked request register |
| PASS0_SAR2_CH6_WORK | 0x409029A0 | FULL | Working data register |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR2_CH6_RESULT | 0x409029A4 | FULL | Result data register |
| PASS0_SAR2_CH6_GRP_STAT | 0x409029A8 | FULL | Group status register |
| PASS0_SAR2_CH6_ENABLE | 0x409029B8 | FULL | Enable register |
| PASS0_SAR2_CH6_TR_CMD | 0x409029BC | FULL | Software triggers |

### 21.3.8 CH 7

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR2_CH7_TR_CTL | 0x409029C0 | FULL | Trigger control. |
| PASS0_SAR2_CH7_SAMPLE_CTL | 0x409029C4 | FULL | Sample control. |
| PASS0_SAR2_CH7_POST_CTL | 0x409029C8 | FULL | Post processing control |
| PASS0_SAR2_CH7_RANGE_CTL | 0x409029CC | FULL | Range thresholds |
| PASS0_SAR2_CH7_INTR | 0x409029D0 | FULL | Interrupt request register. |
| PASS0_SAR2_CH7_INTR_SET | 0x409029D4 | FULL | Interrupt set request register |
| PASS0_SAR2_CH7_INTR_MASK | 0x409029D8 | FULL | Interrupt mask register. |
| PASS0_SAR2_CH7_INTR_MASKED | 0x409029DC | FULL | Interrupt masked request register |
| PASS0_SAR2_CH7_WORK | 0x409029E0 | FULL | Working data register |
| PASS0_SAR2_CH7_RESULT | 0x409029E4 | FULL | Result data register |
| PASS0_SAR2_CH7_GRP_STAT | 0x409029E8 | FULL | Group status register |
| PASS0_SAR2_CH7_ENABLE | 0x409029F8 | FULL | Enable register |
| PASS0_SAR2_CH7_TR_CMD | 0x409029FC | FULL | Software triggers |

### 21.3.9 CH 8

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR2_CH8_TR_CTL | 0x40902A00 | FULL | Trigger control. |
| PASS0_SAR2_CH8_SAMPLE_CTL | 0x40902A04 | FULL | Sample control. |
| PASS0_SAR2_CH8_POST_CTL | 0x40902A08 | FULL | Post processing control |
| PASS0_SAR2_CH8_RANGE_CTL | 0x40902A0C | FULL | Range thresholds |
| PASS0_SAR2_CH8_INTR | 0x40902A10 | FULL | Interrupt request register. |
| PASS0_SAR2_CH8_INTR_SET | 0x40902A14 | FULL | Interrupt set request register |
| PASS0_SAR2_CH8_INTR_MASK | 0x40902A18 | FULL | Interrupt mask register. |
| PASS0_SAR2_CH8_INTR_MASKED | 0x40902A1C | FULL | Interrupt masked request register |
| PASS0_SAR2_CH8_WORK | 0x40902A20 | FULL | Working data register |
| PASS0_SAR2_CH8_RESULT | 0x40902A24 | FULL | Result data register |
| PASS0_SAR2_CH8_GRP_STAT | 0x40902A28 | FULL | Group status register |
| PASS0_SAR2_CH8_ENABLE | 0x40902A38 | FULL | Enable register |
| PASS0_SAR2_CH8_TR_CMD | 0x40902A3C | FULL | Software triggers |

### 21.3.10 CH 9

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR2_CH9_TR_CTL | 0x40902A40 | FULL | Trigger control. |
| PASS0_SAR2_CH9_SAMPLE_CTL | 0x40902A44 | FULL | Sample control. |
| PASS0_SAR2_CH9_POST_CTL | 0x40902A48 | FULL | Post processing control |
| PASS0_SAR2_CH9_RANGE_CTL | 0x40902A4C | FULL | Range thresholds |
| PASS0_SAR2_CH9_INTR | 0x40902A50 | FULL | Interrupt request register. |
| PASS0_SAR2_CH9_INTR_SET | 0x40902A54 | FULL | Interrupt set request register |
| PASS0_SAR2_CH9_INTR_MASK | 0x40902A58 | FULL | Interrupt mask register. |
| PASS0_SAR2_CH9_INTR_MASKED | 0x40902A5C | FULL | Interrupt masked request register |
| PASS0_SAR2_CH9_WORK | 0x40902A60 | FULL | Working data register |
| PASS0_SAR2_CH9_RESULT | 0x40902A64 | FULL | Result data register |
| PASS0_SAR2_CH9_GRP_STAT | 0x40902A68 | FULL | Group status register |
| PASS0_SAR2_CH9_ENABLE | 0x40902A78 | FULL | Enable register |
| PASS0_SAR2_CH9_TR_CMD | 0x40902A7C | FULL | Software triggers |

### 21.3.11 CH 10

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR2_CH10_TR_CTL | 0x40902A80 | FULL | Trigger control. |
| PASS0_SAR2_CH10_SAMPLE_CTL | 0x40902A84 | FULL | Sample control. |
| PASS0_SAR2_CH10_POST_CTL | 0x40902A88 | FULL | Post processing control |
| PASS0_SAR2_CH10_RANGE_CTL | 0x40902A8C | FULL | Range thresholds |
| PASS0_SAR2_CH10_INTR | 0x40902A90 | FULL | Interrupt request register. |
| PASS0_SAR2_CH10_INTR_SET | 0x40902A94 | FULL | Interrupt set request register |
| PASS0_SAR2_CH10_INTR_MASK | 0x40902A98 | FULL | Interrupt mask register. |
| PASS0_SAR2_CH10_INTR_MASKED | 0x40902A9C | FULL | Interrupt masked request register |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR2_CH10_WORK | 0x40902AA0 | FULL | Working data register |
| PASS0_SAR2_CH10_RESULT | 0x40902AA4 | FULL | Result data register |
| PASS0_SAR2_CH10_GRP_STAT | 0x40902AA8 | FULL | Group status register |
| PASS0_SAR2_CH10_ENABLE | 0x40902AB8 | FULL | Enable register |
| PASS0_SAR2_CH10_TR_CMD | 0x40902ABC | FULL | Software triggers |

### 21.3.12 CH 11

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR2_CH11_TR_CTL | 0x40902AC0 | FULL | Trigger control. |
| PASS0_SAR2_CH11_SAMPLE_CTL | 0x40902AC4 | FULL | Sample control. |
| PASS0_SAR2_CH11_POST_CTL | 0x40902AC8 | FULL | Post processing control |
| PASS0_SAR2_CH11_RANGE_CTL | 0x40902ACC | FULL | Range thresholds |
| PASS0_SAR2_CH11_INTR | 0x40902AD0 | FULL | Interrupt request register. |
| PASS0_SAR2_CH11_INTR_SET | 0x40902AD4 | FULL | Interrupt set request register |
| PASS0_SAR2_CH11_INTR_MASK | 0x40902AD8 | FULL | Interrupt mask register. |
| PASS0_SAR2_CH11_INTR_MASKED | 0x40902ADC | FULL | Interrupt masked request register |
| PASS0_SAR2_CH11_WORK | 0x40902AE0 | FULL | Working data register |
| PASS0_SAR2_CH11_RESULT | 0x40902AE4 | FULL | Result data register |
| PASS0_SAR2_CH11_GRP_STAT | 0x40902AE8 | FULL | Group status register |
| PASS0_SAR2_CH11_ENABLE | 0x40902AF8 | FULL | Enable register |
| PASS0_SAR2_CH11_TR_CMD | 0x40902AFC | FULL | Software triggers |

### 21.3.13 CH 12

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR2_CH12_TR_CTL | 0x40902B00 | FULL | Trigger control. |
| PASS0_SAR2_CH12_SAMPLE_CTL | 0x40902B04 | FULL | Sample control. |
| PASS0_SAR2_CH12_POST_CTL | 0x40902B08 | FULL | Post processing control |
| PASS0_SAR2_CH12_RANGE_CTL | 0x40902B0C | FULL | Range thresholds |
| PASS0_SAR2_CH12_INTR | 0x40902B10 | FULL | Interrupt request register. |
| PASS0_SAR2_CH12_INTR_SET | 0x40902B14 | FULL | Interrupt set request register |
| PASS0_SAR2_CH12_INTR_MASK | 0x40902B18 | FULL | Interrupt mask register. |
| PASS0_SAR2_CH12_INTR_MASKED | 0x40902B1C | FULL | Interrupt masked request register |
| PASS0_SAR2_CH12_WORK | 0x40902B20 | FULL | Working data register |
| PASS0_SAR2_CH12_RESULT | 0x40902B24 | FULL | Result data register |
| PASS0_SAR2_CH12_GRP_STAT | 0x40902B28 | FULL | Group status register |
| PASS0_SAR2_CH12_ENABLE | 0x40902B38 | FULL | Enable register |
| PASS0_SAR2_CH12_TR_CMD | 0x40902B3C | FULL | Software triggers |

### 21.3.14 CH 13

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR2_CH13_TR_CTL | 0x40902B40 | FULL | Trigger control. |
| PASS0_SAR2_CH13_SAMPLE_CTL | 0x40902B44 | FULL | Sample control. |
| PASS0_SAR2_CH13_POST_CTL | 0x40902B48 | FULL | Post processing control |
| PASS0_SAR2_CH13_RANGE_CTL | 0x40902B4C | FULL | Range thresholds |
| PASS0_SAR2_CH13_INTR | 0x40902B50 | FULL | Interrupt request register. |
| PASS0_SAR2_CH13_INTR_SET | 0x40902B54 | FULL | Interrupt set request register |
| PASS0_SAR2_CH13_INTR_MASK | 0x40902B58 | FULL | Interrupt mask register. |
| PASS0_SAR2_CH13_INTR_MASKED | 0x40902B5C | FULL | Interrupt masked request register |
| PASS0_SAR2_CH13_WORK | 0x40902B60 | FULL | Working data register |
| PASS0_SAR2_CH13_RESULT | 0x40902B64 | FULL | Result data register |
| PASS0_SAR2_CH13_GRP_STAT | 0x40902B68 | FULL | Group status register |
| PASS0_SAR2_CH13_ENABLE | 0x40902B78 | FULL | Enable register |
| PASS0_SAR2_CH13_TR_CMD | 0x40902B7C | FULL | Software triggers |

### 21.3.15 CH 14

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR2_CH14_TR_CTL | 0x40902B80 | FULL | Trigger control. |
| PASS0_SAR2_CH14_SAMPLE_CTL | 0x40902B84 | FULL | Sample control. |
| PASS0_SAR2_CH14_POST_CTL | 0x40902B88 | FULL | Post processing control |
| PASS0_SAR2_CH14_RANGE_CTL | 0x40902B8C | FULL | Range thresholds |
| PASS0_SAR2_CH14_INTR | 0x40902B90 | FULL | Interrupt request register. |
| PASS0_SAR2_CH14_INTR_SET | 0x40902B94 | FULL | Interrupt set request register |
| PASS0_SAR2_CH14_INTR_MASK | 0x40902B98 | FULL | Interrupt mask register. |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR2_CH14_INTR_MASKED | 0x40902B9C | FULL | Interrupt masked request register |
| PASS0_SAR2_CH14_WORK | 0x40902BA0 | FULL | Working data register |
| PASS0_SAR2_CH14_RESULT | 0x40902BA4 | FULL | Result data register |
| PASS0_SAR2_CH14_GRP_STAT | 0x40902BA8 | FULL | Group status register |
| PASS0_SAR2_CH14_ENABLE | 0x40902BB8 | FULL | Enable register |
| PASS0_SAR2_CH14_TR_CMD | 0x40902BBC | FULL | Software triggers |

### 21.3.16 CH 15

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR2_CH15_TR_CTL | 0x40902BC0 | FULL | Trigger control. |
| PASS0_SAR2_CH15_SAMPLE_CTL | 0x40902BC4 | FULL | Sample control. |
| PASS0_SAR2_CH15_POST_CTL | 0x40902BC8 | FULL | Post processing control |
| PASS0_SAR2_CH15_RANGE_CTL | 0x40902BCC | FULL | Range thresholds |
| PASS0_SAR2_CH15_INTR | 0x40902BD0 | FULL | Interrupt request register. |
| PASS0_SAR2_CH15_INTR_SET | 0x40902BD4 | FULL | Interrupt set request register |
| PASS0_SAR2_CH15_INTR_MASK | 0x40902BD8 | FULL | Interrupt mask register. |
| PASS0_SAR2_CH15_INTR_MASKED | 0x40902BDC | FULL | Interrupt masked request register |
| PASS0_SAR2_CH15_WORK | 0x40902BE0 | FULL | Working data register |
| PASS0_SAR2_CH15_RESULT | 0x40902BE4 | FULL | Result data register |
| PASS0_SAR2_CH15_GRP_STAT | 0x40902BE8 | FULL | Group status register |
| PASS0_SAR2_CH15_ENABLE | 0x40902BF8 | FULL | Enable register |
| PASS0_SAR2_CH15_TR_CMD | 0x40902BFC | FULL | Software triggers |

### 21.3.17 CH 16

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR2_CH16_TR_CTL | 0x40902C00 | FULL | Trigger control. |
| PASS0_SAR2_CH16_SAMPLE_CTL | 0x40902C04 | FULL | Sample control. |
| PASS0_SAR2_CH16_POST_CTL | 0x40902C08 | FULL | Post processing control |
| PASS0_SAR2_CH16_RANGE_CTL | 0x40902C0C | FULL | Range thresholds |
| PASS0_SAR2_CH16_INTR | 0x40902C10 | FULL | Interrupt request register. |
| PASS0_SAR2_CH16_INTR_SET | 0x40902C14 | FULL | Interrupt set request register |
| PASS0_SAR2_CH16_INTR_MASK | 0x40902C18 | FULL | Interrupt mask register. |
| PASS0_SAR2_CH16_INTR_MASKED | 0x40902C1C | FULL | Interrupt masked request register |
| PASS0_SAR2_CH16_WORK | 0x40902C20 | FULL | Working data register |
| PASS0_SAR2_CH16_RESULT | 0x40902C24 | FULL | Result data register |
| PASS0_SAR2_CH16_GRP_STAT | 0x40902C28 | FULL | Group status register |
| PASS0_SAR2_CH16_ENABLE | 0x40902C38 | FULL | Enable register |
| PASS0_SAR2_CH16_TR_CMD | 0x40902C3C | FULL | Software triggers |

### 21.3.18 CH 17

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR2_CH17_TR_CTL | 0x40902C40 | FULL | Trigger control. |
| PASS0_SAR2_CH17_SAMPLE_CTL | 0x40902C44 | FULL | Sample control. |
| PASS0_SAR2_CH17_POST_CTL | 0x40902C48 | FULL | Post processing control |
| PASS0_SAR2_CH17_RANGE_CTL | 0x40902C4C | FULL | Range thresholds |
| PASS0_SAR2_CH17_INTR | 0x40902C50 | FULL | Interrupt request register. |
| PASS0_SAR2_CH17_INTR_SET | 0x40902C54 | FULL | Interrupt set request register |
| PASS0_SAR2_CH17_INTR_MASK | 0x40902C58 | FULL | Interrupt mask register. |
| PASS0_SAR2_CH17_INTR_MASKED | 0x40902C5C | FULL | Interrupt masked request register |
| PASS0_SAR2_CH17_WORK | 0x40902C60 | FULL | Working data register |
| PASS0_SAR2_CH17_RESULT | 0x40902C64 | FULL | Result data register |
| PASS0_SAR2_CH17_GRP_STAT | 0x40902C68 | FULL | Group status register |
| PASS0_SAR2_CH17_ENABLE | 0x40902C78 | FULL | Enable register |
| PASS0_SAR2_CH17_TR_CMD | 0x40902C7C | FULL | Software triggers |

### 21.3.19 CH 18

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR2_CH18_TR_CTL | 0x40902C80 | FULL | Trigger control. |
| PASS0_SAR2_CH18_SAMPLE_CTL | 0x40902C84 | FULL | Sample control. |
| PASS0_SAR2_CH18_POST_CTL | 0x40902C88 | FULL | Post processing control |
| PASS0_SAR2_CH18_RANGE_CTL | 0x40902C8C | FULL | Range thresholds |
| PASS0_SAR2_CH18_INTR | 0x40902C90 | FULL | Interrupt request register. |
| PASS0_SAR2_CH18_INTR_SET | 0x40902C94 | FULL | Interrupt set request register |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR2_CH18_INTR_MASK | 0x40902C98 | FULL | Interrupt mask register. |
| PASS0_SAR2_CH18_INTR_MASKED | 0x40902C9C | FULL | Interrupt masked request register |
| PASS0_SAR2_CH18_WORK | 0x40902CA0 | FULL | Working data register |
| PASS0_SAR2_CH18_RESULT | 0x40902CA4 | FULL | Result data register |
| PASS0_SAR2_CH18_GRP_STAT | 0x40902CA8 | FULL | Group status register |
| PASS0_SAR2_CH18_ENABLE | 0x40902CB8 | FULL | Enable register |
| PASS0_SAR2_CH18_TR_CMD | 0x40902CBC | FULL | Software triggers |

### 21.3.20 CH 19

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR2_CH19_TR_CTL | 0x40902CC0 | FULL | Trigger control. |
| PASS0_SAR2_CH19_SAMPLE_CTL | 0x40902CC4 | FULL | Sample control. |
| PASS0_SAR2_CH19_POST_CTL | 0x40902CC8 | FULL | Post processing control |
| PASS0_SAR2_CH19_RANGE_CTL | 0x40902CCC | FULL | Range thresholds |
| PASS0_SAR2_CH19_INTR | 0x40902CD0 | FULL | Interrupt request register. |
| PASS0_SAR2_CH19_INTR_SET | 0x40902CD4 | FULL | Interrupt set request register |
| PASS0_SAR2_CH19_INTR_MASK | 0x40902CD8 | FULL | Interrupt mask register. |
| PASS0_SAR2_CH19_INTR_MASKED | 0x40902CDC | FULL | Interrupt masked request register |
| PASS0_SAR2_CH19_WORK | 0x40902CE0 | FULL | Working data register |
| PASS0_SAR2_CH19_RESULT | 0x40902CE4 | FULL | Result data register |
| PASS0_SAR2_CH19_GRP_STAT | 0x40902CE8 | FULL | Group status register |
| PASS0_SAR2_CH19_ENABLE | 0x40902CF8 | FULL | Enable register |
| PASS0_SAR2_CH19_TR_CMD | 0x40902CFC | FULL | Software triggers |

### 21.3.21 CH 20

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR2_CH20_TR_CTL | 0x40902D00 | FULL | Trigger control. |
| PASS0_SAR2_CH20_SAMPLE_CTL | 0x40902D04 | FULL | Sample control. |
| PASS0_SAR2_CH20_POST_CTL | 0x40902D08 | FULL | Post processing control |
| PASS0_SAR2_CH20_RANGE_CTL | 0x40902D0C | FULL | Range thresholds |
| PASS0_SAR2_CH20_INTR | 0x40902D10 | FULL | Interrupt request register. |
| PASS0_SAR2_CH20_INTR_SET | 0x40902D14 | FULL | Interrupt set request register |
| PASS0_SAR2_CH20_INTR_MASK | 0x40902D18 | FULL | Interrupt mask register. |
| PASS0_SAR2_CH20_INTR_MASKED | 0x40902D1C | FULL | Interrupt masked request register |
| PASS0_SAR2_CH20_WORK | 0x40902D20 | FULL | Working data register |
| PASS0_SAR2_CH20_RESULT | 0x40902D24 | FULL | Result data register |
| PASS0_SAR2_CH20_GRP_STAT | 0x40902D28 | FULL | Group status register |
| PASS0_SAR2_CH20_ENABLE | 0x40902D38 | FULL | Enable register |
| PASS0_SAR2_CH20_TR_CMD | 0x40902D3C | FULL | Software triggers |

### 21.3.22 CH 21

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR2_CH21_TR_CTL | 0x40902D40 | FULL | Trigger control. |
| PASS0_SAR2_CH21_SAMPLE_CTL | 0x40902D44 | FULL | Sample control. |
| PASS0_SAR2_CH21_POST_CTL | 0x40902D48 | FULL | Post processing control |
| PASS0_SAR2_CH21_RANGE_CTL | 0x40902D4C | FULL | Range thresholds |
| PASS0_SAR2_CH21_INTR | 0x40902D50 | FULL | Interrupt request register. |
| PASS0_SAR2_CH21_INTR_SET | 0x40902D54 | FULL | Interrupt set request register |
| PASS0_SAR2_CH21_INTR_MASK | 0x40902D58 | FULL | Interrupt mask register. |
| PASS0_SAR2_CH21_INTR_MASKED | 0x40902D5C | FULL | Interrupt masked request register |
| PASS0_SAR2_CH21_WORK | 0x40902D60 | FULL | Working data register |
| PASS0_SAR2_CH21_RESULT | 0x40902D64 | FULL | Result data register |
| PASS0_SAR2_CH21_GRP_STAT | 0x40902D68 | FULL | Group status register |
| PASS0_SAR2_CH21_ENABLE | 0x40902D78 | FULL | Enable register |
| PASS0_SAR2_CH21_TR_CMD | 0x40902D7C | FULL | Software triggers |

### 21.3.23 CH 22

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR2_CH22_TR_CTL | 0x40902D80 | FULL | Trigger control. |
| PASS0_SAR2_CH22_SAMPLE_CTL | 0x40902D84 | FULL | Sample control. |
| PASS0_SAR2_CH22_POST_CTL | 0x40902D88 | FULL | Post processing control |
| PASS0_SAR2_CH22_RANGE_CTL | 0x40902D8C | FULL | Range thresholds |
| PASS0_SAR2_CH22_INTR | 0x40902D90 | FULL | Interrupt request register. |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR2_CH22_INTR_SET | 0x40902D94 | FULL | Interrupt set request register |
| PASS0_SAR2_CH22_INTR_MASK | 0x40902D98 | FULL | Interrupt mask register. |
| PASS0_SAR2_CH22_INTR_MASKED | 0x40902D9C | FULL | Interrupt masked request register |
| PASS0_SAR2_CH22_WORK | 0x40902DA0 | FULL | Working data register |
| PASS0_SAR2_CH22_RESULT | 0x40902DA4 | FULL | Result data register |
| PASS0_SAR2_CH22_GRP_STAT | 0x40902DA8 | FULL | Group status register |
| PASS0_SAR2_CH22_ENABLE | 0x40902DB8 | FULL | Enable register |
| PASS0_SAR2_CH22_TR_CMD | 0x40902DBC | FULL | Software triggers |

### 21.3.24 CH 23

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR2_CH23_TR_CTL | 0x40902DC0 | FULL | Trigger control. |
| PASS0_SAR2_CH23_SAMPLE_CTL | 0x40902DC4 | FULL | Sample control. |
| PASS0_SAR2_CH23_POST_CTL | 0x40902DC8 | FULL | Post processing control |
| PASS0_SAR2_CH23_RANGE_CTL | 0x40902DCC | FULL | Range thresholds |
| PASS0_SAR2_CH23_INTR | 0x40902DD0 | FULL | Interrupt request register. |
| PASS0_SAR2_CH23_INTR_SET | 0x40902DD4 | FULL | Interrupt set request register |
| PASS0_SAR2_CH23_INTR_MASK | 0x40902DD8 | FULL | Interrupt mask register. |
| PASS0_SAR2_CH23_INTR_MASKED | 0x40902DDC | FULL | Interrupt masked request register |
| PASS0_SAR2_CH23_WORK | 0x40902DE0 | FULL | Working data register |
| PASS0_SAR2_CH23_RESULT | 0x40902DE4 | FULL | Result data register |
| PASS0_SAR2_CH23_GRP_STAT | 0x40902DE8 | FULL | Group status register |
| PASS0_SAR2_CH23_ENABLE | 0x40902DF8 | FULL | Enable register |
| PASS0_SAR2_CH23_TR_CMD | 0x40902DFC | FULL | Software triggers |

### 21.3.25 CH 24

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR2_CH24_TR_CTL | 0x40902E00 | FULL | Trigger control. |
| PASS0_SAR2_CH24_SAMPLE_CTL | 0x40902E04 | FULL | Sample control. |
| PASS0_SAR2_CH24_POST_CTL | 0x40902E08 | FULL | Post processing control |
| PASS0_SAR2_CH24_RANGE_CTL | 0x40902E0C | FULL | Range thresholds |
| PASS0_SAR2_CH24_INTR | 0x40902E10 | FULL | Interrupt request register. |
| PASS0_SAR2_CH24_INTR_SET | 0x40902E14 | FULL | Interrupt set request register |
| PASS0_SAR2_CH24_INTR_MASK | 0x40902E18 | FULL | Interrupt mask register. |
| PASS0_SAR2_CH24_INTR_MASKED | 0x40902E1C | FULL | Interrupt masked request register |
| PASS0_SAR2_CH24_WORK | 0x40902E20 | FULL | Working data register |
| PASS0_SAR2_CH24_RESULT | 0x40902E24 | FULL | Result data register |
| PASS0_SAR2_CH24_GRP_STAT | 0x40902E28 | FULL | Group status register |
| PASS0_SAR2_CH24_ENABLE | 0x40902E38 | FULL | Enable register |
| PASS0_SAR2_CH24_TR_CMD | 0x40902E3C | FULL | Software triggers |

### 21.3.26 CH 25

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR2_CH25_TR_CTL | 0x40902E40 | FULL | Trigger control. |
| PASS0_SAR2_CH25_SAMPLE_CTL | 0x40902E44 | FULL | Sample control. |
| PASS0_SAR2_CH25_POST_CTL | 0x40902E48 | FULL | Post processing control |
| PASS0_SAR2_CH25_RANGE_CTL | 0x40902E4C | FULL | Range thresholds |
| PASS0_SAR2_CH25_INTR | 0x40902E50 | FULL | Interrupt request register. |
| PASS0_SAR2_CH25_INTR_SET | 0x40902E54 | FULL | Interrupt set request register |
| PASS0_SAR2_CH25_INTR_MASK | 0x40902E58 | FULL | Interrupt mask register. |
| PASS0_SAR2_CH25_INTR_MASKED | 0x40902E5C | FULL | Interrupt masked request register |
| PASS0_SAR2_CH25_WORK | 0x40902E60 | FULL | Working data register |
| PASS0_SAR2_CH25_RESULT | 0x40902E64 | FULL | Result data register |
| PASS0_SAR2_CH25_GRP_STAT | 0x40902E68 | FULL | Group status register |
| PASS0_SAR2_CH25_ENABLE | 0x40902E78 | FULL | Enable register |
| PASS0_SAR2_CH25_TR_CMD | 0x40902E7C | FULL | Software triggers |

### 21.3.27 CH 26

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR2_CH26_TR_CTL | 0x40902E80 | FULL | Trigger control. |
| PASS0_SAR2_CH26_SAMPLE_CTL | 0x40902E84 | FULL | Sample control. |
| PASS0_SAR2_CH26_POST_CTL | 0x40902E88 | FULL | Post processing control |
| PASS0_SAR2_CH26_RANGE_CTL | 0x40902E8C | FULL | Range thresholds |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR2_CH26_INTR | 0x40902E90 | FULL | Interrupt request register. |
| PASS0_SAR2_CH26_INTR_SET | 0x40902E94 | FULL | Interrupt set request register |
| PASS0_SAR2_CH26_INTR_MASK | 0x40902E98 | FULL | Interrupt mask register. |
| PASS0_SAR2_CH26_INTR_MASKED | 0x40902E9C | FULL | Interrupt masked request register |
| PASS0_SAR2_CH26_WORK | 0x40902EA0 | FULL | Working data register |
| PASS0_SAR2_CH26_RESULT | 0x40902EA4 | FULL | Result data register |
| PASS0_SAR2_CH26_GRP_STAT | 0x40902EA8 | FULL | Group status register |
| PASS0_SAR2_CH26_ENABLE | 0x40902EB8 | FULL | Enable register |
| PASS0_SAR2_CH26_TR_CMD | 0x40902EBC | FULL | Software triggers |

### 21.3.28 CH 27

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR2_CH27_TR_CTL | 0x40902EC0 | FULL | Trigger control. |
| PASS0_SAR2_CH27_SAMPLE_CTL | 0x40902EC4 | FULL | Sample control. |
| PASS0_SAR2_CH27_POST_CTL | 0x40902EC8 | FULL | Post processing control |
| PASS0_SAR2_CH27_RANGE_CTL | 0x40902ECC | FULL | Range thresholds |
| PASS0_SAR2_CH27_INTR | 0x40902ED0 | FULL | Interrupt request register. |
| PASS0_SAR2_CH27_INTR_SET | 0x40902ED4 | FULL | Interrupt set request register |
| PASS0_SAR2_CH27_INTR_MASK | 0x40902ED8 | FULL | Interrupt mask register. |
| PASS0_SAR2_CH27_INTR_MASKED | 0x40902EDC | FULL | Interrupt masked request register |
| PASS0_SAR2_CH27_WORK | 0x40902EE0 | FULL | Working data register |
| PASS0_SAR2_CH27_RESULT | 0x40902EE4 | FULL | Result data register |
| PASS0_SAR2_CH27_GRP_STAT | 0x40902EE8 | FULL | Group status register |
| PASS0_SAR2_CH27_ENABLE | 0x40902EF8 | FULL | Enable register |
| PASS0_SAR2_CH27_TR_CMD | 0x40902EFC | FULL | Software triggers |

### 21.3.29 CH 28

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR2_CH28_TR_CTL | 0x40902F00 | FULL | Trigger control. |
| PASS0_SAR2_CH28_SAMPLE_CTL | 0x40902F04 | FULL | Sample control. |
| PASS0_SAR2_CH28_POST_CTL | 0x40902F08 | FULL | Post processing control |
| PASS0_SAR2_CH28_RANGE_CTL | 0x40902F0C | FULL | Range thresholds |
| PASS0_SAR2_CH28_INTR | 0x40902F10 | FULL | Interrupt request register. |
| PASS0_SAR2_CH28_INTR_SET | 0x40902F14 | FULL | Interrupt set request register |
| PASS0_SAR2_CH28_INTR_MASK | 0x40902F18 | FULL | Interrupt mask register. |
| PASS0_SAR2_CH28_INTR_MASKED | 0x40902F1C | FULL | Interrupt masked request register |
| PASS0_SAR2_CH28_WORK | 0x40902F20 | FULL | Working data register |
| PASS0_SAR2_CH28_RESULT | 0x40902F24 | FULL | Result data register |
| PASS0_SAR2_CH28_GRP_STAT | 0x40902F28 | FULL | Group status register |
| PASS0_SAR2_CH28_ENABLE | 0x40902F38 | FULL | Enable register |
| PASS0_SAR2_CH28_TR_CMD | 0x40902F3C | FULL | Software triggers |

### 21.3.30 CH 29

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR2_CH29_TR_CTL | 0x40902F40 | FULL | Trigger control. |
| PASS0_SAR2_CH29_SAMPLE_CTL | 0x40902F44 | FULL | Sample control. |
| PASS0_SAR2_CH29_POST_CTL | 0x40902F48 | FULL | Post processing control |
| PASS0_SAR2_CH29_RANGE_CTL | 0x40902F4C | FULL | Range thresholds |
| PASS0_SAR2_CH29_INTR | 0x40902F50 | FULL | Interrupt request register. |
| PASS0_SAR2_CH29_INTR_SET | 0x40902F54 | FULL | Interrupt set request register |
| PASS0_SAR2_CH29_INTR_MASK | 0x40902F58 | FULL | Interrupt mask register. |
| PASS0_SAR2_CH29_INTR_MASKED | 0x40902F5C | FULL | Interrupt masked request register |
| PASS0_SAR2_CH29_WORK | 0x40902F60 | FULL | Working data register |
| PASS0_SAR2_CH29_RESULT | 0x40902F64 | FULL | Result data register |
| PASS0_SAR2_CH29_GRP_STAT | 0x40902F68 | FULL | Group status register |
| PASS0_SAR2_CH29_ENABLE | 0x40902F78 | FULL | Enable register |
| PASS0_SAR2_CH29_TR_CMD | 0x40902F7C | FULL | Software triggers |

### 21.3.31 CH 30

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR2_CH30_TR_CTL | 0x40902F80 | FULL | Trigger control. |
| PASS0_SAR2_CH30_SAMPLE_CTL | 0x40902F84 | FULL | Sample control. |
| PASS0_SAR2_CH30_POST_CTL | 0x40902F88 | FULL | Post processing control |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR2_CH30_RANGE_CTL | 0x40902F8C | FULL | Range thresholds |
| PASS0_SAR2_CH30_INTR | 0x40902F90 | FULL | Interrupt request register. |
| PASS0_SAR2_CH30_INTR_SET | 0x40902F94 | FULL | Interrupt set request register |
| PASS0_SAR2_CH30_INTR_MASK | 0x40902F98 | FULL | Interrupt mask register. |
| PASS0_SAR2_CH30_INTR_MASKED | 0x40902F9C | FULL | Interrupt masked request register |
| PASS0_SAR2_CH30_WORK | 0x40902FA0 | FULL | Working data register |
| PASS0_SAR2_CH30_RESULT | 0x40902FA4 | FULL | Result data register |
| PASS0_SAR2_CH30_GRP_STAT | 0x40902FA8 | FULL | Group status register |
| PASS0_SAR2_CH30_ENABLE | 0x40902FB8 | FULL | Enable register |
| PASS0_SAR2_CH30_TR_CMD | 0x40902FBC | FULL | Software triggers |

### 21.3.32 CH 31

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_SAR2_CH31_TR_CTL | 0x40902FC0 | FULL | Trigger control. |
| PASS0_SAR2_CH31_SAMPLE_CTL | 0x40902FC4 | FULL | Sample control. |
| PASS0_SAR2_CH31_POST_CTL | 0x40902FC8 | FULL | Post processing control |
| PASS0_SAR2_CH31_RANGE_CTL | 0x40902FCC | FULL | Range thresholds |
| PASS0_SAR2_CH31_INTR | 0x40902FD0 | FULL | Interrupt request register. |
| PASS0_SAR2_CH31_INTR_SET | 0x40902FD4 | FULL | Interrupt set request register |
| PASS0_SAR2_CH31_INTR_MASK | 0x40902FD8 | FULL | Interrupt mask register. |
| PASS0_SAR2_CH31_INTR_MASKED | 0x40902FDC | FULL | Interrupt masked request register |
| PASS0_SAR2_CH31_WORK | 0x40902FE0 | FULL | Working data register |
| PASS0_SAR2_CH31_RESULT | 0x40902FE4 | FULL | Result data register |
| PASS0_SAR2_CH31_GRP_STAT | 0x40902FE8 | FULL | Group status register |
| PASS0_SAR2_CH31_ENABLE | 0x40902FF8 | FULL | Enable register |
| PASS0_SAR2_CH31_TR_CMD | 0x40902FFC | FULL | Software triggers |

## 21.4 EPASS_MMIO

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PASS0_PASS_CTL | 0x409F0000 | FULL | PASS control register |
| PASS0_SAR_TR_IN_SEL0 | 0x409F0020 | FULL | per SAR generic input trigger select |
| PASS0_SAR_TR_IN_SEL1 | 0x409F0024 | FULL | per SAR generic input trigger select |
| PASS0_SAR_TR_IN_SEL2 | 0x409F0028 | FULL | per SAR generic input trigger select |
| PASS0_SAR_TR_OUT_SEL0 | 0x409F0040 | FULL | per SAR generic output trigger select |
| PASS0_SAR_TR_OUT_SEL1 | 0x409F0044 | FULL | per SAR generic output trigger select |
| PASS0_SAR_TR_OUT_SEL2 | 0x409F0048 | FULL | per SAR generic output trigger select |
| PASS0_TEST_CTL | 0x409F0080 | FULL | Test control bits |

## 21.5 Register Details

### 21.5.1 SAR

#### 21.5.1.1 PASS_SAR_CTL

**Description:** Analog control register.
**Address:** 0x40900000
**Offset:** 0x0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | PWRUP_TIME [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:11] | | | | | HALF_LSB [10:10] | MSB _STRETCH [9:9] | IDLE _PWRDWN [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | ENABLED [31:31] | ADC_EN [30:30] | SARMUX _EN [29:29] | None [28:24] | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | PWRUP_TIME | RW | R | 0 | Number cycles to wait to power up after IDLE_PWRDWN.<br>Check the STATUS.PWRUP_BUSY flag to see if the delay is still in progress.<br>The power up delay is 1 us. |
| 8 | IDLE_PWRDWN | RW | R | 0 | When idle automatically power down the analog.<br>After an automatic power down a new trigger will power up the analog, however it will take PWRUP_TIME cycles before the first acquisition can be started. Note that re-arbitration happens at that time, i.e. the trigger that caused the power up may not get handled first. |
| 9 | MSB_STRETCH | RW | R | 0 | When set use 2 cycles for the Most Significant Bit (MSB)<br>- 0: Use 1 clock cycle for MSB<br>- 1: Use 2 clock cycles for MSB |
| 10 | HALF_LSB | RW | R | 0 | When set take an extra cycle to convert the half LSB and add it to 12-bit result for Missing Code Recovery This bit should always be set to '1'<br>- 0: disable half LSB conversion (not recommended)<br>- 1: enable half LSB conversion |
| 29 | SARMUX_EN | RW | R | 0 | Enable the SARMUX (only valid if ENABLED=1)<br>- 0: SARMUX disabled (put analog in power down)<br>- 1: SARMUX enabled. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 30 | ADC_EN | RW | R | 0 | Enable the SAR ADC and SAR sequencer (only valid if ENABLED=1)<br>- 0: SARADC and SARSEQ are disabled (put SARADC analog in power down and stop clocks), also clears all pending triggers.<br>- 1: SAR ADC and SARSEQ are enabled.<br>To enable ADC0 to borrow SARMUX1-3 the corresponding ADC_EN must be set to 0. |
| 31 | ENABLED | RW | R | 0 | - 0: SAR IP disabled (put analog in power down and stop clocks), also clears all pending triggers.<br>- 1: SAR IP enabled. |

### 21.5.1.2 PASS_SAR_DIAG_CTL

**Description:** Diagnostic Reference control register.
**Address:** 0x40900004
**Offset:** 0x4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:4] | | | | DIAG_SEL [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | DIAG_EN [31:31] | None [30:24] | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | DIAG_SEL | RW | R | 0 | Select Diagnostic Reference function |
| | VREFL | | | 0 | DiagOut = VrefL |
| | VREFH_1DIV8 | | | 1 | DiagOut = VrefH * 1/8 |
| | VREFH_2DIV8 | | | 2 | DiagOut = VrefH * 2/8 |
| | VREFH_3DIV8 | | | 3 | DiagOut = VrefH * 3/8 |
| | VREFH_4DIV8 | | | 4 | DiagOut = VrefH * 4/8 |
| | VREFH_5DIV8 | | | 5 | DiagOut = VrefH * 5/8 |
| | VREFH_6DIV8 | | | 6 | DiagOut = VrefH * 6/8 |
| | VREFH_7DIV8 | | | 7 | DiagOut = VrefH * 7/8 |
| | VREFH | | | 8 | DiagOut = VrefH |
| | VREFX | | | 9 | DiagOut = VrefX = VrefH * 199/200 |
| | VBG | | | 10 | DiagOut = Vbg from SRSS |
| | VIN1 | | | 11 | DiagOut = Vin1 |
| | VIN2 | | | 12 | DiagOut = Vin2 |
| | VIN3 | | | 13 | DiagOut = Vin3 |
| | I_SOURCE | | | 14 | DiagOut = Isource (10uA) |
| | I_SINK | | | 15 | DiagOut = Isink (10uA) |
| 31 | DIAG_EN | RW | R | 0 | Diagnostic Reference enable (only valid if ENABLED=1)<br>- 0: Diagnostic Reference disabled (powered down resistor ladder and current mirrors, DiagOut = Vssa).<br>- 1: Diagnostic Reference enabled, output signal select according to DIAG_SEL (note also EPASS_MMIO.PASS_CTL.REFBUF_EN must be set). |

### 21.5.1.3 PASS_SAR_PRECOND_CTL

**Description:** Preconditioning control register.
**Address:** 0x40900010
**Offset:** 0x10
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Precondition time value used when a channel enables preconditioning (PRECOND_MODE)
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:4] | | | | PRECOND_TIME [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | PRECOND_TIME | RW | R | 0 | Number ADC clock cycles that Preconditioning is done before the sample window starts. If OVERLAP_EN=0 there will be 1 additional break before make cycle between preconditioning and sampling.<br>Note that the minimum value is 1 (0 gives the same result as 1). |

### 21.5.1.4 PASS_SAR_ANA_CAL

**Description:** Current analog calibration values
**Address:** 0x40900080
**Offset:** 0x80
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Hardware can update this register if software sets the CAL_UPD_CMD.UPDATE
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | AOFFSET [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:21] | | | AGAIN [20:16] | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | AOFFSET | RW | RW | 0 | Analog offset correction |
| 16:20 | AGAIN | RW | RW | 0 | Analog gain correction |

### 21.5.1.5 PASS_SAR_DIG_CAL

**Description:** Current digital calibration values
**Address:** 0x40900084
**Offset:** 0x84
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Hardware can update this register if software sets the CAL_UPD_CMD.UPDATE
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DOFFSET [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:12] | | | | DOFFSET [11:8] | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:22] | | DGAIN [21:16] | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:11 | DOFFSET | RW | RW | 0 | Digital offset correction<br>Subtract DOFFSET from ADC output. |
| 16:21 | DGAIN | RW | RW | 0 | Digital gain correction.<br>Signed value to correct +/- 30 codes for the maximum input voltage.<br>Corrected = (D - DOFFSET) + ( (D - DOFFSET) * DGAIN + 0x800) / 0x1000 |

### 21.5.1.6 PASS_SAR_ANA_CAL_ALT

**Description:** Alternate analog calibration values
**Address:** 0x40900090
**Offset:** 0x90
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Also known as 'shadow' calibration registers to enable background calibration
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | AOFFSET [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:21] | | | AGAIN [20:16] | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | AOFFSET | RW | R | 0 | See corresponding ANA_CAL field |
| 16:20 | AGAIN | RW | R | 0 | See corresponding ANA_CAL field |

### 21.5.1.7 PASS_SAR_DIG_CAL_ALT

**Description:** Alternate digital calibration values
**Address:** 0x40900094
**Offset:** 0x94
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** First use analog calibration to avoid saturation for the required input voltage range. Then use this digital calibration to map codes on full 12-bit range.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DOFFSET [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:12] | | | | DOFFSET [11:8] | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:22] | | DGAIN [21:16] | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:11 | DOFFSET | RW | R | 0 | See corresponding DIG_CAL field |
| 16:21 | DGAIN | RW | R | 0 | See corresponding DIG_CAL field |

### 21.5.1.8 PASS_SAR_CAL_UPD_CMD

**Description:** Calibration update command
**Address:** 0x40900098
**Offset:** 0x98
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:1] | | | | | | | UPDATE [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | UPDATE | RW | RW1C | 0 | Calibration update command: coherently copy values from alternate calibration regs to current calibration regs.<br>Software sets this bit when the alternate calibration values have been set with the new values. Hardware will do the calibration update as soon as the ADC is idle or a 'continuous' triggered group completes. This ensures that all acquisitions within a group scan (even if preempted) are done with the same calibration values.<br>This bit is cleared at the same time the calibration update is done. By clearing this bit software can cancel a requested update.<br>Note: if the ADC is always busy with acquisitions for non continuously triggered groups/channels then the calibration update will remain pending forever. In such a case the software can either do a non coherent update by writing directly to the current calibration registers, or software can force the ADC to idle by disabling some or all channels.<br>Software can check/poll this bit to see if the calibration update has taken effect. |

### 21.5.1.9 PASS_SAR_TR_PEND

**Description:** Trigger pending status
**Address:** 0x40900100
**Offset:** 0x100
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** Status
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | TR_PEND [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | TR_PEND [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | TR_PEND [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | TR_PEND [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | TR_PEND | R | W | 0 | Trigger Pending.<br>Hardware will set this bit if a hardware trigger is received. |

### 21.5.1.10 PASS_SAR_WORK_VALID

**Description:** Channel working data register 'valid' bits
**Address:** 0x40900180
**Offset:** 0x180
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** bits of disabled channels will be reset
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | WORK_VALID [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | WORK_VALID [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | WORK_VALID [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | WORK_VALID [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | WORK_VALID | R | RW | 0 | If set the corresponding WORK register is valid, i.e. was already acquired during the current group scan. If this bit is low then either the channel is not enabled, not yet acquired or it is used as a pulse detect channel. |

### 21.5.1.11 PASS_SAR_WORK_RANGE

**Description:** Range detected
**Address:** 0x40900184
**Offset:** 0x184
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** bits of disabled channels will be reset
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | RANGE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | RANGE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | RANGE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | RANGE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | RANGE | R | RW | 0 | N/A |

### 21.5.1.12 PASS_SAR_WORK_RANGE_HI

**Description:** Range detect above Hi flag
**Address:** 0x40900188
**Offset:** 0x188
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** bits of disabled channels will be reset
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | ABOVE_HI [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | ABOVE_HI [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | ABOVE_HI [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | ABOVE_HI [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | ABOVE_HI | R | RW | 0 | Out of range was detected and the value was above the Hi threshold |

### 21.5.1.13 PASS_SAR_WORK_PULSE

**Description:** Pulse detected
**Address:** 0x4090018C
**Offset:** 0x18C
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** bits of disabled channels will be reset
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | PULSE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | PULSE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | PULSE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | PULSE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | PULSE | R | RW | 0 | N/A |

### 21.5.1.14 PASS_SAR_RESULT_VALID

**Description:** Channel result data register 'valid' bits
**Address:** 0x409001A0
**Offset:** 0x1A0
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | RESULT_VALID [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | RESULT_VALID [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | RESULT_VALID [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | RESULT_VALID [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | RESULT_VALID | R | RW | 0 | If set the corresponding RESULT register is valid, i.e. was acquired during the preceding group scan. If this bit is low, after a group scan completed, then either the channel is not enabled or is used as a pulse detect channel. |

### 21.5.1.15 PASS_SAR_RESULT_RANGE_HI

**Description:** Channel Range above Hi flags
**Address:** 0x409001A4
**Offset:** 0x1A4
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | ABOVE_HI [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | ABOVE_HI [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | ABOVE_HI [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | ABOVE_HI [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | ABOVE_HI | R | RW | 0 | Out of range was detected and the value was above the Hi threshold |

### 21.5.1.16 PASS_SAR_STATUS

**Description:** Current status of internal SAR registers (mostly for debug)
**Address:** 0x40900200
**Offset:** 0x200
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:5] | | | CUR_CHAN [4:0] | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:14] | | CUR_PREEMPT_TYPE [13:12] | | None [11:11] | CUR_PRIO [10:8] | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | BUSY [31:31] | PWRUP_BUSY [30:30] | DBG_FREEZE [29:29] | None [28:24] | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:4 | CUR_CHAN | R | W | 0 | current channel being acquired, only valid if BUSY. |
| 8:10 | CUR_PRIO | R | W | 0 | priority of current group/channel, only valid if BUSY. |
| 12:13 | CUR_PREEMPT_TYPE | R | W | 0 | Preempting type of current group/channel, only valid if BUSY. |
| 29 | DBG_FREEZE | R | W | 0 | If high then the SAR is prevented from starting a new acquisition, see DBG_FREEZE_EN. |
| 30 | PWRUP_BUSY | R | W | 0 | If high then the SAR is waiting for PWRUP_TIME due to IDLE_PWRDWN |
| 31 | BUSY | R | W | 0 | If high then the SAR is busy with a conversion. |

### 21.5.1.17 PASS_SAR_AVG_STAT

**Description:** Current averaging status (for debug)
**Address:** 0x40900204
**Offset:** 0x204
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | CUR_AVG_ACCU [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | CUR_AVG_ACCU [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:20] | | | | CUR_AVG_ACCU [19:16] | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | CUR_AVG_CNT [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:19 | CUR_AVG_ACCU | R | W | 0 | the current value of the averaging accumulator |
| 24:31 | CUR_AVG_CNT | R | W | 0 | the current value of the averaging counter. Note that the value shown is updated after the sample window and therefore runs ahead of the accumulator update. |

### 21.5.1.18 CH

#### 21.5.1.18.1 PASS_SAR_CH_TR_CTL

**Description:** Trigger control.
**Address:** 0x40900800
**Offset:** 0x0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Make sure the channel or the IP is disabled before changing this register
**Default:** 0x800

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:7] | PRIO [6:4] | | | None [3:3] | SEL [2:0] | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:12] | | | | GROUP_END [11:11] | None [10:10] | PREEMPT_TYPE [9:8] | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | DONE_LEVEL [31:31] | None [30:24] | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:2 | SEL | RW | R | 0 | Trigger select |
| | OFF | | | 0 | Use for channels in group, except the first channel |
| | TCPWM | | | 1 | Trigger from corresponding TCPWM channel |
| | GENERIC0 | | | 2 | Generic trigger input 0 |
| | GENERIC1 | | | 3 | N/A |
| | GENERIC2 | | | 4 | N/A |
| | GENERIC3 | | | 5 | N/A |
| | GENERIC4 | | | 6 | N/A |
| | CONTINUOUS | | | 7 | Always triggered (also called idle), can only be used for at most 1 channel |
| 4:6 | PRIO | RW | R | 0 | Channel priority:<br>'0': highest priority.<br>'1'<br>...<br>'6'<br>'7': lowest priority.<br><br>Channels with the same priority constitute a priority level. Priority decoding determines the highest priority pending channel. This channel is determined as follows. First, the highest priority level with pending channels is identified. Second, within this priority level, round robin arbitration is applied. Round robin arbitration (within a priority level) gives the highest priority to the lower channel indices (within the priority level). |
| 8:9 | PREEMPT_TYPE | RW | R | 0 | Preemption type allow for this group |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| | ABORT_CANCEL | | | 0 | Abort ongoing acquisition, do not return<br>Clear pending trigger for aborted group and set Cancelled interrupt.<br>Also 'Abort' whenever this group (do not pend the trigger) is not immediately scheduled for acquisition after a new trigger arrives.<br>For this preemption type only, only a positive edge on the trigger can trigger the channel, i.e. CONTINUOUS or level high operation is not supported (to avoid continuous Cancelled interrupts).<br>In case CTL.IDLE_PWRDWN is used and the analog is powered down, the group cannot be immediately scheduled for acquisition and therefore a trigger for a group with this preemption type will power up the analog, but the group will ABORT and set the Cancelled interrupt |
| | ABORT_RESTART | | | 1 | Abort ongoing acquisition, up on return Restart group from first channel. |
| | ABORT_RESUME | | | 2 | Abort ongoing acquisition, up on return Resume group from aborted channel<br>If averaging, discard averaging results so far and restart averaging. |
| | FINISH_RESUME | | | 3 | Complete ongoing acquisition (including averaging), up on return Resume group from next channel |
| 11 | GROUP_END | RW | R | 1 | 0: continue group with next channel<br>1: last channel of a group.<br><br>Note that for the channel with the highest index (SAR_CH_NR) this always needs to be set |
| 31 | DONE_LEVEL | RW | R | 0 | select level or pulse for 'tr_ch_done' trigger output<br>Also see POST_CTL.TR_DONE_GRP_VIO |
| | PULSE | | | 0 | tr_ch_done generates a 2 cycle pulse (clk_sys), no need to read the result to clear (also no ch_overflow detection) |
| | LEVEL | | | 1 | tr_ch_done is a level output until the result register is read (typical for DW usage, this also enables ch_overflow detection when DW is too slow) |

### 21.5.1.18.2 PASS_SAR_CH_SAMPLE_CTL

**Description:** Sample control.
**Address:** 0x40900804
**Offset:** 0x4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Make sure the channel or the IP is disabled before changing this register
**Default:** Undefined as one or more bit fields have a default value that is undefined

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | PORT_ADDR [7:6] | | PIN_ADDR [5:0] | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | OVERLAP_DIAG [15:14] | | PRECOND_MODE [13:12] | | EXT_MUX _EN [11:11] | EXT_MUX_SEL [10:8] | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | SAMPLE_TIME [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | ALT_CAL [31:31] | None [30:28] | | | SAMPLE_TIME [27:24] | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:5 | PIN_ADDR | RW | R | Undefined | Address of the analog signal (pin) to be sampled by this channel<br>- 0..31 : Vout = AN0..31, select corresponding analog input<br>- 32: Vout = Vmotor, select motor input<br>- 33: Vout = Vaux, select auxiliary input<br>- 34: Vout = AmuxbusA<br>- 35: Vout = AmuxbusB<br>- 36: Vout = Vccd<br>- 37: Vout = Vdda<br>- 38: Vout = Vbg, Bandgap voltage from SRSS<br>- 39: Vout = Vtemp, select temperature sensor. Make sure that only 1 ADC is allowed to use this.<br>- 40..61: Vout = undefined, reserved for future products<br>- 62: Vout = VrefL (VrefL actually bypasses the SARMUX (XSL))<br>- 63: Vout = VrefH (VrefH actually bypasses the SARMUX (XSH))<br><br>Note: When PORT_ADDR is not set to SARMUX0, pin addresses from 32-63 are not available. Only addresses 0-31 can be accessed from SARMUX1-3 |
| 6:7 | PORT_ADDR | RW | R | Undefined | Select the physical port. This field is only valid for ADC0.<br>ADC0 can control and connect to the SARMUX of the neighboring ADC1-3. This requires the corresponding ADC to be off while the SARMUX is left on.<br>When ADC0 controls another SARMUX it uses the PIN_ADDR, EXT_MUX_EN/SEL of this channel to control the other SARMUX. |
| | SARMUX0 | | | 0 | ADC uses it's own SARMUX |
| | SARMUX1 | | | 1 | ADC0 uses SARMUX1 (only valid for ADC0, undefined result if used for ADC1-3) |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| | SARMUX2 | | | 2 | ADC0 uses SARMUX2 (only valid for ADC0, undefined result if used for ADC1-3) |
| | SARMUX3 | | | 3 | ADC0 uses SARMUX3 (only valid for ADC0, undefined result if used for ADC1-3) |
| 8:10 | EXT_MUX_SEL | RW | R | Undefined | External analog mux select.<br>This bit setting is related to EXT_MUX[x]_y on pin assignment.<br>0x0: Select EXT_MUX[x]_0 pin<br>0x1: Select EXT_MUX[x]_1 pin |
| 11 | EXT_MUX_EN | RW | R | Undefined | External analog mux enable.<br>This enable can be used as enable (chip select) for the external analog mux (this enable is not used as enable for the GPIO output driver).<br>This enable also prevents unnecessary toggle activity on the select signals of the external analog mux. When this enable is low EXT_MUX_SEL value will be ignored and the previous value will be maintained.<br>Note that an external analog mux can only be used in combination with a pin input, i.e. PIN_ADDR<32 or Vmotor. If an internal signal is selected this enable should be 0. |
| 12:13 | PRECOND_MODE | RW | R | Undefined | Select preconditioning mode.<br>Preconditioning (dis)charges the SAR sample capacitor to the selected reference voltage for PRECOND_TIME (global) cycles, a break before make cycle will be inserted before sampling starts (SAMPLE_TIME). |
| | OFF | | | 0 | No preconditioning |
| | VREFL | | | 1 | Discharge to VREFL |
| | VREFH | | | 2 | Charge to VREFH |
| | DIAG | | | 3 | Connect the Diagnostic reference output during preconditioning. The Diagnostic reference should be configured to output a reference voltage.<br>Note: this selection is mutual exclusive with using the Diagnostic reference to supply an ibias current for OVERLAP. |
| 14:15 | OVERLAP_DIAG | RW | R | Undefined | Select Overlap mode or SARMUX Diagnostics, in both cases the Diagnostic reference is used.<br>With Overlap the Diagnostic reference typically sources or sinks a small current which is connected at the same time as the analog signal being sampled.<br>For SARMUX Diagnostics the Diagnostic reference should provide a reference voltage which is selected at the SARMUX input instead of the normal analog signal being sampled. |
| | OFF | | | 0 | No overlap or SARMUX Diagnostics |
| | HALF | | | 1 | Sample the selected analog input for 2 SAMPLE_TIME periods. During the first period use overlap sampling, i.e. connect both the analog input and Diagnostic reference. During second period only connect the analog input. |
| | FULL | | | 2 | Like normal sample the selected analog input for a single SAMPLE_TIME period but use overlap sampling, i.e. connect both the analog input and Diagnostic reference. |
| | MUX_DIAG | | | 3 | Select Diagnostic reference instead of analog signal at the input of the SARMUX. This enables a functional safety check of the SARMUX analog connections. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 16:27 | SAMPLE_TIME | RW | R | Undefined | Sample time (aperture) in ADC clock cycles. Minimum is 1 (0 gives the same result as 1), minimum time needed for proper settling is at least 412ns, i.e.11 clock cycles at the max frequency of 26.7MHz. |
| 31 | ALT_CAL | RW | R | Undefined | Use alternate calibration values instead of the current calibration values.<br>This allows the firmware to allocate one or more channels to quietly re-calibrate the ADC in the background of regular processing.<br>0 = use regular calibration values (ANA/DIG_CAL)<br>1 = use alternate calibration values (ANA/DIG_CAL_ALT)<br>Note: typically calibration measurements select VrefL (PIN_ADDR=62) or VrefH (PIN_ADDR=63) |

### 21.5.1.18.3 PASS_SAR_CH_POST_CTL

**Description:** Post processing control
**Address:** 0x40900808
**Offset:** 0x8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Make sure the channel or the IP is disabled before changing this register
**Default:** Undefined as one or more bit fields have a default value that is undefined

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | SIGN_EXT [7:7] | LEFT_ALIGN [6:6] | None [5:3] | | | POST_PROC [2:0] | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | AVG_CNT [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | RANGE_MODE [23:22] | | None [21:21] | SHIFT_R [20:16] | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:26] | | | | | | TR_DONE_GRP_VIO [25:25] | None [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:2 | POST_PROC | RW | R | Undefined | Post processing |
| | NONE | | | 0 | No postprocessing |
| | AVG | | | 1 | Averaging |
| | AVG_RANGE | | | 2 | Averaging followed by Range detect |
| | RANGE | | | 3 | Range detect |
| | RANGE_PULSE | | | 4 | Range detect followed by pulse detect |
| | RESERVED0 | | | 5 | N/A |
| | RESERVED1 | | | 6 | N/A |
| | RESERVED2 | | | 7 | N/A |
| 6 | LEFT_ALIGN | RW | R | Undefined | Left or right align data in result[15:0].<br>0: the data is right aligned in result[11:0], with sign extension to 16 bits if enabled<br>1: the data is left aligned in result[15:4] with the lower nibble 0. Caveat if the result was more than 12 bits (e.g. after averaging) then the bits above 12 will be discarded. |
| 7 | SIGN_EXT | RW | R | Undefined | Output data is sign extended |
| | UNSIGNED | | | 0 | Default: result data is unsigned (zero extended if needed) |
| | SIGNED | | | 1 | Result data is signed (sign extended if needed) |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 8:15 | AVG_CNT | RW | R | Undefined | Either averaging count (minus 1) or Pulse positive reload value<br><br>Averaging Count for channels that have averaging enabled. A channel will be sampled (AVG_CNT+1) = [1..256] times.<br>The signal will be acquired back to back (1st order accumulate and dump filter), the average result is calculated and stored and then the next enabled channel is sampled.<br>If more than 16 sample are taken (AVG_CNT>=16) then AVG_SHIFT must be set so that the result after shifting fits in 16 bits<br><br>Pulse detect positive reload value PULSE_POS_RL[7:0] |
| 16:20 | SHIFT_R | RW | R | Undefined | Either Shift Right (no pulse detection) or Pulse negative reload value (if pulse detection is enabled)<br><br>Shift right SHIFT_R[3:0] = [0..12]: the result (typically after averaging) is shifted right as specified here. Software has to make sure that the result fits in less than 16 bits.<br>Any value >12 will be treated as 12, bit [4] is always ignored. This can also be used to fit the 12-bit result in 8 bits.<br><br>Pulse detect negative reload value PULSE_NEG_RL[4:0] |
| 22:23 | RANGE_MODE | RW | R | Undefined | Range detect mode |
| | BELOW_LO | | | 0 | Below Low threshold (result < Lo) |
| | INSIDE_RANGE | | | 1 | Inside range (Lo <= result < Hi) |
| | ABOVE_HI | | | 2 | Above high threshold (Hi <= result) |
| | OUTSIDE_RANGE | | | 3 | Outside range (result < Lo \|\| Hi <= result) |
| 25 | TR_DONE_GRP_VIO | RW | R | Undefined | Select tr_sar_ch_done mode for last channel of a group, ignored for all other channels<br>Also see TR_CTL.DONE_LEVEL |
| | DONE | | | 0 | Default: tr_sar_ch_done is set when the group is done |
| | GRP_RANGE_VIO | | | 1 | tr_sar_ch_done is only set if any of the channels in the group has a Range Violation. This mode is ignored if this is not the last channel in the group.<br>Note that if none of the channels in the group have Range detection enabled then the trigger will never get set. |

### 21.5.1.18.4 PASS_SAR_CH_RANGE_CTL

**Description:** Range thresholds
**Address:** 0x4090080C
**Offset:** 0xC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Make sure the channel or the IP is disabled before changing this register
**Default:** Undefined as one or more bit fields have a default value that is undefined

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | RANGE_LO [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | RANGE_LO [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | RANGE_HI [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | RANGE_HI [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | RANGE_LO | RW | R | Undefined | Range detect low threshold (Lo) |
| 16:31 | RANGE_HI | RW | R | Undefined | Range detect high threshold (Hi) |

### 21.5.1.18.5 PASS_SAR_CH_INTR

**Description:** Interrupt request register.
**Address:** 0x40900810
**Offset:** 0x10
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** interrupts for one channel
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:3] | | | | | GRP_OVERFLOW [2:2] | GRP_CANCELLED [1:1] | GRP_DONE [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:11] | | | | | CH_OVERFLOW [10:10] | CH_PULSE [9:9] | CH_RANGE [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | GRP_DONE | RW1C | RW1S | 0 | Done Interrupt: hardware sets this interrupt for the last channel of a group if the group scan is done. Write with '1' to clear bit. |
| 1 | GRP_CANCELLED | RW1C | RW1S | 0 | Cancelled Interrupt: hardware sets this interrupt for the last channel of a group if the group scan was preempted and CANCELLED. Note that it is possible that also the GRP_DONE interrupt is set. If that is the case one or more new triggers were detected while the group was already busy, i.e. triggers are too fast. Write with '1' to clear bit. |
| 2 | GRP_OVERFLOW | RW1C | RW1S | 0 | Overflow Interrupt: hardware sets this interrupt for the last channel of a group if the group scan is done and the Done interrupt is already (still) pending. Write with '1' to clear bit. |
| 8 | CH_RANGE | RW1C | RW1S | 0 | Range detect Interrupt: hardware sets this interrupt for each channel if the conversion result (after averaging) of that channel met the condition specified by the SAR_RANGE registers. This interrupt is mutual exclusive with Pulse detect interrupt. Write with '1' to clear bit. |
| 9 | CH_PULSE | RW1C | RW1S | 0 | Pulse detect Interrupt: hardware sets this interrupt for each channel if the positive pulse counter reaches zero. This interrupt is mutual exclusive with Range detect interrupt. Write with '1' to clear bit. |
| 10 | CH_OVERFLOW | RW1C | RW1S | 0 | Channel overflow Interrupt: hardware sets this interrupt for each channel if a new Pulse or Range interrupt is detected while the interrupt is still pending or when DW did not acknowledge data pickup. Write with '1' to clear bit. |

### 21.5.1.18.6 PASS_SAR_CH_INTR_SET

**Description:** Interrupt set request register
**Address:** 0x40900814
**Offset:** 0x14
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** Not really a register, intended for verification/debug. When read, this register reflects the interrupt request register.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:3] | | | | | GRP_OVERFLOW_SET [2:2] | GRP_CANCELLED_SET [1:1] | GRP_DONE_SET [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:11] | | | | | CH_OVERFLOW_SET [10:10] | CH_PULSE_SET [9:9] | CH_RANGE_SET [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | GRP_DONE_SET | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt request register. |
| 1 | GRP_CANCELLED_SET | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt request register. |
| 2 | GRP_OVERFLOW_SET | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt request register. |
| 8 | CH_RANGE_SET | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt request register. |
| 9 | CH_PULSE_SET | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt request register. |
| 10 | CH_OVERFLOW_SET | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt request register. |

### 21.5.1.18.7 PASS_SAR_CH_INTR_MASK

**Description:** Interrupt mask register.
**Address:** 0x40900818
**Offset:** 0x18
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:3] | | | | | GRP_OVERFLOW_MASK [2:2] | GRP_CANCELLED_MASK [1:1] | GRP_DONE_MASK [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:11] | | | | | CH_OVERFLOW_MASK [10:10] | CH_PULSE_MASK [9:9] | CH_RANGE_MASK [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | GRP_DONE_MASK | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |
| 1 | GRP_CANCELLED_MASK | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |
| 2 | GRP_OVERFLOW_MASK | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |
| 8 | CH_RANGE_MASK | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |
| 9 | CH_PULSE_MASK | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |
| 10 | CH_OVERFLOW_MASK | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |

### 21.5.1.18.8 PASS_SAR_CH_INTR_MASKED

**Description:** Interrupt masked request register
**Address:** 0x4090081C
**Offset:** 0x1C
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** If the value is not zero then the SAR interrupt signal to the NVIC is high. When read, this register reflects a bitwise AND between the interrupt request and mask registers.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:3] | | | | | GRP_OVERFLOW_MASKED [2:2] | GRP_CANCELLED_MASKED [1:1] | GRP_DONE_MASKED [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:11] | | | | | CH_OVERFLOW_MASKED [10:10] | CH_PULSE_MASKED [9:9] | CH_RANGE_MASKED [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | GRP_DONE_MASKED | R | W | 0 | Logical and of corresponding request and mask bits. |
| 1 | GRP_CANCELLED_MASKED | R | W | 0 | Logical and of corresponding request and mask bits. |
| 2 | GRP_OVERFLOW_MASKED | R | W | 0 | Logical and of corresponding request and mask bits. |
| 8 | CH_RANGE_MASKED | R | W | 0 | Logical and of corresponding request and mask bits. |
| 9 | CH_PULSE_MASKED | R | W | 0 | Logical and of corresponding request and mask bits. |
| 10 | CH_OVERFLOW_MASKED | R | W | 0 | Logical and of corresponding request and mask bits. |

### 21.5.1.18.9 PASS_SAR_CH_WORK

**Description:** Working data register
**Address:** 0x40900820
**Offset:** 0x20
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** Undefined as one or more bit fields have a default value that is undefined

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | WORK [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | WORK [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALID_MIR [31:31] | PULSE_MIR [30:30] | RANGE_MIR [29:29] | ABOVE_HI_MIR [28:28] | None [27:24] | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | WORK | R | RW | Undefined | SAR conversion working data of the channel. The data is written here right after sampling this channel. |
| 28 | ABOVE_HI_MIR | R | W | 0 | mirror bit of the corresponding ABOVE_HI bit |
| 29 | RANGE_MIR | R | W | 0 | mirror bit of corresponding bit in WORK_RANGE register |
| 30 | PULSE_MIR | R | W | 0 | mirror bit of corresponding bit in WORK_PULSE register |
| 31 | VALID_MIR | R | W | 0 | mirror bit of corresponding bit in WORK_VALID register |

### 21.5.1.18.10 PASS_SAR_CH_RESULT

**Description:** Result data register
**Address:** 0x40900824
**Offset:** 0x24
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** Undefined as one or more bit fields have a default value that is undefined

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | RESULT [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | RESULT [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALID_MIR [31:31] | PULSE_INTR_MIR [30:30] | RANGE_INTR_MIR [29:29] | ABOVE_HI_MIR [28:28] | None [27:24] | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | RESULT | R | W | Undefined | SAR conversion result of the channel. The data is copied here from the WORK field after all enabled channels in this scan have been sampled. |
| 28 | ABOVE_HI_MIR | R | W | 0 | mirror bit of the corresponding ABOVE_HI bit |
| 29 | RANGE_INTR_MIR | R | W | 0 | mirror bit of INTR.CH_RANGE bit |
| 30 | PULSE_INTR_MIR | R | W | 0 | mirror bit of INTR.CH_PULSE bit |
| 31 | VALID_MIR | R | W | 0 | mirror bit of the corresponding bit in RESULT_VALID register |

### 21.5.1.18.11 PASS_SAR_CH_GRP_STAT

**Description:** Group status register
**Address:** 0x40900828
**Offset:** 0x28
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** This register contains the status information required for a coherent read for the AutoSAR 'ADC Channel Group Status Service'
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:3] | | | | | GRP_OVERFLOW [2:2] | GRP_CANCELLED [1:1] | GRP_COMPLETE [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:11] | | | | | CH_OVERFLOW [10:10] | CH_PULSE_COMPLETE [9:9] | CH_RANGE_COMPLETE [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:17] | | | | | | | GRP_BUSY [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | GRP_COMPLETE | R | W | 0 | Group acquisition complete.<br>This is a copy of the INTR.GRP_DONE bit. |
| 1 | GRP_CANCELLED | R | W | 0 | Group Cancelled.<br>This is a copy of the INTR.GRP_CANCELLED bit. |
| 2 | GRP_OVERFLOW | R | W | 0 | Group Overflow.<br>This is a copy of the INTR.GRP_OVERFLOW bit. |
| 8 | CH_RANGE_COMPLETE | R | W | 0 | Channel Range complete.<br>This is a copy of the INTR.CH_RANGE bit. |
| 9 | CH_PULSE_COMPLETE | R | W | 0 | Channel Pulse complete.<br>This is a copy of the INTR.CH_PULSE bit. |
| 10 | CH_OVERFLOW | R | W | 0 | Channel Overflow.<br>This is a copy of the INTR.CH_OVERFLOW bit. |
| 16 | GRP_BUSY | R | W | 0 | Group acquisition busy.<br>This is a copy of the TR_PENDING bit of the first channel of the group. |

### 21.5.1.18.12 PASS_SAR_CH_ENABLE

**Description:** Enable register
**Address:** 0x40900838
**Offset:** 0x38
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:1] | | | | | | | CHAN_EN [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | CHAN_EN | RW | R | 0 | Channel enable.<br>- 0: the corresponding channel is disabled. Corresponding trigger will be reset immediately.<br>- 1: the corresponding channel is enabled.<br><br>Note: To disable a group either stop the trigger first or begin with disabling the lowest channel first. To enable a group either start with enabling the last channel first and the first channel last, or start the trigger after all channels are enabled. If these rules are not followed the result is undefined. |

### 21.5.1.18.13 PASS_SAR_CH_TR_CMD

**Description:** Software triggers
**Address:** 0x4090083C
**Offset:** 0x3C
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:1] | | | | | | | START [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | START | RW1S | A | 0 | Software start trigger. When written with '1', a start trigger is generated which sets the corresponding TR_PEND bit (only if the channel is enabled). A read always returns a 0. |

### 21.5.2 EPASS_MMIO

#### 21.5.2.1 PASS_PASS_CTL

**Description:** PASS control register
**Address:** 0x409F0000
**Offset:** 0x0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:6] | | SUPPLY_MON_LVL_B [5:5] | SUPPLY_MON_EN_B [4:4] | None [3:2] | | SUPPLY_MON_LVL_A [1:1] | SUPPLY_MON_EN_A [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:23] | REFBUF_MODE [22:21] | | None [20:16] | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:31] | DBG_FREEZE_EN [30:28] | | | None [27:24] | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | SUPPLY_MON_EN_A | RW | R | 0 | Supply monitor enable for AMUXBUS_A (amuxbus_a_mon) |
| 1 | SUPPLY_MON_LVL_A | RW | R | 0 | Supply monitor level select for AMUXBUS_A |
| | VRL | | | 0 | amuxbus_a_mon = VRL |
| | VRH | | | 1 | amuxbus_a_mon = VRH |
| 4 | SUPPLY_MON_EN_B | RW | R | 0 | Supply monitor enable for AMUXBUS_B (amuxbus_b_mon) |
| 5 | SUPPLY_MON_LVL_B | RW | R | 0 | Supply monitor level select for AMUXBUS_B |
| | VRL | | | 0 | amuxbus_b_mon = VRL |
| | VRH | | | 1 | amuxbus_b_mon = VRH |
| 21:22 | REFBUF_MODE | RW | R | 0 | Reference mode.<br>The reference needs to be present when using TEMP sensor or diagnostic reference (in addition to SAR.DIAG_CTL.DIAG_EN).<br>Note that setting this mode is not required for the ADC operation itself. |
| | OFF | | | 0 | No reference |
| | ON | | | 1 | Reference = buffered Vbg from SRSS |
| | RESERVED | | | 2 | undefined |
| | BYPASS | | | 3 | Reference = unbuffered Vbg from SRSS |
| 28:30 | DBG_FREEZE_EN | RW | R | 0 | Debug pause enable, 1 per ADC.<br>When set a high tr_debug_freeze trigger will prevent the scheduler from starting acquisitions on a new channel. Note that averaging for an already started channel will be completed. |

### 21.5.2.2 PASS_SAR_TR_IN_SEL

**Description:** per SAR generic input trigger select
**Address:** 0x409F0020
**Offset:** 0x20
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** forward 5 out of max 16 generic input triggers to one SAR instance (there are 5 generic input triggers per SAR)
**Default:** 0x43210

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | IN1_SEL [7:4] | | | | IN0_SEL [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | IN3_SEL [15:12] | | | | IN2_SEL [11:8] | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:20] | | | | IN4_SEL [19:16] | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | IN0_SEL | RW | R | 0 | Select generic trigger for SAR generic trigger input 0 |
| 4:7 | IN1_SEL | RW | R | 1 | Select generic trigger for SAR generic trigger input 1 |
| 8:11 | IN2_SEL | RW | R | 2 | Select generic trigger for SAR generic trigger input 2 |
| 12:15 | IN3_SEL | RW | R | 3 | Select generic trigger for SAR generic trigger input 3 |
| 16:19 | IN4_SEL | RW | R | 4 | Select generic trigger for SAR generic trigger input 4 |

### 21.5.2.3 PASS_SAR_TR_OUT_SEL

**Description:** per SAR generic output trigger select
**Address:** 0x409F0040
**Offset:** 0x40
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** forward 2 of the up to 64 SAR triggers (tr_sar_ch_done + tr_sar_ch_rangevio) to a generic output trigger
**Default:** 0x100

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:6] | | OUT0_SEL [5:0] | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:14] | | OUT1_SEL [13:8] | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:5 | OUT0_SEL | RW | R | 0 | Select SAR output trigger for generic trigger output 0<br>0-31: selects a tr_sar_ch_done trigger<br>32-63: selects a tr_sar_ch_rangvio trigger |
| 8:13 | OUT1_SEL | RW | R | 1 | Select SAR output trigger for generic trigger output 1 |

### 21.5.2.4 PASS_TEST_CTL

**Description:** Test control bits
**Address:** 0x409F0080
**Offset:** 0x80
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** Note: All bits besides 6, 8, 9 are reserved, and should not be modified by the user
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:7] | TS_CAL_VI_SEL [6:6] | TS_CAL_DIODE_PNP_EN [5:5] | TS_CAL_DIODE_EN [4:4] | TS_CAL_VE_OUT [3:3] | TS_CAL_VB_OUT [2:2] | None [1:1] | TS_CAL_CUR_IN [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:13] | | | TS_CAL_SPARE [12:12] | None [11:10] | | TS_CAL_CUR_SEL [9:8] | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | TS_CAL_CUR_IN | RW | R | 0 | External current input switch control, for Temperature Sensor Calibration |
| 2 | TS_CAL_VB_OUT | RW | R | 0 | Voltage Base switch control, for Temperature Sensor Calibration |
| 3 | TS_CAL_VE_OUT | RW | R | 0 | Voltage Emitter switch control, for Temperature Sensor Calibration |
| 4 | TS_CAL_DIODE_EN | RW | R | 0 | Diode Enable, disconnect or connect the base and collector terminal of the BJT |
| 5 | TS_CAL_DIODE_PNP_EN | RW | R | 0 | Enable signal for PNP transistor. This transistor will be used only during calibration for accurate estimation of chip temp.<br>0 = Turn PNP off<br>1 = Configure PNP as a diode (short base and collector) |
| 6 | TS_CAL_VI_SEL | RW | R | 0 | Select current or voltage output on 'v_temp' pin, for Temperature Sensor Calibration |
| | CURRENT | | | 0 | Current is selected |
| | VOLTAGE | | | 1 | Voltage is selected |
| 8:9 | TS_CAL_CUR_SEL | RW | R | 0 | Select the current going into the BJT, for Temperature Sensor Calibration |
| | I_1U | | | 0 | Select 1 uA |
| | I_2U | | | 1 | Select 2 uA |
| | I_5U | | | 2 | Select 5 uA |
| | I_10U | | | 3 | Select 10 uA |
| 12 | TS_CAL_SPARE | RW | R | 0 | Spare |

# 22 PERI

**Description** Peripheral interconnect
**Base Address** 0x40000000
**Size** 0x10000
**Slave Num** MMIO0 - 0

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_TIMEOUT_CTL | 0x40000200 | FULL | Timeout control |
| PERI_TR_CMD | 0x40000220 | FULL | Trigger command |
| PERI_ECC_CTL | 0x40002000 | FULL | ECC control |

## 22.1 GR 0

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_GR0_SL_CTL | 0x40004010 | FULL | Slave control<br>Note:ENABLED_3 ENABLED_4 ENABLED_5 ENABLED_6 ENABLED_7 ENABLED_8 ENABLED_9 ENABLED_10 ENABLED_11 ENABLED_12 ENABLED_13 ENABLED_14 ENABLED_15 are not available for this register |

## 22.2 GR 1

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_GR1_SL_CTL | 0x40004050 | FULL | Slave control<br>Note:ENABLED_1 ENABLED_2 ENABLED_3 ENABLED_4 ENABLED_5 ENABLED_6 ENABLED_7 ENABLED_8 ENABLED_9 ENABLED_10 ENABLED_11 ENABLED_12 ENABLED_13 ENABLED_14 ENABLED_15 are not available for this register |

## 22.3 GR 2

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_GR2_SL_CTL | 0x40004090 | FULL | Slave control<br>Note:ENABLED_12 ENABLED_13 ENABLED_14 ENABLED_15 are not available for this register |

## 22.4 GR 3

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_GR3_CLOCK_CTL | 0x400040C0 | FULL | Clock control |
| PERI_GR3_SL_CTL | 0x400040D0 | FULL | Slave control<br>Note:ENABLED_5 ENABLED_6 ENABLED_7 ENABLED_8 ENABLED_9 ENABLED_10 ENABLED_11 ENABLED_12 ENABLED_13 ENABLED_14 ENABLED_15 are not available for this register |

## 22.5 GR 4

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_GR4_CLOCK_CTL | 0x40004100 | FULL | Clock control |
| PERI_GR4_SL_CTL | 0x40004110 | FULL | Slave control<br>Note:ENABLED_4 ENABLED_5 ENABLED_6 ENABLED_7 ENABLED_8 ENABLED_9 ENABLED_10 ENABLED_11 ENABLED_12 ENABLED_13 ENABLED_14 ENABLED_15 are not available for this register |

## 22.6 GR 5

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_GR5_CLOCK_CTL | 0x40004140 | FULL | Clock control |
| PERI_GR5_SL_CTL | 0x40004150 | FULL | Slave control<br>Note:ENABLED_5 ENABLED_6 ENABLED_7 ENABLED_8 ENABLED_9 ENABLED_10 ENABLED_11 ENABLED_12 ENABLED_13 ENABLED_14 ENABLED_15 are not available for this register |

## 22.7 GR 6

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_GR6_CLOCK_CTL | 0x40004180 | FULL | Clock control |
| PERI_GR6_SL_CTL | 0x40004190 | FULL | Slave control<br>Note:ENABLED_11 ENABLED_12 ENABLED_13 ENABLED_14 ENABLED_15 are not available for this register |

## 22.8 GR 8

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_GR8_CLOCK_CTL | 0x40004200 | FULL | Clock control |
| PERI_GR8_SL_CTL | 0x40004210 | FULL | Slave control<br>Note:ENABLED_3 ENABLED_4 ENABLED_5 ENABLED_6 ENABLED_7 ENABLED_8 ENABLED_9 ENABLED_10 ENABLED_11 ENABLED_12 ENABLED_13 ENABLED_14 ENABLED_15 are not available for this register |

## 22.9 GR 9

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_GR9_CLOCK_CTL | 0x40004240 | FULL | Clock control |
| PERI_GR9_SL_CTL | 0x40004250 | FULL | Slave control<br>Note:ENABLED_1 ENABLED_2 ENABLED_3 ENABLED_4 ENABLED_5 ENABLED_6 ENABLED_7 ENABLED_8 ENABLED_9 ENABLED_10 ENABLED_11 ENABLED_12 ENABLED_13 ENABLED_14 ENABLED_15 are not available for this register |

## 22.10 TR_GR 0

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_TR_GR0_TR_CTL0 | 0x40008000 | FULL | Trigger control register |
| PERI_TR_GR0_TR_CTL1 | 0x40008004 | FULL | Trigger control register |
| PERI_TR_GR0_TR_CTL2 | 0x40008008 | FULL | Trigger control register |
| PERI_TR_GR0_TR_CTL3 | 0x4000800C | FULL | Trigger control register |
| PERI_TR_GR0_TR_CTL4 | 0x40008010 | FULL | Trigger control register |
| PERI_TR_GR0_TR_CTL5 | 0x40008014 | FULL | Trigger control register |
| PERI_TR_GR0_TR_CTL6 | 0x40008018 | FULL | Trigger control register |
| PERI_TR_GR0_TR_CTL7 | 0x4000801C | FULL | Trigger control register |
| PERI_TR_GR0_TR_CTL8 | 0x40008020 | FULL | Trigger control register |
| PERI_TR_GR0_TR_CTL9 | 0x40008024 | FULL | Trigger control register |
| PERI_TR_GR0_TR_CTL10 | 0x40008028 | FULL | Trigger control register |
| PERI_TR_GR0_TR_CTL11 | 0x4000802C | FULL | Trigger control register |
| PERI_TR_GR0_TR_CTL12 | 0x40008030 | FULL | Trigger control register |
| PERI_TR_GR0_TR_CTL13 | 0x40008034 | FULL | Trigger control register |
| PERI_TR_GR0_TR_CTL14 | 0x40008038 | FULL | Trigger control register |
| PERI_TR_GR0_TR_CTL15 | 0x4000803C | FULL | Trigger control register |

## 22.11 TR_GR 1

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_TR_GR1_TR_CTL0 | 0x40008400 | FULL | Trigger control register |
| PERI_TR_GR1_TR_CTL1 | 0x40008404 | FULL | Trigger control register |
| PERI_TR_GR1_TR_CTL2 | 0x40008408 | FULL | Trigger control register |
| PERI_TR_GR1_TR_CTL3 | 0x4000840C | FULL | Trigger control register |
| PERI_TR_GR1_TR_CTL4 | 0x40008410 | FULL | Trigger control register |
| PERI_TR_GR1_TR_CTL5 | 0x40008414 | FULL | Trigger control register |
| PERI_TR_GR1_TR_CTL6 | 0x40008418 | FULL | Trigger control register |
| PERI_TR_GR1_TR_CTL7 | 0x4000841C | FULL | Trigger control register |
| PERI_TR_GR1_TR_CTL8 | 0x40008420 | FULL | Trigger control register |
| PERI_TR_GR1_TR_CTL9 | 0x40008424 | FULL | Trigger control register |
| PERI_TR_GR1_TR_CTL10 | 0x40008428 | FULL | Trigger control register |
| PERI_TR_GR1_TR_CTL11 | 0x4000842C | FULL | Trigger control register |
| PERI_TR_GR1_TR_CTL12 | 0x40008430 | FULL | Trigger control register |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_TR_GR1_TR_CTL13 | 0x40008434 | FULL | Trigger control register |
| PERI_TR_GR1_TR_CTL14 | 0x40008438 | FULL | Trigger control register |
| PERI_TR_GR1_TR_CTL15 | 0x4000843C | FULL | Trigger control register |

## 22.12 TR_GR 2

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_TR_GR2_TR_CTL0 | 0x40008800 | FULL | Trigger control register |
| PERI_TR_GR2_TR_CTL1 | 0x40008804 | FULL | Trigger control register |
| PERI_TR_GR2_TR_CTL2 | 0x40008808 | FULL | Trigger control register |
| PERI_TR_GR2_TR_CTL3 | 0x4000880C | FULL | Trigger control register |
| PERI_TR_GR2_TR_CTL4 | 0x40008810 | FULL | Trigger control register |
| PERI_TR_GR2_TR_CTL5 | 0x40008814 | FULL | Trigger control register |
| PERI_TR_GR2_TR_CTL6 | 0x40008818 | FULL | Trigger control register |
| PERI_TR_GR2_TR_CTL7 | 0x4000881C | FULL | Trigger control register |
| PERI_TR_GR2_TR_CTL8 | 0x40008820 | FULL | Trigger control register |
| PERI_TR_GR2_TR_CTL9 | 0x40008824 | FULL | Trigger control register |
| PERI_TR_GR2_TR_CTL10 | 0x40008828 | FULL | Trigger control register |
| PERI_TR_GR2_TR_CTL11 | 0x4000882C | FULL | Trigger control register |
| PERI_TR_GR2_TR_CTL12 | 0x40008830 | FULL | Trigger control register |
| PERI_TR_GR2_TR_CTL13 | 0x40008834 | FULL | Trigger control register |
| PERI_TR_GR2_TR_CTL14 | 0x40008838 | FULL | Trigger control register |
| PERI_TR_GR2_TR_CTL15 | 0x4000883C | FULL | Trigger control register |

## 22.13 TR_GR 3

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_TR_GR3_TR_CTL0 | 0x40008C00 | FULL | Trigger control register |
| PERI_TR_GR3_TR_CTL1 | 0x40008C04 | FULL | Trigger control register |
| PERI_TR_GR3_TR_CTL2 | 0x40008C08 | FULL | Trigger control register |
| PERI_TR_GR3_TR_CTL3 | 0x40008C0C | FULL | Trigger control register |
| PERI_TR_GR3_TR_CTL4 | 0x40008C10 | FULL | Trigger control register |
| PERI_TR_GR3_TR_CTL5 | 0x40008C14 | FULL | Trigger control register |
| PERI_TR_GR3_TR_CTL6 | 0x40008C18 | FULL | Trigger control register |
| PERI_TR_GR3_TR_CTL7 | 0x40008C1C | FULL | Trigger control register |

## 22.14 TR_GR 4

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_TR_GR4_TR_CTL0 | 0x40009000 | FULL | Trigger control register |
| PERI_TR_GR4_TR_CTL1 | 0x40009004 | FULL | Trigger control register |
| PERI_TR_GR4_TR_CTL2 | 0x40009008 | FULL | Trigger control register |
| PERI_TR_GR4_TR_CTL3 | 0x4000900C | FULL | Trigger control register |
| PERI_TR_GR4_TR_CTL4 | 0x40009010 | FULL | Trigger control register |
| PERI_TR_GR4_TR_CTL5 | 0x40009014 | FULL | Trigger control register |
| PERI_TR_GR4_TR_CTL6 | 0x40009018 | FULL | Trigger control register |
| PERI_TR_GR4_TR_CTL7 | 0x4000901C | FULL | Trigger control register |
| PERI_TR_GR4_TR_CTL8 | 0x40009020 | FULL | Trigger control register |
| PERI_TR_GR4_TR_CTL9 | 0x40009024 | FULL | Trigger control register |
| PERI_TR_GR4_TR_CTL10 | 0x40009028 | FULL | Trigger control register |
| PERI_TR_GR4_TR_CTL11 | 0x4000902C | FULL | Trigger control register |

## 22.15 TR_GR 5

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_TR_GR5_TR_CTL0 | 0x40009400 | FULL | Trigger control register |
| PERI_TR_GR5_TR_CTL1 | 0x40009404 | FULL | Trigger control register |
| PERI_TR_GR5_TR_CTL2 | 0x40009408 | FULL | Trigger control register |
| PERI_TR_GR5_TR_CTL3 | 0x4000940C | FULL | Trigger control register |
| PERI_TR_GR5_TR_CTL4 | 0x40009410 | FULL | Trigger control register |
| PERI_TR_GR5_TR_CTL5 | 0x40009414 | FULL | Trigger control register |
| PERI_TR_GR5_TR_CTL6 | 0x40009418 | FULL | Trigger control register |
| PERI_TR_GR5_TR_CTL7 | 0x4000941C | FULL | Trigger control register |
| PERI_TR_GR5_TR_CTL8 | 0x40009420 | FULL | Trigger control register |
| PERI_TR_GR5_TR_CTL9 | 0x40009424 | FULL | Trigger control register |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_TR_GR5_TR_CTL10 | 0x40009428 | FULL | Trigger control register |
| PERI_TR_GR5_TR_CTL11 | 0x4000942C | FULL | Trigger control register |

## 22.16 TR_GR 6

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_TR_GR6_TR_CTL0 | 0x40009800 | FULL | Trigger control register |
| PERI_TR_GR6_TR_CTL1 | 0x40009804 | FULL | Trigger control register |
| PERI_TR_GR6_TR_CTL2 | 0x40009808 | FULL | Trigger control register |
| PERI_TR_GR6_TR_CTL3 | 0x4000980C | FULL | Trigger control register |
| PERI_TR_GR6_TR_CTL4 | 0x40009810 | FULL | Trigger control register |
| PERI_TR_GR6_TR_CTL5 | 0x40009814 | FULL | Trigger control register |
| PERI_TR_GR6_TR_CTL6 | 0x40009818 | FULL | Trigger control register |
| PERI_TR_GR6_TR_CTL7 | 0x4000981C | FULL | Trigger control register |
| PERI_TR_GR6_TR_CTL8 | 0x40009820 | FULL | Trigger control register |
| PERI_TR_GR6_TR_CTL9 | 0x40009824 | FULL | Trigger control register |
| PERI_TR_GR6_TR_CTL10 | 0x40009828 | FULL | Trigger control register |
| PERI_TR_GR6_TR_CTL11 | 0x4000982C | FULL | Trigger control register |
| PERI_TR_GR6_TR_CTL12 | 0x40009830 | FULL | Trigger control register |
| PERI_TR_GR6_TR_CTL13 | 0x40009834 | FULL | Trigger control register |
| PERI_TR_GR6_TR_CTL14 | 0x40009838 | FULL | Trigger control register |
| PERI_TR_GR6_TR_CTL15 | 0x4000983C | FULL | Trigger control register |
| PERI_TR_GR6_TR_CTL16 | 0x40009840 | FULL | Trigger control register |
| PERI_TR_GR6_TR_CTL17 | 0x40009844 | FULL | Trigger control register |
| PERI_TR_GR6_TR_CTL18 | 0x40009848 | FULL | Trigger control register |
| PERI_TR_GR6_TR_CTL19 | 0x4000984C | FULL | Trigger control register |
| PERI_TR_GR6_TR_CTL20 | 0x40009850 | FULL | Trigger control register |
| PERI_TR_GR6_TR_CTL21 | 0x40009854 | FULL | Trigger control register |
| PERI_TR_GR6_TR_CTL22 | 0x40009858 | FULL | Trigger control register |
| PERI_TR_GR6_TR_CTL23 | 0x4000985C | FULL | Trigger control register |
| PERI_TR_GR6_TR_CTL24 | 0x40009860 | FULL | Trigger control register |
| PERI_TR_GR6_TR_CTL25 | 0x40009864 | FULL | Trigger control register |
| PERI_TR_GR6_TR_CTL26 | 0x40009868 | FULL | Trigger control register |
| PERI_TR_GR6_TR_CTL27 | 0x4000986C | FULL | Trigger control register |
| PERI_TR_GR6_TR_CTL28 | 0x40009870 | FULL | Trigger control register |

## 22.17 TR_GR 7

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_TR_GR7_TR_CTL0 | 0x40009C00 | FULL | Trigger control register |
| PERI_TR_GR7_TR_CTL1 | 0x40009C04 | FULL | Trigger control register |
| PERI_TR_GR7_TR_CTL2 | 0x40009C08 | FULL | Trigger control register |
| PERI_TR_GR7_TR_CTL3 | 0x40009C0C | FULL | Trigger control register |
| PERI_TR_GR7_TR_CTL4 | 0x40009C10 | FULL | Trigger control register |
| PERI_TR_GR7_TR_CTL5 | 0x40009C14 | FULL | Trigger control register |
| PERI_TR_GR7_TR_CTL6 | 0x40009C18 | FULL | Trigger control register |
| PERI_TR_GR7_TR_CTL7 | 0x40009C1C | FULL | Trigger control register |
| PERI_TR_GR7_TR_CTL8 | 0x40009C20 | FULL | Trigger control register |
| PERI_TR_GR7_TR_CTL9 | 0x40009C24 | FULL | Trigger control register |
| PERI_TR_GR7_TR_CTL10 | 0x40009C28 | FULL | Trigger control register |
| PERI_TR_GR7_TR_CTL11 | 0x40009C2C | FULL | Trigger control register |

## 22.18 TR_GR 8

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_TR_GR8_TR_CTL0 | 0x4000A000 | FULL | Trigger control register |
| PERI_TR_GR8_TR_CTL1 | 0x4000A004 | FULL | Trigger control register |
| PERI_TR_GR8_TR_CTL2 | 0x4000A008 | FULL | Trigger control register |
| PERI_TR_GR8_TR_CTL3 | 0x4000A00C | FULL | Trigger control register |
| PERI_TR_GR8_TR_CTL4 | 0x4000A010 | FULL | Trigger control register |
| PERI_TR_GR8_TR_CTL5 | 0x4000A014 | FULL | Trigger control register |
| PERI_TR_GR8_TR_CTL6 | 0x4000A018 | FULL | Trigger control register |
| PERI_TR_GR8_TR_CTL7 | 0x4000A01C | FULL | Trigger control register |
| PERI_TR_GR8_TR_CTL8 | 0x4000A020 | FULL | Trigger control register |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_TR_GR8_TR_CTL9 | 0x4000A024 | FULL | Trigger control register |
| PERI_TR_GR8_TR_CTL10 | 0x4000A028 | FULL | Trigger control register |

## 22.19 TR_GR 9

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_TR_GR9_TR_CTL0 | 0x4000A400 | FULL | Trigger control register |
| PERI_TR_GR9_TR_CTL1 | 0x4000A404 | FULL | Trigger control register |
| PERI_TR_GR9_TR_CTL2 | 0x4000A408 | FULL | Trigger control register |
| PERI_TR_GR9_TR_CTL3 | 0x4000A40C | FULL | Trigger control register |
| PERI_TR_GR9_TR_CTL4 | 0x4000A410 | FULL | Trigger control register |
| PERI_TR_GR9_TR_CTL5 | 0x4000A414 | FULL | Trigger control register |
| PERI_TR_GR9_TR_CTL6 | 0x4000A418 | FULL | Trigger control register |
| PERI_TR_GR9_TR_CTL7 | 0x4000A41C | FULL | Trigger control register |
| PERI_TR_GR9_TR_CTL8 | 0x4000A420 | FULL | Trigger control register |
| PERI_TR_GR9_TR_CTL9 | 0x4000A424 | FULL | Trigger control register |
| PERI_TR_GR9_TR_CTL10 | 0x4000A428 | FULL | Trigger control register |
| PERI_TR_GR9_TR_CTL11 | 0x4000A42C | FULL | Trigger control register |

## 22.20 TR_GR 10

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_TR_GR10_TR_CTL0 | 0x4000A800 | FULL | Trigger control register<br>Note:TR_INV TR_EDGE are not available for this register |
| PERI_TR_GR10_TR_CTL1 | 0x4000A804 | FULL | Trigger control register |
| PERI_TR_GR10_TR_CTL2 | 0x4000A808 | FULL | Trigger control register |
| PERI_TR_GR10_TR_CTL3 | 0x4000A80C | FULL | Trigger control register |
| PERI_TR_GR10_TR_CTL4 | 0x4000A810 | FULL | Trigger control register |

## 22.21 TR_GR 11

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_TR_GR11_TR_CTL0 | 0x4000AC00 | FULL | Trigger control register<br>Note:TR_INV TR_EDGE are not available for this register |
| PERI_TR_GR11_TR_CTL1 | 0x4000AC04 | FULL | Trigger control register |
| PERI_TR_GR11_TR_CTL2 | 0x4000AC08 | FULL | Trigger control register |
| PERI_TR_GR11_TR_CTL3 | 0x4000AC0C | FULL | Trigger control register |
| PERI_TR_GR11_TR_CTL4 | 0x4000AC10 | FULL | Trigger control register |

## 22.22 TR_GR 12

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_TR_GR12_TR_CTL0 | 0x4000B000 | FULL | Trigger control register<br>Note:TR_INV TR_EDGE are not available for this register |
| PERI_TR_GR12_TR_CTL1 | 0x4000B004 | FULL | Trigger control register |
| PERI_TR_GR12_TR_CTL2 | 0x4000B008 | FULL | Trigger control register |
| PERI_TR_GR12_TR_CTL3 | 0x4000B00C | FULL | Trigger control register |
| PERI_TR_GR12_TR_CTL4 | 0x4000B010 | FULL | Trigger control register |

## 22.23 TR_1TO1_GR 0

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_TR_1TO1_GR0_TR_CTL0 | 0x4000C000 | FULL | Trigger control register |
| PERI_TR_1TO1_GR0_TR_CTL1 | 0x4000C004 | FULL | Trigger control register |
| PERI_TR_1TO1_GR0_TR_CTL2 | 0x4000C008 | FULL | Trigger control register |
| PERI_TR_1TO1_GR0_TR_CTL3 | 0x4000C00C | FULL | Trigger control register |
| PERI_TR_1TO1_GR0_TR_CTL4 | 0x4000C010 | FULL | Trigger control register |
| PERI_TR_1TO1_GR0_TR_CTL5 | 0x4000C014 | FULL | Trigger control register |
| PERI_TR_1TO1_GR0_TR_CTL6 | 0x4000C018 | FULL | Trigger control register |
| PERI_TR_1TO1_GR0_TR_CTL7 | 0x4000C01C | FULL | Trigger control register |
| PERI_TR_1TO1_GR0_TR_CTL8 | 0x4000C020 | FULL | Trigger control register |
| PERI_TR_1TO1_GR0_TR_CTL9 | 0x4000C024 | FULL | Trigger control register |
| PERI_TR_1TO1_GR0_TR_CTL10 | 0x4000C028 | FULL | Trigger control register |
| PERI_TR_1TO1_GR0_TR_CTL11 | 0x4000C02C | FULL | Trigger control register |
| PERI_TR_1TO1_GR0_TR_CTL12 | 0x4000C030 | FULL | Trigger control register |
| PERI_TR_1TO1_GR0_TR_CTL13 | 0x4000C034 | FULL | Trigger control register |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_TR_1TO1_GR0_TR_CTL14 | 0x4000C038 | FULL | Trigger control register |

## 22.24 TR_1TO1_GR 1

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_TR_1TO1_GR1_TR_CTL0 | 0x4000C400 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL1 | 0x4000C404 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL2 | 0x4000C408 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL3 | 0x4000C40C | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL4 | 0x4000C410 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL5 | 0x4000C414 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL6 | 0x4000C418 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL7 | 0x4000C41C | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL8 | 0x4000C420 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL9 | 0x4000C424 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL10 | 0x4000C428 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL11 | 0x4000C42C | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL12 | 0x4000C430 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL13 | 0x4000C434 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL14 | 0x4000C438 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL15 | 0x4000C43C | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL16 | 0x4000C440 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL17 | 0x4000C444 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL18 | 0x4000C448 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL19 | 0x4000C44C | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL20 | 0x4000C450 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL21 | 0x4000C454 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL22 | 0x4000C458 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL23 | 0x4000C45C | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL24 | 0x4000C460 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL25 | 0x4000C464 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL26 | 0x4000C468 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL27 | 0x4000C46C | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL28 | 0x4000C470 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL29 | 0x4000C474 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL30 | 0x4000C478 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL31 | 0x4000C47C | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL32 | 0x4000C480 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL33 | 0x4000C484 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL34 | 0x4000C488 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL35 | 0x4000C48C | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL36 | 0x4000C490 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL37 | 0x4000C494 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL38 | 0x4000C498 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL39 | 0x4000C49C | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL40 | 0x4000C4A0 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL41 | 0x4000C4A4 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL42 | 0x4000C4A8 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL43 | 0x4000C4AC | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL44 | 0x4000C4B0 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL45 | 0x4000C4B4 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL46 | 0x4000C4B8 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL47 | 0x4000C4BC | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL48 | 0x4000C4C0 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL49 | 0x4000C4C4 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL50 | 0x4000C4C8 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL51 | 0x4000C4CC | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL52 | 0x4000C4D0 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL53 | 0x4000C4D4 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL54 | 0x4000C4D8 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL55 | 0x4000C4DC | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL56 | 0x4000C4E0 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL57 | 0x4000C4E4 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL58 | 0x4000C4E8 | FULL | Trigger control register |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_TR_1TO1_GR1_TR_CTL59 | 0x4000C4EC | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL60 | 0x4000C4F0 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL61 | 0x4000C4F4 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL62 | 0x4000C4F8 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL63 | 0x4000C4FC | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL64 | 0x4000C500 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL65 | 0x4000C504 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL66 | 0x4000C508 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL67 | 0x4000C50C | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL68 | 0x4000C510 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL69 | 0x4000C514 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL70 | 0x4000C518 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL71 | 0x4000C51C | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL72 | 0x4000C520 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL73 | 0x4000C524 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL74 | 0x4000C528 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL75 | 0x4000C52C | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL76 | 0x4000C530 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL77 | 0x4000C534 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL78 | 0x4000C538 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL79 | 0x4000C53C | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL80 | 0x4000C540 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL81 | 0x4000C544 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL82 | 0x4000C548 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL83 | 0x4000C54C | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL84 | 0x4000C550 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL85 | 0x4000C554 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL86 | 0x4000C558 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL87 | 0x4000C55C | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL88 | 0x4000C560 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL89 | 0x4000C564 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL90 | 0x4000C568 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL91 | 0x4000C56C | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL92 | 0x4000C570 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL93 | 0x4000C574 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL94 | 0x4000C578 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL95 | 0x4000C57C | FULL | Trigger control register |

## 22.25 TR_1TO1_GR 2

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_TR_1TO1_GR2_TR_CTL0 | 0x4000C800 | FULL | Trigger control register |
| PERI_TR_1TO1_GR2_TR_CTL1 | 0x4000C804 | FULL | Trigger control register |
| PERI_TR_1TO1_GR2_TR_CTL2 | 0x4000C808 | FULL | Trigger control register |
| PERI_TR_1TO1_GR2_TR_CTL3 | 0x4000C80C | FULL | Trigger control register |
| PERI_TR_1TO1_GR2_TR_CTL4 | 0x4000C810 | FULL | Trigger control register |
| PERI_TR_1TO1_GR2_TR_CTL5 | 0x4000C814 | FULL | Trigger control register |
| PERI_TR_1TO1_GR2_TR_CTL6 | 0x4000C818 | FULL | Trigger control register |
| PERI_TR_1TO1_GR2_TR_CTL7 | 0x4000C81C | FULL | Trigger control register |
| PERI_TR_1TO1_GR2_TR_CTL8 | 0x4000C820 | FULL | Trigger control register |
| PERI_TR_1TO1_GR2_TR_CTL9 | 0x4000C824 | FULL | Trigger control register |
| PERI_TR_1TO1_GR2_TR_CTL10 | 0x4000C828 | FULL | Trigger control register |
| PERI_TR_1TO1_GR2_TR_CTL11 | 0x4000C82C | FULL | Trigger control register |
| PERI_TR_1TO1_GR2_TR_CTL12 | 0x4000C830 | FULL | Trigger control register |
| PERI_TR_1TO1_GR2_TR_CTL13 | 0x4000C834 | FULL | Trigger control register |
| PERI_TR_1TO1_GR2_TR_CTL14 | 0x4000C838 | FULL | Trigger control register |
| PERI_TR_1TO1_GR2_TR_CTL15 | 0x4000C83C | FULL | Trigger control register |
| PERI_TR_1TO1_GR2_TR_CTL16 | 0x4000C840 | FULL | Trigger control register |
| PERI_TR_1TO1_GR2_TR_CTL17 | 0x4000C844 | FULL | Trigger control register |
| PERI_TR_1TO1_GR2_TR_CTL18 | 0x4000C848 | FULL | Trigger control register |
| PERI_TR_1TO1_GR2_TR_CTL19 | 0x4000C84C | FULL | Trigger control register |
| PERI_TR_1TO1_GR2_TR_CTL20 | 0x4000C850 | FULL | Trigger control register |
| PERI_TR_1TO1_GR2_TR_CTL21 | 0x4000C854 | FULL | Trigger control register |

## 22.26 TR_1TO1_GR 3

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_TR_1TO1_GR3_TR_CTL0 | 0x4000CC00 | FULL | Trigger control register |
| PERI_TR_1TO1_GR3_TR_CTL1 | 0x4000CC04 | FULL | Trigger control register |

## 22.27 TR_1TO1_GR 4

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_TR_1TO1_GR4_TR_CTL0 | 0x4000D000 | FULL | Trigger control register |
| PERI_TR_1TO1_GR4_TR_CTL1 | 0x4000D004 | FULL | Trigger control register |
| PERI_TR_1TO1_GR4_TR_CTL2 | 0x4000D008 | FULL | Trigger control register |
| PERI_TR_1TO1_GR4_TR_CTL3 | 0x4000D00C | FULL | Trigger control register |
| PERI_TR_1TO1_GR4_TR_CTL4 | 0x4000D010 | FULL | Trigger control register |
| PERI_TR_1TO1_GR4_TR_CTL5 | 0x4000D014 | FULL | Trigger control register |
| PERI_TR_1TO1_GR4_TR_CTL6 | 0x4000D018 | FULL | Trigger control register |
| PERI_TR_1TO1_GR4_TR_CTL7 | 0x4000D01C | FULL | Trigger control register |
| PERI_TR_1TO1_GR4_TR_CTL8 | 0x4000D020 | FULL | Trigger control register |
| PERI_TR_1TO1_GR4_TR_CTL9 | 0x4000D024 | FULL | Trigger control register |
| PERI_TR_1TO1_GR4_TR_CTL10 | 0x4000D028 | FULL | Trigger control register |
| PERI_TR_1TO1_GR4_TR_CTL11 | 0x4000D02C | FULL | Trigger control register |
| PERI_TR_1TO1_GR4_TR_CTL12 | 0x4000D030 | FULL | Trigger control register |
| PERI_TR_1TO1_GR4_TR_CTL13 | 0x4000D034 | FULL | Trigger control register |
| PERI_TR_1TO1_GR4_TR_CTL14 | 0x4000D038 | FULL | Trigger control register |

## 22.28 TR_1TO1_GR 5

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_TR_1TO1_GR5_TR_CTL0 | 0x4000D400 | FULL | Trigger control register |
| PERI_TR_1TO1_GR5_TR_CTL1 | 0x4000D404 | FULL | Trigger control register |
| PERI_TR_1TO1_GR5_TR_CTL2 | 0x4000D408 | FULL | Trigger control register |
| PERI_TR_1TO1_GR5_TR_CTL3 | 0x4000D40C | FULL | Trigger control register |
| PERI_TR_1TO1_GR5_TR_CTL4 | 0x4000D410 | FULL | Trigger control register |
| PERI_TR_1TO1_GR5_TR_CTL5 | 0x4000D414 | FULL | Trigger control register |

## 22.29 TR_1TO1_GR 6

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_TR_1TO1_GR6_TR_CTL0 | 0x4000D800 | FULL | Trigger control register |
| PERI_TR_1TO1_GR6_TR_CTL1 | 0x4000D804 | FULL | Trigger control register |
| PERI_TR_1TO1_GR6_TR_CTL2 | 0x4000D808 | FULL | Trigger control register |
| PERI_TR_1TO1_GR6_TR_CTL3 | 0x4000D80C | FULL | Trigger control register |
| PERI_TR_1TO1_GR6_TR_CTL4 | 0x4000D810 | FULL | Trigger control register |
| PERI_TR_1TO1_GR6_TR_CTL5 | 0x4000D814 | FULL | Trigger control register |
| PERI_TR_1TO1_GR6_TR_CTL6 | 0x4000D818 | FULL | Trigger control register |
| PERI_TR_1TO1_GR6_TR_CTL7 | 0x4000D81C | FULL | Trigger control register |
| PERI_TR_1TO1_GR6_TR_CTL8 | 0x4000D820 | FULL | Trigger control register |
| PERI_TR_1TO1_GR6_TR_CTL9 | 0x4000D824 | FULL | Trigger control register |
| PERI_TR_1TO1_GR6_TR_CTL10 | 0x4000D828 | FULL | Trigger control register |
| PERI_TR_1TO1_GR6_TR_CTL11 | 0x4000D82C | FULL | Trigger control register |
| PERI_TR_1TO1_GR6_TR_CTL12 | 0x4000D830 | FULL | Trigger control register |
| PERI_TR_1TO1_GR6_TR_CTL13 | 0x4000D834 | FULL | Trigger control register |
| PERI_TR_1TO1_GR6_TR_CTL14 | 0x4000D838 | FULL | Trigger control register |
| PERI_TR_1TO1_GR6_TR_CTL15 | 0x4000D83C | FULL | Trigger control register |
| PERI_TR_1TO1_GR6_TR_CTL16 | 0x4000D840 | FULL | Trigger control register |
| PERI_TR_1TO1_GR6_TR_CTL17 | 0x4000D844 | FULL | Trigger control register |
| PERI_TR_1TO1_GR6_TR_CTL18 | 0x4000D848 | FULL | Trigger control register |
| PERI_TR_1TO1_GR6_TR_CTL19 | 0x4000D84C | FULL | Trigger control register |
| PERI_TR_1TO1_GR6_TR_CTL20 | 0x4000D850 | FULL | Trigger control register |
| PERI_TR_1TO1_GR6_TR_CTL21 | 0x4000D854 | FULL | Trigger control register |
| PERI_TR_1TO1_GR6_TR_CTL22 | 0x4000D858 | FULL | Trigger control register |
| PERI_TR_1TO1_GR6_TR_CTL23 | 0x4000D85C | FULL | Trigger control register |
| PERI_TR_1TO1_GR6_TR_CTL24 | 0x4000D860 | FULL | Trigger control register |
| PERI_TR_1TO1_GR6_TR_CTL25 | 0x4000D864 | FULL | Trigger control register |
| PERI_TR_1TO1_GR6_TR_CTL26 | 0x4000D868 | FULL | Trigger control register |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_TR_1TO1_GR6_TR_CTL27 | 0x4000D86C | FULL | Trigger control register |
| PERI_TR_1TO1_GR6_TR_CTL28 | 0x4000D870 | FULL | Trigger control register |
| PERI_TR_1TO1_GR6_TR_CTL29 | 0x4000D874 | FULL | Trigger control register |
| PERI_TR_1TO1_GR6_TR_CTL30 | 0x4000D878 | FULL | Trigger control register |
| PERI_TR_1TO1_GR6_TR_CTL31 | 0x4000D87C | FULL | Trigger control register |
| PERI_TR_1TO1_GR6_TR_CTL32 | 0x4000D880 | FULL | Trigger control register |
| PERI_TR_1TO1_GR6_TR_CTL33 | 0x4000D884 | FULL | Trigger control register |
| PERI_TR_1TO1_GR6_TR_CTL34 | 0x4000D888 | FULL | Trigger control register |
| PERI_TR_1TO1_GR6_TR_CTL35 | 0x4000D88C | FULL | Trigger control register |
| PERI_TR_1TO1_GR6_TR_CTL36 | 0x4000D890 | FULL | Trigger control register |
| PERI_TR_1TO1_GR6_TR_CTL37 | 0x4000D894 | FULL | Trigger control register |
| PERI_TR_1TO1_GR6_TR_CTL38 | 0x4000D898 | FULL | Trigger control register |
| PERI_TR_1TO1_GR6_TR_CTL39 | 0x4000D89C | FULL | Trigger control register |
| PERI_TR_1TO1_GR6_TR_CTL40 | 0x4000D8A0 | FULL | Trigger control register |
| PERI_TR_1TO1_GR6_TR_CTL41 | 0x4000D8A4 | FULL | Trigger control register |
| PERI_TR_1TO1_GR6_TR_CTL42 | 0x4000D8A8 | FULL | Trigger control register |
| PERI_TR_1TO1_GR6_TR_CTL43 | 0x4000D8AC | FULL | Trigger control register |
| PERI_TR_1TO1_GR6_TR_CTL44 | 0x4000D8B0 | FULL | Trigger control register |
| PERI_TR_1TO1_GR6_TR_CTL45 | 0x4000D8B4 | FULL | Trigger control register |
| PERI_TR_1TO1_GR6_TR_CTL46 | 0x4000D8B8 | FULL | Trigger control register |
| PERI_TR_1TO1_GR6_TR_CTL47 | 0x4000D8BC | FULL | Trigger control register |
| PERI_TR_1TO1_GR6_TR_CTL48 | 0x4000D8C0 | FULL | Trigger control register |
| PERI_TR_1TO1_GR6_TR_CTL49 | 0x4000D8C4 | FULL | Trigger control register |
| PERI_TR_1TO1_GR6_TR_CTL50 | 0x4000D8C8 | FULL | Trigger control register |
| PERI_TR_1TO1_GR6_TR_CTL51 | 0x4000D8CC | FULL | Trigger control register |
| PERI_TR_1TO1_GR6_TR_CTL52 | 0x4000D8D0 | FULL | Trigger control register |
| PERI_TR_1TO1_GR6_TR_CTL53 | 0x4000D8D4 | FULL | Trigger control register |
| PERI_TR_1TO1_GR6_TR_CTL54 | 0x4000D8D8 | FULL | Trigger control register |
| PERI_TR_1TO1_GR6_TR_CTL55 | 0x4000D8DC | FULL | Trigger control register |
| PERI_TR_1TO1_GR6_TR_CTL56 | 0x4000D8E0 | FULL | Trigger control register |
| PERI_TR_1TO1_GR6_TR_CTL57 | 0x4000D8E4 | FULL | Trigger control register |
| PERI_TR_1TO1_GR6_TR_CTL58 | 0x4000D8E8 | FULL | Trigger control register |
| PERI_TR_1TO1_GR6_TR_CTL59 | 0x4000D8EC | FULL | Trigger control register |
| PERI_TR_1TO1_GR6_TR_CTL60 | 0x4000D8F0 | FULL | Trigger control register |
| PERI_TR_1TO1_GR6_TR_CTL61 | 0x4000D8F4 | FULL | Trigger control register |
| PERI_TR_1TO1_GR6_TR_CTL62 | 0x4000D8F8 | FULL | Trigger control register |
| PERI_TR_1TO1_GR6_TR_CTL63 | 0x4000D8FC | FULL | Trigger control register |
| PERI_TR_1TO1_GR6_TR_CTL64 | 0x4000D900 | FULL | Trigger control register |
| PERI_TR_1TO1_GR6_TR_CTL65 | 0x4000D904 | FULL | Trigger control register |
| PERI_TR_1TO1_GR6_TR_CTL66 | 0x4000D908 | FULL | Trigger control register |
| PERI_TR_1TO1_GR6_TR_CTL67 | 0x4000D90C | FULL | Trigger control register |
| PERI_TR_1TO1_GR6_TR_CTL68 | 0x4000D910 | FULL | Trigger control register |
| PERI_TR_1TO1_GR6_TR_CTL69 | 0x4000D914 | FULL | Trigger control register |
| PERI_TR_1TO1_GR6_TR_CTL70 | 0x4000D918 | FULL | Trigger control register |
| PERI_TR_1TO1_GR6_TR_CTL71 | 0x4000D91C | FULL | Trigger control register |
| PERI_TR_1TO1_GR6_TR_CTL72 | 0x4000D920 | FULL | Trigger control register |
| PERI_TR_1TO1_GR6_TR_CTL73 | 0x4000D924 | FULL | Trigger control register |
| PERI_TR_1TO1_GR6_TR_CTL74 | 0x4000D928 | FULL | Trigger control register |
| PERI_TR_1TO1_GR6_TR_CTL75 | 0x4000D92C | FULL | Trigger control register |
| PERI_TR_1TO1_GR6_TR_CTL76 | 0x4000D930 | FULL | Trigger control register |
| PERI_TR_1TO1_GR6_TR_CTL77 | 0x4000D934 | FULL | Trigger control register |
| PERI_TR_1TO1_GR6_TR_CTL78 | 0x4000D938 | FULL | Trigger control register |
| PERI_TR_1TO1_GR6_TR_CTL79 | 0x4000D93C | FULL | Trigger control register |
| PERI_TR_1TO1_GR6_TR_CTL80 | 0x4000D940 | FULL | Trigger control register |
| PERI_TR_1TO1_GR6_TR_CTL81 | 0x4000D944 | FULL | Trigger control register |
| PERI_TR_1TO1_GR6_TR_CTL82 | 0x4000D948 | FULL | Trigger control register |
| PERI_TR_1TO1_GR6_TR_CTL83 | 0x4000D94C | FULL | Trigger control register |
| PERI_TR_1TO1_GR6_TR_CTL84 | 0x4000D950 | FULL | Trigger control register |
| PERI_TR_1TO1_GR6_TR_CTL85 | 0x4000D954 | FULL | Trigger control register |
| PERI_TR_1TO1_GR6_TR_CTL86 | 0x4000D958 | FULL | Trigger control register |
| PERI_TR_1TO1_GR6_TR_CTL87 | 0x4000D95C | FULL | Trigger control register |
| PERI_TR_1TO1_GR6_TR_CTL88 | 0x4000D960 | FULL | Trigger control register |
| PERI_TR_1TO1_GR6_TR_CTL89 | 0x4000D964 | FULL | Trigger control register |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_TR_1TO1_GR6_TR_CTL90 | 0x4000D968 | FULL | Trigger control register |
| PERI_TR_1TO1_GR6_TR_CTL91 | 0x4000D96C | FULL | Trigger control register |
| PERI_TR_1TO1_GR6_TR_CTL92 | 0x4000D970 | FULL | Trigger control register |
| PERI_TR_1TO1_GR6_TR_CTL93 | 0x4000D974 | FULL | Trigger control register |
| PERI_TR_1TO1_GR6_TR_CTL94 | 0x4000D978 | FULL | Trigger control register |
| PERI_TR_1TO1_GR6_TR_CTL95 | 0x4000D97C | FULL | Trigger control register |

## 22.30 TR_1TO1_GR 7

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_TR_1TO1_GR7_TR_CTL0 | 0x4000DC00 | FULL | Trigger control register |
| PERI_TR_1TO1_GR7_TR_CTL1 | 0x4000DC04 | FULL | Trigger control register |
| PERI_TR_1TO1_GR7_TR_CTL2 | 0x4000DC08 | FULL | Trigger control register |
| PERI_TR_1TO1_GR7_TR_CTL3 | 0x4000DC0C | FULL | Trigger control register |
| PERI_TR_1TO1_GR7_TR_CTL4 | 0x4000DC10 | FULL | Trigger control register |
| PERI_TR_1TO1_GR7_TR_CTL5 | 0x4000DC14 | FULL | Trigger control register |
| PERI_TR_1TO1_GR7_TR_CTL6 | 0x4000DC18 | FULL | Trigger control register |
| PERI_TR_1TO1_GR7_TR_CTL7 | 0x4000DC1C | FULL | Trigger control register |
| PERI_TR_1TO1_GR7_TR_CTL8 | 0x4000DC20 | FULL | Trigger control register |
| PERI_TR_1TO1_GR7_TR_CTL9 | 0x4000DC24 | FULL | Trigger control register |
| PERI_TR_1TO1_GR7_TR_CTL10 | 0x4000DC28 | FULL | Trigger control register |
| PERI_TR_1TO1_GR7_TR_CTL11 | 0x4000DC2C | FULL | Trigger control register |
| PERI_TR_1TO1_GR7_TR_CTL12 | 0x4000DC30 | FULL | Trigger control register |
| PERI_TR_1TO1_GR7_TR_CTL13 | 0x4000DC34 | FULL | Trigger control register |
| PERI_TR_1TO1_GR7_TR_CTL14 | 0x4000DC38 | FULL | Trigger control register |
| PERI_TR_1TO1_GR7_TR_CTL15 | 0x4000DC3C | FULL | Trigger control register |
| PERI_TR_1TO1_GR7_TR_CTL16 | 0x4000DC40 | FULL | Trigger control register |
| PERI_TR_1TO1_GR7_TR_CTL17 | 0x4000DC44 | FULL | Trigger control register |
| PERI_TR_1TO1_GR7_TR_CTL18 | 0x4000DC48 | FULL | Trigger control register |
| PERI_TR_1TO1_GR7_TR_CTL19 | 0x4000DC4C | FULL | Trigger control register |
| PERI_TR_1TO1_GR7_TR_CTL20 | 0x4000DC50 | FULL | Trigger control register |
| PERI_TR_1TO1_GR7_TR_CTL21 | 0x4000DC54 | FULL | Trigger control register |
| PERI_TR_1TO1_GR7_TR_CTL22 | 0x4000DC58 | FULL | Trigger control register |
| PERI_TR_1TO1_GR7_TR_CTL23 | 0x4000DC5C | FULL | Trigger control register |
| PERI_TR_1TO1_GR7_TR_CTL24 | 0x4000DC60 | FULL | Trigger control register |
| PERI_TR_1TO1_GR7_TR_CTL25 | 0x4000DC64 | FULL | Trigger control register |
| PERI_TR_1TO1_GR7_TR_CTL26 | 0x4000DC68 | FULL | Trigger control register |
| PERI_TR_1TO1_GR7_TR_CTL27 | 0x4000DC6C | FULL | Trigger control register |
| PERI_TR_1TO1_GR7_TR_CTL28 | 0x4000DC70 | FULL | Trigger control register |
| PERI_TR_1TO1_GR7_TR_CTL29 | 0x4000DC74 | FULL | Trigger control register |
| PERI_TR_1TO1_GR7_TR_CTL30 | 0x4000DC78 | FULL | Trigger control register |
| PERI_TR_1TO1_GR7_TR_CTL31 | 0x4000DC7C | FULL | Trigger control register |
| PERI_TR_1TO1_GR7_TR_CTL32 | 0x4000DC80 | FULL | Trigger control register |
| PERI_TR_1TO1_GR7_TR_CTL33 | 0x4000DC84 | FULL | Trigger control register |
| PERI_TR_1TO1_GR7_TR_CTL34 | 0x4000DC88 | FULL | Trigger control register |
| PERI_TR_1TO1_GR7_TR_CTL35 | 0x4000DC8C | FULL | Trigger control register |
| PERI_TR_1TO1_GR7_TR_CTL36 | 0x4000DC90 | FULL | Trigger control register |
| PERI_TR_1TO1_GR7_TR_CTL37 | 0x4000DC94 | FULL | Trigger control register |
| PERI_TR_1TO1_GR7_TR_CTL38 | 0x4000DC98 | FULL | Trigger control register |
| PERI_TR_1TO1_GR7_TR_CTL39 | 0x4000DC9C | FULL | Trigger control register |
| PERI_TR_1TO1_GR7_TR_CTL40 | 0x4000DCA0 | FULL | Trigger control register |
| PERI_TR_1TO1_GR7_TR_CTL41 | 0x4000DCA4 | FULL | Trigger control register |
| PERI_TR_1TO1_GR7_TR_CTL42 | 0x4000DCA8 | FULL | Trigger control register |
| PERI_TR_1TO1_GR7_TR_CTL43 | 0x4000DCAC | FULL | Trigger control register |
| PERI_TR_1TO1_GR7_TR_CTL44 | 0x4000DCB0 | FULL | Trigger control register |
| PERI_TR_1TO1_GR7_TR_CTL45 | 0x4000DCB4 | FULL | Trigger control register |
| PERI_TR_1TO1_GR7_TR_CTL46 | 0x4000DCB8 | FULL | Trigger control register |
| PERI_TR_1TO1_GR7_TR_CTL47 | 0x4000DCBC | FULL | Trigger control register |
| PERI_TR_1TO1_GR7_TR_CTL48 | 0x4000DCC0 | FULL | Trigger control register |
| PERI_TR_1TO1_GR7_TR_CTL49 | 0x4000DCC4 | FULL | Trigger control register |
| PERI_TR_1TO1_GR7_TR_CTL50 | 0x4000DCC8 | FULL | Trigger control register |
| PERI_TR_1TO1_GR7_TR_CTL51 | 0x4000DCCC | FULL | Trigger control register |
| PERI_TR_1TO1_GR7_TR_CTL52 | 0x4000DCD0 | FULL | Trigger control register |
| PERI_TR_1TO1_GR7_TR_CTL53 | 0x4000DCD4 | FULL | Trigger control register |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_TR_1TO1_GR7_TR_CTL54 | 0x4000DCD8 | FULL | Trigger control register |
| PERI_TR_1TO1_GR7_TR_CTL55 | 0x4000DCDC | FULL | Trigger control register |
| PERI_TR_1TO1_GR7_TR_CTL56 | 0x4000DCE0 | FULL | Trigger control register |
| PERI_TR_1TO1_GR7_TR_CTL57 | 0x4000DCE4 | FULL | Trigger control register |
| PERI_TR_1TO1_GR7_TR_CTL58 | 0x4000DCE8 | FULL | Trigger control register |
| PERI_TR_1TO1_GR7_TR_CTL59 | 0x4000DCEC | FULL | Trigger control register |
| PERI_TR_1TO1_GR7_TR_CTL60 | 0x4000DCF0 | FULL | Trigger control register |
| PERI_TR_1TO1_GR7_TR_CTL61 | 0x4000DCF4 | FULL | Trigger control register |
| PERI_TR_1TO1_GR7_TR_CTL62 | 0x4000DCF8 | FULL | Trigger control register |
| PERI_TR_1TO1_GR7_TR_CTL63 | 0x4000DCFC | FULL | Trigger control register |
| PERI_TR_1TO1_GR7_TR_CTL64 | 0x4000DD00 | FULL | Trigger control register |
| PERI_TR_1TO1_GR7_TR_CTL65 | 0x4000DD04 | FULL | Trigger control register |
| PERI_TR_1TO1_GR7_TR_CTL66 | 0x4000DD08 | FULL | Trigger control register |
| PERI_TR_1TO1_GR7_TR_CTL67 | 0x4000DD0C | FULL | Trigger control register |
| PERI_TR_1TO1_GR7_TR_CTL68 | 0x4000DD10 | FULL | Trigger control register |
| PERI_TR_1TO1_GR7_TR_CTL69 | 0x4000DD14 | FULL | Trigger control register |
| PERI_TR_1TO1_GR7_TR_CTL70 | 0x4000DD18 | FULL | Trigger control register |
| PERI_TR_1TO1_GR7_TR_CTL71 | 0x4000DD1C | FULL | Trigger control register |
| PERI_TR_1TO1_GR7_TR_CTL72 | 0x4000DD20 | FULL | Trigger control register |
| PERI_TR_1TO1_GR7_TR_CTL73 | 0x4000DD24 | FULL | Trigger control register |
| PERI_TR_1TO1_GR7_TR_CTL74 | 0x4000DD28 | FULL | Trigger control register |
| PERI_TR_1TO1_GR7_TR_CTL75 | 0x4000DD2C | FULL | Trigger control register |
| PERI_TR_1TO1_GR7_TR_CTL76 | 0x4000DD30 | FULL | Trigger control register |
| PERI_TR_1TO1_GR7_TR_CTL77 | 0x4000DD34 | FULL | Trigger control register |
| PERI_TR_1TO1_GR7_TR_CTL78 | 0x4000DD38 | FULL | Trigger control register |
| PERI_TR_1TO1_GR7_TR_CTL79 | 0x4000DD3C | FULL | Trigger control register |
| PERI_TR_1TO1_GR7_TR_CTL80 | 0x4000DD40 | FULL | Trigger control register |
| PERI_TR_1TO1_GR7_TR_CTL81 | 0x4000DD44 | FULL | Trigger control register |
| PERI_TR_1TO1_GR7_TR_CTL82 | 0x4000DD48 | FULL | Trigger control register |
| PERI_TR_1TO1_GR7_TR_CTL83 | 0x4000DD4C | FULL | Trigger control register |
| PERI_TR_1TO1_GR7_TR_CTL84 | 0x4000DD50 | FULL | Trigger control register |
| PERI_TR_1TO1_GR7_TR_CTL85 | 0x4000DD54 | FULL | Trigger control register |
| PERI_TR_1TO1_GR7_TR_CTL86 | 0x4000DD58 | FULL | Trigger control register |
| PERI_TR_1TO1_GR7_TR_CTL87 | 0x4000DD5C | FULL | Trigger control register |
| PERI_TR_1TO1_GR7_TR_CTL88 | 0x4000DD60 | FULL | Trigger control register |
| PERI_TR_1TO1_GR7_TR_CTL89 | 0x4000DD64 | FULL | Trigger control register |
| PERI_TR_1TO1_GR7_TR_CTL90 | 0x4000DD68 | FULL | Trigger control register |
| PERI_TR_1TO1_GR7_TR_CTL91 | 0x4000DD6C | FULL | Trigger control register |
| PERI_TR_1TO1_GR7_TR_CTL92 | 0x4000DD70 | FULL | Trigger control register |
| PERI_TR_1TO1_GR7_TR_CTL93 | 0x4000DD74 | FULL | Trigger control register |
| PERI_TR_1TO1_GR7_TR_CTL94 | 0x4000DD78 | FULL | Trigger control register |
| PERI_TR_1TO1_GR7_TR_CTL95 | 0x4000DD7C | FULL | Trigger control register |

## 22.31 TR_1TO1_GR 8

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_TR_1TO1_GR8_TR_CTL0 | 0x4000E000 | FULL | Trigger control register |
| PERI_TR_1TO1_GR8_TR_CTL1 | 0x4000E004 | FULL | Trigger control register |
| PERI_TR_1TO1_GR8_TR_CTL2 | 0x4000E008 | FULL | Trigger control register |
| PERI_TR_1TO1_GR8_TR_CTL3 | 0x4000E00C | FULL | Trigger control register |
| PERI_TR_1TO1_GR8_TR_CTL4 | 0x4000E010 | FULL | Trigger control register |

## 22.32 TR_1TO1_GR 9

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_TR_1TO1_GR9_TR_CTL0 | 0x4000E400 | FULL | Trigger control register |
| PERI_TR_1TO1_GR9_TR_CTL1 | 0x4000E404 | FULL | Trigger control register |
| PERI_TR_1TO1_GR9_TR_CTL2 | 0x4000E408 | FULL | Trigger control register |
| PERI_TR_1TO1_GR9_TR_CTL3 | 0x4000E40C | FULL | Trigger control register |
| PERI_TR_1TO1_GR9_TR_CTL4 | 0x4000E410 | FULL | Trigger control register |

## 22.33 TR_1TO1_GR 10

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_TR_1TO1_GR10_TR_CTL0 | 0x4000E800 | FULL | Trigger control register |
| PERI_TR_1TO1_GR10_TR_CTL1 | 0x4000E804 | FULL | Trigger control register |
| PERI_TR_1TO1_GR10_TR_CTL2 | 0x4000E808 | FULL | Trigger control register |
| PERI_TR_1TO1_GR10_TR_CTL3 | 0x4000E80C | FULL | Trigger control register |
| PERI_TR_1TO1_GR10_TR_CTL4 | 0x4000E810 | FULL | Trigger control register |
| PERI_TR_1TO1_GR10_TR_CTL5 | 0x4000E814 | FULL | Trigger control register |
| PERI_TR_1TO1_GR10_TR_CTL6 | 0x4000E818 | FULL | Trigger control register |
| PERI_TR_1TO1_GR10_TR_CTL7 | 0x4000E81C | FULL | Trigger control register |
| PERI_TR_1TO1_GR10_TR_CTL8 | 0x4000E820 | FULL | Trigger control register |
| PERI_TR_1TO1_GR10_TR_CTL9 | 0x4000E824 | FULL | Trigger control register |
| PERI_TR_1TO1_GR10_TR_CTL10 | 0x4000E828 | FULL | Trigger control register |
| PERI_TR_1TO1_GR10_TR_CTL11 | 0x4000E82C | FULL | Trigger control register |
| PERI_TR_1TO1_GR10_TR_CTL12 | 0x4000E830 | FULL | Trigger control register |
| PERI_TR_1TO1_GR10_TR_CTL13 | 0x4000E834 | FULL | Trigger control register |
| PERI_TR_1TO1_GR10_TR_CTL14 | 0x4000E838 | FULL | Trigger control register |
| PERI_TR_1TO1_GR10_TR_CTL15 | 0x4000E83C | FULL | Trigger control register |
| PERI_TR_1TO1_GR10_TR_CTL16 | 0x4000E840 | FULL | Trigger control register |
| PERI_TR_1TO1_GR10_TR_CTL17 | 0x4000E844 | FULL | Trigger control register |
| PERI_TR_1TO1_GR10_TR_CTL18 | 0x4000E848 | FULL | Trigger control register |
| PERI_TR_1TO1_GR10_TR_CTL19 | 0x4000E84C | FULL | Trigger control register |

## 22.34 TR_1TO1_GR 11

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_TR_1TO1_GR11_TR_CTL0 | 0x4000EC00 | FULL | Trigger control register |
| PERI_TR_1TO1_GR11_TR_CTL1 | 0x4000EC04 | FULL | Trigger control register |

## 22.35 TR_1TO1_GR 12

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_TR_1TO1_GR12_TR_CTL0 | 0x4000F000 | FULL | Trigger control register |
| PERI_TR_1TO1_GR12_TR_CTL1 | 0x4000F004 | FULL | Trigger control register |

## 22.36 TR_1TO1_GR 13

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_TR_1TO1_GR13_TR_CTL0 | 0x4000F400 | FULL | Trigger control register |
| PERI_TR_1TO1_GR13_TR_CTL1 | 0x4000F404 | FULL | Trigger control register |

## 22.37 Register Details

### 22.37.1 PERI_TIMEOUT_CTL

**Description:** Timeout control
**Address:** 0x40000200
**Offset:** 0x200
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** The presence of the TIMEOUT_CTL register is dependent on the TIMEOUT_PRESENT parameter.

The presence of TIMEOUT_CTL requires slave 0 of the peripheral group to be present (SL0_PRESENT must be '1').
**Default:** 0xFFFF

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | TIMEOUT [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | TIMEOUT [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | TIMEOUT | RW | R | 65535 | This field specifies a number of clock cycles (clk_slow). If an AHB-Lite bus transfer takes more than the specified number of cycles (timeout detection), the bus transfer is terminated with an AHB-Lite bus error and a fault is generated (and possibly recorded in the fault report structure(s)).<br>'0x0000'-'0xfffe': Number of clock cycles.<br>'0xffff': This value is the default/reset value and specifies that no timeout detection is performed: a bus transfer will never be terminated and a fault will never be generated. |

### 22.37.2 PERI_TR_CMD

**Description:** Trigger command
**Address:** 0x40000220
**Offset:** 0x220
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** This register provides SW control over trigger activation. This is useful for SW initiated triggers (e.g. DW/DMA transfers) or for debugging purposes. The control enables SW activation of one specific input trigger or output trigger of the trigger multiplexer structure.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | TR_SEL [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:13] | | | GROUP_SEL [12:8] | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | ACTIVATE [31:31] | OUT_SEL [30:30] | TR_EDGE [29:29] | None [28:24] | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | TR_SEL | RW | R | 0 | Specifies the activated trigger when ACTIVATE is '1'. If the specified trigger is not present, the trigger activation has no effect. |
| 8:12 | GROUP_SEL | RW | R | 0 | Specifies the trigger group:<br>'0'-'15': trigger multiplexer groups.<br>'16'-'31': trigger 1-to-1 groups. |
| 29 | TR_EDGE | RW | R | 0 | Specifies if the activated trigger is treated as a level sensitive or edge sensitive trigger.<br>'0': level sensitive. The trigger reflects TR_CMD.ACTIVATE.<br>'1': edge sensitive trigger. The trigger is activated for two clk_peri cycles. |
| 30 | OUT_SEL | RW | R | 0 | Specifies whether trigger activation is for a specific input or output trigger of the trigger multiplexer. Activation of a specific input trigger, will result in activation of all output triggers that have the specific input trigger selected through their TR_OUT_CTL.TR_SEL field. Activation of a specific output trigger, will result in activation of the specified TR_SEL output trigger only.<br>'0': TR_SEL selection and trigger activation is for an input trigger to the trigger multiplexer.<br>'1': TR_SEL selection and trigger activation is for an output trigger from the trigger multiplexer.<br><br>Note: this field is not used for trigger 1-to-1 groups. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 31 | ACTIVATE | RW | RW1C | 0 | SW sets this field to '1' to activate (set to '1') a trigger as identified by TR_SEL, TR_EDGE and OUT_SEL. HW sets this field to '0' for edge sensitive triggers AFTER the selected trigger is activated for two clk_peri cycles.<br><br>Note: when ACTIVATE is '1', SW should not modify the other register fields.<br>SW MUST NOT set ACTIVATE bit to '1' while updating the other register bits simultaneously. At first the SW MUST update the other register bits as needed, and then set ACTIVATE to '1' with a new register write. |

### 22.37.3 PERI_ECC_CTL

**Description:** ECC control
**Address:** 0x40002000
**Offset:** 0x2000
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register provides ECC support for the protection structures SRAM in the master interfaces peripheral (peripheral group 0, peripheral 1).
**Default:** 0x10000

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | WORD_ADDR [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:11] | | | | | WORD_ADDR [10:8] | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:19] | | | | | ECC_INJ_EN [18:18] | None [17:17] | ECC_EN [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | PARITY [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:10 | WORD_ADDR | RW | R | 0 | Specifies the word address where the parity is injected.<br>- On a 32-bit write access to this SRAM address and when ECC_INJ_EN bit is '1', the parity (PARITY) is injected. |
| 16 | ECC_EN | RW | R | 1 | Enable ECC:<br>'0': Disabled (on write ECC parity bits will not be correctly written).<br>'1': Enabled. |
| 18 | ECC_INJ_EN | RW | R | 0 | Enable error injection for PERI protection structure SRAM.<br>When '1', the parity (PARITY) is used when a write is done to the WORD_ADDR word address of the SRAM. |
| 24:31 | PARITY | RW | R | 0 | ECC parity to use for ECC error injection at address WORD_ADDR. |

## 22.37.4 GR

### 22.37.4.1 PERI_GR_CLOCK_CTL

**Description:** Clock control
**Address:** 0x40004000
**Offset:** 0x0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** The peripheral interconnect supports up to sixteen groups: group 0, group 1, ..., group 15. Peripheral groups 0, 1 and 2 use clk_slow (clk_group[0] = clk_group[1] = clk_group[2] = clk_slow) and do NOT have a CLOCK_GROUP_DIV_CTL register. Peripheral groups 3, 4, ..., 15 have a dedicated CLOCK_GROUP_DIV_CTL register.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | INT8_DIV [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 8:15 | INT8_DIV | RW | R | 0 | Specifies a group clock divider (from the peripheral clock 'clk_peri' to the group clock 'clk_group[3/4/5/...15]'). Integer division by (1+INT8_DIV). Allows for integer divisions in the range [1, 256].<br><br>Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to '0' when transitioning from DeepSleep to Active power mode. |

### 22.37.4.2 PERI_GR_SL_CTL

**Description:** Slave control
**Address:** 0x40004010
**Offset:** 0x10
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xFFFF

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | ENABLED_7 [7:7] | ENABLED_6 [6:6] | ENABLED_5 [5:5] | ENABLED_4 [4:4] | ENABLED_3 [3:3] | ENABLED_2 [2:2] | ENABLED_1 [1:1] | ENABLED_0 [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:12] | | | | ENABLED_11 [11:11] | ENABLED_10 [10:10] | ENABLED_9 [9:9] | ENABLED_8 [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | ENABLED_0 | RW | R | 1 | Peripheral group, slave 0 enable. If the slave is disabled, its clock is gated off (constant '0') and its resets are activated.<br><br>Note: For peripheral group 0 (the peripheral interconnect MMIO registers), this field is a constant '1' (SW: R): the slave can NOT be disabled. |
| 1 | ENABLED_1 | RW | R | 1 | Peripheral group, slave 1 enable. If the slave is disabled, its clock is gated off (constant '0') and its resets are activated.<br><br>Note: For peripheral group 0 (the peripheral interconnect, master interface MMIO registers), this field is a constant '1' (SW: R): the slave can NOT be disabled. |
| 2 | ENABLED_2 | RW | R | 1 | Peripheral group, slave 2 enable. If the slave is disabled, its clock is gated off (constant '0') and its resets are activated.<br><br>Note: For peripheral group 0 (the peripheral interconnect, PCLK group MMIO registers), this field is a constant '1' (SW: R): the slave can NOT be disabled. |
| 3 | ENABLED_3 | RW | R | 1 | N/A |
| 4 | ENABLED_4 | RW | R | 1 | N/A |
| 5 | ENABLED_5 | RW | R | 1 | N/A |
| 6 | ENABLED_6 | RW | R | 1 | N/A |
| 7 | ENABLED_7 | RW | R | 1 | N/A |
| 8 | ENABLED_8 | RW | R | 1 | N/A |
| 9 | ENABLED_9 | RW | R | 1 | N/A |
| 10 | ENABLED_10 | RW | R | 1 | N/A |
| 11 | ENABLED_11 | RW | R | 1 | N/A |

## 22.37.5 TR_GR

### 22.37.5.1 PERI_TR_GR_TR_CTL

**Description:** Trigger control register
**Address:** 0x40008000
**Offset:** 0x0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register specifies the input trigger for a specific output trigger in trigger group 0. Note that for SW initiated triggers, SW is responsible for activating the output trigger, rather than relying on a specific HW input trigger. For this reason, input trigger 0 is typically connected to a constant signal level of '0' at chip integration (design decision) and SW initiated output triggers are all connected to input trigger 0 (SW responsibility: TR_OUT_CTL.TR_SEL should be set to '0' to select the constant signal level '0' from chip level). As a result, SW initiated triggers can never be activated by a HW input trigger to the trigger multiplexer.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | TR_SEL [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:13] | | | DBG _FREEZE _EN [12:12] | None [11:10] | | TR_EDGE [9:9] | TR_INV [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | TR_SEL | RW | R | 0 | Specifies input trigger. This field is typically set during the setup of a chip use case scenario. Changing this field while activated triggers are present on the input triggers may result in unpredictable behavior. Note that input trigger 0 (default value) is typically connected to a constant signal level of '0', and as a result will not cause HW activation of the output trigger. |
| 8 | TR_INV | RW | R | 0 | Specifies if the output trigger is inverted. |
| 9 | TR_EDGE | RW | R | 0 | Specifies if the (inverted) output trigger is treated as a level sensitive or edge sensitive trigger.<br>'0': level sensitive.<br>'1': edge sensitive trigger. The (inverted) output trigger duration needs to be at least 2 cycles on the consumer clock. the(inverted) output trigger is synchronized to the consumer clock and a two cycle pulse is generated on the consumer clock. |
| 12 | DBG_FREEZE_EN | RW | R | 0 | Specifies if the output trigger is blocked in debug mode. When set high tr_dbg_freeze will block the output trigger generation. |

### 22.37.6 TR_1TO1_GR

#### 22.37.6.1 PERI_TR_1TO1_GR_TR_CTL

**Description:** Trigger control register
**Address:** 0x4000C000
**Offset:** 0x0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:1] | | | | | | | TR_SEL [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:13] | | | DBG _FREEZE _EN [12:12] | None [11:10] | | TR_EDGE [9:9] | TR_INV [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | TR_SEL | RW | R | 0 | Specifies input trigger:<br>'0": constant signal level '0'.<br>'1': input trigger. |
| 8 | TR_INV | RW | R | 0 | Specifies if the output trigger is inverted. |
| 9 | TR_EDGE | RW | R | 0 | Specifies if the (inverted) output trigger is treated as a level sensitive or edge sensitive trigger.<br>'0': level sensitive.<br>'1': edge sensitive trigger. The (inverted) output trigger duration needs to be at least 2 cycles on the consumer clock. the(inverted) output trigger is synchronized to the consumer clock and a two cycle pulse is generated on the consumer clock. |
| 12 | DBG_FREEZE_EN | RW | R | 0 | Specifies if the output trigger is blocked in debug mode. When set high tr_dbg_freeze will block the output trigger generation. |

# 23 PERI_MS

**Description** Peripheral interconnect, master interface
**Base Address** 0x40020000
**Size** 0x20000
**Slave Num** MMIO0 - 1

## 23.1 PPU_PR 0

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_PR0_SL_ADDR | 0x40020000 | FULL | Slave region, base address |
| PERI_MS_PPU_PR0_SL_SIZE | 0x40020004 | FULL | Slave region, size |
| PERI_MS_PPU_PR0_SL_ATT0 | 0x40020010 | FULL | Slave attributes 0 |
| PERI_MS_PPU_PR0_SL_ATT1 | 0x40020014 | FULL | Slave attributes 1 |
| PERI_MS_PPU_PR0_SL_ATT2 | 0x40020018 | FULL | Slave attributes 2 |
| PERI_MS_PPU_PR0_SL_ATT3 | 0x4002001C | FULL | Slave attributes 3 |
| PERI_MS_PPU_PR0_MS_ADDR | 0x40020020 | FULL | Master region, base address |
| PERI_MS_PPU_PR0_MS_SIZE | 0x40020024 | FULL | Master region, size |
| PERI_MS_PPU_PR0_MS_ATT0 | 0x40020030 | FULL | Master attributes 0 |
| PERI_MS_PPU_PR0_MS_ATT1 | 0x40020034 | FULL | Master attributes 1 |
| PERI_MS_PPU_PR0_MS_ATT2 | 0x40020038 | FULL | Master attributes 2 |
| PERI_MS_PPU_PR0_MS_ATT3 | 0x4002003C | FULL | Master attributes 3 |

## 23.2 PPU_PR 1

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_PR1_SL_ADDR | 0x40020040 | FULL | Slave region, base address |
| PERI_MS_PPU_PR1_SL_SIZE | 0x40020044 | FULL | Slave region, size |
| PERI_MS_PPU_PR1_SL_ATT0 | 0x40020050 | FULL | Slave attributes 0 |
| PERI_MS_PPU_PR1_SL_ATT1 | 0x40020054 | FULL | Slave attributes 1 |
| PERI_MS_PPU_PR1_SL_ATT2 | 0x40020058 | FULL | Slave attributes 2 |
| PERI_MS_PPU_PR1_SL_ATT3 | 0x4002005C | FULL | Slave attributes 3 |
| PERI_MS_PPU_PR1_MS_ADDR | 0x40020060 | FULL | Master region, base address |
| PERI_MS_PPU_PR1_MS_SIZE | 0x40020064 | FULL | Master region, size |
| PERI_MS_PPU_PR1_MS_ATT0 | 0x40020070 | FULL | Master attributes 0 |
| PERI_MS_PPU_PR1_MS_ATT1 | 0x40020074 | FULL | Master attributes 1 |
| PERI_MS_PPU_PR1_MS_ATT2 | 0x40020078 | FULL | Master attributes 2 |
| PERI_MS_PPU_PR1_MS_ATT3 | 0x4002007C | FULL | Master attributes 3 |

## 23.3 PPU_PR 2

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_PR2_SL_ADDR | 0x40020080 | FULL | Slave region, base address |
| PERI_MS_PPU_PR2_SL_SIZE | 0x40020084 | FULL | Slave region, size |
| PERI_MS_PPU_PR2_SL_ATT0 | 0x40020090 | FULL | Slave attributes 0 |
| PERI_MS_PPU_PR2_SL_ATT1 | 0x40020094 | FULL | Slave attributes 1 |
| PERI_MS_PPU_PR2_SL_ATT2 | 0x40020098 | FULL | Slave attributes 2 |
| PERI_MS_PPU_PR2_SL_ATT3 | 0x4002009C | FULL | Slave attributes 3 |
| PERI_MS_PPU_PR2_MS_ADDR | 0x400200A0 | FULL | Master region, base address |
| PERI_MS_PPU_PR2_MS_SIZE | 0x400200A4 | FULL | Master region, size |
| PERI_MS_PPU_PR2_MS_ATT0 | 0x400200B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_PR2_MS_ATT1 | 0x400200B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_PR2_MS_ATT2 | 0x400200B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_PR2_MS_ATT3 | 0x400200BC | FULL | Master attributes 3 |

## 23.4 PPU_PR 3

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_PR3_SL_ADDR | 0x400200C0 | FULL | Slave region, base address |
| PERI_MS_PPU_PR3_SL_SIZE | 0x400200C4 | FULL | Slave region, size |
| PERI_MS_PPU_PR3_SL_ATT0 | 0x400200D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_PR3_SL_ATT1 | 0x400200D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_PR3_SL_ATT2 | 0x400200D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_PR3_SL_ATT3 | 0x400200DC | FULL | Slave attributes 3 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_PR3_MS_ADDR | 0x400200E0 | FULL | Master region, base address |
| PERI_MS_PPU_PR3_MS_SIZE | 0x400200E4 | FULL | Master region, size |
| PERI_MS_PPU_PR3_MS_ATT0 | 0x400200F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_PR3_MS_ATT1 | 0x400200F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_PR3_MS_ATT2 | 0x400200F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_PR3_MS_ATT3 | 0x400200FC | FULL | Master attributes 3 |

## 23.5 PPU_PR 4

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_PR4_SL_ADDR | 0x40020100 | FULL | Slave region, base address |
| PERI_MS_PPU_PR4_SL_SIZE | 0x40020104 | FULL | Slave region, size |
| PERI_MS_PPU_PR4_SL_ATT0 | 0x40020110 | FULL | Slave attributes 0 |
| PERI_MS_PPU_PR4_SL_ATT1 | 0x40020114 | FULL | Slave attributes 1 |
| PERI_MS_PPU_PR4_SL_ATT2 | 0x40020118 | FULL | Slave attributes 2 |
| PERI_MS_PPU_PR4_SL_ATT3 | 0x4002011C | FULL | Slave attributes 3 |
| PERI_MS_PPU_PR4_MS_ADDR | 0x40020120 | FULL | Master region, base address |
| PERI_MS_PPU_PR4_MS_SIZE | 0x40020124 | FULL | Master region, size |
| PERI_MS_PPU_PR4_MS_ATT0 | 0x40020130 | FULL | Master attributes 0 |
| PERI_MS_PPU_PR4_MS_ATT1 | 0x40020134 | FULL | Master attributes 1 |
| PERI_MS_PPU_PR4_MS_ATT2 | 0x40020138 | FULL | Master attributes 2 |
| PERI_MS_PPU_PR4_MS_ATT3 | 0x4002013C | FULL | Master attributes 3 |

## 23.6 PPU_PR 5

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_PR5_SL_ADDR | 0x40020140 | FULL | Slave region, base address |
| PERI_MS_PPU_PR5_SL_SIZE | 0x40020144 | FULL | Slave region, size |
| PERI_MS_PPU_PR5_SL_ATT0 | 0x40020150 | FULL | Slave attributes 0 |
| PERI_MS_PPU_PR5_SL_ATT1 | 0x40020154 | FULL | Slave attributes 1 |
| PERI_MS_PPU_PR5_SL_ATT2 | 0x40020158 | FULL | Slave attributes 2 |
| PERI_MS_PPU_PR5_SL_ATT3 | 0x4002015C | FULL | Slave attributes 3 |
| PERI_MS_PPU_PR5_MS_ADDR | 0x40020160 | FULL | Master region, base address |
| PERI_MS_PPU_PR5_MS_SIZE | 0x40020164 | FULL | Master region, size |
| PERI_MS_PPU_PR5_MS_ATT0 | 0x40020170 | FULL | Master attributes 0 |
| PERI_MS_PPU_PR5_MS_ATT1 | 0x40020174 | FULL | Master attributes 1 |
| PERI_MS_PPU_PR5_MS_ATT2 | 0x40020178 | FULL | Master attributes 2 |
| PERI_MS_PPU_PR5_MS_ATT3 | 0x4002017C | FULL | Master attributes 3 |

## 23.7 PPU_PR 6

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_PR6_SL_ADDR | 0x40020180 | FULL | Slave region, base address |
| PERI_MS_PPU_PR6_SL_SIZE | 0x40020184 | FULL | Slave region, size |
| PERI_MS_PPU_PR6_SL_ATT0 | 0x40020190 | FULL | Slave attributes 0 |
| PERI_MS_PPU_PR6_SL_ATT1 | 0x40020194 | FULL | Slave attributes 1 |
| PERI_MS_PPU_PR6_SL_ATT2 | 0x40020198 | FULL | Slave attributes 2 |
| PERI_MS_PPU_PR6_SL_ATT3 | 0x4002019C | FULL | Slave attributes 3 |
| PERI_MS_PPU_PR6_MS_ADDR | 0x400201A0 | FULL | Master region, base address |
| PERI_MS_PPU_PR6_MS_SIZE | 0x400201A4 | FULL | Master region, size |
| PERI_MS_PPU_PR6_MS_ATT0 | 0x400201B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_PR6_MS_ATT1 | 0x400201B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_PR6_MS_ATT2 | 0x400201B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_PR6_MS_ATT3 | 0x400201BC | FULL | Master attributes 3 |

## 23.8 PPU_PR 7

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_PR7_SL_ADDR | 0x400201C0 | FULL | Slave region, base address |
| PERI_MS_PPU_PR7_SL_SIZE | 0x400201C4 | FULL | Slave region, size |
| PERI_MS_PPU_PR7_SL_ATT0 | 0x400201D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_PR7_SL_ATT1 | 0x400201D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_PR7_SL_ATT2 | 0x400201D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_PR7_SL_ATT3 | 0x400201DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_PR7_MS_ADDR | 0x400201E0 | FULL | Master region, base address |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_PR7_MS_SIZE | 0x400201E4 | FULL | Master region, size |
| PERI_MS_PPU_PR7_MS_ATT0 | 0x400201F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_PR7_MS_ATT1 | 0x400201F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_PR7_MS_ATT2 | 0x400201F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_PR7_MS_ATT3 | 0x400201FC | FULL | Master attributes 3 |

## 23.9 PPU_PR 8

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_PR8_SL_ADDR | 0x40020200 | FULL | Slave region, base address |
| PERI_MS_PPU_PR8_SL_SIZE | 0x40020204 | FULL | Slave region, size |
| PERI_MS_PPU_PR8_SL_ATT0 | 0x40020210 | FULL | Slave attributes 0 |
| PERI_MS_PPU_PR8_SL_ATT1 | 0x40020214 | FULL | Slave attributes 1 |
| PERI_MS_PPU_PR8_SL_ATT2 | 0x40020218 | FULL | Slave attributes 2 |
| PERI_MS_PPU_PR8_SL_ATT3 | 0x4002021C | FULL | Slave attributes 3 |
| PERI_MS_PPU_PR8_MS_ADDR | 0x40020220 | FULL | Master region, base address |
| PERI_MS_PPU_PR8_MS_SIZE | 0x40020224 | FULL | Master region, size |
| PERI_MS_PPU_PR8_MS_ATT0 | 0x40020230 | FULL | Master attributes 0 |
| PERI_MS_PPU_PR8_MS_ATT1 | 0x40020234 | FULL | Master attributes 1 |
| PERI_MS_PPU_PR8_MS_ATT2 | 0x40020238 | FULL | Master attributes 2 |
| PERI_MS_PPU_PR8_MS_ATT3 | 0x4002023C | FULL | Master attributes 3 |

## 23.10 PPU_PR 9

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_PR9_SL_ADDR | 0x40020240 | FULL | Slave region, base address |
| PERI_MS_PPU_PR9_SL_SIZE | 0x40020244 | FULL | Slave region, size |
| PERI_MS_PPU_PR9_SL_ATT0 | 0x40020250 | FULL | Slave attributes 0 |
| PERI_MS_PPU_PR9_SL_ATT1 | 0x40020254 | FULL | Slave attributes 1 |
| PERI_MS_PPU_PR9_SL_ATT2 | 0x40020258 | FULL | Slave attributes 2 |
| PERI_MS_PPU_PR9_SL_ATT3 | 0x4002025C | FULL | Slave attributes 3 |
| PERI_MS_PPU_PR9_MS_ADDR | 0x40020260 | FULL | Master region, base address |
| PERI_MS_PPU_PR9_MS_SIZE | 0x40020264 | FULL | Master region, size |
| PERI_MS_PPU_PR9_MS_ATT0 | 0x40020270 | FULL | Master attributes 0 |
| PERI_MS_PPU_PR9_MS_ATT1 | 0x40020274 | FULL | Master attributes 1 |
| PERI_MS_PPU_PR9_MS_ATT2 | 0x40020278 | FULL | Master attributes 2 |
| PERI_MS_PPU_PR9_MS_ATT3 | 0x4002027C | FULL | Master attributes 3 |

## 23.11 PPU_PR 10

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_PR10_SL_ADDR | 0x40020280 | FULL | Slave region, base address |
| PERI_MS_PPU_PR10_SL_SIZE | 0x40020284 | FULL | Slave region, size |
| PERI_MS_PPU_PR10_SL_ATT0 | 0x40020290 | FULL | Slave attributes 0 |
| PERI_MS_PPU_PR10_SL_ATT1 | 0x40020294 | FULL | Slave attributes 1 |
| PERI_MS_PPU_PR10_SL_ATT2 | 0x40020298 | FULL | Slave attributes 2 |
| PERI_MS_PPU_PR10_SL_ATT3 | 0x4002029C | FULL | Slave attributes 3 |
| PERI_MS_PPU_PR10_MS_ADDR | 0x400202A0 | FULL | Master region, base address |
| PERI_MS_PPU_PR10_MS_SIZE | 0x400202A4 | FULL | Master region, size |
| PERI_MS_PPU_PR10_MS_ATT0 | 0x400202B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_PR10_MS_ATT1 | 0x400202B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_PR10_MS_ATT2 | 0x400202B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_PR10_MS_ATT3 | 0x400202BC | FULL | Master attributes 3 |

## 23.12 PPU_PR 11

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_PR11_SL_ADDR | 0x400202C0 | FULL | Slave region, base address |
| PERI_MS_PPU_PR11_SL_SIZE | 0x400202C4 | FULL | Slave region, size |
| PERI_MS_PPU_PR11_SL_ATT0 | 0x400202D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_PR11_SL_ATT1 | 0x400202D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_PR11_SL_ATT2 | 0x400202D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_PR11_SL_ATT3 | 0x400202DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_PR11_MS_ADDR | 0x400202E0 | FULL | Master region, base address |
| PERI_MS_PPU_PR11_MS_SIZE | 0x400202E4 | FULL | Master region, size |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_PR11_MS_ATT0 | 0x400202F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_PR11_MS_ATT1 | 0x400202F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_PR11_MS_ATT2 | 0x400202F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_PR11_MS_ATT3 | 0x400202FC | FULL | Master attributes 3 |

## 23.13 PPU_PR 12

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_PR12_SL_ADDR | 0x40020300 | FULL | Slave region, base address |
| PERI_MS_PPU_PR12_SL_SIZE | 0x40020304 | FULL | Slave region, size |
| PERI_MS_PPU_PR12_SL_ATT0 | 0x40020310 | FULL | Slave attributes 0 |
| PERI_MS_PPU_PR12_SL_ATT1 | 0x40020314 | FULL | Slave attributes 1 |
| PERI_MS_PPU_PR12_SL_ATT2 | 0x40020318 | FULL | Slave attributes 2 |
| PERI_MS_PPU_PR12_SL_ATT3 | 0x4002031C | FULL | Slave attributes 3 |
| PERI_MS_PPU_PR12_MS_ADDR | 0x40020320 | FULL | Master region, base address |
| PERI_MS_PPU_PR12_MS_SIZE | 0x40020324 | FULL | Master region, size |
| PERI_MS_PPU_PR12_MS_ATT0 | 0x40020330 | FULL | Master attributes 0 |
| PERI_MS_PPU_PR12_MS_ATT1 | 0x40020334 | FULL | Master attributes 1 |
| PERI_MS_PPU_PR12_MS_ATT2 | 0x40020338 | FULL | Master attributes 2 |
| PERI_MS_PPU_PR12_MS_ATT3 | 0x4002033C | FULL | Master attributes 3 |

## 23.14 PPU_PR 13

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_PR13_SL_ADDR | 0x40020340 | FULL | Slave region, base address |
| PERI_MS_PPU_PR13_SL_SIZE | 0x40020344 | FULL | Slave region, size |
| PERI_MS_PPU_PR13_SL_ATT0 | 0x40020350 | FULL | Slave attributes 0 |
| PERI_MS_PPU_PR13_SL_ATT1 | 0x40020354 | FULL | Slave attributes 1 |
| PERI_MS_PPU_PR13_SL_ATT2 | 0x40020358 | FULL | Slave attributes 2 |
| PERI_MS_PPU_PR13_SL_ATT3 | 0x4002035C | FULL | Slave attributes 3 |
| PERI_MS_PPU_PR13_MS_ADDR | 0x40020360 | FULL | Master region, base address |
| PERI_MS_PPU_PR13_MS_SIZE | 0x40020364 | FULL | Master region, size |
| PERI_MS_PPU_PR13_MS_ATT0 | 0x40020370 | FULL | Master attributes 0 |
| PERI_MS_PPU_PR13_MS_ATT1 | 0x40020374 | FULL | Master attributes 1 |
| PERI_MS_PPU_PR13_MS_ATT2 | 0x40020378 | FULL | Master attributes 2 |
| PERI_MS_PPU_PR13_MS_ATT3 | 0x4002037C | FULL | Master attributes 3 |

## 23.15 PPU_PR 14

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_PR14_SL_ADDR | 0x40020380 | FULL | Slave region, base address |
| PERI_MS_PPU_PR14_SL_SIZE | 0x40020384 | FULL | Slave region, size |
| PERI_MS_PPU_PR14_SL_ATT0 | 0x40020390 | FULL | Slave attributes 0 |
| PERI_MS_PPU_PR14_SL_ATT1 | 0x40020394 | FULL | Slave attributes 1 |
| PERI_MS_PPU_PR14_SL_ATT2 | 0x40020398 | FULL | Slave attributes 2 |
| PERI_MS_PPU_PR14_SL_ATT3 | 0x4002039C | FULL | Slave attributes 3 |
| PERI_MS_PPU_PR14_MS_ADDR | 0x400203A0 | FULL | Master region, base address |
| PERI_MS_PPU_PR14_MS_SIZE | 0x400203A4 | FULL | Master region, size |
| PERI_MS_PPU_PR14_MS_ATT0 | 0x400203B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_PR14_MS_ATT1 | 0x400203B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_PR14_MS_ATT2 | 0x400203B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_PR14_MS_ATT3 | 0x400203BC | FULL | Master attributes 3 |

## 23.16 PPU_PR 15

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_PR15_SL_ADDR | 0x400203C0 | FULL | Slave region, base address |
| PERI_MS_PPU_PR15_SL_SIZE | 0x400203C4 | FULL | Slave region, size |
| PERI_MS_PPU_PR15_SL_ATT0 | 0x400203D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_PR15_SL_ATT1 | 0x400203D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_PR15_SL_ATT2 | 0x400203D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_PR15_SL_ATT3 | 0x400203DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_PR15_MS_ADDR | 0x400203E0 | FULL | Master region, base address |
| PERI_MS_PPU_PR15_MS_SIZE | 0x400203E4 | FULL | Master region, size |
| PERI_MS_PPU_PR15_MS_ATT0 | 0x400203F0 | FULL | Master attributes 0 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_PR15_MS_ATT1 | 0x400203F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_PR15_MS_ATT2 | 0x400203F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_PR15_MS_ATT3 | 0x400203FC | FULL | Master attributes 3 |

## 23.17 PPU_FX 0

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX0_SL_ADDR | 0x40020800 | FULL | Slave region, base address |
| PERI_MS_PPU_FX0_SL_SIZE | 0x40020804 | FULL | Slave region, size |
| PERI_MS_PPU_FX0_SL_ATT0 | 0x40020810 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX0_SL_ATT1 | 0x40020814 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX0_SL_ATT2 | 0x40020818 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX0_SL_ATT3 | 0x4002081C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX0_MS_ADDR | 0x40020820 | FULL | Master region, base address |
| PERI_MS_PPU_FX0_MS_SIZE | 0x40020824 | FULL | Master region, size |
| PERI_MS_PPU_FX0_MS_ATT0 | 0x40020830 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX0_MS_ATT1 | 0x40020834 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX0_MS_ATT2 | 0x40020838 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX0_MS_ATT3 | 0x4002083C | FULL | Master attributes 3 |

## 23.18 PPU_FX 1

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX1_SL_ADDR | 0x40020840 | FULL | Slave region, base address |
| PERI_MS_PPU_FX1_SL_SIZE | 0x40020844 | FULL | Slave region, size |
| PERI_MS_PPU_FX1_SL_ATT0 | 0x40020850 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX1_SL_ATT1 | 0x40020854 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX1_SL_ATT2 | 0x40020858 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX1_SL_ATT3 | 0x4002085C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX1_MS_ADDR | 0x40020860 | FULL | Master region, base address |
| PERI_MS_PPU_FX1_MS_SIZE | 0x40020864 | FULL | Master region, size |
| PERI_MS_PPU_FX1_MS_ATT0 | 0x40020870 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX1_MS_ATT1 | 0x40020874 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX1_MS_ATT2 | 0x40020878 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX1_MS_ATT3 | 0x4002087C | FULL | Master attributes 3 |

## 23.19 PPU_FX 2

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX2_SL_ADDR | 0x40020880 | FULL | Slave region, base address |
| PERI_MS_PPU_FX2_SL_SIZE | 0x40020884 | FULL | Slave region, size |
| PERI_MS_PPU_FX2_SL_ATT0 | 0x40020890 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX2_SL_ATT1 | 0x40020894 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX2_SL_ATT2 | 0x40020898 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX2_SL_ATT3 | 0x4002089C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX2_MS_ADDR | 0x400208A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX2_MS_SIZE | 0x400208A4 | FULL | Master region, size |
| PERI_MS_PPU_FX2_MS_ATT0 | 0x400208B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX2_MS_ATT1 | 0x400208B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX2_MS_ATT2 | 0x400208B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX2_MS_ATT3 | 0x400208BC | FULL | Master attributes 3 |

## 23.20 PPU_FX 3

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX3_SL_ADDR | 0x400208C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX3_SL_SIZE | 0x400208C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX3_SL_ATT0 | 0x400208D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX3_SL_ATT1 | 0x400208D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX3_SL_ATT2 | 0x400208D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX3_SL_ATT3 | 0x400208DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX3_MS_ADDR | 0x400208E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX3_MS_SIZE | 0x400208E4 | FULL | Master region, size |
| PERI_MS_PPU_FX3_MS_ATT0 | 0x400208F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX3_MS_ATT1 | 0x400208F4 | FULL | Master attributes 1 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX3_MS_ATT2 | 0x400208F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX3_MS_ATT3 | 0x400208FC | FULL | Master attributes 3 |

## 23.21 PPU_FX 4

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX4_SL_ADDR | 0x40020900 | FULL | Slave region, base address |
| PERI_MS_PPU_FX4_SL_SIZE | 0x40020904 | FULL | Slave region, size |
| PERI_MS_PPU_FX4_SL_ATT0 | 0x40020910 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX4_SL_ATT1 | 0x40020914 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX4_SL_ATT2 | 0x40020918 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX4_SL_ATT3 | 0x4002091C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX4_MS_ADDR | 0x40020920 | FULL | Master region, base address |
| PERI_MS_PPU_FX4_MS_SIZE | 0x40020924 | FULL | Master region, size |
| PERI_MS_PPU_FX4_MS_ATT0 | 0x40020930 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX4_MS_ATT1 | 0x40020934 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX4_MS_ATT2 | 0x40020938 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX4_MS_ATT3 | 0x4002093C | FULL | Master attributes 3 |

## 23.22 PPU_FX 5

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX5_SL_ADDR | 0x40020940 | FULL | Slave region, base address |
| PERI_MS_PPU_FX5_SL_SIZE | 0x40020944 | FULL | Slave region, size |
| PERI_MS_PPU_FX5_SL_ATT0 | 0x40020950 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX5_SL_ATT1 | 0x40020954 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX5_SL_ATT2 | 0x40020958 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX5_SL_ATT3 | 0x4002095C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX5_MS_ADDR | 0x40020960 | FULL | Master region, base address |
| PERI_MS_PPU_FX5_MS_SIZE | 0x40020964 | FULL | Master region, size |
| PERI_MS_PPU_FX5_MS_ATT0 | 0x40020970 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX5_MS_ATT1 | 0x40020974 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX5_MS_ATT2 | 0x40020978 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX5_MS_ATT3 | 0x4002097C | FULL | Master attributes 3 |

## 23.23 PPU_FX 6

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX6_SL_ADDR | 0x40020980 | FULL | Slave region, base address |
| PERI_MS_PPU_FX6_SL_SIZE | 0x40020984 | FULL | Slave region, size |
| PERI_MS_PPU_FX6_SL_ATT0 | 0x40020990 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX6_SL_ATT1 | 0x40020994 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX6_SL_ATT2 | 0x40020998 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX6_SL_ATT3 | 0x4002099C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX6_MS_ADDR | 0x400209A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX6_MS_SIZE | 0x400209A4 | FULL | Master region, size |
| PERI_MS_PPU_FX6_MS_ATT0 | 0x400209B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX6_MS_ATT1 | 0x400209B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX6_MS_ATT2 | 0x400209B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX6_MS_ATT3 | 0x400209BC | FULL | Master attributes 3 |

## 23.24 PPU_FX 7

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX7_SL_ADDR | 0x400209C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX7_SL_SIZE | 0x400209C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX7_SL_ATT0 | 0x400209D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX7_SL_ATT1 | 0x400209D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX7_SL_ATT2 | 0x400209D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX7_SL_ATT3 | 0x400209DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX7_MS_ADDR | 0x400209E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX7_MS_SIZE | 0x400209E4 | FULL | Master region, size |
| PERI_MS_PPU_FX7_MS_ATT0 | 0x400209F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX7_MS_ATT1 | 0x400209F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX7_MS_ATT2 | 0x400209F8 | FULL | Master attributes 2 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX7_MS_ATT3 | 0x400209FC | FULL | Master attributes 3 |

## 23.25 PPU_FX 8

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX8_SL_ADDR | 0x40020A00 | FULL | Slave region, base address |
| PERI_MS_PPU_FX8_SL_SIZE | 0x40020A04 | FULL | Slave region, size |
| PERI_MS_PPU_FX8_SL_ATT0 | 0x40020A10 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX8_SL_ATT1 | 0x40020A14 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX8_SL_ATT2 | 0x40020A18 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX8_SL_ATT3 | 0x40020A1C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX8_MS_ADDR | 0x40020A20 | FULL | Master region, base address |
| PERI_MS_PPU_FX8_MS_SIZE | 0x40020A24 | FULL | Master region, size |
| PERI_MS_PPU_FX8_MS_ATT0 | 0x40020A30 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX8_MS_ATT1 | 0x40020A34 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX8_MS_ATT2 | 0x40020A38 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX8_MS_ATT3 | 0x40020A3C | FULL | Master attributes 3 |

## 23.26 PPU_FX 9

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX9_SL_ADDR | 0x40020A40 | FULL | Slave region, base address |
| PERI_MS_PPU_FX9_SL_SIZE | 0x40020A44 | FULL | Slave region, size |
| PERI_MS_PPU_FX9_SL_ATT0 | 0x40020A50 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX9_SL_ATT1 | 0x40020A54 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX9_SL_ATT2 | 0x40020A58 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX9_SL_ATT3 | 0x40020A5C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX9_MS_ADDR | 0x40020A60 | FULL | Master region, base address |
| PERI_MS_PPU_FX9_MS_SIZE | 0x40020A64 | FULL | Master region, size |
| PERI_MS_PPU_FX9_MS_ATT0 | 0x40020A70 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX9_MS_ATT1 | 0x40020A74 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX9_MS_ATT2 | 0x40020A78 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX9_MS_ATT3 | 0x40020A7C | FULL | Master attributes 3 |

## 23.27 PPU_FX 10

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX10_SL_ADDR | 0x40020A80 | FULL | Slave region, base address |
| PERI_MS_PPU_FX10_SL_SIZE | 0x40020A84 | FULL | Slave region, size |
| PERI_MS_PPU_FX10_SL_ATT0 | 0x40020A90 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX10_SL_ATT1 | 0x40020A94 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX10_SL_ATT2 | 0x40020A98 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX10_SL_ATT3 | 0x40020A9C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX10_MS_ADDR | 0x40020AA0 | FULL | Master region, base address |
| PERI_MS_PPU_FX10_MS_SIZE | 0x40020AA4 | FULL | Master region, size |
| PERI_MS_PPU_FX10_MS_ATT0 | 0x40020AB0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX10_MS_ATT1 | 0x40020AB4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX10_MS_ATT2 | 0x40020AB8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX10_MS_ATT3 | 0x40020ABC | FULL | Master attributes 3 |

## 23.28 PPU_FX 11

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX11_SL_ADDR | 0x40020AC0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX11_SL_SIZE | 0x40020AC4 | FULL | Slave region, size |
| PERI_MS_PPU_FX11_SL_ATT0 | 0x40020AD0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX11_SL_ATT1 | 0x40020AD4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX11_SL_ATT2 | 0x40020AD8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX11_SL_ATT3 | 0x40020ADC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX11_MS_ADDR | 0x40020AE0 | FULL | Master region, base address |
| PERI_MS_PPU_FX11_MS_SIZE | 0x40020AE4 | FULL | Master region, size |
| PERI_MS_PPU_FX11_MS_ATT0 | 0x40020AF0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX11_MS_ATT1 | 0x40020AF4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX11_MS_ATT2 | 0x40020AF8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX11_MS_ATT3 | 0x40020AFC | FULL | Master attributes 3 |

## 23.29 PPU_FX 12

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX12_SL_ADDR | 0x40020B00 | FULL | Slave region, base address |
| PERI_MS_PPU_FX12_SL_SIZE | 0x40020B04 | FULL | Slave region, size |
| PERI_MS_PPU_FX12_SL_ATT0 | 0x40020B10 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX12_SL_ATT1 | 0x40020B14 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX12_SL_ATT2 | 0x40020B18 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX12_SL_ATT3 | 0x40020B1C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX12_MS_ADDR | 0x40020B20 | FULL | Master region, base address |
| PERI_MS_PPU_FX12_MS_SIZE | 0x40020B24 | FULL | Master region, size |
| PERI_MS_PPU_FX12_MS_ATT0 | 0x40020B30 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX12_MS_ATT1 | 0x40020B34 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX12_MS_ATT2 | 0x40020B38 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX12_MS_ATT3 | 0x40020B3C | FULL | Master attributes 3 |

## 23.30 PPU_FX 13

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX13_SL_ADDR | 0x40020B40 | READ | Slave region, base address |
| PERI_MS_PPU_FX13_SL_SIZE | 0x40020B44 | READ | Slave region, size |
| PERI_MS_PPU_FX13_SL_ATT0 | 0x40020B50 | READ | Slave attributes 0 |
| PERI_MS_PPU_FX13_SL_ATT1 | 0x40020B54 | READ | Slave attributes 1 |
| PERI_MS_PPU_FX13_SL_ATT2 | 0x40020B58 | READ | Slave attributes 2 |
| PERI_MS_PPU_FX13_SL_ATT3 | 0x40020B5C | READ | Slave attributes 3 |
| PERI_MS_PPU_FX13_MS_ADDR | 0x40020B60 | READ | Master region, base address |
| PERI_MS_PPU_FX13_MS_SIZE | 0x40020B64 | READ | Master region, size |
| PERI_MS_PPU_FX13_MS_ATT0 | 0x40020B70 | READ | Master attributes 0 |
| PERI_MS_PPU_FX13_MS_ATT1 | 0x40020B74 | READ | Master attributes 1 |
| PERI_MS_PPU_FX13_MS_ATT2 | 0x40020B78 | READ | Master attributes 2 |
| PERI_MS_PPU_FX13_MS_ATT3 | 0x40020B7C | READ | Master attributes 3 |

## 23.31 PPU_FX 14

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX14_SL_ADDR | 0x40020B80 | FULL | Slave region, base address |
| PERI_MS_PPU_FX14_SL_SIZE | 0x40020B84 | FULL | Slave region, size |
| PERI_MS_PPU_FX14_SL_ATT0 | 0x40020B90 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX14_SL_ATT1 | 0x40020B94 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX14_SL_ATT2 | 0x40020B98 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX14_SL_ATT3 | 0x40020B9C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX14_MS_ADDR | 0x40020BA0 | FULL | Master region, base address |
| PERI_MS_PPU_FX14_MS_SIZE | 0x40020BA4 | FULL | Master region, size |
| PERI_MS_PPU_FX14_MS_ATT0 | 0x40020BB0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX14_MS_ATT1 | 0x40020BB4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX14_MS_ATT2 | 0x40020BB8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX14_MS_ATT3 | 0x40020BBC | FULL | Master attributes 3 |

## 23.32 PPU_FX 15

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX15_SL_ADDR | 0x40020BC0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX15_SL_SIZE | 0x40020BC4 | FULL | Slave region, size |
| PERI_MS_PPU_FX15_SL_ATT0 | 0x40020BD0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX15_SL_ATT1 | 0x40020BD4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX15_SL_ATT2 | 0x40020BD8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX15_SL_ATT3 | 0x40020BDC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX15_MS_ADDR | 0x40020BE0 | FULL | Master region, base address |
| PERI_MS_PPU_FX15_MS_SIZE | 0x40020BE4 | FULL | Master region, size |
| PERI_MS_PPU_FX15_MS_ATT0 | 0x40020BF0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX15_MS_ATT1 | 0x40020BF4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX15_MS_ATT2 | 0x40020BF8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX15_MS_ATT3 | 0x40020BFC | FULL | Master attributes 3 |

## 23.33 PPU_FX 16

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX16_SL_ADDR | 0x40020C00 | FULL | Slave region, base address |
| PERI_MS_PPU_FX16_SL_SIZE | 0x40020C04 | FULL | Slave region, size |
| PERI_MS_PPU_FX16_SL_ATT0 | 0x40020C10 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX16_SL_ATT1 | 0x40020C14 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX16_SL_ATT2 | 0x40020C18 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX16_SL_ATT3 | 0x40020C1C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX16_MS_ADDR | 0x40020C20 | FULL | Master region, base address |
| PERI_MS_PPU_FX16_MS_SIZE | 0x40020C24 | FULL | Master region, size |
| PERI_MS_PPU_FX16_MS_ATT0 | 0x40020C30 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX16_MS_ATT1 | 0x40020C34 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX16_MS_ATT2 | 0x40020C38 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX16_MS_ATT3 | 0x40020C3C | FULL | Master attributes 3 |

## 23.34 PPU_FX 17

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX17_SL_ADDR | 0x40020C40 | FULL | Slave region, base address |
| PERI_MS_PPU_FX17_SL_SIZE | 0x40020C44 | FULL | Slave region, size |
| PERI_MS_PPU_FX17_SL_ATT0 | 0x40020C50 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX17_SL_ATT1 | 0x40020C54 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX17_SL_ATT2 | 0x40020C58 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX17_SL_ATT3 | 0x40020C5C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX17_MS_ADDR | 0x40020C60 | FULL | Master region, base address |
| PERI_MS_PPU_FX17_MS_SIZE | 0x40020C64 | FULL | Master region, size |
| PERI_MS_PPU_FX17_MS_ATT0 | 0x40020C70 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX17_MS_ATT1 | 0x40020C74 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX17_MS_ATT2 | 0x40020C78 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX17_MS_ATT3 | 0x40020C7C | FULL | Master attributes 3 |

## 23.35 PPU_FX 18

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX18_SL_ADDR | 0x40020C80 | FULL | Slave region, base address |
| PERI_MS_PPU_FX18_SL_SIZE | 0x40020C84 | FULL | Slave region, size |
| PERI_MS_PPU_FX18_SL_ATT0 | 0x40020C90 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX18_SL_ATT1 | 0x40020C94 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX18_SL_ATT2 | 0x40020C98 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX18_SL_ATT3 | 0x40020C9C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX18_MS_ADDR | 0x40020CA0 | FULL | Master region, base address |
| PERI_MS_PPU_FX18_MS_SIZE | 0x40020CA4 | FULL | Master region, size |
| PERI_MS_PPU_FX18_MS_ATT0 | 0x40020CB0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX18_MS_ATT1 | 0x40020CB4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX18_MS_ATT2 | 0x40020CB8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX18_MS_ATT3 | 0x40020CBC | FULL | Master attributes 3 |

## 23.36 PPU_FX 19

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX19_SL_ADDR | 0x40020CC0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX19_SL_SIZE | 0x40020CC4 | FULL | Slave region, size |
| PERI_MS_PPU_FX19_SL_ATT0 | 0x40020CD0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX19_SL_ATT1 | 0x40020CD4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX19_SL_ATT2 | 0x40020CD8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX19_SL_ATT3 | 0x40020CDC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX19_MS_ADDR | 0x40020CE0 | FULL | Master region, base address |
| PERI_MS_PPU_FX19_MS_SIZE | 0x40020CE4 | FULL | Master region, size |
| PERI_MS_PPU_FX19_MS_ATT0 | 0x40020CF0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX19_MS_ATT1 | 0x40020CF4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX19_MS_ATT2 | 0x40020CF8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX19_MS_ATT3 | 0x40020CFC | FULL | Master attributes 3 |

## 23.37 PPU_FX 20

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX20_SL_ADDR | 0x40020D00 | FULL | Slave region, base address |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX20_SL_SIZE | 0x40020D04 | FULL | Slave region, size |
| PERI_MS_PPU_FX20_SL_ATT0 | 0x40020D10 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX20_SL_ATT1 | 0x40020D14 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX20_SL_ATT2 | 0x40020D18 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX20_SL_ATT3 | 0x40020D1C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX20_MS_ADDR | 0x40020D20 | FULL | Master region, base address |
| PERI_MS_PPU_FX20_MS_SIZE | 0x40020D24 | FULL | Master region, size |
| PERI_MS_PPU_FX20_MS_ATT0 | 0x40020D30 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX20_MS_ATT1 | 0x40020D34 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX20_MS_ATT2 | 0x40020D38 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX20_MS_ATT3 | 0x40020D3C | FULL | Master attributes 3 |

## 23.38 PPU_FX 21

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX21_SL_ADDR | 0x40020D40 | FULL | Slave region, base address |
| PERI_MS_PPU_FX21_SL_SIZE | 0x40020D44 | FULL | Slave region, size |
| PERI_MS_PPU_FX21_SL_ATT0 | 0x40020D50 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX21_SL_ATT1 | 0x40020D54 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX21_SL_ATT2 | 0x40020D58 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX21_SL_ATT3 | 0x40020D5C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX21_MS_ADDR | 0x40020D60 | FULL | Master region, base address |
| PERI_MS_PPU_FX21_MS_SIZE | 0x40020D64 | FULL | Master region, size |
| PERI_MS_PPU_FX21_MS_ATT0 | 0x40020D70 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX21_MS_ATT1 | 0x40020D74 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX21_MS_ATT2 | 0x40020D78 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX21_MS_ATT3 | 0x40020D7C | FULL | Master attributes 3 |

## 23.39 PPU_FX 22

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX22_SL_ADDR | 0x40020D80 | FULL | Slave region, base address |
| PERI_MS_PPU_FX22_SL_SIZE | 0x40020D84 | FULL | Slave region, size |
| PERI_MS_PPU_FX22_SL_ATT0 | 0x40020D90 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX22_SL_ATT1 | 0x40020D94 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX22_SL_ATT2 | 0x40020D98 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX22_SL_ATT3 | 0x40020D9C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX22_MS_ADDR | 0x40020DA0 | FULL | Master region, base address |
| PERI_MS_PPU_FX22_MS_SIZE | 0x40020DA4 | FULL | Master region, size |
| PERI_MS_PPU_FX22_MS_ATT0 | 0x40020DB0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX22_MS_ATT1 | 0x40020DB4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX22_MS_ATT2 | 0x40020DB8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX22_MS_ATT3 | 0x40020DBC | FULL | Master attributes 3 |

## 23.40 PPU_FX 23

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX23_SL_ADDR | 0x40020DC0 | PRIVILEGE - WRITE | Slave region, base address |
| PERI_MS_PPU_FX23_SL_SIZE | 0x40020DC4 | PRIVILEGE - WRITE | Slave region, size |
| PERI_MS_PPU_FX23_SL_ATT0 | 0x40020DD0 | PRIVILEGE - WRITE | Slave attributes 0 |
| PERI_MS_PPU_FX23_SL_ATT1 | 0x40020DD4 | PRIVILEGE - WRITE | Slave attributes 1 |
| PERI_MS_PPU_FX23_SL_ATT2 | 0x40020DD8 | PRIVILEGE - WRITE | Slave attributes 2 |
| PERI_MS_PPU_FX23_SL_ATT3 | 0x40020DDC | PRIVILEGE - WRITE | Slave attributes 3 |
| PERI_MS_PPU_FX23_MS_ADDR | 0x40020DE0 | PRIVILEGE - WRITE | Master region, base address |
| PERI_MS_PPU_FX23_MS_SIZE | 0x40020DE4 | PRIVILEGE - WRITE | Master region, size |
| PERI_MS_PPU_FX23_MS_ATT0 | 0x40020DF0 | PRIVILEGE - WRITE | Master attributes 0 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX23_MS_ATT1 | 0x40020DF4 | PRIVILEGE - WRITE | Master attributes 1 |
| PERI_MS_PPU_FX23_MS_ATT2 | 0x40020DF8 | PRIVILEGE - WRITE | Master attributes 2 |
| PERI_MS_PPU_FX23_MS_ATT3 | 0x40020DFC | PRIVILEGE - WRITE | Master attributes 3 |

## 23.41 PPU_FX 24

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX24_SL_ADDR | 0x40020E00 | PRIVILEGE - WRITE | Slave region, base address |
| PERI_MS_PPU_FX24_SL_SIZE | 0x40020E04 | PRIVILEGE - WRITE | Slave region, size |
| PERI_MS_PPU_FX24_SL_ATT0 | 0x40020E10 | PRIVILEGE - WRITE | Slave attributes 0 |
| PERI_MS_PPU_FX24_SL_ATT1 | 0x40020E14 | PRIVILEGE - WRITE | Slave attributes 1 |
| PERI_MS_PPU_FX24_SL_ATT2 | 0x40020E18 | PRIVILEGE - WRITE | Slave attributes 2 |
| PERI_MS_PPU_FX24_SL_ATT3 | 0x40020E1C | PRIVILEGE - WRITE | Slave attributes 3 |
| PERI_MS_PPU_FX24_MS_ADDR | 0x40020E20 | PRIVILEGE - WRITE | Master region, base address |
| PERI_MS_PPU_FX24_MS_SIZE | 0x40020E24 | PRIVILEGE - WRITE | Master region, size |
| PERI_MS_PPU_FX24_MS_ATT0 | 0x40020E30 | PRIVILEGE - WRITE | Master attributes 0 |
| PERI_MS_PPU_FX24_MS_ATT1 | 0x40020E34 | PRIVILEGE - WRITE | Master attributes 1 |
| PERI_MS_PPU_FX24_MS_ATT2 | 0x40020E38 | PRIVILEGE - WRITE | Master attributes 2 |
| PERI_MS_PPU_FX24_MS_ATT3 | 0x40020E3C | PRIVILEGE - WRITE | Master attributes 3 |

## 23.42 PPU_FX 25

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX25_SL_ADDR | 0x40020E40 | READ | Slave region, base address |
| PERI_MS_PPU_FX25_SL_SIZE | 0x40020E44 | READ | Slave region, size |
| PERI_MS_PPU_FX25_SL_ATT0 | 0x40020E50 | READ | Slave attributes 0 |
| PERI_MS_PPU_FX25_SL_ATT1 | 0x40020E54 | READ | Slave attributes 1 |
| PERI_MS_PPU_FX25_SL_ATT2 | 0x40020E58 | READ | Slave attributes 2 |
| PERI_MS_PPU_FX25_SL_ATT3 | 0x40020E5C | READ | Slave attributes 3 |
| PERI_MS_PPU_FX25_MS_ADDR | 0x40020E60 | READ | Master region, base address |
| PERI_MS_PPU_FX25_MS_SIZE | 0x40020E64 | READ | Master region, size |
| PERI_MS_PPU_FX25_MS_ATT0 | 0x40020E70 | READ | Master attributes 0 |
| PERI_MS_PPU_FX25_MS_ATT1 | 0x40020E74 | READ | Master attributes 1 |
| PERI_MS_PPU_FX25_MS_ATT2 | 0x40020E78 | READ | Master attributes 2 |
| PERI_MS_PPU_FX25_MS_ATT3 | 0x40020E7C | READ | Master attributes 3 |

## 23.43 PPU_FX 26

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX26_SL_ADDR | 0x40020E80 | FULL | Slave region, base address |
| PERI_MS_PPU_FX26_SL_SIZE | 0x40020E84 | FULL | Slave region, size |
| PERI_MS_PPU_FX26_SL_ATT0 | 0x40020E90 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX26_SL_ATT1 | 0x40020E94 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX26_SL_ATT2 | 0x40020E98 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX26_SL_ATT3 | 0x40020E9C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX26_MS_ADDR | 0x40020EA0 | FULL | Master region, base address |
| PERI_MS_PPU_FX26_MS_SIZE | 0x40020EA4 | FULL | Master region, size |
| PERI_MS_PPU_FX26_MS_ATT0 | 0x40020EB0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX26_MS_ATT1 | 0x40020EB4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX26_MS_ATT2 | 0x40020EB8 | FULL | Master attributes 2 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX26_MS_ATT3 | 0x40020EBC | FULL | Master attributes 3 |

## 23.44 PPU_FX 27

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX27_SL_ADDR | 0x40020EC0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX27_SL_SIZE | 0x40020EC4 | FULL | Slave region, size |
| PERI_MS_PPU_FX27_SL_ATT0 | 0x40020ED0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX27_SL_ATT1 | 0x40020ED4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX27_SL_ATT2 | 0x40020ED8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX27_SL_ATT3 | 0x40020EDC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX27_MS_ADDR | 0x40020EE0 | FULL | Master region, base address |
| PERI_MS_PPU_FX27_MS_SIZE | 0x40020EE4 | FULL | Master region, size |
| PERI_MS_PPU_FX27_MS_ATT0 | 0x40020EF0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX27_MS_ATT1 | 0x40020EF4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX27_MS_ATT2 | 0x40020EF8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX27_MS_ATT3 | 0x40020EFC | FULL | Master attributes 3 |

## 23.45 PPU_FX 28

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX28_SL_ADDR | 0x40020F00 | PRIVILEGE - WRITE | Slave region, base address |
| PERI_MS_PPU_FX28_SL_SIZE | 0x40020F04 | PRIVILEGE - WRITE | Slave region, size |
| PERI_MS_PPU_FX28_SL_ATT0 | 0x40020F10 | PRIVILEGE - WRITE | Slave attributes 0 |
| PERI_MS_PPU_FX28_SL_ATT1 | 0x40020F14 | PRIVILEGE - WRITE | Slave attributes 1 |
| PERI_MS_PPU_FX28_SL_ATT2 | 0x40020F18 | PRIVILEGE - WRITE | Slave attributes 2 |
| PERI_MS_PPU_FX28_SL_ATT3 | 0x40020F1C | PRIVILEGE - WRITE | Slave attributes 3 |
| PERI_MS_PPU_FX28_MS_ADDR | 0x40020F20 | PRIVILEGE - WRITE | Master region, base address |
| PERI_MS_PPU_FX28_MS_SIZE | 0x40020F24 | PRIVILEGE - WRITE | Master region, size |
| PERI_MS_PPU_FX28_MS_ATT0 | 0x40020F30 | PRIVILEGE - WRITE | Master attributes 0 |
| PERI_MS_PPU_FX28_MS_ATT1 | 0x40020F34 | PRIVILEGE - WRITE | Master attributes 1 |
| PERI_MS_PPU_FX28_MS_ATT2 | 0x40020F38 | PRIVILEGE - WRITE | Master attributes 2 |
| PERI_MS_PPU_FX28_MS_ATT3 | 0x40020F3C | PRIVILEGE - WRITE | Master attributes 3 |

## 23.46 PPU_FX 29

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX29_SL_ADDR | 0x40020F40 | FULL | Slave region, base address |
| PERI_MS_PPU_FX29_SL_SIZE | 0x40020F44 | FULL | Slave region, size |
| PERI_MS_PPU_FX29_SL_ATT0 | 0x40020F50 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX29_SL_ATT1 | 0x40020F54 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX29_SL_ATT2 | 0x40020F58 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX29_SL_ATT3 | 0x40020F5C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX29_MS_ADDR | 0x40020F60 | FULL | Master region, base address |
| PERI_MS_PPU_FX29_MS_SIZE | 0x40020F64 | FULL | Master region, size |
| PERI_MS_PPU_FX29_MS_ATT0 | 0x40020F70 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX29_MS_ATT1 | 0x40020F74 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX29_MS_ATT2 | 0x40020F78 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX29_MS_ATT3 | 0x40020F7C | FULL | Master attributes 3 |

## 23.47 PPU_FX 30

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX30_SL_ADDR | 0x40020F80 | FULL | Slave region, base address |
| PERI_MS_PPU_FX30_SL_SIZE | 0x40020F84 | FULL | Slave region, size |
| PERI_MS_PPU_FX30_SL_ATT0 | 0x40020F90 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX30_SL_ATT1 | 0x40020F94 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX30_SL_ATT2 | 0x40020F98 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX30_SL_ATT3 | 0x40020F9C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX30_MS_ADDR | 0x40020FA0 | FULL | Master region, base address |
| PERI_MS_PPU_FX30_MS_SIZE | 0x40020FA4 | FULL | Master region, size |
| PERI_MS_PPU_FX30_MS_ATT0 | 0x40020FB0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX30_MS_ATT1 | 0x40020FB4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX30_MS_ATT2 | 0x40020FB8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX30_MS_ATT3 | 0x40020FBC | FULL | Master attributes 3 |

## 23.48 PPU_FX 31

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX31_SL_ADDR | 0x40020FC0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX31_SL_SIZE | 0x40020FC4 | FULL | Slave region, size |
| PERI_MS_PPU_FX31_SL_ATT0 | 0x40020FD0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX31_SL_ATT1 | 0x40020FD4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX31_SL_ATT2 | 0x40020FD8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX31_SL_ATT3 | 0x40020FDC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX31_MS_ADDR | 0x40020FE0 | FULL | Master region, base address |
| PERI_MS_PPU_FX31_MS_SIZE | 0x40020FE4 | FULL | Master region, size |
| PERI_MS_PPU_FX31_MS_ATT0 | 0x40020FF0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX31_MS_ATT1 | 0x40020FF4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX31_MS_ATT2 | 0x40020FF8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX31_MS_ATT3 | 0x40020FFC | FULL | Master attributes 3 |

## 23.49 PPU_FX 32

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX32_SL_ADDR | 0x40021000 | READ | Slave region, base address |
| PERI_MS_PPU_FX32_SL_SIZE | 0x40021004 | READ | Slave region, size |
| PERI_MS_PPU_FX32_SL_ATT0 | 0x40021010 | READ | Slave attributes 0 |
| PERI_MS_PPU_FX32_SL_ATT1 | 0x40021014 | READ | Slave attributes 1 |
| PERI_MS_PPU_FX32_SL_ATT2 | 0x40021018 | READ | Slave attributes 2 |
| PERI_MS_PPU_FX32_SL_ATT3 | 0x4002101C | READ | Slave attributes 3 |
| PERI_MS_PPU_FX32_MS_ADDR | 0x40021020 | READ | Master region, base address |
| PERI_MS_PPU_FX32_MS_SIZE | 0x40021024 | READ | Master region, size |
| PERI_MS_PPU_FX32_MS_ATT0 | 0x40021030 | READ | Master attributes 0 |
| PERI_MS_PPU_FX32_MS_ATT1 | 0x40021034 | READ | Master attributes 1 |
| PERI_MS_PPU_FX32_MS_ATT2 | 0x40021038 | READ | Master attributes 2 |
| PERI_MS_PPU_FX32_MS_ATT3 | 0x4002103C | READ | Master attributes 3 |

## 23.50 PPU_FX 33

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX33_SL_ADDR | 0x40021040 | FULL | Slave region, base address |
| PERI_MS_PPU_FX33_SL_SIZE | 0x40021044 | FULL | Slave region, size |
| PERI_MS_PPU_FX33_SL_ATT0 | 0x40021050 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX33_SL_ATT1 | 0x40021054 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX33_SL_ATT2 | 0x40021058 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX33_SL_ATT3 | 0x4002105C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX33_MS_ADDR | 0x40021060 | FULL | Master region, base address |
| PERI_MS_PPU_FX33_MS_SIZE | 0x40021064 | FULL | Master region, size |
| PERI_MS_PPU_FX33_MS_ATT0 | 0x40021070 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX33_MS_ATT1 | 0x40021074 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX33_MS_ATT2 | 0x40021078 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX33_MS_ATT3 | 0x4002107C | FULL | Master attributes 3 |

## 23.51 PPU_FX 34

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX34_SL_ADDR | 0x40021080 | FULL | Slave region, base address |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX34_SL_SIZE | 0x40021084 | FULL | Slave region, size |
| PERI_MS_PPU_FX34_SL_ATT0 | 0x40021090 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX34_SL_ATT1 | 0x40021094 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX34_SL_ATT2 | 0x40021098 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX34_SL_ATT3 | 0x4002109C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX34_MS_ADDR | 0x400210A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX34_MS_SIZE | 0x400210A4 | FULL | Master region, size |
| PERI_MS_PPU_FX34_MS_ATT0 | 0x400210B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX34_MS_ATT1 | 0x400210B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX34_MS_ATT2 | 0x400210B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX34_MS_ATT3 | 0x400210BC | FULL | Master attributes 3 |

## 23.52 PPU_FX 35

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX35_SL_ADDR | 0x400210C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX35_SL_SIZE | 0x400210C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX35_SL_ATT0 | 0x400210D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX35_SL_ATT1 | 0x400210D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX35_SL_ATT2 | 0x400210D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX35_SL_ATT3 | 0x400210DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX35_MS_ADDR | 0x400210E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX35_MS_SIZE | 0x400210E4 | FULL | Master region, size |
| PERI_MS_PPU_FX35_MS_ATT0 | 0x400210F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX35_MS_ATT1 | 0x400210F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX35_MS_ATT2 | 0x400210F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX35_MS_ATT3 | 0x400210FC | FULL | Master attributes 3 |

## 23.53 PPU_FX 36

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX36_SL_ADDR | 0x40021100 | FULL | Slave region, base address |
| PERI_MS_PPU_FX36_SL_SIZE | 0x40021104 | FULL | Slave region, size |
| PERI_MS_PPU_FX36_SL_ATT0 | 0x40021110 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX36_SL_ATT1 | 0x40021114 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX36_SL_ATT2 | 0x40021118 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX36_SL_ATT3 | 0x4002111C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX36_MS_ADDR | 0x40021120 | FULL | Master region, base address |
| PERI_MS_PPU_FX36_MS_SIZE | 0x40021124 | FULL | Master region, size |
| PERI_MS_PPU_FX36_MS_ATT0 | 0x40021130 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX36_MS_ATT1 | 0x40021134 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX36_MS_ATT2 | 0x40021138 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX36_MS_ATT3 | 0x4002113C | FULL | Master attributes 3 |

## 23.54 PPU_FX 37

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX37_SL_ADDR | 0x40021140 | FULL | Slave region, base address |
| PERI_MS_PPU_FX37_SL_SIZE | 0x40021144 | FULL | Slave region, size |
| PERI_MS_PPU_FX37_SL_ATT0 | 0x40021150 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX37_SL_ATT1 | 0x40021154 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX37_SL_ATT2 | 0x40021158 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX37_SL_ATT3 | 0x4002115C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX37_MS_ADDR | 0x40021160 | FULL | Master region, base address |
| PERI_MS_PPU_FX37_MS_SIZE | 0x40021164 | FULL | Master region, size |
| PERI_MS_PPU_FX37_MS_ATT0 | 0x40021170 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX37_MS_ATT1 | 0x40021174 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX37_MS_ATT2 | 0x40021178 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX37_MS_ATT3 | 0x4002117C | FULL | Master attributes 3 |

## 23.55 PPU_FX 38

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX38_SL_ADDR | 0x40021180 | FULL | Slave region, base address |
| PERI_MS_PPU_FX38_SL_SIZE | 0x40021184 | FULL | Slave region, size |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX38_SL_ATT0 | 0x40021190 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX38_SL_ATT1 | 0x40021194 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX38_SL_ATT2 | 0x40021198 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX38_SL_ATT3 | 0x4002119C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX38_MS_ADDR | 0x400211A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX38_MS_SIZE | 0x400211A4 | FULL | Master region, size |
| PERI_MS_PPU_FX38_MS_ATT0 | 0x400211B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX38_MS_ATT1 | 0x400211B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX38_MS_ATT2 | 0x400211B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX38_MS_ATT3 | 0x400211BC | FULL | Master attributes 3 |

## 23.56 PPU_FX 39

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX39_SL_ADDR | 0x400211C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX39_SL_SIZE | 0x400211C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX39_SL_ATT0 | 0x400211D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX39_SL_ATT1 | 0x400211D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX39_SL_ATT2 | 0x400211D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX39_SL_ATT3 | 0x400211DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX39_MS_ADDR | 0x400211E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX39_MS_SIZE | 0x400211E4 | FULL | Master region, size |
| PERI_MS_PPU_FX39_MS_ATT0 | 0x400211F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX39_MS_ATT1 | 0x400211F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX39_MS_ATT2 | 0x400211F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX39_MS_ATT3 | 0x400211FC | FULL | Master attributes 3 |

## 23.57 PPU_FX 40

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX40_SL_ADDR | 0x40021200 | PRIVILEGE - WRITE | Slave region, base address |
| PERI_MS_PPU_FX40_SL_SIZE | 0x40021204 | PRIVILEGE - WRITE | Slave region, size |
| PERI_MS_PPU_FX40_SL_ATT0 | 0x40021210 | PRIVILEGE - WRITE | Slave attributes 0 |
| PERI_MS_PPU_FX40_SL_ATT1 | 0x40021214 | PRIVILEGE - WRITE | Slave attributes 1 |
| PERI_MS_PPU_FX40_SL_ATT2 | 0x40021218 | PRIVILEGE - WRITE | Slave attributes 2 |
| PERI_MS_PPU_FX40_SL_ATT3 | 0x4002121C | PRIVILEGE - WRITE | Slave attributes 3 |
| PERI_MS_PPU_FX40_MS_ADDR | 0x40021220 | PRIVILEGE - WRITE | Master region, base address |
| PERI_MS_PPU_FX40_MS_SIZE | 0x40021224 | PRIVILEGE - WRITE | Master region, size |
| PERI_MS_PPU_FX40_MS_ATT0 | 0x40021230 | PRIVILEGE - WRITE | Master attributes 0 |
| PERI_MS_PPU_FX40_MS_ATT1 | 0x40021234 | PRIVILEGE - WRITE | Master attributes 1 |
| PERI_MS_PPU_FX40_MS_ATT2 | 0x40021238 | PRIVILEGE - WRITE | Master attributes 2 |
| PERI_MS_PPU_FX40_MS_ATT3 | 0x4002123C | PRIVILEGE - WRITE | Master attributes 3 |

## 23.58 PPU_FX 41

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX41_SL_ADDR | 0x40021240 | PRIVILEGE - WRITE | Slave region, base address |
| PERI_MS_PPU_FX41_SL_SIZE | 0x40021244 | PRIVILEGE - WRITE | Slave region, size |
| PERI_MS_PPU_FX41_SL_ATT0 | 0x40021250 | PRIVILEGE - WRITE | Slave attributes 0 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX41_SL_ATT1 | 0x40021254 | PRIVILEGE - WRITE | Slave attributes 1 |
| PERI_MS_PPU_FX41_SL_ATT2 | 0x40021258 | PRIVILEGE - WRITE | Slave attributes 2 |
| PERI_MS_PPU_FX41_SL_ATT3 | 0x4002125C | PRIVILEGE - WRITE | Slave attributes 3 |
| PERI_MS_PPU_FX41_MS_ADDR | 0x40021260 | PRIVILEGE - WRITE | Master region, base address |
| PERI_MS_PPU_FX41_MS_SIZE | 0x40021264 | PRIVILEGE - WRITE | Master region, size |
| PERI_MS_PPU_FX41_MS_ATT0 | 0x40021270 | PRIVILEGE - WRITE | Master attributes 0 |
| PERI_MS_PPU_FX41_MS_ATT1 | 0x40021274 | PRIVILEGE - WRITE | Master attributes 1 |
| PERI_MS_PPU_FX41_MS_ATT2 | 0x40021278 | PRIVILEGE - WRITE | Master attributes 2 |
| PERI_MS_PPU_FX41_MS_ATT3 | 0x4002127C | PRIVILEGE - WRITE | Master attributes 3 |

## 23.59 PPU_FX 42

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX42_SL_ADDR | 0x40021280 | PRIVILEGE - WRITE | Slave region, base address |
| PERI_MS_PPU_FX42_SL_SIZE | 0x40021284 | PRIVILEGE - WRITE | Slave region, size |
| PERI_MS_PPU_FX42_SL_ATT0 | 0x40021290 | PRIVILEGE - WRITE | Slave attributes 0 |
| PERI_MS_PPU_FX42_SL_ATT1 | 0x40021294 | PRIVILEGE - WRITE | Slave attributes 1 |
| PERI_MS_PPU_FX42_SL_ATT2 | 0x40021298 | PRIVILEGE - WRITE | Slave attributes 2 |
| PERI_MS_PPU_FX42_SL_ATT3 | 0x4002129C | PRIVILEGE - WRITE | Slave attributes 3 |
| PERI_MS_PPU_FX42_MS_ADDR | 0x400212A0 | PRIVILEGE - WRITE | Master region, base address |
| PERI_MS_PPU_FX42_MS_SIZE | 0x400212A4 | PRIVILEGE - WRITE | Master region, size |
| PERI_MS_PPU_FX42_MS_ATT0 | 0x400212B0 | PRIVILEGE - WRITE | Master attributes 0 |
| PERI_MS_PPU_FX42_MS_ATT1 | 0x400212B4 | PRIVILEGE - WRITE | Master attributes 1 |
| PERI_MS_PPU_FX42_MS_ATT2 | 0x400212B8 | PRIVILEGE - WRITE | Master attributes 2 |
| PERI_MS_PPU_FX42_MS_ATT3 | 0x400212BC | PRIVILEGE - WRITE | Master attributes 3 |

## 23.60 PPU_FX 43

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX43_SL_ADDR | 0x400212C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX43_SL_SIZE | 0x400212C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX43_SL_ATT0 | 0x400212D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX43_SL_ATT1 | 0x400212D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX43_SL_ATT2 | 0x400212D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX43_SL_ATT3 | 0x400212DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX43_MS_ADDR | 0x400212E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX43_MS_SIZE | 0x400212E4 | FULL | Master region, size |
| PERI_MS_PPU_FX43_MS_ATT0 | 0x400212F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX43_MS_ATT1 | 0x400212F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX43_MS_ATT2 | 0x400212F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX43_MS_ATT3 | 0x400212FC | FULL | Master attributes 3 |

## 23.61 PPU_FX 44

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX44_SL_ADDR | 0x40021300 | FULL | Slave region, base address |
| PERI_MS_PPU_FX44_SL_SIZE | 0x40021304 | FULL | Slave region, size |
| PERI_MS_PPU_FX44_SL_ATT0 | 0x40021310 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX44_SL_ATT1 | 0x40021314 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX44_SL_ATT2 | 0x40021318 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX44_SL_ATT3 | 0x4002131C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX44_MS_ADDR | 0x40021320 | FULL | Master region, base address |
| PERI_MS_PPU_FX44_MS_SIZE | 0x40021324 | FULL | Master region, size |
| PERI_MS_PPU_FX44_MS_ATT0 | 0x40021330 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX44_MS_ATT1 | 0x40021334 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX44_MS_ATT2 | 0x40021338 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX44_MS_ATT3 | 0x4002133C | FULL | Master attributes 3 |

## 23.62 PPU_FX 45

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX45_SL_ADDR | 0x40021340 | FULL | Slave region, base address |
| PERI_MS_PPU_FX45_SL_SIZE | 0x40021344 | FULL | Slave region, size |
| PERI_MS_PPU_FX45_SL_ATT0 | 0x40021350 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX45_SL_ATT1 | 0x40021354 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX45_SL_ATT2 | 0x40021358 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX45_SL_ATT3 | 0x4002135C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX45_MS_ADDR | 0x40021360 | FULL | Master region, base address |
| PERI_MS_PPU_FX45_MS_SIZE | 0x40021364 | FULL | Master region, size |
| PERI_MS_PPU_FX45_MS_ATT0 | 0x40021370 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX45_MS_ATT1 | 0x40021374 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX45_MS_ATT2 | 0x40021378 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX45_MS_ATT3 | 0x4002137C | FULL | Master attributes 3 |

## 23.63 PPU_FX 46

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX46_SL_ADDR | 0x40021380 | FULL | Slave region, base address |
| PERI_MS_PPU_FX46_SL_SIZE | 0x40021384 | FULL | Slave region, size |
| PERI_MS_PPU_FX46_SL_ATT0 | 0x40021390 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX46_SL_ATT1 | 0x40021394 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX46_SL_ATT2 | 0x40021398 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX46_SL_ATT3 | 0x4002139C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX46_MS_ADDR | 0x400213A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX46_MS_SIZE | 0x400213A4 | FULL | Master region, size |
| PERI_MS_PPU_FX46_MS_ATT0 | 0x400213B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX46_MS_ATT1 | 0x400213B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX46_MS_ATT2 | 0x400213B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX46_MS_ATT3 | 0x400213BC | FULL | Master attributes 3 |

## 23.64 PPU_FX 47

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX47_SL_ADDR | 0x400213C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX47_SL_SIZE | 0x400213C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX47_SL_ATT0 | 0x400213D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX47_SL_ATT1 | 0x400213D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX47_SL_ATT2 | 0x400213D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX47_SL_ATT3 | 0x400213DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX47_MS_ADDR | 0x400213E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX47_MS_SIZE | 0x400213E4 | FULL | Master region, size |
| PERI_MS_PPU_FX47_MS_ATT0 | 0x400213F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX47_MS_ATT1 | 0x400213F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX47_MS_ATT2 | 0x400213F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX47_MS_ATT3 | 0x400213FC | FULL | Master attributes 3 |

## 23.65 PPU_FX 48

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX48_SL_ADDR | 0x40021400 | FULL | Slave region, base address |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX48_SL_SIZE | 0x40021404 | FULL | Slave region, size |
| PERI_MS_PPU_FX48_SL_ATT0 | 0x40021410 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX48_SL_ATT1 | 0x40021414 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX48_SL_ATT2 | 0x40021418 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX48_SL_ATT3 | 0x4002141C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX48_MS_ADDR | 0x40021420 | FULL | Master region, base address |
| PERI_MS_PPU_FX48_MS_SIZE | 0x40021424 | FULL | Master region, size |
| PERI_MS_PPU_FX48_MS_ATT0 | 0x40021430 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX48_MS_ATT1 | 0x40021434 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX48_MS_ATT2 | 0x40021438 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX48_MS_ATT3 | 0x4002143C | FULL | Master attributes 3 |

## 23.66 PPU_FX 49

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX49_SL_ADDR | 0x40021440 | FULL | Slave region, base address |
| PERI_MS_PPU_FX49_SL_SIZE | 0x40021444 | FULL | Slave region, size |
| PERI_MS_PPU_FX49_SL_ATT0 | 0x40021450 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX49_SL_ATT1 | 0x40021454 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX49_SL_ATT2 | 0x40021458 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX49_SL_ATT3 | 0x4002145C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX49_MS_ADDR | 0x40021460 | FULL | Master region, base address |
| PERI_MS_PPU_FX49_MS_SIZE | 0x40021464 | FULL | Master region, size |
| PERI_MS_PPU_FX49_MS_ATT0 | 0x40021470 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX49_MS_ATT1 | 0x40021474 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX49_MS_ATT2 | 0x40021478 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX49_MS_ATT3 | 0x4002147C | FULL | Master attributes 3 |

## 23.67 PPU_FX 50

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX50_SL_ADDR | 0x40021480 | FULL | Slave region, base address |
| PERI_MS_PPU_FX50_SL_SIZE | 0x40021484 | FULL | Slave region, size |
| PERI_MS_PPU_FX50_SL_ATT0 | 0x40021490 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX50_SL_ATT1 | 0x40021494 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX50_SL_ATT2 | 0x40021498 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX50_SL_ATT3 | 0x4002149C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX50_MS_ADDR | 0x400214A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX50_MS_SIZE | 0x400214A4 | FULL | Master region, size |
| PERI_MS_PPU_FX50_MS_ATT0 | 0x400214B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX50_MS_ATT1 | 0x400214B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX50_MS_ATT2 | 0x400214B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX50_MS_ATT3 | 0x400214BC | FULL | Master attributes 3 |

## 23.68 PPU_FX 51

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX51_SL_ADDR | 0x400214C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX51_SL_SIZE | 0x400214C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX51_SL_ATT0 | 0x400214D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX51_SL_ATT1 | 0x400214D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX51_SL_ATT2 | 0x400214D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX51_SL_ATT3 | 0x400214DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX51_MS_ADDR | 0x400214E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX51_MS_SIZE | 0x400214E4 | FULL | Master region, size |
| PERI_MS_PPU_FX51_MS_ATT0 | 0x400214F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX51_MS_ATT1 | 0x400214F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX51_MS_ATT2 | 0x400214F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX51_MS_ATT3 | 0x400214FC | FULL | Master attributes 3 |

## 23.69 PPU_FX 52

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX52_SL_ADDR | 0x40021500 | FULL | Slave region, base address |
| PERI_MS_PPU_FX52_SL_SIZE | 0x40021504 | FULL | Slave region, size |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX52_SL_ATT0 | 0x40021510 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX52_SL_ATT1 | 0x40021514 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX52_SL_ATT2 | 0x40021518 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX52_SL_ATT3 | 0x4002151C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX52_MS_ADDR | 0x40021520 | FULL | Master region, base address |
| PERI_MS_PPU_FX52_MS_SIZE | 0x40021524 | FULL | Master region, size |
| PERI_MS_PPU_FX52_MS_ATT0 | 0x40021530 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX52_MS_ATT1 | 0x40021534 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX52_MS_ATT2 | 0x40021538 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX52_MS_ATT3 | 0x4002153C | FULL | Master attributes 3 |

## 23.70 PPU_FX 53

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX53_SL_ADDR | 0x40021540 | FULL | Slave region, base address |
| PERI_MS_PPU_FX53_SL_SIZE | 0x40021544 | FULL | Slave region, size |
| PERI_MS_PPU_FX53_SL_ATT0 | 0x40021550 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX53_SL_ATT1 | 0x40021554 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX53_SL_ATT2 | 0x40021558 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX53_SL_ATT3 | 0x4002155C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX53_MS_ADDR | 0x40021560 | FULL | Master region, base address |
| PERI_MS_PPU_FX53_MS_SIZE | 0x40021564 | FULL | Master region, size |
| PERI_MS_PPU_FX53_MS_ATT0 | 0x40021570 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX53_MS_ATT1 | 0x40021574 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX53_MS_ATT2 | 0x40021578 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX53_MS_ATT3 | 0x4002157C | FULL | Master attributes 3 |

## 23.71 PPU_FX 54

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX54_SL_ADDR | 0x40021580 | FULL | Slave region, base address |
| PERI_MS_PPU_FX54_SL_SIZE | 0x40021584 | FULL | Slave region, size |
| PERI_MS_PPU_FX54_SL_ATT0 | 0x40021590 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX54_SL_ATT1 | 0x40021594 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX54_SL_ATT2 | 0x40021598 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX54_SL_ATT3 | 0x4002159C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX54_MS_ADDR | 0x400215A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX54_MS_SIZE | 0x400215A4 | FULL | Master region, size |
| PERI_MS_PPU_FX54_MS_ATT0 | 0x400215B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX54_MS_ATT1 | 0x400215B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX54_MS_ATT2 | 0x400215B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX54_MS_ATT3 | 0x400215BC | FULL | Master attributes 3 |

## 23.72 PPU_FX 55

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX55_SL_ADDR | 0x400215C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX55_SL_SIZE | 0x400215C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX55_SL_ATT0 | 0x400215D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX55_SL_ATT1 | 0x400215D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX55_SL_ATT2 | 0x400215D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX55_SL_ATT3 | 0x400215DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX55_MS_ADDR | 0x400215E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX55_MS_SIZE | 0x400215E4 | FULL | Master region, size |
| PERI_MS_PPU_FX55_MS_ATT0 | 0x400215F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX55_MS_ATT1 | 0x400215F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX55_MS_ATT2 | 0x400215F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX55_MS_ATT3 | 0x400215FC | FULL | Master attributes 3 |

## 23.73 PPU_FX 56

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX56_SL_ADDR | 0x40021600 | FULL | Slave region, base address |
| PERI_MS_PPU_FX56_SL_SIZE | 0x40021604 | FULL | Slave region, size |
| PERI_MS_PPU_FX56_SL_ATT0 | 0x40021610 | FULL | Slave attributes 0 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX56_SL_ATT1 | 0x40021614 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX56_SL_ATT2 | 0x40021618 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX56_SL_ATT3 | 0x4002161C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX56_MS_ADDR | 0x40021620 | FULL | Master region, base address |
| PERI_MS_PPU_FX56_MS_SIZE | 0x40021624 | FULL | Master region, size |
| PERI_MS_PPU_FX56_MS_ATT0 | 0x40021630 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX56_MS_ATT1 | 0x40021634 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX56_MS_ATT2 | 0x40021638 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX56_MS_ATT3 | 0x4002163C | FULL | Master attributes 3 |

## 23.74 PPU_FX 57

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX57_SL_ADDR | 0x40021640 | FULL | Slave region, base address |
| PERI_MS_PPU_FX57_SL_SIZE | 0x40021644 | FULL | Slave region, size |
| PERI_MS_PPU_FX57_SL_ATT0 | 0x40021650 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX57_SL_ATT1 | 0x40021654 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX57_SL_ATT2 | 0x40021658 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX57_SL_ATT3 | 0x4002165C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX57_MS_ADDR | 0x40021660 | FULL | Master region, base address |
| PERI_MS_PPU_FX57_MS_SIZE | 0x40021664 | FULL | Master region, size |
| PERI_MS_PPU_FX57_MS_ATT0 | 0x40021670 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX57_MS_ATT1 | 0x40021674 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX57_MS_ATT2 | 0x40021678 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX57_MS_ATT3 | 0x4002167C | FULL | Master attributes 3 |

## 23.75 PPU_FX 58

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX58_SL_ADDR | 0x40021680 | FULL | Slave region, base address |
| PERI_MS_PPU_FX58_SL_SIZE | 0x40021684 | FULL | Slave region, size |
| PERI_MS_PPU_FX58_SL_ATT0 | 0x40021690 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX58_SL_ATT1 | 0x40021694 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX58_SL_ATT2 | 0x40021698 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX58_SL_ATT3 | 0x4002169C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX58_MS_ADDR | 0x400216A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX58_MS_SIZE | 0x400216A4 | FULL | Master region, size |
| PERI_MS_PPU_FX58_MS_ATT0 | 0x400216B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX58_MS_ATT1 | 0x400216B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX58_MS_ATT2 | 0x400216B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX58_MS_ATT3 | 0x400216BC | FULL | Master attributes 3 |

## 23.76 PPU_FX 59

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX59_SL_ADDR | 0x400216C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX59_SL_SIZE | 0x400216C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX59_SL_ATT0 | 0x400216D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX59_SL_ATT1 | 0x400216D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX59_SL_ATT2 | 0x400216D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX59_SL_ATT3 | 0x400216DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX59_MS_ADDR | 0x400216E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX59_MS_SIZE | 0x400216E4 | FULL | Master region, size |
| PERI_MS_PPU_FX59_MS_ATT0 | 0x400216F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX59_MS_ATT1 | 0x400216F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX59_MS_ATT2 | 0x400216F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX59_MS_ATT3 | 0x400216FC | FULL | Master attributes 3 |

## 23.77 PPU_FX 60

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX60_SL_ADDR | 0x40021700 | FULL | Slave region, base address |
| PERI_MS_PPU_FX60_SL_SIZE | 0x40021704 | FULL | Slave region, size |
| PERI_MS_PPU_FX60_SL_ATT0 | 0x40021710 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX60_SL_ATT1 | 0x40021714 | FULL | Slave attributes 1 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX60_SL_ATT2 | 0x40021718 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX60_SL_ATT3 | 0x4002171C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX60_MS_ADDR | 0x40021720 | FULL | Master region, base address |
| PERI_MS_PPU_FX60_MS_SIZE | 0x40021724 | FULL | Master region, size |
| PERI_MS_PPU_FX60_MS_ATT0 | 0x40021730 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX60_MS_ATT1 | 0x40021734 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX60_MS_ATT2 | 0x40021738 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX60_MS_ATT3 | 0x4002173C | FULL | Master attributes 3 |

## 23.78 PPU_FX 61

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX61_SL_ADDR | 0x40021740 | FULL | Slave region, base address |
| PERI_MS_PPU_FX61_SL_SIZE | 0x40021744 | FULL | Slave region, size |
| PERI_MS_PPU_FX61_SL_ATT0 | 0x40021750 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX61_SL_ATT1 | 0x40021754 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX61_SL_ATT2 | 0x40021758 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX61_SL_ATT3 | 0x4002175C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX61_MS_ADDR | 0x40021760 | FULL | Master region, base address |
| PERI_MS_PPU_FX61_MS_SIZE | 0x40021764 | FULL | Master region, size |
| PERI_MS_PPU_FX61_MS_ATT0 | 0x40021770 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX61_MS_ATT1 | 0x40021774 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX61_MS_ATT2 | 0x40021778 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX61_MS_ATT3 | 0x4002177C | FULL | Master attributes 3 |

## 23.79 PPU_FX 62

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX62_SL_ADDR | 0x40021780 | FULL | Slave region, base address |
| PERI_MS_PPU_FX62_SL_SIZE | 0x40021784 | FULL | Slave region, size |
| PERI_MS_PPU_FX62_SL_ATT0 | 0x40021790 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX62_SL_ATT1 | 0x40021794 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX62_SL_ATT2 | 0x40021798 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX62_SL_ATT3 | 0x4002179C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX62_MS_ADDR | 0x400217A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX62_MS_SIZE | 0x400217A4 | FULL | Master region, size |
| PERI_MS_PPU_FX62_MS_ATT0 | 0x400217B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX62_MS_ATT1 | 0x400217B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX62_MS_ATT2 | 0x400217B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX62_MS_ATT3 | 0x400217BC | FULL | Master attributes 3 |

## 23.80 PPU_FX 63

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX63_SL_ADDR | 0x400217C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX63_SL_SIZE | 0x400217C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX63_SL_ATT0 | 0x400217D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX63_SL_ATT1 | 0x400217D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX63_SL_ATT2 | 0x400217D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX63_SL_ATT3 | 0x400217DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX63_MS_ADDR | 0x400217E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX63_MS_SIZE | 0x400217E4 | FULL | Master region, size |
| PERI_MS_PPU_FX63_MS_ATT0 | 0x400217F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX63_MS_ATT1 | 0x400217F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX63_MS_ATT2 | 0x400217F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX63_MS_ATT3 | 0x400217FC | FULL | Master attributes 3 |

## 23.81 PPU_FX 64

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX64_SL_ADDR | 0x40021800 | FULL | Slave region, base address |
| PERI_MS_PPU_FX64_SL_SIZE | 0x40021804 | FULL | Slave region, size |
| PERI_MS_PPU_FX64_SL_ATT0 | 0x40021810 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX64_SL_ATT1 | 0x40021814 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX64_SL_ATT2 | 0x40021818 | FULL | Slave attributes 2 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX64_SL_ATT3 | 0x4002181C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX64_MS_ADDR | 0x40021820 | FULL | Master region, base address |
| PERI_MS_PPU_FX64_MS_SIZE | 0x40021824 | FULL | Master region, size |
| PERI_MS_PPU_FX64_MS_ATT0 | 0x40021830 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX64_MS_ATT1 | 0x40021834 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX64_MS_ATT2 | 0x40021838 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX64_MS_ATT3 | 0x4002183C | FULL | Master attributes 3 |

## 23.82 PPU_FX 65

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX65_SL_ADDR | 0x40021840 | FULL | Slave region, base address |
| PERI_MS_PPU_FX65_SL_SIZE | 0x40021844 | FULL | Slave region, size |
| PERI_MS_PPU_FX65_SL_ATT0 | 0x40021850 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX65_SL_ATT1 | 0x40021854 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX65_SL_ATT2 | 0x40021858 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX65_SL_ATT3 | 0x4002185C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX65_MS_ADDR | 0x40021860 | FULL | Master region, base address |
| PERI_MS_PPU_FX65_MS_SIZE | 0x40021864 | FULL | Master region, size |
| PERI_MS_PPU_FX65_MS_ATT0 | 0x40021870 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX65_MS_ATT1 | 0x40021874 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX65_MS_ATT2 | 0x40021878 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX65_MS_ATT3 | 0x4002187C | FULL | Master attributes 3 |

## 23.83 PPU_FX 66

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX66_SL_ADDR | 0x40021880 | READ | Slave region, base address |
| PERI_MS_PPU_FX66_SL_SIZE | 0x40021884 | READ | Slave region, size |
| PERI_MS_PPU_FX66_SL_ATT0 | 0x40021890 | READ | Slave attributes 0 |
| PERI_MS_PPU_FX66_SL_ATT1 | 0x40021894 | READ | Slave attributes 1 |
| PERI_MS_PPU_FX66_SL_ATT2 | 0x40021898 | READ | Slave attributes 2 |
| PERI_MS_PPU_FX66_SL_ATT3 | 0x4002189C | READ | Slave attributes 3 |
| PERI_MS_PPU_FX66_MS_ADDR | 0x400218A0 | READ | Master region, base address |
| PERI_MS_PPU_FX66_MS_SIZE | 0x400218A4 | READ | Master region, size |
| PERI_MS_PPU_FX66_MS_ATT0 | 0x400218B0 | READ | Master attributes 0 |
| PERI_MS_PPU_FX66_MS_ATT1 | 0x400218B4 | READ | Master attributes 1 |
| PERI_MS_PPU_FX66_MS_ATT2 | 0x400218B8 | READ | Master attributes 2 |
| PERI_MS_PPU_FX66_MS_ATT3 | 0x400218BC | READ | Master attributes 3 |

## 23.84 PPU_FX 67

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX67_SL_ADDR | 0x400218C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX67_SL_SIZE | 0x400218C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX67_SL_ATT0 | 0x400218D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX67_SL_ATT1 | 0x400218D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX67_SL_ATT2 | 0x400218D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX67_SL_ATT3 | 0x400218DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX67_MS_ADDR | 0x400218E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX67_MS_SIZE | 0x400218E4 | FULL | Master region, size |
| PERI_MS_PPU_FX67_MS_ATT0 | 0x400218F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX67_MS_ATT1 | 0x400218F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX67_MS_ATT2 | 0x400218F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX67_MS_ATT3 | 0x400218FC | FULL | Master attributes 3 |

## 23.85 PPU_FX 68

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX68_SL_ADDR | 0x40021900 | FULL | Slave region, base address |
| PERI_MS_PPU_FX68_SL_SIZE | 0x40021904 | FULL | Slave region, size |
| PERI_MS_PPU_FX68_SL_ATT0 | 0x40021910 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX68_SL_ATT1 | 0x40021914 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX68_SL_ATT2 | 0x40021918 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX68_SL_ATT3 | 0x4002191C | FULL | Slave attributes 3 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX68_MS_ADDR | 0x40021920 | FULL | Master region, base address |
| PERI_MS_PPU_FX68_MS_SIZE | 0x40021924 | FULL | Master region, size |
| PERI_MS_PPU_FX68_MS_ATT0 | 0x40021930 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX68_MS_ATT1 | 0x40021934 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX68_MS_ATT2 | 0x40021938 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX68_MS_ATT3 | 0x4002193C | FULL | Master attributes 3 |

## 23.86 PPU_FX 69

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX69_SL_ADDR | 0x40021940 | FULL | Slave region, base address |
| PERI_MS_PPU_FX69_SL_SIZE | 0x40021944 | FULL | Slave region, size |
| PERI_MS_PPU_FX69_SL_ATT0 | 0x40021950 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX69_SL_ATT1 | 0x40021954 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX69_SL_ATT2 | 0x40021958 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX69_SL_ATT3 | 0x4002195C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX69_MS_ADDR | 0x40021960 | FULL | Master region, base address |
| PERI_MS_PPU_FX69_MS_SIZE | 0x40021964 | FULL | Master region, size |
| PERI_MS_PPU_FX69_MS_ATT0 | 0x40021970 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX69_MS_ATT1 | 0x40021974 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX69_MS_ATT2 | 0x40021978 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX69_MS_ATT3 | 0x4002197C | FULL | Master attributes 3 |

## 23.87 PPU_FX 70

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX70_SL_ADDR | 0x40021980 | FULL | Slave region, base address |
| PERI_MS_PPU_FX70_SL_SIZE | 0x40021984 | FULL | Slave region, size |
| PERI_MS_PPU_FX70_SL_ATT0 | 0x40021990 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX70_SL_ATT1 | 0x40021994 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX70_SL_ATT2 | 0x40021998 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX70_SL_ATT3 | 0x4002199C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX70_MS_ADDR | 0x400219A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX70_MS_SIZE | 0x400219A4 | FULL | Master region, size |
| PERI_MS_PPU_FX70_MS_ATT0 | 0x400219B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX70_MS_ATT1 | 0x400219B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX70_MS_ATT2 | 0x400219B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX70_MS_ATT3 | 0x400219BC | FULL | Master attributes 3 |

## 23.88 PPU_FX 71

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX71_SL_ADDR | 0x400219C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX71_SL_SIZE | 0x400219C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX71_SL_ATT0 | 0x400219D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX71_SL_ATT1 | 0x400219D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX71_SL_ATT2 | 0x400219D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX71_SL_ATT3 | 0x400219DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX71_MS_ADDR | 0x400219E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX71_MS_SIZE | 0x400219E4 | FULL | Master region, size |
| PERI_MS_PPU_FX71_MS_ATT0 | 0x400219F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX71_MS_ATT1 | 0x400219F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX71_MS_ATT2 | 0x400219F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX71_MS_ATT3 | 0x400219FC | FULL | Master attributes 3 |

## 23.89 PPU_FX 72

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX72_SL_ADDR | 0x40021A00 | FULL | Slave region, base address |
| PERI_MS_PPU_FX72_SL_SIZE | 0x40021A04 | FULL | Slave region, size |
| PERI_MS_PPU_FX72_SL_ATT0 | 0x40021A10 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX72_SL_ATT1 | 0x40021A14 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX72_SL_ATT2 | 0x40021A18 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX72_SL_ATT3 | 0x40021A1C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX72_MS_ADDR | 0x40021A20 | FULL | Master region, base address |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX72_MS_SIZE | 0x40021A24 | FULL | Master region, size |
| PERI_MS_PPU_FX72_MS_ATT0 | 0x40021A30 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX72_MS_ATT1 | 0x40021A34 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX72_MS_ATT2 | 0x40021A38 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX72_MS_ATT3 | 0x40021A3C | FULL | Master attributes 3 |

## 23.90 PPU_FX 73

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX73_SL_ADDR | 0x40021A40 | FULL | Slave region, base address |
| PERI_MS_PPU_FX73_SL_SIZE | 0x40021A44 | FULL | Slave region, size |
| PERI_MS_PPU_FX73_SL_ATT0 | 0x40021A50 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX73_SL_ATT1 | 0x40021A54 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX73_SL_ATT2 | 0x40021A58 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX73_SL_ATT3 | 0x40021A5C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX73_MS_ADDR | 0x40021A60 | FULL | Master region, base address |
| PERI_MS_PPU_FX73_MS_SIZE | 0x40021A64 | FULL | Master region, size |
| PERI_MS_PPU_FX73_MS_ATT0 | 0x40021A70 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX73_MS_ATT1 | 0x40021A74 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX73_MS_ATT2 | 0x40021A78 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX73_MS_ATT3 | 0x40021A7C | FULL | Master attributes 3 |

## 23.91 PPU_FX 74

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX74_SL_ADDR | 0x40021A80 | FULL | Slave region, base address |
| PERI_MS_PPU_FX74_SL_SIZE | 0x40021A84 | FULL | Slave region, size |
| PERI_MS_PPU_FX74_SL_ATT0 | 0x40021A90 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX74_SL_ATT1 | 0x40021A94 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX74_SL_ATT2 | 0x40021A98 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX74_SL_ATT3 | 0x40021A9C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX74_MS_ADDR | 0x40021AA0 | FULL | Master region, base address |
| PERI_MS_PPU_FX74_MS_SIZE | 0x40021AA4 | FULL | Master region, size |
| PERI_MS_PPU_FX74_MS_ATT0 | 0x40021AB0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX74_MS_ATT1 | 0x40021AB4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX74_MS_ATT2 | 0x40021AB8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX74_MS_ATT3 | 0x40021ABC | FULL | Master attributes 3 |

## 23.92 PPU_FX 75

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX75_SL_ADDR | 0x40021AC0 | READ | Slave region, base address |
| PERI_MS_PPU_FX75_SL_SIZE | 0x40021AC4 | READ | Slave region, size |
| PERI_MS_PPU_FX75_SL_ATT0 | 0x40021AD0 | READ | Slave attributes 0 |
| PERI_MS_PPU_FX75_SL_ATT1 | 0x40021AD4 | READ | Slave attributes 1 |
| PERI_MS_PPU_FX75_SL_ATT2 | 0x40021AD8 | READ | Slave attributes 2 |
| PERI_MS_PPU_FX75_SL_ATT3 | 0x40021ADC | READ | Slave attributes 3 |
| PERI_MS_PPU_FX75_MS_ADDR | 0x40021AE0 | READ | Master region, base address |
| PERI_MS_PPU_FX75_MS_SIZE | 0x40021AE4 | READ | Master region, size |
| PERI_MS_PPU_FX75_MS_ATT0 | 0x40021AF0 | READ | Master attributes 0 |
| PERI_MS_PPU_FX75_MS_ATT1 | 0x40021AF4 | READ | Master attributes 1 |
| PERI_MS_PPU_FX75_MS_ATT2 | 0x40021AF8 | READ | Master attributes 2 |
| PERI_MS_PPU_FX75_MS_ATT3 | 0x40021AFC | READ | Master attributes 3 |

## 23.93 PPU_FX 76

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX76_SL_ADDR | 0x40021B00 | FULL | Slave region, base address |
| PERI_MS_PPU_FX76_SL_SIZE | 0x40021B04 | FULL | Slave region, size |
| PERI_MS_PPU_FX76_SL_ATT0 | 0x40021B10 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX76_SL_ATT1 | 0x40021B14 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX76_SL_ATT2 | 0x40021B18 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX76_SL_ATT3 | 0x40021B1C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX76_MS_ADDR | 0x40021B20 | FULL | Master region, base address |
| PERI_MS_PPU_FX76_MS_SIZE | 0x40021B24 | FULL | Master region, size |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX76_MS_ATT0 | 0x40021B30 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX76_MS_ATT1 | 0x40021B34 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX76_MS_ATT2 | 0x40021B38 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX76_MS_ATT3 | 0x40021B3C | FULL | Master attributes 3 |

## 23.94 PPU_FX 77

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX77_SL_ADDR | 0x40021B40 | FULL | Slave region, base address |
| PERI_MS_PPU_FX77_SL_SIZE | 0x40021B44 | FULL | Slave region, size |
| PERI_MS_PPU_FX77_SL_ATT0 | 0x40021B50 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX77_SL_ATT1 | 0x40021B54 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX77_SL_ATT2 | 0x40021B58 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX77_SL_ATT3 | 0x40021B5C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX77_MS_ADDR | 0x40021B60 | FULL | Master region, base address |
| PERI_MS_PPU_FX77_MS_SIZE | 0x40021B64 | FULL | Master region, size |
| PERI_MS_PPU_FX77_MS_ATT0 | 0x40021B70 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX77_MS_ATT1 | 0x40021B74 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX77_MS_ATT2 | 0x40021B78 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX77_MS_ATT3 | 0x40021B7C | FULL | Master attributes 3 |

## 23.95 PPU_FX 78

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX78_SL_ADDR | 0x40021B80 | FULL | Slave region, base address |
| PERI_MS_PPU_FX78_SL_SIZE | 0x40021B84 | FULL | Slave region, size |
| PERI_MS_PPU_FX78_SL_ATT0 | 0x40021B90 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX78_SL_ATT1 | 0x40021B94 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX78_SL_ATT2 | 0x40021B98 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX78_SL_ATT3 | 0x40021B9C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX78_MS_ADDR | 0x40021BA0 | FULL | Master region, base address |
| PERI_MS_PPU_FX78_MS_SIZE | 0x40021BA4 | FULL | Master region, size |
| PERI_MS_PPU_FX78_MS_ATT0 | 0x40021BB0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX78_MS_ATT1 | 0x40021BB4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX78_MS_ATT2 | 0x40021BB8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX78_MS_ATT3 | 0x40021BBC | FULL | Master attributes 3 |

## 23.96 PPU_FX 79

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX79_SL_ADDR | 0x40021BC0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX79_SL_SIZE | 0x40021BC4 | FULL | Slave region, size |
| PERI_MS_PPU_FX79_SL_ATT0 | 0x40021BD0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX79_SL_ATT1 | 0x40021BD4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX79_SL_ATT2 | 0x40021BD8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX79_SL_ATT3 | 0x40021BDC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX79_MS_ADDR | 0x40021BE0 | FULL | Master region, base address |
| PERI_MS_PPU_FX79_MS_SIZE | 0x40021BE4 | FULL | Master region, size |
| PERI_MS_PPU_FX79_MS_ATT0 | 0x40021BF0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX79_MS_ATT1 | 0x40021BF4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX79_MS_ATT2 | 0x40021BF8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX79_MS_ATT3 | 0x40021BFC | FULL | Master attributes 3 |

## 23.97 PPU_FX 80

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX80_SL_ADDR | 0x40021C00 | READ | Slave region, base address |
| PERI_MS_PPU_FX80_SL_SIZE | 0x40021C04 | READ | Slave region, size |
| PERI_MS_PPU_FX80_SL_ATT0 | 0x40021C10 | READ | Slave attributes 0 |
| PERI_MS_PPU_FX80_SL_ATT1 | 0x40021C14 | READ | Slave attributes 1 |
| PERI_MS_PPU_FX80_SL_ATT2 | 0x40021C18 | READ | Slave attributes 2 |
| PERI_MS_PPU_FX80_SL_ATT3 | 0x40021C1C | READ | Slave attributes 3 |
| PERI_MS_PPU_FX80_MS_ADDR | 0x40021C20 | READ | Master region, base address |
| PERI_MS_PPU_FX80_MS_SIZE | 0x40021C24 | READ | Master region, size |
| PERI_MS_PPU_FX80_MS_ATT0 | 0x40021C30 | READ | Master attributes 0 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX80_MS_ATT1 | 0x40021C34 | READ | Master attributes 1 |
| PERI_MS_PPU_FX80_MS_ATT2 | 0x40021C38 | READ | Master attributes 2 |
| PERI_MS_PPU_FX80_MS_ATT3 | 0x40021C3C | READ | Master attributes 3 |

## 23.98 PPU_FX 81

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX81_SL_ADDR | 0x40021C40 | FULL | Slave region, base address |
| PERI_MS_PPU_FX81_SL_SIZE | 0x40021C44 | FULL | Slave region, size |
| PERI_MS_PPU_FX81_SL_ATT0 | 0x40021C50 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX81_SL_ATT1 | 0x40021C54 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX81_SL_ATT2 | 0x40021C58 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX81_SL_ATT3 | 0x40021C5C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX81_MS_ADDR | 0x40021C60 | FULL | Master region, base address |
| PERI_MS_PPU_FX81_MS_SIZE | 0x40021C64 | FULL | Master region, size |
| PERI_MS_PPU_FX81_MS_ATT0 | 0x40021C70 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX81_MS_ATT1 | 0x40021C74 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX81_MS_ATT2 | 0x40021C78 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX81_MS_ATT3 | 0x40021C7C | FULL | Master attributes 3 |

## 23.99 PPU_FX 82

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX82_SL_ADDR | 0x40021C80 | FULL | Slave region, base address |
| PERI_MS_PPU_FX82_SL_SIZE | 0x40021C84 | FULL | Slave region, size |
| PERI_MS_PPU_FX82_SL_ATT0 | 0x40021C90 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX82_SL_ATT1 | 0x40021C94 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX82_SL_ATT2 | 0x40021C98 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX82_SL_ATT3 | 0x40021C9C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX82_MS_ADDR | 0x40021CA0 | FULL | Master region, base address |
| PERI_MS_PPU_FX82_MS_SIZE | 0x40021CA4 | FULL | Master region, size |
| PERI_MS_PPU_FX82_MS_ATT0 | 0x40021CB0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX82_MS_ATT1 | 0x40021CB4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX82_MS_ATT2 | 0x40021CB8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX82_MS_ATT3 | 0x40021CBC | FULL | Master attributes 3 |

## 23.100 PPU_FX 83

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX83_SL_ADDR | 0x40021CC0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX83_SL_SIZE | 0x40021CC4 | FULL | Slave region, size |
| PERI_MS_PPU_FX83_SL_ATT0 | 0x40021CD0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX83_SL_ATT1 | 0x40021CD4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX83_SL_ATT2 | 0x40021CD8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX83_SL_ATT3 | 0x40021CDC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX83_MS_ADDR | 0x40021CE0 | FULL | Master region, base address |
| PERI_MS_PPU_FX83_MS_SIZE | 0x40021CE4 | FULL | Master region, size |
| PERI_MS_PPU_FX83_MS_ATT0 | 0x40021CF0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX83_MS_ATT1 | 0x40021CF4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX83_MS_ATT2 | 0x40021CF8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX83_MS_ATT3 | 0x40021CFC | FULL | Master attributes 3 |

## 23.101 PPU_FX 84

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX84_SL_ADDR | 0x40021D00 | FULL | Slave region, base address |
| PERI_MS_PPU_FX84_SL_SIZE | 0x40021D04 | FULL | Slave region, size |
| PERI_MS_PPU_FX84_SL_ATT0 | 0x40021D10 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX84_SL_ATT1 | 0x40021D14 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX84_SL_ATT2 | 0x40021D18 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX84_SL_ATT3 | 0x40021D1C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX84_MS_ADDR | 0x40021D20 | FULL | Master region, base address |
| PERI_MS_PPU_FX84_MS_SIZE | 0x40021D24 | FULL | Master region, size |
| PERI_MS_PPU_FX84_MS_ATT0 | 0x40021D30 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX84_MS_ATT1 | 0x40021D34 | FULL | Master attributes 1 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX84_MS_ATT2 | 0x40021D38 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX84_MS_ATT3 | 0x40021D3C | FULL | Master attributes 3 |

## 23.102 PPU_FX 85

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX85_SL_ADDR | 0x40021D40 | FULL | Slave region, base address |
| PERI_MS_PPU_FX85_SL_SIZE | 0x40021D44 | FULL | Slave region, size |
| PERI_MS_PPU_FX85_SL_ATT0 | 0x40021D50 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX85_SL_ATT1 | 0x40021D54 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX85_SL_ATT2 | 0x40021D58 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX85_SL_ATT3 | 0x40021D5C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX85_MS_ADDR | 0x40021D60 | FULL | Master region, base address |
| PERI_MS_PPU_FX85_MS_SIZE | 0x40021D64 | FULL | Master region, size |
| PERI_MS_PPU_FX85_MS_ATT0 | 0x40021D70 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX85_MS_ATT1 | 0x40021D74 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX85_MS_ATT2 | 0x40021D78 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX85_MS_ATT3 | 0x40021D7C | FULL | Master attributes 3 |

## 23.103 PPU_FX 86

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX86_SL_ADDR | 0x40021D80 | FULL | Slave region, base address |
| PERI_MS_PPU_FX86_SL_SIZE | 0x40021D84 | FULL | Slave region, size |
| PERI_MS_PPU_FX86_SL_ATT0 | 0x40021D90 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX86_SL_ATT1 | 0x40021D94 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX86_SL_ATT2 | 0x40021D98 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX86_SL_ATT3 | 0x40021D9C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX86_MS_ADDR | 0x40021DA0 | FULL | Master region, base address |
| PERI_MS_PPU_FX86_MS_SIZE | 0x40021DA4 | FULL | Master region, size |
| PERI_MS_PPU_FX86_MS_ATT0 | 0x40021DB0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX86_MS_ATT1 | 0x40021DB4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX86_MS_ATT2 | 0x40021DB8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX86_MS_ATT3 | 0x40021DBC | FULL | Master attributes 3 |

## 23.104 PPU_FX 87

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX87_SL_ADDR | 0x40021DC0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX87_SL_SIZE | 0x40021DC4 | FULL | Slave region, size |
| PERI_MS_PPU_FX87_SL_ATT0 | 0x40021DD0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX87_SL_ATT1 | 0x40021DD4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX87_SL_ATT2 | 0x40021DD8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX87_SL_ATT3 | 0x40021DDC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX87_MS_ADDR | 0x40021DE0 | FULL | Master region, base address |
| PERI_MS_PPU_FX87_MS_SIZE | 0x40021DE4 | FULL | Master region, size |
| PERI_MS_PPU_FX87_MS_ATT0 | 0x40021DF0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX87_MS_ATT1 | 0x40021DF4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX87_MS_ATT2 | 0x40021DF8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX87_MS_ATT3 | 0x40021DFC | FULL | Master attributes 3 |

## 23.105 PPU_FX 88

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX88_SL_ADDR | 0x40021E00 | FULL | Slave region, base address |
| PERI_MS_PPU_FX88_SL_SIZE | 0x40021E04 | FULL | Slave region, size |
| PERI_MS_PPU_FX88_SL_ATT0 | 0x40021E10 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX88_SL_ATT1 | 0x40021E14 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX88_SL_ATT2 | 0x40021E18 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX88_SL_ATT3 | 0x40021E1C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX88_MS_ADDR | 0x40021E20 | FULL | Master region, base address |
| PERI_MS_PPU_FX88_MS_SIZE | 0x40021E24 | FULL | Master region, size |
| PERI_MS_PPU_FX88_MS_ATT0 | 0x40021E30 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX88_MS_ATT1 | 0x40021E34 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX88_MS_ATT2 | 0x40021E38 | FULL | Master attributes 2 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX88_MS_ATT3 | 0x40021E3C | FULL | Master attributes 3 |

## 23.106 PPU_FX 89

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX89_SL_ADDR | 0x40021E40 | FULL | Slave region, base address |
| PERI_MS_PPU_FX89_SL_SIZE | 0x40021E44 | FULL | Slave region, size |
| PERI_MS_PPU_FX89_SL_ATT0 | 0x40021E50 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX89_SL_ATT1 | 0x40021E54 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX89_SL_ATT2 | 0x40021E58 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX89_SL_ATT3 | 0x40021E5C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX89_MS_ADDR | 0x40021E60 | FULL | Master region, base address |
| PERI_MS_PPU_FX89_MS_SIZE | 0x40021E64 | FULL | Master region, size |
| PERI_MS_PPU_FX89_MS_ATT0 | 0x40021E70 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX89_MS_ATT1 | 0x40021E74 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX89_MS_ATT2 | 0x40021E78 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX89_MS_ATT3 | 0x40021E7C | FULL | Master attributes 3 |

## 23.107 PPU_FX 90

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX90_SL_ADDR | 0x40021E80 | FULL | Slave region, base address |
| PERI_MS_PPU_FX90_SL_SIZE | 0x40021E84 | FULL | Slave region, size |
| PERI_MS_PPU_FX90_SL_ATT0 | 0x40021E90 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX90_SL_ATT1 | 0x40021E94 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX90_SL_ATT2 | 0x40021E98 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX90_SL_ATT3 | 0x40021E9C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX90_MS_ADDR | 0x40021EA0 | FULL | Master region, base address |
| PERI_MS_PPU_FX90_MS_SIZE | 0x40021EA4 | FULL | Master region, size |
| PERI_MS_PPU_FX90_MS_ATT0 | 0x40021EB0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX90_MS_ATT1 | 0x40021EB4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX90_MS_ATT2 | 0x40021EB8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX90_MS_ATT3 | 0x40021EBC | FULL | Master attributes 3 |

## 23.108 PPU_FX 91

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX91_SL_ADDR | 0x40021EC0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX91_SL_SIZE | 0x40021EC4 | FULL | Slave region, size |
| PERI_MS_PPU_FX91_SL_ATT0 | 0x40021ED0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX91_SL_ATT1 | 0x40021ED4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX91_SL_ATT2 | 0x40021ED8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX91_SL_ATT3 | 0x40021EDC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX91_MS_ADDR | 0x40021EE0 | FULL | Master region, base address |
| PERI_MS_PPU_FX91_MS_SIZE | 0x40021EE4 | FULL | Master region, size |
| PERI_MS_PPU_FX91_MS_ATT0 | 0x40021EF0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX91_MS_ATT1 | 0x40021EF4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX91_MS_ATT2 | 0x40021EF8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX91_MS_ATT3 | 0x40021EFC | FULL | Master attributes 3 |

## 23.109 PPU_FX 92

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX92_SL_ADDR | 0x40021F00 | FULL | Slave region, base address |
| PERI_MS_PPU_FX92_SL_SIZE | 0x40021F04 | FULL | Slave region, size |
| PERI_MS_PPU_FX92_SL_ATT0 | 0x40021F10 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX92_SL_ATT1 | 0x40021F14 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX92_SL_ATT2 | 0x40021F18 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX92_SL_ATT3 | 0x40021F1C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX92_MS_ADDR | 0x40021F20 | FULL | Master region, base address |
| PERI_MS_PPU_FX92_MS_SIZE | 0x40021F24 | FULL | Master region, size |
| PERI_MS_PPU_FX92_MS_ATT0 | 0x40021F30 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX92_MS_ATT1 | 0x40021F34 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX92_MS_ATT2 | 0x40021F38 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX92_MS_ATT3 | 0x40021F3C | FULL | Master attributes 3 |

## 23.110 PPU_FX 93

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX93_SL_ADDR | 0x40021F40 | FULL | Slave region, base address |
| PERI_MS_PPU_FX93_SL_SIZE | 0x40021F44 | FULL | Slave region, size |
| PERI_MS_PPU_FX93_SL_ATT0 | 0x40021F50 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX93_SL_ATT1 | 0x40021F54 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX93_SL_ATT2 | 0x40021F58 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX93_SL_ATT3 | 0x40021F5C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX93_MS_ADDR | 0x40021F60 | FULL | Master region, base address |
| PERI_MS_PPU_FX93_MS_SIZE | 0x40021F64 | FULL | Master region, size |
| PERI_MS_PPU_FX93_MS_ATT0 | 0x40021F70 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX93_MS_ATT1 | 0x40021F74 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX93_MS_ATT2 | 0x40021F78 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX93_MS_ATT3 | 0x40021F7C | FULL | Master attributes 3 |

## 23.111 PPU_FX 94

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX94_SL_ADDR | 0x40021F80 | FULL | Slave region, base address |
| PERI_MS_PPU_FX94_SL_SIZE | 0x40021F84 | FULL | Slave region, size |
| PERI_MS_PPU_FX94_SL_ATT0 | 0x40021F90 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX94_SL_ATT1 | 0x40021F94 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX94_SL_ATT2 | 0x40021F98 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX94_SL_ATT3 | 0x40021F9C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX94_MS_ADDR | 0x40021FA0 | FULL | Master region, base address |
| PERI_MS_PPU_FX94_MS_SIZE | 0x40021FA4 | FULL | Master region, size |
| PERI_MS_PPU_FX94_MS_ATT0 | 0x40021FB0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX94_MS_ATT1 | 0x40021FB4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX94_MS_ATT2 | 0x40021FB8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX94_MS_ATT3 | 0x40021FBC | FULL | Master attributes 3 |

## 23.112 PPU_FX 95

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX95_SL_ADDR | 0x40021FC0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX95_SL_SIZE | 0x40021FC4 | FULL | Slave region, size |
| PERI_MS_PPU_FX95_SL_ATT0 | 0x40021FD0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX95_SL_ATT1 | 0x40021FD4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX95_SL_ATT2 | 0x40021FD8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX95_SL_ATT3 | 0x40021FDC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX95_MS_ADDR | 0x40021FE0 | FULL | Master region, base address |
| PERI_MS_PPU_FX95_MS_SIZE | 0x40021FE4 | FULL | Master region, size |
| PERI_MS_PPU_FX95_MS_ATT0 | 0x40021FF0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX95_MS_ATT1 | 0x40021FF4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX95_MS_ATT2 | 0x40021FF8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX95_MS_ATT3 | 0x40021FFC | FULL | Master attributes 3 |

## 23.113 PPU_FX 96

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX96_SL_ADDR | 0x40022000 | FULL | Slave region, base address |
| PERI_MS_PPU_FX96_SL_SIZE | 0x40022004 | FULL | Slave region, size |
| PERI_MS_PPU_FX96_SL_ATT0 | 0x40022010 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX96_SL_ATT1 | 0x40022014 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX96_SL_ATT2 | 0x40022018 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX96_SL_ATT3 | 0x4002201C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX96_MS_ADDR | 0x40022020 | FULL | Master region, base address |
| PERI_MS_PPU_FX96_MS_SIZE | 0x40022024 | FULL | Master region, size |
| PERI_MS_PPU_FX96_MS_ATT0 | 0x40022030 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX96_MS_ATT1 | 0x40022034 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX96_MS_ATT2 | 0x40022038 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX96_MS_ATT3 | 0x4002203C | FULL | Master attributes 3 |

## 23.114 PPU_FX 97

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX97_SL_ADDR | 0x40022040 | FULL | Slave region, base address |
| PERI_MS_PPU_FX97_SL_SIZE | 0x40022044 | FULL | Slave region, size |
| PERI_MS_PPU_FX97_SL_ATT0 | 0x40022050 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX97_SL_ATT1 | 0x40022054 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX97_SL_ATT2 | 0x40022058 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX97_SL_ATT3 | 0x4002205C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX97_MS_ADDR | 0x40022060 | FULL | Master region, base address |
| PERI_MS_PPU_FX97_MS_SIZE | 0x40022064 | FULL | Master region, size |
| PERI_MS_PPU_FX97_MS_ATT0 | 0x40022070 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX97_MS_ATT1 | 0x40022074 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX97_MS_ATT2 | 0x40022078 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX97_MS_ATT3 | 0x4002207C | FULL | Master attributes 3 |

## 23.115 PPU_FX 98

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX98_SL_ADDR | 0x40022080 | FULL | Slave region, base address |
| PERI_MS_PPU_FX98_SL_SIZE | 0x40022084 | FULL | Slave region, size |
| PERI_MS_PPU_FX98_SL_ATT0 | 0x40022090 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX98_SL_ATT1 | 0x40022094 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX98_SL_ATT2 | 0x40022098 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX98_SL_ATT3 | 0x4002209C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX98_MS_ADDR | 0x400220A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX98_MS_SIZE | 0x400220A4 | FULL | Master region, size |
| PERI_MS_PPU_FX98_MS_ATT0 | 0x400220B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX98_MS_ATT1 | 0x400220B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX98_MS_ATT2 | 0x400220B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX98_MS_ATT3 | 0x400220BC | FULL | Master attributes 3 |

## 23.116 PPU_FX 99

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX99_SL_ADDR | 0x400220C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX99_SL_SIZE | 0x400220C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX99_SL_ATT0 | 0x400220D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX99_SL_ATT1 | 0x400220D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX99_SL_ATT2 | 0x400220D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX99_SL_ATT3 | 0x400220DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX99_MS_ADDR | 0x400220E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX99_MS_SIZE | 0x400220E4 | FULL | Master region, size |
| PERI_MS_PPU_FX99_MS_ATT0 | 0x400220F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX99_MS_ATT1 | 0x400220F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX99_MS_ATT2 | 0x400220F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX99_MS_ATT3 | 0x400220FC | FULL | Master attributes 3 |

## 23.117 PPU_FX 100

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX100_SL_ADDR | 0x40022100 | FULL | Slave region, base address |
| PERI_MS_PPU_FX100_SL_SIZE | 0x40022104 | FULL | Slave region, size |
| PERI_MS_PPU_FX100_SL_ATT0 | 0x40022110 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX100_SL_ATT1 | 0x40022114 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX100_SL_ATT2 | 0x40022118 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX100_SL_ATT3 | 0x4002211C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX100_MS_ADDR | 0x40022120 | FULL | Master region, base address |
| PERI_MS_PPU_FX100_MS_SIZE | 0x40022124 | FULL | Master region, size |
| PERI_MS_PPU_FX100_MS_ATT0 | 0x40022130 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX100_MS_ATT1 | 0x40022134 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX100_MS_ATT2 | 0x40022138 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX100_MS_ATT3 | 0x4002213C | FULL | Master attributes 3 |

## 23.118 PPU_FX 101

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX101_SL_ADDR | 0x40022140 | FULL | Slave region, base address |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX101_SL_SIZE | 0x40022144 | FULL | Slave region, size |
| PERI_MS_PPU_FX101_SL_ATT0 | 0x40022150 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX101_SL_ATT1 | 0x40022154 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX101_SL_ATT2 | 0x40022158 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX101_SL_ATT3 | 0x4002215C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX101_MS_ADDR | 0x40022160 | FULL | Master region, base address |
| PERI_MS_PPU_FX101_MS_SIZE | 0x40022164 | FULL | Master region, size |
| PERI_MS_PPU_FX101_MS_ATT0 | 0x40022170 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX101_MS_ATT1 | 0x40022174 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX101_MS_ATT2 | 0x40022178 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX101_MS_ATT3 | 0x4002217C | FULL | Master attributes 3 |

## 23.119 PPU_FX 102

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX102_SL_ADDR | 0x40022180 | FULL | Slave region, base address |
| PERI_MS_PPU_FX102_SL_SIZE | 0x40022184 | FULL | Slave region, size |
| PERI_MS_PPU_FX102_SL_ATT0 | 0x40022190 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX102_SL_ATT1 | 0x40022194 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX102_SL_ATT2 | 0x40022198 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX102_SL_ATT3 | 0x4002219C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX102_MS_ADDR | 0x400221A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX102_MS_SIZE | 0x400221A4 | FULL | Master region, size |
| PERI_MS_PPU_FX102_MS_ATT0 | 0x400221B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX102_MS_ATT1 | 0x400221B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX102_MS_ATT2 | 0x400221B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX102_MS_ATT3 | 0x400221BC | FULL | Master attributes 3 |

## 23.120 PPU_FX 103

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX103_SL_ADDR | 0x400221C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX103_SL_SIZE | 0x400221C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX103_SL_ATT0 | 0x400221D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX103_SL_ATT1 | 0x400221D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX103_SL_ATT2 | 0x400221D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX103_SL_ATT3 | 0x400221DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX103_MS_ADDR | 0x400221E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX103_MS_SIZE | 0x400221E4 | FULL | Master region, size |
| PERI_MS_PPU_FX103_MS_ATT0 | 0x400221F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX103_MS_ATT1 | 0x400221F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX103_MS_ATT2 | 0x400221F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX103_MS_ATT3 | 0x400221FC | FULL | Master attributes 3 |

## 23.121 PPU_FX 104

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX104_SL_ADDR | 0x40022200 | FULL | Slave region, base address |
| PERI_MS_PPU_FX104_SL_SIZE | 0x40022204 | FULL | Slave region, size |
| PERI_MS_PPU_FX104_SL_ATT0 | 0x40022210 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX104_SL_ATT1 | 0x40022214 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX104_SL_ATT2 | 0x40022218 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX104_SL_ATT3 | 0x4002221C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX104_MS_ADDR | 0x40022220 | FULL | Master region, base address |
| PERI_MS_PPU_FX104_MS_SIZE | 0x40022224 | FULL | Master region, size |
| PERI_MS_PPU_FX104_MS_ATT0 | 0x40022230 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX104_MS_ATT1 | 0x40022234 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX104_MS_ATT2 | 0x40022238 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX104_MS_ATT3 | 0x4002223C | FULL | Master attributes 3 |

## 23.122 PPU_FX 105

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX105_SL_ADDR | 0x40022240 | FULL | Slave region, base address |
| PERI_MS_PPU_FX105_SL_SIZE | 0x40022244 | FULL | Slave region, size |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX105_SL_ATT0 | 0x40022250 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX105_SL_ATT1 | 0x40022254 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX105_SL_ATT2 | 0x40022258 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX105_SL_ATT3 | 0x4002225C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX105_MS_ADDR | 0x40022260 | FULL | Master region, base address |
| PERI_MS_PPU_FX105_MS_SIZE | 0x40022264 | FULL | Master region, size |
| PERI_MS_PPU_FX105_MS_ATT0 | 0x40022270 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX105_MS_ATT1 | 0x40022274 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX105_MS_ATT2 | 0x40022278 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX105_MS_ATT3 | 0x4002227C | FULL | Master attributes 3 |

## 23.123 PPU_FX 106

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX106_SL_ADDR | 0x40022280 | FULL | Slave region, base address |
| PERI_MS_PPU_FX106_SL_SIZE | 0x40022284 | FULL | Slave region, size |
| PERI_MS_PPU_FX106_SL_ATT0 | 0x40022290 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX106_SL_ATT1 | 0x40022294 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX106_SL_ATT2 | 0x40022298 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX106_SL_ATT3 | 0x4002229C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX106_MS_ADDR | 0x400222A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX106_MS_SIZE | 0x400222A4 | FULL | Master region, size |
| PERI_MS_PPU_FX106_MS_ATT0 | 0x400222B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX106_MS_ATT1 | 0x400222B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX106_MS_ATT2 | 0x400222B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX106_MS_ATT3 | 0x400222BC | FULL | Master attributes 3 |

## 23.124 PPU_FX 107

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX107_SL_ADDR | 0x400222C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX107_SL_SIZE | 0x400222C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX107_SL_ATT0 | 0x400222D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX107_SL_ATT1 | 0x400222D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX107_SL_ATT2 | 0x400222D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX107_SL_ATT3 | 0x400222DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX107_MS_ADDR | 0x400222E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX107_MS_SIZE | 0x400222E4 | FULL | Master region, size |
| PERI_MS_PPU_FX107_MS_ATT0 | 0x400222F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX107_MS_ATT1 | 0x400222F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX107_MS_ATT2 | 0x400222F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX107_MS_ATT3 | 0x400222FC | FULL | Master attributes 3 |

## 23.125 PPU_FX 108

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX108_SL_ADDR | 0x40022300 | FULL | Slave region, base address |
| PERI_MS_PPU_FX108_SL_SIZE | 0x40022304 | FULL | Slave region, size |
| PERI_MS_PPU_FX108_SL_ATT0 | 0x40022310 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX108_SL_ATT1 | 0x40022314 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX108_SL_ATT2 | 0x40022318 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX108_SL_ATT3 | 0x4002231C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX108_MS_ADDR | 0x40022320 | FULL | Master region, base address |
| PERI_MS_PPU_FX108_MS_SIZE | 0x40022324 | FULL | Master region, size |
| PERI_MS_PPU_FX108_MS_ATT0 | 0x40022330 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX108_MS_ATT1 | 0x40022334 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX108_MS_ATT2 | 0x40022338 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX108_MS_ATT3 | 0x4002233C | FULL | Master attributes 3 |

## 23.126 PPU_FX 109

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX109_SL_ADDR | 0x40022340 | FULL | Slave region, base address |
| PERI_MS_PPU_FX109_SL_SIZE | 0x40022344 | FULL | Slave region, size |
| PERI_MS_PPU_FX109_SL_ATT0 | 0x40022350 | FULL | Slave attributes 0 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX109_SL_ATT1 | 0x40022354 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX109_SL_ATT2 | 0x40022358 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX109_SL_ATT3 | 0x4002235C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX109_MS_ADDR | 0x40022360 | FULL | Master region, base address |
| PERI_MS_PPU_FX109_MS_SIZE | 0x40022364 | FULL | Master region, size |
| PERI_MS_PPU_FX109_MS_ATT0 | 0x40022370 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX109_MS_ATT1 | 0x40022374 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX109_MS_ATT2 | 0x40022378 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX109_MS_ATT3 | 0x4002237C | FULL | Master attributes 3 |

## 23.127 PPU_FX 110

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX110_SL_ADDR | 0x40022380 | FULL | Slave region, base address |
| PERI_MS_PPU_FX110_SL_SIZE | 0x40022384 | FULL | Slave region, size |
| PERI_MS_PPU_FX110_SL_ATT0 | 0x40022390 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX110_SL_ATT1 | 0x40022394 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX110_SL_ATT2 | 0x40022398 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX110_SL_ATT3 | 0x4002239C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX110_MS_ADDR | 0x400223A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX110_MS_SIZE | 0x400223A4 | FULL | Master region, size |
| PERI_MS_PPU_FX110_MS_ATT0 | 0x400223B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX110_MS_ATT1 | 0x400223B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX110_MS_ATT2 | 0x400223B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX110_MS_ATT3 | 0x400223BC | FULL | Master attributes 3 |

## 23.128 PPU_FX 111

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX111_SL_ADDR | 0x400223C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX111_SL_SIZE | 0x400223C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX111_SL_ATT0 | 0x400223D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX111_SL_ATT1 | 0x400223D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX111_SL_ATT2 | 0x400223D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX111_SL_ATT3 | 0x400223DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX111_MS_ADDR | 0x400223E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX111_MS_SIZE | 0x400223E4 | FULL | Master region, size |
| PERI_MS_PPU_FX111_MS_ATT0 | 0x400223F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX111_MS_ATT1 | 0x400223F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX111_MS_ATT2 | 0x400223F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX111_MS_ATT3 | 0x400223FC | FULL | Master attributes 3 |

## 23.129 PPU_FX 112

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX112_SL_ADDR | 0x40022400 | FULL | Slave region, base address |
| PERI_MS_PPU_FX112_SL_SIZE | 0x40022404 | FULL | Slave region, size |
| PERI_MS_PPU_FX112_SL_ATT0 | 0x40022410 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX112_SL_ATT1 | 0x40022414 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX112_SL_ATT2 | 0x40022418 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX112_SL_ATT3 | 0x4002241C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX112_MS_ADDR | 0x40022420 | FULL | Master region, base address |
| PERI_MS_PPU_FX112_MS_SIZE | 0x40022424 | FULL | Master region, size |
| PERI_MS_PPU_FX112_MS_ATT0 | 0x40022430 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX112_MS_ATT1 | 0x40022434 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX112_MS_ATT2 | 0x40022438 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX112_MS_ATT3 | 0x4002243C | FULL | Master attributes 3 |

## 23.130 PPU_FX 113

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX113_SL_ADDR | 0x40022440 | FULL | Slave region, base address |
| PERI_MS_PPU_FX113_SL_SIZE | 0x40022444 | FULL | Slave region, size |
| PERI_MS_PPU_FX113_SL_ATT0 | 0x40022450 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX113_SL_ATT1 | 0x40022454 | FULL | Slave attributes 1 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX113_SL_ATT2 | 0x40022458 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX113_SL_ATT3 | 0x4002245C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX113_MS_ADDR | 0x40022460 | FULL | Master region, base address |
| PERI_MS_PPU_FX113_MS_SIZE | 0x40022464 | FULL | Master region, size |
| PERI_MS_PPU_FX113_MS_ATT0 | 0x40022470 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX113_MS_ATT1 | 0x40022474 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX113_MS_ATT2 | 0x40022478 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX113_MS_ATT3 | 0x4002247C | FULL | Master attributes 3 |

## 23.131 PPU_FX 114

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX114_SL_ADDR | 0x40022480 | FULL | Slave region, base address |
| PERI_MS_PPU_FX114_SL_SIZE | 0x40022484 | FULL | Slave region, size |
| PERI_MS_PPU_FX114_SL_ATT0 | 0x40022490 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX114_SL_ATT1 | 0x40022494 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX114_SL_ATT2 | 0x40022498 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX114_SL_ATT3 | 0x4002249C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX114_MS_ADDR | 0x400224A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX114_MS_SIZE | 0x400224A4 | FULL | Master region, size |
| PERI_MS_PPU_FX114_MS_ATT0 | 0x400224B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX114_MS_ATT1 | 0x400224B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX114_MS_ATT2 | 0x400224B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX114_MS_ATT3 | 0x400224BC | FULL | Master attributes 3 |

## 23.132 PPU_FX 115

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX115_SL_ADDR | 0x400224C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX115_SL_SIZE | 0x400224C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX115_SL_ATT0 | 0x400224D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX115_SL_ATT1 | 0x400224D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX115_SL_ATT2 | 0x400224D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX115_SL_ATT3 | 0x400224DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX115_MS_ADDR | 0x400224E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX115_MS_SIZE | 0x400224E4 | FULL | Master region, size |
| PERI_MS_PPU_FX115_MS_ATT0 | 0x400224F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX115_MS_ATT1 | 0x400224F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX115_MS_ATT2 | 0x400224F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX115_MS_ATT3 | 0x400224FC | FULL | Master attributes 3 |

## 23.133 PPU_FX 116

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX116_SL_ADDR | 0x40022500 | FULL | Slave region, base address |
| PERI_MS_PPU_FX116_SL_SIZE | 0x40022504 | FULL | Slave region, size |
| PERI_MS_PPU_FX116_SL_ATT0 | 0x40022510 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX116_SL_ATT1 | 0x40022514 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX116_SL_ATT2 | 0x40022518 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX116_SL_ATT3 | 0x4002251C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX116_MS_ADDR | 0x40022520 | FULL | Master region, base address |
| PERI_MS_PPU_FX116_MS_SIZE | 0x40022524 | FULL | Master region, size |
| PERI_MS_PPU_FX116_MS_ATT0 | 0x40022530 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX116_MS_ATT1 | 0x40022534 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX116_MS_ATT2 | 0x40022538 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX116_MS_ATT3 | 0x4002253C | FULL | Master attributes 3 |

## 23.134 PPU_FX 117

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX117_SL_ADDR | 0x40022540 | FULL | Slave region, base address |
| PERI_MS_PPU_FX117_SL_SIZE | 0x40022544 | FULL | Slave region, size |
| PERI_MS_PPU_FX117_SL_ATT0 | 0x40022550 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX117_SL_ATT1 | 0x40022554 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX117_SL_ATT2 | 0x40022558 | FULL | Slave attributes 2 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX117_SL_ATT3 | 0x4002255C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX117_MS_ADDR | 0x40022560 | FULL | Master region, base address |
| PERI_MS_PPU_FX117_MS_SIZE | 0x40022564 | FULL | Master region, size |
| PERI_MS_PPU_FX117_MS_ATT0 | 0x40022570 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX117_MS_ATT1 | 0x40022574 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX117_MS_ATT2 | 0x40022578 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX117_MS_ATT3 | 0x4002257C | FULL | Master attributes 3 |

## 23.135 PPU_FX 118

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX118_SL_ADDR | 0x40022580 | FULL | Slave region, base address |
| PERI_MS_PPU_FX118_SL_SIZE | 0x40022584 | FULL | Slave region, size |
| PERI_MS_PPU_FX118_SL_ATT0 | 0x40022590 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX118_SL_ATT1 | 0x40022594 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX118_SL_ATT2 | 0x40022598 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX118_SL_ATT3 | 0x4002259C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX118_MS_ADDR | 0x400225A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX118_MS_SIZE | 0x400225A4 | FULL | Master region, size |
| PERI_MS_PPU_FX118_MS_ATT0 | 0x400225B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX118_MS_ATT1 | 0x400225B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX118_MS_ATT2 | 0x400225B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX118_MS_ATT3 | 0x400225BC | FULL | Master attributes 3 |

## 23.136 PPU_FX 119

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX119_SL_ADDR | 0x400225C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX119_SL_SIZE | 0x400225C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX119_SL_ATT0 | 0x400225D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX119_SL_ATT1 | 0x400225D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX119_SL_ATT2 | 0x400225D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX119_SL_ATT3 | 0x400225DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX119_MS_ADDR | 0x400225E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX119_MS_SIZE | 0x400225E4 | FULL | Master region, size |
| PERI_MS_PPU_FX119_MS_ATT0 | 0x400225F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX119_MS_ATT1 | 0x400225F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX119_MS_ATT2 | 0x400225F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX119_MS_ATT3 | 0x400225FC | FULL | Master attributes 3 |

## 23.137 PPU_FX 120

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX120_SL_ADDR | 0x40022600 | FULL | Slave region, base address |
| PERI_MS_PPU_FX120_SL_SIZE | 0x40022604 | FULL | Slave region, size |
| PERI_MS_PPU_FX120_SL_ATT0 | 0x40022610 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX120_SL_ATT1 | 0x40022614 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX120_SL_ATT2 | 0x40022618 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX120_SL_ATT3 | 0x4002261C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX120_MS_ADDR | 0x40022620 | FULL | Master region, base address |
| PERI_MS_PPU_FX120_MS_SIZE | 0x40022624 | FULL | Master region, size |
| PERI_MS_PPU_FX120_MS_ATT0 | 0x40022630 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX120_MS_ATT1 | 0x40022634 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX120_MS_ATT2 | 0x40022638 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX120_MS_ATT3 | 0x4002263C | FULL | Master attributes 3 |

## 23.138 PPU_FX 121

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX121_SL_ADDR | 0x40022640 | FULL | Slave region, base address |
| PERI_MS_PPU_FX121_SL_SIZE | 0x40022644 | FULL | Slave region, size |
| PERI_MS_PPU_FX121_SL_ATT0 | 0x40022650 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX121_SL_ATT1 | 0x40022654 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX121_SL_ATT2 | 0x40022658 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX121_SL_ATT3 | 0x4002265C | FULL | Slave attributes 3 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX121_MS_ADDR | 0x40022660 | FULL | Master region, base address |
| PERI_MS_PPU_FX121_MS_SIZE | 0x40022664 | FULL | Master region, size |
| PERI_MS_PPU_FX121_MS_ATT0 | 0x40022670 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX121_MS_ATT1 | 0x40022674 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX121_MS_ATT2 | 0x40022678 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX121_MS_ATT3 | 0x4002267C | FULL | Master attributes 3 |

## 23.139 PPU_FX 122

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX122_SL_ADDR | 0x40022680 | FULL | Slave region, base address |
| PERI_MS_PPU_FX122_SL_SIZE | 0x40022684 | FULL | Slave region, size |
| PERI_MS_PPU_FX122_SL_ATT0 | 0x40022690 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX122_SL_ATT1 | 0x40022694 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX122_SL_ATT2 | 0x40022698 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX122_SL_ATT3 | 0x4002269C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX122_MS_ADDR | 0x400226A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX122_MS_SIZE | 0x400226A4 | FULL | Master region, size |
| PERI_MS_PPU_FX122_MS_ATT0 | 0x400226B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX122_MS_ATT1 | 0x400226B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX122_MS_ATT2 | 0x400226B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX122_MS_ATT3 | 0x400226BC | FULL | Master attributes 3 |

## 23.140 PPU_FX 123

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX123_SL_ADDR | 0x400226C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX123_SL_SIZE | 0x400226C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX123_SL_ATT0 | 0x400226D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX123_SL_ATT1 | 0x400226D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX123_SL_ATT2 | 0x400226D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX123_SL_ATT3 | 0x400226DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX123_MS_ADDR | 0x400226E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX123_MS_SIZE | 0x400226E4 | FULL | Master region, size |
| PERI_MS_PPU_FX123_MS_ATT0 | 0x400226F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX123_MS_ATT1 | 0x400226F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX123_MS_ATT2 | 0x400226F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX123_MS_ATT3 | 0x400226FC | FULL | Master attributes 3 |

## 23.141 PPU_FX 124

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX124_SL_ADDR | 0x40022700 | FULL | Slave region, base address |
| PERI_MS_PPU_FX124_SL_SIZE | 0x40022704 | FULL | Slave region, size |
| PERI_MS_PPU_FX124_SL_ATT0 | 0x40022710 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX124_SL_ATT1 | 0x40022714 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX124_SL_ATT2 | 0x40022718 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX124_SL_ATT3 | 0x4002271C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX124_MS_ADDR | 0x40022720 | FULL | Master region, base address |
| PERI_MS_PPU_FX124_MS_SIZE | 0x40022724 | FULL | Master region, size |
| PERI_MS_PPU_FX124_MS_ATT0 | 0x40022730 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX124_MS_ATT1 | 0x40022734 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX124_MS_ATT2 | 0x40022738 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX124_MS_ATT3 | 0x4002273C | FULL | Master attributes 3 |

## 23.142 PPU_FX 125

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX125_SL_ADDR | 0x40022740 | FULL | Slave region, base address |
| PERI_MS_PPU_FX125_SL_SIZE | 0x40022744 | FULL | Slave region, size |
| PERI_MS_PPU_FX125_SL_ATT0 | 0x40022750 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX125_SL_ATT1 | 0x40022754 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX125_SL_ATT2 | 0x40022758 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX125_SL_ATT3 | 0x4002275C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX125_MS_ADDR | 0x40022760 | FULL | Master region, base address |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX125_MS_SIZE | 0x40022764 | FULL | Master region, size |
| PERI_MS_PPU_FX125_MS_ATT0 | 0x40022770 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX125_MS_ATT1 | 0x40022774 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX125_MS_ATT2 | 0x40022778 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX125_MS_ATT3 | 0x4002277C | FULL | Master attributes 3 |

## 23.143 PPU_FX 126

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX126_SL_ADDR | 0x40022780 | FULL | Slave region, base address |
| PERI_MS_PPU_FX126_SL_SIZE | 0x40022784 | FULL | Slave region, size |
| PERI_MS_PPU_FX126_SL_ATT0 | 0x40022790 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX126_SL_ATT1 | 0x40022794 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX126_SL_ATT2 | 0x40022798 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX126_SL_ATT3 | 0x4002279C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX126_MS_ADDR | 0x400227A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX126_MS_SIZE | 0x400227A4 | FULL | Master region, size |
| PERI_MS_PPU_FX126_MS_ATT0 | 0x400227B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX126_MS_ATT1 | 0x400227B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX126_MS_ATT2 | 0x400227B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX126_MS_ATT3 | 0x400227BC | FULL | Master attributes 3 |

## 23.144 PPU_FX 127

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX127_SL_ADDR | 0x400227C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX127_SL_SIZE | 0x400227C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX127_SL_ATT0 | 0x400227D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX127_SL_ATT1 | 0x400227D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX127_SL_ATT2 | 0x400227D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX127_SL_ATT3 | 0x400227DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX127_MS_ADDR | 0x400227E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX127_MS_SIZE | 0x400227E4 | FULL | Master region, size |
| PERI_MS_PPU_FX127_MS_ATT0 | 0x400227F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX127_MS_ATT1 | 0x400227F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX127_MS_ATT2 | 0x400227F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX127_MS_ATT3 | 0x400227FC | FULL | Master attributes 3 |

## 23.145 PPU_FX 128

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX128_SL_ADDR | 0x40022800 | FULL | Slave region, base address |
| PERI_MS_PPU_FX128_SL_SIZE | 0x40022804 | FULL | Slave region, size |
| PERI_MS_PPU_FX128_SL_ATT0 | 0x40022810 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX128_SL_ATT1 | 0x40022814 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX128_SL_ATT2 | 0x40022818 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX128_SL_ATT3 | 0x4002281C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX128_MS_ADDR | 0x40022820 | FULL | Master region, base address |
| PERI_MS_PPU_FX128_MS_SIZE | 0x40022824 | FULL | Master region, size |
| PERI_MS_PPU_FX128_MS_ATT0 | 0x40022830 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX128_MS_ATT1 | 0x40022834 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX128_MS_ATT2 | 0x40022838 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX128_MS_ATT3 | 0x4002283C | FULL | Master attributes 3 |

## 23.146 PPU_FX 129

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX129_SL_ADDR | 0x40022840 | FULL | Slave region, base address |
| PERI_MS_PPU_FX129_SL_SIZE | 0x40022844 | FULL | Slave region, size |
| PERI_MS_PPU_FX129_SL_ATT0 | 0x40022850 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX129_SL_ATT1 | 0x40022854 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX129_SL_ATT2 | 0x40022858 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX129_SL_ATT3 | 0x4002285C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX129_MS_ADDR | 0x40022860 | FULL | Master region, base address |
| PERI_MS_PPU_FX129_MS_SIZE | 0x40022864 | FULL | Master region, size |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX129_MS_ATT0 | 0x40022870 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX129_MS_ATT1 | 0x40022874 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX129_MS_ATT2 | 0x40022878 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX129_MS_ATT3 | 0x4002287C | FULL | Master attributes 3 |

## 23.147 PPU_FX 130

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX130_SL_ADDR | 0x40022880 | FULL | Slave region, base address |
| PERI_MS_PPU_FX130_SL_SIZE | 0x40022884 | FULL | Slave region, size |
| PERI_MS_PPU_FX130_SL_ATT0 | 0x40022890 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX130_SL_ATT1 | 0x40022894 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX130_SL_ATT2 | 0x40022898 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX130_SL_ATT3 | 0x4002289C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX130_MS_ADDR | 0x400228A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX130_MS_SIZE | 0x400228A4 | FULL | Master region, size |
| PERI_MS_PPU_FX130_MS_ATT0 | 0x400228B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX130_MS_ATT1 | 0x400228B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX130_MS_ATT2 | 0x400228B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX130_MS_ATT3 | 0x400228BC | FULL | Master attributes 3 |

## 23.148 PPU_FX 131

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX131_SL_ADDR | 0x400228C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX131_SL_SIZE | 0x400228C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX131_SL_ATT0 | 0x400228D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX131_SL_ATT1 | 0x400228D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX131_SL_ATT2 | 0x400228D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX131_SL_ATT3 | 0x400228DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX131_MS_ADDR | 0x400228E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX131_MS_SIZE | 0x400228E4 | FULL | Master region, size |
| PERI_MS_PPU_FX131_MS_ATT0 | 0x400228F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX131_MS_ATT1 | 0x400228F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX131_MS_ATT2 | 0x400228F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX131_MS_ATT3 | 0x400228FC | FULL | Master attributes 3 |

## 23.149 PPU_FX 132

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX132_SL_ADDR | 0x40022900 | FULL | Slave region, base address |
| PERI_MS_PPU_FX132_SL_SIZE | 0x40022904 | FULL | Slave region, size |
| PERI_MS_PPU_FX132_SL_ATT0 | 0x40022910 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX132_SL_ATT1 | 0x40022914 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX132_SL_ATT2 | 0x40022918 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX132_SL_ATT3 | 0x4002291C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX132_MS_ADDR | 0x40022920 | FULL | Master region, base address |
| PERI_MS_PPU_FX132_MS_SIZE | 0x40022924 | FULL | Master region, size |
| PERI_MS_PPU_FX132_MS_ATT0 | 0x40022930 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX132_MS_ATT1 | 0x40022934 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX132_MS_ATT2 | 0x40022938 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX132_MS_ATT3 | 0x4002293C | FULL | Master attributes 3 |

## 23.150 PPU_FX 133

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX133_SL_ADDR | 0x40022940 | FULL | Slave region, base address |
| PERI_MS_PPU_FX133_SL_SIZE | 0x40022944 | FULL | Slave region, size |
| PERI_MS_PPU_FX133_SL_ATT0 | 0x40022950 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX133_SL_ATT1 | 0x40022954 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX133_SL_ATT2 | 0x40022958 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX133_SL_ATT3 | 0x4002295C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX133_MS_ADDR | 0x40022960 | FULL | Master region, base address |
| PERI_MS_PPU_FX133_MS_SIZE | 0x40022964 | FULL | Master region, size |
| PERI_MS_PPU_FX133_MS_ATT0 | 0x40022970 | FULL | Master attributes 0 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX133_MS_ATT1 | 0x40022974 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX133_MS_ATT2 | 0x40022978 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX133_MS_ATT3 | 0x4002297C | FULL | Master attributes 3 |

## 23.151 PPU_FX 134

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX134_SL_ADDR | 0x40022980 | FULL | Slave region, base address |
| PERI_MS_PPU_FX134_SL_SIZE | 0x40022984 | FULL | Slave region, size |
| PERI_MS_PPU_FX134_SL_ATT0 | 0x40022990 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX134_SL_ATT1 | 0x40022994 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX134_SL_ATT2 | 0x40022998 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX134_SL_ATT3 | 0x4002299C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX134_MS_ADDR | 0x400229A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX134_MS_SIZE | 0x400229A4 | FULL | Master region, size |
| PERI_MS_PPU_FX134_MS_ATT0 | 0x400229B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX134_MS_ATT1 | 0x400229B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX134_MS_ATT2 | 0x400229B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX134_MS_ATT3 | 0x400229BC | FULL | Master attributes 3 |

## 23.152 PPU_FX 135

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX135_SL_ADDR | 0x400229C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX135_SL_SIZE | 0x400229C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX135_SL_ATT0 | 0x400229D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX135_SL_ATT1 | 0x400229D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX135_SL_ATT2 | 0x400229D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX135_SL_ATT3 | 0x400229DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX135_MS_ADDR | 0x400229E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX135_MS_SIZE | 0x400229E4 | FULL | Master region, size |
| PERI_MS_PPU_FX135_MS_ATT0 | 0x400229F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX135_MS_ATT1 | 0x400229F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX135_MS_ATT2 | 0x400229F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX135_MS_ATT3 | 0x400229FC | FULL | Master attributes 3 |

## 23.153 PPU_FX 136

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX136_SL_ADDR | 0x40022A00 | FULL | Slave region, base address |
| PERI_MS_PPU_FX136_SL_SIZE | 0x40022A04 | FULL | Slave region, size |
| PERI_MS_PPU_FX136_SL_ATT0 | 0x40022A10 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX136_SL_ATT1 | 0x40022A14 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX136_SL_ATT2 | 0x40022A18 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX136_SL_ATT3 | 0x40022A1C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX136_MS_ADDR | 0x40022A20 | FULL | Master region, base address |
| PERI_MS_PPU_FX136_MS_SIZE | 0x40022A24 | FULL | Master region, size |
| PERI_MS_PPU_FX136_MS_ATT0 | 0x40022A30 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX136_MS_ATT1 | 0x40022A34 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX136_MS_ATT2 | 0x40022A38 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX136_MS_ATT3 | 0x40022A3C | FULL | Master attributes 3 |

## 23.154 PPU_FX 137

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX137_SL_ADDR | 0x40022A40 | FULL | Slave region, base address |
| PERI_MS_PPU_FX137_SL_SIZE | 0x40022A44 | FULL | Slave region, size |
| PERI_MS_PPU_FX137_SL_ATT0 | 0x40022A50 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX137_SL_ATT1 | 0x40022A54 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX137_SL_ATT2 | 0x40022A58 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX137_SL_ATT3 | 0x40022A5C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX137_MS_ADDR | 0x40022A60 | FULL | Master region, base address |
| PERI_MS_PPU_FX137_MS_SIZE | 0x40022A64 | FULL | Master region, size |
| PERI_MS_PPU_FX137_MS_ATT0 | 0x40022A70 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX137_MS_ATT1 | 0x40022A74 | FULL | Master attributes 1 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX137_MS_ATT2 | 0x40022A78 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX137_MS_ATT3 | 0x40022A7C | FULL | Master attributes 3 |

## 23.155 PPU_FX 138

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX138_SL_ADDR | 0x40022A80 | FULL | Slave region, base address |
| PERI_MS_PPU_FX138_SL_SIZE | 0x40022A84 | FULL | Slave region, size |
| PERI_MS_PPU_FX138_SL_ATT0 | 0x40022A90 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX138_SL_ATT1 | 0x40022A94 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX138_SL_ATT2 | 0x40022A98 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX138_SL_ATT3 | 0x40022A9C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX138_MS_ADDR | 0x40022AA0 | FULL | Master region, base address |
| PERI_MS_PPU_FX138_MS_SIZE | 0x40022AA4 | FULL | Master region, size |
| PERI_MS_PPU_FX138_MS_ATT0 | 0x40022AB0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX138_MS_ATT1 | 0x40022AB4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX138_MS_ATT2 | 0x40022AB8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX138_MS_ATT3 | 0x40022ABC | FULL | Master attributes 3 |

## 23.156 PPU_FX 139

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX139_SL_ADDR | 0x40022AC0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX139_SL_SIZE | 0x40022AC4 | FULL | Slave region, size |
| PERI_MS_PPU_FX139_SL_ATT0 | 0x40022AD0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX139_SL_ATT1 | 0x40022AD4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX139_SL_ATT2 | 0x40022AD8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX139_SL_ATT3 | 0x40022ADC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX139_MS_ADDR | 0x40022AE0 | FULL | Master region, base address |
| PERI_MS_PPU_FX139_MS_SIZE | 0x40022AE4 | FULL | Master region, size |
| PERI_MS_PPU_FX139_MS_ATT0 | 0x40022AF0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX139_MS_ATT1 | 0x40022AF4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX139_MS_ATT2 | 0x40022AF8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX139_MS_ATT3 | 0x40022AFC | FULL | Master attributes 3 |

## 23.157 PPU_FX 140

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX140_SL_ADDR | 0x40022B00 | FULL | Slave region, base address |
| PERI_MS_PPU_FX140_SL_SIZE | 0x40022B04 | FULL | Slave region, size |
| PERI_MS_PPU_FX140_SL_ATT0 | 0x40022B10 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX140_SL_ATT1 | 0x40022B14 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX140_SL_ATT2 | 0x40022B18 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX140_SL_ATT3 | 0x40022B1C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX140_MS_ADDR | 0x40022B20 | FULL | Master region, base address |
| PERI_MS_PPU_FX140_MS_SIZE | 0x40022B24 | FULL | Master region, size |
| PERI_MS_PPU_FX140_MS_ATT0 | 0x40022B30 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX140_MS_ATT1 | 0x40022B34 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX140_MS_ATT2 | 0x40022B38 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX140_MS_ATT3 | 0x40022B3C | FULL | Master attributes 3 |

## 23.158 PPU_FX 141

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX141_SL_ADDR | 0x40022B40 | FULL | Slave region, base address |
| PERI_MS_PPU_FX141_SL_SIZE | 0x40022B44 | FULL | Slave region, size |
| PERI_MS_PPU_FX141_SL_ATT0 | 0x40022B50 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX141_SL_ATT1 | 0x40022B54 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX141_SL_ATT2 | 0x40022B58 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX141_SL_ATT3 | 0x40022B5C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX141_MS_ADDR | 0x40022B60 | FULL | Master region, base address |
| PERI_MS_PPU_FX141_MS_SIZE | 0x40022B64 | FULL | Master region, size |
| PERI_MS_PPU_FX141_MS_ATT0 | 0x40022B70 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX141_MS_ATT1 | 0x40022B74 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX141_MS_ATT2 | 0x40022B78 | FULL | Master attributes 2 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX141_MS_ATT3 | 0x40022B7C | FULL | Master attributes 3 |

## 23.159 PPU_FX 142

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX142_SL_ADDR | 0x40022B80 | FULL | Slave region, base address |
| PERI_MS_PPU_FX142_SL_SIZE | 0x40022B84 | FULL | Slave region, size |
| PERI_MS_PPU_FX142_SL_ATT0 | 0x40022B90 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX142_SL_ATT1 | 0x40022B94 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX142_SL_ATT2 | 0x40022B98 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX142_SL_ATT3 | 0x40022B9C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX142_MS_ADDR | 0x40022BA0 | FULL | Master region, base address |
| PERI_MS_PPU_FX142_MS_SIZE | 0x40022BA4 | FULL | Master region, size |
| PERI_MS_PPU_FX142_MS_ATT0 | 0x40022BB0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX142_MS_ATT1 | 0x40022BB4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX142_MS_ATT2 | 0x40022BB8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX142_MS_ATT3 | 0x40022BBC | FULL | Master attributes 3 |

## 23.160 PPU_FX 143

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX143_SL_ADDR | 0x40022BC0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX143_SL_SIZE | 0x40022BC4 | FULL | Slave region, size |
| PERI_MS_PPU_FX143_SL_ATT0 | 0x40022BD0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX143_SL_ATT1 | 0x40022BD4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX143_SL_ATT2 | 0x40022BD8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX143_SL_ATT3 | 0x40022BDC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX143_MS_ADDR | 0x40022BE0 | FULL | Master region, base address |
| PERI_MS_PPU_FX143_MS_SIZE | 0x40022BE4 | FULL | Master region, size |
| PERI_MS_PPU_FX143_MS_ATT0 | 0x40022BF0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX143_MS_ATT1 | 0x40022BF4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX143_MS_ATT2 | 0x40022BF8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX143_MS_ATT3 | 0x40022BFC | FULL | Master attributes 3 |

## 23.161 PPU_FX 144

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX144_SL_ADDR | 0x40022C00 | FULL | Slave region, base address |
| PERI_MS_PPU_FX144_SL_SIZE | 0x40022C04 | FULL | Slave region, size |
| PERI_MS_PPU_FX144_SL_ATT0 | 0x40022C10 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX144_SL_ATT1 | 0x40022C14 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX144_SL_ATT2 | 0x40022C18 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX144_SL_ATT3 | 0x40022C1C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX144_MS_ADDR | 0x40022C20 | FULL | Master region, base address |
| PERI_MS_PPU_FX144_MS_SIZE | 0x40022C24 | FULL | Master region, size |
| PERI_MS_PPU_FX144_MS_ATT0 | 0x40022C30 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX144_MS_ATT1 | 0x40022C34 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX144_MS_ATT2 | 0x40022C38 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX144_MS_ATT3 | 0x40022C3C | FULL | Master attributes 3 |

## 23.162 PPU_FX 145

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX145_SL_ADDR | 0x40022C40 | FULL | Slave region, base address |
| PERI_MS_PPU_FX145_SL_SIZE | 0x40022C44 | FULL | Slave region, size |
| PERI_MS_PPU_FX145_SL_ATT0 | 0x40022C50 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX145_SL_ATT1 | 0x40022C54 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX145_SL_ATT2 | 0x40022C58 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX145_SL_ATT3 | 0x40022C5C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX145_MS_ADDR | 0x40022C60 | FULL | Master region, base address |
| PERI_MS_PPU_FX145_MS_SIZE | 0x40022C64 | FULL | Master region, size |
| PERI_MS_PPU_FX145_MS_ATT0 | 0x40022C70 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX145_MS_ATT1 | 0x40022C74 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX145_MS_ATT2 | 0x40022C78 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX145_MS_ATT3 | 0x40022C7C | FULL | Master attributes 3 |

## 23.163 PPU_FX 146

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX146_SL_ADDR | 0x40022C80 | FULL | Slave region, base address |
| PERI_MS_PPU_FX146_SL_SIZE | 0x40022C84 | FULL | Slave region, size |
| PERI_MS_PPU_FX146_SL_ATT0 | 0x40022C90 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX146_SL_ATT1 | 0x40022C94 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX146_SL_ATT2 | 0x40022C98 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX146_SL_ATT3 | 0x40022C9C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX146_MS_ADDR | 0x40022CA0 | FULL | Master region, base address |
| PERI_MS_PPU_FX146_MS_SIZE | 0x40022CA4 | FULL | Master region, size |
| PERI_MS_PPU_FX146_MS_ATT0 | 0x40022CB0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX146_MS_ATT1 | 0x40022CB4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX146_MS_ATT2 | 0x40022CB8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX146_MS_ATT3 | 0x40022CBC | FULL | Master attributes 3 |

## 23.164 PPU_FX 147

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX147_SL_ADDR | 0x40022CC0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX147_SL_SIZE | 0x40022CC4 | FULL | Slave region, size |
| PERI_MS_PPU_FX147_SL_ATT0 | 0x40022CD0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX147_SL_ATT1 | 0x40022CD4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX147_SL_ATT2 | 0x40022CD8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX147_SL_ATT3 | 0x40022CDC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX147_MS_ADDR | 0x40022CE0 | FULL | Master region, base address |
| PERI_MS_PPU_FX147_MS_SIZE | 0x40022CE4 | FULL | Master region, size |
| PERI_MS_PPU_FX147_MS_ATT0 | 0x40022CF0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX147_MS_ATT1 | 0x40022CF4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX147_MS_ATT2 | 0x40022CF8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX147_MS_ATT3 | 0x40022CFC | FULL | Master attributes 3 |

## 23.165 PPU_FX 148

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX148_SL_ADDR | 0x40022D00 | FULL | Slave region, base address |
| PERI_MS_PPU_FX148_SL_SIZE | 0x40022D04 | FULL | Slave region, size |
| PERI_MS_PPU_FX148_SL_ATT0 | 0x40022D10 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX148_SL_ATT1 | 0x40022D14 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX148_SL_ATT2 | 0x40022D18 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX148_SL_ATT3 | 0x40022D1C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX148_MS_ADDR | 0x40022D20 | FULL | Master region, base address |
| PERI_MS_PPU_FX148_MS_SIZE | 0x40022D24 | FULL | Master region, size |
| PERI_MS_PPU_FX148_MS_ATT0 | 0x40022D30 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX148_MS_ATT1 | 0x40022D34 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX148_MS_ATT2 | 0x40022D38 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX148_MS_ATT3 | 0x40022D3C | FULL | Master attributes 3 |

## 23.166 PPU_FX 149

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX149_SL_ADDR | 0x40022D40 | FULL | Slave region, base address |
| PERI_MS_PPU_FX149_SL_SIZE | 0x40022D44 | FULL | Slave region, size |
| PERI_MS_PPU_FX149_SL_ATT0 | 0x40022D50 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX149_SL_ATT1 | 0x40022D54 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX149_SL_ATT2 | 0x40022D58 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX149_SL_ATT3 | 0x40022D5C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX149_MS_ADDR | 0x40022D60 | FULL | Master region, base address |
| PERI_MS_PPU_FX149_MS_SIZE | 0x40022D64 | FULL | Master region, size |
| PERI_MS_PPU_FX149_MS_ATT0 | 0x40022D70 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX149_MS_ATT1 | 0x40022D74 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX149_MS_ATT2 | 0x40022D78 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX149_MS_ATT3 | 0x40022D7C | FULL | Master attributes 3 |

## 23.167 PPU_FX 150

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX150_SL_ADDR | 0x40022D80 | FULL | Slave region, base address |
| PERI_MS_PPU_FX150_SL_SIZE | 0x40022D84 | FULL | Slave region, size |
| PERI_MS_PPU_FX150_SL_ATT0 | 0x40022D90 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX150_SL_ATT1 | 0x40022D94 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX150_SL_ATT2 | 0x40022D98 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX150_SL_ATT3 | 0x40022D9C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX150_MS_ADDR | 0x40022DA0 | FULL | Master region, base address |
| PERI_MS_PPU_FX150_MS_SIZE | 0x40022DA4 | FULL | Master region, size |
| PERI_MS_PPU_FX150_MS_ATT0 | 0x40022DB0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX150_MS_ATT1 | 0x40022DB4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX150_MS_ATT2 | 0x40022DB8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX150_MS_ATT3 | 0x40022DBC | FULL | Master attributes 3 |

## 23.168 PPU_FX 151

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX151_SL_ADDR | 0x40022DC0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX151_SL_SIZE | 0x40022DC4 | FULL | Slave region, size |
| PERI_MS_PPU_FX151_SL_ATT0 | 0x40022DD0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX151_SL_ATT1 | 0x40022DD4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX151_SL_ATT2 | 0x40022DD8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX151_SL_ATT3 | 0x40022DDC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX151_MS_ADDR | 0x40022DE0 | FULL | Master region, base address |
| PERI_MS_PPU_FX151_MS_SIZE | 0x40022DE4 | FULL | Master region, size |
| PERI_MS_PPU_FX151_MS_ATT0 | 0x40022DF0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX151_MS_ATT1 | 0x40022DF4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX151_MS_ATT2 | 0x40022DF8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX151_MS_ATT3 | 0x40022DFC | FULL | Master attributes 3 |

## 23.169 PPU_FX 152

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX152_SL_ADDR | 0x40022E00 | FULL | Slave region, base address |
| PERI_MS_PPU_FX152_SL_SIZE | 0x40022E04 | FULL | Slave region, size |
| PERI_MS_PPU_FX152_SL_ATT0 | 0x40022E10 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX152_SL_ATT1 | 0x40022E14 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX152_SL_ATT2 | 0x40022E18 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX152_SL_ATT3 | 0x40022E1C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX152_MS_ADDR | 0x40022E20 | FULL | Master region, base address |
| PERI_MS_PPU_FX152_MS_SIZE | 0x40022E24 | FULL | Master region, size |
| PERI_MS_PPU_FX152_MS_ATT0 | 0x40022E30 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX152_MS_ATT1 | 0x40022E34 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX152_MS_ATT2 | 0x40022E38 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX152_MS_ATT3 | 0x40022E3C | FULL | Master attributes 3 |

## 23.170 PPU_FX 153

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX153_SL_ADDR | 0x40022E40 | FULL | Slave region, base address |
| PERI_MS_PPU_FX153_SL_SIZE | 0x40022E44 | FULL | Slave region, size |
| PERI_MS_PPU_FX153_SL_ATT0 | 0x40022E50 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX153_SL_ATT1 | 0x40022E54 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX153_SL_ATT2 | 0x40022E58 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX153_SL_ATT3 | 0x40022E5C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX153_MS_ADDR | 0x40022E60 | FULL | Master region, base address |
| PERI_MS_PPU_FX153_MS_SIZE | 0x40022E64 | FULL | Master region, size |
| PERI_MS_PPU_FX153_MS_ATT0 | 0x40022E70 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX153_MS_ATT1 | 0x40022E74 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX153_MS_ATT2 | 0x40022E78 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX153_MS_ATT3 | 0x40022E7C | FULL | Master attributes 3 |

## 23.171 PPU_FX 154

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX154_SL_ADDR | 0x40022E80 | FULL | Slave region, base address |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX154_SL_SIZE | 0x40022E84 | FULL | Slave region, size |
| PERI_MS_PPU_FX154_SL_ATT0 | 0x40022E90 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX154_SL_ATT1 | 0x40022E94 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX154_SL_ATT2 | 0x40022E98 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX154_SL_ATT3 | 0x40022E9C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX154_MS_ADDR | 0x40022EA0 | FULL | Master region, base address |
| PERI_MS_PPU_FX154_MS_SIZE | 0x40022EA4 | FULL | Master region, size |
| PERI_MS_PPU_FX154_MS_ATT0 | 0x40022EB0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX154_MS_ATT1 | 0x40022EB4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX154_MS_ATT2 | 0x40022EB8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX154_MS_ATT3 | 0x40022EBC | FULL | Master attributes 3 |

## 23.172 PPU_FX 155

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX155_SL_ADDR | 0x40022EC0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX155_SL_SIZE | 0x40022EC4 | FULL | Slave region, size |
| PERI_MS_PPU_FX155_SL_ATT0 | 0x40022ED0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX155_SL_ATT1 | 0x40022ED4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX155_SL_ATT2 | 0x40022ED8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX155_SL_ATT3 | 0x40022EDC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX155_MS_ADDR | 0x40022EE0 | FULL | Master region, base address |
| PERI_MS_PPU_FX155_MS_SIZE | 0x40022EE4 | FULL | Master region, size |
| PERI_MS_PPU_FX155_MS_ATT0 | 0x40022EF0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX155_MS_ATT1 | 0x40022EF4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX155_MS_ATT2 | 0x40022EF8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX155_MS_ATT3 | 0x40022EFC | FULL | Master attributes 3 |

## 23.173 PPU_FX 156

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX156_SL_ADDR | 0x40022F00 | FULL | Slave region, base address |
| PERI_MS_PPU_FX156_SL_SIZE | 0x40022F04 | FULL | Slave region, size |
| PERI_MS_PPU_FX156_SL_ATT0 | 0x40022F10 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX156_SL_ATT1 | 0x40022F14 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX156_SL_ATT2 | 0x40022F18 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX156_SL_ATT3 | 0x40022F1C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX156_MS_ADDR | 0x40022F20 | FULL | Master region, base address |
| PERI_MS_PPU_FX156_MS_SIZE | 0x40022F24 | FULL | Master region, size |
| PERI_MS_PPU_FX156_MS_ATT0 | 0x40022F30 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX156_MS_ATT1 | 0x40022F34 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX156_MS_ATT2 | 0x40022F38 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX156_MS_ATT3 | 0x40022F3C | FULL | Master attributes 3 |

## 23.174 PPU_FX 157

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX157_SL_ADDR | 0x40022F40 | FULL | Slave region, base address |
| PERI_MS_PPU_FX157_SL_SIZE | 0x40022F44 | FULL | Slave region, size |
| PERI_MS_PPU_FX157_SL_ATT0 | 0x40022F50 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX157_SL_ATT1 | 0x40022F54 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX157_SL_ATT2 | 0x40022F58 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX157_SL_ATT3 | 0x40022F5C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX157_MS_ADDR | 0x40022F60 | FULL | Master region, base address |
| PERI_MS_PPU_FX157_MS_SIZE | 0x40022F64 | FULL | Master region, size |
| PERI_MS_PPU_FX157_MS_ATT0 | 0x40022F70 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX157_MS_ATT1 | 0x40022F74 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX157_MS_ATT2 | 0x40022F78 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX157_MS_ATT3 | 0x40022F7C | FULL | Master attributes 3 |

## 23.175 PPU_FX 158

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX158_SL_ADDR | 0x40022F80 | FULL | Slave region, base address |
| PERI_MS_PPU_FX158_SL_SIZE | 0x40022F84 | FULL | Slave region, size |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX158_SL_ATT0 | 0x40022F90 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX158_SL_ATT1 | 0x40022F94 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX158_SL_ATT2 | 0x40022F98 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX158_SL_ATT3 | 0x40022F9C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX158_MS_ADDR | 0x40022FA0 | FULL | Master region, base address |
| PERI_MS_PPU_FX158_MS_SIZE | 0x40022FA4 | FULL | Master region, size |
| PERI_MS_PPU_FX158_MS_ATT0 | 0x40022FB0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX158_MS_ATT1 | 0x40022FB4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX158_MS_ATT2 | 0x40022FB8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX158_MS_ATT3 | 0x40022FBC | FULL | Master attributes 3 |

## 23.176 PPU_FX 159

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX159_SL_ADDR | 0x40022FC0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX159_SL_SIZE | 0x40022FC4 | FULL | Slave region, size |
| PERI_MS_PPU_FX159_SL_ATT0 | 0x40022FD0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX159_SL_ATT1 | 0x40022FD4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX159_SL_ATT2 | 0x40022FD8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX159_SL_ATT3 | 0x40022FDC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX159_MS_ADDR | 0x40022FE0 | FULL | Master region, base address |
| PERI_MS_PPU_FX159_MS_SIZE | 0x40022FE4 | FULL | Master region, size |
| PERI_MS_PPU_FX159_MS_ATT0 | 0x40022FF0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX159_MS_ATT1 | 0x40022FF4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX159_MS_ATT2 | 0x40022FF8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX159_MS_ATT3 | 0x40022FFC | FULL | Master attributes 3 |

## 23.177 PPU_FX 160

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX160_SL_ADDR | 0x40023000 | FULL | Slave region, base address |
| PERI_MS_PPU_FX160_SL_SIZE | 0x40023004 | FULL | Slave region, size |
| PERI_MS_PPU_FX160_SL_ATT0 | 0x40023010 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX160_SL_ATT1 | 0x40023014 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX160_SL_ATT2 | 0x40023018 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX160_SL_ATT3 | 0x4002301C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX160_MS_ADDR | 0x40023020 | FULL | Master region, base address |
| PERI_MS_PPU_FX160_MS_SIZE | 0x40023024 | FULL | Master region, size |
| PERI_MS_PPU_FX160_MS_ATT0 | 0x40023030 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX160_MS_ATT1 | 0x40023034 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX160_MS_ATT2 | 0x40023038 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX160_MS_ATT3 | 0x4002303C | FULL | Master attributes 3 |

## 23.178 PPU_FX 161

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX161_SL_ADDR | 0x40023040 | FULL | Slave region, base address |
| PERI_MS_PPU_FX161_SL_SIZE | 0x40023044 | FULL | Slave region, size |
| PERI_MS_PPU_FX161_SL_ATT0 | 0x40023050 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX161_SL_ATT1 | 0x40023054 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX161_SL_ATT2 | 0x40023058 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX161_SL_ATT3 | 0x4002305C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX161_MS_ADDR | 0x40023060 | FULL | Master region, base address |
| PERI_MS_PPU_FX161_MS_SIZE | 0x40023064 | FULL | Master region, size |
| PERI_MS_PPU_FX161_MS_ATT0 | 0x40023070 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX161_MS_ATT1 | 0x40023074 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX161_MS_ATT2 | 0x40023078 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX161_MS_ATT3 | 0x4002307C | FULL | Master attributes 3 |

## 23.179 PPU_FX 162

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX162_SL_ADDR | 0x40023080 | FULL | Slave region, base address |
| PERI_MS_PPU_FX162_SL_SIZE | 0x40023084 | FULL | Slave region, size |
| PERI_MS_PPU_FX162_SL_ATT0 | 0x40023090 | FULL | Slave attributes 0 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX162_SL_ATT1 | 0x40023094 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX162_SL_ATT2 | 0x40023098 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX162_SL_ATT3 | 0x4002309C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX162_MS_ADDR | 0x400230A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX162_MS_SIZE | 0x400230A4 | FULL | Master region, size |
| PERI_MS_PPU_FX162_MS_ATT0 | 0x400230B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX162_MS_ATT1 | 0x400230B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX162_MS_ATT2 | 0x400230B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX162_MS_ATT3 | 0x400230BC | FULL | Master attributes 3 |

## 23.180 PPU_FX 163

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX163_SL_ADDR | 0x400230C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX163_SL_SIZE | 0x400230C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX163_SL_ATT0 | 0x400230D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX163_SL_ATT1 | 0x400230D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX163_SL_ATT2 | 0x400230D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX163_SL_ATT3 | 0x400230DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX163_MS_ADDR | 0x400230E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX163_MS_SIZE | 0x400230E4 | FULL | Master region, size |
| PERI_MS_PPU_FX163_MS_ATT0 | 0x400230F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX163_MS_ATT1 | 0x400230F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX163_MS_ATT2 | 0x400230F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX163_MS_ATT3 | 0x400230FC | FULL | Master attributes 3 |

## 23.181 PPU_FX 164

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX164_SL_ADDR | 0x40023100 | FULL | Slave region, base address |
| PERI_MS_PPU_FX164_SL_SIZE | 0x40023104 | FULL | Slave region, size |
| PERI_MS_PPU_FX164_SL_ATT0 | 0x40023110 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX164_SL_ATT1 | 0x40023114 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX164_SL_ATT2 | 0x40023118 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX164_SL_ATT3 | 0x4002311C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX164_MS_ADDR | 0x40023120 | FULL | Master region, base address |
| PERI_MS_PPU_FX164_MS_SIZE | 0x40023124 | FULL | Master region, size |
| PERI_MS_PPU_FX164_MS_ATT0 | 0x40023130 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX164_MS_ATT1 | 0x40023134 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX164_MS_ATT2 | 0x40023138 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX164_MS_ATT3 | 0x4002313C | FULL | Master attributes 3 |

## 23.182 PPU_FX 165

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX165_SL_ADDR | 0x40023140 | FULL | Slave region, base address |
| PERI_MS_PPU_FX165_SL_SIZE | 0x40023144 | FULL | Slave region, size |
| PERI_MS_PPU_FX165_SL_ATT0 | 0x40023150 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX165_SL_ATT1 | 0x40023154 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX165_SL_ATT2 | 0x40023158 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX165_SL_ATT3 | 0x4002315C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX165_MS_ADDR | 0x40023160 | FULL | Master region, base address |
| PERI_MS_PPU_FX165_MS_SIZE | 0x40023164 | FULL | Master region, size |
| PERI_MS_PPU_FX165_MS_ATT0 | 0x40023170 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX165_MS_ATT1 | 0x40023174 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX165_MS_ATT2 | 0x40023178 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX165_MS_ATT3 | 0x4002317C | FULL | Master attributes 3 |

## 23.183 PPU_FX 166

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX166_SL_ADDR | 0x40023180 | FULL | Slave region, base address |
| PERI_MS_PPU_FX166_SL_SIZE | 0x40023184 | FULL | Slave region, size |
| PERI_MS_PPU_FX166_SL_ATT0 | 0x40023190 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX166_SL_ATT1 | 0x40023194 | FULL | Slave attributes 1 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX166_SL_ATT2 | 0x40023198 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX166_SL_ATT3 | 0x4002319C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX166_MS_ADDR | 0x400231A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX166_MS_SIZE | 0x400231A4 | FULL | Master region, size |
| PERI_MS_PPU_FX166_MS_ATT0 | 0x400231B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX166_MS_ATT1 | 0x400231B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX166_MS_ATT2 | 0x400231B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX166_MS_ATT3 | 0x400231BC | FULL | Master attributes 3 |

## 23.184 PPU_FX 167

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX167_SL_ADDR | 0x400231C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX167_SL_SIZE | 0x400231C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX167_SL_ATT0 | 0x400231D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX167_SL_ATT1 | 0x400231D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX167_SL_ATT2 | 0x400231D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX167_SL_ATT3 | 0x400231DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX167_MS_ADDR | 0x400231E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX167_MS_SIZE | 0x400231E4 | FULL | Master region, size |
| PERI_MS_PPU_FX167_MS_ATT0 | 0x400231F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX167_MS_ATT1 | 0x400231F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX167_MS_ATT2 | 0x400231F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX167_MS_ATT3 | 0x400231FC | FULL | Master attributes 3 |

## 23.185 PPU_FX 168

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX168_SL_ADDR | 0x40023200 | FULL | Slave region, base address |
| PERI_MS_PPU_FX168_SL_SIZE | 0x40023204 | FULL | Slave region, size |
| PERI_MS_PPU_FX168_SL_ATT0 | 0x40023210 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX168_SL_ATT1 | 0x40023214 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX168_SL_ATT2 | 0x40023218 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX168_SL_ATT3 | 0x4002321C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX168_MS_ADDR | 0x40023220 | FULL | Master region, base address |
| PERI_MS_PPU_FX168_MS_SIZE | 0x40023224 | FULL | Master region, size |
| PERI_MS_PPU_FX168_MS_ATT0 | 0x40023230 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX168_MS_ATT1 | 0x40023234 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX168_MS_ATT2 | 0x40023238 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX168_MS_ATT3 | 0x4002323C | FULL | Master attributes 3 |

## 23.186 PPU_FX 169

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX169_SL_ADDR | 0x40023240 | FULL | Slave region, base address |
| PERI_MS_PPU_FX169_SL_SIZE | 0x40023244 | FULL | Slave region, size |
| PERI_MS_PPU_FX169_SL_ATT0 | 0x40023250 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX169_SL_ATT1 | 0x40023254 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX169_SL_ATT2 | 0x40023258 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX169_SL_ATT3 | 0x4002325C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX169_MS_ADDR | 0x40023260 | FULL | Master region, base address |
| PERI_MS_PPU_FX169_MS_SIZE | 0x40023264 | FULL | Master region, size |
| PERI_MS_PPU_FX169_MS_ATT0 | 0x40023270 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX169_MS_ATT1 | 0x40023274 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX169_MS_ATT2 | 0x40023278 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX169_MS_ATT3 | 0x4002327C | FULL | Master attributes 3 |

## 23.187 PPU_FX 170

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX170_SL_ADDR | 0x40023280 | FULL | Slave region, base address |
| PERI_MS_PPU_FX170_SL_SIZE | 0x40023284 | FULL | Slave region, size |
| PERI_MS_PPU_FX170_SL_ATT0 | 0x40023290 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX170_SL_ATT1 | 0x40023294 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX170_SL_ATT2 | 0x40023298 | FULL | Slave attributes 2 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX170_SL_ATT3 | 0x4002329C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX170_MS_ADDR | 0x400232A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX170_MS_SIZE | 0x400232A4 | FULL | Master region, size |
| PERI_MS_PPU_FX170_MS_ATT0 | 0x400232B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX170_MS_ATT1 | 0x400232B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX170_MS_ATT2 | 0x400232B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX170_MS_ATT3 | 0x400232BC | FULL | Master attributes 3 |

## 23.188 PPU_FX 171

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX171_SL_ADDR | 0x400232C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX171_SL_SIZE | 0x400232C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX171_SL_ATT0 | 0x400232D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX171_SL_ATT1 | 0x400232D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX171_SL_ATT2 | 0x400232D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX171_SL_ATT3 | 0x400232DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX171_MS_ADDR | 0x400232E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX171_MS_SIZE | 0x400232E4 | FULL | Master region, size |
| PERI_MS_PPU_FX171_MS_ATT0 | 0x400232F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX171_MS_ATT1 | 0x400232F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX171_MS_ATT2 | 0x400232F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX171_MS_ATT3 | 0x400232FC | FULL | Master attributes 3 |

## 23.189 PPU_FX 172

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX172_SL_ADDR | 0x40023300 | FULL | Slave region, base address |
| PERI_MS_PPU_FX172_SL_SIZE | 0x40023304 | FULL | Slave region, size |
| PERI_MS_PPU_FX172_SL_ATT0 | 0x40023310 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX172_SL_ATT1 | 0x40023314 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX172_SL_ATT2 | 0x40023318 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX172_SL_ATT3 | 0x4002331C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX172_MS_ADDR | 0x40023320 | FULL | Master region, base address |
| PERI_MS_PPU_FX172_MS_SIZE | 0x40023324 | FULL | Master region, size |
| PERI_MS_PPU_FX172_MS_ATT0 | 0x40023330 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX172_MS_ATT1 | 0x40023334 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX172_MS_ATT2 | 0x40023338 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX172_MS_ATT3 | 0x4002333C | FULL | Master attributes 3 |

## 23.190 PPU_FX 173

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX173_SL_ADDR | 0x40023340 | FULL | Slave region, base address |
| PERI_MS_PPU_FX173_SL_SIZE | 0x40023344 | FULL | Slave region, size |
| PERI_MS_PPU_FX173_SL_ATT0 | 0x40023350 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX173_SL_ATT1 | 0x40023354 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX173_SL_ATT2 | 0x40023358 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX173_SL_ATT3 | 0x4002335C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX173_MS_ADDR | 0x40023360 | FULL | Master region, base address |
| PERI_MS_PPU_FX173_MS_SIZE | 0x40023364 | FULL | Master region, size |
| PERI_MS_PPU_FX173_MS_ATT0 | 0x40023370 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX173_MS_ATT1 | 0x40023374 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX173_MS_ATT2 | 0x40023378 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX173_MS_ATT3 | 0x4002337C | FULL | Master attributes 3 |

## 23.191 PPU_FX 174

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX174_SL_ADDR | 0x40023380 | FULL | Slave region, base address |
| PERI_MS_PPU_FX174_SL_SIZE | 0x40023384 | FULL | Slave region, size |
| PERI_MS_PPU_FX174_SL_ATT0 | 0x40023390 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX174_SL_ATT1 | 0x40023394 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX174_SL_ATT2 | 0x40023398 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX174_SL_ATT3 | 0x4002339C | FULL | Slave attributes 3 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX174_MS_ADDR | 0x400233A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX174_MS_SIZE | 0x400233A4 | FULL | Master region, size |
| PERI_MS_PPU_FX174_MS_ATT0 | 0x400233B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX174_MS_ATT1 | 0x400233B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX174_MS_ATT2 | 0x400233B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX174_MS_ATT3 | 0x400233BC | FULL | Master attributes 3 |

## 23.192 PPU_FX 175

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX175_SL_ADDR | 0x400233C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX175_SL_SIZE | 0x400233C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX175_SL_ATT0 | 0x400233D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX175_SL_ATT1 | 0x400233D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX175_SL_ATT2 | 0x400233D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX175_SL_ATT3 | 0x400233DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX175_MS_ADDR | 0x400233E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX175_MS_SIZE | 0x400233E4 | FULL | Master region, size |
| PERI_MS_PPU_FX175_MS_ATT0 | 0x400233F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX175_MS_ATT1 | 0x400233F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX175_MS_ATT2 | 0x400233F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX175_MS_ATT3 | 0x400233FC | FULL | Master attributes 3 |

## 23.193 PPU_FX 176

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX176_SL_ADDR | 0x40023400 | FULL | Slave region, base address |
| PERI_MS_PPU_FX176_SL_SIZE | 0x40023404 | FULL | Slave region, size |
| PERI_MS_PPU_FX176_SL_ATT0 | 0x40023410 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX176_SL_ATT1 | 0x40023414 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX176_SL_ATT2 | 0x40023418 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX176_SL_ATT3 | 0x4002341C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX176_MS_ADDR | 0x40023420 | FULL | Master region, base address |
| PERI_MS_PPU_FX176_MS_SIZE | 0x40023424 | FULL | Master region, size |
| PERI_MS_PPU_FX176_MS_ATT0 | 0x40023430 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX176_MS_ATT1 | 0x40023434 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX176_MS_ATT2 | 0x40023438 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX176_MS_ATT3 | 0x4002343C | FULL | Master attributes 3 |

## 23.194 PPU_FX 177

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX177_SL_ADDR | 0x40023440 | FULL | Slave region, base address |
| PERI_MS_PPU_FX177_SL_SIZE | 0x40023444 | FULL | Slave region, size |
| PERI_MS_PPU_FX177_SL_ATT0 | 0x40023450 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX177_SL_ATT1 | 0x40023454 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX177_SL_ATT2 | 0x40023458 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX177_SL_ATT3 | 0x4002345C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX177_MS_ADDR | 0x40023460 | FULL | Master region, base address |
| PERI_MS_PPU_FX177_MS_SIZE | 0x40023464 | FULL | Master region, size |
| PERI_MS_PPU_FX177_MS_ATT0 | 0x40023470 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX177_MS_ATT1 | 0x40023474 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX177_MS_ATT2 | 0x40023478 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX177_MS_ATT3 | 0x4002347C | FULL | Master attributes 3 |

## 23.195 PPU_FX 178

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX178_SL_ADDR | 0x40023480 | FULL | Slave region, base address |
| PERI_MS_PPU_FX178_SL_SIZE | 0x40023484 | FULL | Slave region, size |
| PERI_MS_PPU_FX178_SL_ATT0 | 0x40023490 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX178_SL_ATT1 | 0x40023494 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX178_SL_ATT2 | 0x40023498 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX178_SL_ATT3 | 0x4002349C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX178_MS_ADDR | 0x400234A0 | FULL | Master region, base address |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX178_MS_SIZE | 0x400234A4 | FULL | Master region, size |
| PERI_MS_PPU_FX178_MS_ATT0 | 0x400234B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX178_MS_ATT1 | 0x400234B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX178_MS_ATT2 | 0x400234B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX178_MS_ATT3 | 0x400234BC | FULL | Master attributes 3 |

## 23.196 PPU_FX 179

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX179_SL_ADDR | 0x400234C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX179_SL_SIZE | 0x400234C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX179_SL_ATT0 | 0x400234D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX179_SL_ATT1 | 0x400234D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX179_SL_ATT2 | 0x400234D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX179_SL_ATT3 | 0x400234DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX179_MS_ADDR | 0x400234E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX179_MS_SIZE | 0x400234E4 | FULL | Master region, size |
| PERI_MS_PPU_FX179_MS_ATT0 | 0x400234F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX179_MS_ATT1 | 0x400234F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX179_MS_ATT2 | 0x400234F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX179_MS_ATT3 | 0x400234FC | FULL | Master attributes 3 |

## 23.197 PPU_FX 180

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX180_SL_ADDR | 0x40023500 | FULL | Slave region, base address |
| PERI_MS_PPU_FX180_SL_SIZE | 0x40023504 | FULL | Slave region, size |
| PERI_MS_PPU_FX180_SL_ATT0 | 0x40023510 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX180_SL_ATT1 | 0x40023514 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX180_SL_ATT2 | 0x40023518 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX180_SL_ATT3 | 0x4002351C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX180_MS_ADDR | 0x40023520 | FULL | Master region, base address |
| PERI_MS_PPU_FX180_MS_SIZE | 0x40023524 | FULL | Master region, size |
| PERI_MS_PPU_FX180_MS_ATT0 | 0x40023530 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX180_MS_ATT1 | 0x40023534 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX180_MS_ATT2 | 0x40023538 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX180_MS_ATT3 | 0x4002353C | FULL | Master attributes 3 |

## 23.198 PPU_FX 181

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX181_SL_ADDR | 0x40023540 | FULL | Slave region, base address |
| PERI_MS_PPU_FX181_SL_SIZE | 0x40023544 | FULL | Slave region, size |
| PERI_MS_PPU_FX181_SL_ATT0 | 0x40023550 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX181_SL_ATT1 | 0x40023554 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX181_SL_ATT2 | 0x40023558 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX181_SL_ATT3 | 0x4002355C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX181_MS_ADDR | 0x40023560 | FULL | Master region, base address |
| PERI_MS_PPU_FX181_MS_SIZE | 0x40023564 | FULL | Master region, size |
| PERI_MS_PPU_FX181_MS_ATT0 | 0x40023570 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX181_MS_ATT1 | 0x40023574 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX181_MS_ATT2 | 0x40023578 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX181_MS_ATT3 | 0x4002357C | FULL | Master attributes 3 |

## 23.199 PPU_FX 182

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX182_SL_ADDR | 0x40023580 | FULL | Slave region, base address |
| PERI_MS_PPU_FX182_SL_SIZE | 0x40023584 | FULL | Slave region, size |
| PERI_MS_PPU_FX182_SL_ATT0 | 0x40023590 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX182_SL_ATT1 | 0x40023594 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX182_SL_ATT2 | 0x40023598 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX182_SL_ATT3 | 0x4002359C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX182_MS_ADDR | 0x400235A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX182_MS_SIZE | 0x400235A4 | FULL | Master region, size |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX182_MS_ATT0 | 0x400235B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX182_MS_ATT1 | 0x400235B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX182_MS_ATT2 | 0x400235B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX182_MS_ATT3 | 0x400235BC | FULL | Master attributes 3 |

## 23.200 PPU_FX 183

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX183_SL_ADDR | 0x400235C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX183_SL_SIZE | 0x400235C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX183_SL_ATT0 | 0x400235D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX183_SL_ATT1 | 0x400235D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX183_SL_ATT2 | 0x400235D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX183_SL_ATT3 | 0x400235DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX183_MS_ADDR | 0x400235E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX183_MS_SIZE | 0x400235E4 | FULL | Master region, size |
| PERI_MS_PPU_FX183_MS_ATT0 | 0x400235F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX183_MS_ATT1 | 0x400235F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX183_MS_ATT2 | 0x400235F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX183_MS_ATT3 | 0x400235FC | FULL | Master attributes 3 |

## 23.201 PPU_FX 184

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX184_SL_ADDR | 0x40023600 | FULL | Slave region, base address |
| PERI_MS_PPU_FX184_SL_SIZE | 0x40023604 | FULL | Slave region, size |
| PERI_MS_PPU_FX184_SL_ATT0 | 0x40023610 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX184_SL_ATT1 | 0x40023614 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX184_SL_ATT2 | 0x40023618 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX184_SL_ATT3 | 0x4002361C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX184_MS_ADDR | 0x40023620 | FULL | Master region, base address |
| PERI_MS_PPU_FX184_MS_SIZE | 0x40023624 | FULL | Master region, size |
| PERI_MS_PPU_FX184_MS_ATT0 | 0x40023630 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX184_MS_ATT1 | 0x40023634 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX184_MS_ATT2 | 0x40023638 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX184_MS_ATT3 | 0x4002363C | FULL | Master attributes 3 |

## 23.202 PPU_FX 185

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX185_SL_ADDR | 0x40023640 | FULL | Slave region, base address |
| PERI_MS_PPU_FX185_SL_SIZE | 0x40023644 | FULL | Slave region, size |
| PERI_MS_PPU_FX185_SL_ATT0 | 0x40023650 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX185_SL_ATT1 | 0x40023654 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX185_SL_ATT2 | 0x40023658 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX185_SL_ATT3 | 0x4002365C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX185_MS_ADDR | 0x40023660 | FULL | Master region, base address |
| PERI_MS_PPU_FX185_MS_SIZE | 0x40023664 | FULL | Master region, size |
| PERI_MS_PPU_FX185_MS_ATT0 | 0x40023670 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX185_MS_ATT1 | 0x40023674 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX185_MS_ATT2 | 0x40023678 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX185_MS_ATT3 | 0x4002367C | FULL | Master attributes 3 |

## 23.203 PPU_FX 186

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX186_SL_ADDR | 0x40023680 | FULL | Slave region, base address |
| PERI_MS_PPU_FX186_SL_SIZE | 0x40023684 | FULL | Slave region, size |
| PERI_MS_PPU_FX186_SL_ATT0 | 0x40023690 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX186_SL_ATT1 | 0x40023694 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX186_SL_ATT2 | 0x40023698 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX186_SL_ATT3 | 0x4002369C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX186_MS_ADDR | 0x400236A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX186_MS_SIZE | 0x400236A4 | FULL | Master region, size |
| PERI_MS_PPU_FX186_MS_ATT0 | 0x400236B0 | FULL | Master attributes 0 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX186_MS_ATT1 | 0x400236B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX186_MS_ATT2 | 0x400236B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX186_MS_ATT3 | 0x400236BC | FULL | Master attributes 3 |

## 23.204 PPU_FX 187

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX187_SL_ADDR | 0x400236C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX187_SL_SIZE | 0x400236C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX187_SL_ATT0 | 0x400236D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX187_SL_ATT1 | 0x400236D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX187_SL_ATT2 | 0x400236D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX187_SL_ATT3 | 0x400236DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX187_MS_ADDR | 0x400236E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX187_MS_SIZE | 0x400236E4 | FULL | Master region, size |
| PERI_MS_PPU_FX187_MS_ATT0 | 0x400236F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX187_MS_ATT1 | 0x400236F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX187_MS_ATT2 | 0x400236F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX187_MS_ATT3 | 0x400236FC | FULL | Master attributes 3 |

## 23.205 PPU_FX 188

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX188_SL_ADDR | 0x40023700 | FULL | Slave region, base address |
| PERI_MS_PPU_FX188_SL_SIZE | 0x40023704 | FULL | Slave region, size |
| PERI_MS_PPU_FX188_SL_ATT0 | 0x40023710 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX188_SL_ATT1 | 0x40023714 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX188_SL_ATT2 | 0x40023718 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX188_SL_ATT3 | 0x4002371C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX188_MS_ADDR | 0x40023720 | FULL | Master region, base address |
| PERI_MS_PPU_FX188_MS_SIZE | 0x40023724 | FULL | Master region, size |
| PERI_MS_PPU_FX188_MS_ATT0 | 0x40023730 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX188_MS_ATT1 | 0x40023734 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX188_MS_ATT2 | 0x40023738 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX188_MS_ATT3 | 0x4002373C | FULL | Master attributes 3 |

## 23.206 PPU_FX 189

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX189_SL_ADDR | 0x40023740 | FULL | Slave region, base address |
| PERI_MS_PPU_FX189_SL_SIZE | 0x40023744 | FULL | Slave region, size |
| PERI_MS_PPU_FX189_SL_ATT0 | 0x40023750 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX189_SL_ATT1 | 0x40023754 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX189_SL_ATT2 | 0x40023758 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX189_SL_ATT3 | 0x4002375C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX189_MS_ADDR | 0x40023760 | FULL | Master region, base address |
| PERI_MS_PPU_FX189_MS_SIZE | 0x40023764 | FULL | Master region, size |
| PERI_MS_PPU_FX189_MS_ATT0 | 0x40023770 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX189_MS_ATT1 | 0x40023774 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX189_MS_ATT2 | 0x40023778 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX189_MS_ATT3 | 0x4002377C | FULL | Master attributes 3 |

## 23.207 PPU_FX 190

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX190_SL_ADDR | 0x40023780 | FULL | Slave region, base address |
| PERI_MS_PPU_FX190_SL_SIZE | 0x40023784 | FULL | Slave region, size |
| PERI_MS_PPU_FX190_SL_ATT0 | 0x40023790 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX190_SL_ATT1 | 0x40023794 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX190_SL_ATT2 | 0x40023798 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX190_SL_ATT3 | 0x4002379C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX190_MS_ADDR | 0x400237A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX190_MS_SIZE | 0x400237A4 | FULL | Master region, size |
| PERI_MS_PPU_FX190_MS_ATT0 | 0x400237B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX190_MS_ATT1 | 0x400237B4 | FULL | Master attributes 1 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX190_MS_ATT2 | 0x400237B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX190_MS_ATT3 | 0x400237BC | FULL | Master attributes 3 |

## 23.208 PPU_FX 191

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX191_SL_ADDR | 0x400237C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX191_SL_SIZE | 0x400237C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX191_SL_ATT0 | 0x400237D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX191_SL_ATT1 | 0x400237D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX191_SL_ATT2 | 0x400237D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX191_SL_ATT3 | 0x400237DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX191_MS_ADDR | 0x400237E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX191_MS_SIZE | 0x400237E4 | FULL | Master region, size |
| PERI_MS_PPU_FX191_MS_ATT0 | 0x400237F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX191_MS_ATT1 | 0x400237F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX191_MS_ATT2 | 0x400237F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX191_MS_ATT3 | 0x400237FC | FULL | Master attributes 3 |

## 23.209 PPU_FX 192

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX192_SL_ADDR | 0x40023800 | FULL | Slave region, base address |
| PERI_MS_PPU_FX192_SL_SIZE | 0x40023804 | FULL | Slave region, size |
| PERI_MS_PPU_FX192_SL_ATT0 | 0x40023810 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX192_SL_ATT1 | 0x40023814 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX192_SL_ATT2 | 0x40023818 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX192_SL_ATT3 | 0x4002381C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX192_MS_ADDR | 0x40023820 | FULL | Master region, base address |
| PERI_MS_PPU_FX192_MS_SIZE | 0x40023824 | FULL | Master region, size |
| PERI_MS_PPU_FX192_MS_ATT0 | 0x40023830 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX192_MS_ATT1 | 0x40023834 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX192_MS_ATT2 | 0x40023838 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX192_MS_ATT3 | 0x4002383C | FULL | Master attributes 3 |

## 23.210 PPU_FX 193

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX193_SL_ADDR | 0x40023840 | FULL | Slave region, base address |
| PERI_MS_PPU_FX193_SL_SIZE | 0x40023844 | FULL | Slave region, size |
| PERI_MS_PPU_FX193_SL_ATT0 | 0x40023850 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX193_SL_ATT1 | 0x40023854 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX193_SL_ATT2 | 0x40023858 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX193_SL_ATT3 | 0x4002385C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX193_MS_ADDR | 0x40023860 | FULL | Master region, base address |
| PERI_MS_PPU_FX193_MS_SIZE | 0x40023864 | FULL | Master region, size |
| PERI_MS_PPU_FX193_MS_ATT0 | 0x40023870 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX193_MS_ATT1 | 0x40023874 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX193_MS_ATT2 | 0x40023878 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX193_MS_ATT3 | 0x4002387C | FULL | Master attributes 3 |

## 23.211 PPU_FX 194

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX194_SL_ADDR | 0x40023880 | FULL | Slave region, base address |
| PERI_MS_PPU_FX194_SL_SIZE | 0x40023884 | FULL | Slave region, size |
| PERI_MS_PPU_FX194_SL_ATT0 | 0x40023890 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX194_SL_ATT1 | 0x40023894 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX194_SL_ATT2 | 0x40023898 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX194_SL_ATT3 | 0x4002389C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX194_MS_ADDR | 0x400238A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX194_MS_SIZE | 0x400238A4 | FULL | Master region, size |
| PERI_MS_PPU_FX194_MS_ATT0 | 0x400238B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX194_MS_ATT1 | 0x400238B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX194_MS_ATT2 | 0x400238B8 | FULL | Master attributes 2 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX194_MS_ATT3 | 0x400238BC | FULL | Master attributes 3 |

## 23.212 PPU_FX 195

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX195_SL_ADDR | 0x400238C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX195_SL_SIZE | 0x400238C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX195_SL_ATT0 | 0x400238D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX195_SL_ATT1 | 0x400238D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX195_SL_ATT2 | 0x400238D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX195_SL_ATT3 | 0x400238DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX195_MS_ADDR | 0x400238E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX195_MS_SIZE | 0x400238E4 | FULL | Master region, size |
| PERI_MS_PPU_FX195_MS_ATT0 | 0x400238F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX195_MS_ATT1 | 0x400238F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX195_MS_ATT2 | 0x400238F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX195_MS_ATT3 | 0x400238FC | FULL | Master attributes 3 |

## 23.213 PPU_FX 196

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX196_SL_ADDR | 0x40023900 | FULL | Slave region, base address |
| PERI_MS_PPU_FX196_SL_SIZE | 0x40023904 | FULL | Slave region, size |
| PERI_MS_PPU_FX196_SL_ATT0 | 0x40023910 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX196_SL_ATT1 | 0x40023914 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX196_SL_ATT2 | 0x40023918 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX196_SL_ATT3 | 0x4002391C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX196_MS_ADDR | 0x40023920 | FULL | Master region, base address |
| PERI_MS_PPU_FX196_MS_SIZE | 0x40023924 | FULL | Master region, size |
| PERI_MS_PPU_FX196_MS_ATT0 | 0x40023930 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX196_MS_ATT1 | 0x40023934 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX196_MS_ATT2 | 0x40023938 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX196_MS_ATT3 | 0x4002393C | FULL | Master attributes 3 |

## 23.214 PPU_FX 197

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX197_SL_ADDR | 0x40023940 | FULL | Slave region, base address |
| PERI_MS_PPU_FX197_SL_SIZE | 0x40023944 | FULL | Slave region, size |
| PERI_MS_PPU_FX197_SL_ATT0 | 0x40023950 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX197_SL_ATT1 | 0x40023954 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX197_SL_ATT2 | 0x40023958 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX197_SL_ATT3 | 0x4002395C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX197_MS_ADDR | 0x40023960 | FULL | Master region, base address |
| PERI_MS_PPU_FX197_MS_SIZE | 0x40023964 | FULL | Master region, size |
| PERI_MS_PPU_FX197_MS_ATT0 | 0x40023970 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX197_MS_ATT1 | 0x40023974 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX197_MS_ATT2 | 0x40023978 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX197_MS_ATT3 | 0x4002397C | FULL | Master attributes 3 |

## 23.215 PPU_FX 198

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX198_SL_ADDR | 0x40023980 | FULL | Slave region, base address |
| PERI_MS_PPU_FX198_SL_SIZE | 0x40023984 | FULL | Slave region, size |
| PERI_MS_PPU_FX198_SL_ATT0 | 0x40023990 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX198_SL_ATT1 | 0x40023994 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX198_SL_ATT2 | 0x40023998 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX198_SL_ATT3 | 0x4002399C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX198_MS_ADDR | 0x400239A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX198_MS_SIZE | 0x400239A4 | FULL | Master region, size |
| PERI_MS_PPU_FX198_MS_ATT0 | 0x400239B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX198_MS_ATT1 | 0x400239B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX198_MS_ATT2 | 0x400239B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX198_MS_ATT3 | 0x400239BC | FULL | Master attributes 3 |

## 23.216 PPU_FX 199

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX199_SL_ADDR | 0x400239C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX199_SL_SIZE | 0x400239C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX199_SL_ATT0 | 0x400239D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX199_SL_ATT1 | 0x400239D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX199_SL_ATT2 | 0x400239D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX199_SL_ATT3 | 0x400239DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX199_MS_ADDR | 0x400239E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX199_MS_SIZE | 0x400239E4 | FULL | Master region, size |
| PERI_MS_PPU_FX199_MS_ATT0 | 0x400239F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX199_MS_ATT1 | 0x400239F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX199_MS_ATT2 | 0x400239F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX199_MS_ATT3 | 0x400239FC | FULL | Master attributes 3 |

## 23.217 PPU_FX 200

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX200_SL_ADDR | 0x40023A00 | FULL | Slave region, base address |
| PERI_MS_PPU_FX200_SL_SIZE | 0x40023A04 | FULL | Slave region, size |
| PERI_MS_PPU_FX200_SL_ATT0 | 0x40023A10 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX200_SL_ATT1 | 0x40023A14 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX200_SL_ATT2 | 0x40023A18 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX200_SL_ATT3 | 0x40023A1C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX200_MS_ADDR | 0x40023A20 | FULL | Master region, base address |
| PERI_MS_PPU_FX200_MS_SIZE | 0x40023A24 | FULL | Master region, size |
| PERI_MS_PPU_FX200_MS_ATT0 | 0x40023A30 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX200_MS_ATT1 | 0x40023A34 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX200_MS_ATT2 | 0x40023A38 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX200_MS_ATT3 | 0x40023A3C | FULL | Master attributes 3 |

## 23.218 PPU_FX 201

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX201_SL_ADDR | 0x40023A40 | FULL | Slave region, base address |
| PERI_MS_PPU_FX201_SL_SIZE | 0x40023A44 | FULL | Slave region, size |
| PERI_MS_PPU_FX201_SL_ATT0 | 0x40023A50 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX201_SL_ATT1 | 0x40023A54 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX201_SL_ATT2 | 0x40023A58 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX201_SL_ATT3 | 0x40023A5C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX201_MS_ADDR | 0x40023A60 | FULL | Master region, base address |
| PERI_MS_PPU_FX201_MS_SIZE | 0x40023A64 | FULL | Master region, size |
| PERI_MS_PPU_FX201_MS_ATT0 | 0x40023A70 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX201_MS_ATT1 | 0x40023A74 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX201_MS_ATT2 | 0x40023A78 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX201_MS_ATT3 | 0x40023A7C | FULL | Master attributes 3 |

## 23.219 PPU_FX 202

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX202_SL_ADDR | 0x40023A80 | FULL | Slave region, base address |
| PERI_MS_PPU_FX202_SL_SIZE | 0x40023A84 | FULL | Slave region, size |
| PERI_MS_PPU_FX202_SL_ATT0 | 0x40023A90 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX202_SL_ATT1 | 0x40023A94 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX202_SL_ATT2 | 0x40023A98 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX202_SL_ATT3 | 0x40023A9C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX202_MS_ADDR | 0x40023AA0 | FULL | Master region, base address |
| PERI_MS_PPU_FX202_MS_SIZE | 0x40023AA4 | FULL | Master region, size |
| PERI_MS_PPU_FX202_MS_ATT0 | 0x40023AB0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX202_MS_ATT1 | 0x40023AB4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX202_MS_ATT2 | 0x40023AB8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX202_MS_ATT3 | 0x40023ABC | FULL | Master attributes 3 |

## 23.220 PPU_FX 203

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX203_SL_ADDR | 0x40023AC0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX203_SL_SIZE | 0x40023AC4 | FULL | Slave region, size |
| PERI_MS_PPU_FX203_SL_ATT0 | 0x40023AD0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX203_SL_ATT1 | 0x40023AD4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX203_SL_ATT2 | 0x40023AD8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX203_SL_ATT3 | 0x40023ADC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX203_MS_ADDR | 0x40023AE0 | FULL | Master region, base address |
| PERI_MS_PPU_FX203_MS_SIZE | 0x40023AE4 | FULL | Master region, size |
| PERI_MS_PPU_FX203_MS_ATT0 | 0x40023AF0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX203_MS_ATT1 | 0x40023AF4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX203_MS_ATT2 | 0x40023AF8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX203_MS_ATT3 | 0x40023AFC | FULL | Master attributes 3 |

## 23.221 PPU_FX 204

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX204_SL_ADDR | 0x40023B00 | FULL | Slave region, base address |
| PERI_MS_PPU_FX204_SL_SIZE | 0x40023B04 | FULL | Slave region, size |
| PERI_MS_PPU_FX204_SL_ATT0 | 0x40023B10 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX204_SL_ATT1 | 0x40023B14 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX204_SL_ATT2 | 0x40023B18 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX204_SL_ATT3 | 0x40023B1C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX204_MS_ADDR | 0x40023B20 | FULL | Master region, base address |
| PERI_MS_PPU_FX204_MS_SIZE | 0x40023B24 | FULL | Master region, size |
| PERI_MS_PPU_FX204_MS_ATT0 | 0x40023B30 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX204_MS_ATT1 | 0x40023B34 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX204_MS_ATT2 | 0x40023B38 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX204_MS_ATT3 | 0x40023B3C | FULL | Master attributes 3 |

## 23.222 PPU_FX 205

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX205_SL_ADDR | 0x40023B40 | FULL | Slave region, base address |
| PERI_MS_PPU_FX205_SL_SIZE | 0x40023B44 | FULL | Slave region, size |
| PERI_MS_PPU_FX205_SL_ATT0 | 0x40023B50 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX205_SL_ATT1 | 0x40023B54 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX205_SL_ATT2 | 0x40023B58 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX205_SL_ATT3 | 0x40023B5C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX205_MS_ADDR | 0x40023B60 | FULL | Master region, base address |
| PERI_MS_PPU_FX205_MS_SIZE | 0x40023B64 | FULL | Master region, size |
| PERI_MS_PPU_FX205_MS_ATT0 | 0x40023B70 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX205_MS_ATT1 | 0x40023B74 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX205_MS_ATT2 | 0x40023B78 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX205_MS_ATT3 | 0x40023B7C | FULL | Master attributes 3 |

## 23.223 PPU_FX 206

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX206_SL_ADDR | 0x40023B80 | FULL | Slave region, base address |
| PERI_MS_PPU_FX206_SL_SIZE | 0x40023B84 | FULL | Slave region, size |
| PERI_MS_PPU_FX206_SL_ATT0 | 0x40023B90 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX206_SL_ATT1 | 0x40023B94 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX206_SL_ATT2 | 0x40023B98 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX206_SL_ATT3 | 0x40023B9C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX206_MS_ADDR | 0x40023BA0 | FULL | Master region, base address |
| PERI_MS_PPU_FX206_MS_SIZE | 0x40023BA4 | FULL | Master region, size |
| PERI_MS_PPU_FX206_MS_ATT0 | 0x40023BB0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX206_MS_ATT1 | 0x40023BB4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX206_MS_ATT2 | 0x40023BB8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX206_MS_ATT3 | 0x40023BBC | FULL | Master attributes 3 |

## 23.224 PPU_FX 207

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX207_SL_ADDR | 0x40023BC0 | FULL | Slave region, base address |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX207_SL_SIZE | 0x40023BC4 | FULL | Slave region, size |
| PERI_MS_PPU_FX207_SL_ATT0 | 0x40023BD0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX207_SL_ATT1 | 0x40023BD4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX207_SL_ATT2 | 0x40023BD8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX207_SL_ATT3 | 0x40023BDC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX207_MS_ADDR | 0x40023BE0 | FULL | Master region, base address |
| PERI_MS_PPU_FX207_MS_SIZE | 0x40023BE4 | FULL | Master region, size |
| PERI_MS_PPU_FX207_MS_ATT0 | 0x40023BF0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX207_MS_ATT1 | 0x40023BF4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX207_MS_ATT2 | 0x40023BF8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX207_MS_ATT3 | 0x40023BFC | FULL | Master attributes 3 |

## 23.225 PPU_FX 208

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX208_SL_ADDR | 0x40023C00 | FULL | Slave region, base address |
| PERI_MS_PPU_FX208_SL_SIZE | 0x40023C04 | FULL | Slave region, size |
| PERI_MS_PPU_FX208_SL_ATT0 | 0x40023C10 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX208_SL_ATT1 | 0x40023C14 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX208_SL_ATT2 | 0x40023C18 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX208_SL_ATT3 | 0x40023C1C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX208_MS_ADDR | 0x40023C20 | FULL | Master region, base address |
| PERI_MS_PPU_FX208_MS_SIZE | 0x40023C24 | FULL | Master region, size |
| PERI_MS_PPU_FX208_MS_ATT0 | 0x40023C30 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX208_MS_ATT1 | 0x40023C34 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX208_MS_ATT2 | 0x40023C38 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX208_MS_ATT3 | 0x40023C3C | FULL | Master attributes 3 |

## 23.226 PPU_FX 209

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX209_SL_ADDR | 0x40023C40 | FULL | Slave region, base address |
| PERI_MS_PPU_FX209_SL_SIZE | 0x40023C44 | FULL | Slave region, size |
| PERI_MS_PPU_FX209_SL_ATT0 | 0x40023C50 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX209_SL_ATT1 | 0x40023C54 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX209_SL_ATT2 | 0x40023C58 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX209_SL_ATT3 | 0x40023C5C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX209_MS_ADDR | 0x40023C60 | FULL | Master region, base address |
| PERI_MS_PPU_FX209_MS_SIZE | 0x40023C64 | FULL | Master region, size |
| PERI_MS_PPU_FX209_MS_ATT0 | 0x40023C70 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX209_MS_ATT1 | 0x40023C74 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX209_MS_ATT2 | 0x40023C78 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX209_MS_ATT3 | 0x40023C7C | FULL | Master attributes 3 |

## 23.227 PPU_FX 210

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX210_SL_ADDR | 0x40023C80 | FULL | Slave region, base address |
| PERI_MS_PPU_FX210_SL_SIZE | 0x40023C84 | FULL | Slave region, size |
| PERI_MS_PPU_FX210_SL_ATT0 | 0x40023C90 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX210_SL_ATT1 | 0x40023C94 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX210_SL_ATT2 | 0x40023C98 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX210_SL_ATT3 | 0x40023C9C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX210_MS_ADDR | 0x40023CA0 | FULL | Master region, base address |
| PERI_MS_PPU_FX210_MS_SIZE | 0x40023CA4 | FULL | Master region, size |
| PERI_MS_PPU_FX210_MS_ATT0 | 0x40023CB0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX210_MS_ATT1 | 0x40023CB4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX210_MS_ATT2 | 0x40023CB8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX210_MS_ATT3 | 0x40023CBC | FULL | Master attributes 3 |

## 23.228 PPU_FX 211

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX211_SL_ADDR | 0x40023CC0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX211_SL_SIZE | 0x40023CC4 | FULL | Slave region, size |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX211_SL_ATT0 | 0x40023CD0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX211_SL_ATT1 | 0x40023CD4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX211_SL_ATT2 | 0x40023CD8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX211_SL_ATT3 | 0x40023CDC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX211_MS_ADDR | 0x40023CE0 | FULL | Master region, base address |
| PERI_MS_PPU_FX211_MS_SIZE | 0x40023CE4 | FULL | Master region, size |
| PERI_MS_PPU_FX211_MS_ATT0 | 0x40023CF0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX211_MS_ATT1 | 0x40023CF4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX211_MS_ATT2 | 0x40023CF8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX211_MS_ATT3 | 0x40023CFC | FULL | Master attributes 3 |

## 23.229 PPU_FX 212

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX212_SL_ADDR | 0x40023D00 | FULL | Slave region, base address |
| PERI_MS_PPU_FX212_SL_SIZE | 0x40023D04 | FULL | Slave region, size |
| PERI_MS_PPU_FX212_SL_ATT0 | 0x40023D10 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX212_SL_ATT1 | 0x40023D14 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX212_SL_ATT2 | 0x40023D18 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX212_SL_ATT3 | 0x40023D1C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX212_MS_ADDR | 0x40023D20 | FULL | Master region, base address |
| PERI_MS_PPU_FX212_MS_SIZE | 0x40023D24 | FULL | Master region, size |
| PERI_MS_PPU_FX212_MS_ATT0 | 0x40023D30 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX212_MS_ATT1 | 0x40023D34 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX212_MS_ATT2 | 0x40023D38 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX212_MS_ATT3 | 0x40023D3C | FULL | Master attributes 3 |

## 23.230 PPU_FX 213

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX213_SL_ADDR | 0x40023D40 | FULL | Slave region, base address |
| PERI_MS_PPU_FX213_SL_SIZE | 0x40023D44 | FULL | Slave region, size |
| PERI_MS_PPU_FX213_SL_ATT0 | 0x40023D50 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX213_SL_ATT1 | 0x40023D54 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX213_SL_ATT2 | 0x40023D58 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX213_SL_ATT3 | 0x40023D5C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX213_MS_ADDR | 0x40023D60 | FULL | Master region, base address |
| PERI_MS_PPU_FX213_MS_SIZE | 0x40023D64 | FULL | Master region, size |
| PERI_MS_PPU_FX213_MS_ATT0 | 0x40023D70 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX213_MS_ATT1 | 0x40023D74 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX213_MS_ATT2 | 0x40023D78 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX213_MS_ATT3 | 0x40023D7C | FULL | Master attributes 3 |

## 23.231 PPU_FX 214

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX214_SL_ADDR | 0x40023D80 | FULL | Slave region, base address |
| PERI_MS_PPU_FX214_SL_SIZE | 0x40023D84 | FULL | Slave region, size |
| PERI_MS_PPU_FX214_SL_ATT0 | 0x40023D90 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX214_SL_ATT1 | 0x40023D94 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX214_SL_ATT2 | 0x40023D98 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX214_SL_ATT3 | 0x40023D9C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX214_MS_ADDR | 0x40023DA0 | FULL | Master region, base address |
| PERI_MS_PPU_FX214_MS_SIZE | 0x40023DA4 | FULL | Master region, size |
| PERI_MS_PPU_FX214_MS_ATT0 | 0x40023DB0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX214_MS_ATT1 | 0x40023DB4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX214_MS_ATT2 | 0x40023DB8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX214_MS_ATT3 | 0x40023DBC | FULL | Master attributes 3 |

## 23.232 PPU_FX 215

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX215_SL_ADDR | 0x40023DC0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX215_SL_SIZE | 0x40023DC4 | FULL | Slave region, size |
| PERI_MS_PPU_FX215_SL_ATT0 | 0x40023DD0 | FULL | Slave attributes 0 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX215_SL_ATT1 | 0x40023DD4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX215_SL_ATT2 | 0x40023DD8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX215_SL_ATT3 | 0x40023DDC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX215_MS_ADDR | 0x40023DE0 | FULL | Master region, base address |
| PERI_MS_PPU_FX215_MS_SIZE | 0x40023DE4 | FULL | Master region, size |
| PERI_MS_PPU_FX215_MS_ATT0 | 0x40023DF0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX215_MS_ATT1 | 0x40023DF4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX215_MS_ATT2 | 0x40023DF8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX215_MS_ATT3 | 0x40023DFC | FULL | Master attributes 3 |

## 23.233 PPU_FX 216

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX216_SL_ADDR | 0x40023E00 | FULL | Slave region, base address |
| PERI_MS_PPU_FX216_SL_SIZE | 0x40023E04 | FULL | Slave region, size |
| PERI_MS_PPU_FX216_SL_ATT0 | 0x40023E10 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX216_SL_ATT1 | 0x40023E14 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX216_SL_ATT2 | 0x40023E18 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX216_SL_ATT3 | 0x40023E1C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX216_MS_ADDR | 0x40023E20 | FULL | Master region, base address |
| PERI_MS_PPU_FX216_MS_SIZE | 0x40023E24 | FULL | Master region, size |
| PERI_MS_PPU_FX216_MS_ATT0 | 0x40023E30 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX216_MS_ATT1 | 0x40023E34 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX216_MS_ATT2 | 0x40023E38 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX216_MS_ATT3 | 0x40023E3C | FULL | Master attributes 3 |

## 23.234 PPU_FX 217

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX217_SL_ADDR | 0x40023E40 | FULL | Slave region, base address |
| PERI_MS_PPU_FX217_SL_SIZE | 0x40023E44 | FULL | Slave region, size |
| PERI_MS_PPU_FX217_SL_ATT0 | 0x40023E50 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX217_SL_ATT1 | 0x40023E54 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX217_SL_ATT2 | 0x40023E58 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX217_SL_ATT3 | 0x40023E5C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX217_MS_ADDR | 0x40023E60 | FULL | Master region, base address |
| PERI_MS_PPU_FX217_MS_SIZE | 0x40023E64 | FULL | Master region, size |
| PERI_MS_PPU_FX217_MS_ATT0 | 0x40023E70 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX217_MS_ATT1 | 0x40023E74 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX217_MS_ATT2 | 0x40023E78 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX217_MS_ATT3 | 0x40023E7C | FULL | Master attributes 3 |

## 23.235 PPU_FX 218

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX218_SL_ADDR | 0x40023E80 | FULL | Slave region, base address |
| PERI_MS_PPU_FX218_SL_SIZE | 0x40023E84 | FULL | Slave region, size |
| PERI_MS_PPU_FX218_SL_ATT0 | 0x40023E90 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX218_SL_ATT1 | 0x40023E94 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX218_SL_ATT2 | 0x40023E98 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX218_SL_ATT3 | 0x40023E9C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX218_MS_ADDR | 0x40023EA0 | FULL | Master region, base address |
| PERI_MS_PPU_FX218_MS_SIZE | 0x40023EA4 | FULL | Master region, size |
| PERI_MS_PPU_FX218_MS_ATT0 | 0x40023EB0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX218_MS_ATT1 | 0x40023EB4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX218_MS_ATT2 | 0x40023EB8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX218_MS_ATT3 | 0x40023EBC | FULL | Master attributes 3 |

## 23.236 PPU_FX 219

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX219_SL_ADDR | 0x40023EC0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX219_SL_SIZE | 0x40023EC4 | FULL | Slave region, size |
| PERI_MS_PPU_FX219_SL_ATT0 | 0x40023ED0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX219_SL_ATT1 | 0x40023ED4 | FULL | Slave attributes 1 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX219_SL_ATT2 | 0x40023ED8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX219_SL_ATT3 | 0x40023EDC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX219_MS_ADDR | 0x40023EE0 | FULL | Master region, base address |
| PERI_MS_PPU_FX219_MS_SIZE | 0x40023EE4 | FULL | Master region, size |
| PERI_MS_PPU_FX219_MS_ATT0 | 0x40023EF0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX219_MS_ATT1 | 0x40023EF4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX219_MS_ATT2 | 0x40023EF8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX219_MS_ATT3 | 0x40023EFC | FULL | Master attributes 3 |

## 23.237 PPU_FX 220

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX220_SL_ADDR | 0x40023F00 | FULL | Slave region, base address |
| PERI_MS_PPU_FX220_SL_SIZE | 0x40023F04 | FULL | Slave region, size |
| PERI_MS_PPU_FX220_SL_ATT0 | 0x40023F10 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX220_SL_ATT1 | 0x40023F14 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX220_SL_ATT2 | 0x40023F18 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX220_SL_ATT3 | 0x40023F1C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX220_MS_ADDR | 0x40023F20 | FULL | Master region, base address |
| PERI_MS_PPU_FX220_MS_SIZE | 0x40023F24 | FULL | Master region, size |
| PERI_MS_PPU_FX220_MS_ATT0 | 0x40023F30 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX220_MS_ATT1 | 0x40023F34 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX220_MS_ATT2 | 0x40023F38 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX220_MS_ATT3 | 0x40023F3C | FULL | Master attributes 3 |

## 23.238 PPU_FX 221

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX221_SL_ADDR | 0x40023F40 | FULL | Slave region, base address |
| PERI_MS_PPU_FX221_SL_SIZE | 0x40023F44 | FULL | Slave region, size |
| PERI_MS_PPU_FX221_SL_ATT0 | 0x40023F50 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX221_SL_ATT1 | 0x40023F54 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX221_SL_ATT2 | 0x40023F58 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX221_SL_ATT3 | 0x40023F5C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX221_MS_ADDR | 0x40023F60 | FULL | Master region, base address |
| PERI_MS_PPU_FX221_MS_SIZE | 0x40023F64 | FULL | Master region, size |
| PERI_MS_PPU_FX221_MS_ATT0 | 0x40023F70 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX221_MS_ATT1 | 0x40023F74 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX221_MS_ATT2 | 0x40023F78 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX221_MS_ATT3 | 0x40023F7C | FULL | Master attributes 3 |

## 23.239 PPU_FX 222

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX222_SL_ADDR | 0x40023F80 | FULL | Slave region, base address |
| PERI_MS_PPU_FX222_SL_SIZE | 0x40023F84 | FULL | Slave region, size |
| PERI_MS_PPU_FX222_SL_ATT0 | 0x40023F90 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX222_SL_ATT1 | 0x40023F94 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX222_SL_ATT2 | 0x40023F98 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX222_SL_ATT3 | 0x40023F9C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX222_MS_ADDR | 0x40023FA0 | FULL | Master region, base address |
| PERI_MS_PPU_FX222_MS_SIZE | 0x40023FA4 | FULL | Master region, size |
| PERI_MS_PPU_FX222_MS_ATT0 | 0x40023FB0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX222_MS_ATT1 | 0x40023FB4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX222_MS_ATT2 | 0x40023FB8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX222_MS_ATT3 | 0x40023FBC | FULL | Master attributes 3 |

## 23.240 PPU_FX 223

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX223_SL_ADDR | 0x40023FC0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX223_SL_SIZE | 0x40023FC4 | FULL | Slave region, size |
| PERI_MS_PPU_FX223_SL_ATT0 | 0x40023FD0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX223_SL_ATT1 | 0x40023FD4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX223_SL_ATT2 | 0x40023FD8 | FULL | Slave attributes 2 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX223_SL_ATT3 | 0x40023FDC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX223_MS_ADDR | 0x40023FE0 | FULL | Master region, base address |
| PERI_MS_PPU_FX223_MS_SIZE | 0x40023FE4 | FULL | Master region, size |
| PERI_MS_PPU_FX223_MS_ATT0 | 0x40023FF0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX223_MS_ATT1 | 0x40023FF4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX223_MS_ATT2 | 0x40023FF8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX223_MS_ATT3 | 0x40023FFC | FULL | Master attributes 3 |

## 23.241 PPU_FX 224

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX224_SL_ADDR | 0x40024000 | FULL | Slave region, base address |
| PERI_MS_PPU_FX224_SL_SIZE | 0x40024004 | FULL | Slave region, size |
| PERI_MS_PPU_FX224_SL_ATT0 | 0x40024010 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX224_SL_ATT1 | 0x40024014 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX224_SL_ATT2 | 0x40024018 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX224_SL_ATT3 | 0x4002401C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX224_MS_ADDR | 0x40024020 | FULL | Master region, base address |
| PERI_MS_PPU_FX224_MS_SIZE | 0x40024024 | FULL | Master region, size |
| PERI_MS_PPU_FX224_MS_ATT0 | 0x40024030 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX224_MS_ATT1 | 0x40024034 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX224_MS_ATT2 | 0x40024038 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX224_MS_ATT3 | 0x4002403C | FULL | Master attributes 3 |

## 23.242 PPU_FX 225

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX225_SL_ADDR | 0x40024040 | FULL | Slave region, base address |
| PERI_MS_PPU_FX225_SL_SIZE | 0x40024044 | FULL | Slave region, size |
| PERI_MS_PPU_FX225_SL_ATT0 | 0x40024050 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX225_SL_ATT1 | 0x40024054 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX225_SL_ATT2 | 0x40024058 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX225_SL_ATT3 | 0x4002405C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX225_MS_ADDR | 0x40024060 | FULL | Master region, base address |
| PERI_MS_PPU_FX225_MS_SIZE | 0x40024064 | FULL | Master region, size |
| PERI_MS_PPU_FX225_MS_ATT0 | 0x40024070 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX225_MS_ATT1 | 0x40024074 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX225_MS_ATT2 | 0x40024078 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX225_MS_ATT3 | 0x4002407C | FULL | Master attributes 3 |

## 23.243 PPU_FX 226

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX226_SL_ADDR | 0x40024080 | FULL | Slave region, base address |
| PERI_MS_PPU_FX226_SL_SIZE | 0x40024084 | FULL | Slave region, size |
| PERI_MS_PPU_FX226_SL_ATT0 | 0x40024090 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX226_SL_ATT1 | 0x40024094 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX226_SL_ATT2 | 0x40024098 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX226_SL_ATT3 | 0x4002409C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX226_MS_ADDR | 0x400240A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX226_MS_SIZE | 0x400240A4 | FULL | Master region, size |
| PERI_MS_PPU_FX226_MS_ATT0 | 0x400240B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX226_MS_ATT1 | 0x400240B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX226_MS_ATT2 | 0x400240B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX226_MS_ATT3 | 0x400240BC | FULL | Master attributes 3 |

## 23.244 PPU_FX 227

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX227_SL_ADDR | 0x400240C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX227_SL_SIZE | 0x400240C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX227_SL_ATT0 | 0x400240D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX227_SL_ATT1 | 0x400240D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX227_SL_ATT2 | 0x400240D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX227_SL_ATT3 | 0x400240DC | FULL | Slave attributes 3 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX227_MS_ADDR | 0x400240E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX227_MS_SIZE | 0x400240E4 | FULL | Master region, size |
| PERI_MS_PPU_FX227_MS_ATT0 | 0x400240F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX227_MS_ATT1 | 0x400240F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX227_MS_ATT2 | 0x400240F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX227_MS_ATT3 | 0x400240FC | FULL | Master attributes 3 |

## 23.245 PPU_FX 228

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX228_SL_ADDR | 0x40024100 | FULL | Slave region, base address |
| PERI_MS_PPU_FX228_SL_SIZE | 0x40024104 | FULL | Slave region, size |
| PERI_MS_PPU_FX228_SL_ATT0 | 0x40024110 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX228_SL_ATT1 | 0x40024114 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX228_SL_ATT2 | 0x40024118 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX228_SL_ATT3 | 0x4002411C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX228_MS_ADDR | 0x40024120 | FULL | Master region, base address |
| PERI_MS_PPU_FX228_MS_SIZE | 0x40024124 | FULL | Master region, size |
| PERI_MS_PPU_FX228_MS_ATT0 | 0x40024130 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX228_MS_ATT1 | 0x40024134 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX228_MS_ATT2 | 0x40024138 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX228_MS_ATT3 | 0x4002413C | FULL | Master attributes 3 |

## 23.246 PPU_FX 229

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX229_SL_ADDR | 0x40024140 | FULL | Slave region, base address |
| PERI_MS_PPU_FX229_SL_SIZE | 0x40024144 | FULL | Slave region, size |
| PERI_MS_PPU_FX229_SL_ATT0 | 0x40024150 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX229_SL_ATT1 | 0x40024154 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX229_SL_ATT2 | 0x40024158 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX229_SL_ATT3 | 0x4002415C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX229_MS_ADDR | 0x40024160 | FULL | Master region, base address |
| PERI_MS_PPU_FX229_MS_SIZE | 0x40024164 | FULL | Master region, size |
| PERI_MS_PPU_FX229_MS_ATT0 | 0x40024170 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX229_MS_ATT1 | 0x40024174 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX229_MS_ATT2 | 0x40024178 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX229_MS_ATT3 | 0x4002417C | FULL | Master attributes 3 |

## 23.247 PPU_FX 230

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX230_SL_ADDR | 0x40024180 | FULL | Slave region, base address |
| PERI_MS_PPU_FX230_SL_SIZE | 0x40024184 | FULL | Slave region, size |
| PERI_MS_PPU_FX230_SL_ATT0 | 0x40024190 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX230_SL_ATT1 | 0x40024194 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX230_SL_ATT2 | 0x40024198 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX230_SL_ATT3 | 0x4002419C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX230_MS_ADDR | 0x400241A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX230_MS_SIZE | 0x400241A4 | FULL | Master region, size |
| PERI_MS_PPU_FX230_MS_ATT0 | 0x400241B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX230_MS_ATT1 | 0x400241B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX230_MS_ATT2 | 0x400241B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX230_MS_ATT3 | 0x400241BC | FULL | Master attributes 3 |

## 23.248 PPU_FX 231

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX231_SL_ADDR | 0x400241C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX231_SL_SIZE | 0x400241C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX231_SL_ATT0 | 0x400241D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX231_SL_ATT1 | 0x400241D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX231_SL_ATT2 | 0x400241D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX231_SL_ATT3 | 0x400241DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX231_MS_ADDR | 0x400241E0 | FULL | Master region, base address |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX231_MS_SIZE | 0x400241E4 | FULL | Master region, size |
| PERI_MS_PPU_FX231_MS_ATT0 | 0x400241F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX231_MS_ATT1 | 0x400241F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX231_MS_ATT2 | 0x400241F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX231_MS_ATT3 | 0x400241FC | FULL | Master attributes 3 |

## 23.249 PPU_FX 232

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX232_SL_ADDR | 0x40024200 | FULL | Slave region, base address |
| PERI_MS_PPU_FX232_SL_SIZE | 0x40024204 | FULL | Slave region, size |
| PERI_MS_PPU_FX232_SL_ATT0 | 0x40024210 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX232_SL_ATT1 | 0x40024214 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX232_SL_ATT2 | 0x40024218 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX232_SL_ATT3 | 0x4002421C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX232_MS_ADDR | 0x40024220 | FULL | Master region, base address |
| PERI_MS_PPU_FX232_MS_SIZE | 0x40024224 | FULL | Master region, size |
| PERI_MS_PPU_FX232_MS_ATT0 | 0x40024230 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX232_MS_ATT1 | 0x40024234 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX232_MS_ATT2 | 0x40024238 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX232_MS_ATT3 | 0x4002423C | FULL | Master attributes 3 |

## 23.250 PPU_FX 233

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX233_SL_ADDR | 0x40024240 | FULL | Slave region, base address |
| PERI_MS_PPU_FX233_SL_SIZE | 0x40024244 | FULL | Slave region, size |
| PERI_MS_PPU_FX233_SL_ATT0 | 0x40024250 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX233_SL_ATT1 | 0x40024254 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX233_SL_ATT2 | 0x40024258 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX233_SL_ATT3 | 0x4002425C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX233_MS_ADDR | 0x40024260 | FULL | Master region, base address |
| PERI_MS_PPU_FX233_MS_SIZE | 0x40024264 | FULL | Master region, size |
| PERI_MS_PPU_FX233_MS_ATT0 | 0x40024270 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX233_MS_ATT1 | 0x40024274 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX233_MS_ATT2 | 0x40024278 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX233_MS_ATT3 | 0x4002427C | FULL | Master attributes 3 |

## 23.251 PPU_FX 234

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX234_SL_ADDR | 0x40024280 | FULL | Slave region, base address |
| PERI_MS_PPU_FX234_SL_SIZE | 0x40024284 | FULL | Slave region, size |
| PERI_MS_PPU_FX234_SL_ATT0 | 0x40024290 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX234_SL_ATT1 | 0x40024294 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX234_SL_ATT2 | 0x40024298 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX234_SL_ATT3 | 0x4002429C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX234_MS_ADDR | 0x400242A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX234_MS_SIZE | 0x400242A4 | FULL | Master region, size |
| PERI_MS_PPU_FX234_MS_ATT0 | 0x400242B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX234_MS_ATT1 | 0x400242B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX234_MS_ATT2 | 0x400242B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX234_MS_ATT3 | 0x400242BC | FULL | Master attributes 3 |

## 23.252 PPU_FX 235

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX235_SL_ADDR | 0x400242C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX235_SL_SIZE | 0x400242C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX235_SL_ATT0 | 0x400242D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX235_SL_ATT1 | 0x400242D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX235_SL_ATT2 | 0x400242D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX235_SL_ATT3 | 0x400242DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX235_MS_ADDR | 0x400242E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX235_MS_SIZE | 0x400242E4 | FULL | Master region, size |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX235_MS_ATT0 | 0x400242F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX235_MS_ATT1 | 0x400242F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX235_MS_ATT2 | 0x400242F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX235_MS_ATT3 | 0x400242FC | FULL | Master attributes 3 |

## 23.253 PPU_FX 236

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX236_SL_ADDR | 0x40024300 | FULL | Slave region, base address |
| PERI_MS_PPU_FX236_SL_SIZE | 0x40024304 | FULL | Slave region, size |
| PERI_MS_PPU_FX236_SL_ATT0 | 0x40024310 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX236_SL_ATT1 | 0x40024314 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX236_SL_ATT2 | 0x40024318 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX236_SL_ATT3 | 0x4002431C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX236_MS_ADDR | 0x40024320 | FULL | Master region, base address |
| PERI_MS_PPU_FX236_MS_SIZE | 0x40024324 | FULL | Master region, size |
| PERI_MS_PPU_FX236_MS_ATT0 | 0x40024330 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX236_MS_ATT1 | 0x40024334 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX236_MS_ATT2 | 0x40024338 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX236_MS_ATT3 | 0x4002433C | FULL | Master attributes 3 |

## 23.254 PPU_FX 237

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX237_SL_ADDR | 0x40024340 | FULL | Slave region, base address |
| PERI_MS_PPU_FX237_SL_SIZE | 0x40024344 | FULL | Slave region, size |
| PERI_MS_PPU_FX237_SL_ATT0 | 0x40024350 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX237_SL_ATT1 | 0x40024354 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX237_SL_ATT2 | 0x40024358 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX237_SL_ATT3 | 0x4002435C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX237_MS_ADDR | 0x40024360 | FULL | Master region, base address |
| PERI_MS_PPU_FX237_MS_SIZE | 0x40024364 | FULL | Master region, size |
| PERI_MS_PPU_FX237_MS_ATT0 | 0x40024370 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX237_MS_ATT1 | 0x40024374 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX237_MS_ATT2 | 0x40024378 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX237_MS_ATT3 | 0x4002437C | FULL | Master attributes 3 |

## 23.255 PPU_FX 238

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX238_SL_ADDR | 0x40024380 | FULL | Slave region, base address |
| PERI_MS_PPU_FX238_SL_SIZE | 0x40024384 | FULL | Slave region, size |
| PERI_MS_PPU_FX238_SL_ATT0 | 0x40024390 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX238_SL_ATT1 | 0x40024394 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX238_SL_ATT2 | 0x40024398 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX238_SL_ATT3 | 0x4002439C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX238_MS_ADDR | 0x400243A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX238_MS_SIZE | 0x400243A4 | FULL | Master region, size |
| PERI_MS_PPU_FX238_MS_ATT0 | 0x400243B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX238_MS_ATT1 | 0x400243B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX238_MS_ATT2 | 0x400243B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX238_MS_ATT3 | 0x400243BC | FULL | Master attributes 3 |

## 23.256 PPU_FX 239

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX239_SL_ADDR | 0x400243C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX239_SL_SIZE | 0x400243C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX239_SL_ATT0 | 0x400243D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX239_SL_ATT1 | 0x400243D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX239_SL_ATT2 | 0x400243D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX239_SL_ATT3 | 0x400243DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX239_MS_ADDR | 0x400243E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX239_MS_SIZE | 0x400243E4 | FULL | Master region, size |
| PERI_MS_PPU_FX239_MS_ATT0 | 0x400243F0 | FULL | Master attributes 0 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX239_MS_ATT1 | 0x400243F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX239_MS_ATT2 | 0x400243F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX239_MS_ATT3 | 0x400243FC | FULL | Master attributes 3 |

## 23.257 PPU_FX 240

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX240_SL_ADDR | 0x40024400 | FULL | Slave region, base address |
| PERI_MS_PPU_FX240_SL_SIZE | 0x40024404 | FULL | Slave region, size |
| PERI_MS_PPU_FX240_SL_ATT0 | 0x40024410 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX240_SL_ATT1 | 0x40024414 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX240_SL_ATT2 | 0x40024418 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX240_SL_ATT3 | 0x4002441C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX240_MS_ADDR | 0x40024420 | FULL | Master region, base address |
| PERI_MS_PPU_FX240_MS_SIZE | 0x40024424 | FULL | Master region, size |
| PERI_MS_PPU_FX240_MS_ATT0 | 0x40024430 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX240_MS_ATT1 | 0x40024434 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX240_MS_ATT2 | 0x40024438 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX240_MS_ATT3 | 0x4002443C | FULL | Master attributes 3 |

## 23.258 PPU_FX 241

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX241_SL_ADDR | 0x40024440 | FULL | Slave region, base address |
| PERI_MS_PPU_FX241_SL_SIZE | 0x40024444 | FULL | Slave region, size |
| PERI_MS_PPU_FX241_SL_ATT0 | 0x40024450 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX241_SL_ATT1 | 0x40024454 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX241_SL_ATT2 | 0x40024458 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX241_SL_ATT3 | 0x4002445C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX241_MS_ADDR | 0x40024460 | FULL | Master region, base address |
| PERI_MS_PPU_FX241_MS_SIZE | 0x40024464 | FULL | Master region, size |
| PERI_MS_PPU_FX241_MS_ATT0 | 0x40024470 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX241_MS_ATT1 | 0x40024474 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX241_MS_ATT2 | 0x40024478 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX241_MS_ATT3 | 0x4002447C | FULL | Master attributes 3 |

## 23.259 PPU_FX 242

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX242_SL_ADDR | 0x40024480 | FULL | Slave region, base address |
| PERI_MS_PPU_FX242_SL_SIZE | 0x40024484 | FULL | Slave region, size |
| PERI_MS_PPU_FX242_SL_ATT0 | 0x40024490 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX242_SL_ATT1 | 0x40024494 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX242_SL_ATT2 | 0x40024498 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX242_SL_ATT3 | 0x4002449C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX242_MS_ADDR | 0x400244A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX242_MS_SIZE | 0x400244A4 | FULL | Master region, size |
| PERI_MS_PPU_FX242_MS_ATT0 | 0x400244B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX242_MS_ATT1 | 0x400244B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX242_MS_ATT2 | 0x400244B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX242_MS_ATT3 | 0x400244BC | FULL | Master attributes 3 |

## 23.260 PPU_FX 243

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX243_SL_ADDR | 0x400244C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX243_SL_SIZE | 0x400244C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX243_SL_ATT0 | 0x400244D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX243_SL_ATT1 | 0x400244D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX243_SL_ATT2 | 0x400244D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX243_SL_ATT3 | 0x400244DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX243_MS_ADDR | 0x400244E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX243_MS_SIZE | 0x400244E4 | FULL | Master region, size |
| PERI_MS_PPU_FX243_MS_ATT0 | 0x400244F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX243_MS_ATT1 | 0x400244F4 | FULL | Master attributes 1 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX243_MS_ATT2 | 0x400244F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX243_MS_ATT3 | 0x400244FC | FULL | Master attributes 3 |

## 23.261 PPU_FX 244

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX244_SL_ADDR | 0x40024500 | FULL | Slave region, base address |
| PERI_MS_PPU_FX244_SL_SIZE | 0x40024504 | FULL | Slave region, size |
| PERI_MS_PPU_FX244_SL_ATT0 | 0x40024510 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX244_SL_ATT1 | 0x40024514 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX244_SL_ATT2 | 0x40024518 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX244_SL_ATT3 | 0x4002451C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX244_MS_ADDR | 0x40024520 | FULL | Master region, base address |
| PERI_MS_PPU_FX244_MS_SIZE | 0x40024524 | FULL | Master region, size |
| PERI_MS_PPU_FX244_MS_ATT0 | 0x40024530 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX244_MS_ATT1 | 0x40024534 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX244_MS_ATT2 | 0x40024538 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX244_MS_ATT3 | 0x4002453C | FULL | Master attributes 3 |

## 23.262 PPU_FX 245

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX245_SL_ADDR | 0x40024540 | FULL | Slave region, base address |
| PERI_MS_PPU_FX245_SL_SIZE | 0x40024544 | FULL | Slave region, size |
| PERI_MS_PPU_FX245_SL_ATT0 | 0x40024550 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX245_SL_ATT1 | 0x40024554 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX245_SL_ATT2 | 0x40024558 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX245_SL_ATT3 | 0x4002455C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX245_MS_ADDR | 0x40024560 | FULL | Master region, base address |
| PERI_MS_PPU_FX245_MS_SIZE | 0x40024564 | FULL | Master region, size |
| PERI_MS_PPU_FX245_MS_ATT0 | 0x40024570 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX245_MS_ATT1 | 0x40024574 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX245_MS_ATT2 | 0x40024578 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX245_MS_ATT3 | 0x4002457C | FULL | Master attributes 3 |

## 23.263 PPU_FX 246

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX246_SL_ADDR | 0x40024580 | FULL | Slave region, base address |
| PERI_MS_PPU_FX246_SL_SIZE | 0x40024584 | FULL | Slave region, size |
| PERI_MS_PPU_FX246_SL_ATT0 | 0x40024590 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX246_SL_ATT1 | 0x40024594 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX246_SL_ATT2 | 0x40024598 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX246_SL_ATT3 | 0x4002459C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX246_MS_ADDR | 0x400245A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX246_MS_SIZE | 0x400245A4 | FULL | Master region, size |
| PERI_MS_PPU_FX246_MS_ATT0 | 0x400245B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX246_MS_ATT1 | 0x400245B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX246_MS_ATT2 | 0x400245B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX246_MS_ATT3 | 0x400245BC | FULL | Master attributes 3 |

## 23.264 PPU_FX 247

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX247_SL_ADDR | 0x400245C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX247_SL_SIZE | 0x400245C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX247_SL_ATT0 | 0x400245D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX247_SL_ATT1 | 0x400245D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX247_SL_ATT2 | 0x400245D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX247_SL_ATT3 | 0x400245DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX247_MS_ADDR | 0x400245E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX247_MS_SIZE | 0x400245E4 | FULL | Master region, size |
| PERI_MS_PPU_FX247_MS_ATT0 | 0x400245F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX247_MS_ATT1 | 0x400245F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX247_MS_ATT2 | 0x400245F8 | FULL | Master attributes 2 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX247_MS_ATT3 | 0x400245FC | FULL | Master attributes 3 |

## 23.265 PPU_FX 248

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX248_SL_ADDR | 0x40024600 | FULL | Slave region, base address |
| PERI_MS_PPU_FX248_SL_SIZE | 0x40024604 | FULL | Slave region, size |
| PERI_MS_PPU_FX248_SL_ATT0 | 0x40024610 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX248_SL_ATT1 | 0x40024614 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX248_SL_ATT2 | 0x40024618 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX248_SL_ATT3 | 0x4002461C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX248_MS_ADDR | 0x40024620 | FULL | Master region, base address |
| PERI_MS_PPU_FX248_MS_SIZE | 0x40024624 | FULL | Master region, size |
| PERI_MS_PPU_FX248_MS_ATT0 | 0x40024630 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX248_MS_ATT1 | 0x40024634 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX248_MS_ATT2 | 0x40024638 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX248_MS_ATT3 | 0x4002463C | FULL | Master attributes 3 |

## 23.266 PPU_FX 249

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX249_SL_ADDR | 0x40024640 | FULL | Slave region, base address |
| PERI_MS_PPU_FX249_SL_SIZE | 0x40024644 | FULL | Slave region, size |
| PERI_MS_PPU_FX249_SL_ATT0 | 0x40024650 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX249_SL_ATT1 | 0x40024654 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX249_SL_ATT2 | 0x40024658 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX249_SL_ATT3 | 0x4002465C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX249_MS_ADDR | 0x40024660 | FULL | Master region, base address |
| PERI_MS_PPU_FX249_MS_SIZE | 0x40024664 | FULL | Master region, size |
| PERI_MS_PPU_FX249_MS_ATT0 | 0x40024670 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX249_MS_ATT1 | 0x40024674 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX249_MS_ATT2 | 0x40024678 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX249_MS_ATT3 | 0x4002467C | FULL | Master attributes 3 |

## 23.267 PPU_FX 250

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX250_SL_ADDR | 0x40024680 | FULL | Slave region, base address |
| PERI_MS_PPU_FX250_SL_SIZE | 0x40024684 | FULL | Slave region, size |
| PERI_MS_PPU_FX250_SL_ATT0 | 0x40024690 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX250_SL_ATT1 | 0x40024694 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX250_SL_ATT2 | 0x40024698 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX250_SL_ATT3 | 0x4002469C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX250_MS_ADDR | 0x400246A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX250_MS_SIZE | 0x400246A4 | FULL | Master region, size |
| PERI_MS_PPU_FX250_MS_ATT0 | 0x400246B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX250_MS_ATT1 | 0x400246B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX250_MS_ATT2 | 0x400246B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX250_MS_ATT3 | 0x400246BC | FULL | Master attributes 3 |

## 23.268 PPU_FX 251

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX251_SL_ADDR | 0x400246C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX251_SL_SIZE | 0x400246C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX251_SL_ATT0 | 0x400246D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX251_SL_ATT1 | 0x400246D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX251_SL_ATT2 | 0x400246D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX251_SL_ATT3 | 0x400246DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX251_MS_ADDR | 0x400246E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX251_MS_SIZE | 0x400246E4 | FULL | Master region, size |
| PERI_MS_PPU_FX251_MS_ATT0 | 0x400246F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX251_MS_ATT1 | 0x400246F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX251_MS_ATT2 | 0x400246F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX251_MS_ATT3 | 0x400246FC | FULL | Master attributes 3 |

## 23.269 PPU_FX 252

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX252_SL_ADDR | 0x40024700 | FULL | Slave region, base address |
| PERI_MS_PPU_FX252_SL_SIZE | 0x40024704 | FULL | Slave region, size |
| PERI_MS_PPU_FX252_SL_ATT0 | 0x40024710 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX252_SL_ATT1 | 0x40024714 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX252_SL_ATT2 | 0x40024718 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX252_SL_ATT3 | 0x4002471C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX252_MS_ADDR | 0x40024720 | FULL | Master region, base address |
| PERI_MS_PPU_FX252_MS_SIZE | 0x40024724 | FULL | Master region, size |
| PERI_MS_PPU_FX252_MS_ATT0 | 0x40024730 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX252_MS_ATT1 | 0x40024734 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX252_MS_ATT2 | 0x40024738 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX252_MS_ATT3 | 0x4002473C | FULL | Master attributes 3 |

## 23.270 PPU_FX 253

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX253_SL_ADDR | 0x40024740 | FULL | Slave region, base address |
| PERI_MS_PPU_FX253_SL_SIZE | 0x40024744 | FULL | Slave region, size |
| PERI_MS_PPU_FX253_SL_ATT0 | 0x40024750 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX253_SL_ATT1 | 0x40024754 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX253_SL_ATT2 | 0x40024758 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX253_SL_ATT3 | 0x4002475C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX253_MS_ADDR | 0x40024760 | FULL | Master region, base address |
| PERI_MS_PPU_FX253_MS_SIZE | 0x40024764 | FULL | Master region, size |
| PERI_MS_PPU_FX253_MS_ATT0 | 0x40024770 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX253_MS_ATT1 | 0x40024774 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX253_MS_ATT2 | 0x40024778 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX253_MS_ATT3 | 0x4002477C | FULL | Master attributes 3 |

## 23.271 PPU_FX 254

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX254_SL_ADDR | 0x40024780 | FULL | Slave region, base address |
| PERI_MS_PPU_FX254_SL_SIZE | 0x40024784 | FULL | Slave region, size |
| PERI_MS_PPU_FX254_SL_ATT0 | 0x40024790 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX254_SL_ATT1 | 0x40024794 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX254_SL_ATT2 | 0x40024798 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX254_SL_ATT3 | 0x4002479C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX254_MS_ADDR | 0x400247A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX254_MS_SIZE | 0x400247A4 | FULL | Master region, size |
| PERI_MS_PPU_FX254_MS_ATT0 | 0x400247B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX254_MS_ATT1 | 0x400247B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX254_MS_ATT2 | 0x400247B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX254_MS_ATT3 | 0x400247BC | FULL | Master attributes 3 |

## 23.272 PPU_FX 255

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX255_SL_ADDR | 0x400247C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX255_SL_SIZE | 0x400247C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX255_SL_ATT0 | 0x400247D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX255_SL_ATT1 | 0x400247D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX255_SL_ATT2 | 0x400247D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX255_SL_ATT3 | 0x400247DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX255_MS_ADDR | 0x400247E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX255_MS_SIZE | 0x400247E4 | FULL | Master region, size |
| PERI_MS_PPU_FX255_MS_ATT0 | 0x400247F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX255_MS_ATT1 | 0x400247F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX255_MS_ATT2 | 0x400247F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX255_MS_ATT3 | 0x400247FC | FULL | Master attributes 3 |

## 23.273 PPU_FX 256

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX256_SL_ADDR | 0x40024800 | FULL | Slave region, base address |
| PERI_MS_PPU_FX256_SL_SIZE | 0x40024804 | FULL | Slave region, size |
| PERI_MS_PPU_FX256_SL_ATT0 | 0x40024810 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX256_SL_ATT1 | 0x40024814 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX256_SL_ATT2 | 0x40024818 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX256_SL_ATT3 | 0x4002481C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX256_MS_ADDR | 0x40024820 | FULL | Master region, base address |
| PERI_MS_PPU_FX256_MS_SIZE | 0x40024824 | FULL | Master region, size |
| PERI_MS_PPU_FX256_MS_ATT0 | 0x40024830 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX256_MS_ATT1 | 0x40024834 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX256_MS_ATT2 | 0x40024838 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX256_MS_ATT3 | 0x4002483C | FULL | Master attributes 3 |

## 23.274 PPU_FX 257

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX257_SL_ADDR | 0x40024840 | FULL | Slave region, base address |
| PERI_MS_PPU_FX257_SL_SIZE | 0x40024844 | FULL | Slave region, size |
| PERI_MS_PPU_FX257_SL_ATT0 | 0x40024850 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX257_SL_ATT1 | 0x40024854 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX257_SL_ATT2 | 0x40024858 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX257_SL_ATT3 | 0x4002485C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX257_MS_ADDR | 0x40024860 | FULL | Master region, base address |
| PERI_MS_PPU_FX257_MS_SIZE | 0x40024864 | FULL | Master region, size |
| PERI_MS_PPU_FX257_MS_ATT0 | 0x40024870 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX257_MS_ATT1 | 0x40024874 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX257_MS_ATT2 | 0x40024878 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX257_MS_ATT3 | 0x4002487C | FULL | Master attributes 3 |

## 23.275 PPU_FX 258

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX258_SL_ADDR | 0x40024880 | FULL | Slave region, base address |
| PERI_MS_PPU_FX258_SL_SIZE | 0x40024884 | FULL | Slave region, size |
| PERI_MS_PPU_FX258_SL_ATT0 | 0x40024890 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX258_SL_ATT1 | 0x40024894 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX258_SL_ATT2 | 0x40024898 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX258_SL_ATT3 | 0x4002489C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX258_MS_ADDR | 0x400248A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX258_MS_SIZE | 0x400248A4 | FULL | Master region, size |
| PERI_MS_PPU_FX258_MS_ATT0 | 0x400248B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX258_MS_ATT1 | 0x400248B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX258_MS_ATT2 | 0x400248B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX258_MS_ATT3 | 0x400248BC | FULL | Master attributes 3 |

## 23.276 PPU_FX 259

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX259_SL_ADDR | 0x400248C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX259_SL_SIZE | 0x400248C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX259_SL_ATT0 | 0x400248D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX259_SL_ATT1 | 0x400248D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX259_SL_ATT2 | 0x400248D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX259_SL_ATT3 | 0x400248DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX259_MS_ADDR | 0x400248E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX259_MS_SIZE | 0x400248E4 | FULL | Master region, size |
| PERI_MS_PPU_FX259_MS_ATT0 | 0x400248F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX259_MS_ATT1 | 0x400248F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX259_MS_ATT2 | 0x400248F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX259_MS_ATT3 | 0x400248FC | FULL | Master attributes 3 |

## 23.277 PPU_FX 260

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX260_SL_ADDR | 0x40024900 | FULL | Slave region, base address |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX260_SL_SIZE | 0x40024904 | FULL | Slave region, size |
| PERI_MS_PPU_FX260_SL_ATT0 | 0x40024910 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX260_SL_ATT1 | 0x40024914 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX260_SL_ATT2 | 0x40024918 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX260_SL_ATT3 | 0x4002491C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX260_MS_ADDR | 0x40024920 | FULL | Master region, base address |
| PERI_MS_PPU_FX260_MS_SIZE | 0x40024924 | FULL | Master region, size |
| PERI_MS_PPU_FX260_MS_ATT0 | 0x40024930 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX260_MS_ATT1 | 0x40024934 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX260_MS_ATT2 | 0x40024938 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX260_MS_ATT3 | 0x4002493C | FULL | Master attributes 3 |

## 23.278 PPU_FX 261

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX261_SL_ADDR | 0x40024940 | FULL | Slave region, base address |
| PERI_MS_PPU_FX261_SL_SIZE | 0x40024944 | FULL | Slave region, size |
| PERI_MS_PPU_FX261_SL_ATT0 | 0x40024950 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX261_SL_ATT1 | 0x40024954 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX261_SL_ATT2 | 0x40024958 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX261_SL_ATT3 | 0x4002495C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX261_MS_ADDR | 0x40024960 | FULL | Master region, base address |
| PERI_MS_PPU_FX261_MS_SIZE | 0x40024964 | FULL | Master region, size |
| PERI_MS_PPU_FX261_MS_ATT0 | 0x40024970 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX261_MS_ATT1 | 0x40024974 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX261_MS_ATT2 | 0x40024978 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX261_MS_ATT3 | 0x4002497C | FULL | Master attributes 3 |

## 23.279 PPU_FX 262

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX262_SL_ADDR | 0x40024980 | FULL | Slave region, base address |
| PERI_MS_PPU_FX262_SL_SIZE | 0x40024984 | FULL | Slave region, size |
| PERI_MS_PPU_FX262_SL_ATT0 | 0x40024990 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX262_SL_ATT1 | 0x40024994 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX262_SL_ATT2 | 0x40024998 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX262_SL_ATT3 | 0x4002499C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX262_MS_ADDR | 0x400249A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX262_MS_SIZE | 0x400249A4 | FULL | Master region, size |
| PERI_MS_PPU_FX262_MS_ATT0 | 0x400249B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX262_MS_ATT1 | 0x400249B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX262_MS_ATT2 | 0x400249B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX262_MS_ATT3 | 0x400249BC | FULL | Master attributes 3 |

## 23.280 PPU_FX 263

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX263_SL_ADDR | 0x400249C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX263_SL_SIZE | 0x400249C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX263_SL_ATT0 | 0x400249D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX263_SL_ATT1 | 0x400249D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX263_SL_ATT2 | 0x400249D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX263_SL_ATT3 | 0x400249DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX263_MS_ADDR | 0x400249E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX263_MS_SIZE | 0x400249E4 | FULL | Master region, size |
| PERI_MS_PPU_FX263_MS_ATT0 | 0x400249F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX263_MS_ATT1 | 0x400249F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX263_MS_ATT2 | 0x400249F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX263_MS_ATT3 | 0x400249FC | FULL | Master attributes 3 |

## 23.281 PPU_FX 264

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX264_SL_ADDR | 0x40024A00 | FULL | Slave region, base address |
| PERI_MS_PPU_FX264_SL_SIZE | 0x40024A04 | FULL | Slave region, size |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX264_SL_ATT0 | 0x40024A10 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX264_SL_ATT1 | 0x40024A14 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX264_SL_ATT2 | 0x40024A18 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX264_SL_ATT3 | 0x40024A1C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX264_MS_ADDR | 0x40024A20 | FULL | Master region, base address |
| PERI_MS_PPU_FX264_MS_SIZE | 0x40024A24 | FULL | Master region, size |
| PERI_MS_PPU_FX264_MS_ATT0 | 0x40024A30 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX264_MS_ATT1 | 0x40024A34 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX264_MS_ATT2 | 0x40024A38 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX264_MS_ATT3 | 0x40024A3C | FULL | Master attributes 3 |

## 23.282 PPU_FX 265

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX265_SL_ADDR | 0x40024A40 | FULL | Slave region, base address |
| PERI_MS_PPU_FX265_SL_SIZE | 0x40024A44 | FULL | Slave region, size |
| PERI_MS_PPU_FX265_SL_ATT0 | 0x40024A50 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX265_SL_ATT1 | 0x40024A54 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX265_SL_ATT2 | 0x40024A58 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX265_SL_ATT3 | 0x40024A5C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX265_MS_ADDR | 0x40024A60 | FULL | Master region, base address |
| PERI_MS_PPU_FX265_MS_SIZE | 0x40024A64 | FULL | Master region, size |
| PERI_MS_PPU_FX265_MS_ATT0 | 0x40024A70 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX265_MS_ATT1 | 0x40024A74 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX265_MS_ATT2 | 0x40024A78 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX265_MS_ATT3 | 0x40024A7C | FULL | Master attributes 3 |

## 23.283 PPU_FX 266

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX266_SL_ADDR | 0x40024A80 | FULL | Slave region, base address |
| PERI_MS_PPU_FX266_SL_SIZE | 0x40024A84 | FULL | Slave region, size |
| PERI_MS_PPU_FX266_SL_ATT0 | 0x40024A90 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX266_SL_ATT1 | 0x40024A94 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX266_SL_ATT2 | 0x40024A98 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX266_SL_ATT3 | 0x40024A9C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX266_MS_ADDR | 0x40024AA0 | FULL | Master region, base address |
| PERI_MS_PPU_FX266_MS_SIZE | 0x40024AA4 | FULL | Master region, size |
| PERI_MS_PPU_FX266_MS_ATT0 | 0x40024AB0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX266_MS_ATT1 | 0x40024AB4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX266_MS_ATT2 | 0x40024AB8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX266_MS_ATT3 | 0x40024ABC | FULL | Master attributes 3 |

## 23.284 PPU_FX 267

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX267_SL_ADDR | 0x40024AC0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX267_SL_SIZE | 0x40024AC4 | FULL | Slave region, size |
| PERI_MS_PPU_FX267_SL_ATT0 | 0x40024AD0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX267_SL_ATT1 | 0x40024AD4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX267_SL_ATT2 | 0x40024AD8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX267_SL_ATT3 | 0x40024ADC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX267_MS_ADDR | 0x40024AE0 | FULL | Master region, base address |
| PERI_MS_PPU_FX267_MS_SIZE | 0x40024AE4 | FULL | Master region, size |
| PERI_MS_PPU_FX267_MS_ATT0 | 0x40024AF0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX267_MS_ATT1 | 0x40024AF4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX267_MS_ATT2 | 0x40024AF8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX267_MS_ATT3 | 0x40024AFC | FULL | Master attributes 3 |

## 23.285 PPU_FX 268

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX268_SL_ADDR | 0x40024B00 | FULL | Slave region, base address |
| PERI_MS_PPU_FX268_SL_SIZE | 0x40024B04 | FULL | Slave region, size |
| PERI_MS_PPU_FX268_SL_ATT0 | 0x40024B10 | FULL | Slave attributes 0 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX268_SL_ATT1 | 0x40024B14 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX268_SL_ATT2 | 0x40024B18 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX268_SL_ATT3 | 0x40024B1C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX268_MS_ADDR | 0x40024B20 | FULL | Master region, base address |
| PERI_MS_PPU_FX268_MS_SIZE | 0x40024B24 | FULL | Master region, size |
| PERI_MS_PPU_FX268_MS_ATT0 | 0x40024B30 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX268_MS_ATT1 | 0x40024B34 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX268_MS_ATT2 | 0x40024B38 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX268_MS_ATT3 | 0x40024B3C | FULL | Master attributes 3 |

## 23.286 PPU_FX 269

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX269_SL_ADDR | 0x40024B40 | FULL | Slave region, base address |
| PERI_MS_PPU_FX269_SL_SIZE | 0x40024B44 | FULL | Slave region, size |
| PERI_MS_PPU_FX269_SL_ATT0 | 0x40024B50 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX269_SL_ATT1 | 0x40024B54 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX269_SL_ATT2 | 0x40024B58 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX269_SL_ATT3 | 0x40024B5C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX269_MS_ADDR | 0x40024B60 | FULL | Master region, base address |
| PERI_MS_PPU_FX269_MS_SIZE | 0x40024B64 | FULL | Master region, size |
| PERI_MS_PPU_FX269_MS_ATT0 | 0x40024B70 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX269_MS_ATT1 | 0x40024B74 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX269_MS_ATT2 | 0x40024B78 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX269_MS_ATT3 | 0x40024B7C | FULL | Master attributes 3 |

## 23.287 PPU_FX 270

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX270_SL_ADDR | 0x40024B80 | FULL | Slave region, base address |
| PERI_MS_PPU_FX270_SL_SIZE | 0x40024B84 | FULL | Slave region, size |
| PERI_MS_PPU_FX270_SL_ATT0 | 0x40024B90 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX270_SL_ATT1 | 0x40024B94 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX270_SL_ATT2 | 0x40024B98 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX270_SL_ATT3 | 0x40024B9C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX270_MS_ADDR | 0x40024BA0 | FULL | Master region, base address |
| PERI_MS_PPU_FX270_MS_SIZE | 0x40024BA4 | FULL | Master region, size |
| PERI_MS_PPU_FX270_MS_ATT0 | 0x40024BB0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX270_MS_ATT1 | 0x40024BB4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX270_MS_ATT2 | 0x40024BB8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX270_MS_ATT3 | 0x40024BBC | FULL | Master attributes 3 |

## 23.288 PPU_FX 271

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX271_SL_ADDR | 0x40024BC0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX271_SL_SIZE | 0x40024BC4 | FULL | Slave region, size |
| PERI_MS_PPU_FX271_SL_ATT0 | 0x40024BD0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX271_SL_ATT1 | 0x40024BD4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX271_SL_ATT2 | 0x40024BD8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX271_SL_ATT3 | 0x40024BDC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX271_MS_ADDR | 0x40024BE0 | FULL | Master region, base address |
| PERI_MS_PPU_FX271_MS_SIZE | 0x40024BE4 | FULL | Master region, size |
| PERI_MS_PPU_FX271_MS_ATT0 | 0x40024BF0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX271_MS_ATT1 | 0x40024BF4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX271_MS_ATT2 | 0x40024BF8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX271_MS_ATT3 | 0x40024BFC | FULL | Master attributes 3 |

## 23.289 PPU_FX 272

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX272_SL_ADDR | 0x40024C00 | FULL | Slave region, base address |
| PERI_MS_PPU_FX272_SL_SIZE | 0x40024C04 | FULL | Slave region, size |
| PERI_MS_PPU_FX272_SL_ATT0 | 0x40024C10 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX272_SL_ATT1 | 0x40024C14 | FULL | Slave attributes 1 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX272_SL_ATT2 | 0x40024C18 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX272_SL_ATT3 | 0x40024C1C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX272_MS_ADDR | 0x40024C20 | FULL | Master region, base address |
| PERI_MS_PPU_FX272_MS_SIZE | 0x40024C24 | FULL | Master region, size |
| PERI_MS_PPU_FX272_MS_ATT0 | 0x40024C30 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX272_MS_ATT1 | 0x40024C34 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX272_MS_ATT2 | 0x40024C38 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX272_MS_ATT3 | 0x40024C3C | FULL | Master attributes 3 |

## 23.290 PPU_FX 273

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX273_SL_ADDR | 0x40024C40 | FULL | Slave region, base address |
| PERI_MS_PPU_FX273_SL_SIZE | 0x40024C44 | FULL | Slave region, size |
| PERI_MS_PPU_FX273_SL_ATT0 | 0x40024C50 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX273_SL_ATT1 | 0x40024C54 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX273_SL_ATT2 | 0x40024C58 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX273_SL_ATT3 | 0x40024C5C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX273_MS_ADDR | 0x40024C60 | FULL | Master region, base address |
| PERI_MS_PPU_FX273_MS_SIZE | 0x40024C64 | FULL | Master region, size |
| PERI_MS_PPU_FX273_MS_ATT0 | 0x40024C70 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX273_MS_ATT1 | 0x40024C74 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX273_MS_ATT2 | 0x40024C78 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX273_MS_ATT3 | 0x40024C7C | FULL | Master attributes 3 |

## 23.291 PPU_FX 274

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX274_SL_ADDR | 0x40024C80 | FULL | Slave region, base address |
| PERI_MS_PPU_FX274_SL_SIZE | 0x40024C84 | FULL | Slave region, size |
| PERI_MS_PPU_FX274_SL_ATT0 | 0x40024C90 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX274_SL_ATT1 | 0x40024C94 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX274_SL_ATT2 | 0x40024C98 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX274_SL_ATT3 | 0x40024C9C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX274_MS_ADDR | 0x40024CA0 | FULL | Master region, base address |
| PERI_MS_PPU_FX274_MS_SIZE | 0x40024CA4 | FULL | Master region, size |
| PERI_MS_PPU_FX274_MS_ATT0 | 0x40024CB0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX274_MS_ATT1 | 0x40024CB4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX274_MS_ATT2 | 0x40024CB8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX274_MS_ATT3 | 0x40024CBC | FULL | Master attributes 3 |

## 23.292 PPU_FX 275

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX275_SL_ADDR | 0x40024CC0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX275_SL_SIZE | 0x40024CC4 | FULL | Slave region, size |
| PERI_MS_PPU_FX275_SL_ATT0 | 0x40024CD0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX275_SL_ATT1 | 0x40024CD4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX275_SL_ATT2 | 0x40024CD8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX275_SL_ATT3 | 0x40024CDC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX275_MS_ADDR | 0x40024CE0 | FULL | Master region, base address |
| PERI_MS_PPU_FX275_MS_SIZE | 0x40024CE4 | FULL | Master region, size |
| PERI_MS_PPU_FX275_MS_ATT0 | 0x40024CF0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX275_MS_ATT1 | 0x40024CF4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX275_MS_ATT2 | 0x40024CF8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX275_MS_ATT3 | 0x40024CFC | FULL | Master attributes 3 |

## 23.293 PPU_FX 276

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX276_SL_ADDR | 0x40024D00 | FULL | Slave region, base address |
| PERI_MS_PPU_FX276_SL_SIZE | 0x40024D04 | FULL | Slave region, size |
| PERI_MS_PPU_FX276_SL_ATT0 | 0x40024D10 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX276_SL_ATT1 | 0x40024D14 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX276_SL_ATT2 | 0x40024D18 | FULL | Slave attributes 2 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX276_SL_ATT3 | 0x40024D1C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX276_MS_ADDR | 0x40024D20 | FULL | Master region, base address |
| PERI_MS_PPU_FX276_MS_SIZE | 0x40024D24 | FULL | Master region, size |
| PERI_MS_PPU_FX276_MS_ATT0 | 0x40024D30 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX276_MS_ATT1 | 0x40024D34 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX276_MS_ATT2 | 0x40024D38 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX276_MS_ATT3 | 0x40024D3C | FULL | Master attributes 3 |

## 23.294 PPU_FX 277

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX277_SL_ADDR | 0x40024D40 | FULL | Slave region, base address |
| PERI_MS_PPU_FX277_SL_SIZE | 0x40024D44 | FULL | Slave region, size |
| PERI_MS_PPU_FX277_SL_ATT0 | 0x40024D50 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX277_SL_ATT1 | 0x40024D54 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX277_SL_ATT2 | 0x40024D58 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX277_SL_ATT3 | 0x40024D5C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX277_MS_ADDR | 0x40024D60 | FULL | Master region, base address |
| PERI_MS_PPU_FX277_MS_SIZE | 0x40024D64 | FULL | Master region, size |
| PERI_MS_PPU_FX277_MS_ATT0 | 0x40024D70 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX277_MS_ATT1 | 0x40024D74 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX277_MS_ATT2 | 0x40024D78 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX277_MS_ATT3 | 0x40024D7C | FULL | Master attributes 3 |

## 23.295 PPU_FX 278

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX278_SL_ADDR | 0x40024D80 | FULL | Slave region, base address |
| PERI_MS_PPU_FX278_SL_SIZE | 0x40024D84 | FULL | Slave region, size |
| PERI_MS_PPU_FX278_SL_ATT0 | 0x40024D90 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX278_SL_ATT1 | 0x40024D94 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX278_SL_ATT2 | 0x40024D98 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX278_SL_ATT3 | 0x40024D9C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX278_MS_ADDR | 0x40024DA0 | FULL | Master region, base address |
| PERI_MS_PPU_FX278_MS_SIZE | 0x40024DA4 | FULL | Master region, size |
| PERI_MS_PPU_FX278_MS_ATT0 | 0x40024DB0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX278_MS_ATT1 | 0x40024DB4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX278_MS_ATT2 | 0x40024DB8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX278_MS_ATT3 | 0x40024DBC | FULL | Master attributes 3 |

## 23.296 PPU_FX 279

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX279_SL_ADDR | 0x40024DC0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX279_SL_SIZE | 0x40024DC4 | FULL | Slave region, size |
| PERI_MS_PPU_FX279_SL_ATT0 | 0x40024DD0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX279_SL_ATT1 | 0x40024DD4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX279_SL_ATT2 | 0x40024DD8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX279_SL_ATT3 | 0x40024DDC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX279_MS_ADDR | 0x40024DE0 | FULL | Master region, base address |
| PERI_MS_PPU_FX279_MS_SIZE | 0x40024DE4 | FULL | Master region, size |
| PERI_MS_PPU_FX279_MS_ATT0 | 0x40024DF0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX279_MS_ATT1 | 0x40024DF4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX279_MS_ATT2 | 0x40024DF8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX279_MS_ATT3 | 0x40024DFC | FULL | Master attributes 3 |

## 23.297 PPU_FX 280

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX280_SL_ADDR | 0x40024E00 | FULL | Slave region, base address |
| PERI_MS_PPU_FX280_SL_SIZE | 0x40024E04 | FULL | Slave region, size |
| PERI_MS_PPU_FX280_SL_ATT0 | 0x40024E10 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX280_SL_ATT1 | 0x40024E14 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX280_SL_ATT2 | 0x40024E18 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX280_SL_ATT3 | 0x40024E1C | FULL | Slave attributes 3 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX280_MS_ADDR | 0x40024E20 | FULL | Master region, base address |
| PERI_MS_PPU_FX280_MS_SIZE | 0x40024E24 | FULL | Master region, size |
| PERI_MS_PPU_FX280_MS_ATT0 | 0x40024E30 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX280_MS_ATT1 | 0x40024E34 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX280_MS_ATT2 | 0x40024E38 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX280_MS_ATT3 | 0x40024E3C | FULL | Master attributes 3 |

## 23.298 PPU_FX 281

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX281_SL_ADDR | 0x40024E40 | FULL | Slave region, base address |
| PERI_MS_PPU_FX281_SL_SIZE | 0x40024E44 | FULL | Slave region, size |
| PERI_MS_PPU_FX281_SL_ATT0 | 0x40024E50 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX281_SL_ATT1 | 0x40024E54 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX281_SL_ATT2 | 0x40024E58 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX281_SL_ATT3 | 0x40024E5C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX281_MS_ADDR | 0x40024E60 | FULL | Master region, base address |
| PERI_MS_PPU_FX281_MS_SIZE | 0x40024E64 | FULL | Master region, size |
| PERI_MS_PPU_FX281_MS_ATT0 | 0x40024E70 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX281_MS_ATT1 | 0x40024E74 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX281_MS_ATT2 | 0x40024E78 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX281_MS_ATT3 | 0x40024E7C | FULL | Master attributes 3 |

## 23.299 PPU_FX 282

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX282_SL_ADDR | 0x40024E80 | FULL | Slave region, base address |
| PERI_MS_PPU_FX282_SL_SIZE | 0x40024E84 | FULL | Slave region, size |
| PERI_MS_PPU_FX282_SL_ATT0 | 0x40024E90 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX282_SL_ATT1 | 0x40024E94 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX282_SL_ATT2 | 0x40024E98 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX282_SL_ATT3 | 0x40024E9C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX282_MS_ADDR | 0x40024EA0 | FULL | Master region, base address |
| PERI_MS_PPU_FX282_MS_SIZE | 0x40024EA4 | FULL | Master region, size |
| PERI_MS_PPU_FX282_MS_ATT0 | 0x40024EB0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX282_MS_ATT1 | 0x40024EB4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX282_MS_ATT2 | 0x40024EB8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX282_MS_ATT3 | 0x40024EBC | FULL | Master attributes 3 |

## 23.300 PPU_FX 283

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX283_SL_ADDR | 0x40024EC0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX283_SL_SIZE | 0x40024EC4 | FULL | Slave region, size |
| PERI_MS_PPU_FX283_SL_ATT0 | 0x40024ED0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX283_SL_ATT1 | 0x40024ED4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX283_SL_ATT2 | 0x40024ED8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX283_SL_ATT3 | 0x40024EDC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX283_MS_ADDR | 0x40024EE0 | FULL | Master region, base address |
| PERI_MS_PPU_FX283_MS_SIZE | 0x40024EE4 | FULL | Master region, size |
| PERI_MS_PPU_FX283_MS_ATT0 | 0x40024EF0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX283_MS_ATT1 | 0x40024EF4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX283_MS_ATT2 | 0x40024EF8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX283_MS_ATT3 | 0x40024EFC | FULL | Master attributes 3 |

## 23.301 PPU_FX 284

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX284_SL_ADDR | 0x40024F00 | FULL | Slave region, base address |
| PERI_MS_PPU_FX284_SL_SIZE | 0x40024F04 | FULL | Slave region, size |
| PERI_MS_PPU_FX284_SL_ATT0 | 0x40024F10 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX284_SL_ATT1 | 0x40024F14 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX284_SL_ATT2 | 0x40024F18 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX284_SL_ATT3 | 0x40024F1C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX284_MS_ADDR | 0x40024F20 | FULL | Master region, base address |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX284_MS_SIZE | 0x40024F24 | FULL | Master region, size |
| PERI_MS_PPU_FX284_MS_ATT0 | 0x40024F30 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX284_MS_ATT1 | 0x40024F34 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX284_MS_ATT2 | 0x40024F38 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX284_MS_ATT3 | 0x40024F3C | FULL | Master attributes 3 |

## 23.302 PPU_FX 285

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX285_SL_ADDR | 0x40024F40 | FULL | Slave region, base address |
| PERI_MS_PPU_FX285_SL_SIZE | 0x40024F44 | FULL | Slave region, size |
| PERI_MS_PPU_FX285_SL_ATT0 | 0x40024F50 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX285_SL_ATT1 | 0x40024F54 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX285_SL_ATT2 | 0x40024F58 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX285_SL_ATT3 | 0x40024F5C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX285_MS_ADDR | 0x40024F60 | FULL | Master region, base address |
| PERI_MS_PPU_FX285_MS_SIZE | 0x40024F64 | FULL | Master region, size |
| PERI_MS_PPU_FX285_MS_ATT0 | 0x40024F70 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX285_MS_ATT1 | 0x40024F74 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX285_MS_ATT2 | 0x40024F78 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX285_MS_ATT3 | 0x40024F7C | FULL | Master attributes 3 |

## 23.303 PPU_FX 286

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX286_SL_ADDR | 0x40024F80 | FULL | Slave region, base address |
| PERI_MS_PPU_FX286_SL_SIZE | 0x40024F84 | FULL | Slave region, size |
| PERI_MS_PPU_FX286_SL_ATT0 | 0x40024F90 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX286_SL_ATT1 | 0x40024F94 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX286_SL_ATT2 | 0x40024F98 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX286_SL_ATT3 | 0x40024F9C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX286_MS_ADDR | 0x40024FA0 | FULL | Master region, base address |
| PERI_MS_PPU_FX286_MS_SIZE | 0x40024FA4 | FULL | Master region, size |
| PERI_MS_PPU_FX286_MS_ATT0 | 0x40024FB0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX286_MS_ATT1 | 0x40024FB4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX286_MS_ATT2 | 0x40024FB8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX286_MS_ATT3 | 0x40024FBC | FULL | Master attributes 3 |

## 23.304 PPU_FX 287

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX287_SL_ADDR | 0x40024FC0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX287_SL_SIZE | 0x40024FC4 | FULL | Slave region, size |
| PERI_MS_PPU_FX287_SL_ATT0 | 0x40024FD0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX287_SL_ATT1 | 0x40024FD4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX287_SL_ATT2 | 0x40024FD8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX287_SL_ATT3 | 0x40024FDC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX287_MS_ADDR | 0x40024FE0 | FULL | Master region, base address |
| PERI_MS_PPU_FX287_MS_SIZE | 0x40024FE4 | FULL | Master region, size |
| PERI_MS_PPU_FX287_MS_ATT0 | 0x40024FF0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX287_MS_ATT1 | 0x40024FF4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX287_MS_ATT2 | 0x40024FF8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX287_MS_ATT3 | 0x40024FFC | FULL | Master attributes 3 |

## 23.305 PPU_FX 288

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX288_SL_ADDR | 0x40025000 | FULL | Slave region, base address |
| PERI_MS_PPU_FX288_SL_SIZE | 0x40025004 | FULL | Slave region, size |
| PERI_MS_PPU_FX288_SL_ATT0 | 0x40025010 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX288_SL_ATT1 | 0x40025014 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX288_SL_ATT2 | 0x40025018 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX288_SL_ATT3 | 0x4002501C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX288_MS_ADDR | 0x40025020 | FULL | Master region, base address |
| PERI_MS_PPU_FX288_MS_SIZE | 0x40025024 | FULL | Master region, size |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX288_MS_ATT0 | 0x40025030 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX288_MS_ATT1 | 0x40025034 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX288_MS_ATT2 | 0x40025038 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX288_MS_ATT3 | 0x4002503C | FULL | Master attributes 3 |

## 23.306 PPU_FX 289

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX289_SL_ADDR | 0x40025040 | FULL | Slave region, base address |
| PERI_MS_PPU_FX289_SL_SIZE | 0x40025044 | FULL | Slave region, size |
| PERI_MS_PPU_FX289_SL_ATT0 | 0x40025050 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX289_SL_ATT1 | 0x40025054 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX289_SL_ATT2 | 0x40025058 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX289_SL_ATT3 | 0x4002505C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX289_MS_ADDR | 0x40025060 | FULL | Master region, base address |
| PERI_MS_PPU_FX289_MS_SIZE | 0x40025064 | FULL | Master region, size |
| PERI_MS_PPU_FX289_MS_ATT0 | 0x40025070 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX289_MS_ATT1 | 0x40025074 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX289_MS_ATT2 | 0x40025078 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX289_MS_ATT3 | 0x4002507C | FULL | Master attributes 3 |

## 23.307 PPU_FX 290

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX290_SL_ADDR | 0x40025080 | FULL | Slave region, base address |
| PERI_MS_PPU_FX290_SL_SIZE | 0x40025084 | FULL | Slave region, size |
| PERI_MS_PPU_FX290_SL_ATT0 | 0x40025090 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX290_SL_ATT1 | 0x40025094 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX290_SL_ATT2 | 0x40025098 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX290_SL_ATT3 | 0x4002509C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX290_MS_ADDR | 0x400250A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX290_MS_SIZE | 0x400250A4 | FULL | Master region, size |
| PERI_MS_PPU_FX290_MS_ATT0 | 0x400250B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX290_MS_ATT1 | 0x400250B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX290_MS_ATT2 | 0x400250B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX290_MS_ATT3 | 0x400250BC | FULL | Master attributes 3 |

## 23.308 PPU_FX 291

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX291_SL_ADDR | 0x400250C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX291_SL_SIZE | 0x400250C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX291_SL_ATT0 | 0x400250D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX291_SL_ATT1 | 0x400250D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX291_SL_ATT2 | 0x400250D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX291_SL_ATT3 | 0x400250DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX291_MS_ADDR | 0x400250E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX291_MS_SIZE | 0x400250E4 | FULL | Master region, size |
| PERI_MS_PPU_FX291_MS_ATT0 | 0x400250F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX291_MS_ATT1 | 0x400250F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX291_MS_ATT2 | 0x400250F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX291_MS_ATT3 | 0x400250FC | FULL | Master attributes 3 |

## 23.309 PPU_FX 292

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX292_SL_ADDR | 0x40025100 | FULL | Slave region, base address |
| PERI_MS_PPU_FX292_SL_SIZE | 0x40025104 | FULL | Slave region, size |
| PERI_MS_PPU_FX292_SL_ATT0 | 0x40025110 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX292_SL_ATT1 | 0x40025114 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX292_SL_ATT2 | 0x40025118 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX292_SL_ATT3 | 0x4002511C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX292_MS_ADDR | 0x40025120 | FULL | Master region, base address |
| PERI_MS_PPU_FX292_MS_SIZE | 0x40025124 | FULL | Master region, size |
| PERI_MS_PPU_FX292_MS_ATT0 | 0x40025130 | FULL | Master attributes 0 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX292_MS_ATT1 | 0x40025134 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX292_MS_ATT2 | 0x40025138 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX292_MS_ATT3 | 0x4002513C | FULL | Master attributes 3 |

## 23.310 PPU_FX 293

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX293_SL_ADDR | 0x40025140 | FULL | Slave region, base address |
| PERI_MS_PPU_FX293_SL_SIZE | 0x40025144 | FULL | Slave region, size |
| PERI_MS_PPU_FX293_SL_ATT0 | 0x40025150 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX293_SL_ATT1 | 0x40025154 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX293_SL_ATT2 | 0x40025158 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX293_SL_ATT3 | 0x4002515C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX293_MS_ADDR | 0x40025160 | FULL | Master region, base address |
| PERI_MS_PPU_FX293_MS_SIZE | 0x40025164 | FULL | Master region, size |
| PERI_MS_PPU_FX293_MS_ATT0 | 0x40025170 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX293_MS_ATT1 | 0x40025174 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX293_MS_ATT2 | 0x40025178 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX293_MS_ATT3 | 0x4002517C | FULL | Master attributes 3 |

## 23.311 PPU_FX 294

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX294_SL_ADDR | 0x40025180 | FULL | Slave region, base address |
| PERI_MS_PPU_FX294_SL_SIZE | 0x40025184 | FULL | Slave region, size |
| PERI_MS_PPU_FX294_SL_ATT0 | 0x40025190 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX294_SL_ATT1 | 0x40025194 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX294_SL_ATT2 | 0x40025198 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX294_SL_ATT3 | 0x4002519C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX294_MS_ADDR | 0x400251A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX294_MS_SIZE | 0x400251A4 | FULL | Master region, size |
| PERI_MS_PPU_FX294_MS_ATT0 | 0x400251B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX294_MS_ATT1 | 0x400251B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX294_MS_ATT2 | 0x400251B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX294_MS_ATT3 | 0x400251BC | FULL | Master attributes 3 |

## 23.312 PPU_FX 295

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX295_SL_ADDR | 0x400251C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX295_SL_SIZE | 0x400251C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX295_SL_ATT0 | 0x400251D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX295_SL_ATT1 | 0x400251D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX295_SL_ATT2 | 0x400251D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX295_SL_ATT3 | 0x400251DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX295_MS_ADDR | 0x400251E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX295_MS_SIZE | 0x400251E4 | FULL | Master region, size |
| PERI_MS_PPU_FX295_MS_ATT0 | 0x400251F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX295_MS_ATT1 | 0x400251F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX295_MS_ATT2 | 0x400251F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX295_MS_ATT3 | 0x400251FC | FULL | Master attributes 3 |

## 23.313 PPU_FX 296

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX296_SL_ADDR | 0x40025200 | FULL | Slave region, base address |
| PERI_MS_PPU_FX296_SL_SIZE | 0x40025204 | FULL | Slave region, size |
| PERI_MS_PPU_FX296_SL_ATT0 | 0x40025210 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX296_SL_ATT1 | 0x40025214 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX296_SL_ATT2 | 0x40025218 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX296_SL_ATT3 | 0x4002521C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX296_MS_ADDR | 0x40025220 | FULL | Master region, base address |
| PERI_MS_PPU_FX296_MS_SIZE | 0x40025224 | FULL | Master region, size |
| PERI_MS_PPU_FX296_MS_ATT0 | 0x40025230 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX296_MS_ATT1 | 0x40025234 | FULL | Master attributes 1 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX296_MS_ATT2 | 0x40025238 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX296_MS_ATT3 | 0x4002523C | FULL | Master attributes 3 |

## 23.314 PPU_FX 297

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX297_SL_ADDR | 0x40025240 | FULL | Slave region, base address |
| PERI_MS_PPU_FX297_SL_SIZE | 0x40025244 | FULL | Slave region, size |
| PERI_MS_PPU_FX297_SL_ATT0 | 0x40025250 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX297_SL_ATT1 | 0x40025254 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX297_SL_ATT2 | 0x40025258 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX297_SL_ATT3 | 0x4002525C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX297_MS_ADDR | 0x40025260 | FULL | Master region, base address |
| PERI_MS_PPU_FX297_MS_SIZE | 0x40025264 | FULL | Master region, size |
| PERI_MS_PPU_FX297_MS_ATT0 | 0x40025270 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX297_MS_ATT1 | 0x40025274 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX297_MS_ATT2 | 0x40025278 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX297_MS_ATT3 | 0x4002527C | FULL | Master attributes 3 |

## 23.315 PPU_FX 298

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX298_SL_ADDR | 0x40025280 | FULL | Slave region, base address |
| PERI_MS_PPU_FX298_SL_SIZE | 0x40025284 | FULL | Slave region, size |
| PERI_MS_PPU_FX298_SL_ATT0 | 0x40025290 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX298_SL_ATT1 | 0x40025294 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX298_SL_ATT2 | 0x40025298 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX298_SL_ATT3 | 0x4002529C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX298_MS_ADDR | 0x400252A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX298_MS_SIZE | 0x400252A4 | FULL | Master region, size |
| PERI_MS_PPU_FX298_MS_ATT0 | 0x400252B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX298_MS_ATT1 | 0x400252B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX298_MS_ATT2 | 0x400252B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX298_MS_ATT3 | 0x400252BC | FULL | Master attributes 3 |

## 23.316 PPU_FX 299

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX299_SL_ADDR | 0x400252C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX299_SL_SIZE | 0x400252C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX299_SL_ATT0 | 0x400252D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX299_SL_ATT1 | 0x400252D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX299_SL_ATT2 | 0x400252D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX299_SL_ATT3 | 0x400252DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX299_MS_ADDR | 0x400252E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX299_MS_SIZE | 0x400252E4 | FULL | Master region, size |
| PERI_MS_PPU_FX299_MS_ATT0 | 0x400252F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX299_MS_ATT1 | 0x400252F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX299_MS_ATT2 | 0x400252F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX299_MS_ATT3 | 0x400252FC | FULL | Master attributes 3 |

## 23.317 PPU_FX 300

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX300_SL_ADDR | 0x40025300 | FULL | Slave region, base address |
| PERI_MS_PPU_FX300_SL_SIZE | 0x40025304 | FULL | Slave region, size |
| PERI_MS_PPU_FX300_SL_ATT0 | 0x40025310 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX300_SL_ATT1 | 0x40025314 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX300_SL_ATT2 | 0x40025318 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX300_SL_ATT3 | 0x4002531C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX300_MS_ADDR | 0x40025320 | FULL | Master region, base address |
| PERI_MS_PPU_FX300_MS_SIZE | 0x40025324 | FULL | Master region, size |
| PERI_MS_PPU_FX300_MS_ATT0 | 0x40025330 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX300_MS_ATT1 | 0x40025334 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX300_MS_ATT2 | 0x40025338 | FULL | Master attributes 2 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX300_MS_ATT3 | 0x4002533C | FULL | Master attributes 3 |

## 23.318 PPU_FX 301

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX301_SL_ADDR | 0x40025340 | FULL | Slave region, base address |
| PERI_MS_PPU_FX301_SL_SIZE | 0x40025344 | FULL | Slave region, size |
| PERI_MS_PPU_FX301_SL_ATT0 | 0x40025350 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX301_SL_ATT1 | 0x40025354 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX301_SL_ATT2 | 0x40025358 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX301_SL_ATT3 | 0x4002535C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX301_MS_ADDR | 0x40025360 | FULL | Master region, base address |
| PERI_MS_PPU_FX301_MS_SIZE | 0x40025364 | FULL | Master region, size |
| PERI_MS_PPU_FX301_MS_ATT0 | 0x40025370 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX301_MS_ATT1 | 0x40025374 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX301_MS_ATT2 | 0x40025378 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX301_MS_ATT3 | 0x4002537C | FULL | Master attributes 3 |

## 23.319 PPU_FX 302

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX302_SL_ADDR | 0x40025380 | FULL | Slave region, base address |
| PERI_MS_PPU_FX302_SL_SIZE | 0x40025384 | FULL | Slave region, size |
| PERI_MS_PPU_FX302_SL_ATT0 | 0x40025390 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX302_SL_ATT1 | 0x40025394 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX302_SL_ATT2 | 0x40025398 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX302_SL_ATT3 | 0x4002539C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX302_MS_ADDR | 0x400253A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX302_MS_SIZE | 0x400253A4 | FULL | Master region, size |
| PERI_MS_PPU_FX302_MS_ATT0 | 0x400253B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX302_MS_ATT1 | 0x400253B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX302_MS_ATT2 | 0x400253B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX302_MS_ATT3 | 0x400253BC | FULL | Master attributes 3 |

## 23.320 PPU_FX 303

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX303_SL_ADDR | 0x400253C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX303_SL_SIZE | 0x400253C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX303_SL_ATT0 | 0x400253D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX303_SL_ATT1 | 0x400253D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX303_SL_ATT2 | 0x400253D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX303_SL_ATT3 | 0x400253DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX303_MS_ADDR | 0x400253E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX303_MS_SIZE | 0x400253E4 | FULL | Master region, size |
| PERI_MS_PPU_FX303_MS_ATT0 | 0x400253F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX303_MS_ATT1 | 0x400253F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX303_MS_ATT2 | 0x400253F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX303_MS_ATT3 | 0x400253FC | FULL | Master attributes 3 |

## 23.321 PPU_FX 304

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX304_SL_ADDR | 0x40025400 | FULL | Slave region, base address |
| PERI_MS_PPU_FX304_SL_SIZE | 0x40025404 | FULL | Slave region, size |
| PERI_MS_PPU_FX304_SL_ATT0 | 0x40025410 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX304_SL_ATT1 | 0x40025414 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX304_SL_ATT2 | 0x40025418 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX304_SL_ATT3 | 0x4002541C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX304_MS_ADDR | 0x40025420 | FULL | Master region, base address |
| PERI_MS_PPU_FX304_MS_SIZE | 0x40025424 | FULL | Master region, size |
| PERI_MS_PPU_FX304_MS_ATT0 | 0x40025430 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX304_MS_ATT1 | 0x40025434 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX304_MS_ATT2 | 0x40025438 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX304_MS_ATT3 | 0x4002543C | FULL | Master attributes 3 |

## 23.322 PPU_FX 305

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX305_SL_ADDR | 0x40025440 | FULL | Slave region, base address |
| PERI_MS_PPU_FX305_SL_SIZE | 0x40025444 | FULL | Slave region, size |
| PERI_MS_PPU_FX305_SL_ATT0 | 0x40025450 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX305_SL_ATT1 | 0x40025454 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX305_SL_ATT2 | 0x40025458 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX305_SL_ATT3 | 0x4002545C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX305_MS_ADDR | 0x40025460 | FULL | Master region, base address |
| PERI_MS_PPU_FX305_MS_SIZE | 0x40025464 | FULL | Master region, size |
| PERI_MS_PPU_FX305_MS_ATT0 | 0x40025470 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX305_MS_ATT1 | 0x40025474 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX305_MS_ATT2 | 0x40025478 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX305_MS_ATT3 | 0x4002547C | FULL | Master attributes 3 |

## 23.323 PPU_FX 306

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX306_SL_ADDR | 0x40025480 | FULL | Slave region, base address |
| PERI_MS_PPU_FX306_SL_SIZE | 0x40025484 | FULL | Slave region, size |
| PERI_MS_PPU_FX306_SL_ATT0 | 0x40025490 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX306_SL_ATT1 | 0x40025494 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX306_SL_ATT2 | 0x40025498 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX306_SL_ATT3 | 0x4002549C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX306_MS_ADDR | 0x400254A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX306_MS_SIZE | 0x400254A4 | FULL | Master region, size |
| PERI_MS_PPU_FX306_MS_ATT0 | 0x400254B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX306_MS_ATT1 | 0x400254B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX306_MS_ATT2 | 0x400254B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX306_MS_ATT3 | 0x400254BC | FULL | Master attributes 3 |

## 23.324 PPU_FX 307

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX307_SL_ADDR | 0x400254C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX307_SL_SIZE | 0x400254C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX307_SL_ATT0 | 0x400254D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX307_SL_ATT1 | 0x400254D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX307_SL_ATT2 | 0x400254D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX307_SL_ATT3 | 0x400254DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX307_MS_ADDR | 0x400254E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX307_MS_SIZE | 0x400254E4 | FULL | Master region, size |
| PERI_MS_PPU_FX307_MS_ATT0 | 0x400254F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX307_MS_ATT1 | 0x400254F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX307_MS_ATT2 | 0x400254F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX307_MS_ATT3 | 0x400254FC | FULL | Master attributes 3 |

## 23.325 PPU_FX 308

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX308_SL_ADDR | 0x40025500 | FULL | Slave region, base address |
| PERI_MS_PPU_FX308_SL_SIZE | 0x40025504 | FULL | Slave region, size |
| PERI_MS_PPU_FX308_SL_ATT0 | 0x40025510 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX308_SL_ATT1 | 0x40025514 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX308_SL_ATT2 | 0x40025518 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX308_SL_ATT3 | 0x4002551C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX308_MS_ADDR | 0x40025520 | FULL | Master region, base address |
| PERI_MS_PPU_FX308_MS_SIZE | 0x40025524 | FULL | Master region, size |
| PERI_MS_PPU_FX308_MS_ATT0 | 0x40025530 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX308_MS_ATT1 | 0x40025534 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX308_MS_ATT2 | 0x40025538 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX308_MS_ATT3 | 0x4002553C | FULL | Master attributes 3 |

## 23.326 PPU_FX 309

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX309_SL_ADDR | 0x40025540 | FULL | Slave region, base address |
| PERI_MS_PPU_FX309_SL_SIZE | 0x40025544 | FULL | Slave region, size |
| PERI_MS_PPU_FX309_SL_ATT0 | 0x40025550 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX309_SL_ATT1 | 0x40025554 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX309_SL_ATT2 | 0x40025558 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX309_SL_ATT3 | 0x4002555C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX309_MS_ADDR | 0x40025560 | FULL | Master region, base address |
| PERI_MS_PPU_FX309_MS_SIZE | 0x40025564 | FULL | Master region, size |
| PERI_MS_PPU_FX309_MS_ATT0 | 0x40025570 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX309_MS_ATT1 | 0x40025574 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX309_MS_ATT2 | 0x40025578 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX309_MS_ATT3 | 0x4002557C | FULL | Master attributes 3 |

## 23.327 PPU_FX 310

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX310_SL_ADDR | 0x40025580 | FULL | Slave region, base address |
| PERI_MS_PPU_FX310_SL_SIZE | 0x40025584 | FULL | Slave region, size |
| PERI_MS_PPU_FX310_SL_ATT0 | 0x40025590 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX310_SL_ATT1 | 0x40025594 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX310_SL_ATT2 | 0x40025598 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX310_SL_ATT3 | 0x4002559C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX310_MS_ADDR | 0x400255A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX310_MS_SIZE | 0x400255A4 | FULL | Master region, size |
| PERI_MS_PPU_FX310_MS_ATT0 | 0x400255B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX310_MS_ATT1 | 0x400255B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX310_MS_ATT2 | 0x400255B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX310_MS_ATT3 | 0x400255BC | FULL | Master attributes 3 |

## 23.328 PPU_FX 311

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX311_SL_ADDR | 0x400255C0 | READ | Slave region, base address |
| PERI_MS_PPU_FX311_SL_SIZE | 0x400255C4 | READ | Slave region, size |
| PERI_MS_PPU_FX311_SL_ATT0 | 0x400255D0 | READ | Slave attributes 0 |
| PERI_MS_PPU_FX311_SL_ATT1 | 0x400255D4 | READ | Slave attributes 1 |
| PERI_MS_PPU_FX311_SL_ATT2 | 0x400255D8 | READ | Slave attributes 2 |
| PERI_MS_PPU_FX311_SL_ATT3 | 0x400255DC | READ | Slave attributes 3 |
| PERI_MS_PPU_FX311_MS_ADDR | 0x400255E0 | READ | Master region, base address |
| PERI_MS_PPU_FX311_MS_SIZE | 0x400255E4 | READ | Master region, size |
| PERI_MS_PPU_FX311_MS_ATT0 | 0x400255F0 | READ | Master attributes 0 |
| PERI_MS_PPU_FX311_MS_ATT1 | 0x400255F4 | READ | Master attributes 1 |
| PERI_MS_PPU_FX311_MS_ATT2 | 0x400255F8 | READ | Master attributes 2 |
| PERI_MS_PPU_FX311_MS_ATT3 | 0x400255FC | READ | Master attributes 3 |

## 23.329 PPU_FX 312

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX312_SL_ADDR | 0x40025600 | READ | Slave region, base address |
| PERI_MS_PPU_FX312_SL_SIZE | 0x40025604 | READ | Slave region, size |
| PERI_MS_PPU_FX312_SL_ATT0 | 0x40025610 | READ | Slave attributes 0 |
| PERI_MS_PPU_FX312_SL_ATT1 | 0x40025614 | READ | Slave attributes 1 |
| PERI_MS_PPU_FX312_SL_ATT2 | 0x40025618 | READ | Slave attributes 2 |
| PERI_MS_PPU_FX312_SL_ATT3 | 0x4002561C | READ | Slave attributes 3 |
| PERI_MS_PPU_FX312_MS_ADDR | 0x40025620 | READ | Master region, base address |
| PERI_MS_PPU_FX312_MS_SIZE | 0x40025624 | READ | Master region, size |
| PERI_MS_PPU_FX312_MS_ATT0 | 0x40025630 | READ | Master attributes 0 |
| PERI_MS_PPU_FX312_MS_ATT1 | 0x40025634 | READ | Master attributes 1 |
| PERI_MS_PPU_FX312_MS_ATT2 | 0x40025638 | READ | Master attributes 2 |
| PERI_MS_PPU_FX312_MS_ATT3 | 0x4002563C | READ | Master attributes 3 |

## 23.330 PPU_FX 313

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX313_SL_ADDR | 0x40025640 | READ | Slave region, base address |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX313_SL_SIZE | 0x40025644 | READ | Slave region, size |
| PERI_MS_PPU_FX313_SL_ATT0 | 0x40025650 | READ | Slave attributes 0 |
| PERI_MS_PPU_FX313_SL_ATT1 | 0x40025654 | READ | Slave attributes 1 |
| PERI_MS_PPU_FX313_SL_ATT2 | 0x40025658 | READ | Slave attributes 2 |
| PERI_MS_PPU_FX313_SL_ATT3 | 0x4002565C | READ | Slave attributes 3 |
| PERI_MS_PPU_FX313_MS_ADDR | 0x40025660 | READ | Master region, base address |
| PERI_MS_PPU_FX313_MS_SIZE | 0x40025664 | READ | Master region, size |
| PERI_MS_PPU_FX313_MS_ATT0 | 0x40025670 | READ | Master attributes 0 |
| PERI_MS_PPU_FX313_MS_ATT1 | 0x40025674 | READ | Master attributes 1 |
| PERI_MS_PPU_FX313_MS_ATT2 | 0x40025678 | READ | Master attributes 2 |
| PERI_MS_PPU_FX313_MS_ATT3 | 0x4002567C | READ | Master attributes 3 |

## 23.331 PPU_FX 314

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX314_SL_ADDR | 0x40025680 | FULL | Slave region, base address |
| PERI_MS_PPU_FX314_SL_SIZE | 0x40025684 | FULL | Slave region, size |
| PERI_MS_PPU_FX314_SL_ATT0 | 0x40025690 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX314_SL_ATT1 | 0x40025694 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX314_SL_ATT2 | 0x40025698 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX314_SL_ATT3 | 0x4002569C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX314_MS_ADDR | 0x400256A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX314_MS_SIZE | 0x400256A4 | FULL | Master region, size |
| PERI_MS_PPU_FX314_MS_ATT0 | 0x400256B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX314_MS_ATT1 | 0x400256B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX314_MS_ATT2 | 0x400256B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX314_MS_ATT3 | 0x400256BC | FULL | Master attributes 3 |

## 23.332 PPU_FX 315

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX315_SL_ADDR | 0x400256C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX315_SL_SIZE | 0x400256C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX315_SL_ATT0 | 0x400256D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX315_SL_ATT1 | 0x400256D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX315_SL_ATT2 | 0x400256D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX315_SL_ATT3 | 0x400256DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX315_MS_ADDR | 0x400256E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX315_MS_SIZE | 0x400256E4 | FULL | Master region, size |
| PERI_MS_PPU_FX315_MS_ATT0 | 0x400256F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX315_MS_ATT1 | 0x400256F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX315_MS_ATT2 | 0x400256F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX315_MS_ATT3 | 0x400256FC | FULL | Master attributes 3 |

## 23.333 PPU_FX 316

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX316_SL_ADDR | 0x40025700 | FULL | Slave region, base address |
| PERI_MS_PPU_FX316_SL_SIZE | 0x40025704 | FULL | Slave region, size |
| PERI_MS_PPU_FX316_SL_ATT0 | 0x40025710 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX316_SL_ATT1 | 0x40025714 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX316_SL_ATT2 | 0x40025718 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX316_SL_ATT3 | 0x4002571C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX316_MS_ADDR | 0x40025720 | FULL | Master region, base address |
| PERI_MS_PPU_FX316_MS_SIZE | 0x40025724 | FULL | Master region, size |
| PERI_MS_PPU_FX316_MS_ATT0 | 0x40025730 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX316_MS_ATT1 | 0x40025734 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX316_MS_ATT2 | 0x40025738 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX316_MS_ATT3 | 0x4002573C | FULL | Master attributes 3 |

## 23.334 PPU_FX 317

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX317_SL_ADDR | 0x40025740 | FULL | Slave region, base address |
| PERI_MS_PPU_FX317_SL_SIZE | 0x40025744 | FULL | Slave region, size |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX317_SL_ATT0 | 0x40025750 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX317_SL_ATT1 | 0x40025754 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX317_SL_ATT2 | 0x40025758 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX317_SL_ATT3 | 0x4002575C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX317_MS_ADDR | 0x40025760 | FULL | Master region, base address |
| PERI_MS_PPU_FX317_MS_SIZE | 0x40025764 | FULL | Master region, size |
| PERI_MS_PPU_FX317_MS_ATT0 | 0x40025770 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX317_MS_ATT1 | 0x40025774 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX317_MS_ATT2 | 0x40025778 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX317_MS_ATT3 | 0x4002577C | FULL | Master attributes 3 |

## 23.335 PPU_FX 318

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX318_SL_ADDR | 0x40025780 | FULL | Slave region, base address |
| PERI_MS_PPU_FX318_SL_SIZE | 0x40025784 | FULL | Slave region, size |
| PERI_MS_PPU_FX318_SL_ATT0 | 0x40025790 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX318_SL_ATT1 | 0x40025794 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX318_SL_ATT2 | 0x40025798 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX318_SL_ATT3 | 0x4002579C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX318_MS_ADDR | 0x400257A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX318_MS_SIZE | 0x400257A4 | FULL | Master region, size |
| PERI_MS_PPU_FX318_MS_ATT0 | 0x400257B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX318_MS_ATT1 | 0x400257B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX318_MS_ATT2 | 0x400257B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX318_MS_ATT3 | 0x400257BC | FULL | Master attributes 3 |

## 23.336 PPU_FX 319

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX319_SL_ADDR | 0x400257C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX319_SL_SIZE | 0x400257C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX319_SL_ATT0 | 0x400257D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX319_SL_ATT1 | 0x400257D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX319_SL_ATT2 | 0x400257D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX319_SL_ATT3 | 0x400257DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX319_MS_ADDR | 0x400257E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX319_MS_SIZE | 0x400257E4 | FULL | Master region, size |
| PERI_MS_PPU_FX319_MS_ATT0 | 0x400257F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX319_MS_ATT1 | 0x400257F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX319_MS_ATT2 | 0x400257F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX319_MS_ATT3 | 0x400257FC | FULL | Master attributes 3 |

## 23.337 PPU_FX 320

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX320_SL_ADDR | 0x40025800 | FULL | Slave region, base address |
| PERI_MS_PPU_FX320_SL_SIZE | 0x40025804 | FULL | Slave region, size |
| PERI_MS_PPU_FX320_SL_ATT0 | 0x40025810 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX320_SL_ATT1 | 0x40025814 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX320_SL_ATT2 | 0x40025818 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX320_SL_ATT3 | 0x4002581C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX320_MS_ADDR | 0x40025820 | FULL | Master region, base address |
| PERI_MS_PPU_FX320_MS_SIZE | 0x40025824 | FULL | Master region, size |
| PERI_MS_PPU_FX320_MS_ATT0 | 0x40025830 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX320_MS_ATT1 | 0x40025834 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX320_MS_ATT2 | 0x40025838 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX320_MS_ATT3 | 0x4002583C | FULL | Master attributes 3 |

## 23.338 PPU_FX 321

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX321_SL_ADDR | 0x40025840 | FULL | Slave region, base address |
| PERI_MS_PPU_FX321_SL_SIZE | 0x40025844 | FULL | Slave region, size |
| PERI_MS_PPU_FX321_SL_ATT0 | 0x40025850 | FULL | Slave attributes 0 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX321_SL_ATT1 | 0x40025854 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX321_SL_ATT2 | 0x40025858 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX321_SL_ATT3 | 0x4002585C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX321_MS_ADDR | 0x40025860 | FULL | Master region, base address |
| PERI_MS_PPU_FX321_MS_SIZE | 0x40025864 | FULL | Master region, size |
| PERI_MS_PPU_FX321_MS_ATT0 | 0x40025870 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX321_MS_ATT1 | 0x40025874 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX321_MS_ATT2 | 0x40025878 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX321_MS_ATT3 | 0x4002587C | FULL | Master attributes 3 |

## 23.339 PPU_FX 322

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX322_SL_ADDR | 0x40025880 | FULL | Slave region, base address |
| PERI_MS_PPU_FX322_SL_SIZE | 0x40025884 | FULL | Slave region, size |
| PERI_MS_PPU_FX322_SL_ATT0 | 0x40025890 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX322_SL_ATT1 | 0x40025894 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX322_SL_ATT2 | 0x40025898 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX322_SL_ATT3 | 0x4002589C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX322_MS_ADDR | 0x400258A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX322_MS_SIZE | 0x400258A4 | FULL | Master region, size |
| PERI_MS_PPU_FX322_MS_ATT0 | 0x400258B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX322_MS_ATT1 | 0x400258B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX322_MS_ATT2 | 0x400258B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX322_MS_ATT3 | 0x400258BC | FULL | Master attributes 3 |

## 23.340 PPU_FX 323

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX323_SL_ADDR | 0x400258C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX323_SL_SIZE | 0x400258C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX323_SL_ATT0 | 0x400258D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX323_SL_ATT1 | 0x400258D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX323_SL_ATT2 | 0x400258D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX323_SL_ATT3 | 0x400258DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX323_MS_ADDR | 0x400258E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX323_MS_SIZE | 0x400258E4 | FULL | Master region, size |
| PERI_MS_PPU_FX323_MS_ATT0 | 0x400258F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX323_MS_ATT1 | 0x400258F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX323_MS_ATT2 | 0x400258F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX323_MS_ATT3 | 0x400258FC | FULL | Master attributes 3 |

## 23.341 PPU_FX 324

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX324_SL_ADDR | 0x40025900 | FULL | Slave region, base address |
| PERI_MS_PPU_FX324_SL_SIZE | 0x40025904 | FULL | Slave region, size |
| PERI_MS_PPU_FX324_SL_ATT0 | 0x40025910 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX324_SL_ATT1 | 0x40025914 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX324_SL_ATT2 | 0x40025918 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX324_SL_ATT3 | 0x4002591C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX324_MS_ADDR | 0x40025920 | FULL | Master region, base address |
| PERI_MS_PPU_FX324_MS_SIZE | 0x40025924 | FULL | Master region, size |
| PERI_MS_PPU_FX324_MS_ATT0 | 0x40025930 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX324_MS_ATT1 | 0x40025934 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX324_MS_ATT2 | 0x40025938 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX324_MS_ATT3 | 0x4002593C | FULL | Master attributes 3 |

## 23.342 PPU_FX 325

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX325_SL_ADDR | 0x40025940 | FULL | Slave region, base address |
| PERI_MS_PPU_FX325_SL_SIZE | 0x40025944 | FULL | Slave region, size |
| PERI_MS_PPU_FX325_SL_ATT0 | 0x40025950 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX325_SL_ATT1 | 0x40025954 | FULL | Slave attributes 1 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX325_SL_ATT2 | 0x40025958 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX325_SL_ATT3 | 0x4002595C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX325_MS_ADDR | 0x40025960 | FULL | Master region, base address |
| PERI_MS_PPU_FX325_MS_SIZE | 0x40025964 | FULL | Master region, size |
| PERI_MS_PPU_FX325_MS_ATT0 | 0x40025970 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX325_MS_ATT1 | 0x40025974 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX325_MS_ATT2 | 0x40025978 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX325_MS_ATT3 | 0x4002597C | FULL | Master attributes 3 |

## 23.343 PPU_FX 326

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX326_SL_ADDR | 0x40025980 | FULL | Slave region, base address |
| PERI_MS_PPU_FX326_SL_SIZE | 0x40025984 | FULL | Slave region, size |
| PERI_MS_PPU_FX326_SL_ATT0 | 0x40025990 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX326_SL_ATT1 | 0x40025994 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX326_SL_ATT2 | 0x40025998 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX326_SL_ATT3 | 0x4002599C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX326_MS_ADDR | 0x400259A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX326_MS_SIZE | 0x400259A4 | FULL | Master region, size |
| PERI_MS_PPU_FX326_MS_ATT0 | 0x400259B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX326_MS_ATT1 | 0x400259B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX326_MS_ATT2 | 0x400259B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX326_MS_ATT3 | 0x400259BC | FULL | Master attributes 3 |

## 23.344 PPU_FX 327

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX327_SL_ADDR | 0x400259C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX327_SL_SIZE | 0x400259C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX327_SL_ATT0 | 0x400259D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX327_SL_ATT1 | 0x400259D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX327_SL_ATT2 | 0x400259D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX327_SL_ATT3 | 0x400259DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX327_MS_ADDR | 0x400259E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX327_MS_SIZE | 0x400259E4 | FULL | Master region, size |
| PERI_MS_PPU_FX327_MS_ATT0 | 0x400259F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX327_MS_ATT1 | 0x400259F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX327_MS_ATT2 | 0x400259F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX327_MS_ATT3 | 0x400259FC | FULL | Master attributes 3 |

## 23.345 PPU_FX 328

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX328_SL_ADDR | 0x40025A00 | FULL | Slave region, base address |
| PERI_MS_PPU_FX328_SL_SIZE | 0x40025A04 | FULL | Slave region, size |
| PERI_MS_PPU_FX328_SL_ATT0 | 0x40025A10 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX328_SL_ATT1 | 0x40025A14 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX328_SL_ATT2 | 0x40025A18 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX328_SL_ATT3 | 0x40025A1C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX328_MS_ADDR | 0x40025A20 | FULL | Master region, base address |
| PERI_MS_PPU_FX328_MS_SIZE | 0x40025A24 | FULL | Master region, size |
| PERI_MS_PPU_FX328_MS_ATT0 | 0x40025A30 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX328_MS_ATT1 | 0x40025A34 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX328_MS_ATT2 | 0x40025A38 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX328_MS_ATT3 | 0x40025A3C | FULL | Master attributes 3 |

## 23.346 PPU_FX 329

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX329_SL_ADDR | 0x40025A40 | FULL | Slave region, base address |
| PERI_MS_PPU_FX329_SL_SIZE | 0x40025A44 | FULL | Slave region, size |
| PERI_MS_PPU_FX329_SL_ATT0 | 0x40025A50 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX329_SL_ATT1 | 0x40025A54 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX329_SL_ATT2 | 0x40025A58 | FULL | Slave attributes 2 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX329_SL_ATT3 | 0x40025A5C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX329_MS_ADDR | 0x40025A60 | FULL | Master region, base address |
| PERI_MS_PPU_FX329_MS_SIZE | 0x40025A64 | FULL | Master region, size |
| PERI_MS_PPU_FX329_MS_ATT0 | 0x40025A70 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX329_MS_ATT1 | 0x40025A74 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX329_MS_ATT2 | 0x40025A78 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX329_MS_ATT3 | 0x40025A7C | FULL | Master attributes 3 |

## 23.347 PPU_FX 330

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX330_SL_ADDR | 0x40025A80 | FULL | Slave region, base address |
| PERI_MS_PPU_FX330_SL_SIZE | 0x40025A84 | FULL | Slave region, size |
| PERI_MS_PPU_FX330_SL_ATT0 | 0x40025A90 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX330_SL_ATT1 | 0x40025A94 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX330_SL_ATT2 | 0x40025A98 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX330_SL_ATT3 | 0x40025A9C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX330_MS_ADDR | 0x40025AA0 | FULL | Master region, base address |
| PERI_MS_PPU_FX330_MS_SIZE | 0x40025AA4 | FULL | Master region, size |
| PERI_MS_PPU_FX330_MS_ATT0 | 0x40025AB0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX330_MS_ATT1 | 0x40025AB4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX330_MS_ATT2 | 0x40025AB8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX330_MS_ATT3 | 0x40025ABC | FULL | Master attributes 3 |

## 23.348 PPU_FX 331

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX331_SL_ADDR | 0x40025AC0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX331_SL_SIZE | 0x40025AC4 | FULL | Slave region, size |
| PERI_MS_PPU_FX331_SL_ATT0 | 0x40025AD0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX331_SL_ATT1 | 0x40025AD4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX331_SL_ATT2 | 0x40025AD8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX331_SL_ATT3 | 0x40025ADC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX331_MS_ADDR | 0x40025AE0 | FULL | Master region, base address |
| PERI_MS_PPU_FX331_MS_SIZE | 0x40025AE4 | FULL | Master region, size |
| PERI_MS_PPU_FX331_MS_ATT0 | 0x40025AF0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX331_MS_ATT1 | 0x40025AF4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX331_MS_ATT2 | 0x40025AF8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX331_MS_ATT3 | 0x40025AFC | FULL | Master attributes 3 |

## 23.349 PPU_FX 332

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX332_SL_ADDR | 0x40025B00 | FULL | Slave region, base address |
| PERI_MS_PPU_FX332_SL_SIZE | 0x40025B04 | FULL | Slave region, size |
| PERI_MS_PPU_FX332_SL_ATT0 | 0x40025B10 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX332_SL_ATT1 | 0x40025B14 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX332_SL_ATT2 | 0x40025B18 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX332_SL_ATT3 | 0x40025B1C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX332_MS_ADDR | 0x40025B20 | FULL | Master region, base address |
| PERI_MS_PPU_FX332_MS_SIZE | 0x40025B24 | FULL | Master region, size |
| PERI_MS_PPU_FX332_MS_ATT0 | 0x40025B30 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX332_MS_ATT1 | 0x40025B34 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX332_MS_ATT2 | 0x40025B38 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX332_MS_ATT3 | 0x40025B3C | FULL | Master attributes 3 |

## 23.350 PPU_FX 333

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX333_SL_ADDR | 0x40025B40 | FULL | Slave region, base address |
| PERI_MS_PPU_FX333_SL_SIZE | 0x40025B44 | FULL | Slave region, size |
| PERI_MS_PPU_FX333_SL_ATT0 | 0x40025B50 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX333_SL_ATT1 | 0x40025B54 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX333_SL_ATT2 | 0x40025B58 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX333_SL_ATT3 | 0x40025B5C | FULL | Slave attributes 3 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX333_MS_ADDR | 0x40025B60 | FULL | Master region, base address |
| PERI_MS_PPU_FX333_MS_SIZE | 0x40025B64 | FULL | Master region, size |
| PERI_MS_PPU_FX333_MS_ATT0 | 0x40025B70 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX333_MS_ATT1 | 0x40025B74 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX333_MS_ATT2 | 0x40025B78 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX333_MS_ATT3 | 0x40025B7C | FULL | Master attributes 3 |

## 23.351 PPU_FX 334

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX334_SL_ADDR | 0x40025B80 | FULL | Slave region, base address |
| PERI_MS_PPU_FX334_SL_SIZE | 0x40025B84 | FULL | Slave region, size |
| PERI_MS_PPU_FX334_SL_ATT0 | 0x40025B90 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX334_SL_ATT1 | 0x40025B94 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX334_SL_ATT2 | 0x40025B98 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX334_SL_ATT3 | 0x40025B9C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX334_MS_ADDR | 0x40025BA0 | FULL | Master region, base address |
| PERI_MS_PPU_FX334_MS_SIZE | 0x40025BA4 | FULL | Master region, size |
| PERI_MS_PPU_FX334_MS_ATT0 | 0x40025BB0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX334_MS_ATT1 | 0x40025BB4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX334_MS_ATT2 | 0x40025BB8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX334_MS_ATT3 | 0x40025BBC | FULL | Master attributes 3 |

## 23.352 PPU_FX 335

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX335_SL_ADDR | 0x40025BC0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX335_SL_SIZE | 0x40025BC4 | FULL | Slave region, size |
| PERI_MS_PPU_FX335_SL_ATT0 | 0x40025BD0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX335_SL_ATT1 | 0x40025BD4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX335_SL_ATT2 | 0x40025BD8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX335_SL_ATT3 | 0x40025BDC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX335_MS_ADDR | 0x40025BE0 | FULL | Master region, base address |
| PERI_MS_PPU_FX335_MS_SIZE | 0x40025BE4 | FULL | Master region, size |
| PERI_MS_PPU_FX335_MS_ATT0 | 0x40025BF0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX335_MS_ATT1 | 0x40025BF4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX335_MS_ATT2 | 0x40025BF8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX335_MS_ATT3 | 0x40025BFC | FULL | Master attributes 3 |

## 23.353 PPU_FX 336

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX336_SL_ADDR | 0x40025C00 | FULL | Slave region, base address |
| PERI_MS_PPU_FX336_SL_SIZE | 0x40025C04 | FULL | Slave region, size |
| PERI_MS_PPU_FX336_SL_ATT0 | 0x40025C10 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX336_SL_ATT1 | 0x40025C14 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX336_SL_ATT2 | 0x40025C18 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX336_SL_ATT3 | 0x40025C1C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX336_MS_ADDR | 0x40025C20 | FULL | Master region, base address |
| PERI_MS_PPU_FX336_MS_SIZE | 0x40025C24 | FULL | Master region, size |
| PERI_MS_PPU_FX336_MS_ATT0 | 0x40025C30 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX336_MS_ATT1 | 0x40025C34 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX336_MS_ATT2 | 0x40025C38 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX336_MS_ATT3 | 0x40025C3C | FULL | Master attributes 3 |

## 23.354 PPU_FX 337

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX337_SL_ADDR | 0x40025C40 | FULL | Slave region, base address |
| PERI_MS_PPU_FX337_SL_SIZE | 0x40025C44 | FULL | Slave region, size |
| PERI_MS_PPU_FX337_SL_ATT0 | 0x40025C50 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX337_SL_ATT1 | 0x40025C54 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX337_SL_ATT2 | 0x40025C58 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX337_SL_ATT3 | 0x40025C5C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX337_MS_ADDR | 0x40025C60 | FULL | Master region, base address |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX337_MS_SIZE | 0x40025C64 | FULL | Master region, size |
| PERI_MS_PPU_FX337_MS_ATT0 | 0x40025C70 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX337_MS_ATT1 | 0x40025C74 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX337_MS_ATT2 | 0x40025C78 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX337_MS_ATT3 | 0x40025C7C | FULL | Master attributes 3 |

## 23.355 PPU_FX 338

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX338_SL_ADDR | 0x40025C80 | FULL | Slave region, base address |
| PERI_MS_PPU_FX338_SL_SIZE | 0x40025C84 | FULL | Slave region, size |
| PERI_MS_PPU_FX338_SL_ATT0 | 0x40025C90 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX338_SL_ATT1 | 0x40025C94 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX338_SL_ATT2 | 0x40025C98 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX338_SL_ATT3 | 0x40025C9C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX338_MS_ADDR | 0x40025CA0 | FULL | Master region, base address |
| PERI_MS_PPU_FX338_MS_SIZE | 0x40025CA4 | FULL | Master region, size |
| PERI_MS_PPU_FX338_MS_ATT0 | 0x40025CB0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX338_MS_ATT1 | 0x40025CB4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX338_MS_ATT2 | 0x40025CB8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX338_MS_ATT3 | 0x40025CBC | FULL | Master attributes 3 |

## 23.356 PPU_FX 339

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX339_SL_ADDR | 0x40025CC0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX339_SL_SIZE | 0x40025CC4 | FULL | Slave region, size |
| PERI_MS_PPU_FX339_SL_ATT0 | 0x40025CD0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX339_SL_ATT1 | 0x40025CD4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX339_SL_ATT2 | 0x40025CD8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX339_SL_ATT3 | 0x40025CDC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX339_MS_ADDR | 0x40025CE0 | FULL | Master region, base address |
| PERI_MS_PPU_FX339_MS_SIZE | 0x40025CE4 | FULL | Master region, size |
| PERI_MS_PPU_FX339_MS_ATT0 | 0x40025CF0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX339_MS_ATT1 | 0x40025CF4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX339_MS_ATT2 | 0x40025CF8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX339_MS_ATT3 | 0x40025CFC | FULL | Master attributes 3 |

## 23.357 PPU_FX 340

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX340_SL_ADDR | 0x40025D00 | FULL | Slave region, base address |
| PERI_MS_PPU_FX340_SL_SIZE | 0x40025D04 | FULL | Slave region, size |
| PERI_MS_PPU_FX340_SL_ATT0 | 0x40025D10 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX340_SL_ATT1 | 0x40025D14 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX340_SL_ATT2 | 0x40025D18 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX340_SL_ATT3 | 0x40025D1C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX340_MS_ADDR | 0x40025D20 | FULL | Master region, base address |
| PERI_MS_PPU_FX340_MS_SIZE | 0x40025D24 | FULL | Master region, size |
| PERI_MS_PPU_FX340_MS_ATT0 | 0x40025D30 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX340_MS_ATT1 | 0x40025D34 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX340_MS_ATT2 | 0x40025D38 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX340_MS_ATT3 | 0x40025D3C | FULL | Master attributes 3 |

## 23.358 PPU_FX 341

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX341_SL_ADDR | 0x40025D40 | FULL | Slave region, base address |
| PERI_MS_PPU_FX341_SL_SIZE | 0x40025D44 | FULL | Slave region, size |
| PERI_MS_PPU_FX341_SL_ATT0 | 0x40025D50 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX341_SL_ATT1 | 0x40025D54 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX341_SL_ATT2 | 0x40025D58 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX341_SL_ATT3 | 0x40025D5C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX341_MS_ADDR | 0x40025D60 | FULL | Master region, base address |
| PERI_MS_PPU_FX341_MS_SIZE | 0x40025D64 | FULL | Master region, size |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX341_MS_ATT0 | 0x40025D70 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX341_MS_ATT1 | 0x40025D74 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX341_MS_ATT2 | 0x40025D78 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX341_MS_ATT3 | 0x40025D7C | FULL | Master attributes 3 |

## 23.359 PPU_FX 342

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX342_SL_ADDR | 0x40025D80 | FULL | Slave region, base address |
| PERI_MS_PPU_FX342_SL_SIZE | 0x40025D84 | FULL | Slave region, size |
| PERI_MS_PPU_FX342_SL_ATT0 | 0x40025D90 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX342_SL_ATT1 | 0x40025D94 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX342_SL_ATT2 | 0x40025D98 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX342_SL_ATT3 | 0x40025D9C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX342_MS_ADDR | 0x40025DA0 | FULL | Master region, base address |
| PERI_MS_PPU_FX342_MS_SIZE | 0x40025DA4 | FULL | Master region, size |
| PERI_MS_PPU_FX342_MS_ATT0 | 0x40025DB0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX342_MS_ATT1 | 0x40025DB4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX342_MS_ATT2 | 0x40025DB8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX342_MS_ATT3 | 0x40025DBC | FULL | Master attributes 3 |

## 23.360 PPU_FX 343

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX343_SL_ADDR | 0x40025DC0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX343_SL_SIZE | 0x40025DC4 | FULL | Slave region, size |
| PERI_MS_PPU_FX343_SL_ATT0 | 0x40025DD0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX343_SL_ATT1 | 0x40025DD4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX343_SL_ATT2 | 0x40025DD8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX343_SL_ATT3 | 0x40025DDC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX343_MS_ADDR | 0x40025DE0 | FULL | Master region, base address |
| PERI_MS_PPU_FX343_MS_SIZE | 0x40025DE4 | FULL | Master region, size |
| PERI_MS_PPU_FX343_MS_ATT0 | 0x40025DF0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX343_MS_ATT1 | 0x40025DF4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX343_MS_ATT2 | 0x40025DF8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX343_MS_ATT3 | 0x40025DFC | FULL | Master attributes 3 |

## 23.361 PPU_FX 344

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX344_SL_ADDR | 0x40025E00 | FULL | Slave region, base address |
| PERI_MS_PPU_FX344_SL_SIZE | 0x40025E04 | FULL | Slave region, size |
| PERI_MS_PPU_FX344_SL_ATT0 | 0x40025E10 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX344_SL_ATT1 | 0x40025E14 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX344_SL_ATT2 | 0x40025E18 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX344_SL_ATT3 | 0x40025E1C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX344_MS_ADDR | 0x40025E20 | FULL | Master region, base address |
| PERI_MS_PPU_FX344_MS_SIZE | 0x40025E24 | FULL | Master region, size |
| PERI_MS_PPU_FX344_MS_ATT0 | 0x40025E30 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX344_MS_ATT1 | 0x40025E34 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX344_MS_ATT2 | 0x40025E38 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX344_MS_ATT3 | 0x40025E3C | FULL | Master attributes 3 |

## 23.362 PPU_FX 345

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX345_SL_ADDR | 0x40025E40 | FULL | Slave region, base address |
| PERI_MS_PPU_FX345_SL_SIZE | 0x40025E44 | FULL | Slave region, size |
| PERI_MS_PPU_FX345_SL_ATT0 | 0x40025E50 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX345_SL_ATT1 | 0x40025E54 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX345_SL_ATT2 | 0x40025E58 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX345_SL_ATT3 | 0x40025E5C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX345_MS_ADDR | 0x40025E60 | FULL | Master region, base address |
| PERI_MS_PPU_FX345_MS_SIZE | 0x40025E64 | FULL | Master region, size |
| PERI_MS_PPU_FX345_MS_ATT0 | 0x40025E70 | FULL | Master attributes 0 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX345_MS_ATT1 | 0x40025E74 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX345_MS_ATT2 | 0x40025E78 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX345_MS_ATT3 | 0x40025E7C | FULL | Master attributes 3 |

## 23.363 PPU_FX 346

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX346_SL_ADDR | 0x40025E80 | FULL | Slave region, base address |
| PERI_MS_PPU_FX346_SL_SIZE | 0x40025E84 | FULL | Slave region, size |
| PERI_MS_PPU_FX346_SL_ATT0 | 0x40025E90 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX346_SL_ATT1 | 0x40025E94 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX346_SL_ATT2 | 0x40025E98 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX346_SL_ATT3 | 0x40025E9C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX346_MS_ADDR | 0x40025EA0 | FULL | Master region, base address |
| PERI_MS_PPU_FX346_MS_SIZE | 0x40025EA4 | FULL | Master region, size |
| PERI_MS_PPU_FX346_MS_ATT0 | 0x40025EB0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX346_MS_ATT1 | 0x40025EB4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX346_MS_ATT2 | 0x40025EB8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX346_MS_ATT3 | 0x40025EBC | FULL | Master attributes 3 |

## 23.364 PPU_FX 347

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX347_SL_ADDR | 0x40025EC0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX347_SL_SIZE | 0x40025EC4 | FULL | Slave region, size |
| PERI_MS_PPU_FX347_SL_ATT0 | 0x40025ED0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX347_SL_ATT1 | 0x40025ED4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX347_SL_ATT2 | 0x40025ED8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX347_SL_ATT3 | 0x40025EDC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX347_MS_ADDR | 0x40025EE0 | FULL | Master region, base address |
| PERI_MS_PPU_FX347_MS_SIZE | 0x40025EE4 | FULL | Master region, size |
| PERI_MS_PPU_FX347_MS_ATT0 | 0x40025EF0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX347_MS_ATT1 | 0x40025EF4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX347_MS_ATT2 | 0x40025EF8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX347_MS_ATT3 | 0x40025EFC | FULL | Master attributes 3 |

## 23.365 PPU_FX 348

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX348_SL_ADDR | 0x40025F00 | FULL | Slave region, base address |
| PERI_MS_PPU_FX348_SL_SIZE | 0x40025F04 | FULL | Slave region, size |
| PERI_MS_PPU_FX348_SL_ATT0 | 0x40025F10 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX348_SL_ATT1 | 0x40025F14 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX348_SL_ATT2 | 0x40025F18 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX348_SL_ATT3 | 0x40025F1C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX348_MS_ADDR | 0x40025F20 | FULL | Master region, base address |
| PERI_MS_PPU_FX348_MS_SIZE | 0x40025F24 | FULL | Master region, size |
| PERI_MS_PPU_FX348_MS_ATT0 | 0x40025F30 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX348_MS_ATT1 | 0x40025F34 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX348_MS_ATT2 | 0x40025F38 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX348_MS_ATT3 | 0x40025F3C | FULL | Master attributes 3 |

## 23.366 PPU_FX 349

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX349_SL_ADDR | 0x40025F40 | FULL | Slave region, base address |
| PERI_MS_PPU_FX349_SL_SIZE | 0x40025F44 | FULL | Slave region, size |
| PERI_MS_PPU_FX349_SL_ATT0 | 0x40025F50 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX349_SL_ATT1 | 0x40025F54 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX349_SL_ATT2 | 0x40025F58 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX349_SL_ATT3 | 0x40025F5C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX349_MS_ADDR | 0x40025F60 | FULL | Master region, base address |
| PERI_MS_PPU_FX349_MS_SIZE | 0x40025F64 | FULL | Master region, size |
| PERI_MS_PPU_FX349_MS_ATT0 | 0x40025F70 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX349_MS_ATT1 | 0x40025F74 | FULL | Master attributes 1 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX349_MS_ATT2 | 0x40025F78 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX349_MS_ATT3 | 0x40025F7C | FULL | Master attributes 3 |

## 23.367 PPU_FX 350

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX350_SL_ADDR | 0x40025F80 | FULL | Slave region, base address |
| PERI_MS_PPU_FX350_SL_SIZE | 0x40025F84 | FULL | Slave region, size |
| PERI_MS_PPU_FX350_SL_ATT0 | 0x40025F90 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX350_SL_ATT1 | 0x40025F94 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX350_SL_ATT2 | 0x40025F98 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX350_SL_ATT3 | 0x40025F9C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX350_MS_ADDR | 0x40025FA0 | FULL | Master region, base address |
| PERI_MS_PPU_FX350_MS_SIZE | 0x40025FA4 | FULL | Master region, size |
| PERI_MS_PPU_FX350_MS_ATT0 | 0x40025FB0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX350_MS_ATT1 | 0x40025FB4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX350_MS_ATT2 | 0x40025FB8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX350_MS_ATT3 | 0x40025FBC | FULL | Master attributes 3 |

## 23.368 PPU_FX 351

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX351_SL_ADDR | 0x40025FC0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX351_SL_SIZE | 0x40025FC4 | FULL | Slave region, size |
| PERI_MS_PPU_FX351_SL_ATT0 | 0x40025FD0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX351_SL_ATT1 | 0x40025FD4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX351_SL_ATT2 | 0x40025FD8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX351_SL_ATT3 | 0x40025FDC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX351_MS_ADDR | 0x40025FE0 | FULL | Master region, base address |
| PERI_MS_PPU_FX351_MS_SIZE | 0x40025FE4 | FULL | Master region, size |
| PERI_MS_PPU_FX351_MS_ATT0 | 0x40025FF0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX351_MS_ATT1 | 0x40025FF4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX351_MS_ATT2 | 0x40025FF8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX351_MS_ATT3 | 0x40025FFC | FULL | Master attributes 3 |

## 23.369 PPU_FX 352

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX352_SL_ADDR | 0x40026000 | FULL | Slave region, base address |
| PERI_MS_PPU_FX352_SL_SIZE | 0x40026004 | FULL | Slave region, size |
| PERI_MS_PPU_FX352_SL_ATT0 | 0x40026010 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX352_SL_ATT1 | 0x40026014 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX352_SL_ATT2 | 0x40026018 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX352_SL_ATT3 | 0x4002601C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX352_MS_ADDR | 0x40026020 | FULL | Master region, base address |
| PERI_MS_PPU_FX352_MS_SIZE | 0x40026024 | FULL | Master region, size |
| PERI_MS_PPU_FX352_MS_ATT0 | 0x40026030 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX352_MS_ATT1 | 0x40026034 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX352_MS_ATT2 | 0x40026038 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX352_MS_ATT3 | 0x4002603C | FULL | Master attributes 3 |

## 23.370 PPU_FX 353

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX353_SL_ADDR | 0x40026040 | FULL | Slave region, base address |
| PERI_MS_PPU_FX353_SL_SIZE | 0x40026044 | FULL | Slave region, size |
| PERI_MS_PPU_FX353_SL_ATT0 | 0x40026050 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX353_SL_ATT1 | 0x40026054 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX353_SL_ATT2 | 0x40026058 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX353_SL_ATT3 | 0x4002605C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX353_MS_ADDR | 0x40026060 | FULL | Master region, base address |
| PERI_MS_PPU_FX353_MS_SIZE | 0x40026064 | FULL | Master region, size |
| PERI_MS_PPU_FX353_MS_ATT0 | 0x40026070 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX353_MS_ATT1 | 0x40026074 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX353_MS_ATT2 | 0x40026078 | FULL | Master attributes 2 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX353_MS_ATT3 | 0x4002607C | FULL | Master attributes 3 |

## 23.371 PPU_FX 354

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX354_SL_ADDR | 0x40026080 | FULL | Slave region, base address |
| PERI_MS_PPU_FX354_SL_SIZE | 0x40026084 | FULL | Slave region, size |
| PERI_MS_PPU_FX354_SL_ATT0 | 0x40026090 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX354_SL_ATT1 | 0x40026094 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX354_SL_ATT2 | 0x40026098 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX354_SL_ATT3 | 0x4002609C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX354_MS_ADDR | 0x400260A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX354_MS_SIZE | 0x400260A4 | FULL | Master region, size |
| PERI_MS_PPU_FX354_MS_ATT0 | 0x400260B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX354_MS_ATT1 | 0x400260B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX354_MS_ATT2 | 0x400260B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX354_MS_ATT3 | 0x400260BC | FULL | Master attributes 3 |

## 23.372 PPU_FX 355

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX355_SL_ADDR | 0x400260C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX355_SL_SIZE | 0x400260C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX355_SL_ATT0 | 0x400260D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX355_SL_ATT1 | 0x400260D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX355_SL_ATT2 | 0x400260D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX355_SL_ATT3 | 0x400260DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX355_MS_ADDR | 0x400260E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX355_MS_SIZE | 0x400260E4 | FULL | Master region, size |
| PERI_MS_PPU_FX355_MS_ATT0 | 0x400260F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX355_MS_ATT1 | 0x400260F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX355_MS_ATT2 | 0x400260F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX355_MS_ATT3 | 0x400260FC | FULL | Master attributes 3 |

## 23.373 PPU_FX 356

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX356_SL_ADDR | 0x40026100 | FULL | Slave region, base address |
| PERI_MS_PPU_FX356_SL_SIZE | 0x40026104 | FULL | Slave region, size |
| PERI_MS_PPU_FX356_SL_ATT0 | 0x40026110 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX356_SL_ATT1 | 0x40026114 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX356_SL_ATT2 | 0x40026118 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX356_SL_ATT3 | 0x4002611C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX356_MS_ADDR | 0x40026120 | FULL | Master region, base address |
| PERI_MS_PPU_FX356_MS_SIZE | 0x40026124 | FULL | Master region, size |
| PERI_MS_PPU_FX356_MS_ATT0 | 0x40026130 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX356_MS_ATT1 | 0x40026134 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX356_MS_ATT2 | 0x40026138 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX356_MS_ATT3 | 0x4002613C | FULL | Master attributes 3 |

## 23.374 PPU_FX 357

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX357_SL_ADDR | 0x40026140 | FULL | Slave region, base address |
| PERI_MS_PPU_FX357_SL_SIZE | 0x40026144 | FULL | Slave region, size |
| PERI_MS_PPU_FX357_SL_ATT0 | 0x40026150 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX357_SL_ATT1 | 0x40026154 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX357_SL_ATT2 | 0x40026158 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX357_SL_ATT3 | 0x4002615C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX357_MS_ADDR | 0x40026160 | FULL | Master region, base address |
| PERI_MS_PPU_FX357_MS_SIZE | 0x40026164 | FULL | Master region, size |
| PERI_MS_PPU_FX357_MS_ATT0 | 0x40026170 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX357_MS_ATT1 | 0x40026174 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX357_MS_ATT2 | 0x40026178 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX357_MS_ATT3 | 0x4002617C | FULL | Master attributes 3 |

## 23.375 PPU_FX 358

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX358_SL_ADDR | 0x40026180 | FULL | Slave region, base address |
| PERI_MS_PPU_FX358_SL_SIZE | 0x40026184 | FULL | Slave region, size |
| PERI_MS_PPU_FX358_SL_ATT0 | 0x40026190 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX358_SL_ATT1 | 0x40026194 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX358_SL_ATT2 | 0x40026198 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX358_SL_ATT3 | 0x4002619C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX358_MS_ADDR | 0x400261A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX358_MS_SIZE | 0x400261A4 | FULL | Master region, size |
| PERI_MS_PPU_FX358_MS_ATT0 | 0x400261B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX358_MS_ATT1 | 0x400261B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX358_MS_ATT2 | 0x400261B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX358_MS_ATT3 | 0x400261BC | FULL | Master attributes 3 |

## 23.376 PPU_FX 359

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX359_SL_ADDR | 0x400261C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX359_SL_SIZE | 0x400261C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX359_SL_ATT0 | 0x400261D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX359_SL_ATT1 | 0x400261D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX359_SL_ATT2 | 0x400261D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX359_SL_ATT3 | 0x400261DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX359_MS_ADDR | 0x400261E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX359_MS_SIZE | 0x400261E4 | FULL | Master region, size |
| PERI_MS_PPU_FX359_MS_ATT0 | 0x400261F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX359_MS_ATT1 | 0x400261F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX359_MS_ATT2 | 0x400261F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX359_MS_ATT3 | 0x400261FC | FULL | Master attributes 3 |

## 23.377 PPU_FX 360

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX360_SL_ADDR | 0x40026200 | FULL | Slave region, base address |
| PERI_MS_PPU_FX360_SL_SIZE | 0x40026204 | FULL | Slave region, size |
| PERI_MS_PPU_FX360_SL_ATT0 | 0x40026210 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX360_SL_ATT1 | 0x40026214 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX360_SL_ATT2 | 0x40026218 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX360_SL_ATT3 | 0x4002621C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX360_MS_ADDR | 0x40026220 | FULL | Master region, base address |
| PERI_MS_PPU_FX360_MS_SIZE | 0x40026224 | FULL | Master region, size |
| PERI_MS_PPU_FX360_MS_ATT0 | 0x40026230 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX360_MS_ATT1 | 0x40026234 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX360_MS_ATT2 | 0x40026238 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX360_MS_ATT3 | 0x4002623C | FULL | Master attributes 3 |

## 23.378 PPU_FX 361

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX361_SL_ADDR | 0x40026240 | FULL | Slave region, base address |
| PERI_MS_PPU_FX361_SL_SIZE | 0x40026244 | FULL | Slave region, size |
| PERI_MS_PPU_FX361_SL_ATT0 | 0x40026250 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX361_SL_ATT1 | 0x40026254 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX361_SL_ATT2 | 0x40026258 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX361_SL_ATT3 | 0x4002625C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX361_MS_ADDR | 0x40026260 | FULL | Master region, base address |
| PERI_MS_PPU_FX361_MS_SIZE | 0x40026264 | FULL | Master region, size |
| PERI_MS_PPU_FX361_MS_ATT0 | 0x40026270 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX361_MS_ATT1 | 0x40026274 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX361_MS_ATT2 | 0x40026278 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX361_MS_ATT3 | 0x4002627C | FULL | Master attributes 3 |

## 23.379 PPU_FX 362

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX362_SL_ADDR | 0x40026280 | FULL | Slave region, base address |
| PERI_MS_PPU_FX362_SL_SIZE | 0x40026284 | FULL | Slave region, size |
| PERI_MS_PPU_FX362_SL_ATT0 | 0x40026290 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX362_SL_ATT1 | 0x40026294 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX362_SL_ATT2 | 0x40026298 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX362_SL_ATT3 | 0x4002629C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX362_MS_ADDR | 0x400262A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX362_MS_SIZE | 0x400262A4 | FULL | Master region, size |
| PERI_MS_PPU_FX362_MS_ATT0 | 0x400262B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX362_MS_ATT1 | 0x400262B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX362_MS_ATT2 | 0x400262B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX362_MS_ATT3 | 0x400262BC | FULL | Master attributes 3 |

## 23.380 PPU_FX 363

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX363_SL_ADDR | 0x400262C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX363_SL_SIZE | 0x400262C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX363_SL_ATT0 | 0x400262D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX363_SL_ATT1 | 0x400262D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX363_SL_ATT2 | 0x400262D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX363_SL_ATT3 | 0x400262DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX363_MS_ADDR | 0x400262E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX363_MS_SIZE | 0x400262E4 | FULL | Master region, size |
| PERI_MS_PPU_FX363_MS_ATT0 | 0x400262F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX363_MS_ATT1 | 0x400262F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX363_MS_ATT2 | 0x400262F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX363_MS_ATT3 | 0x400262FC | FULL | Master attributes 3 |

## 23.381 PPU_FX 364

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX364_SL_ADDR | 0x40026300 | FULL | Slave region, base address |
| PERI_MS_PPU_FX364_SL_SIZE | 0x40026304 | FULL | Slave region, size |
| PERI_MS_PPU_FX364_SL_ATT0 | 0x40026310 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX364_SL_ATT1 | 0x40026314 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX364_SL_ATT2 | 0x40026318 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX364_SL_ATT3 | 0x4002631C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX364_MS_ADDR | 0x40026320 | FULL | Master region, base address |
| PERI_MS_PPU_FX364_MS_SIZE | 0x40026324 | FULL | Master region, size |
| PERI_MS_PPU_FX364_MS_ATT0 | 0x40026330 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX364_MS_ATT1 | 0x40026334 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX364_MS_ATT2 | 0x40026338 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX364_MS_ATT3 | 0x4002633C | FULL | Master attributes 3 |

## 23.382 PPU_FX 365

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX365_SL_ADDR | 0x40026340 | FULL | Slave region, base address |
| PERI_MS_PPU_FX365_SL_SIZE | 0x40026344 | FULL | Slave region, size |
| PERI_MS_PPU_FX365_SL_ATT0 | 0x40026350 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX365_SL_ATT1 | 0x40026354 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX365_SL_ATT2 | 0x40026358 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX365_SL_ATT3 | 0x4002635C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX365_MS_ADDR | 0x40026360 | FULL | Master region, base address |
| PERI_MS_PPU_FX365_MS_SIZE | 0x40026364 | FULL | Master region, size |
| PERI_MS_PPU_FX365_MS_ATT0 | 0x40026370 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX365_MS_ATT1 | 0x40026374 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX365_MS_ATT2 | 0x40026378 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX365_MS_ATT3 | 0x4002637C | FULL | Master attributes 3 |

## 23.383 PPU_FX 366

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX366_SL_ADDR | 0x40026380 | FULL | Slave region, base address |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX366_SL_SIZE | 0x40026384 | FULL | Slave region, size |
| PERI_MS_PPU_FX366_SL_ATT0 | 0x40026390 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX366_SL_ATT1 | 0x40026394 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX366_SL_ATT2 | 0x40026398 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX366_SL_ATT3 | 0x4002639C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX366_MS_ADDR | 0x400263A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX366_MS_SIZE | 0x400263A4 | FULL | Master region, size |
| PERI_MS_PPU_FX366_MS_ATT0 | 0x400263B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX366_MS_ATT1 | 0x400263B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX366_MS_ATT2 | 0x400263B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX366_MS_ATT3 | 0x400263BC | FULL | Master attributes 3 |

## 23.384 PPU_FX 367

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX367_SL_ADDR | 0x400263C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX367_SL_SIZE | 0x400263C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX367_SL_ATT0 | 0x400263D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX367_SL_ATT1 | 0x400263D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX367_SL_ATT2 | 0x400263D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX367_SL_ATT3 | 0x400263DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX367_MS_ADDR | 0x400263E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX367_MS_SIZE | 0x400263E4 | FULL | Master region, size |
| PERI_MS_PPU_FX367_MS_ATT0 | 0x400263F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX367_MS_ATT1 | 0x400263F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX367_MS_ATT2 | 0x400263F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX367_MS_ATT3 | 0x400263FC | FULL | Master attributes 3 |

## 23.385 PPU_FX 368

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX368_SL_ADDR | 0x40026400 | FULL | Slave region, base address |
| PERI_MS_PPU_FX368_SL_SIZE | 0x40026404 | FULL | Slave region, size |
| PERI_MS_PPU_FX368_SL_ATT0 | 0x40026410 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX368_SL_ATT1 | 0x40026414 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX368_SL_ATT2 | 0x40026418 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX368_SL_ATT3 | 0x4002641C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX368_MS_ADDR | 0x40026420 | FULL | Master region, base address |
| PERI_MS_PPU_FX368_MS_SIZE | 0x40026424 | FULL | Master region, size |
| PERI_MS_PPU_FX368_MS_ATT0 | 0x40026430 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX368_MS_ATT1 | 0x40026434 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX368_MS_ATT2 | 0x40026438 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX368_MS_ATT3 | 0x4002643C | FULL | Master attributes 3 |

## 23.386 PPU_FX 369

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX369_SL_ADDR | 0x40026440 | FULL | Slave region, base address |
| PERI_MS_PPU_FX369_SL_SIZE | 0x40026444 | FULL | Slave region, size |
| PERI_MS_PPU_FX369_SL_ATT0 | 0x40026450 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX369_SL_ATT1 | 0x40026454 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX369_SL_ATT2 | 0x40026458 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX369_SL_ATT3 | 0x4002645C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX369_MS_ADDR | 0x40026460 | FULL | Master region, base address |
| PERI_MS_PPU_FX369_MS_SIZE | 0x40026464 | FULL | Master region, size |
| PERI_MS_PPU_FX369_MS_ATT0 | 0x40026470 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX369_MS_ATT1 | 0x40026474 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX369_MS_ATT2 | 0x40026478 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX369_MS_ATT3 | 0x4002647C | FULL | Master attributes 3 |

## 23.387 PPU_FX 370

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX370_SL_ADDR | 0x40026480 | FULL | Slave region, base address |
| PERI_MS_PPU_FX370_SL_SIZE | 0x40026484 | FULL | Slave region, size |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX370_SL_ATT0 | 0x40026490 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX370_SL_ATT1 | 0x40026494 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX370_SL_ATT2 | 0x40026498 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX370_SL_ATT3 | 0x4002649C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX370_MS_ADDR | 0x400264A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX370_MS_SIZE | 0x400264A4 | FULL | Master region, size |
| PERI_MS_PPU_FX370_MS_ATT0 | 0x400264B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX370_MS_ATT1 | 0x400264B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX370_MS_ATT2 | 0x400264B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX370_MS_ATT3 | 0x400264BC | FULL | Master attributes 3 |

## 23.388 PPU_FX 371

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX371_SL_ADDR | 0x400264C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX371_SL_SIZE | 0x400264C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX371_SL_ATT0 | 0x400264D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX371_SL_ATT1 | 0x400264D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX371_SL_ATT2 | 0x400264D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX371_SL_ATT3 | 0x400264DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX371_MS_ADDR | 0x400264E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX371_MS_SIZE | 0x400264E4 | FULL | Master region, size |
| PERI_MS_PPU_FX371_MS_ATT0 | 0x400264F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX371_MS_ATT1 | 0x400264F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX371_MS_ATT2 | 0x400264F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX371_MS_ATT3 | 0x400264FC | FULL | Master attributes 3 |

## 23.389 PPU_FX 372

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX372_SL_ADDR | 0x40026500 | FULL | Slave region, base address |
| PERI_MS_PPU_FX372_SL_SIZE | 0x40026504 | FULL | Slave region, size |
| PERI_MS_PPU_FX372_SL_ATT0 | 0x40026510 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX372_SL_ATT1 | 0x40026514 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX372_SL_ATT2 | 0x40026518 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX372_SL_ATT3 | 0x4002651C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX372_MS_ADDR | 0x40026520 | FULL | Master region, base address |
| PERI_MS_PPU_FX372_MS_SIZE | 0x40026524 | FULL | Master region, size |
| PERI_MS_PPU_FX372_MS_ATT0 | 0x40026530 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX372_MS_ATT1 | 0x40026534 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX372_MS_ATT2 | 0x40026538 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX372_MS_ATT3 | 0x4002653C | FULL | Master attributes 3 |

## 23.390 PPU_FX 373

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX373_SL_ADDR | 0x40026540 | FULL | Slave region, base address |
| PERI_MS_PPU_FX373_SL_SIZE | 0x40026544 | FULL | Slave region, size |
| PERI_MS_PPU_FX373_SL_ATT0 | 0x40026550 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX373_SL_ATT1 | 0x40026554 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX373_SL_ATT2 | 0x40026558 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX373_SL_ATT3 | 0x4002655C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX373_MS_ADDR | 0x40026560 | FULL | Master region, base address |
| PERI_MS_PPU_FX373_MS_SIZE | 0x40026564 | FULL | Master region, size |
| PERI_MS_PPU_FX373_MS_ATT0 | 0x40026570 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX373_MS_ATT1 | 0x40026574 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX373_MS_ATT2 | 0x40026578 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX373_MS_ATT3 | 0x4002657C | FULL | Master attributes 3 |

## 23.391 PPU_FX 374

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX374_SL_ADDR | 0x40026580 | FULL | Slave region, base address |
| PERI_MS_PPU_FX374_SL_SIZE | 0x40026584 | FULL | Slave region, size |
| PERI_MS_PPU_FX374_SL_ATT0 | 0x40026590 | FULL | Slave attributes 0 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX374_SL_ATT1 | 0x40026594 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX374_SL_ATT2 | 0x40026598 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX374_SL_ATT3 | 0x4002659C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX374_MS_ADDR | 0x400265A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX374_MS_SIZE | 0x400265A4 | FULL | Master region, size |
| PERI_MS_PPU_FX374_MS_ATT0 | 0x400265B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX374_MS_ATT1 | 0x400265B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX374_MS_ATT2 | 0x400265B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX374_MS_ATT3 | 0x400265BC | FULL | Master attributes 3 |

## 23.392 PPU_FX 375

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX375_SL_ADDR | 0x400265C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX375_SL_SIZE | 0x400265C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX375_SL_ATT0 | 0x400265D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX375_SL_ATT1 | 0x400265D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX375_SL_ATT2 | 0x400265D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX375_SL_ATT3 | 0x400265DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX375_MS_ADDR | 0x400265E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX375_MS_SIZE | 0x400265E4 | FULL | Master region, size |
| PERI_MS_PPU_FX375_MS_ATT0 | 0x400265F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX375_MS_ATT1 | 0x400265F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX375_MS_ATT2 | 0x400265F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX375_MS_ATT3 | 0x400265FC | FULL | Master attributes 3 |

## 23.393 PPU_FX 376

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX376_SL_ADDR | 0x40026600 | FULL | Slave region, base address |
| PERI_MS_PPU_FX376_SL_SIZE | 0x40026604 | FULL | Slave region, size |
| PERI_MS_PPU_FX376_SL_ATT0 | 0x40026610 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX376_SL_ATT1 | 0x40026614 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX376_SL_ATT2 | 0x40026618 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX376_SL_ATT3 | 0x4002661C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX376_MS_ADDR | 0x40026620 | FULL | Master region, base address |
| PERI_MS_PPU_FX376_MS_SIZE | 0x40026624 | FULL | Master region, size |
| PERI_MS_PPU_FX376_MS_ATT0 | 0x40026630 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX376_MS_ATT1 | 0x40026634 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX376_MS_ATT2 | 0x40026638 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX376_MS_ATT3 | 0x4002663C | FULL | Master attributes 3 |

## 23.394 PPU_FX 377

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX377_SL_ADDR | 0x40026640 | FULL | Slave region, base address |
| PERI_MS_PPU_FX377_SL_SIZE | 0x40026644 | FULL | Slave region, size |
| PERI_MS_PPU_FX377_SL_ATT0 | 0x40026650 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX377_SL_ATT1 | 0x40026654 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX377_SL_ATT2 | 0x40026658 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX377_SL_ATT3 | 0x4002665C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX377_MS_ADDR | 0x40026660 | FULL | Master region, base address |
| PERI_MS_PPU_FX377_MS_SIZE | 0x40026664 | FULL | Master region, size |
| PERI_MS_PPU_FX377_MS_ATT0 | 0x40026670 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX377_MS_ATT1 | 0x40026674 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX377_MS_ATT2 | 0x40026678 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX377_MS_ATT3 | 0x4002667C | FULL | Master attributes 3 |

## 23.395 PPU_FX 378

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX378_SL_ADDR | 0x40026680 | FULL | Slave region, base address |
| PERI_MS_PPU_FX378_SL_SIZE | 0x40026684 | FULL | Slave region, size |
| PERI_MS_PPU_FX378_SL_ATT0 | 0x40026690 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX378_SL_ATT1 | 0x40026694 | FULL | Slave attributes 1 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX378_SL_ATT2 | 0x40026698 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX378_SL_ATT3 | 0x4002669C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX378_MS_ADDR | 0x400266A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX378_MS_SIZE | 0x400266A4 | FULL | Master region, size |
| PERI_MS_PPU_FX378_MS_ATT0 | 0x400266B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX378_MS_ATT1 | 0x400266B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX378_MS_ATT2 | 0x400266B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX378_MS_ATT3 | 0x400266BC | FULL | Master attributes 3 |

## 23.396 PPU_FX 379

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX379_SL_ADDR | 0x400266C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX379_SL_SIZE | 0x400266C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX379_SL_ATT0 | 0x400266D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX379_SL_ATT1 | 0x400266D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX379_SL_ATT2 | 0x400266D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX379_SL_ATT3 | 0x400266DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX379_MS_ADDR | 0x400266E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX379_MS_SIZE | 0x400266E4 | FULL | Master region, size |
| PERI_MS_PPU_FX379_MS_ATT0 | 0x400266F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX379_MS_ATT1 | 0x400266F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX379_MS_ATT2 | 0x400266F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX379_MS_ATT3 | 0x400266FC | FULL | Master attributes 3 |

## 23.397 PPU_FX 380

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX380_SL_ADDR | 0x40026700 | FULL | Slave region, base address |
| PERI_MS_PPU_FX380_SL_SIZE | 0x40026704 | FULL | Slave region, size |
| PERI_MS_PPU_FX380_SL_ATT0 | 0x40026710 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX380_SL_ATT1 | 0x40026714 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX380_SL_ATT2 | 0x40026718 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX380_SL_ATT3 | 0x4002671C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX380_MS_ADDR | 0x40026720 | FULL | Master region, base address |
| PERI_MS_PPU_FX380_MS_SIZE | 0x40026724 | FULL | Master region, size |
| PERI_MS_PPU_FX380_MS_ATT0 | 0x40026730 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX380_MS_ATT1 | 0x40026734 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX380_MS_ATT2 | 0x40026738 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX380_MS_ATT3 | 0x4002673C | FULL | Master attributes 3 |

## 23.398 PPU_FX 381

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX381_SL_ADDR | 0x40026740 | FULL | Slave region, base address |
| PERI_MS_PPU_FX381_SL_SIZE | 0x40026744 | FULL | Slave region, size |
| PERI_MS_PPU_FX381_SL_ATT0 | 0x40026750 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX381_SL_ATT1 | 0x40026754 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX381_SL_ATT2 | 0x40026758 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX381_SL_ATT3 | 0x4002675C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX381_MS_ADDR | 0x40026760 | FULL | Master region, base address |
| PERI_MS_PPU_FX381_MS_SIZE | 0x40026764 | FULL | Master region, size |
| PERI_MS_PPU_FX381_MS_ATT0 | 0x40026770 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX381_MS_ATT1 | 0x40026774 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX381_MS_ATT2 | 0x40026778 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX381_MS_ATT3 | 0x4002677C | FULL | Master attributes 3 |

## 23.399 PPU_FX 382

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX382_SL_ADDR | 0x40026780 | FULL | Slave region, base address |
| PERI_MS_PPU_FX382_SL_SIZE | 0x40026784 | FULL | Slave region, size |
| PERI_MS_PPU_FX382_SL_ATT0 | 0x40026790 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX382_SL_ATT1 | 0x40026794 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX382_SL_ATT2 | 0x40026798 | FULL | Slave attributes 2 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX382_SL_ATT3 | 0x4002679C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX382_MS_ADDR | 0x400267A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX382_MS_SIZE | 0x400267A4 | FULL | Master region, size |
| PERI_MS_PPU_FX382_MS_ATT0 | 0x400267B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX382_MS_ATT1 | 0x400267B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX382_MS_ATT2 | 0x400267B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX382_MS_ATT3 | 0x400267BC | FULL | Master attributes 3 |

## 23.400 PPU_FX 383

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX383_SL_ADDR | 0x400267C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX383_SL_SIZE | 0x400267C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX383_SL_ATT0 | 0x400267D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX383_SL_ATT1 | 0x400267D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX383_SL_ATT2 | 0x400267D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX383_SL_ATT3 | 0x400267DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX383_MS_ADDR | 0x400267E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX383_MS_SIZE | 0x400267E4 | FULL | Master region, size |
| PERI_MS_PPU_FX383_MS_ATT0 | 0x400267F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX383_MS_ATT1 | 0x400267F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX383_MS_ATT2 | 0x400267F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX383_MS_ATT3 | 0x400267FC | FULL | Master attributes 3 |

## 23.401 PPU_FX 384

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX384_SL_ADDR | 0x40026800 | FULL | Slave region, base address |
| PERI_MS_PPU_FX384_SL_SIZE | 0x40026804 | FULL | Slave region, size |
| PERI_MS_PPU_FX384_SL_ATT0 | 0x40026810 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX384_SL_ATT1 | 0x40026814 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX384_SL_ATT2 | 0x40026818 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX384_SL_ATT3 | 0x4002681C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX384_MS_ADDR | 0x40026820 | FULL | Master region, base address |
| PERI_MS_PPU_FX384_MS_SIZE | 0x40026824 | FULL | Master region, size |
| PERI_MS_PPU_FX384_MS_ATT0 | 0x40026830 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX384_MS_ATT1 | 0x40026834 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX384_MS_ATT2 | 0x40026838 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX384_MS_ATT3 | 0x4002683C | FULL | Master attributes 3 |

## 23.402 PPU_FX 385

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX385_SL_ADDR | 0x40026840 | FULL | Slave region, base address |
| PERI_MS_PPU_FX385_SL_SIZE | 0x40026844 | FULL | Slave region, size |
| PERI_MS_PPU_FX385_SL_ATT0 | 0x40026850 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX385_SL_ATT1 | 0x40026854 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX385_SL_ATT2 | 0x40026858 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX385_SL_ATT3 | 0x4002685C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX385_MS_ADDR | 0x40026860 | FULL | Master region, base address |
| PERI_MS_PPU_FX385_MS_SIZE | 0x40026864 | FULL | Master region, size |
| PERI_MS_PPU_FX385_MS_ATT0 | 0x40026870 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX385_MS_ATT1 | 0x40026874 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX385_MS_ATT2 | 0x40026878 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX385_MS_ATT3 | 0x4002687C | FULL | Master attributes 3 |

## 23.403 PPU_FX 386

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX386_SL_ADDR | 0x40026880 | FULL | Slave region, base address |
| PERI_MS_PPU_FX386_SL_SIZE | 0x40026884 | FULL | Slave region, size |
| PERI_MS_PPU_FX386_SL_ATT0 | 0x40026890 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX386_SL_ATT1 | 0x40026894 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX386_SL_ATT2 | 0x40026898 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX386_SL_ATT3 | 0x4002689C | FULL | Slave attributes 3 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX386_MS_ADDR | 0x400268A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX386_MS_SIZE | 0x400268A4 | FULL | Master region, size |
| PERI_MS_PPU_FX386_MS_ATT0 | 0x400268B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX386_MS_ATT1 | 0x400268B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX386_MS_ATT2 | 0x400268B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX386_MS_ATT3 | 0x400268BC | FULL | Master attributes 3 |

## 23.404 PPU_FX 387

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX387_SL_ADDR | 0x400268C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX387_SL_SIZE | 0x400268C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX387_SL_ATT0 | 0x400268D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX387_SL_ATT1 | 0x400268D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX387_SL_ATT2 | 0x400268D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX387_SL_ATT3 | 0x400268DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX387_MS_ADDR | 0x400268E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX387_MS_SIZE | 0x400268E4 | FULL | Master region, size |
| PERI_MS_PPU_FX387_MS_ATT0 | 0x400268F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX387_MS_ATT1 | 0x400268F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX387_MS_ATT2 | 0x400268F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX387_MS_ATT3 | 0x400268FC | FULL | Master attributes 3 |

## 23.405 PPU_FX 388

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX388_SL_ADDR | 0x40026900 | FULL | Slave region, base address |
| PERI_MS_PPU_FX388_SL_SIZE | 0x40026904 | FULL | Slave region, size |
| PERI_MS_PPU_FX388_SL_ATT0 | 0x40026910 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX388_SL_ATT1 | 0x40026914 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX388_SL_ATT2 | 0x40026918 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX388_SL_ATT3 | 0x4002691C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX388_MS_ADDR | 0x40026920 | FULL | Master region, base address |
| PERI_MS_PPU_FX388_MS_SIZE | 0x40026924 | FULL | Master region, size |
| PERI_MS_PPU_FX388_MS_ATT0 | 0x40026930 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX388_MS_ATT1 | 0x40026934 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX388_MS_ATT2 | 0x40026938 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX388_MS_ATT3 | 0x4002693C | FULL | Master attributes 3 |

## 23.406 PPU_FX 389

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX389_SL_ADDR | 0x40026940 | FULL | Slave region, base address |
| PERI_MS_PPU_FX389_SL_SIZE | 0x40026944 | FULL | Slave region, size |
| PERI_MS_PPU_FX389_SL_ATT0 | 0x40026950 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX389_SL_ATT1 | 0x40026954 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX389_SL_ATT2 | 0x40026958 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX389_SL_ATT3 | 0x4002695C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX389_MS_ADDR | 0x40026960 | FULL | Master region, base address |
| PERI_MS_PPU_FX389_MS_SIZE | 0x40026964 | FULL | Master region, size |
| PERI_MS_PPU_FX389_MS_ATT0 | 0x40026970 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX389_MS_ATT1 | 0x40026974 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX389_MS_ATT2 | 0x40026978 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX389_MS_ATT3 | 0x4002697C | FULL | Master attributes 3 |

## 23.407 PPU_FX 390

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX390_SL_ADDR | 0x40026980 | FULL | Slave region, base address |
| PERI_MS_PPU_FX390_SL_SIZE | 0x40026984 | FULL | Slave region, size |
| PERI_MS_PPU_FX390_SL_ATT0 | 0x40026990 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX390_SL_ATT1 | 0x40026994 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX390_SL_ATT2 | 0x40026998 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX390_SL_ATT3 | 0x4002699C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX390_MS_ADDR | 0x400269A0 | FULL | Master region, base address |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX390_MS_SIZE | 0x400269A4 | FULL | Master region, size |
| PERI_MS_PPU_FX390_MS_ATT0 | 0x400269B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX390_MS_ATT1 | 0x400269B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX390_MS_ATT2 | 0x400269B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX390_MS_ATT3 | 0x400269BC | FULL | Master attributes 3 |

## 23.408 PPU_FX 391

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX391_SL_ADDR | 0x400269C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX391_SL_SIZE | 0x400269C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX391_SL_ATT0 | 0x400269D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX391_SL_ATT1 | 0x400269D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX391_SL_ATT2 | 0x400269D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX391_SL_ATT3 | 0x400269DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX391_MS_ADDR | 0x400269E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX391_MS_SIZE | 0x400269E4 | FULL | Master region, size |
| PERI_MS_PPU_FX391_MS_ATT0 | 0x400269F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX391_MS_ATT1 | 0x400269F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX391_MS_ATT2 | 0x400269F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX391_MS_ATT3 | 0x400269FC | FULL | Master attributes 3 |

## 23.409 PPU_FX 392

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX392_SL_ADDR | 0x40026A00 | FULL | Slave region, base address |
| PERI_MS_PPU_FX392_SL_SIZE | 0x40026A04 | FULL | Slave region, size |
| PERI_MS_PPU_FX392_SL_ATT0 | 0x40026A10 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX392_SL_ATT1 | 0x40026A14 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX392_SL_ATT2 | 0x40026A18 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX392_SL_ATT3 | 0x40026A1C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX392_MS_ADDR | 0x40026A20 | FULL | Master region, base address |
| PERI_MS_PPU_FX392_MS_SIZE | 0x40026A24 | FULL | Master region, size |
| PERI_MS_PPU_FX392_MS_ATT0 | 0x40026A30 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX392_MS_ATT1 | 0x40026A34 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX392_MS_ATT2 | 0x40026A38 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX392_MS_ATT3 | 0x40026A3C | FULL | Master attributes 3 |

## 23.410 PPU_FX 393

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX393_SL_ADDR | 0x40026A40 | FULL | Slave region, base address |
| PERI_MS_PPU_FX393_SL_SIZE | 0x40026A44 | FULL | Slave region, size |
| PERI_MS_PPU_FX393_SL_ATT0 | 0x40026A50 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX393_SL_ATT1 | 0x40026A54 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX393_SL_ATT2 | 0x40026A58 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX393_SL_ATT3 | 0x40026A5C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX393_MS_ADDR | 0x40026A60 | FULL | Master region, base address |
| PERI_MS_PPU_FX393_MS_SIZE | 0x40026A64 | FULL | Master region, size |
| PERI_MS_PPU_FX393_MS_ATT0 | 0x40026A70 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX393_MS_ATT1 | 0x40026A74 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX393_MS_ATT2 | 0x40026A78 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX393_MS_ATT3 | 0x40026A7C | FULL | Master attributes 3 |

## 23.411 PPU_FX 394

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX394_SL_ADDR | 0x40026A80 | FULL | Slave region, base address |
| PERI_MS_PPU_FX394_SL_SIZE | 0x40026A84 | FULL | Slave region, size |
| PERI_MS_PPU_FX394_SL_ATT0 | 0x40026A90 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX394_SL_ATT1 | 0x40026A94 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX394_SL_ATT2 | 0x40026A98 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX394_SL_ATT3 | 0x40026A9C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX394_MS_ADDR | 0x40026AA0 | FULL | Master region, base address |
| PERI_MS_PPU_FX394_MS_SIZE | 0x40026AA4 | FULL | Master region, size |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX394_MS_ATT0 | 0x40026AB0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX394_MS_ATT1 | 0x40026AB4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX394_MS_ATT2 | 0x40026AB8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX394_MS_ATT3 | 0x40026ABC | FULL | Master attributes 3 |

## 23.412 PPU_FX 395

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX395_SL_ADDR | 0x40026AC0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX395_SL_SIZE | 0x40026AC4 | FULL | Slave region, size |
| PERI_MS_PPU_FX395_SL_ATT0 | 0x40026AD0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX395_SL_ATT1 | 0x40026AD4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX395_SL_ATT2 | 0x40026AD8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX395_SL_ATT3 | 0x40026ADC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX395_MS_ADDR | 0x40026AE0 | FULL | Master region, base address |
| PERI_MS_PPU_FX395_MS_SIZE | 0x40026AE4 | FULL | Master region, size |
| PERI_MS_PPU_FX395_MS_ATT0 | 0x40026AF0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX395_MS_ATT1 | 0x40026AF4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX395_MS_ATT2 | 0x40026AF8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX395_MS_ATT3 | 0x40026AFC | FULL | Master attributes 3 |

## 23.413 PPU_FX 396

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX396_SL_ADDR | 0x40026B00 | FULL | Slave region, base address |
| PERI_MS_PPU_FX396_SL_SIZE | 0x40026B04 | FULL | Slave region, size |
| PERI_MS_PPU_FX396_SL_ATT0 | 0x40026B10 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX396_SL_ATT1 | 0x40026B14 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX396_SL_ATT2 | 0x40026B18 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX396_SL_ATT3 | 0x40026B1C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX396_MS_ADDR | 0x40026B20 | FULL | Master region, base address |
| PERI_MS_PPU_FX396_MS_SIZE | 0x40026B24 | FULL | Master region, size |
| PERI_MS_PPU_FX396_MS_ATT0 | 0x40026B30 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX396_MS_ATT1 | 0x40026B34 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX396_MS_ATT2 | 0x40026B38 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX396_MS_ATT3 | 0x40026B3C | FULL | Master attributes 3 |

## 23.414 PPU_FX 397

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX397_SL_ADDR | 0x40026B40 | FULL | Slave region, base address |
| PERI_MS_PPU_FX397_SL_SIZE | 0x40026B44 | FULL | Slave region, size |
| PERI_MS_PPU_FX397_SL_ATT0 | 0x40026B50 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX397_SL_ATT1 | 0x40026B54 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX397_SL_ATT2 | 0x40026B58 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX397_SL_ATT3 | 0x40026B5C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX397_MS_ADDR | 0x40026B60 | FULL | Master region, base address |
| PERI_MS_PPU_FX397_MS_SIZE | 0x40026B64 | FULL | Master region, size |
| PERI_MS_PPU_FX397_MS_ATT0 | 0x40026B70 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX397_MS_ATT1 | 0x40026B74 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX397_MS_ATT2 | 0x40026B78 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX397_MS_ATT3 | 0x40026B7C | FULL | Master attributes 3 |

## 23.415 PPU_FX 398

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX398_SL_ADDR | 0x40026B80 | FULL | Slave region, base address |
| PERI_MS_PPU_FX398_SL_SIZE | 0x40026B84 | FULL | Slave region, size |
| PERI_MS_PPU_FX398_SL_ATT0 | 0x40026B90 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX398_SL_ATT1 | 0x40026B94 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX398_SL_ATT2 | 0x40026B98 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX398_SL_ATT3 | 0x40026B9C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX398_MS_ADDR | 0x40026BA0 | FULL | Master region, base address |
| PERI_MS_PPU_FX398_MS_SIZE | 0x40026BA4 | FULL | Master region, size |
| PERI_MS_PPU_FX398_MS_ATT0 | 0x40026BB0 | FULL | Master attributes 0 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX398_MS_ATT1 | 0x40026BB4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX398_MS_ATT2 | 0x40026BB8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX398_MS_ATT3 | 0x40026BBC | FULL | Master attributes 3 |

## 23.416 PPU_FX 399

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX399_SL_ADDR | 0x40026BC0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX399_SL_SIZE | 0x40026BC4 | FULL | Slave region, size |
| PERI_MS_PPU_FX399_SL_ATT0 | 0x40026BD0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX399_SL_ATT1 | 0x40026BD4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX399_SL_ATT2 | 0x40026BD8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX399_SL_ATT3 | 0x40026BDC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX399_MS_ADDR | 0x40026BE0 | FULL | Master region, base address |
| PERI_MS_PPU_FX399_MS_SIZE | 0x40026BE4 | FULL | Master region, size |
| PERI_MS_PPU_FX399_MS_ATT0 | 0x40026BF0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX399_MS_ATT1 | 0x40026BF4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX399_MS_ATT2 | 0x40026BF8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX399_MS_ATT3 | 0x40026BFC | FULL | Master attributes 3 |

## 23.417 PPU_FX 400

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX400_SL_ADDR | 0x40026C00 | FULL | Slave region, base address |
| PERI_MS_PPU_FX400_SL_SIZE | 0x40026C04 | FULL | Slave region, size |
| PERI_MS_PPU_FX400_SL_ATT0 | 0x40026C10 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX400_SL_ATT1 | 0x40026C14 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX400_SL_ATT2 | 0x40026C18 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX400_SL_ATT3 | 0x40026C1C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX400_MS_ADDR | 0x40026C20 | FULL | Master region, base address |
| PERI_MS_PPU_FX400_MS_SIZE | 0x40026C24 | FULL | Master region, size |
| PERI_MS_PPU_FX400_MS_ATT0 | 0x40026C30 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX400_MS_ATT1 | 0x40026C34 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX400_MS_ATT2 | 0x40026C38 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX400_MS_ATT3 | 0x40026C3C | FULL | Master attributes 3 |

## 23.418 PPU_FX 401

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX401_SL_ADDR | 0x40026C40 | FULL | Slave region, base address |
| PERI_MS_PPU_FX401_SL_SIZE | 0x40026C44 | FULL | Slave region, size |
| PERI_MS_PPU_FX401_SL_ATT0 | 0x40026C50 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX401_SL_ATT1 | 0x40026C54 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX401_SL_ATT2 | 0x40026C58 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX401_SL_ATT3 | 0x40026C5C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX401_MS_ADDR | 0x40026C60 | FULL | Master region, base address |
| PERI_MS_PPU_FX401_MS_SIZE | 0x40026C64 | FULL | Master region, size |
| PERI_MS_PPU_FX401_MS_ATT0 | 0x40026C70 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX401_MS_ATT1 | 0x40026C74 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX401_MS_ATT2 | 0x40026C78 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX401_MS_ATT3 | 0x40026C7C | FULL | Master attributes 3 |

## 23.419 PPU_FX 402

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX402_SL_ADDR | 0x40026C80 | FULL | Slave region, base address |
| PERI_MS_PPU_FX402_SL_SIZE | 0x40026C84 | FULL | Slave region, size |
| PERI_MS_PPU_FX402_SL_ATT0 | 0x40026C90 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX402_SL_ATT1 | 0x40026C94 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX402_SL_ATT2 | 0x40026C98 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX402_SL_ATT3 | 0x40026C9C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX402_MS_ADDR | 0x40026CA0 | FULL | Master region, base address |
| PERI_MS_PPU_FX402_MS_SIZE | 0x40026CA4 | FULL | Master region, size |
| PERI_MS_PPU_FX402_MS_ATT0 | 0x40026CB0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX402_MS_ATT1 | 0x40026CB4 | FULL | Master attributes 1 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX402_MS_ATT2 | 0x40026CB8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX402_MS_ATT3 | 0x40026CBC | FULL | Master attributes 3 |

## 23.420 PPU_FX 403

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX403_SL_ADDR | 0x40026CC0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX403_SL_SIZE | 0x40026CC4 | FULL | Slave region, size |
| PERI_MS_PPU_FX403_SL_ATT0 | 0x40026CD0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX403_SL_ATT1 | 0x40026CD4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX403_SL_ATT2 | 0x40026CD8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX403_SL_ATT3 | 0x40026CDC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX403_MS_ADDR | 0x40026CE0 | FULL | Master region, base address |
| PERI_MS_PPU_FX403_MS_SIZE | 0x40026CE4 | FULL | Master region, size |
| PERI_MS_PPU_FX403_MS_ATT0 | 0x40026CF0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX403_MS_ATT1 | 0x40026CF4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX403_MS_ATT2 | 0x40026CF8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX403_MS_ATT3 | 0x40026CFC | FULL | Master attributes 3 |

## 23.421 PPU_FX 404

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX404_SL_ADDR | 0x40026D00 | FULL | Slave region, base address |
| PERI_MS_PPU_FX404_SL_SIZE | 0x40026D04 | FULL | Slave region, size |
| PERI_MS_PPU_FX404_SL_ATT0 | 0x40026D10 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX404_SL_ATT1 | 0x40026D14 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX404_SL_ATT2 | 0x40026D18 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX404_SL_ATT3 | 0x40026D1C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX404_MS_ADDR | 0x40026D20 | FULL | Master region, base address |
| PERI_MS_PPU_FX404_MS_SIZE | 0x40026D24 | FULL | Master region, size |
| PERI_MS_PPU_FX404_MS_ATT0 | 0x40026D30 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX404_MS_ATT1 | 0x40026D34 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX404_MS_ATT2 | 0x40026D38 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX404_MS_ATT3 | 0x40026D3C | FULL | Master attributes 3 |

## 23.422 PPU_FX 405

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX405_SL_ADDR | 0x40026D40 | FULL | Slave region, base address |
| PERI_MS_PPU_FX405_SL_SIZE | 0x40026D44 | FULL | Slave region, size |
| PERI_MS_PPU_FX405_SL_ATT0 | 0x40026D50 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX405_SL_ATT1 | 0x40026D54 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX405_SL_ATT2 | 0x40026D58 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX405_SL_ATT3 | 0x40026D5C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX405_MS_ADDR | 0x40026D60 | FULL | Master region, base address |
| PERI_MS_PPU_FX405_MS_SIZE | 0x40026D64 | FULL | Master region, size |
| PERI_MS_PPU_FX405_MS_ATT0 | 0x40026D70 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX405_MS_ATT1 | 0x40026D74 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX405_MS_ATT2 | 0x40026D78 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX405_MS_ATT3 | 0x40026D7C | FULL | Master attributes 3 |

## 23.423 PPU_FX 406

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX406_SL_ADDR | 0x40026D80 | FULL | Slave region, base address |
| PERI_MS_PPU_FX406_SL_SIZE | 0x40026D84 | FULL | Slave region, size |
| PERI_MS_PPU_FX406_SL_ATT0 | 0x40026D90 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX406_SL_ATT1 | 0x40026D94 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX406_SL_ATT2 | 0x40026D98 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX406_SL_ATT3 | 0x40026D9C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX406_MS_ADDR | 0x40026DA0 | FULL | Master region, base address |
| PERI_MS_PPU_FX406_MS_SIZE | 0x40026DA4 | FULL | Master region, size |
| PERI_MS_PPU_FX406_MS_ATT0 | 0x40026DB0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX406_MS_ATT1 | 0x40026DB4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX406_MS_ATT2 | 0x40026DB8 | FULL | Master attributes 2 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX406_MS_ATT3 | 0x40026DBC | FULL | Master attributes 3 |

## 23.424 PPU_FX 407

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX407_SL_ADDR | 0x40026DC0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX407_SL_SIZE | 0x40026DC4 | FULL | Slave region, size |
| PERI_MS_PPU_FX407_SL_ATT0 | 0x40026DD0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX407_SL_ATT1 | 0x40026DD4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX407_SL_ATT2 | 0x40026DD8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX407_SL_ATT3 | 0x40026DDC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX407_MS_ADDR | 0x40026DE0 | FULL | Master region, base address |
| PERI_MS_PPU_FX407_MS_SIZE | 0x40026DE4 | FULL | Master region, size |
| PERI_MS_PPU_FX407_MS_ATT0 | 0x40026DF0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX407_MS_ATT1 | 0x40026DF4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX407_MS_ATT2 | 0x40026DF8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX407_MS_ATT3 | 0x40026DFC | FULL | Master attributes 3 |

## 23.425 PPU_FX 408

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX408_SL_ADDR | 0x40026E00 | FULL | Slave region, base address |
| PERI_MS_PPU_FX408_SL_SIZE | 0x40026E04 | FULL | Slave region, size |
| PERI_MS_PPU_FX408_SL_ATT0 | 0x40026E10 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX408_SL_ATT1 | 0x40026E14 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX408_SL_ATT2 | 0x40026E18 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX408_SL_ATT3 | 0x40026E1C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX408_MS_ADDR | 0x40026E20 | FULL | Master region, base address |
| PERI_MS_PPU_FX408_MS_SIZE | 0x40026E24 | FULL | Master region, size |
| PERI_MS_PPU_FX408_MS_ATT0 | 0x40026E30 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX408_MS_ATT1 | 0x40026E34 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX408_MS_ATT2 | 0x40026E38 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX408_MS_ATT3 | 0x40026E3C | FULL | Master attributes 3 |

## 23.426 PPU_FX 409

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX409_SL_ADDR | 0x40026E40 | FULL | Slave region, base address |
| PERI_MS_PPU_FX409_SL_SIZE | 0x40026E44 | FULL | Slave region, size |
| PERI_MS_PPU_FX409_SL_ATT0 | 0x40026E50 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX409_SL_ATT1 | 0x40026E54 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX409_SL_ATT2 | 0x40026E58 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX409_SL_ATT3 | 0x40026E5C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX409_MS_ADDR | 0x40026E60 | FULL | Master region, base address |
| PERI_MS_PPU_FX409_MS_SIZE | 0x40026E64 | FULL | Master region, size |
| PERI_MS_PPU_FX409_MS_ATT0 | 0x40026E70 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX409_MS_ATT1 | 0x40026E74 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX409_MS_ATT2 | 0x40026E78 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX409_MS_ATT3 | 0x40026E7C | FULL | Master attributes 3 |

## 23.427 PPU_FX 410

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX410_SL_ADDR | 0x40026E80 | FULL | Slave region, base address |
| PERI_MS_PPU_FX410_SL_SIZE | 0x40026E84 | FULL | Slave region, size |
| PERI_MS_PPU_FX410_SL_ATT0 | 0x40026E90 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX410_SL_ATT1 | 0x40026E94 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX410_SL_ATT2 | 0x40026E98 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX410_SL_ATT3 | 0x40026E9C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX410_MS_ADDR | 0x40026EA0 | FULL | Master region, base address |
| PERI_MS_PPU_FX410_MS_SIZE | 0x40026EA4 | FULL | Master region, size |
| PERI_MS_PPU_FX410_MS_ATT0 | 0x40026EB0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX410_MS_ATT1 | 0x40026EB4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX410_MS_ATT2 | 0x40026EB8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX410_MS_ATT3 | 0x40026EBC | FULL | Master attributes 3 |

## 23.428 PPU_FX 411

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX411_SL_ADDR | 0x40026EC0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX411_SL_SIZE | 0x40026EC4 | FULL | Slave region, size |
| PERI_MS_PPU_FX411_SL_ATT0 | 0x40026ED0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX411_SL_ATT1 | 0x40026ED4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX411_SL_ATT2 | 0x40026ED8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX411_SL_ATT3 | 0x40026EDC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX411_MS_ADDR | 0x40026EE0 | FULL | Master region, base address |
| PERI_MS_PPU_FX411_MS_SIZE | 0x40026EE4 | FULL | Master region, size |
| PERI_MS_PPU_FX411_MS_ATT0 | 0x40026EF0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX411_MS_ATT1 | 0x40026EF4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX411_MS_ATT2 | 0x40026EF8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX411_MS_ATT3 | 0x40026EFC | FULL | Master attributes 3 |

## 23.429 PPU_FX 412

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX412_SL_ADDR | 0x40026F00 | FULL | Slave region, base address |
| PERI_MS_PPU_FX412_SL_SIZE | 0x40026F04 | FULL | Slave region, size |
| PERI_MS_PPU_FX412_SL_ATT0 | 0x40026F10 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX412_SL_ATT1 | 0x40026F14 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX412_SL_ATT2 | 0x40026F18 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX412_SL_ATT3 | 0x40026F1C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX412_MS_ADDR | 0x40026F20 | FULL | Master region, base address |
| PERI_MS_PPU_FX412_MS_SIZE | 0x40026F24 | FULL | Master region, size |
| PERI_MS_PPU_FX412_MS_ATT0 | 0x40026F30 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX412_MS_ATT1 | 0x40026F34 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX412_MS_ATT2 | 0x40026F38 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX412_MS_ATT3 | 0x40026F3C | FULL | Master attributes 3 |

## 23.430 PPU_FX 413

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX413_SL_ADDR | 0x40026F40 | FULL | Slave region, base address |
| PERI_MS_PPU_FX413_SL_SIZE | 0x40026F44 | FULL | Slave region, size |
| PERI_MS_PPU_FX413_SL_ATT0 | 0x40026F50 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX413_SL_ATT1 | 0x40026F54 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX413_SL_ATT2 | 0x40026F58 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX413_SL_ATT3 | 0x40026F5C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX413_MS_ADDR | 0x40026F60 | FULL | Master region, base address |
| PERI_MS_PPU_FX413_MS_SIZE | 0x40026F64 | FULL | Master region, size |
| PERI_MS_PPU_FX413_MS_ATT0 | 0x40026F70 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX413_MS_ATT1 | 0x40026F74 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX413_MS_ATT2 | 0x40026F78 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX413_MS_ATT3 | 0x40026F7C | FULL | Master attributes 3 |

## 23.431 PPU_FX 414

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX414_SL_ADDR | 0x40026F80 | FULL | Slave region, base address |
| PERI_MS_PPU_FX414_SL_SIZE | 0x40026F84 | FULL | Slave region, size |
| PERI_MS_PPU_FX414_SL_ATT0 | 0x40026F90 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX414_SL_ATT1 | 0x40026F94 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX414_SL_ATT2 | 0x40026F98 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX414_SL_ATT3 | 0x40026F9C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX414_MS_ADDR | 0x40026FA0 | FULL | Master region, base address |
| PERI_MS_PPU_FX414_MS_SIZE | 0x40026FA4 | FULL | Master region, size |
| PERI_MS_PPU_FX414_MS_ATT0 | 0x40026FB0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX414_MS_ATT1 | 0x40026FB4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX414_MS_ATT2 | 0x40026FB8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX414_MS_ATT3 | 0x40026FBC | FULL | Master attributes 3 |

## 23.432 PPU_FX 415

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX415_SL_ADDR | 0x40026FC0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX415_SL_SIZE | 0x40026FC4 | FULL | Slave region, size |
| PERI_MS_PPU_FX415_SL_ATT0 | 0x40026FD0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX415_SL_ATT1 | 0x40026FD4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX415_SL_ATT2 | 0x40026FD8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX415_SL_ATT3 | 0x40026FDC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX415_MS_ADDR | 0x40026FE0 | FULL | Master region, base address |
| PERI_MS_PPU_FX415_MS_SIZE | 0x40026FE4 | FULL | Master region, size |
| PERI_MS_PPU_FX415_MS_ATT0 | 0x40026FF0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX415_MS_ATT1 | 0x40026FF4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX415_MS_ATT2 | 0x40026FF8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX415_MS_ATT3 | 0x40026FFC | FULL | Master attributes 3 |

## 23.433 PPU_FX 416

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX416_SL_ADDR | 0x40027000 | FULL | Slave region, base address |
| PERI_MS_PPU_FX416_SL_SIZE | 0x40027004 | FULL | Slave region, size |
| PERI_MS_PPU_FX416_SL_ATT0 | 0x40027010 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX416_SL_ATT1 | 0x40027014 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX416_SL_ATT2 | 0x40027018 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX416_SL_ATT3 | 0x4002701C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX416_MS_ADDR | 0x40027020 | FULL | Master region, base address |
| PERI_MS_PPU_FX416_MS_SIZE | 0x40027024 | FULL | Master region, size |
| PERI_MS_PPU_FX416_MS_ATT0 | 0x40027030 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX416_MS_ATT1 | 0x40027034 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX416_MS_ATT2 | 0x40027038 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX416_MS_ATT3 | 0x4002703C | FULL | Master attributes 3 |

## 23.434 PPU_FX 417

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX417_SL_ADDR | 0x40027040 | FULL | Slave region, base address |
| PERI_MS_PPU_FX417_SL_SIZE | 0x40027044 | FULL | Slave region, size |
| PERI_MS_PPU_FX417_SL_ATT0 | 0x40027050 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX417_SL_ATT1 | 0x40027054 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX417_SL_ATT2 | 0x40027058 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX417_SL_ATT3 | 0x4002705C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX417_MS_ADDR | 0x40027060 | FULL | Master region, base address |
| PERI_MS_PPU_FX417_MS_SIZE | 0x40027064 | FULL | Master region, size |
| PERI_MS_PPU_FX417_MS_ATT0 | 0x40027070 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX417_MS_ATT1 | 0x40027074 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX417_MS_ATT2 | 0x40027078 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX417_MS_ATT3 | 0x4002707C | FULL | Master attributes 3 |

## 23.435 PPU_FX 418

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX418_SL_ADDR | 0x40027080 | FULL | Slave region, base address |
| PERI_MS_PPU_FX418_SL_SIZE | 0x40027084 | FULL | Slave region, size |
| PERI_MS_PPU_FX418_SL_ATT0 | 0x40027090 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX418_SL_ATT1 | 0x40027094 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX418_SL_ATT2 | 0x40027098 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX418_SL_ATT3 | 0x4002709C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX418_MS_ADDR | 0x400270A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX418_MS_SIZE | 0x400270A4 | FULL | Master region, size |
| PERI_MS_PPU_FX418_MS_ATT0 | 0x400270B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX418_MS_ATT1 | 0x400270B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX418_MS_ATT2 | 0x400270B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX418_MS_ATT3 | 0x400270BC | FULL | Master attributes 3 |

## 23.436 PPU_FX 419

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX419_SL_ADDR | 0x400270C0 | FULL | Slave region, base address |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX419_SL_SIZE | 0x400270C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX419_SL_ATT0 | 0x400270D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX419_SL_ATT1 | 0x400270D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX419_SL_ATT2 | 0x400270D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX419_SL_ATT3 | 0x400270DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX419_MS_ADDR | 0x400270E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX419_MS_SIZE | 0x400270E4 | FULL | Master region, size |
| PERI_MS_PPU_FX419_MS_ATT0 | 0x400270F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX419_MS_ATT1 | 0x400270F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX419_MS_ATT2 | 0x400270F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX419_MS_ATT3 | 0x400270FC | FULL | Master attributes 3 |

## 23.437 PPU_FX 420

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX420_SL_ADDR | 0x40027100 | FULL | Slave region, base address |
| PERI_MS_PPU_FX420_SL_SIZE | 0x40027104 | FULL | Slave region, size |
| PERI_MS_PPU_FX420_SL_ATT0 | 0x40027110 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX420_SL_ATT1 | 0x40027114 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX420_SL_ATT2 | 0x40027118 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX420_SL_ATT3 | 0x4002711C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX420_MS_ADDR | 0x40027120 | FULL | Master region, base address |
| PERI_MS_PPU_FX420_MS_SIZE | 0x40027124 | FULL | Master region, size |
| PERI_MS_PPU_FX420_MS_ATT0 | 0x40027130 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX420_MS_ATT1 | 0x40027134 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX420_MS_ATT2 | 0x40027138 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX420_MS_ATT3 | 0x4002713C | FULL | Master attributes 3 |

## 23.438 PPU_FX 421

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX421_SL_ADDR | 0x40027140 | FULL | Slave region, base address |
| PERI_MS_PPU_FX421_SL_SIZE | 0x40027144 | FULL | Slave region, size |
| PERI_MS_PPU_FX421_SL_ATT0 | 0x40027150 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX421_SL_ATT1 | 0x40027154 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX421_SL_ATT2 | 0x40027158 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX421_SL_ATT3 | 0x4002715C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX421_MS_ADDR | 0x40027160 | FULL | Master region, base address |
| PERI_MS_PPU_FX421_MS_SIZE | 0x40027164 | FULL | Master region, size |
| PERI_MS_PPU_FX421_MS_ATT0 | 0x40027170 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX421_MS_ATT1 | 0x40027174 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX421_MS_ATT2 | 0x40027178 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX421_MS_ATT3 | 0x4002717C | FULL | Master attributes 3 |

## 23.439 PPU_FX 422

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX422_SL_ADDR | 0x40027180 | FULL | Slave region, base address |
| PERI_MS_PPU_FX422_SL_SIZE | 0x40027184 | FULL | Slave region, size |
| PERI_MS_PPU_FX422_SL_ATT0 | 0x40027190 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX422_SL_ATT1 | 0x40027194 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX422_SL_ATT2 | 0x40027198 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX422_SL_ATT3 | 0x4002719C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX422_MS_ADDR | 0x400271A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX422_MS_SIZE | 0x400271A4 | FULL | Master region, size |
| PERI_MS_PPU_FX422_MS_ATT0 | 0x400271B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX422_MS_ATT1 | 0x400271B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX422_MS_ATT2 | 0x400271B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX422_MS_ATT3 | 0x400271BC | FULL | Master attributes 3 |

## 23.440 PPU_FX 423

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX423_SL_ADDR | 0x400271C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX423_SL_SIZE | 0x400271C4 | FULL | Slave region, size |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX423_SL_ATT0 | 0x400271D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX423_SL_ATT1 | 0x400271D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX423_SL_ATT2 | 0x400271D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX423_SL_ATT3 | 0x400271DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX423_MS_ADDR | 0x400271E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX423_MS_SIZE | 0x400271E4 | FULL | Master region, size |
| PERI_MS_PPU_FX423_MS_ATT0 | 0x400271F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX423_MS_ATT1 | 0x400271F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX423_MS_ATT2 | 0x400271F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX423_MS_ATT3 | 0x400271FC | FULL | Master attributes 3 |

## 23.441 PPU_FX 424

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX424_SL_ADDR | 0x40027200 | FULL | Slave region, base address |
| PERI_MS_PPU_FX424_SL_SIZE | 0x40027204 | FULL | Slave region, size |
| PERI_MS_PPU_FX424_SL_ATT0 | 0x40027210 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX424_SL_ATT1 | 0x40027214 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX424_SL_ATT2 | 0x40027218 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX424_SL_ATT3 | 0x4002721C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX424_MS_ADDR | 0x40027220 | FULL | Master region, base address |
| PERI_MS_PPU_FX424_MS_SIZE | 0x40027224 | FULL | Master region, size |
| PERI_MS_PPU_FX424_MS_ATT0 | 0x40027230 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX424_MS_ATT1 | 0x40027234 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX424_MS_ATT2 | 0x40027238 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX424_MS_ATT3 | 0x4002723C | FULL | Master attributes 3 |

## 23.442 PPU_FX 425

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX425_SL_ADDR | 0x40027240 | FULL | Slave region, base address |
| PERI_MS_PPU_FX425_SL_SIZE | 0x40027244 | FULL | Slave region, size |
| PERI_MS_PPU_FX425_SL_ATT0 | 0x40027250 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX425_SL_ATT1 | 0x40027254 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX425_SL_ATT2 | 0x40027258 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX425_SL_ATT3 | 0x4002725C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX425_MS_ADDR | 0x40027260 | FULL | Master region, base address |
| PERI_MS_PPU_FX425_MS_SIZE | 0x40027264 | FULL | Master region, size |
| PERI_MS_PPU_FX425_MS_ATT0 | 0x40027270 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX425_MS_ATT1 | 0x40027274 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX425_MS_ATT2 | 0x40027278 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX425_MS_ATT3 | 0x4002727C | FULL | Master attributes 3 |

## 23.443 PPU_FX 426

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX426_SL_ADDR | 0x40027280 | FULL | Slave region, base address |
| PERI_MS_PPU_FX426_SL_SIZE | 0x40027284 | FULL | Slave region, size |
| PERI_MS_PPU_FX426_SL_ATT0 | 0x40027290 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX426_SL_ATT1 | 0x40027294 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX426_SL_ATT2 | 0x40027298 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX426_SL_ATT3 | 0x4002729C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX426_MS_ADDR | 0x400272A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX426_MS_SIZE | 0x400272A4 | FULL | Master region, size |
| PERI_MS_PPU_FX426_MS_ATT0 | 0x400272B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX426_MS_ATT1 | 0x400272B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX426_MS_ATT2 | 0x400272B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX426_MS_ATT3 | 0x400272BC | FULL | Master attributes 3 |

## 23.444 PPU_FX 427

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX427_SL_ADDR | 0x400272C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX427_SL_SIZE | 0x400272C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX427_SL_ATT0 | 0x400272D0 | FULL | Slave attributes 0 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX427_SL_ATT1 | 0x400272D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX427_SL_ATT2 | 0x400272D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX427_SL_ATT3 | 0x400272DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX427_MS_ADDR | 0x400272E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX427_MS_SIZE | 0x400272E4 | FULL | Master region, size |
| PERI_MS_PPU_FX427_MS_ATT0 | 0x400272F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX427_MS_ATT1 | 0x400272F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX427_MS_ATT2 | 0x400272F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX427_MS_ATT3 | 0x400272FC | FULL | Master attributes 3 |

## 23.445 PPU_FX 428

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX428_SL_ADDR | 0x40027300 | FULL | Slave region, base address |
| PERI_MS_PPU_FX428_SL_SIZE | 0x40027304 | FULL | Slave region, size |
| PERI_MS_PPU_FX428_SL_ATT0 | 0x40027310 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX428_SL_ATT1 | 0x40027314 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX428_SL_ATT2 | 0x40027318 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX428_SL_ATT3 | 0x4002731C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX428_MS_ADDR | 0x40027320 | FULL | Master region, base address |
| PERI_MS_PPU_FX428_MS_SIZE | 0x40027324 | FULL | Master region, size |
| PERI_MS_PPU_FX428_MS_ATT0 | 0x40027330 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX428_MS_ATT1 | 0x40027334 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX428_MS_ATT2 | 0x40027338 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX428_MS_ATT3 | 0x4002733C | FULL | Master attributes 3 |

## 23.446 PPU_FX 429

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX429_SL_ADDR | 0x40027340 | FULL | Slave region, base address |
| PERI_MS_PPU_FX429_SL_SIZE | 0x40027344 | FULL | Slave region, size |
| PERI_MS_PPU_FX429_SL_ATT0 | 0x40027350 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX429_SL_ATT1 | 0x40027354 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX429_SL_ATT2 | 0x40027358 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX429_SL_ATT3 | 0x4002735C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX429_MS_ADDR | 0x40027360 | FULL | Master region, base address |
| PERI_MS_PPU_FX429_MS_SIZE | 0x40027364 | FULL | Master region, size |
| PERI_MS_PPU_FX429_MS_ATT0 | 0x40027370 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX429_MS_ATT1 | 0x40027374 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX429_MS_ATT2 | 0x40027378 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX429_MS_ATT3 | 0x4002737C | FULL | Master attributes 3 |

## 23.447 PPU_FX 430

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX430_SL_ADDR | 0x40027380 | FULL | Slave region, base address |
| PERI_MS_PPU_FX430_SL_SIZE | 0x40027384 | FULL | Slave region, size |
| PERI_MS_PPU_FX430_SL_ATT0 | 0x40027390 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX430_SL_ATT1 | 0x40027394 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX430_SL_ATT2 | 0x40027398 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX430_SL_ATT3 | 0x4002739C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX430_MS_ADDR | 0x400273A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX430_MS_SIZE | 0x400273A4 | FULL | Master region, size |
| PERI_MS_PPU_FX430_MS_ATT0 | 0x400273B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX430_MS_ATT1 | 0x400273B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX430_MS_ATT2 | 0x400273B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX430_MS_ATT3 | 0x400273BC | FULL | Master attributes 3 |

## 23.448 PPU_FX 431

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX431_SL_ADDR | 0x400273C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX431_SL_SIZE | 0x400273C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX431_SL_ATT0 | 0x400273D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX431_SL_ATT1 | 0x400273D4 | FULL | Slave attributes 1 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX431_SL_ATT2 | 0x400273D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX431_SL_ATT3 | 0x400273DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX431_MS_ADDR | 0x400273E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX431_MS_SIZE | 0x400273E4 | FULL | Master region, size |
| PERI_MS_PPU_FX431_MS_ATT0 | 0x400273F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX431_MS_ATT1 | 0x400273F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX431_MS_ATT2 | 0x400273F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX431_MS_ATT3 | 0x400273FC | FULL | Master attributes 3 |

## 23.449 PPU_FX 432

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX432_SL_ADDR | 0x40027400 | FULL | Slave region, base address |
| PERI_MS_PPU_FX432_SL_SIZE | 0x40027404 | FULL | Slave region, size |
| PERI_MS_PPU_FX432_SL_ATT0 | 0x40027410 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX432_SL_ATT1 | 0x40027414 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX432_SL_ATT2 | 0x40027418 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX432_SL_ATT3 | 0x4002741C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX432_MS_ADDR | 0x40027420 | FULL | Master region, base address |
| PERI_MS_PPU_FX432_MS_SIZE | 0x40027424 | FULL | Master region, size |
| PERI_MS_PPU_FX432_MS_ATT0 | 0x40027430 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX432_MS_ATT1 | 0x40027434 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX432_MS_ATT2 | 0x40027438 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX432_MS_ATT3 | 0x4002743C | FULL | Master attributes 3 |

## 23.450 PPU_FX 433

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX433_SL_ADDR | 0x40027440 | FULL | Slave region, base address |
| PERI_MS_PPU_FX433_SL_SIZE | 0x40027444 | FULL | Slave region, size |
| PERI_MS_PPU_FX433_SL_ATT0 | 0x40027450 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX433_SL_ATT1 | 0x40027454 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX433_SL_ATT2 | 0x40027458 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX433_SL_ATT3 | 0x4002745C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX433_MS_ADDR | 0x40027460 | FULL | Master region, base address |
| PERI_MS_PPU_FX433_MS_SIZE | 0x40027464 | FULL | Master region, size |
| PERI_MS_PPU_FX433_MS_ATT0 | 0x40027470 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX433_MS_ATT1 | 0x40027474 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX433_MS_ATT2 | 0x40027478 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX433_MS_ATT3 | 0x4002747C | FULL | Master attributes 3 |

## 23.451 PPU_FX 434

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX434_SL_ADDR | 0x40027480 | FULL | Slave region, base address |
| PERI_MS_PPU_FX434_SL_SIZE | 0x40027484 | FULL | Slave region, size |
| PERI_MS_PPU_FX434_SL_ATT0 | 0x40027490 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX434_SL_ATT1 | 0x40027494 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX434_SL_ATT2 | 0x40027498 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX434_SL_ATT3 | 0x4002749C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX434_MS_ADDR | 0x400274A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX434_MS_SIZE | 0x400274A4 | FULL | Master region, size |
| PERI_MS_PPU_FX434_MS_ATT0 | 0x400274B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX434_MS_ATT1 | 0x400274B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX434_MS_ATT2 | 0x400274B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX434_MS_ATT3 | 0x400274BC | FULL | Master attributes 3 |

## 23.452 PPU_FX 435

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX435_SL_ADDR | 0x400274C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX435_SL_SIZE | 0x400274C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX435_SL_ATT0 | 0x400274D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX435_SL_ATT1 | 0x400274D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX435_SL_ATT2 | 0x400274D8 | FULL | Slave attributes 2 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX435_SL_ATT3 | 0x400274DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX435_MS_ADDR | 0x400274E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX435_MS_SIZE | 0x400274E4 | FULL | Master region, size |
| PERI_MS_PPU_FX435_MS_ATT0 | 0x400274F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX435_MS_ATT1 | 0x400274F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX435_MS_ATT2 | 0x400274F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX435_MS_ATT3 | 0x400274FC | FULL | Master attributes 3 |

## 23.453 PPU_FX 436

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX436_SL_ADDR | 0x40027500 | FULL | Slave region, base address |
| PERI_MS_PPU_FX436_SL_SIZE | 0x40027504 | FULL | Slave region, size |
| PERI_MS_PPU_FX436_SL_ATT0 | 0x40027510 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX436_SL_ATT1 | 0x40027514 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX436_SL_ATT2 | 0x40027518 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX436_SL_ATT3 | 0x4002751C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX436_MS_ADDR | 0x40027520 | FULL | Master region, base address |
| PERI_MS_PPU_FX436_MS_SIZE | 0x40027524 | FULL | Master region, size |
| PERI_MS_PPU_FX436_MS_ATT0 | 0x40027530 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX436_MS_ATT1 | 0x40027534 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX436_MS_ATT2 | 0x40027538 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX436_MS_ATT3 | 0x4002753C | FULL | Master attributes 3 |

## 23.454 PPU_FX 437

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX437_SL_ADDR | 0x40027540 | FULL | Slave region, base address |
| PERI_MS_PPU_FX437_SL_SIZE | 0x40027544 | FULL | Slave region, size |
| PERI_MS_PPU_FX437_SL_ATT0 | 0x40027550 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX437_SL_ATT1 | 0x40027554 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX437_SL_ATT2 | 0x40027558 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX437_SL_ATT3 | 0x4002755C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX437_MS_ADDR | 0x40027560 | FULL | Master region, base address |
| PERI_MS_PPU_FX437_MS_SIZE | 0x40027564 | FULL | Master region, size |
| PERI_MS_PPU_FX437_MS_ATT0 | 0x40027570 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX437_MS_ATT1 | 0x40027574 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX437_MS_ATT2 | 0x40027578 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX437_MS_ATT3 | 0x4002757C | FULL | Master attributes 3 |

## 23.455 PPU_FX 438

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX438_SL_ADDR | 0x40027580 | FULL | Slave region, base address |
| PERI_MS_PPU_FX438_SL_SIZE | 0x40027584 | FULL | Slave region, size |
| PERI_MS_PPU_FX438_SL_ATT0 | 0x40027590 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX438_SL_ATT1 | 0x40027594 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX438_SL_ATT2 | 0x40027598 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX438_SL_ATT3 | 0x4002759C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX438_MS_ADDR | 0x400275A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX438_MS_SIZE | 0x400275A4 | FULL | Master region, size |
| PERI_MS_PPU_FX438_MS_ATT0 | 0x400275B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX438_MS_ATT1 | 0x400275B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX438_MS_ATT2 | 0x400275B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX438_MS_ATT3 | 0x400275BC | FULL | Master attributes 3 |

## 23.456 PPU_FX 439

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX439_SL_ADDR | 0x400275C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX439_SL_SIZE | 0x400275C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX439_SL_ATT0 | 0x400275D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX439_SL_ATT1 | 0x400275D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX439_SL_ATT2 | 0x400275D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX439_SL_ATT3 | 0x400275DC | FULL | Slave attributes 3 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX439_MS_ADDR | 0x400275E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX439_MS_SIZE | 0x400275E4 | FULL | Master region, size |
| PERI_MS_PPU_FX439_MS_ATT0 | 0x400275F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX439_MS_ATT1 | 0x400275F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX439_MS_ATT2 | 0x400275F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX439_MS_ATT3 | 0x400275FC | FULL | Master attributes 3 |

## 23.457 PPU_FX 440

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX440_SL_ADDR | 0x40027600 | FULL | Slave region, base address |
| PERI_MS_PPU_FX440_SL_SIZE | 0x40027604 | FULL | Slave region, size |
| PERI_MS_PPU_FX440_SL_ATT0 | 0x40027610 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX440_SL_ATT1 | 0x40027614 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX440_SL_ATT2 | 0x40027618 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX440_SL_ATT3 | 0x4002761C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX440_MS_ADDR | 0x40027620 | FULL | Master region, base address |
| PERI_MS_PPU_FX440_MS_SIZE | 0x40027624 | FULL | Master region, size |
| PERI_MS_PPU_FX440_MS_ATT0 | 0x40027630 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX440_MS_ATT1 | 0x40027634 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX440_MS_ATT2 | 0x40027638 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX440_MS_ATT3 | 0x4002763C | FULL | Master attributes 3 |

## 23.458 PPU_FX 441

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX441_SL_ADDR | 0x40027640 | FULL | Slave region, base address |
| PERI_MS_PPU_FX441_SL_SIZE | 0x40027644 | FULL | Slave region, size |
| PERI_MS_PPU_FX441_SL_ATT0 | 0x40027650 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX441_SL_ATT1 | 0x40027654 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX441_SL_ATT2 | 0x40027658 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX441_SL_ATT3 | 0x4002765C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX441_MS_ADDR | 0x40027660 | FULL | Master region, base address |
| PERI_MS_PPU_FX441_MS_SIZE | 0x40027664 | FULL | Master region, size |
| PERI_MS_PPU_FX441_MS_ATT0 | 0x40027670 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX441_MS_ATT1 | 0x40027674 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX441_MS_ATT2 | 0x40027678 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX441_MS_ATT3 | 0x4002767C | FULL | Master attributes 3 |

## 23.459 PPU_FX 442

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX442_SL_ADDR | 0x40027680 | FULL | Slave region, base address |
| PERI_MS_PPU_FX442_SL_SIZE | 0x40027684 | FULL | Slave region, size |
| PERI_MS_PPU_FX442_SL_ATT0 | 0x40027690 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX442_SL_ATT1 | 0x40027694 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX442_SL_ATT2 | 0x40027698 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX442_SL_ATT3 | 0x4002769C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX442_MS_ADDR | 0x400276A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX442_MS_SIZE | 0x400276A4 | FULL | Master region, size |
| PERI_MS_PPU_FX442_MS_ATT0 | 0x400276B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX442_MS_ATT1 | 0x400276B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX442_MS_ATT2 | 0x400276B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX442_MS_ATT3 | 0x400276BC | FULL | Master attributes 3 |

## 23.460 PPU_FX 443

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX443_SL_ADDR | 0x400276C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX443_SL_SIZE | 0x400276C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX443_SL_ATT0 | 0x400276D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX443_SL_ATT1 | 0x400276D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX443_SL_ATT2 | 0x400276D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX443_SL_ATT3 | 0x400276DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX443_MS_ADDR | 0x400276E0 | FULL | Master region, base address |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX443_MS_SIZE | 0x400276E4 | FULL | Master region, size |
| PERI_MS_PPU_FX443_MS_ATT0 | 0x400276F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX443_MS_ATT1 | 0x400276F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX443_MS_ATT2 | 0x400276F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX443_MS_ATT3 | 0x400276FC | FULL | Master attributes 3 |

## 23.461 PPU_FX 444

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX444_SL_ADDR | 0x40027700 | FULL | Slave region, base address |
| PERI_MS_PPU_FX444_SL_SIZE | 0x40027704 | FULL | Slave region, size |
| PERI_MS_PPU_FX444_SL_ATT0 | 0x40027710 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX444_SL_ATT1 | 0x40027714 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX444_SL_ATT2 | 0x40027718 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX444_SL_ATT3 | 0x4002771C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX444_MS_ADDR | 0x40027720 | FULL | Master region, base address |
| PERI_MS_PPU_FX444_MS_SIZE | 0x40027724 | FULL | Master region, size |
| PERI_MS_PPU_FX444_MS_ATT0 | 0x40027730 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX444_MS_ATT1 | 0x40027734 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX444_MS_ATT2 | 0x40027738 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX444_MS_ATT3 | 0x4002773C | FULL | Master attributes 3 |

## 23.462 PPU_FX 445

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX445_SL_ADDR | 0x40027740 | FULL | Slave region, base address |
| PERI_MS_PPU_FX445_SL_SIZE | 0x40027744 | FULL | Slave region, size |
| PERI_MS_PPU_FX445_SL_ATT0 | 0x40027750 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX445_SL_ATT1 | 0x40027754 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX445_SL_ATT2 | 0x40027758 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX445_SL_ATT3 | 0x4002775C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX445_MS_ADDR | 0x40027760 | FULL | Master region, base address |
| PERI_MS_PPU_FX445_MS_SIZE | 0x40027764 | FULL | Master region, size |
| PERI_MS_PPU_FX445_MS_ATT0 | 0x40027770 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX445_MS_ATT1 | 0x40027774 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX445_MS_ATT2 | 0x40027778 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX445_MS_ATT3 | 0x4002777C | FULL | Master attributes 3 |

## 23.463 PPU_FX 446

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX446_SL_ADDR | 0x40027780 | FULL | Slave region, base address |
| PERI_MS_PPU_FX446_SL_SIZE | 0x40027784 | FULL | Slave region, size |
| PERI_MS_PPU_FX446_SL_ATT0 | 0x40027790 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX446_SL_ATT1 | 0x40027794 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX446_SL_ATT2 | 0x40027798 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX446_SL_ATT3 | 0x4002779C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX446_MS_ADDR | 0x400277A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX446_MS_SIZE | 0x400277A4 | FULL | Master region, size |
| PERI_MS_PPU_FX446_MS_ATT0 | 0x400277B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX446_MS_ATT1 | 0x400277B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX446_MS_ATT2 | 0x400277B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX446_MS_ATT3 | 0x400277BC | FULL | Master attributes 3 |

## 23.464 PPU_FX 447

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX447_SL_ADDR | 0x400277C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX447_SL_SIZE | 0x400277C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX447_SL_ATT0 | 0x400277D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX447_SL_ATT1 | 0x400277D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX447_SL_ATT2 | 0x400277D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX447_SL_ATT3 | 0x400277DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX447_MS_ADDR | 0x400277E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX447_MS_SIZE | 0x400277E4 | FULL | Master region, size |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX447_MS_ATT0 | 0x400277F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX447_MS_ATT1 | 0x400277F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX447_MS_ATT2 | 0x400277F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX447_MS_ATT3 | 0x400277FC | FULL | Master attributes 3 |

## 23.465 PPU_FX 448

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX448_SL_ADDR | 0x40027800 | FULL | Slave region, base address |
| PERI_MS_PPU_FX448_SL_SIZE | 0x40027804 | FULL | Slave region, size |
| PERI_MS_PPU_FX448_SL_ATT0 | 0x40027810 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX448_SL_ATT1 | 0x40027814 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX448_SL_ATT2 | 0x40027818 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX448_SL_ATT3 | 0x4002781C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX448_MS_ADDR | 0x40027820 | FULL | Master region, base address |
| PERI_MS_PPU_FX448_MS_SIZE | 0x40027824 | FULL | Master region, size |
| PERI_MS_PPU_FX448_MS_ATT0 | 0x40027830 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX448_MS_ATT1 | 0x40027834 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX448_MS_ATT2 | 0x40027838 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX448_MS_ATT3 | 0x4002783C | FULL | Master attributes 3 |

## 23.466 PPU_FX 449

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX449_SL_ADDR | 0x40027840 | FULL | Slave region, base address |
| PERI_MS_PPU_FX449_SL_SIZE | 0x40027844 | FULL | Slave region, size |
| PERI_MS_PPU_FX449_SL_ATT0 | 0x40027850 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX449_SL_ATT1 | 0x40027854 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX449_SL_ATT2 | 0x40027858 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX449_SL_ATT3 | 0x4002785C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX449_MS_ADDR | 0x40027860 | FULL | Master region, base address |
| PERI_MS_PPU_FX449_MS_SIZE | 0x40027864 | FULL | Master region, size |
| PERI_MS_PPU_FX449_MS_ATT0 | 0x40027870 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX449_MS_ATT1 | 0x40027874 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX449_MS_ATT2 | 0x40027878 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX449_MS_ATT3 | 0x4002787C | FULL | Master attributes 3 |

## 23.467 PPU_FX 450

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX450_SL_ADDR | 0x40027880 | FULL | Slave region, base address |
| PERI_MS_PPU_FX450_SL_SIZE | 0x40027884 | FULL | Slave region, size |
| PERI_MS_PPU_FX450_SL_ATT0 | 0x40027890 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX450_SL_ATT1 | 0x40027894 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX450_SL_ATT2 | 0x40027898 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX450_SL_ATT3 | 0x4002789C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX450_MS_ADDR | 0x400278A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX450_MS_SIZE | 0x400278A4 | FULL | Master region, size |
| PERI_MS_PPU_FX450_MS_ATT0 | 0x400278B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX450_MS_ATT1 | 0x400278B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX450_MS_ATT2 | 0x400278B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX450_MS_ATT3 | 0x400278BC | FULL | Master attributes 3 |

## 23.468 PPU_FX 451

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX451_SL_ADDR | 0x400278C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX451_SL_SIZE | 0x400278C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX451_SL_ATT0 | 0x400278D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX451_SL_ATT1 | 0x400278D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX451_SL_ATT2 | 0x400278D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX451_SL_ATT3 | 0x400278DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX451_MS_ADDR | 0x400278E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX451_MS_SIZE | 0x400278E4 | FULL | Master region, size |
| PERI_MS_PPU_FX451_MS_ATT0 | 0x400278F0 | FULL | Master attributes 0 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX451_MS_ATT1 | 0x400278F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX451_MS_ATT2 | 0x400278F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX451_MS_ATT3 | 0x400278FC | FULL | Master attributes 3 |

## 23.469 PPU_FX 452

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX452_SL_ADDR | 0x40027900 | FULL | Slave region, base address |
| PERI_MS_PPU_FX452_SL_SIZE | 0x40027904 | FULL | Slave region, size |
| PERI_MS_PPU_FX452_SL_ATT0 | 0x40027910 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX452_SL_ATT1 | 0x40027914 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX452_SL_ATT2 | 0x40027918 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX452_SL_ATT3 | 0x4002791C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX452_MS_ADDR | 0x40027920 | FULL | Master region, base address |
| PERI_MS_PPU_FX452_MS_SIZE | 0x40027924 | FULL | Master region, size |
| PERI_MS_PPU_FX452_MS_ATT0 | 0x40027930 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX452_MS_ATT1 | 0x40027934 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX452_MS_ATT2 | 0x40027938 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX452_MS_ATT3 | 0x4002793C | FULL | Master attributes 3 |

## 23.470 PPU_FX 453

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX453_SL_ADDR | 0x40027940 | FULL | Slave region, base address |
| PERI_MS_PPU_FX453_SL_SIZE | 0x40027944 | FULL | Slave region, size |
| PERI_MS_PPU_FX453_SL_ATT0 | 0x40027950 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX453_SL_ATT1 | 0x40027954 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX453_SL_ATT2 | 0x40027958 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX453_SL_ATT3 | 0x4002795C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX453_MS_ADDR | 0x40027960 | FULL | Master region, base address |
| PERI_MS_PPU_FX453_MS_SIZE | 0x40027964 | FULL | Master region, size |
| PERI_MS_PPU_FX453_MS_ATT0 | 0x40027970 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX453_MS_ATT1 | 0x40027974 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX453_MS_ATT2 | 0x40027978 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX453_MS_ATT3 | 0x4002797C | FULL | Master attributes 3 |

## 23.471 PPU_FX 454

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX454_SL_ADDR | 0x40027980 | FULL | Slave region, base address |
| PERI_MS_PPU_FX454_SL_SIZE | 0x40027984 | FULL | Slave region, size |
| PERI_MS_PPU_FX454_SL_ATT0 | 0x40027990 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX454_SL_ATT1 | 0x40027994 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX454_SL_ATT2 | 0x40027998 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX454_SL_ATT3 | 0x4002799C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX454_MS_ADDR | 0x400279A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX454_MS_SIZE | 0x400279A4 | FULL | Master region, size |
| PERI_MS_PPU_FX454_MS_ATT0 | 0x400279B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX454_MS_ATT1 | 0x400279B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX454_MS_ATT2 | 0x400279B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX454_MS_ATT3 | 0x400279BC | FULL | Master attributes 3 |

## 23.472 PPU_FX 455

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX455_SL_ADDR | 0x400279C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX455_SL_SIZE | 0x400279C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX455_SL_ATT0 | 0x400279D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX455_SL_ATT1 | 0x400279D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX455_SL_ATT2 | 0x400279D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX455_SL_ATT3 | 0x400279DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX455_MS_ADDR | 0x400279E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX455_MS_SIZE | 0x400279E4 | FULL | Master region, size |
| PERI_MS_PPU_FX455_MS_ATT0 | 0x400279F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX455_MS_ATT1 | 0x400279F4 | FULL | Master attributes 1 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX455_MS_ATT2 | 0x400279F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX455_MS_ATT3 | 0x400279FC | FULL | Master attributes 3 |

## 23.473 PPU_FX 456

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX456_SL_ADDR | 0x40027A00 | FULL | Slave region, base address |
| PERI_MS_PPU_FX456_SL_SIZE | 0x40027A04 | FULL | Slave region, size |
| PERI_MS_PPU_FX456_SL_ATT0 | 0x40027A10 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX456_SL_ATT1 | 0x40027A14 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX456_SL_ATT2 | 0x40027A18 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX456_SL_ATT3 | 0x40027A1C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX456_MS_ADDR | 0x40027A20 | FULL | Master region, base address |
| PERI_MS_PPU_FX456_MS_SIZE | 0x40027A24 | FULL | Master region, size |
| PERI_MS_PPU_FX456_MS_ATT0 | 0x40027A30 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX456_MS_ATT1 | 0x40027A34 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX456_MS_ATT2 | 0x40027A38 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX456_MS_ATT3 | 0x40027A3C | FULL | Master attributes 3 |

## 23.474 PPU_FX 457

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX457_SL_ADDR | 0x40027A40 | FULL | Slave region, base address |
| PERI_MS_PPU_FX457_SL_SIZE | 0x40027A44 | FULL | Slave region, size |
| PERI_MS_PPU_FX457_SL_ATT0 | 0x40027A50 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX457_SL_ATT1 | 0x40027A54 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX457_SL_ATT2 | 0x40027A58 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX457_SL_ATT3 | 0x40027A5C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX457_MS_ADDR | 0x40027A60 | FULL | Master region, base address |
| PERI_MS_PPU_FX457_MS_SIZE | 0x40027A64 | FULL | Master region, size |
| PERI_MS_PPU_FX457_MS_ATT0 | 0x40027A70 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX457_MS_ATT1 | 0x40027A74 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX457_MS_ATT2 | 0x40027A78 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX457_MS_ATT3 | 0x40027A7C | FULL | Master attributes 3 |

## 23.475 PPU_FX 458

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX458_SL_ADDR | 0x40027A80 | FULL | Slave region, base address |
| PERI_MS_PPU_FX458_SL_SIZE | 0x40027A84 | FULL | Slave region, size |
| PERI_MS_PPU_FX458_SL_ATT0 | 0x40027A90 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX458_SL_ATT1 | 0x40027A94 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX458_SL_ATT2 | 0x40027A98 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX458_SL_ATT3 | 0x40027A9C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX458_MS_ADDR | 0x40027AA0 | FULL | Master region, base address |
| PERI_MS_PPU_FX458_MS_SIZE | 0x40027AA4 | FULL | Master region, size |
| PERI_MS_PPU_FX458_MS_ATT0 | 0x40027AB0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX458_MS_ATT1 | 0x40027AB4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX458_MS_ATT2 | 0x40027AB8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX458_MS_ATT3 | 0x40027ABC | FULL | Master attributes 3 |

## 23.476 PPU_FX 459

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX459_SL_ADDR | 0x40027AC0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX459_SL_SIZE | 0x40027AC4 | FULL | Slave region, size |
| PERI_MS_PPU_FX459_SL_ATT0 | 0x40027AD0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX459_SL_ATT1 | 0x40027AD4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX459_SL_ATT2 | 0x40027AD8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX459_SL_ATT3 | 0x40027ADC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX459_MS_ADDR | 0x40027AE0 | FULL | Master region, base address |
| PERI_MS_PPU_FX459_MS_SIZE | 0x40027AE4 | FULL | Master region, size |
| PERI_MS_PPU_FX459_MS_ATT0 | 0x40027AF0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX459_MS_ATT1 | 0x40027AF4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX459_MS_ATT2 | 0x40027AF8 | FULL | Master attributes 2 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX459_MS_ATT3 | 0x40027AFC | FULL | Master attributes 3 |

## 23.477 PPU_FX 460

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX460_SL_ADDR | 0x40027B00 | FULL | Slave region, base address |
| PERI_MS_PPU_FX460_SL_SIZE | 0x40027B04 | FULL | Slave region, size |
| PERI_MS_PPU_FX460_SL_ATT0 | 0x40027B10 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX460_SL_ATT1 | 0x40027B14 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX460_SL_ATT2 | 0x40027B18 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX460_SL_ATT3 | 0x40027B1C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX460_MS_ADDR | 0x40027B20 | FULL | Master region, base address |
| PERI_MS_PPU_FX460_MS_SIZE | 0x40027B24 | FULL | Master region, size |
| PERI_MS_PPU_FX460_MS_ATT0 | 0x40027B30 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX460_MS_ATT1 | 0x40027B34 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX460_MS_ATT2 | 0x40027B38 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX460_MS_ATT3 | 0x40027B3C | FULL | Master attributes 3 |

## 23.478 PPU_FX 461

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX461_SL_ADDR | 0x40027B40 | FULL | Slave region, base address |
| PERI_MS_PPU_FX461_SL_SIZE | 0x40027B44 | FULL | Slave region, size |
| PERI_MS_PPU_FX461_SL_ATT0 | 0x40027B50 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX461_SL_ATT1 | 0x40027B54 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX461_SL_ATT2 | 0x40027B58 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX461_SL_ATT3 | 0x40027B5C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX461_MS_ADDR | 0x40027B60 | FULL | Master region, base address |
| PERI_MS_PPU_FX461_MS_SIZE | 0x40027B64 | FULL | Master region, size |
| PERI_MS_PPU_FX461_MS_ATT0 | 0x40027B70 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX461_MS_ATT1 | 0x40027B74 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX461_MS_ATT2 | 0x40027B78 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX461_MS_ATT3 | 0x40027B7C | FULL | Master attributes 3 |

## 23.479 PPU_FX 462

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX462_SL_ADDR | 0x40027B80 | FULL | Slave region, base address |
| PERI_MS_PPU_FX462_SL_SIZE | 0x40027B84 | FULL | Slave region, size |
| PERI_MS_PPU_FX462_SL_ATT0 | 0x40027B90 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX462_SL_ATT1 | 0x40027B94 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX462_SL_ATT2 | 0x40027B98 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX462_SL_ATT3 | 0x40027B9C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX462_MS_ADDR | 0x40027BA0 | FULL | Master region, base address |
| PERI_MS_PPU_FX462_MS_SIZE | 0x40027BA4 | FULL | Master region, size |
| PERI_MS_PPU_FX462_MS_ATT0 | 0x40027BB0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX462_MS_ATT1 | 0x40027BB4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX462_MS_ATT2 | 0x40027BB8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX462_MS_ATT3 | 0x40027BBC | FULL | Master attributes 3 |

## 23.480 PPU_FX 463

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX463_SL_ADDR | 0x40027BC0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX463_SL_SIZE | 0x40027BC4 | FULL | Slave region, size |
| PERI_MS_PPU_FX463_SL_ATT0 | 0x40027BD0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX463_SL_ATT1 | 0x40027BD4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX463_SL_ATT2 | 0x40027BD8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX463_SL_ATT3 | 0x40027BDC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX463_MS_ADDR | 0x40027BE0 | FULL | Master region, base address |
| PERI_MS_PPU_FX463_MS_SIZE | 0x40027BE4 | FULL | Master region, size |
| PERI_MS_PPU_FX463_MS_ATT0 | 0x40027BF0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX463_MS_ATT1 | 0x40027BF4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX463_MS_ATT2 | 0x40027BF8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX463_MS_ATT3 | 0x40027BFC | FULL | Master attributes 3 |

## 23.481 PPU_FX 464

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX464_SL_ADDR | 0x40027C00 | FULL | Slave region, base address |
| PERI_MS_PPU_FX464_SL_SIZE | 0x40027C04 | FULL | Slave region, size |
| PERI_MS_PPU_FX464_SL_ATT0 | 0x40027C10 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX464_SL_ATT1 | 0x40027C14 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX464_SL_ATT2 | 0x40027C18 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX464_SL_ATT3 | 0x40027C1C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX464_MS_ADDR | 0x40027C20 | FULL | Master region, base address |
| PERI_MS_PPU_FX464_MS_SIZE | 0x40027C24 | FULL | Master region, size |
| PERI_MS_PPU_FX464_MS_ATT0 | 0x40027C30 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX464_MS_ATT1 | 0x40027C34 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX464_MS_ATT2 | 0x40027C38 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX464_MS_ATT3 | 0x40027C3C | FULL | Master attributes 3 |

## 23.482 PPU_FX 465

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX465_SL_ADDR | 0x40027C40 | FULL | Slave region, base address |
| PERI_MS_PPU_FX465_SL_SIZE | 0x40027C44 | FULL | Slave region, size |
| PERI_MS_PPU_FX465_SL_ATT0 | 0x40027C50 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX465_SL_ATT1 | 0x40027C54 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX465_SL_ATT2 | 0x40027C58 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX465_SL_ATT3 | 0x40027C5C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX465_MS_ADDR | 0x40027C60 | FULL | Master region, base address |
| PERI_MS_PPU_FX465_MS_SIZE | 0x40027C64 | FULL | Master region, size |
| PERI_MS_PPU_FX465_MS_ATT0 | 0x40027C70 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX465_MS_ATT1 | 0x40027C74 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX465_MS_ATT2 | 0x40027C78 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX465_MS_ATT3 | 0x40027C7C | FULL | Master attributes 3 |

## 23.483 PPU_FX 466

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX466_SL_ADDR | 0x40027C80 | FULL | Slave region, base address |
| PERI_MS_PPU_FX466_SL_SIZE | 0x40027C84 | FULL | Slave region, size |
| PERI_MS_PPU_FX466_SL_ATT0 | 0x40027C90 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX466_SL_ATT1 | 0x40027C94 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX466_SL_ATT2 | 0x40027C98 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX466_SL_ATT3 | 0x40027C9C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX466_MS_ADDR | 0x40027CA0 | FULL | Master region, base address |
| PERI_MS_PPU_FX466_MS_SIZE | 0x40027CA4 | FULL | Master region, size |
| PERI_MS_PPU_FX466_MS_ATT0 | 0x40027CB0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX466_MS_ATT1 | 0x40027CB4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX466_MS_ATT2 | 0x40027CB8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX466_MS_ATT3 | 0x40027CBC | FULL | Master attributes 3 |

## 23.484 PPU_FX 467

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX467_SL_ADDR | 0x40027CC0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX467_SL_SIZE | 0x40027CC4 | FULL | Slave region, size |
| PERI_MS_PPU_FX467_SL_ATT0 | 0x40027CD0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX467_SL_ATT1 | 0x40027CD4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX467_SL_ATT2 | 0x40027CD8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX467_SL_ATT3 | 0x40027CDC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX467_MS_ADDR | 0x40027CE0 | FULL | Master region, base address |
| PERI_MS_PPU_FX467_MS_SIZE | 0x40027CE4 | FULL | Master region, size |
| PERI_MS_PPU_FX467_MS_ATT0 | 0x40027CF0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX467_MS_ATT1 | 0x40027CF4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX467_MS_ATT2 | 0x40027CF8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX467_MS_ATT3 | 0x40027CFC | FULL | Master attributes 3 |

## 23.485 PPU_FX 468

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX468_SL_ADDR | 0x40027D00 | FULL | Slave region, base address |
| PERI_MS_PPU_FX468_SL_SIZE | 0x40027D04 | FULL | Slave region, size |
| PERI_MS_PPU_FX468_SL_ATT0 | 0x40027D10 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX468_SL_ATT1 | 0x40027D14 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX468_SL_ATT2 | 0x40027D18 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX468_SL_ATT3 | 0x40027D1C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX468_MS_ADDR | 0x40027D20 | FULL | Master region, base address |
| PERI_MS_PPU_FX468_MS_SIZE | 0x40027D24 | FULL | Master region, size |
| PERI_MS_PPU_FX468_MS_ATT0 | 0x40027D30 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX468_MS_ATT1 | 0x40027D34 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX468_MS_ATT2 | 0x40027D38 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX468_MS_ATT3 | 0x40027D3C | FULL | Master attributes 3 |

## 23.486 PPU_FX 469

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX469_SL_ADDR | 0x40027D40 | FULL | Slave region, base address |
| PERI_MS_PPU_FX469_SL_SIZE | 0x40027D44 | FULL | Slave region, size |
| PERI_MS_PPU_FX469_SL_ATT0 | 0x40027D50 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX469_SL_ATT1 | 0x40027D54 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX469_SL_ATT2 | 0x40027D58 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX469_SL_ATT3 | 0x40027D5C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX469_MS_ADDR | 0x40027D60 | FULL | Master region, base address |
| PERI_MS_PPU_FX469_MS_SIZE | 0x40027D64 | FULL | Master region, size |
| PERI_MS_PPU_FX469_MS_ATT0 | 0x40027D70 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX469_MS_ATT1 | 0x40027D74 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX469_MS_ATT2 | 0x40027D78 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX469_MS_ATT3 | 0x40027D7C | FULL | Master attributes 3 |

## 23.487 PPU_FX 470

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX470_SL_ADDR | 0x40027D80 | FULL | Slave region, base address |
| PERI_MS_PPU_FX470_SL_SIZE | 0x40027D84 | FULL | Slave region, size |
| PERI_MS_PPU_FX470_SL_ATT0 | 0x40027D90 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX470_SL_ATT1 | 0x40027D94 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX470_SL_ATT2 | 0x40027D98 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX470_SL_ATT3 | 0x40027D9C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX470_MS_ADDR | 0x40027DA0 | FULL | Master region, base address |
| PERI_MS_PPU_FX470_MS_SIZE | 0x40027DA4 | FULL | Master region, size |
| PERI_MS_PPU_FX470_MS_ATT0 | 0x40027DB0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX470_MS_ATT1 | 0x40027DB4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX470_MS_ATT2 | 0x40027DB8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX470_MS_ATT3 | 0x40027DBC | FULL | Master attributes 3 |

## 23.488 PPU_FX 471

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX471_SL_ADDR | 0x40027DC0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX471_SL_SIZE | 0x40027DC4 | FULL | Slave region, size |
| PERI_MS_PPU_FX471_SL_ATT0 | 0x40027DD0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX471_SL_ATT1 | 0x40027DD4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX471_SL_ATT2 | 0x40027DD8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX471_SL_ATT3 | 0x40027DDC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX471_MS_ADDR | 0x40027DE0 | FULL | Master region, base address |
| PERI_MS_PPU_FX471_MS_SIZE | 0x40027DE4 | FULL | Master region, size |
| PERI_MS_PPU_FX471_MS_ATT0 | 0x40027DF0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX471_MS_ATT1 | 0x40027DF4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX471_MS_ATT2 | 0x40027DF8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX471_MS_ATT3 | 0x40027DFC | FULL | Master attributes 3 |

## 23.489 PPU_FX 472

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX472_SL_ADDR | 0x40027E00 | FULL | Slave region, base address |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX472_SL_SIZE | 0x40027E04 | FULL | Slave region, size |
| PERI_MS_PPU_FX472_SL_ATT0 | 0x40027E10 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX472_SL_ATT1 | 0x40027E14 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX472_SL_ATT2 | 0x40027E18 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX472_SL_ATT3 | 0x40027E1C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX472_MS_ADDR | 0x40027E20 | FULL | Master region, base address |
| PERI_MS_PPU_FX472_MS_SIZE | 0x40027E24 | FULL | Master region, size |
| PERI_MS_PPU_FX472_MS_ATT0 | 0x40027E30 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX472_MS_ATT1 | 0x40027E34 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX472_MS_ATT2 | 0x40027E38 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX472_MS_ATT3 | 0x40027E3C | FULL | Master attributes 3 |

## 23.490 PPU_FX 473

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX473_SL_ADDR | 0x40027E40 | FULL | Slave region, base address |
| PERI_MS_PPU_FX473_SL_SIZE | 0x40027E44 | FULL | Slave region, size |
| PERI_MS_PPU_FX473_SL_ATT0 | 0x40027E50 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX473_SL_ATT1 | 0x40027E54 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX473_SL_ATT2 | 0x40027E58 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX473_SL_ATT3 | 0x40027E5C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX473_MS_ADDR | 0x40027E60 | FULL | Master region, base address |
| PERI_MS_PPU_FX473_MS_SIZE | 0x40027E64 | FULL | Master region, size |
| PERI_MS_PPU_FX473_MS_ATT0 | 0x40027E70 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX473_MS_ATT1 | 0x40027E74 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX473_MS_ATT2 | 0x40027E78 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX473_MS_ATT3 | 0x40027E7C | FULL | Master attributes 3 |

## 23.491 PPU_FX 474

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX474_SL_ADDR | 0x40027E80 | FULL | Slave region, base address |
| PERI_MS_PPU_FX474_SL_SIZE | 0x40027E84 | FULL | Slave region, size |
| PERI_MS_PPU_FX474_SL_ATT0 | 0x40027E90 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX474_SL_ATT1 | 0x40027E94 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX474_SL_ATT2 | 0x40027E98 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX474_SL_ATT3 | 0x40027E9C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX474_MS_ADDR | 0x40027EA0 | FULL | Master region, base address |
| PERI_MS_PPU_FX474_MS_SIZE | 0x40027EA4 | FULL | Master region, size |
| PERI_MS_PPU_FX474_MS_ATT0 | 0x40027EB0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX474_MS_ATT1 | 0x40027EB4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX474_MS_ATT2 | 0x40027EB8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX474_MS_ATT3 | 0x40027EBC | FULL | Master attributes 3 |

## 23.492 PPU_FX 475

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX475_SL_ADDR | 0x40027EC0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX475_SL_SIZE | 0x40027EC4 | FULL | Slave region, size |
| PERI_MS_PPU_FX475_SL_ATT0 | 0x40027ED0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX475_SL_ATT1 | 0x40027ED4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX475_SL_ATT2 | 0x40027ED8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX475_SL_ATT3 | 0x40027EDC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX475_MS_ADDR | 0x40027EE0 | FULL | Master region, base address |
| PERI_MS_PPU_FX475_MS_SIZE | 0x40027EE4 | FULL | Master region, size |
| PERI_MS_PPU_FX475_MS_ATT0 | 0x40027EF0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX475_MS_ATT1 | 0x40027EF4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX475_MS_ATT2 | 0x40027EF8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX475_MS_ATT3 | 0x40027EFC | FULL | Master attributes 3 |

## 23.493 PPU_FX 476

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX476_SL_ADDR | 0x40027F00 | FULL | Slave region, base address |
| PERI_MS_PPU_FX476_SL_SIZE | 0x40027F04 | FULL | Slave region, size |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX476_SL_ATT0 | 0x40027F10 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX476_SL_ATT1 | 0x40027F14 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX476_SL_ATT2 | 0x40027F18 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX476_SL_ATT3 | 0x40027F1C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX476_MS_ADDR | 0x40027F20 | FULL | Master region, base address |
| PERI_MS_PPU_FX476_MS_SIZE | 0x40027F24 | FULL | Master region, size |
| PERI_MS_PPU_FX476_MS_ATT0 | 0x40027F30 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX476_MS_ATT1 | 0x40027F34 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX476_MS_ATT2 | 0x40027F38 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX476_MS_ATT3 | 0x40027F3C | FULL | Master attributes 3 |

## 23.494 PPU_FX 477

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX477_SL_ADDR | 0x40027F40 | FULL | Slave region, base address |
| PERI_MS_PPU_FX477_SL_SIZE | 0x40027F44 | FULL | Slave region, size |
| PERI_MS_PPU_FX477_SL_ATT0 | 0x40027F50 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX477_SL_ATT1 | 0x40027F54 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX477_SL_ATT2 | 0x40027F58 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX477_SL_ATT3 | 0x40027F5C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX477_MS_ADDR | 0x40027F60 | FULL | Master region, base address |
| PERI_MS_PPU_FX477_MS_SIZE | 0x40027F64 | FULL | Master region, size |
| PERI_MS_PPU_FX477_MS_ATT0 | 0x40027F70 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX477_MS_ATT1 | 0x40027F74 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX477_MS_ATT2 | 0x40027F78 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX477_MS_ATT3 | 0x40027F7C | FULL | Master attributes 3 |

## 23.495 PPU_FX 478

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX478_SL_ADDR | 0x40027F80 | FULL | Slave region, base address |
| PERI_MS_PPU_FX478_SL_SIZE | 0x40027F84 | FULL | Slave region, size |
| PERI_MS_PPU_FX478_SL_ATT0 | 0x40027F90 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX478_SL_ATT1 | 0x40027F94 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX478_SL_ATT2 | 0x40027F98 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX478_SL_ATT3 | 0x40027F9C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX478_MS_ADDR | 0x40027FA0 | FULL | Master region, base address |
| PERI_MS_PPU_FX478_MS_SIZE | 0x40027FA4 | FULL | Master region, size |
| PERI_MS_PPU_FX478_MS_ATT0 | 0x40027FB0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX478_MS_ATT1 | 0x40027FB4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX478_MS_ATT2 | 0x40027FB8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX478_MS_ATT3 | 0x40027FBC | FULL | Master attributes 3 |

## 23.496 PPU_FX 479

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX479_SL_ADDR | 0x40027FC0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX479_SL_SIZE | 0x40027FC4 | FULL | Slave region, size |
| PERI_MS_PPU_FX479_SL_ATT0 | 0x40027FD0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX479_SL_ATT1 | 0x40027FD4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX479_SL_ATT2 | 0x40027FD8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX479_SL_ATT3 | 0x40027FDC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX479_MS_ADDR | 0x40027FE0 | FULL | Master region, base address |
| PERI_MS_PPU_FX479_MS_SIZE | 0x40027FE4 | FULL | Master region, size |
| PERI_MS_PPU_FX479_MS_ATT0 | 0x40027FF0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX479_MS_ATT1 | 0x40027FF4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX479_MS_ATT2 | 0x40027FF8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX479_MS_ATT3 | 0x40027FFC | FULL | Master attributes 3 |

## 23.497 PPU_FX 480

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX480_SL_ADDR | 0x40028000 | FULL | Slave region, base address |
| PERI_MS_PPU_FX480_SL_SIZE | 0x40028004 | FULL | Slave region, size |
| PERI_MS_PPU_FX480_SL_ATT0 | 0x40028010 | FULL | Slave attributes 0 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX480_SL_ATT1 | 0x40028014 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX480_SL_ATT2 | 0x40028018 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX480_SL_ATT3 | 0x4002801C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX480_MS_ADDR | 0x40028020 | FULL | Master region, base address |
| PERI_MS_PPU_FX480_MS_SIZE | 0x40028024 | FULL | Master region, size |
| PERI_MS_PPU_FX480_MS_ATT0 | 0x40028030 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX480_MS_ATT1 | 0x40028034 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX480_MS_ATT2 | 0x40028038 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX480_MS_ATT3 | 0x4002803C | FULL | Master attributes 3 |

## 23.498 PPU_FX 481

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX481_SL_ADDR | 0x40028040 | FULL | Slave region, base address |
| PERI_MS_PPU_FX481_SL_SIZE | 0x40028044 | FULL | Slave region, size |
| PERI_MS_PPU_FX481_SL_ATT0 | 0x40028050 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX481_SL_ATT1 | 0x40028054 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX481_SL_ATT2 | 0x40028058 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX481_SL_ATT3 | 0x4002805C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX481_MS_ADDR | 0x40028060 | FULL | Master region, base address |
| PERI_MS_PPU_FX481_MS_SIZE | 0x40028064 | FULL | Master region, size |
| PERI_MS_PPU_FX481_MS_ATT0 | 0x40028070 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX481_MS_ATT1 | 0x40028074 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX481_MS_ATT2 | 0x40028078 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX481_MS_ATT3 | 0x4002807C | FULL | Master attributes 3 |

## 23.499 PPU_FX 482

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX482_SL_ADDR | 0x40028080 | FULL | Slave region, base address |
| PERI_MS_PPU_FX482_SL_SIZE | 0x40028084 | FULL | Slave region, size |
| PERI_MS_PPU_FX482_SL_ATT0 | 0x40028090 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX482_SL_ATT1 | 0x40028094 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX482_SL_ATT2 | 0x40028098 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX482_SL_ATT3 | 0x4002809C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX482_MS_ADDR | 0x400280A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX482_MS_SIZE | 0x400280A4 | FULL | Master region, size |
| PERI_MS_PPU_FX482_MS_ATT0 | 0x400280B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX482_MS_ATT1 | 0x400280B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX482_MS_ATT2 | 0x400280B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX482_MS_ATT3 | 0x400280BC | FULL | Master attributes 3 |

## 23.500 PPU_FX 483

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX483_SL_ADDR | 0x400280C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX483_SL_SIZE | 0x400280C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX483_SL_ATT0 | 0x400280D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX483_SL_ATT1 | 0x400280D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX483_SL_ATT2 | 0x400280D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX483_SL_ATT3 | 0x400280DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX483_MS_ADDR | 0x400280E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX483_MS_SIZE | 0x400280E4 | FULL | Master region, size |
| PERI_MS_PPU_FX483_MS_ATT0 | 0x400280F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX483_MS_ATT1 | 0x400280F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX483_MS_ATT2 | 0x400280F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX483_MS_ATT3 | 0x400280FC | FULL | Master attributes 3 |

## 23.501 PPU_FX 484

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX484_SL_ADDR | 0x40028100 | FULL | Slave region, base address |
| PERI_MS_PPU_FX484_SL_SIZE | 0x40028104 | FULL | Slave region, size |
| PERI_MS_PPU_FX484_SL_ATT0 | 0x40028110 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX484_SL_ATT1 | 0x40028114 | FULL | Slave attributes 1 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX484_SL_ATT2 | 0x40028118 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX484_SL_ATT3 | 0x4002811C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX484_MS_ADDR | 0x40028120 | FULL | Master region, base address |
| PERI_MS_PPU_FX484_MS_SIZE | 0x40028124 | FULL | Master region, size |
| PERI_MS_PPU_FX484_MS_ATT0 | 0x40028130 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX484_MS_ATT1 | 0x40028134 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX484_MS_ATT2 | 0x40028138 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX484_MS_ATT3 | 0x4002813C | FULL | Master attributes 3 |

## 23.502 PPU_FX 485

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX485_SL_ADDR | 0x40028140 | FULL | Slave region, base address |
| PERI_MS_PPU_FX485_SL_SIZE | 0x40028144 | FULL | Slave region, size |
| PERI_MS_PPU_FX485_SL_ATT0 | 0x40028150 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX485_SL_ATT1 | 0x40028154 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX485_SL_ATT2 | 0x40028158 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX485_SL_ATT3 | 0x4002815C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX485_MS_ADDR | 0x40028160 | FULL | Master region, base address |
| PERI_MS_PPU_FX485_MS_SIZE | 0x40028164 | FULL | Master region, size |
| PERI_MS_PPU_FX485_MS_ATT0 | 0x40028170 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX485_MS_ATT1 | 0x40028174 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX485_MS_ATT2 | 0x40028178 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX485_MS_ATT3 | 0x4002817C | FULL | Master attributes 3 |

## 23.503 PPU_FX 486

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX486_SL_ADDR | 0x40028180 | FULL | Slave region, base address |
| PERI_MS_PPU_FX486_SL_SIZE | 0x40028184 | FULL | Slave region, size |
| PERI_MS_PPU_FX486_SL_ATT0 | 0x40028190 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX486_SL_ATT1 | 0x40028194 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX486_SL_ATT2 | 0x40028198 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX486_SL_ATT3 | 0x4002819C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX486_MS_ADDR | 0x400281A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX486_MS_SIZE | 0x400281A4 | FULL | Master region, size |
| PERI_MS_PPU_FX486_MS_ATT0 | 0x400281B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX486_MS_ATT1 | 0x400281B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX486_MS_ATT2 | 0x400281B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX486_MS_ATT3 | 0x400281BC | FULL | Master attributes 3 |

## 23.504 PPU_FX 487

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX487_SL_ADDR | 0x400281C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX487_SL_SIZE | 0x400281C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX487_SL_ATT0 | 0x400281D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX487_SL_ATT1 | 0x400281D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX487_SL_ATT2 | 0x400281D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX487_SL_ATT3 | 0x400281DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX487_MS_ADDR | 0x400281E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX487_MS_SIZE | 0x400281E4 | FULL | Master region, size |
| PERI_MS_PPU_FX487_MS_ATT0 | 0x400281F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX487_MS_ATT1 | 0x400281F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX487_MS_ATT2 | 0x400281F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX487_MS_ATT3 | 0x400281FC | FULL | Master attributes 3 |

## 23.505 PPU_FX 488

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX488_SL_ADDR | 0x40028200 | FULL | Slave region, base address |
| PERI_MS_PPU_FX488_SL_SIZE | 0x40028204 | FULL | Slave region, size |
| PERI_MS_PPU_FX488_SL_ATT0 | 0x40028210 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX488_SL_ATT1 | 0x40028214 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX488_SL_ATT2 | 0x40028218 | FULL | Slave attributes 2 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX488_SL_ATT3 | 0x4002821C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX488_MS_ADDR | 0x40028220 | FULL | Master region, base address |
| PERI_MS_PPU_FX488_MS_SIZE | 0x40028224 | FULL | Master region, size |
| PERI_MS_PPU_FX488_MS_ATT0 | 0x40028230 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX488_MS_ATT1 | 0x40028234 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX488_MS_ATT2 | 0x40028238 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX488_MS_ATT3 | 0x4002823C | FULL | Master attributes 3 |

## 23.506 PPU_FX 489

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX489_SL_ADDR | 0x40028240 | FULL | Slave region, base address |
| PERI_MS_PPU_FX489_SL_SIZE | 0x40028244 | FULL | Slave region, size |
| PERI_MS_PPU_FX489_SL_ATT0 | 0x40028250 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX489_SL_ATT1 | 0x40028254 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX489_SL_ATT2 | 0x40028258 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX489_SL_ATT3 | 0x4002825C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX489_MS_ADDR | 0x40028260 | FULL | Master region, base address |
| PERI_MS_PPU_FX489_MS_SIZE | 0x40028264 | FULL | Master region, size |
| PERI_MS_PPU_FX489_MS_ATT0 | 0x40028270 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX489_MS_ATT1 | 0x40028274 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX489_MS_ATT2 | 0x40028278 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX489_MS_ATT3 | 0x4002827C | FULL | Master attributes 3 |

## 23.507 PPU_FX 490

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX490_SL_ADDR | 0x40028280 | FULL | Slave region, base address |
| PERI_MS_PPU_FX490_SL_SIZE | 0x40028284 | FULL | Slave region, size |
| PERI_MS_PPU_FX490_SL_ATT0 | 0x40028290 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX490_SL_ATT1 | 0x40028294 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX490_SL_ATT2 | 0x40028298 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX490_SL_ATT3 | 0x4002829C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX490_MS_ADDR | 0x400282A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX490_MS_SIZE | 0x400282A4 | FULL | Master region, size |
| PERI_MS_PPU_FX490_MS_ATT0 | 0x400282B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX490_MS_ATT1 | 0x400282B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX490_MS_ATT2 | 0x400282B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX490_MS_ATT3 | 0x400282BC | FULL | Master attributes 3 |

## 23.508 PPU_FX 491

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX491_SL_ADDR | 0x400282C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX491_SL_SIZE | 0x400282C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX491_SL_ATT0 | 0x400282D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX491_SL_ATT1 | 0x400282D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX491_SL_ATT2 | 0x400282D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX491_SL_ATT3 | 0x400282DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX491_MS_ADDR | 0x400282E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX491_MS_SIZE | 0x400282E4 | FULL | Master region, size |
| PERI_MS_PPU_FX491_MS_ATT0 | 0x400282F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX491_MS_ATT1 | 0x400282F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX491_MS_ATT2 | 0x400282F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX491_MS_ATT3 | 0x400282FC | FULL | Master attributes 3 |

## 23.509 PPU_FX 492

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX492_SL_ADDR | 0x40028300 | FULL | Slave region, base address |
| PERI_MS_PPU_FX492_SL_SIZE | 0x40028304 | FULL | Slave region, size |
| PERI_MS_PPU_FX492_SL_ATT0 | 0x40028310 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX492_SL_ATT1 | 0x40028314 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX492_SL_ATT2 | 0x40028318 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX492_SL_ATT3 | 0x4002831C | FULL | Slave attributes 3 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX492_MS_ADDR | 0x40028320 | FULL | Master region, base address |
| PERI_MS_PPU_FX492_MS_SIZE | 0x40028324 | FULL | Master region, size |
| PERI_MS_PPU_FX492_MS_ATT0 | 0x40028330 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX492_MS_ATT1 | 0x40028334 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX492_MS_ATT2 | 0x40028338 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX492_MS_ATT3 | 0x4002833C | FULL | Master attributes 3 |

## 23.510 PPU_FX 493

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX493_SL_ADDR | 0x40028340 | FULL | Slave region, base address |
| PERI_MS_PPU_FX493_SL_SIZE | 0x40028344 | FULL | Slave region, size |
| PERI_MS_PPU_FX493_SL_ATT0 | 0x40028350 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX493_SL_ATT1 | 0x40028354 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX493_SL_ATT2 | 0x40028358 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX493_SL_ATT3 | 0x4002835C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX493_MS_ADDR | 0x40028360 | FULL | Master region, base address |
| PERI_MS_PPU_FX493_MS_SIZE | 0x40028364 | FULL | Master region, size |
| PERI_MS_PPU_FX493_MS_ATT0 | 0x40028370 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX493_MS_ATT1 | 0x40028374 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX493_MS_ATT2 | 0x40028378 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX493_MS_ATT3 | 0x4002837C | FULL | Master attributes 3 |

## 23.511 PPU_FX 494

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX494_SL_ADDR | 0x40028380 | FULL | Slave region, base address |
| PERI_MS_PPU_FX494_SL_SIZE | 0x40028384 | FULL | Slave region, size |
| PERI_MS_PPU_FX494_SL_ATT0 | 0x40028390 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX494_SL_ATT1 | 0x40028394 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX494_SL_ATT2 | 0x40028398 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX494_SL_ATT3 | 0x4002839C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX494_MS_ADDR | 0x400283A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX494_MS_SIZE | 0x400283A4 | FULL | Master region, size |
| PERI_MS_PPU_FX494_MS_ATT0 | 0x400283B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX494_MS_ATT1 | 0x400283B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX494_MS_ATT2 | 0x400283B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX494_MS_ATT3 | 0x400283BC | FULL | Master attributes 3 |

## 23.512 PPU_FX 495

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX495_SL_ADDR | 0x400283C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX495_SL_SIZE | 0x400283C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX495_SL_ATT0 | 0x400283D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX495_SL_ATT1 | 0x400283D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX495_SL_ATT2 | 0x400283D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX495_SL_ATT3 | 0x400283DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX495_MS_ADDR | 0x400283E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX495_MS_SIZE | 0x400283E4 | FULL | Master region, size |
| PERI_MS_PPU_FX495_MS_ATT0 | 0x400283F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX495_MS_ATT1 | 0x400283F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX495_MS_ATT2 | 0x400283F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX495_MS_ATT3 | 0x400283FC | FULL | Master attributes 3 |

## 23.513 PPU_FX 496

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX496_SL_ADDR | 0x40028400 | FULL | Slave region, base address |
| PERI_MS_PPU_FX496_SL_SIZE | 0x40028404 | FULL | Slave region, size |
| PERI_MS_PPU_FX496_SL_ATT0 | 0x40028410 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX496_SL_ATT1 | 0x40028414 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX496_SL_ATT2 | 0x40028418 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX496_SL_ATT3 | 0x4002841C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX496_MS_ADDR | 0x40028420 | FULL | Master region, base address |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX496_MS_SIZE | 0x40028424 | FULL | Master region, size |
| PERI_MS_PPU_FX496_MS_ATT0 | 0x40028430 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX496_MS_ATT1 | 0x40028434 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX496_MS_ATT2 | 0x40028438 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX496_MS_ATT3 | 0x4002843C | FULL | Master attributes 3 |

## 23.514 PPU_FX 497

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX497_SL_ADDR | 0x40028440 | FULL | Slave region, base address |
| PERI_MS_PPU_FX497_SL_SIZE | 0x40028444 | FULL | Slave region, size |
| PERI_MS_PPU_FX497_SL_ATT0 | 0x40028450 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX497_SL_ATT1 | 0x40028454 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX497_SL_ATT2 | 0x40028458 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX497_SL_ATT3 | 0x4002845C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX497_MS_ADDR | 0x40028460 | FULL | Master region, base address |
| PERI_MS_PPU_FX497_MS_SIZE | 0x40028464 | FULL | Master region, size |
| PERI_MS_PPU_FX497_MS_ATT0 | 0x40028470 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX497_MS_ATT1 | 0x40028474 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX497_MS_ATT2 | 0x40028478 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX497_MS_ATT3 | 0x4002847C | FULL | Master attributes 3 |

## 23.515 PPU_FX 498

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX498_SL_ADDR | 0x40028480 | FULL | Slave region, base address |
| PERI_MS_PPU_FX498_SL_SIZE | 0x40028484 | FULL | Slave region, size |
| PERI_MS_PPU_FX498_SL_ATT0 | 0x40028490 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX498_SL_ATT1 | 0x40028494 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX498_SL_ATT2 | 0x40028498 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX498_SL_ATT3 | 0x4002849C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX498_MS_ADDR | 0x400284A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX498_MS_SIZE | 0x400284A4 | FULL | Master region, size |
| PERI_MS_PPU_FX498_MS_ATT0 | 0x400284B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX498_MS_ATT1 | 0x400284B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX498_MS_ATT2 | 0x400284B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX498_MS_ATT3 | 0x400284BC | FULL | Master attributes 3 |

## 23.516 PPU_FX 499

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX499_SL_ADDR | 0x400284C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX499_SL_SIZE | 0x400284C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX499_SL_ATT0 | 0x400284D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX499_SL_ATT1 | 0x400284D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX499_SL_ATT2 | 0x400284D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX499_SL_ATT3 | 0x400284DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX499_MS_ADDR | 0x400284E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX499_MS_SIZE | 0x400284E4 | FULL | Master region, size |
| PERI_MS_PPU_FX499_MS_ATT0 | 0x400284F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX499_MS_ATT1 | 0x400284F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX499_MS_ATT2 | 0x400284F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX499_MS_ATT3 | 0x400284FC | FULL | Master attributes 3 |

## 23.517 PPU_FX 500

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX500_SL_ADDR | 0x40028500 | FULL | Slave region, base address |
| PERI_MS_PPU_FX500_SL_SIZE | 0x40028504 | FULL | Slave region, size |
| PERI_MS_PPU_FX500_SL_ATT0 | 0x40028510 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX500_SL_ATT1 | 0x40028514 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX500_SL_ATT2 | 0x40028518 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX500_SL_ATT3 | 0x4002851C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX500_MS_ADDR | 0x40028520 | FULL | Master region, base address |
| PERI_MS_PPU_FX500_MS_SIZE | 0x40028524 | FULL | Master region, size |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX500_MS_ATT0 | 0x40028530 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX500_MS_ATT1 | 0x40028534 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX500_MS_ATT2 | 0x40028538 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX500_MS_ATT3 | 0x4002853C | FULL | Master attributes 3 |

## 23.518 PPU_FX 501

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX501_SL_ADDR | 0x40028540 | FULL | Slave region, base address |
| PERI_MS_PPU_FX501_SL_SIZE | 0x40028544 | FULL | Slave region, size |
| PERI_MS_PPU_FX501_SL_ATT0 | 0x40028550 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX501_SL_ATT1 | 0x40028554 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX501_SL_ATT2 | 0x40028558 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX501_SL_ATT3 | 0x4002855C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX501_MS_ADDR | 0x40028560 | FULL | Master region, base address |
| PERI_MS_PPU_FX501_MS_SIZE | 0x40028564 | FULL | Master region, size |
| PERI_MS_PPU_FX501_MS_ATT0 | 0x40028570 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX501_MS_ATT1 | 0x40028574 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX501_MS_ATT2 | 0x40028578 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX501_MS_ATT3 | 0x4002857C | FULL | Master attributes 3 |

## 23.519 PPU_FX 502

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX502_SL_ADDR | 0x40028580 | FULL | Slave region, base address |
| PERI_MS_PPU_FX502_SL_SIZE | 0x40028584 | FULL | Slave region, size |
| PERI_MS_PPU_FX502_SL_ATT0 | 0x40028590 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX502_SL_ATT1 | 0x40028594 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX502_SL_ATT2 | 0x40028598 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX502_SL_ATT3 | 0x4002859C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX502_MS_ADDR | 0x400285A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX502_MS_SIZE | 0x400285A4 | FULL | Master region, size |
| PERI_MS_PPU_FX502_MS_ATT0 | 0x400285B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX502_MS_ATT1 | 0x400285B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX502_MS_ATT2 | 0x400285B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX502_MS_ATT3 | 0x400285BC | FULL | Master attributes 3 |

## 23.520 PPU_FX 503

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX503_SL_ADDR | 0x400285C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX503_SL_SIZE | 0x400285C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX503_SL_ATT0 | 0x400285D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX503_SL_ATT1 | 0x400285D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX503_SL_ATT2 | 0x400285D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX503_SL_ATT3 | 0x400285DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX503_MS_ADDR | 0x400285E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX503_MS_SIZE | 0x400285E4 | FULL | Master region, size |
| PERI_MS_PPU_FX503_MS_ATT0 | 0x400285F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX503_MS_ATT1 | 0x400285F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX503_MS_ATT2 | 0x400285F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX503_MS_ATT3 | 0x400285FC | FULL | Master attributes 3 |

## 23.521 PPU_FX 504

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX504_SL_ADDR | 0x40028600 | FULL | Slave region, base address |
| PERI_MS_PPU_FX504_SL_SIZE | 0x40028604 | FULL | Slave region, size |
| PERI_MS_PPU_FX504_SL_ATT0 | 0x40028610 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX504_SL_ATT1 | 0x40028614 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX504_SL_ATT2 | 0x40028618 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX504_SL_ATT3 | 0x4002861C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX504_MS_ADDR | 0x40028620 | FULL | Master region, base address |
| PERI_MS_PPU_FX504_MS_SIZE | 0x40028624 | FULL | Master region, size |
| PERI_MS_PPU_FX504_MS_ATT0 | 0x40028630 | FULL | Master attributes 0 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX504_MS_ATT1 | 0x40028634 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX504_MS_ATT2 | 0x40028638 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX504_MS_ATT3 | 0x4002863C | FULL | Master attributes 3 |

## 23.522 PPU_FX 505

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX505_SL_ADDR | 0x40028640 | FULL | Slave region, base address |
| PERI_MS_PPU_FX505_SL_SIZE | 0x40028644 | FULL | Slave region, size |
| PERI_MS_PPU_FX505_SL_ATT0 | 0x40028650 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX505_SL_ATT1 | 0x40028654 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX505_SL_ATT2 | 0x40028658 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX505_SL_ATT3 | 0x4002865C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX505_MS_ADDR | 0x40028660 | FULL | Master region, base address |
| PERI_MS_PPU_FX505_MS_SIZE | 0x40028664 | FULL | Master region, size |
| PERI_MS_PPU_FX505_MS_ATT0 | 0x40028670 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX505_MS_ATT1 | 0x40028674 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX505_MS_ATT2 | 0x40028678 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX505_MS_ATT3 | 0x4002867C | FULL | Master attributes 3 |

## 23.523 PPU_FX 506

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX506_SL_ADDR | 0x40028680 | FULL | Slave region, base address |
| PERI_MS_PPU_FX506_SL_SIZE | 0x40028684 | FULL | Slave region, size |
| PERI_MS_PPU_FX506_SL_ATT0 | 0x40028690 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX506_SL_ATT1 | 0x40028694 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX506_SL_ATT2 | 0x40028698 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX506_SL_ATT3 | 0x4002869C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX506_MS_ADDR | 0x400286A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX506_MS_SIZE | 0x400286A4 | FULL | Master region, size |
| PERI_MS_PPU_FX506_MS_ATT0 | 0x400286B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX506_MS_ATT1 | 0x400286B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX506_MS_ATT2 | 0x400286B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX506_MS_ATT3 | 0x400286BC | FULL | Master attributes 3 |

## 23.524 PPU_FX 507

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX507_SL_ADDR | 0x400286C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX507_SL_SIZE | 0x400286C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX507_SL_ATT0 | 0x400286D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX507_SL_ATT1 | 0x400286D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX507_SL_ATT2 | 0x400286D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX507_SL_ATT3 | 0x400286DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX507_MS_ADDR | 0x400286E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX507_MS_SIZE | 0x400286E4 | FULL | Master region, size |
| PERI_MS_PPU_FX507_MS_ATT0 | 0x400286F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX507_MS_ATT1 | 0x400286F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX507_MS_ATT2 | 0x400286F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX507_MS_ATT3 | 0x400286FC | FULL | Master attributes 3 |

## 23.525 PPU_FX 508

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX508_SL_ADDR | 0x40028700 | FULL | Slave region, base address |
| PERI_MS_PPU_FX508_SL_SIZE | 0x40028704 | FULL | Slave region, size |
| PERI_MS_PPU_FX508_SL_ATT0 | 0x40028710 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX508_SL_ATT1 | 0x40028714 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX508_SL_ATT2 | 0x40028718 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX508_SL_ATT3 | 0x4002871C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX508_MS_ADDR | 0x40028720 | FULL | Master region, base address |
| PERI_MS_PPU_FX508_MS_SIZE | 0x40028724 | FULL | Master region, size |
| PERI_MS_PPU_FX508_MS_ATT0 | 0x40028730 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX508_MS_ATT1 | 0x40028734 | FULL | Master attributes 1 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX508_MS_ATT2 | 0x40028738 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX508_MS_ATT3 | 0x4002873C | FULL | Master attributes 3 |

## 23.526 PPU_FX 509

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX509_SL_ADDR | 0x40028740 | FULL | Slave region, base address |
| PERI_MS_PPU_FX509_SL_SIZE | 0x40028744 | FULL | Slave region, size |
| PERI_MS_PPU_FX509_SL_ATT0 | 0x40028750 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX509_SL_ATT1 | 0x40028754 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX509_SL_ATT2 | 0x40028758 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX509_SL_ATT3 | 0x4002875C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX509_MS_ADDR | 0x40028760 | FULL | Master region, base address |
| PERI_MS_PPU_FX509_MS_SIZE | 0x40028764 | FULL | Master region, size |
| PERI_MS_PPU_FX509_MS_ATT0 | 0x40028770 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX509_MS_ATT1 | 0x40028774 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX509_MS_ATT2 | 0x40028778 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX509_MS_ATT3 | 0x4002877C | FULL | Master attributes 3 |

## 23.527 PPU_FX 510

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX510_SL_ADDR | 0x40028780 | FULL | Slave region, base address |
| PERI_MS_PPU_FX510_SL_SIZE | 0x40028784 | FULL | Slave region, size |
| PERI_MS_PPU_FX510_SL_ATT0 | 0x40028790 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX510_SL_ATT1 | 0x40028794 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX510_SL_ATT2 | 0x40028798 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX510_SL_ATT3 | 0x4002879C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX510_MS_ADDR | 0x400287A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX510_MS_SIZE | 0x400287A4 | FULL | Master region, size |
| PERI_MS_PPU_FX510_MS_ATT0 | 0x400287B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX510_MS_ATT1 | 0x400287B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX510_MS_ATT2 | 0x400287B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX510_MS_ATT3 | 0x400287BC | FULL | Master attributes 3 |

## 23.528 PPU_FX 511

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX511_SL_ADDR | 0x400287C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX511_SL_SIZE | 0x400287C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX511_SL_ATT0 | 0x400287D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX511_SL_ATT1 | 0x400287D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX511_SL_ATT2 | 0x400287D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX511_SL_ATT3 | 0x400287DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX511_MS_ADDR | 0x400287E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX511_MS_SIZE | 0x400287E4 | FULL | Master region, size |
| PERI_MS_PPU_FX511_MS_ATT0 | 0x400287F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX511_MS_ATT1 | 0x400287F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX511_MS_ATT2 | 0x400287F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX511_MS_ATT3 | 0x400287FC | FULL | Master attributes 3 |

## 23.529 PPU_FX 512

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX512_SL_ADDR | 0x40028800 | FULL | Slave region, base address |
| PERI_MS_PPU_FX512_SL_SIZE | 0x40028804 | FULL | Slave region, size |
| PERI_MS_PPU_FX512_SL_ATT0 | 0x40028810 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX512_SL_ATT1 | 0x40028814 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX512_SL_ATT2 | 0x40028818 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX512_SL_ATT3 | 0x4002881C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX512_MS_ADDR | 0x40028820 | FULL | Master region, base address |
| PERI_MS_PPU_FX512_MS_SIZE | 0x40028824 | FULL | Master region, size |
| PERI_MS_PPU_FX512_MS_ATT0 | 0x40028830 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX512_MS_ATT1 | 0x40028834 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX512_MS_ATT2 | 0x40028838 | FULL | Master attributes 2 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX512_MS_ATT3 | 0x4002883C | FULL | Master attributes 3 |

## 23.530 PPU_FX 513

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX513_SL_ADDR | 0x40028840 | FULL | Slave region, base address |
| PERI_MS_PPU_FX513_SL_SIZE | 0x40028844 | FULL | Slave region, size |
| PERI_MS_PPU_FX513_SL_ATT0 | 0x40028850 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX513_SL_ATT1 | 0x40028854 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX513_SL_ATT2 | 0x40028858 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX513_SL_ATT3 | 0x4002885C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX513_MS_ADDR | 0x40028860 | FULL | Master region, base address |
| PERI_MS_PPU_FX513_MS_SIZE | 0x40028864 | FULL | Master region, size |
| PERI_MS_PPU_FX513_MS_ATT0 | 0x40028870 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX513_MS_ATT1 | 0x40028874 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX513_MS_ATT2 | 0x40028878 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX513_MS_ATT3 | 0x4002887C | FULL | Master attributes 3 |

## 23.531 PPU_FX 514

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX514_SL_ADDR | 0x40028880 | FULL | Slave region, base address |
| PERI_MS_PPU_FX514_SL_SIZE | 0x40028884 | FULL | Slave region, size |
| PERI_MS_PPU_FX514_SL_ATT0 | 0x40028890 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX514_SL_ATT1 | 0x40028894 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX514_SL_ATT2 | 0x40028898 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX514_SL_ATT3 | 0x4002889C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX514_MS_ADDR | 0x400288A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX514_MS_SIZE | 0x400288A4 | FULL | Master region, size |
| PERI_MS_PPU_FX514_MS_ATT0 | 0x400288B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX514_MS_ATT1 | 0x400288B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX514_MS_ATT2 | 0x400288B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX514_MS_ATT3 | 0x400288BC | FULL | Master attributes 3 |

## 23.532 PPU_FX 515

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX515_SL_ADDR | 0x400288C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX515_SL_SIZE | 0x400288C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX515_SL_ATT0 | 0x400288D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX515_SL_ATT1 | 0x400288D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX515_SL_ATT2 | 0x400288D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX515_SL_ATT3 | 0x400288DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX515_MS_ADDR | 0x400288E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX515_MS_SIZE | 0x400288E4 | FULL | Master region, size |
| PERI_MS_PPU_FX515_MS_ATT0 | 0x400288F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX515_MS_ATT1 | 0x400288F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX515_MS_ATT2 | 0x400288F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX515_MS_ATT3 | 0x400288FC | FULL | Master attributes 3 |

## 23.533 PPU_FX 516

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX516_SL_ADDR | 0x40028900 | FULL | Slave region, base address |
| PERI_MS_PPU_FX516_SL_SIZE | 0x40028904 | FULL | Slave region, size |
| PERI_MS_PPU_FX516_SL_ATT0 | 0x40028910 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX516_SL_ATT1 | 0x40028914 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX516_SL_ATT2 | 0x40028918 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX516_SL_ATT3 | 0x4002891C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX516_MS_ADDR | 0x40028920 | FULL | Master region, base address |
| PERI_MS_PPU_FX516_MS_SIZE | 0x40028924 | FULL | Master region, size |
| PERI_MS_PPU_FX516_MS_ATT0 | 0x40028930 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX516_MS_ATT1 | 0x40028934 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX516_MS_ATT2 | 0x40028938 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX516_MS_ATT3 | 0x4002893C | FULL | Master attributes 3 |

## 23.534 PPU_FX 517

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX517_SL_ADDR | 0x40028940 | FULL | Slave region, base address |
| PERI_MS_PPU_FX517_SL_SIZE | 0x40028944 | FULL | Slave region, size |
| PERI_MS_PPU_FX517_SL_ATT0 | 0x40028950 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX517_SL_ATT1 | 0x40028954 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX517_SL_ATT2 | 0x40028958 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX517_SL_ATT3 | 0x4002895C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX517_MS_ADDR | 0x40028960 | FULL | Master region, base address |
| PERI_MS_PPU_FX517_MS_SIZE | 0x40028964 | FULL | Master region, size |
| PERI_MS_PPU_FX517_MS_ATT0 | 0x40028970 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX517_MS_ATT1 | 0x40028974 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX517_MS_ATT2 | 0x40028978 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX517_MS_ATT3 | 0x4002897C | FULL | Master attributes 3 |

## 23.535 PPU_FX 518

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX518_SL_ADDR | 0x40028980 | FULL | Slave region, base address |
| PERI_MS_PPU_FX518_SL_SIZE | 0x40028984 | FULL | Slave region, size |
| PERI_MS_PPU_FX518_SL_ATT0 | 0x40028990 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX518_SL_ATT1 | 0x40028994 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX518_SL_ATT2 | 0x40028998 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX518_SL_ATT3 | 0x4002899C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX518_MS_ADDR | 0x400289A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX518_MS_SIZE | 0x400289A4 | FULL | Master region, size |
| PERI_MS_PPU_FX518_MS_ATT0 | 0x400289B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX518_MS_ATT1 | 0x400289B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX518_MS_ATT2 | 0x400289B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX518_MS_ATT3 | 0x400289BC | FULL | Master attributes 3 |

## 23.536 PPU_FX 519

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX519_SL_ADDR | 0x400289C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX519_SL_SIZE | 0x400289C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX519_SL_ATT0 | 0x400289D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX519_SL_ATT1 | 0x400289D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX519_SL_ATT2 | 0x400289D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX519_SL_ATT3 | 0x400289DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX519_MS_ADDR | 0x400289E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX519_MS_SIZE | 0x400289E4 | FULL | Master region, size |
| PERI_MS_PPU_FX519_MS_ATT0 | 0x400289F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX519_MS_ATT1 | 0x400289F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX519_MS_ATT2 | 0x400289F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX519_MS_ATT3 | 0x400289FC | FULL | Master attributes 3 |

## 23.537 PPU_FX 520

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX520_SL_ADDR | 0x40028A00 | FULL | Slave region, base address |
| PERI_MS_PPU_FX520_SL_SIZE | 0x40028A04 | FULL | Slave region, size |
| PERI_MS_PPU_FX520_SL_ATT0 | 0x40028A10 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX520_SL_ATT1 | 0x40028A14 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX520_SL_ATT2 | 0x40028A18 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX520_SL_ATT3 | 0x40028A1C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX520_MS_ADDR | 0x40028A20 | FULL | Master region, base address |
| PERI_MS_PPU_FX520_MS_SIZE | 0x40028A24 | FULL | Master region, size |
| PERI_MS_PPU_FX520_MS_ATT0 | 0x40028A30 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX520_MS_ATT1 | 0x40028A34 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX520_MS_ATT2 | 0x40028A38 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX520_MS_ATT3 | 0x40028A3C | FULL | Master attributes 3 |

## 23.538 PPU_FX 521

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX521_SL_ADDR | 0x40028A40 | FULL | Slave region, base address |
| PERI_MS_PPU_FX521_SL_SIZE | 0x40028A44 | FULL | Slave region, size |
| PERI_MS_PPU_FX521_SL_ATT0 | 0x40028A50 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX521_SL_ATT1 | 0x40028A54 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX521_SL_ATT2 | 0x40028A58 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX521_SL_ATT3 | 0x40028A5C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX521_MS_ADDR | 0x40028A60 | FULL | Master region, base address |
| PERI_MS_PPU_FX521_MS_SIZE | 0x40028A64 | FULL | Master region, size |
| PERI_MS_PPU_FX521_MS_ATT0 | 0x40028A70 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX521_MS_ATT1 | 0x40028A74 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX521_MS_ATT2 | 0x40028A78 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX521_MS_ATT3 | 0x40028A7C | FULL | Master attributes 3 |

## 23.539 PPU_FX 522

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX522_SL_ADDR | 0x40028A80 | FULL | Slave region, base address |
| PERI_MS_PPU_FX522_SL_SIZE | 0x40028A84 | FULL | Slave region, size |
| PERI_MS_PPU_FX522_SL_ATT0 | 0x40028A90 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX522_SL_ATT1 | 0x40028A94 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX522_SL_ATT2 | 0x40028A98 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX522_SL_ATT3 | 0x40028A9C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX522_MS_ADDR | 0x40028AA0 | FULL | Master region, base address |
| PERI_MS_PPU_FX522_MS_SIZE | 0x40028AA4 | FULL | Master region, size |
| PERI_MS_PPU_FX522_MS_ATT0 | 0x40028AB0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX522_MS_ATT1 | 0x40028AB4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX522_MS_ATT2 | 0x40028AB8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX522_MS_ATT3 | 0x40028ABC | FULL | Master attributes 3 |

## 23.540 PPU_FX 523

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX523_SL_ADDR | 0x40028AC0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX523_SL_SIZE | 0x40028AC4 | FULL | Slave region, size |
| PERI_MS_PPU_FX523_SL_ATT0 | 0x40028AD0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX523_SL_ATT1 | 0x40028AD4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX523_SL_ATT2 | 0x40028AD8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX523_SL_ATT3 | 0x40028ADC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX523_MS_ADDR | 0x40028AE0 | FULL | Master region, base address |
| PERI_MS_PPU_FX523_MS_SIZE | 0x40028AE4 | FULL | Master region, size |
| PERI_MS_PPU_FX523_MS_ATT0 | 0x40028AF0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX523_MS_ATT1 | 0x40028AF4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX523_MS_ATT2 | 0x40028AF8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX523_MS_ATT3 | 0x40028AFC | FULL | Master attributes 3 |

## 23.541 PPU_FX 524

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX524_SL_ADDR | 0x40028B00 | FULL | Slave region, base address |
| PERI_MS_PPU_FX524_SL_SIZE | 0x40028B04 | FULL | Slave region, size |
| PERI_MS_PPU_FX524_SL_ATT0 | 0x40028B10 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX524_SL_ATT1 | 0x40028B14 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX524_SL_ATT2 | 0x40028B18 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX524_SL_ATT3 | 0x40028B1C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX524_MS_ADDR | 0x40028B20 | FULL | Master region, base address |
| PERI_MS_PPU_FX524_MS_SIZE | 0x40028B24 | FULL | Master region, size |
| PERI_MS_PPU_FX524_MS_ATT0 | 0x40028B30 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX524_MS_ATT1 | 0x40028B34 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX524_MS_ATT2 | 0x40028B38 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX524_MS_ATT3 | 0x40028B3C | FULL | Master attributes 3 |

## 23.542 PPU_FX 525

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX525_SL_ADDR | 0x40028B40 | FULL | Slave region, base address |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX525_SL_SIZE | 0x40028B44 | FULL | Slave region, size |
| PERI_MS_PPU_FX525_SL_ATT0 | 0x40028B50 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX525_SL_ATT1 | 0x40028B54 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX525_SL_ATT2 | 0x40028B58 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX525_SL_ATT3 | 0x40028B5C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX525_MS_ADDR | 0x40028B60 | FULL | Master region, base address |
| PERI_MS_PPU_FX525_MS_SIZE | 0x40028B64 | FULL | Master region, size |
| PERI_MS_PPU_FX525_MS_ATT0 | 0x40028B70 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX525_MS_ATT1 | 0x40028B74 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX525_MS_ATT2 | 0x40028B78 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX525_MS_ATT3 | 0x40028B7C | FULL | Master attributes 3 |

## 23.543 PPU_FX 526

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX526_SL_ADDR | 0x40028B80 | FULL | Slave region, base address |
| PERI_MS_PPU_FX526_SL_SIZE | 0x40028B84 | FULL | Slave region, size |
| PERI_MS_PPU_FX526_SL_ATT0 | 0x40028B90 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX526_SL_ATT1 | 0x40028B94 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX526_SL_ATT2 | 0x40028B98 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX526_SL_ATT3 | 0x40028B9C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX526_MS_ADDR | 0x40028BA0 | FULL | Master region, base address |
| PERI_MS_PPU_FX526_MS_SIZE | 0x40028BA4 | FULL | Master region, size |
| PERI_MS_PPU_FX526_MS_ATT0 | 0x40028BB0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX526_MS_ATT1 | 0x40028BB4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX526_MS_ATT2 | 0x40028BB8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX526_MS_ATT3 | 0x40028BBC | FULL | Master attributes 3 |

## 23.544 PPU_FX 527

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX527_SL_ADDR | 0x40028BC0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX527_SL_SIZE | 0x40028BC4 | FULL | Slave region, size |
| PERI_MS_PPU_FX527_SL_ATT0 | 0x40028BD0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX527_SL_ATT1 | 0x40028BD4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX527_SL_ATT2 | 0x40028BD8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX527_SL_ATT3 | 0x40028BDC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX527_MS_ADDR | 0x40028BE0 | FULL | Master region, base address |
| PERI_MS_PPU_FX527_MS_SIZE | 0x40028BE4 | FULL | Master region, size |
| PERI_MS_PPU_FX527_MS_ATT0 | 0x40028BF0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX527_MS_ATT1 | 0x40028BF4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX527_MS_ATT2 | 0x40028BF8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX527_MS_ATT3 | 0x40028BFC | FULL | Master attributes 3 |

## 23.545 PPU_FX 528

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX528_SL_ADDR | 0x40028C00 | FULL | Slave region, base address |
| PERI_MS_PPU_FX528_SL_SIZE | 0x40028C04 | FULL | Slave region, size |
| PERI_MS_PPU_FX528_SL_ATT0 | 0x40028C10 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX528_SL_ATT1 | 0x40028C14 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX528_SL_ATT2 | 0x40028C18 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX528_SL_ATT3 | 0x40028C1C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX528_MS_ADDR | 0x40028C20 | FULL | Master region, base address |
| PERI_MS_PPU_FX528_MS_SIZE | 0x40028C24 | FULL | Master region, size |
| PERI_MS_PPU_FX528_MS_ATT0 | 0x40028C30 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX528_MS_ATT1 | 0x40028C34 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX528_MS_ATT2 | 0x40028C38 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX528_MS_ATT3 | 0x40028C3C | FULL | Master attributes 3 |

## 23.546 PPU_FX 529

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX529_SL_ADDR | 0x40028C40 | FULL | Slave region, base address |
| PERI_MS_PPU_FX529_SL_SIZE | 0x40028C44 | FULL | Slave region, size |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX529_SL_ATT0 | 0x40028C50 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX529_SL_ATT1 | 0x40028C54 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX529_SL_ATT2 | 0x40028C58 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX529_SL_ATT3 | 0x40028C5C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX529_MS_ADDR | 0x40028C60 | FULL | Master region, base address |
| PERI_MS_PPU_FX529_MS_SIZE | 0x40028C64 | FULL | Master region, size |
| PERI_MS_PPU_FX529_MS_ATT0 | 0x40028C70 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX529_MS_ATT1 | 0x40028C74 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX529_MS_ATT2 | 0x40028C78 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX529_MS_ATT3 | 0x40028C7C | FULL | Master attributes 3 |

## 23.547 PPU_FX 530

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX530_SL_ADDR | 0x40028C80 | FULL | Slave region, base address |
| PERI_MS_PPU_FX530_SL_SIZE | 0x40028C84 | FULL | Slave region, size |
| PERI_MS_PPU_FX530_SL_ATT0 | 0x40028C90 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX530_SL_ATT1 | 0x40028C94 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX530_SL_ATT2 | 0x40028C98 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX530_SL_ATT3 | 0x40028C9C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX530_MS_ADDR | 0x40028CA0 | FULL | Master region, base address |
| PERI_MS_PPU_FX530_MS_SIZE | 0x40028CA4 | FULL | Master region, size |
| PERI_MS_PPU_FX530_MS_ATT0 | 0x40028CB0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX530_MS_ATT1 | 0x40028CB4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX530_MS_ATT2 | 0x40028CB8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX530_MS_ATT3 | 0x40028CBC | FULL | Master attributes 3 |

## 23.548 PPU_FX 531

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX531_SL_ADDR | 0x40028CC0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX531_SL_SIZE | 0x40028CC4 | FULL | Slave region, size |
| PERI_MS_PPU_FX531_SL_ATT0 | 0x40028CD0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX531_SL_ATT1 | 0x40028CD4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX531_SL_ATT2 | 0x40028CD8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX531_SL_ATT3 | 0x40028CDC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX531_MS_ADDR | 0x40028CE0 | FULL | Master region, base address |
| PERI_MS_PPU_FX531_MS_SIZE | 0x40028CE4 | FULL | Master region, size |
| PERI_MS_PPU_FX531_MS_ATT0 | 0x40028CF0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX531_MS_ATT1 | 0x40028CF4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX531_MS_ATT2 | 0x40028CF8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX531_MS_ATT3 | 0x40028CFC | FULL | Master attributes 3 |

## 23.549 PPU_FX 532

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX532_SL_ADDR | 0x40028D00 | FULL | Slave region, base address |
| PERI_MS_PPU_FX532_SL_SIZE | 0x40028D04 | FULL | Slave region, size |
| PERI_MS_PPU_FX532_SL_ATT0 | 0x40028D10 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX532_SL_ATT1 | 0x40028D14 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX532_SL_ATT2 | 0x40028D18 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX532_SL_ATT3 | 0x40028D1C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX532_MS_ADDR | 0x40028D20 | FULL | Master region, base address |
| PERI_MS_PPU_FX532_MS_SIZE | 0x40028D24 | FULL | Master region, size |
| PERI_MS_PPU_FX532_MS_ATT0 | 0x40028D30 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX532_MS_ATT1 | 0x40028D34 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX532_MS_ATT2 | 0x40028D38 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX532_MS_ATT3 | 0x40028D3C | FULL | Master attributes 3 |

## 23.550 PPU_FX 533

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX533_SL_ADDR | 0x40028D40 | FULL | Slave region, base address |
| PERI_MS_PPU_FX533_SL_SIZE | 0x40028D44 | FULL | Slave region, size |
| PERI_MS_PPU_FX533_SL_ATT0 | 0x40028D50 | FULL | Slave attributes 0 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX533_SL_ATT1 | 0x40028D54 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX533_SL_ATT2 | 0x40028D58 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX533_SL_ATT3 | 0x40028D5C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX533_MS_ADDR | 0x40028D60 | FULL | Master region, base address |
| PERI_MS_PPU_FX533_MS_SIZE | 0x40028D64 | FULL | Master region, size |
| PERI_MS_PPU_FX533_MS_ATT0 | 0x40028D70 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX533_MS_ATT1 | 0x40028D74 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX533_MS_ATT2 | 0x40028D78 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX533_MS_ATT3 | 0x40028D7C | FULL | Master attributes 3 |

## 23.551 PPU_FX 534

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX534_SL_ADDR | 0x40028D80 | FULL | Slave region, base address |
| PERI_MS_PPU_FX534_SL_SIZE | 0x40028D84 | FULL | Slave region, size |
| PERI_MS_PPU_FX534_SL_ATT0 | 0x40028D90 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX534_SL_ATT1 | 0x40028D94 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX534_SL_ATT2 | 0x40028D98 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX534_SL_ATT3 | 0x40028D9C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX534_MS_ADDR | 0x40028DA0 | FULL | Master region, base address |
| PERI_MS_PPU_FX534_MS_SIZE | 0x40028DA4 | FULL | Master region, size |
| PERI_MS_PPU_FX534_MS_ATT0 | 0x40028DB0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX534_MS_ATT1 | 0x40028DB4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX534_MS_ATT2 | 0x40028DB8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX534_MS_ATT3 | 0x40028DBC | FULL | Master attributes 3 |

## 23.552 PPU_FX 535

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX535_SL_ADDR | 0x40028DC0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX535_SL_SIZE | 0x40028DC4 | FULL | Slave region, size |
| PERI_MS_PPU_FX535_SL_ATT0 | 0x40028DD0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX535_SL_ATT1 | 0x40028DD4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX535_SL_ATT2 | 0x40028DD8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX535_SL_ATT3 | 0x40028DDC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX535_MS_ADDR | 0x40028DE0 | FULL | Master region, base address |
| PERI_MS_PPU_FX535_MS_SIZE | 0x40028DE4 | FULL | Master region, size |
| PERI_MS_PPU_FX535_MS_ATT0 | 0x40028DF0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX535_MS_ATT1 | 0x40028DF4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX535_MS_ATT2 | 0x40028DF8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX535_MS_ATT3 | 0x40028DFC | FULL | Master attributes 3 |

## 23.553 PPU_FX 536

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX536_SL_ADDR | 0x40028E00 | FULL | Slave region, base address |
| PERI_MS_PPU_FX536_SL_SIZE | 0x40028E04 | FULL | Slave region, size |
| PERI_MS_PPU_FX536_SL_ATT0 | 0x40028E10 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX536_SL_ATT1 | 0x40028E14 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX536_SL_ATT2 | 0x40028E18 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX536_SL_ATT3 | 0x40028E1C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX536_MS_ADDR | 0x40028E20 | FULL | Master region, base address |
| PERI_MS_PPU_FX536_MS_SIZE | 0x40028E24 | FULL | Master region, size |
| PERI_MS_PPU_FX536_MS_ATT0 | 0x40028E30 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX536_MS_ATT1 | 0x40028E34 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX536_MS_ATT2 | 0x40028E38 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX536_MS_ATT3 | 0x40028E3C | FULL | Master attributes 3 |

## 23.554 PPU_FX 537

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX537_SL_ADDR | 0x40028E40 | FULL | Slave region, base address |
| PERI_MS_PPU_FX537_SL_SIZE | 0x40028E44 | FULL | Slave region, size |
| PERI_MS_PPU_FX537_SL_ATT0 | 0x40028E50 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX537_SL_ATT1 | 0x40028E54 | FULL | Slave attributes 1 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX537_SL_ATT2 | 0x40028E58 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX537_SL_ATT3 | 0x40028E5C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX537_MS_ADDR | 0x40028E60 | FULL | Master region, base address |
| PERI_MS_PPU_FX537_MS_SIZE | 0x40028E64 | FULL | Master region, size |
| PERI_MS_PPU_FX537_MS_ATT0 | 0x40028E70 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX537_MS_ATT1 | 0x40028E74 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX537_MS_ATT2 | 0x40028E78 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX537_MS_ATT3 | 0x40028E7C | FULL | Master attributes 3 |

## 23.555 PPU_FX 538

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX538_SL_ADDR | 0x40028E80 | FULL | Slave region, base address |
| PERI_MS_PPU_FX538_SL_SIZE | 0x40028E84 | FULL | Slave region, size |
| PERI_MS_PPU_FX538_SL_ATT0 | 0x40028E90 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX538_SL_ATT1 | 0x40028E94 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX538_SL_ATT2 | 0x40028E98 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX538_SL_ATT3 | 0x40028E9C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX538_MS_ADDR | 0x40028EA0 | FULL | Master region, base address |
| PERI_MS_PPU_FX538_MS_SIZE | 0x40028EA4 | FULL | Master region, size |
| PERI_MS_PPU_FX538_MS_ATT0 | 0x40028EB0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX538_MS_ATT1 | 0x40028EB4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX538_MS_ATT2 | 0x40028EB8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX538_MS_ATT3 | 0x40028EBC | FULL | Master attributes 3 |

## 23.556 PPU_FX 539

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX539_SL_ADDR | 0x40028EC0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX539_SL_SIZE | 0x40028EC4 | FULL | Slave region, size |
| PERI_MS_PPU_FX539_SL_ATT0 | 0x40028ED0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX539_SL_ATT1 | 0x40028ED4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX539_SL_ATT2 | 0x40028ED8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX539_SL_ATT3 | 0x40028EDC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX539_MS_ADDR | 0x40028EE0 | FULL | Master region, base address |
| PERI_MS_PPU_FX539_MS_SIZE | 0x40028EE4 | FULL | Master region, size |
| PERI_MS_PPU_FX539_MS_ATT0 | 0x40028EF0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX539_MS_ATT1 | 0x40028EF4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX539_MS_ATT2 | 0x40028EF8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX539_MS_ATT3 | 0x40028EFC | FULL | Master attributes 3 |

## 23.557 PPU_FX 540

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX540_SL_ADDR | 0x40028F00 | FULL | Slave region, base address |
| PERI_MS_PPU_FX540_SL_SIZE | 0x40028F04 | FULL | Slave region, size |
| PERI_MS_PPU_FX540_SL_ATT0 | 0x40028F10 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX540_SL_ATT1 | 0x40028F14 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX540_SL_ATT2 | 0x40028F18 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX540_SL_ATT3 | 0x40028F1C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX540_MS_ADDR | 0x40028F20 | FULL | Master region, base address |
| PERI_MS_PPU_FX540_MS_SIZE | 0x40028F24 | FULL | Master region, size |
| PERI_MS_PPU_FX540_MS_ATT0 | 0x40028F30 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX540_MS_ATT1 | 0x40028F34 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX540_MS_ATT2 | 0x40028F38 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX540_MS_ATT3 | 0x40028F3C | FULL | Master attributes 3 |

## 23.558 PPU_FX 541

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX541_SL_ADDR | 0x40028F40 | FULL | Slave region, base address |
| PERI_MS_PPU_FX541_SL_SIZE | 0x40028F44 | FULL | Slave region, size |
| PERI_MS_PPU_FX541_SL_ATT0 | 0x40028F50 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX541_SL_ATT1 | 0x40028F54 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX541_SL_ATT2 | 0x40028F58 | FULL | Slave attributes 2 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX541_SL_ATT3 | 0x40028F5C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX541_MS_ADDR | 0x40028F60 | FULL | Master region, base address |
| PERI_MS_PPU_FX541_MS_SIZE | 0x40028F64 | FULL | Master region, size |
| PERI_MS_PPU_FX541_MS_ATT0 | 0x40028F70 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX541_MS_ATT1 | 0x40028F74 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX541_MS_ATT2 | 0x40028F78 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX541_MS_ATT3 | 0x40028F7C | FULL | Master attributes 3 |

## 23.559 PPU_FX 542

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX542_SL_ADDR | 0x40028F80 | FULL | Slave region, base address |
| PERI_MS_PPU_FX542_SL_SIZE | 0x40028F84 | FULL | Slave region, size |
| PERI_MS_PPU_FX542_SL_ATT0 | 0x40028F90 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX542_SL_ATT1 | 0x40028F94 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX542_SL_ATT2 | 0x40028F98 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX542_SL_ATT3 | 0x40028F9C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX542_MS_ADDR | 0x40028FA0 | FULL | Master region, base address |
| PERI_MS_PPU_FX542_MS_SIZE | 0x40028FA4 | FULL | Master region, size |
| PERI_MS_PPU_FX542_MS_ATT0 | 0x40028FB0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX542_MS_ATT1 | 0x40028FB4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX542_MS_ATT2 | 0x40028FB8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX542_MS_ATT3 | 0x40028FBC | FULL | Master attributes 3 |

## 23.560 PPU_FX 543

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX543_SL_ADDR | 0x40028FC0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX543_SL_SIZE | 0x40028FC4 | FULL | Slave region, size |
| PERI_MS_PPU_FX543_SL_ATT0 | 0x40028FD0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX543_SL_ATT1 | 0x40028FD4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX543_SL_ATT2 | 0x40028FD8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX543_SL_ATT3 | 0x40028FDC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX543_MS_ADDR | 0x40028FE0 | FULL | Master region, base address |
| PERI_MS_PPU_FX543_MS_SIZE | 0x40028FE4 | FULL | Master region, size |
| PERI_MS_PPU_FX543_MS_ATT0 | 0x40028FF0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX543_MS_ATT1 | 0x40028FF4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX543_MS_ATT2 | 0x40028FF8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX543_MS_ATT3 | 0x40028FFC | FULL | Master attributes 3 |

## 23.561 PPU_FX 544

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX544_SL_ADDR | 0x40029000 | FULL | Slave region, base address |
| PERI_MS_PPU_FX544_SL_SIZE | 0x40029004 | FULL | Slave region, size |
| PERI_MS_PPU_FX544_SL_ATT0 | 0x40029010 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX544_SL_ATT1 | 0x40029014 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX544_SL_ATT2 | 0x40029018 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX544_SL_ATT3 | 0x4002901C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX544_MS_ADDR | 0x40029020 | FULL | Master region, base address |
| PERI_MS_PPU_FX544_MS_SIZE | 0x40029024 | FULL | Master region, size |
| PERI_MS_PPU_FX544_MS_ATT0 | 0x40029030 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX544_MS_ATT1 | 0x40029034 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX544_MS_ATT2 | 0x40029038 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX544_MS_ATT3 | 0x4002903C | FULL | Master attributes 3 |

## 23.562 PPU_FX 545

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX545_SL_ADDR | 0x40029040 | FULL | Slave region, base address |
| PERI_MS_PPU_FX545_SL_SIZE | 0x40029044 | FULL | Slave region, size |
| PERI_MS_PPU_FX545_SL_ATT0 | 0x40029050 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX545_SL_ATT1 | 0x40029054 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX545_SL_ATT2 | 0x40029058 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX545_SL_ATT3 | 0x4002905C | FULL | Slave attributes 3 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX545_MS_ADDR | 0x40029060 | FULL | Master region, base address |
| PERI_MS_PPU_FX545_MS_SIZE | 0x40029064 | FULL | Master region, size |
| PERI_MS_PPU_FX545_MS_ATT0 | 0x40029070 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX545_MS_ATT1 | 0x40029074 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX545_MS_ATT2 | 0x40029078 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX545_MS_ATT3 | 0x4002907C | FULL | Master attributes 3 |

## 23.563 PPU_FX 546

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX546_SL_ADDR | 0x40029080 | FULL | Slave region, base address |
| PERI_MS_PPU_FX546_SL_SIZE | 0x40029084 | FULL | Slave region, size |
| PERI_MS_PPU_FX546_SL_ATT0 | 0x40029090 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX546_SL_ATT1 | 0x40029094 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX546_SL_ATT2 | 0x40029098 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX546_SL_ATT3 | 0x4002909C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX546_MS_ADDR | 0x400290A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX546_MS_SIZE | 0x400290A4 | FULL | Master region, size |
| PERI_MS_PPU_FX546_MS_ATT0 | 0x400290B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX546_MS_ATT1 | 0x400290B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX546_MS_ATT2 | 0x400290B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX546_MS_ATT3 | 0x400290BC | FULL | Master attributes 3 |

## 23.564 PPU_FX 547

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX547_SL_ADDR | 0x400290C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX547_SL_SIZE | 0x400290C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX547_SL_ATT0 | 0x400290D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX547_SL_ATT1 | 0x400290D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX547_SL_ATT2 | 0x400290D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX547_SL_ATT3 | 0x400290DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX547_MS_ADDR | 0x400290E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX547_MS_SIZE | 0x400290E4 | FULL | Master region, size |
| PERI_MS_PPU_FX547_MS_ATT0 | 0x400290F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX547_MS_ATT1 | 0x400290F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX547_MS_ATT2 | 0x400290F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX547_MS_ATT3 | 0x400290FC | FULL | Master attributes 3 |

## 23.565 PPU_FX 548

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX548_SL_ADDR | 0x40029100 | FULL | Slave region, base address |
| PERI_MS_PPU_FX548_SL_SIZE | 0x40029104 | FULL | Slave region, size |
| PERI_MS_PPU_FX548_SL_ATT0 | 0x40029110 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX548_SL_ATT1 | 0x40029114 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX548_SL_ATT2 | 0x40029118 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX548_SL_ATT3 | 0x4002911C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX548_MS_ADDR | 0x40029120 | FULL | Master region, base address |
| PERI_MS_PPU_FX548_MS_SIZE | 0x40029124 | FULL | Master region, size |
| PERI_MS_PPU_FX548_MS_ATT0 | 0x40029130 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX548_MS_ATT1 | 0x40029134 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX548_MS_ATT2 | 0x40029138 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX548_MS_ATT3 | 0x4002913C | FULL | Master attributes 3 |

## 23.566 PPU_FX 549

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX549_SL_ADDR | 0x40029140 | FULL | Slave region, base address |
| PERI_MS_PPU_FX549_SL_SIZE | 0x40029144 | FULL | Slave region, size |
| PERI_MS_PPU_FX549_SL_ATT0 | 0x40029150 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX549_SL_ATT1 | 0x40029154 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX549_SL_ATT2 | 0x40029158 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX549_SL_ATT3 | 0x4002915C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX549_MS_ADDR | 0x40029160 | FULL | Master region, base address |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX549_MS_SIZE | 0x40029164 | FULL | Master region, size |
| PERI_MS_PPU_FX549_MS_ATT0 | 0x40029170 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX549_MS_ATT1 | 0x40029174 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX549_MS_ATT2 | 0x40029178 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX549_MS_ATT3 | 0x4002917C | FULL | Master attributes 3 |

## 23.567 PPU_FX 550

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX550_SL_ADDR | 0x40029180 | FULL | Slave region, base address |
| PERI_MS_PPU_FX550_SL_SIZE | 0x40029184 | FULL | Slave region, size |
| PERI_MS_PPU_FX550_SL_ATT0 | 0x40029190 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX550_SL_ATT1 | 0x40029194 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX550_SL_ATT2 | 0x40029198 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX550_SL_ATT3 | 0x4002919C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX550_MS_ADDR | 0x400291A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX550_MS_SIZE | 0x400291A4 | FULL | Master region, size |
| PERI_MS_PPU_FX550_MS_ATT0 | 0x400291B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX550_MS_ATT1 | 0x400291B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX550_MS_ATT2 | 0x400291B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX550_MS_ATT3 | 0x400291BC | FULL | Master attributes 3 |

## 23.568 PPU_FX 551

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX551_SL_ADDR | 0x400291C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX551_SL_SIZE | 0x400291C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX551_SL_ATT0 | 0x400291D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX551_SL_ATT1 | 0x400291D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX551_SL_ATT2 | 0x400291D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX551_SL_ATT3 | 0x400291DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX551_MS_ADDR | 0x400291E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX551_MS_SIZE | 0x400291E4 | FULL | Master region, size |
| PERI_MS_PPU_FX551_MS_ATT0 | 0x400291F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX551_MS_ATT1 | 0x400291F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX551_MS_ATT2 | 0x400291F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX551_MS_ATT3 | 0x400291FC | FULL | Master attributes 3 |

## 23.569 PPU_FX 552

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX552_SL_ADDR | 0x40029200 | FULL | Slave region, base address |
| PERI_MS_PPU_FX552_SL_SIZE | 0x40029204 | FULL | Slave region, size |
| PERI_MS_PPU_FX552_SL_ATT0 | 0x40029210 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX552_SL_ATT1 | 0x40029214 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX552_SL_ATT2 | 0x40029218 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX552_SL_ATT3 | 0x4002921C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX552_MS_ADDR | 0x40029220 | FULL | Master region, base address |
| PERI_MS_PPU_FX552_MS_SIZE | 0x40029224 | FULL | Master region, size |
| PERI_MS_PPU_FX552_MS_ATT0 | 0x40029230 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX552_MS_ATT1 | 0x40029234 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX552_MS_ATT2 | 0x40029238 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX552_MS_ATT3 | 0x4002923C | FULL | Master attributes 3 |

## 23.570 PPU_FX 553

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX553_SL_ADDR | 0x40029240 | FULL | Slave region, base address |
| PERI_MS_PPU_FX553_SL_SIZE | 0x40029244 | FULL | Slave region, size |
| PERI_MS_PPU_FX553_SL_ATT0 | 0x40029250 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX553_SL_ATT1 | 0x40029254 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX553_SL_ATT2 | 0x40029258 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX553_SL_ATT3 | 0x4002925C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX553_MS_ADDR | 0x40029260 | FULL | Master region, base address |
| PERI_MS_PPU_FX553_MS_SIZE | 0x40029264 | FULL | Master region, size |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX553_MS_ATT0 | 0x40029270 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX553_MS_ATT1 | 0x40029274 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX553_MS_ATT2 | 0x40029278 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX553_MS_ATT3 | 0x4002927C | FULL | Master attributes 3 |

## 23.571 PPU_FX 554

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX554_SL_ADDR | 0x40029280 | FULL | Slave region, base address |
| PERI_MS_PPU_FX554_SL_SIZE | 0x40029284 | FULL | Slave region, size |
| PERI_MS_PPU_FX554_SL_ATT0 | 0x40029290 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX554_SL_ATT1 | 0x40029294 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX554_SL_ATT2 | 0x40029298 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX554_SL_ATT3 | 0x4002929C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX554_MS_ADDR | 0x400292A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX554_MS_SIZE | 0x400292A4 | FULL | Master region, size |
| PERI_MS_PPU_FX554_MS_ATT0 | 0x400292B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX554_MS_ATT1 | 0x400292B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX554_MS_ATT2 | 0x400292B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX554_MS_ATT3 | 0x400292BC | FULL | Master attributes 3 |

## 23.572 PPU_FX 555

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX555_SL_ADDR | 0x400292C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX555_SL_SIZE | 0x400292C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX555_SL_ATT0 | 0x400292D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX555_SL_ATT1 | 0x400292D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX555_SL_ATT2 | 0x400292D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX555_SL_ATT3 | 0x400292DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX555_MS_ADDR | 0x400292E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX555_MS_SIZE | 0x400292E4 | FULL | Master region, size |
| PERI_MS_PPU_FX555_MS_ATT0 | 0x400292F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX555_MS_ATT1 | 0x400292F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX555_MS_ATT2 | 0x400292F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX555_MS_ATT3 | 0x400292FC | FULL | Master attributes 3 |

## 23.573 PPU_FX 556

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX556_SL_ADDR | 0x40029300 | FULL | Slave region, base address |
| PERI_MS_PPU_FX556_SL_SIZE | 0x40029304 | FULL | Slave region, size |
| PERI_MS_PPU_FX556_SL_ATT0 | 0x40029310 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX556_SL_ATT1 | 0x40029314 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX556_SL_ATT2 | 0x40029318 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX556_SL_ATT3 | 0x4002931C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX556_MS_ADDR | 0x40029320 | FULL | Master region, base address |
| PERI_MS_PPU_FX556_MS_SIZE | 0x40029324 | FULL | Master region, size |
| PERI_MS_PPU_FX556_MS_ATT0 | 0x40029330 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX556_MS_ATT1 | 0x40029334 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX556_MS_ATT2 | 0x40029338 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX556_MS_ATT3 | 0x4002933C | FULL | Master attributes 3 |

## 23.574 PPU_FX 557

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX557_SL_ADDR | 0x40029340 | FULL | Slave region, base address |
| PERI_MS_PPU_FX557_SL_SIZE | 0x40029344 | FULL | Slave region, size |
| PERI_MS_PPU_FX557_SL_ATT0 | 0x40029350 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX557_SL_ATT1 | 0x40029354 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX557_SL_ATT2 | 0x40029358 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX557_SL_ATT3 | 0x4002935C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX557_MS_ADDR | 0x40029360 | FULL | Master region, base address |
| PERI_MS_PPU_FX557_MS_SIZE | 0x40029364 | FULL | Master region, size |
| PERI_MS_PPU_FX557_MS_ATT0 | 0x40029370 | FULL | Master attributes 0 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX557_MS_ATT1 | 0x40029374 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX557_MS_ATT2 | 0x40029378 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX557_MS_ATT3 | 0x4002937C | FULL | Master attributes 3 |

## 23.575 PPU_FX 558

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX558_SL_ADDR | 0x40029380 | FULL | Slave region, base address |
| PERI_MS_PPU_FX558_SL_SIZE | 0x40029384 | FULL | Slave region, size |
| PERI_MS_PPU_FX558_SL_ATT0 | 0x40029390 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX558_SL_ATT1 | 0x40029394 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX558_SL_ATT2 | 0x40029398 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX558_SL_ATT3 | 0x4002939C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX558_MS_ADDR | 0x400293A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX558_MS_SIZE | 0x400293A4 | FULL | Master region, size |
| PERI_MS_PPU_FX558_MS_ATT0 | 0x400293B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX558_MS_ATT1 | 0x400293B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX558_MS_ATT2 | 0x400293B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX558_MS_ATT3 | 0x400293BC | FULL | Master attributes 3 |

## 23.576 PPU_FX 559

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX559_SL_ADDR | 0x400293C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX559_SL_SIZE | 0x400293C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX559_SL_ATT0 | 0x400293D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX559_SL_ATT1 | 0x400293D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX559_SL_ATT2 | 0x400293D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX559_SL_ATT3 | 0x400293DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX559_MS_ADDR | 0x400293E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX559_MS_SIZE | 0x400293E4 | FULL | Master region, size |
| PERI_MS_PPU_FX559_MS_ATT0 | 0x400293F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX559_MS_ATT1 | 0x400293F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX559_MS_ATT2 | 0x400293F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX559_MS_ATT3 | 0x400293FC | FULL | Master attributes 3 |

## 23.577 PPU_FX 560

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX560_SL_ADDR | 0x40029400 | FULL | Slave region, base address |
| PERI_MS_PPU_FX560_SL_SIZE | 0x40029404 | FULL | Slave region, size |
| PERI_MS_PPU_FX560_SL_ATT0 | 0x40029410 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX560_SL_ATT1 | 0x40029414 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX560_SL_ATT2 | 0x40029418 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX560_SL_ATT3 | 0x4002941C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX560_MS_ADDR | 0x40029420 | FULL | Master region, base address |
| PERI_MS_PPU_FX560_MS_SIZE | 0x40029424 | FULL | Master region, size |
| PERI_MS_PPU_FX560_MS_ATT0 | 0x40029430 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX560_MS_ATT1 | 0x40029434 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX560_MS_ATT2 | 0x40029438 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX560_MS_ATT3 | 0x4002943C | FULL | Master attributes 3 |

## 23.578 PPU_FX 561

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX561_SL_ADDR | 0x40029440 | FULL | Slave region, base address |
| PERI_MS_PPU_FX561_SL_SIZE | 0x40029444 | FULL | Slave region, size |
| PERI_MS_PPU_FX561_SL_ATT0 | 0x40029450 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX561_SL_ATT1 | 0x40029454 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX561_SL_ATT2 | 0x40029458 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX561_SL_ATT3 | 0x4002945C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX561_MS_ADDR | 0x40029460 | FULL | Master region, base address |
| PERI_MS_PPU_FX561_MS_SIZE | 0x40029464 | FULL | Master region, size |
| PERI_MS_PPU_FX561_MS_ATT0 | 0x40029470 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX561_MS_ATT1 | 0x40029474 | FULL | Master attributes 1 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX561_MS_ATT2 | 0x40029478 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX561_MS_ATT3 | 0x4002947C | FULL | Master attributes 3 |

## 23.579 PPU_FX 562

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX562_SL_ADDR | 0x40029480 | FULL | Slave region, base address |
| PERI_MS_PPU_FX562_SL_SIZE | 0x40029484 | FULL | Slave region, size |
| PERI_MS_PPU_FX562_SL_ATT0 | 0x40029490 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX562_SL_ATT1 | 0x40029494 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX562_SL_ATT2 | 0x40029498 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX562_SL_ATT3 | 0x4002949C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX562_MS_ADDR | 0x400294A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX562_MS_SIZE | 0x400294A4 | FULL | Master region, size |
| PERI_MS_PPU_FX562_MS_ATT0 | 0x400294B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX562_MS_ATT1 | 0x400294B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX562_MS_ATT2 | 0x400294B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX562_MS_ATT3 | 0x400294BC | FULL | Master attributes 3 |

## 23.580 PPU_FX 563

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX563_SL_ADDR | 0x400294C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX563_SL_SIZE | 0x400294C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX563_SL_ATT0 | 0x400294D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX563_SL_ATT1 | 0x400294D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX563_SL_ATT2 | 0x400294D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX563_SL_ATT3 | 0x400294DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX563_MS_ADDR | 0x400294E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX563_MS_SIZE | 0x400294E4 | FULL | Master region, size |
| PERI_MS_PPU_FX563_MS_ATT0 | 0x400294F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX563_MS_ATT1 | 0x400294F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX563_MS_ATT2 | 0x400294F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX563_MS_ATT3 | 0x400294FC | FULL | Master attributes 3 |

## 23.581 PPU_FX 564

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX564_SL_ADDR | 0x40029500 | FULL | Slave region, base address |
| PERI_MS_PPU_FX564_SL_SIZE | 0x40029504 | FULL | Slave region, size |
| PERI_MS_PPU_FX564_SL_ATT0 | 0x40029510 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX564_SL_ATT1 | 0x40029514 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX564_SL_ATT2 | 0x40029518 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX564_SL_ATT3 | 0x4002951C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX564_MS_ADDR | 0x40029520 | FULL | Master region, base address |
| PERI_MS_PPU_FX564_MS_SIZE | 0x40029524 | FULL | Master region, size |
| PERI_MS_PPU_FX564_MS_ATT0 | 0x40029530 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX564_MS_ATT1 | 0x40029534 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX564_MS_ATT2 | 0x40029538 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX564_MS_ATT3 | 0x4002953C | FULL | Master attributes 3 |

## 23.582 PPU_FX 565

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX565_SL_ADDR | 0x40029540 | FULL | Slave region, base address |
| PERI_MS_PPU_FX565_SL_SIZE | 0x40029544 | FULL | Slave region, size |
| PERI_MS_PPU_FX565_SL_ATT0 | 0x40029550 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX565_SL_ATT1 | 0x40029554 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX565_SL_ATT2 | 0x40029558 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX565_SL_ATT3 | 0x4002955C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX565_MS_ADDR | 0x40029560 | FULL | Master region, base address |
| PERI_MS_PPU_FX565_MS_SIZE | 0x40029564 | FULL | Master region, size |
| PERI_MS_PPU_FX565_MS_ATT0 | 0x40029570 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX565_MS_ATT1 | 0x40029574 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX565_MS_ATT2 | 0x40029578 | FULL | Master attributes 2 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX565_MS_ATT3 | 0x4002957C | FULL | Master attributes 3 |

## 23.583 PPU_FX 566

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX566_SL_ADDR | 0x40029580 | FULL | Slave region, base address |
| PERI_MS_PPU_FX566_SL_SIZE | 0x40029584 | FULL | Slave region, size |
| PERI_MS_PPU_FX566_SL_ATT0 | 0x40029590 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX566_SL_ATT1 | 0x40029594 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX566_SL_ATT2 | 0x40029598 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX566_SL_ATT3 | 0x4002959C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX566_MS_ADDR | 0x400295A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX566_MS_SIZE | 0x400295A4 | FULL | Master region, size |
| PERI_MS_PPU_FX566_MS_ATT0 | 0x400295B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX566_MS_ATT1 | 0x400295B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX566_MS_ATT2 | 0x400295B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX566_MS_ATT3 | 0x400295BC | FULL | Master attributes 3 |

## 23.584 PPU_FX 567

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX567_SL_ADDR | 0x400295C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX567_SL_SIZE | 0x400295C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX567_SL_ATT0 | 0x400295D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX567_SL_ATT1 | 0x400295D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX567_SL_ATT2 | 0x400295D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX567_SL_ATT3 | 0x400295DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX567_MS_ADDR | 0x400295E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX567_MS_SIZE | 0x400295E4 | FULL | Master region, size |
| PERI_MS_PPU_FX567_MS_ATT0 | 0x400295F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX567_MS_ATT1 | 0x400295F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX567_MS_ATT2 | 0x400295F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX567_MS_ATT3 | 0x400295FC | FULL | Master attributes 3 |

## 23.585 PPU_FX 568

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX568_SL_ADDR | 0x40029600 | FULL | Slave region, base address |
| PERI_MS_PPU_FX568_SL_SIZE | 0x40029604 | FULL | Slave region, size |
| PERI_MS_PPU_FX568_SL_ATT0 | 0x40029610 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX568_SL_ATT1 | 0x40029614 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX568_SL_ATT2 | 0x40029618 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX568_SL_ATT3 | 0x4002961C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX568_MS_ADDR | 0x40029620 | FULL | Master region, base address |
| PERI_MS_PPU_FX568_MS_SIZE | 0x40029624 | FULL | Master region, size |
| PERI_MS_PPU_FX568_MS_ATT0 | 0x40029630 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX568_MS_ATT1 | 0x40029634 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX568_MS_ATT2 | 0x40029638 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX568_MS_ATT3 | 0x4002963C | FULL | Master attributes 3 |

## 23.586 PPU_FX 569

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX569_SL_ADDR | 0x40029640 | FULL | Slave region, base address |
| PERI_MS_PPU_FX569_SL_SIZE | 0x40029644 | FULL | Slave region, size |
| PERI_MS_PPU_FX569_SL_ATT0 | 0x40029650 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX569_SL_ATT1 | 0x40029654 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX569_SL_ATT2 | 0x40029658 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX569_SL_ATT3 | 0x4002965C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX569_MS_ADDR | 0x40029660 | FULL | Master region, base address |
| PERI_MS_PPU_FX569_MS_SIZE | 0x40029664 | FULL | Master region, size |
| PERI_MS_PPU_FX569_MS_ATT0 | 0x40029670 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX569_MS_ATT1 | 0x40029674 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX569_MS_ATT2 | 0x40029678 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX569_MS_ATT3 | 0x4002967C | FULL | Master attributes 3 |

## 23.587 PPU_FX 570

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX570_SL_ADDR | 0x40029680 | FULL | Slave region, base address |
| PERI_MS_PPU_FX570_SL_SIZE | 0x40029684 | FULL | Slave region, size |
| PERI_MS_PPU_FX570_SL_ATT0 | 0x40029690 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX570_SL_ATT1 | 0x40029694 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX570_SL_ATT2 | 0x40029698 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX570_SL_ATT3 | 0x4002969C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX570_MS_ADDR | 0x400296A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX570_MS_SIZE | 0x400296A4 | FULL | Master region, size |
| PERI_MS_PPU_FX570_MS_ATT0 | 0x400296B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX570_MS_ATT1 | 0x400296B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX570_MS_ATT2 | 0x400296B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX570_MS_ATT3 | 0x400296BC | FULL | Master attributes 3 |

## 23.588 PPU_FX 571

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX571_SL_ADDR | 0x400296C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX571_SL_SIZE | 0x400296C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX571_SL_ATT0 | 0x400296D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX571_SL_ATT1 | 0x400296D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX571_SL_ATT2 | 0x400296D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX571_SL_ATT3 | 0x400296DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX571_MS_ADDR | 0x400296E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX571_MS_SIZE | 0x400296E4 | FULL | Master region, size |
| PERI_MS_PPU_FX571_MS_ATT0 | 0x400296F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX571_MS_ATT1 | 0x400296F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX571_MS_ATT2 | 0x400296F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX571_MS_ATT3 | 0x400296FC | FULL | Master attributes 3 |

## 23.589 PPU_FX 572

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX572_SL_ADDR | 0x40029700 | FULL | Slave region, base address |
| PERI_MS_PPU_FX572_SL_SIZE | 0x40029704 | FULL | Slave region, size |
| PERI_MS_PPU_FX572_SL_ATT0 | 0x40029710 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX572_SL_ATT1 | 0x40029714 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX572_SL_ATT2 | 0x40029718 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX572_SL_ATT3 | 0x4002971C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX572_MS_ADDR | 0x40029720 | FULL | Master region, base address |
| PERI_MS_PPU_FX572_MS_SIZE | 0x40029724 | FULL | Master region, size |
| PERI_MS_PPU_FX572_MS_ATT0 | 0x40029730 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX572_MS_ATT1 | 0x40029734 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX572_MS_ATT2 | 0x40029738 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX572_MS_ATT3 | 0x4002973C | FULL | Master attributes 3 |

## 23.590 PPU_FX 573

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX573_SL_ADDR | 0x40029740 | FULL | Slave region, base address |
| PERI_MS_PPU_FX573_SL_SIZE | 0x40029744 | FULL | Slave region, size |
| PERI_MS_PPU_FX573_SL_ATT0 | 0x40029750 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX573_SL_ATT1 | 0x40029754 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX573_SL_ATT2 | 0x40029758 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX573_SL_ATT3 | 0x4002975C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX573_MS_ADDR | 0x40029760 | FULL | Master region, base address |
| PERI_MS_PPU_FX573_MS_SIZE | 0x40029764 | FULL | Master region, size |
| PERI_MS_PPU_FX573_MS_ATT0 | 0x40029770 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX573_MS_ATT1 | 0x40029774 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX573_MS_ATT2 | 0x40029778 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX573_MS_ATT3 | 0x4002977C | FULL | Master attributes 3 |

## 23.591 PPU_FX 574

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX574_SL_ADDR | 0x40029780 | FULL | Slave region, base address |
| PERI_MS_PPU_FX574_SL_SIZE | 0x40029784 | FULL | Slave region, size |
| PERI_MS_PPU_FX574_SL_ATT0 | 0x40029790 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX574_SL_ATT1 | 0x40029794 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX574_SL_ATT2 | 0x40029798 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX574_SL_ATT3 | 0x4002979C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX574_MS_ADDR | 0x400297A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX574_MS_SIZE | 0x400297A4 | FULL | Master region, size |
| PERI_MS_PPU_FX574_MS_ATT0 | 0x400297B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX574_MS_ATT1 | 0x400297B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX574_MS_ATT2 | 0x400297B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX574_MS_ATT3 | 0x400297BC | FULL | Master attributes 3 |

## 23.592 PPU_FX 575

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX575_SL_ADDR | 0x400297C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX575_SL_SIZE | 0x400297C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX575_SL_ATT0 | 0x400297D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX575_SL_ATT1 | 0x400297D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX575_SL_ATT2 | 0x400297D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX575_SL_ATT3 | 0x400297DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX575_MS_ADDR | 0x400297E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX575_MS_SIZE | 0x400297E4 | FULL | Master region, size |
| PERI_MS_PPU_FX575_MS_ATT0 | 0x400297F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX575_MS_ATT1 | 0x400297F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX575_MS_ATT2 | 0x400297F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX575_MS_ATT3 | 0x400297FC | FULL | Master attributes 3 |

## 23.593 PPU_FX 576

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX576_SL_ADDR | 0x40029800 | FULL | Slave region, base address |
| PERI_MS_PPU_FX576_SL_SIZE | 0x40029804 | FULL | Slave region, size |
| PERI_MS_PPU_FX576_SL_ATT0 | 0x40029810 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX576_SL_ATT1 | 0x40029814 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX576_SL_ATT2 | 0x40029818 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX576_SL_ATT3 | 0x4002981C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX576_MS_ADDR | 0x40029820 | FULL | Master region, base address |
| PERI_MS_PPU_FX576_MS_SIZE | 0x40029824 | FULL | Master region, size |
| PERI_MS_PPU_FX576_MS_ATT0 | 0x40029830 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX576_MS_ATT1 | 0x40029834 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX576_MS_ATT2 | 0x40029838 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX576_MS_ATT3 | 0x4002983C | FULL | Master attributes 3 |

## 23.594 PPU_FX 577

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX577_SL_ADDR | 0x40029840 | FULL | Slave region, base address |
| PERI_MS_PPU_FX577_SL_SIZE | 0x40029844 | FULL | Slave region, size |
| PERI_MS_PPU_FX577_SL_ATT0 | 0x40029850 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX577_SL_ATT1 | 0x40029854 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX577_SL_ATT2 | 0x40029858 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX577_SL_ATT3 | 0x4002985C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX577_MS_ADDR | 0x40029860 | FULL | Master region, base address |
| PERI_MS_PPU_FX577_MS_SIZE | 0x40029864 | FULL | Master region, size |
| PERI_MS_PPU_FX577_MS_ATT0 | 0x40029870 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX577_MS_ATT1 | 0x40029874 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX577_MS_ATT2 | 0x40029878 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX577_MS_ATT3 | 0x4002987C | FULL | Master attributes 3 |

## 23.595 PPU_FX 578

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX578_SL_ADDR | 0x40029880 | FULL | Slave region, base address |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX578_SL_SIZE | 0x40029884 | FULL | Slave region, size |
| PERI_MS_PPU_FX578_SL_ATT0 | 0x40029890 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX578_SL_ATT1 | 0x40029894 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX578_SL_ATT2 | 0x40029898 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX578_SL_ATT3 | 0x4002989C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX578_MS_ADDR | 0x400298A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX578_MS_SIZE | 0x400298A4 | FULL | Master region, size |
| PERI_MS_PPU_FX578_MS_ATT0 | 0x400298B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX578_MS_ATT1 | 0x400298B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX578_MS_ATT2 | 0x400298B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX578_MS_ATT3 | 0x400298BC | FULL | Master attributes 3 |

## 23.596 PPU_FX 579

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX579_SL_ADDR | 0x400298C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX579_SL_SIZE | 0x400298C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX579_SL_ATT0 | 0x400298D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX579_SL_ATT1 | 0x400298D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX579_SL_ATT2 | 0x400298D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX579_SL_ATT3 | 0x400298DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX579_MS_ADDR | 0x400298E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX579_MS_SIZE | 0x400298E4 | FULL | Master region, size |
| PERI_MS_PPU_FX579_MS_ATT0 | 0x400298F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX579_MS_ATT1 | 0x400298F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX579_MS_ATT2 | 0x400298F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX579_MS_ATT3 | 0x400298FC | FULL | Master attributes 3 |

## 23.597 PPU_FX 580

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX580_SL_ADDR | 0x40029900 | FULL | Slave region, base address |
| PERI_MS_PPU_FX580_SL_SIZE | 0x40029904 | FULL | Slave region, size |
| PERI_MS_PPU_FX580_SL_ATT0 | 0x40029910 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX580_SL_ATT1 | 0x40029914 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX580_SL_ATT2 | 0x40029918 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX580_SL_ATT3 | 0x4002991C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX580_MS_ADDR | 0x40029920 | FULL | Master region, base address |
| PERI_MS_PPU_FX580_MS_SIZE | 0x40029924 | FULL | Master region, size |
| PERI_MS_PPU_FX580_MS_ATT0 | 0x40029930 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX580_MS_ATT1 | 0x40029934 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX580_MS_ATT2 | 0x40029938 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX580_MS_ATT3 | 0x4002993C | FULL | Master attributes 3 |

## 23.598 PPU_FX 581

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX581_SL_ADDR | 0x40029940 | FULL | Slave region, base address |
| PERI_MS_PPU_FX581_SL_SIZE | 0x40029944 | FULL | Slave region, size |
| PERI_MS_PPU_FX581_SL_ATT0 | 0x40029950 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX581_SL_ATT1 | 0x40029954 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX581_SL_ATT2 | 0x40029958 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX581_SL_ATT3 | 0x4002995C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX581_MS_ADDR | 0x40029960 | FULL | Master region, base address |
| PERI_MS_PPU_FX581_MS_SIZE | 0x40029964 | FULL | Master region, size |
| PERI_MS_PPU_FX581_MS_ATT0 | 0x40029970 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX581_MS_ATT1 | 0x40029974 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX581_MS_ATT2 | 0x40029978 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX581_MS_ATT3 | 0x4002997C | FULL | Master attributes 3 |

## 23.599 PPU_FX 582

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX582_SL_ADDR | 0x40029980 | FULL | Slave region, base address |
| PERI_MS_PPU_FX582_SL_SIZE | 0x40029984 | FULL | Slave region, size |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX582_SL_ATT0 | 0x40029990 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX582_SL_ATT1 | 0x40029994 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX582_SL_ATT2 | 0x40029998 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX582_SL_ATT3 | 0x4002999C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX582_MS_ADDR | 0x400299A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX582_MS_SIZE | 0x400299A4 | FULL | Master region, size |
| PERI_MS_PPU_FX582_MS_ATT0 | 0x400299B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX582_MS_ATT1 | 0x400299B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX582_MS_ATT2 | 0x400299B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX582_MS_ATT3 | 0x400299BC | FULL | Master attributes 3 |

## 23.600 PPU_FX 583

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX583_SL_ADDR | 0x400299C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX583_SL_SIZE | 0x400299C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX583_SL_ATT0 | 0x400299D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX583_SL_ATT1 | 0x400299D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX583_SL_ATT2 | 0x400299D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX583_SL_ATT3 | 0x400299DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX583_MS_ADDR | 0x400299E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX583_MS_SIZE | 0x400299E4 | FULL | Master region, size |
| PERI_MS_PPU_FX583_MS_ATT0 | 0x400299F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX583_MS_ATT1 | 0x400299F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX583_MS_ATT2 | 0x400299F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX583_MS_ATT3 | 0x400299FC | FULL | Master attributes 3 |

## 23.601 PPU_FX 584

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX584_SL_ADDR | 0x40029A00 | FULL | Slave region, base address |
| PERI_MS_PPU_FX584_SL_SIZE | 0x40029A04 | FULL | Slave region, size |
| PERI_MS_PPU_FX584_SL_ATT0 | 0x40029A10 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX584_SL_ATT1 | 0x40029A14 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX584_SL_ATT2 | 0x40029A18 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX584_SL_ATT3 | 0x40029A1C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX584_MS_ADDR | 0x40029A20 | FULL | Master region, base address |
| PERI_MS_PPU_FX584_MS_SIZE | 0x40029A24 | FULL | Master region, size |
| PERI_MS_PPU_FX584_MS_ATT0 | 0x40029A30 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX584_MS_ATT1 | 0x40029A34 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX584_MS_ATT2 | 0x40029A38 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX584_MS_ATT3 | 0x40029A3C | FULL | Master attributes 3 |

## 23.602 PPU_FX 585

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX585_SL_ADDR | 0x40029A40 | FULL | Slave region, base address |
| PERI_MS_PPU_FX585_SL_SIZE | 0x40029A44 | FULL | Slave region, size |
| PERI_MS_PPU_FX585_SL_ATT0 | 0x40029A50 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX585_SL_ATT1 | 0x40029A54 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX585_SL_ATT2 | 0x40029A58 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX585_SL_ATT3 | 0x40029A5C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX585_MS_ADDR | 0x40029A60 | FULL | Master region, base address |
| PERI_MS_PPU_FX585_MS_SIZE | 0x40029A64 | FULL | Master region, size |
| PERI_MS_PPU_FX585_MS_ATT0 | 0x40029A70 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX585_MS_ATT1 | 0x40029A74 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX585_MS_ATT2 | 0x40029A78 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX585_MS_ATT3 | 0x40029A7C | FULL | Master attributes 3 |

## 23.603 PPU_FX 586

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX586_SL_ADDR | 0x40029A80 | FULL | Slave region, base address |
| PERI_MS_PPU_FX586_SL_SIZE | 0x40029A84 | FULL | Slave region, size |
| PERI_MS_PPU_FX586_SL_ATT0 | 0x40029A90 | FULL | Slave attributes 0 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX586_SL_ATT1 | 0x40029A94 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX586_SL_ATT2 | 0x40029A98 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX586_SL_ATT3 | 0x40029A9C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX586_MS_ADDR | 0x40029AA0 | FULL | Master region, base address |
| PERI_MS_PPU_FX586_MS_SIZE | 0x40029AA4 | FULL | Master region, size |
| PERI_MS_PPU_FX586_MS_ATT0 | 0x40029AB0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX586_MS_ATT1 | 0x40029AB4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX586_MS_ATT2 | 0x40029AB8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX586_MS_ATT3 | 0x40029ABC | FULL | Master attributes 3 |

## 23.604 PPU_FX 587

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX587_SL_ADDR | 0x40029AC0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX587_SL_SIZE | 0x40029AC4 | FULL | Slave region, size |
| PERI_MS_PPU_FX587_SL_ATT0 | 0x40029AD0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX587_SL_ATT1 | 0x40029AD4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX587_SL_ATT2 | 0x40029AD8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX587_SL_ATT3 | 0x40029ADC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX587_MS_ADDR | 0x40029AE0 | FULL | Master region, base address |
| PERI_MS_PPU_FX587_MS_SIZE | 0x40029AE4 | FULL | Master region, size |
| PERI_MS_PPU_FX587_MS_ATT0 | 0x40029AF0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX587_MS_ATT1 | 0x40029AF4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX587_MS_ATT2 | 0x40029AF8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX587_MS_ATT3 | 0x40029AFC | FULL | Master attributes 3 |

## 23.605 PPU_FX 588

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX588_SL_ADDR | 0x40029B00 | FULL | Slave region, base address |
| PERI_MS_PPU_FX588_SL_SIZE | 0x40029B04 | FULL | Slave region, size |
| PERI_MS_PPU_FX588_SL_ATT0 | 0x40029B10 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX588_SL_ATT1 | 0x40029B14 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX588_SL_ATT2 | 0x40029B18 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX588_SL_ATT3 | 0x40029B1C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX588_MS_ADDR | 0x40029B20 | FULL | Master region, base address |
| PERI_MS_PPU_FX588_MS_SIZE | 0x40029B24 | FULL | Master region, size |
| PERI_MS_PPU_FX588_MS_ATT0 | 0x40029B30 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX588_MS_ATT1 | 0x40029B34 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX588_MS_ATT2 | 0x40029B38 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX588_MS_ATT3 | 0x40029B3C | FULL | Master attributes 3 |

## 23.606 PPU_FX 589

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX589_SL_ADDR | 0x40029B40 | FULL | Slave region, base address |
| PERI_MS_PPU_FX589_SL_SIZE | 0x40029B44 | FULL | Slave region, size |
| PERI_MS_PPU_FX589_SL_ATT0 | 0x40029B50 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX589_SL_ATT1 | 0x40029B54 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX589_SL_ATT2 | 0x40029B58 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX589_SL_ATT3 | 0x40029B5C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX589_MS_ADDR | 0x40029B60 | FULL | Master region, base address |
| PERI_MS_PPU_FX589_MS_SIZE | 0x40029B64 | FULL | Master region, size |
| PERI_MS_PPU_FX589_MS_ATT0 | 0x40029B70 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX589_MS_ATT1 | 0x40029B74 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX589_MS_ATT2 | 0x40029B78 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX589_MS_ATT3 | 0x40029B7C | FULL | Master attributes 3 |

## 23.607 PPU_FX 590

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX590_SL_ADDR | 0x40029B80 | FULL | Slave region, base address |
| PERI_MS_PPU_FX590_SL_SIZE | 0x40029B84 | FULL | Slave region, size |
| PERI_MS_PPU_FX590_SL_ATT0 | 0x40029B90 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX590_SL_ATT1 | 0x40029B94 | FULL | Slave attributes 1 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX590_SL_ATT2 | 0x40029B98 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX590_SL_ATT3 | 0x40029B9C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX590_MS_ADDR | 0x40029BA0 | FULL | Master region, base address |
| PERI_MS_PPU_FX590_MS_SIZE | 0x40029BA4 | FULL | Master region, size |
| PERI_MS_PPU_FX590_MS_ATT0 | 0x40029BB0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX590_MS_ATT1 | 0x40029BB4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX590_MS_ATT2 | 0x40029BB8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX590_MS_ATT3 | 0x40029BBC | FULL | Master attributes 3 |

## 23.608 PPU_FX 591

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX591_SL_ADDR | 0x40029BC0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX591_SL_SIZE | 0x40029BC4 | FULL | Slave region, size |
| PERI_MS_PPU_FX591_SL_ATT0 | 0x40029BD0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX591_SL_ATT1 | 0x40029BD4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX591_SL_ATT2 | 0x40029BD8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX591_SL_ATT3 | 0x40029BDC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX591_MS_ADDR | 0x40029BE0 | FULL | Master region, base address |
| PERI_MS_PPU_FX591_MS_SIZE | 0x40029BE4 | FULL | Master region, size |
| PERI_MS_PPU_FX591_MS_ATT0 | 0x40029BF0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX591_MS_ATT1 | 0x40029BF4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX591_MS_ATT2 | 0x40029BF8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX591_MS_ATT3 | 0x40029BFC | FULL | Master attributes 3 |

## 23.609 PPU_FX 592

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX592_SL_ADDR | 0x40029C00 | FULL | Slave region, base address |
| PERI_MS_PPU_FX592_SL_SIZE | 0x40029C04 | FULL | Slave region, size |
| PERI_MS_PPU_FX592_SL_ATT0 | 0x40029C10 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX592_SL_ATT1 | 0x40029C14 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX592_SL_ATT2 | 0x40029C18 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX592_SL_ATT3 | 0x40029C1C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX592_MS_ADDR | 0x40029C20 | FULL | Master region, base address |
| PERI_MS_PPU_FX592_MS_SIZE | 0x40029C24 | FULL | Master region, size |
| PERI_MS_PPU_FX592_MS_ATT0 | 0x40029C30 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX592_MS_ATT1 | 0x40029C34 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX592_MS_ATT2 | 0x40029C38 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX592_MS_ATT3 | 0x40029C3C | FULL | Master attributes 3 |

## 23.610 PPU_FX 593

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX593_SL_ADDR | 0x40029C40 | FULL | Slave region, base address |
| PERI_MS_PPU_FX593_SL_SIZE | 0x40029C44 | FULL | Slave region, size |
| PERI_MS_PPU_FX593_SL_ATT0 | 0x40029C50 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX593_SL_ATT1 | 0x40029C54 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX593_SL_ATT2 | 0x40029C58 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX593_SL_ATT3 | 0x40029C5C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX593_MS_ADDR | 0x40029C60 | FULL | Master region, base address |
| PERI_MS_PPU_FX593_MS_SIZE | 0x40029C64 | FULL | Master region, size |
| PERI_MS_PPU_FX593_MS_ATT0 | 0x40029C70 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX593_MS_ATT1 | 0x40029C74 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX593_MS_ATT2 | 0x40029C78 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX593_MS_ATT3 | 0x40029C7C | FULL | Master attributes 3 |

## 23.611 PPU_FX 594

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX594_SL_ADDR | 0x40029C80 | FULL | Slave region, base address |
| PERI_MS_PPU_FX594_SL_SIZE | 0x40029C84 | FULL | Slave region, size |
| PERI_MS_PPU_FX594_SL_ATT0 | 0x40029C90 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX594_SL_ATT1 | 0x40029C94 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX594_SL_ATT2 | 0x40029C98 | FULL | Slave attributes 2 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX594_SL_ATT3 | 0x40029C9C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX594_MS_ADDR | 0x40029CA0 | FULL | Master region, base address |
| PERI_MS_PPU_FX594_MS_SIZE | 0x40029CA4 | FULL | Master region, size |
| PERI_MS_PPU_FX594_MS_ATT0 | 0x40029CB0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX594_MS_ATT1 | 0x40029CB4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX594_MS_ATT2 | 0x40029CB8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX594_MS_ATT3 | 0x40029CBC | FULL | Master attributes 3 |

## 23.612 PPU_FX 595

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX595_SL_ADDR | 0x40029CC0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX595_SL_SIZE | 0x40029CC4 | FULL | Slave region, size |
| PERI_MS_PPU_FX595_SL_ATT0 | 0x40029CD0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX595_SL_ATT1 | 0x40029CD4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX595_SL_ATT2 | 0x40029CD8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX595_SL_ATT3 | 0x40029CDC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX595_MS_ADDR | 0x40029CE0 | FULL | Master region, base address |
| PERI_MS_PPU_FX595_MS_SIZE | 0x40029CE4 | FULL | Master region, size |
| PERI_MS_PPU_FX595_MS_ATT0 | 0x40029CF0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX595_MS_ATT1 | 0x40029CF4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX595_MS_ATT2 | 0x40029CF8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX595_MS_ATT3 | 0x40029CFC | FULL | Master attributes 3 |

## 23.613 PPU_FX 596

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX596_SL_ADDR | 0x40029D00 | FULL | Slave region, base address |
| PERI_MS_PPU_FX596_SL_SIZE | 0x40029D04 | FULL | Slave region, size |
| PERI_MS_PPU_FX596_SL_ATT0 | 0x40029D10 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX596_SL_ATT1 | 0x40029D14 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX596_SL_ATT2 | 0x40029D18 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX596_SL_ATT3 | 0x40029D1C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX596_MS_ADDR | 0x40029D20 | FULL | Master region, base address |
| PERI_MS_PPU_FX596_MS_SIZE | 0x40029D24 | FULL | Master region, size |
| PERI_MS_PPU_FX596_MS_ATT0 | 0x40029D30 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX596_MS_ATT1 | 0x40029D34 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX596_MS_ATT2 | 0x40029D38 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX596_MS_ATT3 | 0x40029D3C | FULL | Master attributes 3 |

## 23.614 PPU_FX 597

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX597_SL_ADDR | 0x40029D40 | FULL | Slave region, base address |
| PERI_MS_PPU_FX597_SL_SIZE | 0x40029D44 | FULL | Slave region, size |
| PERI_MS_PPU_FX597_SL_ATT0 | 0x40029D50 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX597_SL_ATT1 | 0x40029D54 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX597_SL_ATT2 | 0x40029D58 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX597_SL_ATT3 | 0x40029D5C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX597_MS_ADDR | 0x40029D60 | FULL | Master region, base address |
| PERI_MS_PPU_FX597_MS_SIZE | 0x40029D64 | FULL | Master region, size |
| PERI_MS_PPU_FX597_MS_ATT0 | 0x40029D70 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX597_MS_ATT1 | 0x40029D74 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX597_MS_ATT2 | 0x40029D78 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX597_MS_ATT3 | 0x40029D7C | FULL | Master attributes 3 |

## 23.615 PPU_FX 598

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX598_SL_ADDR | 0x40029D80 | FULL | Slave region, base address |
| PERI_MS_PPU_FX598_SL_SIZE | 0x40029D84 | FULL | Slave region, size |
| PERI_MS_PPU_FX598_SL_ATT0 | 0x40029D90 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX598_SL_ATT1 | 0x40029D94 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX598_SL_ATT2 | 0x40029D98 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX598_SL_ATT3 | 0x40029D9C | FULL | Slave attributes 3 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX598_MS_ADDR | 0x40029DA0 | FULL | Master region, base address |
| PERI_MS_PPU_FX598_MS_SIZE | 0x40029DA4 | FULL | Master region, size |
| PERI_MS_PPU_FX598_MS_ATT0 | 0x40029DB0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX598_MS_ATT1 | 0x40029DB4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX598_MS_ATT2 | 0x40029DB8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX598_MS_ATT3 | 0x40029DBC | FULL | Master attributes 3 |

## 23.616 PPU_FX 599

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX599_SL_ADDR | 0x40029DC0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX599_SL_SIZE | 0x40029DC4 | FULL | Slave region, size |
| PERI_MS_PPU_FX599_SL_ATT0 | 0x40029DD0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX599_SL_ATT1 | 0x40029DD4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX599_SL_ATT2 | 0x40029DD8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX599_SL_ATT3 | 0x40029DDC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX599_MS_ADDR | 0x40029DE0 | FULL | Master region, base address |
| PERI_MS_PPU_FX599_MS_SIZE | 0x40029DE4 | FULL | Master region, size |
| PERI_MS_PPU_FX599_MS_ATT0 | 0x40029DF0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX599_MS_ATT1 | 0x40029DF4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX599_MS_ATT2 | 0x40029DF8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX599_MS_ATT3 | 0x40029DFC | FULL | Master attributes 3 |

## 23.617 PPU_FX 600

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX600_SL_ADDR | 0x40029E00 | FULL | Slave region, base address |
| PERI_MS_PPU_FX600_SL_SIZE | 0x40029E04 | FULL | Slave region, size |
| PERI_MS_PPU_FX600_SL_ATT0 | 0x40029E10 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX600_SL_ATT1 | 0x40029E14 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX600_SL_ATT2 | 0x40029E18 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX600_SL_ATT3 | 0x40029E1C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX600_MS_ADDR | 0x40029E20 | FULL | Master region, base address |
| PERI_MS_PPU_FX600_MS_SIZE | 0x40029E24 | FULL | Master region, size |
| PERI_MS_PPU_FX600_MS_ATT0 | 0x40029E30 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX600_MS_ATT1 | 0x40029E34 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX600_MS_ATT2 | 0x40029E38 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX600_MS_ATT3 | 0x40029E3C | FULL | Master attributes 3 |

## 23.618 PPU_FX 601

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX601_SL_ADDR | 0x40029E40 | FULL | Slave region, base address |
| PERI_MS_PPU_FX601_SL_SIZE | 0x40029E44 | FULL | Slave region, size |
| PERI_MS_PPU_FX601_SL_ATT0 | 0x40029E50 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX601_SL_ATT1 | 0x40029E54 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX601_SL_ATT2 | 0x40029E58 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX601_SL_ATT3 | 0x40029E5C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX601_MS_ADDR | 0x40029E60 | FULL | Master region, base address |
| PERI_MS_PPU_FX601_MS_SIZE | 0x40029E64 | FULL | Master region, size |
| PERI_MS_PPU_FX601_MS_ATT0 | 0x40029E70 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX601_MS_ATT1 | 0x40029E74 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX601_MS_ATT2 | 0x40029E78 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX601_MS_ATT3 | 0x40029E7C | FULL | Master attributes 3 |

## 23.619 PPU_FX 602

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX602_SL_ADDR | 0x40029E80 | FULL | Slave region, base address |
| PERI_MS_PPU_FX602_SL_SIZE | 0x40029E84 | FULL | Slave region, size |
| PERI_MS_PPU_FX602_SL_ATT0 | 0x40029E90 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX602_SL_ATT1 | 0x40029E94 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX602_SL_ATT2 | 0x40029E98 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX602_SL_ATT3 | 0x40029E9C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX602_MS_ADDR | 0x40029EA0 | FULL | Master region, base address |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX602_MS_SIZE | 0x40029EA4 | FULL | Master region, size |
| PERI_MS_PPU_FX602_MS_ATT0 | 0x40029EB0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX602_MS_ATT1 | 0x40029EB4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX602_MS_ATT2 | 0x40029EB8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX602_MS_ATT3 | 0x40029EBC | FULL | Master attributes 3 |

## 23.620 PPU_FX 603

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX603_SL_ADDR | 0x40029EC0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX603_SL_SIZE | 0x40029EC4 | FULL | Slave region, size |
| PERI_MS_PPU_FX603_SL_ATT0 | 0x40029ED0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX603_SL_ATT1 | 0x40029ED4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX603_SL_ATT2 | 0x40029ED8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX603_SL_ATT3 | 0x40029EDC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX603_MS_ADDR | 0x40029EE0 | FULL | Master region, base address |
| PERI_MS_PPU_FX603_MS_SIZE | 0x40029EE4 | FULL | Master region, size |
| PERI_MS_PPU_FX603_MS_ATT0 | 0x40029EF0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX603_MS_ATT1 | 0x40029EF4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX603_MS_ATT2 | 0x40029EF8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX603_MS_ATT3 | 0x40029EFC | FULL | Master attributes 3 |

## 23.621 PPU_FX 604

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX604_SL_ADDR | 0x40029F00 | FULL | Slave region, base address |
| PERI_MS_PPU_FX604_SL_SIZE | 0x40029F04 | FULL | Slave region, size |
| PERI_MS_PPU_FX604_SL_ATT0 | 0x40029F10 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX604_SL_ATT1 | 0x40029F14 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX604_SL_ATT2 | 0x40029F18 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX604_SL_ATT3 | 0x40029F1C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX604_MS_ADDR | 0x40029F20 | FULL | Master region, base address |
| PERI_MS_PPU_FX604_MS_SIZE | 0x40029F24 | FULL | Master region, size |
| PERI_MS_PPU_FX604_MS_ATT0 | 0x40029F30 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX604_MS_ATT1 | 0x40029F34 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX604_MS_ATT2 | 0x40029F38 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX604_MS_ATT3 | 0x40029F3C | FULL | Master attributes 3 |

## 23.622 PPU_FX 605

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX605_SL_ADDR | 0x40029F40 | FULL | Slave region, base address |
| PERI_MS_PPU_FX605_SL_SIZE | 0x40029F44 | FULL | Slave region, size |
| PERI_MS_PPU_FX605_SL_ATT0 | 0x40029F50 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX605_SL_ATT1 | 0x40029F54 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX605_SL_ATT2 | 0x40029F58 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX605_SL_ATT3 | 0x40029F5C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX605_MS_ADDR | 0x40029F60 | FULL | Master region, base address |
| PERI_MS_PPU_FX605_MS_SIZE | 0x40029F64 | FULL | Master region, size |
| PERI_MS_PPU_FX605_MS_ATT0 | 0x40029F70 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX605_MS_ATT1 | 0x40029F74 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX605_MS_ATT2 | 0x40029F78 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX605_MS_ATT3 | 0x40029F7C | FULL | Master attributes 3 |

## 23.623 PPU_FX 606

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX606_SL_ADDR | 0x40029F80 | FULL | Slave region, base address |
| PERI_MS_PPU_FX606_SL_SIZE | 0x40029F84 | FULL | Slave region, size |
| PERI_MS_PPU_FX606_SL_ATT0 | 0x40029F90 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX606_SL_ATT1 | 0x40029F94 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX606_SL_ATT2 | 0x40029F98 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX606_SL_ATT3 | 0x40029F9C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX606_MS_ADDR | 0x40029FA0 | FULL | Master region, base address |
| PERI_MS_PPU_FX606_MS_SIZE | 0x40029FA4 | FULL | Master region, size |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX606_MS_ATT0 | 0x40029FB0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX606_MS_ATT1 | 0x40029FB4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX606_MS_ATT2 | 0x40029FB8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX606_MS_ATT3 | 0x40029FBC | FULL | Master attributes 3 |

## 23.624 PPU_FX 607

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX607_SL_ADDR | 0x40029FC0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX607_SL_SIZE | 0x40029FC4 | FULL | Slave region, size |
| PERI_MS_PPU_FX607_SL_ATT0 | 0x40029FD0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX607_SL_ATT1 | 0x40029FD4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX607_SL_ATT2 | 0x40029FD8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX607_SL_ATT3 | 0x40029FDC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX607_MS_ADDR | 0x40029FE0 | FULL | Master region, base address |
| PERI_MS_PPU_FX607_MS_SIZE | 0x40029FE4 | FULL | Master region, size |
| PERI_MS_PPU_FX607_MS_ATT0 | 0x40029FF0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX607_MS_ATT1 | 0x40029FF4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX607_MS_ATT2 | 0x40029FF8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX607_MS_ATT3 | 0x40029FFC | FULL | Master attributes 3 |

## 23.625 PPU_FX 608

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX608_SL_ADDR | 0x4002A000 | FULL | Slave region, base address |
| PERI_MS_PPU_FX608_SL_SIZE | 0x4002A004 | FULL | Slave region, size |
| PERI_MS_PPU_FX608_SL_ATT0 | 0x4002A010 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX608_SL_ATT1 | 0x4002A014 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX608_SL_ATT2 | 0x4002A018 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX608_SL_ATT3 | 0x4002A01C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX608_MS_ADDR | 0x4002A020 | FULL | Master region, base address |
| PERI_MS_PPU_FX608_MS_SIZE | 0x4002A024 | FULL | Master region, size |
| PERI_MS_PPU_FX608_MS_ATT0 | 0x4002A030 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX608_MS_ATT1 | 0x4002A034 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX608_MS_ATT2 | 0x4002A038 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX608_MS_ATT3 | 0x4002A03C | FULL | Master attributes 3 |

## 23.626 PPU_FX 609

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX609_SL_ADDR | 0x4002A040 | FULL | Slave region, base address |
| PERI_MS_PPU_FX609_SL_SIZE | 0x4002A044 | FULL | Slave region, size |
| PERI_MS_PPU_FX609_SL_ATT0 | 0x4002A050 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX609_SL_ATT1 | 0x4002A054 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX609_SL_ATT2 | 0x4002A058 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX609_SL_ATT3 | 0x4002A05C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX609_MS_ADDR | 0x4002A060 | FULL | Master region, base address |
| PERI_MS_PPU_FX609_MS_SIZE | 0x4002A064 | FULL | Master region, size |
| PERI_MS_PPU_FX609_MS_ATT0 | 0x4002A070 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX609_MS_ATT1 | 0x4002A074 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX609_MS_ATT2 | 0x4002A078 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX609_MS_ATT3 | 0x4002A07C | FULL | Master attributes 3 |

## 23.627 PPU_FX 610

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX610_SL_ADDR | 0x4002A080 | FULL | Slave region, base address |
| PERI_MS_PPU_FX610_SL_SIZE | 0x4002A084 | FULL | Slave region, size |
| PERI_MS_PPU_FX610_SL_ATT0 | 0x4002A090 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX610_SL_ATT1 | 0x4002A094 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX610_SL_ATT2 | 0x4002A098 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX610_SL_ATT3 | 0x4002A09C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX610_MS_ADDR | 0x4002A0A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX610_MS_SIZE | 0x4002A0A4 | FULL | Master region, size |
| PERI_MS_PPU_FX610_MS_ATT0 | 0x4002A0B0 | FULL | Master attributes 0 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX610_MS_ATT1 | 0x4002A0B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX610_MS_ATT2 | 0x4002A0B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX610_MS_ATT3 | 0x4002A0BC | FULL | Master attributes 3 |

## 23.628 PPU_FX 611

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX611_SL_ADDR | 0x4002A0C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX611_SL_SIZE | 0x4002A0C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX611_SL_ATT0 | 0x4002A0D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX611_SL_ATT1 | 0x4002A0D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX611_SL_ATT2 | 0x4002A0D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX611_SL_ATT3 | 0x4002A0DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX611_MS_ADDR | 0x4002A0E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX611_MS_SIZE | 0x4002A0E4 | FULL | Master region, size |
| PERI_MS_PPU_FX611_MS_ATT0 | 0x4002A0F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX611_MS_ATT1 | 0x4002A0F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX611_MS_ATT2 | 0x4002A0F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX611_MS_ATT3 | 0x4002A0FC | FULL | Master attributes 3 |

## 23.629 PPU_FX 612

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX612_SL_ADDR | 0x4002A100 | FULL | Slave region, base address |
| PERI_MS_PPU_FX612_SL_SIZE | 0x4002A104 | FULL | Slave region, size |
| PERI_MS_PPU_FX612_SL_ATT0 | 0x4002A110 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX612_SL_ATT1 | 0x4002A114 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX612_SL_ATT2 | 0x4002A118 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX612_SL_ATT3 | 0x4002A11C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX612_MS_ADDR | 0x4002A120 | FULL | Master region, base address |
| PERI_MS_PPU_FX612_MS_SIZE | 0x4002A124 | FULL | Master region, size |
| PERI_MS_PPU_FX612_MS_ATT0 | 0x4002A130 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX612_MS_ATT1 | 0x4002A134 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX612_MS_ATT2 | 0x4002A138 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX612_MS_ATT3 | 0x4002A13C | FULL | Master attributes 3 |

## 23.630 PPU_FX 613

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX613_SL_ADDR | 0x4002A140 | FULL | Slave region, base address |
| PERI_MS_PPU_FX613_SL_SIZE | 0x4002A144 | FULL | Slave region, size |
| PERI_MS_PPU_FX613_SL_ATT0 | 0x4002A150 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX613_SL_ATT1 | 0x4002A154 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX613_SL_ATT2 | 0x4002A158 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX613_SL_ATT3 | 0x4002A15C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX613_MS_ADDR | 0x4002A160 | FULL | Master region, base address |
| PERI_MS_PPU_FX613_MS_SIZE | 0x4002A164 | FULL | Master region, size |
| PERI_MS_PPU_FX613_MS_ATT0 | 0x4002A170 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX613_MS_ATT1 | 0x4002A174 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX613_MS_ATT2 | 0x4002A178 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX613_MS_ATT3 | 0x4002A17C | FULL | Master attributes 3 |

## 23.631 PPU_FX 614

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX614_SL_ADDR | 0x4002A180 | FULL | Slave region, base address |
| PERI_MS_PPU_FX614_SL_SIZE | 0x4002A184 | FULL | Slave region, size |
| PERI_MS_PPU_FX614_SL_ATT0 | 0x4002A190 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX614_SL_ATT1 | 0x4002A194 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX614_SL_ATT2 | 0x4002A198 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX614_SL_ATT3 | 0x4002A19C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX614_MS_ADDR | 0x4002A1A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX614_MS_SIZE | 0x4002A1A4 | FULL | Master region, size |
| PERI_MS_PPU_FX614_MS_ATT0 | 0x4002A1B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX614_MS_ATT1 | 0x4002A1B4 | FULL | Master attributes 1 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX614_MS_ATT2 | 0x4002A1B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX614_MS_ATT3 | 0x4002A1BC | FULL | Master attributes 3 |

## 23.632 PPU_FX 615

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX615_SL_ADDR | 0x4002A1C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX615_SL_SIZE | 0x4002A1C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX615_SL_ATT0 | 0x4002A1D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX615_SL_ATT1 | 0x4002A1D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX615_SL_ATT2 | 0x4002A1D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX615_SL_ATT3 | 0x4002A1DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX615_MS_ADDR | 0x4002A1E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX615_MS_SIZE | 0x4002A1E4 | FULL | Master region, size |
| PERI_MS_PPU_FX615_MS_ATT0 | 0x4002A1F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX615_MS_ATT1 | 0x4002A1F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX615_MS_ATT2 | 0x4002A1F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX615_MS_ATT3 | 0x4002A1FC | FULL | Master attributes 3 |

## 23.633 PPU_FX 616

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX616_SL_ADDR | 0x4002A200 | FULL | Slave region, base address |
| PERI_MS_PPU_FX616_SL_SIZE | 0x4002A204 | FULL | Slave region, size |
| PERI_MS_PPU_FX616_SL_ATT0 | 0x4002A210 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX616_SL_ATT1 | 0x4002A214 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX616_SL_ATT2 | 0x4002A218 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX616_SL_ATT3 | 0x4002A21C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX616_MS_ADDR | 0x4002A220 | FULL | Master region, base address |
| PERI_MS_PPU_FX616_MS_SIZE | 0x4002A224 | FULL | Master region, size |
| PERI_MS_PPU_FX616_MS_ATT0 | 0x4002A230 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX616_MS_ATT1 | 0x4002A234 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX616_MS_ATT2 | 0x4002A238 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX616_MS_ATT3 | 0x4002A23C | FULL | Master attributes 3 |

## 23.634 PPU_FX 617

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX617_SL_ADDR | 0x4002A240 | FULL | Slave region, base address |
| PERI_MS_PPU_FX617_SL_SIZE | 0x4002A244 | FULL | Slave region, size |
| PERI_MS_PPU_FX617_SL_ATT0 | 0x4002A250 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX617_SL_ATT1 | 0x4002A254 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX617_SL_ATT2 | 0x4002A258 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX617_SL_ATT3 | 0x4002A25C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX617_MS_ADDR | 0x4002A260 | FULL | Master region, base address |
| PERI_MS_PPU_FX617_MS_SIZE | 0x4002A264 | FULL | Master region, size |
| PERI_MS_PPU_FX617_MS_ATT0 | 0x4002A270 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX617_MS_ATT1 | 0x4002A274 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX617_MS_ATT2 | 0x4002A278 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX617_MS_ATT3 | 0x4002A27C | FULL | Master attributes 3 |

## 23.635 PPU_FX 618

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX618_SL_ADDR | 0x4002A280 | FULL | Slave region, base address |
| PERI_MS_PPU_FX618_SL_SIZE | 0x4002A284 | FULL | Slave region, size |
| PERI_MS_PPU_FX618_SL_ATT0 | 0x4002A290 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX618_SL_ATT1 | 0x4002A294 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX618_SL_ATT2 | 0x4002A298 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX618_SL_ATT3 | 0x4002A29C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX618_MS_ADDR | 0x4002A2A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX618_MS_SIZE | 0x4002A2A4 | FULL | Master region, size |
| PERI_MS_PPU_FX618_MS_ATT0 | 0x4002A2B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX618_MS_ATT1 | 0x4002A2B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX618_MS_ATT2 | 0x4002A2B8 | FULL | Master attributes 2 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX618_MS_ATT3 | 0x4002A2BC | FULL | Master attributes 3 |

## 23.636 PPU_FX 619

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX619_SL_ADDR | 0x4002A2C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX619_SL_SIZE | 0x4002A2C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX619_SL_ATT0 | 0x4002A2D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX619_SL_ATT1 | 0x4002A2D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX619_SL_ATT2 | 0x4002A2D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX619_SL_ATT3 | 0x4002A2DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX619_MS_ADDR | 0x4002A2E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX619_MS_SIZE | 0x4002A2E4 | FULL | Master region, size |
| PERI_MS_PPU_FX619_MS_ATT0 | 0x4002A2F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX619_MS_ATT1 | 0x4002A2F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX619_MS_ATT2 | 0x4002A2F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX619_MS_ATT3 | 0x4002A2FC | FULL | Master attributes 3 |

## 23.637 PPU_FX 620

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX620_SL_ADDR | 0x4002A300 | FULL | Slave region, base address |
| PERI_MS_PPU_FX620_SL_SIZE | 0x4002A304 | FULL | Slave region, size |
| PERI_MS_PPU_FX620_SL_ATT0 | 0x4002A310 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX620_SL_ATT1 | 0x4002A314 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX620_SL_ATT2 | 0x4002A318 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX620_SL_ATT3 | 0x4002A31C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX620_MS_ADDR | 0x4002A320 | FULL | Master region, base address |
| PERI_MS_PPU_FX620_MS_SIZE | 0x4002A324 | FULL | Master region, size |
| PERI_MS_PPU_FX620_MS_ATT0 | 0x4002A330 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX620_MS_ATT1 | 0x4002A334 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX620_MS_ATT2 | 0x4002A338 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX620_MS_ATT3 | 0x4002A33C | FULL | Master attributes 3 |

## 23.638 PPU_FX 621

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX621_SL_ADDR | 0x4002A340 | FULL | Slave region, base address |
| PERI_MS_PPU_FX621_SL_SIZE | 0x4002A344 | FULL | Slave region, size |
| PERI_MS_PPU_FX621_SL_ATT0 | 0x4002A350 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX621_SL_ATT1 | 0x4002A354 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX621_SL_ATT2 | 0x4002A358 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX621_SL_ATT3 | 0x4002A35C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX621_MS_ADDR | 0x4002A360 | FULL | Master region, base address |
| PERI_MS_PPU_FX621_MS_SIZE | 0x4002A364 | FULL | Master region, size |
| PERI_MS_PPU_FX621_MS_ATT0 | 0x4002A370 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX621_MS_ATT1 | 0x4002A374 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX621_MS_ATT2 | 0x4002A378 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX621_MS_ATT3 | 0x4002A37C | FULL | Master attributes 3 |

## 23.639 PPU_FX 622

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX622_SL_ADDR | 0x4002A380 | FULL | Slave region, base address |
| PERI_MS_PPU_FX622_SL_SIZE | 0x4002A384 | FULL | Slave region, size |
| PERI_MS_PPU_FX622_SL_ATT0 | 0x4002A390 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX622_SL_ATT1 | 0x4002A394 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX622_SL_ATT2 | 0x4002A398 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX622_SL_ATT3 | 0x4002A39C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX622_MS_ADDR | 0x4002A3A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX622_MS_SIZE | 0x4002A3A4 | FULL | Master region, size |
| PERI_MS_PPU_FX622_MS_ATT0 | 0x4002A3B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX622_MS_ATT1 | 0x4002A3B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX622_MS_ATT2 | 0x4002A3B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX622_MS_ATT3 | 0x4002A3BC | FULL | Master attributes 3 |

## 23.640 PPU_FX 623

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX623_SL_ADDR | 0x4002A3C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX623_SL_SIZE | 0x4002A3C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX623_SL_ATT0 | 0x4002A3D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX623_SL_ATT1 | 0x4002A3D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX623_SL_ATT2 | 0x4002A3D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX623_SL_ATT3 | 0x4002A3DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX623_MS_ADDR | 0x4002A3E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX623_MS_SIZE | 0x4002A3E4 | FULL | Master region, size |
| PERI_MS_PPU_FX623_MS_ATT0 | 0x4002A3F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX623_MS_ATT1 | 0x4002A3F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX623_MS_ATT2 | 0x4002A3F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX623_MS_ATT3 | 0x4002A3FC | FULL | Master attributes 3 |

## 23.641 PPU_FX 624

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX624_SL_ADDR | 0x4002A400 | FULL | Slave region, base address |
| PERI_MS_PPU_FX624_SL_SIZE | 0x4002A404 | FULL | Slave region, size |
| PERI_MS_PPU_FX624_SL_ATT0 | 0x4002A410 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX624_SL_ATT1 | 0x4002A414 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX624_SL_ATT2 | 0x4002A418 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX624_SL_ATT3 | 0x4002A41C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX624_MS_ADDR | 0x4002A420 | FULL | Master region, base address |
| PERI_MS_PPU_FX624_MS_SIZE | 0x4002A424 | FULL | Master region, size |
| PERI_MS_PPU_FX624_MS_ATT0 | 0x4002A430 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX624_MS_ATT1 | 0x4002A434 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX624_MS_ATT2 | 0x4002A438 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX624_MS_ATT3 | 0x4002A43C | FULL | Master attributes 3 |

## 23.642 PPU_FX 625

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX625_SL_ADDR | 0x4002A440 | FULL | Slave region, base address |
| PERI_MS_PPU_FX625_SL_SIZE | 0x4002A444 | FULL | Slave region, size |
| PERI_MS_PPU_FX625_SL_ATT0 | 0x4002A450 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX625_SL_ATT1 | 0x4002A454 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX625_SL_ATT2 | 0x4002A458 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX625_SL_ATT3 | 0x4002A45C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX625_MS_ADDR | 0x4002A460 | FULL | Master region, base address |
| PERI_MS_PPU_FX625_MS_SIZE | 0x4002A464 | FULL | Master region, size |
| PERI_MS_PPU_FX625_MS_ATT0 | 0x4002A470 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX625_MS_ATT1 | 0x4002A474 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX625_MS_ATT2 | 0x4002A478 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX625_MS_ATT3 | 0x4002A47C | FULL | Master attributes 3 |

## 23.643 PPU_FX 626

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX626_SL_ADDR | 0x4002A480 | FULL | Slave region, base address |
| PERI_MS_PPU_FX626_SL_SIZE | 0x4002A484 | FULL | Slave region, size |
| PERI_MS_PPU_FX626_SL_ATT0 | 0x4002A490 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX626_SL_ATT1 | 0x4002A494 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX626_SL_ATT2 | 0x4002A498 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX626_SL_ATT3 | 0x4002A49C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX626_MS_ADDR | 0x4002A4A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX626_MS_SIZE | 0x4002A4A4 | FULL | Master region, size |
| PERI_MS_PPU_FX626_MS_ATT0 | 0x4002A4B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX626_MS_ATT1 | 0x4002A4B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX626_MS_ATT2 | 0x4002A4B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX626_MS_ATT3 | 0x4002A4BC | FULL | Master attributes 3 |

## 23.644 PPU_FX 627

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX627_SL_ADDR | 0x4002A4C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX627_SL_SIZE | 0x4002A4C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX627_SL_ATT0 | 0x4002A4D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX627_SL_ATT1 | 0x4002A4D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX627_SL_ATT2 | 0x4002A4D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX627_SL_ATT3 | 0x4002A4DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX627_MS_ADDR | 0x4002A4E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX627_MS_SIZE | 0x4002A4E4 | FULL | Master region, size |
| PERI_MS_PPU_FX627_MS_ATT0 | 0x4002A4F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX627_MS_ATT1 | 0x4002A4F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX627_MS_ATT2 | 0x4002A4F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX627_MS_ATT3 | 0x4002A4FC | FULL | Master attributes 3 |

## 23.645 PPU_FX 628

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX628_SL_ADDR | 0x4002A500 | FULL | Slave region, base address |
| PERI_MS_PPU_FX628_SL_SIZE | 0x4002A504 | FULL | Slave region, size |
| PERI_MS_PPU_FX628_SL_ATT0 | 0x4002A510 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX628_SL_ATT1 | 0x4002A514 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX628_SL_ATT2 | 0x4002A518 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX628_SL_ATT3 | 0x4002A51C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX628_MS_ADDR | 0x4002A520 | FULL | Master region, base address |
| PERI_MS_PPU_FX628_MS_SIZE | 0x4002A524 | FULL | Master region, size |
| PERI_MS_PPU_FX628_MS_ATT0 | 0x4002A530 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX628_MS_ATT1 | 0x4002A534 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX628_MS_ATT2 | 0x4002A538 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX628_MS_ATT3 | 0x4002A53C | FULL | Master attributes 3 |

## 23.646 PPU_FX 629

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX629_SL_ADDR | 0x4002A540 | FULL | Slave region, base address |
| PERI_MS_PPU_FX629_SL_SIZE | 0x4002A544 | FULL | Slave region, size |
| PERI_MS_PPU_FX629_SL_ATT0 | 0x4002A550 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX629_SL_ATT1 | 0x4002A554 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX629_SL_ATT2 | 0x4002A558 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX629_SL_ATT3 | 0x4002A55C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX629_MS_ADDR | 0x4002A560 | FULL | Master region, base address |
| PERI_MS_PPU_FX629_MS_SIZE | 0x4002A564 | FULL | Master region, size |
| PERI_MS_PPU_FX629_MS_ATT0 | 0x4002A570 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX629_MS_ATT1 | 0x4002A574 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX629_MS_ATT2 | 0x4002A578 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX629_MS_ATT3 | 0x4002A57C | FULL | Master attributes 3 |

## 23.647 PPU_FX 630

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX630_SL_ADDR | 0x4002A580 | FULL | Slave region, base address |
| PERI_MS_PPU_FX630_SL_SIZE | 0x4002A584 | FULL | Slave region, size |
| PERI_MS_PPU_FX630_SL_ATT0 | 0x4002A590 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX630_SL_ATT1 | 0x4002A594 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX630_SL_ATT2 | 0x4002A598 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX630_SL_ATT3 | 0x4002A59C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX630_MS_ADDR | 0x4002A5A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX630_MS_SIZE | 0x4002A5A4 | FULL | Master region, size |
| PERI_MS_PPU_FX630_MS_ATT0 | 0x4002A5B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX630_MS_ATT1 | 0x4002A5B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX630_MS_ATT2 | 0x4002A5B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX630_MS_ATT3 | 0x4002A5BC | FULL | Master attributes 3 |

## 23.648 PPU_FX 631

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX631_SL_ADDR | 0x4002A5C0 | FULL | Slave region, base address |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX631_SL_SIZE | 0x4002A5C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX631_SL_ATT0 | 0x4002A5D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX631_SL_ATT1 | 0x4002A5D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX631_SL_ATT2 | 0x4002A5D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX631_SL_ATT3 | 0x4002A5DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX631_MS_ADDR | 0x4002A5E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX631_MS_SIZE | 0x4002A5E4 | FULL | Master region, size |
| PERI_MS_PPU_FX631_MS_ATT0 | 0x4002A5F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX631_MS_ATT1 | 0x4002A5F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX631_MS_ATT2 | 0x4002A5F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX631_MS_ATT3 | 0x4002A5FC | FULL | Master attributes 3 |

## 23.649 PPU_FX 632

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX632_SL_ADDR | 0x4002A600 | FULL | Slave region, base address |
| PERI_MS_PPU_FX632_SL_SIZE | 0x4002A604 | FULL | Slave region, size |
| PERI_MS_PPU_FX632_SL_ATT0 | 0x4002A610 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX632_SL_ATT1 | 0x4002A614 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX632_SL_ATT2 | 0x4002A618 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX632_SL_ATT3 | 0x4002A61C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX632_MS_ADDR | 0x4002A620 | FULL | Master region, base address |
| PERI_MS_PPU_FX632_MS_SIZE | 0x4002A624 | FULL | Master region, size |
| PERI_MS_PPU_FX632_MS_ATT0 | 0x4002A630 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX632_MS_ATT1 | 0x4002A634 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX632_MS_ATT2 | 0x4002A638 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX632_MS_ATT3 | 0x4002A63C | FULL | Master attributes 3 |

## 23.650 PPU_FX 633

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX633_SL_ADDR | 0x4002A640 | FULL | Slave region, base address |
| PERI_MS_PPU_FX633_SL_SIZE | 0x4002A644 | FULL | Slave region, size |
| PERI_MS_PPU_FX633_SL_ATT0 | 0x4002A650 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX633_SL_ATT1 | 0x4002A654 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX633_SL_ATT2 | 0x4002A658 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX633_SL_ATT3 | 0x4002A65C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX633_MS_ADDR | 0x4002A660 | FULL | Master region, base address |
| PERI_MS_PPU_FX633_MS_SIZE | 0x4002A664 | FULL | Master region, size |
| PERI_MS_PPU_FX633_MS_ATT0 | 0x4002A670 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX633_MS_ATT1 | 0x4002A674 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX633_MS_ATT2 | 0x4002A678 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX633_MS_ATT3 | 0x4002A67C | FULL | Master attributes 3 |

## 23.651 PPU_FX 634

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX634_SL_ADDR | 0x4002A680 | FULL | Slave region, base address |
| PERI_MS_PPU_FX634_SL_SIZE | 0x4002A684 | FULL | Slave region, size |
| PERI_MS_PPU_FX634_SL_ATT0 | 0x4002A690 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX634_SL_ATT1 | 0x4002A694 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX634_SL_ATT2 | 0x4002A698 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX634_SL_ATT3 | 0x4002A69C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX634_MS_ADDR | 0x4002A6A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX634_MS_SIZE | 0x4002A6A4 | FULL | Master region, size |
| PERI_MS_PPU_FX634_MS_ATT0 | 0x4002A6B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX634_MS_ATT1 | 0x4002A6B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX634_MS_ATT2 | 0x4002A6B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX634_MS_ATT3 | 0x4002A6BC | FULL | Master attributes 3 |

## 23.652 PPU_FX 635

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX635_SL_ADDR | 0x4002A6C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX635_SL_SIZE | 0x4002A6C4 | FULL | Slave region, size |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX635_SL_ATT0 | 0x4002A6D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX635_SL_ATT1 | 0x4002A6D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX635_SL_ATT2 | 0x4002A6D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX635_SL_ATT3 | 0x4002A6DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX635_MS_ADDR | 0x4002A6E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX635_MS_SIZE | 0x4002A6E4 | FULL | Master region, size |
| PERI_MS_PPU_FX635_MS_ATT0 | 0x4002A6F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX635_MS_ATT1 | 0x4002A6F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX635_MS_ATT2 | 0x4002A6F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX635_MS_ATT3 | 0x4002A6FC | FULL | Master attributes 3 |

## 23.653 PPU_FX 636

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX636_SL_ADDR | 0x4002A700 | FULL | Slave region, base address |
| PERI_MS_PPU_FX636_SL_SIZE | 0x4002A704 | FULL | Slave region, size |
| PERI_MS_PPU_FX636_SL_ATT0 | 0x4002A710 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX636_SL_ATT1 | 0x4002A714 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX636_SL_ATT2 | 0x4002A718 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX636_SL_ATT3 | 0x4002A71C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX636_MS_ADDR | 0x4002A720 | FULL | Master region, base address |
| PERI_MS_PPU_FX636_MS_SIZE | 0x4002A724 | FULL | Master region, size |
| PERI_MS_PPU_FX636_MS_ATT0 | 0x4002A730 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX636_MS_ATT1 | 0x4002A734 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX636_MS_ATT2 | 0x4002A738 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX636_MS_ATT3 | 0x4002A73C | FULL | Master attributes 3 |

## 23.654 PPU_FX 637

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX637_SL_ADDR | 0x4002A740 | FULL | Slave region, base address |
| PERI_MS_PPU_FX637_SL_SIZE | 0x4002A744 | FULL | Slave region, size |
| PERI_MS_PPU_FX637_SL_ATT0 | 0x4002A750 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX637_SL_ATT1 | 0x4002A754 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX637_SL_ATT2 | 0x4002A758 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX637_SL_ATT3 | 0x4002A75C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX637_MS_ADDR | 0x4002A760 | FULL | Master region, base address |
| PERI_MS_PPU_FX637_MS_SIZE | 0x4002A764 | FULL | Master region, size |
| PERI_MS_PPU_FX637_MS_ATT0 | 0x4002A770 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX637_MS_ATT1 | 0x4002A774 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX637_MS_ATT2 | 0x4002A778 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX637_MS_ATT3 | 0x4002A77C | FULL | Master attributes 3 |

## 23.655 PPU_FX 638

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX638_SL_ADDR | 0x4002A780 | FULL | Slave region, base address |
| PERI_MS_PPU_FX638_SL_SIZE | 0x4002A784 | FULL | Slave region, size |
| PERI_MS_PPU_FX638_SL_ATT0 | 0x4002A790 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX638_SL_ATT1 | 0x4002A794 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX638_SL_ATT2 | 0x4002A798 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX638_SL_ATT3 | 0x4002A79C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX638_MS_ADDR | 0x4002A7A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX638_MS_SIZE | 0x4002A7A4 | FULL | Master region, size |
| PERI_MS_PPU_FX638_MS_ATT0 | 0x4002A7B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX638_MS_ATT1 | 0x4002A7B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX638_MS_ATT2 | 0x4002A7B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX638_MS_ATT3 | 0x4002A7BC | FULL | Master attributes 3 |

## 23.656 PPU_FX 639

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX639_SL_ADDR | 0x4002A7C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX639_SL_SIZE | 0x4002A7C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX639_SL_ATT0 | 0x4002A7D0 | FULL | Slave attributes 0 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX639_SL_ATT1 | 0x4002A7D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX639_SL_ATT2 | 0x4002A7D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX639_SL_ATT3 | 0x4002A7DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX639_MS_ADDR | 0x4002A7E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX639_MS_SIZE | 0x4002A7E4 | FULL | Master region, size |
| PERI_MS_PPU_FX639_MS_ATT0 | 0x4002A7F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX639_MS_ATT1 | 0x4002A7F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX639_MS_ATT2 | 0x4002A7F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX639_MS_ATT3 | 0x4002A7FC | FULL | Master attributes 3 |

## 23.657 PPU_FX 640

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX640_SL_ADDR | 0x4002A800 | FULL | Slave region, base address |
| PERI_MS_PPU_FX640_SL_SIZE | 0x4002A804 | FULL | Slave region, size |
| PERI_MS_PPU_FX640_SL_ATT0 | 0x4002A810 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX640_SL_ATT1 | 0x4002A814 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX640_SL_ATT2 | 0x4002A818 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX640_SL_ATT3 | 0x4002A81C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX640_MS_ADDR | 0x4002A820 | FULL | Master region, base address |
| PERI_MS_PPU_FX640_MS_SIZE | 0x4002A824 | FULL | Master region, size |
| PERI_MS_PPU_FX640_MS_ATT0 | 0x4002A830 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX640_MS_ATT1 | 0x4002A834 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX640_MS_ATT2 | 0x4002A838 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX640_MS_ATT3 | 0x4002A83C | FULL | Master attributes 3 |

## 23.658 PPU_FX 641

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX641_SL_ADDR | 0x4002A840 | FULL | Slave region, base address |
| PERI_MS_PPU_FX641_SL_SIZE | 0x4002A844 | FULL | Slave region, size |
| PERI_MS_PPU_FX641_SL_ATT0 | 0x4002A850 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX641_SL_ATT1 | 0x4002A854 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX641_SL_ATT2 | 0x4002A858 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX641_SL_ATT3 | 0x4002A85C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX641_MS_ADDR | 0x4002A860 | FULL | Master region, base address |
| PERI_MS_PPU_FX641_MS_SIZE | 0x4002A864 | FULL | Master region, size |
| PERI_MS_PPU_FX641_MS_ATT0 | 0x4002A870 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX641_MS_ATT1 | 0x4002A874 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX641_MS_ATT2 | 0x4002A878 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX641_MS_ATT3 | 0x4002A87C | FULL | Master attributes 3 |

## 23.659 PPU_FX 642

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX642_SL_ADDR | 0x4002A880 | FULL | Slave region, base address |
| PERI_MS_PPU_FX642_SL_SIZE | 0x4002A884 | FULL | Slave region, size |
| PERI_MS_PPU_FX642_SL_ATT0 | 0x4002A890 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX642_SL_ATT1 | 0x4002A894 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX642_SL_ATT2 | 0x4002A898 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX642_SL_ATT3 | 0x4002A89C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX642_MS_ADDR | 0x4002A8A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX642_MS_SIZE | 0x4002A8A4 | FULL | Master region, size |
| PERI_MS_PPU_FX642_MS_ATT0 | 0x4002A8B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX642_MS_ATT1 | 0x4002A8B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX642_MS_ATT2 | 0x4002A8B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX642_MS_ATT3 | 0x4002A8BC | FULL | Master attributes 3 |

## 23.660 PPU_FX 643

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX643_SL_ADDR | 0x4002A8C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX643_SL_SIZE | 0x4002A8C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX643_SL_ATT0 | 0x4002A8D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX643_SL_ATT1 | 0x4002A8D4 | FULL | Slave attributes 1 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX643_SL_ATT2 | 0x4002A8D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX643_SL_ATT3 | 0x4002A8DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX643_MS_ADDR | 0x4002A8E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX643_MS_SIZE | 0x4002A8E4 | FULL | Master region, size |
| PERI_MS_PPU_FX643_MS_ATT0 | 0x4002A8F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX643_MS_ATT1 | 0x4002A8F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX643_MS_ATT2 | 0x4002A8F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX643_MS_ATT3 | 0x4002A8FC | FULL | Master attributes 3 |

## 23.661 PPU_FX 644

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX644_SL_ADDR | 0x4002A900 | FULL | Slave region, base address |
| PERI_MS_PPU_FX644_SL_SIZE | 0x4002A904 | FULL | Slave region, size |
| PERI_MS_PPU_FX644_SL_ATT0 | 0x4002A910 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX644_SL_ATT1 | 0x4002A914 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX644_SL_ATT2 | 0x4002A918 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX644_SL_ATT3 | 0x4002A91C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX644_MS_ADDR | 0x4002A920 | FULL | Master region, base address |
| PERI_MS_PPU_FX644_MS_SIZE | 0x4002A924 | FULL | Master region, size |
| PERI_MS_PPU_FX644_MS_ATT0 | 0x4002A930 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX644_MS_ATT1 | 0x4002A934 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX644_MS_ATT2 | 0x4002A938 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX644_MS_ATT3 | 0x4002A93C | FULL | Master attributes 3 |

## 23.662 PPU_FX 645

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX645_SL_ADDR | 0x4002A940 | FULL | Slave region, base address |
| PERI_MS_PPU_FX645_SL_SIZE | 0x4002A944 | FULL | Slave region, size |
| PERI_MS_PPU_FX645_SL_ATT0 | 0x4002A950 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX645_SL_ATT1 | 0x4002A954 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX645_SL_ATT2 | 0x4002A958 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX645_SL_ATT3 | 0x4002A95C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX645_MS_ADDR | 0x4002A960 | FULL | Master region, base address |
| PERI_MS_PPU_FX645_MS_SIZE | 0x4002A964 | FULL | Master region, size |
| PERI_MS_PPU_FX645_MS_ATT0 | 0x4002A970 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX645_MS_ATT1 | 0x4002A974 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX645_MS_ATT2 | 0x4002A978 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX645_MS_ATT3 | 0x4002A97C | FULL | Master attributes 3 |

## 23.663 PPU_FX 646

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX646_SL_ADDR | 0x4002A980 | FULL | Slave region, base address |
| PERI_MS_PPU_FX646_SL_SIZE | 0x4002A984 | FULL | Slave region, size |
| PERI_MS_PPU_FX646_SL_ATT0 | 0x4002A990 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX646_SL_ATT1 | 0x4002A994 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX646_SL_ATT2 | 0x4002A998 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX646_SL_ATT3 | 0x4002A99C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX646_MS_ADDR | 0x4002A9A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX646_MS_SIZE | 0x4002A9A4 | FULL | Master region, size |
| PERI_MS_PPU_FX646_MS_ATT0 | 0x4002A9B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX646_MS_ATT1 | 0x4002A9B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX646_MS_ATT2 | 0x4002A9B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX646_MS_ATT3 | 0x4002A9BC | FULL | Master attributes 3 |

## 23.664 PPU_FX 647

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX647_SL_ADDR | 0x4002A9C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX647_SL_SIZE | 0x4002A9C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX647_SL_ATT0 | 0x4002A9D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX647_SL_ATT1 | 0x4002A9D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX647_SL_ATT2 | 0x4002A9D8 | FULL | Slave attributes 2 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX647_SL_ATT3 | 0x4002A9DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX647_MS_ADDR | 0x4002A9E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX647_MS_SIZE | 0x4002A9E4 | FULL | Master region, size |
| PERI_MS_PPU_FX647_MS_ATT0 | 0x4002A9F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX647_MS_ATT1 | 0x4002A9F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX647_MS_ATT2 | 0x4002A9F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX647_MS_ATT3 | 0x4002A9FC | FULL | Master attributes 3 |

## 23.665 PPU_FX 648

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX648_SL_ADDR | 0x4002AA00 | FULL | Slave region, base address |
| PERI_MS_PPU_FX648_SL_SIZE | 0x4002AA04 | FULL | Slave region, size |
| PERI_MS_PPU_FX648_SL_ATT0 | 0x4002AA10 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX648_SL_ATT1 | 0x4002AA14 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX648_SL_ATT2 | 0x4002AA18 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX648_SL_ATT3 | 0x4002AA1C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX648_MS_ADDR | 0x4002AA20 | FULL | Master region, base address |
| PERI_MS_PPU_FX648_MS_SIZE | 0x4002AA24 | FULL | Master region, size |
| PERI_MS_PPU_FX648_MS_ATT0 | 0x4002AA30 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX648_MS_ATT1 | 0x4002AA34 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX648_MS_ATT2 | 0x4002AA38 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX648_MS_ATT3 | 0x4002AA3C | FULL | Master attributes 3 |

## 23.666 PPU_FX 649

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX649_SL_ADDR | 0x4002AA40 | FULL | Slave region, base address |
| PERI_MS_PPU_FX649_SL_SIZE | 0x4002AA44 | FULL | Slave region, size |
| PERI_MS_PPU_FX649_SL_ATT0 | 0x4002AA50 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX649_SL_ATT1 | 0x4002AA54 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX649_SL_ATT2 | 0x4002AA58 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX649_SL_ATT3 | 0x4002AA5C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX649_MS_ADDR | 0x4002AA60 | FULL | Master region, base address |
| PERI_MS_PPU_FX649_MS_SIZE | 0x4002AA64 | FULL | Master region, size |
| PERI_MS_PPU_FX649_MS_ATT0 | 0x4002AA70 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX649_MS_ATT1 | 0x4002AA74 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX649_MS_ATT2 | 0x4002AA78 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX649_MS_ATT3 | 0x4002AA7C | FULL | Master attributes 3 |

## 23.667 PPU_FX 650

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX650_SL_ADDR | 0x4002AA80 | FULL | Slave region, base address |
| PERI_MS_PPU_FX650_SL_SIZE | 0x4002AA84 | FULL | Slave region, size |
| PERI_MS_PPU_FX650_SL_ATT0 | 0x4002AA90 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX650_SL_ATT1 | 0x4002AA94 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX650_SL_ATT2 | 0x4002AA98 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX650_SL_ATT3 | 0x4002AA9C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX650_MS_ADDR | 0x4002AAA0 | FULL | Master region, base address |
| PERI_MS_PPU_FX650_MS_SIZE | 0x4002AAA4 | FULL | Master region, size |
| PERI_MS_PPU_FX650_MS_ATT0 | 0x4002AAB0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX650_MS_ATT1 | 0x4002AAB4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX650_MS_ATT2 | 0x4002AAB8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX650_MS_ATT3 | 0x4002AABC | FULL | Master attributes 3 |

## 23.668 PPU_FX 651

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX651_SL_ADDR | 0x4002AAC0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX651_SL_SIZE | 0x4002AAC4 | FULL | Slave region, size |
| PERI_MS_PPU_FX651_SL_ATT0 | 0x4002AAD0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX651_SL_ATT1 | 0x4002AAD4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX651_SL_ATT2 | 0x4002AAD8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX651_SL_ATT3 | 0x4002AADC | FULL | Slave attributes 3 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX651_MS_ADDR | 0x4002AAE0 | FULL | Master region, base address |
| PERI_MS_PPU_FX651_MS_SIZE | 0x4002AAE4 | FULL | Master region, size |
| PERI_MS_PPU_FX651_MS_ATT0 | 0x4002AAF0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX651_MS_ATT1 | 0x4002AAF4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX651_MS_ATT2 | 0x4002AAF8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX651_MS_ATT3 | 0x4002AAFC | FULL | Master attributes 3 |

## 23.669 PPU_FX 652

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX652_SL_ADDR | 0x4002AB00 | FULL | Slave region, base address |
| PERI_MS_PPU_FX652_SL_SIZE | 0x4002AB04 | FULL | Slave region, size |
| PERI_MS_PPU_FX652_SL_ATT0 | 0x4002AB10 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX652_SL_ATT1 | 0x4002AB14 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX652_SL_ATT2 | 0x4002AB18 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX652_SL_ATT3 | 0x4002AB1C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX652_MS_ADDR | 0x4002AB20 | FULL | Master region, base address |
| PERI_MS_PPU_FX652_MS_SIZE | 0x4002AB24 | FULL | Master region, size |
| PERI_MS_PPU_FX652_MS_ATT0 | 0x4002AB30 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX652_MS_ATT1 | 0x4002AB34 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX652_MS_ATT2 | 0x4002AB38 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX652_MS_ATT3 | 0x4002AB3C | FULL | Master attributes 3 |

## 23.670 PPU_FX 653

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX653_SL_ADDR | 0x4002AB40 | FULL | Slave region, base address |
| PERI_MS_PPU_FX653_SL_SIZE | 0x4002AB44 | FULL | Slave region, size |
| PERI_MS_PPU_FX653_SL_ATT0 | 0x4002AB50 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX653_SL_ATT1 | 0x4002AB54 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX653_SL_ATT2 | 0x4002AB58 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX653_SL_ATT3 | 0x4002AB5C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX653_MS_ADDR | 0x4002AB60 | FULL | Master region, base address |
| PERI_MS_PPU_FX653_MS_SIZE | 0x4002AB64 | FULL | Master region, size |
| PERI_MS_PPU_FX653_MS_ATT0 | 0x4002AB70 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX653_MS_ATT1 | 0x4002AB74 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX653_MS_ATT2 | 0x4002AB78 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX653_MS_ATT3 | 0x4002AB7C | FULL | Master attributes 3 |

## 23.671 PPU_FX 654

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX654_SL_ADDR | 0x4002AB80 | FULL | Slave region, base address |
| PERI_MS_PPU_FX654_SL_SIZE | 0x4002AB84 | FULL | Slave region, size |
| PERI_MS_PPU_FX654_SL_ATT0 | 0x4002AB90 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX654_SL_ATT1 | 0x4002AB94 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX654_SL_ATT2 | 0x4002AB98 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX654_SL_ATT3 | 0x4002AB9C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX654_MS_ADDR | 0x4002ABA0 | FULL | Master region, base address |
| PERI_MS_PPU_FX654_MS_SIZE | 0x4002ABA4 | FULL | Master region, size |
| PERI_MS_PPU_FX654_MS_ATT0 | 0x4002ABB0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX654_MS_ATT1 | 0x4002ABB4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX654_MS_ATT2 | 0x4002ABB8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX654_MS_ATT3 | 0x4002ABBC | FULL | Master attributes 3 |

## 23.672 PPU_FX 655

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX655_SL_ADDR | 0x4002ABC0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX655_SL_SIZE | 0x4002ABC4 | FULL | Slave region, size |
| PERI_MS_PPU_FX655_SL_ATT0 | 0x4002ABD0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX655_SL_ATT1 | 0x4002ABD4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX655_SL_ATT2 | 0x4002ABD8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX655_SL_ATT3 | 0x4002ABDC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX655_MS_ADDR | 0x4002ABE0 | FULL | Master region, base address |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX655_MS_SIZE | 0x4002ABE4 | FULL | Master region, size |
| PERI_MS_PPU_FX655_MS_ATT0 | 0x4002ABF0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX655_MS_ATT1 | 0x4002ABF4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX655_MS_ATT2 | 0x4002ABF8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX655_MS_ATT3 | 0x4002ABFC | FULL | Master attributes 3 |

## 23.673 PPU_FX 656

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX656_SL_ADDR | 0x4002AC00 | FULL | Slave region, base address |
| PERI_MS_PPU_FX656_SL_SIZE | 0x4002AC04 | FULL | Slave region, size |
| PERI_MS_PPU_FX656_SL_ATT0 | 0x4002AC10 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX656_SL_ATT1 | 0x4002AC14 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX656_SL_ATT2 | 0x4002AC18 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX656_SL_ATT3 | 0x4002AC1C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX656_MS_ADDR | 0x4002AC20 | FULL | Master region, base address |
| PERI_MS_PPU_FX656_MS_SIZE | 0x4002AC24 | FULL | Master region, size |
| PERI_MS_PPU_FX656_MS_ATT0 | 0x4002AC30 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX656_MS_ATT1 | 0x4002AC34 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX656_MS_ATT2 | 0x4002AC38 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX656_MS_ATT3 | 0x4002AC3C | FULL | Master attributes 3 |

## 23.674 PPU_FX 657

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX657_SL_ADDR | 0x4002AC40 | FULL | Slave region, base address |
| PERI_MS_PPU_FX657_SL_SIZE | 0x4002AC44 | FULL | Slave region, size |
| PERI_MS_PPU_FX657_SL_ATT0 | 0x4002AC50 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX657_SL_ATT1 | 0x4002AC54 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX657_SL_ATT2 | 0x4002AC58 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX657_SL_ATT3 | 0x4002AC5C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX657_MS_ADDR | 0x4002AC60 | FULL | Master region, base address |
| PERI_MS_PPU_FX657_MS_SIZE | 0x4002AC64 | FULL | Master region, size |
| PERI_MS_PPU_FX657_MS_ATT0 | 0x4002AC70 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX657_MS_ATT1 | 0x4002AC74 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX657_MS_ATT2 | 0x4002AC78 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX657_MS_ATT3 | 0x4002AC7C | FULL | Master attributes 3 |

## 23.675 PPU_FX 658

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX658_SL_ADDR | 0x4002AC80 | FULL | Slave region, base address |
| PERI_MS_PPU_FX658_SL_SIZE | 0x4002AC84 | FULL | Slave region, size |
| PERI_MS_PPU_FX658_SL_ATT0 | 0x4002AC90 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX658_SL_ATT1 | 0x4002AC94 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX658_SL_ATT2 | 0x4002AC98 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX658_SL_ATT3 | 0x4002AC9C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX658_MS_ADDR | 0x4002ACA0 | FULL | Master region, base address |
| PERI_MS_PPU_FX658_MS_SIZE | 0x4002ACA4 | FULL | Master region, size |
| PERI_MS_PPU_FX658_MS_ATT0 | 0x4002ACB0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX658_MS_ATT1 | 0x4002ACB4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX658_MS_ATT2 | 0x4002ACB8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX658_MS_ATT3 | 0x4002ACBC | FULL | Master attributes 3 |

## 23.676 PPU_FX 659

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX659_SL_ADDR | 0x4002ACC0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX659_SL_SIZE | 0x4002ACC4 | FULL | Slave region, size |
| PERI_MS_PPU_FX659_SL_ATT0 | 0x4002ACD0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX659_SL_ATT1 | 0x4002ACD4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX659_SL_ATT2 | 0x4002ACD8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX659_SL_ATT3 | 0x4002ACDC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX659_MS_ADDR | 0x4002ACE0 | FULL | Master region, base address |
| PERI_MS_PPU_FX659_MS_SIZE | 0x4002ACE4 | FULL | Master region, size |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX659_MS_ATT0 | 0x4002ACF0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX659_MS_ATT1 | 0x4002ACF4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX659_MS_ATT2 | 0x4002ACF8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX659_MS_ATT3 | 0x4002ACFC | FULL | Master attributes 3 |

## 23.677 PPU_FX 660

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX660_SL_ADDR | 0x4002AD00 | FULL | Slave region, base address |
| PERI_MS_PPU_FX660_SL_SIZE | 0x4002AD04 | FULL | Slave region, size |
| PERI_MS_PPU_FX660_SL_ATT0 | 0x4002AD10 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX660_SL_ATT1 | 0x4002AD14 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX660_SL_ATT2 | 0x4002AD18 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX660_SL_ATT3 | 0x4002AD1C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX660_MS_ADDR | 0x4002AD20 | FULL | Master region, base address |
| PERI_MS_PPU_FX660_MS_SIZE | 0x4002AD24 | FULL | Master region, size |
| PERI_MS_PPU_FX660_MS_ATT0 | 0x4002AD30 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX660_MS_ATT1 | 0x4002AD34 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX660_MS_ATT2 | 0x4002AD38 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX660_MS_ATT3 | 0x4002AD3C | FULL | Master attributes 3 |

## 23.678 PPU_FX 661

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX661_SL_ADDR | 0x4002AD40 | FULL | Slave region, base address |
| PERI_MS_PPU_FX661_SL_SIZE | 0x4002AD44 | FULL | Slave region, size |
| PERI_MS_PPU_FX661_SL_ATT0 | 0x4002AD50 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX661_SL_ATT1 | 0x4002AD54 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX661_SL_ATT2 | 0x4002AD58 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX661_SL_ATT3 | 0x4002AD5C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX661_MS_ADDR | 0x4002AD60 | FULL | Master region, base address |
| PERI_MS_PPU_FX661_MS_SIZE | 0x4002AD64 | FULL | Master region, size |
| PERI_MS_PPU_FX661_MS_ATT0 | 0x4002AD70 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX661_MS_ATT1 | 0x4002AD74 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX661_MS_ATT2 | 0x4002AD78 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX661_MS_ATT3 | 0x4002AD7C | FULL | Master attributes 3 |

## 23.679 PPU_FX 662

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX662_SL_ADDR | 0x4002AD80 | FULL | Slave region, base address |
| PERI_MS_PPU_FX662_SL_SIZE | 0x4002AD84 | FULL | Slave region, size |
| PERI_MS_PPU_FX662_SL_ATT0 | 0x4002AD90 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX662_SL_ATT1 | 0x4002AD94 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX662_SL_ATT2 | 0x4002AD98 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX662_SL_ATT3 | 0x4002AD9C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX662_MS_ADDR | 0x4002ADA0 | FULL | Master region, base address |
| PERI_MS_PPU_FX662_MS_SIZE | 0x4002ADA4 | FULL | Master region, size |
| PERI_MS_PPU_FX662_MS_ATT0 | 0x4002ADB0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX662_MS_ATT1 | 0x4002ADB4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX662_MS_ATT2 | 0x4002ADB8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX662_MS_ATT3 | 0x4002ADBC | FULL | Master attributes 3 |

## 23.680 PPU_FX 663

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX663_SL_ADDR | 0x4002ADC0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX663_SL_SIZE | 0x4002ADC4 | FULL | Slave region, size |
| PERI_MS_PPU_FX663_SL_ATT0 | 0x4002ADD0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX663_SL_ATT1 | 0x4002ADD4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX663_SL_ATT2 | 0x4002ADD8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX663_SL_ATT3 | 0x4002ADDC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX663_MS_ADDR | 0x4002ADE0 | FULL | Master region, base address |
| PERI_MS_PPU_FX663_MS_SIZE | 0x4002ADE4 | FULL | Master region, size |
| PERI_MS_PPU_FX663_MS_ATT0 | 0x4002ADF0 | FULL | Master attributes 0 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX663_MS_ATT1 | 0x4002ADF4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX663_MS_ATT2 | 0x4002ADF8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX663_MS_ATT3 | 0x4002ADFC | FULL | Master attributes 3 |

## 23.681 PPU_FX 664

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX664_SL_ADDR | 0x4002AE00 | FULL | Slave region, base address |
| PERI_MS_PPU_FX664_SL_SIZE | 0x4002AE04 | FULL | Slave region, size |
| PERI_MS_PPU_FX664_SL_ATT0 | 0x4002AE10 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX664_SL_ATT1 | 0x4002AE14 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX664_SL_ATT2 | 0x4002AE18 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX664_SL_ATT3 | 0x4002AE1C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX664_MS_ADDR | 0x4002AE20 | FULL | Master region, base address |
| PERI_MS_PPU_FX664_MS_SIZE | 0x4002AE24 | FULL | Master region, size |
| PERI_MS_PPU_FX664_MS_ATT0 | 0x4002AE30 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX664_MS_ATT1 | 0x4002AE34 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX664_MS_ATT2 | 0x4002AE38 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX664_MS_ATT3 | 0x4002AE3C | FULL | Master attributes 3 |

## 23.682 PPU_FX 665

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX665_SL_ADDR | 0x4002AE40 | FULL | Slave region, base address |
| PERI_MS_PPU_FX665_SL_SIZE | 0x4002AE44 | FULL | Slave region, size |
| PERI_MS_PPU_FX665_SL_ATT0 | 0x4002AE50 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX665_SL_ATT1 | 0x4002AE54 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX665_SL_ATT2 | 0x4002AE58 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX665_SL_ATT3 | 0x4002AE5C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX665_MS_ADDR | 0x4002AE60 | FULL | Master region, base address |
| PERI_MS_PPU_FX665_MS_SIZE | 0x4002AE64 | FULL | Master region, size |
| PERI_MS_PPU_FX665_MS_ATT0 | 0x4002AE70 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX665_MS_ATT1 | 0x4002AE74 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX665_MS_ATT2 | 0x4002AE78 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX665_MS_ATT3 | 0x4002AE7C | FULL | Master attributes 3 |

## 23.683 PPU_FX 666

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX666_SL_ADDR | 0x4002AE80 | FULL | Slave region, base address |
| PERI_MS_PPU_FX666_SL_SIZE | 0x4002AE84 | FULL | Slave region, size |
| PERI_MS_PPU_FX666_SL_ATT0 | 0x4002AE90 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX666_SL_ATT1 | 0x4002AE94 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX666_SL_ATT2 | 0x4002AE98 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX666_SL_ATT3 | 0x4002AE9C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX666_MS_ADDR | 0x4002AEA0 | FULL | Master region, base address |
| PERI_MS_PPU_FX666_MS_SIZE | 0x4002AEA4 | FULL | Master region, size |
| PERI_MS_PPU_FX666_MS_ATT0 | 0x4002AEB0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX666_MS_ATT1 | 0x4002AEB4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX666_MS_ATT2 | 0x4002AEB8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX666_MS_ATT3 | 0x4002AEBC | FULL | Master attributes 3 |

## 23.684 PPU_FX 667

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX667_SL_ADDR | 0x4002AEC0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX667_SL_SIZE | 0x4002AEC4 | FULL | Slave region, size |
| PERI_MS_PPU_FX667_SL_ATT0 | 0x4002AED0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX667_SL_ATT1 | 0x4002AED4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX667_SL_ATT2 | 0x4002AED8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX667_SL_ATT3 | 0x4002AEDC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX667_MS_ADDR | 0x4002AEE0 | FULL | Master region, base address |
| PERI_MS_PPU_FX667_MS_SIZE | 0x4002AEE4 | FULL | Master region, size |
| PERI_MS_PPU_FX667_MS_ATT0 | 0x4002AEF0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX667_MS_ATT1 | 0x4002AEF4 | FULL | Master attributes 1 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX667_MS_ATT2 | 0x4002AEF8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX667_MS_ATT3 | 0x4002AEFC | FULL | Master attributes 3 |

## 23.685 PPU_FX 668

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX668_SL_ADDR | 0x4002AF00 | FULL | Slave region, base address |
| PERI_MS_PPU_FX668_SL_SIZE | 0x4002AF04 | FULL | Slave region, size |
| PERI_MS_PPU_FX668_SL_ATT0 | 0x4002AF10 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX668_SL_ATT1 | 0x4002AF14 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX668_SL_ATT2 | 0x4002AF18 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX668_SL_ATT3 | 0x4002AF1C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX668_MS_ADDR | 0x4002AF20 | FULL | Master region, base address |
| PERI_MS_PPU_FX668_MS_SIZE | 0x4002AF24 | FULL | Master region, size |
| PERI_MS_PPU_FX668_MS_ATT0 | 0x4002AF30 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX668_MS_ATT1 | 0x4002AF34 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX668_MS_ATT2 | 0x4002AF38 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX668_MS_ATT3 | 0x4002AF3C | FULL | Master attributes 3 |

## 23.686 PPU_FX 669

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX669_SL_ADDR | 0x4002AF40 | FULL | Slave region, base address |
| PERI_MS_PPU_FX669_SL_SIZE | 0x4002AF44 | FULL | Slave region, size |
| PERI_MS_PPU_FX669_SL_ATT0 | 0x4002AF50 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX669_SL_ATT1 | 0x4002AF54 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX669_SL_ATT2 | 0x4002AF58 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX669_SL_ATT3 | 0x4002AF5C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX669_MS_ADDR | 0x4002AF60 | FULL | Master region, base address |
| PERI_MS_PPU_FX669_MS_SIZE | 0x4002AF64 | FULL | Master region, size |
| PERI_MS_PPU_FX669_MS_ATT0 | 0x4002AF70 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX669_MS_ATT1 | 0x4002AF74 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX669_MS_ATT2 | 0x4002AF78 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX669_MS_ATT3 | 0x4002AF7C | FULL | Master attributes 3 |

## 23.687 PPU_FX 670

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX670_SL_ADDR | 0x4002AF80 | FULL | Slave region, base address |
| PERI_MS_PPU_FX670_SL_SIZE | 0x4002AF84 | FULL | Slave region, size |
| PERI_MS_PPU_FX670_SL_ATT0 | 0x4002AF90 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX670_SL_ATT1 | 0x4002AF94 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX670_SL_ATT2 | 0x4002AF98 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX670_SL_ATT3 | 0x4002AF9C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX670_MS_ADDR | 0x4002AFA0 | FULL | Master region, base address |
| PERI_MS_PPU_FX670_MS_SIZE | 0x4002AFA4 | FULL | Master region, size |
| PERI_MS_PPU_FX670_MS_ATT0 | 0x4002AFB0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX670_MS_ATT1 | 0x4002AFB4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX670_MS_ATT2 | 0x4002AFB8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX670_MS_ATT3 | 0x4002AFBC | FULL | Master attributes 3 |

## 23.688 PPU_FX 671

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX671_SL_ADDR | 0x4002AFC0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX671_SL_SIZE | 0x4002AFC4 | FULL | Slave region, size |
| PERI_MS_PPU_FX671_SL_ATT0 | 0x4002AFD0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX671_SL_ATT1 | 0x4002AFD4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX671_SL_ATT2 | 0x4002AFD8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX671_SL_ATT3 | 0x4002AFDC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX671_MS_ADDR | 0x4002AFE0 | FULL | Master region, base address |
| PERI_MS_PPU_FX671_MS_SIZE | 0x4002AFE4 | FULL | Master region, size |
| PERI_MS_PPU_FX671_MS_ATT0 | 0x4002AFF0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX671_MS_ATT1 | 0x4002AFF4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX671_MS_ATT2 | 0x4002AFF8 | FULL | Master attributes 2 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX671_MS_ATT3 | 0x4002AFFC | FULL | Master attributes 3 |

## 23.689 PPU_FX 672

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX672_SL_ADDR | 0x4002B000 | FULL | Slave region, base address |
| PERI_MS_PPU_FX672_SL_SIZE | 0x4002B004 | FULL | Slave region, size |
| PERI_MS_PPU_FX672_SL_ATT0 | 0x4002B010 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX672_SL_ATT1 | 0x4002B014 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX672_SL_ATT2 | 0x4002B018 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX672_SL_ATT3 | 0x4002B01C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX672_MS_ADDR | 0x4002B020 | FULL | Master region, base address |
| PERI_MS_PPU_FX672_MS_SIZE | 0x4002B024 | FULL | Master region, size |
| PERI_MS_PPU_FX672_MS_ATT0 | 0x4002B030 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX672_MS_ATT1 | 0x4002B034 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX672_MS_ATT2 | 0x4002B038 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX672_MS_ATT3 | 0x4002B03C | FULL | Master attributes 3 |

## 23.690 PPU_FX 673

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX673_SL_ADDR | 0x4002B040 | FULL | Slave region, base address |
| PERI_MS_PPU_FX673_SL_SIZE | 0x4002B044 | FULL | Slave region, size |
| PERI_MS_PPU_FX673_SL_ATT0 | 0x4002B050 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX673_SL_ATT1 | 0x4002B054 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX673_SL_ATT2 | 0x4002B058 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX673_SL_ATT3 | 0x4002B05C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX673_MS_ADDR | 0x4002B060 | FULL | Master region, base address |
| PERI_MS_PPU_FX673_MS_SIZE | 0x4002B064 | FULL | Master region, size |
| PERI_MS_PPU_FX673_MS_ATT0 | 0x4002B070 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX673_MS_ATT1 | 0x4002B074 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX673_MS_ATT2 | 0x4002B078 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX673_MS_ATT3 | 0x4002B07C | FULL | Master attributes 3 |

## 23.691 PPU_FX 674

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX674_SL_ADDR | 0x4002B080 | FULL | Slave region, base address |
| PERI_MS_PPU_FX674_SL_SIZE | 0x4002B084 | FULL | Slave region, size |
| PERI_MS_PPU_FX674_SL_ATT0 | 0x4002B090 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX674_SL_ATT1 | 0x4002B094 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX674_SL_ATT2 | 0x4002B098 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX674_SL_ATT3 | 0x4002B09C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX674_MS_ADDR | 0x4002B0A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX674_MS_SIZE | 0x4002B0A4 | FULL | Master region, size |
| PERI_MS_PPU_FX674_MS_ATT0 | 0x4002B0B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX674_MS_ATT1 | 0x4002B0B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX674_MS_ATT2 | 0x4002B0B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX674_MS_ATT3 | 0x4002B0BC | FULL | Master attributes 3 |

## 23.692 PPU_FX 675

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX675_SL_ADDR | 0x4002B0C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX675_SL_SIZE | 0x4002B0C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX675_SL_ATT0 | 0x4002B0D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX675_SL_ATT1 | 0x4002B0D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX675_SL_ATT2 | 0x4002B0D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX675_SL_ATT3 | 0x4002B0DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX675_MS_ADDR | 0x4002B0E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX675_MS_SIZE | 0x4002B0E4 | FULL | Master region, size |
| PERI_MS_PPU_FX675_MS_ATT0 | 0x4002B0F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX675_MS_ATT1 | 0x4002B0F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX675_MS_ATT2 | 0x4002B0F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX675_MS_ATT3 | 0x4002B0FC | FULL | Master attributes 3 |

## 23.693 PPU_FX 676

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX676_SL_ADDR | 0x4002B100 | FULL | Slave region, base address |
| PERI_MS_PPU_FX676_SL_SIZE | 0x4002B104 | FULL | Slave region, size |
| PERI_MS_PPU_FX676_SL_ATT0 | 0x4002B110 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX676_SL_ATT1 | 0x4002B114 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX676_SL_ATT2 | 0x4002B118 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX676_SL_ATT3 | 0x4002B11C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX676_MS_ADDR | 0x4002B120 | FULL | Master region, base address |
| PERI_MS_PPU_FX676_MS_SIZE | 0x4002B124 | FULL | Master region, size |
| PERI_MS_PPU_FX676_MS_ATT0 | 0x4002B130 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX676_MS_ATT1 | 0x4002B134 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX676_MS_ATT2 | 0x4002B138 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX676_MS_ATT3 | 0x4002B13C | FULL | Master attributes 3 |

## 23.694 PPU_FX 677

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX677_SL_ADDR | 0x4002B140 | FULL | Slave region, base address |
| PERI_MS_PPU_FX677_SL_SIZE | 0x4002B144 | FULL | Slave region, size |
| PERI_MS_PPU_FX677_SL_ATT0 | 0x4002B150 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX677_SL_ATT1 | 0x4002B154 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX677_SL_ATT2 | 0x4002B158 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX677_SL_ATT3 | 0x4002B15C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX677_MS_ADDR | 0x4002B160 | FULL | Master region, base address |
| PERI_MS_PPU_FX677_MS_SIZE | 0x4002B164 | FULL | Master region, size |
| PERI_MS_PPU_FX677_MS_ATT0 | 0x4002B170 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX677_MS_ATT1 | 0x4002B174 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX677_MS_ATT2 | 0x4002B178 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX677_MS_ATT3 | 0x4002B17C | FULL | Master attributes 3 |

## 23.695 PPU_FX 678

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX678_SL_ADDR | 0x4002B180 | FULL | Slave region, base address |
| PERI_MS_PPU_FX678_SL_SIZE | 0x4002B184 | FULL | Slave region, size |
| PERI_MS_PPU_FX678_SL_ATT0 | 0x4002B190 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX678_SL_ATT1 | 0x4002B194 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX678_SL_ATT2 | 0x4002B198 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX678_SL_ATT3 | 0x4002B19C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX678_MS_ADDR | 0x4002B1A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX678_MS_SIZE | 0x4002B1A4 | FULL | Master region, size |
| PERI_MS_PPU_FX678_MS_ATT0 | 0x4002B1B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX678_MS_ATT1 | 0x4002B1B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX678_MS_ATT2 | 0x4002B1B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX678_MS_ATT3 | 0x4002B1BC | FULL | Master attributes 3 |

## 23.696 PPU_FX 679

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX679_SL_ADDR | 0x4002B1C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX679_SL_SIZE | 0x4002B1C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX679_SL_ATT0 | 0x4002B1D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX679_SL_ATT1 | 0x4002B1D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX679_SL_ATT2 | 0x4002B1D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX679_SL_ATT3 | 0x4002B1DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX679_MS_ADDR | 0x4002B1E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX679_MS_SIZE | 0x4002B1E4 | FULL | Master region, size |
| PERI_MS_PPU_FX679_MS_ATT0 | 0x4002B1F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX679_MS_ATT1 | 0x4002B1F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX679_MS_ATT2 | 0x4002B1F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX679_MS_ATT3 | 0x4002B1FC | FULL | Master attributes 3 |

## 23.697 PPU_FX 680

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX680_SL_ADDR | 0x4002B200 | FULL | Slave region, base address |
| PERI_MS_PPU_FX680_SL_SIZE | 0x4002B204 | FULL | Slave region, size |
| PERI_MS_PPU_FX680_SL_ATT0 | 0x4002B210 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX680_SL_ATT1 | 0x4002B214 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX680_SL_ATT2 | 0x4002B218 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX680_SL_ATT3 | 0x4002B21C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX680_MS_ADDR | 0x4002B220 | FULL | Master region, base address |
| PERI_MS_PPU_FX680_MS_SIZE | 0x4002B224 | FULL | Master region, size |
| PERI_MS_PPU_FX680_MS_ATT0 | 0x4002B230 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX680_MS_ATT1 | 0x4002B234 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX680_MS_ATT2 | 0x4002B238 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX680_MS_ATT3 | 0x4002B23C | FULL | Master attributes 3 |

## 23.698 PPU_FX 681

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX681_SL_ADDR | 0x4002B240 | FULL | Slave region, base address |
| PERI_MS_PPU_FX681_SL_SIZE | 0x4002B244 | FULL | Slave region, size |
| PERI_MS_PPU_FX681_SL_ATT0 | 0x4002B250 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX681_SL_ATT1 | 0x4002B254 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX681_SL_ATT2 | 0x4002B258 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX681_SL_ATT3 | 0x4002B25C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX681_MS_ADDR | 0x4002B260 | FULL | Master region, base address |
| PERI_MS_PPU_FX681_MS_SIZE | 0x4002B264 | FULL | Master region, size |
| PERI_MS_PPU_FX681_MS_ATT0 | 0x4002B270 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX681_MS_ATT1 | 0x4002B274 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX681_MS_ATT2 | 0x4002B278 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX681_MS_ATT3 | 0x4002B27C | FULL | Master attributes 3 |

## 23.699 PPU_FX 682

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX682_SL_ADDR | 0x4002B280 | FULL | Slave region, base address |
| PERI_MS_PPU_FX682_SL_SIZE | 0x4002B284 | FULL | Slave region, size |
| PERI_MS_PPU_FX682_SL_ATT0 | 0x4002B290 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX682_SL_ATT1 | 0x4002B294 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX682_SL_ATT2 | 0x4002B298 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX682_SL_ATT3 | 0x4002B29C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX682_MS_ADDR | 0x4002B2A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX682_MS_SIZE | 0x4002B2A4 | FULL | Master region, size |
| PERI_MS_PPU_FX682_MS_ATT0 | 0x4002B2B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX682_MS_ATT1 | 0x4002B2B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX682_MS_ATT2 | 0x4002B2B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX682_MS_ATT3 | 0x4002B2BC | FULL | Master attributes 3 |

## 23.700 PPU_FX 683

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX683_SL_ADDR | 0x4002B2C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX683_SL_SIZE | 0x4002B2C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX683_SL_ATT0 | 0x4002B2D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX683_SL_ATT1 | 0x4002B2D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX683_SL_ATT2 | 0x4002B2D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX683_SL_ATT3 | 0x4002B2DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX683_MS_ADDR | 0x4002B2E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX683_MS_SIZE | 0x4002B2E4 | FULL | Master region, size |
| PERI_MS_PPU_FX683_MS_ATT0 | 0x4002B2F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX683_MS_ATT1 | 0x4002B2F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX683_MS_ATT2 | 0x4002B2F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX683_MS_ATT3 | 0x4002B2FC | FULL | Master attributes 3 |

## 23.701 PPU_FX 684

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX684_SL_ADDR | 0x4002B300 | FULL | Slave region, base address |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX684_SL_SIZE | 0x4002B304 | FULL | Slave region, size |
| PERI_MS_PPU_FX684_SL_ATT0 | 0x4002B310 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX684_SL_ATT1 | 0x4002B314 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX684_SL_ATT2 | 0x4002B318 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX684_SL_ATT3 | 0x4002B31C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX684_MS_ADDR | 0x4002B320 | FULL | Master region, base address |
| PERI_MS_PPU_FX684_MS_SIZE | 0x4002B324 | FULL | Master region, size |
| PERI_MS_PPU_FX684_MS_ATT0 | 0x4002B330 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX684_MS_ATT1 | 0x4002B334 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX684_MS_ATT2 | 0x4002B338 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX684_MS_ATT3 | 0x4002B33C | FULL | Master attributes 3 |

## 23.702 PPU_FX 685

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX685_SL_ADDR | 0x4002B340 | FULL | Slave region, base address |
| PERI_MS_PPU_FX685_SL_SIZE | 0x4002B344 | FULL | Slave region, size |
| PERI_MS_PPU_FX685_SL_ATT0 | 0x4002B350 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX685_SL_ATT1 | 0x4002B354 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX685_SL_ATT2 | 0x4002B358 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX685_SL_ATT3 | 0x4002B35C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX685_MS_ADDR | 0x4002B360 | FULL | Master region, base address |
| PERI_MS_PPU_FX685_MS_SIZE | 0x4002B364 | FULL | Master region, size |
| PERI_MS_PPU_FX685_MS_ATT0 | 0x4002B370 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX685_MS_ATT1 | 0x4002B374 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX685_MS_ATT2 | 0x4002B378 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX685_MS_ATT3 | 0x4002B37C | FULL | Master attributes 3 |

## 23.703 PPU_FX 686

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX686_SL_ADDR | 0x4002B380 | FULL | Slave region, base address |
| PERI_MS_PPU_FX686_SL_SIZE | 0x4002B384 | FULL | Slave region, size |
| PERI_MS_PPU_FX686_SL_ATT0 | 0x4002B390 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX686_SL_ATT1 | 0x4002B394 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX686_SL_ATT2 | 0x4002B398 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX686_SL_ATT3 | 0x4002B39C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX686_MS_ADDR | 0x4002B3A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX686_MS_SIZE | 0x4002B3A4 | FULL | Master region, size |
| PERI_MS_PPU_FX686_MS_ATT0 | 0x4002B3B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX686_MS_ATT1 | 0x4002B3B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX686_MS_ATT2 | 0x4002B3B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX686_MS_ATT3 | 0x4002B3BC | FULL | Master attributes 3 |

## 23.704 PPU_FX 687

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX687_SL_ADDR | 0x4002B3C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX687_SL_SIZE | 0x4002B3C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX687_SL_ATT0 | 0x4002B3D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX687_SL_ATT1 | 0x4002B3D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX687_SL_ATT2 | 0x4002B3D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX687_SL_ATT3 | 0x4002B3DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX687_MS_ADDR | 0x4002B3E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX687_MS_SIZE | 0x4002B3E4 | FULL | Master region, size |
| PERI_MS_PPU_FX687_MS_ATT0 | 0x4002B3F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX687_MS_ATT1 | 0x4002B3F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX687_MS_ATT2 | 0x4002B3F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX687_MS_ATT3 | 0x4002B3FC | FULL | Master attributes 3 |

## 23.705 PPU_FX 688

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX688_SL_ADDR | 0x4002B400 | FULL | Slave region, base address |
| PERI_MS_PPU_FX688_SL_SIZE | 0x4002B404 | FULL | Slave region, size |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX688_SL_ATT0 | 0x4002B410 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX688_SL_ATT1 | 0x4002B414 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX688_SL_ATT2 | 0x4002B418 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX688_SL_ATT3 | 0x4002B41C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX688_MS_ADDR | 0x4002B420 | FULL | Master region, base address |
| PERI_MS_PPU_FX688_MS_SIZE | 0x4002B424 | FULL | Master region, size |
| PERI_MS_PPU_FX688_MS_ATT0 | 0x4002B430 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX688_MS_ATT1 | 0x4002B434 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX688_MS_ATT2 | 0x4002B438 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX688_MS_ATT3 | 0x4002B43C | FULL | Master attributes 3 |

## 23.706 PPU_FX 689

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX689_SL_ADDR | 0x4002B440 | FULL | Slave region, base address |
| PERI_MS_PPU_FX689_SL_SIZE | 0x4002B444 | FULL | Slave region, size |
| PERI_MS_PPU_FX689_SL_ATT0 | 0x4002B450 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX689_SL_ATT1 | 0x4002B454 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX689_SL_ATT2 | 0x4002B458 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX689_SL_ATT3 | 0x4002B45C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX689_MS_ADDR | 0x4002B460 | FULL | Master region, base address |
| PERI_MS_PPU_FX689_MS_SIZE | 0x4002B464 | FULL | Master region, size |
| PERI_MS_PPU_FX689_MS_ATT0 | 0x4002B470 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX689_MS_ATT1 | 0x4002B474 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX689_MS_ATT2 | 0x4002B478 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX689_MS_ATT3 | 0x4002B47C | FULL | Master attributes 3 |

## 23.707 PPU_FX 690

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX690_SL_ADDR | 0x4002B480 | FULL | Slave region, base address |
| PERI_MS_PPU_FX690_SL_SIZE | 0x4002B484 | FULL | Slave region, size |
| PERI_MS_PPU_FX690_SL_ATT0 | 0x4002B490 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX690_SL_ATT1 | 0x4002B494 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX690_SL_ATT2 | 0x4002B498 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX690_SL_ATT3 | 0x4002B49C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX690_MS_ADDR | 0x4002B4A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX690_MS_SIZE | 0x4002B4A4 | FULL | Master region, size |
| PERI_MS_PPU_FX690_MS_ATT0 | 0x4002B4B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX690_MS_ATT1 | 0x4002B4B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX690_MS_ATT2 | 0x4002B4B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX690_MS_ATT3 | 0x4002B4BC | FULL | Master attributes 3 |

## 23.708 PPU_FX 691

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX691_SL_ADDR | 0x4002B4C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX691_SL_SIZE | 0x4002B4C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX691_SL_ATT0 | 0x4002B4D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX691_SL_ATT1 | 0x4002B4D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX691_SL_ATT2 | 0x4002B4D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX691_SL_ATT3 | 0x4002B4DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX691_MS_ADDR | 0x4002B4E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX691_MS_SIZE | 0x4002B4E4 | FULL | Master region, size |
| PERI_MS_PPU_FX691_MS_ATT0 | 0x4002B4F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX691_MS_ATT1 | 0x4002B4F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX691_MS_ATT2 | 0x4002B4F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX691_MS_ATT3 | 0x4002B4FC | FULL | Master attributes 3 |

## 23.709 PPU_FX 692

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX692_SL_ADDR | 0x4002B500 | FULL | Slave region, base address |
| PERI_MS_PPU_FX692_SL_SIZE | 0x4002B504 | FULL | Slave region, size |
| PERI_MS_PPU_FX692_SL_ATT0 | 0x4002B510 | FULL | Slave attributes 0 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX692_SL_ATT1 | 0x4002B514 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX692_SL_ATT2 | 0x4002B518 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX692_SL_ATT3 | 0x4002B51C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX692_MS_ADDR | 0x4002B520 | FULL | Master region, base address |
| PERI_MS_PPU_FX692_MS_SIZE | 0x4002B524 | FULL | Master region, size |
| PERI_MS_PPU_FX692_MS_ATT0 | 0x4002B530 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX692_MS_ATT1 | 0x4002B534 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX692_MS_ATT2 | 0x4002B538 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX692_MS_ATT3 | 0x4002B53C | FULL | Master attributes 3 |

## 23.710 PPU_FX 693

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX693_SL_ADDR | 0x4002B540 | FULL | Slave region, base address |
| PERI_MS_PPU_FX693_SL_SIZE | 0x4002B544 | FULL | Slave region, size |
| PERI_MS_PPU_FX693_SL_ATT0 | 0x4002B550 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX693_SL_ATT1 | 0x4002B554 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX693_SL_ATT2 | 0x4002B558 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX693_SL_ATT3 | 0x4002B55C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX693_MS_ADDR | 0x4002B560 | FULL | Master region, base address |
| PERI_MS_PPU_FX693_MS_SIZE | 0x4002B564 | FULL | Master region, size |
| PERI_MS_PPU_FX693_MS_ATT0 | 0x4002B570 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX693_MS_ATT1 | 0x4002B574 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX693_MS_ATT2 | 0x4002B578 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX693_MS_ATT3 | 0x4002B57C | FULL | Master attributes 3 |

## 23.711 PPU_FX 694

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX694_SL_ADDR | 0x4002B580 | FULL | Slave region, base address |
| PERI_MS_PPU_FX694_SL_SIZE | 0x4002B584 | FULL | Slave region, size |
| PERI_MS_PPU_FX694_SL_ATT0 | 0x4002B590 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX694_SL_ATT1 | 0x4002B594 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX694_SL_ATT2 | 0x4002B598 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX694_SL_ATT3 | 0x4002B59C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX694_MS_ADDR | 0x4002B5A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX694_MS_SIZE | 0x4002B5A4 | FULL | Master region, size |
| PERI_MS_PPU_FX694_MS_ATT0 | 0x4002B5B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX694_MS_ATT1 | 0x4002B5B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX694_MS_ATT2 | 0x4002B5B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX694_MS_ATT3 | 0x4002B5BC | FULL | Master attributes 3 |

## 23.712 PPU_FX 695

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX695_SL_ADDR | 0x4002B5C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX695_SL_SIZE | 0x4002B5C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX695_SL_ATT0 | 0x4002B5D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX695_SL_ATT1 | 0x4002B5D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX695_SL_ATT2 | 0x4002B5D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX695_SL_ATT3 | 0x4002B5DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX695_MS_ADDR | 0x4002B5E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX695_MS_SIZE | 0x4002B5E4 | FULL | Master region, size |
| PERI_MS_PPU_FX695_MS_ATT0 | 0x4002B5F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX695_MS_ATT1 | 0x4002B5F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX695_MS_ATT2 | 0x4002B5F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX695_MS_ATT3 | 0x4002B5FC | FULL | Master attributes 3 |

## 23.713 PPU_FX 696

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX696_SL_ADDR | 0x4002B600 | FULL | Slave region, base address |
| PERI_MS_PPU_FX696_SL_SIZE | 0x4002B604 | FULL | Slave region, size |
| PERI_MS_PPU_FX696_SL_ATT0 | 0x4002B610 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX696_SL_ATT1 | 0x4002B614 | FULL | Slave attributes 1 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX696_SL_ATT2 | 0x4002B618 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX696_SL_ATT3 | 0x4002B61C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX696_MS_ADDR | 0x4002B620 | FULL | Master region, base address |
| PERI_MS_PPU_FX696_MS_SIZE | 0x4002B624 | FULL | Master region, size |
| PERI_MS_PPU_FX696_MS_ATT0 | 0x4002B630 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX696_MS_ATT1 | 0x4002B634 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX696_MS_ATT2 | 0x4002B638 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX696_MS_ATT3 | 0x4002B63C | FULL | Master attributes 3 |

## 23.714 PPU_FX 697

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX697_SL_ADDR | 0x4002B640 | FULL | Slave region, base address |
| PERI_MS_PPU_FX697_SL_SIZE | 0x4002B644 | FULL | Slave region, size |
| PERI_MS_PPU_FX697_SL_ATT0 | 0x4002B650 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX697_SL_ATT1 | 0x4002B654 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX697_SL_ATT2 | 0x4002B658 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX697_SL_ATT3 | 0x4002B65C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX697_MS_ADDR | 0x4002B660 | FULL | Master region, base address |
| PERI_MS_PPU_FX697_MS_SIZE | 0x4002B664 | FULL | Master region, size |
| PERI_MS_PPU_FX697_MS_ATT0 | 0x4002B670 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX697_MS_ATT1 | 0x4002B674 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX697_MS_ATT2 | 0x4002B678 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX697_MS_ATT3 | 0x4002B67C | FULL | Master attributes 3 |

## 23.715 PPU_FX 698

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX698_SL_ADDR | 0x4002B680 | FULL | Slave region, base address |
| PERI_MS_PPU_FX698_SL_SIZE | 0x4002B684 | FULL | Slave region, size |
| PERI_MS_PPU_FX698_SL_ATT0 | 0x4002B690 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX698_SL_ATT1 | 0x4002B694 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX698_SL_ATT2 | 0x4002B698 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX698_SL_ATT3 | 0x4002B69C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX698_MS_ADDR | 0x4002B6A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX698_MS_SIZE | 0x4002B6A4 | FULL | Master region, size |
| PERI_MS_PPU_FX698_MS_ATT0 | 0x4002B6B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX698_MS_ATT1 | 0x4002B6B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX698_MS_ATT2 | 0x4002B6B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX698_MS_ATT3 | 0x4002B6BC | FULL | Master attributes 3 |

## 23.716 PPU_FX 699

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX699_SL_ADDR | 0x4002B6C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX699_SL_SIZE | 0x4002B6C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX699_SL_ATT0 | 0x4002B6D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX699_SL_ATT1 | 0x4002B6D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX699_SL_ATT2 | 0x4002B6D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX699_SL_ATT3 | 0x4002B6DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX699_MS_ADDR | 0x4002B6E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX699_MS_SIZE | 0x4002B6E4 | FULL | Master region, size |
| PERI_MS_PPU_FX699_MS_ATT0 | 0x4002B6F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX699_MS_ATT1 | 0x4002B6F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX699_MS_ATT2 | 0x4002B6F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX699_MS_ATT3 | 0x4002B6FC | FULL | Master attributes 3 |

## 23.717 PPU_FX 700

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX700_SL_ADDR | 0x4002B700 | FULL | Slave region, base address |
| PERI_MS_PPU_FX700_SL_SIZE | 0x4002B704 | FULL | Slave region, size |
| PERI_MS_PPU_FX700_SL_ATT0 | 0x4002B710 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX700_SL_ATT1 | 0x4002B714 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX700_SL_ATT2 | 0x4002B718 | FULL | Slave attributes 2 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX700_SL_ATT3 | 0x4002B71C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX700_MS_ADDR | 0x4002B720 | FULL | Master region, base address |
| PERI_MS_PPU_FX700_MS_SIZE | 0x4002B724 | FULL | Master region, size |
| PERI_MS_PPU_FX700_MS_ATT0 | 0x4002B730 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX700_MS_ATT1 | 0x4002B734 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX700_MS_ATT2 | 0x4002B738 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX700_MS_ATT3 | 0x4002B73C | FULL | Master attributes 3 |

## 23.718 PPU_FX 701

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_MS_PPU_FX701_SL_ADDR | 0x4002B740 | FULL | Slave region, base address |
| PERI_MS_PPU_FX701_SL_SIZE | 0x4002B744 | FULL | Slave region, size |
| PERI_MS_PPU_FX701_SL_ATT0 | 0x4002B750 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX701_SL_ATT1 | 0x4002B754 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX701_SL_ATT2 | 0x4002B758 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX701_SL_ATT3 | 0x4002B75C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX701_MS_ADDR | 0x4002B760 | FULL | Master region, base address |
| PERI_MS_PPU_FX701_MS_SIZE | 0x4002B764 | FULL | Master region, size |
| PERI_MS_PPU_FX701_MS_ATT0 | 0x4002B770 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX701_MS_ATT1 | 0x4002B774 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX701_MS_ATT2 | 0x4002B778 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX701_MS_ATT3 | 0x4002B77C | FULL | Master attributes 3 |

## 23.719 Register Details

### 23.719.1 PPU_PR

#### 23.719.1.1 PERI_MS_PPU_PR_SL_ADDR

**Description:** Slave region, base address
**Address:** 0x40020000
**Offset:** 0x0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** SL_ADDR can only be written by protection context '0' (protection context '0' has unrestricted access). The access privileges for other protection contexts are determined by MS_ATT0, ..., MS_ATT3, with the additional restriction that SL_ADDR can NOT be written.

Typically, the SL_ADDR and SL_SIZE registers are programmed by the boot process with protection context '0'.
**Default:** Undefined as one or more bit fields have a default value that is undefined

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDR30 [7:2] | | | | | | None [1:0] | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDR30 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDR30 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDR30 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 2:31 | ADDR30 | RW | R | Undefined | This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is '15') must be 64 KByte aligned, and ADDR30[13:0] must be '0's. |

### 23.719.1.2 PERI_MS_PPU_PR_SL_SIZE

**Description:** Slave region, size
**Address:** 0x40020004
**Offset:** 0x4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** SL_SIZE can only be written by protection context '0' (protection context '0' has unrestricted access). The access privileges for other protection contexts are determined by MS_ATT0, ..., MS_ATT3, with the additional restriction that SL_SIZE can NOT be written.
**Default:** Undefined as one or more bit fields have a default value that is undefined

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALID [31:31] | None [30:29] | | REGION_SIZE [28:24] | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 24:28 | REGION_SIZE | RW | R | Undefined | This field specifies the size of the slave region:<br>'0': Undefined.<br>'1': 4 B region (this is the smallest region size).<br>'2': 8 B region<br>'3': 16 B region<br>'4': 32 B region<br>'5': 64 B region<br>'6': 128 B region<br>'7': 256 B region<br>'8': 512 B region<br>'9': 1 KB region<br>'10': 2 KB region<br>'11': 4 KB region<br>'12': 8 KB region<br>'13': 16 KB region<br>'14': 32 KB region<br>'15': 64 KB region<br>'16': 128 KB region<br>'17': 256 KB region<br>'18': 512 KB region<br>'19': 1 MB region<br>'20': 2 MB region<br>'21': 4 MB region<br>'22': 8 MB region<br>'23': 16 MB region<br>'24': 32 MB region<br>'25': 64 MB region<br>'26': 128 MB region<br>'27': 256 MB region<br>'28': 512 MB region<br>'29': 1 GB region<br>'30': 2 GB region<br>'31': 4 GB region |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 31 | VALID | RW | R | 0 | Slave region enable:<br>'0': Disabled. A disabled region will never result in a match on the transfer address.<br>'1': Enabled. |

### 23.719.1.3 PERI_MS_PPU_PR_SL_ATT0

**Description:** Slave attributes 0
**Address:** 0x40020010
**Offset:** 0x10
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** The access privileges for SL_ATT0, ..., SL_ATT3 are determined by MS_ATT0, ..., MS_ATT3.

Note that protection context '0' has unrestricted access: PC0_UR, ..., PC0_NS fields are fixed to '1's. The other protection contexts have SW programmable fields.

Typically, the SL_ATT0, ..., SL_ATT3 registers are initialized by the boot process with protection context '0'.

For 4 or less protection contexts (PC_NR <= 4), only SL_ATT0 is present. For 5 through 8 protection contexts, only SL_ATT0 and SL_ATT1 are present. For 9 through 12 or less protection contexts, only SL_ATT0, SL_ATT1 and SL_ATT2 are present. For 13 through 16 protection contexts, SL_ATT0, SL_ATT1, SL_ATT2 and SL_ATT3 are all present. If the number of protection contexts is not a multiple of 4, the 'missing' protection contexts in a register have no associated access fields (and the field positions read as '0').

**Default:** 0x1F1F1F1F

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:5] | | | PC0_NS [4:4] | PC0_PW [3:3] | PC0_PR [2:2] | PC0_UW [1:1] | PC0_UR [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:13] | | | PC1_NS [12:12] | PC1_PW [11:11] | PC1_PR [10:10] | PC1_UW [9:9] | PC1_UR [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:21] | | | PC2_NS [20:20] | PC2_PW [19:19] | PC2_PR [18:18] | PC2_UW [17:17] | PC2_UR [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:29] | | | PC3_NS [28:28] | PC3_PW [27:27] | PC3_PR [26:26] | PC3_UW [25:25] | PC3_UR [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | PC0_UR | R | R | 1 | Protection context 0, user read enable:<br>'0': Disabled (user, read accesses are NOT allowed).<br>'1': Enabled (user, read accesses are allowed). |
| 1 | PC0_UW | R | R | 1 | Protection context 0, user write enable:<br>'0': Disabled (user, write accesses are NOT allowed).<br>'1': Enabled (user, write accesses are allowed). |
| 2 | PC0_PR | R | R | 1 | Protection context 0, privileged read enable:<br>'0': Disabled (privileged, read accesses are NOT allowed).<br>'1': Enabled (privileged, read accesses are allowed). |
| 3 | PC0_PW | R | R | 1 | Protection context 0, privileged write enable:<br>'0': Disabled (privileged, write accesses are NOT allowed).<br>'1': Enabled (privileged, write accesses are allowed). |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 4 | PC0_NS | R | R | 1 | Protection context 0, non-secure:<br>'0': Secure (secure accesses allowed, non-secure access NOT allowed).<br>'1': Non-secure (both secure and non-secure accesses allowed). |
| 8 | PC1_UR | RW | R | 1 | Protection context 1, user read enable. |
| 9 | PC1_UW | RW | R | 1 | Protection context 1, user write enable. |
| 10 | PC1_PR | RW | R | 1 | Protection context 1, privileged read enable. |
| 11 | PC1_PW | RW | R | 1 | Protection context 1, privileged write enable. |
| 12 | PC1_NS | RW | R | 1 | Protection context 1, non-secure. |
| 16 | PC2_UR | RW | R | 1 | Protection context 2, user read enable. |
| 17 | PC2_UW | RW | R | 1 | Protection context 2, user write enable. |
| 18 | PC2_PR | RW | R | 1 | Protection context 2, privileged read enable. |
| 19 | PC2_PW | RW | R | 1 | Protection context 2, privileged write enable. |
| 20 | PC2_NS | RW | R | 1 | Protection context 2, non-secure. |
| 24 | PC3_UR | RW | R | 1 | Protection context 3, user read enable. |
| 25 | PC3_UW | RW | R | 1 | Protection context 3, user write enable. |
| 26 | PC3_PR | RW | R | 1 | Protection context 3, privileged read enable. |
| 27 | PC3_PW | RW | R | 1 | Protection context 3, privileged write enable. |
| 28 | PC3_NS | RW | R | 1 | Protection context 3, non-secure. |

### 23.719.1.4 PERI_MS_PPU_PR_SL_ATT1

**Description:** Slave attributes 1
**Address:** 0x40020014
**Offset:** 0x14
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x1F1F1F1F

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:5] | | | PC4_NS [4:4] | PC4_PW [3:3] | PC4_PR [2:2] | PC4_UW [1:1] | PC4_UR [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:13] | | | PC5_NS [12:12] | PC5_PW [11:11] | PC5_PR [10:10] | PC5_UW [9:9] | PC5_UR [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:21] | | | PC6_NS [20:20] | PC6_PW [19:19] | PC6_PR [18:18] | PC6_UW [17:17] | PC6_UR [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:29] | | | PC7_NS [28:28] | PC7_PW [27:27] | PC7_PR [26:26] | PC7_UW [25:25] | PC7_UR [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | PC4_UR | RW | R | 1 | Protection context 4, user read enable. |
| 1 | PC4_UW | RW | R | 1 | Protection context 4, user write enable. |
| 2 | PC4_PR | RW | R | 1 | Protection context 4, privileged read enable. |
| 3 | PC4_PW | RW | R | 1 | Protection context 4, privileged write enable. |
| 4 | PC4_NS | RW | R | 1 | Protection context 4, non-secure. |
| 8 | PC5_UR | RW | R | 1 | Protection context 5, user read enable. |
| 9 | PC5_UW | RW | R | 1 | Protection context 5, user write enable. |
| 10 | PC5_PR | RW | R | 1 | Protection context 5, privileged read enable. |
| 11 | PC5_PW | RW | R | 1 | Protection context 5, privileged write enable. |
| 12 | PC5_NS | RW | R | 1 | Protection context 5, non-secure. |
| 16 | PC6_UR | RW | R | 1 | Protection context 6, user read enable. |
| 17 | PC6_UW | RW | R | 1 | Protection context 6, user write enable. |
| 18 | PC6_PR | RW | R | 1 | Protection context 6, privileged read enable. |
| 19 | PC6_PW | RW | R | 1 | Protection context 6, privileged write enable. |
| 20 | PC6_NS | RW | R | 1 | Protection context 6, non-secure. |
| 24 | PC7_UR | RW | R | 1 | Protection context 7, user read enable. |
| 25 | PC7_UW | RW | R | 1 | Protection context 7, user write enable. |
| 26 | PC7_PR | RW | R | 1 | Protection context 7, privileged read enable. |
| 27 | PC7_PW | RW | R | 1 | Protection context 7, privileged write enable. |
| 28 | PC7_NS | RW | R | 1 | Protection context 7, non-secure. |

### 23.719.1.5 PERI_MS_PPU_PR_SL_ATT2

**Description:** Slave attributes 2
**Address:** 0x40020018
**Offset:** 0x18
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x1F1F1F1F

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:5] | | | PC8_NS [4:4] | PC8_PW [3:3] | PC8_PR [2:2] | PC8_UW [1:1] | PC8_UR [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:13] | | | PC9_NS [12:12] | PC9_PW [11:11] | PC9_PR [10:10] | PC9_UW [9:9] | PC9_UR [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:21] | | | PC10_NS [20:20] | PC10_PW [19:19] | PC10_PR [18:18] | PC10_UW [17:17] | PC10_UR [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:29] | | | PC11_NS [28:28] | PC11_PW [27:27] | PC11_PR [26:26] | PC11_UW [25:25] | PC11_UR [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | PC8_UR | RW | R | 1 | Protection context 8, user read enable. |
| 1 | PC8_UW | RW | R | 1 | Protection context 8, user write enable. |
| 2 | PC8_PR | RW | R | 1 | Protection context 8, privileged read enable. |
| 3 | PC8_PW | RW | R | 1 | Protection context 8, privileged write enable. |
| 4 | PC8_NS | RW | R | 1 | Protection context 8, non-secure. |
| 8 | PC9_UR | RW | R | 1 | Protection context 9, user read enable. |
| 9 | PC9_UW | RW | R | 1 | Protection context 9, user write enable. |
| 10 | PC9_PR | RW | R | 1 | Protection context 9, privileged read enable. |
| 11 | PC9_PW | RW | R | 1 | Protection context 9, privileged write enable. |
| 12 | PC9_NS | RW | R | 1 | Protection context 9, non-secure. |
| 16 | PC10_UR | RW | R | 1 | Protection context 10, user read enable. |
| 17 | PC10_UW | RW | R | 1 | Protection context 10, user write enable. |
| 18 | PC10_PR | RW | R | 1 | Protection context 10, privileged read enable. |
| 19 | PC10_PW | RW | R | 1 | Protection context 10, privileged write enable. |
| 20 | PC10_NS | RW | R | 1 | Protection context 10, non-secure. |
| 24 | PC11_UR | RW | R | 1 | Protection context 11, user read enable. |
| 25 | PC11_UW | RW | R | 1 | Protection context 11, user write enable. |
| 26 | PC11_PR | RW | R | 1 | Protection context 11, privileged read enable. |
| 27 | PC11_PW | RW | R | 1 | Protection context 11, privileged write enable. |
| 28 | PC11_NS | RW | R | 1 | Protection context 11, non-secure. |

### 23.719.1.6 PERI_MS_PPU_PR_SL_ATT3

**Description:** Slave attributes 3
**Address:** 0x4002001C
**Offset:** 0x1C
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x1F1F1F1F

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:5] | | | PC12_NS [4:4] | PC12_PW [3:3] | PC12_PR [2:2] | PC12_UW [1:1] | PC12_UR [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:13] | | | PC13_NS [12:12] | PC13_PW [11:11] | PC13_PR [10:10] | PC13_UW [9:9] | PC13_UR [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:21] | | | PC14_NS [20:20] | PC14_PW [19:19] | PC14_PR [18:18] | PC14_UW [17:17] | PC14_UR [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:29] | | | PC15_NS [28:28] | PC15_PW [27:27] | PC15_PR [26:26] | PC15_UW [25:25] | PC15_UR [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | PC12_UR | RW | R | 1 | Protection context 12, user read enable. |
| 1 | PC12_UW | RW | R | 1 | Protection context 12, user write enable. |
| 2 | PC12_PR | RW | R | 1 | Protection context 12, privileged read enable. |
| 3 | PC12_PW | RW | R | 1 | Protection context 12, privileged write enable. |
| 4 | PC12_NS | RW | R | 1 | Protection context 12, non-secure. |
| 8 | PC13_UR | RW | R | 1 | Protection context 13, user read enable. |
| 9 | PC13_UW | RW | R | 1 | Protection context 13, user write enable. |
| 10 | PC13_PR | RW | R | 1 | Protection context 13, privileged read enable. |
| 11 | PC13_PW | RW | R | 1 | Protection context 13, privileged write enable. |
| 12 | PC13_NS | RW | R | 1 | Protection context 13, non-secure. |
| 16 | PC14_UR | RW | R | 1 | Protection context 14, user read enable. |
| 17 | PC14_UW | RW | R | 1 | Protection context 14, user write enable. |
| 18 | PC14_PR | RW | R | 1 | Protection context 14, privileged read enable. |
| 19 | PC14_PW | RW | R | 1 | Protection context 14, privileged write enable. |
| 20 | PC14_NS | RW | R | 1 | Protection context 14, non-secure. |
| 24 | PC15_UR | RW | R | 1 | Protection context 15, user read enable. |
| 25 | PC15_UW | RW | R | 1 | Protection context 15, user write enable. |
| 26 | PC15_PR | RW | R | 1 | Protection context 15, privileged read enable. |
| 27 | PC15_PW | RW | R | 1 | Protection context 15, privileged write enable. |
| 28 | PC15_NS | RW | R | 1 | Protection context 15, non-secure. |

### 23.719.1.7 PERI_MS_PPU_PR_MS_ADDR

**Description:** Master region, base address
**Address:** 0x40020020
**Offset:** 0x20
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** MS_ADDR is fixed (non-programmable).

The access privileges for MS_ADDR are determined by MS_ATT0, ..., MS_ATT3.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDR26 [7:6] | | None [5:0] | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDR26 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDR26 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDR26 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 6:31 | ADDR26 | R | R | 16779264 | This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. |

### 23.719.1.8 PERI_MS_PPU_PR_MS_SIZE

**Description:** Master region, size
**Address:** 0x40020024
**Offset:** 0x24
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** MS_SIZE is fixed (non-programmable).

The access privileges for MS_SIZE are determined by MS_ATT0, ..., MS_ATT3.
**Default:** 0x85000000

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALID [31:31] | None [30:29] | | REGION_SIZE [28:24] | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 24:28 | REGION_SIZE | R | R | 5 | This field specifies the size of the master region:<br>'5': 64 B region<br><br>The master region includes the SL_ADDR, SL_SIZE, SL_ATT0, ..., SL_ATT3, MS_ADDR, MS_SIZE, MS_ATT0, ..., MS_ATT3 registers. Therefore, the access privileges for all these registers is determined by MS_ATT0, ..., MS_ATT3. |
| 31 | VALID | R | R | 1 | Master region enable:<br>'1': Enabled. |

### 23.719.1.9 PERI_MS_PPU_PR_MS_ATT0

**Description:** Master attributes 0
**Address:** 0x40020030
**Offset:** 0x30
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** The access privileges for MS_ATT0, ..., MS_ATT3 are determined by MS_ATT0, ..., MS_ATT3.

Note that protection context '0' has unrestricted access: PC0_UR, ..., PC0_NS fields are fixed to '1's. The other protection contexts have SW programmable fields.

Typically, the MS_ATT0, ..., MS_ATT3 registers are programmed by the boot process with protection context '0'.
**Default:** 0x1F1F1F1F

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:5] | | | PC0_NS [4:4] | PC0_PW [3:3] | PC0_PR [2:2] | PC0_UW [1:1] | PC0_UR [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:13] | | | PC1_NS [12:12] | PC1_PW [11:11] | PC1_PR [10:10] | PC1_UW [9:9] | PC1_UR [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:21] | | | PC2_NS [20:20] | PC2_PW [19:19] | PC2_PR [18:18] | PC2_UW [17:17] | PC2_UR [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:29] | | | PC3_NS [28:28] | PC3_PW [27:27] | PC3_PR [26:26] | PC3_UW [25:25] | PC3_UR [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | PC0_UR | R | R | 1 | Protection context 0, user read enable:<br>'0': Disabled (user, read accesses are NOT allowed).<br>'1': Enabled (user, read accesses are allowed). |
| 1 | PC0_UW | R | R | 1 | Protection context 0, user write enable:<br>'0': Disabled (user, write accesses are NOT allowed).<br>'1': Enabled (user, write accesses are allowed). |
| 2 | PC0_PR | R | R | 1 | Protection context 0, privileged read enable:<br>'0': Disabled (privileged, read accesses are NOT allowed).<br>'1': Enabled (privileged, read accesses are allowed). |
| 3 | PC0_PW | R | R | 1 | Protection context 0, privileged write enable:<br>'0': Disabled (privileged, write accesses are NOT allowed).<br>'1': Enabled (privileged, write accesses are allowed). |
| 4 | PC0_NS | R | R | 1 | Protection context 0, non-secure:<br>'0': Secure (secure accesses allowed, non-secure access NOT allowed).<br>'1': Non-secure (both secure and non-secure accesses allowed). |
| 8 | PC1_UR | R | R | 1 | Protection context 1, user read enable. |
| 9 | PC1_UW | RW | R | 1 | Protection context 1, user write enable. |
| 10 | PC1_PR | R | R | 1 | Protection context 1, privileged read enable. |
| 11 | PC1_PW | RW | R | 1 | Protection context 1, privileged write enable. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 12 | PC1_NS | RW | R | 1 | Protection context 1, non-secure. |
| 16 | PC2_UR | R | R | 1 | Protection context 2, user read enable. |
| 17 | PC2_UW | RW | R | 1 | Protection context 2, user write enable. |
| 18 | PC2_PR | R | R | 1 | Protection context 2, privileged read enable. |
| 19 | PC2_PW | RW | R | 1 | Protection context 2, privileged write enable. |
| 20 | PC2_NS | RW | R | 1 | Protection context 2, non-secure. |
| 24 | PC3_UR | R | R | 1 | Protection context 3, user read enable. |
| 25 | PC3_UW | RW | R | 1 | Protection context 3, user write enable. |
| 26 | PC3_PR | R | R | 1 | Protection context 3, privileged read enable. |
| 27 | PC3_PW | RW | R | 1 | Protection context 3, privileged write enable. |
| 28 | PC3_NS | RW | R | 1 | Protection context 3, non-secure. |

### 23.719.1.10 PERI_MS_PPU_PR_MS_ATT1

**Description:** Master attributes 1
**Address:** 0x40020034
**Offset:** 0x34
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x1F1F1F1F

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:5] | | | PC4_NS [4:4] | PC4_PW [3:3] | PC4_PR [2:2] | PC4_UW [1:1] | PC4_UR [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:13] | | | PC5_NS [12:12] | PC5_PW [11:11] | PC5_PR [10:10] | PC5_UW [9:9] | PC5_UR [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:21] | | | PC6_NS [20:20] | PC6_PW [19:19] | PC6_PR [18:18] | PC6_UW [17:17] | PC6_UR [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:29] | | | PC7_NS [28:28] | PC7_PW [27:27] | PC7_PR [26:26] | PC7_UW [25:25] | PC7_UR [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | PC4_UR | R | R | 1 | Protection context 4, user read enable. |
| 1 | PC4_UW | RW | R | 1 | Protection context 4, user write enable. |
| 2 | PC4_PR | R | R | 1 | Protection context 4, privileged read enable. |
| 3 | PC4_PW | RW | R | 1 | Protection context 4, privileged write enable. |
| 4 | PC4_NS | RW | R | 1 | Protection context 4, non-secure. |
| 8 | PC5_UR | R | R | 1 | Protection context 5, user read enable. |
| 9 | PC5_UW | RW | R | 1 | Protection context 5, user write enable. |
| 10 | PC5_PR | R | R | 1 | Protection context 5, privileged read enable. |
| 11 | PC5_PW | RW | R | 1 | Protection context 5, privileged write enable. |
| 12 | PC5_NS | RW | R | 1 | Protection context 5, non-secure. |
| 16 | PC6_UR | R | R | 1 | Protection context 6, user read enable. |
| 17 | PC6_UW | RW | R | 1 | Protection context 6, user write enable. |
| 18 | PC6_PR | R | R | 1 | Protection context 6, privileged read enable. |
| 19 | PC6_PW | RW | R | 1 | Protection context 6, privileged write enable. |
| 20 | PC6_NS | RW | R | 1 | Protection context 6, non-secure. |
| 24 | PC7_UR | R | R | 1 | Protection context 7, user read enable. |
| 25 | PC7_UW | RW | R | 1 | Protection context 7, user write enable. |
| 26 | PC7_PR | R | R | 1 | Protection context 7, privileged read enable. |
| 27 | PC7_PW | RW | R | 1 | Protection context 7, privileged write enable. |
| 28 | PC7_NS | RW | R | 1 | Protection context 7, non-secure. |

### 23.719.1.11 PERI_MS_PPU_PR_MS_ATT2

**Description:** Master attributes 2
**Address:** 0x40020038
**Offset:** 0x38
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x1F1F1F1F

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:5] | | | PC8_NS [4:4] | PC8_PW [3:3] | PC8_PR [2:2] | PC8_UW [1:1] | PC8_UR [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:13] | | | PC9_NS [12:12] | PC9_PW [11:11] | PC9_PR [10:10] | PC9_UW [9:9] | PC9_UR [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:21] | | | PC10_NS [20:20] | PC10_PW [19:19] | PC10_PR [18:18] | PC10_UW [17:17] | PC10_UR [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:29] | | | PC11_NS [28:28] | PC11_PW [27:27] | PC11_PR [26:26] | PC11_UW [25:25] | PC11_UR [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | PC8_UR | R | R | 1 | Protection context 8, user read enable. |
| 1 | PC8_UW | RW | R | 1 | Protection context 8, user write enable. |
| 2 | PC8_PR | R | R | 1 | Protection context 8, privileged read enable. |
| 3 | PC8_PW | RW | R | 1 | Protection context 8, privileged write enable. |
| 4 | PC8_NS | RW | R | 1 | Protection context 8, non-secure. |
| 8 | PC9_UR | R | R | 1 | Protection context 9, user read enable. |
| 9 | PC9_UW | RW | R | 1 | Protection context 9, user write enable. |
| 10 | PC9_PR | R | R | 1 | Protection context 9, privileged read enable. |
| 11 | PC9_PW | RW | R | 1 | Protection context 9, privileged write enable. |
| 12 | PC9_NS | RW | R | 1 | Protection context 9, non-secure. |
| 16 | PC10_UR | R | R | 1 | Protection context 10, user read enable. |
| 17 | PC10_UW | RW | R | 1 | Protection context 10, user write enable. |
| 18 | PC10_PR | R | R | 1 | Protection context 10, privileged read enable. |
| 19 | PC10_PW | RW | R | 1 | Protection context 10, privileged write enable. |
| 20 | PC10_NS | RW | R | 1 | Protection context 10, non-secure. |
| 24 | PC11_UR | R | R | 1 | Protection context 11, user read enable. |
| 25 | PC11_UW | RW | R | 1 | Protection context 11, user write enable. |
| 26 | PC11_PR | R | R | 1 | Protection context 11, privileged read enable. |
| 27 | PC11_PW | RW | R | 1 | Protection context 11, privileged write enable. |
| 28 | PC11_NS | RW | R | 1 | Protection context 11, non-secure. |

### 23.719.1.12 PERI_MS_PPU_PR_MS_ATT3

**Description:** Master attributes 3
**Address:** 0x4002003C
**Offset:** 0x3C
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x1F1F1F1F

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:5] | | | PC12_NS [4:4] | PC12_PW [3:3] | PC12_PR [2:2] | PC12_UW [1:1] | PC12_UR [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:13] | | | PC13_NS [12:12] | PC13_PW [11:11] | PC13_PR [10:10] | PC13_UW [9:9] | PC13_UR [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:21] | | | PC14_NS [20:20] | PC14_PW [19:19] | PC14_PR [18:18] | PC14_UW [17:17] | PC14_UR [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:29] | | | PC15_NS [28:28] | PC15_PW [27:27] | PC15_PR [26:26] | PC15_UW [25:25] | PC15_UR [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | PC12_UR | R | R | 1 | Protection context 12, user read enable. |
| 1 | PC12_UW | RW | R | 1 | Protection context 12, user write enable. |
| 2 | PC12_PR | R | R | 1 | Protection context 12, privileged read enable. |
| 3 | PC12_PW | RW | R | 1 | Protection context 12, privileged write enable. |
| 4 | PC12_NS | RW | R | 1 | Protection context 12, non-secure. |
| 8 | PC13_UR | R | R | 1 | Protection context 13, user read enable. |
| 9 | PC13_UW | RW | R | 1 | Protection context 13, user write enable. |
| 10 | PC13_PR | R | R | 1 | Protection context 13, privileged read enable. |
| 11 | PC13_PW | RW | R | 1 | Protection context 13, privileged write enable. |
| 12 | PC13_NS | RW | R | 1 | Protection context 13, non-secure. |
| 16 | PC14_UR | R | R | 1 | Protection context 14, user read enable. |
| 17 | PC14_UW | RW | R | 1 | Protection context 14, user write enable. |
| 18 | PC14_PR | R | R | 1 | Protection context 14, privileged read enable. |
| 19 | PC14_PW | RW | R | 1 | Protection context 14, privileged write enable. |
| 20 | PC14_NS | RW | R | 1 | Protection context 14, non-secure. |
| 24 | PC15_UR | R | R | 1 | Protection context 15, user read enable. |
| 25 | PC15_UW | RW | R | 1 | Protection context 15, user write enable. |
| 26 | PC15_PR | R | R | 1 | Protection context 15, privileged read enable. |
| 27 | PC15_PW | RW | R | 1 | Protection context 15, privileged write enable. |
| 28 | PC15_NS | RW | R | 1 | Protection context 15, non-secure. |

### 23.719.2 PPU_FX

#### 23.719.2.1 PERI_MS_PPU_FX_SL_ADDR

**Description:** Slave region, base address
**Address:** 0x40020800
**Offset:** 0x0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** SL_ADDR is fixed (non-programmable).
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDR30 [7:2] | | | | | | None [1:0] | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDR30 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDR30 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDR30 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 2:31 | ADDR30 | R | R | 268435584 | This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is '15') must be 64 KByte aligned, and ADDR30[13:0] must be '0's. |

### 23.719.2.2 PERI_MS_PPU_FX_SL_SIZE

**Description:** Slave region, size
**Address:** 0x40020804
**Offset:** 0x4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** SL_SIZE is fixed (non-programmable).
**Default:** 0x80000000

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALID [31:31] | None [30:29] | | REGION_SIZE [28:24] | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 24:28 | REGION_SIZE | R | R | 5 | This field specifies the size of the slave region:<br>'0': Undefined.<br>'1': 4 B region (this is the smallest region size).<br>'2': 8 B region<br>'3': 16 B region<br>'4': 32 B region<br>'5': 64 B region<br>'6': 128 B region<br>'7': 256 B region<br>'8': 512 B region<br>'9': 1 KB region<br>'10': 2 KB region<br>'11': 4 KB region<br>'12': 8 KB region<br>'13': 16 KB region<br>'14': 32 KB region<br>'15': 64 KB region<br>'16': 128 KB region<br>'17': 256 KB region<br>'18': 512 KB region<br>'19': 1 MB region<br>'20': 2 MB region<br>'21': 4 MB region<br>'22': 8 MB region<br>'23': 16 MB region<br>'24': 32 MB region<br>'25': 64 MB region<br>'26': 128 MB region<br>'27': 256 MB region<br>'28': 512 MB region<br>'29': 1 GB region<br>'30': 2 GB region<br>'31': 4 GB region |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 31 | VALID | R | R | 1 | Slave region enable:<br>'0': Disabled. A disabled region will never result in a match on the transfer address.<br>'1': Enabled. |

### 23.719.2.3 PERI_MS_PPU_FX_SL_ATT0

**Description:** Slave attributes 0
**Address:** 0x40020810
**Offset:** 0x10
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** The access privileges for SL_ATT0, ..., SL_ATT3 are determined by MS_ATT0, ..., MS_ATT3.

Note that protection context '0' has unrestricted access: PC0_UR, ..., PC0_NS fields are fixed to '1's. The other protection contexts have SW programmable fields.

Typically, the SL_ATT0, ..., SL_ATT3 registers are initialized by the boot process with protection context '0'.

For 4 or less protection contexts (PC_NR <= 4), only SL_ATT0 is present. For 5 through 8 protection contexts, only SL_ATT0 and SL_ATT1 are present. For 9 through 12 or less protection contexts, only SL_ATT0, SL_ATT1 and SL_ATT2 are present. For 13 through 16 protection contexts, SL_ATT0, SL_ATT1, SL_ATT2 and SL_ATT3 are all present. If the number of protection contexts is not a multiple of 4, the 'missing' protection contexts in a register have no associated access fields (and the field positions read as '0').

**Default:** 0x1F1F1F1F

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:5] | | | PC0_NS [4:4] | PC0_PW [3:3] | PC0_PR [2:2] | PC0_UW [1:1] | PC0_UR [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:13] | | | PC1_NS [12:12] | PC1_PW [11:11] | PC1_PR [10:10] | PC1_UW [9:9] | PC1_UR [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:21] | | | PC2_NS [20:20] | PC2_PW [19:19] | PC2_PR [18:18] | PC2_UW [17:17] | PC2_UR [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:29] | | | PC3_NS [28:28] | PC3_PW [27:27] | PC3_PR [26:26] | PC3_UW [25:25] | PC3_UR [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | PC0_UR | R | R | 1 | Protection context 0, user read enable:<br>'0': Disabled (user, read accesses are NOT allowed).<br>'1': Enabled (user, read accesses are allowed). |
| 1 | PC0_UW | R | R | 1 | Protection context 0, user write enable:<br>'0': Disabled (user, write accesses are NOT allowed).<br>'1': Enabled (user, write accesses are allowed). |
| 2 | PC0_PR | R | R | 1 | Protection context 0, privileged read enable:<br>'0': Disabled (privileged, read accesses are NOT allowed).<br>'1': Enabled (privileged, read accesses are allowed). |
| 3 | PC0_PW | R | R | 1 | Protection context 0, privileged write enable:<br>'0': Disabled (privileged, write accesses are NOT allowed).<br>'1': Enabled (privileged, write accesses are allowed). |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 4 | PC0_NS | R | R | 1 | Protection context 0, non-secure:<br>'0': Secure (secure accesses allowed, non-secure access NOT allowed).<br>'1': Non-secure (both secure and non-secure accesses allowed). |
| 8 | PC1_UR | RW | R | 1 | Protection context 1, user read enable. |
| 9 | PC1_UW | RW | R | 1 | Protection context 1, user write enable. |
| 10 | PC1_PR | RW | R | 1 | Protection context 1, privileged read enable. |
| 11 | PC1_PW | RW | R | 1 | Protection context 1, privileged write enable. |
| 12 | PC1_NS | RW | R | 1 | Protection context 1, non-secure. |
| 16 | PC2_UR | RW | R | 1 | Protection context 2, user read enable. |
| 17 | PC2_UW | RW | R | 1 | Protection context 2, user write enable. |
| 18 | PC2_PR | RW | R | 1 | Protection context 2, privileged read enable. |
| 19 | PC2_PW | RW | R | 1 | Protection context 2, privileged write enable. |
| 20 | PC2_NS | RW | R | 1 | Protection context 2, non-secure. |
| 24 | PC3_UR | RW | R | 1 | Protection context 3, user read enable. |
| 25 | PC3_UW | RW | R | 1 | Protection context 3, user write enable. |
| 26 | PC3_PR | RW | R | 1 | Protection context 3, privileged read enable. |
| 27 | PC3_PW | RW | R | 1 | Protection context 3, privileged write enable. |
| 28 | PC3_NS | RW | R | 1 | Protection context 3, non-secure. |

### 23.719.2.4 PERI_MS_PPU_FX_SL_ATT1

**Description:** Slave attributes 1
**Address:** 0x40020814
**Offset:** 0x14
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x1F1F1F1F

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:5] | | | PC4_NS [4:4] | PC4_PW [3:3] | PC4_PR [2:2] | PC4_UW [1:1] | PC4_UR [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:13] | | | PC5_NS [12:12] | PC5_PW [11:11] | PC5_PR [10:10] | PC5_UW [9:9] | PC5_UR [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:21] | | | PC6_NS [20:20] | PC6_PW [19:19] | PC6_PR [18:18] | PC6_UW [17:17] | PC6_UR [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:29] | | | PC7_NS [28:28] | PC7_PW [27:27] | PC7_PR [26:26] | PC7_UW [25:25] | PC7_UR [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | PC4_UR | RW | R | 1 | Protection context 4, user read enable. |
| 1 | PC4_UW | RW | R | 1 | Protection context 4, user write enable. |
| 2 | PC4_PR | RW | R | 1 | Protection context 4, privileged read enable. |
| 3 | PC4_PW | RW | R | 1 | Protection context 4, privileged write enable. |
| 4 | PC4_NS | RW | R | 1 | Protection context 4, non-secure. |
| 8 | PC5_UR | RW | R | 1 | Protection context 5, user read enable. |
| 9 | PC5_UW | RW | R | 1 | Protection context 5, user write enable. |
| 10 | PC5_PR | RW | R | 1 | Protection context 5, privileged read enable. |
| 11 | PC5_PW | RW | R | 1 | Protection context 5, privileged write enable. |
| 12 | PC5_NS | RW | R | 1 | Protection context 5, non-secure. |
| 16 | PC6_UR | RW | R | 1 | Protection context 6, user read enable. |
| 17 | PC6_UW | RW | R | 1 | Protection context 6, user write enable. |
| 18 | PC6_PR | RW | R | 1 | Protection context 6, privileged read enable. |
| 19 | PC6_PW | RW | R | 1 | Protection context 6, privileged write enable. |
| 20 | PC6_NS | RW | R | 1 | Protection context 6, non-secure. |
| 24 | PC7_UR | RW | R | 1 | Protection context 7, user read enable. |
| 25 | PC7_UW | RW | R | 1 | Protection context 7, user write enable. |
| 26 | PC7_PR | RW | R | 1 | Protection context 7, privileged read enable. |
| 27 | PC7_PW | RW | R | 1 | Protection context 7, privileged write enable. |
| 28 | PC7_NS | RW | R | 1 | Protection context 7, non-secure. |

### 23.719.2.5 PERI_MS_PPU_FX_SL_ATT2

**Description:** Slave attributes 2
**Address:** 0x40020818
**Offset:** 0x18
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x1F1F1F1F

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:5] | | | PC8_NS [4:4] | PC8_PW [3:3] | PC8_PR [2:2] | PC8_UW [1:1] | PC8_UR [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:13] | | | PC9_NS [12:12] | PC9_PW [11:11] | PC9_PR [10:10] | PC9_UW [9:9] | PC9_UR [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:21] | | | PC10_NS [20:20] | PC10_PW [19:19] | PC10_PR [18:18] | PC10_UW [17:17] | PC10_UR [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:29] | | | PC11_NS [28:28] | PC11_PW [27:27] | PC11_PR [26:26] | PC11_UW [25:25] | PC11_UR [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | PC8_UR | RW | R | 1 | Protection context 8, user read enable. |
| 1 | PC8_UW | RW | R | 1 | Protection context 8, user write enable. |
| 2 | PC8_PR | RW | R | 1 | Protection context 8, privileged read enable. |
| 3 | PC8_PW | RW | R | 1 | Protection context 8, privileged write enable. |
| 4 | PC8_NS | RW | R | 1 | Protection context 8, non-secure. |
| 8 | PC9_UR | RW | R | 1 | Protection context 9, user read enable. |
| 9 | PC9_UW | RW | R | 1 | Protection context 9, user write enable. |
| 10 | PC9_PR | RW | R | 1 | Protection context 9, privileged read enable. |
| 11 | PC9_PW | RW | R | 1 | Protection context 9, privileged write enable. |
| 12 | PC9_NS | RW | R | 1 | Protection context 9, non-secure. |
| 16 | PC10_UR | RW | R | 1 | Protection context 10, user read enable. |
| 17 | PC10_UW | RW | R | 1 | Protection context 10, user write enable. |
| 18 | PC10_PR | RW | R | 1 | Protection context 10, privileged read enable. |
| 19 | PC10_PW | RW | R | 1 | Protection context 10, privileged write enable. |
| 20 | PC10_NS | RW | R | 1 | Protection context 10, non-secure. |
| 24 | PC11_UR | RW | R | 1 | Protection context 11, user read enable. |
| 25 | PC11_UW | RW | R | 1 | Protection context 11, user write enable. |
| 26 | PC11_PR | RW | R | 1 | Protection context 11, privileged read enable. |
| 27 | PC11_PW | RW | R | 1 | Protection context 11, privileged write enable. |
| 28 | PC11_NS | RW | R | 1 | Protection context 11, non-secure. |

### 23.719.2.6 PERI_MS_PPU_FX_SL_ATT3

**Description:** Slave attributes 3
**Address:** 0x4002081C
**Offset:** 0x1C
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x1F1F1F1F

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:5] | | | PC12_NS [4:4] | PC12_PW [3:3] | PC12_PR [2:2] | PC12_UW [1:1] | PC12_UR [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:13] | | | PC13_NS [12:12] | PC13_PW [11:11] | PC13_PR [10:10] | PC13_UW [9:9] | PC13_UR [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:21] | | | PC14_NS [20:20] | PC14_PW [19:19] | PC14_PR [18:18] | PC14_UW [17:17] | PC14_UR [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:29] | | | PC15_NS [28:28] | PC15_PW [27:27] | PC15_PR [26:26] | PC15_UW [25:25] | PC15_UR [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | PC12_UR | RW | R | 1 | Protection context 12, user read enable. |
| 1 | PC12_UW | RW | R | 1 | Protection context 12, user write enable. |
| 2 | PC12_PR | RW | R | 1 | Protection context 12, privileged read enable. |
| 3 | PC12_PW | RW | R | 1 | Protection context 12, privileged write enable. |
| 4 | PC12_NS | RW | R | 1 | Protection context 12, non-secure. |
| 8 | PC13_UR | RW | R | 1 | Protection context 13, user read enable. |
| 9 | PC13_UW | RW | R | 1 | Protection context 13, user write enable. |
| 10 | PC13_PR | RW | R | 1 | Protection context 13, privileged read enable. |
| 11 | PC13_PW | RW | R | 1 | Protection context 13, privileged write enable. |
| 12 | PC13_NS | RW | R | 1 | Protection context 13, non-secure. |
| 16 | PC14_UR | RW | R | 1 | Protection context 14, user read enable. |
| 17 | PC14_UW | RW | R | 1 | Protection context 14, user write enable. |
| 18 | PC14_PR | RW | R | 1 | Protection context 14, privileged read enable. |
| 19 | PC14_PW | RW | R | 1 | Protection context 14, privileged write enable. |
| 20 | PC14_NS | RW | R | 1 | Protection context 14, non-secure. |
| 24 | PC15_UR | RW | R | 1 | Protection context 15, user read enable. |
| 25 | PC15_UW | RW | R | 1 | Protection context 15, user write enable. |
| 26 | PC15_PR | RW | R | 1 | Protection context 15, privileged read enable. |
| 27 | PC15_PW | RW | R | 1 | Protection context 15, privileged write enable. |
| 28 | PC15_NS | RW | R | 1 | Protection context 15, non-secure. |

### 23.719.2.7 PERI_MS_PPU_FX_MS_ADDR

**Description:** Master region, base address
**Address:** 0x40020820
**Offset:** 0x20
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** MS_ADDR is fixed (non-programmable).

The access privileges for MS_ADDR are determined by MS_ATT0, ..., MS_ATT3.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDR26 [7:6] | | None [5:0] | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDR26 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDR26 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDR26 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 6:31 | ADDR26 | R | R | 16779296 | This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. |

### 23.719.2.8 PERI_MS_PPU_FX_MS_SIZE

**Description:** Master region, size
**Address:** 0x40020824
**Offset:** 0x24
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** MS_SIZE is fixed (non-programmable).

The access privileges for MS_SIZE are determined by MS_ATT0, ..., MS_ATT3.
**Default:** 0x85000000

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALID [31:31] | None [30:29] | | REGION_SIZE [28:24] | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 24:28 | REGION_SIZE | R | R | 5 | This field specifies the size of the master region:<br>'5': 64 B region<br><br>The master region includes the SL_ADDR, SL_SIZE, SL_ATT0, ..., SL_ATT3, MS_ADDR, MS_SIZE, MS_ATT0, ..., MS_ATT3 registers. Therefore, the access privileges for all these registers is determined by MS_ATT0, ..., MS_ATT3. |
| 31 | VALID | R | R | 1 | Master region enable:<br>'1': Enabled. |

### 23.719.2.9 PERI_MS_PPU_FX_MS_ATT0

**Description:** Master attributes 0
**Address:** 0x40020830
**Offset:** 0x30
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** The access privileges for MS_ATT0, ..., MS_ATT3 are determined by MS_ATT0, ..., MS_ATT3.

Note that protection context '0' has unrestricted access: PC0_UR, ..., PC0_NS fields are fixed to '1's. The other protection contexts have SW programmable fields.

Typically, the MS_ATT0, ..., MS_ATT3 registers are programmed by the boot process with protection context '0'.
**Default:** 0x1F1F1F1F

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:5] | | | PC0_NS [4:4] | PC0_PW [3:3] | PC0_PR [2:2] | PC0_UW [1:1] | PC0_UR [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:13] | | | PC1_NS [12:12] | PC1_PW [11:11] | PC1_PR [10:10] | PC1_UW [9:9] | PC1_UR [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:21] | | | PC2_NS [20:20] | PC2_PW [19:19] | PC2_PR [18:18] | PC2_UW [17:17] | PC2_UR [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:29] | | | PC3_NS [28:28] | PC3_PW [27:27] | PC3_PR [26:26] | PC3_UW [25:25] | PC3_UR [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | PC0_UR | R | R | 1 | Protection context 0, user read enable:<br>'0': Disabled (user, read accesses are NOT allowed).<br>'1': Enabled (user, read accesses are allowed). |
| 1 | PC0_UW | R | R | 1 | Protection context 0, user write enable:<br>'0': Disabled (user, write accesses are NOT allowed).<br>'1': Enabled (user, write accesses are allowed). |
| 2 | PC0_PR | R | R | 1 | Protection context 0, privileged read enable:<br>'0': Disabled (privileged, read accesses are NOT allowed).<br>'1': Enabled (privileged, read accesses are allowed). |
| 3 | PC0_PW | R | R | 1 | Protection context 0, privileged write enable:<br>'0': Disabled (privileged, write accesses are NOT allowed).<br>'1': Enabled (privileged, write accesses are allowed). |
| 4 | PC0_NS | R | R | 1 | Protection context 0, non-secure:<br>'0': Secure (secure accesses allowed, non-secure access NOT allowed).<br>'1': Non-secure (both secure and non-secure accesses allowed). |
| 8 | PC1_UR | R | R | 1 | Protection context 1, user read enable. |
| 9 | PC1_UW | RW | R | 1 | Protection context 1, user write enable. |
| 10 | PC1_PR | R | R | 1 | Protection context 1, privileged read enable. |
| 11 | PC1_PW | RW | R | 1 | Protection context 1, privileged write enable. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 12 | PC1_NS | RW | R | 1 | Protection context 1, non-secure. |
| 16 | PC2_UR | R | R | 1 | Protection context 2, user read enable. |
| 17 | PC2_UW | RW | R | 1 | Protection context 2, user write enable. |
| 18 | PC2_PR | R | R | 1 | Protection context 2, privileged read enable. |
| 19 | PC2_PW | RW | R | 1 | Protection context 2, privileged write enable. |
| 20 | PC2_NS | RW | R | 1 | Protection context 2, non-secure. |
| 24 | PC3_UR | R | R | 1 | Protection context 3, user read enable. |
| 25 | PC3_UW | RW | R | 1 | Protection context 3, user write enable. |
| 26 | PC3_PR | R | R | 1 | Protection context 3, privileged read enable. |
| 27 | PC3_PW | RW | R | 1 | Protection context 3, privileged write enable. |
| 28 | PC3_NS | RW | R | 1 | Protection context 3, non-secure. |

### 23.719.2.10 PERI_MS_PPU_FX_MS_ATT1

**Description:** Master attributes 1
**Address:** 0x40020834
**Offset:** 0x34
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x1F1F1F1F

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:5] | | | PC4_NS [4:4] | PC4_PW [3:3] | PC4_PR [2:2] | PC4_UW [1:1] | PC4_UR [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:13] | | | PC5_NS [12:12] | PC5_PW [11:11] | PC5_PR [10:10] | PC5_UW [9:9] | PC5_UR [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:21] | | | PC6_NS [20:20] | PC6_PW [19:19] | PC6_PR [18:18] | PC6_UW [17:17] | PC6_UR [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:29] | | | PC7_NS [28:28] | PC7_PW [27:27] | PC7_PR [26:26] | PC7_UW [25:25] | PC7_UR [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | PC4_UR | R | R | 1 | Protection context 4, user read enable. |
| 1 | PC4_UW | RW | R | 1 | Protection context 4, user write enable. |
| 2 | PC4_PR | R | R | 1 | Protection context 4, privileged read enable. |
| 3 | PC4_PW | RW | R | 1 | Protection context 4, privileged write enable. |
| 4 | PC4_NS | RW | R | 1 | Protection context 4, non-secure. |
| 8 | PC5_UR | R | R | 1 | Protection context 5, user read enable. |
| 9 | PC5_UW | RW | R | 1 | Protection context 5, user write enable. |
| 10 | PC5_PR | R | R | 1 | Protection context 5, privileged read enable. |
| 11 | PC5_PW | RW | R | 1 | Protection context 5, privileged write enable. |
| 12 | PC5_NS | RW | R | 1 | Protection context 5, non-secure. |
| 16 | PC6_UR | R | R | 1 | Protection context 6, user read enable. |
| 17 | PC6_UW | RW | R | 1 | Protection context 6, user write enable. |
| 18 | PC6_PR | R | R | 1 | Protection context 6, privileged read enable. |
| 19 | PC6_PW | RW | R | 1 | Protection context 6, privileged write enable. |
| 20 | PC6_NS | RW | R | 1 | Protection context 6, non-secure. |
| 24 | PC7_UR | R | R | 1 | Protection context 7, user read enable. |
| 25 | PC7_UW | RW | R | 1 | Protection context 7, user write enable. |
| 26 | PC7_PR | R | R | 1 | Protection context 7, privileged read enable. |
| 27 | PC7_PW | RW | R | 1 | Protection context 7, privileged write enable. |
| 28 | PC7_NS | RW | R | 1 | Protection context 7, non-secure. |

### 23.719.2.11 PERI_MS_PPU_FX_MS_ATT2

**Description:** Master attributes 2
**Address:** 0x40020838
**Offset:** 0x38
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x1F1F1F1F

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:5] | | | PC8_NS [4:4] | PC8_PW [3:3] | PC8_PR [2:2] | PC8_UW [1:1] | PC8_UR [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:13] | | | PC9_NS [12:12] | PC9_PW [11:11] | PC9_PR [10:10] | PC9_UW [9:9] | PC9_UR [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:21] | | | PC10_NS [20:20] | PC10_PW [19:19] | PC10_PR [18:18] | PC10_UW [17:17] | PC10_UR [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:29] | | | PC11_NS [28:28] | PC11_PW [27:27] | PC11_PR [26:26] | PC11_UW [25:25] | PC11_UR [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | PC8_UR | R | R | 1 | Protection context 8, user read enable. |
| 1 | PC8_UW | RW | R | 1 | Protection context 8, user write enable. |
| 2 | PC8_PR | R | R | 1 | Protection context 8, privileged read enable. |
| 3 | PC8_PW | RW | R | 1 | Protection context 8, privileged write enable. |
| 4 | PC8_NS | RW | R | 1 | Protection context 8, non-secure. |
| 8 | PC9_UR | R | R | 1 | Protection context 9, user read enable. |
| 9 | PC9_UW | RW | R | 1 | Protection context 9, user write enable. |
| 10 | PC9_PR | R | R | 1 | Protection context 9, privileged read enable. |
| 11 | PC9_PW | RW | R | 1 | Protection context 9, privileged write enable. |
| 12 | PC9_NS | RW | R | 1 | Protection context 9, non-secure. |
| 16 | PC10_UR | R | R | 1 | Protection context 10, user read enable. |
| 17 | PC10_UW | RW | R | 1 | Protection context 10, user write enable. |
| 18 | PC10_PR | R | R | 1 | Protection context 10, privileged read enable. |
| 19 | PC10_PW | RW | R | 1 | Protection context 10, privileged write enable. |
| 20 | PC10_NS | RW | R | 1 | Protection context 10, non-secure. |
| 24 | PC11_UR | R | R | 1 | Protection context 11, user read enable. |
| 25 | PC11_UW | RW | R | 1 | Protection context 11, user write enable. |
| 26 | PC11_PR | R | R | 1 | Protection context 11, privileged read enable. |
| 27 | PC11_PW | RW | R | 1 | Protection context 11, privileged write enable. |
| 28 | PC11_NS | RW | R | 1 | Protection context 11, non-secure. |

### 23.719.2.12 PERI_MS_PPU_FX_MS_ATT3

**Description:** Master attributes 3
**Address:** 0x4002083C
**Offset:** 0x3C
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x1F1F1F1F

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:5] | | | PC12_NS [4:4] | PC12_PW [3:3] | PC12_PR [2:2] | PC12_UW [1:1] | PC12_UR [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:13] | | | PC13_NS [12:12] | PC13_PW [11:11] | PC13_PR [10:10] | PC13_UW [9:9] | PC13_UR [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:21] | | | PC14_NS [20:20] | PC14_PW [19:19] | PC14_PR [18:18] | PC14_UW [17:17] | PC14_UR [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:29] | | | PC15_NS [28:28] | PC15_PW [27:27] | PC15_PR [26:26] | PC15_UW [25:25] | PC15_UR [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | PC12_UR | R | R | 1 | Protection context 12, user read enable. |
| 1 | PC12_UW | RW | R | 1 | Protection context 12, user write enable. |
| 2 | PC12_PR | R | R | 1 | Protection context 12, privileged read enable. |
| 3 | PC12_PW | RW | R | 1 | Protection context 12, privileged write enable. |
| 4 | PC12_NS | RW | R | 1 | Protection context 12, non-secure. |
| 8 | PC13_UR | R | R | 1 | Protection context 13, user read enable. |
| 9 | PC13_UW | RW | R | 1 | Protection context 13, user write enable. |
| 10 | PC13_PR | R | R | 1 | Protection context 13, privileged read enable. |
| 11 | PC13_PW | RW | R | 1 | Protection context 13, privileged write enable. |
| 12 | PC13_NS | RW | R | 1 | Protection context 13, non-secure. |
| 16 | PC14_UR | R | R | 1 | Protection context 14, user read enable. |
| 17 | PC14_UW | RW | R | 1 | Protection context 14, user write enable. |
| 18 | PC14_PR | R | R | 1 | Protection context 14, privileged read enable. |
| 19 | PC14_PW | RW | R | 1 | Protection context 14, privileged write enable. |
| 20 | PC14_NS | RW | R | 1 | Protection context 14, non-secure. |
| 24 | PC15_UR | R | R | 1 | Protection context 15, user read enable. |
| 25 | PC15_UW | RW | R | 1 | Protection context 15, user write enable. |
| 26 | PC15_PR | R | R | 1 | Protection context 15, privileged read enable. |
| 27 | PC15_PW | RW | R | 1 | Protection context 15, privileged write enable. |
| 28 | PC15_NS | RW | R | 1 | Protection context 15, non-secure. |

# 24 PERI_PCLK

**Description** Peripheral PCLK groups
**Base Address** 0x40040000
**Size** 0x20000
**Slave Num** MMIO0 - 2

## 24.1 GR 0

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_PCLK_GR0_DIV_CMD | 0x40040000 | FULL | Divider command |
| PERI_PCLK_GR0_CLOCK_CTL0 | 0x40040C00 | FULL | Clock control |
| PERI_PCLK_GR0_CLOCK_CTL1 | 0x40040C04 | FULL | Clock control |
| PERI_PCLK_GR0_CLOCK_CTL2 | 0x40040C08 | FULL | Clock control |
| PERI_PCLK_GR0_CLOCK_CTL3 | 0x40040C0C | FULL | Clock control |
| PERI_PCLK_GR0_CLOCK_CTL4 | 0x40040C10 | FULL | Clock control |
| PERI_PCLK_GR0_CLOCK_CTL5 | 0x40040C14 | FULL | Clock control |
| PERI_PCLK_GR0_CLOCK_CTL6 | 0x40040C18 | FULL | Clock control |
| PERI_PCLK_GR0_CLOCK_CTL7 | 0x40040C1C | FULL | Clock control |
| PERI_PCLK_GR0_CLOCK_CTL8 | 0x40040C20 | FULL | Clock control |
| PERI_PCLK_GR0_CLOCK_CTL9 | 0x40040C24 | FULL | Clock control |
| PERI_PCLK_GR0_CLOCK_CTL10 | 0x40040C28 | FULL | Clock control |
| PERI_PCLK_GR0_CLOCK_CTL11 | 0x40040C2C | FULL | Clock control |
| PERI_PCLK_GR0_CLOCK_CTL12 | 0x40040C30 | FULL | Clock control |
| PERI_PCLK_GR0_CLOCK_CTL13 | 0x40040C34 | FULL | Clock control |
| PERI_PCLK_GR0_CLOCK_CTL14 | 0x40040C38 | FULL | Clock control |
| PERI_PCLK_GR0_DIV_8_CTL0 | 0x40041000 | FULL | Divider control (for 8.0 divider) |
| PERI_PCLK_GR0_DIV_8_CTL1 | 0x40041004 | FULL | Divider control (for 8.0 divider) |
| PERI_PCLK_GR0_DIV_8_CTL2 | 0x40041008 | FULL | Divider control (for 8.0 divider) |
| PERI_PCLK_GR0_DIV_8_CTL3 | 0x4004100C | FULL | Divider control (for 8.0 divider) |
| PERI_PCLK_GR0_DIV_16_CTL0 | 0x40041400 | FULL | Divider control (for 16.0 divider) |
| PERI_PCLK_GR0_DIV_16_CTL1 | 0x40041404 | FULL | Divider control (for 16.0 divider) |
| PERI_PCLK_GR0_DIV_16_CTL2 | 0x40041408 | FULL | Divider control (for 16.0 divider) |
| PERI_PCLK_GR0_DIV_24_5_CTL0 | 0x40041C00 | FULL | Divider control (for 24.5 divider) |

## 24.2 GR 1

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_PCLK_GR1_DIV_CMD | 0x40042000 | FULL | Divider command |
| PERI_PCLK_GR1_CLOCK_CTL0 | 0x40042C00 | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL1 | 0x40042C04 | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL2 | 0x40042C08 | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL3 | 0x40042C0C | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL4 | 0x40042C10 | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL5 | 0x40042C14 | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL6 | 0x40042C18 | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL7 | 0x40042C1C | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL8 | 0x40042C20 | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL9 | 0x40042C24 | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL10 | 0x40042C28 | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL11 | 0x40042C2C | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL12 | 0x40042C30 | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL13 | 0x40042C34 | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL14 | 0x40042C38 | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL15 | 0x40042C3C | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL16 | 0x40042C40 | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL17 | 0x40042C44 | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL18 | 0x40042C48 | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL19 | 0x40042C4C | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL20 | 0x40042C50 | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL21 | 0x40042C54 | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL22 | 0x40042C58 | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL23 | 0x40042C5C | FULL | Clock control |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_PCLK_GR1_CLOCK_CTL24 | 0x40042C60 | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL25 | 0x40042C64 | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL26 | 0x40042C68 | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL27 | 0x40042C6C | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL28 | 0x40042C70 | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL29 | 0x40042C74 | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL30 | 0x40042C78 | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL31 | 0x40042C7C | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL32 | 0x40042C80 | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL33 | 0x40042C84 | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL34 | 0x40042C88 | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL35 | 0x40042C8C | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL36 | 0x40042C90 | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL37 | 0x40042C94 | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL38 | 0x40042C98 | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL39 | 0x40042C9C | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL40 | 0x40042CA0 | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL41 | 0x40042CA4 | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL42 | 0x40042CA8 | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL43 | 0x40042CAC | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL44 | 0x40042CB0 | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL45 | 0x40042CB4 | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL46 | 0x40042CB8 | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL47 | 0x40042CBC | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL48 | 0x40042CC0 | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL49 | 0x40042CC4 | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL50 | 0x40042CC8 | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL51 | 0x40042CCC | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL52 | 0x40042CD0 | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL53 | 0x40042CD4 | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL54 | 0x40042CD8 | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL55 | 0x40042CDC | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL56 | 0x40042CE0 | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL57 | 0x40042CE4 | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL58 | 0x40042CE8 | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL59 | 0x40042CEC | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL60 | 0x40042CF0 | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL61 | 0x40042CF4 | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL62 | 0x40042CF8 | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL63 | 0x40042CFC | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL64 | 0x40042D00 | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL65 | 0x40042D04 | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL66 | 0x40042D08 | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL67 | 0x40042D0C | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL68 | 0x40042D10 | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL69 | 0x40042D14 | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL70 | 0x40042D18 | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL71 | 0x40042D1C | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL72 | 0x40042D20 | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL73 | 0x40042D24 | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL74 | 0x40042D28 | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL75 | 0x40042D2C | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL76 | 0x40042D30 | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL77 | 0x40042D34 | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL78 | 0x40042D38 | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL79 | 0x40042D3C | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL80 | 0x40042D40 | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL81 | 0x40042D44 | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL82 | 0x40042D48 | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL83 | 0x40042D4C | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL84 | 0x40042D50 | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL85 | 0x40042D54 | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL86 | 0x40042D58 | FULL | Clock control |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_PCLK_GR1_CLOCK_CTL87 | 0x40042D5C | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL88 | 0x40042D60 | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL89 | 0x40042D64 | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL90 | 0x40042D68 | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL91 | 0x40042D6C | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL92 | 0x40042D70 | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL93 | 0x40042D74 | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL94 | 0x40042D78 | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL95 | 0x40042D7C | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL96 | 0x40042D80 | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL97 | 0x40042D84 | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL98 | 0x40042D88 | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL99 | 0x40042D8C | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL100 | 0x40042D90 | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL101 | 0x40042D94 | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL102 | 0x40042D98 | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL103 | 0x40042D9C | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL104 | 0x40042DA0 | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL105 | 0x40042DA4 | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL106 | 0x40042DA8 | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL107 | 0x40042DAC | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL108 | 0x40042DB0 | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL109 | 0x40042DB4 | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL110 | 0x40042DB8 | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL111 | 0x40042DBC | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL112 | 0x40042DC0 | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL113 | 0x40042DC4 | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL114 | 0x40042DC8 | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL115 | 0x40042DCC | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL116 | 0x40042DD0 | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL117 | 0x40042DD4 | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL118 | 0x40042DD8 | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL119 | 0x40042DDC | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL120 | 0x40042DE0 | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL121 | 0x40042DE4 | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL122 | 0x40042DE8 | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL123 | 0x40042DEC | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL124 | 0x40042DF0 | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL125 | 0x40042DF4 | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL126 | 0x40042DF8 | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL127 | 0x40042DFC | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL128 | 0x40042E00 | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL129 | 0x40042E04 | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL130 | 0x40042E08 | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL131 | 0x40042E0C | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL132 | 0x40042E10 | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL133 | 0x40042E14 | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL134 | 0x40042E18 | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL135 | 0x40042E1C | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL136 | 0x40042E20 | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL137 | 0x40042E24 | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL138 | 0x40042E28 | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL139 | 0x40042E2C | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL140 | 0x40042E30 | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL141 | 0x40042E34 | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL142 | 0x40042E38 | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL143 | 0x40042E3C | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL144 | 0x40042E40 | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL145 | 0x40042E44 | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL146 | 0x40042E48 | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL147 | 0x40042E4C | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL148 | 0x40042E50 | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL149 | 0x40042E54 | FULL | Clock control |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_PCLK_GR1_CLOCK_CTL150 | 0x40042E58 | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL151 | 0x40042E5C | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL152 | 0x40042E60 | FULL | Clock control |
| PERI_PCLK_GR1_CLOCK_CTL153 | 0x40042E64 | FULL | Clock control |
| PERI_PCLK_GR1_DIV_8_CTL0 | 0x40043000 | FULL | Divider control (for 8.0 divider) |
| PERI_PCLK_GR1_DIV_8_CTL1 | 0x40043004 | FULL | Divider control (for 8.0 divider) |
| PERI_PCLK_GR1_DIV_8_CTL2 | 0x40043008 | FULL | Divider control (for 8.0 divider) |
| PERI_PCLK_GR1_DIV_8_CTL3 | 0x4004300C | FULL | Divider control (for 8.0 divider) |
| PERI_PCLK_GR1_DIV_8_CTL4 | 0x40043010 | FULL | Divider control (for 8.0 divider) |
| PERI_PCLK_GR1_DIV_8_CTL5 | 0x40043014 | FULL | Divider control (for 8.0 divider) |
| PERI_PCLK_GR1_DIV_8_CTL6 | 0x40043018 | FULL | Divider control (for 8.0 divider) |
| PERI_PCLK_GR1_DIV_8_CTL7 | 0x4004301C | FULL | Divider control (for 8.0 divider) |
| PERI_PCLK_GR1_DIV_8_CTL8 | 0x40043020 | FULL | Divider control (for 8.0 divider) |
| PERI_PCLK_GR1_DIV_8_CTL9 | 0x40043024 | FULL | Divider control (for 8.0 divider) |
| PERI_PCLK_GR1_DIV_8_CTL10 | 0x40043028 | FULL | Divider control (for 8.0 divider) |
| PERI_PCLK_GR1_DIV_8_CTL11 | 0x4004302C | FULL | Divider control (for 8.0 divider) |
| PERI_PCLK_GR1_DIV_8_CTL12 | 0x40043030 | FULL | Divider control (for 8.0 divider) |
| PERI_PCLK_GR1_DIV_8_CTL13 | 0x40043034 | FULL | Divider control (for 8.0 divider) |
| PERI_PCLK_GR1_DIV_8_CTL14 | 0x40043038 | FULL | Divider control (for 8.0 divider) |
| PERI_PCLK_GR1_DIV_8_CTL15 | 0x4004303C | FULL | Divider control (for 8.0 divider) |
| PERI_PCLK_GR1_DIV_8_CTL16 | 0x40043040 | FULL | Divider control (for 8.0 divider) |
| PERI_PCLK_GR1_DIV_8_CTL17 | 0x40043044 | FULL | Divider control (for 8.0 divider) |
| PERI_PCLK_GR1_DIV_8_CTL18 | 0x40043048 | FULL | Divider control (for 8.0 divider) |
| PERI_PCLK_GR1_DIV_16_CTL0 | 0x40043400 | FULL | Divider control (for 16.0 divider) |
| PERI_PCLK_GR1_DIV_16_CTL1 | 0x40043404 | FULL | Divider control (for 16.0 divider) |
| PERI_PCLK_GR1_DIV_16_CTL2 | 0x40043408 | FULL | Divider control (for 16.0 divider) |
| PERI_PCLK_GR1_DIV_16_CTL3 | 0x4004340C | FULL | Divider control (for 16.0 divider) |
| PERI_PCLK_GR1_DIV_16_CTL4 | 0x40043410 | FULL | Divider control (for 16.0 divider) |
| PERI_PCLK_GR1_DIV_16_CTL5 | 0x40043414 | FULL | Divider control (for 16.0 divider) |
| PERI_PCLK_GR1_DIV_16_CTL6 | 0x40043418 | FULL | Divider control (for 16.0 divider) |
| PERI_PCLK_GR1_DIV_16_CTL7 | 0x4004341C | FULL | Divider control (for 16.0 divider) |
| PERI_PCLK_GR1_DIV_16_CTL8 | 0x40043420 | FULL | Divider control (for 16.0 divider) |
| PERI_PCLK_GR1_DIV_16_CTL9 | 0x40043424 | FULL | Divider control (for 16.0 divider) |
| PERI_PCLK_GR1_DIV_16_CTL10 | 0x40043428 | FULL | Divider control (for 16.0 divider) |
| PERI_PCLK_GR1_DIV_16_CTL11 | 0x4004342C | FULL | Divider control (for 16.0 divider) |
| PERI_PCLK_GR1_DIV_16_CTL12 | 0x40043430 | FULL | Divider control (for 16.0 divider) |
| PERI_PCLK_GR1_DIV_16_CTL13 | 0x40043434 | FULL | Divider control (for 16.0 divider) |
| PERI_PCLK_GR1_DIV_16_CTL14 | 0x40043438 | FULL | Divider control (for 16.0 divider) |
| PERI_PCLK_GR1_DIV_16_CTL15 | 0x4004343C | FULL | Divider control (for 16.0 divider) |
| PERI_PCLK_GR1_DIV_16_CTL16 | 0x40043440 | FULL | Divider control (for 16.0 divider) |
| PERI_PCLK_GR1_DIV_16_CTL17 | 0x40043444 | FULL | Divider control (for 16.0 divider) |
| PERI_PCLK_GR1_DIV_16_CTL18 | 0x40043448 | FULL | Divider control (for 16.0 divider) |
| PERI_PCLK_GR1_DIV_16_CTL19 | 0x4004344C | FULL | Divider control (for 16.0 divider) |
| PERI_PCLK_GR1_DIV_24_5_CTL0 | 0x40043C00 | FULL | Divider control (for 24.5 divider) |
| PERI_PCLK_GR1_DIV_24_5_CTL1 | 0x40043C04 | FULL | Divider control (for 24.5 divider) |
| PERI_PCLK_GR1_DIV_24_5_CTL2 | 0x40043C08 | FULL | Divider control (for 24.5 divider) |
| PERI_PCLK_GR1_DIV_24_5_CTL3 | 0x40043C0C | FULL | Divider control (for 24.5 divider) |
| PERI_PCLK_GR1_DIV_24_5_CTL4 | 0x40043C10 | FULL | Divider control (for 24.5 divider) |
| PERI_PCLK_GR1_DIV_24_5_CTL5 | 0x40043C14 | FULL | Divider control (for 24.5 divider) |
| PERI_PCLK_GR1_DIV_24_5_CTL6 | 0x40043C18 | FULL | Divider control (for 24.5 divider) |
| PERI_PCLK_GR1_DIV_24_5_CTL7 | 0x40043C1C | FULL | Divider control (for 24.5 divider) |
| PERI_PCLK_GR1_DIV_24_5_CTL8 | 0x40043C20 | FULL | Divider control (for 24.5 divider) |
| PERI_PCLK_GR1_DIV_24_5_CTL9 | 0x40043C24 | FULL | Divider control (for 24.5 divider) |
| PERI_PCLK_GR1_DIV_24_5_CTL10 | 0x40043C28 | FULL | Divider control (for 24.5 divider) |
| PERI_PCLK_GR1_DIV_24_5_CTL11 | 0x40043C2C | FULL | Divider control (for 24.5 divider) |
| PERI_PCLK_GR1_DIV_24_5_CTL12 | 0x40043C30 | FULL | Divider control (for 24.5 divider) |
| PERI_PCLK_GR1_DIV_24_5_CTL13 | 0x40043C34 | FULL | Divider control (for 24.5 divider) |
| PERI_PCLK_GR1_DIV_24_5_CTL14 | 0x40043C38 | FULL | Divider control (for 24.5 divider) |
| PERI_PCLK_GR1_DIV_24_5_CTL15 | 0x40043C3C | FULL | Divider control (for 24.5 divider) |
| PERI_PCLK_GR1_DIV_24_5_CTL16 | 0x40043C40 | FULL | Divider control (for 24.5 divider) |
| PERI_PCLK_GR1_DIV_24_5_CTL17 | 0x40043C44 | FULL | Divider control (for 24.5 divider) |
| PERI_PCLK_GR1_DIV_24_5_CTL18 | 0x40043C48 | FULL | Divider control (for 24.5 divider) |
| PERI_PCLK_GR1_DIV_24_5_CTL19 | 0x40043C4C | FULL | Divider control (for 24.5 divider) |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PERI_PCLK_GR1_DIV_24_5_CTL20 | 0x40043C50 | FULL | Divider control (for 24.5 divider) |

## 24.3 Register Details

### 24.3.1 GR

#### 24.3.1.1 PERI_PCLK_GR_DIV_CMD

**Description:** Divider command
**Address:** 0x40040000
**Offset:** 0x0
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** The (PA_TYPE_SEL, PA_DIV_SEL) field pair allows a divider to be phase aligned with another divider. E.g., consider a 48 MHz 'clk_pclk_root[i]', and a need for a 12 MHz divided clock A and a 8 MHz divided clock B. Clock A uses 8.0 integer divider 0 and is created by aligning it to 'clk_pclk_root[i]' ((PA_TYPE_SEL, PA_DIV_SEL) is (3, 63)) and DIV_8_CTL0.INT8_DIV is '4-1'. Clock B uses 8.0 integer divider 1 and is created by aligning it to clock A ((PA_TYPE_SEL, PA_DIV_SEL) is (0, 0)) and DIV_8_CTL1.INT8_DIV is '6-1'. This guarantees that clock B is phase aligned with clock A: as the smallest common multiple of the two clock periods is 12 'clk_pclk_root[i]' cycles, the clocks A and B will be aligned every 12 'clk_pclk_root[i]' cycles. Note: clock B is phase aligned to clock A, but still uses 'clk_pclk_root[i]' as a reference clock for its divider value.
**Default:** 0x3FF03FF

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DIV_SEL [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:10] | | | | | | TYPE_SEL [9:8] | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | PA_DIV_SEL [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | ENABLE [31:31] | DISABLE [30:30] | None [29:26] | | | | PA_TYPE_SEL [25:24] | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | DIV_SEL | RW | R | 255 | (TYPE_SEL, DIV_SEL) specifies the divider on which the command (DISABLE/ENABLE) is performed.<br><br>If DIV_SEL is '255' and TYPE_SEL is '3' (default/reset value), no divider is specified and no clock signal(s) are generated. |
| 8:9 | TYPE_SEL | RW | R | 3 | Specifies the divider type of the divider on which the command is performed:<br>0: 8.0 (integer) clock dividers.<br>1: 16.0 (integer) clock dividers.<br>2: 16.5 (fractional) clock dividers.<br>3: 24.5 (fractional) clock dividers. |
| 16:23 | PA_DIV_SEL | RW | R | 255 | (PA_TYPE_SEL, PA_DIV_SEL) specifies the divider to which phase alignment is performed for the clock enable command. Any enabled divider can be used as reference. This allows all dividers to be aligned with each other, even when they are enabled at different times.<br><br>If PA_DIV_SEL is '255' and PA_TYPE_SEL is '3', 'clk_pclk_root[i]' is used as reference. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 24:25 | PA_TYPE_SEL | RW | R | 3 | Specifies the divider type of the divider to which phase alignment is performed for the clock enable command:<br>0: 8.0 (integer) clock dividers.<br>1: 16.0 (integer) clock dividers.<br>2: 16.5 (fractional) clock dividers.<br>3: 24.5 (fractional) clock dividers. |
| 30 | DISABLE | RW | RW1C | 0 | Clock divider disable command (mutually exclusive with ENABLE). SW sets this field to '1' and HW sets this field to '0'.<br><br>The DIV_SEL and TYPE_SEL fields specify which divider is to be disabled.<br><br>The HW sets the DISABLE field to '0' immediately and the HW sets the DIV_XXX_CTL.EN field of the divider to '0' immediately. |
| 31 | ENABLE | RW | RW1C | 0 | Clock divider enable command (mutually exclusive with DISABLE). Typically, SW sets this field to '1' to enable a divider and HW sets this field to '0' to indicate that divider enabling has completed. When a divider is enabled, its integer and fractional (if present) counters are initialized to '0'. If a divider is to be re-enabled using different integer and fractional divider values, the SW should follow these steps:<br>0: Disable the divider using the DIV_CMD.DISABLE field.<br>1: Configure the divider's DIV_XXX_CTL register.<br>2: Enable the divider using the DIV_CMD_ENABLE field.<br><br>The DIV_SEL and TYPE_SEL fields specify which divider is to be enabled. The enabled divider may be phase aligned to either 'clk_pclk_root[i]' (typical usage) or to ANY enabled divider.<br><br>The PA_DIV_SEL and PA_TYPE_SEL fields specify the reference divider.<br><br>The HW sets the ENABLE field to '0' when the enabling is performed and the HW set the DIV_XXX_CTL.EN field of the divider to '1' when the enabling is performed. Note that enabling with phase alignment to a low frequency divider takes time. E.g. To align to a divider that generates a clock of 'clk_pclk_root[i]'/n (with n being the integer divider value INT_DIV+1), up to n cycles may be required to perform alignment. Phase alignment to 'clk_pclk_root[i]' takes affect immediately. SW can set this field to '0' during phase alignment to abort the enabling process. |

### 24.3.1.2 PERI_PCLK_GR_CLOCK_CTL

**Description:** Clock control
**Address:** 0x40040C00
**Offset:** 0xC00
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x3FF

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DIV_SEL [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:10] | | | | | | TYPE_SEL [9:8] | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | DIV_SEL | RW | R | 255 | Specifies one of the dividers of the divider type specified by TYPE_SEL.<br><br>If DIV_SEL is '255' and TYPE_SEL is '3' (default/reset value), no divider is specified and no clock control signal(s) are generated.<br><br>When transitioning a clock between two out-of-phase dividers, spurious clock control signals may be generated for one 'clk_pclk_root[i]' cycle during this transition. These clock control signals may cause a single clock period that is smaller than any of the two divider periods. To prevent these spurious clock signals, the clock multiplexer can be disconnected (DIV_SEL is '255' and TYPE_SEL is '3') for a transition time that is larger than the smaller of the two divider periods. |
| 8:9 | TYPE_SEL | RW | R | 3 | Specifies divider type:<br>0: 8.0 (integer) clock dividers.<br>1: 16.0 (integer) clock dividers.<br>2: 16.5 (fractional) clock dividers.<br>3: 24.5 (fractional) clock dividers. |

### 24.3.1.3 PERI_PCLK_GR_DIV_8_CTL

**Description:** Divider control (for 8.0 divider)
**Address:** 0x40041000
**Offset:** 0x1000
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Smallest of the divider types.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:1] | | | | | | | EN [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | INT8_DIV [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | EN | R | RW | 0 | Divider enabled. HW sets this field to '1' as a result of an ENABLE command. HW sets this field to '0' as a result on a DISABLE command.<br><br>Note that this field is retained. As a result, the divider does NOT have to be re-enabled after transitioning from DeepSleep to Active power mode. |
| 8:15 | INT8_DIV | RW | R | 0 | Integer division by (1+INT8_DIV). Allows for integer divisions in the range [1, 256]. Note: this type of divider does NOT allow for a fractional division.<br><br>For the generation of a divided clock, the integer division range is restricted to [2, 256].<br><br>For the generation of a 50/50 percent duty cycle digital divided clock, the integer division range is restricted to even numbers in the range [2, 256]. The generation of a 50/50 percent duty cycle analog divided clock has no restrictions.<br><br>Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to '0' when transitioning from DeepSleep to Active power mode. |

### 24.3.1.4 PERI_PCLK_GR_DIV_16_CTL

**Description:** Divider control (for 16.0 divider)
**Address:** 0x40041400
**Offset:** 0x1400
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:1] | | | | | | | EN [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | INT16_DIV [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | INT16_DIV [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | EN | R | RW | 0 | Divider enabled. HW sets this field to '1' as a result of an ENABLE command. HW sets this field to '0' as a result on a DISABLE command.<br><br>Note that this field is retained. As a result, the divider does NOT have to be re-enabled after transitioning from DeepSleep to Active power mode. |
| 8:23 | INT16_DIV | RW | R | 0 | Integer division by (1+INT16_DIV). Allows for integer divisions in the range [1, 65,536]. Note: this type of divider does NOT allow for a fractional division.<br><br>For the generation of a divided clock, the integer division range is restricted to [2, 65,536].<br><br>For the generation of a 50/50 percent duty cycle digital divided clock, the integer division range is restricted to even numbers in the range [2, 65,536]. The generation of a 50/50 percent duty cycle analog divided clock has no restrictions.<br><br>Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to '0' when transitioning from DeepSleep to Active power mode. |

### 24.3.1.5 PERI_PCLK_GR_DIV_24_5_CTL

**Description:** Divider control (for 24.5 divider)
**Address:** 0x40041C00
**Offset:** 0x1C00
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Largest of the divider types.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | FRAC5_DIV [7:3] | | | | | None [2:1] | | EN [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | INT24_DIV [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | INT24_DIV [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | INT24_DIV [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | EN | R | RW | 0 | Divider enabled. HW sets this field to '1' as a result of an ENABLE command. HW sets this field to '0' as a result on a DISABLE command.<br><br>Note that this field is retained. As a result, the divider does NOT have to be re-enabled after transitioning from DeepSleep to Active power mode. |
| 3:7 | FRAC5_DIV | RW | R | 0 | Fractional division by (FRAC5_DIV/32). Allows for fractional divisions in the range [0, 31/32]. Note that fractional division results in clock jitter as some clock periods may be 1 'clk_pclk_root[i]' cycle longer than other clock periods.<br><br>Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to '0' when transitioning from DeepSleep to Active power mode. |
| 8:31 | INT24_DIV | RW | R | 0 | Integer division by (1+INT24_DIV). Allows for integer divisions in the range [1, 16,777,216]. Note: combined with fractional division, this divider type allows for a division in the range [1, 16,777,216 31/32] in 1/32 increments.<br><br>For the generation of a divided clock, the integer division range is restricted to [2, 16,777,216 31/32].<br><br>For the generation of a 50/50 percent duty cycle divided clock, the division range is restricted to [2, 16,777,216].<br><br>Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to '0' when transitioning from DeepSleep to Active power mode. |

# 25 PROT

**Description** Protection
**Base Address** 0x40230000
**Size** 0x10000
**Slave Num** MMIO2 - 3

## 25.1 SMPU

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PROT_SMPU_MS0_CTL | 0x40230000 | FULL | Master 0 protection context control |
| PROT_SMPU_MS1_CTL | 0x40230004 | FULL | Master 1 protection context control<br>Note:P NS PC_MASK_15_TO_1 are not available for this register |
| PROT_SMPU_MS2_CTL | 0x40230008 | FULL | Master 2 protection context control<br>Note:P NS PC_MASK_15_TO_1 are not available for this register |
| PROT_SMPU_MS3_CTL | 0x4023000C | FULL | Master 3 protection context control<br>Note:P NS PC_MASK_15_TO_1 are not available for this register |
| PROT_SMPU_MS4_CTL | 0x40230010 | FULL | Master 4 protection context control<br>Note:P NS PC_MASK_15_TO_1 are not available for this register |
| PROT_SMPU_MS5_CTL | 0x40230014 | FULL | Master 5 protection context control |
| PROT_SMPU_MS9_CTL | 0x40230024 | FULL | Master 9 protection context control |
| PROT_SMPU_MS10_CTL | 0x40230028 | FULL | Master 10 protection context control |
| PROT_SMPU_MS13_CTL | 0x40230034 | FULL | Master 13 protection context control |
| PROT_SMPU_MS14_CTL | 0x40230038 | FULL | Master 14 protection context control |
| PROT_SMPU_MS15_CTL | 0x4023003C | FULL | Master 15 protection context control |

### 25.1.1 SMPU_STRUCT 0

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PROT_SMPU_SMPU_STRUCT0_ADDR0 | 0x40232000 | FULL | SMPU region address 0 (slave structure) |
| PROT_SMPU_SMPU_STRUCT0_ATT0 | 0x40232004 | FULL | SMPU region attributes 0 (slave structure) |
| PROT_SMPU_SMPU_STRUCT0_ADDR1 | 0x40232020 | FULL | SMPU region address 1 (master structure) |
| PROT_SMPU_SMPU_STRUCT0_ATT1 | 0x40232024 | FULL | SMPU region attributes 1 (master structure) |

### 25.1.2 SMPU_STRUCT 1

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PROT_SMPU_SMPU_STRUCT1_ADDR0 | 0x40232040 | FULL | SMPU region address 0 (slave structure) |
| PROT_SMPU_SMPU_STRUCT1_ATT0 | 0x40232044 | FULL | SMPU region attributes 0 (slave structure) |
| PROT_SMPU_SMPU_STRUCT1_ADDR1 | 0x40232060 | FULL | SMPU region address 1 (master structure) |
| PROT_SMPU_SMPU_STRUCT1_ATT1 | 0x40232064 | FULL | SMPU region attributes 1 (master structure) |

### 25.1.3 SMPU_STRUCT 2

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PROT_SMPU_SMPU_STRUCT2_ADDR0 | 0x40232080 | FULL | SMPU region address 0 (slave structure) |
| PROT_SMPU_SMPU_STRUCT2_ATT0 | 0x40232084 | FULL | SMPU region attributes 0 (slave structure) |
| PROT_SMPU_SMPU_STRUCT2_ADDR1 | 0x402320A0 | FULL | SMPU region address 1 (master structure) |
| PROT_SMPU_SMPU_STRUCT2_ATT1 | 0x402320A4 | FULL | SMPU region attributes 1 (master structure) |

### 25.1.4 SMPU_STRUCT 3

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PROT_SMPU_SMPU_STRUCT3_ADDR0 | 0x402320C0 | FULL | SMPU region address 0 (slave structure) |
| PROT_SMPU_SMPU_STRUCT3_ATT0 | 0x402320C4 | FULL | SMPU region attributes 0 (slave structure) |
| PROT_SMPU_SMPU_STRUCT3_ADDR1 | 0x402320E0 | FULL | SMPU region address 1 (master structure) |
| PROT_SMPU_SMPU_STRUCT3_ATT1 | 0x402320E4 | FULL | SMPU region attributes 1 (master structure) |

### 25.1.5 SMPU_STRUCT 4

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PROT_SMPU_SMPU_STRUCT4_ADDR0 | 0x40232100 | FULL | SMPU region address 0 (slave structure) |
| PROT_SMPU_SMPU_STRUCT4_ATT0 | 0x40232104 | FULL | SMPU region attributes 0 (slave structure) |
| PROT_SMPU_SMPU_STRUCT4_ADDR1 | 0x40232120 | FULL | SMPU region address 1 (master structure) |
| PROT_SMPU_SMPU_STRUCT4_ATT1 | 0x40232124 | FULL | SMPU region attributes 1 (master structure) |

### 25.1.6 SMPU_STRUCT 5

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PROT_SMPU_SMPU_STRUCT5_ADDR0 | 0x40232140 | FULL | SMPU region address 0 (slave structure) |
| PROT_SMPU_SMPU_STRUCT5_ATT0 | 0x40232144 | FULL | SMPU region attributes 0 (slave structure) |
| PROT_SMPU_SMPU_STRUCT5_ADDR1 | 0x40232160 | FULL | SMPU region address 1 (master structure) |
| PROT_SMPU_SMPU_STRUCT5_ATT1 | 0x40232164 | FULL | SMPU region attributes 1 (master structure) |

### 25.1.7 SMPU_STRUCT 6

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PROT_SMPU_SMPU_STRUCT6_ADDR0 | 0x40232180 | FULL | SMPU region address 0 (slave structure) |
| PROT_SMPU_SMPU_STRUCT6_ATT0 | 0x40232184 | FULL | SMPU region attributes 0 (slave structure) |
| PROT_SMPU_SMPU_STRUCT6_ADDR1 | 0x402321A0 | FULL | SMPU region address 1 (master structure) |
| PROT_SMPU_SMPU_STRUCT6_ATT1 | 0x402321A4 | FULL | SMPU region attributes 1 (master structure) |

### 25.1.8 SMPU_STRUCT 7

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PROT_SMPU_SMPU_STRUCT7_ADDR0 | 0x402321C0 | FULL | SMPU region address 0 (slave structure) |
| PROT_SMPU_SMPU_STRUCT7_ATT0 | 0x402321C4 | FULL | SMPU region attributes 0 (slave structure) |
| PROT_SMPU_SMPU_STRUCT7_ADDR1 | 0x402321E0 | FULL | SMPU region address 1 (master structure) |
| PROT_SMPU_SMPU_STRUCT7_ATT1 | 0x402321E4 | FULL | SMPU region attributes 1 (master structure) |

### 25.1.9 SMPU_STRUCT 8

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PROT_SMPU_SMPU_STRUCT8_ADDR0 | 0x40232200 | FULL | SMPU region address 0 (slave structure) |
| PROT_SMPU_SMPU_STRUCT8_ATT0 | 0x40232204 | FULL | SMPU region attributes 0 (slave structure) |
| PROT_SMPU_SMPU_STRUCT8_ADDR1 | 0x40232220 | FULL | SMPU region address 1 (master structure) |
| PROT_SMPU_SMPU_STRUCT8_ATT1 | 0x40232224 | FULL | SMPU region attributes 1 (master structure) |

### 25.1.10 SMPU_STRUCT 9

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PROT_SMPU_SMPU_STRUCT9_ADDR0 | 0x40232240 | FULL | SMPU region address 0 (slave structure) |
| PROT_SMPU_SMPU_STRUCT9_ATT0 | 0x40232244 | FULL | SMPU region attributes 0 (slave structure) |
| PROT_SMPU_SMPU_STRUCT9_ADDR1 | 0x40232260 | FULL | SMPU region address 1 (master structure) |
| PROT_SMPU_SMPU_STRUCT9_ATT1 | 0x40232264 | FULL | SMPU region attributes 1 (master structure) |

### 25.1.11 SMPU_STRUCT 10

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PROT_SMPU_SMPU_STRUCT10_ADDR0 | 0x40232280 | FULL | SMPU region address 0 (slave structure) |
| PROT_SMPU_SMPU_STRUCT10_ATT0 | 0x40232284 | FULL | SMPU region attributes 0 (slave structure) |
| PROT_SMPU_SMPU_STRUCT10_ADDR1 | 0x402322A0 | FULL | SMPU region address 1 (master structure) |
| PROT_SMPU_SMPU_STRUCT10_ATT1 | 0x402322A4 | FULL | SMPU region attributes 1 (master structure) |

### 25.1.12 SMPU_STRUCT 11

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PROT_SMPU_SMPU_STRUCT11_ADDR0 | 0x402322C0 | FULL | SMPU region address 0 (slave structure) |
| PROT_SMPU_SMPU_STRUCT11_ATT0 | 0x402322C4 | FULL | SMPU region attributes 0 (slave structure) |
| PROT_SMPU_SMPU_STRUCT11_ADDR1 | 0x402322E0 | FULL | SMPU region address 1 (master structure) |
| PROT_SMPU_SMPU_STRUCT11_ATT1 | 0x402322E4 | FULL | SMPU region attributes 1 (master structure) |

### 25.1.13 SMPU_STRUCT 12

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PROT_SMPU_SMPU_STRUCT12_ADDR0 | 0x40232300 | FULL | SMPU region address 0 (slave structure) |
| PROT_SMPU_SMPU_STRUCT12_ATT0 | 0x40232304 | FULL | SMPU region attributes 0 (slave structure) |
| PROT_SMPU_SMPU_STRUCT12_ADDR1 | 0x40232320 | FULL | SMPU region address 1 (master structure) |
| PROT_SMPU_SMPU_STRUCT12_ATT1 | 0x40232324 | FULL | SMPU region attributes 1 (master structure) |

### 25.1.14 SMPU_STRUCT 13

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PROT_SMPU_SMPU_STRUCT13_ADDR0 | 0x40232340 | FULL | SMPU region address 0 (slave structure) |
| PROT_SMPU_SMPU_STRUCT13_ATT0 | 0x40232344 | FULL | SMPU region attributes 0 (slave structure) |
| PROT_SMPU_SMPU_STRUCT13_ADDR1 | 0x40232360 | FULL | SMPU region address 1 (master structure) |
| PROT_SMPU_SMPU_STRUCT13_ATT1 | 0x40232364 | FULL | SMPU region attributes 1 (master structure) |

### 25.1.15 SMPU_STRUCT 14

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PROT_SMPU_SMPU_STRUCT14_ADDR0 | 0x40232380 | SECURE - READ | SMPU region address 0 (slave structure) |
| PROT_SMPU_SMPU_STRUCT14_ATT0 | 0x40232384 | SECURE - READ | SMPU region attributes 0 (slave structure) |
| PROT_SMPU_SMPU_STRUCT14_ADDR1 | 0x402323A0 | SECURE - READ | SMPU region address 1 (master structure) |
| PROT_SMPU_SMPU_STRUCT14_ATT1 | 0x402323A4 | SECURE - READ | SMPU region attributes 1 (master structure) |

### 25.1.16 SMPU_STRUCT 15

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PROT_SMPU_SMPU_STRUCT15_ADDR0 | 0x402323C0 | SECURE - READ | SMPU region address 0 (slave structure) |
| PROT_SMPU_SMPU_STRUCT15_ATT0 | 0x402323C4 | SECURE - READ | SMPU region attributes 0 (slave structure) |
| PROT_SMPU_SMPU_STRUCT15_ADDR1 | 0x402323E0 | SECURE - READ | SMPU region address 1 (master structure) |
| PROT_SMPU_SMPU_STRUCT15_ATT1 | 0x402323E4 | SECURE - READ | SMPU region attributes 1 (master structure) |

## 25.2 MPU 0

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PROT_MPU0_MS_CTL | 0x40234000 | FULL | Master control |
| PROT_MPU0_MS_CTL_READ_MIR0 | 0x40234004 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR1 | 0x40234008 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR2 | 0x4023400C | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR3 | 0x40234010 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR4 | 0x40234014 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR5 | 0x40234018 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR6 | 0x4023401C | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR7 | 0x40234020 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR8 | 0x40234024 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR9 | 0x40234028 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR10 | 0x4023402C | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR11 | 0x40234030 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR12 | 0x40234034 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR13 | 0x40234038 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR14 | 0x4023403C | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR15 | 0x40234040 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR16 | 0x40234044 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR17 | 0x40234048 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR18 | 0x4023404C | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR19 | 0x40234050 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR20 | 0x40234054 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR21 | 0x40234058 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR22 | 0x4023405C | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR23 | 0x40234060 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR24 | 0x40234064 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR25 | 0x40234068 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR26 | 0x4023406C | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR27 | 0x40234070 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR28 | 0x40234074 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR29 | 0x40234078 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR30 | 0x4023407C | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR31 | 0x40234080 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR32 | 0x40234084 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR33 | 0x40234088 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR34 | 0x4023408C | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR35 | 0x40234090 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR36 | 0x40234094 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR37 | 0x40234098 | FULL | Master control read mirror |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PROT_MPU0_MS_CTL_READ_MIR38 | 0x4023409C | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR39 | 0x402340A0 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR40 | 0x402340A4 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR41 | 0x402340A8 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR42 | 0x402340AC | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR43 | 0x402340B0 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR44 | 0x402340B4 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR45 | 0x402340B8 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR46 | 0x402340BC | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR47 | 0x402340C0 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR48 | 0x402340C4 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR49 | 0x402340C8 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR50 | 0x402340CC | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR51 | 0x402340D0 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR52 | 0x402340D4 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR53 | 0x402340D8 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR54 | 0x402340DC | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR55 | 0x402340E0 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR56 | 0x402340E4 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR57 | 0x402340E8 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR58 | 0x402340EC | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR59 | 0x402340F0 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR60 | 0x402340F4 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR61 | 0x402340F8 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR62 | 0x402340FC | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR63 | 0x40234100 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR64 | 0x40234104 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR65 | 0x40234108 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR66 | 0x4023410C | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR67 | 0x40234110 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR68 | 0x40234114 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR69 | 0x40234118 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR70 | 0x4023411C | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR71 | 0x40234120 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR72 | 0x40234124 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR73 | 0x40234128 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR74 | 0x4023412C | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR75 | 0x40234130 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR76 | 0x40234134 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR77 | 0x40234138 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR78 | 0x4023413C | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR79 | 0x40234140 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR80 | 0x40234144 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR81 | 0x40234148 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR82 | 0x4023414C | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR83 | 0x40234150 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR84 | 0x40234154 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR85 | 0x40234158 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR86 | 0x4023415C | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR87 | 0x40234160 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR88 | 0x40234164 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR89 | 0x40234168 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR90 | 0x4023416C | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR91 | 0x40234170 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR92 | 0x40234174 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR93 | 0x40234178 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR94 | 0x4023417C | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR95 | 0x40234180 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR96 | 0x40234184 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR97 | 0x40234188 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR98 | 0x4023418C | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR99 | 0x40234190 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR100 | 0x40234194 | FULL | Master control read mirror |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PROT_MPU0_MS_CTL_READ_MIR101 | 0x40234198 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR102 | 0x4023419C | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR103 | 0x402341A0 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR104 | 0x402341A4 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR105 | 0x402341A8 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR106 | 0x402341AC | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR107 | 0x402341B0 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR108 | 0x402341B4 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR109 | 0x402341B8 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR110 | 0x402341BC | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR111 | 0x402341C0 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR112 | 0x402341C4 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR113 | 0x402341C8 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR114 | 0x402341CC | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR115 | 0x402341D0 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR116 | 0x402341D4 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR117 | 0x402341D8 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR118 | 0x402341DC | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR119 | 0x402341E0 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR120 | 0x402341E4 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR121 | 0x402341E8 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR122 | 0x402341EC | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR123 | 0x402341F0 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR124 | 0x402341F4 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR125 | 0x402341F8 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR126 | 0x402341FC | FULL | Master control read mirror |

## 25.3 MPU 5

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PROT_MPU5_MS_CTL | 0x40235400 | FULL | Master control<br>Note:PC_SAVED is not available for this register |
| PROT_MPU5_MS_CTL_READ_MIR0 | 0x40235404 | FULL | Master control read mirror<br>Note:PC_SAVED is not available for this register |
| PROT_MPU5_MS_CTL_READ_MIR1 | 0x40235408 | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR2 | 0x4023540C | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR3 | 0x40235410 | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR4 | 0x40235414 | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR5 | 0x40235418 | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR6 | 0x4023541C | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR7 | 0x40235420 | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR8 | 0x40235424 | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR9 | 0x40235428 | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR10 | 0x4023542C | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR11 | 0x40235430 | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR12 | 0x40235434 | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR13 | 0x40235438 | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR14 | 0x4023543C | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR15 | 0x40235440 | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR16 | 0x40235444 | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR17 | 0x40235448 | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR18 | 0x4023544C | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR19 | 0x40235450 | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR20 | 0x40235454 | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR21 | 0x40235458 | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR22 | 0x4023545C | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR23 | 0x40235460 | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR24 | 0x40235464 | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR25 | 0x40235468 | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR26 | 0x4023546C | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR27 | 0x40235470 | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR28 | 0x40235474 | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR29 | 0x40235478 | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR30 | 0x4023547C | FULL | Master control read mirror |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PROT_MPU5_MS_CTL_READ_MIR31 | 0x40235480 | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR32 | 0x40235484 | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR33 | 0x40235488 | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR34 | 0x4023548C | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR35 | 0x40235490 | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR36 | 0x40235494 | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR37 | 0x40235498 | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR38 | 0x4023549C | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR39 | 0x402354A0 | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR40 | 0x402354A4 | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR41 | 0x402354A8 | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR42 | 0x402354AC | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR43 | 0x402354B0 | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR44 | 0x402354B4 | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR45 | 0x402354B8 | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR46 | 0x402354BC | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR47 | 0x402354C0 | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR48 | 0x402354C4 | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR49 | 0x402354C8 | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR50 | 0x402354CC | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR51 | 0x402354D0 | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR52 | 0x402354D4 | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR53 | 0x402354D8 | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR54 | 0x402354DC | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR55 | 0x402354E0 | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR56 | 0x402354E4 | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR57 | 0x402354E8 | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR58 | 0x402354EC | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR59 | 0x402354F0 | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR60 | 0x402354F4 | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR61 | 0x402354F8 | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR62 | 0x402354FC | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR63 | 0x40235500 | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR64 | 0x40235504 | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR65 | 0x40235508 | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR66 | 0x4023550C | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR67 | 0x40235510 | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR68 | 0x40235514 | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR69 | 0x40235518 | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR70 | 0x4023551C | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR71 | 0x40235520 | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR72 | 0x40235524 | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR73 | 0x40235528 | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR74 | 0x4023552C | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR75 | 0x40235530 | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR76 | 0x40235534 | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR77 | 0x40235538 | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR78 | 0x4023553C | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR79 | 0x40235540 | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR80 | 0x40235544 | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR81 | 0x40235548 | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR82 | 0x4023554C | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR83 | 0x40235550 | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR84 | 0x40235554 | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR85 | 0x40235558 | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR86 | 0x4023555C | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR87 | 0x40235560 | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR88 | 0x40235564 | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR89 | 0x40235568 | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR90 | 0x4023556C | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR91 | 0x40235570 | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR92 | 0x40235574 | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR93 | 0x40235578 | FULL | Master control read mirror |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PROT_MPU5_MS_CTL_READ_MIR94 | 0x4023557C | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR95 | 0x40235580 | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR96 | 0x40235584 | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR97 | 0x40235588 | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR98 | 0x4023558C | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR99 | 0x40235590 | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR100 | 0x40235594 | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR101 | 0x40235598 | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR102 | 0x4023559C | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR103 | 0x402355A0 | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR104 | 0x402355A4 | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR105 | 0x402355A8 | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR106 | 0x402355AC | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR107 | 0x402355B0 | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR108 | 0x402355B4 | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR109 | 0x402355B8 | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR110 | 0x402355BC | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR111 | 0x402355C0 | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR112 | 0x402355C4 | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR113 | 0x402355C8 | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR114 | 0x402355CC | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR115 | 0x402355D0 | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR116 | 0x402355D4 | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR117 | 0x402355D8 | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR118 | 0x402355DC | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR119 | 0x402355E0 | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR120 | 0x402355E4 | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR121 | 0x402355E8 | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR122 | 0x402355EC | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR123 | 0x402355F0 | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR124 | 0x402355F4 | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR125 | 0x402355F8 | FULL | Master control read mirror |
| PROT_MPU5_MS_CTL_READ_MIR126 | 0x402355FC | FULL | Master control read mirror |

### 25.3.1 MPU_STRUCT 0

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PROT_MPU5_MPU_STRUCT0_ADDR | 0x40235600 | FULL | MPU region address |
| PROT_MPU5_MPU_STRUCT0_ATT | 0x40235604 | FULL | MPU region attrributes |

### 25.3.2 MPU_STRUCT 1

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PROT_MPU5_MPU_STRUCT1_ADDR | 0x40235620 | FULL | MPU region address |
| PROT_MPU5_MPU_STRUCT1_ATT | 0x40235624 | FULL | MPU region attrributes |

### 25.3.3 MPU_STRUCT 2

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PROT_MPU5_MPU_STRUCT2_ADDR | 0x40235640 | FULL | MPU region address |
| PROT_MPU5_MPU_STRUCT2_ATT | 0x40235644 | FULL | MPU region attrributes |

### 25.3.4 MPU_STRUCT 3

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PROT_MPU5_MPU_STRUCT3_ADDR | 0x40235660 | FULL | MPU region address |
| PROT_MPU5_MPU_STRUCT3_ATT | 0x40235664 | FULL | MPU region attrributes |

### 25.3.5 MPU_STRUCT 4

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PROT_MPU5_MPU_STRUCT4_ADDR | 0x40235680 | FULL | MPU region address |
| PROT_MPU5_MPU_STRUCT4_ATT | 0x40235684 | FULL | MPU region attrributes |

### 25.3.6 MPU_STRUCT 5

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PROT_MPU5_MPU_STRUCT5_ADDR | 0x402356A0 | FULL | MPU region address |
| PROT_MPU5_MPU_STRUCT5_ATT | 0x402356A4 | FULL | MPU region attrributes |

### 25.3.7 MPU_STRUCT 6

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PROT_MPU5_MPU_STRUCT6_ADDR | 0x402356C0 | FULL | MPU region address |
| PROT_MPU5_MPU_STRUCT6_ATT | 0x402356C4 | FULL | MPU region attrributes |

### 25.3.8 MPU_STRUCT 7

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PROT_MPU5_MPU_STRUCT7_ADDR | 0x402356E0 | FULL | MPU region address |
| PROT_MPU5_MPU_STRUCT7_ATT | 0x402356E4 | FULL | MPU region attrributes |

## 25.4 MPU 9

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PROT_MPU9_MS_CTL | 0x40236400 | FULL | Master control<br>Note:PC_SAVED is not available for this register |
| PROT_MPU9_MS_CTL_READ_MIR0 | 0x40236404 | FULL | Master control read mirror<br>Note:PC_SAVED is not available for this register |
| PROT_MPU9_MS_CTL_READ_MIR1 | 0x40236408 | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR2 | 0x4023640C | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR3 | 0x40236410 | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR4 | 0x40236414 | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR5 | 0x40236418 | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR6 | 0x4023641C | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR7 | 0x40236420 | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR8 | 0x40236424 | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR9 | 0x40236428 | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR10 | 0x4023642C | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR11 | 0x40236430 | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR12 | 0x40236434 | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR13 | 0x40236438 | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR14 | 0x4023643C | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR15 | 0x40236440 | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR16 | 0x40236444 | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR17 | 0x40236448 | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR18 | 0x4023644C | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR19 | 0x40236450 | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR20 | 0x40236454 | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR21 | 0x40236458 | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR22 | 0x4023645C | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR23 | 0x40236460 | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR24 | 0x40236464 | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR25 | 0x40236468 | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR26 | 0x4023646C | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR27 | 0x40236470 | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR28 | 0x40236474 | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR29 | 0x40236478 | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR30 | 0x4023647C | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR31 | 0x40236480 | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR32 | 0x40236484 | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR33 | 0x40236488 | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR34 | 0x4023648C | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR35 | 0x40236490 | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR36 | 0x40236494 | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR37 | 0x40236498 | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR38 | 0x4023649C | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR39 | 0x402364A0 | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR40 | 0x402364A4 | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR41 | 0x402364A8 | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR42 | 0x402364AC | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR43 | 0x402364B0 | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR44 | 0x402364B4 | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR45 | 0x402364B8 | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR46 | 0x402364BC | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR47 | 0x402364C0 | FULL | Master control read mirror |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PROT_MPU9_MS_CTL_READ_MIR48 | 0x402364C4 | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR49 | 0x402364C8 | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR50 | 0x402364CC | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR51 | 0x402364D0 | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR52 | 0x402364D4 | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR53 | 0x402364D8 | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR54 | 0x402364DC | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR55 | 0x402364E0 | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR56 | 0x402364E4 | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR57 | 0x402364E8 | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR58 | 0x402364EC | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR59 | 0x402364F0 | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR60 | 0x402364F4 | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR61 | 0x402364F8 | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR62 | 0x402364FC | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR63 | 0x40236500 | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR64 | 0x40236504 | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR65 | 0x40236508 | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR66 | 0x4023650C | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR67 | 0x40236510 | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR68 | 0x40236514 | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR69 | 0x40236518 | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR70 | 0x4023651C | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR71 | 0x40236520 | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR72 | 0x40236524 | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR73 | 0x40236528 | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR74 | 0x4023652C | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR75 | 0x40236530 | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR76 | 0x40236534 | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR77 | 0x40236538 | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR78 | 0x4023653C | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR79 | 0x40236540 | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR80 | 0x40236544 | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR81 | 0x40236548 | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR82 | 0x4023654C | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR83 | 0x40236550 | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR84 | 0x40236554 | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR85 | 0x40236558 | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR86 | 0x4023655C | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR87 | 0x40236560 | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR88 | 0x40236564 | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR89 | 0x40236568 | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR90 | 0x4023656C | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR91 | 0x40236570 | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR92 | 0x40236574 | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR93 | 0x40236578 | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR94 | 0x4023657C | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR95 | 0x40236580 | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR96 | 0x40236584 | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR97 | 0x40236588 | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR98 | 0x4023658C | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR99 | 0x40236590 | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR100 | 0x40236594 | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR101 | 0x40236598 | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR102 | 0x4023659C | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR103 | 0x402365A0 | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR104 | 0x402365A4 | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR105 | 0x402365A8 | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR106 | 0x402365AC | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR107 | 0x402365B0 | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR108 | 0x402365B4 | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR109 | 0x402365B8 | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR110 | 0x402365BC | FULL | Master control read mirror |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PROT_MPU9_MS_CTL_READ_MIR111 | 0x402365C0 | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR112 | 0x402365C4 | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR113 | 0x402365C8 | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR114 | 0x402365CC | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR115 | 0x402365D0 | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR116 | 0x402365D4 | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR117 | 0x402365D8 | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR118 | 0x402365DC | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR119 | 0x402365E0 | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR120 | 0x402365E4 | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR121 | 0x402365E8 | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR122 | 0x402365EC | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR123 | 0x402365F0 | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR124 | 0x402365F4 | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR125 | 0x402365F8 | FULL | Master control read mirror |
| PROT_MPU9_MS_CTL_READ_MIR126 | 0x402365FC | FULL | Master control read mirror |

### 25.4.1 MPU_STRUCT 0

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PROT_MPU9_MPU_STRUCT0_ADDR | 0x40236600 | FULL | MPU region address |
| PROT_MPU9_MPU_STRUCT0_ATT | 0x40236604 | FULL | MPU region attrributes |

### 25.4.2 MPU_STRUCT 1

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PROT_MPU9_MPU_STRUCT1_ADDR | 0x40236620 | FULL | MPU region address |
| PROT_MPU9_MPU_STRUCT1_ATT | 0x40236624 | FULL | MPU region attrributes |

### 25.4.3 MPU_STRUCT 2

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PROT_MPU9_MPU_STRUCT2_ADDR | 0x40236640 | FULL | MPU region address |
| PROT_MPU9_MPU_STRUCT2_ATT | 0x40236644 | FULL | MPU region attrributes |

### 25.4.4 MPU_STRUCT 3

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PROT_MPU9_MPU_STRUCT3_ADDR | 0x40236660 | FULL | MPU region address |
| PROT_MPU9_MPU_STRUCT3_ATT | 0x40236664 | FULL | MPU region attrributes |

### 25.4.5 MPU_STRUCT 4

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PROT_MPU9_MPU_STRUCT4_ADDR | 0x40236680 | FULL | MPU region address |
| PROT_MPU9_MPU_STRUCT4_ATT | 0x40236684 | FULL | MPU region attrributes |

### 25.4.6 MPU_STRUCT 5

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PROT_MPU9_MPU_STRUCT5_ADDR | 0x402366A0 | FULL | MPU region address |
| PROT_MPU9_MPU_STRUCT5_ATT | 0x402366A4 | FULL | MPU region attrributes |

### 25.4.7 MPU_STRUCT 6

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PROT_MPU9_MPU_STRUCT6_ADDR | 0x402366C0 | FULL | MPU region address |
| PROT_MPU9_MPU_STRUCT6_ATT | 0x402366C4 | FULL | MPU region attrributes |

### 25.4.8 MPU_STRUCT 7

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PROT_MPU9_MPU_STRUCT7_ADDR | 0x402366E0 | FULL | MPU region address |
| PROT_MPU9_MPU_STRUCT7_ATT | 0x402366E4 | FULL | MPU region attrributes |

## 25.5 MPU 10

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PROT_MPU10_MS_CTL | 0x40236800 | FULL | Master control<br>Note:PC_SAVED is not available for this register |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PROT_MPU10_MS_CTL_READ_MIR0 | 0x40236804 | FULL | Master control read mirror<br>Note:PC_SAVED is not available for this register |
| PROT_MPU10_MS_CTL_READ_MIR1 | 0x40236808 | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR2 | 0x4023680C | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR3 | 0x40236810 | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR4 | 0x40236814 | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR5 | 0x40236818 | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR6 | 0x4023681C | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR7 | 0x40236820 | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR8 | 0x40236824 | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR9 | 0x40236828 | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR10 | 0x4023682C | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR11 | 0x40236830 | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR12 | 0x40236834 | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR13 | 0x40236838 | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR14 | 0x4023683C | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR15 | 0x40236840 | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR16 | 0x40236844 | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR17 | 0x40236848 | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR18 | 0x4023684C | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR19 | 0x40236850 | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR20 | 0x40236854 | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR21 | 0x40236858 | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR22 | 0x4023685C | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR23 | 0x40236860 | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR24 | 0x40236864 | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR25 | 0x40236868 | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR26 | 0x4023686C | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR27 | 0x40236870 | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR28 | 0x40236874 | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR29 | 0x40236878 | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR30 | 0x4023687C | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR31 | 0x40236880 | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR32 | 0x40236884 | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR33 | 0x40236888 | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR34 | 0x4023688C | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR35 | 0x40236890 | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR36 | 0x40236894 | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR37 | 0x40236898 | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR38 | 0x4023689C | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR39 | 0x402368A0 | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR40 | 0x402368A4 | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR41 | 0x402368A8 | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR42 | 0x402368AC | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR43 | 0x402368B0 | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR44 | 0x402368B4 | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR45 | 0x402368B8 | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR46 | 0x402368BC | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR47 | 0x402368C0 | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR48 | 0x402368C4 | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR49 | 0x402368C8 | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR50 | 0x402368CC | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR51 | 0x402368D0 | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR52 | 0x402368D4 | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR53 | 0x402368D8 | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR54 | 0x402368DC | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR55 | 0x402368E0 | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR56 | 0x402368E4 | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR57 | 0x402368E8 | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR58 | 0x402368EC | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR59 | 0x402368F0 | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR60 | 0x402368F4 | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR61 | 0x402368F8 | FULL | Master control read mirror |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PROT_MPU10_MS_CTL_READ_MIR62 | 0x402368FC | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR63 | 0x40236900 | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR64 | 0x40236904 | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR65 | 0x40236908 | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR66 | 0x4023690C | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR67 | 0x40236910 | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR68 | 0x40236914 | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR69 | 0x40236918 | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR70 | 0x4023691C | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR71 | 0x40236920 | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR72 | 0x40236924 | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR73 | 0x40236928 | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR74 | 0x4023692C | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR75 | 0x40236930 | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR76 | 0x40236934 | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR77 | 0x40236938 | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR78 | 0x4023693C | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR79 | 0x40236940 | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR80 | 0x40236944 | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR81 | 0x40236948 | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR82 | 0x4023694C | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR83 | 0x40236950 | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR84 | 0x40236954 | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR85 | 0x40236958 | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR86 | 0x4023695C | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR87 | 0x40236960 | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR88 | 0x40236964 | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR89 | 0x40236968 | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR90 | 0x4023696C | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR91 | 0x40236970 | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR92 | 0x40236974 | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR93 | 0x40236978 | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR94 | 0x4023697C | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR95 | 0x40236980 | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR96 | 0x40236984 | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR97 | 0x40236988 | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR98 | 0x4023698C | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR99 | 0x40236990 | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR100 | 0x40236994 | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR101 | 0x40236998 | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR102 | 0x4023699C | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR103 | 0x402369A0 | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR104 | 0x402369A4 | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR105 | 0x402369A8 | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR106 | 0x402369AC | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR107 | 0x402369B0 | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR108 | 0x402369B4 | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR109 | 0x402369B8 | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR110 | 0x402369BC | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR111 | 0x402369C0 | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR112 | 0x402369C4 | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR113 | 0x402369C8 | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR114 | 0x402369CC | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR115 | 0x402369D0 | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR116 | 0x402369D4 | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR117 | 0x402369D8 | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR118 | 0x402369DC | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR119 | 0x402369E0 | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR120 | 0x402369E4 | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR121 | 0x402369E8 | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR122 | 0x402369EC | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR123 | 0x402369F0 | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR124 | 0x402369F4 | FULL | Master control read mirror |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PROT_MPU10_MS_CTL_READ_MIR125 | 0x402369F8 | FULL | Master control read mirror |
| PROT_MPU10_MS_CTL_READ_MIR126 | 0x402369FC | FULL | Master control read mirror |

### 25.5.1 MPU_STRUCT 0

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PROT_MPU10_MPU_STRUCT0_ADDR | 0x40236A00 | FULL | MPU region address |
| PROT_MPU10_MPU_STRUCT0_ATT | 0x40236A04 | FULL | MPU region attrributes |

### 25.5.2 MPU_STRUCT 1

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PROT_MPU10_MPU_STRUCT1_ADDR | 0x40236A20 | FULL | MPU region address |
| PROT_MPU10_MPU_STRUCT1_ATT | 0x40236A24 | FULL | MPU region attrributes |

### 25.5.3 MPU_STRUCT 2

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PROT_MPU10_MPU_STRUCT2_ADDR | 0x40236A40 | FULL | MPU region address |
| PROT_MPU10_MPU_STRUCT2_ATT | 0x40236A44 | FULL | MPU region attrributes |

### 25.5.4 MPU_STRUCT 3

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PROT_MPU10_MPU_STRUCT3_ADDR | 0x40236A60 | FULL | MPU region address |
| PROT_MPU10_MPU_STRUCT3_ATT | 0x40236A64 | FULL | MPU region attrributes |

### 25.5.5 MPU_STRUCT 4

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PROT_MPU10_MPU_STRUCT4_ADDR | 0x40236A80 | FULL | MPU region address |
| PROT_MPU10_MPU_STRUCT4_ATT | 0x40236A84 | FULL | MPU region attrributes |

### 25.5.6 MPU_STRUCT 5

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PROT_MPU10_MPU_STRUCT5_ADDR | 0x40236AA0 | FULL | MPU region address |
| PROT_MPU10_MPU_STRUCT5_ATT | 0x40236AA4 | FULL | MPU region attrributes |

### 25.5.7 MPU_STRUCT 6

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PROT_MPU10_MPU_STRUCT6_ADDR | 0x40236AC0 | FULL | MPU region address |
| PROT_MPU10_MPU_STRUCT6_ATT | 0x40236AC4 | FULL | MPU region attrributes |

### 25.5.8 MPU_STRUCT 7

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PROT_MPU10_MPU_STRUCT7_ADDR | 0x40236AE0 | FULL | MPU region address |
| PROT_MPU10_MPU_STRUCT7_ATT | 0x40236AE4 | FULL | MPU region attrributes |

## 25.6 MPU 13

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PROT_MPU13_MS_CTL | 0x40237400 | FULL | Master control<br>Note:PC_SAVED is not available for this register |
| PROT_MPU13_MS_CTL_READ_MIR0 | 0x40237404 | FULL | Master control read mirror<br>Note:PC_SAVED is not available for this register |
| PROT_MPU13_MS_CTL_READ_MIR1 | 0x40237408 | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR2 | 0x4023740C | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR3 | 0x40237410 | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR4 | 0x40237414 | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR5 | 0x40237418 | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR6 | 0x4023741C | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR7 | 0x40237420 | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR8 | 0x40237424 | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR9 | 0x40237428 | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR10 | 0x4023742C | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR11 | 0x40237430 | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR12 | 0x40237434 | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR13 | 0x40237438 | FULL | Master control read mirror |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PROT_MPU13_MS_CTL_READ_MIR14 | 0x4023743C | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR15 | 0x40237440 | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR16 | 0x40237444 | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR17 | 0x40237448 | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR18 | 0x4023744C | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR19 | 0x40237450 | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR20 | 0x40237454 | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR21 | 0x40237458 | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR22 | 0x4023745C | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR23 | 0x40237460 | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR24 | 0x40237464 | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR25 | 0x40237468 | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR26 | 0x4023746C | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR27 | 0x40237470 | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR28 | 0x40237474 | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR29 | 0x40237478 | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR30 | 0x4023747C | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR31 | 0x40237480 | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR32 | 0x40237484 | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR33 | 0x40237488 | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR34 | 0x4023748C | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR35 | 0x40237490 | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR36 | 0x40237494 | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR37 | 0x40237498 | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR38 | 0x4023749C | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR39 | 0x402374A0 | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR40 | 0x402374A4 | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR41 | 0x402374A8 | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR42 | 0x402374AC | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR43 | 0x402374B0 | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR44 | 0x402374B4 | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR45 | 0x402374B8 | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR46 | 0x402374BC | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR47 | 0x402374C0 | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR48 | 0x402374C4 | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR49 | 0x402374C8 | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR50 | 0x402374CC | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR51 | 0x402374D0 | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR52 | 0x402374D4 | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR53 | 0x402374D8 | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR54 | 0x402374DC | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR55 | 0x402374E0 | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR56 | 0x402374E4 | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR57 | 0x402374E8 | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR58 | 0x402374EC | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR59 | 0x402374F0 | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR60 | 0x402374F4 | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR61 | 0x402374F8 | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR62 | 0x402374FC | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR63 | 0x40237500 | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR64 | 0x40237504 | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR65 | 0x40237508 | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR66 | 0x4023750C | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR67 | 0x40237510 | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR68 | 0x40237514 | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR69 | 0x40237518 | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR70 | 0x4023751C | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR71 | 0x40237520 | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR72 | 0x40237524 | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR73 | 0x40237528 | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR74 | 0x4023752C | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR75 | 0x40237530 | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR76 | 0x40237534 | FULL | Master control read mirror |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PROT_MPU13_MS_CTL_READ_MIR77 | 0x40237538 | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR78 | 0x4023753C | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR79 | 0x40237540 | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR80 | 0x40237544 | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR81 | 0x40237548 | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR82 | 0x4023754C | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR83 | 0x40237550 | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR84 | 0x40237554 | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR85 | 0x40237558 | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR86 | 0x4023755C | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR87 | 0x40237560 | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR88 | 0x40237564 | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR89 | 0x40237568 | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR90 | 0x4023756C | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR91 | 0x40237570 | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR92 | 0x40237574 | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR93 | 0x40237578 | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR94 | 0x4023757C | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR95 | 0x40237580 | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR96 | 0x40237584 | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR97 | 0x40237588 | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR98 | 0x4023758C | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR99 | 0x40237590 | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR100 | 0x40237594 | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR101 | 0x40237598 | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR102 | 0x4023759C | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR103 | 0x402375A0 | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR104 | 0x402375A4 | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR105 | 0x402375A8 | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR106 | 0x402375AC | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR107 | 0x402375B0 | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR108 | 0x402375B4 | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR109 | 0x402375B8 | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR110 | 0x402375BC | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR111 | 0x402375C0 | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR112 | 0x402375C4 | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR113 | 0x402375C8 | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR114 | 0x402375CC | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR115 | 0x402375D0 | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR116 | 0x402375D4 | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR117 | 0x402375D8 | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR118 | 0x402375DC | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR119 | 0x402375E0 | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR120 | 0x402375E4 | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR121 | 0x402375E8 | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR122 | 0x402375EC | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR123 | 0x402375F0 | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR124 | 0x402375F4 | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR125 | 0x402375F8 | FULL | Master control read mirror |
| PROT_MPU13_MS_CTL_READ_MIR126 | 0x402375FC | FULL | Master control read mirror |

## 25.7 MPU 14

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PROT_MPU14_MS_CTL | 0x40237800 | FULL | Master control<br>Note:PC_SAVED is not available for this register |
| PROT_MPU14_MS_CTL_READ_MIR0 | 0x40237804 | FULL | Master control read mirror<br>Note:PC_SAVED is not available for this register |
| PROT_MPU14_MS_CTL_READ_MIR1 | 0x40237808 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR2 | 0x4023780C | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR3 | 0x40237810 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR4 | 0x40237814 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR5 | 0x40237818 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR6 | 0x4023781C | FULL | Master control read mirror |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PROT_MPU14_MS_CTL_READ_MIR7 | 0x40237820 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR8 | 0x40237824 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR9 | 0x40237828 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR10 | 0x4023782C | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR11 | 0x40237830 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR12 | 0x40237834 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR13 | 0x40237838 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR14 | 0x4023783C | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR15 | 0x40237840 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR16 | 0x40237844 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR17 | 0x40237848 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR18 | 0x4023784C | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR19 | 0x40237850 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR20 | 0x40237854 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR21 | 0x40237858 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR22 | 0x4023785C | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR23 | 0x40237860 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR24 | 0x40237864 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR25 | 0x40237868 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR26 | 0x4023786C | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR27 | 0x40237870 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR28 | 0x40237874 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR29 | 0x40237878 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR30 | 0x4023787C | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR31 | 0x40237880 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR32 | 0x40237884 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR33 | 0x40237888 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR34 | 0x4023788C | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR35 | 0x40237890 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR36 | 0x40237894 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR37 | 0x40237898 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR38 | 0x4023789C | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR39 | 0x402378A0 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR40 | 0x402378A4 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR41 | 0x402378A8 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR42 | 0x402378AC | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR43 | 0x402378B0 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR44 | 0x402378B4 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR45 | 0x402378B8 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR46 | 0x402378BC | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR47 | 0x402378C0 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR48 | 0x402378C4 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR49 | 0x402378C8 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR50 | 0x402378CC | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR51 | 0x402378D0 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR52 | 0x402378D4 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR53 | 0x402378D8 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR54 | 0x402378DC | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR55 | 0x402378E0 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR56 | 0x402378E4 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR57 | 0x402378E8 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR58 | 0x402378EC | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR59 | 0x402378F0 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR60 | 0x402378F4 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR61 | 0x402378F8 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR62 | 0x402378FC | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR63 | 0x40237900 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR64 | 0x40237904 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR65 | 0x40237908 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR66 | 0x4023790C | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR67 | 0x40237910 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR68 | 0x40237914 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR69 | 0x40237918 | FULL | Master control read mirror |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PROT_MPU14_MS_CTL_READ_MIR70 | 0x4023791C | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR71 | 0x40237920 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR72 | 0x40237924 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR73 | 0x40237928 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR74 | 0x4023792C | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR75 | 0x40237930 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR76 | 0x40237934 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR77 | 0x40237938 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR78 | 0x4023793C | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR79 | 0x40237940 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR80 | 0x40237944 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR81 | 0x40237948 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR82 | 0x4023794C | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR83 | 0x40237950 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR84 | 0x40237954 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR85 | 0x40237958 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR86 | 0x4023795C | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR87 | 0x40237960 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR88 | 0x40237964 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR89 | 0x40237968 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR90 | 0x4023796C | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR91 | 0x40237970 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR92 | 0x40237974 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR93 | 0x40237978 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR94 | 0x4023797C | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR95 | 0x40237980 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR96 | 0x40237984 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR97 | 0x40237988 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR98 | 0x4023798C | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR99 | 0x40237990 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR100 | 0x40237994 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR101 | 0x40237998 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR102 | 0x4023799C | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR103 | 0x402379A0 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR104 | 0x402379A4 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR105 | 0x402379A8 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR106 | 0x402379AC | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR107 | 0x402379B0 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR108 | 0x402379B4 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR109 | 0x402379B8 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR110 | 0x402379BC | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR111 | 0x402379C0 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR112 | 0x402379C4 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR113 | 0x402379C8 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR114 | 0x402379CC | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR115 | 0x402379D0 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR116 | 0x402379D4 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR117 | 0x402379D8 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR118 | 0x402379DC | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR119 | 0x402379E0 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR120 | 0x402379E4 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR121 | 0x402379E8 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR122 | 0x402379EC | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR123 | 0x402379F0 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR124 | 0x402379F4 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR125 | 0x402379F8 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR126 | 0x402379FC | FULL | Master control read mirror |

## 25.8 MPU 15

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PROT_MPU15_MS_CTL | 0x40237C00 | FULL | Master control<br>Note:PC_SAVED is not available for this register |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PROT_MPU15_MS_CTL_READ_MIR0 | 0x40237C04 | FULL | Master control read mirror<br>Note:PC_SAVED is not available for this register |
| PROT_MPU15_MS_CTL_READ_MIR1 | 0x40237C08 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR2 | 0x40237C0C | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR3 | 0x40237C10 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR4 | 0x40237C14 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR5 | 0x40237C18 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR6 | 0x40237C1C | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR7 | 0x40237C20 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR8 | 0x40237C24 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR9 | 0x40237C28 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR10 | 0x40237C2C | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR11 | 0x40237C30 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR12 | 0x40237C34 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR13 | 0x40237C38 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR14 | 0x40237C3C | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR15 | 0x40237C40 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR16 | 0x40237C44 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR17 | 0x40237C48 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR18 | 0x40237C4C | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR19 | 0x40237C50 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR20 | 0x40237C54 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR21 | 0x40237C58 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR22 | 0x40237C5C | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR23 | 0x40237C60 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR24 | 0x40237C64 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR25 | 0x40237C68 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR26 | 0x40237C6C | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR27 | 0x40237C70 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR28 | 0x40237C74 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR29 | 0x40237C78 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR30 | 0x40237C7C | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR31 | 0x40237C80 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR32 | 0x40237C84 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR33 | 0x40237C88 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR34 | 0x40237C8C | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR35 | 0x40237C90 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR36 | 0x40237C94 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR37 | 0x40237C98 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR38 | 0x40237C9C | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR39 | 0x40237CA0 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR40 | 0x40237CA4 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR41 | 0x40237CA8 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR42 | 0x40237CAC | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR43 | 0x40237CB0 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR44 | 0x40237CB4 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR45 | 0x40237CB8 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR46 | 0x40237CBC | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR47 | 0x40237CC0 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR48 | 0x40237CC4 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR49 | 0x40237CC8 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR50 | 0x40237CCC | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR51 | 0x40237CD0 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR52 | 0x40237CD4 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR53 | 0x40237CD8 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR54 | 0x40237CDC | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR55 | 0x40237CE0 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR56 | 0x40237CE4 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR57 | 0x40237CE8 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR58 | 0x40237CEC | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR59 | 0x40237CF0 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR60 | 0x40237CF4 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR61 | 0x40237CF8 | FULL | Master control read mirror |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PROT_MPU15_MS_CTL_READ_MIR62 | 0x40237CFC | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR63 | 0x40237D00 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR64 | 0x40237D04 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR65 | 0x40237D08 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR66 | 0x40237D0C | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR67 | 0x40237D10 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR68 | 0x40237D14 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR69 | 0x40237D18 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR70 | 0x40237D1C | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR71 | 0x40237D20 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR72 | 0x40237D24 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR73 | 0x40237D28 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR74 | 0x40237D2C | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR75 | 0x40237D30 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR76 | 0x40237D34 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR77 | 0x40237D38 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR78 | 0x40237D3C | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR79 | 0x40237D40 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR80 | 0x40237D44 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR81 | 0x40237D48 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR82 | 0x40237D4C | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR83 | 0x40237D50 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR84 | 0x40237D54 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR85 | 0x40237D58 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR86 | 0x40237D5C | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR87 | 0x40237D60 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR88 | 0x40237D64 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR89 | 0x40237D68 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR90 | 0x40237D6C | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR91 | 0x40237D70 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR92 | 0x40237D74 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR93 | 0x40237D78 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR94 | 0x40237D7C | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR95 | 0x40237D80 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR96 | 0x40237D84 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR97 | 0x40237D88 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR98 | 0x40237D8C | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR99 | 0x40237D90 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR100 | 0x40237D94 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR101 | 0x40237D98 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR102 | 0x40237D9C | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR103 | 0x40237DA0 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR104 | 0x40237DA4 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR105 | 0x40237DA8 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR106 | 0x40237DAC | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR107 | 0x40237DB0 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR108 | 0x40237DB4 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR109 | 0x40237DB8 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR110 | 0x40237DBC | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR111 | 0x40237DC0 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR112 | 0x40237DC4 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR113 | 0x40237DC8 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR114 | 0x40237DCC | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR115 | 0x40237DD0 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR116 | 0x40237DD4 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR117 | 0x40237DD8 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR118 | 0x40237DDC | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR119 | 0x40237DE0 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR120 | 0x40237DE4 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR121 | 0x40237DE8 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR122 | 0x40237DEC | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR123 | 0x40237DF0 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR124 | 0x40237DF4 | FULL | Master control read mirror |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PROT_MPU15_MS_CTL_READ_MIR125 | 0x40237DF8 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR126 | 0x40237DFC | FULL | Master control read mirror |

### 25.8.1 MPU_STRUCT 0

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PROT_MPU15_MPU_STRUCT0_ADDR | 0x40237E00 | FULL | MPU region address |
| PROT_MPU15_MPU_STRUCT0_ATT | 0x40237E04 | FULL | MPU region attrributes |

### 25.8.2 MPU_STRUCT 1

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PROT_MPU15_MPU_STRUCT1_ADDR | 0x40237E20 | FULL | MPU region address |
| PROT_MPU15_MPU_STRUCT1_ATT | 0x40237E24 | FULL | MPU region attrributes |

### 25.8.3 MPU_STRUCT 2

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PROT_MPU15_MPU_STRUCT2_ADDR | 0x40237E40 | FULL | MPU region address |
| PROT_MPU15_MPU_STRUCT2_ATT | 0x40237E44 | FULL | MPU region attrributes |

### 25.8.4 MPU_STRUCT 3

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PROT_MPU15_MPU_STRUCT3_ADDR | 0x40237E60 | FULL | MPU region address |
| PROT_MPU15_MPU_STRUCT3_ATT | 0x40237E64 | FULL | MPU region attrributes |

### 25.8.5 MPU_STRUCT 4

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PROT_MPU15_MPU_STRUCT4_ADDR | 0x40237E80 | FULL | MPU region address |
| PROT_MPU15_MPU_STRUCT4_ATT | 0x40237E84 | FULL | MPU region attrributes |

### 25.8.6 MPU_STRUCT 5

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PROT_MPU15_MPU_STRUCT5_ADDR | 0x40237EA0 | FULL | MPU region address |
| PROT_MPU15_MPU_STRUCT5_ATT | 0x40237EA4 | FULL | MPU region attrributes |

### 25.8.7 MPU_STRUCT 6

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PROT_MPU15_MPU_STRUCT6_ADDR | 0x40237EC0 | FULL | MPU region address |
| PROT_MPU15_MPU_STRUCT6_ATT | 0x40237EC4 | FULL | MPU region attrributes |

### 25.8.8 MPU_STRUCT 7

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PROT_MPU15_MPU_STRUCT7_ADDR | 0x40237EE0 | FULL | MPU region address |
| PROT_MPU15_MPU_STRUCT7_ATT | 0x40237EE4 | FULL | MPU region attrributes |

## 25.9 Register Details

### 25.9.1 SMPU

#### 25.9.1.1 PROT_SMPU_MS0_CTL

**Description:** Master 0 protection context control
**Address:** 0x40230000
**Offset:** 0x0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Each master has an associated SMPU MS_CTL register. This register provides master specific information. In a system with a secure entity, this register is typically only accessible by the secure entity, to prevent a master from changing its own privileged setting, security setting, arbitration priority or enabled protection contexts.
Master 0 (CM0+ processor) uses SMPU MS0_CTL.
Master 1 (cryptography IP) uses SMPU MS1_CTL.
Master 2 (DataWire 0) uses SMPU MS2_CTL.
Master 3 (DataWire 1) uses SMPU MS3_CTL.
....
Master 14 (CM4 processor) uses SMPU MS14_CTL.
Master 15 (test controller) uses SMPU MS15_CTL.
**Default:** 0x303

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:2] | | | | | | NS [1:1] | P [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:10] | | | | | | PRIO [9:8] | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | PC_MASK_15_TO_1 [23:17] | | | | | | | PC_MASK_0 [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | P | RW | R | 1 | Privileged setting ('0': user mode; '1': privileged mode).<br><br>Notes:<br>This field is ONLY used for masters that do NOT provide their own user/privileged access control attribute.<br>The default/reset field value provides privileged mode access capabilities. |
| 1 | NS | RW | R | 1 | Security setting ('0': secure mode; '1': non-secure mode).<br><br>Notes:<br>This field is ONLY used for masters that do NOT provide their own secure/non-secure access control attribute.<br>Note that the default/reset field value provides non-secure mode access capabilities to all masters. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 8:9 | PRIO | RW | R | 3 | Device wide bus arbitration priority setting ('0': highest priority, '3': lowest priority).<br><br>Notes:<br>The AHB-Lite interconnect performs arbitration on the individual beats/transfers of a burst (this optimizes latency over locality/bandwidth).<br>The AXI-Lite interconnects performs a single arbitration for the complete burst (this optimizes locality/bandwidth over latency).<br>Masters with the same priority setting form a 'priority group'. Within a 'priority group', round robin arbitration is performed. |
| 16 | PC_MASK_0 | R | R | 0 | Protection context mask for protection context '0'. This field is a constant '0':<br>- PC_MASK_0 is '0': MPU MS_CTL.PC[3:0] can NOT be set to '0' and PC[3:0] is not changed. If the protection context of the write transfer is '0', protection is not applied and PC[3:0] can be changed. |
| 17:23 | PC_MASK_15_TO_1 | RW | R | 0 | Protection context mask for protection contexts '15' down to '1'. Bit PC_MASK_15_TO_1[i] indicates if the MPU MS_CTL.PC[3:0] protection context field can be set to the value 'i+1':<br>- PC_MASK_15_TO_1[i] is '0': MPU MS_CTL.PC[3:0] can NOT be set to 'i+1'; and PC[3:0] is not changed. If the protection context of the write transfer is '0', protection is not applied and PC[3:0] can be changed.<br>- PC_MASK_15_TO_1[i] is '1': MPU MS_CTL.PC[3:0] can be set to 'i+1'.<br><br>Note: When CPUSS_CM0_PC_CTL.VALID[i] is '1' (the associated protection context handler is valid), write transfers to PC_MASK_15_TO_1[i-1] always write '0', regardless of data written. This ensures that when valid protection context handlers are used to enter protection contexts 1, 2 or 3 through (HW modifies MPU MS_CTL.PC[3:0] on entry of the handler), it is NOT possible for SW to enter those protection contexts (SW modifies MPU MS_CTL.PC[3:0]). |

### 25.9.1.2 PROT_SMPU_MS1_CTL

**Description:** Master 1 protection context control
**Address:** 0x40230004
**Offset:** 0x4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x303

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:10] | | | | | | PRIO [9:8] | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:17] | | | | | | | PC_MASK_0 [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 8:9 | PRIO | RW | R | 3 | See MS0_CTL.PRIO |
| 16 | PC_MASK_0 | R | R | 0 | See MS0_CTL.PC_MASK_0. |

### 25.9.1.3 PROT_SMPU_MS2_CTL

**Description:** Master 2 protection context control
**Address:** 0x40230008
**Offset:** 0x8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x303

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:10] | | | | | | PRIO [9:8] | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:17] | | | | | | | PC_MASK_0 [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 8:9 | PRIO | RW | R | 3 | See MS0_CTL.PRIO |
| 16 | PC_MASK_0 | R | R | 0 | See MS0_CTL.PC_MASK_0. |

### 25.9.1.4 PROT_SMPU_MS3_CTL

**Description:** Master 3 protection context control
**Address:** 0x4023000C
**Offset:** 0xC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x303

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:10] | | | | | | PRIO [9:8] | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:17] | | | | | | | PC_MASK_0 [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 8:9 | PRIO | RW | R | 3 | See MS0_CTL.PRIO |
| 16 | PC_MASK_0 | R | R | 0 | See MS0_CTL.PC_MASK_0. |

### 25.9.1.5 PROT_SMPU_MS4_CTL

**Description:** Master 4 protection context control
**Address:** 0x40230010
**Offset:** 0x10
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x303

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:10] | | | | | | PRIO [9:8] | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:17] | | | | | | | PC_MASK_0 [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 8:9 | PRIO | RW | R | 3 | See MS0_CTL.PRIO |
| 16 | PC_MASK_0 | R | R | 0 | See MS0_CTL.PC_MASK_0. |

### 25.9.1.6 PROT_SMPU_MS5_CTL

**Description:** Master 5 protection context control
**Address:** 0x40230014
**Offset:** 0x14
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x303

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:2] | | | | | | NS [1:1] | P [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:10] | | | | | | PRIO [9:8] | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | PC_MASK_15_TO_1 [23:17] | | | | | | | PC_MASK_0 [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | P | RW | R | 1 | See MS0_CTL.P. |
| 1 | NS | RW | R | 1 | See MS0_CTL.NS. |
| 8:9 | PRIO | RW | R | 3 | See MS0_CTL.PRIO |
| 16 | PC_MASK_0 | R | R | 0 | See MS0_CTL.PC_MASK_0. |
| 17:23 | PC_MASK_15_TO_1 | RW | R | 0 | See MS0_CTL.PC_MASK_15_TO_1. |

### 25.9.1.7 PROT_SMPU_MS9_CTL

**Description:** Master 9 protection context control
**Address:** 0x40230024
**Offset:** 0x24
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x303

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:2] | | | | | | NS [1:1] | P [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:10] | | | | | | PRIO [9:8] | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | PC_MASK_15_TO_1 [23:17] | | | | | | | PC_MASK_0 [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | P | RW | R | 1 | See MS0_CTL.P. |
| 1 | NS | RW | R | 1 | See MS0_CTL.NS. |
| 8:9 | PRIO | RW | R | 3 | See MS0_CTL.PRIO |
| 16 | PC_MASK_0 | R | R | 0 | See MS0_CTL.PC_MASK_0. |
| 17:23 | PC_MASK_15_TO_1 | RW | R | 0 | See MS0_CTL.PC_MASK_15_TO_1. |

### 25.9.1.8 PROT_SMPU_MS10_CTL

**Description:** Master 10 protection context control
**Address:** 0x40230028
**Offset:** 0x28
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x303

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:2] | | | | | | NS [1:1] | P [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:10] | | | | | | PRIO [9:8] | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | PC_MASK_15_TO_1 [23:17] | | | | | | | PC_MASK_0 [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | P | RW | R | 1 | See MS0_CTL.P. |
| 1 | NS | RW | R | 1 | See MS0_CTL.NS. |
| 8:9 | PRIO | RW | R | 3 | See MS0_CTL.PRIO |
| 16 | PC_MASK_0 | R | R | 0 | See MS0_CTL.PC_MASK_0. |
| 17:23 | PC_MASK_15_TO_1 | RW | R | 0 | See MS0_CTL.PC_MASK_15_TO_1. |

### 25.9.1.9 PROT_SMPU_MS13_CTL

**Description:** Master 13 protection context control
**Address:** 0x40230034
**Offset:** 0x34
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x303

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:2] | | | | | | NS [1:1] | P [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:10] | | | | | | PRIO [9:8] | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | PC_MASK_15_TO_1 [23:17] | | | | | | | PC_MASK_0 [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | P | RW | R | 1 | See MS0_CTL.P. |
| 1 | NS | RW | R | 1 | See MS0_CTL.NS. |
| 8:9 | PRIO | RW | R | 3 | See MS0_CTL.PRIO |
| 16 | PC_MASK_0 | R | R | 0 | See MS0_CTL.PC_MASK_0. |
| 17:23 | PC_MASK_15_TO_1 | RW | R | 0 | See MS0_CTL.PC_MASK_15_TO_1. |

### 25.9.1.10 PROT_SMPU_MS14_CTL

**Description:** Master 14 protection context control
**Address:** 0x40230038
**Offset:** 0x38
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x303

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:2] | | | | | | NS [1:1] | P [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:10] | | | | | | PRIO [9:8] | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | PC_MASK_15_TO_1 [23:17] | | | | | | | PC_MASK_0 [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | P | RW | R | 1 | See MS0_CTL.P. |
| 1 | NS | RW | R | 1 | See MS0_CTL.NS. |
| 8:9 | PRIO | RW | R | 3 | See MS0_CTL.PRIO |
| 16 | PC_MASK_0 | R | R | 0 | See MS0_CTL.PC_MASK_0. |
| 17:23 | PC_MASK_15_TO_1 | RW | R | 0 | See MS0_CTL.PC_MASK_15_TO_1. |

### 25.9.1.11 PROT_SMPU_MS15_CTL

**Description:** Master 15 protection context control
**Address:** 0x4023003C
**Offset:** 0x3C
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x303

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:2] | | | | | | NS [1:1] | P [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:10] | | | | | | PRIO [9:8] | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | PC_MASK_15_TO_1 [23:17] | | | | | | | PC_MASK_0 [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | P | RW | R | 1 | See MS0_CTL.P. |
| 1 | NS | RW | R | 1 | See MS0_CTL.NS. |
| 8:9 | PRIO | RW | R | 3 | See MS0_CTL.PRIO |
| 16 | PC_MASK_0 | R | R | 0 | See MS0_CTL.PC_MASK_0. |
| 17:23 | PC_MASK_15_TO_1 | RW | R | 0 | See MS0_CTL.PC_MASK_15_TO_1. |

### 25.9.1.12 SMPU_STRUCT

#### 25.9.1.12.1 PROT_SMPU_SMPU_STRUCT_ADDR0

**Description:** SMPU region address 0 (slave structure)
**Address:** 0x40232000
**Offset:** 0x0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register defines a SMPU address region.
**Default:** Undefined as one or more bit fields have a default value that is undefined

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | SUBREGION_DISABLE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDR24 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDR24 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDR24 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | SUBREGION_DISABLE | RW | R | Undefined | This field is used to individually disabled the eight equally sized subregions in which a region is partitioned. Subregion disable:<br>Bit 0: subregion 0 disable.<br>Bit 1: subregion 1 disable.<br>Bit 2: subregion 2 disable.<br>Bit 3: subregion 3 disable.<br>Bit 4: subregion 4 disable.<br>Bit 5: subregion 5 disable.<br>Bit 6: subregion 6 disable.<br>Bit 7: subregion 7 disable.<br>E.g., a 64 KByte address region (ATT0.REGION_SIZE is '15') has eight 8 KByte subregions. The access control as defined by ATT0 applies if the bus transfer address is within the address region AND the addressed subregion is NOT disabled. Note that the smallest region size is 256 B and the smallest subregion size is 32 B. |
| 8:31 | ADDR24 | RW | R | Undefined | This field specifies the most significant bits of the 32-bit address of an address region. The region size is defined by ATT0.REGION_SIZE. A region of n Byte is always n Byte aligned. As a result, some of the lesser significant address bits of ADDR24 may be ignored in determining whether a bus transfer address is within an address region. E.g., a 64 KByte address region (REGION_SIZE is '15') is 64 KByte aligned, and ADDR24[7:0] are ignored. |

### 25.9.1.12.2 PROT_SMPU_SMPU_STRUCT_ATT0

**Description:** SMPU region attributes 0 (slave structure)
**Address:** 0x40232004
**Offset:** 0x4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register defines SMPU access control.
**Default:** Undefined as one or more bit fields have a default value that is undefined

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:7] | NS [6:6] | PX [5:5] | PW [4:4] | PR [3:3] | UX [2:2] | UW [1:1] | UR [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | PC_MASK_15_TO_1 [15:9] | | | | | | | PC_MASK_0 [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | ENABLED [31:31] | PC_MATCH [30:30] | None [29:29] | REGION_SIZE [28:24] | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | UR | RW | R | Undefined | User read enable:<br>'0': Disabled (user, read accesses are NOT allowed).<br>'1': Enabled (user, read accesses are allowed). |
| 1 | UW | RW | R | Undefined | User write enable:<br>'0': Disabled (user, write accesses are NOT allowed).<br>'1': Enabled (user, write accesses are allowed). |
| 2 | UX | RW | R | Undefined | User execute enable:<br>'0': Disabled (user, execute accesses are NOT allowed).<br>'1': Enabled (user, execute accesses are allowed). |
| 3 | PR | RW | R | Undefined | Privileged read enable:<br>'0': Disabled (privileged, read accesses are NOT allowed).<br>'1': Enabled (privileged, read accesses are allowed). |
| 4 | PW | RW | R | Undefined | Privileged write enable:<br>'0': Disabled (privileged, write accesses are NOT allowed).<br>'1': Enabled (privileged, write accesses are allowed). |
| 5 | PX | RW | R | Undefined | Privileged execute enable:<br>'0': Disabled (privileged, execute accesses are NOT allowed).<br>'1': Enabled (privileged, execute accesses are allowed). |
| 6 | NS | RW | R | Undefined | Non-secure:<br>'0': Secure (secure accesses allowed, non-secure access NOT allowed).<br>'1': Non-secure (both secure and non-secure accesses allowed). |
| 8 | PC_MASK_0 | R | R | 1 | This field specifies protection context identifier based access control for protection context '0'. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 9:15 | PC_MASK_15_TO_1 | RW | R | Undefined | This field specifies protection context identifier based access control.<br>Bit i: protection context i+1 enable. If '0', protection context i+1 access is disabled; i.e. not allowed. If '1', protection context i+1 access is enabled; i.e. allowed. |
| 24:28 | REGION_SIZE | RW | R | Undefined | This field specifies the region size:<br>'0'-'6': Undefined.<br>'7': 256 B region<br>'8': 512 B region<br>'9': 1 KB region<br>'10': 2 KB region<br>'11': 4 KB region<br>'12': 8 KB region<br>'13': 16 KB region<br>'14': 32 KB region<br>'15': 64 KB region<br>'16': 128 KB region<br>'17': 256 KB region<br>'18': 512 KB region<br>'19': 1 MB region<br>'20': 2 MB region<br>'21': 4 MB region<br>'22': 8 MB region<br>'23': 16 MB region<br>'24': 32 MB region<br>'25': 64 MB region<br>'26': 128 MB region<br>'27': 256 MB region<br>'28': 512 MB region<br>'39': 1 GB region<br>'30': 2 GB region<br>'31': 4 GB region |
| 30 | PC_MATCH | RW | R | Undefined | This field specifies if the PC field participates in the 'matching' process or the 'access evaluation' process:<br>'0': PC field participates in 'access evaluation'.<br>'1': PC field participates in 'matching'.<br><br>'Matching' process. For each protection structure, the process identifies if a transfer address is contained within the address range. This identifies the 'matching' regions.<br>'Access evaluation' process. For each protection structure, the process evaluates the bus transfer access attributes against the access control attributes.<br><br>Note that it is possible to define different access control for multiple protection contexts by using multiple protection structures with the same address region and PC_MATCH set to '1'. |
| 31 | ENABLED | RW | R | 0 | Region enable:<br>'0': Disabled. A disabled region will never result in a match on the bus transfer address.<br>'1': Enabled.<br><br>Note: a disabled address region performs logic gating to reduce dynamic power consumption. |

### 25.9.1.12.3 PROT_SMPU_SMPU_STRUCT_ADDR1

**Description:** SMPU region address 1 (master structure)
**Address:** 0x40232020
**Offset:** 0x20
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register defines a SMPU address region. The address region is fixed, the region size is 64 B (two 32 B subregions within a 256 B region) and includes the ADDR0, ATT0, ADDR1 and ATT0 registers.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | SUBREGION_DISABLE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDR24 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDR24 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDR24 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | SUBREGION_DISABLE | R | R | 252 | This field is used to individually disabled the eight equally sized subregions in which a region is partitioned. Subregion disable:<br>Bit 0: subregion 0 disable.<br>Bit 1: subregion 1 disable.<br>Bit 2: subregion 2 disable.<br>Bit 3: subregion 3 disable.<br>Bit 4: subregion 4 disable.<br>Bit 5: subregion 5 disable.<br>Bit 6: subregion 6 disable.<br>Bit 7: subregion 7 disable.<br><br>Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1.<br><br>Note: this field is read-only. |
| 8:31 | ADDR24 | R | R | 4203296 | This field specifies the most significant bits of the 32-bit address of an address region.<br><br>'ADDR_DEF1': base address of structure.<br><br>Note: this field is read-only. |

### 25.9.1.12.4 PROT_SMPU_SMPU_STRUCT_ATT1

**Description:** SMPU region attributes 1 (master structure)
**Address:** 0x40232024
**Offset:** 0x24
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register defines SMPU access control.
**Default:** Undefined as one or more bit fields have a default value that is undefined

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:7] | NS [6:6] | PX [5:5] | PW [4:4] | PR [3:3] | UX [2:2] | UW [1:1] | UR [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | PC_MASK_15_TO_1 [15:9] | | | | | | | PC_MASK_0 [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | ENABLED [31:31] | PC_MATCH [30:30] | None [29:29] | REGION_SIZE [28:24] | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | UR | R | R | 1 | User read enable:<br>'0': Disabled (user, read accesses are NOT allowed).<br>'1': Enabled (user, read accesses are allowed).<br><br>Note that this register is constant '1'; i.e. user read accesses are ALWAYS allowed. |
| 1 | UW | RW | R | Undefined | User write enable:<br>'0': Disabled (user, write accesses are NOT allowed).<br>'1': Enabled (user, write accesses are allowed). |
| 2 | UX | R | R | 0 | User execute enable:<br>'0': Disabled (user, execute accesses are NOT allowed).<br>'1': Enabled (user, execute accesses are allowed).<br><br>Note that this register is constant '0'; i.e. user execute accesses are NEVER allowed. |
| 3 | PR | R | R | 1 | Privileged read enable:<br>'0': Disabled (privileged, read accesses are NOT allowed).<br>'1': Enabled (privileged, read accesses are allowed).<br><br>Note that this register is constant '1'; i.e. privileged read accesses are ALWAYS allowed. |
| 4 | PW | RW | R | Undefined | Privileged write enable:<br>'0': Disabled (privileged, write accesses are NOT allowed).<br>'1': Enabled (privileged, write accesses are allowed). |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 5 | PX | R | R | 0 | Privileged execute enable:<br>'0': Disabled (privileged, execute accesses are NOT allowed).<br>'1': Enabled (privileged, execute accesses are allowed).<br><br>Note that this register is constant '0'; i.e. privileged execute accesses are NEVER allowed. |
| 6 | NS | RW | R | Undefined | Non-secure:<br>'0': Secure (secure accesses allowed, non-secure access NOT allowed).<br>'1': Non-secure (both secure and non-secure accesses allowed). |
| 8 | PC_MASK_0 | R | R | 1 | This field specifies protection context identifier based access control for protection context '0'. |
| 9:15 | PC_MASK_15_TO_1 | RW | R | Undefined | This field specifies protection context identifier based access control.<br>Bit i: protection context i+1 enable. If '0', protection context i+1 access is disabled; i.e. not allowed. If '1', protection context i+1 access is enabled; i.e. allowed. |
| 24:28 | REGION_SIZE | R | R | 7 | This field specifies the region size:<br>'7': 256 B region (8 32 B subregions)<br><br>Note: this field is read-only. |
| 30 | PC_MATCH | RW | R | Undefined | This field specifies if the PC field participates in the 'matching' process or the 'access evaluation' process:<br>'0': PC field participates in 'access evaluation'.<br>'1': PC field participates in 'matching'.<br><br>'Matching' process. For each protection structure, the process identifies if a transfer address is contained within the address range. This identifies the 'matching' regions.<br>'Access evaluation' process. For each protection structure, the process evaluates the bus transfer access attributes against the access control attributes.<br><br>Note that it is possible to define different access control for multiple protection contexts by using multiple protection structures with the same address region and PC_MATCH set to '1'. |
| 31 | ENABLED | RW | R | 0 | Region enable:<br>'0': Disabled. A disabled region will never result in a match on the bus transfer address.<br>'1': Enabled. |

### 25.9.2 MPU

#### 25.9.2.1 PROT_MPU_MS_CTL

**Description:** Master control
**Address:** 0x40234000
**Offset:** 0x0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:4] | | | | PC [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:20] | | | | PC_SAVED [19:16] | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | PC | RW | RW | 0 | Active protection context (PC). Modifications to this field are constrained by the associated SMPU MS_CTL.PC_MASK_0 and MS_CTL.PC_MASK_15_TO_1[] fields. In addition, a write transfer with protection context '0' can change this field (protection context 0 has unrestricted access).<br><br>The CM0+ MPU MS_CTL register is special: the PC field is modifiable by BOTH HW and SW (for all other masters, the MPU MS_CTL.PC field is modifiable by SW ONLY. For CM0+ PC field HW modifications, the following holds:<br>* On entry of a CM0_PC0/1/2/3_HANDLER exception/interrupt handler:<br>IF (the new PC is the same as MS_CTL.PC)<br>PC is not affected; PC_SAVED is not affected.<br>ELSE IF (CM0_PC_CTL.VALID[MS_CTL.PC])<br>An AHB-Lite bus error is generated for the exception handler fetch;<br>PC is not affected; PC_SAVED is not affected.<br>ELSE<br>PC = 'new PC'; PC_SAVED = PC (push operation).<br>* On entry of any other exception/interrupt handler:<br>PC = PC_SAVED; PC_SAVED is not affected (pop operation).<br><br>Note that the CM0_PC0/1/2/3_HANDLER and CM0_PC_CTL registers are part of repecitve CPUSS MMIO registers.<br><br>Note: this field is NOT used by the DW controllers, DMA controller, AXI DMA controller, CRYPTO component and VIDEOSS. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 16:19 | PC_SAVED | RW | RW | 0 | Saved protection context. Modifications to this field are constrained by the associated SMPU MS_CTL.PC_MASK_0 and MS_CTL.PC_MASK_15_TO_1[] fields.<br><br>Note: this field is ONLY used by the CM0+. |

### 25.9.2.2 PROT_MPU_MS_CTL_READ_MIR

**Description:** Master control read mirror
**Address:** 0x40234004
**Offset:** 0x4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:4] | | | | PC [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:20] | | | | PC_SAVED [19:16] | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | PC | R | W | 0 | Read-only mirror of MS_CTL.PC |
| 16:19 | PC_SAVED | R | W | 0 | Read-only mirror of MS_CTL.PC_SAVED |

### 25.9.2.3 MPU_STRUCT

#### 25.9.2.3.1 PROT_MPU_MPU_STRUCT_ADDR

**Description:** MPU region address
**Address:** 0x40234200
**Offset:** 0x0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register defines a MPU address region.
**Default:** Undefined as one or more bit fields have a default value that is undefined

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | SUBREGION_DISABLE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDR24 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDR24 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDR24 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | SUBREGION_DISABLE | RW | R | Undefined | This field is used to individually disabled the eight equally sized subregions in which a region is partitioned. Subregion disable:<br>Bit 0: subregion 0 disable.<br>Bit 1: subregion 1 disable.<br>Bit 2: subregion 2 disable.<br>Bit 3: subregion 3 disable.<br>Bit 4: subregion 4 disable.<br>Bit 5: subregion 5 disable.<br>Bit 6: subregion 6 disable.<br>Bit 7: subregion 7 disable.<br>E.g., a 64 KByte address region (REGION_SIZE is '15') has eight 8 KByte subregions. The access control as defined by MPU_REGION_ATT applies if the bus transfer address is within the address region AND the addressed subregion is NOT disabled. Note that the smallest region size is 256 B and the smallest subregion size is 32 B. |
| 8:31 | ADDR24 | RW | R | Undefined | This field specifies the most significant bits of the 32-bit address of an address region. The region size is defined by ATT.REGION_SIZE. A region of n Byte is always n Byte aligned. As a result, some of the lesser significant address bits of ADDR24 may be ignored in determining whether a bus transfer address is within an address region. E.g., a 64 KByte address region (REGION_SIZE is '15') is 64 KByte aligned, and ADDR24[7:0] are ignored. |

### 25.9.2.3.2 PROT_MPU_MPU_STRUCT_ATT

**Description:** MPU region attrributes
**Address:** 0x40234204
**Offset:** 0x4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register defines a MPU access control register.
**Default:** Undefined as one or more bit fields have a default value that is undefined

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:7] | NS [6:6] | PX [5:5] | PW [4:4] | PR [3:3] | UX [2:2] | UW [1:1] | UR [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | ENABLED [31:31] | None [30:29] | | REGION_SIZE [28:24] | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | UR | RW | R | Undefined | User read enable:<br>'0': Disabled (user, read accesses are NOT allowed).<br>'1': Enabled (user, read accesses are allowed). |
| 1 | UW | RW | R | Undefined | User write enable:<br>'0': Disabled (user, write accesses are NOT allowed).<br>'1': Enabled (user, write accesses are allowed). |
| 2 | UX | RW | R | Undefined | User execute enable:<br>'0': Disabled (user, execute accesses are NOT allowed).<br>'1': Enabled (user, execute accesses are allowed). |
| 3 | PR | RW | R | Undefined | Privileged read enable:<br>'0': Disabled (privileged, read accesses are NOT allowed).<br>'1': Enabled (privileged, read accesses are allowed). |
| 4 | PW | RW | R | Undefined | Privileged write enable:<br>'0': Disabled (privileged, write accesses are NOT allowed).<br>'1': Enabled (privileged, write accesses are allowed). |
| 5 | PX | RW | R | Undefined | Privileged execute enable:<br>'0': Disabled (privileged, execute accesses are NOT allowed).<br>'1': Enabled (privileged, execute accesses are allowed). |
| 6 | NS | RW | R | Undefined | Non-secure:<br>'0': Secure (secure accesses allowed, non-secure access NOT allowed).<br>'1': Non-secure (both secure and non-secure accesses allowed). |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 24:28 | REGION_SIZE | RW | R | Undefined | This field specifies the region size:<br>'0'-'6': Undefined.<br>'7': 256 B region<br>'8': 512 B region<br>'9': 1 KB region<br>'10': 2 KB region<br>'11': 4 KB region<br>'12': 8 KB region<br>'13': 16 KB region<br>'14': 32 KB region<br>'15': 64 KB region<br>'16': 128 KB region<br>'17': 256 KB region<br>'18': 512 KB region<br>'19': 1 MB region<br>'20': 2 MB region<br>'21': 4 MB region<br>'22': 8 MB region<br>'23': 16 MB region<br>'24': 32 MB region<br>'25': 64 MB region<br>'26': 128 MB region<br>'27': 256 MB region<br>'28': 512 MB region<br>'39': 1 GB region<br>'30': 2 GB region<br>'31': 4 GB region |
| 31 | ENABLED | RW | R | 0 | Region enable:<br>'0': Disabled. A disabled region will never result in a match on the bus transfer address.<br>'1': Enabled.<br><br>Note: a disabled address region performs logic gating to reduce dynamic power consumption. |

# 26 SCB

## 26.1 SCB 0

**Description** Serial Communications Block (SPI/UART/I2C)
**Base Address** 0x40600000
**Size** 0x10000
**Slave Num** MMIO6 - 0

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SCB0_CTRL | 0x40600000 | FULL | Generic control |
| SCB0_STATUS | 0x40600004 | FULL | Generic status |
| SCB0_CMD_RESP_CTRL | 0x40600008 | FULL | Command/response control |
| SCB0_CMD_RESP_STATUS | 0x4060000C | FULL | Command/response status |
| SCB0_SPI_CTRL | 0x40600020 | FULL | SPI control |
| SCB0_SPI_STATUS | 0x40600024 | FULL | SPI status |
| SCB0_SPI_TX_CTRL | 0x40600028 | FULL | SPI transmitter control |
| SCB0_SPI_RX_CTRL | 0x4060002C | FULL | SPI receiver control |
| SCB0_UART_CTRL | 0x40600040 | FULL | UART control |
| SCB0_UART_TX_CTRL | 0x40600044 | FULL | UART transmitter control |
| SCB0_UART_RX_CTRL | 0x40600048 | FULL | UART receiver control |
| SCB0_UART_RX_STATUS | 0x4060004C | FULL | UART receiver status |
| SCB0_UART_FLOW_CTRL | 0x40600050 | FULL | UART flow control |
| SCB0_I2C_CTRL | 0x40600060 | FULL | I2C control |
| SCB0_I2C_STATUS | 0x40600064 | FULL | I2C status |
| SCB0_I2C_M_CMD | 0x40600068 | FULL | I2C master command |
| SCB0_I2C_S_CMD | 0x4060006C | FULL | I2C slave command |
| SCB0_I2C_CFG | 0x40600070 | FULL | I2C configuration |
| SCB0_TX_CTRL | 0x40600200 | FULL | Transmitter control |
| SCB0_TX_FIFO_CTRL | 0x40600204 | FULL | Transmitter FIFO control |
| SCB0_TX_FIFO_STATUS | 0x40600208 | FULL | Transmitter FIFO status |
| SCB0_TX_FIFO_WR | 0x40600240 | FULL | Transmitter FIFO write |
| SCB0_RX_CTRL | 0x40600300 | FULL | Receiver control |
| SCB0_RX_FIFO_CTRL | 0x40600304 | FULL | Receiver FIFO control |
| SCB0_RX_FIFO_STATUS | 0x40600308 | FULL | Receiver FIFO status |
| SCB0_RX_MATCH | 0x40600310 | FULL | Slave address and mask |
| SCB0_RX_FIFO_RD | 0x40600340 | FULL | Receiver FIFO read |
| SCB0_RX_FIFO_RD_SILENT | 0x40600344 | FULL | Receiver FIFO read silent |
| SCB0_EZ_DATA0 | 0x40600400 | FULL | Memory buffer |
| SCB0_EZ_DATA1 | 0x40600404 | FULL | Memory buffer |
| SCB0_EZ_DATA2 | 0x40600408 | FULL | Memory buffer |
| SCB0_EZ_DATA3 | 0x4060040C | FULL | Memory buffer |
| SCB0_EZ_DATA4 | 0x40600410 | FULL | Memory buffer |
| SCB0_EZ_DATA5 | 0x40600414 | FULL | Memory buffer |
| SCB0_EZ_DATA6 | 0x40600418 | FULL | Memory buffer |
| SCB0_EZ_DATA7 | 0x4060041C | FULL | Memory buffer |
| SCB0_EZ_DATA8 | 0x40600420 | FULL | Memory buffer |
| SCB0_EZ_DATA9 | 0x40600424 | FULL | Memory buffer |
| SCB0_EZ_DATA10 | 0x40600428 | FULL | Memory buffer |
| SCB0_EZ_DATA11 | 0x4060042C | FULL | Memory buffer |
| SCB0_EZ_DATA12 | 0x40600430 | FULL | Memory buffer |
| SCB0_EZ_DATA13 | 0x40600434 | FULL | Memory buffer |
| SCB0_EZ_DATA14 | 0x40600438 | FULL | Memory buffer |
| SCB0_EZ_DATA15 | 0x4060043C | FULL | Memory buffer |
| SCB0_EZ_DATA16 | 0x40600440 | FULL | Memory buffer |
| SCB0_EZ_DATA17 | 0x40600444 | FULL | Memory buffer |
| SCB0_EZ_DATA18 | 0x40600448 | FULL | Memory buffer |
| SCB0_EZ_DATA19 | 0x4060044C | FULL | Memory buffer |
| SCB0_EZ_DATA20 | 0x40600450 | FULL | Memory buffer |
| SCB0_EZ_DATA21 | 0x40600454 | FULL | Memory buffer |
| SCB0_EZ_DATA22 | 0x40600458 | FULL | Memory buffer |
| SCB0_EZ_DATA23 | 0x4060045C | FULL | Memory buffer |
| SCB0_EZ_DATA24 | 0x40600460 | FULL | Memory buffer |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SCB0_EZ_DATA25 | 0x40600464 | FULL | Memory buffer |
| SCB0_EZ_DATA26 | 0x40600468 | FULL | Memory buffer |
| SCB0_EZ_DATA27 | 0x4060046C | FULL | Memory buffer |
| SCB0_EZ_DATA28 | 0x40600470 | FULL | Memory buffer |
| SCB0_EZ_DATA29 | 0x40600474 | FULL | Memory buffer |
| SCB0_EZ_DATA30 | 0x40600478 | FULL | Memory buffer |
| SCB0_EZ_DATA31 | 0x4060047C | FULL | Memory buffer |
| SCB0_EZ_DATA32 | 0x40600480 | FULL | Memory buffer |
| SCB0_EZ_DATA33 | 0x40600484 | FULL | Memory buffer |
| SCB0_EZ_DATA34 | 0x40600488 | FULL | Memory buffer |
| SCB0_EZ_DATA35 | 0x4060048C | FULL | Memory buffer |
| SCB0_EZ_DATA36 | 0x40600490 | FULL | Memory buffer |
| SCB0_EZ_DATA37 | 0x40600494 | FULL | Memory buffer |
| SCB0_EZ_DATA38 | 0x40600498 | FULL | Memory buffer |
| SCB0_EZ_DATA39 | 0x4060049C | FULL | Memory buffer |
| SCB0_EZ_DATA40 | 0x406004A0 | FULL | Memory buffer |
| SCB0_EZ_DATA41 | 0x406004A4 | FULL | Memory buffer |
| SCB0_EZ_DATA42 | 0x406004A8 | FULL | Memory buffer |
| SCB0_EZ_DATA43 | 0x406004AC | FULL | Memory buffer |
| SCB0_EZ_DATA44 | 0x406004B0 | FULL | Memory buffer |
| SCB0_EZ_DATA45 | 0x406004B4 | FULL | Memory buffer |
| SCB0_EZ_DATA46 | 0x406004B8 | FULL | Memory buffer |
| SCB0_EZ_DATA47 | 0x406004BC | FULL | Memory buffer |
| SCB0_EZ_DATA48 | 0x406004C0 | FULL | Memory buffer |
| SCB0_EZ_DATA49 | 0x406004C4 | FULL | Memory buffer |
| SCB0_EZ_DATA50 | 0x406004C8 | FULL | Memory buffer |
| SCB0_EZ_DATA51 | 0x406004CC | FULL | Memory buffer |
| SCB0_EZ_DATA52 | 0x406004D0 | FULL | Memory buffer |
| SCB0_EZ_DATA53 | 0x406004D4 | FULL | Memory buffer |
| SCB0_EZ_DATA54 | 0x406004D8 | FULL | Memory buffer |
| SCB0_EZ_DATA55 | 0x406004DC | FULL | Memory buffer |
| SCB0_EZ_DATA56 | 0x406004E0 | FULL | Memory buffer |
| SCB0_EZ_DATA57 | 0x406004E4 | FULL | Memory buffer |
| SCB0_EZ_DATA58 | 0x406004E8 | FULL | Memory buffer |
| SCB0_EZ_DATA59 | 0x406004EC | FULL | Memory buffer |
| SCB0_EZ_DATA60 | 0x406004F0 | FULL | Memory buffer |
| SCB0_EZ_DATA61 | 0x406004F4 | FULL | Memory buffer |
| SCB0_EZ_DATA62 | 0x406004F8 | FULL | Memory buffer |
| SCB0_EZ_DATA63 | 0x406004FC | FULL | Memory buffer |
| SCB0_EZ_DATA64 | 0x40600500 | FULL | Memory buffer |
| SCB0_EZ_DATA65 | 0x40600504 | FULL | Memory buffer |
| SCB0_EZ_DATA66 | 0x40600508 | FULL | Memory buffer |
| SCB0_EZ_DATA67 | 0x4060050C | FULL | Memory buffer |
| SCB0_EZ_DATA68 | 0x40600510 | FULL | Memory buffer |
| SCB0_EZ_DATA69 | 0x40600514 | FULL | Memory buffer |
| SCB0_EZ_DATA70 | 0x40600518 | FULL | Memory buffer |
| SCB0_EZ_DATA71 | 0x4060051C | FULL | Memory buffer |
| SCB0_EZ_DATA72 | 0x40600520 | FULL | Memory buffer |
| SCB0_EZ_DATA73 | 0x40600524 | FULL | Memory buffer |
| SCB0_EZ_DATA74 | 0x40600528 | FULL | Memory buffer |
| SCB0_EZ_DATA75 | 0x4060052C | FULL | Memory buffer |
| SCB0_EZ_DATA76 | 0x40600530 | FULL | Memory buffer |
| SCB0_EZ_DATA77 | 0x40600534 | FULL | Memory buffer |
| SCB0_EZ_DATA78 | 0x40600538 | FULL | Memory buffer |
| SCB0_EZ_DATA79 | 0x4060053C | FULL | Memory buffer |
| SCB0_EZ_DATA80 | 0x40600540 | FULL | Memory buffer |
| SCB0_EZ_DATA81 | 0x40600544 | FULL | Memory buffer |
| SCB0_EZ_DATA82 | 0x40600548 | FULL | Memory buffer |
| SCB0_EZ_DATA83 | 0x4060054C | FULL | Memory buffer |
| SCB0_EZ_DATA84 | 0x40600550 | FULL | Memory buffer |
| SCB0_EZ_DATA85 | 0x40600554 | FULL | Memory buffer |
| SCB0_EZ_DATA86 | 0x40600558 | FULL | Memory buffer |
| SCB0_EZ_DATA87 | 0x4060055C | FULL | Memory buffer |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SCB0_EZ_DATA88 | 0x40600560 | FULL | Memory buffer |
| SCB0_EZ_DATA89 | 0x40600564 | FULL | Memory buffer |
| SCB0_EZ_DATA90 | 0x40600568 | FULL | Memory buffer |
| SCB0_EZ_DATA91 | 0x4060056C | FULL | Memory buffer |
| SCB0_EZ_DATA92 | 0x40600570 | FULL | Memory buffer |
| SCB0_EZ_DATA93 | 0x40600574 | FULL | Memory buffer |
| SCB0_EZ_DATA94 | 0x40600578 | FULL | Memory buffer |
| SCB0_EZ_DATA95 | 0x4060057C | FULL | Memory buffer |
| SCB0_EZ_DATA96 | 0x40600580 | FULL | Memory buffer |
| SCB0_EZ_DATA97 | 0x40600584 | FULL | Memory buffer |
| SCB0_EZ_DATA98 | 0x40600588 | FULL | Memory buffer |
| SCB0_EZ_DATA99 | 0x4060058C | FULL | Memory buffer |
| SCB0_EZ_DATA100 | 0x40600590 | FULL | Memory buffer |
| SCB0_EZ_DATA101 | 0x40600594 | FULL | Memory buffer |
| SCB0_EZ_DATA102 | 0x40600598 | FULL | Memory buffer |
| SCB0_EZ_DATA103 | 0x4060059C | FULL | Memory buffer |
| SCB0_EZ_DATA104 | 0x406005A0 | FULL | Memory buffer |
| SCB0_EZ_DATA105 | 0x406005A4 | FULL | Memory buffer |
| SCB0_EZ_DATA106 | 0x406005A8 | FULL | Memory buffer |
| SCB0_EZ_DATA107 | 0x406005AC | FULL | Memory buffer |
| SCB0_EZ_DATA108 | 0x406005B0 | FULL | Memory buffer |
| SCB0_EZ_DATA109 | 0x406005B4 | FULL | Memory buffer |
| SCB0_EZ_DATA110 | 0x406005B8 | FULL | Memory buffer |
| SCB0_EZ_DATA111 | 0x406005BC | FULL | Memory buffer |
| SCB0_EZ_DATA112 | 0x406005C0 | FULL | Memory buffer |
| SCB0_EZ_DATA113 | 0x406005C4 | FULL | Memory buffer |
| SCB0_EZ_DATA114 | 0x406005C8 | FULL | Memory buffer |
| SCB0_EZ_DATA115 | 0x406005CC | FULL | Memory buffer |
| SCB0_EZ_DATA116 | 0x406005D0 | FULL | Memory buffer |
| SCB0_EZ_DATA117 | 0x406005D4 | FULL | Memory buffer |
| SCB0_EZ_DATA118 | 0x406005D8 | FULL | Memory buffer |
| SCB0_EZ_DATA119 | 0x406005DC | FULL | Memory buffer |
| SCB0_EZ_DATA120 | 0x406005E0 | FULL | Memory buffer |
| SCB0_EZ_DATA121 | 0x406005E4 | FULL | Memory buffer |
| SCB0_EZ_DATA122 | 0x406005E8 | FULL | Memory buffer |
| SCB0_EZ_DATA123 | 0x406005EC | FULL | Memory buffer |
| SCB0_EZ_DATA124 | 0x406005F0 | FULL | Memory buffer |
| SCB0_EZ_DATA125 | 0x406005F4 | FULL | Memory buffer |
| SCB0_EZ_DATA126 | 0x406005F8 | FULL | Memory buffer |
| SCB0_EZ_DATA127 | 0x406005FC | FULL | Memory buffer |
| SCB0_EZ_DATA128 | 0x40600600 | FULL | Memory buffer |
| SCB0_EZ_DATA129 | 0x40600604 | FULL | Memory buffer |
| SCB0_EZ_DATA130 | 0x40600608 | FULL | Memory buffer |
| SCB0_EZ_DATA131 | 0x4060060C | FULL | Memory buffer |
| SCB0_EZ_DATA132 | 0x40600610 | FULL | Memory buffer |
| SCB0_EZ_DATA133 | 0x40600614 | FULL | Memory buffer |
| SCB0_EZ_DATA134 | 0x40600618 | FULL | Memory buffer |
| SCB0_EZ_DATA135 | 0x4060061C | FULL | Memory buffer |
| SCB0_EZ_DATA136 | 0x40600620 | FULL | Memory buffer |
| SCB0_EZ_DATA137 | 0x40600624 | FULL | Memory buffer |
| SCB0_EZ_DATA138 | 0x40600628 | FULL | Memory buffer |
| SCB0_EZ_DATA139 | 0x4060062C | FULL | Memory buffer |
| SCB0_EZ_DATA140 | 0x40600630 | FULL | Memory buffer |
| SCB0_EZ_DATA141 | 0x40600634 | FULL | Memory buffer |
| SCB0_EZ_DATA142 | 0x40600638 | FULL | Memory buffer |
| SCB0_EZ_DATA143 | 0x4060063C | FULL | Memory buffer |
| SCB0_EZ_DATA144 | 0x40600640 | FULL | Memory buffer |
| SCB0_EZ_DATA145 | 0x40600644 | FULL | Memory buffer |
| SCB0_EZ_DATA146 | 0x40600648 | FULL | Memory buffer |
| SCB0_EZ_DATA147 | 0x4060064C | FULL | Memory buffer |
| SCB0_EZ_DATA148 | 0x40600650 | FULL | Memory buffer |
| SCB0_EZ_DATA149 | 0x40600654 | FULL | Memory buffer |
| SCB0_EZ_DATA150 | 0x40600658 | FULL | Memory buffer |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SCB0_EZ_DATA151 | 0x4060065C | FULL | Memory buffer |
| SCB0_EZ_DATA152 | 0x40600660 | FULL | Memory buffer |
| SCB0_EZ_DATA153 | 0x40600664 | FULL | Memory buffer |
| SCB0_EZ_DATA154 | 0x40600668 | FULL | Memory buffer |
| SCB0_EZ_DATA155 | 0x4060066C | FULL | Memory buffer |
| SCB0_EZ_DATA156 | 0x40600670 | FULL | Memory buffer |
| SCB0_EZ_DATA157 | 0x40600674 | FULL | Memory buffer |
| SCB0_EZ_DATA158 | 0x40600678 | FULL | Memory buffer |
| SCB0_EZ_DATA159 | 0x4060067C | FULL | Memory buffer |
| SCB0_EZ_DATA160 | 0x40600680 | FULL | Memory buffer |
| SCB0_EZ_DATA161 | 0x40600684 | FULL | Memory buffer |
| SCB0_EZ_DATA162 | 0x40600688 | FULL | Memory buffer |
| SCB0_EZ_DATA163 | 0x4060068C | FULL | Memory buffer |
| SCB0_EZ_DATA164 | 0x40600690 | FULL | Memory buffer |
| SCB0_EZ_DATA165 | 0x40600694 | FULL | Memory buffer |
| SCB0_EZ_DATA166 | 0x40600698 | FULL | Memory buffer |
| SCB0_EZ_DATA167 | 0x4060069C | FULL | Memory buffer |
| SCB0_EZ_DATA168 | 0x406006A0 | FULL | Memory buffer |
| SCB0_EZ_DATA169 | 0x406006A4 | FULL | Memory buffer |
| SCB0_EZ_DATA170 | 0x406006A8 | FULL | Memory buffer |
| SCB0_EZ_DATA171 | 0x406006AC | FULL | Memory buffer |
| SCB0_EZ_DATA172 | 0x406006B0 | FULL | Memory buffer |
| SCB0_EZ_DATA173 | 0x406006B4 | FULL | Memory buffer |
| SCB0_EZ_DATA174 | 0x406006B8 | FULL | Memory buffer |
| SCB0_EZ_DATA175 | 0x406006BC | FULL | Memory buffer |
| SCB0_EZ_DATA176 | 0x406006C0 | FULL | Memory buffer |
| SCB0_EZ_DATA177 | 0x406006C4 | FULL | Memory buffer |
| SCB0_EZ_DATA178 | 0x406006C8 | FULL | Memory buffer |
| SCB0_EZ_DATA179 | 0x406006CC | FULL | Memory buffer |
| SCB0_EZ_DATA180 | 0x406006D0 | FULL | Memory buffer |
| SCB0_EZ_DATA181 | 0x406006D4 | FULL | Memory buffer |
| SCB0_EZ_DATA182 | 0x406006D8 | FULL | Memory buffer |
| SCB0_EZ_DATA183 | 0x406006DC | FULL | Memory buffer |
| SCB0_EZ_DATA184 | 0x406006E0 | FULL | Memory buffer |
| SCB0_EZ_DATA185 | 0x406006E4 | FULL | Memory buffer |
| SCB0_EZ_DATA186 | 0x406006E8 | FULL | Memory buffer |
| SCB0_EZ_DATA187 | 0x406006EC | FULL | Memory buffer |
| SCB0_EZ_DATA188 | 0x406006F0 | FULL | Memory buffer |
| SCB0_EZ_DATA189 | 0x406006F4 | FULL | Memory buffer |
| SCB0_EZ_DATA190 | 0x406006F8 | FULL | Memory buffer |
| SCB0_EZ_DATA191 | 0x406006FC | FULL | Memory buffer |
| SCB0_EZ_DATA192 | 0x40600700 | FULL | Memory buffer |
| SCB0_EZ_DATA193 | 0x40600704 | FULL | Memory buffer |
| SCB0_EZ_DATA194 | 0x40600708 | FULL | Memory buffer |
| SCB0_EZ_DATA195 | 0x4060070C | FULL | Memory buffer |
| SCB0_EZ_DATA196 | 0x40600710 | FULL | Memory buffer |
| SCB0_EZ_DATA197 | 0x40600714 | FULL | Memory buffer |
| SCB0_EZ_DATA198 | 0x40600718 | FULL | Memory buffer |
| SCB0_EZ_DATA199 | 0x4060071C | FULL | Memory buffer |
| SCB0_EZ_DATA200 | 0x40600720 | FULL | Memory buffer |
| SCB0_EZ_DATA201 | 0x40600724 | FULL | Memory buffer |
| SCB0_EZ_DATA202 | 0x40600728 | FULL | Memory buffer |
| SCB0_EZ_DATA203 | 0x4060072C | FULL | Memory buffer |
| SCB0_EZ_DATA204 | 0x40600730 | FULL | Memory buffer |
| SCB0_EZ_DATA205 | 0x40600734 | FULL | Memory buffer |
| SCB0_EZ_DATA206 | 0x40600738 | FULL | Memory buffer |
| SCB0_EZ_DATA207 | 0x4060073C | FULL | Memory buffer |
| SCB0_EZ_DATA208 | 0x40600740 | FULL | Memory buffer |
| SCB0_EZ_DATA209 | 0x40600744 | FULL | Memory buffer |
| SCB0_EZ_DATA210 | 0x40600748 | FULL | Memory buffer |
| SCB0_EZ_DATA211 | 0x4060074C | FULL | Memory buffer |
| SCB0_EZ_DATA212 | 0x40600750 | FULL | Memory buffer |
| SCB0_EZ_DATA213 | 0x40600754 | FULL | Memory buffer |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SCB0_EZ_DATA214 | 0x40600758 | FULL | Memory buffer |
| SCB0_EZ_DATA215 | 0x4060075C | FULL | Memory buffer |
| SCB0_EZ_DATA216 | 0x40600760 | FULL | Memory buffer |
| SCB0_EZ_DATA217 | 0x40600764 | FULL | Memory buffer |
| SCB0_EZ_DATA218 | 0x40600768 | FULL | Memory buffer |
| SCB0_EZ_DATA219 | 0x4060076C | FULL | Memory buffer |
| SCB0_EZ_DATA220 | 0x40600770 | FULL | Memory buffer |
| SCB0_EZ_DATA221 | 0x40600774 | FULL | Memory buffer |
| SCB0_EZ_DATA222 | 0x40600778 | FULL | Memory buffer |
| SCB0_EZ_DATA223 | 0x4060077C | FULL | Memory buffer |
| SCB0_EZ_DATA224 | 0x40600780 | FULL | Memory buffer |
| SCB0_EZ_DATA225 | 0x40600784 | FULL | Memory buffer |
| SCB0_EZ_DATA226 | 0x40600788 | FULL | Memory buffer |
| SCB0_EZ_DATA227 | 0x4060078C | FULL | Memory buffer |
| SCB0_EZ_DATA228 | 0x40600790 | FULL | Memory buffer |
| SCB0_EZ_DATA229 | 0x40600794 | FULL | Memory buffer |
| SCB0_EZ_DATA230 | 0x40600798 | FULL | Memory buffer |
| SCB0_EZ_DATA231 | 0x4060079C | FULL | Memory buffer |
| SCB0_EZ_DATA232 | 0x406007A0 | FULL | Memory buffer |
| SCB0_EZ_DATA233 | 0x406007A4 | FULL | Memory buffer |
| SCB0_EZ_DATA234 | 0x406007A8 | FULL | Memory buffer |
| SCB0_EZ_DATA235 | 0x406007AC | FULL | Memory buffer |
| SCB0_EZ_DATA236 | 0x406007B0 | FULL | Memory buffer |
| SCB0_EZ_DATA237 | 0x406007B4 | FULL | Memory buffer |
| SCB0_EZ_DATA238 | 0x406007B8 | FULL | Memory buffer |
| SCB0_EZ_DATA239 | 0x406007BC | FULL | Memory buffer |
| SCB0_EZ_DATA240 | 0x406007C0 | FULL | Memory buffer |
| SCB0_EZ_DATA241 | 0x406007C4 | FULL | Memory buffer |
| SCB0_EZ_DATA242 | 0x406007C8 | FULL | Memory buffer |
| SCB0_EZ_DATA243 | 0x406007CC | FULL | Memory buffer |
| SCB0_EZ_DATA244 | 0x406007D0 | FULL | Memory buffer |
| SCB0_EZ_DATA245 | 0x406007D4 | FULL | Memory buffer |
| SCB0_EZ_DATA246 | 0x406007D8 | FULL | Memory buffer |
| SCB0_EZ_DATA247 | 0x406007DC | FULL | Memory buffer |
| SCB0_EZ_DATA248 | 0x406007E0 | FULL | Memory buffer |
| SCB0_EZ_DATA249 | 0x406007E4 | FULL | Memory buffer |
| SCB0_EZ_DATA250 | 0x406007E8 | FULL | Memory buffer |
| SCB0_EZ_DATA251 | 0x406007EC | FULL | Memory buffer |
| SCB0_EZ_DATA252 | 0x406007F0 | FULL | Memory buffer |
| SCB0_EZ_DATA253 | 0x406007F4 | FULL | Memory buffer |
| SCB0_EZ_DATA254 | 0x406007F8 | FULL | Memory buffer |
| SCB0_EZ_DATA255 | 0x406007FC | FULL | Memory buffer |
| SCB0_INTR_CAUSE | 0x40600E00 | FULL | Active clocked interrupt signal |
| SCB0_INTR_I2C_EC | 0x40600E80 | FULL | Externally clocked I2C interrupt request |
| SCB0_INTR_I2C_EC_MASK | 0x40600E88 | FULL | Externally clocked I2C interrupt mask |
| SCB0_INTR_I2C_EC_MASKED | 0x40600E8C | FULL | Externally clocked I2C interrupt masked |
| SCB0_INTR_SPI_EC | 0x40600EC0 | FULL | Externally clocked SPI interrupt request |
| SCB0_INTR_SPI_EC_MASK | 0x40600EC8 | FULL | Externally clocked SPI interrupt mask |
| SCB0_INTR_SPI_EC_MASKED | 0x40600ECC | FULL | Externally clocked SPI interrupt masked |
| SCB0_INTR_M | 0x40600F00 | FULL | Master interrupt request |
| SCB0_INTR_M_SET | 0x40600F04 | FULL | Master interrupt set request |
| SCB0_INTR_M_MASK | 0x40600F08 | FULL | Master interrupt mask |
| SCB0_INTR_M_MASKED | 0x40600F0C | FULL | Master interrupt masked request |
| SCB0_INTR_S | 0x40600F40 | FULL | Slave interrupt request |
| SCB0_INTR_S_SET | 0x40600F44 | FULL | Slave interrupt set request |
| SCB0_INTR_S_MASK | 0x40600F48 | FULL | Slave interrupt mask |
| SCB0_INTR_S_MASKED | 0x40600F4C | FULL | Slave interrupt masked request |
| SCB0_INTR_TX | 0x40600F80 | FULL | Transmitter interrupt request |
| SCB0_INTR_TX_SET | 0x40600F84 | FULL | Transmitter interrupt set request |
| SCB0_INTR_TX_MASK | 0x40600F88 | FULL | Transmitter interrupt mask |
| SCB0_INTR_TX_MASKED | 0x40600F8C | FULL | Transmitter interrupt masked request |
| SCB0_INTR_RX | 0x40600FC0 | FULL | Receiver interrupt request |
| SCB0_INTR_RX_SET | 0x40600FC4 | FULL | Receiver interrupt set request |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SCB0_INTR_RX_MASK | 0x40600FC8 | FULL | Receiver interrupt mask |
| SCB0_INTR_RX_MASKED | 0x40600FCC | FULL | Receiver interrupt masked request |

## 26.2 SCB 1

**Description** Serial Communications Block (SPI/UART/I2C)
**Base Address** 0x40610000
**Size** 0x10000
**Slave Num** MMIO6 - 1

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SCB1_CTRL | 0x40610000 | FULL | Generic control<br>Note:CMD_RESP_MODE is not available for this register |
| SCB1_STATUS | 0x40610004 | FULL | Generic status |
| SCB1_SPI_CTRL | 0x40610020 | FULL | SPI control |
| SCB1_SPI_STATUS | 0x40610024 | FULL | SPI status |
| SCB1_SPI_TX_CTRL | 0x40610028 | FULL | SPI transmitter control |
| SCB1_SPI_RX_CTRL | 0x4061002C | FULL | SPI receiver control |
| SCB1_UART_CTRL | 0x40610040 | FULL | UART control |
| SCB1_UART_TX_CTRL | 0x40610044 | FULL | UART transmitter control |
| SCB1_UART_RX_CTRL | 0x40610048 | FULL | UART receiver control |
| SCB1_UART_RX_STATUS | 0x4061004C | FULL | UART receiver status |
| SCB1_UART_FLOW_CTRL | 0x40610050 | FULL | UART flow control |
| SCB1_I2C_CTRL | 0x40610060 | FULL | I2C control |
| SCB1_I2C_STATUS | 0x40610064 | FULL | I2C status<br>Note:I2C_EC_BUSY is not available for this register |
| SCB1_I2C_M_CMD | 0x40610068 | FULL | I2C master command |
| SCB1_I2C_S_CMD | 0x4061006C | FULL | I2C slave command |
| SCB1_I2C_CFG | 0x40610070 | FULL | I2C configuration |
| SCB1_TX_CTRL | 0x40610200 | FULL | Transmitter control |
| SCB1_TX_FIFO_CTRL | 0x40610204 | FULL | Transmitter FIFO control |
| SCB1_TX_FIFO_STATUS | 0x40610208 | FULL | Transmitter FIFO status |
| SCB1_TX_FIFO_WR | 0x40610240 | FULL | Transmitter FIFO write |
| SCB1_RX_CTRL | 0x40610300 | FULL | Receiver control |
| SCB1_RX_FIFO_CTRL | 0x40610304 | FULL | Receiver FIFO control |
| SCB1_RX_FIFO_STATUS | 0x40610308 | FULL | Receiver FIFO status |
| SCB1_RX_MATCH | 0x40610310 | FULL | Slave address and mask |
| SCB1_RX_FIFO_RD | 0x40610340 | FULL | Receiver FIFO read |
| SCB1_RX_FIFO_RD_SILENT | 0x40610344 | FULL | Receiver FIFO read silent |
| SCB1_EZ_DATA0 | 0x40610400 | FULL | Memory buffer |
| SCB1_EZ_DATA1 | 0x40610404 | FULL | Memory buffer |
| SCB1_EZ_DATA2 | 0x40610408 | FULL | Memory buffer |
| SCB1_EZ_DATA3 | 0x4061040C | FULL | Memory buffer |
| SCB1_EZ_DATA4 | 0x40610410 | FULL | Memory buffer |
| SCB1_EZ_DATA5 | 0x40610414 | FULL | Memory buffer |
| SCB1_EZ_DATA6 | 0x40610418 | FULL | Memory buffer |
| SCB1_EZ_DATA7 | 0x4061041C | FULL | Memory buffer |
| SCB1_EZ_DATA8 | 0x40610420 | FULL | Memory buffer |
| SCB1_EZ_DATA9 | 0x40610424 | FULL | Memory buffer |
| SCB1_EZ_DATA10 | 0x40610428 | FULL | Memory buffer |
| SCB1_EZ_DATA11 | 0x4061042C | FULL | Memory buffer |
| SCB1_EZ_DATA12 | 0x40610430 | FULL | Memory buffer |
| SCB1_EZ_DATA13 | 0x40610434 | FULL | Memory buffer |
| SCB1_EZ_DATA14 | 0x40610438 | FULL | Memory buffer |
| SCB1_EZ_DATA15 | 0x4061043C | FULL | Memory buffer |
| SCB1_EZ_DATA16 | 0x40610440 | FULL | Memory buffer |
| SCB1_EZ_DATA17 | 0x40610444 | FULL | Memory buffer |
| SCB1_EZ_DATA18 | 0x40610448 | FULL | Memory buffer |
| SCB1_EZ_DATA19 | 0x4061044C | FULL | Memory buffer |
| SCB1_EZ_DATA20 | 0x40610450 | FULL | Memory buffer |
| SCB1_EZ_DATA21 | 0x40610454 | FULL | Memory buffer |
| SCB1_EZ_DATA22 | 0x40610458 | FULL | Memory buffer |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SCB1_EZ_DATA23 | 0x4061045C | FULL | Memory buffer |
| SCB1_EZ_DATA24 | 0x40610460 | FULL | Memory buffer |
| SCB1_EZ_DATA25 | 0x40610464 | FULL | Memory buffer |
| SCB1_EZ_DATA26 | 0x40610468 | FULL | Memory buffer |
| SCB1_EZ_DATA27 | 0x4061046C | FULL | Memory buffer |
| SCB1_EZ_DATA28 | 0x40610470 | FULL | Memory buffer |
| SCB1_EZ_DATA29 | 0x40610474 | FULL | Memory buffer |
| SCB1_EZ_DATA30 | 0x40610478 | FULL | Memory buffer |
| SCB1_EZ_DATA31 | 0x4061047C | FULL | Memory buffer |
| SCB1_EZ_DATA32 | 0x40610480 | FULL | Memory buffer |
| SCB1_EZ_DATA33 | 0x40610484 | FULL | Memory buffer |
| SCB1_EZ_DATA34 | 0x40610488 | FULL | Memory buffer |
| SCB1_EZ_DATA35 | 0x4061048C | FULL | Memory buffer |
| SCB1_EZ_DATA36 | 0x40610490 | FULL | Memory buffer |
| SCB1_EZ_DATA37 | 0x40610494 | FULL | Memory buffer |
| SCB1_EZ_DATA38 | 0x40610498 | FULL | Memory buffer |
| SCB1_EZ_DATA39 | 0x4061049C | FULL | Memory buffer |
| SCB1_EZ_DATA40 | 0x406104A0 | FULL | Memory buffer |
| SCB1_EZ_DATA41 | 0x406104A4 | FULL | Memory buffer |
| SCB1_EZ_DATA42 | 0x406104A8 | FULL | Memory buffer |
| SCB1_EZ_DATA43 | 0x406104AC | FULL | Memory buffer |
| SCB1_EZ_DATA44 | 0x406104B0 | FULL | Memory buffer |
| SCB1_EZ_DATA45 | 0x406104B4 | FULL | Memory buffer |
| SCB1_EZ_DATA46 | 0x406104B8 | FULL | Memory buffer |
| SCB1_EZ_DATA47 | 0x406104BC | FULL | Memory buffer |
| SCB1_EZ_DATA48 | 0x406104C0 | FULL | Memory buffer |
| SCB1_EZ_DATA49 | 0x406104C4 | FULL | Memory buffer |
| SCB1_EZ_DATA50 | 0x406104C8 | FULL | Memory buffer |
| SCB1_EZ_DATA51 | 0x406104CC | FULL | Memory buffer |
| SCB1_EZ_DATA52 | 0x406104D0 | FULL | Memory buffer |
| SCB1_EZ_DATA53 | 0x406104D4 | FULL | Memory buffer |
| SCB1_EZ_DATA54 | 0x406104D8 | FULL | Memory buffer |
| SCB1_EZ_DATA55 | 0x406104DC | FULL | Memory buffer |
| SCB1_EZ_DATA56 | 0x406104E0 | FULL | Memory buffer |
| SCB1_EZ_DATA57 | 0x406104E4 | FULL | Memory buffer |
| SCB1_EZ_DATA58 | 0x406104E8 | FULL | Memory buffer |
| SCB1_EZ_DATA59 | 0x406104EC | FULL | Memory buffer |
| SCB1_EZ_DATA60 | 0x406104F0 | FULL | Memory buffer |
| SCB1_EZ_DATA61 | 0x406104F4 | FULL | Memory buffer |
| SCB1_EZ_DATA62 | 0x406104F8 | FULL | Memory buffer |
| SCB1_EZ_DATA63 | 0x406104FC | FULL | Memory buffer |
| SCB1_EZ_DATA64 | 0x40610500 | FULL | Memory buffer |
| SCB1_EZ_DATA65 | 0x40610504 | FULL | Memory buffer |
| SCB1_EZ_DATA66 | 0x40610508 | FULL | Memory buffer |
| SCB1_EZ_DATA67 | 0x4061050C | FULL | Memory buffer |
| SCB1_EZ_DATA68 | 0x40610510 | FULL | Memory buffer |
| SCB1_EZ_DATA69 | 0x40610514 | FULL | Memory buffer |
| SCB1_EZ_DATA70 | 0x40610518 | FULL | Memory buffer |
| SCB1_EZ_DATA71 | 0x4061051C | FULL | Memory buffer |
| SCB1_EZ_DATA72 | 0x40610520 | FULL | Memory buffer |
| SCB1_EZ_DATA73 | 0x40610524 | FULL | Memory buffer |
| SCB1_EZ_DATA74 | 0x40610528 | FULL | Memory buffer |
| SCB1_EZ_DATA75 | 0x4061052C | FULL | Memory buffer |
| SCB1_EZ_DATA76 | 0x40610530 | FULL | Memory buffer |
| SCB1_EZ_DATA77 | 0x40610534 | FULL | Memory buffer |
| SCB1_EZ_DATA78 | 0x40610538 | FULL | Memory buffer |
| SCB1_EZ_DATA79 | 0x4061053C | FULL | Memory buffer |
| SCB1_EZ_DATA80 | 0x40610540 | FULL | Memory buffer |
| SCB1_EZ_DATA81 | 0x40610544 | FULL | Memory buffer |
| SCB1_EZ_DATA82 | 0x40610548 | FULL | Memory buffer |
| SCB1_EZ_DATA83 | 0x4061054C | FULL | Memory buffer |
| SCB1_EZ_DATA84 | 0x40610550 | FULL | Memory buffer |
| SCB1_EZ_DATA85 | 0x40610554 | FULL | Memory buffer |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SCB1_EZ_DATA86 | 0x40610558 | FULL | Memory buffer |
| SCB1_EZ_DATA87 | 0x4061055C | FULL | Memory buffer |
| SCB1_EZ_DATA88 | 0x40610560 | FULL | Memory buffer |
| SCB1_EZ_DATA89 | 0x40610564 | FULL | Memory buffer |
| SCB1_EZ_DATA90 | 0x40610568 | FULL | Memory buffer |
| SCB1_EZ_DATA91 | 0x4061056C | FULL | Memory buffer |
| SCB1_EZ_DATA92 | 0x40610570 | FULL | Memory buffer |
| SCB1_EZ_DATA93 | 0x40610574 | FULL | Memory buffer |
| SCB1_EZ_DATA94 | 0x40610578 | FULL | Memory buffer |
| SCB1_EZ_DATA95 | 0x4061057C | FULL | Memory buffer |
| SCB1_EZ_DATA96 | 0x40610580 | FULL | Memory buffer |
| SCB1_EZ_DATA97 | 0x40610584 | FULL | Memory buffer |
| SCB1_EZ_DATA98 | 0x40610588 | FULL | Memory buffer |
| SCB1_EZ_DATA99 | 0x4061058C | FULL | Memory buffer |
| SCB1_EZ_DATA100 | 0x40610590 | FULL | Memory buffer |
| SCB1_EZ_DATA101 | 0x40610594 | FULL | Memory buffer |
| SCB1_EZ_DATA102 | 0x40610598 | FULL | Memory buffer |
| SCB1_EZ_DATA103 | 0x4061059C | FULL | Memory buffer |
| SCB1_EZ_DATA104 | 0x406105A0 | FULL | Memory buffer |
| SCB1_EZ_DATA105 | 0x406105A4 | FULL | Memory buffer |
| SCB1_EZ_DATA106 | 0x406105A8 | FULL | Memory buffer |
| SCB1_EZ_DATA107 | 0x406105AC | FULL | Memory buffer |
| SCB1_EZ_DATA108 | 0x406105B0 | FULL | Memory buffer |
| SCB1_EZ_DATA109 | 0x406105B4 | FULL | Memory buffer |
| SCB1_EZ_DATA110 | 0x406105B8 | FULL | Memory buffer |
| SCB1_EZ_DATA111 | 0x406105BC | FULL | Memory buffer |
| SCB1_EZ_DATA112 | 0x406105C0 | FULL | Memory buffer |
| SCB1_EZ_DATA113 | 0x406105C4 | FULL | Memory buffer |
| SCB1_EZ_DATA114 | 0x406105C8 | FULL | Memory buffer |
| SCB1_EZ_DATA115 | 0x406105CC | FULL | Memory buffer |
| SCB1_EZ_DATA116 | 0x406105D0 | FULL | Memory buffer |
| SCB1_EZ_DATA117 | 0x406105D4 | FULL | Memory buffer |
| SCB1_EZ_DATA118 | 0x406105D8 | FULL | Memory buffer |
| SCB1_EZ_DATA119 | 0x406105DC | FULL | Memory buffer |
| SCB1_EZ_DATA120 | 0x406105E0 | FULL | Memory buffer |
| SCB1_EZ_DATA121 | 0x406105E4 | FULL | Memory buffer |
| SCB1_EZ_DATA122 | 0x406105E8 | FULL | Memory buffer |
| SCB1_EZ_DATA123 | 0x406105EC | FULL | Memory buffer |
| SCB1_EZ_DATA124 | 0x406105F0 | FULL | Memory buffer |
| SCB1_EZ_DATA125 | 0x406105F4 | FULL | Memory buffer |
| SCB1_EZ_DATA126 | 0x406105F8 | FULL | Memory buffer |
| SCB1_EZ_DATA127 | 0x406105FC | FULL | Memory buffer |
| SCB1_EZ_DATA128 | 0x40610600 | FULL | Memory buffer |
| SCB1_EZ_DATA129 | 0x40610604 | FULL | Memory buffer |
| SCB1_EZ_DATA130 | 0x40610608 | FULL | Memory buffer |
| SCB1_EZ_DATA131 | 0x4061060C | FULL | Memory buffer |
| SCB1_EZ_DATA132 | 0x40610610 | FULL | Memory buffer |
| SCB1_EZ_DATA133 | 0x40610614 | FULL | Memory buffer |
| SCB1_EZ_DATA134 | 0x40610618 | FULL | Memory buffer |
| SCB1_EZ_DATA135 | 0x4061061C | FULL | Memory buffer |
| SCB1_EZ_DATA136 | 0x40610620 | FULL | Memory buffer |
| SCB1_EZ_DATA137 | 0x40610624 | FULL | Memory buffer |
| SCB1_EZ_DATA138 | 0x40610628 | FULL | Memory buffer |
| SCB1_EZ_DATA139 | 0x4061062C | FULL | Memory buffer |
| SCB1_EZ_DATA140 | 0x40610630 | FULL | Memory buffer |
| SCB1_EZ_DATA141 | 0x40610634 | FULL | Memory buffer |
| SCB1_EZ_DATA142 | 0x40610638 | FULL | Memory buffer |
| SCB1_EZ_DATA143 | 0x4061063C | FULL | Memory buffer |
| SCB1_EZ_DATA144 | 0x40610640 | FULL | Memory buffer |
| SCB1_EZ_DATA145 | 0x40610644 | FULL | Memory buffer |
| SCB1_EZ_DATA146 | 0x40610648 | FULL | Memory buffer |
| SCB1_EZ_DATA147 | 0x4061064C | FULL | Memory buffer |
| SCB1_EZ_DATA148 | 0x40610650 | FULL | Memory buffer |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SCB1_EZ_DATA149 | 0x40610654 | FULL | Memory buffer |
| SCB1_EZ_DATA150 | 0x40610658 | FULL | Memory buffer |
| SCB1_EZ_DATA151 | 0x4061065C | FULL | Memory buffer |
| SCB1_EZ_DATA152 | 0x40610660 | FULL | Memory buffer |
| SCB1_EZ_DATA153 | 0x40610664 | FULL | Memory buffer |
| SCB1_EZ_DATA154 | 0x40610668 | FULL | Memory buffer |
| SCB1_EZ_DATA155 | 0x4061066C | FULL | Memory buffer |
| SCB1_EZ_DATA156 | 0x40610670 | FULL | Memory buffer |
| SCB1_EZ_DATA157 | 0x40610674 | FULL | Memory buffer |
| SCB1_EZ_DATA158 | 0x40610678 | FULL | Memory buffer |
| SCB1_EZ_DATA159 | 0x4061067C | FULL | Memory buffer |
| SCB1_EZ_DATA160 | 0x40610680 | FULL | Memory buffer |
| SCB1_EZ_DATA161 | 0x40610684 | FULL | Memory buffer |
| SCB1_EZ_DATA162 | 0x40610688 | FULL | Memory buffer |
| SCB1_EZ_DATA163 | 0x4061068C | FULL | Memory buffer |
| SCB1_EZ_DATA164 | 0x40610690 | FULL | Memory buffer |
| SCB1_EZ_DATA165 | 0x40610694 | FULL | Memory buffer |
| SCB1_EZ_DATA166 | 0x40610698 | FULL | Memory buffer |
| SCB1_EZ_DATA167 | 0x4061069C | FULL | Memory buffer |
| SCB1_EZ_DATA168 | 0x406106A0 | FULL | Memory buffer |
| SCB1_EZ_DATA169 | 0x406106A4 | FULL | Memory buffer |
| SCB1_EZ_DATA170 | 0x406106A8 | FULL | Memory buffer |
| SCB1_EZ_DATA171 | 0x406106AC | FULL | Memory buffer |
| SCB1_EZ_DATA172 | 0x406106B0 | FULL | Memory buffer |
| SCB1_EZ_DATA173 | 0x406106B4 | FULL | Memory buffer |
| SCB1_EZ_DATA174 | 0x406106B8 | FULL | Memory buffer |
| SCB1_EZ_DATA175 | 0x406106BC | FULL | Memory buffer |
| SCB1_EZ_DATA176 | 0x406106C0 | FULL | Memory buffer |
| SCB1_EZ_DATA177 | 0x406106C4 | FULL | Memory buffer |
| SCB1_EZ_DATA178 | 0x406106C8 | FULL | Memory buffer |
| SCB1_EZ_DATA179 | 0x406106CC | FULL | Memory buffer |
| SCB1_EZ_DATA180 | 0x406106D0 | FULL | Memory buffer |
| SCB1_EZ_DATA181 | 0x406106D4 | FULL | Memory buffer |
| SCB1_EZ_DATA182 | 0x406106D8 | FULL | Memory buffer |
| SCB1_EZ_DATA183 | 0x406106DC | FULL | Memory buffer |
| SCB1_EZ_DATA184 | 0x406106E0 | FULL | Memory buffer |
| SCB1_EZ_DATA185 | 0x406106E4 | FULL | Memory buffer |
| SCB1_EZ_DATA186 | 0x406106E8 | FULL | Memory buffer |
| SCB1_EZ_DATA187 | 0x406106EC | FULL | Memory buffer |
| SCB1_EZ_DATA188 | 0x406106F0 | FULL | Memory buffer |
| SCB1_EZ_DATA189 | 0x406106F4 | FULL | Memory buffer |
| SCB1_EZ_DATA190 | 0x406106F8 | FULL | Memory buffer |
| SCB1_EZ_DATA191 | 0x406106FC | FULL | Memory buffer |
| SCB1_EZ_DATA192 | 0x40610700 | FULL | Memory buffer |
| SCB1_EZ_DATA193 | 0x40610704 | FULL | Memory buffer |
| SCB1_EZ_DATA194 | 0x40610708 | FULL | Memory buffer |
| SCB1_EZ_DATA195 | 0x4061070C | FULL | Memory buffer |
| SCB1_EZ_DATA196 | 0x40610710 | FULL | Memory buffer |
| SCB1_EZ_DATA197 | 0x40610714 | FULL | Memory buffer |
| SCB1_EZ_DATA198 | 0x40610718 | FULL | Memory buffer |
| SCB1_EZ_DATA199 | 0x4061071C | FULL | Memory buffer |
| SCB1_EZ_DATA200 | 0x40610720 | FULL | Memory buffer |
| SCB1_EZ_DATA201 | 0x40610724 | FULL | Memory buffer |
| SCB1_EZ_DATA202 | 0x40610728 | FULL | Memory buffer |
| SCB1_EZ_DATA203 | 0x4061072C | FULL | Memory buffer |
| SCB1_EZ_DATA204 | 0x40610730 | FULL | Memory buffer |
| SCB1_EZ_DATA205 | 0x40610734 | FULL | Memory buffer |
| SCB1_EZ_DATA206 | 0x40610738 | FULL | Memory buffer |
| SCB1_EZ_DATA207 | 0x4061073C | FULL | Memory buffer |
| SCB1_EZ_DATA208 | 0x40610740 | FULL | Memory buffer |
| SCB1_EZ_DATA209 | 0x40610744 | FULL | Memory buffer |
| SCB1_EZ_DATA210 | 0x40610748 | FULL | Memory buffer |
| SCB1_EZ_DATA211 | 0x4061074C | FULL | Memory buffer |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SCB1_EZ_DATA212 | 0x40610750 | FULL | Memory buffer |
| SCB1_EZ_DATA213 | 0x40610754 | FULL | Memory buffer |
| SCB1_EZ_DATA214 | 0x40610758 | FULL | Memory buffer |
| SCB1_EZ_DATA215 | 0x4061075C | FULL | Memory buffer |
| SCB1_EZ_DATA216 | 0x40610760 | FULL | Memory buffer |
| SCB1_EZ_DATA217 | 0x40610764 | FULL | Memory buffer |
| SCB1_EZ_DATA218 | 0x40610768 | FULL | Memory buffer |
| SCB1_EZ_DATA219 | 0x4061076C | FULL | Memory buffer |
| SCB1_EZ_DATA220 | 0x40610770 | FULL | Memory buffer |
| SCB1_EZ_DATA221 | 0x40610774 | FULL | Memory buffer |
| SCB1_EZ_DATA222 | 0x40610778 | FULL | Memory buffer |
| SCB1_EZ_DATA223 | 0x4061077C | FULL | Memory buffer |
| SCB1_EZ_DATA224 | 0x40610780 | FULL | Memory buffer |
| SCB1_EZ_DATA225 | 0x40610784 | FULL | Memory buffer |
| SCB1_EZ_DATA226 | 0x40610788 | FULL | Memory buffer |
| SCB1_EZ_DATA227 | 0x4061078C | FULL | Memory buffer |
| SCB1_EZ_DATA228 | 0x40610790 | FULL | Memory buffer |
| SCB1_EZ_DATA229 | 0x40610794 | FULL | Memory buffer |
| SCB1_EZ_DATA230 | 0x40610798 | FULL | Memory buffer |
| SCB1_EZ_DATA231 | 0x4061079C | FULL | Memory buffer |
| SCB1_EZ_DATA232 | 0x406107A0 | FULL | Memory buffer |
| SCB1_EZ_DATA233 | 0x406107A4 | FULL | Memory buffer |
| SCB1_EZ_DATA234 | 0x406107A8 | FULL | Memory buffer |
| SCB1_EZ_DATA235 | 0x406107AC | FULL | Memory buffer |
| SCB1_EZ_DATA236 | 0x406107B0 | FULL | Memory buffer |
| SCB1_EZ_DATA237 | 0x406107B4 | FULL | Memory buffer |
| SCB1_EZ_DATA238 | 0x406107B8 | FULL | Memory buffer |
| SCB1_EZ_DATA239 | 0x406107BC | FULL | Memory buffer |
| SCB1_EZ_DATA240 | 0x406107C0 | FULL | Memory buffer |
| SCB1_EZ_DATA241 | 0x406107C4 | FULL | Memory buffer |
| SCB1_EZ_DATA242 | 0x406107C8 | FULL | Memory buffer |
| SCB1_EZ_DATA243 | 0x406107CC | FULL | Memory buffer |
| SCB1_EZ_DATA244 | 0x406107D0 | FULL | Memory buffer |
| SCB1_EZ_DATA245 | 0x406107D4 | FULL | Memory buffer |
| SCB1_EZ_DATA246 | 0x406107D8 | FULL | Memory buffer |
| SCB1_EZ_DATA247 | 0x406107DC | FULL | Memory buffer |
| SCB1_EZ_DATA248 | 0x406107E0 | FULL | Memory buffer |
| SCB1_EZ_DATA249 | 0x406107E4 | FULL | Memory buffer |
| SCB1_EZ_DATA250 | 0x406107E8 | FULL | Memory buffer |
| SCB1_EZ_DATA251 | 0x406107EC | FULL | Memory buffer |
| SCB1_EZ_DATA252 | 0x406107F0 | FULL | Memory buffer |
| SCB1_EZ_DATA253 | 0x406107F4 | FULL | Memory buffer |
| SCB1_EZ_DATA254 | 0x406107F8 | FULL | Memory buffer |
| SCB1_EZ_DATA255 | 0x406107FC | FULL | Memory buffer |
| SCB1_INTR_CAUSE | 0x40610E00 | FULL | Active clocked interrupt signal<br>Note:I2C_EC is not available for this register |
| SCB1_INTR_SPI_EC | 0x40610EC0 | FULL | Externally clocked SPI interrupt request |
| SCB1_INTR_SPI_EC_MASK | 0x40610EC8 | FULL | Externally clocked SPI interrupt mask |
| SCB1_INTR_SPI_EC_MASKED | 0x40610ECC | FULL | Externally clocked SPI interrupt masked |
| SCB1_INTR_M | 0x40610F00 | FULL | Master interrupt request |
| SCB1_INTR_M_SET | 0x40610F04 | FULL | Master interrupt set request |
| SCB1_INTR_M_MASK | 0x40610F08 | FULL | Master interrupt mask |
| SCB1_INTR_M_MASKED | 0x40610F0C | FULL | Master interrupt masked request |
| SCB1_INTR_S | 0x40610F40 | FULL | Slave interrupt request |
| SCB1_INTR_S_SET | 0x40610F44 | FULL | Slave interrupt set request |
| SCB1_INTR_S_MASK | 0x40610F48 | FULL | Slave interrupt mask |
| SCB1_INTR_S_MASKED | 0x40610F4C | FULL | Slave interrupt masked request |
| SCB1_INTR_TX | 0x40610F80 | FULL | Transmitter interrupt request |
| SCB1_INTR_TX_SET | 0x40610F84 | FULL | Transmitter interrupt set request |
| SCB1_INTR_TX_MASK | 0x40610F88 | FULL | Transmitter interrupt mask |
| SCB1_INTR_TX_MASKED | 0x40610F8C | FULL | Transmitter interrupt masked request |
| SCB1_INTR_RX | 0x40610FC0 | FULL | Receiver interrupt request |
| SCB1_INTR_RX_SET | 0x40610FC4 | FULL | Receiver interrupt set request |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SCB1_INTR_RX_MASK | 0x40610FC8 | FULL | Receiver interrupt mask |
| SCB1_INTR_RX_MASKED | 0x40610FCC | FULL | Receiver interrupt masked request |

## 26.3 SCB 2

**Description** Serial Communications Block (SPI/UART/I2C)
**Base Address** 0x40620000
**Size** 0x10000
**Slave Num** MMIO6 - 2

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SCB2_CTRL | 0x40620000 | FULL | Generic control<br>Note:CMD_RESP_MODE is not available for this register |
| SCB2_STATUS | 0x40620004 | FULL | Generic status |
| SCB2_SPI_CTRL | 0x40620020 | FULL | SPI control |
| SCB2_SPI_STATUS | 0x40620024 | FULL | SPI status |
| SCB2_SPI_TX_CTRL | 0x40620028 | FULL | SPI transmitter control |
| SCB2_SPI_RX_CTRL | 0x4062002C | FULL | SPI receiver control |
| SCB2_UART_CTRL | 0x40620040 | FULL | UART control |
| SCB2_UART_TX_CTRL | 0x40620044 | FULL | UART transmitter control |
| SCB2_UART_RX_CTRL | 0x40620048 | FULL | UART receiver control |
| SCB2_UART_RX_STATUS | 0x4062004C | FULL | UART receiver status |
| SCB2_UART_FLOW_CTRL | 0x40620050 | FULL | UART flow control |
| SCB2_I2C_CTRL | 0x40620060 | FULL | I2C control |
| SCB2_I2C_STATUS | 0x40620064 | FULL | I2C status<br>Note:I2C_EC_BUSY is not available for this register |
| SCB2_I2C_M_CMD | 0x40620068 | FULL | I2C master command |
| SCB2_I2C_S_CMD | 0x4062006C | FULL | I2C slave command |
| SCB2_I2C_CFG | 0x40620070 | FULL | I2C configuration |
| SCB2_TX_CTRL | 0x40620200 | FULL | Transmitter control |
| SCB2_TX_FIFO_CTRL | 0x40620204 | FULL | Transmitter FIFO control |
| SCB2_TX_FIFO_STATUS | 0x40620208 | FULL | Transmitter FIFO status |
| SCB2_TX_FIFO_WR | 0x40620240 | FULL | Transmitter FIFO write |
| SCB2_RX_CTRL | 0x40620300 | FULL | Receiver control |
| SCB2_RX_FIFO_CTRL | 0x40620304 | FULL | Receiver FIFO control |
| SCB2_RX_FIFO_STATUS | 0x40620308 | FULL | Receiver FIFO status |
| SCB2_RX_MATCH | 0x40620310 | FULL | Slave address and mask |
| SCB2_RX_FIFO_RD | 0x40620340 | FULL | Receiver FIFO read |
| SCB2_RX_FIFO_RD_SILENT | 0x40620344 | FULL | Receiver FIFO read silent |
| SCB2_EZ_DATA0 | 0x40620400 | FULL | Memory buffer |
| SCB2_EZ_DATA1 | 0x40620404 | FULL | Memory buffer |
| SCB2_EZ_DATA2 | 0x40620408 | FULL | Memory buffer |
| SCB2_EZ_DATA3 | 0x4062040C | FULL | Memory buffer |
| SCB2_EZ_DATA4 | 0x40620410 | FULL | Memory buffer |
| SCB2_EZ_DATA5 | 0x40620414 | FULL | Memory buffer |
| SCB2_EZ_DATA6 | 0x40620418 | FULL | Memory buffer |
| SCB2_EZ_DATA7 | 0x4062041C | FULL | Memory buffer |
| SCB2_EZ_DATA8 | 0x40620420 | FULL | Memory buffer |
| SCB2_EZ_DATA9 | 0x40620424 | FULL | Memory buffer |
| SCB2_EZ_DATA10 | 0x40620428 | FULL | Memory buffer |
| SCB2_EZ_DATA11 | 0x4062042C | FULL | Memory buffer |
| SCB2_EZ_DATA12 | 0x40620430 | FULL | Memory buffer |
| SCB2_EZ_DATA13 | 0x40620434 | FULL | Memory buffer |
| SCB2_EZ_DATA14 | 0x40620438 | FULL | Memory buffer |
| SCB2_EZ_DATA15 | 0x4062043C | FULL | Memory buffer |
| SCB2_EZ_DATA16 | 0x40620440 | FULL | Memory buffer |
| SCB2_EZ_DATA17 | 0x40620444 | FULL | Memory buffer |
| SCB2_EZ_DATA18 | 0x40620448 | FULL | Memory buffer |
| SCB2_EZ_DATA19 | 0x4062044C | FULL | Memory buffer |
| SCB2_EZ_DATA20 | 0x40620450 | FULL | Memory buffer |
| SCB2_EZ_DATA21 | 0x40620454 | FULL | Memory buffer |
| SCB2_EZ_DATA22 | 0x40620458 | FULL | Memory buffer |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SCB2_EZ_DATA23 | 0x4062045C | FULL | Memory buffer |
| SCB2_EZ_DATA24 | 0x40620460 | FULL | Memory buffer |
| SCB2_EZ_DATA25 | 0x40620464 | FULL | Memory buffer |
| SCB2_EZ_DATA26 | 0x40620468 | FULL | Memory buffer |
| SCB2_EZ_DATA27 | 0x4062046C | FULL | Memory buffer |
| SCB2_EZ_DATA28 | 0x40620470 | FULL | Memory buffer |
| SCB2_EZ_DATA29 | 0x40620474 | FULL | Memory buffer |
| SCB2_EZ_DATA30 | 0x40620478 | FULL | Memory buffer |
| SCB2_EZ_DATA31 | 0x4062047C | FULL | Memory buffer |
| SCB2_EZ_DATA32 | 0x40620480 | FULL | Memory buffer |
| SCB2_EZ_DATA33 | 0x40620484 | FULL | Memory buffer |
| SCB2_EZ_DATA34 | 0x40620488 | FULL | Memory buffer |
| SCB2_EZ_DATA35 | 0x4062048C | FULL | Memory buffer |
| SCB2_EZ_DATA36 | 0x40620490 | FULL | Memory buffer |
| SCB2_EZ_DATA37 | 0x40620494 | FULL | Memory buffer |
| SCB2_EZ_DATA38 | 0x40620498 | FULL | Memory buffer |
| SCB2_EZ_DATA39 | 0x4062049C | FULL | Memory buffer |
| SCB2_EZ_DATA40 | 0x406204A0 | FULL | Memory buffer |
| SCB2_EZ_DATA41 | 0x406204A4 | FULL | Memory buffer |
| SCB2_EZ_DATA42 | 0x406204A8 | FULL | Memory buffer |
| SCB2_EZ_DATA43 | 0x406204AC | FULL | Memory buffer |
| SCB2_EZ_DATA44 | 0x406204B0 | FULL | Memory buffer |
| SCB2_EZ_DATA45 | 0x406204B4 | FULL | Memory buffer |
| SCB2_EZ_DATA46 | 0x406204B8 | FULL | Memory buffer |
| SCB2_EZ_DATA47 | 0x406204BC | FULL | Memory buffer |
| SCB2_EZ_DATA48 | 0x406204C0 | FULL | Memory buffer |
| SCB2_EZ_DATA49 | 0x406204C4 | FULL | Memory buffer |
| SCB2_EZ_DATA50 | 0x406204C8 | FULL | Memory buffer |
| SCB2_EZ_DATA51 | 0x406204CC | FULL | Memory buffer |
| SCB2_EZ_DATA52 | 0x406204D0 | FULL | Memory buffer |
| SCB2_EZ_DATA53 | 0x406204D4 | FULL | Memory buffer |
| SCB2_EZ_DATA54 | 0x406204D8 | FULL | Memory buffer |
| SCB2_EZ_DATA55 | 0x406204DC | FULL | Memory buffer |
| SCB2_EZ_DATA56 | 0x406204E0 | FULL | Memory buffer |
| SCB2_EZ_DATA57 | 0x406204E4 | FULL | Memory buffer |
| SCB2_EZ_DATA58 | 0x406204E8 | FULL | Memory buffer |
| SCB2_EZ_DATA59 | 0x406204EC | FULL | Memory buffer |
| SCB2_EZ_DATA60 | 0x406204F0 | FULL | Memory buffer |
| SCB2_EZ_DATA61 | 0x406204F4 | FULL | Memory buffer |
| SCB2_EZ_DATA62 | 0x406204F8 | FULL | Memory buffer |
| SCB2_EZ_DATA63 | 0x406204FC | FULL | Memory buffer |
| SCB2_EZ_DATA64 | 0x40620500 | FULL | Memory buffer |
| SCB2_EZ_DATA65 | 0x40620504 | FULL | Memory buffer |
| SCB2_EZ_DATA66 | 0x40620508 | FULL | Memory buffer |
| SCB2_EZ_DATA67 | 0x4062050C | FULL | Memory buffer |
| SCB2_EZ_DATA68 | 0x40620510 | FULL | Memory buffer |
| SCB2_EZ_DATA69 | 0x40620514 | FULL | Memory buffer |
| SCB2_EZ_DATA70 | 0x40620518 | FULL | Memory buffer |
| SCB2_EZ_DATA71 | 0x4062051C | FULL | Memory buffer |
| SCB2_EZ_DATA72 | 0x40620520 | FULL | Memory buffer |
| SCB2_EZ_DATA73 | 0x40620524 | FULL | Memory buffer |
| SCB2_EZ_DATA74 | 0x40620528 | FULL | Memory buffer |
| SCB2_EZ_DATA75 | 0x4062052C | FULL | Memory buffer |
| SCB2_EZ_DATA76 | 0x40620530 | FULL | Memory buffer |
| SCB2_EZ_DATA77 | 0x40620534 | FULL | Memory buffer |
| SCB2_EZ_DATA78 | 0x40620538 | FULL | Memory buffer |
| SCB2_EZ_DATA79 | 0x4062053C | FULL | Memory buffer |
| SCB2_EZ_DATA80 | 0x40620540 | FULL | Memory buffer |
| SCB2_EZ_DATA81 | 0x40620544 | FULL | Memory buffer |
| SCB2_EZ_DATA82 | 0x40620548 | FULL | Memory buffer |
| SCB2_EZ_DATA83 | 0x4062054C | FULL | Memory buffer |
| SCB2_EZ_DATA84 | 0x40620550 | FULL | Memory buffer |
| SCB2_EZ_DATA85 | 0x40620554 | FULL | Memory buffer |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SCB2_EZ_DATA86 | 0x40620558 | FULL | Memory buffer |
| SCB2_EZ_DATA87 | 0x4062055C | FULL | Memory buffer |
| SCB2_EZ_DATA88 | 0x40620560 | FULL | Memory buffer |
| SCB2_EZ_DATA89 | 0x40620564 | FULL | Memory buffer |
| SCB2_EZ_DATA90 | 0x40620568 | FULL | Memory buffer |
| SCB2_EZ_DATA91 | 0x4062056C | FULL | Memory buffer |
| SCB2_EZ_DATA92 | 0x40620570 | FULL | Memory buffer |
| SCB2_EZ_DATA93 | 0x40620574 | FULL | Memory buffer |
| SCB2_EZ_DATA94 | 0x40620578 | FULL | Memory buffer |
| SCB2_EZ_DATA95 | 0x4062057C | FULL | Memory buffer |
| SCB2_EZ_DATA96 | 0x40620580 | FULL | Memory buffer |
| SCB2_EZ_DATA97 | 0x40620584 | FULL | Memory buffer |
| SCB2_EZ_DATA98 | 0x40620588 | FULL | Memory buffer |
| SCB2_EZ_DATA99 | 0x4062058C | FULL | Memory buffer |
| SCB2_EZ_DATA100 | 0x40620590 | FULL | Memory buffer |
| SCB2_EZ_DATA101 | 0x40620594 | FULL | Memory buffer |
| SCB2_EZ_DATA102 | 0x40620598 | FULL | Memory buffer |
| SCB2_EZ_DATA103 | 0x4062059C | FULL | Memory buffer |
| SCB2_EZ_DATA104 | 0x406205A0 | FULL | Memory buffer |
| SCB2_EZ_DATA105 | 0x406205A4 | FULL | Memory buffer |
| SCB2_EZ_DATA106 | 0x406205A8 | FULL | Memory buffer |
| SCB2_EZ_DATA107 | 0x406205AC | FULL | Memory buffer |
| SCB2_EZ_DATA108 | 0x406205B0 | FULL | Memory buffer |
| SCB2_EZ_DATA109 | 0x406205B4 | FULL | Memory buffer |
| SCB2_EZ_DATA110 | 0x406205B8 | FULL | Memory buffer |
| SCB2_EZ_DATA111 | 0x406205BC | FULL | Memory buffer |
| SCB2_EZ_DATA112 | 0x406205C0 | FULL | Memory buffer |
| SCB2_EZ_DATA113 | 0x406205C4 | FULL | Memory buffer |
| SCB2_EZ_DATA114 | 0x406205C8 | FULL | Memory buffer |
| SCB2_EZ_DATA115 | 0x406205CC | FULL | Memory buffer |
| SCB2_EZ_DATA116 | 0x406205D0 | FULL | Memory buffer |
| SCB2_EZ_DATA117 | 0x406205D4 | FULL | Memory buffer |
| SCB2_EZ_DATA118 | 0x406205D8 | FULL | Memory buffer |
| SCB2_EZ_DATA119 | 0x406205DC | FULL | Memory buffer |
| SCB2_EZ_DATA120 | 0x406205E0 | FULL | Memory buffer |
| SCB2_EZ_DATA121 | 0x406205E4 | FULL | Memory buffer |
| SCB2_EZ_DATA122 | 0x406205E8 | FULL | Memory buffer |
| SCB2_EZ_DATA123 | 0x406205EC | FULL | Memory buffer |
| SCB2_EZ_DATA124 | 0x406205F0 | FULL | Memory buffer |
| SCB2_EZ_DATA125 | 0x406205F4 | FULL | Memory buffer |
| SCB2_EZ_DATA126 | 0x406205F8 | FULL | Memory buffer |
| SCB2_EZ_DATA127 | 0x406205FC | FULL | Memory buffer |
| SCB2_EZ_DATA128 | 0x40620600 | FULL | Memory buffer |
| SCB2_EZ_DATA129 | 0x40620604 | FULL | Memory buffer |
| SCB2_EZ_DATA130 | 0x40620608 | FULL | Memory buffer |
| SCB2_EZ_DATA131 | 0x4062060C | FULL | Memory buffer |
| SCB2_EZ_DATA132 | 0x40620610 | FULL | Memory buffer |
| SCB2_EZ_DATA133 | 0x40620614 | FULL | Memory buffer |
| SCB2_EZ_DATA134 | 0x40620618 | FULL | Memory buffer |
| SCB2_EZ_DATA135 | 0x4062061C | FULL | Memory buffer |
| SCB2_EZ_DATA136 | 0x40620620 | FULL | Memory buffer |
| SCB2_EZ_DATA137 | 0x40620624 | FULL | Memory buffer |
| SCB2_EZ_DATA138 | 0x40620628 | FULL | Memory buffer |
| SCB2_EZ_DATA139 | 0x4062062C | FULL | Memory buffer |
| SCB2_EZ_DATA140 | 0x40620630 | FULL | Memory buffer |
| SCB2_EZ_DATA141 | 0x40620634 | FULL | Memory buffer |
| SCB2_EZ_DATA142 | 0x40620638 | FULL | Memory buffer |
| SCB2_EZ_DATA143 | 0x4062063C | FULL | Memory buffer |
| SCB2_EZ_DATA144 | 0x40620640 | FULL | Memory buffer |
| SCB2_EZ_DATA145 | 0x40620644 | FULL | Memory buffer |
| SCB2_EZ_DATA146 | 0x40620648 | FULL | Memory buffer |
| SCB2_EZ_DATA147 | 0x4062064C | FULL | Memory buffer |
| SCB2_EZ_DATA148 | 0x40620650 | FULL | Memory buffer |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SCB2_EZ_DATA149 | 0x40620654 | FULL | Memory buffer |
| SCB2_EZ_DATA150 | 0x40620658 | FULL | Memory buffer |
| SCB2_EZ_DATA151 | 0x4062065C | FULL | Memory buffer |
| SCB2_EZ_DATA152 | 0x40620660 | FULL | Memory buffer |
| SCB2_EZ_DATA153 | 0x40620664 | FULL | Memory buffer |
| SCB2_EZ_DATA154 | 0x40620668 | FULL | Memory buffer |
| SCB2_EZ_DATA155 | 0x4062066C | FULL | Memory buffer |
| SCB2_EZ_DATA156 | 0x40620670 | FULL | Memory buffer |
| SCB2_EZ_DATA157 | 0x40620674 | FULL | Memory buffer |
| SCB2_EZ_DATA158 | 0x40620678 | FULL | Memory buffer |
| SCB2_EZ_DATA159 | 0x4062067C | FULL | Memory buffer |
| SCB2_EZ_DATA160 | 0x40620680 | FULL | Memory buffer |
| SCB2_EZ_DATA161 | 0x40620684 | FULL | Memory buffer |
| SCB2_EZ_DATA162 | 0x40620688 | FULL | Memory buffer |
| SCB2_EZ_DATA163 | 0x4062068C | FULL | Memory buffer |
| SCB2_EZ_DATA164 | 0x40620690 | FULL | Memory buffer |
| SCB2_EZ_DATA165 | 0x40620694 | FULL | Memory buffer |
| SCB2_EZ_DATA166 | 0x40620698 | FULL | Memory buffer |
| SCB2_EZ_DATA167 | 0x4062069C | FULL | Memory buffer |
| SCB2_EZ_DATA168 | 0x406206A0 | FULL | Memory buffer |
| SCB2_EZ_DATA169 | 0x406206A4 | FULL | Memory buffer |
| SCB2_EZ_DATA170 | 0x406206A8 | FULL | Memory buffer |
| SCB2_EZ_DATA171 | 0x406206AC | FULL | Memory buffer |
| SCB2_EZ_DATA172 | 0x406206B0 | FULL | Memory buffer |
| SCB2_EZ_DATA173 | 0x406206B4 | FULL | Memory buffer |
| SCB2_EZ_DATA174 | 0x406206B8 | FULL | Memory buffer |
| SCB2_EZ_DATA175 | 0x406206BC | FULL | Memory buffer |
| SCB2_EZ_DATA176 | 0x406206C0 | FULL | Memory buffer |
| SCB2_EZ_DATA177 | 0x406206C4 | FULL | Memory buffer |
| SCB2_EZ_DATA178 | 0x406206C8 | FULL | Memory buffer |
| SCB2_EZ_DATA179 | 0x406206CC | FULL | Memory buffer |
| SCB2_EZ_DATA180 | 0x406206D0 | FULL | Memory buffer |
| SCB2_EZ_DATA181 | 0x406206D4 | FULL | Memory buffer |
| SCB2_EZ_DATA182 | 0x406206D8 | FULL | Memory buffer |
| SCB2_EZ_DATA183 | 0x406206DC | FULL | Memory buffer |
| SCB2_EZ_DATA184 | 0x406206E0 | FULL | Memory buffer |
| SCB2_EZ_DATA185 | 0x406206E4 | FULL | Memory buffer |
| SCB2_EZ_DATA186 | 0x406206E8 | FULL | Memory buffer |
| SCB2_EZ_DATA187 | 0x406206EC | FULL | Memory buffer |
| SCB2_EZ_DATA188 | 0x406206F0 | FULL | Memory buffer |
| SCB2_EZ_DATA189 | 0x406206F4 | FULL | Memory buffer |
| SCB2_EZ_DATA190 | 0x406206F8 | FULL | Memory buffer |
| SCB2_EZ_DATA191 | 0x406206FC | FULL | Memory buffer |
| SCB2_EZ_DATA192 | 0x40620700 | FULL | Memory buffer |
| SCB2_EZ_DATA193 | 0x40620704 | FULL | Memory buffer |
| SCB2_EZ_DATA194 | 0x40620708 | FULL | Memory buffer |
| SCB2_EZ_DATA195 | 0x4062070C | FULL | Memory buffer |
| SCB2_EZ_DATA196 | 0x40620710 | FULL | Memory buffer |
| SCB2_EZ_DATA197 | 0x40620714 | FULL | Memory buffer |
| SCB2_EZ_DATA198 | 0x40620718 | FULL | Memory buffer |
| SCB2_EZ_DATA199 | 0x4062071C | FULL | Memory buffer |
| SCB2_EZ_DATA200 | 0x40620720 | FULL | Memory buffer |
| SCB2_EZ_DATA201 | 0x40620724 | FULL | Memory buffer |
| SCB2_EZ_DATA202 | 0x40620728 | FULL | Memory buffer |
| SCB2_EZ_DATA203 | 0x4062072C | FULL | Memory buffer |
| SCB2_EZ_DATA204 | 0x40620730 | FULL | Memory buffer |
| SCB2_EZ_DATA205 | 0x40620734 | FULL | Memory buffer |
| SCB2_EZ_DATA206 | 0x40620738 | FULL | Memory buffer |
| SCB2_EZ_DATA207 | 0x4062073C | FULL | Memory buffer |
| SCB2_EZ_DATA208 | 0x40620740 | FULL | Memory buffer |
| SCB2_EZ_DATA209 | 0x40620744 | FULL | Memory buffer |
| SCB2_EZ_DATA210 | 0x40620748 | FULL | Memory buffer |
| SCB2_EZ_DATA211 | 0x4062074C | FULL | Memory buffer |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SCB2_EZ_DATA212 | 0x40620750 | FULL | Memory buffer |
| SCB2_EZ_DATA213 | 0x40620754 | FULL | Memory buffer |
| SCB2_EZ_DATA214 | 0x40620758 | FULL | Memory buffer |
| SCB2_EZ_DATA215 | 0x4062075C | FULL | Memory buffer |
| SCB2_EZ_DATA216 | 0x40620760 | FULL | Memory buffer |
| SCB2_EZ_DATA217 | 0x40620764 | FULL | Memory buffer |
| SCB2_EZ_DATA218 | 0x40620768 | FULL | Memory buffer |
| SCB2_EZ_DATA219 | 0x4062076C | FULL | Memory buffer |
| SCB2_EZ_DATA220 | 0x40620770 | FULL | Memory buffer |
| SCB2_EZ_DATA221 | 0x40620774 | FULL | Memory buffer |
| SCB2_EZ_DATA222 | 0x40620778 | FULL | Memory buffer |
| SCB2_EZ_DATA223 | 0x4062077C | FULL | Memory buffer |
| SCB2_EZ_DATA224 | 0x40620780 | FULL | Memory buffer |
| SCB2_EZ_DATA225 | 0x40620784 | FULL | Memory buffer |
| SCB2_EZ_DATA226 | 0x40620788 | FULL | Memory buffer |
| SCB2_EZ_DATA227 | 0x4062078C | FULL | Memory buffer |
| SCB2_EZ_DATA228 | 0x40620790 | FULL | Memory buffer |
| SCB2_EZ_DATA229 | 0x40620794 | FULL | Memory buffer |
| SCB2_EZ_DATA230 | 0x40620798 | FULL | Memory buffer |
| SCB2_EZ_DATA231 | 0x4062079C | FULL | Memory buffer |
| SCB2_EZ_DATA232 | 0x406207A0 | FULL | Memory buffer |
| SCB2_EZ_DATA233 | 0x406207A4 | FULL | Memory buffer |
| SCB2_EZ_DATA234 | 0x406207A8 | FULL | Memory buffer |
| SCB2_EZ_DATA235 | 0x406207AC | FULL | Memory buffer |
| SCB2_EZ_DATA236 | 0x406207B0 | FULL | Memory buffer |
| SCB2_EZ_DATA237 | 0x406207B4 | FULL | Memory buffer |
| SCB2_EZ_DATA238 | 0x406207B8 | FULL | Memory buffer |
| SCB2_EZ_DATA239 | 0x406207BC | FULL | Memory buffer |
| SCB2_EZ_DATA240 | 0x406207C0 | FULL | Memory buffer |
| SCB2_EZ_DATA241 | 0x406207C4 | FULL | Memory buffer |
| SCB2_EZ_DATA242 | 0x406207C8 | FULL | Memory buffer |
| SCB2_EZ_DATA243 | 0x406207CC | FULL | Memory buffer |
| SCB2_EZ_DATA244 | 0x406207D0 | FULL | Memory buffer |
| SCB2_EZ_DATA245 | 0x406207D4 | FULL | Memory buffer |
| SCB2_EZ_DATA246 | 0x406207D8 | FULL | Memory buffer |
| SCB2_EZ_DATA247 | 0x406207DC | FULL | Memory buffer |
| SCB2_EZ_DATA248 | 0x406207E0 | FULL | Memory buffer |
| SCB2_EZ_DATA249 | 0x406207E4 | FULL | Memory buffer |
| SCB2_EZ_DATA250 | 0x406207E8 | FULL | Memory buffer |
| SCB2_EZ_DATA251 | 0x406207EC | FULL | Memory buffer |
| SCB2_EZ_DATA252 | 0x406207F0 | FULL | Memory buffer |
| SCB2_EZ_DATA253 | 0x406207F4 | FULL | Memory buffer |
| SCB2_EZ_DATA254 | 0x406207F8 | FULL | Memory buffer |
| SCB2_EZ_DATA255 | 0x406207FC | FULL | Memory buffer |
| SCB2_INTR_CAUSE | 0x40620E00 | FULL | Active clocked interrupt signal<br>Note:I2C_EC is not available for this register |
| SCB2_INTR_SPI_EC | 0x40620EC0 | FULL | Externally clocked SPI interrupt request |
| SCB2_INTR_SPI_EC_MASK | 0x40620EC8 | FULL | Externally clocked SPI interrupt mask |
| SCB2_INTR_SPI_EC_MASKED | 0x40620ECC | FULL | Externally clocked SPI interrupt masked |
| SCB2_INTR_M | 0x40620F00 | FULL | Master interrupt request |
| SCB2_INTR_M_SET | 0x40620F04 | FULL | Master interrupt set request |
| SCB2_INTR_M_MASK | 0x40620F08 | FULL | Master interrupt mask |
| SCB2_INTR_M_MASKED | 0x40620F0C | FULL | Master interrupt masked request |
| SCB2_INTR_S | 0x40620F40 | FULL | Slave interrupt request |
| SCB2_INTR_S_SET | 0x40620F44 | FULL | Slave interrupt set request |
| SCB2_INTR_S_MASK | 0x40620F48 | FULL | Slave interrupt mask |
| SCB2_INTR_S_MASKED | 0x40620F4C | FULL | Slave interrupt masked request |
| SCB2_INTR_TX | 0x40620F80 | FULL | Transmitter interrupt request |
| SCB2_INTR_TX_SET | 0x40620F84 | FULL | Transmitter interrupt set request |
| SCB2_INTR_TX_MASK | 0x40620F88 | FULL | Transmitter interrupt mask |
| SCB2_INTR_TX_MASKED | 0x40620F8C | FULL | Transmitter interrupt masked request |
| SCB2_INTR_RX | 0x40620FC0 | FULL | Receiver interrupt request |
| SCB2_INTR_RX_SET | 0x40620FC4 | FULL | Receiver interrupt set request |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SCB2_INTR_RX_MASK | 0x40620FC8 | FULL | Receiver interrupt mask |
| SCB2_INTR_RX_MASKED | 0x40620FCC | FULL | Receiver interrupt masked request |

## 26.4 SCB 3

**Description** Serial Communications Block (SPI/UART/I2C)
**Base Address** 0x40630000
**Size** 0x10000
**Slave Num** MMIO6 - 3

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SCB3_CTRL | 0x40630000 | FULL | Generic control<br>Note:CMD_RESP_MODE is not available for this register |
| SCB3_STATUS | 0x40630004 | FULL | Generic status |
| SCB3_SPI_CTRL | 0x40630020 | FULL | SPI control |
| SCB3_SPI_STATUS | 0x40630024 | FULL | SPI status |
| SCB3_SPI_TX_CTRL | 0x40630028 | FULL | SPI transmitter control |
| SCB3_SPI_RX_CTRL | 0x4063002C | FULL | SPI receiver control |
| SCB3_UART_CTRL | 0x40630040 | FULL | UART control |
| SCB3_UART_TX_CTRL | 0x40630044 | FULL | UART transmitter control |
| SCB3_UART_RX_CTRL | 0x40630048 | FULL | UART receiver control |
| SCB3_UART_RX_STATUS | 0x4063004C | FULL | UART receiver status |
| SCB3_UART_FLOW_CTRL | 0x40630050 | FULL | UART flow control |
| SCB3_I2C_CTRL | 0x40630060 | FULL | I2C control |
| SCB3_I2C_STATUS | 0x40630064 | FULL | I2C status<br>Note:I2C_EC_BUSY is not available for this register |
| SCB3_I2C_M_CMD | 0x40630068 | FULL | I2C master command |
| SCB3_I2C_S_CMD | 0x4063006C | FULL | I2C slave command |
| SCB3_I2C_CFG | 0x40630070 | FULL | I2C configuration |
| SCB3_TX_CTRL | 0x40630200 | FULL | Transmitter control |
| SCB3_TX_FIFO_CTRL | 0x40630204 | FULL | Transmitter FIFO control |
| SCB3_TX_FIFO_STATUS | 0x40630208 | FULL | Transmitter FIFO status |
| SCB3_TX_FIFO_WR | 0x40630240 | FULL | Transmitter FIFO write |
| SCB3_RX_CTRL | 0x40630300 | FULL | Receiver control |
| SCB3_RX_FIFO_CTRL | 0x40630304 | FULL | Receiver FIFO control |
| SCB3_RX_FIFO_STATUS | 0x40630308 | FULL | Receiver FIFO status |
| SCB3_RX_MATCH | 0x40630310 | FULL | Slave address and mask |
| SCB3_RX_FIFO_RD | 0x40630340 | FULL | Receiver FIFO read |
| SCB3_RX_FIFO_RD_SILENT | 0x40630344 | FULL | Receiver FIFO read silent |
| SCB3_EZ_DATA0 | 0x40630400 | FULL | Memory buffer |
| SCB3_EZ_DATA1 | 0x40630404 | FULL | Memory buffer |
| SCB3_EZ_DATA2 | 0x40630408 | FULL | Memory buffer |
| SCB3_EZ_DATA3 | 0x4063040C | FULL | Memory buffer |
| SCB3_EZ_DATA4 | 0x40630410 | FULL | Memory buffer |
| SCB3_EZ_DATA5 | 0x40630414 | FULL | Memory buffer |
| SCB3_EZ_DATA6 | 0x40630418 | FULL | Memory buffer |
| SCB3_EZ_DATA7 | 0x4063041C | FULL | Memory buffer |
| SCB3_EZ_DATA8 | 0x40630420 | FULL | Memory buffer |
| SCB3_EZ_DATA9 | 0x40630424 | FULL | Memory buffer |
| SCB3_EZ_DATA10 | 0x40630428 | FULL | Memory buffer |
| SCB3_EZ_DATA11 | 0x4063042C | FULL | Memory buffer |
| SCB3_EZ_DATA12 | 0x40630430 | FULL | Memory buffer |
| SCB3_EZ_DATA13 | 0x40630434 | FULL | Memory buffer |
| SCB3_EZ_DATA14 | 0x40630438 | FULL | Memory buffer |
| SCB3_EZ_DATA15 | 0x4063043C | FULL | Memory buffer |
| SCB3_EZ_DATA16 | 0x40630440 | FULL | Memory buffer |
| SCB3_EZ_DATA17 | 0x40630444 | FULL | Memory buffer |
| SCB3_EZ_DATA18 | 0x40630448 | FULL | Memory buffer |
| SCB3_EZ_DATA19 | 0x4063044C | FULL | Memory buffer |
| SCB3_EZ_DATA20 | 0x40630450 | FULL | Memory buffer |
| SCB3_EZ_DATA21 | 0x40630454 | FULL | Memory buffer |
| SCB3_EZ_DATA22 | 0x40630458 | FULL | Memory buffer |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SCB3_EZ_DATA23 | 0x4063045C | FULL | Memory buffer |
| SCB3_EZ_DATA24 | 0x40630460 | FULL | Memory buffer |
| SCB3_EZ_DATA25 | 0x40630464 | FULL | Memory buffer |
| SCB3_EZ_DATA26 | 0x40630468 | FULL | Memory buffer |
| SCB3_EZ_DATA27 | 0x4063046C | FULL | Memory buffer |
| SCB3_EZ_DATA28 | 0x40630470 | FULL | Memory buffer |
| SCB3_EZ_DATA29 | 0x40630474 | FULL | Memory buffer |
| SCB3_EZ_DATA30 | 0x40630478 | FULL | Memory buffer |
| SCB3_EZ_DATA31 | 0x4063047C | FULL | Memory buffer |
| SCB3_EZ_DATA32 | 0x40630480 | FULL | Memory buffer |
| SCB3_EZ_DATA33 | 0x40630484 | FULL | Memory buffer |
| SCB3_EZ_DATA34 | 0x40630488 | FULL | Memory buffer |
| SCB3_EZ_DATA35 | 0x4063048C | FULL | Memory buffer |
| SCB3_EZ_DATA36 | 0x40630490 | FULL | Memory buffer |
| SCB3_EZ_DATA37 | 0x40630494 | FULL | Memory buffer |
| SCB3_EZ_DATA38 | 0x40630498 | FULL | Memory buffer |
| SCB3_EZ_DATA39 | 0x4063049C | FULL | Memory buffer |
| SCB3_EZ_DATA40 | 0x406304A0 | FULL | Memory buffer |
| SCB3_EZ_DATA41 | 0x406304A4 | FULL | Memory buffer |
| SCB3_EZ_DATA42 | 0x406304A8 | FULL | Memory buffer |
| SCB3_EZ_DATA43 | 0x406304AC | FULL | Memory buffer |
| SCB3_EZ_DATA44 | 0x406304B0 | FULL | Memory buffer |
| SCB3_EZ_DATA45 | 0x406304B4 | FULL | Memory buffer |
| SCB3_EZ_DATA46 | 0x406304B8 | FULL | Memory buffer |
| SCB3_EZ_DATA47 | 0x406304BC | FULL | Memory buffer |
| SCB3_EZ_DATA48 | 0x406304C0 | FULL | Memory buffer |
| SCB3_EZ_DATA49 | 0x406304C4 | FULL | Memory buffer |
| SCB3_EZ_DATA50 | 0x406304C8 | FULL | Memory buffer |
| SCB3_EZ_DATA51 | 0x406304CC | FULL | Memory buffer |
| SCB3_EZ_DATA52 | 0x406304D0 | FULL | Memory buffer |
| SCB3_EZ_DATA53 | 0x406304D4 | FULL | Memory buffer |
| SCB3_EZ_DATA54 | 0x406304D8 | FULL | Memory buffer |
| SCB3_EZ_DATA55 | 0x406304DC | FULL | Memory buffer |
| SCB3_EZ_DATA56 | 0x406304E0 | FULL | Memory buffer |
| SCB3_EZ_DATA57 | 0x406304E4 | FULL | Memory buffer |
| SCB3_EZ_DATA58 | 0x406304E8 | FULL | Memory buffer |
| SCB3_EZ_DATA59 | 0x406304EC | FULL | Memory buffer |
| SCB3_EZ_DATA60 | 0x406304F0 | FULL | Memory buffer |
| SCB3_EZ_DATA61 | 0x406304F4 | FULL | Memory buffer |
| SCB3_EZ_DATA62 | 0x406304F8 | FULL | Memory buffer |
| SCB3_EZ_DATA63 | 0x406304FC | FULL | Memory buffer |
| SCB3_EZ_DATA64 | 0x40630500 | FULL | Memory buffer |
| SCB3_EZ_DATA65 | 0x40630504 | FULL | Memory buffer |
| SCB3_EZ_DATA66 | 0x40630508 | FULL | Memory buffer |
| SCB3_EZ_DATA67 | 0x4063050C | FULL | Memory buffer |
| SCB3_EZ_DATA68 | 0x40630510 | FULL | Memory buffer |
| SCB3_EZ_DATA69 | 0x40630514 | FULL | Memory buffer |
| SCB3_EZ_DATA70 | 0x40630518 | FULL | Memory buffer |
| SCB3_EZ_DATA71 | 0x4063051C | FULL | Memory buffer |
| SCB3_EZ_DATA72 | 0x40630520 | FULL | Memory buffer |
| SCB3_EZ_DATA73 | 0x40630524 | FULL | Memory buffer |
| SCB3_EZ_DATA74 | 0x40630528 | FULL | Memory buffer |
| SCB3_EZ_DATA75 | 0x4063052C | FULL | Memory buffer |
| SCB3_EZ_DATA76 | 0x40630530 | FULL | Memory buffer |
| SCB3_EZ_DATA77 | 0x40630534 | FULL | Memory buffer |
| SCB3_EZ_DATA78 | 0x40630538 | FULL | Memory buffer |
| SCB3_EZ_DATA79 | 0x4063053C | FULL | Memory buffer |
| SCB3_EZ_DATA80 | 0x40630540 | FULL | Memory buffer |
| SCB3_EZ_DATA81 | 0x40630544 | FULL | Memory buffer |
| SCB3_EZ_DATA82 | 0x40630548 | FULL | Memory buffer |
| SCB3_EZ_DATA83 | 0x4063054C | FULL | Memory buffer |
| SCB3_EZ_DATA84 | 0x40630550 | FULL | Memory buffer |
| SCB3_EZ_DATA85 | 0x40630554 | FULL | Memory buffer |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SCB3_EZ_DATA86 | 0x40630558 | FULL | Memory buffer |
| SCB3_EZ_DATA87 | 0x4063055C | FULL | Memory buffer |
| SCB3_EZ_DATA88 | 0x40630560 | FULL | Memory buffer |
| SCB3_EZ_DATA89 | 0x40630564 | FULL | Memory buffer |
| SCB3_EZ_DATA90 | 0x40630568 | FULL | Memory buffer |
| SCB3_EZ_DATA91 | 0x4063056C | FULL | Memory buffer |
| SCB3_EZ_DATA92 | 0x40630570 | FULL | Memory buffer |
| SCB3_EZ_DATA93 | 0x40630574 | FULL | Memory buffer |
| SCB3_EZ_DATA94 | 0x40630578 | FULL | Memory buffer |
| SCB3_EZ_DATA95 | 0x4063057C | FULL | Memory buffer |
| SCB3_EZ_DATA96 | 0x40630580 | FULL | Memory buffer |
| SCB3_EZ_DATA97 | 0x40630584 | FULL | Memory buffer |
| SCB3_EZ_DATA98 | 0x40630588 | FULL | Memory buffer |
| SCB3_EZ_DATA99 | 0x4063058C | FULL | Memory buffer |
| SCB3_EZ_DATA100 | 0x40630590 | FULL | Memory buffer |
| SCB3_EZ_DATA101 | 0x40630594 | FULL | Memory buffer |
| SCB3_EZ_DATA102 | 0x40630598 | FULL | Memory buffer |
| SCB3_EZ_DATA103 | 0x4063059C | FULL | Memory buffer |
| SCB3_EZ_DATA104 | 0x406305A0 | FULL | Memory buffer |
| SCB3_EZ_DATA105 | 0x406305A4 | FULL | Memory buffer |
| SCB3_EZ_DATA106 | 0x406305A8 | FULL | Memory buffer |
| SCB3_EZ_DATA107 | 0x406305AC | FULL | Memory buffer |
| SCB3_EZ_DATA108 | 0x406305B0 | FULL | Memory buffer |
| SCB3_EZ_DATA109 | 0x406305B4 | FULL | Memory buffer |
| SCB3_EZ_DATA110 | 0x406305B8 | FULL | Memory buffer |
| SCB3_EZ_DATA111 | 0x406305BC | FULL | Memory buffer |
| SCB3_EZ_DATA112 | 0x406305C0 | FULL | Memory buffer |
| SCB3_EZ_DATA113 | 0x406305C4 | FULL | Memory buffer |
| SCB3_EZ_DATA114 | 0x406305C8 | FULL | Memory buffer |
| SCB3_EZ_DATA115 | 0x406305CC | FULL | Memory buffer |
| SCB3_EZ_DATA116 | 0x406305D0 | FULL | Memory buffer |
| SCB3_EZ_DATA117 | 0x406305D4 | FULL | Memory buffer |
| SCB3_EZ_DATA118 | 0x406305D8 | FULL | Memory buffer |
| SCB3_EZ_DATA119 | 0x406305DC | FULL | Memory buffer |
| SCB3_EZ_DATA120 | 0x406305E0 | FULL | Memory buffer |
| SCB3_EZ_DATA121 | 0x406305E4 | FULL | Memory buffer |
| SCB3_EZ_DATA122 | 0x406305E8 | FULL | Memory buffer |
| SCB3_EZ_DATA123 | 0x406305EC | FULL | Memory buffer |
| SCB3_EZ_DATA124 | 0x406305F0 | FULL | Memory buffer |
| SCB3_EZ_DATA125 | 0x406305F4 | FULL | Memory buffer |
| SCB3_EZ_DATA126 | 0x406305F8 | FULL | Memory buffer |
| SCB3_EZ_DATA127 | 0x406305FC | FULL | Memory buffer |
| SCB3_EZ_DATA128 | 0x40630600 | FULL | Memory buffer |
| SCB3_EZ_DATA129 | 0x40630604 | FULL | Memory buffer |
| SCB3_EZ_DATA130 | 0x40630608 | FULL | Memory buffer |
| SCB3_EZ_DATA131 | 0x4063060C | FULL | Memory buffer |
| SCB3_EZ_DATA132 | 0x40630610 | FULL | Memory buffer |
| SCB3_EZ_DATA133 | 0x40630614 | FULL | Memory buffer |
| SCB3_EZ_DATA134 | 0x40630618 | FULL | Memory buffer |
| SCB3_EZ_DATA135 | 0x4063061C | FULL | Memory buffer |
| SCB3_EZ_DATA136 | 0x40630620 | FULL | Memory buffer |
| SCB3_EZ_DATA137 | 0x40630624 | FULL | Memory buffer |
| SCB3_EZ_DATA138 | 0x40630628 | FULL | Memory buffer |
| SCB3_EZ_DATA139 | 0x4063062C | FULL | Memory buffer |
| SCB3_EZ_DATA140 | 0x40630630 | FULL | Memory buffer |
| SCB3_EZ_DATA141 | 0x40630634 | FULL | Memory buffer |
| SCB3_EZ_DATA142 | 0x40630638 | FULL | Memory buffer |
| SCB3_EZ_DATA143 | 0x4063063C | FULL | Memory buffer |
| SCB3_EZ_DATA144 | 0x40630640 | FULL | Memory buffer |
| SCB3_EZ_DATA145 | 0x40630644 | FULL | Memory buffer |
| SCB3_EZ_DATA146 | 0x40630648 | FULL | Memory buffer |
| SCB3_EZ_DATA147 | 0x4063064C | FULL | Memory buffer |
| SCB3_EZ_DATA148 | 0x40630650 | FULL | Memory buffer |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SCB3_EZ_DATA149 | 0x40630654 | FULL | Memory buffer |
| SCB3_EZ_DATA150 | 0x40630658 | FULL | Memory buffer |
| SCB3_EZ_DATA151 | 0x4063065C | FULL | Memory buffer |
| SCB3_EZ_DATA152 | 0x40630660 | FULL | Memory buffer |
| SCB3_EZ_DATA153 | 0x40630664 | FULL | Memory buffer |
| SCB3_EZ_DATA154 | 0x40630668 | FULL | Memory buffer |
| SCB3_EZ_DATA155 | 0x4063066C | FULL | Memory buffer |
| SCB3_EZ_DATA156 | 0x40630670 | FULL | Memory buffer |
| SCB3_EZ_DATA157 | 0x40630674 | FULL | Memory buffer |
| SCB3_EZ_DATA158 | 0x40630678 | FULL | Memory buffer |
| SCB3_EZ_DATA159 | 0x4063067C | FULL | Memory buffer |
| SCB3_EZ_DATA160 | 0x40630680 | FULL | Memory buffer |
| SCB3_EZ_DATA161 | 0x40630684 | FULL | Memory buffer |
| SCB3_EZ_DATA162 | 0x40630688 | FULL | Memory buffer |
| SCB3_EZ_DATA163 | 0x4063068C | FULL | Memory buffer |
| SCB3_EZ_DATA164 | 0x40630690 | FULL | Memory buffer |
| SCB3_EZ_DATA165 | 0x40630694 | FULL | Memory buffer |
| SCB3_EZ_DATA166 | 0x40630698 | FULL | Memory buffer |
| SCB3_EZ_DATA167 | 0x4063069C | FULL | Memory buffer |
| SCB3_EZ_DATA168 | 0x406306A0 | FULL | Memory buffer |
| SCB3_EZ_DATA169 | 0x406306A4 | FULL | Memory buffer |
| SCB3_EZ_DATA170 | 0x406306A8 | FULL | Memory buffer |
| SCB3_EZ_DATA171 | 0x406306AC | FULL | Memory buffer |
| SCB3_EZ_DATA172 | 0x406306B0 | FULL | Memory buffer |
| SCB3_EZ_DATA173 | 0x406306B4 | FULL | Memory buffer |
| SCB3_EZ_DATA174 | 0x406306B8 | FULL | Memory buffer |
| SCB3_EZ_DATA175 | 0x406306BC | FULL | Memory buffer |
| SCB3_EZ_DATA176 | 0x406306C0 | FULL | Memory buffer |
| SCB3_EZ_DATA177 | 0x406306C4 | FULL | Memory buffer |
| SCB3_EZ_DATA178 | 0x406306C8 | FULL | Memory buffer |
| SCB3_EZ_DATA179 | 0x406306CC | FULL | Memory buffer |
| SCB3_EZ_DATA180 | 0x406306D0 | FULL | Memory buffer |
| SCB3_EZ_DATA181 | 0x406306D4 | FULL | Memory buffer |
| SCB3_EZ_DATA182 | 0x406306D8 | FULL | Memory buffer |
| SCB3_EZ_DATA183 | 0x406306DC | FULL | Memory buffer |
| SCB3_EZ_DATA184 | 0x406306E0 | FULL | Memory buffer |
| SCB3_EZ_DATA185 | 0x406306E4 | FULL | Memory buffer |
| SCB3_EZ_DATA186 | 0x406306E8 | FULL | Memory buffer |
| SCB3_EZ_DATA187 | 0x406306EC | FULL | Memory buffer |
| SCB3_EZ_DATA188 | 0x406306F0 | FULL | Memory buffer |
| SCB3_EZ_DATA189 | 0x406306F4 | FULL | Memory buffer |
| SCB3_EZ_DATA190 | 0x406306F8 | FULL | Memory buffer |
| SCB3_EZ_DATA191 | 0x406306FC | FULL | Memory buffer |
| SCB3_EZ_DATA192 | 0x40630700 | FULL | Memory buffer |
| SCB3_EZ_DATA193 | 0x40630704 | FULL | Memory buffer |
| SCB3_EZ_DATA194 | 0x40630708 | FULL | Memory buffer |
| SCB3_EZ_DATA195 | 0x4063070C | FULL | Memory buffer |
| SCB3_EZ_DATA196 | 0x40630710 | FULL | Memory buffer |
| SCB3_EZ_DATA197 | 0x40630714 | FULL | Memory buffer |
| SCB3_EZ_DATA198 | 0x40630718 | FULL | Memory buffer |
| SCB3_EZ_DATA199 | 0x4063071C | FULL | Memory buffer |
| SCB3_EZ_DATA200 | 0x40630720 | FULL | Memory buffer |
| SCB3_EZ_DATA201 | 0x40630724 | FULL | Memory buffer |
| SCB3_EZ_DATA202 | 0x40630728 | FULL | Memory buffer |
| SCB3_EZ_DATA203 | 0x4063072C | FULL | Memory buffer |
| SCB3_EZ_DATA204 | 0x40630730 | FULL | Memory buffer |
| SCB3_EZ_DATA205 | 0x40630734 | FULL | Memory buffer |
| SCB3_EZ_DATA206 | 0x40630738 | FULL | Memory buffer |
| SCB3_EZ_DATA207 | 0x4063073C | FULL | Memory buffer |
| SCB3_EZ_DATA208 | 0x40630740 | FULL | Memory buffer |
| SCB3_EZ_DATA209 | 0x40630744 | FULL | Memory buffer |
| SCB3_EZ_DATA210 | 0x40630748 | FULL | Memory buffer |
| SCB3_EZ_DATA211 | 0x4063074C | FULL | Memory buffer |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SCB3_EZ_DATA212 | 0x40630750 | FULL | Memory buffer |
| SCB3_EZ_DATA213 | 0x40630754 | FULL | Memory buffer |
| SCB3_EZ_DATA214 | 0x40630758 | FULL | Memory buffer |
| SCB3_EZ_DATA215 | 0x4063075C | FULL | Memory buffer |
| SCB3_EZ_DATA216 | 0x40630760 | FULL | Memory buffer |
| SCB3_EZ_DATA217 | 0x40630764 | FULL | Memory buffer |
| SCB3_EZ_DATA218 | 0x40630768 | FULL | Memory buffer |
| SCB3_EZ_DATA219 | 0x4063076C | FULL | Memory buffer |
| SCB3_EZ_DATA220 | 0x40630770 | FULL | Memory buffer |
| SCB3_EZ_DATA221 | 0x40630774 | FULL | Memory buffer |
| SCB3_EZ_DATA222 | 0x40630778 | FULL | Memory buffer |
| SCB3_EZ_DATA223 | 0x4063077C | FULL | Memory buffer |
| SCB3_EZ_DATA224 | 0x40630780 | FULL | Memory buffer |
| SCB3_EZ_DATA225 | 0x40630784 | FULL | Memory buffer |
| SCB3_EZ_DATA226 | 0x40630788 | FULL | Memory buffer |
| SCB3_EZ_DATA227 | 0x4063078C | FULL | Memory buffer |
| SCB3_EZ_DATA228 | 0x40630790 | FULL | Memory buffer |
| SCB3_EZ_DATA229 | 0x40630794 | FULL | Memory buffer |
| SCB3_EZ_DATA230 | 0x40630798 | FULL | Memory buffer |
| SCB3_EZ_DATA231 | 0x4063079C | FULL | Memory buffer |
| SCB3_EZ_DATA232 | 0x406307A0 | FULL | Memory buffer |
| SCB3_EZ_DATA233 | 0x406307A4 | FULL | Memory buffer |
| SCB3_EZ_DATA234 | 0x406307A8 | FULL | Memory buffer |
| SCB3_EZ_DATA235 | 0x406307AC | FULL | Memory buffer |
| SCB3_EZ_DATA236 | 0x406307B0 | FULL | Memory buffer |
| SCB3_EZ_DATA237 | 0x406307B4 | FULL | Memory buffer |
| SCB3_EZ_DATA238 | 0x406307B8 | FULL | Memory buffer |
| SCB3_EZ_DATA239 | 0x406307BC | FULL | Memory buffer |
| SCB3_EZ_DATA240 | 0x406307C0 | FULL | Memory buffer |
| SCB3_EZ_DATA241 | 0x406307C4 | FULL | Memory buffer |
| SCB3_EZ_DATA242 | 0x406307C8 | FULL | Memory buffer |
| SCB3_EZ_DATA243 | 0x406307CC | FULL | Memory buffer |
| SCB3_EZ_DATA244 | 0x406307D0 | FULL | Memory buffer |
| SCB3_EZ_DATA245 | 0x406307D4 | FULL | Memory buffer |
| SCB3_EZ_DATA246 | 0x406307D8 | FULL | Memory buffer |
| SCB3_EZ_DATA247 | 0x406307DC | FULL | Memory buffer |
| SCB3_EZ_DATA248 | 0x406307E0 | FULL | Memory buffer |
| SCB3_EZ_DATA249 | 0x406307E4 | FULL | Memory buffer |
| SCB3_EZ_DATA250 | 0x406307E8 | FULL | Memory buffer |
| SCB3_EZ_DATA251 | 0x406307EC | FULL | Memory buffer |
| SCB3_EZ_DATA252 | 0x406307F0 | FULL | Memory buffer |
| SCB3_EZ_DATA253 | 0x406307F4 | FULL | Memory buffer |
| SCB3_EZ_DATA254 | 0x406307F8 | FULL | Memory buffer |
| SCB3_EZ_DATA255 | 0x406307FC | FULL | Memory buffer |
| SCB3_INTR_CAUSE | 0x40630E00 | FULL | Active clocked interrupt signal<br>Note:I2C_EC is not available for this register |
| SCB3_INTR_SPI_EC | 0x40630EC0 | FULL | Externally clocked SPI interrupt request |
| SCB3_INTR_SPI_EC_MASK | 0x40630EC8 | FULL | Externally clocked SPI interrupt mask |
| SCB3_INTR_SPI_EC_MASKED | 0x40630ECC | FULL | Externally clocked SPI interrupt masked |
| SCB3_INTR_M | 0x40630F00 | FULL | Master interrupt request |
| SCB3_INTR_M_SET | 0x40630F04 | FULL | Master interrupt set request |
| SCB3_INTR_M_MASK | 0x40630F08 | FULL | Master interrupt mask |
| SCB3_INTR_M_MASKED | 0x40630F0C | FULL | Master interrupt masked request |
| SCB3_INTR_S | 0x40630F40 | FULL | Slave interrupt request |
| SCB3_INTR_S_SET | 0x40630F44 | FULL | Slave interrupt set request |
| SCB3_INTR_S_MASK | 0x40630F48 | FULL | Slave interrupt mask |
| SCB3_INTR_S_MASKED | 0x40630F4C | FULL | Slave interrupt masked request |
| SCB3_INTR_TX | 0x40630F80 | FULL | Transmitter interrupt request |
| SCB3_INTR_TX_SET | 0x40630F84 | FULL | Transmitter interrupt set request |
| SCB3_INTR_TX_MASK | 0x40630F88 | FULL | Transmitter interrupt mask |
| SCB3_INTR_TX_MASKED | 0x40630F8C | FULL | Transmitter interrupt masked request |
| SCB3_INTR_RX | 0x40630FC0 | FULL | Receiver interrupt request |
| SCB3_INTR_RX_SET | 0x40630FC4 | FULL | Receiver interrupt set request |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SCB3_INTR_RX_MASK | 0x40630FC8 | FULL | Receiver interrupt mask |
| SCB3_INTR_RX_MASKED | 0x40630FCC | FULL | Receiver interrupt masked request |

## 26.5 SCB 4

**Description** Serial Communications Block (SPI/UART/I2C)
**Base Address** 0x40640000
**Size** 0x10000
**Slave Num** MMIO6 - 4

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SCB4_CTRL | 0x40640000 | FULL | Generic control<br>Note:CMD_RESP_MODE is not available for this register |
| SCB4_STATUS | 0x40640004 | FULL | Generic status |
| SCB4_SPI_CTRL | 0x40640020 | FULL | SPI control |
| SCB4_SPI_STATUS | 0x40640024 | FULL | SPI status |
| SCB4_SPI_TX_CTRL | 0x40640028 | FULL | SPI transmitter control |
| SCB4_SPI_RX_CTRL | 0x4064002C | FULL | SPI receiver control |
| SCB4_UART_CTRL | 0x40640040 | FULL | UART control |
| SCB4_UART_TX_CTRL | 0x40640044 | FULL | UART transmitter control |
| SCB4_UART_RX_CTRL | 0x40640048 | FULL | UART receiver control |
| SCB4_UART_RX_STATUS | 0x4064004C | FULL | UART receiver status |
| SCB4_UART_FLOW_CTRL | 0x40640050 | FULL | UART flow control |
| SCB4_I2C_CTRL | 0x40640060 | FULL | I2C control |
| SCB4_I2C_STATUS | 0x40640064 | FULL | I2C status<br>Note:I2C_EC_BUSY is not available for this register |
| SCB4_I2C_M_CMD | 0x40640068 | FULL | I2C master command |
| SCB4_I2C_S_CMD | 0x4064006C | FULL | I2C slave command |
| SCB4_I2C_CFG | 0x40640070 | FULL | I2C configuration |
| SCB4_TX_CTRL | 0x40640200 | FULL | Transmitter control |
| SCB4_TX_FIFO_CTRL | 0x40640204 | FULL | Transmitter FIFO control |
| SCB4_TX_FIFO_STATUS | 0x40640208 | FULL | Transmitter FIFO status |
| SCB4_TX_FIFO_WR | 0x40640240 | FULL | Transmitter FIFO write |
| SCB4_RX_CTRL | 0x40640300 | FULL | Receiver control |
| SCB4_RX_FIFO_CTRL | 0x40640304 | FULL | Receiver FIFO control |
| SCB4_RX_FIFO_STATUS | 0x40640308 | FULL | Receiver FIFO status |
| SCB4_RX_MATCH | 0x40640310 | FULL | Slave address and mask |
| SCB4_RX_FIFO_RD | 0x40640340 | FULL | Receiver FIFO read |
| SCB4_RX_FIFO_RD_SILENT | 0x40640344 | FULL | Receiver FIFO read silent |
| SCB4_EZ_DATA0 | 0x40640400 | FULL | Memory buffer |
| SCB4_EZ_DATA1 | 0x40640404 | FULL | Memory buffer |
| SCB4_EZ_DATA2 | 0x40640408 | FULL | Memory buffer |
| SCB4_EZ_DATA3 | 0x4064040C | FULL | Memory buffer |
| SCB4_EZ_DATA4 | 0x40640410 | FULL | Memory buffer |
| SCB4_EZ_DATA5 | 0x40640414 | FULL | Memory buffer |
| SCB4_EZ_DATA6 | 0x40640418 | FULL | Memory buffer |
| SCB4_EZ_DATA7 | 0x4064041C | FULL | Memory buffer |
| SCB4_EZ_DATA8 | 0x40640420 | FULL | Memory buffer |
| SCB4_EZ_DATA9 | 0x40640424 | FULL | Memory buffer |
| SCB4_EZ_DATA10 | 0x40640428 | FULL | Memory buffer |
| SCB4_EZ_DATA11 | 0x4064042C | FULL | Memory buffer |
| SCB4_EZ_DATA12 | 0x40640430 | FULL | Memory buffer |
| SCB4_EZ_DATA13 | 0x40640434 | FULL | Memory buffer |
| SCB4_EZ_DATA14 | 0x40640438 | FULL | Memory buffer |
| SCB4_EZ_DATA15 | 0x4064043C | FULL | Memory buffer |
| SCB4_EZ_DATA16 | 0x40640440 | FULL | Memory buffer |
| SCB4_EZ_DATA17 | 0x40640444 | FULL | Memory buffer |
| SCB4_EZ_DATA18 | 0x40640448 | FULL | Memory buffer |
| SCB4_EZ_DATA19 | 0x4064044C | FULL | Memory buffer |
| SCB4_EZ_DATA20 | 0x40640450 | FULL | Memory buffer |
| SCB4_EZ_DATA21 | 0x40640454 | FULL | Memory buffer |
| SCB4_EZ_DATA22 | 0x40640458 | FULL | Memory buffer |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SCB4_EZ_DATA23 | 0x4064045C | FULL | Memory buffer |
| SCB4_EZ_DATA24 | 0x40640460 | FULL | Memory buffer |
| SCB4_EZ_DATA25 | 0x40640464 | FULL | Memory buffer |
| SCB4_EZ_DATA26 | 0x40640468 | FULL | Memory buffer |
| SCB4_EZ_DATA27 | 0x4064046C | FULL | Memory buffer |
| SCB4_EZ_DATA28 | 0x40640470 | FULL | Memory buffer |
| SCB4_EZ_DATA29 | 0x40640474 | FULL | Memory buffer |
| SCB4_EZ_DATA30 | 0x40640478 | FULL | Memory buffer |
| SCB4_EZ_DATA31 | 0x4064047C | FULL | Memory buffer |
| SCB4_EZ_DATA32 | 0x40640480 | FULL | Memory buffer |
| SCB4_EZ_DATA33 | 0x40640484 | FULL | Memory buffer |
| SCB4_EZ_DATA34 | 0x40640488 | FULL | Memory buffer |
| SCB4_EZ_DATA35 | 0x4064048C | FULL | Memory buffer |
| SCB4_EZ_DATA36 | 0x40640490 | FULL | Memory buffer |
| SCB4_EZ_DATA37 | 0x40640494 | FULL | Memory buffer |
| SCB4_EZ_DATA38 | 0x40640498 | FULL | Memory buffer |
| SCB4_EZ_DATA39 | 0x4064049C | FULL | Memory buffer |
| SCB4_EZ_DATA40 | 0x406404A0 | FULL | Memory buffer |
| SCB4_EZ_DATA41 | 0x406404A4 | FULL | Memory buffer |
| SCB4_EZ_DATA42 | 0x406404A8 | FULL | Memory buffer |
| SCB4_EZ_DATA43 | 0x406404AC | FULL | Memory buffer |
| SCB4_EZ_DATA44 | 0x406404B0 | FULL | Memory buffer |
| SCB4_EZ_DATA45 | 0x406404B4 | FULL | Memory buffer |
| SCB4_EZ_DATA46 | 0x406404B8 | FULL | Memory buffer |
| SCB4_EZ_DATA47 | 0x406404BC | FULL | Memory buffer |
| SCB4_EZ_DATA48 | 0x406404C0 | FULL | Memory buffer |
| SCB4_EZ_DATA49 | 0x406404C4 | FULL | Memory buffer |
| SCB4_EZ_DATA50 | 0x406404C8 | FULL | Memory buffer |
| SCB4_EZ_DATA51 | 0x406404CC | FULL | Memory buffer |
| SCB4_EZ_DATA52 | 0x406404D0 | FULL | Memory buffer |
| SCB4_EZ_DATA53 | 0x406404D4 | FULL | Memory buffer |
| SCB4_EZ_DATA54 | 0x406404D8 | FULL | Memory buffer |
| SCB4_EZ_DATA55 | 0x406404DC | FULL | Memory buffer |
| SCB4_EZ_DATA56 | 0x406404E0 | FULL | Memory buffer |
| SCB4_EZ_DATA57 | 0x406404E4 | FULL | Memory buffer |
| SCB4_EZ_DATA58 | 0x406404E8 | FULL | Memory buffer |
| SCB4_EZ_DATA59 | 0x406404EC | FULL | Memory buffer |
| SCB4_EZ_DATA60 | 0x406404F0 | FULL | Memory buffer |
| SCB4_EZ_DATA61 | 0x406404F4 | FULL | Memory buffer |
| SCB4_EZ_DATA62 | 0x406404F8 | FULL | Memory buffer |
| SCB4_EZ_DATA63 | 0x406404FC | FULL | Memory buffer |
| SCB4_EZ_DATA64 | 0x40640500 | FULL | Memory buffer |
| SCB4_EZ_DATA65 | 0x40640504 | FULL | Memory buffer |
| SCB4_EZ_DATA66 | 0x40640508 | FULL | Memory buffer |
| SCB4_EZ_DATA67 | 0x4064050C | FULL | Memory buffer |
| SCB4_EZ_DATA68 | 0x40640510 | FULL | Memory buffer |
| SCB4_EZ_DATA69 | 0x40640514 | FULL | Memory buffer |
| SCB4_EZ_DATA70 | 0x40640518 | FULL | Memory buffer |
| SCB4_EZ_DATA71 | 0x4064051C | FULL | Memory buffer |
| SCB4_EZ_DATA72 | 0x40640520 | FULL | Memory buffer |
| SCB4_EZ_DATA73 | 0x40640524 | FULL | Memory buffer |
| SCB4_EZ_DATA74 | 0x40640528 | FULL | Memory buffer |
| SCB4_EZ_DATA75 | 0x4064052C | FULL | Memory buffer |
| SCB4_EZ_DATA76 | 0x40640530 | FULL | Memory buffer |
| SCB4_EZ_DATA77 | 0x40640534 | FULL | Memory buffer |
| SCB4_EZ_DATA78 | 0x40640538 | FULL | Memory buffer |
| SCB4_EZ_DATA79 | 0x4064053C | FULL | Memory buffer |
| SCB4_EZ_DATA80 | 0x40640540 | FULL | Memory buffer |
| SCB4_EZ_DATA81 | 0x40640544 | FULL | Memory buffer |
| SCB4_EZ_DATA82 | 0x40640548 | FULL | Memory buffer |
| SCB4_EZ_DATA83 | 0x4064054C | FULL | Memory buffer |
| SCB4_EZ_DATA84 | 0x40640550 | FULL | Memory buffer |
| SCB4_EZ_DATA85 | 0x40640554 | FULL | Memory buffer |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SCB4_EZ_DATA86 | 0x40640558 | FULL | Memory buffer |
| SCB4_EZ_DATA87 | 0x4064055C | FULL | Memory buffer |
| SCB4_EZ_DATA88 | 0x40640560 | FULL | Memory buffer |
| SCB4_EZ_DATA89 | 0x40640564 | FULL | Memory buffer |
| SCB4_EZ_DATA90 | 0x40640568 | FULL | Memory buffer |
| SCB4_EZ_DATA91 | 0x4064056C | FULL | Memory buffer |
| SCB4_EZ_DATA92 | 0x40640570 | FULL | Memory buffer |
| SCB4_EZ_DATA93 | 0x40640574 | FULL | Memory buffer |
| SCB4_EZ_DATA94 | 0x40640578 | FULL | Memory buffer |
| SCB4_EZ_DATA95 | 0x4064057C | FULL | Memory buffer |
| SCB4_EZ_DATA96 | 0x40640580 | FULL | Memory buffer |
| SCB4_EZ_DATA97 | 0x40640584 | FULL | Memory buffer |
| SCB4_EZ_DATA98 | 0x40640588 | FULL | Memory buffer |
| SCB4_EZ_DATA99 | 0x4064058C | FULL | Memory buffer |
| SCB4_EZ_DATA100 | 0x40640590 | FULL | Memory buffer |
| SCB4_EZ_DATA101 | 0x40640594 | FULL | Memory buffer |
| SCB4_EZ_DATA102 | 0x40640598 | FULL | Memory buffer |
| SCB4_EZ_DATA103 | 0x4064059C | FULL | Memory buffer |
| SCB4_EZ_DATA104 | 0x406405A0 | FULL | Memory buffer |
| SCB4_EZ_DATA105 | 0x406405A4 | FULL | Memory buffer |
| SCB4_EZ_DATA106 | 0x406405A8 | FULL | Memory buffer |
| SCB4_EZ_DATA107 | 0x406405AC | FULL | Memory buffer |
| SCB4_EZ_DATA108 | 0x406405B0 | FULL | Memory buffer |
| SCB4_EZ_DATA109 | 0x406405B4 | FULL | Memory buffer |
| SCB4_EZ_DATA110 | 0x406405B8 | FULL | Memory buffer |
| SCB4_EZ_DATA111 | 0x406405BC | FULL | Memory buffer |
| SCB4_EZ_DATA112 | 0x406405C0 | FULL | Memory buffer |
| SCB4_EZ_DATA113 | 0x406405C4 | FULL | Memory buffer |
| SCB4_EZ_DATA114 | 0x406405C8 | FULL | Memory buffer |
| SCB4_EZ_DATA115 | 0x406405CC | FULL | Memory buffer |
| SCB4_EZ_DATA116 | 0x406405D0 | FULL | Memory buffer |
| SCB4_EZ_DATA117 | 0x406405D4 | FULL | Memory buffer |
| SCB4_EZ_DATA118 | 0x406405D8 | FULL | Memory buffer |
| SCB4_EZ_DATA119 | 0x406405DC | FULL | Memory buffer |
| SCB4_EZ_DATA120 | 0x406405E0 | FULL | Memory buffer |
| SCB4_EZ_DATA121 | 0x406405E4 | FULL | Memory buffer |
| SCB4_EZ_DATA122 | 0x406405E8 | FULL | Memory buffer |
| SCB4_EZ_DATA123 | 0x406405EC | FULL | Memory buffer |
| SCB4_EZ_DATA124 | 0x406405F0 | FULL | Memory buffer |
| SCB4_EZ_DATA125 | 0x406405F4 | FULL | Memory buffer |
| SCB4_EZ_DATA126 | 0x406405F8 | FULL | Memory buffer |
| SCB4_EZ_DATA127 | 0x406405FC | FULL | Memory buffer |
| SCB4_EZ_DATA128 | 0x40640600 | FULL | Memory buffer |
| SCB4_EZ_DATA129 | 0x40640604 | FULL | Memory buffer |
| SCB4_EZ_DATA130 | 0x40640608 | FULL | Memory buffer |
| SCB4_EZ_DATA131 | 0x4064060C | FULL | Memory buffer |
| SCB4_EZ_DATA132 | 0x40640610 | FULL | Memory buffer |
| SCB4_EZ_DATA133 | 0x40640614 | FULL | Memory buffer |
| SCB4_EZ_DATA134 | 0x40640618 | FULL | Memory buffer |
| SCB4_EZ_DATA135 | 0x4064061C | FULL | Memory buffer |
| SCB4_EZ_DATA136 | 0x40640620 | FULL | Memory buffer |
| SCB4_EZ_DATA137 | 0x40640624 | FULL | Memory buffer |
| SCB4_EZ_DATA138 | 0x40640628 | FULL | Memory buffer |
| SCB4_EZ_DATA139 | 0x4064062C | FULL | Memory buffer |
| SCB4_EZ_DATA140 | 0x40640630 | FULL | Memory buffer |
| SCB4_EZ_DATA141 | 0x40640634 | FULL | Memory buffer |
| SCB4_EZ_DATA142 | 0x40640638 | FULL | Memory buffer |
| SCB4_EZ_DATA143 | 0x4064063C | FULL | Memory buffer |
| SCB4_EZ_DATA144 | 0x40640640 | FULL | Memory buffer |
| SCB4_EZ_DATA145 | 0x40640644 | FULL | Memory buffer |
| SCB4_EZ_DATA146 | 0x40640648 | FULL | Memory buffer |
| SCB4_EZ_DATA147 | 0x4064064C | FULL | Memory buffer |
| SCB4_EZ_DATA148 | 0x40640650 | FULL | Memory buffer |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SCB4_EZ_DATA149 | 0x40640654 | FULL | Memory buffer |
| SCB4_EZ_DATA150 | 0x40640658 | FULL | Memory buffer |
| SCB4_EZ_DATA151 | 0x4064065C | FULL | Memory buffer |
| SCB4_EZ_DATA152 | 0x40640660 | FULL | Memory buffer |
| SCB4_EZ_DATA153 | 0x40640664 | FULL | Memory buffer |
| SCB4_EZ_DATA154 | 0x40640668 | FULL | Memory buffer |
| SCB4_EZ_DATA155 | 0x4064066C | FULL | Memory buffer |
| SCB4_EZ_DATA156 | 0x40640670 | FULL | Memory buffer |
| SCB4_EZ_DATA157 | 0x40640674 | FULL | Memory buffer |
| SCB4_EZ_DATA158 | 0x40640678 | FULL | Memory buffer |
| SCB4_EZ_DATA159 | 0x4064067C | FULL | Memory buffer |
| SCB4_EZ_DATA160 | 0x40640680 | FULL | Memory buffer |
| SCB4_EZ_DATA161 | 0x40640684 | FULL | Memory buffer |
| SCB4_EZ_DATA162 | 0x40640688 | FULL | Memory buffer |
| SCB4_EZ_DATA163 | 0x4064068C | FULL | Memory buffer |
| SCB4_EZ_DATA164 | 0x40640690 | FULL | Memory buffer |
| SCB4_EZ_DATA165 | 0x40640694 | FULL | Memory buffer |
| SCB4_EZ_DATA166 | 0x40640698 | FULL | Memory buffer |
| SCB4_EZ_DATA167 | 0x4064069C | FULL | Memory buffer |
| SCB4_EZ_DATA168 | 0x406406A0 | FULL | Memory buffer |
| SCB4_EZ_DATA169 | 0x406406A4 | FULL | Memory buffer |
| SCB4_EZ_DATA170 | 0x406406A8 | FULL | Memory buffer |
| SCB4_EZ_DATA171 | 0x406406AC | FULL | Memory buffer |
| SCB4_EZ_DATA172 | 0x406406B0 | FULL | Memory buffer |
| SCB4_EZ_DATA173 | 0x406406B4 | FULL | Memory buffer |
| SCB4_EZ_DATA174 | 0x406406B8 | FULL | Memory buffer |
| SCB4_EZ_DATA175 | 0x406406BC | FULL | Memory buffer |
| SCB4_EZ_DATA176 | 0x406406C0 | FULL | Memory buffer |
| SCB4_EZ_DATA177 | 0x406406C4 | FULL | Memory buffer |
| SCB4_EZ_DATA178 | 0x406406C8 | FULL | Memory buffer |
| SCB4_EZ_DATA179 | 0x406406CC | FULL | Memory buffer |
| SCB4_EZ_DATA180 | 0x406406D0 | FULL | Memory buffer |
| SCB4_EZ_DATA181 | 0x406406D4 | FULL | Memory buffer |
| SCB4_EZ_DATA182 | 0x406406D8 | FULL | Memory buffer |
| SCB4_EZ_DATA183 | 0x406406DC | FULL | Memory buffer |
| SCB4_EZ_DATA184 | 0x406406E0 | FULL | Memory buffer |
| SCB4_EZ_DATA185 | 0x406406E4 | FULL | Memory buffer |
| SCB4_EZ_DATA186 | 0x406406E8 | FULL | Memory buffer |
| SCB4_EZ_DATA187 | 0x406406EC | FULL | Memory buffer |
| SCB4_EZ_DATA188 | 0x406406F0 | FULL | Memory buffer |
| SCB4_EZ_DATA189 | 0x406406F4 | FULL | Memory buffer |
| SCB4_EZ_DATA190 | 0x406406F8 | FULL | Memory buffer |
| SCB4_EZ_DATA191 | 0x406406FC | FULL | Memory buffer |
| SCB4_EZ_DATA192 | 0x40640700 | FULL | Memory buffer |
| SCB4_EZ_DATA193 | 0x40640704 | FULL | Memory buffer |
| SCB4_EZ_DATA194 | 0x40640708 | FULL | Memory buffer |
| SCB4_EZ_DATA195 | 0x4064070C | FULL | Memory buffer |
| SCB4_EZ_DATA196 | 0x40640710 | FULL | Memory buffer |
| SCB4_EZ_DATA197 | 0x40640714 | FULL | Memory buffer |
| SCB4_EZ_DATA198 | 0x40640718 | FULL | Memory buffer |
| SCB4_EZ_DATA199 | 0x4064071C | FULL | Memory buffer |
| SCB4_EZ_DATA200 | 0x40640720 | FULL | Memory buffer |
| SCB4_EZ_DATA201 | 0x40640724 | FULL | Memory buffer |
| SCB4_EZ_DATA202 | 0x40640728 | FULL | Memory buffer |
| SCB4_EZ_DATA203 | 0x4064072C | FULL | Memory buffer |
| SCB4_EZ_DATA204 | 0x40640730 | FULL | Memory buffer |
| SCB4_EZ_DATA205 | 0x40640734 | FULL | Memory buffer |
| SCB4_EZ_DATA206 | 0x40640738 | FULL | Memory buffer |
| SCB4_EZ_DATA207 | 0x4064073C | FULL | Memory buffer |
| SCB4_EZ_DATA208 | 0x40640740 | FULL | Memory buffer |
| SCB4_EZ_DATA209 | 0x40640744 | FULL | Memory buffer |
| SCB4_EZ_DATA210 | 0x40640748 | FULL | Memory buffer |
| SCB4_EZ_DATA211 | 0x4064074C | FULL | Memory buffer |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SCB4_EZ_DATA212 | 0x40640750 | FULL | Memory buffer |
| SCB4_EZ_DATA213 | 0x40640754 | FULL | Memory buffer |
| SCB4_EZ_DATA214 | 0x40640758 | FULL | Memory buffer |
| SCB4_EZ_DATA215 | 0x4064075C | FULL | Memory buffer |
| SCB4_EZ_DATA216 | 0x40640760 | FULL | Memory buffer |
| SCB4_EZ_DATA217 | 0x40640764 | FULL | Memory buffer |
| SCB4_EZ_DATA218 | 0x40640768 | FULL | Memory buffer |
| SCB4_EZ_DATA219 | 0x4064076C | FULL | Memory buffer |
| SCB4_EZ_DATA220 | 0x40640770 | FULL | Memory buffer |
| SCB4_EZ_DATA221 | 0x40640774 | FULL | Memory buffer |
| SCB4_EZ_DATA222 | 0x40640778 | FULL | Memory buffer |
| SCB4_EZ_DATA223 | 0x4064077C | FULL | Memory buffer |
| SCB4_EZ_DATA224 | 0x40640780 | FULL | Memory buffer |
| SCB4_EZ_DATA225 | 0x40640784 | FULL | Memory buffer |
| SCB4_EZ_DATA226 | 0x40640788 | FULL | Memory buffer |
| SCB4_EZ_DATA227 | 0x4064078C | FULL | Memory buffer |
| SCB4_EZ_DATA228 | 0x40640790 | FULL | Memory buffer |
| SCB4_EZ_DATA229 | 0x40640794 | FULL | Memory buffer |
| SCB4_EZ_DATA230 | 0x40640798 | FULL | Memory buffer |
| SCB4_EZ_DATA231 | 0x4064079C | FULL | Memory buffer |
| SCB4_EZ_DATA232 | 0x406407A0 | FULL | Memory buffer |
| SCB4_EZ_DATA233 | 0x406407A4 | FULL | Memory buffer |
| SCB4_EZ_DATA234 | 0x406407A8 | FULL | Memory buffer |
| SCB4_EZ_DATA235 | 0x406407AC | FULL | Memory buffer |
| SCB4_EZ_DATA236 | 0x406407B0 | FULL | Memory buffer |
| SCB4_EZ_DATA237 | 0x406407B4 | FULL | Memory buffer |
| SCB4_EZ_DATA238 | 0x406407B8 | FULL | Memory buffer |
| SCB4_EZ_DATA239 | 0x406407BC | FULL | Memory buffer |
| SCB4_EZ_DATA240 | 0x406407C0 | FULL | Memory buffer |
| SCB4_EZ_DATA241 | 0x406407C4 | FULL | Memory buffer |
| SCB4_EZ_DATA242 | 0x406407C8 | FULL | Memory buffer |
| SCB4_EZ_DATA243 | 0x406407CC | FULL | Memory buffer |
| SCB4_EZ_DATA244 | 0x406407D0 | FULL | Memory buffer |
| SCB4_EZ_DATA245 | 0x406407D4 | FULL | Memory buffer |
| SCB4_EZ_DATA246 | 0x406407D8 | FULL | Memory buffer |
| SCB4_EZ_DATA247 | 0x406407DC | FULL | Memory buffer |
| SCB4_EZ_DATA248 | 0x406407E0 | FULL | Memory buffer |
| SCB4_EZ_DATA249 | 0x406407E4 | FULL | Memory buffer |
| SCB4_EZ_DATA250 | 0x406407E8 | FULL | Memory buffer |
| SCB4_EZ_DATA251 | 0x406407EC | FULL | Memory buffer |
| SCB4_EZ_DATA252 | 0x406407F0 | FULL | Memory buffer |
| SCB4_EZ_DATA253 | 0x406407F4 | FULL | Memory buffer |
| SCB4_EZ_DATA254 | 0x406407F8 | FULL | Memory buffer |
| SCB4_EZ_DATA255 | 0x406407FC | FULL | Memory buffer |
| SCB4_INTR_CAUSE | 0x40640E00 | FULL | Active clocked interrupt signal<br>Note:I2C_EC is not available for this register |
| SCB4_INTR_SPI_EC | 0x40640EC0 | FULL | Externally clocked SPI interrupt request |
| SCB4_INTR_SPI_EC_MASK | 0x40640EC8 | FULL | Externally clocked SPI interrupt mask |
| SCB4_INTR_SPI_EC_MASKED | 0x40640ECC | FULL | Externally clocked SPI interrupt masked |
| SCB4_INTR_M | 0x40640F00 | FULL | Master interrupt request |
| SCB4_INTR_M_SET | 0x40640F04 | FULL | Master interrupt set request |
| SCB4_INTR_M_MASK | 0x40640F08 | FULL | Master interrupt mask |
| SCB4_INTR_M_MASKED | 0x40640F0C | FULL | Master interrupt masked request |
| SCB4_INTR_S | 0x40640F40 | FULL | Slave interrupt request |
| SCB4_INTR_S_SET | 0x40640F44 | FULL | Slave interrupt set request |
| SCB4_INTR_S_MASK | 0x40640F48 | FULL | Slave interrupt mask |
| SCB4_INTR_S_MASKED | 0x40640F4C | FULL | Slave interrupt masked request |
| SCB4_INTR_TX | 0x40640F80 | FULL | Transmitter interrupt request |
| SCB4_INTR_TX_SET | 0x40640F84 | FULL | Transmitter interrupt set request |
| SCB4_INTR_TX_MASK | 0x40640F88 | FULL | Transmitter interrupt mask |
| SCB4_INTR_TX_MASKED | 0x40640F8C | FULL | Transmitter interrupt masked request |
| SCB4_INTR_RX | 0x40640FC0 | FULL | Receiver interrupt request |
| SCB4_INTR_RX_SET | 0x40640FC4 | FULL | Receiver interrupt set request |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SCB4_INTR_RX_MASK | 0x40640FC8 | FULL | Receiver interrupt mask |
| SCB4_INTR_RX_MASKED | 0x40640FCC | FULL | Receiver interrupt masked request |

## 26.6 SCB 5

**Description** Serial Communications Block (SPI/UART/I2C)
**Base Address** 0x40650000
**Size** 0x10000
**Slave Num** MMIO6 - 5

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SCB5_CTRL | 0x40650000 | FULL | Generic control<br>Note:CMD_RESP_MODE is not available for this register |
| SCB5_STATUS | 0x40650004 | FULL | Generic status |
| SCB5_SPI_CTRL | 0x40650020 | FULL | SPI control |
| SCB5_SPI_STATUS | 0x40650024 | FULL | SPI status |
| SCB5_SPI_TX_CTRL | 0x40650028 | FULL | SPI transmitter control |
| SCB5_SPI_RX_CTRL | 0x4065002C | FULL | SPI receiver control |
| SCB5_UART_CTRL | 0x40650040 | FULL | UART control |
| SCB5_UART_TX_CTRL | 0x40650044 | FULL | UART transmitter control |
| SCB5_UART_RX_CTRL | 0x40650048 | FULL | UART receiver control |
| SCB5_UART_RX_STATUS | 0x4065004C | FULL | UART receiver status |
| SCB5_UART_FLOW_CTRL | 0x40650050 | FULL | UART flow control |
| SCB5_I2C_CTRL | 0x40650060 | FULL | I2C control |
| SCB5_I2C_STATUS | 0x40650064 | FULL | I2C status<br>Note:I2C_EC_BUSY is not available for this register |
| SCB5_I2C_M_CMD | 0x40650068 | FULL | I2C master command |
| SCB5_I2C_S_CMD | 0x4065006C | FULL | I2C slave command |
| SCB5_I2C_CFG | 0x40650070 | FULL | I2C configuration |
| SCB5_TX_CTRL | 0x40650200 | FULL | Transmitter control |
| SCB5_TX_FIFO_CTRL | 0x40650204 | FULL | Transmitter FIFO control |
| SCB5_TX_FIFO_STATUS | 0x40650208 | FULL | Transmitter FIFO status |
| SCB5_TX_FIFO_WR | 0x40650240 | FULL | Transmitter FIFO write |
| SCB5_RX_CTRL | 0x40650300 | FULL | Receiver control |
| SCB5_RX_FIFO_CTRL | 0x40650304 | FULL | Receiver FIFO control |
| SCB5_RX_FIFO_STATUS | 0x40650308 | FULL | Receiver FIFO status |
| SCB5_RX_MATCH | 0x40650310 | FULL | Slave address and mask |
| SCB5_RX_FIFO_RD | 0x40650340 | FULL | Receiver FIFO read |
| SCB5_RX_FIFO_RD_SILENT | 0x40650344 | FULL | Receiver FIFO read silent |
| SCB5_EZ_DATA0 | 0x40650400 | FULL | Memory buffer |
| SCB5_EZ_DATA1 | 0x40650404 | FULL | Memory buffer |
| SCB5_EZ_DATA2 | 0x40650408 | FULL | Memory buffer |
| SCB5_EZ_DATA3 | 0x4065040C | FULL | Memory buffer |
| SCB5_EZ_DATA4 | 0x40650410 | FULL | Memory buffer |
| SCB5_EZ_DATA5 | 0x40650414 | FULL | Memory buffer |
| SCB5_EZ_DATA6 | 0x40650418 | FULL | Memory buffer |
| SCB5_EZ_DATA7 | 0x4065041C | FULL | Memory buffer |
| SCB5_EZ_DATA8 | 0x40650420 | FULL | Memory buffer |
| SCB5_EZ_DATA9 | 0x40650424 | FULL | Memory buffer |
| SCB5_EZ_DATA10 | 0x40650428 | FULL | Memory buffer |
| SCB5_EZ_DATA11 | 0x4065042C | FULL | Memory buffer |
| SCB5_EZ_DATA12 | 0x40650430 | FULL | Memory buffer |
| SCB5_EZ_DATA13 | 0x40650434 | FULL | Memory buffer |
| SCB5_EZ_DATA14 | 0x40650438 | FULL | Memory buffer |
| SCB5_EZ_DATA15 | 0x4065043C | FULL | Memory buffer |
| SCB5_EZ_DATA16 | 0x40650440 | FULL | Memory buffer |
| SCB5_EZ_DATA17 | 0x40650444 | FULL | Memory buffer |
| SCB5_EZ_DATA18 | 0x40650448 | FULL | Memory buffer |
| SCB5_EZ_DATA19 | 0x4065044C | FULL | Memory buffer |
| SCB5_EZ_DATA20 | 0x40650450 | FULL | Memory buffer |
| SCB5_EZ_DATA21 | 0x40650454 | FULL | Memory buffer |
| SCB5_EZ_DATA22 | 0x40650458 | FULL | Memory buffer |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SCB5_EZ_DATA23 | 0x4065045C | FULL | Memory buffer |
| SCB5_EZ_DATA24 | 0x40650460 | FULL | Memory buffer |
| SCB5_EZ_DATA25 | 0x40650464 | FULL | Memory buffer |
| SCB5_EZ_DATA26 | 0x40650468 | FULL | Memory buffer |
| SCB5_EZ_DATA27 | 0x4065046C | FULL | Memory buffer |
| SCB5_EZ_DATA28 | 0x40650470 | FULL | Memory buffer |
| SCB5_EZ_DATA29 | 0x40650474 | FULL | Memory buffer |
| SCB5_EZ_DATA30 | 0x40650478 | FULL | Memory buffer |
| SCB5_EZ_DATA31 | 0x4065047C | FULL | Memory buffer |
| SCB5_EZ_DATA32 | 0x40650480 | FULL | Memory buffer |
| SCB5_EZ_DATA33 | 0x40650484 | FULL | Memory buffer |
| SCB5_EZ_DATA34 | 0x40650488 | FULL | Memory buffer |
| SCB5_EZ_DATA35 | 0x4065048C | FULL | Memory buffer |
| SCB5_EZ_DATA36 | 0x40650490 | FULL | Memory buffer |
| SCB5_EZ_DATA37 | 0x40650494 | FULL | Memory buffer |
| SCB5_EZ_DATA38 | 0x40650498 | FULL | Memory buffer |
| SCB5_EZ_DATA39 | 0x4065049C | FULL | Memory buffer |
| SCB5_EZ_DATA40 | 0x406504A0 | FULL | Memory buffer |
| SCB5_EZ_DATA41 | 0x406504A4 | FULL | Memory buffer |
| SCB5_EZ_DATA42 | 0x406504A8 | FULL | Memory buffer |
| SCB5_EZ_DATA43 | 0x406504AC | FULL | Memory buffer |
| SCB5_EZ_DATA44 | 0x406504B0 | FULL | Memory buffer |
| SCB5_EZ_DATA45 | 0x406504B4 | FULL | Memory buffer |
| SCB5_EZ_DATA46 | 0x406504B8 | FULL | Memory buffer |
| SCB5_EZ_DATA47 | 0x406504BC | FULL | Memory buffer |
| SCB5_EZ_DATA48 | 0x406504C0 | FULL | Memory buffer |
| SCB5_EZ_DATA49 | 0x406504C4 | FULL | Memory buffer |
| SCB5_EZ_DATA50 | 0x406504C8 | FULL | Memory buffer |
| SCB5_EZ_DATA51 | 0x406504CC | FULL | Memory buffer |
| SCB5_EZ_DATA52 | 0x406504D0 | FULL | Memory buffer |
| SCB5_EZ_DATA53 | 0x406504D4 | FULL | Memory buffer |
| SCB5_EZ_DATA54 | 0x406504D8 | FULL | Memory buffer |
| SCB5_EZ_DATA55 | 0x406504DC | FULL | Memory buffer |
| SCB5_EZ_DATA56 | 0x406504E0 | FULL | Memory buffer |
| SCB5_EZ_DATA57 | 0x406504E4 | FULL | Memory buffer |
| SCB5_EZ_DATA58 | 0x406504E8 | FULL | Memory buffer |
| SCB5_EZ_DATA59 | 0x406504EC | FULL | Memory buffer |
| SCB5_EZ_DATA60 | 0x406504F0 | FULL | Memory buffer |
| SCB5_EZ_DATA61 | 0x406504F4 | FULL | Memory buffer |
| SCB5_EZ_DATA62 | 0x406504F8 | FULL | Memory buffer |
| SCB5_EZ_DATA63 | 0x406504FC | FULL | Memory buffer |
| SCB5_EZ_DATA64 | 0x40650500 | FULL | Memory buffer |
| SCB5_EZ_DATA65 | 0x40650504 | FULL | Memory buffer |
| SCB5_EZ_DATA66 | 0x40650508 | FULL | Memory buffer |
| SCB5_EZ_DATA67 | 0x4065050C | FULL | Memory buffer |
| SCB5_EZ_DATA68 | 0x40650510 | FULL | Memory buffer |
| SCB5_EZ_DATA69 | 0x40650514 | FULL | Memory buffer |
| SCB5_EZ_DATA70 | 0x40650518 | FULL | Memory buffer |
| SCB5_EZ_DATA71 | 0x4065051C | FULL | Memory buffer |
| SCB5_EZ_DATA72 | 0x40650520 | FULL | Memory buffer |
| SCB5_EZ_DATA73 | 0x40650524 | FULL | Memory buffer |
| SCB5_EZ_DATA74 | 0x40650528 | FULL | Memory buffer |
| SCB5_EZ_DATA75 | 0x4065052C | FULL | Memory buffer |
| SCB5_EZ_DATA76 | 0x40650530 | FULL | Memory buffer |
| SCB5_EZ_DATA77 | 0x40650534 | FULL | Memory buffer |
| SCB5_EZ_DATA78 | 0x40650538 | FULL | Memory buffer |
| SCB5_EZ_DATA79 | 0x4065053C | FULL | Memory buffer |
| SCB5_EZ_DATA80 | 0x40650540 | FULL | Memory buffer |
| SCB5_EZ_DATA81 | 0x40650544 | FULL | Memory buffer |
| SCB5_EZ_DATA82 | 0x40650548 | FULL | Memory buffer |
| SCB5_EZ_DATA83 | 0x4065054C | FULL | Memory buffer |
| SCB5_EZ_DATA84 | 0x40650550 | FULL | Memory buffer |
| SCB5_EZ_DATA85 | 0x40650554 | FULL | Memory buffer |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SCB5_EZ_DATA86 | 0x40650558 | FULL | Memory buffer |
| SCB5_EZ_DATA87 | 0x4065055C | FULL | Memory buffer |
| SCB5_EZ_DATA88 | 0x40650560 | FULL | Memory buffer |
| SCB5_EZ_DATA89 | 0x40650564 | FULL | Memory buffer |
| SCB5_EZ_DATA90 | 0x40650568 | FULL | Memory buffer |
| SCB5_EZ_DATA91 | 0x4065056C | FULL | Memory buffer |
| SCB5_EZ_DATA92 | 0x40650570 | FULL | Memory buffer |
| SCB5_EZ_DATA93 | 0x40650574 | FULL | Memory buffer |
| SCB5_EZ_DATA94 | 0x40650578 | FULL | Memory buffer |
| SCB5_EZ_DATA95 | 0x4065057C | FULL | Memory buffer |
| SCB5_EZ_DATA96 | 0x40650580 | FULL | Memory buffer |
| SCB5_EZ_DATA97 | 0x40650584 | FULL | Memory buffer |
| SCB5_EZ_DATA98 | 0x40650588 | FULL | Memory buffer |
| SCB5_EZ_DATA99 | 0x4065058C | FULL | Memory buffer |
| SCB5_EZ_DATA100 | 0x40650590 | FULL | Memory buffer |
| SCB5_EZ_DATA101 | 0x40650594 | FULL | Memory buffer |
| SCB5_EZ_DATA102 | 0x40650598 | FULL | Memory buffer |
| SCB5_EZ_DATA103 | 0x4065059C | FULL | Memory buffer |
| SCB5_EZ_DATA104 | 0x406505A0 | FULL | Memory buffer |
| SCB5_EZ_DATA105 | 0x406505A4 | FULL | Memory buffer |
| SCB5_EZ_DATA106 | 0x406505A8 | FULL | Memory buffer |
| SCB5_EZ_DATA107 | 0x406505AC | FULL | Memory buffer |
| SCB5_EZ_DATA108 | 0x406505B0 | FULL | Memory buffer |
| SCB5_EZ_DATA109 | 0x406505B4 | FULL | Memory buffer |
| SCB5_EZ_DATA110 | 0x406505B8 | FULL | Memory buffer |
| SCB5_EZ_DATA111 | 0x406505BC | FULL | Memory buffer |
| SCB5_EZ_DATA112 | 0x406505C0 | FULL | Memory buffer |
| SCB5_EZ_DATA113 | 0x406505C4 | FULL | Memory buffer |
| SCB5_EZ_DATA114 | 0x406505C8 | FULL | Memory buffer |
| SCB5_EZ_DATA115 | 0x406505CC | FULL | Memory buffer |
| SCB5_EZ_DATA116 | 0x406505D0 | FULL | Memory buffer |
| SCB5_EZ_DATA117 | 0x406505D4 | FULL | Memory buffer |
| SCB5_EZ_DATA118 | 0x406505D8 | FULL | Memory buffer |
| SCB5_EZ_DATA119 | 0x406505DC | FULL | Memory buffer |
| SCB5_EZ_DATA120 | 0x406505E0 | FULL | Memory buffer |
| SCB5_EZ_DATA121 | 0x406505E4 | FULL | Memory buffer |
| SCB5_EZ_DATA122 | 0x406505E8 | FULL | Memory buffer |
| SCB5_EZ_DATA123 | 0x406505EC | FULL | Memory buffer |
| SCB5_EZ_DATA124 | 0x406505F0 | FULL | Memory buffer |
| SCB5_EZ_DATA125 | 0x406505F4 | FULL | Memory buffer |
| SCB5_EZ_DATA126 | 0x406505F8 | FULL | Memory buffer |
| SCB5_EZ_DATA127 | 0x406505FC | FULL | Memory buffer |
| SCB5_EZ_DATA128 | 0x40650600 | FULL | Memory buffer |
| SCB5_EZ_DATA129 | 0x40650604 | FULL | Memory buffer |
| SCB5_EZ_DATA130 | 0x40650608 | FULL | Memory buffer |
| SCB5_EZ_DATA131 | 0x4065060C | FULL | Memory buffer |
| SCB5_EZ_DATA132 | 0x40650610 | FULL | Memory buffer |
| SCB5_EZ_DATA133 | 0x40650614 | FULL | Memory buffer |
| SCB5_EZ_DATA134 | 0x40650618 | FULL | Memory buffer |
| SCB5_EZ_DATA135 | 0x4065061C | FULL | Memory buffer |
| SCB5_EZ_DATA136 | 0x40650620 | FULL | Memory buffer |
| SCB5_EZ_DATA137 | 0x40650624 | FULL | Memory buffer |
| SCB5_EZ_DATA138 | 0x40650628 | FULL | Memory buffer |
| SCB5_EZ_DATA139 | 0x4065062C | FULL | Memory buffer |
| SCB5_EZ_DATA140 | 0x40650630 | FULL | Memory buffer |
| SCB5_EZ_DATA141 | 0x40650634 | FULL | Memory buffer |
| SCB5_EZ_DATA142 | 0x40650638 | FULL | Memory buffer |
| SCB5_EZ_DATA143 | 0x4065063C | FULL | Memory buffer |
| SCB5_EZ_DATA144 | 0x40650640 | FULL | Memory buffer |
| SCB5_EZ_DATA145 | 0x40650644 | FULL | Memory buffer |
| SCB5_EZ_DATA146 | 0x40650648 | FULL | Memory buffer |
| SCB5_EZ_DATA147 | 0x4065064C | FULL | Memory buffer |
| SCB5_EZ_DATA148 | 0x40650650 | FULL | Memory buffer |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SCB5_EZ_DATA149 | 0x40650654 | FULL | Memory buffer |
| SCB5_EZ_DATA150 | 0x40650658 | FULL | Memory buffer |
| SCB5_EZ_DATA151 | 0x4065065C | FULL | Memory buffer |
| SCB5_EZ_DATA152 | 0x40650660 | FULL | Memory buffer |
| SCB5_EZ_DATA153 | 0x40650664 | FULL | Memory buffer |
| SCB5_EZ_DATA154 | 0x40650668 | FULL | Memory buffer |
| SCB5_EZ_DATA155 | 0x4065066C | FULL | Memory buffer |
| SCB5_EZ_DATA156 | 0x40650670 | FULL | Memory buffer |
| SCB5_EZ_DATA157 | 0x40650674 | FULL | Memory buffer |
| SCB5_EZ_DATA158 | 0x40650678 | FULL | Memory buffer |
| SCB5_EZ_DATA159 | 0x4065067C | FULL | Memory buffer |
| SCB5_EZ_DATA160 | 0x40650680 | FULL | Memory buffer |
| SCB5_EZ_DATA161 | 0x40650684 | FULL | Memory buffer |
| SCB5_EZ_DATA162 | 0x40650688 | FULL | Memory buffer |
| SCB5_EZ_DATA163 | 0x4065068C | FULL | Memory buffer |
| SCB5_EZ_DATA164 | 0x40650690 | FULL | Memory buffer |
| SCB5_EZ_DATA165 | 0x40650694 | FULL | Memory buffer |
| SCB5_EZ_DATA166 | 0x40650698 | FULL | Memory buffer |
| SCB5_EZ_DATA167 | 0x4065069C | FULL | Memory buffer |
| SCB5_EZ_DATA168 | 0x406506A0 | FULL | Memory buffer |
| SCB5_EZ_DATA169 | 0x406506A4 | FULL | Memory buffer |
| SCB5_EZ_DATA170 | 0x406506A8 | FULL | Memory buffer |
| SCB5_EZ_DATA171 | 0x406506AC | FULL | Memory buffer |
| SCB5_EZ_DATA172 | 0x406506B0 | FULL | Memory buffer |
| SCB5_EZ_DATA173 | 0x406506B4 | FULL | Memory buffer |
| SCB5_EZ_DATA174 | 0x406506B8 | FULL | Memory buffer |
| SCB5_EZ_DATA175 | 0x406506BC | FULL | Memory buffer |
| SCB5_EZ_DATA176 | 0x406506C0 | FULL | Memory buffer |
| SCB5_EZ_DATA177 | 0x406506C4 | FULL | Memory buffer |
| SCB5_EZ_DATA178 | 0x406506C8 | FULL | Memory buffer |
| SCB5_EZ_DATA179 | 0x406506CC | FULL | Memory buffer |
| SCB5_EZ_DATA180 | 0x406506D0 | FULL | Memory buffer |
| SCB5_EZ_DATA181 | 0x406506D4 | FULL | Memory buffer |
| SCB5_EZ_DATA182 | 0x406506D8 | FULL | Memory buffer |
| SCB5_EZ_DATA183 | 0x406506DC | FULL | Memory buffer |
| SCB5_EZ_DATA184 | 0x406506E0 | FULL | Memory buffer |
| SCB5_EZ_DATA185 | 0x406506E4 | FULL | Memory buffer |
| SCB5_EZ_DATA186 | 0x406506E8 | FULL | Memory buffer |
| SCB5_EZ_DATA187 | 0x406506EC | FULL | Memory buffer |
| SCB5_EZ_DATA188 | 0x406506F0 | FULL | Memory buffer |
| SCB5_EZ_DATA189 | 0x406506F4 | FULL | Memory buffer |
| SCB5_EZ_DATA190 | 0x406506F8 | FULL | Memory buffer |
| SCB5_EZ_DATA191 | 0x406506FC | FULL | Memory buffer |
| SCB5_EZ_DATA192 | 0x40650700 | FULL | Memory buffer |
| SCB5_EZ_DATA193 | 0x40650704 | FULL | Memory buffer |
| SCB5_EZ_DATA194 | 0x40650708 | FULL | Memory buffer |
| SCB5_EZ_DATA195 | 0x4065070C | FULL | Memory buffer |
| SCB5_EZ_DATA196 | 0x40650710 | FULL | Memory buffer |
| SCB5_EZ_DATA197 | 0x40650714 | FULL | Memory buffer |
| SCB5_EZ_DATA198 | 0x40650718 | FULL | Memory buffer |
| SCB5_EZ_DATA199 | 0x4065071C | FULL | Memory buffer |
| SCB5_EZ_DATA200 | 0x40650720 | FULL | Memory buffer |
| SCB5_EZ_DATA201 | 0x40650724 | FULL | Memory buffer |
| SCB5_EZ_DATA202 | 0x40650728 | FULL | Memory buffer |
| SCB5_EZ_DATA203 | 0x4065072C | FULL | Memory buffer |
| SCB5_EZ_DATA204 | 0x40650730 | FULL | Memory buffer |
| SCB5_EZ_DATA205 | 0x40650734 | FULL | Memory buffer |
| SCB5_EZ_DATA206 | 0x40650738 | FULL | Memory buffer |
| SCB5_EZ_DATA207 | 0x4065073C | FULL | Memory buffer |
| SCB5_EZ_DATA208 | 0x40650740 | FULL | Memory buffer |
| SCB5_EZ_DATA209 | 0x40650744 | FULL | Memory buffer |
| SCB5_EZ_DATA210 | 0x40650748 | FULL | Memory buffer |
| SCB5_EZ_DATA211 | 0x4065074C | FULL | Memory buffer |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SCB5_EZ_DATA212 | 0x40650750 | FULL | Memory buffer |
| SCB5_EZ_DATA213 | 0x40650754 | FULL | Memory buffer |
| SCB5_EZ_DATA214 | 0x40650758 | FULL | Memory buffer |
| SCB5_EZ_DATA215 | 0x4065075C | FULL | Memory buffer |
| SCB5_EZ_DATA216 | 0x40650760 | FULL | Memory buffer |
| SCB5_EZ_DATA217 | 0x40650764 | FULL | Memory buffer |
| SCB5_EZ_DATA218 | 0x40650768 | FULL | Memory buffer |
| SCB5_EZ_DATA219 | 0x4065076C | FULL | Memory buffer |
| SCB5_EZ_DATA220 | 0x40650770 | FULL | Memory buffer |
| SCB5_EZ_DATA221 | 0x40650774 | FULL | Memory buffer |
| SCB5_EZ_DATA222 | 0x40650778 | FULL | Memory buffer |
| SCB5_EZ_DATA223 | 0x4065077C | FULL | Memory buffer |
| SCB5_EZ_DATA224 | 0x40650780 | FULL | Memory buffer |
| SCB5_EZ_DATA225 | 0x40650784 | FULL | Memory buffer |
| SCB5_EZ_DATA226 | 0x40650788 | FULL | Memory buffer |
| SCB5_EZ_DATA227 | 0x4065078C | FULL | Memory buffer |
| SCB5_EZ_DATA228 | 0x40650790 | FULL | Memory buffer |
| SCB5_EZ_DATA229 | 0x40650794 | FULL | Memory buffer |
| SCB5_EZ_DATA230 | 0x40650798 | FULL | Memory buffer |
| SCB5_EZ_DATA231 | 0x4065079C | FULL | Memory buffer |
| SCB5_EZ_DATA232 | 0x406507A0 | FULL | Memory buffer |
| SCB5_EZ_DATA233 | 0x406507A4 | FULL | Memory buffer |
| SCB5_EZ_DATA234 | 0x406507A8 | FULL | Memory buffer |
| SCB5_EZ_DATA235 | 0x406507AC | FULL | Memory buffer |
| SCB5_EZ_DATA236 | 0x406507B0 | FULL | Memory buffer |
| SCB5_EZ_DATA237 | 0x406507B4 | FULL | Memory buffer |
| SCB5_EZ_DATA238 | 0x406507B8 | FULL | Memory buffer |
| SCB5_EZ_DATA239 | 0x406507BC | FULL | Memory buffer |
| SCB5_EZ_DATA240 | 0x406507C0 | FULL | Memory buffer |
| SCB5_EZ_DATA241 | 0x406507C4 | FULL | Memory buffer |
| SCB5_EZ_DATA242 | 0x406507C8 | FULL | Memory buffer |
| SCB5_EZ_DATA243 | 0x406507CC | FULL | Memory buffer |
| SCB5_EZ_DATA244 | 0x406507D0 | FULL | Memory buffer |
| SCB5_EZ_DATA245 | 0x406507D4 | FULL | Memory buffer |
| SCB5_EZ_DATA246 | 0x406507D8 | FULL | Memory buffer |
| SCB5_EZ_DATA247 | 0x406507DC | FULL | Memory buffer |
| SCB5_EZ_DATA248 | 0x406507E0 | FULL | Memory buffer |
| SCB5_EZ_DATA249 | 0x406507E4 | FULL | Memory buffer |
| SCB5_EZ_DATA250 | 0x406507E8 | FULL | Memory buffer |
| SCB5_EZ_DATA251 | 0x406507EC | FULL | Memory buffer |
| SCB5_EZ_DATA252 | 0x406507F0 | FULL | Memory buffer |
| SCB5_EZ_DATA253 | 0x406507F4 | FULL | Memory buffer |
| SCB5_EZ_DATA254 | 0x406507F8 | FULL | Memory buffer |
| SCB5_EZ_DATA255 | 0x406507FC | FULL | Memory buffer |
| SCB5_INTR_CAUSE | 0x40650E00 | FULL | Active clocked interrupt signal<br>Note:I2C_EC is not available for this register |
| SCB5_INTR_SPI_EC | 0x40650EC0 | FULL | Externally clocked SPI interrupt request |
| SCB5_INTR_SPI_EC_MASK | 0x40650EC8 | FULL | Externally clocked SPI interrupt mask |
| SCB5_INTR_SPI_EC_MASKED | 0x40650ECC | FULL | Externally clocked SPI interrupt masked |
| SCB5_INTR_M | 0x40650F00 | FULL | Master interrupt request |
| SCB5_INTR_M_SET | 0x40650F04 | FULL | Master interrupt set request |
| SCB5_INTR_M_MASK | 0x40650F08 | FULL | Master interrupt mask |
| SCB5_INTR_M_MASKED | 0x40650F0C | FULL | Master interrupt masked request |
| SCB5_INTR_S | 0x40650F40 | FULL | Slave interrupt request |
| SCB5_INTR_S_SET | 0x40650F44 | FULL | Slave interrupt set request |
| SCB5_INTR_S_MASK | 0x40650F48 | FULL | Slave interrupt mask |
| SCB5_INTR_S_MASKED | 0x40650F4C | FULL | Slave interrupt masked request |
| SCB5_INTR_TX | 0x40650F80 | FULL | Transmitter interrupt request |
| SCB5_INTR_TX_SET | 0x40650F84 | FULL | Transmitter interrupt set request |
| SCB5_INTR_TX_MASK | 0x40650F88 | FULL | Transmitter interrupt mask |
| SCB5_INTR_TX_MASKED | 0x40650F8C | FULL | Transmitter interrupt masked request |
| SCB5_INTR_RX | 0x40650FC0 | FULL | Receiver interrupt request |
| SCB5_INTR_RX_SET | 0x40650FC4 | FULL | Receiver interrupt set request |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SCB5_INTR_RX_MASK | 0x40650FC8 | FULL | Receiver interrupt mask |
| SCB5_INTR_RX_MASKED | 0x40650FCC | FULL | Receiver interrupt masked request |

## 26.7 SCB 6

**Description** Serial Communications Block (SPI/UART/I2C)
**Base Address** 0x40660000
**Size** 0x10000
**Slave Num** MMIO6 - 6

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SCB6_CTRL | 0x40660000 | FULL | Generic control<br>Note:CMD_RESP_MODE is not available for this register |
| SCB6_STATUS | 0x40660004 | FULL | Generic status |
| SCB6_SPI_CTRL | 0x40660020 | FULL | SPI control |
| SCB6_SPI_STATUS | 0x40660024 | FULL | SPI status |
| SCB6_SPI_TX_CTRL | 0x40660028 | FULL | SPI transmitter control |
| SCB6_SPI_RX_CTRL | 0x4066002C | FULL | SPI receiver control |
| SCB6_UART_CTRL | 0x40660040 | FULL | UART control |
| SCB6_UART_TX_CTRL | 0x40660044 | FULL | UART transmitter control |
| SCB6_UART_RX_CTRL | 0x40660048 | FULL | UART receiver control |
| SCB6_UART_RX_STATUS | 0x4066004C | FULL | UART receiver status |
| SCB6_UART_FLOW_CTRL | 0x40660050 | FULL | UART flow control |
| SCB6_I2C_CTRL | 0x40660060 | FULL | I2C control |
| SCB6_I2C_STATUS | 0x40660064 | FULL | I2C status<br>Note:I2C_EC_BUSY is not available for this register |
| SCB6_I2C_M_CMD | 0x40660068 | FULL | I2C master command |
| SCB6_I2C_S_CMD | 0x4066006C | FULL | I2C slave command |
| SCB6_I2C_CFG | 0x40660070 | FULL | I2C configuration |
| SCB6_TX_CTRL | 0x40660200 | FULL | Transmitter control |
| SCB6_TX_FIFO_CTRL | 0x40660204 | FULL | Transmitter FIFO control |
| SCB6_TX_FIFO_STATUS | 0x40660208 | FULL | Transmitter FIFO status |
| SCB6_TX_FIFO_WR | 0x40660240 | FULL | Transmitter FIFO write |
| SCB6_RX_CTRL | 0x40660300 | FULL | Receiver control |
| SCB6_RX_FIFO_CTRL | 0x40660304 | FULL | Receiver FIFO control |
| SCB6_RX_FIFO_STATUS | 0x40660308 | FULL | Receiver FIFO status |
| SCB6_RX_MATCH | 0x40660310 | FULL | Slave address and mask |
| SCB6_RX_FIFO_RD | 0x40660340 | FULL | Receiver FIFO read |
| SCB6_RX_FIFO_RD_SILENT | 0x40660344 | FULL | Receiver FIFO read silent |
| SCB6_EZ_DATA0 | 0x40660400 | FULL | Memory buffer |
| SCB6_EZ_DATA1 | 0x40660404 | FULL | Memory buffer |
| SCB6_EZ_DATA2 | 0x40660408 | FULL | Memory buffer |
| SCB6_EZ_DATA3 | 0x4066040C | FULL | Memory buffer |
| SCB6_EZ_DATA4 | 0x40660410 | FULL | Memory buffer |
| SCB6_EZ_DATA5 | 0x40660414 | FULL | Memory buffer |
| SCB6_EZ_DATA6 | 0x40660418 | FULL | Memory buffer |
| SCB6_EZ_DATA7 | 0x4066041C | FULL | Memory buffer |
| SCB6_EZ_DATA8 | 0x40660420 | FULL | Memory buffer |
| SCB6_EZ_DATA9 | 0x40660424 | FULL | Memory buffer |
| SCB6_EZ_DATA10 | 0x40660428 | FULL | Memory buffer |
| SCB6_EZ_DATA11 | 0x4066042C | FULL | Memory buffer |
| SCB6_EZ_DATA12 | 0x40660430 | FULL | Memory buffer |
| SCB6_EZ_DATA13 | 0x40660434 | FULL | Memory buffer |
| SCB6_EZ_DATA14 | 0x40660438 | FULL | Memory buffer |
| SCB6_EZ_DATA15 | 0x4066043C | FULL | Memory buffer |
| SCB6_EZ_DATA16 | 0x40660440 | FULL | Memory buffer |
| SCB6_EZ_DATA17 | 0x40660444 | FULL | Memory buffer |
| SCB6_EZ_DATA18 | 0x40660448 | FULL | Memory buffer |
| SCB6_EZ_DATA19 | 0x4066044C | FULL | Memory buffer |
| SCB6_EZ_DATA20 | 0x40660450 | FULL | Memory buffer |
| SCB6_EZ_DATA21 | 0x40660454 | FULL | Memory buffer |
| SCB6_EZ_DATA22 | 0x40660458 | FULL | Memory buffer |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SCB6_EZ_DATA23 | 0x4066045C | FULL | Memory buffer |
| SCB6_EZ_DATA24 | 0x40660460 | FULL | Memory buffer |
| SCB6_EZ_DATA25 | 0x40660464 | FULL | Memory buffer |
| SCB6_EZ_DATA26 | 0x40660468 | FULL | Memory buffer |
| SCB6_EZ_DATA27 | 0x4066046C | FULL | Memory buffer |
| SCB6_EZ_DATA28 | 0x40660470 | FULL | Memory buffer |
| SCB6_EZ_DATA29 | 0x40660474 | FULL | Memory buffer |
| SCB6_EZ_DATA30 | 0x40660478 | FULL | Memory buffer |
| SCB6_EZ_DATA31 | 0x4066047C | FULL | Memory buffer |
| SCB6_EZ_DATA32 | 0x40660480 | FULL | Memory buffer |
| SCB6_EZ_DATA33 | 0x40660484 | FULL | Memory buffer |
| SCB6_EZ_DATA34 | 0x40660488 | FULL | Memory buffer |
| SCB6_EZ_DATA35 | 0x4066048C | FULL | Memory buffer |
| SCB6_EZ_DATA36 | 0x40660490 | FULL | Memory buffer |
| SCB6_EZ_DATA37 | 0x40660494 | FULL | Memory buffer |
| SCB6_EZ_DATA38 | 0x40660498 | FULL | Memory buffer |
| SCB6_EZ_DATA39 | 0x4066049C | FULL | Memory buffer |
| SCB6_EZ_DATA40 | 0x406604A0 | FULL | Memory buffer |
| SCB6_EZ_DATA41 | 0x406604A4 | FULL | Memory buffer |
| SCB6_EZ_DATA42 | 0x406604A8 | FULL | Memory buffer |
| SCB6_EZ_DATA43 | 0x406604AC | FULL | Memory buffer |
| SCB6_EZ_DATA44 | 0x406604B0 | FULL | Memory buffer |
| SCB6_EZ_DATA45 | 0x406604B4 | FULL | Memory buffer |
| SCB6_EZ_DATA46 | 0x406604B8 | FULL | Memory buffer |
| SCB6_EZ_DATA47 | 0x406604BC | FULL | Memory buffer |
| SCB6_EZ_DATA48 | 0x406604C0 | FULL | Memory buffer |
| SCB6_EZ_DATA49 | 0x406604C4 | FULL | Memory buffer |
| SCB6_EZ_DATA50 | 0x406604C8 | FULL | Memory buffer |
| SCB6_EZ_DATA51 | 0x406604CC | FULL | Memory buffer |
| SCB6_EZ_DATA52 | 0x406604D0 | FULL | Memory buffer |
| SCB6_EZ_DATA53 | 0x406604D4 | FULL | Memory buffer |
| SCB6_EZ_DATA54 | 0x406604D8 | FULL | Memory buffer |
| SCB6_EZ_DATA55 | 0x406604DC | FULL | Memory buffer |
| SCB6_EZ_DATA56 | 0x406604E0 | FULL | Memory buffer |
| SCB6_EZ_DATA57 | 0x406604E4 | FULL | Memory buffer |
| SCB6_EZ_DATA58 | 0x406604E8 | FULL | Memory buffer |
| SCB6_EZ_DATA59 | 0x406604EC | FULL | Memory buffer |
| SCB6_EZ_DATA60 | 0x406604F0 | FULL | Memory buffer |
| SCB6_EZ_DATA61 | 0x406604F4 | FULL | Memory buffer |
| SCB6_EZ_DATA62 | 0x406604F8 | FULL | Memory buffer |
| SCB6_EZ_DATA63 | 0x406604FC | FULL | Memory buffer |
| SCB6_EZ_DATA64 | 0x40660500 | FULL | Memory buffer |
| SCB6_EZ_DATA65 | 0x40660504 | FULL | Memory buffer |
| SCB6_EZ_DATA66 | 0x40660508 | FULL | Memory buffer |
| SCB6_EZ_DATA67 | 0x4066050C | FULL | Memory buffer |
| SCB6_EZ_DATA68 | 0x40660510 | FULL | Memory buffer |
| SCB6_EZ_DATA69 | 0x40660514 | FULL | Memory buffer |
| SCB6_EZ_DATA70 | 0x40660518 | FULL | Memory buffer |
| SCB6_EZ_DATA71 | 0x4066051C | FULL | Memory buffer |
| SCB6_EZ_DATA72 | 0x40660520 | FULL | Memory buffer |
| SCB6_EZ_DATA73 | 0x40660524 | FULL | Memory buffer |
| SCB6_EZ_DATA74 | 0x40660528 | FULL | Memory buffer |
| SCB6_EZ_DATA75 | 0x4066052C | FULL | Memory buffer |
| SCB6_EZ_DATA76 | 0x40660530 | FULL | Memory buffer |
| SCB6_EZ_DATA77 | 0x40660534 | FULL | Memory buffer |
| SCB6_EZ_DATA78 | 0x40660538 | FULL | Memory buffer |
| SCB6_EZ_DATA79 | 0x4066053C | FULL | Memory buffer |
| SCB6_EZ_DATA80 | 0x40660540 | FULL | Memory buffer |
| SCB6_EZ_DATA81 | 0x40660544 | FULL | Memory buffer |
| SCB6_EZ_DATA82 | 0x40660548 | FULL | Memory buffer |
| SCB6_EZ_DATA83 | 0x4066054C | FULL | Memory buffer |
| SCB6_EZ_DATA84 | 0x40660550 | FULL | Memory buffer |
| SCB6_EZ_DATA85 | 0x40660554 | FULL | Memory buffer |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SCB6_EZ_DATA86 | 0x40660558 | FULL | Memory buffer |
| SCB6_EZ_DATA87 | 0x4066055C | FULL | Memory buffer |
| SCB6_EZ_DATA88 | 0x40660560 | FULL | Memory buffer |
| SCB6_EZ_DATA89 | 0x40660564 | FULL | Memory buffer |
| SCB6_EZ_DATA90 | 0x40660568 | FULL | Memory buffer |
| SCB6_EZ_DATA91 | 0x4066056C | FULL | Memory buffer |
| SCB6_EZ_DATA92 | 0x40660570 | FULL | Memory buffer |
| SCB6_EZ_DATA93 | 0x40660574 | FULL | Memory buffer |
| SCB6_EZ_DATA94 | 0x40660578 | FULL | Memory buffer |
| SCB6_EZ_DATA95 | 0x4066057C | FULL | Memory buffer |
| SCB6_EZ_DATA96 | 0x40660580 | FULL | Memory buffer |
| SCB6_EZ_DATA97 | 0x40660584 | FULL | Memory buffer |
| SCB6_EZ_DATA98 | 0x40660588 | FULL | Memory buffer |
| SCB6_EZ_DATA99 | 0x4066058C | FULL | Memory buffer |
| SCB6_EZ_DATA100 | 0x40660590 | FULL | Memory buffer |
| SCB6_EZ_DATA101 | 0x40660594 | FULL | Memory buffer |
| SCB6_EZ_DATA102 | 0x40660598 | FULL | Memory buffer |
| SCB6_EZ_DATA103 | 0x4066059C | FULL | Memory buffer |
| SCB6_EZ_DATA104 | 0x406605A0 | FULL | Memory buffer |
| SCB6_EZ_DATA105 | 0x406605A4 | FULL | Memory buffer |
| SCB6_EZ_DATA106 | 0x406605A8 | FULL | Memory buffer |
| SCB6_EZ_DATA107 | 0x406605AC | FULL | Memory buffer |
| SCB6_EZ_DATA108 | 0x406605B0 | FULL | Memory buffer |
| SCB6_EZ_DATA109 | 0x406605B4 | FULL | Memory buffer |
| SCB6_EZ_DATA110 | 0x406605B8 | FULL | Memory buffer |
| SCB6_EZ_DATA111 | 0x406605BC | FULL | Memory buffer |
| SCB6_EZ_DATA112 | 0x406605C0 | FULL | Memory buffer |
| SCB6_EZ_DATA113 | 0x406605C4 | FULL | Memory buffer |
| SCB6_EZ_DATA114 | 0x406605C8 | FULL | Memory buffer |
| SCB6_EZ_DATA115 | 0x406605CC | FULL | Memory buffer |
| SCB6_EZ_DATA116 | 0x406605D0 | FULL | Memory buffer |
| SCB6_EZ_DATA117 | 0x406605D4 | FULL | Memory buffer |
| SCB6_EZ_DATA118 | 0x406605D8 | FULL | Memory buffer |
| SCB6_EZ_DATA119 | 0x406605DC | FULL | Memory buffer |
| SCB6_EZ_DATA120 | 0x406605E0 | FULL | Memory buffer |
| SCB6_EZ_DATA121 | 0x406605E4 | FULL | Memory buffer |
| SCB6_EZ_DATA122 | 0x406605E8 | FULL | Memory buffer |
| SCB6_EZ_DATA123 | 0x406605EC | FULL | Memory buffer |
| SCB6_EZ_DATA124 | 0x406605F0 | FULL | Memory buffer |
| SCB6_EZ_DATA125 | 0x406605F4 | FULL | Memory buffer |
| SCB6_EZ_DATA126 | 0x406605F8 | FULL | Memory buffer |
| SCB6_EZ_DATA127 | 0x406605FC | FULL | Memory buffer |
| SCB6_EZ_DATA128 | 0x40660600 | FULL | Memory buffer |
| SCB6_EZ_DATA129 | 0x40660604 | FULL | Memory buffer |
| SCB6_EZ_DATA130 | 0x40660608 | FULL | Memory buffer |
| SCB6_EZ_DATA131 | 0x4066060C | FULL | Memory buffer |
| SCB6_EZ_DATA132 | 0x40660610 | FULL | Memory buffer |
| SCB6_EZ_DATA133 | 0x40660614 | FULL | Memory buffer |
| SCB6_EZ_DATA134 | 0x40660618 | FULL | Memory buffer |
| SCB6_EZ_DATA135 | 0x4066061C | FULL | Memory buffer |
| SCB6_EZ_DATA136 | 0x40660620 | FULL | Memory buffer |
| SCB6_EZ_DATA137 | 0x40660624 | FULL | Memory buffer |
| SCB6_EZ_DATA138 | 0x40660628 | FULL | Memory buffer |
| SCB6_EZ_DATA139 | 0x4066062C | FULL | Memory buffer |
| SCB6_EZ_DATA140 | 0x40660630 | FULL | Memory buffer |
| SCB6_EZ_DATA141 | 0x40660634 | FULL | Memory buffer |
| SCB6_EZ_DATA142 | 0x40660638 | FULL | Memory buffer |
| SCB6_EZ_DATA143 | 0x4066063C | FULL | Memory buffer |
| SCB6_EZ_DATA144 | 0x40660640 | FULL | Memory buffer |
| SCB6_EZ_DATA145 | 0x40660644 | FULL | Memory buffer |
| SCB6_EZ_DATA146 | 0x40660648 | FULL | Memory buffer |
| SCB6_EZ_DATA147 | 0x4066064C | FULL | Memory buffer |
| SCB6_EZ_DATA148 | 0x40660650 | FULL | Memory buffer |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SCB6_EZ_DATA149 | 0x40660654 | FULL | Memory buffer |
| SCB6_EZ_DATA150 | 0x40660658 | FULL | Memory buffer |
| SCB6_EZ_DATA151 | 0x4066065C | FULL | Memory buffer |
| SCB6_EZ_DATA152 | 0x40660660 | FULL | Memory buffer |
| SCB6_EZ_DATA153 | 0x40660664 | FULL | Memory buffer |
| SCB6_EZ_DATA154 | 0x40660668 | FULL | Memory buffer |
| SCB6_EZ_DATA155 | 0x4066066C | FULL | Memory buffer |
| SCB6_EZ_DATA156 | 0x40660670 | FULL | Memory buffer |
| SCB6_EZ_DATA157 | 0x40660674 | FULL | Memory buffer |
| SCB6_EZ_DATA158 | 0x40660678 | FULL | Memory buffer |
| SCB6_EZ_DATA159 | 0x4066067C | FULL | Memory buffer |
| SCB6_EZ_DATA160 | 0x40660680 | FULL | Memory buffer |
| SCB6_EZ_DATA161 | 0x40660684 | FULL | Memory buffer |
| SCB6_EZ_DATA162 | 0x40660688 | FULL | Memory buffer |
| SCB6_EZ_DATA163 | 0x4066068C | FULL | Memory buffer |
| SCB6_EZ_DATA164 | 0x40660690 | FULL | Memory buffer |
| SCB6_EZ_DATA165 | 0x40660694 | FULL | Memory buffer |
| SCB6_EZ_DATA166 | 0x40660698 | FULL | Memory buffer |
| SCB6_EZ_DATA167 | 0x4066069C | FULL | Memory buffer |
| SCB6_EZ_DATA168 | 0x406606A0 | FULL | Memory buffer |
| SCB6_EZ_DATA169 | 0x406606A4 | FULL | Memory buffer |
| SCB6_EZ_DATA170 | 0x406606A8 | FULL | Memory buffer |
| SCB6_EZ_DATA171 | 0x406606AC | FULL | Memory buffer |
| SCB6_EZ_DATA172 | 0x406606B0 | FULL | Memory buffer |
| SCB6_EZ_DATA173 | 0x406606B4 | FULL | Memory buffer |
| SCB6_EZ_DATA174 | 0x406606B8 | FULL | Memory buffer |
| SCB6_EZ_DATA175 | 0x406606BC | FULL | Memory buffer |
| SCB6_EZ_DATA176 | 0x406606C0 | FULL | Memory buffer |
| SCB6_EZ_DATA177 | 0x406606C4 | FULL | Memory buffer |
| SCB6_EZ_DATA178 | 0x406606C8 | FULL | Memory buffer |
| SCB6_EZ_DATA179 | 0x406606CC | FULL | Memory buffer |
| SCB6_EZ_DATA180 | 0x406606D0 | FULL | Memory buffer |
| SCB6_EZ_DATA181 | 0x406606D4 | FULL | Memory buffer |
| SCB6_EZ_DATA182 | 0x406606D8 | FULL | Memory buffer |
| SCB6_EZ_DATA183 | 0x406606DC | FULL | Memory buffer |
| SCB6_EZ_DATA184 | 0x406606E0 | FULL | Memory buffer |
| SCB6_EZ_DATA185 | 0x406606E4 | FULL | Memory buffer |
| SCB6_EZ_DATA186 | 0x406606E8 | FULL | Memory buffer |
| SCB6_EZ_DATA187 | 0x406606EC | FULL | Memory buffer |
| SCB6_EZ_DATA188 | 0x406606F0 | FULL | Memory buffer |
| SCB6_EZ_DATA189 | 0x406606F4 | FULL | Memory buffer |
| SCB6_EZ_DATA190 | 0x406606F8 | FULL | Memory buffer |
| SCB6_EZ_DATA191 | 0x406606FC | FULL | Memory buffer |
| SCB6_EZ_DATA192 | 0x40660700 | FULL | Memory buffer |
| SCB6_EZ_DATA193 | 0x40660704 | FULL | Memory buffer |
| SCB6_EZ_DATA194 | 0x40660708 | FULL | Memory buffer |
| SCB6_EZ_DATA195 | 0x4066070C | FULL | Memory buffer |
| SCB6_EZ_DATA196 | 0x40660710 | FULL | Memory buffer |
| SCB6_EZ_DATA197 | 0x40660714 | FULL | Memory buffer |
| SCB6_EZ_DATA198 | 0x40660718 | FULL | Memory buffer |
| SCB6_EZ_DATA199 | 0x4066071C | FULL | Memory buffer |
| SCB6_EZ_DATA200 | 0x40660720 | FULL | Memory buffer |
| SCB6_EZ_DATA201 | 0x40660724 | FULL | Memory buffer |
| SCB6_EZ_DATA202 | 0x40660728 | FULL | Memory buffer |
| SCB6_EZ_DATA203 | 0x4066072C | FULL | Memory buffer |
| SCB6_EZ_DATA204 | 0x40660730 | FULL | Memory buffer |
| SCB6_EZ_DATA205 | 0x40660734 | FULL | Memory buffer |
| SCB6_EZ_DATA206 | 0x40660738 | FULL | Memory buffer |
| SCB6_EZ_DATA207 | 0x4066073C | FULL | Memory buffer |
| SCB6_EZ_DATA208 | 0x40660740 | FULL | Memory buffer |
| SCB6_EZ_DATA209 | 0x40660744 | FULL | Memory buffer |
| SCB6_EZ_DATA210 | 0x40660748 | FULL | Memory buffer |
| SCB6_EZ_DATA211 | 0x4066074C | FULL | Memory buffer |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SCB6_EZ_DATA212 | 0x40660750 | FULL | Memory buffer |
| SCB6_EZ_DATA213 | 0x40660754 | FULL | Memory buffer |
| SCB6_EZ_DATA214 | 0x40660758 | FULL | Memory buffer |
| SCB6_EZ_DATA215 | 0x4066075C | FULL | Memory buffer |
| SCB6_EZ_DATA216 | 0x40660760 | FULL | Memory buffer |
| SCB6_EZ_DATA217 | 0x40660764 | FULL | Memory buffer |
| SCB6_EZ_DATA218 | 0x40660768 | FULL | Memory buffer |
| SCB6_EZ_DATA219 | 0x4066076C | FULL | Memory buffer |
| SCB6_EZ_DATA220 | 0x40660770 | FULL | Memory buffer |
| SCB6_EZ_DATA221 | 0x40660774 | FULL | Memory buffer |
| SCB6_EZ_DATA222 | 0x40660778 | FULL | Memory buffer |
| SCB6_EZ_DATA223 | 0x4066077C | FULL | Memory buffer |
| SCB6_EZ_DATA224 | 0x40660780 | FULL | Memory buffer |
| SCB6_EZ_DATA225 | 0x40660784 | FULL | Memory buffer |
| SCB6_EZ_DATA226 | 0x40660788 | FULL | Memory buffer |
| SCB6_EZ_DATA227 | 0x4066078C | FULL | Memory buffer |
| SCB6_EZ_DATA228 | 0x40660790 | FULL | Memory buffer |
| SCB6_EZ_DATA229 | 0x40660794 | FULL | Memory buffer |
| SCB6_EZ_DATA230 | 0x40660798 | FULL | Memory buffer |
| SCB6_EZ_DATA231 | 0x4066079C | FULL | Memory buffer |
| SCB6_EZ_DATA232 | 0x406607A0 | FULL | Memory buffer |
| SCB6_EZ_DATA233 | 0x406607A4 | FULL | Memory buffer |
| SCB6_EZ_DATA234 | 0x406607A8 | FULL | Memory buffer |
| SCB6_EZ_DATA235 | 0x406607AC | FULL | Memory buffer |
| SCB6_EZ_DATA236 | 0x406607B0 | FULL | Memory buffer |
| SCB6_EZ_DATA237 | 0x406607B4 | FULL | Memory buffer |
| SCB6_EZ_DATA238 | 0x406607B8 | FULL | Memory buffer |
| SCB6_EZ_DATA239 | 0x406607BC | FULL | Memory buffer |
| SCB6_EZ_DATA240 | 0x406607C0 | FULL | Memory buffer |
| SCB6_EZ_DATA241 | 0x406607C4 | FULL | Memory buffer |
| SCB6_EZ_DATA242 | 0x406607C8 | FULL | Memory buffer |
| SCB6_EZ_DATA243 | 0x406607CC | FULL | Memory buffer |
| SCB6_EZ_DATA244 | 0x406607D0 | FULL | Memory buffer |
| SCB6_EZ_DATA245 | 0x406607D4 | FULL | Memory buffer |
| SCB6_EZ_DATA246 | 0x406607D8 | FULL | Memory buffer |
| SCB6_EZ_DATA247 | 0x406607DC | FULL | Memory buffer |
| SCB6_EZ_DATA248 | 0x406607E0 | FULL | Memory buffer |
| SCB6_EZ_DATA249 | 0x406607E4 | FULL | Memory buffer |
| SCB6_EZ_DATA250 | 0x406607E8 | FULL | Memory buffer |
| SCB6_EZ_DATA251 | 0x406607EC | FULL | Memory buffer |
| SCB6_EZ_DATA252 | 0x406607F0 | FULL | Memory buffer |
| SCB6_EZ_DATA253 | 0x406607F4 | FULL | Memory buffer |
| SCB6_EZ_DATA254 | 0x406607F8 | FULL | Memory buffer |
| SCB6_EZ_DATA255 | 0x406607FC | FULL | Memory buffer |
| SCB6_INTR_CAUSE | 0x40660E00 | FULL | Active clocked interrupt signal<br>Note:I2C_EC is not available for this register |
| SCB6_INTR_SPI_EC | 0x40660EC0 | FULL | Externally clocked SPI interrupt request |
| SCB6_INTR_SPI_EC_MASK | 0x40660EC8 | FULL | Externally clocked SPI interrupt mask |
| SCB6_INTR_SPI_EC_MASKED | 0x40660ECC | FULL | Externally clocked SPI interrupt masked |
| SCB6_INTR_M | 0x40660F00 | FULL | Master interrupt request |
| SCB6_INTR_M_SET | 0x40660F04 | FULL | Master interrupt set request |
| SCB6_INTR_M_MASK | 0x40660F08 | FULL | Master interrupt mask |
| SCB6_INTR_M_MASKED | 0x40660F0C | FULL | Master interrupt masked request |
| SCB6_INTR_S | 0x40660F40 | FULL | Slave interrupt request |
| SCB6_INTR_S_SET | 0x40660F44 | FULL | Slave interrupt set request |
| SCB6_INTR_S_MASK | 0x40660F48 | FULL | Slave interrupt mask |
| SCB6_INTR_S_MASKED | 0x40660F4C | FULL | Slave interrupt masked request |
| SCB6_INTR_TX | 0x40660F80 | FULL | Transmitter interrupt request |
| SCB6_INTR_TX_SET | 0x40660F84 | FULL | Transmitter interrupt set request |
| SCB6_INTR_TX_MASK | 0x40660F88 | FULL | Transmitter interrupt mask |
| SCB6_INTR_TX_MASKED | 0x40660F8C | FULL | Transmitter interrupt masked request |
| SCB6_INTR_RX | 0x40660FC0 | FULL | Receiver interrupt request |
| SCB6_INTR_RX_SET | 0x40660FC4 | FULL | Receiver interrupt set request |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SCB6_INTR_RX_MASK | 0x40660FC8 | FULL | Receiver interrupt mask |
| SCB6_INTR_RX_MASKED | 0x40660FCC | FULL | Receiver interrupt masked request |

## 26.8 SCB 7

**Description** Serial Communications Block (SPI/UART/I2C)
**Base Address** 0x40670000
**Size** 0x10000
**Slave Num** MMIO6 - 7

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SCB7_CTRL | 0x40670000 | FULL | Generic control<br>Note:CMD_RESP_MODE is not available for this register |
| SCB7_STATUS | 0x40670004 | FULL | Generic status |
| SCB7_SPI_CTRL | 0x40670020 | FULL | SPI control |
| SCB7_SPI_STATUS | 0x40670024 | FULL | SPI status |
| SCB7_SPI_TX_CTRL | 0x40670028 | FULL | SPI transmitter control |
| SCB7_SPI_RX_CTRL | 0x4067002C | FULL | SPI receiver control |
| SCB7_UART_CTRL | 0x40670040 | FULL | UART control |
| SCB7_UART_TX_CTRL | 0x40670044 | FULL | UART transmitter control |
| SCB7_UART_RX_CTRL | 0x40670048 | FULL | UART receiver control |
| SCB7_UART_RX_STATUS | 0x4067004C | FULL | UART receiver status |
| SCB7_UART_FLOW_CTRL | 0x40670050 | FULL | UART flow control |
| SCB7_I2C_CTRL | 0x40670060 | FULL | I2C control |
| SCB7_I2C_STATUS | 0x40670064 | FULL | I2C status<br>Note:I2C_EC_BUSY is not available for this register |
| SCB7_I2C_M_CMD | 0x40670068 | FULL | I2C master command |
| SCB7_I2C_S_CMD | 0x4067006C | FULL | I2C slave command |
| SCB7_I2C_CFG | 0x40670070 | FULL | I2C configuration |
| SCB7_TX_CTRL | 0x40670200 | FULL | Transmitter control |
| SCB7_TX_FIFO_CTRL | 0x40670204 | FULL | Transmitter FIFO control |
| SCB7_TX_FIFO_STATUS | 0x40670208 | FULL | Transmitter FIFO status |
| SCB7_TX_FIFO_WR | 0x40670240 | FULL | Transmitter FIFO write |
| SCB7_RX_CTRL | 0x40670300 | FULL | Receiver control |
| SCB7_RX_FIFO_CTRL | 0x40670304 | FULL | Receiver FIFO control |
| SCB7_RX_FIFO_STATUS | 0x40670308 | FULL | Receiver FIFO status |
| SCB7_RX_MATCH | 0x40670310 | FULL | Slave address and mask |
| SCB7_RX_FIFO_RD | 0x40670340 | FULL | Receiver FIFO read |
| SCB7_RX_FIFO_RD_SILENT | 0x40670344 | FULL | Receiver FIFO read silent |
| SCB7_EZ_DATA0 | 0x40670400 | FULL | Memory buffer |
| SCB7_EZ_DATA1 | 0x40670404 | FULL | Memory buffer |
| SCB7_EZ_DATA2 | 0x40670408 | FULL | Memory buffer |
| SCB7_EZ_DATA3 | 0x4067040C | FULL | Memory buffer |
| SCB7_EZ_DATA4 | 0x40670410 | FULL | Memory buffer |
| SCB7_EZ_DATA5 | 0x40670414 | FULL | Memory buffer |
| SCB7_EZ_DATA6 | 0x40670418 | FULL | Memory buffer |
| SCB7_EZ_DATA7 | 0x4067041C | FULL | Memory buffer |
| SCB7_EZ_DATA8 | 0x40670420 | FULL | Memory buffer |
| SCB7_EZ_DATA9 | 0x40670424 | FULL | Memory buffer |
| SCB7_EZ_DATA10 | 0x40670428 | FULL | Memory buffer |
| SCB7_EZ_DATA11 | 0x4067042C | FULL | Memory buffer |
| SCB7_EZ_DATA12 | 0x40670430 | FULL | Memory buffer |
| SCB7_EZ_DATA13 | 0x40670434 | FULL | Memory buffer |
| SCB7_EZ_DATA14 | 0x40670438 | FULL | Memory buffer |
| SCB7_EZ_DATA15 | 0x4067043C | FULL | Memory buffer |
| SCB7_EZ_DATA16 | 0x40670440 | FULL | Memory buffer |
| SCB7_EZ_DATA17 | 0x40670444 | FULL | Memory buffer |
| SCB7_EZ_DATA18 | 0x40670448 | FULL | Memory buffer |
| SCB7_EZ_DATA19 | 0x4067044C | FULL | Memory buffer |
| SCB7_EZ_DATA20 | 0x40670450 | FULL | Memory buffer |
| SCB7_EZ_DATA21 | 0x40670454 | FULL | Memory buffer |
| SCB7_EZ_DATA22 | 0x40670458 | FULL | Memory buffer |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SCB7_EZ_DATA23 | 0x4067045C | FULL | Memory buffer |
| SCB7_EZ_DATA24 | 0x40670460 | FULL | Memory buffer |
| SCB7_EZ_DATA25 | 0x40670464 | FULL | Memory buffer |
| SCB7_EZ_DATA26 | 0x40670468 | FULL | Memory buffer |
| SCB7_EZ_DATA27 | 0x4067046C | FULL | Memory buffer |
| SCB7_EZ_DATA28 | 0x40670470 | FULL | Memory buffer |
| SCB7_EZ_DATA29 | 0x40670474 | FULL | Memory buffer |
| SCB7_EZ_DATA30 | 0x40670478 | FULL | Memory buffer |
| SCB7_EZ_DATA31 | 0x4067047C | FULL | Memory buffer |
| SCB7_EZ_DATA32 | 0x40670480 | FULL | Memory buffer |
| SCB7_EZ_DATA33 | 0x40670484 | FULL | Memory buffer |
| SCB7_EZ_DATA34 | 0x40670488 | FULL | Memory buffer |
| SCB7_EZ_DATA35 | 0x4067048C | FULL | Memory buffer |
| SCB7_EZ_DATA36 | 0x40670490 | FULL | Memory buffer |
| SCB7_EZ_DATA37 | 0x40670494 | FULL | Memory buffer |
| SCB7_EZ_DATA38 | 0x40670498 | FULL | Memory buffer |
| SCB7_EZ_DATA39 | 0x4067049C | FULL | Memory buffer |
| SCB7_EZ_DATA40 | 0x406704A0 | FULL | Memory buffer |
| SCB7_EZ_DATA41 | 0x406704A4 | FULL | Memory buffer |
| SCB7_EZ_DATA42 | 0x406704A8 | FULL | Memory buffer |
| SCB7_EZ_DATA43 | 0x406704AC | FULL | Memory buffer |
| SCB7_EZ_DATA44 | 0x406704B0 | FULL | Memory buffer |
| SCB7_EZ_DATA45 | 0x406704B4 | FULL | Memory buffer |
| SCB7_EZ_DATA46 | 0x406704B8 | FULL | Memory buffer |
| SCB7_EZ_DATA47 | 0x406704BC | FULL | Memory buffer |
| SCB7_EZ_DATA48 | 0x406704C0 | FULL | Memory buffer |
| SCB7_EZ_DATA49 | 0x406704C4 | FULL | Memory buffer |
| SCB7_EZ_DATA50 | 0x406704C8 | FULL | Memory buffer |
| SCB7_EZ_DATA51 | 0x406704CC | FULL | Memory buffer |
| SCB7_EZ_DATA52 | 0x406704D0 | FULL | Memory buffer |
| SCB7_EZ_DATA53 | 0x406704D4 | FULL | Memory buffer |
| SCB7_EZ_DATA54 | 0x406704D8 | FULL | Memory buffer |
| SCB7_EZ_DATA55 | 0x406704DC | FULL | Memory buffer |
| SCB7_EZ_DATA56 | 0x406704E0 | FULL | Memory buffer |
| SCB7_EZ_DATA57 | 0x406704E4 | FULL | Memory buffer |
| SCB7_EZ_DATA58 | 0x406704E8 | FULL | Memory buffer |
| SCB7_EZ_DATA59 | 0x406704EC | FULL | Memory buffer |
| SCB7_EZ_DATA60 | 0x406704F0 | FULL | Memory buffer |
| SCB7_EZ_DATA61 | 0x406704F4 | FULL | Memory buffer |
| SCB7_EZ_DATA62 | 0x406704F8 | FULL | Memory buffer |
| SCB7_EZ_DATA63 | 0x406704FC | FULL | Memory buffer |
| SCB7_EZ_DATA64 | 0x40670500 | FULL | Memory buffer |
| SCB7_EZ_DATA65 | 0x40670504 | FULL | Memory buffer |
| SCB7_EZ_DATA66 | 0x40670508 | FULL | Memory buffer |
| SCB7_EZ_DATA67 | 0x4067050C | FULL | Memory buffer |
| SCB7_EZ_DATA68 | 0x40670510 | FULL | Memory buffer |
| SCB7_EZ_DATA69 | 0x40670514 | FULL | Memory buffer |
| SCB7_EZ_DATA70 | 0x40670518 | FULL | Memory buffer |
| SCB7_EZ_DATA71 | 0x4067051C | FULL | Memory buffer |
| SCB7_EZ_DATA72 | 0x40670520 | FULL | Memory buffer |
| SCB7_EZ_DATA73 | 0x40670524 | FULL | Memory buffer |
| SCB7_EZ_DATA74 | 0x40670528 | FULL | Memory buffer |
| SCB7_EZ_DATA75 | 0x4067052C | FULL | Memory buffer |
| SCB7_EZ_DATA76 | 0x40670530 | FULL | Memory buffer |
| SCB7_EZ_DATA77 | 0x40670534 | FULL | Memory buffer |
| SCB7_EZ_DATA78 | 0x40670538 | FULL | Memory buffer |
| SCB7_EZ_DATA79 | 0x4067053C | FULL | Memory buffer |
| SCB7_EZ_DATA80 | 0x40670540 | FULL | Memory buffer |
| SCB7_EZ_DATA81 | 0x40670544 | FULL | Memory buffer |
| SCB7_EZ_DATA82 | 0x40670548 | FULL | Memory buffer |
| SCB7_EZ_DATA83 | 0x4067054C | FULL | Memory buffer |
| SCB7_EZ_DATA84 | 0x40670550 | FULL | Memory buffer |
| SCB7_EZ_DATA85 | 0x40670554 | FULL | Memory buffer |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SCB7_EZ_DATA86 | 0x40670558 | FULL | Memory buffer |
| SCB7_EZ_DATA87 | 0x4067055C | FULL | Memory buffer |
| SCB7_EZ_DATA88 | 0x40670560 | FULL | Memory buffer |
| SCB7_EZ_DATA89 | 0x40670564 | FULL | Memory buffer |
| SCB7_EZ_DATA90 | 0x40670568 | FULL | Memory buffer |
| SCB7_EZ_DATA91 | 0x4067056C | FULL | Memory buffer |
| SCB7_EZ_DATA92 | 0x40670570 | FULL | Memory buffer |
| SCB7_EZ_DATA93 | 0x40670574 | FULL | Memory buffer |
| SCB7_EZ_DATA94 | 0x40670578 | FULL | Memory buffer |
| SCB7_EZ_DATA95 | 0x4067057C | FULL | Memory buffer |
| SCB7_EZ_DATA96 | 0x40670580 | FULL | Memory buffer |
| SCB7_EZ_DATA97 | 0x40670584 | FULL | Memory buffer |
| SCB7_EZ_DATA98 | 0x40670588 | FULL | Memory buffer |
| SCB7_EZ_DATA99 | 0x4067058C | FULL | Memory buffer |
| SCB7_EZ_DATA100 | 0x40670590 | FULL | Memory buffer |
| SCB7_EZ_DATA101 | 0x40670594 | FULL | Memory buffer |
| SCB7_EZ_DATA102 | 0x40670598 | FULL | Memory buffer |
| SCB7_EZ_DATA103 | 0x4067059C | FULL | Memory buffer |
| SCB7_EZ_DATA104 | 0x406705A0 | FULL | Memory buffer |
| SCB7_EZ_DATA105 | 0x406705A4 | FULL | Memory buffer |
| SCB7_EZ_DATA106 | 0x406705A8 | FULL | Memory buffer |
| SCB7_EZ_DATA107 | 0x406705AC | FULL | Memory buffer |
| SCB7_EZ_DATA108 | 0x406705B0 | FULL | Memory buffer |
| SCB7_EZ_DATA109 | 0x406705B4 | FULL | Memory buffer |
| SCB7_EZ_DATA110 | 0x406705B8 | FULL | Memory buffer |
| SCB7_EZ_DATA111 | 0x406705BC | FULL | Memory buffer |
| SCB7_EZ_DATA112 | 0x406705C0 | FULL | Memory buffer |
| SCB7_EZ_DATA113 | 0x406705C4 | FULL | Memory buffer |
| SCB7_EZ_DATA114 | 0x406705C8 | FULL | Memory buffer |
| SCB7_EZ_DATA115 | 0x406705CC | FULL | Memory buffer |
| SCB7_EZ_DATA116 | 0x406705D0 | FULL | Memory buffer |
| SCB7_EZ_DATA117 | 0x406705D4 | FULL | Memory buffer |
| SCB7_EZ_DATA118 | 0x406705D8 | FULL | Memory buffer |
| SCB7_EZ_DATA119 | 0x406705DC | FULL | Memory buffer |
| SCB7_EZ_DATA120 | 0x406705E0 | FULL | Memory buffer |
| SCB7_EZ_DATA121 | 0x406705E4 | FULL | Memory buffer |
| SCB7_EZ_DATA122 | 0x406705E8 | FULL | Memory buffer |
| SCB7_EZ_DATA123 | 0x406705EC | FULL | Memory buffer |
| SCB7_EZ_DATA124 | 0x406705F0 | FULL | Memory buffer |
| SCB7_EZ_DATA125 | 0x406705F4 | FULL | Memory buffer |
| SCB7_EZ_DATA126 | 0x406705F8 | FULL | Memory buffer |
| SCB7_EZ_DATA127 | 0x406705FC | FULL | Memory buffer |
| SCB7_EZ_DATA128 | 0x40670600 | FULL | Memory buffer |
| SCB7_EZ_DATA129 | 0x40670604 | FULL | Memory buffer |
| SCB7_EZ_DATA130 | 0x40670608 | FULL | Memory buffer |
| SCB7_EZ_DATA131 | 0x4067060C | FULL | Memory buffer |
| SCB7_EZ_DATA132 | 0x40670610 | FULL | Memory buffer |
| SCB7_EZ_DATA133 | 0x40670614 | FULL | Memory buffer |
| SCB7_EZ_DATA134 | 0x40670618 | FULL | Memory buffer |
| SCB7_EZ_DATA135 | 0x4067061C | FULL | Memory buffer |
| SCB7_EZ_DATA136 | 0x40670620 | FULL | Memory buffer |
| SCB7_EZ_DATA137 | 0x40670624 | FULL | Memory buffer |
| SCB7_EZ_DATA138 | 0x40670628 | FULL | Memory buffer |
| SCB7_EZ_DATA139 | 0x4067062C | FULL | Memory buffer |
| SCB7_EZ_DATA140 | 0x40670630 | FULL | Memory buffer |
| SCB7_EZ_DATA141 | 0x40670634 | FULL | Memory buffer |
| SCB7_EZ_DATA142 | 0x40670638 | FULL | Memory buffer |
| SCB7_EZ_DATA143 | 0x4067063C | FULL | Memory buffer |
| SCB7_EZ_DATA144 | 0x40670640 | FULL | Memory buffer |
| SCB7_EZ_DATA145 | 0x40670644 | FULL | Memory buffer |
| SCB7_EZ_DATA146 | 0x40670648 | FULL | Memory buffer |
| SCB7_EZ_DATA147 | 0x4067064C | FULL | Memory buffer |
| SCB7_EZ_DATA148 | 0x40670650 | FULL | Memory buffer |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SCB7_EZ_DATA149 | 0x40670654 | FULL | Memory buffer |
| SCB7_EZ_DATA150 | 0x40670658 | FULL | Memory buffer |
| SCB7_EZ_DATA151 | 0x4067065C | FULL | Memory buffer |
| SCB7_EZ_DATA152 | 0x40670660 | FULL | Memory buffer |
| SCB7_EZ_DATA153 | 0x40670664 | FULL | Memory buffer |
| SCB7_EZ_DATA154 | 0x40670668 | FULL | Memory buffer |
| SCB7_EZ_DATA155 | 0x4067066C | FULL | Memory buffer |
| SCB7_EZ_DATA156 | 0x40670670 | FULL | Memory buffer |
| SCB7_EZ_DATA157 | 0x40670674 | FULL | Memory buffer |
| SCB7_EZ_DATA158 | 0x40670678 | FULL | Memory buffer |
| SCB7_EZ_DATA159 | 0x4067067C | FULL | Memory buffer |
| SCB7_EZ_DATA160 | 0x40670680 | FULL | Memory buffer |
| SCB7_EZ_DATA161 | 0x40670684 | FULL | Memory buffer |
| SCB7_EZ_DATA162 | 0x40670688 | FULL | Memory buffer |
| SCB7_EZ_DATA163 | 0x4067068C | FULL | Memory buffer |
| SCB7_EZ_DATA164 | 0x40670690 | FULL | Memory buffer |
| SCB7_EZ_DATA165 | 0x40670694 | FULL | Memory buffer |
| SCB7_EZ_DATA166 | 0x40670698 | FULL | Memory buffer |
| SCB7_EZ_DATA167 | 0x4067069C | FULL | Memory buffer |
| SCB7_EZ_DATA168 | 0x406706A0 | FULL | Memory buffer |
| SCB7_EZ_DATA169 | 0x406706A4 | FULL | Memory buffer |
| SCB7_EZ_DATA170 | 0x406706A8 | FULL | Memory buffer |
| SCB7_EZ_DATA171 | 0x406706AC | FULL | Memory buffer |
| SCB7_EZ_DATA172 | 0x406706B0 | FULL | Memory buffer |
| SCB7_EZ_DATA173 | 0x406706B4 | FULL | Memory buffer |
| SCB7_EZ_DATA174 | 0x406706B8 | FULL | Memory buffer |
| SCB7_EZ_DATA175 | 0x406706BC | FULL | Memory buffer |
| SCB7_EZ_DATA176 | 0x406706C0 | FULL | Memory buffer |
| SCB7_EZ_DATA177 | 0x406706C4 | FULL | Memory buffer |
| SCB7_EZ_DATA178 | 0x406706C8 | FULL | Memory buffer |
| SCB7_EZ_DATA179 | 0x406706CC | FULL | Memory buffer |
| SCB7_EZ_DATA180 | 0x406706D0 | FULL | Memory buffer |
| SCB7_EZ_DATA181 | 0x406706D4 | FULL | Memory buffer |
| SCB7_EZ_DATA182 | 0x406706D8 | FULL | Memory buffer |
| SCB7_EZ_DATA183 | 0x406706DC | FULL | Memory buffer |
| SCB7_EZ_DATA184 | 0x406706E0 | FULL | Memory buffer |
| SCB7_EZ_DATA185 | 0x406706E4 | FULL | Memory buffer |
| SCB7_EZ_DATA186 | 0x406706E8 | FULL | Memory buffer |
| SCB7_EZ_DATA187 | 0x406706EC | FULL | Memory buffer |
| SCB7_EZ_DATA188 | 0x406706F0 | FULL | Memory buffer |
| SCB7_EZ_DATA189 | 0x406706F4 | FULL | Memory buffer |
| SCB7_EZ_DATA190 | 0x406706F8 | FULL | Memory buffer |
| SCB7_EZ_DATA191 | 0x406706FC | FULL | Memory buffer |
| SCB7_EZ_DATA192 | 0x40670700 | FULL | Memory buffer |
| SCB7_EZ_DATA193 | 0x40670704 | FULL | Memory buffer |
| SCB7_EZ_DATA194 | 0x40670708 | FULL | Memory buffer |
| SCB7_EZ_DATA195 | 0x4067070C | FULL | Memory buffer |
| SCB7_EZ_DATA196 | 0x40670710 | FULL | Memory buffer |
| SCB7_EZ_DATA197 | 0x40670714 | FULL | Memory buffer |
| SCB7_EZ_DATA198 | 0x40670718 | FULL | Memory buffer |
| SCB7_EZ_DATA199 | 0x4067071C | FULL | Memory buffer |
| SCB7_EZ_DATA200 | 0x40670720 | FULL | Memory buffer |
| SCB7_EZ_DATA201 | 0x40670724 | FULL | Memory buffer |
| SCB7_EZ_DATA202 | 0x40670728 | FULL | Memory buffer |
| SCB7_EZ_DATA203 | 0x4067072C | FULL | Memory buffer |
| SCB7_EZ_DATA204 | 0x40670730 | FULL | Memory buffer |
| SCB7_EZ_DATA205 | 0x40670734 | FULL | Memory buffer |
| SCB7_EZ_DATA206 | 0x40670738 | FULL | Memory buffer |
| SCB7_EZ_DATA207 | 0x4067073C | FULL | Memory buffer |
| SCB7_EZ_DATA208 | 0x40670740 | FULL | Memory buffer |
| SCB7_EZ_DATA209 | 0x40670744 | FULL | Memory buffer |
| SCB7_EZ_DATA210 | 0x40670748 | FULL | Memory buffer |
| SCB7_EZ_DATA211 | 0x4067074C | FULL | Memory buffer |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SCB7_EZ_DATA212 | 0x40670750 | FULL | Memory buffer |
| SCB7_EZ_DATA213 | 0x40670754 | FULL | Memory buffer |
| SCB7_EZ_DATA214 | 0x40670758 | FULL | Memory buffer |
| SCB7_EZ_DATA215 | 0x4067075C | FULL | Memory buffer |
| SCB7_EZ_DATA216 | 0x40670760 | FULL | Memory buffer |
| SCB7_EZ_DATA217 | 0x40670764 | FULL | Memory buffer |
| SCB7_EZ_DATA218 | 0x40670768 | FULL | Memory buffer |
| SCB7_EZ_DATA219 | 0x4067076C | FULL | Memory buffer |
| SCB7_EZ_DATA220 | 0x40670770 | FULL | Memory buffer |
| SCB7_EZ_DATA221 | 0x40670774 | FULL | Memory buffer |
| SCB7_EZ_DATA222 | 0x40670778 | FULL | Memory buffer |
| SCB7_EZ_DATA223 | 0x4067077C | FULL | Memory buffer |
| SCB7_EZ_DATA224 | 0x40670780 | FULL | Memory buffer |
| SCB7_EZ_DATA225 | 0x40670784 | FULL | Memory buffer |
| SCB7_EZ_DATA226 | 0x40670788 | FULL | Memory buffer |
| SCB7_EZ_DATA227 | 0x4067078C | FULL | Memory buffer |
| SCB7_EZ_DATA228 | 0x40670790 | FULL | Memory buffer |
| SCB7_EZ_DATA229 | 0x40670794 | FULL | Memory buffer |
| SCB7_EZ_DATA230 | 0x40670798 | FULL | Memory buffer |
| SCB7_EZ_DATA231 | 0x4067079C | FULL | Memory buffer |
| SCB7_EZ_DATA232 | 0x406707A0 | FULL | Memory buffer |
| SCB7_EZ_DATA233 | 0x406707A4 | FULL | Memory buffer |
| SCB7_EZ_DATA234 | 0x406707A8 | FULL | Memory buffer |
| SCB7_EZ_DATA235 | 0x406707AC | FULL | Memory buffer |
| SCB7_EZ_DATA236 | 0x406707B0 | FULL | Memory buffer |
| SCB7_EZ_DATA237 | 0x406707B4 | FULL | Memory buffer |
| SCB7_EZ_DATA238 | 0x406707B8 | FULL | Memory buffer |
| SCB7_EZ_DATA239 | 0x406707BC | FULL | Memory buffer |
| SCB7_EZ_DATA240 | 0x406707C0 | FULL | Memory buffer |
| SCB7_EZ_DATA241 | 0x406707C4 | FULL | Memory buffer |
| SCB7_EZ_DATA242 | 0x406707C8 | FULL | Memory buffer |
| SCB7_EZ_DATA243 | 0x406707CC | FULL | Memory buffer |
| SCB7_EZ_DATA244 | 0x406707D0 | FULL | Memory buffer |
| SCB7_EZ_DATA245 | 0x406707D4 | FULL | Memory buffer |
| SCB7_EZ_DATA246 | 0x406707D8 | FULL | Memory buffer |
| SCB7_EZ_DATA247 | 0x406707DC | FULL | Memory buffer |
| SCB7_EZ_DATA248 | 0x406707E0 | FULL | Memory buffer |
| SCB7_EZ_DATA249 | 0x406707E4 | FULL | Memory buffer |
| SCB7_EZ_DATA250 | 0x406707E8 | FULL | Memory buffer |
| SCB7_EZ_DATA251 | 0x406707EC | FULL | Memory buffer |
| SCB7_EZ_DATA252 | 0x406707F0 | FULL | Memory buffer |
| SCB7_EZ_DATA253 | 0x406707F4 | FULL | Memory buffer |
| SCB7_EZ_DATA254 | 0x406707F8 | FULL | Memory buffer |
| SCB7_EZ_DATA255 | 0x406707FC | FULL | Memory buffer |
| SCB7_INTR_CAUSE | 0x40670E00 | FULL | Active clocked interrupt signal<br>Note:I2C_EC is not available for this register |
| SCB7_INTR_SPI_EC | 0x40670EC0 | FULL | Externally clocked SPI interrupt request |
| SCB7_INTR_SPI_EC_MASK | 0x40670EC8 | FULL | Externally clocked SPI interrupt mask |
| SCB7_INTR_SPI_EC_MASKED | 0x40670ECC | FULL | Externally clocked SPI interrupt masked |
| SCB7_INTR_M | 0x40670F00 | FULL | Master interrupt request |
| SCB7_INTR_M_SET | 0x40670F04 | FULL | Master interrupt set request |
| SCB7_INTR_M_MASK | 0x40670F08 | FULL | Master interrupt mask |
| SCB7_INTR_M_MASKED | 0x40670F0C | FULL | Master interrupt masked request |
| SCB7_INTR_S | 0x40670F40 | FULL | Slave interrupt request |
| SCB7_INTR_S_SET | 0x40670F44 | FULL | Slave interrupt set request |
| SCB7_INTR_S_MASK | 0x40670F48 | FULL | Slave interrupt mask |
| SCB7_INTR_S_MASKED | 0x40670F4C | FULL | Slave interrupt masked request |
| SCB7_INTR_TX | 0x40670F80 | FULL | Transmitter interrupt request |
| SCB7_INTR_TX_SET | 0x40670F84 | FULL | Transmitter interrupt set request |
| SCB7_INTR_TX_MASK | 0x40670F88 | FULL | Transmitter interrupt mask |
| SCB7_INTR_TX_MASKED | 0x40670F8C | FULL | Transmitter interrupt masked request |
| SCB7_INTR_RX | 0x40670FC0 | FULL | Receiver interrupt request |
| SCB7_INTR_RX_SET | 0x40670FC4 | FULL | Receiver interrupt set request |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SCB7_INTR_RX_MASK | 0x40670FC8 | FULL | Receiver interrupt mask |
| SCB7_INTR_RX_MASKED | 0x40670FCC | FULL | Receiver interrupt masked request |

## 26.9 SCB 8

**Description** Serial Communications Block (SPI/UART/I2C)
**Base Address** 0x40680000
**Size** 0x10000
**Slave Num** MMIO6 - 8

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SCB8_CTRL | 0x40680000 | FULL | Generic control<br>Note:CMD_RESP_MODE is not available for this register |
| SCB8_STATUS | 0x40680004 | FULL | Generic status |
| SCB8_SPI_CTRL | 0x40680020 | FULL | SPI control |
| SCB8_SPI_STATUS | 0x40680024 | FULL | SPI status |
| SCB8_SPI_TX_CTRL | 0x40680028 | FULL | SPI transmitter control |
| SCB8_SPI_RX_CTRL | 0x4068002C | FULL | SPI receiver control |
| SCB8_UART_CTRL | 0x40680040 | FULL | UART control |
| SCB8_UART_TX_CTRL | 0x40680044 | FULL | UART transmitter control |
| SCB8_UART_RX_CTRL | 0x40680048 | FULL | UART receiver control |
| SCB8_UART_RX_STATUS | 0x4068004C | FULL | UART receiver status |
| SCB8_UART_FLOW_CTRL | 0x40680050 | FULL | UART flow control |
| SCB8_I2C_CTRL | 0x40680060 | FULL | I2C control |
| SCB8_I2C_STATUS | 0x40680064 | FULL | I2C status<br>Note:I2C_EC_BUSY is not available for this register |
| SCB8_I2C_M_CMD | 0x40680068 | FULL | I2C master command |
| SCB8_I2C_S_CMD | 0x4068006C | FULL | I2C slave command |
| SCB8_I2C_CFG | 0x40680070 | FULL | I2C configuration |
| SCB8_TX_CTRL | 0x40680200 | FULL | Transmitter control |
| SCB8_TX_FIFO_CTRL | 0x40680204 | FULL | Transmitter FIFO control |
| SCB8_TX_FIFO_STATUS | 0x40680208 | FULL | Transmitter FIFO status |
| SCB8_TX_FIFO_WR | 0x40680240 | FULL | Transmitter FIFO write |
| SCB8_RX_CTRL | 0x40680300 | FULL | Receiver control |
| SCB8_RX_FIFO_CTRL | 0x40680304 | FULL | Receiver FIFO control |
| SCB8_RX_FIFO_STATUS | 0x40680308 | FULL | Receiver FIFO status |
| SCB8_RX_MATCH | 0x40680310 | FULL | Slave address and mask |
| SCB8_RX_FIFO_RD | 0x40680340 | FULL | Receiver FIFO read |
| SCB8_RX_FIFO_RD_SILENT | 0x40680344 | FULL | Receiver FIFO read silent |
| SCB8_EZ_DATA0 | 0x40680400 | FULL | Memory buffer |
| SCB8_EZ_DATA1 | 0x40680404 | FULL | Memory buffer |
| SCB8_EZ_DATA2 | 0x40680408 | FULL | Memory buffer |
| SCB8_EZ_DATA3 | 0x4068040C | FULL | Memory buffer |
| SCB8_EZ_DATA4 | 0x40680410 | FULL | Memory buffer |
| SCB8_EZ_DATA5 | 0x40680414 | FULL | Memory buffer |
| SCB8_EZ_DATA6 | 0x40680418 | FULL | Memory buffer |
| SCB8_EZ_DATA7 | 0x4068041C | FULL | Memory buffer |
| SCB8_EZ_DATA8 | 0x40680420 | FULL | Memory buffer |
| SCB8_EZ_DATA9 | 0x40680424 | FULL | Memory buffer |
| SCB8_EZ_DATA10 | 0x40680428 | FULL | Memory buffer |
| SCB8_EZ_DATA11 | 0x4068042C | FULL | Memory buffer |
| SCB8_EZ_DATA12 | 0x40680430 | FULL | Memory buffer |
| SCB8_EZ_DATA13 | 0x40680434 | FULL | Memory buffer |
| SCB8_EZ_DATA14 | 0x40680438 | FULL | Memory buffer |
| SCB8_EZ_DATA15 | 0x4068043C | FULL | Memory buffer |
| SCB8_EZ_DATA16 | 0x40680440 | FULL | Memory buffer |
| SCB8_EZ_DATA17 | 0x40680444 | FULL | Memory buffer |
| SCB8_EZ_DATA18 | 0x40680448 | FULL | Memory buffer |
| SCB8_EZ_DATA19 | 0x4068044C | FULL | Memory buffer |
| SCB8_EZ_DATA20 | 0x40680450 | FULL | Memory buffer |
| SCB8_EZ_DATA21 | 0x40680454 | FULL | Memory buffer |
| SCB8_EZ_DATA22 | 0x40680458 | FULL | Memory buffer |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SCB8_EZ_DATA23 | 0x4068045C | FULL | Memory buffer |
| SCB8_EZ_DATA24 | 0x40680460 | FULL | Memory buffer |
| SCB8_EZ_DATA25 | 0x40680464 | FULL | Memory buffer |
| SCB8_EZ_DATA26 | 0x40680468 | FULL | Memory buffer |
| SCB8_EZ_DATA27 | 0x4068046C | FULL | Memory buffer |
| SCB8_EZ_DATA28 | 0x40680470 | FULL | Memory buffer |
| SCB8_EZ_DATA29 | 0x40680474 | FULL | Memory buffer |
| SCB8_EZ_DATA30 | 0x40680478 | FULL | Memory buffer |
| SCB8_EZ_DATA31 | 0x4068047C | FULL | Memory buffer |
| SCB8_EZ_DATA32 | 0x40680480 | FULL | Memory buffer |
| SCB8_EZ_DATA33 | 0x40680484 | FULL | Memory buffer |
| SCB8_EZ_DATA34 | 0x40680488 | FULL | Memory buffer |
| SCB8_EZ_DATA35 | 0x4068048C | FULL | Memory buffer |
| SCB8_EZ_DATA36 | 0x40680490 | FULL | Memory buffer |
| SCB8_EZ_DATA37 | 0x40680494 | FULL | Memory buffer |
| SCB8_EZ_DATA38 | 0x40680498 | FULL | Memory buffer |
| SCB8_EZ_DATA39 | 0x4068049C | FULL | Memory buffer |
| SCB8_EZ_DATA40 | 0x406804A0 | FULL | Memory buffer |
| SCB8_EZ_DATA41 | 0x406804A4 | FULL | Memory buffer |
| SCB8_EZ_DATA42 | 0x406804A8 | FULL | Memory buffer |
| SCB8_EZ_DATA43 | 0x406804AC | FULL | Memory buffer |
| SCB8_EZ_DATA44 | 0x406804B0 | FULL | Memory buffer |
| SCB8_EZ_DATA45 | 0x406804B4 | FULL | Memory buffer |
| SCB8_EZ_DATA46 | 0x406804B8 | FULL | Memory buffer |
| SCB8_EZ_DATA47 | 0x406804BC | FULL | Memory buffer |
| SCB8_EZ_DATA48 | 0x406804C0 | FULL | Memory buffer |
| SCB8_EZ_DATA49 | 0x406804C4 | FULL | Memory buffer |
| SCB8_EZ_DATA50 | 0x406804C8 | FULL | Memory buffer |
| SCB8_EZ_DATA51 | 0x406804CC | FULL | Memory buffer |
| SCB8_EZ_DATA52 | 0x406804D0 | FULL | Memory buffer |
| SCB8_EZ_DATA53 | 0x406804D4 | FULL | Memory buffer |
| SCB8_EZ_DATA54 | 0x406804D8 | FULL | Memory buffer |
| SCB8_EZ_DATA55 | 0x406804DC | FULL | Memory buffer |
| SCB8_EZ_DATA56 | 0x406804E0 | FULL | Memory buffer |
| SCB8_EZ_DATA57 | 0x406804E4 | FULL | Memory buffer |
| SCB8_EZ_DATA58 | 0x406804E8 | FULL | Memory buffer |
| SCB8_EZ_DATA59 | 0x406804EC | FULL | Memory buffer |
| SCB8_EZ_DATA60 | 0x406804F0 | FULL | Memory buffer |
| SCB8_EZ_DATA61 | 0x406804F4 | FULL | Memory buffer |
| SCB8_EZ_DATA62 | 0x406804F8 | FULL | Memory buffer |
| SCB8_EZ_DATA63 | 0x406804FC | FULL | Memory buffer |
| SCB8_EZ_DATA64 | 0x40680500 | FULL | Memory buffer |
| SCB8_EZ_DATA65 | 0x40680504 | FULL | Memory buffer |
| SCB8_EZ_DATA66 | 0x40680508 | FULL | Memory buffer |
| SCB8_EZ_DATA67 | 0x4068050C | FULL | Memory buffer |
| SCB8_EZ_DATA68 | 0x40680510 | FULL | Memory buffer |
| SCB8_EZ_DATA69 | 0x40680514 | FULL | Memory buffer |
| SCB8_EZ_DATA70 | 0x40680518 | FULL | Memory buffer |
| SCB8_EZ_DATA71 | 0x4068051C | FULL | Memory buffer |
| SCB8_EZ_DATA72 | 0x40680520 | FULL | Memory buffer |
| SCB8_EZ_DATA73 | 0x40680524 | FULL | Memory buffer |
| SCB8_EZ_DATA74 | 0x40680528 | FULL | Memory buffer |
| SCB8_EZ_DATA75 | 0x4068052C | FULL | Memory buffer |
| SCB8_EZ_DATA76 | 0x40680530 | FULL | Memory buffer |
| SCB8_EZ_DATA77 | 0x40680534 | FULL | Memory buffer |
| SCB8_EZ_DATA78 | 0x40680538 | FULL | Memory buffer |
| SCB8_EZ_DATA79 | 0x4068053C | FULL | Memory buffer |
| SCB8_EZ_DATA80 | 0x40680540 | FULL | Memory buffer |
| SCB8_EZ_DATA81 | 0x40680544 | FULL | Memory buffer |
| SCB8_EZ_DATA82 | 0x40680548 | FULL | Memory buffer |
| SCB8_EZ_DATA83 | 0x4068054C | FULL | Memory buffer |
| SCB8_EZ_DATA84 | 0x40680550 | FULL | Memory buffer |
| SCB8_EZ_DATA85 | 0x40680554 | FULL | Memory buffer |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SCB8_EZ_DATA86 | 0x40680558 | FULL | Memory buffer |
| SCB8_EZ_DATA87 | 0x4068055C | FULL | Memory buffer |
| SCB8_EZ_DATA88 | 0x40680560 | FULL | Memory buffer |
| SCB8_EZ_DATA89 | 0x40680564 | FULL | Memory buffer |
| SCB8_EZ_DATA90 | 0x40680568 | FULL | Memory buffer |
| SCB8_EZ_DATA91 | 0x4068056C | FULL | Memory buffer |
| SCB8_EZ_DATA92 | 0x40680570 | FULL | Memory buffer |
| SCB8_EZ_DATA93 | 0x40680574 | FULL | Memory buffer |
| SCB8_EZ_DATA94 | 0x40680578 | FULL | Memory buffer |
| SCB8_EZ_DATA95 | 0x4068057C | FULL | Memory buffer |
| SCB8_EZ_DATA96 | 0x40680580 | FULL | Memory buffer |
| SCB8_EZ_DATA97 | 0x40680584 | FULL | Memory buffer |
| SCB8_EZ_DATA98 | 0x40680588 | FULL | Memory buffer |
| SCB8_EZ_DATA99 | 0x4068058C | FULL | Memory buffer |
| SCB8_EZ_DATA100 | 0x40680590 | FULL | Memory buffer |
| SCB8_EZ_DATA101 | 0x40680594 | FULL | Memory buffer |
| SCB8_EZ_DATA102 | 0x40680598 | FULL | Memory buffer |
| SCB8_EZ_DATA103 | 0x4068059C | FULL | Memory buffer |
| SCB8_EZ_DATA104 | 0x406805A0 | FULL | Memory buffer |
| SCB8_EZ_DATA105 | 0x406805A4 | FULL | Memory buffer |
| SCB8_EZ_DATA106 | 0x406805A8 | FULL | Memory buffer |
| SCB8_EZ_DATA107 | 0x406805AC | FULL | Memory buffer |
| SCB8_EZ_DATA108 | 0x406805B0 | FULL | Memory buffer |
| SCB8_EZ_DATA109 | 0x406805B4 | FULL | Memory buffer |
| SCB8_EZ_DATA110 | 0x406805B8 | FULL | Memory buffer |
| SCB8_EZ_DATA111 | 0x406805BC | FULL | Memory buffer |
| SCB8_EZ_DATA112 | 0x406805C0 | FULL | Memory buffer |
| SCB8_EZ_DATA113 | 0x406805C4 | FULL | Memory buffer |
| SCB8_EZ_DATA114 | 0x406805C8 | FULL | Memory buffer |
| SCB8_EZ_DATA115 | 0x406805CC | FULL | Memory buffer |
| SCB8_EZ_DATA116 | 0x406805D0 | FULL | Memory buffer |
| SCB8_EZ_DATA117 | 0x406805D4 | FULL | Memory buffer |
| SCB8_EZ_DATA118 | 0x406805D8 | FULL | Memory buffer |
| SCB8_EZ_DATA119 | 0x406805DC | FULL | Memory buffer |
| SCB8_EZ_DATA120 | 0x406805E0 | FULL | Memory buffer |
| SCB8_EZ_DATA121 | 0x406805E4 | FULL | Memory buffer |
| SCB8_EZ_DATA122 | 0x406805E8 | FULL | Memory buffer |
| SCB8_EZ_DATA123 | 0x406805EC | FULL | Memory buffer |
| SCB8_EZ_DATA124 | 0x406805F0 | FULL | Memory buffer |
| SCB8_EZ_DATA125 | 0x406805F4 | FULL | Memory buffer |
| SCB8_EZ_DATA126 | 0x406805F8 | FULL | Memory buffer |
| SCB8_EZ_DATA127 | 0x406805FC | FULL | Memory buffer |
| SCB8_EZ_DATA128 | 0x40680600 | FULL | Memory buffer |
| SCB8_EZ_DATA129 | 0x40680604 | FULL | Memory buffer |
| SCB8_EZ_DATA130 | 0x40680608 | FULL | Memory buffer |
| SCB8_EZ_DATA131 | 0x4068060C | FULL | Memory buffer |
| SCB8_EZ_DATA132 | 0x40680610 | FULL | Memory buffer |
| SCB8_EZ_DATA133 | 0x40680614 | FULL | Memory buffer |
| SCB8_EZ_DATA134 | 0x40680618 | FULL | Memory buffer |
| SCB8_EZ_DATA135 | 0x4068061C | FULL | Memory buffer |
| SCB8_EZ_DATA136 | 0x40680620 | FULL | Memory buffer |
| SCB8_EZ_DATA137 | 0x40680624 | FULL | Memory buffer |
| SCB8_EZ_DATA138 | 0x40680628 | FULL | Memory buffer |
| SCB8_EZ_DATA139 | 0x4068062C | FULL | Memory buffer |
| SCB8_EZ_DATA140 | 0x40680630 | FULL | Memory buffer |
| SCB8_EZ_DATA141 | 0x40680634 | FULL | Memory buffer |
| SCB8_EZ_DATA142 | 0x40680638 | FULL | Memory buffer |
| SCB8_EZ_DATA143 | 0x4068063C | FULL | Memory buffer |
| SCB8_EZ_DATA144 | 0x40680640 | FULL | Memory buffer |
| SCB8_EZ_DATA145 | 0x40680644 | FULL | Memory buffer |
| SCB8_EZ_DATA146 | 0x40680648 | FULL | Memory buffer |
| SCB8_EZ_DATA147 | 0x4068064C | FULL | Memory buffer |
| SCB8_EZ_DATA148 | 0x40680650 | FULL | Memory buffer |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SCB8_EZ_DATA149 | 0x40680654 | FULL | Memory buffer |
| SCB8_EZ_DATA150 | 0x40680658 | FULL | Memory buffer |
| SCB8_EZ_DATA151 | 0x4068065C | FULL | Memory buffer |
| SCB8_EZ_DATA152 | 0x40680660 | FULL | Memory buffer |
| SCB8_EZ_DATA153 | 0x40680664 | FULL | Memory buffer |
| SCB8_EZ_DATA154 | 0x40680668 | FULL | Memory buffer |
| SCB8_EZ_DATA155 | 0x4068066C | FULL | Memory buffer |
| SCB8_EZ_DATA156 | 0x40680670 | FULL | Memory buffer |
| SCB8_EZ_DATA157 | 0x40680674 | FULL | Memory buffer |
| SCB8_EZ_DATA158 | 0x40680678 | FULL | Memory buffer |
| SCB8_EZ_DATA159 | 0x4068067C | FULL | Memory buffer |
| SCB8_EZ_DATA160 | 0x40680680 | FULL | Memory buffer |
| SCB8_EZ_DATA161 | 0x40680684 | FULL | Memory buffer |
| SCB8_EZ_DATA162 | 0x40680688 | FULL | Memory buffer |
| SCB8_EZ_DATA163 | 0x4068068C | FULL | Memory buffer |
| SCB8_EZ_DATA164 | 0x40680690 | FULL | Memory buffer |
| SCB8_EZ_DATA165 | 0x40680694 | FULL | Memory buffer |
| SCB8_EZ_DATA166 | 0x40680698 | FULL | Memory buffer |
| SCB8_EZ_DATA167 | 0x4068069C | FULL | Memory buffer |
| SCB8_EZ_DATA168 | 0x406806A0 | FULL | Memory buffer |
| SCB8_EZ_DATA169 | 0x406806A4 | FULL | Memory buffer |
| SCB8_EZ_DATA170 | 0x406806A8 | FULL | Memory buffer |
| SCB8_EZ_DATA171 | 0x406806AC | FULL | Memory buffer |
| SCB8_EZ_DATA172 | 0x406806B0 | FULL | Memory buffer |
| SCB8_EZ_DATA173 | 0x406806B4 | FULL | Memory buffer |
| SCB8_EZ_DATA174 | 0x406806B8 | FULL | Memory buffer |
| SCB8_EZ_DATA175 | 0x406806BC | FULL | Memory buffer |
| SCB8_EZ_DATA176 | 0x406806C0 | FULL | Memory buffer |
| SCB8_EZ_DATA177 | 0x406806C4 | FULL | Memory buffer |
| SCB8_EZ_DATA178 | 0x406806C8 | FULL | Memory buffer |
| SCB8_EZ_DATA179 | 0x406806CC | FULL | Memory buffer |
| SCB8_EZ_DATA180 | 0x406806D0 | FULL | Memory buffer |
| SCB8_EZ_DATA181 | 0x406806D4 | FULL | Memory buffer |
| SCB8_EZ_DATA182 | 0x406806D8 | FULL | Memory buffer |
| SCB8_EZ_DATA183 | 0x406806DC | FULL | Memory buffer |
| SCB8_EZ_DATA184 | 0x406806E0 | FULL | Memory buffer |
| SCB8_EZ_DATA185 | 0x406806E4 | FULL | Memory buffer |
| SCB8_EZ_DATA186 | 0x406806E8 | FULL | Memory buffer |
| SCB8_EZ_DATA187 | 0x406806EC | FULL | Memory buffer |
| SCB8_EZ_DATA188 | 0x406806F0 | FULL | Memory buffer |
| SCB8_EZ_DATA189 | 0x406806F4 | FULL | Memory buffer |
| SCB8_EZ_DATA190 | 0x406806F8 | FULL | Memory buffer |
| SCB8_EZ_DATA191 | 0x406806FC | FULL | Memory buffer |
| SCB8_EZ_DATA192 | 0x40680700 | FULL | Memory buffer |
| SCB8_EZ_DATA193 | 0x40680704 | FULL | Memory buffer |
| SCB8_EZ_DATA194 | 0x40680708 | FULL | Memory buffer |
| SCB8_EZ_DATA195 | 0x4068070C | FULL | Memory buffer |
| SCB8_EZ_DATA196 | 0x40680710 | FULL | Memory buffer |
| SCB8_EZ_DATA197 | 0x40680714 | FULL | Memory buffer |
| SCB8_EZ_DATA198 | 0x40680718 | FULL | Memory buffer |
| SCB8_EZ_DATA199 | 0x4068071C | FULL | Memory buffer |
| SCB8_EZ_DATA200 | 0x40680720 | FULL | Memory buffer |
| SCB8_EZ_DATA201 | 0x40680724 | FULL | Memory buffer |
| SCB8_EZ_DATA202 | 0x40680728 | FULL | Memory buffer |
| SCB8_EZ_DATA203 | 0x4068072C | FULL | Memory buffer |
| SCB8_EZ_DATA204 | 0x40680730 | FULL | Memory buffer |
| SCB8_EZ_DATA205 | 0x40680734 | FULL | Memory buffer |
| SCB8_EZ_DATA206 | 0x40680738 | FULL | Memory buffer |
| SCB8_EZ_DATA207 | 0x4068073C | FULL | Memory buffer |
| SCB8_EZ_DATA208 | 0x40680740 | FULL | Memory buffer |
| SCB8_EZ_DATA209 | 0x40680744 | FULL | Memory buffer |
| SCB8_EZ_DATA210 | 0x40680748 | FULL | Memory buffer |
| SCB8_EZ_DATA211 | 0x4068074C | FULL | Memory buffer |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SCB8_EZ_DATA212 | 0x40680750 | FULL | Memory buffer |
| SCB8_EZ_DATA213 | 0x40680754 | FULL | Memory buffer |
| SCB8_EZ_DATA214 | 0x40680758 | FULL | Memory buffer |
| SCB8_EZ_DATA215 | 0x4068075C | FULL | Memory buffer |
| SCB8_EZ_DATA216 | 0x40680760 | FULL | Memory buffer |
| SCB8_EZ_DATA217 | 0x40680764 | FULL | Memory buffer |
| SCB8_EZ_DATA218 | 0x40680768 | FULL | Memory buffer |
| SCB8_EZ_DATA219 | 0x4068076C | FULL | Memory buffer |
| SCB8_EZ_DATA220 | 0x40680770 | FULL | Memory buffer |
| SCB8_EZ_DATA221 | 0x40680774 | FULL | Memory buffer |
| SCB8_EZ_DATA222 | 0x40680778 | FULL | Memory buffer |
| SCB8_EZ_DATA223 | 0x4068077C | FULL | Memory buffer |
| SCB8_EZ_DATA224 | 0x40680780 | FULL | Memory buffer |
| SCB8_EZ_DATA225 | 0x40680784 | FULL | Memory buffer |
| SCB8_EZ_DATA226 | 0x40680788 | FULL | Memory buffer |
| SCB8_EZ_DATA227 | 0x4068078C | FULL | Memory buffer |
| SCB8_EZ_DATA228 | 0x40680790 | FULL | Memory buffer |
| SCB8_EZ_DATA229 | 0x40680794 | FULL | Memory buffer |
| SCB8_EZ_DATA230 | 0x40680798 | FULL | Memory buffer |
| SCB8_EZ_DATA231 | 0x4068079C | FULL | Memory buffer |
| SCB8_EZ_DATA232 | 0x406807A0 | FULL | Memory buffer |
| SCB8_EZ_DATA233 | 0x406807A4 | FULL | Memory buffer |
| SCB8_EZ_DATA234 | 0x406807A8 | FULL | Memory buffer |
| SCB8_EZ_DATA235 | 0x406807AC | FULL | Memory buffer |
| SCB8_EZ_DATA236 | 0x406807B0 | FULL | Memory buffer |
| SCB8_EZ_DATA237 | 0x406807B4 | FULL | Memory buffer |
| SCB8_EZ_DATA238 | 0x406807B8 | FULL | Memory buffer |
| SCB8_EZ_DATA239 | 0x406807BC | FULL | Memory buffer |
| SCB8_EZ_DATA240 | 0x406807C0 | FULL | Memory buffer |
| SCB8_EZ_DATA241 | 0x406807C4 | FULL | Memory buffer |
| SCB8_EZ_DATA242 | 0x406807C8 | FULL | Memory buffer |
| SCB8_EZ_DATA243 | 0x406807CC | FULL | Memory buffer |
| SCB8_EZ_DATA244 | 0x406807D0 | FULL | Memory buffer |
| SCB8_EZ_DATA245 | 0x406807D4 | FULL | Memory buffer |
| SCB8_EZ_DATA246 | 0x406807D8 | FULL | Memory buffer |
| SCB8_EZ_DATA247 | 0x406807DC | FULL | Memory buffer |
| SCB8_EZ_DATA248 | 0x406807E0 | FULL | Memory buffer |
| SCB8_EZ_DATA249 | 0x406807E4 | FULL | Memory buffer |
| SCB8_EZ_DATA250 | 0x406807E8 | FULL | Memory buffer |
| SCB8_EZ_DATA251 | 0x406807EC | FULL | Memory buffer |
| SCB8_EZ_DATA252 | 0x406807F0 | FULL | Memory buffer |
| SCB8_EZ_DATA253 | 0x406807F4 | FULL | Memory buffer |
| SCB8_EZ_DATA254 | 0x406807F8 | FULL | Memory buffer |
| SCB8_EZ_DATA255 | 0x406807FC | FULL | Memory buffer |
| SCB8_INTR_CAUSE | 0x40680E00 | FULL | Active clocked interrupt signal<br>Note:I2C_EC is not available for this register |
| SCB8_INTR_SPI_EC | 0x40680EC0 | FULL | Externally clocked SPI interrupt request |
| SCB8_INTR_SPI_EC_MASK | 0x40680EC8 | FULL | Externally clocked SPI interrupt mask |
| SCB8_INTR_SPI_EC_MASKED | 0x40680ECC | FULL | Externally clocked SPI interrupt masked |
| SCB8_INTR_M | 0x40680F00 | FULL | Master interrupt request |
| SCB8_INTR_M_SET | 0x40680F04 | FULL | Master interrupt set request |
| SCB8_INTR_M_MASK | 0x40680F08 | FULL | Master interrupt mask |
| SCB8_INTR_M_MASKED | 0x40680F0C | FULL | Master interrupt masked request |
| SCB8_INTR_S | 0x40680F40 | FULL | Slave interrupt request |
| SCB8_INTR_S_SET | 0x40680F44 | FULL | Slave interrupt set request |
| SCB8_INTR_S_MASK | 0x40680F48 | FULL | Slave interrupt mask |
| SCB8_INTR_S_MASKED | 0x40680F4C | FULL | Slave interrupt masked request |
| SCB8_INTR_TX | 0x40680F80 | FULL | Transmitter interrupt request |
| SCB8_INTR_TX_SET | 0x40680F84 | FULL | Transmitter interrupt set request |
| SCB8_INTR_TX_MASK | 0x40680F88 | FULL | Transmitter interrupt mask |
| SCB8_INTR_TX_MASKED | 0x40680F8C | FULL | Transmitter interrupt masked request |
| SCB8_INTR_RX | 0x40680FC0 | FULL | Receiver interrupt request |
| SCB8_INTR_RX_SET | 0x40680FC4 | FULL | Receiver interrupt set request |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SCB8_INTR_RX_MASK | 0x40680FC8 | FULL | Receiver interrupt mask |
| SCB8_INTR_RX_MASKED | 0x40680FCC | FULL | Receiver interrupt masked request |

## 26.10 SCB 9

**Description** Serial Communications Block (SPI/UART/I2C)
**Base Address** 0x40690000
**Size** 0x10000
**Slave Num** MMIO6 - 9

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SCB9_CTRL | 0x40690000 | FULL | Generic control<br>Note:CMD_RESP_MODE is not available for this register |
| SCB9_STATUS | 0x40690004 | FULL | Generic status |
| SCB9_SPI_CTRL | 0x40690020 | FULL | SPI control |
| SCB9_SPI_STATUS | 0x40690024 | FULL | SPI status |
| SCB9_SPI_TX_CTRL | 0x40690028 | FULL | SPI transmitter control |
| SCB9_SPI_RX_CTRL | 0x4069002C | FULL | SPI receiver control |
| SCB9_UART_CTRL | 0x40690040 | FULL | UART control |
| SCB9_UART_TX_CTRL | 0x40690044 | FULL | UART transmitter control |
| SCB9_UART_RX_CTRL | 0x40690048 | FULL | UART receiver control |
| SCB9_UART_RX_STATUS | 0x4069004C | FULL | UART receiver status |
| SCB9_UART_FLOW_CTRL | 0x40690050 | FULL | UART flow control |
| SCB9_I2C_CTRL | 0x40690060 | FULL | I2C control |
| SCB9_I2C_STATUS | 0x40690064 | FULL | I2C status<br>Note:I2C_EC_BUSY is not available for this register |
| SCB9_I2C_M_CMD | 0x40690068 | FULL | I2C master command |
| SCB9_I2C_S_CMD | 0x4069006C | FULL | I2C slave command |
| SCB9_I2C_CFG | 0x40690070 | FULL | I2C configuration |
| SCB9_TX_CTRL | 0x40690200 | FULL | Transmitter control |
| SCB9_TX_FIFO_CTRL | 0x40690204 | FULL | Transmitter FIFO control |
| SCB9_TX_FIFO_STATUS | 0x40690208 | FULL | Transmitter FIFO status |
| SCB9_TX_FIFO_WR | 0x40690240 | FULL | Transmitter FIFO write |
| SCB9_RX_CTRL | 0x40690300 | FULL | Receiver control |
| SCB9_RX_FIFO_CTRL | 0x40690304 | FULL | Receiver FIFO control |
| SCB9_RX_FIFO_STATUS | 0x40690308 | FULL | Receiver FIFO status |
| SCB9_RX_MATCH | 0x40690310 | FULL | Slave address and mask |
| SCB9_RX_FIFO_RD | 0x40690340 | FULL | Receiver FIFO read |
| SCB9_RX_FIFO_RD_SILENT | 0x40690344 | FULL | Receiver FIFO read silent |
| SCB9_EZ_DATA0 | 0x40690400 | FULL | Memory buffer |
| SCB9_EZ_DATA1 | 0x40690404 | FULL | Memory buffer |
| SCB9_EZ_DATA2 | 0x40690408 | FULL | Memory buffer |
| SCB9_EZ_DATA3 | 0x4069040C | FULL | Memory buffer |
| SCB9_EZ_DATA4 | 0x40690410 | FULL | Memory buffer |
| SCB9_EZ_DATA5 | 0x40690414 | FULL | Memory buffer |
| SCB9_EZ_DATA6 | 0x40690418 | FULL | Memory buffer |
| SCB9_EZ_DATA7 | 0x4069041C | FULL | Memory buffer |
| SCB9_EZ_DATA8 | 0x40690420 | FULL | Memory buffer |
| SCB9_EZ_DATA9 | 0x40690424 | FULL | Memory buffer |
| SCB9_EZ_DATA10 | 0x40690428 | FULL | Memory buffer |
| SCB9_EZ_DATA11 | 0x4069042C | FULL | Memory buffer |
| SCB9_EZ_DATA12 | 0x40690430 | FULL | Memory buffer |
| SCB9_EZ_DATA13 | 0x40690434 | FULL | Memory buffer |
| SCB9_EZ_DATA14 | 0x40690438 | FULL | Memory buffer |
| SCB9_EZ_DATA15 | 0x4069043C | FULL | Memory buffer |
| SCB9_EZ_DATA16 | 0x40690440 | FULL | Memory buffer |
| SCB9_EZ_DATA17 | 0x40690444 | FULL | Memory buffer |
| SCB9_EZ_DATA18 | 0x40690448 | FULL | Memory buffer |
| SCB9_EZ_DATA19 | 0x4069044C | FULL | Memory buffer |
| SCB9_EZ_DATA20 | 0x40690450 | FULL | Memory buffer |
| SCB9_EZ_DATA21 | 0x40690454 | FULL | Memory buffer |
| SCB9_EZ_DATA22 | 0x40690458 | FULL | Memory buffer |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SCB9_EZ_DATA23 | 0x4069045C | FULL | Memory buffer |
| SCB9_EZ_DATA24 | 0x40690460 | FULL | Memory buffer |
| SCB9_EZ_DATA25 | 0x40690464 | FULL | Memory buffer |
| SCB9_EZ_DATA26 | 0x40690468 | FULL | Memory buffer |
| SCB9_EZ_DATA27 | 0x4069046C | FULL | Memory buffer |
| SCB9_EZ_DATA28 | 0x40690470 | FULL | Memory buffer |
| SCB9_EZ_DATA29 | 0x40690474 | FULL | Memory buffer |
| SCB9_EZ_DATA30 | 0x40690478 | FULL | Memory buffer |
| SCB9_EZ_DATA31 | 0x4069047C | FULL | Memory buffer |
| SCB9_EZ_DATA32 | 0x40690480 | FULL | Memory buffer |
| SCB9_EZ_DATA33 | 0x40690484 | FULL | Memory buffer |
| SCB9_EZ_DATA34 | 0x40690488 | FULL | Memory buffer |
| SCB9_EZ_DATA35 | 0x4069048C | FULL | Memory buffer |
| SCB9_EZ_DATA36 | 0x40690490 | FULL | Memory buffer |
| SCB9_EZ_DATA37 | 0x40690494 | FULL | Memory buffer |
| SCB9_EZ_DATA38 | 0x40690498 | FULL | Memory buffer |
| SCB9_EZ_DATA39 | 0x4069049C | FULL | Memory buffer |
| SCB9_EZ_DATA40 | 0x406904A0 | FULL | Memory buffer |
| SCB9_EZ_DATA41 | 0x406904A4 | FULL | Memory buffer |
| SCB9_EZ_DATA42 | 0x406904A8 | FULL | Memory buffer |
| SCB9_EZ_DATA43 | 0x406904AC | FULL | Memory buffer |
| SCB9_EZ_DATA44 | 0x406904B0 | FULL | Memory buffer |
| SCB9_EZ_DATA45 | 0x406904B4 | FULL | Memory buffer |
| SCB9_EZ_DATA46 | 0x406904B8 | FULL | Memory buffer |
| SCB9_EZ_DATA47 | 0x406904BC | FULL | Memory buffer |
| SCB9_EZ_DATA48 | 0x406904C0 | FULL | Memory buffer |
| SCB9_EZ_DATA49 | 0x406904C4 | FULL | Memory buffer |
| SCB9_EZ_DATA50 | 0x406904C8 | FULL | Memory buffer |
| SCB9_EZ_DATA51 | 0x406904CC | FULL | Memory buffer |
| SCB9_EZ_DATA52 | 0x406904D0 | FULL | Memory buffer |
| SCB9_EZ_DATA53 | 0x406904D4 | FULL | Memory buffer |
| SCB9_EZ_DATA54 | 0x406904D8 | FULL | Memory buffer |
| SCB9_EZ_DATA55 | 0x406904DC | FULL | Memory buffer |
| SCB9_EZ_DATA56 | 0x406904E0 | FULL | Memory buffer |
| SCB9_EZ_DATA57 | 0x406904E4 | FULL | Memory buffer |
| SCB9_EZ_DATA58 | 0x406904E8 | FULL | Memory buffer |
| SCB9_EZ_DATA59 | 0x406904EC | FULL | Memory buffer |
| SCB9_EZ_DATA60 | 0x406904F0 | FULL | Memory buffer |
| SCB9_EZ_DATA61 | 0x406904F4 | FULL | Memory buffer |
| SCB9_EZ_DATA62 | 0x406904F8 | FULL | Memory buffer |
| SCB9_EZ_DATA63 | 0x406904FC | FULL | Memory buffer |
| SCB9_EZ_DATA64 | 0x40690500 | FULL | Memory buffer |
| SCB9_EZ_DATA65 | 0x40690504 | FULL | Memory buffer |
| SCB9_EZ_DATA66 | 0x40690508 | FULL | Memory buffer |
| SCB9_EZ_DATA67 | 0x4069050C | FULL | Memory buffer |
| SCB9_EZ_DATA68 | 0x40690510 | FULL | Memory buffer |
| SCB9_EZ_DATA69 | 0x40690514 | FULL | Memory buffer |
| SCB9_EZ_DATA70 | 0x40690518 | FULL | Memory buffer |
| SCB9_EZ_DATA71 | 0x4069051C | FULL | Memory buffer |
| SCB9_EZ_DATA72 | 0x40690520 | FULL | Memory buffer |
| SCB9_EZ_DATA73 | 0x40690524 | FULL | Memory buffer |
| SCB9_EZ_DATA74 | 0x40690528 | FULL | Memory buffer |
| SCB9_EZ_DATA75 | 0x4069052C | FULL | Memory buffer |
| SCB9_EZ_DATA76 | 0x40690530 | FULL | Memory buffer |
| SCB9_EZ_DATA77 | 0x40690534 | FULL | Memory buffer |
| SCB9_EZ_DATA78 | 0x40690538 | FULL | Memory buffer |
| SCB9_EZ_DATA79 | 0x4069053C | FULL | Memory buffer |
| SCB9_EZ_DATA80 | 0x40690540 | FULL | Memory buffer |
| SCB9_EZ_DATA81 | 0x40690544 | FULL | Memory buffer |
| SCB9_EZ_DATA82 | 0x40690548 | FULL | Memory buffer |
| SCB9_EZ_DATA83 | 0x4069054C | FULL | Memory buffer |
| SCB9_EZ_DATA84 | 0x40690550 | FULL | Memory buffer |
| SCB9_EZ_DATA85 | 0x40690554 | FULL | Memory buffer |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SCB9_EZ_DATA86 | 0x40690558 | FULL | Memory buffer |
| SCB9_EZ_DATA87 | 0x4069055C | FULL | Memory buffer |
| SCB9_EZ_DATA88 | 0x40690560 | FULL | Memory buffer |
| SCB9_EZ_DATA89 | 0x40690564 | FULL | Memory buffer |
| SCB9_EZ_DATA90 | 0x40690568 | FULL | Memory buffer |
| SCB9_EZ_DATA91 | 0x4069056C | FULL | Memory buffer |
| SCB9_EZ_DATA92 | 0x40690570 | FULL | Memory buffer |
| SCB9_EZ_DATA93 | 0x40690574 | FULL | Memory buffer |
| SCB9_EZ_DATA94 | 0x40690578 | FULL | Memory buffer |
| SCB9_EZ_DATA95 | 0x4069057C | FULL | Memory buffer |
| SCB9_EZ_DATA96 | 0x40690580 | FULL | Memory buffer |
| SCB9_EZ_DATA97 | 0x40690584 | FULL | Memory buffer |
| SCB9_EZ_DATA98 | 0x40690588 | FULL | Memory buffer |
| SCB9_EZ_DATA99 | 0x4069058C | FULL | Memory buffer |
| SCB9_EZ_DATA100 | 0x40690590 | FULL | Memory buffer |
| SCB9_EZ_DATA101 | 0x40690594 | FULL | Memory buffer |
| SCB9_EZ_DATA102 | 0x40690598 | FULL | Memory buffer |
| SCB9_EZ_DATA103 | 0x4069059C | FULL | Memory buffer |
| SCB9_EZ_DATA104 | 0x406905A0 | FULL | Memory buffer |
| SCB9_EZ_DATA105 | 0x406905A4 | FULL | Memory buffer |
| SCB9_EZ_DATA106 | 0x406905A8 | FULL | Memory buffer |
| SCB9_EZ_DATA107 | 0x406905AC | FULL | Memory buffer |
| SCB9_EZ_DATA108 | 0x406905B0 | FULL | Memory buffer |
| SCB9_EZ_DATA109 | 0x406905B4 | FULL | Memory buffer |
| SCB9_EZ_DATA110 | 0x406905B8 | FULL | Memory buffer |
| SCB9_EZ_DATA111 | 0x406905BC | FULL | Memory buffer |
| SCB9_EZ_DATA112 | 0x406905C0 | FULL | Memory buffer |
| SCB9_EZ_DATA113 | 0x406905C4 | FULL | Memory buffer |
| SCB9_EZ_DATA114 | 0x406905C8 | FULL | Memory buffer |
| SCB9_EZ_DATA115 | 0x406905CC | FULL | Memory buffer |
| SCB9_EZ_DATA116 | 0x406905D0 | FULL | Memory buffer |
| SCB9_EZ_DATA117 | 0x406905D4 | FULL | Memory buffer |
| SCB9_EZ_DATA118 | 0x406905D8 | FULL | Memory buffer |
| SCB9_EZ_DATA119 | 0x406905DC | FULL | Memory buffer |
| SCB9_EZ_DATA120 | 0x406905E0 | FULL | Memory buffer |
| SCB9_EZ_DATA121 | 0x406905E4 | FULL | Memory buffer |
| SCB9_EZ_DATA122 | 0x406905E8 | FULL | Memory buffer |
| SCB9_EZ_DATA123 | 0x406905EC | FULL | Memory buffer |
| SCB9_EZ_DATA124 | 0x406905F0 | FULL | Memory buffer |
| SCB9_EZ_DATA125 | 0x406905F4 | FULL | Memory buffer |
| SCB9_EZ_DATA126 | 0x406905F8 | FULL | Memory buffer |
| SCB9_EZ_DATA127 | 0x406905FC | FULL | Memory buffer |
| SCB9_EZ_DATA128 | 0x40690600 | FULL | Memory buffer |
| SCB9_EZ_DATA129 | 0x40690604 | FULL | Memory buffer |
| SCB9_EZ_DATA130 | 0x40690608 | FULL | Memory buffer |
| SCB9_EZ_DATA131 | 0x4069060C | FULL | Memory buffer |
| SCB9_EZ_DATA132 | 0x40690610 | FULL | Memory buffer |
| SCB9_EZ_DATA133 | 0x40690614 | FULL | Memory buffer |
| SCB9_EZ_DATA134 | 0x40690618 | FULL | Memory buffer |
| SCB9_EZ_DATA135 | 0x4069061C | FULL | Memory buffer |
| SCB9_EZ_DATA136 | 0x40690620 | FULL | Memory buffer |
| SCB9_EZ_DATA137 | 0x40690624 | FULL | Memory buffer |
| SCB9_EZ_DATA138 | 0x40690628 | FULL | Memory buffer |
| SCB9_EZ_DATA139 | 0x4069062C | FULL | Memory buffer |
| SCB9_EZ_DATA140 | 0x40690630 | FULL | Memory buffer |
| SCB9_EZ_DATA141 | 0x40690634 | FULL | Memory buffer |
| SCB9_EZ_DATA142 | 0x40690638 | FULL | Memory buffer |
| SCB9_EZ_DATA143 | 0x4069063C | FULL | Memory buffer |
| SCB9_EZ_DATA144 | 0x40690640 | FULL | Memory buffer |
| SCB9_EZ_DATA145 | 0x40690644 | FULL | Memory buffer |
| SCB9_EZ_DATA146 | 0x40690648 | FULL | Memory buffer |
| SCB9_EZ_DATA147 | 0x4069064C | FULL | Memory buffer |
| SCB9_EZ_DATA148 | 0x40690650 | FULL | Memory buffer |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SCB9_EZ_DATA149 | 0x40690654 | FULL | Memory buffer |
| SCB9_EZ_DATA150 | 0x40690658 | FULL | Memory buffer |
| SCB9_EZ_DATA151 | 0x4069065C | FULL | Memory buffer |
| SCB9_EZ_DATA152 | 0x40690660 | FULL | Memory buffer |
| SCB9_EZ_DATA153 | 0x40690664 | FULL | Memory buffer |
| SCB9_EZ_DATA154 | 0x40690668 | FULL | Memory buffer |
| SCB9_EZ_DATA155 | 0x4069066C | FULL | Memory buffer |
| SCB9_EZ_DATA156 | 0x40690670 | FULL | Memory buffer |
| SCB9_EZ_DATA157 | 0x40690674 | FULL | Memory buffer |
| SCB9_EZ_DATA158 | 0x40690678 | FULL | Memory buffer |
| SCB9_EZ_DATA159 | 0x4069067C | FULL | Memory buffer |
| SCB9_EZ_DATA160 | 0x40690680 | FULL | Memory buffer |
| SCB9_EZ_DATA161 | 0x40690684 | FULL | Memory buffer |
| SCB9_EZ_DATA162 | 0x40690688 | FULL | Memory buffer |
| SCB9_EZ_DATA163 | 0x4069068C | FULL | Memory buffer |
| SCB9_EZ_DATA164 | 0x40690690 | FULL | Memory buffer |
| SCB9_EZ_DATA165 | 0x40690694 | FULL | Memory buffer |
| SCB9_EZ_DATA166 | 0x40690698 | FULL | Memory buffer |
| SCB9_EZ_DATA167 | 0x4069069C | FULL | Memory buffer |
| SCB9_EZ_DATA168 | 0x406906A0 | FULL | Memory buffer |
| SCB9_EZ_DATA169 | 0x406906A4 | FULL | Memory buffer |
| SCB9_EZ_DATA170 | 0x406906A8 | FULL | Memory buffer |
| SCB9_EZ_DATA171 | 0x406906AC | FULL | Memory buffer |
| SCB9_EZ_DATA172 | 0x406906B0 | FULL | Memory buffer |
| SCB9_EZ_DATA173 | 0x406906B4 | FULL | Memory buffer |
| SCB9_EZ_DATA174 | 0x406906B8 | FULL | Memory buffer |
| SCB9_EZ_DATA175 | 0x406906BC | FULL | Memory buffer |
| SCB9_EZ_DATA176 | 0x406906C0 | FULL | Memory buffer |
| SCB9_EZ_DATA177 | 0x406906C4 | FULL | Memory buffer |
| SCB9_EZ_DATA178 | 0x406906C8 | FULL | Memory buffer |
| SCB9_EZ_DATA179 | 0x406906CC | FULL | Memory buffer |
| SCB9_EZ_DATA180 | 0x406906D0 | FULL | Memory buffer |
| SCB9_EZ_DATA181 | 0x406906D4 | FULL | Memory buffer |
| SCB9_EZ_DATA182 | 0x406906D8 | FULL | Memory buffer |
| SCB9_EZ_DATA183 | 0x406906DC | FULL | Memory buffer |
| SCB9_EZ_DATA184 | 0x406906E0 | FULL | Memory buffer |
| SCB9_EZ_DATA185 | 0x406906E4 | FULL | Memory buffer |
| SCB9_EZ_DATA186 | 0x406906E8 | FULL | Memory buffer |
| SCB9_EZ_DATA187 | 0x406906EC | FULL | Memory buffer |
| SCB9_EZ_DATA188 | 0x406906F0 | FULL | Memory buffer |
| SCB9_EZ_DATA189 | 0x406906F4 | FULL | Memory buffer |
| SCB9_EZ_DATA190 | 0x406906F8 | FULL | Memory buffer |
| SCB9_EZ_DATA191 | 0x406906FC | FULL | Memory buffer |
| SCB9_EZ_DATA192 | 0x40690700 | FULL | Memory buffer |
| SCB9_EZ_DATA193 | 0x40690704 | FULL | Memory buffer |
| SCB9_EZ_DATA194 | 0x40690708 | FULL | Memory buffer |
| SCB9_EZ_DATA195 | 0x4069070C | FULL | Memory buffer |
| SCB9_EZ_DATA196 | 0x40690710 | FULL | Memory buffer |
| SCB9_EZ_DATA197 | 0x40690714 | FULL | Memory buffer |
| SCB9_EZ_DATA198 | 0x40690718 | FULL | Memory buffer |
| SCB9_EZ_DATA199 | 0x4069071C | FULL | Memory buffer |
| SCB9_EZ_DATA200 | 0x40690720 | FULL | Memory buffer |
| SCB9_EZ_DATA201 | 0x40690724 | FULL | Memory buffer |
| SCB9_EZ_DATA202 | 0x40690728 | FULL | Memory buffer |
| SCB9_EZ_DATA203 | 0x4069072C | FULL | Memory buffer |
| SCB9_EZ_DATA204 | 0x40690730 | FULL | Memory buffer |
| SCB9_EZ_DATA205 | 0x40690734 | FULL | Memory buffer |
| SCB9_EZ_DATA206 | 0x40690738 | FULL | Memory buffer |
| SCB9_EZ_DATA207 | 0x4069073C | FULL | Memory buffer |
| SCB9_EZ_DATA208 | 0x40690740 | FULL | Memory buffer |
| SCB9_EZ_DATA209 | 0x40690744 | FULL | Memory buffer |
| SCB9_EZ_DATA210 | 0x40690748 | FULL | Memory buffer |
| SCB9_EZ_DATA211 | 0x4069074C | FULL | Memory buffer |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SCB9_EZ_DATA212 | 0x40690750 | FULL | Memory buffer |
| SCB9_EZ_DATA213 | 0x40690754 | FULL | Memory buffer |
| SCB9_EZ_DATA214 | 0x40690758 | FULL | Memory buffer |
| SCB9_EZ_DATA215 | 0x4069075C | FULL | Memory buffer |
| SCB9_EZ_DATA216 | 0x40690760 | FULL | Memory buffer |
| SCB9_EZ_DATA217 | 0x40690764 | FULL | Memory buffer |
| SCB9_EZ_DATA218 | 0x40690768 | FULL | Memory buffer |
| SCB9_EZ_DATA219 | 0x4069076C | FULL | Memory buffer |
| SCB9_EZ_DATA220 | 0x40690770 | FULL | Memory buffer |
| SCB9_EZ_DATA221 | 0x40690774 | FULL | Memory buffer |
| SCB9_EZ_DATA222 | 0x40690778 | FULL | Memory buffer |
| SCB9_EZ_DATA223 | 0x4069077C | FULL | Memory buffer |
| SCB9_EZ_DATA224 | 0x40690780 | FULL | Memory buffer |
| SCB9_EZ_DATA225 | 0x40690784 | FULL | Memory buffer |
| SCB9_EZ_DATA226 | 0x40690788 | FULL | Memory buffer |
| SCB9_EZ_DATA227 | 0x4069078C | FULL | Memory buffer |
| SCB9_EZ_DATA228 | 0x40690790 | FULL | Memory buffer |
| SCB9_EZ_DATA229 | 0x40690794 | FULL | Memory buffer |
| SCB9_EZ_DATA230 | 0x40690798 | FULL | Memory buffer |
| SCB9_EZ_DATA231 | 0x4069079C | FULL | Memory buffer |
| SCB9_EZ_DATA232 | 0x406907A0 | FULL | Memory buffer |
| SCB9_EZ_DATA233 | 0x406907A4 | FULL | Memory buffer |
| SCB9_EZ_DATA234 | 0x406907A8 | FULL | Memory buffer |
| SCB9_EZ_DATA235 | 0x406907AC | FULL | Memory buffer |
| SCB9_EZ_DATA236 | 0x406907B0 | FULL | Memory buffer |
| SCB9_EZ_DATA237 | 0x406907B4 | FULL | Memory buffer |
| SCB9_EZ_DATA238 | 0x406907B8 | FULL | Memory buffer |
| SCB9_EZ_DATA239 | 0x406907BC | FULL | Memory buffer |
| SCB9_EZ_DATA240 | 0x406907C0 | FULL | Memory buffer |
| SCB9_EZ_DATA241 | 0x406907C4 | FULL | Memory buffer |
| SCB9_EZ_DATA242 | 0x406907C8 | FULL | Memory buffer |
| SCB9_EZ_DATA243 | 0x406907CC | FULL | Memory buffer |
| SCB9_EZ_DATA244 | 0x406907D0 | FULL | Memory buffer |
| SCB9_EZ_DATA245 | 0x406907D4 | FULL | Memory buffer |
| SCB9_EZ_DATA246 | 0x406907D8 | FULL | Memory buffer |
| SCB9_EZ_DATA247 | 0x406907DC | FULL | Memory buffer |
| SCB9_EZ_DATA248 | 0x406907E0 | FULL | Memory buffer |
| SCB9_EZ_DATA249 | 0x406907E4 | FULL | Memory buffer |
| SCB9_EZ_DATA250 | 0x406907E8 | FULL | Memory buffer |
| SCB9_EZ_DATA251 | 0x406907EC | FULL | Memory buffer |
| SCB9_EZ_DATA252 | 0x406907F0 | FULL | Memory buffer |
| SCB9_EZ_DATA253 | 0x406907F4 | FULL | Memory buffer |
| SCB9_EZ_DATA254 | 0x406907F8 | FULL | Memory buffer |
| SCB9_EZ_DATA255 | 0x406907FC | FULL | Memory buffer |
| SCB9_INTR_CAUSE | 0x40690E00 | FULL | Active clocked interrupt signal<br>Note:I2C_EC is not available for this register |
| SCB9_INTR_SPI_EC | 0x40690EC0 | FULL | Externally clocked SPI interrupt request |
| SCB9_INTR_SPI_EC_MASK | 0x40690EC8 | FULL | Externally clocked SPI interrupt mask |
| SCB9_INTR_SPI_EC_MASKED | 0x40690ECC | FULL | Externally clocked SPI interrupt masked |
| SCB9_INTR_M | 0x40690F00 | FULL | Master interrupt request |
| SCB9_INTR_M_SET | 0x40690F04 | FULL | Master interrupt set request |
| SCB9_INTR_M_MASK | 0x40690F08 | FULL | Master interrupt mask |
| SCB9_INTR_M_MASKED | 0x40690F0C | FULL | Master interrupt masked request |
| SCB9_INTR_S | 0x40690F40 | FULL | Slave interrupt request |
| SCB9_INTR_S_SET | 0x40690F44 | FULL | Slave interrupt set request |
| SCB9_INTR_S_MASK | 0x40690F48 | FULL | Slave interrupt mask |
| SCB9_INTR_S_MASKED | 0x40690F4C | FULL | Slave interrupt masked request |
| SCB9_INTR_TX | 0x40690F80 | FULL | Transmitter interrupt request |
| SCB9_INTR_TX_SET | 0x40690F84 | FULL | Transmitter interrupt set request |
| SCB9_INTR_TX_MASK | 0x40690F88 | FULL | Transmitter interrupt mask |
| SCB9_INTR_TX_MASKED | 0x40690F8C | FULL | Transmitter interrupt masked request |
| SCB9_INTR_RX | 0x40690FC0 | FULL | Receiver interrupt request |
| SCB9_INTR_RX_SET | 0x40690FC4 | FULL | Receiver interrupt set request |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SCB9_INTR_RX_MASK | 0x40690FC8 | FULL | Receiver interrupt mask |
| SCB9_INTR_RX_MASKED | 0x40690FCC | FULL | Receiver interrupt masked request |

## 26.11 SCB 10

**Description** Serial Communications Block (SPI/UART/I2C)
**Base Address** 0x406A0000
**Size** 0x10000
**Slave Num** MMIO6 - 10

This instance is not available in the following part numbers:
CYT4BF8CES, CYT4BF8CEE, CYT4A0M1BE, CYT4BF8DES, CYT4BF8DEE, CYT4BF8CDS, CYT4A0M14S, CYT4BF8CDE, CYT4A0M14E, CYT4BF8CXE, CYT4BF8DDS, CYT4BF8DDE.

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SCB10_CTRL | 0x406A0000 | FULL | Generic control<br>Note:CMD_RESP_MODE is not available for this register |
| SCB10_STATUS | 0x406A0004 | FULL | Generic status |
| SCB10_SPI_CTRL | 0x406A0020 | FULL | SPI control |
| SCB10_SPI_STATUS | 0x406A0024 | FULL | SPI status |
| SCB10_SPI_TX_CTRL | 0x406A0028 | FULL | SPI transmitter control |
| SCB10_SPI_RX_CTRL | 0x406A002C | FULL | SPI receiver control |
| SCB10_UART_CTRL | 0x406A0040 | FULL | UART control |
| SCB10_UART_TX_CTRL | 0x406A0044 | FULL | UART transmitter control |
| SCB10_UART_RX_CTRL | 0x406A0048 | FULL | UART receiver control |
| SCB10_UART_RX_STATUS | 0x406A004C | FULL | UART receiver status |
| SCB10_UART_FLOW_CTRL | 0x406A0050 | FULL | UART flow control |
| SCB10_I2C_CTRL | 0x406A0060 | FULL | I2C control |
| SCB10_I2C_STATUS | 0x406A0064 | FULL | I2C status<br>Note:I2C_EC_BUSY is not available for this register |
| SCB10_I2C_M_CMD | 0x406A0068 | FULL | I2C master command |
| SCB10_I2C_S_CMD | 0x406A006C | FULL | I2C slave command |
| SCB10_I2C_CFG | 0x406A0070 | FULL | I2C configuration |
| SCB10_TX_CTRL | 0x406A0200 | FULL | Transmitter control |
| SCB10_TX_FIFO_CTRL | 0x406A0204 | FULL | Transmitter FIFO control |
| SCB10_TX_FIFO_STATUS | 0x406A0208 | FULL | Transmitter FIFO status |
| SCB10_TX_FIFO_WR | 0x406A0240 | FULL | Transmitter FIFO write |
| SCB10_RX_CTRL | 0x406A0300 | FULL | Receiver control |
| SCB10_RX_FIFO_CTRL | 0x406A0304 | FULL | Receiver FIFO control |
| SCB10_RX_FIFO_STATUS | 0x406A0308 | FULL | Receiver FIFO status |
| SCB10_RX_MATCH | 0x406A0310 | FULL | Slave address and mask |
| SCB10_RX_FIFO_RD | 0x406A0340 | FULL | Receiver FIFO read |
| SCB10_RX_FIFO_RD_SILENT | 0x406A0344 | FULL | Receiver FIFO read silent |
| SCB10_EZ_DATA0 | 0x406A0400 | FULL | Memory buffer |
| SCB10_EZ_DATA1 | 0x406A0404 | FULL | Memory buffer |
| SCB10_EZ_DATA2 | 0x406A0408 | FULL | Memory buffer |
| SCB10_EZ_DATA3 | 0x406A040C | FULL | Memory buffer |
| SCB10_EZ_DATA4 | 0x406A0410 | FULL | Memory buffer |
| SCB10_EZ_DATA5 | 0x406A0414 | FULL | Memory buffer |
| SCB10_EZ_DATA6 | 0x406A0418 | FULL | Memory buffer |
| SCB10_EZ_DATA7 | 0x406A041C | FULL | Memory buffer |
| SCB10_EZ_DATA8 | 0x406A0420 | FULL | Memory buffer |
| SCB10_EZ_DATA9 | 0x406A0424 | FULL | Memory buffer |
| SCB10_EZ_DATA10 | 0x406A0428 | FULL | Memory buffer |
| SCB10_EZ_DATA11 | 0x406A042C | FULL | Memory buffer |
| SCB10_EZ_DATA12 | 0x406A0430 | FULL | Memory buffer |
| SCB10_EZ_DATA13 | 0x406A0434 | FULL | Memory buffer |
| SCB10_EZ_DATA14 | 0x406A0438 | FULL | Memory buffer |
| SCB10_EZ_DATA15 | 0x406A043C | FULL | Memory buffer |
| SCB10_EZ_DATA16 | 0x406A0440 | FULL | Memory buffer |
| SCB10_EZ_DATA17 | 0x406A0444 | FULL | Memory buffer |
| SCB10_EZ_DATA18 | 0x406A0448 | FULL | Memory buffer |
| SCB10_EZ_DATA19 | 0x406A044C | FULL | Memory buffer |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SCB10_EZ_DATA20 | 0x406A0450 | FULL | Memory buffer |
| SCB10_EZ_DATA21 | 0x406A0454 | FULL | Memory buffer |
| SCB10_EZ_DATA22 | 0x406A0458 | FULL | Memory buffer |
| SCB10_EZ_DATA23 | 0x406A045C | FULL | Memory buffer |
| SCB10_EZ_DATA24 | 0x406A0460 | FULL | Memory buffer |
| SCB10_EZ_DATA25 | 0x406A0464 | FULL | Memory buffer |
| SCB10_EZ_DATA26 | 0x406A0468 | FULL | Memory buffer |
| SCB10_EZ_DATA27 | 0x406A046C | FULL | Memory buffer |
| SCB10_EZ_DATA28 | 0x406A0470 | FULL | Memory buffer |
| SCB10_EZ_DATA29 | 0x406A0474 | FULL | Memory buffer |
| SCB10_EZ_DATA30 | 0x406A0478 | FULL | Memory buffer |
| SCB10_EZ_DATA31 | 0x406A047C | FULL | Memory buffer |
| SCB10_EZ_DATA32 | 0x406A0480 | FULL | Memory buffer |
| SCB10_EZ_DATA33 | 0x406A0484 | FULL | Memory buffer |
| SCB10_EZ_DATA34 | 0x406A0488 | FULL | Memory buffer |
| SCB10_EZ_DATA35 | 0x406A048C | FULL | Memory buffer |
| SCB10_EZ_DATA36 | 0x406A0490 | FULL | Memory buffer |
| SCB10_EZ_DATA37 | 0x406A0494 | FULL | Memory buffer |
| SCB10_EZ_DATA38 | 0x406A0498 | FULL | Memory buffer |
| SCB10_EZ_DATA39 | 0x406A049C | FULL | Memory buffer |
| SCB10_EZ_DATA40 | 0x406A04A0 | FULL | Memory buffer |
| SCB10_EZ_DATA41 | 0x406A04A4 | FULL | Memory buffer |
| SCB10_EZ_DATA42 | 0x406A04A8 | FULL | Memory buffer |
| SCB10_EZ_DATA43 | 0x406A04AC | FULL | Memory buffer |
| SCB10_EZ_DATA44 | 0x406A04B0 | FULL | Memory buffer |
| SCB10_EZ_DATA45 | 0x406A04B4 | FULL | Memory buffer |
| SCB10_EZ_DATA46 | 0x406A04B8 | FULL | Memory buffer |
| SCB10_EZ_DATA47 | 0x406A04BC | FULL | Memory buffer |
| SCB10_EZ_DATA48 | 0x406A04C0 | FULL | Memory buffer |
| SCB10_EZ_DATA49 | 0x406A04C4 | FULL | Memory buffer |
| SCB10_EZ_DATA50 | 0x406A04C8 | FULL | Memory buffer |
| SCB10_EZ_DATA51 | 0x406A04CC | FULL | Memory buffer |
| SCB10_EZ_DATA52 | 0x406A04D0 | FULL | Memory buffer |
| SCB10_EZ_DATA53 | 0x406A04D4 | FULL | Memory buffer |
| SCB10_EZ_DATA54 | 0x406A04D8 | FULL | Memory buffer |
| SCB10_EZ_DATA55 | 0x406A04DC | FULL | Memory buffer |
| SCB10_EZ_DATA56 | 0x406A04E0 | FULL | Memory buffer |
| SCB10_EZ_DATA57 | 0x406A04E4 | FULL | Memory buffer |
| SCB10_EZ_DATA58 | 0x406A04E8 | FULL | Memory buffer |
| SCB10_EZ_DATA59 | 0x406A04EC | FULL | Memory buffer |
| SCB10_EZ_DATA60 | 0x406A04F0 | FULL | Memory buffer |
| SCB10_EZ_DATA61 | 0x406A04F4 | FULL | Memory buffer |
| SCB10_EZ_DATA62 | 0x406A04F8 | FULL | Memory buffer |
| SCB10_EZ_DATA63 | 0x406A04FC | FULL | Memory buffer |
| SCB10_EZ_DATA64 | 0x406A0500 | FULL | Memory buffer |
| SCB10_EZ_DATA65 | 0x406A0504 | FULL | Memory buffer |
| SCB10_EZ_DATA66 | 0x406A0508 | FULL | Memory buffer |
| SCB10_EZ_DATA67 | 0x406A050C | FULL | Memory buffer |
| SCB10_EZ_DATA68 | 0x406A0510 | FULL | Memory buffer |
| SCB10_EZ_DATA69 | 0x406A0514 | FULL | Memory buffer |
| SCB10_EZ_DATA70 | 0x406A0518 | FULL | Memory buffer |
| SCB10_EZ_DATA71 | 0x406A051C | FULL | Memory buffer |
| SCB10_EZ_DATA72 | 0x406A0520 | FULL | Memory buffer |
| SCB10_EZ_DATA73 | 0x406A0524 | FULL | Memory buffer |
| SCB10_EZ_DATA74 | 0x406A0528 | FULL | Memory buffer |
| SCB10_EZ_DATA75 | 0x406A052C | FULL | Memory buffer |
| SCB10_EZ_DATA76 | 0x406A0530 | FULL | Memory buffer |
| SCB10_EZ_DATA77 | 0x406A0534 | FULL | Memory buffer |
| SCB10_EZ_DATA78 | 0x406A0538 | FULL | Memory buffer |
| SCB10_EZ_DATA79 | 0x406A053C | FULL | Memory buffer |
| SCB10_EZ_DATA80 | 0x406A0540 | FULL | Memory buffer |
| SCB10_EZ_DATA81 | 0x406A0544 | FULL | Memory buffer |
| SCB10_EZ_DATA82 | 0x406A0548 | FULL | Memory buffer |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SCB10_EZ_DATA83 | 0x406A054C | FULL | Memory buffer |
| SCB10_EZ_DATA84 | 0x406A0550 | FULL | Memory buffer |
| SCB10_EZ_DATA85 | 0x406A0554 | FULL | Memory buffer |
| SCB10_EZ_DATA86 | 0x406A0558 | FULL | Memory buffer |
| SCB10_EZ_DATA87 | 0x406A055C | FULL | Memory buffer |
| SCB10_EZ_DATA88 | 0x406A0560 | FULL | Memory buffer |
| SCB10_EZ_DATA89 | 0x406A0564 | FULL | Memory buffer |
| SCB10_EZ_DATA90 | 0x406A0568 | FULL | Memory buffer |
| SCB10_EZ_DATA91 | 0x406A056C | FULL | Memory buffer |
| SCB10_EZ_DATA92 | 0x406A0570 | FULL | Memory buffer |
| SCB10_EZ_DATA93 | 0x406A0574 | FULL | Memory buffer |
| SCB10_EZ_DATA94 | 0x406A0578 | FULL | Memory buffer |
| SCB10_EZ_DATA95 | 0x406A057C | FULL | Memory buffer |
| SCB10_EZ_DATA96 | 0x406A0580 | FULL | Memory buffer |
| SCB10_EZ_DATA97 | 0x406A0584 | FULL | Memory buffer |
| SCB10_EZ_DATA98 | 0x406A0588 | FULL | Memory buffer |
| SCB10_EZ_DATA99 | 0x406A058C | FULL | Memory buffer |
| SCB10_EZ_DATA100 | 0x406A0590 | FULL | Memory buffer |
| SCB10_EZ_DATA101 | 0x406A0594 | FULL | Memory buffer |
| SCB10_EZ_DATA102 | 0x406A0598 | FULL | Memory buffer |
| SCB10_EZ_DATA103 | 0x406A059C | FULL | Memory buffer |
| SCB10_EZ_DATA104 | 0x406A05A0 | FULL | Memory buffer |
| SCB10_EZ_DATA105 | 0x406A05A4 | FULL | Memory buffer |
| SCB10_EZ_DATA106 | 0x406A05A8 | FULL | Memory buffer |
| SCB10_EZ_DATA107 | 0x406A05AC | FULL | Memory buffer |
| SCB10_EZ_DATA108 | 0x406A05B0 | FULL | Memory buffer |
| SCB10_EZ_DATA109 | 0x406A05B4 | FULL | Memory buffer |
| SCB10_EZ_DATA110 | 0x406A05B8 | FULL | Memory buffer |
| SCB10_EZ_DATA111 | 0x406A05BC | FULL | Memory buffer |
| SCB10_EZ_DATA112 | 0x406A05C0 | FULL | Memory buffer |
| SCB10_EZ_DATA113 | 0x406A05C4 | FULL | Memory buffer |
| SCB10_EZ_DATA114 | 0x406A05C8 | FULL | Memory buffer |
| SCB10_EZ_DATA115 | 0x406A05CC | FULL | Memory buffer |
| SCB10_EZ_DATA116 | 0x406A05D0 | FULL | Memory buffer |
| SCB10_EZ_DATA117 | 0x406A05D4 | FULL | Memory buffer |
| SCB10_EZ_DATA118 | 0x406A05D8 | FULL | Memory buffer |
| SCB10_EZ_DATA119 | 0x406A05DC | FULL | Memory buffer |
| SCB10_EZ_DATA120 | 0x406A05E0 | FULL | Memory buffer |
| SCB10_EZ_DATA121 | 0x406A05E4 | FULL | Memory buffer |
| SCB10_EZ_DATA122 | 0x406A05E8 | FULL | Memory buffer |
| SCB10_EZ_DATA123 | 0x406A05EC | FULL | Memory buffer |
| SCB10_EZ_DATA124 | 0x406A05F0 | FULL | Memory buffer |
| SCB10_EZ_DATA125 | 0x406A05F4 | FULL | Memory buffer |
| SCB10_EZ_DATA126 | 0x406A05F8 | FULL | Memory buffer |
| SCB10_EZ_DATA127 | 0x406A05FC | FULL | Memory buffer |
| SCB10_EZ_DATA128 | 0x406A0600 | FULL | Memory buffer |
| SCB10_EZ_DATA129 | 0x406A0604 | FULL | Memory buffer |
| SCB10_EZ_DATA130 | 0x406A0608 | FULL | Memory buffer |
| SCB10_EZ_DATA131 | 0x406A060C | FULL | Memory buffer |
| SCB10_EZ_DATA132 | 0x406A0610 | FULL | Memory buffer |
| SCB10_EZ_DATA133 | 0x406A0614 | FULL | Memory buffer |
| SCB10_EZ_DATA134 | 0x406A0618 | FULL | Memory buffer |
| SCB10_EZ_DATA135 | 0x406A061C | FULL | Memory buffer |
| SCB10_EZ_DATA136 | 0x406A0620 | FULL | Memory buffer |
| SCB10_EZ_DATA137 | 0x406A0624 | FULL | Memory buffer |
| SCB10_EZ_DATA138 | 0x406A0628 | FULL | Memory buffer |
| SCB10_EZ_DATA139 | 0x406A062C | FULL | Memory buffer |
| SCB10_EZ_DATA140 | 0x406A0630 | FULL | Memory buffer |
| SCB10_EZ_DATA141 | 0x406A0634 | FULL | Memory buffer |
| SCB10_EZ_DATA142 | 0x406A0638 | FULL | Memory buffer |
| SCB10_EZ_DATA143 | 0x406A063C | FULL | Memory buffer |
| SCB10_EZ_DATA144 | 0x406A0640 | FULL | Memory buffer |
| SCB10_EZ_DATA145 | 0x406A0644 | FULL | Memory buffer |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SCB10_EZ_DATA146 | 0x406A0648 | FULL | Memory buffer |
| SCB10_EZ_DATA147 | 0x406A064C | FULL | Memory buffer |
| SCB10_EZ_DATA148 | 0x406A0650 | FULL | Memory buffer |
| SCB10_EZ_DATA149 | 0x406A0654 | FULL | Memory buffer |
| SCB10_EZ_DATA150 | 0x406A0658 | FULL | Memory buffer |
| SCB10_EZ_DATA151 | 0x406A065C | FULL | Memory buffer |
| SCB10_EZ_DATA152 | 0x406A0660 | FULL | Memory buffer |
| SCB10_EZ_DATA153 | 0x406A0664 | FULL | Memory buffer |
| SCB10_EZ_DATA154 | 0x406A0668 | FULL | Memory buffer |
| SCB10_EZ_DATA155 | 0x406A066C | FULL | Memory buffer |
| SCB10_EZ_DATA156 | 0x406A0670 | FULL | Memory buffer |
| SCB10_EZ_DATA157 | 0x406A0674 | FULL | Memory buffer |
| SCB10_EZ_DATA158 | 0x406A0678 | FULL | Memory buffer |
| SCB10_EZ_DATA159 | 0x406A067C | FULL | Memory buffer |
| SCB10_EZ_DATA160 | 0x406A0680 | FULL | Memory buffer |
| SCB10_EZ_DATA161 | 0x406A0684 | FULL | Memory buffer |
| SCB10_EZ_DATA162 | 0x406A0688 | FULL | Memory buffer |
| SCB10_EZ_DATA163 | 0x406A068C | FULL | Memory buffer |
| SCB10_EZ_DATA164 | 0x406A0690 | FULL | Memory buffer |
| SCB10_EZ_DATA165 | 0x406A0694 | FULL | Memory buffer |
| SCB10_EZ_DATA166 | 0x406A0698 | FULL | Memory buffer |
| SCB10_EZ_DATA167 | 0x406A069C | FULL | Memory buffer |
| SCB10_EZ_DATA168 | 0x406A06A0 | FULL | Memory buffer |
| SCB10_EZ_DATA169 | 0x406A06A4 | FULL | Memory buffer |
| SCB10_EZ_DATA170 | 0x406A06A8 | FULL | Memory buffer |
| SCB10_EZ_DATA171 | 0x406A06AC | FULL | Memory buffer |
| SCB10_EZ_DATA172 | 0x406A06B0 | FULL | Memory buffer |
| SCB10_EZ_DATA173 | 0x406A06B4 | FULL | Memory buffer |
| SCB10_EZ_DATA174 | 0x406A06B8 | FULL | Memory buffer |
| SCB10_EZ_DATA175 | 0x406A06BC | FULL | Memory buffer |
| SCB10_EZ_DATA176 | 0x406A06C0 | FULL | Memory buffer |
| SCB10_EZ_DATA177 | 0x406A06C4 | FULL | Memory buffer |
| SCB10_EZ_DATA178 | 0x406A06C8 | FULL | Memory buffer |
| SCB10_EZ_DATA179 | 0x406A06CC | FULL | Memory buffer |
| SCB10_EZ_DATA180 | 0x406A06D0 | FULL | Memory buffer |
| SCB10_EZ_DATA181 | 0x406A06D4 | FULL | Memory buffer |
| SCB10_EZ_DATA182 | 0x406A06D8 | FULL | Memory buffer |
| SCB10_EZ_DATA183 | 0x406A06DC | FULL | Memory buffer |
| SCB10_EZ_DATA184 | 0x406A06E0 | FULL | Memory buffer |
| SCB10_EZ_DATA185 | 0x406A06E4 | FULL | Memory buffer |
| SCB10_EZ_DATA186 | 0x406A06E8 | FULL | Memory buffer |
| SCB10_EZ_DATA187 | 0x406A06EC | FULL | Memory buffer |
| SCB10_EZ_DATA188 | 0x406A06F0 | FULL | Memory buffer |
| SCB10_EZ_DATA189 | 0x406A06F4 | FULL | Memory buffer |
| SCB10_EZ_DATA190 | 0x406A06F8 | FULL | Memory buffer |
| SCB10_EZ_DATA191 | 0x406A06FC | FULL | Memory buffer |
| SCB10_EZ_DATA192 | 0x406A0700 | FULL | Memory buffer |
| SCB10_EZ_DATA193 | 0x406A0704 | FULL | Memory buffer |
| SCB10_EZ_DATA194 | 0x406A0708 | FULL | Memory buffer |
| SCB10_EZ_DATA195 | 0x406A070C | FULL | Memory buffer |
| SCB10_EZ_DATA196 | 0x406A0710 | FULL | Memory buffer |
| SCB10_EZ_DATA197 | 0x406A0714 | FULL | Memory buffer |
| SCB10_EZ_DATA198 | 0x406A0718 | FULL | Memory buffer |
| SCB10_EZ_DATA199 | 0x406A071C | FULL | Memory buffer |
| SCB10_EZ_DATA200 | 0x406A0720 | FULL | Memory buffer |
| SCB10_EZ_DATA201 | 0x406A0724 | FULL | Memory buffer |
| SCB10_EZ_DATA202 | 0x406A0728 | FULL | Memory buffer |
| SCB10_EZ_DATA203 | 0x406A072C | FULL | Memory buffer |
| SCB10_EZ_DATA204 | 0x406A0730 | FULL | Memory buffer |
| SCB10_EZ_DATA205 | 0x406A0734 | FULL | Memory buffer |
| SCB10_EZ_DATA206 | 0x406A0738 | FULL | Memory buffer |
| SCB10_EZ_DATA207 | 0x406A073C | FULL | Memory buffer |
| SCB10_EZ_DATA208 | 0x406A0740 | FULL | Memory buffer |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SCB10_EZ_DATA209 | 0x406A0744 | FULL | Memory buffer |
| SCB10_EZ_DATA210 | 0x406A0748 | FULL | Memory buffer |
| SCB10_EZ_DATA211 | 0x406A074C | FULL | Memory buffer |
| SCB10_EZ_DATA212 | 0x406A0750 | FULL | Memory buffer |
| SCB10_EZ_DATA213 | 0x406A0754 | FULL | Memory buffer |
| SCB10_EZ_DATA214 | 0x406A0758 | FULL | Memory buffer |
| SCB10_EZ_DATA215 | 0x406A075C | FULL | Memory buffer |
| SCB10_EZ_DATA216 | 0x406A0760 | FULL | Memory buffer |
| SCB10_EZ_DATA217 | 0x406A0764 | FULL | Memory buffer |
| SCB10_EZ_DATA218 | 0x406A0768 | FULL | Memory buffer |
| SCB10_EZ_DATA219 | 0x406A076C | FULL | Memory buffer |
| SCB10_EZ_DATA220 | 0x406A0770 | FULL | Memory buffer |
| SCB10_EZ_DATA221 | 0x406A0774 | FULL | Memory buffer |
| SCB10_EZ_DATA222 | 0x406A0778 | FULL | Memory buffer |
| SCB10_EZ_DATA223 | 0x406A077C | FULL | Memory buffer |
| SCB10_EZ_DATA224 | 0x406A0780 | FULL | Memory buffer |
| SCB10_EZ_DATA225 | 0x406A0784 | FULL | Memory buffer |
| SCB10_EZ_DATA226 | 0x406A0788 | FULL | Memory buffer |
| SCB10_EZ_DATA227 | 0x406A078C | FULL | Memory buffer |
| SCB10_EZ_DATA228 | 0x406A0790 | FULL | Memory buffer |
| SCB10_EZ_DATA229 | 0x406A0794 | FULL | Memory buffer |
| SCB10_EZ_DATA230 | 0x406A0798 | FULL | Memory buffer |
| SCB10_EZ_DATA231 | 0x406A079C | FULL | Memory buffer |
| SCB10_EZ_DATA232 | 0x406A07A0 | FULL | Memory buffer |
| SCB10_EZ_DATA233 | 0x406A07A4 | FULL | Memory buffer |
| SCB10_EZ_DATA234 | 0x406A07A8 | FULL | Memory buffer |
| SCB10_EZ_DATA235 | 0x406A07AC | FULL | Memory buffer |
| SCB10_EZ_DATA236 | 0x406A07B0 | FULL | Memory buffer |
| SCB10_EZ_DATA237 | 0x406A07B4 | FULL | Memory buffer |
| SCB10_EZ_DATA238 | 0x406A07B8 | FULL | Memory buffer |
| SCB10_EZ_DATA239 | 0x406A07BC | FULL | Memory buffer |
| SCB10_EZ_DATA240 | 0x406A07C0 | FULL | Memory buffer |
| SCB10_EZ_DATA241 | 0x406A07C4 | FULL | Memory buffer |
| SCB10_EZ_DATA242 | 0x406A07C8 | FULL | Memory buffer |
| SCB10_EZ_DATA243 | 0x406A07CC | FULL | Memory buffer |
| SCB10_EZ_DATA244 | 0x406A07D0 | FULL | Memory buffer |
| SCB10_EZ_DATA245 | 0x406A07D4 | FULL | Memory buffer |
| SCB10_EZ_DATA246 | 0x406A07D8 | FULL | Memory buffer |
| SCB10_EZ_DATA247 | 0x406A07DC | FULL | Memory buffer |
| SCB10_EZ_DATA248 | 0x406A07E0 | FULL | Memory buffer |
| SCB10_EZ_DATA249 | 0x406A07E4 | FULL | Memory buffer |
| SCB10_EZ_DATA250 | 0x406A07E8 | FULL | Memory buffer |
| SCB10_EZ_DATA251 | 0x406A07EC | FULL | Memory buffer |
| SCB10_EZ_DATA252 | 0x406A07F0 | FULL | Memory buffer |
| SCB10_EZ_DATA253 | 0x406A07F4 | FULL | Memory buffer |
| SCB10_EZ_DATA254 | 0x406A07F8 | FULL | Memory buffer |
| SCB10_EZ_DATA255 | 0x406A07FC | FULL | Memory buffer |
| SCB10_INTR_CAUSE | 0x406A0E00 | FULL | Active clocked interrupt signal<br>Note:I2C_EC is not available for this register |
| SCB10_INTR_SPI_EC | 0x406A0EC0 | FULL | Externally clocked SPI interrupt request |
| SCB10_INTR_SPI_EC_MASK | 0x406A0EC8 | FULL | Externally clocked SPI interrupt mask |
| SCB10_INTR_SPI_EC_MASKED | 0x406A0ECC | FULL | Externally clocked SPI interrupt masked |
| SCB10_INTR_M | 0x406A0F00 | FULL | Master interrupt request |
| SCB10_INTR_M_SET | 0x406A0F04 | FULL | Master interrupt set request |
| SCB10_INTR_M_MASK | 0x406A0F08 | FULL | Master interrupt mask |
| SCB10_INTR_M_MASKED | 0x406A0F0C | FULL | Master interrupt masked request |
| SCB10_INTR_S | 0x406A0F40 | FULL | Slave interrupt request |
| SCB10_INTR_S_SET | 0x406A0F44 | FULL | Slave interrupt set request |
| SCB10_INTR_S_MASK | 0x406A0F48 | FULL | Slave interrupt mask |
| SCB10_INTR_S_MASKED | 0x406A0F4C | FULL | Slave interrupt masked request |
| SCB10_INTR_TX | 0x406A0F80 | FULL | Transmitter interrupt request |
| SCB10_INTR_TX_SET | 0x406A0F84 | FULL | Transmitter interrupt set request |
| SCB10_INTR_TX_MASK | 0x406A0F88 | FULL | Transmitter interrupt mask |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SCB10_INTR_TX_MASKED | 0x406A0F8C | FULL | Transmitter interrupt masked request |
| SCB10_INTR_RX | 0x406A0FC0 | FULL | Receiver interrupt request |
| SCB10_INTR_RX_SET | 0x406A0FC4 | FULL | Receiver interrupt set request |
| SCB10_INTR_RX_MASK | 0x406A0FC8 | FULL | Receiver interrupt mask |
| SCB10_INTR_RX_MASKED | 0x406A0FCC | FULL | Receiver interrupt masked request |

## 26.12 Register Details

### 26.12.1 SCB_CTRL

**Description:** Generic control
**Address:** 0x40600000
**Offset:** 0x0
**Retention:** Retained
**IsDeepSleep:** No ( supported for SCB0_CTRL )
**Comment:**
**Default:** 0x300400F

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:4] | | | | OVS [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | MEM_WIDTH [15:14] | | None [13:13] | CMD _RESP_ MODE [12:12] | None [11:11] | EZ_MODE [10:10] | EC_OP _MODE [9:9] | EC_AM _MODE [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:18] | | | | | | BLOCK [17:17] | ADDR _ACCEPT [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | ENABLED [31:31] | None [30:29] | | EC _ACCESS [28:28] | None [27:26] | | MODE [25:24] | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | OVS | RW | R | 15 | Serial interface bit period oversampling factor expressed in SCB clock cycles. Used for SPI and UART functionality. OVS + 1 SCB clock cycles constitute a single serial interface clock/bit cycle. This field is NOT used in externally clocked mode. If OVS is odd, the oversampling factor is even and the low and high phase of the interface clock period are the same. If OVS is even, the oversampling factor is odd and the low and high phase can differ by 1 SCB clock period.<br><br>In SPI master mode, the valid range is [3, 15]. At an SCB frequency of 48 MHz, the maximum SPI bit rate is 12 Mbps, assuming ideal (0 ns) IO cell and routing (chip and board) delay. The calculated maximum bit rate decreases, when realistic chip and routing delays are taken into account. The effective system bit rate is dependent on the external SPI slave that we communicate with. If the SPI output clock to SPI MISO input round trip delay is significant (multiple SPI output clock cycles), it may be necessary to increase OVS and/or to set SPI_CTRL.LATE_MISO_SAMPLE to '1' to achieve the maximum possible system bit rate.<br><br>In SPI slave mode, the OVS field is NOT used. However, there is a frequency requirement for the SCB clock wrt. the SPI input clock (IF) on the interface to guarantee functional correct behavior. This requirement is expressed as a ratio: SCB clock/IF clock. The ratio is dependent on the setting of RX_CTRL.MEDIAN and the external SPI master's capability to support 'late MISO sample' functionality (similar to our SPI master functionality represented by SPI_CTRL.LATE_MISO_SAMPLE):<br>- MEDIAN is '0' and external SPI master has NO 'late MISO sample functionality': SCB clock/IF clock >= 6. At a SCB frequency of 48 MHz, the maximum bit rate is 8 Mbps.<br>- MEDIAN is '0' and external SPI master has 'late MISO sample functionality': SCB clock/IF clock >= 3. At a SCB frequency of 48 MHz, the maximum bit rate is 16 Mbps.<br>- MEDIAN is '1' and external SPI master has NO 'late MISO sample functionality': SCB clock/IF clock >= 8. At a SCB frequency of 48 MHz, the maximum bit rate is 6 Mbps.<br>- MEDIAN is '1' and external SPI master has 'late MISO sample functionality': SCB clock/IF clock >= 4. At a SCB frequency of 48 MHz, the maximum bit rate is 12 Mbps.<br>As discussed earlier, the calculated maximum bit rate decreases, when realistic chip and routing delays are taken into account.<br><br>In UART standard submode (including LIN), the valid range is [7, 15]. In UART SmartCard submode, the valid range is [7, 15]. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| | | | | | (Continuation)<br>In UART TX IrDA submode this field indirectly specifies the oversampling. The oversampling determines the interface clock/bit cycle and the width of the pulse. Only normal transmission mode is supported, the pulse is roughly 3/16 of the bit period (for all bit rates). There is only one valid OVS value:<br>- 0: 16 times oversampling.<br>SCB clock frequency of 16*115.2 KHz for 115.2 Kbps.<br>SCB clock frequency of 16*57.6 KHz for 57.6 Kbps.<br>SCB clock frequency of 16*38.4 KHz for 38.4 Kbps.<br>SCB clock frequency of 16*19.2 KHz for 19.2 Kbps.<br>SCB clock frequency of 16*9.6 KHz for 9.6 Kbps.<br>SCB clock frequency of 16*2.4 KHz for 2.4 Kbps.<br>SCB clock frequency of 16*1.2 KHz for 1.2 Kbps.<br>- all other values are not used in normal mode.<br><br>In UART RX IrDA submode (1.2, 2.4, 9.6, 19.2, 38.4, 57.6 and 115.2 Kbps) this field indirectly specifies the oversampling. The oversampling determines the interface clock/bit cycle and the width of the pulse. In normal transmission mode, this pulse is roughly 3/16 of the bit period (for all bit rates). In low power transmission mode, this pulse is potentially smaller (down to 1.62 us typical and 1.41 us minimal) than 3/16 of the bit period (for < 115.2 Kbps bitrates). Pulse widths greater or equal than two SCB clock cycles are guaranteed to be detected by the receiver. Pulse widths less than two SCB clock cycles and greater or equal than one SCB clock cycle may be detected by the receiver. Pulse widths less than one SCB clock cycle will not be detected by the receiver.<br>RX_CTRL.MEDIAN should be set to '1' for IrDA receiver functionality. The SCB clock (as provided by the programmable clock block) and the oversampling together determine the IrDA bitrate. Normal mode, OVS field values (with the required SCB clock frequency):<br>- 0: 16 times oversampling.<br>SCB clock frequency of 16*115.2 KHz for 115.2 Kbps.<br>SCB clock frequency of 16*57.6 KHz for 57.6 Kbps.<br>SCB clock frequency of 16*38.4 KHz for 38.4 Kbps.<br>SCB clock frequency of 16*19.2 KHz for 19.2 Kbps.<br>SCB clock frequency of 16*9.6 KHz for 9.6 Kbps.<br>SCB clock frequency of 16*2.4 KHz for 2.4 Kbps.<br>SCB clock frequency of 16*1.2 KHz for 1.2 Kbps.<br>- all other values are not used in normal mode.<br>Low power mode, OVS field values (with the required SCB clock frequency):<br>- 0: 16 times oversampling.<br>SCB clock frequency of 16*115.2 KHz for 115.2 Kbps.<br>- 1: 32 times oversampling.<br>SCB clock frequency of 32*57.6 KHz for 57.6 Kbps.<br>- 2: 48 times oversampling.<br>SCB clock frequency of 48*38.4 KHz for 38.4 Kbps.<br>- 3: 96 times oversampling.<br>SCB clock frequency of 96*19.2 KHz for 19.2 Kbps.<br>- 4: 192 times oversampling. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| | | | | | (Continuation)<br>SCB clock frequency of 192*9.6 KHz for 9.6 Kbps.<br>- 5: 768 times oversampling.<br>SCB clock frequency of 768*2.4 KHz for 2.4 Kbps.<br>- 6: 1536 times oversampling.<br>SCB clock frequency of 1536*1.2 KHz for 1.2 Kbps.<br>- all other values are not used in low power mode. |
| 8 | EC_AM_MODE | RW | R | 0 | This field specifies the clocking for the address matching (I2C) or slave selection detection logic (SPI)<br>'0': Internally clocked mode<br>'1': Externally clocked mode<br><br>In internally clocked mode, the serial interface protocols run off the SCB clock. In externally clocked mode, the serial interface protocols run off the clock as provided by the serial interface.<br><br>The clocking for the rest of the logic is determined by CTRL.EC_OP_MODE.<br><br>Externally clocked mode is only used for synchronous serial interface protocols (SPI and I2C) in slave mode. In SPI mode, only Motorola submode (all Motorola modes: 0, 1, 2, 3) is supported.<br><br>In UART mode this field should be '0'. |
| 9 | EC_OP_MODE | RW | R | 0 | This field specifies the clocking for the SCB block<br>'0': Internally clocked mode<br>'1': externally clocked mode<br>In internally clocked mode, the serial interface protocols run off the SCB clock. In externally clocked mode, the serial interface protocols run off the clock as provided by the serial interface.<br><br>Externally clocked operation mode is only used for synchronous serial interface protocols (SPI and I2C) in slave mode AND EZ mode. In SPI mode, only Motorola submode (all Motorola modes: 0, 1, 2, 3) is supported. The maximum SPI slave, EZ mode bitrate is 48 Mbps (transmission and IO delays outside the IP will degrade the effective bitrate).<br><br>In UART mode this field should be '0'. |
| 10 | EZ_MODE | RW | R | 0 | Non EZ mode ('0') or EZ mode ('1').<br>In EZ mode, a meta protocol is applied to the serial interface protocol. This meta protocol adds meaning to the data frames transferred by the serial interface protocol: a data frame can represent a memory address, a write memory data element or a read memory data element. EZ mode is only used for synchronous serial interface protocols: SPI and I2C. In SPI mode, only Motorola submode (all Motorola modes: 0, 1, 2, 3) is supported and the transmitter should use continuous data frames; i.e. data frames not separated by slave deselection. This mode is only applicable to slave functionality. In EZ mode, the slave can read from and write to an addressable memory structure of 32 bytes. In EZ mode, data frames should 8-bit in size and should be transmitted and received with the Most Significant Bit (MSB) first.<br><br>In UART mode this field should be '0'. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 12 | CMD_RESP_MODE | RW | R | 0 | Determines CMD_RESP mode of operation:<br>'0': CMD_RESP mode disabled.<br>'1': CMD_RESP mode enabled (also requires EC_AM_MODE and EC_OP_MODE to be set to '1'). |
| 14:15 | MEM_WIDTH | RW | R | 1 | Determines the number of bits per FIFO data element. |
| | BYTE | | | 0 | 8-bit FIFO data elements.<br>This mode provides the biggest amount of FIFO entries, but TX_CTRL.DATA_WIDTH and RX_CTRL.DATA_WIDTH are restricted to [0, 7]. |
| | HALFWORD | | | 1 | 16-bit FIFO data elements.<br>TX_CTRL.DATA_WIDTH and RX_CTRL.DATA_WIDTH are restricted to [0, 15]. |
| | WORD | | | 2 | 32-bit FIFO data elements.<br>This mode provides the smallest amount of FIFO entries, but TX_CTRL.DATA_WIDTH and RX_CTRL.DATA_WIDTH can be in a range of [0, 31]. |
| | Reserved | | | 3 | N/A |
| 16 | ADDR_ACCEPT | RW | R | 0 | Determines whether a received matching address is accepted in the RX FIFO ('1') or not ('0').<br><br>In I2C mode, this field is used to allow the slave to put the received slave address or general call address in the RX FIFO. Note that a received matching address is put in the RX FIFO when this bit is '1' for both I2C read and write transfers.<br><br>In multi-processor UART receiver mode, this field is used to allow the receiver to put the received address in the RX FIFO. Note: non-matching addresses are never put in the RX FIFO. |
| 17 | BLOCK | RW | R | 0 | Only used in externally clocked mode. If the externally clocked logic and the internal CPU accesses to EZ memory coincide/collide, this bit determines whether the CPU access should block and result in bus wait states ('BLOCK is 1') or not (BLOCK is '0'). IF BLOCK is '0' and the accesses collide, CPU read operations return 0xffff:ffff and CPU write operations are ignored. Colliding accesses are registered as interrupt causes: INTR_TX.BLOCKED and INTR_RX.BLOCKED. |
| 24:25 | MODE | RW | R | 3 | Mode of operation (3: Reserved) |
| | I2C | | | 0 | Inter-Integrated Circuits (I2C) mode. |
| | SPI | | | 1 | Serial Peripheral Interface (SPI) mode. |
| | UART | | | 2 | Universal Asynchronous Receiver/Transmitter (UART) mode. |
| 28 | EC_ACCESS | RW | R | 0 | EC_ACCESS is used to enable I2CS_EC or SPIS_EC access to internal EZ memory.<br>1: enable clk_scb<br>0: disable clk_scb<br><br>Before going to deepsleep this field should be set to 1. when waking up from DeepSleep power mode, and PLL is locked (clk_scb is at expected frequency), this filed should be set to 0. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 31 | ENABLED | RW | R | 0 | SCB block is enabled ('1') or not ('0'). The proper order in which to initialize SCB is as follows:<br>- Program protocol specific information using SPI_CTRL, UART_CTRL (and UART_TX_CTRL and UART_RX_CTRL) or I2C_CTRL registers. This includes selection of a submode, master/slave functionality and transmitter/receiver functionality when applicable.<br>- Program generic transmitter (TX_CTRL) and receiver (RX_CTRL) information. This includes enabling of the transmitter and receiver functionality.<br>- Program transmitter FIFO (TX_FIFO_CTRL) and receiver FIFO (RX_FIFO_CTRL) information.<br>- Program CTRL register to enable SCB, select the specific operation mode and oversampling factor.<br>Generally when this block is enabled, no control information should be changed. Changes should be made AFTER disabling this block, e.g. to modify the operation mode (from I2C to SPI) or to go from externally to internally clocked. The change takes effect after the block is re-enabled. Note that disabling the block will cause re-initialization of the design and associated state is lost (e.g. FIFO content).<br><br>Specific to SPI master case, when SCB is idle, below registers can be changed without disabling SCB block,<br>TX_CTRL<br>TX_FIFO_CTRL<br>RX_CTRL<br>RX_FIFO_CTRL<br>SPI_CTRL.SSEL, |

### 26.12.2 SCB_STATUS

**Description:** Generic status
**Address:** 0x40600004
**Offset:** 0x4
**Retention:** Not Retained
**IsDeepSleep:** No ( supported for SCB0_STATUS )
**Comment:**
**Default:** Undefined as one or more bit fields have a default value that is undefined

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:1] | | | | | | | EC_BUSY [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | EC_BUSY | R | W | Undefined | Indicates whether the externally clocked logic is potentially accessing the EZ memory (this is only possible in EZ mode). This bit can be used by SW to determine whether it is safe to issue a SW access to the EZ memory (without bus wait states (a blocked SW access) or bus errors being generated). Note that the INTR_TX.BLOCKED and INTR_RX.BLOCKED interrupt causes are used to indicate whether a SW access was actually blocked by externally clocked logic. |

### 26.12.3 SCB_CMD_RESP_CTRL

**Description:** Command/response control
**Address:** 0x40600008
**Offset:** 0x8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | BASE_RD_ADDR [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | BASE_WR_ADDR [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | BASE_RD_ADDR | RW | R | 0 | I2C/SPI read base address for CMD_RESP mode. At the start of a read transfer this BASE_RD_ADDR is copied to CMD_RESP_STATUS.CURR_RD_ADDR. This field should not be modified during ongoing bus transfers. |
| 16:23 | BASE_WR_ADDR | RW | R | 0 | I2C/SPI write base address for CMD_RESP mode. At the start of a write transfer this BASE_WR_ADDR is copied to CMD_RESP_STATUS.CURR_WR_ADDR. This field should not be modified during ongoing bus transfers. |

### 26.12.4 SCB_CMD_RESP_STATUS

**Description:** Command/response status
**Address:** 0x4060000C
**Offset:** 0xC
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** The register fields reflect register states without a default/reset value (CURR_RD_ADDR and CURR_WR_ADDR) or reflect an external bus state. Therefore, these registers are undefined after the IP is enabled.
**Default:** Undefined as one or more bit fields have a default value that is undefined

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | CURR_RD_ADDR [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | CURR_WR_ADDR [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | CMD_RESP_EC_BUSY [31:31] | CMD_RESP_EC_BUS_BUSY [30:30] | None [29:24] | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | CURR_RD_ADDR | R | W | Undefined | I2C/SPI read current address for CMD_RESP mode. HW increments the field after a read access to the memory buffer. However, when the last memory buffer address is reached, the address is NOT incremented (but remains at the maximum memory buffer address).<br><br>The field is used to determine how many bytes have been read (# bytes = CURR_RD_ADDR - CMD_RESP_CTRL.BASE_RD_ADDR).<br><br>This field is reliable when there is no bus transfer. This field is potentially unreliable when there is a ongoing bus transfer, i.e. when CMD_RESP_EC_BUSY is '0', the field is reliable. |
| 16:23 | CURR_WR_ADDR | R | W | Undefined | I2C/SPI write current address for CMD_RESP mode. HW increments the field after a write access to the memory buffer. However, when the last memory buffer address is reached, the address is NOT incremented (but remains at the maximum memory buffer address).<br><br>The field is used to determine how many bytes have been written (# bytes = CURR_WR_ADDR - CMD_RESP_CTRL.BASE_WR_ADDR).<br><br>This field is reliable when there is no bus transfer. This field is potentially unreliable when there is a ongoing bus transfer, i.e. when CMD_RESP_EC_BUSY is '0', the field is reliable. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 30 | CMD_RESP_EC_BUS_BUSY | R | W | Undefined | Indicates whether there is an ongoing bus transfer to the IP.<br>'0': no ongoing bus transfer.<br>'1': ongoing bus transfer.<br><br>For SPI, the field is '1' when slave mode is selected.<br><br>For I2C, the field is set to '1' at a I2C START/RESTART. In case of an address match, the field is set to '0' on a I2C STOP. In case of NO address match, the field is set to '0' after the failing address match. |
| 31 | CMD_RESP_EC_BUSY | R | W | Undefined | Indicates whether the CURR_RD_ADDR and CURR_WR_ADDR fields in this register are reliable (when CMD_RESP_EC_BUSY is '0') or not reliable (when CMD_RESP_EC_BUSY is '1'). Note:<br>- When there is no ongoing bus transfer, CMD_RESP_EC_BUSY is '0' (reliable).<br>- When there is a ongoing bus transfer, CMD_RESP_EC_BUSY is '0' (reliable), when the CURR_RD_ADDR and CURR_WR_ADDR are not being updated by the HW.<br>- When there is a ongoing bus transfer, CMD_RESP_EC_BUSY is '1' (not reliable), when the CURR_RD_ADDR or CURR_WR_ADDR are being updated by the HW.<br>Note that this update lasts one I2C clock cycle, or two SPI clock cycles. |

### 26.12.5 SCB_SPI_CTRL

**Description:** SPI control
**Address:** 0x40600020
**Offset:** 0x20
**Retention:** Retained
**IsDeepSleep:** No ( supported for SCB0_SPI_CTRL )
**Comment:**
**Default:** 0x3000010

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:6] | | SCLK_CONTINUOUS [5:5] | LATE_MISO_SAMPLE [4:4] | CPOL [3:3] | CPHA [2:2] | SELECT_PRECEDE [1:1] | SSEL_CONTINUOUS [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:15] | SSEL_INTER_FRAME_DEL [14:14] | SSEL_HOLD_DEL [13:13] | SSEL_SETUP_DEL [12:12] | SSEL_POLARITY3 [11:11] | SSEL_POLARITY2 [10:10] | SSEL_POLARITY1 [9:9] | SSEL_POLARITY0 [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:17] | | | | | | | LOOPBACK [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | MASTER_MODE [31:31] | None [30:28] | | | SSEL [27:26] | | MODE [25:24] | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | SSEL_CONTINUOUS | RW | R | 0 | Continuous SPI data transfers enabled ('1') or not ('0'). This field is used in master mode. In slave mode, both continuous and non-continuous SPI data transfers are supported independent of this field.<br><br>When continuous transfers are enabled individual data frame transfers are not necessarily separated by slave deselection (as indicated by the level or pulse on the SELECT line): if the TX FIFO has multiple data frames, data frames are send out without slave deselection.<br><br>When continuous transfers are not enabled individual data frame transfers are always separated by slave deselection: independent of the availability of TX FIFO data frames, data frames are sent out with slave deselection. |
| 1 | SELECT_PRECEDE | RW | R | 0 | Only used in SPI Texas Instruments' submode.<br><br>When '1', the data frame start indication is a pulse on the Slave SELECT line that precedes the transfer of the first data frame bit.<br><br>When '0', the data frame start indication is a pulse on the Slave SELECT line that coincides with the transfer of the first data frame bit. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 2 | CPHA | RW | R | 0 | Indicates the clock phase. This field, together with the CPOL field, indicates when MOSI data is driven and MISO data is captured:<br>- Motorola mode 0. CPOL is '0', CPHA is '0': MOSI is driven on a falling edge of SCLK. MISO is captured on a rising edge of SCLK.<br>- Motorola mode 1. CPOL is '0', CPHA is '1': MOSI is driven on a rising edge of SCLK. MISO is captured on a falling edge of SCLK.<br>- Motorola mode 2. CPOL is '1', CPHA is '0': MOSI is driven on a rising edge of SCLK. MISO is captured on a falling edge of SCLK.<br>- Motorola mode 3. CPOL is '1', CPHA is '1': MOSI is driven on a falling edge of SCLK. MISO is captured on a rising edge of SCLK.<br><br>In SPI Motorola submode, all four CPOL/CPHA modes are valid.<br>in SPI NS submode, only CPOL=0 CPHA=0 mode is valid.<br>in SPI TI submode, only CPOL=0 CPHA=1 mode is valid. |
| 3 | CPOL | RW | R | 0 | Indicates the clock polarity. This field, together with the CPHA field, indicates when MOSI data is driven and MISO data is captured:<br>- CPOL is '0': SCLK is '0' when not transmitting data.<br>- CPOL is '1': SCLK is '1' when not transmitting data. |
| 4 | LATE_MISO_SAMPLE | RW | R | 1 | Changes the SCLK edge on which MISO is captured. Only used in master mode.<br><br>When '0', the default applies (<br>for Motorola as determined by CPOL and CPHA,<br>for Texas Instruments on the falling edge of SCLK and for National Semiconductors on the rising edge of SCLK).<br><br>When '1', the alternate clock edge is used (which comes half a SPI SCLK period later). Late sampling addresses the round trip delay associated with transmitting SCLK from the master to the slave and transmitting MISO from the slave to the master. |
| 5 | SCLK_CONTINUOUS | RW | R | 0 | Only applicable in master mode.<br>'0': SCLK is generated, when the SPI master is enabled and data is transmitted.<br>'1': SCLK is generated, when the SPI master is enabled. This mode is useful for slave devices that use SCLK for functional operation other than just SPI functionality. |
| 8 | SSEL_POLARITY0 | RW | R | 0 | Slave select polarity. SSEL_POLARITY0 applies to the outgoing SPI slave select signal 0 (master mode) and to the incoming SPI slave select signal (slave mode). For Motorola and National Semiconductors submodes:<br><br>'0': slave select is low/'0' active.<br>'1': slave select is high/'1' active.<br>For Texas Instruments submode:<br>'0': high/'1' active precede/coincide pulse.<br>'1': low/'0' active precede/coincide pulse. |
| 9 | SSEL_POLARITY1 | RW | R | 0 | Slave select polarity. |
| 10 | SSEL_POLARITY2 | RW | R | 0 | Slave select polarity. |
| 11 | SSEL_POLARITY3 | RW | R | 0 | Slave select polarity. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 12 | SSEL_SETUP_DEL | RW | R | 0 | Indicates the SPI SELECT setup delay (between SELECT activation and SCLK clock edge to sample the first MOSI bit).<br>'0': 0.75 SPI clock cycles<br>'1': 1.75 SPI clock cycles<br>Only applies in SPI MOTOROLA submode and when SCLK_CONTINUOUS=0, CTRL.OVS>=3.<br><br>above are ideal case at SCB block level, and there is inaccuracy of one clk_scb cycle. |
| 13 | SSEL_HOLD_DEL | RW | R | 0 | Indicates the SPI SELECT hold delay (between SPI clock edge to sample the last MOSI bit, and SELECT deactivation).<br>'0': 0.75 SPI clock cycles<br>'1': 1.75 SPI clock cycles<br>Only applies in SPI MOTOROLA submode and when SCLK_CONTINUOUS=0, CTRL.OVS>=3.<br><br>above are ideal case at SCB block level, and there is inaccuracy of one clk_scb cycle. |
| 14 | SSEL_INTER_FRAME_DEL | RW | R | 0 | Indicates the SPI SELECT inter-dataframe delay (between SELECT deactivation and SELECT activation).<br>'0': 1.5 SPI clock cycles<br>'1': 2.5 SPI clock cycles<br>Only applies in SPI MOTOROLA submode and when SPI_CTRL.SSEL_CONTINUOUS=0, CTRL.OVS>=3.<br><br>above are ideal case at SCB block level, and there is inaccuracy of one clk_scb cycle. |
| 16 | LOOPBACK | RW | R | 0 | Local loopback control (does NOT affect the information on the pins). Only used in master mode. Not used in National Semiconductors submode.<br>'0': No local loopback<br>'1': the SPI master MISO line is connected to the SPI master MOSI line. In other words, in loopback mode the SPI master receives on MISO what it transmits on MOSI. |
| 24:25 | MODE | RW | R | 3 | Submode of SPI operation (3: Reserved). |
| | SPI_MOTOROLA | | | 0 | SPI Motorola submode. In master mode, when not transmitting data (Slave SELECT is inactive), SCLK is stable at CPOL. In slave mode, when not selected, SCLK is ignored; i.e. it can be either stable or clocking. In master mode, when there is no data to transmit (TX FIFO is empty), Slave SELECT is inactive. |
| | SPI_TI | | | 1 | SPI Texas Instruments submode. In master mode, when not transmitting data, SCLK is stable at '0'. In slave mode, when not selected, SCLK is ignored; i.e. it can be either stable or clocking. In master mode, when there is no data to transmit (TX FIFO is empty), Slave SELECT is inactive; i.e. no pulse is generated. |
| | SPI_NS | | | 2 | SPI National Semiconductors submode. In master mode, when not transmitting data, SCLK is stable at '0'. In slave mode, when not selected, SCLK is ignored; i.e. it can be either stable or clocking. In master mode, when there is no data to transmit (TX FIFO is empty), Slave SELECT is inactive. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 26:27 | SSEL | RW | R | 0 | Selects one of the four incoming/outgoing SPI slave select signals:<br>- 0: Slave 0, SSEL[0].<br>- 1: Slave 1, SSEL[1].<br>- 2: Slave 2, SSEL[2].<br>- 3: Slave 3, SSEL[3]. |
| 31 | MASTER_MODE | RW | R | 0 | Master ('1') or slave ('0') mode. In master mode, transmission will commence on availability of data frames in the TX FIFO. In slave mode, when selected and there is no data frame in the TX FIFO, the slave will transmit all '1's. In both master and slave modes, received data frames will be lost if the RX FIFO is full. |

### 26.12.6 SCB_SPI_STATUS

**Description:** SPI status
**Address:** 0x40600024
**Offset:** 0x24
**Retention:** Not Retained
**IsDeepSleep:** No ( supported for SCB0_SPI_STATUS )
**Comment:**
**Default:** Undefined as one or more bit fields have a default value that is undefined

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:2] | | | | | | SPI_EC_BUSY [1:1] | BUS_BUSY [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | CURR_EZ_ADDR [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | BASE_EZ_ADDR [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | BUS_BUSY | R | W | Undefined | SPI bus is busy. The bus is considered busy ('1') during an ongoing transaction. For Motorola and National submodes, the busy bit is '1', when the slave selection is activated. For TI submode, the busy bit is '1' from the time the preceding/coinciding slave select is activated for the first transmitted data frame, till the last MOSI/MISO bit of the last data frame is transmitted. |
| 1 | SPI_EC_BUSY | R | W | Undefined | Indicates whether the externally clocked logic is potentially accessing the EZ memory and/or updating BASE_ADDR or CURR_ADDR (this is only possible in EZ mode). This bit can be used by SW to determine whether BASE_ADDR and CURR_ADDR are reliable. |
| 8:15 | CURR_EZ_ADDR | R | W | Undefined | SPI current EZ address. Current address pointer. This field is only reliable in internally clocked mode. In externally clocked mode the field may be unreliable (during an ongoing transfer when SPI_EC_BUSY is '1'), as clock domain synchronization is not performed in the design. |
| 16:23 | BASE_EZ_ADDR | R | W | Undefined | SPI base EZ address. Address as provided by a SPI write transfer. This field is only reliable in internally clocked mode. In externally clocked mode the field may be unreliable, as clock domain synchronization is not performed in the design. |

### 26.12.7 SCB_SPI_TX_CTRL

**Description:** SPI transmitter control
**Address:** 0x40600028
**Offset:** 0x28
**Retention:** Retained
**IsDeepSleep:** No ( supported for SCB0_SPI_TX_CTRL )
**Comment:** Only applies in SPI MOTOROLA submode, internally clocked SPI operation.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:6] | | PARITY _ENABLED [5:5] | PARITY [4:4] | None [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 4 | PARITY | RW | R | 0 | Parity bit. When '0', the transmitter generates an even parity. When '1', the transmitter generates an odd parity. |
| 5 | PARITY_ENABLED | RW | R | 0 | Parity generation enabled ('1') or not ('0'). |

### 26.12.8 SCB_SPI_RX_CTRL

**Description:** SPI receiver control
**Address:** 0x4060002C
**Offset:** 0x2C
**Retention:** Retained
**IsDeepSleep:** No ( supported for SCB0_SPI_RX_CTRL )
**Comment:** Only applies in SPI MOTOROLA submode, internally clocked SPI operation.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:6] | | PARITY _ENABLED [5:5] | PARITY [4:4] | None [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:9] | | | | | | | DROP_ON _PARITY _ERROR [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 4 | PARITY | RW | R | 0 | Parity bit. When '0', the receiver expects an even parity. When '1', the receiver expects an odd parity. |
| 5 | PARITY_ENABLED | RW | R | 0 | Parity checking enabled ('1') or not ('0'). |
| 8 | DROP_ON_PARITY _ERROR | RW | R | 0 | Behavior when a parity check fails. When '0', received data is send to the RX FIFO. When '1', received data is dropped and lost. |

### 26.12.9 SCB_UART_CTRL

**Description:** UART control
**Address:** 0x40600040
**Offset:** 0x40
**Retention:** Retained
**IsDeepSleep:** No ( supported for SCB0_UART_CTRL )
**Comment:**
**Default:** 0x3000000

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:17] | | | | | | | LOOPBACK [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:26] | | | | | | MODE [25:24] | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 16 | LOOPBACK | RW | R | 0 | Local loopback control (does NOT affect the information on the pins).<br>0: Loopback is not enabled<br>1: UART_TX is connected to UART_RX. UART_RTS is connected to UART_CTS.<br>This allows a SCB UART transmitter to communicate with its receiver counterpart. |
| 24:25 | MODE | RW | R | 3 | Submode of UART operation (3: Reserved) |
| | UART_STD | | | 0 | Standard UART submode. |
| | UART_SMARTCARD | | | 1 | SmartCard (ISO7816) submode. Support for negative acknowledgement (NACK) on the receiver side and retransmission on the transmitter side. |
| | UART_IRDA | | | 2 | Infrared Data Association (IrDA) submode. Return to Zero modulation scheme. In this mode, the oversampling factor should be 16, that is OVS should be set to 15. |

### 26.12.10 SCB_UART_TX_CTRL

**Description:** UART transmitter control
**Address:** 0x40600044
**Offset:** 0x44
**Retention:** Retained
**IsDeepSleep:** No ( supported for SCB0_UART_TX_CTRL )
**Comment:**
**Default:** 0x2

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:6] | | PARITY _ENABLED [5:5] | PARITY [4:4] | None [3:3] | STOP_BITS [2:0] | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:9] | | | | | | | RETRY_ON _NACK [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:2 | STOP_BITS | RW | R | 2 | Stop bits. STOP_BITS + 1 is the duration of the stop period in terms of halve bit periods. Valid range is [1, 7]; i.e. a stop period should last at least one bit period. |
| 4 | PARITY | RW | R | 0 | Parity bit. When '0', the transmitter generates an even parity. When '1', the transmitter generates an odd parity. Only applicable in standard UART and SmartCard submodes. |
| 5 | PARITY_ENABLED | RW | R | 0 | Parity generation enabled ('1') or not ('0'). Only applicable in standard UART submodes. In SmartCard submode, parity generation is always enabled through hardware. In IrDA submode, parity generation is always disabled through hardware |
| 8 | RETRY_ON_NACK | RW | R | 0 | When '1', a data frame is retransmitted when a negative acknowledgement is received. Only applicable to the SmartCard submode. |

### 26.12.11 SCB_UART_RX_CTRL

**Description:** UART receiver control
**Address:** 0x40600048
**Offset:** 0x48
**Retention:** Retained
**IsDeepSleep:** No ( supported for SCB0_UART_RX_CTRL )
**Comment:**
**Default:** 0xA0002

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:7] | POLARITY [6:6] | PARITY _ENABLED [5:5] | PARITY [4:4] | None [3:3] | STOP_BITS [2:0] | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:14] | | SKIP _START [13:13] | LIN_MODE [12:12] | None [11:11] | MP_MODE [10:10] | DROP_ON _FRAME _ERROR [9:9] | DROP_ON _PARITY _ERROR [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:20] | | | | BREAK_WIDTH [19:16] | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:25] | | | | | | | BREAK _LEVEL [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:2 | STOP_BITS | RW | R | 2 | Stop bits. STOP_BITS + 1 is the duration of the stop period in terms of half bit periods. Valid range is [1, 7]; i.e. a stop period should last at least one bit period.<br><br>Note that in case of a stop bits error, the successive data frames may get lost as the receiver needs to resynchronize its start bit detection. The amount of lost data frames depends on both the amount of stop bits, the idle time between data frames and the data frame value. |
| 4 | PARITY | RW | R | 0 | Parity bit. When '0', the receiver expects an even parity. When '1', the receiver expects an odd parity. Only applicable in standard UART and SmartCard submodes. |
| 5 | PARITY_ENABLED | RW | R | 0 | Parity checking enabled ('1') or not ('0'). Only applicable in standard UART submode. In SmartCard submode, parity checking is always enabled through hardware. In IrDA submode, parity checking is always disabled through hardware. |
| 6 | POLARITY | RW | R | 0 | Inverts incoming RX line signal. Inversion is after local loopback. This functionality is intended for IrDA receiver functionality. |
| 8 | DROP_ON_PARITY _ERROR | RW | R | 0 | Behavior when a parity check fails.<br>When '0', received data is sent to the RX FIFO.<br>When '1', received data is dropped and lost.<br>Only applicable in standard UART and SmartCard submodes (negatively acknowledged SmartCard data frames may be dropped with this field). |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 9 | DROP_ON_FRAME_ERROR | RW | R | 0 | Behavior when an error is detected in a start or stop period.<br>When '0', received data is sent to the RX FIFO.<br>When '1', received data is dropped and lost. |
| 10 | MP_MODE | RW | R | 0 | Multi-processor mode. When '1', multi-processor mode is enabled. In this mode, RX_CTRL.DATA_WIDTH should indicate a 9-bit data frame. In multi-processor mode, the 9th received bit of a data frame separates addresses (bit is '1') from data (bit is '0'). A received address is matched with RX_MATCH.DATA and RX_MATCH.MASK. In the case of a match, subsequent received data are sent to the RX FIFO. In the case of NO match, subsequent received data are dropped. |
| 12 | LIN_MODE | RW | R | 0 | Only applicable in standard UART submode. When '1', the receiver performs break detection and baud rate detection on the incoming data. First, break detection counts the amount of bit periods that have a line value of '0'. BREAK_WIDTH specifies the minimum required amount of bit periods. Successful break detection sets the INTR_RX.BREAK_DETECT interrupt cause to '1'. Second, baud rate detection counts the amount of peripheral clock periods that are use to receive the synchronization byte (0x55; least significant bit first). The count is available through UART_RX_STATUS.BR_COUNTER. Successful baud rate detection sets the INTR_RX.BAUD_DETECT interrupt cause to '1' (BR_COUNTER is reliable). This functionality is used to synchronize/refine the receiver clock to the transmitter clock. The receiver software can use the BR_COUNTER value to set the right IP clock (from the programmable clock IP) to guarantee successful receipt of the first LIN data frame (Protected Identifier Field) after the synchronization byte. |
| 13 | SKIP_START | RW | R | 0 | Only applicable in standard UART submode. When '1', the receiver skips start bit detection for the first received data frame. Instead, it synchronizes on the first received data frame bit, which should be a '1'. This functionality is intended for wake up from DeepSleep when receiving a data frame. The transition from idle ('1') to START ('0') on the RX line is used to wake up the CPU. The transition detection (and the associated wake up functionality) is performed by the GPIO2 IP. The woken up CPU will enable the SCB's UART receiver functionality. Once enabled, it is assumed that the START bit is ongoing (the CPU wakeup and SCB enable time should be less than the START bit period). The SCB will synchronize to a '0' to '1' transition, which indicates the first data frame bit is received (first data frame bit should be '1'). After synchronization to the first data frame bit, the SCB will resume normal UART functionality: subsequent data frames will be synchronized on the receipt of a START bit. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 16:19 | BREAK_WIDTH | RW | R | 10 | Break width. BREAK_WIDTH + 1 is the minimum width in bit periods of a break. During a break the transmitted/received line value is '0'. This feature is useful for standard UART submode and LIN submode ('break field' detection). Once, the break is detected, the INTR_RX.BREAK_DETECT bit is set to '1'. Note that break detection precedes baud rate detection, which is used to synchronize/refine the receiver clock to the transmitter clock. As a result, break detection operates with an unsynchronized/unrefined receiver clock. Therefore, the receiver's definition of a bit period is imprecise and the setting of this field should take this imprecision into account. The LIN standard also accounts for this imprecision: a LIN start bit followed by 8 data bits allows for up to 9 consecutive '0' bit periods during regular transmission, whereas the LIN break detection should be at least 13 consecutive '0' bit periods. This provides for a margin of 4 bit periods. Therefore, the default value of this field is set to 10, representing a minimal break field with of 10+1 = 11 bit periods; a value in between the 9 consecutive bit periods of a regular transmission and the 13 consecutive bit periods of a break field. This provides for slight imprecisions of the receiver clock wrt. the transmitter clock. There should not be a need to program this field to any value other than its default value. |
| 24 | BREAK_LEVEL | RW | R | 0 | 0: low level pulse detection, like Break field in LIN protocol<br>1: high level pulse detection, like IFS field in CXPI protocol, or idle line state in UART |

### 26.12.12 SCB_UART_RX_STATUS

**Description:** UART receiver status
**Address:** 0x4060004C
**Offset:** 0x4C
**Retention:** Not Retained
**IsDeepSleep:** No ( supported for SCB0_UART_RX_STATUS )
**Comment:**
**Default:** Undefined as one or more bit fields have a default value that is undefined

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | BR_COUNTER [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:12] | | | | BR_COUNTER [11:8] | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:11 | BR_COUNTER | R | W | Undefined | Amount of SCB clock periods that constitute the transmission of a 0x55 data frame (sent least significant bit first) as determined by the receiver. BR_COUNTER / 8 is the amount of SCB clock periods that constitute a bit period. This field has valid data when INTR_RX.BAUD_DETECT is set to '1'. |

### 26.12.13 SCB_UART_FLOW_CTRL

**Description:** UART flow control
**Address:** 0x40600050
**Offset:** 0x50
**Retention:** Retained
**IsDeepSleep:** No ( supported for SCB0_UART_FLOW_CTRL )
**Comment:** UART flow control is a design time configuration parameter, which make the presence of this MMIO register conditional to the configuration. The 'uart_rts_out' and 'uart_cts_in' are always present on the IP interface. If flow control is configured out, 'uart_rts_out' is NOT connected, and 'uart_cts_in' should be connected to '0'.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:7] | TRIGGER_LEVEL [6:0] | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:17] | | | | | | | RTS_POLARITY [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:26] | | | | | | CTS_ENABLED [25:25] | CTS_POLARITY [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:6 | TRIGGER_LEVEL | RW | R | 0 | Trigger level. When the receiver FIFO has less entries than the amount of this field, a Ready To Send (RTS) output signal is activated. By setting this field to '0', flow control is effectively disabled (may be useful for debug purposes). |
| 16 | RTS_POLARITY | RW | R | 0 | Polarity of the RTS output signal:<br>'0': RTS is active low;<br>'1': RTS is active high;<br><br>During SCB reset (Hibernate system power mode), RTS output signal is '1'. This represents an inactive state assuming an active low polarity. |
| 24 | CTS_POLARITY | RW | R | 0 | Polarity of the CTS input signal<br>'0': CTS is active low ;<br>'1': CTS is active high; |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 25 | CTS_ENABLED | RW | R | 0 | Enable use of CTS input signal by the UART transmitter:<br>'0': Disabled. The UART transmitter ignores the CTS input signal and transmits when a data frame is available for transmission in the TX FIFO or the TX shift register.<br>'1': Enabled. The UART transmitter uses CTS input signal to qualify the transmission of data. It transmits when CTS input signal is active and a data frame is available for transmission in the TX FIFO or the TX shift register.<br><br>If UART_CTRL.LOOPBACK is '1', the CTS input signal is driven by the RTS output signal locally in SCB (both signals are subjected to signal polarity changes are indicated by RTS_POLARITY and CTS_POLARITY). |

### 26.12.14 SCB_I2C_CTRL

**Description:** I2C control
**Address:** 0x40600060
**Offset:** 0x60
**Retention:** Retained
**IsDeepSleep:** No ( supported for SCB0_I2C_CTRL )
**Comment:**
**Default:** 0xFB88

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | LOW_PHASE_OVS [7:4] | | | | HIGH_PHASE_OVS [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | S_NOT_READY_DATA_NACK [15:15] | S_NOT_READY_ADDR_NACK [14:14] | S_READY_DATA_ACK [13:13] | S_READY_ADDR_ACK [12:12] | S_GENERAL_IGNORE [11:11] | None [10:10] | M_NOT_READY_DATA_NACK [9:9] | M_READY_DATA_ACK [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:17] | | | | | | | LOOPBACK [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | MASTER_MODE [31:31] | SLAVE_MODE [30:30] | None [29:24] | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | HIGH_PHASE_OVS | RW | R | 8 | Serial I2C interface high phase oversampling factor. HIGH_PHASE_OVS + 1 SCB clock periods constitute the high phase of a bit period. The valid range is [5, 15] with input signal median filtering and [4, 15] without input signal median filtering.<br><br>The field is only used in master mode. In slave mode, the field is NOT used. However, there is a frequency requirement for the SCB clock wrt. the regular interface (IF) high time to guarantee functional correct behavior. With input signal median filtering, the IF high time should be >= 6 SCB clock cycles and <= 16 SCB clock cycles. Without input signal median filtering, the IF high time should be >= 5 SCB clock cycles and <= 16 SCB clock cycles. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 4:7 | LOW_PHASE_OVS | RW | R | 8 | Serial I2C interface low phase oversampling factor. LOW_PHASE_OVS + 1 SCB clock periods constitute the low phase of a bit period. The valid range is [7, 15] with input signal median filtering and [6, 15] without input signal median filtering.<br><br>The field is only used in master mode. In slave mode, the field is NOT used. However, there is a frequency requirement for the SCB clock wrt. the regular (no stretching) interface (IF) low time to guarantee functionally correct behavior. With input signal median filtering, the IF low time should be >= 8 SCB clock cycles and <= 16 IP clock cycles. Without input signal median filtering, the IF low time should be >= 7 SCB clock cycles and <= 16 SCB clock cycles.<br><br>in slave mode, this field is used to define number of clk_scb cycles for tSU-DAT timing (from ACK/NACK/data ready, to SCL rising edge (released from I2C slave clock stretching)) |
| 8 | M_READY_DATA_ACK | RW | R | 1 | When '1', a received data element by the master is immediately ACK'd when the receiver FIFO is not full. |
| 9 | M_NOT_READY_DATA_NACK | RW | R | 1 | When '1', a received data element byte the master is immediately NACK'd when the receiver FIFO is full. When '0', clock stretching is used instead (till the receiver FIFO is no longer full). |
| 11 | S_GENERAL_IGNORE | RW | R | 1 | When '1', a received general call slave address is immediately NACK'd (no ACK or clock stretching) and treated as a non matching slave address. This is useful for slaves that do not need any data supplied within the general call structure. |
| 12 | S_READY_ADDR_ACK | RW | R | 1 | When '1', a received (matching) slave address is immediately ACK'd when the receiver FIFO is not full. In EZ mode, this field should be set to '1'. |
| 13 | S_READY_DATA_ACK | RW | R | 1 | When '1', a received data element by the slave is immediately ACK'd when the receiver FIFO is not full. In EZ mode, this field should be set to '1'. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 14 | S_NOT_READY_ADDR_NACK | RW | R | 1 | This field is used during an address match or general call address in internally clocked mode<br>Only used when:<br>- EC_AM_MODE is '0', EC_OP_MODE is '0', S_GENERAL_IGNORE is '0] and non EZ mode.<br>Functionality is as follows:<br>- 1: a received (matching) slave address is immediately NACK'd when the receiver FIFO is full.<br>- 0: clock stretching is performed (till the receiver FIFO is no longer full).<br><br>For externally clocked logic (EC_AM is '1') on an address match or general call address (and S_GENERAL_IGNORE is '0'). Only used when (NOT used when EC_AM is '1' and EC_OP is '1' and address match and EZ mode):<br>- EC_AM is '1' and EC_OP is '0'.<br>- EC_AM is '1' and general call address match.<br>- EC_AM is '1' and non EZ mode.<br>Functionality is as follows:<br>- 1: a received (matching or general) slave address is always immediately NACK'd. There are two possibilities:<br>1). the SCB clock is available (in Active system power mode) and it handles the rest of the current transfer. In this case the I2C master will not observe the NACK.<br>2).SCB clock is not present (in DeepSleep system power mode). In this case the I2C master will observe the NACK and may retry the transfer in the future (which gives the internally clocked logic the time to wake up from DeepSleep system power mode).<br>- 0: clock stretching is performed (till the SCB clock is available). The logic will handle the ongoing transfer as soon as the clock is enabled. |
| 15 | S_NOT_READY_DATA_NACK | RW | R | 1 | Only used when:<br>- non EZ mode<br>Functionality is as follows:<br>- 1: a received data element byte the slave is immediately NACK'd when the receiver FIFO is full.<br>- 0: clock stretching is performed (till the receiver FIFO is no longer full). |
| 16 | LOOPBACK | RW | R | 0 | Local loopback control (does NOT affect the information on the pins). Only applicable in master/slave mode.<br>When '0', no loopback<br>When '1', loopback is enabled internally in the peripheral, and as a result unaffected by other I2C devices. This allows a SCB I2C peripheral to address itself. |
| 30 | SLAVE_MODE | RW | R | 0 | Slave mode enabled ('1') or not ('0'). |
| 31 | MASTER_MODE | RW | R | 0 | Master mode enabled ('1') or not ('0'). Note that both master and slave modes can be enabled at the same time. This allows the IP to address itself. |

### 26.12.15 SCB_I2C_STATUS

**Description:** I2C status
**Address:** 0x40600064
**Offset:** 0x64
**Retention:** Not Retained
**IsDeepSleep:** No ( supported for SCB0_I2C_STATUS )
**Comment:**
**Default:** Undefined as one or more bit fields have a default value that is undefined

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:6] | | M_READ [5:5] | S_READ [4:4] | None [3:3] | I2CS_IC_BUSY [2:2] | I2C_EC_BUSY [1:1] | BUS_BUSY [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | CURR_EZ_ADDR [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | BASE_EZ_ADDR [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | BUS_BUSY | R | W | 0 | I2C bus is busy. The bus is considered busy ('1'), from the time a START is detected or from the time the SCL line is '0'. The bus is considered idle ('0'), from the time a STOP is detected. If SCB block is disabled, BUS_BUSY is '0'. After enabling the block, it takes time for the BUS_BUSY to detect a busy bus. This time is the maximum high time of the SCL line. For a 100 kHz interface frequency, this maximum high time may last roughly 5 us (half a bit period).<br><br>For single master systems, BUS_BUSY does not have to be used to detect an idle bus before a master starts a transfer using I2C_M_CMD.M_START (no bus collisions).<br><br>For multi-master systems, BUS_BUSY can be used to detect an idle bus before a master starts a transfer using I2C_M_CMD.M_START_ON_IDLE (to prevent bus collisions). |
| 1 | I2C_EC_BUSY | R | W | Undefined | Indicates whether the externally clocked logic is potentially accessing the EZ memory and/or updating BASE_EZ_ADDR or CURR_EZ_ADDR (this is only possible in EZ mode). This bit can be used by SW to determine whether BASE_EZ_ADDR and CURR_EZ_ADDR are reliable. |
| 2 | I2CS_IC_BUSY | R | W | 0 | Indicates whether the internally clocked slave logic is being accessed by external I2C master.<br>--set at ADDR_MATCH<br>--clear at START/RESET, STOP detection, or BUS_ERROR<br>This bit can be used by SW to determine whether I2CS_IC is busy before entering DeepSleep. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 4 | S_READ | R | W | 0 | I2C slave read transfer ('1') or I2C slave write transfer ('0'). When the I2C slave is inactive/idle or receiving START, REPEATED START, STOP or an address, this field is '0". |
| 5 | M_READ | R | W | 0 | I2C master read transfer ('1') or I2C master write transfer ('0'). When the I2C master is inactive/idle or transmitting START, REPEATED START, STOP or an address, this field is '0". |
| 8:15 | CURR_EZ_ADDR | R | W | Undefined | I2C slave current EZ address. Current address pointer. This field is only reliable in internally clocked mode. In externally clocked mode the field may be unreliable (during an ongoing transfer when I2C_EC_BUSY is '1'), as clock domain synchronization is not performed in the design. |
| 16:23 | BASE_EZ_ADDR | R | W | Undefined | I2C slave base EZ address. Address as provided by an I2C write transfer. This field is only reliable in internally clocked mode. In externally clocked mode the field may be unreliable, as clock domain synchronization is not performed in the design. |

### 26.12.16 SCB_I2C_M_CMD

**Description:** I2C master command
**Address:** 0x40600068
**Offset:** 0x68
**Retention:** Not Retained
**IsDeepSleep:** No ( supported for SCB0_I2C_M_CMD )
**Comment:** The register fields are not retained. This is to ensure that they come up as '0' after coming out of DeepSleep system power mode.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:5] | | | M_STOP [4:4] | M_NACK [3:3] | M_ACK [2:2] | M_START_ON_IDLE [1:1] | M_START [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | M_START | RW | RW1C | 0 | When '1', transmit a START or REPEATED START. Whether a START or REPEATED START is transmitted depends on the state of the master state machine. A START is only transmitted when the master state machine is in the default state. A REPEATED START is transmitted when the master state machine is not in the default state, but is working on an ongoing transaction. The REPEATED START can only be transmitted after a NACK or ACK has been received for a transmitted data element or after a NACK has been transmitted for a received data element. When this action is performed, the hardware sets this field to '0'. |
| 1 | M_START_ON_IDLE | RW | RW1C | 0 | When '1', transmit a START as soon as the bus is idle (I2C_STATUS.BUS_BUSY is '0', note that BUSY has a default value of '0'). For bus idle detection the hardware relies on STOP detection. As a result, bus idle detection is only functional after at least one I2C bus transfer has been detected on the bus (default/reset value of BUSY is '0') . A START is only transmitted when the master state machine is in the default state. When this action is performed, the hardware sets this field to '0'. |
| 2 | M_ACK | RW | RW1C | 0 | When '1', attempt to transmit an acknowledgement (ACK). When this action is performed, the hardware sets this field to '0'. |
| 3 | M_NACK | RW | RW1C | 0 | When '1', attempt to transmit a negative acknowledgement (NACK). When this action is performed, the hardware sets this field to '0'. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 4 | M_STOP | RW | RW1C | 0 | When '1', attempt to transmit a STOP. When this action is performed, the hardware sets this field to '0'. I2C_M_CMD.M_START has a higher priority than this command: in situations where both a STOP and a REPEATED START could be transmitted, M_START takes precedence over M_STOP. |

### 26.12.17 SCB_I2C_S_CMD

**Description:** I2C slave command
**Address:** 0x4060006C
**Offset:** 0x6C
**Retention:** Not Retained
**IsDeepSleep:** No ( supported for SCB0_I2C_S_CMD )
**Comment:** The register fields are not retained. This is to ensure that they come up as '0' after coming out of DeepSleep system power mode.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:2] | | | | | | S_NACK [1:1] | S_ACK [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | S_ACK | RW | RW1C | 0 | When '1', attempt to transmit an acknowledgement (ACK). When this action is performed, the hardware sets this field to '0'. In EZ mode, this field should be set to '0' (it is only to be used in non EZ mode). |
| 1 | S_NACK | RW | RW1C | 0 | When '1', attempt to transmit a negative acknowledgement (NACK). When this action is performed, the hardware sets this field to '0'. In EZ mode, this field should be set to '0' (it is only to be used in non EZ mode). This command has a higher priority than I2C_S_CMD.S_ACK, I2C_CTRL.S_READY_ADDR_ACK or I2C_CTRL.S_READY_DATA_ACK. |

### 26.12.18 SCB_I2C_CFG

**Description:** I2C configuration
**Address:** 0x40600070
**Offset:** 0x70
**Retention:** Retained
**IsDeepSleep:** No ( supported for SCB0_I2C_CFG )
**Comment:** The filters are used to remove glitches and to guarantee I2C compliant SCL and SDA setup and hold times. The filters are trimmable.
**Default:** 0x2A1013

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:5] | | | SDA_IN_FILT_SEL [4:4] | None [3:2] | | SDA_IN_FILT_TRIM [1:0] | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:13] | | | SCL_IN_FILT_SEL [12:12] | None [11:10] | | SCL_IN_FILT_TRIM [9:8] | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:22] | | SDA_OUT_FILT2_TRIM [21:20] | | SDA_OUT_FILT1_TRIM [19:18] | | SDA_OUT_FILT0_TRIM [17:16] | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:30] | | SDA_OUT_FILT_SEL [29:28] | | None [27:24] | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:1 | SDA_IN_FILT_TRIM | RW | R | 3 | Trim settings for the 50ns glitch filter on the SDA input. Default setting meets the I2C glitch rejections specs. Programmability available if required |
| 4 | SDA_IN_FILT_SEL | RW | R | 1 | Enable for 50ns glitch filter on SDA input<br>'0': 0 ns.<br>'1: 50 ns (filter enabled). |
| 8:9 | SCL_IN_FILT_TRIM | RW | R | 0 | Trim settings for the 50ns glitch filter on the SDA input. Default setting meets the I2C glitch rejections specs. Programmability available if required |
| 12 | SCL_IN_FILT_SEL | RW | R | 1 | Enable for 50ns glitch filter on SCL input<br>'0': 0 ns.<br>'1: 50 ns (filter enabled). |
| 16:17 | SDA_OUT_FILT0_TRIM | RW | R | 2 | Trim settings for the 50ns delay filter on SDA output used to guarantee tHD_DAT I2C parameter. Default setting meets the I2C spec. Programmability available if required |
| 18:19 | SDA_OUT_FILT1_TRIM | RW | R | 2 | Trim settings for the 50ns delay filter on SDA output used to guarantee tHD_DAT I2C parameter. Default setting meets the I2C spec. Programmability available if required |
| 20:21 | SDA_OUT_FILT2_TRIM | RW | R | 2 | Trim settings for the 50ns delay filter on SDA output used to guarantee tHD_DAT I2C parameter. Default setting meets the I2C spec. Programmability available if required |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 28:29 | SDA_OUT_FILT_SEL | RW | R | 0 | Selection of cumulative filter delay on SDA output to meet tHD_DAT parameter<br>'0': 0 ns.<br>'1': 50 ns (filter 0 enabled).<br>'2': 100 ns (filters 0 and 1 enabled).<br>'3': 150 ns (filters 0, 1 and 2 enabled). |

### 26.12.19 SCB_TX_CTRL

**Description:** Transmitter control
**Address:** 0x40600200
**Offset:** 0x200
**Retention:** Retained
**IsDeepSleep:** No ( supported for SCB0_TX_CTRL )
**Comment:**
**Default:** 0x107

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:5] | | | DATA_WIDTH [4:0] | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:9] | | | | | | | MSB _FIRST [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:17] | | | | | | | OPEN _DRAIN [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:4 | DATA_WIDTH | RW | R | 7 | Dataframe width. DATA_WIDTH + 1 is the amount of bits in a transmitted data frame. This number does not include start, parity and stop bits. For UART mode, the valid range is [3, 8]. For SPI, the valid range is [3, 31]. For I2C the only valid value is 7. |
| 8 | MSB_FIRST | RW | R | 1 | Least significant bit first ('0') or most significant bit first ('1'). For I2C, this field should be '1'. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 16 | OPEN_DRAIN | RW | R | 0 | Each IO cell 'xxx' has two associated IP output signals 'xxx_out_en' and 'xxx_out'.<br>'0': Normal operation mode. Typically, this operation mode is used for IO cells that are connected to (board) wires/lines that are driven by a single IO cell. In this operation mode, for an IO cell 'xxx' that is used as an output, the 'xxx_out_en' output enable signal is typically constant '1' the 'xxx_out' output is the outputted value. In other words, in normal operation mode, the 'xxx_out' output is used to control the IO cell output value: 'xxx_out' is '0' to drive an IO cell output value of '0' and 'xxx_out' is '1' to drive an IO cell output value of '1'.<br>'1': Open drain operation mode. Typically this operation mode is used for IO cells that are connected to (board) wires/lines that are driven by multiple IO cells (possibly on multiple chips). In this operation mode, for and IO cell 'xxx' that is used as an output, the 'xxx_out_en' output controls the outputted value. Typically, open drain operation mode drives low/'0' and the 'xxx_out' output is constant '1'. In other words, in open drain operation mode, the 'xxx_out_en' output is used to control the IO cell output value: in drive low/'0' mode: 'xxx_out_en' is '1' (drive enabled) to drive an IO cell output value of '0' and 'xxx_out_en' is '1' (drive disabled) to not drive an IO cell output value (another IO cell can drive the wire/line or a pull up results in a wire/line value '1').<br><br>The open drain mode is supported for:<br>- UART mode, 'uart_tx' IO cell.<br>- SPI mode, 'spi_miso' IO cell.<br><br>not applicable to I2C mode, 'i2c_scl' and 'i2c_sda' IO cells. (I2C SCL/SDA always work in open-drain mode) |

### 26.12.20 SCB_TX_FIFO_CTRL

**Description:** Transmitter FIFO control
**Address:** 0x40600204
**Offset:** 0x204
**Retention:** Retained
**IsDeepSleep:** No ( supported for SCB0_TX_FIFO_CTRL )
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:7] | TRIGGER_LEVEL [6:0] | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:18] | | | | | | FREEZE [17:17] | CLEAR [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:6 | TRIGGER_LEVEL | RW | R | 0 | Trigger level. When the transmitter FIFO has less entries than the number of this field, a transmitter trigger event INTR_TX.TRIGGER is generated. |
| 16 | CLEAR | RW | R | 0 | When '1', the transmitter FIFO and transmitter shift register are cleared/invalidated. Invalidation will last for as long as this field is '1'. If a quick clear/invalidation is required, the field should be set to '1' and be followed by a set to '0'. If a clear/invalidation is required for an extended time period, the field should be set to '1' during the complete time period. |
| 17 | FREEZE | RW | R | 0 | When '1', hardware reads from the transmitter FIFO do not remove FIFO entries. Freeze will not advance the TX FIFO read pointer. |

### 26.12.21 SCB_TX_FIFO_STATUS

**Description:** Transmitter FIFO status
**Address:** 0x40600208
**Offset:** 0x208
**Retention:** Not Retained
**IsDeepSleep:** No ( supported for SCB0_TX_FIFO_STATUS )
**Comment:** This register is not used in EZ and CMD_RESP modes.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | USED [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | SR_VALID [15:15] | None [14:8] | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:23] | RD_PTR [22:16] | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:31] | WR_PTR [30:24] | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | USED | R | W | 0 | Amount of entries in the transmitter FIFO. The value of this field ranges from 0 to FF_DATA_NR (EZ_DATA_NR/2). |
| 15 | SR_VALID | R | W | 0 | Indicates whether the TX shift registers holds a valid data frame ('1') or not ('0'). The shift register can be considered the top of the TX FIFO (the data frame is not included in the USED field of the TX FIFO). The shift register is a working register and holds the data frame that is currently transmitted (when the protocol state machine is transmitting a data frame) or the data frame that is transmitted next (when the protocol state machine is not transmitting a data frame). |
| 16:22 | RD_PTR | R | W | 0 | FIFO read pointer: FIFO location from which a data frame is read by the hardware. |
| 24:30 | WR_PTR | R | W | 0 | FIFO write pointer: FIFO location at which a new data frame is written. |

### 26.12.22 SCB_TX_FIFO_WR

**Description:** Transmitter FIFO write
**Address:** 0x40600240
**Offset:** 0x240
**Retention:** Not Retained
**IsDeepSleep:** No ( supported for SCB0_TX_FIFO_WR )
**Comment:** When the IP is disabled (CTRL.ENABLED is '0') or when the TX FIFO is full, a write to this register is dropped. This register should only be used in FIFO mode (and not in EZ or CMD_RESP modes). This register is 'write only'; a read from this register returns '0'.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | DATA | W | R | 0 | Data frame written into the transmitter FIFO. Behavior is similar to that of a PUSH operation. Note that when CTRL.MEM_WIDTH is '0', only DATA[7:0] are used and when CTRL.MEM_WIDTH is '1', only DATA[15:0] are used.<br><br>A write to a full TX FIFO sets INTR_TX.OVERFLOW to '1'. |

### 26.12.23 SCB_RX_CTRL

**Description:** Receiver control
**Address:** 0x40600300
**Offset:** 0x300
**Retention:** Retained
**IsDeepSleep:** No ( supported for SCB0_RX_CTRL )
**Comment:**
**Default:** 0x107

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:5] | | | DATA_WIDTH [4:0] | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:10] | | | | | | MEDIAN [9:9] | MSB _FIRST [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:4 | DATA_WIDTH | RW | R | 7 | Dataframe width. DATA_WIDTH + 1 is the expected amount of bits in received data frame. This number does not include start, parity and stop bits. For UART mode, the valid range is [3, 8]. For SPI, the valid range is [3, 31]. For I2C the only valid value is 7. In EZ mode (for both SPI and I2C), the only valid value is 7. |
| 8 | MSB_FIRST | RW | R | 1 | Least significant bit first ('0') or most significant bit first ('1'). For I2C, this field should be '1'. |
| 9 | MEDIAN | RW | R | 0 | Median filter. When '1', a digital 3 taps median filter is performed on input interface lines. This filter should reduce the susceptibility to errors. However, its requires higher oversampling values. For UART IrDA submode, this field should always be '1'. |

### 26.12.24 SCB_RX_FIFO_CTRL

**Description:** Receiver FIFO control
**Address:** 0x40600304
**Offset:** 0x304
**Retention:** Retained
**IsDeepSleep:** No ( supported for SCB0_RX_FIFO_CTRL )
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:7] | TRIGGER_LEVEL [6:0] | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:18] | | | | | | FREEZE [17:17] | CLEAR [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:6 | TRIGGER_LEVEL | RW | R | 0 | Trigger level. When the receiver FIFO has more entries than the number of this field, a receiver trigger event INTR_RX.TRIGGER is generated. |
| 16 | CLEAR | RW | R | 0 | When '1', the receiver FIFO and receiver shift register are cleared/invalidated. Invalidation will last for as long as this field is '1'. If a quick clear/invalidation is required, the field should be set to '1' and be followed by a set to '0'. If a clear/invalidation is required for an extended time period, the field should be set to '1' during the complete time period. |
| 17 | FREEZE | RW | R | 0 | When '1', hardware writes to the receiver FIFO have no effect. Freeze will not advance the RX FIFO write pointer. |

### 26.12.25 SCB_RX_FIFO_STATUS

**Description:** Receiver FIFO status
**Address:** 0x40600308
**Offset:** 0x308
**Retention:** Not Retained
**IsDeepSleep:** No ( supported for SCB0_RX_FIFO_STATUS )
**Comment:** This register is not used in EZ and CMD_RESP modes.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | USED [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | SR_VALID [15:15] | None [14:8] | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:23] | RD_PTR [22:16] | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:31] | WR_PTR [30:24] | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | USED | R | W | 0 | Amount of entries in the receiver FIFO. The value of this field ranges from 0 to FF_DATA_NR (EZ_DATA_NR/2). |
| 15 | SR_VALID | R | W | 0 | Indicates whether the RX shift registers holds a (partial) valid data frame ('1') or not ('0'). The shift register can be considered the bottom of the RX FIFO (the data frame is not included in the USED field of the RX FIFO). The shift register is a working register and holds the data frame that is currently being received (when the protocol state machine is receiving a data frame). |
| 16:22 | RD_PTR | R | W | 0 | FIFO read pointer: FIFO location from which a data frame is read. |
| 24:30 | WR_PTR | R | W | 0 | FIFO write pointer: FIFO location at which a new data frame is written by the hardware. |

### 26.12.26 SCB_RX_MATCH

**Description:** Slave address and mask
**Address:** 0x40600310
**Offset:** 0x310
**Retention:** Retained
**IsDeepSleep:** No ( supported for SCB0_RX_MATCH )
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDR [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | MASK [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | ADDR | RW | R | 0 | Slave device address.<br><br>In UART multi-processor mode, all 8 bits are used.<br><br>In I2C slave mode, only bits 7 down to 1 are used. This reflects the organization of the first transmitted byte in a I2C transfer: the first 7 bits represent the address of the addressed slave, and the last 1 bit is a read/write indicator ('0': write, '1': read). |
| 16:23 | MASK | RW | R | 0 | Slave device address mask. This field is a mask that specifies which of the slave address bits take part in the matching. MATCH = ((ADDR & MASK) == ('slave address' & MASK)). |

### 26.12.27 SCB_RX_FIFO_RD

**Description:** Receiver FIFO read
**Address:** 0x40600340
**Offset:** 0x340
**Retention:** Not Retained
**IsDeepSleep:** No ( supported for SCB0_RX_FIFO_RD )
**Comment:** When the IP is disabled (CTRL.ENABLED is '0') or when the RX FIFO is empty, a read from this register returns 0xffff:ffff. This register should only be used in FIFO mode (and not in EZ or CMD_RESP modes). This register is 'read only'; a write to this register is ignored.
**Default:** Undefined as one or more bit fields have a default value that is undefined

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | DATA | R | W | Undefined | Data read from the receiver FIFO. Reading a data frame will remove the data frame from the FIFO; i.e. behavior is similar to that of a POP operation. Note that when CTRL.MEM_WIDTH is '0', only DATA[7:0] are used and when CTRL.MEM_WIDTH is '1', only DATA[15:0] are used<br><br>A read from an empty RX FIFO sets INTR_RX.UNDERFLOW to '1'.<br><br>When this register is read through the debugger, the data frame will not be removed from the FIFO. Similar in operation to RX_FIFO_RD_SILENT |

### 26.12.28 SCB_RX_FIFO_RD_SILENT

**Description:** Receiver FIFO read silent
**Address:** 0x40600344
**Offset:** 0x344
**Retention:** Not Retained
**IsDeepSleep:** No ( supported for SCB0_RX_FIFO_RD_SILENT )
**Comment:** When the IP is disabled (CTRL.ENABLED is '0') or when the RX FIFO is empty, a read from this register returns 0xffff:ffff. This register should only be used in FIFO mode (and not in EZ or CMD_RESP modes).
**Default:** Undefined as one or more bit fields have a default value that is undefined

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | DATA | R | W | Undefined | Data read from the receiver FIFO. Reading a data frame will NOT remove the data frame from the FIFO; i.e. behavior is similar to that of a PEEK operation. Note that when CTRL.MEM_WIDTH is '0', only DATA[7:0] are used and when CTRL.MEM_WIDTH is '1', only DATA[15:0] are used<br><br>A read from an empty RX FIFO sets INTR_RX.UNDERFLOW to '1'. |

### 26.12.29 SCB_EZ_DATA

**Description:** Memory buffer
**Address:** 0x40600400
**Offset:** 0x400
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** When the IP is disabled (CTRL.ENABLED is '0'), a read from these registers return 0xffff:ffff. It is under MMIO register control whether accesses to this register should introduce bus wait states or be discarded when the externally clocked logic is accessing the memory structure. These registers should only be used in EZ and CMD_RESP modes (and not in FIFO mode).
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | EZ_DATA [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | EZ_DATA | RW | RW | Undefined | Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. |

### 26.12.30 SCB_INTR_CAUSE

**Description:** Active clocked interrupt signal
**Address:** 0x40600E00
**Offset:** 0xE00
**Retention:** Retained
**IsDeepSleep:** No ( supported for SCB0_INTR_CAUSE )
**Comment:** Enables software to determine the source of the combined interrupt output signals 'interrupt_ic', 'interrupt_ec' and 'interrupt'.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:6] | | SPI_EC [5:5] | I2C_EC [4:4] | RX [3:3] | TX [2:2] | S [1:1] | M [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | M | R | W | 0 | Master interrupt active ('interrupt_master'): INTR_M_MASKED != 0. |
| 1 | S | R | W | 0 | Slave interrupt active ('interrupt_slave'): INTR_S_MASKED != 0. |
| 2 | TX | R | W | 0 | Transmitter interrupt active ('interrupt_tx'): INTR_TX_MASKED != 0. |
| 3 | RX | R | W | 0 | Receiver interrupt active ('interrupt_rx'): INTR_RX_MASKED != 0. |
| 4 | I2C_EC | R | W | 0 | Externally clock I2C interrupt active ('interrupt_i2c_ec'): INTR_I2C_EC_MASKED != 0. |
| 5 | SPI_EC | R | W | 0 | Externally clocked SPI interrupt active ('interrupt_spi_ec'): INTR_SPI_EC_MASKED != 0. |

### 26.12.31 SCB_INTR_I2C_EC

**Description:** Externally clocked I2C interrupt request
**Address:** 0x40600E80
**Offset:** 0xE80
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** The fields in this register are set by HW and are cleared by software by writing a '1'. These interrupt causes are generated by externally clocked logic. HW clears the interrupt causes to '0', when the IP is disabled.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:4] | | | | EZ_READ_STOP [3:3] | EZ_WRITE_STOP [2:2] | EZ_STOP [1:1] | WAKE_UP [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | WAKE_UP | RW1C | A | 0 | Wake up request. Active on incoming slave request (with address match).<br><br>Only used when CTRL.EC_AM_MODE is '1'. |
| 1 | EZ_STOP | RW1C | A | 0 | STOP detection. Activated on the end of a every transfer (I2C STOP).<br><br>Only available for a slave request with an address match, in EZ and CMD_RESP modes, when CTRL.EC_OP_MODE is '1'. |
| 2 | EZ_WRITE_STOP | RW1C | A | 0 | STOP detection after a write transfer occurred. Activated on the end of a write transfer (I2C STOP). This event is an indication that a buffer memory location has been written to. For EZ mode: a transfer that only writes the base address does NOT activate this event.<br><br>Only available for a slave request with an address match, in EZ and CMD_RESP modes, when CTRL.EC_OP_MODE is '1'. |
| 3 | EZ_READ_STOP | RW1C | A | 0 | STOP detection after a read transfer occurred. Activated on the end of a read transfer (I2C STOP). This event is an indication that a buffer memory location has been read from.<br><br>Only available for a slave request with an address match, in EZ and CMD_RESP modes, when CTRL.EC_OP_MODE is '1'. |

### 26.12.32 SCB_INTR_I2C_EC_MASK

**Description:** Externally clocked I2C interrupt mask
**Address:** 0x40600E88
**Offset:** 0xE88
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:4] | | | | EZ_READ_STOP [3:3] | EZ_WRITE_STOP [2:2] | EZ_STOP [1:1] | WAKE_UP [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | WAKE_UP | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |
| 1 | EZ_STOP | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |
| 2 | EZ_WRITE_STOP | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |
| 3 | EZ_READ_STOP | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |

### 26.12.33 SCB_INTR_I2C_EC_MASKED

**Description:** Externally clocked I2C interrupt masked
**Address:** 0x40600E8C
**Offset:** 0xE8C
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** When read, this register reflects a bitwise and between the interrupt request and mask registers. This register allows SW to read the status of all mask enabled interrupt causes with a single load operation, rather than two load operations: one for the interrupt causes and one for the masks. This simplifies Firmware development. The associated interrupt is active ('1'), when INTR_I2C_EC_MASKED != 0.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:4] | | | | EZ_READ_STOP [3:3] | EZ_WRITE_STOP [2:2] | EZ_STOP [1:1] | WAKE_UP [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | WAKE_UP | R | W | 0 | Logical and of corresponding request and mask bits. |
| 1 | EZ_STOP | R | W | 0 | Logical and of corresponding request and mask bits. |
| 2 | EZ_WRITE_STOP | R | W | 0 | Logical and of corresponding request and mask bits. |
| 3 | EZ_READ_STOP | R | W | 0 | Logical and of corresponding request and mask bits. |

### 26.12.34 SCB_INTR_SPI_EC

**Description:** Externally clocked SPI interrupt request
**Address:** 0x40600EC0
**Offset:** 0xEC0
**Retention:** Retained
**IsDeepSleep:** No ( supported for SCB0_INTR_SPI_EC )
**Comment:** The fields in this register are set by HW and are cleared by software by writing a '1'. These interrupt causes are generated by externally clocked logic. HW clears the interrupt causes to '0', when the IP is disabled.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:4] | | | | EZ_READ_STOP [3:3] | EZ_WRITE_STOP [2:2] | EZ_STOP [1:1] | WAKE_UP [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | WAKE_UP | RW1C | A | 0 | Wake up request. Active on incoming slave request when externally clocked selection is '1'.<br><br>Only used when CTRL.EC_AM_MODE is '1'. |
| 1 | EZ_STOP | RW1C | A | 0 | STOP detection. Activated on the end of a every transfer (SPI deselection).<br><br>Only available in EZ and CMD_RESP mode and when CTRL.EC_OP_MODE is '1'. |
| 2 | EZ_WRITE_STOP | RW1C | A | 0 | STOP detection after a write transfer occurred. Activated on the end of a write transfer (SPI deselection). This event is an indication that a buffer memory location has been written to. For EZ mode: a transfer that only writes the base address does NOT activate this event.<br><br>Only used in EZ and CMD_RESP modes and when CTRL.EC_OP_MODE is '1'. |
| 3 | EZ_READ_STOP | RW1C | A | 0 | STOP detection after a read transfer occurred. Activated on the end of a read transfer (SPI deselection). This event is an indication that a buffer memory location has been read from.<br><br>Only used in EZ and CMD_RESP modes and when CTRL.EC_OP_MODE is '1'. |

### 26.12.35 SCB_INTR_SPI_EC_MASK

**Description:** Externally clocked SPI interrupt mask
**Address:** 0x40600EC8
**Offset:** 0xEC8
**Retention:** Retained
**IsDeepSleep:** No ( supported for SCB0_INTR_SPI_EC_MASK )
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:4] | | | | EZ_READ_STOP [3:3] | EZ_WRITE_STOP [2:2] | EZ_STOP [1:1] | WAKE_UP [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | WAKE_UP | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |
| 1 | EZ_STOP | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |
| 2 | EZ_WRITE_STOP | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |
| 3 | EZ_READ_STOP | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |

### 26.12.36 SCB_INTR_SPI_EC_MASKED

**Description:** Externally clocked SPI interrupt masked
**Address:** 0x40600ECC
**Offset:** 0xECC
**Retention:** Retained
**IsDeepSleep:** No ( supported for SCB0_INTR_SPI_EC_MASKED )
**Comment:** When read, this register reflects a bitwise and between the interrupt request and mask registers. This register allows SW to read the status of all mask enabled interrupt causes with a single load operation, rather than two load operations: one for the interrupt causes and one for the masks. This simplifies Firmware development. The associated interrupt is active ('1'), when INTR_SPI_EC_MASKED != 0.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:4] | | | | EZ_READ_STOP [3:3] | EZ_WRITE_STOP [2:2] | EZ_STOP [1:1] | WAKE_UP [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | WAKE_UP | R | W | 0 | Logical and of corresponding request and mask bits. |
| 1 | EZ_STOP | R | W | 0 | Logical and of corresponding request and mask bits. |
| 2 | EZ_WRITE_STOP | R | W | 0 | Logical and of corresponding request and mask bits. |
| 3 | EZ_READ_STOP | R | W | 0 | Logical and of corresponding request and mask bits. |

### 26.12.37 SCB_INTR_M

**Description:** Master interrupt request
**Address:** 0x40600F00
**Offset:** 0xF00
**Retention:** Not Retained
**IsDeepSleep:** No ( supported for SCB0_INTR_M )
**Comment:** The register fields are not retained In DeepSleep power mode: HW clears the interrupt causes to '0', when coming out of DeepSleep power mode. In addition, HW clears the interrupt causes to '0', when the IP is disabled. As a result, the interrupt causes are only available in Active/Sleep power modes; they are generated by internally clocked logic (this logic operates on a clock that is only available in Active/Sleep power modes).

The interrupt causes should only be used for internally clocked operation; i.e. EC_OP is '0'.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:5] | | | I2C_STOP [4:4] | None [3:3] | I2C_ACK [2:2] | I2C_NACK [1:1] | I2C_ARB_LOST [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:10] | | | | | | SPI_DONE [9:9] | I2C_BUS_ERROR [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | I2C_ARB_LOST | RW1C | RW1S | 0 | I2C master lost arbitration: the value driven by the master on the SDA line is not the same as the value observed on the SDA line. |
| 1 | I2C_NACK | RW1C | RW1S | 0 | I2C master negative acknowledgement. Set to '1', when the master receives a NACK (typically after the master transmitted the slave address or TX data). |
| 2 | I2C_ACK | RW1C | RW1S | 0 | I2C master acknowledgement. Set to '1', when the master receives a ACK (typically after the master transmitted the slave address or TX data). |
| 4 | I2C_STOP | RW1C | RW1S | 0 | I2C master STOP. Set to '1', when the master has transmitted a STOP. |
| 8 | I2C_BUS_ERROR | RW1C | RW1S | 0 | I2C master bus error (unexpected detection of START or STOP condition). |
| 9 | SPI_DONE | RW1C | RW1S | 0 | SPI master transfer done event: all data frames in the transmit FIFO are sent, the transmit FIFO is empty (both TX FIFO and transmit shifter register are empty), and SPI select output pin is deselected. |

### 26.12.38 SCB_INTR_M_SET

**Description:** Master interrupt set request
**Address:** 0x40600F04
**Offset:** 0xF04
**Retention:** Not Retained
**IsDeepSleep:** No ( supported for SCB0_INTR_M_SET )
**Comment:** When read, this register reflects the interrupt request register.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:5] | | | I2C_STOP [4:4] | None [3:3] | I2C_ACK [2:2] | I2C_NACK [1:1] | I2C_ARB_LOST [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:10] | | | | | | SPI_DONE [9:9] | I2C_BUS_ERROR [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | I2C_ARB_LOST | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt request register. |
| 1 | I2C_NACK | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt request register. |
| 2 | I2C_ACK | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt request register. |
| 4 | I2C_STOP | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt request register. |
| 8 | I2C_BUS_ERROR | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt request register. |
| 9 | SPI_DONE | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt request register. |

### 26.12.39 SCB_INTR_M_MASK

**Description:** Master interrupt mask
**Address:** 0x40600F08
**Offset:** 0xF08
**Retention:** Retained
**IsDeepSleep:** No ( supported for SCB0_INTR_M_MASK )
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:5] | | | I2C_STOP [4:4] | None [3:3] | I2C_ACK [2:2] | I2C_NACK [1:1] | I2C_ARB_LOST [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:10] | | | | | | SPI_DONE [9:9] | I2C_BUS_ERROR [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | I2C_ARB_LOST | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |
| 1 | I2C_NACK | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |
| 2 | I2C_ACK | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |
| 4 | I2C_STOP | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |
| 8 | I2C_BUS_ERROR | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |
| 9 | SPI_DONE | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |

### 26.12.40 SCB_INTR_M_MASKED

**Description:** Master interrupt masked request
**Address:** 0x40600F0C
**Offset:** 0xF0C
**Retention:** Not Retained
**IsDeepSleep:** No ( supported for SCB0_INTR_M_MASKED )
**Comment:** When read, this register reflects a bitwise and between the interrupt request and mask registers. This register allows SW to read the status of all mask enabled interrupt causes with a single load operation, rather than two load operations: one for the interrupt causes and one for the masks. This simplifies Firmware development. The associated interrupt is active ('1'), when INTR_M_MASKED != 0.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:5] | | | I2C_STOP [4:4] | None [3:3] | I2C_ACK [2:2] | I2C_NACK [1:1] | I2C_ARB_LOST [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:10] | | | | | | SPI_DONE [9:9] | I2C_BUS_ERROR [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | I2C_ARB_LOST | R | W | 0 | Logical and of corresponding request and mask bits. |
| 1 | I2C_NACK | R | W | 0 | Logical and of corresponding request and mask bits. |
| 2 | I2C_ACK | R | W | 0 | Logical and of corresponding request and mask bits. |
| 4 | I2C_STOP | R | W | 0 | Logical and of corresponding request and mask bits. |
| 8 | I2C_BUS_ERROR | R | W | 0 | Logical and of corresponding request and mask bits. |
| 9 | SPI_DONE | R | W | 0 | Logical and of corresponding request and mask bits. |

### 26.12.41 SCB_INTR_S

**Description:** Slave interrupt request
**Address:** 0x40600F40
**Offset:** 0xF40
**Retention:** Not Retained
**IsDeepSleep:** No ( supported for SCB0_INTR_S )
**Comment:** The register fields are not retained In DeepSleep power mode: HW clears the interrupt causes to '0', when coming out of DeepSleep power mode. In addition, HW clears the interrupt causes to '0', when the IP is disabled. As a result, the interrupt causes are only available in Active/Sleep power modes; they are generated by internally clocked logic (this logic operates on a clock that is only available in Active/Sleep power modes).

The interrupt causes should only be used for internally clocked operation; i.e. EC_OP is '0'.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | I2C_GENERAL [7:7] | I2C_ADDR_MATCH [6:6] | I2C_START [5:5] | I2C_STOP [4:4] | I2C_WRITE_STOP [3:3] | I2C_ACK [2:2] | I2C_NACK [1:1] | I2C_ARB_LOST [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:12] | | | | SPI_BUS_ERROR [11:11] | SPI_EZ_STOP [10:10] | SPI_EZ_WRITE_STOP [9:9] | I2C_BUS_ERROR [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | I2C_ARB_LOST | RW1C | RW1S | 0 | I2C slave lost arbitration: the value driven on the SDA line is not the same as the value observed on the SDA line (while the SCL line is '1'). This should not occur, it represents erroneous I2C bus behavior. In case of lost arbitration, the I2C slave state machine aborts the ongoing transfer. The Firmware may decide to clear the TX and RX FIFOs in case of this error. |
| 1 | I2C_NACK | RW1C | RW1S | 0 | I2C slave negative acknowledgement received. Set to '1', when the slave receives a NACK (typically after the slave transmitted TX data). |
| 2 | I2C_ACK | RW1C | RW1S | 0 | I2C slave acknowledgement received. Set to '1', when the slave receives a ACK (typically after the slave transmitted TX data). |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 3 | I2C_WRITE_STOP | RW1C | RW1S | 0 | I2C STOP event for I2C write transfer intended for this slave (address matching is performed). Set to '1', when STOP or REPEATED START event is detected. The REPEATED START event is included in this interrupt cause such that the I2C transfers separated by a REPEATED START can be distinguished and potentially treated separately by the Firmware. Note that the second I2C transfer (after a REPEATED START) may be to a different slave address.<br><br>In non EZ mode, the event is detected on any I2C write transfer intended for this slave. Note that a I2C write address intended for the slave (address is matching and a it is a write transfer) will result in a I2C_WRITE_STOP event independent of whether the I2C address is ACK'd or NACK'd.<br><br>In EZ mode, the event is detected only on I2C write transfers that have EZ data written to the memory structure (an I2C write transfer that only communicates an I2C address and EZ address, will not result in this event being detected). |
| 4 | I2C_STOP | RW1C | RW1S | 0 | I2C STOP event for I2C (read or write) transfer intended for this slave (address matching is performed). Set to '1', when STOP or REPEATED START event is detected. The REPEATED START event is included in this interrupt cause such that the I2C transfers separated by a REPEATED START can be distinguished and potentially treated separately by the Firmware. Note that the second I2C transfer (after a REPEATED START) may be to a different slave address.<br><br>The event is detected on any I2C transfer intended for this slave. Note that a I2C address intended for the slave (address is matching) will result in a I2C_STOP event independent of whether the I2C address is ACK'd or NACK'd. |
| 5 | I2C_START | RW1C | RW1S | 0 | I2C slave START received. Set to '1', when START or REPEATED START event is detected.<br><br>In the case of externally clocked address matching (CTRL.EC_AM_MODE is '1') AND clock stretching is performed (I2C_CTRL.S_NOT_READY_ADDR_NACK is '0'), this field is NOT set. The Firmware should use INTR_S_EC.WAKE_UP, INTR_S.I2C_ADDR_MATCH and INTR_S.I2C_GENERAL. |
| 6 | I2C_ADDR_MATCH | RW1C | RW1S | 0 | I2C slave matching address received. If CTRL.ADDR_ACCEPT, the received address (including the R/W bit) is available in the RX FIFO. In the case of externally clocked address matching (CTRL.EC_AM_MODE is '1') and internally clocked operation (CTRL.EC_OP_MODE is '0'), this field is set when the event is detected. |
| 7 | I2C_GENERAL | RW1C | RW1S | 0 | I2C slave general call address received. If CTRL.ADDR_ACCEPT, the received address 0x00 (including the R/W bit) is available in the RX FIFO. In the case of externally clocked address matching (CTRL.EC_AM_MODE is '1') and internally clocked operation (CTRL.EC_OP_MODE is '0'), this field is set when the event is detected. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 8 | I2C_BUS_ERROR | RW1C | RW1S | 0 | I2C slave bus error (unexpected detection of START or STOP condition). This should not occur, it represents erroneous I2C bus behavior. In case of a bus error, the I2C slave state machine abort the ongoing transfer. The Firmware may decide to clear the TX and RX FIFOs in case of this error. |
| 9 | SPI_EZ_WRITE_STOP | RW1C | RW1S | 0 | SPI slave deselected after a write EZ SPI transfer occurred. |
| 10 | SPI_EZ_STOP | RW1C | RW1S | 0 | SPI slave deselected after any EZ SPI transfer occurred. |
| 11 | SPI_BUS_ERROR | RW1C | RW1S | 0 | SPI slave deselected at an unexpected time in the SPI transfer. The Firmware may decide to clear the TX and RX FIFOs in case of this error. |

### 26.12.42 SCB_INTR_S_SET

**Description:** Slave interrupt set request
**Address:** 0x40600F44
**Offset:** 0xF44
**Retention:** Not Retained
**IsDeepSleep:** No ( supported for SCB0_INTR_S_SET )
**Comment:** When read, this register reflects the interrupt request register.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | I2C_GENERAL [7:7] | I2C_ADDR_MATCH [6:6] | I2C_START [5:5] | I2C_STOP [4:4] | I2C_WRITE_STOP [3:3] | I2C_ACK [2:2] | I2C_NACK [1:1] | I2C_ARB_LOST [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:12] | | | | SPI_BUS_ERROR [11:11] | SPI_EZ_STOP [10:10] | SPI_EZ_WRITE_STOP [9:9] | I2C_BUS_ERROR [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | I2C_ARB_LOST | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt request register. |
| 1 | I2C_NACK | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt request register. |
| 2 | I2C_ACK | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt request register. |
| 3 | I2C_WRITE_STOP | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt request register. |
| 4 | I2C_STOP | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt request register. |
| 5 | I2C_START | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt request register. |
| 6 | I2C_ADDR_MATCH | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt request register. |
| 7 | I2C_GENERAL | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt request register. |
| 8 | I2C_BUS_ERROR | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt request register. |
| 9 | SPI_EZ_WRITE_STOP | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt request register. |
| 10 | SPI_EZ_STOP | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt request register. |
| 11 | SPI_BUS_ERROR | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt request register. |

### 26.12.43 SCB_INTR_S_MASK

**Description:** Slave interrupt mask
**Address:** 0x40600F48
**Offset:** 0xF48
**Retention:** Retained
**IsDeepSleep:** No ( supported for SCB0_INTR_S_MASK )
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | I2C_GENERAL [7:7] | I2C_ADDR_MATCH [6:6] | I2C_START [5:5] | I2C_STOP [4:4] | I2C_WRITE_STOP [3:3] | I2C_ACK [2:2] | I2C_NACK [1:1] | I2C_ARB_LOST [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:12] | | | | SPI_BUS_ERROR [11:11] | SPI_EZ_STOP [10:10] | SPI_EZ_WRITE_STOP [9:9] | I2C_BUS_ERROR [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | I2C_ARB_LOST | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |
| 1 | I2C_NACK | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |
| 2 | I2C_ACK | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |
| 3 | I2C_WRITE_STOP | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |
| 4 | I2C_STOP | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |
| 5 | I2C_START | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |
| 6 | I2C_ADDR_MATCH | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |
| 7 | I2C_GENERAL | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |
| 8 | I2C_BUS_ERROR | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |
| 9 | SPI_EZ_WRITE_STOP | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |
| 10 | SPI_EZ_STOP | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |
| 11 | SPI_BUS_ERROR | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |

### 26.12.44 SCB_INTR_S_MASKED

**Description:** Slave interrupt masked request
**Address:** 0x40600F4C
**Offset:** 0xF4C
**Retention:** Not Retained
**IsDeepSleep:** No ( supported for SCB0_INTR_S_MASKED )
**Comment:** When read, this register reflects a bitwise and between the interrupt request and mask registers. This register allows SW to read the status of all mask enabled interrupt causes with a single load operation, rather than two load operations: one for the interrupt causes and one for the masks. This simplifies Firmware development. The associated interrupt is active ('1'), when INTR_S_MASKED != 0.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | I2C_GENERAL [7:7] | I2C_ADDR_MATCH [6:6] | I2C_START [5:5] | I2C_STOP [4:4] | I2C_WRITE_STOP [3:3] | I2C_ACK [2:2] | I2C_NACK [1:1] | I2C_ARB_LOST [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:12] | | | | SPI_BUS_ERROR [11:11] | SPI_EZ_STOP [10:10] | SPI_EZ_WRITE_STOP [9:9] | I2C_BUS_ERROR [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | I2C_ARB_LOST | R | W | 0 | Logical and of corresponding request and mask bits. |
| 1 | I2C_NACK | R | W | 0 | Logical and of corresponding request and mask bits. |
| 2 | I2C_ACK | R | W | 0 | Logical and of corresponding request and mask bits. |
| 3 | I2C_WRITE_STOP | R | W | 0 | Logical and of corresponding request and mask bits. |
| 4 | I2C_STOP | R | W | 0 | Logical and of corresponding request and mask bits. |
| 5 | I2C_START | R | W | 0 | Logical and of corresponding request and mask bits. |
| 6 | I2C_ADDR_MATCH | R | W | 0 | Logical and of corresponding request and mask bits. |
| 7 | I2C_GENERAL | R | W | 0 | Logical and of corresponding request and mask bits. |
| 8 | I2C_BUS_ERROR | R | W | 0 | Logical and of corresponding request and mask bits. |
| 9 | SPI_EZ_WRITE_STOP | R | W | 0 | Logical and of corresponding request and mask bits. |
| 10 | SPI_EZ_STOP | R | W | 0 | Logical and of corresponding request and mask bits. |
| 11 | SPI_BUS_ERROR | R | W | 0 | Logical and of corresponding request and mask bits. |

### 26.12.45 SCB_INTR_TX

**Description:** Transmitter interrupt request
**Address:** 0x40600F80
**Offset:** 0xF80
**Retention:** Not Retained
**IsDeepSleep:** No ( supported for SCB0_INTR_TX )
**Comment:** The register fields are not retained In DeepSleep power mode: HW clears the interrupt causes to '0', when coming out of DeepSleep power mode. In addition, HW clears the interrupt causes to '0', when the IP is disabled. As a result, the interrupt causes are only available in Active/Sleep power modes; they are generated by internally clocked logic (this logic operates on a clock that is only available in Active/Sleep power modes).
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | BLOCKED [7:7] | UNDERFLOW [6:6] | OVERFLOW [5:5] | EMPTY [4:4] | None [3:2] | | NOT_FULL [1:1] | TRIGGER [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:11] | | | | | UART_ARB_LOST [10:10] | UART_DONE [9:9] | UART_NACK [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | TRIGGER | RW1C | RW1S | 0 | Less entries in the TX FIFO than the value specified by TX_FIFO_CTRL.TRIGGER_LEVEL.<br><br>Only used in FIFO mode. |
| 1 | NOT_FULL | RW1C | RW1S | 0 | TX FIFO is not full. Dependent on CTRL.MEM_WIDTH: (FF_DATA_NR = EZ_DATA_NR/2)<br>MEM_WIDTH is '0': # entries != FF_DATA_NR.<br>MEM_WIDTH is '1': # entries != FF_DATA_NR/2.<br>MEM_WIDTH is '2': # entries != FF_DATA_NR/4.<br><br>Only used in FIFO mode. |
| 4 | EMPTY | RW1C | RW1S | 0 | TX FIFO is empty; i.e. it has 0 entries.<br><br>Only used in FIFO mode. |
| 5 | OVERFLOW | RW1C | RW1S | 0 | Attempt to write to a full TX FIFO.<br><br>Only used in FIFO mode. |
| 6 | UNDERFLOW | RW1C | RW1S | 0 | Attempt to read from an empty TX FIFO. This happens when SCB is ready to transfer data and EMPTY is '1'.<br><br>Only used in FIFO mode.<br>(Note: This bit may be set unintentionally, even if the FIFO is not empty.<br>Workaround: Ignore the bit when the clock frequency of the AHB bus is greater than 3x the internal frequency of SCB and the FIFO is not empty) |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 7 | BLOCKED | RW1C | RW1S | 0 | SW cannot get access to the EZ memory (EZ data access), due to an externally clocked EZ access. This may happen when STATUS.EC_BUSY is '1'. |
| 8 | UART_NACK | RW1C | RW1S | 0 | UART transmitter received a negative acknowledgement in SmartCard mode. Set to '1', when event is detected. Write with '1' to clear bit. |
| 9 | UART_DONE | RW1C | RW1S | 0 | UART transmitter done event. This happens when the IP is done transferring all data in the TX FIFO, and the last stop field is transmitted (both TX FIFO and transmit shifter register are empty). Set to '1', when event is detected. Write with '1' to clear bit. |
| 10 | UART_ARB_LOST | RW1C | RW1S | 0 | UART lost arbitration: the value driven on the TX line is not the same as the value observed on the RX line. This condition event is useful when transmitter and receiver share a TX/RX line. This is the case in LIN or SmartCard modes. Set to '1', when event is detected. Write with '1' to clear bit. |

### 26.12.46 SCB_INTR_TX_SET

**Description:** Transmitter interrupt set request
**Address:** 0x40600F84
**Offset:** 0xF84
**Retention:** Not Retained
**IsDeepSleep:** No ( supported for SCB0_INTR_TX_SET )
**Comment:** When read, this register reflects the interrupt request register.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | BLOCKED [7:7] | UNDERFLOW [6:6] | OVERFLOW [5:5] | EMPTY [4:4] | None [3:2] | | NOT_FULL [1:1] | TRIGGER [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:11] | | | | | UART_ARB_LOST [10:10] | UART_DONE [9:9] | UART_NACK [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | TRIGGER | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt request register. |
| 1 | NOT_FULL | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt request register. |
| 4 | EMPTY | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt request register. |
| 5 | OVERFLOW | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt request register. |
| 6 | UNDERFLOW | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt request register. |
| 7 | BLOCKED | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt request register. |
| 8 | UART_NACK | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt request register. |
| 9 | UART_DONE | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt request register. |
| 10 | UART_ARB_LOST | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt request register. |

### 26.12.47 SCB_INTR_TX_MASK

**Description:** Transmitter interrupt mask
**Address:** 0x40600F88
**Offset:** 0xF88
**Retention:** Retained
**IsDeepSleep:** No ( supported for SCB0_INTR_TX_MASK )
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | BLOCKED [7:7] | UNDERFLOW [6:6] | OVERFLOW [5:5] | EMPTY [4:4] | None [3:2] | | NOT_FULL [1:1] | TRIGGER [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:11] | | | | | UART_ARB_LOST [10:10] | UART_DONE [9:9] | UART_NACK [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | TRIGGER | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |
| 1 | NOT_FULL | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |
| 4 | EMPTY | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |
| 5 | OVERFLOW | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |
| 6 | UNDERFLOW | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |
| 7 | BLOCKED | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |
| 8 | UART_NACK | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |
| 9 | UART_DONE | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |
| 10 | UART_ARB_LOST | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |

### 26.12.48 SCB_INTR_TX_MASKED

**Description:** Transmitter interrupt masked request
**Address:** 0x40600F8C
**Offset:** 0xF8C
**Retention:** Not Retained
**IsDeepSleep:** No ( supported for SCB0_INTR_TX_MASKED )
**Comment:** When read, this register reflects a bitwise and between the interrupt request and mask registers. This register allows SW to read the status of all mask enabled interrupt causes with a single load operation, rather than two load operations: one for the interrupt causes and one for the masks. This simplifies Firmware development. The associated interrupt is active ('1'), when INTR_TX_MASKED != 0.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | BLOCKED [7:7] | UNDERFLOW [6:6] | OVERFLOW [5:5] | EMPTY [4:4] | None [3:2] | | NOT_FULL [1:1] | TRIGGER [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:11] | | | | | UART_ARB_LOST [10:10] | UART_DONE [9:9] | UART_NACK [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | TRIGGER | R | W | 0 | Logical and of corresponding request and mask bits. |
| 1 | NOT_FULL | R | W | 0 | Logical and of corresponding request and mask bits. |
| 4 | EMPTY | R | W | 0 | Logical and of corresponding request and mask bits. |
| 5 | OVERFLOW | R | W | 0 | Logical and of corresponding request and mask bits. |
| 6 | UNDERFLOW | R | W | 0 | Logical and of corresponding request and mask bits. |
| 7 | BLOCKED | R | W | 0 | Logical and of corresponding request and mask bits. |
| 8 | UART_NACK | R | W | 0 | Logical and of corresponding request and mask bits. |
| 9 | UART_DONE | R | W | 0 | Logical and of corresponding request and mask bits. |
| 10 | UART_ARB_LOST | R | W | 0 | Logical and of corresponding request and mask bits. |

### 26.12.49 SCB_INTR_RX

**Description:** Receiver interrupt request
**Address:** 0x40600FC0
**Offset:** 0xFC0
**Retention:** Not Retained
**IsDeepSleep:** No ( supported for SCB0_INTR_RX )
**Comment:** The register fields are not retained In DeepSleep power mode: HW clears the interrupt causes to '0', when coming out of DeepSleep power mode. In addition, HW clears the interrupt causes to '0', when the IP is disabled. As a result, the interrupt causes are only available in Active/Sleep power modes; they are generated by internally clocked logic (this logic operates on a clock that is only available in Active/Sleep power modes).
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | BLOCKED [7:7] | UNDERFLOW [6:6] | OVERFLOW [5:5] | None [4:4] | FULL [3:3] | NOT _EMPTY [2:2] | None [1:1] | TRIGGER [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:12] | | | | BREAK _DETECT [11:11] | BAUD _DETECT [10:10] | PARITY _ERROR [9:9] | FRAME _ERROR [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | TRIGGER | RW1C | RW1S | 0 | More entries in the RX FIFO than the value specified by RX_FIFO_CTRL.TRIGGER_LEVEL.<br><br>Only used in FIFO mode. |
| 2 | NOT_EMPTY | RW1C | RW1S | 0 | RX FIFO is not empty.<br><br>Only used in FIFO mode. |
| 3 | FULL | RW1C | RW1S | 0 | RX FIFO is full. Note that received data frames are lost when the RX FIFO is full. Dependent on CTRL.MEM_WIDTH: (FF_DATA_NR = EZ_DATA_NR/2)<br>MEM_WIDTH is '0': # entries == FF_DATA_NR.<br>MEM_WIDTH is '1': # entries == FF_DATA_NR/2.<br>MEM_WIDTH is '2': # entries == FF_DATA_NR/4.<br><br>Only used in FIFO mode. |
| 5 | OVERFLOW | RW1C | RW1S | 0 | Attempt to write to a full RX FIFO. Note: in I2C mode, the OVERFLOW is set when a data frame is received and the RX FIFO is full, independent of whether it is ACK'd or NACK'd.<br><br>Only used in FIFO mode. |
| 6 | UNDERFLOW | RW1C | RW1S | 0 | Attempt to read from an empty RX FIFO.<br><br>Only used in FIFO mode. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 7 | BLOCKED | RW1C | RW1S | 0 | SW cannot get access to the EZ memory (EZ_DATA accesses), due to an externally clocked EZ access. This may happen when STATUS.EC_BUSY is '1'. |
| 8 | FRAME_ERROR | RW1C | RW1S | 0 | Frame error in received data frame. Set to '1', when event is detected. Write with '1' to clear bit. This can be either a start or stop bit(s) error:<br>Start bit error: after the detection of the beginning of a start bit period (RX line changes from '1' to '0'), the middle of the start bit period is sampled erroneously (RX line is '1'). Note: a start bit error is detected BEFORE a data frame is received.<br>Stop bit error: the RX line is sampled as '0', but a '1' was expected. Note: a stop bit error may result in failure to receive successive data frame(s). Note: a stop bit error is detected AFTER a data frame is received.<br><br>A stop bit error is detected after a data frame is received, and the UART_RX_CTL.DROP_ON_FRAME_ERROR field specifies whether the received frame is dropped or send to the RX FIFO. If UART_RX_CTL.DROP_ON_FRAME_ERROR is '1', the received data frame is dropped. If UART_RX_CTL.DROP_ON_FRAME_ERROR is '0', the received data frame is send to the RX FIFO. Note that Firmware can only identify the erroneous data frame in the RX FIFO if it is fast enough to read the data frame before the hardware writes a next data frame into the RX FIFO; i.e. the RX FIFO does not have error flags to tag erroneous data frames. |
| 9 | PARITY_ERROR | RW1C | RW1S | 0 | Parity error in received data frame. Set to '1', when event is detected. Write with '1' to clear bit. If UART_RX_CTL.DROP_ON_PARITY_ERROR is '1', the received frame is dropped. If UART_RX_CTL.DROP_ON_PARITY_ERROR is '0', the received frame is send to the RX FIFO. In SmartCard submode, negatively acknowledged data frames generate a parity error. Note that Firmware can only identify the erroneous data frame in the RX FIFO if it is fast enough to read the data frame before the hardware writes a next data frame into the RX FIFO. |
| 10 | BAUD_DETECT | RW1C | RW1S | 0 | LIN baudrate detection is completed. The receiver software uses the UART_RX_STATUS.BR_COUNTER value to set the right IP clock (from the programmable clock IP) to guarantee successful receipt of the first LIN data frame (Protected Identifier Field) after the synchronization byte. Set to '1', when event is detected. Write with '1' to clear bit. |
| 11 | BREAK_DETECT | RW1C | RW1S | 0 | Break detection is successful: the line is '0' for UART_RX_CTRL.BREAK_WIDTH + 1 bit period. Can occur at any time to address unanticipated break fields; i.e. 'break-in-data' is supported. This feature is supported for the UART standard and LIN submodes. For the UART standard submodes, ongoing receipt of data frames is NOT affected; i.e. Firmware is expected to take the proper action. For the LIN submode, possible ongoing receipt of a data frame is stopped and the (partially) received data frame is dropped and baud rate detection is started. Set to '1', when event is detected. Write with '1' to clear bit. |

### 26.12.50 SCB_INTR_RX_SET

**Description:** Receiver interrupt set request
**Address:** 0x40600FC4
**Offset:** 0xFC4
**Retention:** Not Retained
**IsDeepSleep:** No ( supported for SCB0_INTR_RX_SET )
**Comment:** When read, this register reflects the interrupt request register.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | BLOCKED [7:7] | UNDERFLOW [6:6] | OVERFLOW [5:5] | None [4:4] | FULL [3:3] | NOT _EMPTY [2:2] | None [1:1] | TRIGGER [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:12] | | | | BREAK _DETECT [11:11] | BAUD _DETECT [10:10] | PARITY _ERROR [9:9] | FRAME _ERROR [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | TRIGGER | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt request register. |
| 2 | NOT_EMPTY | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt status register. |
| 3 | FULL | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt status register. |
| 5 | OVERFLOW | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt status register. |
| 6 | UNDERFLOW | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt status register. |
| 7 | BLOCKED | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt status register. |
| 8 | FRAME_ERROR | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt status register. |
| 9 | PARITY_ERROR | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt status register. |
| 10 | BAUD_DETECT | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt status register. |
| 11 | BREAK_DETECT | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt status register. |

### 26.12.51 SCB_INTR_RX_MASK

**Description:** Receiver interrupt mask
**Address:** 0x40600FC8
**Offset:** 0xFC8
**Retention:** Retained
**IsDeepSleep:** No ( supported for SCB0_INTR_RX_MASK )
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | BLOCKED [7:7] | UNDERFLOW [6:6] | OVERFLOW [5:5] | None [4:4] | FULL [3:3] | NOT _EMPTY [2:2] | None [1:1] | TRIGGER [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:12] | | | | BREAK _DETECT [11:11] | BAUD _DETECT [10:10] | PARITY _ERROR [9:9] | FRAME _ERROR [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | TRIGGER | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |
| 2 | NOT_EMPTY | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |
| 3 | FULL | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |
| 5 | OVERFLOW | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |
| 6 | UNDERFLOW | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |
| 7 | BLOCKED | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |
| 8 | FRAME_ERROR | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |
| 9 | PARITY_ERROR | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |
| 10 | BAUD_DETECT | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |
| 11 | BREAK_DETECT | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |

### 26.12.52 SCB_INTR_RX_MASKED

**Description:** Receiver interrupt masked request
**Address:** 0x40600FCC
**Offset:** 0xFCC
**Retention:** Not Retained
**IsDeepSleep:** No ( supported for SCB0_INTR_RX_MASKED )
**Comment:** When read, this register reflects a bitwise and between the interrupt request and mask registers. This register allows SW to read the status of all mask enabled interrupt causes with a single load operation, rather than two load operations: one for the interrupt causes and one for the masks. This simplifies Firmware development. The associated interrupt is active ('1'), when INTR_RX_MASKED != 0.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | BLOCKED [7:7] | UNDERFLOW [6:6] | OVERFLOW [5:5] | None [4:4] | FULL [3:3] | NOT _EMPTY [2:2] | None [1:1] | TRIGGER [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:12] | | | | BREAK _DETECT [11:11] | BAUD _DETECT [10:10] | PARITY _ERROR [9:9] | FRAME _ERROR [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | TRIGGER | R | W | 0 | Logical and of corresponding request and mask bits. |
| 2 | NOT_EMPTY | R | W | 0 | Logical and of corresponding request and mask bits. |
| 3 | FULL | R | W | 0 | Logical and of corresponding request and mask bits. |
| 5 | OVERFLOW | R | W | 0 | Logical and of corresponding request and mask bits. |
| 6 | UNDERFLOW | R | W | 0 | Logical and of corresponding request and mask bits. |
| 7 | BLOCKED | R | W | 0 | Logical and of corresponding request and mask bits. |
| 8 | FRAME_ERROR | R | W | 0 | Logical and of corresponding request and mask bits. |
| 9 | PARITY_ERROR | R | W | 0 | Logical and of corresponding request and mask bits. |
| 10 | BAUD_DETECT | R | W | 0 | Logical and of corresponding request and mask bits. |
| 11 | BREAK_DETECT | R | W | 0 | Logical and of corresponding request and mask bits. |

# 27 SDHC

**Description** SD/eMMC Host Controller
**Base Address** 0x40460000
**Size** 0x10000
**Slave Num** MMIO4 - 1

## 27.1 WRAP

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SDHC0_WRAP_CTL | 0x40460000 | FULL | Top level wrapper control |

## 27.2 CORE

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SDHC0_CORE_SDMASA_R | 0x40461000 | FULL | SDMA System Address register |
| SDHC0_CORE_BLOCKSIZE_R | 0x40461004 | FULL | Block Size register |
| SDHC0_CORE_BLOCKCOUNT_R | 0x40461006 | FULL | 16-bit Block Count register |
| SDHC0_CORE_ARGUMENT_R | 0x40461008 | FULL | Argument register |
| SDHC0_CORE_XFER_MODE_R | 0x4046100C | FULL | Transfer Mode register |
| SDHC0_CORE_CMD_R | 0x4046100E | FULL | Command register |
| SDHC0_CORE_RESP01_R | 0x40461010 | FULL | Response Register 0/1 |
| SDHC0_CORE_RESP23_R | 0x40461014 | FULL | Response Register 2/3 |
| SDHC0_CORE_RESP45_R | 0x40461018 | FULL | Response Register 4/5 |
| SDHC0_CORE_RESP67_R | 0x4046101C | FULL | Response Register 6/7 |
| SDHC0_CORE_BUF_DATA_R | 0x40461020 | FULL | Buffer Data Port Register |
| SDHC0_CORE_PSTATE_REG | 0x40461024 | FULL | Present State Register |
| SDHC0_CORE_HOST_CTRL1_R | 0x40461028 | FULL | Host Control 1 Register |
| SDHC0_CORE_PWR_CTRL_R | 0x40461029 | FULL | Power Control Register |
| SDHC0_CORE_BGAP_CTRL_R | 0x4046102A | FULL | Block Gap Control Register |
| SDHC0_CORE_WUP_CTRL_R | 0x4046102B | FULL | Wakeup Control Register |
| SDHC0_CORE_CLK_CTRL_R | 0x4046102C | FULL | Clock Control Register |
| SDHC0_CORE_TOUT_CTRL_R | 0x4046102E | FULL | Timeout Control Register |
| SDHC0_CORE_SW_RST_R | 0x4046102F | FULL | Software Reset Register |
| SDHC0_CORE_NORMAL_INT_STAT_R | 0x40461030 | FULL | Normal Interrupt Status Register |
| SDHC0_CORE_ERROR_INT_STAT_R | 0x40461032 | FULL | Error Interrupt Status Register |
| SDHC0_CORE_NORMAL_INT_STAT_EN_R | 0x40461034 | FULL | Normal Interrupt Status Enable Register |
| SDHC0_CORE_ERROR_INT_STAT_EN_R | 0x40461036 | FULL | Error Interrupt Status Enable Register |
| SDHC0_CORE_NORMAL_INT_SIGNAL_EN_R | 0x40461038 | FULL | Normal Interrupt Signal Enable Register |
| SDHC0_CORE_ERROR_INT_SIGNAL_EN_R | 0x4046103A | FULL | Error Interrupt Signal Enable Register |
| SDHC0_CORE_AUTO_CMD_STAT_R | 0x4046103C | FULL | Auto CMD Status Register |
| SDHC0_CORE_HOST_CTRL2_R | 0x4046103E | FULL | Host Control 2 Register |
| SDHC0_CORE_CAPABILITIES1_R | 0x40461040 | FULL | Capabilities 1 Register - 0 to 31 |
| SDHC0_CORE_CAPABILITIES2_R | 0x40461044 | FULL | Capabilities Register - 32 to 63 |
| SDHC0_CORE_CURR_CAPABILITIES1_R | 0x40461048 | FULL | Current Capabilities Register - 0 to 31 |
| SDHC0_CORE_CURR_CAPABILITIES2_R | 0x4046104C | FULL | Maximum Current Capabilities Register - 32 to 63 |
| SDHC0_CORE_FORCE_AUTO_CMD_STAT_R | 0x40461050 | FULL | Force Event Register for Auto CMD Error Status register |
| SDHC0_CORE_FORCE_ERROR_INT_STAT_R | 0x40461052 | FULL | Force Event Register for Error Interrupt Status |
| SDHC0_CORE_ADMA_ERR_STAT_R | 0x40461054 | FULL | ADMA Error Status Register |
| SDHC0_CORE_ADMA_SA_LOW_R | 0x40461058 | FULL | ADMA System Address Register - Low |
| SDHC0_CORE_ADMA_ID_LOW_R | 0x40461078 | FULL | ADMA3 Integrated Descriptor Address Register - Low |
| SDHC0_CORE_HOST_CNTRL_VERS_R | 0x404610FE | FULL | Host Controller Version |
| SDHC0_CORE_MSHC_VER_ID_R | 0x40461500 | FULL | MSHC version |
| SDHC0_CORE_MSHC_VER_TYPE_R | 0x40461504 | FULL | MSHC version type |
| SDHC0_CORE_MSHC_CTRL_R | 0x40461508 | FULL | MSHC Control register |
| SDHC0_CORE_MBIU_CTRL_R | 0x40461510 | FULL | MBIU Control register |
| SDHC0_CORE_EMMC_CTRL_R | 0x4046152C | FULL | eMMC Control register Note:CQE_ALGO_SEL CQE_PREFETCH_DISABLE are not available for this register |
| SDHC0_CORE_BOOT_CTRL_R | 0x4046152E | FULL | eMMC Boot Control register |
| SDHC0_CORE_GP_IN_R | 0x40461530 | FULL | General Purpose Input register |
| SDHC0_CORE_GP_OUT_R | 0x40461534 | FULL | General Purpose Output register |

## 27.3 Register Details

### 27.3.1 WRAP

#### 27.3.1.1 SDHC_WRAP_CTL

**Description:** Top level wrapper control
**Address:** 0x40460000
**Offset:** 0x0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | ENABLE [31:31] | None [30:24] | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 31 | ENABLE | RW | R | 0 | IP Enable:<br>0: IP disabled, RAM in DeepSleep, SDHC_CORE regs are inaccessible (any attempts to access will result in AHB Error responses), IP is NOT held in reset but the clocks are gated<br>1: IP enabled, normal operation |

### 27.3.2 CORE

#### 27.3.2.1 SDHC_CORE_SDMASA_R

**Description:** SDMA System Address register
**Address:** 0x40461000
**Offset:** 0x0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register is used to configure a 32-bit Block Count or an SDMA System Address based on the Host Version 4 Enable bit in the Host Control 2 register. This register is applicable for both SD and eMMC modes.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | BLOCKCNT_SDMASA [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | BLOCKCNT_SDMASA [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | BLOCKCNT_SDMASA [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | BLOCKCNT_SDMASA [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | BLOCKCNT_SDMASA | RW | RW | 0 | 32-bit Block Count (SDMA System Address)<br>- SDMA System Address (Host Version 4 Enable = 0): This<br>register contains the system memory address for an SDMA transfer in the 32-bit addressing mode. When the<br>Host Controller stops an SDMA transfer, this register points to the system address of the next contiguous data<br>position. It can be accessed only if no transaction is executing. Reading this register during data transfers may<br>return an invalid value.<br>- 32-bit Block Count (Host Version 4 Enable = 1): From the<br>Host Controller Version 4.10 specification, this register is<br>redefined as 32-bit Block Count. The Host Controller decrements the block count of this register for every block<br>transfer and the data transfer stops when the count reaches zero. This register must be accessed when no transaction is executing. Reading this register during data<br>transfers may return invalid value.<br>Following are the values for BLOCKCNT_SDMASA:<br>- 0xFFFF_FFFF - 4G - 1 Block<br>- .....<br>- 0x0000_0002 - 2 Blocks<br>- 0x0000_0001 - 1 Block<br>- 0x0000_0000 - Stop Count<br>Note:<br>- When Host Version 4 Enable = 0, SDMA uses this register as system address and hence Auto CMD23 cannot be used with SDMA since this register is assigned for Auto CMD23 as 32-bit Block Count register.<br>-When Host Version 4 Enable = 1, SDMA uses ADMA system address register and this register is reassigned to 32-bit Block Count. This register must be programmed with a non-zero value for data transfer if the 32-bit Block count register is used instead of the 16-bit Block count register. SDMA may use Auto CMD23 if 32-bit Block Count register is used. |

### 27.3.2.2 SDHC_CORE_BLOCKSIZE_R

**Description:** Block Size register
**Address:** 0x40461004
**Offset:** 0x4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register is used to configure an SDMA buffer boundary and the number of bytes in a data block. This register is applicable for both SD and eMMC modes.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | XFER_BLOCK_SIZE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:15] | SDMA_BUF_BDARY [14:12] | | | XFER_BLOCK_SIZE [11:8] | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:11 | XFER_BLOCK_SIZE | RW | R | 0 | Transfer Block Size<br>These bits specify the block size of data transfers. In case of<br>memory, it is set to 512 bytes. It can be accessed only if no<br>transaction is executing. Read operations during transfers<br>may return an invalid value, and write operations are ignored. Following are the values for<br>XFER_BLOCK_SIZE:<br>- 0x1: 1 byte<br>- 0x2: 2 bytes<br>- 0x3: 3 bytes<br>- .....<br>- 0x1FF: 511 byte<br>- 0x200: 512 bytes<br>- .....<br>- 0x800: 2048 bytes<br>Note: This register must be programmed with a non-zero<br>value for data transfer. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 12:14 | SDMA_BUF_BDARY | RW | R | 0 | SDMA Buffer Boundary<br>These bits specify the size of contiguous buffer in system<br>memory. The SDMA transfer waits at every boundary specified by these fields and the Host Controller generates<br>the DMA interrupt to request the Host Driver to update the<br>SDMA System Address register.<br>Values:<br>- 0x0 (BYTES_4K): 4K bytes SDMA Buffer Boundary<br>- 0x1 (BYTES_8K): 8K bytes SDMA Buffer Boundary<br>- 0x2 (BYTES_16K): 16K bytes SDMA Buffer Boundary<br>- 0x3 (BYTES_32K): 32K bytes SDMA Buffer Boundary<br>- 0x4 (BYTES_64K): 64K bytes SDMA Buffer Boundary<br>- 0x5 (BYTES_128K): 128K bytes SDMA Buffer Boundary<br>- 0x6 (BYTES_256K): 256K bytes SDMA Buffer Boundary<br>- 0x7 (BYTES_512K): 512K bytes SDMA Buffer Boundary |

### 27.3.2.3 SDHC_CORE_BLOCKCOUNT_R

**Description:** 16-bit Block Count register
**Address:** 0x40461006
**Offset:** 0x6
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register is used to configure the number of data blocks. This register is applicable for both SD and eMMC modes.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | BLOCK_CNT [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | BLOCK_CNT [15:8] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | BLOCK_CNT | RW | RW | 0 | 16-bit Block Count<br>- If the Host Version 4 Enable bit is set 0 or the 16-bit Block<br>Count register is set to non-zero, the 16-bit Block Count<br>register is selected.<br>- If the Host Version 4 Enable bit is set 1 and the 16-bit Block Count register is set to zero, the 32-bit Block Count<br>register is selected.<br>Following are the values for BLOCK_CNT:<br>- 0x0: Stop Count<br>- 0x1: 1 Block<br>- 0x2: 2 Blocks<br>- ... - ...<br>- 0xFFFF: 65535 Blocks<br>Note: For Host Version 4 Enable = 0, this register must be<br>set to 0000h before programming the 32-bit block count<br>register when Auto CMD23 is enabled for non-DMA and<br>ADMA modes. |

### 27.3.2.4 SDHC_CORE_ARGUMENT_R

**Description:** Argument register
**Address:** 0x40461008
**Offset:** 0x8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register is used to configure the SD/eMMC command argument.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | ARGUMENT [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | ARGUMENT [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | ARGUMENT [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | ARGUMENT [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | ARGUMENT | RW | R | 0 | Command Argument<br>These bits specify the SD/eMMC command argument that is<br>specified in bits 39-8 of the Command format. |

### 27.3.2.5 SDHC_CORE_XFER_MODE_R

**Description:** Transfer Mode register
**Address:** 0x4046100C
**Offset:** 0xC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register is used to control the operation of data transfers for an SD/eMMC mode. The Host driver sets this register before issuing a command that transfers data.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | RESP_ERR_CHK_ENABLE [7:7] | RESP_TYPE [6:6] | MULTI_BLK_SEL [5:5] | DATA_XFER_DIR [4:4] | AUTO_CMD_ENABLE [3:2] | | BLOCK_COUNT_ENABLE [1:1] | DMA_ENABLE [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:9] | | | | | | | RESP_INT_DISABLE [8:8] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | DMA_ENABLE | RW | RW | 0 | DMA Enable<br>This bit enables the DMA functionality. If this bit is set to 1, a<br>DMA operation begins when the Host Driver writes to the<br>Command register. You can select one of the DMA modes by<br>using DMA Select in the Host Control 1 register.<br>Values:<br>- 0x1 (ENABLED): DMA Data transfer<br>- 0x0 (DISABLED): No data transfer or Non-DMA data transfer |
| 1 | BLOCK_COUNT_ENABLE | RW | RW | 0 | Block Count Enable<br>This bit is used to enable the Block Count register, which is<br>relevant for multiple block transfers. If this bit is set to 0, the<br>Block Count register is disabled, which is useful in executing<br>an infinite transfer. The Host Driver must set this bit to 0<br>when ADMA is used. When 16-bit Block Count register is used, the Host Driver can set this bit to 0 in ADMA2 mode to enable larger data transfer than the maximum of 65535 block counts supported by the 16-bit Block Count register. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 2:3 | AUTO_CMD_ENABLE | RW | RW | 0 | Auto Command Enable<br>This field determines use of Auto Command functions.<br>Note: In SDIO, this field must be set as 00b (Auto Command<br>Disabled).<br>Values:<br>- 0x0 (AUTO_CMD_DISABLED): Auto Command Disabled<br>- 0x1 (AUTO_CMD12_ENABLED): Auto CMD12 Enable<br>- 0x2 (AUTO_CMD23_ENABLED): Auto CMD23 Enable<br>- 0x3 (AUTO_CMD_AUTO_SEL): Auto CMD Auto Select |
| 4 | DATA_XFER_DIR | RW | RW | 0 | Data Transfer Direction Select<br>This bit defines the direction of DAT line data transfers. This<br>bit is set to 1 by the Host Driver to transfer data from the<br>SD/eMMC card to the Host Controller and it is set to 0 for all<br>other commands.<br>Values:<br>- 0x1 (READ): Read (Card to Host)<br>- 0x0 (WRITE): Write (Host to Card) |
| 5 | MULTI_BLK_SEL | RW | RW | 0 | Multi/Single Block Select<br>This bit is set when issuing multiple-block transfer commands using the DAT line. If this bit is set to 0, it is not<br>necessary to set the Block Count register. |
| 6 | RESP_TYPE | RW | RW | 0 | Response Type R1/R5<br>This bit selects either R1 or R5 as a response type when the<br>Response Error Check is selected.<br>Error statuses checked in R1:<br>- OUT_OF_RANGE<br>- ADDRESS_ERROR<br>- BLOCK_LEN_ERROR<br>- WP_VIOLATION<br>- CARD_IS_LOCKED<br>- COM_CRC_ERROR<br>- CARD_ECC_FAILED<br>- CC_ERROR<br>- ERROR<br>Response Flags checked in R5:<br>- COM_CRC_ERROR<br>- ERROR<br>- FUNCTION_NUMBER<br>- OUT_OF_RANGE<br>Values:<br>- 0x0 (RESP_R1): R1 (Memory)<br>- 0x1 (RESP_R5): R5 (SDIO) |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 7 | RESP_ERR_CHK _ENABLE | RW | RW | 0 | Response Error Check Enable<br>The Host Controller supports response check function to<br>avoid overhead of response error check by Host driver.<br>Response types of only R1 and R5 can be checked by the<br>Controller. If the Host Controller checks the response error,<br>set this bit to 1 and set Response Interrupt Disable to 1. If an<br>error is detected, the Response Error interrupt is generated<br>in the Error Interrupt Status register.<br>Note:<br>- Response error check must not be enabled for any response type other than R1 and R5.<br>Values:<br>- 0x0 (DISABLED): Response Error Check is disabled<br>- 0x1 (ENABLED): Response Error Check is enabled |
| 8 | RESP_INT_DISABLE | RW | RW | 0 | Response Interrupt Disable<br>The Host Controller supports response check function to<br>avoid overhead of response error check by the Host driver.<br>Response types of only R1 and R5 can be checked by the<br>Controller.<br>If Host Driver checks the response error, set this bit to 0 and<br>wait for Command Complete Interrupt and then check the<br>response register.<br>If the Host Controller checks the response error, set this bit<br>to 1 and set the Response Error Check Enable bit to 1. The<br>Command Complete Interrupt is disabled by this bit<br>regardless of the Command Complete Signal Enable.<br>Values:<br>- 0x0 (ENABLED): Response Interrupt is enabled<br>- 0x1 (DISABLED): Response Interrupt is disabled |

### 27.3.2.6 SDHC_CORE_CMD_R

**Description:** Command register
**Address:** 0x4046100E
**Offset:** 0xE
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register is used to provide the information related to a command and a response packet. This register is applicable for an SD/eMMC mode.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | CMD_TYPE [7:6] | | DATA _PRESENT _SEL [5:5] | CMD_IDX _CHK _ENABLE [4:4] | CMD_CRC _CHK _ENABLE [3:3] | SUB_CMD _FLAG [2:2] | RESP_TYPE_SELECT [1:0] | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:14] | | CMD_INDEX [13:8] | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:1 | RESP_TYPE_SELECT | RW | R | 0 | Response Type Select<br>This bit indicates the type of response expected from the<br>card.<br>Values:<br>- 0x0 (NO_RESP): No Response<br>- 0x1 (RESP_LEN_136): Response Length 136<br>- 0x2 (RESP_LEN_48): Response Length 48<br>- 0x3 (RESP_LEN_48B): Response Length 48; Check Busy after response |
| 2 | SUB_CMD_FLAG | RW | R | 0 | Sub Command Flag<br>This bit distinguishes between a main command and a sub<br>command.<br>Values:<br>- 0x0 (MAIN): Main Command<br>- 0x1 (SUB): Sub Command |
| 3 | CMD_CRC_CHK _ENABLE | RW | R | 0 | Command CRC Check Enable<br>This bit enables the Host Controller to check the CRC field in<br>the response. If an error is detected, it is reported as a Command CRC error.<br>Note:<br>- CRC Check enable must be set to 0 for the command with no response, R3 response, and R4 response.<br>Values:<br>- 0x0 (DISABLED): Disable<br>- 0x1 (ENABLED): Enable |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 4 | CMD_IDX_CHK_ENABLE | RW | R | 0 | Command Index Check Enable<br>This bit enables the Host Controller to check the index field in<br>the response to verify if it has the same value as the command index. If the value is not the same, it is reported as<br>a Command Index error.<br>Note:<br>- Index Check enable must be set to 0 for the command<br>with no response, R2 response, R3 response and R4 response.<br>Values:<br>- 0x0 (DISABLED): Disable<br>- 0x1 (ENABLED): Enable |
| 5 | DATA_PRESENT_SEL | RW | R | 0 | Data Present Select<br>This bit is set to 1 to indicate that data is present and that the<br>data is transferred using the DAT line. This bit is set to 0 in<br>the following instances:<br>- Command using the CMD line<br>- Command with no data transfer but using busy signal on<br>the DAT[0] line<br>- Resume Command<br>Values:<br>- 0x0 (NO_DATA): No Data Present<br>- 0x1 (DATA): Data Present |
| 6:7 | CMD_TYPE | RW | R | 0 | Command Type<br>These bits indicate the command type.<br>Note: While issuing Abort CMD using CMD12/CMD52 or<br>reset CMD using CMD0/CMD52, CMD_TYPE field shall be<br>set to 0x3.<br>Values:<br>- 0x3 (ABORT_CMD): Abort<br>- 0x2 (RESUME_CMD): Resume<br>- 0x1 (SUSPEND_CMD): Suspend<br>- 0x0 (NORMAL_CMD): Normal |
| 8:13 | CMD_INDEX | RW | R | 0 | Command Index<br>These bits are set to the command number that is specified<br>in bits 45-40 of the Command Format. |

### 27.3.2.7 SDHC_CORE_RESP01_R

**Description:** Response Register 0/1
**Address:** 0x40461010
**Offset:** 0x10
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register stores 39-08 bits of the Response Field for an SD/eMMC mode. In UHS-II mode, this register stores the response of the TRANS_ABORT CCMD. The response for an SD/eMMC command can be a maximum of 128 bits. These 128 bits are segregated into four 32-bit
registers: RESP01_R, RESP23_R, RESP45_R and RESP67_R.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | RESP01 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | RESP01 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | RESP01 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | RESP01 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | RESP01 | R | RW | 0 | Command Response<br>These bits reflect 39-8 bits of SD/eMMC Response Field.<br>Note: For Auto CMD, the 32-bit response (bits 39-8 of the<br>Response Field) is updated in the RESP67_R register. |

### 27.3.2.8 SDHC_CORE_RESP23_R

**Description:** Response Register 2/3
**Address:** 0x40461014
**Offset:** 0x14
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register stores 71-40 bits of the Response Field for an SD/eMMC mode. This register is used to store the response from the cards. The response can be a maximum of 128 bits.
These 128 bits are segregated into four 32-bit registers: RESP01_R, RESP23_R, RESP45_R and
RESP67_R. In UHS-II mode, this register is reserved
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | RESP23 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | RESP23 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | RESP23 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | RESP23 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | RESP23 | R | RW | 0 | Command Response<br>These bits reflect 71-40 bits of the SD/eMMC Response |

### 27.3.2.9 SDHC_CORE_RESP45_R

**Description:** Response Register 4/5
**Address:** 0x40461018
**Offset:** 0x18
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register stores 103-72 bits of the Response Field for an SD/eMMC mode. In UHS-II mode, this register is used to store the lower 4-byte CMD12 response. The response for SD/eMMC
command can be a maximum of 128 bits. These 128 bits are segregated into four 32-bit registers:
RESP01_R, RESP23_R, RESP45_R and RESP67_R.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | RESP45 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | RESP45 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | RESP45 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | RESP45 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | RESP45 | R | RW | 0 | Command Response<br>These bits reflect 103-72 bits of the Response Field. |

### 27.3.2.10 SDHC_CORE_RESP67_R

**Description:** Response Register 6/7
**Address:** 0x4046101C
**Offset:** 0x1C
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register stores 135-104 bits of the Response Field for an SD/eMMC mode. In UHSII mode, this register stores the upper 4-byte CMD12 response. The SD/eMMC response can be a
maximum of 128 bits. These 128 bits are segregated into four 32-bit registers: RESP01_R, RESP23_R,
RESP45_R and RESP67_R.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | RESP67 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | RESP67 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | RESP67 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | RESP67 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | RESP67 | R | RW | 0 | Command Response<br>These bits reflect bits 135-104 of SD/EMMC Response Field.<br>Note: For Auto CMD, this register also reflects the 32-bit<br>response (bits 39-8 of the Response Field). |

### 27.3.2.11 SDHC_CORE_BUF_DATA_R

**Description:** Buffer Data Port Register
**Address:** 0x40461020
**Offset:** 0x20
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register is used to access the packet buffer. This register is applicable for an SD/eMMC/UHS-II mode.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | BUF_DATA [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | BUF_DATA [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | BUF_DATA [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | BUF_DATA [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | BUF_DATA | RW | RW | 0 | Buffer Data<br>These bits enable access to the Host Controller packet buffer. |

### 27.3.2.12 SDHC_CORE_PSTATE_REG

**Description:** Present State Register
**Address:** 0x40461024
**Offset:** 0x24
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register indicates the present status of the Host Controller. This register is applicable for an SD/eMMC/UHS-II mode.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DAT_7_4 [7:4] | | | | None [3:3] | DAT_LINE_ ACTIVE [2:2] | CMD _INHIBIT _DAT [1:1] | CMD _INHIBIT [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:12] | | | | BUF_RD _ENABLE [11:11] | BUF_WR _ENABLE [10:10] | RD_XFER _ACTIVE [9:9] | WR_XFER _ACTIVE [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | DAT_3_0 [23:20] | | | | WR _PROTECT _SW_LVL [19:19] | CARD _DETECT _PIN_LEV EL [18:18] | CARD _STABLE [17:17] | CARD _INSE RTED [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:29] | | | SUB_CMD _STAT [28:28] | CMD_ISSU _ERR [27:27] | None [26:26] | HOST _REG_VOL [25:25] | CMD_LINE _LVL [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | CMD_INHIBIT | R | RW | 0 | Command Inhibit (CMD)<br>This bit indicates the following :<br>- SD/eMMC mode: If this bit is set to 0, it indicates that the<br>CMD line is not in use and the Host controller can issue<br>an SD/eMMC command using the CMD line. This bit is set when the command register is written. This bit is cleared when the command response is received. This bit<br>is not cleared by the response of auto CMD12/23 but cleared by the response of read/write command.<br>Values:<br>- 0x0 (READY): Host Controller is ready to issue a command<br>- 0x1 (NOT_READY): Host Controller is not ready to issue<br>a command |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 1 | CMD_INHIBIT_DAT | R | RW | 0 | Command Inhibit (DAT)<br>This bit is applicable for SD/eMMC mode and is generated if<br>either DAT line active or Read transfer active is set to 1. If<br>this bit is set to 0, it indicates that the Host Controller can<br>issue subsequent SD/eMMC commands.<br>Values:<br>- 0x0 (READY): Can issue command which used DAT line<br>- 0x1 (NOT_READY): Cannot issue command which used<br>DAT line |
| 2 | DAT_LINE_ACTIVE | R | RW | 0 | DAT Line Active (SD/eMMC Mode only)<br>This bit indicates whether one of the DAT lines on the SD/eMMC bus is in use.<br>In the case of read transactions, this bit indicates whether a<br>read transfer is executing on the SD/eMMC bus.<br>In the case of write transactions, this bit indicates whether a<br>write transfer is executing on the SD/eMMC bus.<br>For a command with busy, this status indicates whether the<br>command executing busy is executing on an SD or eMMC<br>bus.<br>Values:<br>- 0x0 (INACTIVE): DAT Line Inactive<br>- 0x1 (ACTIVE): DAT Line Active |
| 4:7 | DAT_7_4 | R | RW | 0 | DAT[7:4] Line Signal Level<br>This bit is used to check the DAT line level to recover from<br>errors and for debugging. These bits reflect the value of the<br>sd_dat_in (upper nibble) signal. |
| 8 | WR_XFER_ACTIVE | R | RW | 0 | Write Transfer Active<br>This status indicates whether a write transfer is active for<br>SD/eMMC mode.<br>Values:<br>- 0x0 (INACTIVE): No valid data<br>- 0x1 (ACTIVE): Transferring data |
| 9 | RD_XFER_ACTIVE | R | RW | 0 | Read Transfer Active<br>This bit indicates whether a read transfer is active for SD/eMMC mode.<br>Values:<br>- 0x0 (INACTIVE): No valid data<br>- 0x1 (ACTIVE): Transferring data |
| 10 | BUF_WR_ENABLE | R | RW | 0 | Buffer Write Enable<br>This bit is used for non-DMA transfers. This bit is set if space<br>is available for writing data.<br>Values:<br>- 0x0 (DISABLED): Write disable<br>- 0x1 (ENABLED): Write enable |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 11 | BUF_RD_ENABLE | R | RW | 0 | Buffer Read Enable<br>This bit is used for non-DMA transfers. This bit is set if valid<br>data exists in the Host buffer.<br>Values:<br>- 0x0 (DISABLED): Read disable<br>- 0x1 (ENABLED): Read enable |
| 16 | CARD_INSERTED | R | RW | 0 | Card Inserted<br>This bit indicates whether a card has been inserted. The<br>Host Controller debounces this signal so that Host Driver<br>need not wait for it to stabilize.<br>Values:<br>- 0x0 (FALSE): Reset, Debouncing, or No card<br>- 0x1 (TRUE): Card Inserted |
| 17 | CARD_STABLE | R | RW | 0 | Card Stable<br>This bit indicates the stability of the Card Detect Pin Level. A<br>card is not detected if this bit is set to 1 and the value of the<br>CARD_INSERTED bit is 0.<br>Values:<br>- 0x0 (FALSE): Reset or Debouncing<br>- 0x1 (TRUE): No Card or Inserted |
| 18 | CARD_DETECT_PIN_LEVEL | R | RW | 0 | Card Detect Pin Level<br>This bit reflects the inverse synchronized value of the card_detect_n signal.<br>Values:<br>- 0x0 (FALSE): No card present<br>- 0x1 (TRUE): Card Present |
| 19 | WR_PROTECT_SW_LVL | R | RW | 0 | Write Protect Switch Pin Level<br>This bit is supported only for memory and combo cards. This<br>bit reflects the synchronized value of the card_write_prot<br>signal.<br>Values:<br>- 0x0 (FALSE): Write protected<br>- 0x1 (TRUE): Write enabled |
| 20:23 | DAT_3_0 | R | RW | 0 | DAT[3:0] Line Signal Level<br>This bit is used to check the DAT line level to recover from<br>errors and for debugging. These bits reflect the value of the<br>sd_dat_in (lower nibble) signal. |
| 24 | CMD_LINE_LVL | R | RW | 0 | Command-Line Signal Level<br>This bit is used to check the CMD line level to recover from<br>errors and for debugging. These bits reflect the value of the<br>sd_cmd_in signal. |
| 25 | HOST_REG_VOL | R | RW | 0 | Host Regulator Voltage Stable<br>This bit is used to check whether the host regulator voltage is<br>stable for switching the voltage of UHS-I mode. This bit reflects the synchronized value of the host_reg_vol_stable<br>signal.<br>Values:<br>- 0x0 (FALSE): Host Regulator Voltage is not stable<br>- 0x1 (TRUE): Host Regulator Voltage is stable |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 27 | CMD_ISSU_ERR | R | RW | 0 | Command Not Issued by Error<br>This bit is set if a command cannot be issued after setting<br>the command register due to an error except the Auto CMD12 error.<br>Values:<br>- 0x0 (FALSE): No error for issuing a command<br>- 0x1 (TRUE): Command cannot be issued |
| 28 | SUB_CMD_STAT | R | RW | 0 | Sub Command Status<br>This bit is used to distinguish between a main command and<br>a sub command status.<br>Values:<br>- 0x0 (FALSE): Main Command Status<br>- 0x1 (TRUE): Sub Command Status |

### 27.3.2.13 SDHC_CORE_HOST_CTRL1_R

**Description:** Host Control 1 Register
**Address:** 0x40461028
**Offset:** 0x28
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register is used to control the operation of the Host Controller. This register is applicable for an SD/eMMC/UHS-II mode.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | CARD _DETECT _SIG_SEL [7:7] | CARD _DETECT _TEST_LVL [6:6] | EXT_DAT _XFER [5:5] | DMA_SEL [4:3] | | HIGH _SPEED _EN [2:2] | DAT_XFER _WIDTH [1:1] | LED_CTRL [0:0] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | LED_CTRL | RW | R | 0 | LED Control<br>This bit is used to caution the user not to remove the card<br>while the SD card is being accessed. The value is reflected<br>on the led_ctrl ouput.<br>Values:<br>- 0x0 (OFF): LED off<br>- 0x1 (ON): LED on |
| 1 | DAT_XFER_WIDTH | RW | R | 0 | Data Transfer Width<br>For SD/eMMC mode,this bit selects the data transfer width of<br>the Host Controller. The Host Driver sets it to match the data<br>width of the SD/eMMC card.<br>Values:<br>- 0x1 (FOUR_BIT): 4-bit mode<br>- 0x0 (ONE_BIT): 1-bit mode |
| 2 | HIGH_SPEED_EN | RW | R | 0 | High Speed Enable (SD/eMMC Mode only)<br>Before setting this bit, the Host Driver checks the High Speed<br>Support in the Capabilities register.<br>Note: SDHC always outputs the sd_cmd_out and sd_dat_out lines at the rising edge of card clock irrespective of this bit.<br>Values:<br>- 0x1 (HIGH_SPEED): High Speed mode<br>- 0x0 (NORMAL_SPEED): Normal Speed mode |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 3:4 | DMA_SEL | RW | R | 0 | DMA Select<br>This field is used to select the DMA type.<br>When Host Version 4 Enable is 1 in Host Control 2 register:<br>- 0x0 - SDMA is selected<br>- 0x1 - Reserved<br>- 0x2 - ADMA2 is selected<br>- 0x3 - ADMA2 or ADMA3 is selected<br>When Host Version 4 Enable is 0 in Host Control 2 register:<br>- 0x0 - SDMA is selected<br>- 0x1 - Reserved<br>- 0x2 - 32-bit Address ADMA2 is selected<br>- 0x3 - Reserved<br>Values:<br>- 0x0 (SDMA): SDMA is selected<br>- 0x1 (RSVD_BIT): Reserved<br>- 0x2 (ADMA2): ADMA2 is selected<br>- 0x3 (ADMA2_3): ADMA2 or ADMA3 is selected |
| 5 | EXT_DAT_XFER | RW | R | 0 | Extended Data Transfer Width<br>This bit controls 8-bit bus width mode of embedded device.<br>Values:<br>- 0x1 (EIGHT_BIT): 8-bit Bus Width<br>- 0x0 (DEFAULT): Bus Width is selected by the Data Transfer Width |
| 6 | CARD_DETECT_TEST_LVL | RW | R | 0 | Card Detect Test Level<br>This bit is enabled while the Card Detect Signal Selection is<br>set to 1 and it indicates whether a card inserted or not.<br>Values:<br>- 0x1 (CARD_INSERTED): Card Inserted<br>- 0x0 (No_CARD): No Card |
| 7 | CARD_DETECT_SIG_SEL | RW | R | 0 | Card Detect Signal Selection<br>This bit selects a source for card detection. When the source<br>for the card detection is switched, the interrupt must be disabled during the switching period.<br>Values:<br>- 0x1 (CARD_DT_TEST_LEVEL): Card Detect Test Level<br>is selected (for test purpose)<br>- 0x0 (card_detect_n): card_detect_n signal is selected (for normal use) |

### 27.3.2.14 SDHC_CORE_PWR_CTRL_R

**Description:** Power Control Register
**Address:** 0x40461029
**Offset:** 0x29
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register is used to control the bus power for the Card. This register is applicable for an SD, eMMC, and UHS-II modes.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:4] | | | | SD_BUS_VOL_VDD1 [3:1] | | | SD_BUS_PWR_VDD1 [0:0] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | SD_BUS_PWR_VDD1 | RW | RW | 0 | SD Bus Power for VDD1<br>This bit enables VDD1 power of the card. This setting is<br>available on the card_if_pwr_en output so that it<br>can be used to control the VDD1 power supply of the card.<br>Before setting this bit, the SD Host Driver sets the SD Bus<br>Voltage Select bit. If the Host Controller detects a No Card<br>state, this bit is cleared.<br>In SD mode, if this bit is cleared, the Host Controller stops<br>the SD Clock by clearing the SD_CLK_IN bit in the CLK_CTRL_R register.<br>Values:<br>- 0x0 (OFF): Power off<br>- 0x1 (ON): Power on |
| 1:3 | SD_BUS_VOL_VDD1 | RW | R | 0 | These bits are NON-operational (they can be written and read but they have no effect). In a generic HCI host these would select the card supply voltage. But, for the applications targeted for this block it is assumed that the card supply voltage is always fixed at the board level. If for some reason there is a variable power supply then that can be managed through normal GPIO programming separately. |

### 27.3.2.15 SDHC_CORE_BGAP_CTRL_R

**Description:** Block Gap Control Register
**Address:** 0x4046102A
**Offset:** 0x2A
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register is used by the host driver to control any operation related to Block Gap. This register is applicable for an SD/eMMC/UHS-II mode.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:4] | | | | INT_AT_BGAP [3:3] | RD_WAIT_CTRL [2:2] | CONTINUE_REQ [1:1] | STOP_BG_REQ [0:0] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | STOP_BG_REQ | RW | R | 0 | Stop At Block Gap Request<br>This bit is used to stop executing read and write transactions<br>at the next block gap for non-DMA, SDMA, and ADMA transfers.<br>Values:<br>- 0x0 (XFER): Transfer<br>- 0x1 (STOP): Stop |
| 1 | CONTINUE_REQ | RW | RW | 0 | Continue Request<br>This bit is used to restart the transaction, which was stopped<br>using the Stop At Block Gap Request. The Host Controller<br>automatically clears this bit when the transaction restarts. If<br>stop at block gap request is set to 1, any write to this bit is<br>ignored.<br>Values:<br>- 0x0 (NO_AFFECT): No Affect<br>- 0x1 (RESTART): Restart |
| 2 | RD_WAIT_CTRL | RW | R | 0 | Reserved: set to 0 |
| 3 | INT_AT_BGAP | RW | R | 0 | Interrupt At Block Gap<br>This bit is valid only in the 4-bit mode of an SDIO card and is<br>used to select a sample point in the interrupt cycle. Setting to<br>1 enables interrupt detection at the block gap for a multiple<br>block transfer.<br>Values:<br>- 0x0 (DISABLE): Disabled<br>- 0x1 (ENABLE): Enabled |

### 27.3.2.16 SDHC_CORE_WUP_CTRL_R

**Description:** Wakeup Control Register
**Address:** 0x4046102B
**Offset:** 0x2B
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** The intention of this 'wakeup' register is to wake up an otherwise idle Host driver. It is NOT a wake up from DeepSleep. clk_peri must be running in order for the events below to be detected and reported. All other clocks to the block can be gated, though. Note that the Host Driver must maintain voltage on the SD Bus by setting the SD Bus Power to 1 in the Power Control Register if a wakeup event through the Card Interrupt is desired.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:3] | | | | | WUP _CARD_ REMOVAL [2:2] | WUP _CARD_ INSERT [1:1] | WUP _CARD_ INT [0:0] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | WUP_CARD_INT | RW | R | 0 | Wakeup Event Enable on SDIO Card Interrupt (through DAT[1]).<br>This bit enables wakeup event through an SDIO Card Interrupt<br>assertion in the Normal Interrupt Status register. This bit can<br>be set to 1 if FN_WUS (Wake Up Support) in CIS is set to 1.<br>Values:<br>- 0x0 (DISABLED): Disable<br>- 0x1 (ENABLED): Enable |
| 1 | WUP_CARD_INSERT | RW | R | 0 | Wakeup Event Enable on SD Card Insertion<br>This bit enables wakeup event through Card Insertion<br>assertion in the Normal Interrupt Status register.<br>FN_WUS<br>(Wake Up Support) in CIS does not affect this bit.<br>Values:<br>- 0x0 (DISABLED): Disable<br>- 0x1 (ENABLED): Enable |
| 2 | WUP_CARD_REMOVAL | RW | R | 0 | Wakeup Event Enable on SD Card Removal<br>This bit enables wakeup event through Card Removal<br>assertion in the Normal Interrupt Status register. For the<br>SDIO card, Wake Up Support (FN_WUS) in the Card Information Structure (CIS) register does not affect this bit.<br>Values:<br>- 0x0 (DISABLED): Disable<br>- 0x1 (ENABLED): Enable |

### 27.3.2.17 SDHC_CORE_CLK_CTRL_R

**Description:** Clock Control Register
**Address:** 0x4046102C
**Offset:** 0x2C
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register controls SDCLK (card clock) in an SD/eMMC mode and RCLK in the UHS-II mode. This register is applicable for an SD/eMMC/UHS-II mode.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | UPPER_FREQ_SEL [7:6] | | CLK_GEN _SELECT [5:5] | None [4:4] | PLL _ENABLE [3:3] | SD_CLK _EN [2:2] | INTERNAL _CLK _STABLE [1:1] | INTERNAL _CLK_EN [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | FREQ_SEL [15:8] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | INTERNAL_CLK_EN | RW | R | 0 | Internal Clock Enable<br>This bit is set to 0 when the Host Driver is not using the Host<br>Controller or the Host Controller awaits a wakeup interrupt.<br>The Host Controller must stop its internal clock to enter a<br>very low power state. Certain registers are not accessible when this bit is off. So, to be safe turn it on for any register access.<br>Values:<br>- 0x0 (FALSE): Stop<br>- 0x1 (TRUE): Oscillate |
| 1 | INTERNAL_CLK _STABLE | R | RW | 0 | Internal Clock Stable<br>This bit enables the Host Driver to check the clock stability<br>twice after the Internal Clock Enable bit is set and after the<br>PLL Enable bit is set. This bit reflects the synchronized value of the Internal Clock Stable signal after the Internal Clock<br>Enable bit is set to 1 and also reflects the synchronized<br>value of the Card Clock Stable signal after the PLL Enable bit is<br>set to 1.<br>Values:<br>- 0x0 (FALSE): Not Ready<br>- 0x1 (TRUE): Ready |
| 2 | SD_CLK_EN | RW | R | 0 | SD/eMMC Clock Enable<br>This bit stops the clk_card output when set to 0. The SDCLK Frequency Select bit can be changed when this bit is set to 0.<br>Values:<br>- 0x0 (FALSE): Disable providing clk_card<br>- 0x1 (TRUE): Enable providing clk_card |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 3 | PLL_ENABLE | RW | R | 0 | PLL Enable<br>This bit is used to activate the PLL (applicable when Host<br>Version 4 Enable = 1).<br>Values:<br>- 0x0 (FALSE): PLL is in low power mode<br>- 0x1 (TRUE): PLL is enabled |
| 5 | CLK_GEN_SELECT | RW | RW | 0 | Clock Generator Select<br>This bit is used to select the clock generator mode in SDCLK Frequency Select.<br>Values:<br>- 0x0 (FALSE): Divided Clock Mode<br>- 0x1 (TRUE): Programmable Clock Mode |
| 6:7 | UPPER_FREQ_SEL | RW | RW | 0 | These bits specify the upper 2 bits of 10-bit SDCLK Frequency Select control. |
| 8:15 | FREQ_SEL | RW | RW | 0 | SDCLK Frequency Select<br>These bits are used to select the frequency of the SDCLK<br>signal.<br>10-bit Divided Clock Mode:<br>- 0x3FF - 1/2046 Divided clock<br>- .....<br>- N - 1/2N Divided Clock<br>- .....<br>- 0x002 - 1/4 Divided Clock<br>- 0x001 - 1/2 Divided Clock<br>- 0x000 - Base clock (10MHz - 255 MHz) |

### 27.3.2.18 SDHC_CORE_TOUT_CTRL_R

**Description:** Timeout Control Register
**Address:** 0x4046102E
**Offset:** 0x2E
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register is used to set the Data Timeout Counter value for an SD/eMMC mode according to the timer clock defined by the Capabilities register, while initializig the Host Controller.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:4] | | | | TOUT_CNT [3:0] | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | TOUT_CNT | RW | R | 0 | Data Timeout Counter Value.<br>This value determines the interval by which DAT line timeouts are detected. The Timeout clock frequency is generated by dividing the base clock TMCLK value by this<br>value. When setting this register, prevent inadvertent timeout<br>events by clearing the Data Timeout Error Status Enable (in<br>the Error Interrupt Status Enable register). The values for<br>these bits are:<br>- 0xF - Reserved<br>- 0xE - TMCLK x 2^27<br>- .....<br>- 0x1 - TMCLK x 2^14<br>- 0x0 - TMCLK x 2^13<br>Note: During a boot operating in an eMMC mode, an application must configure the boot data timeout value (approximately 1 sec) in this bit. |

### 27.3.2.19 SDHC_CORE_SW_RST_R

**Description:** Software Reset Register
**Address:** 0x4046102F
**Offset:** 0x2F
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register is used to generate a reset pulse by writing 1 to each bit of this register. After completing the reset, the Host Controller clears each bit. As it takes some time to complete a
software reset, the Host Driver confirms that these bits are 0. This register is applicable for an SD/eMMC/UHS-II mode.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:3] | | | | | SW_RST _DAT [2:2] | SW_RST _CMD [1:1] | SW_RST _ALL [0:0] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | SW_RST_ALL | RW | RW | 0 | Software Reset For All<br>This reset affects the entire Host Controller except for the<br>card detection circuit. During its initialization, the Host Driver<br>sets this bit to 1 to reset the Host Controller. All registers are<br>reset except the capabilities register. If this bit is set to 1, the<br>Host Driver must issue reset command and reinitialize the<br>card.<br>Values:<br>- 0x0 (FALSE): Work<br>- 0x1 (TRUE): Reset |
| 1 | SW_RST_CMD | RW | RW | 0 | Software Reset For CMD line<br>This bit resets only a part of the command circuit to be able<br>to issue a command. This reset is effective only for a command<br>issuing circuit (including response error statuses related to<br>Command Inhibit (CMD) control) and does not affect the<br>data transfer circuit. Host Controller can continue data transfer even after this reset is executed while handling<br>subcommand-response errors.<br>The following registers and bits are cleared by this bit:<br>- Present State register - Command Inhibit (CMD) bit<br>- Normal Interrupt Status register - Command Complete bit<br>- Error Interrupt Status - Response error statuses related<br>to Command Inhibit (CMD) bit<br>Values:<br>- 0x0 (FALSE): Work<br>- 0x1 (TRUE): Reset |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 2 | SW_RST_DAT | RW | RW | 0 | Software Reset For DAT line<br>This bit is used in SD/eMMC mode and it resets only a part<br>of the data circuit and the DMA circuit is also reset.<br>The following registers and bits are cleared by this bit:<br>- Buffer Data Port register<br>- Buffer is cleared and initialized.<br>- Present state register<br>- Buffer Read Enable<br>- Buffer Write Enable<br>- Read Transfer Active<br>- Write Transfer Active<br>- DAT Line Active<br>- Command Inhibit (DAT)<br>- Block Gap Control register<br>- Continue Request<br>- Stop At Block Gap Request<br>- Normal Interrupt status register<br>- Buffer Read Ready<br>- Buffer Write Ready<br>- DMA Interrupt<br>- Block Gap Event<br>- Transfer Complete<br>Values:<br>- 0x0 (FALSE): Work<br>- 0x1 (TRUE): Reset |

### 27.3.2.20 SDHC_CORE_NORMAL_INT_STAT_R

**Description:** Normal Interrupt Status Register
**Address:** 0x40461030
**Offset:** 0x30
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register reflects the status of the Normal Interrupt. This register is applicable for an SD/eMMC/UHS-II mode.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | CARD_REMOVAL [7:7] | CARD_INSERTION [6:6] | BUF_RD_READY [5:5] | BUF_WR_READY [4:4] | DMA_INTERRUPT [3:3] | BGAP_EVENT [2:2] | XFER_COMPLETE [1:1] | CMD_COMPLETE [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | ERR_INTERRUPT [15:15] | CQE_EVENT [14:14] | FX_EVENT [13:13] | None [12:9] | | | | CARD_INTERRUPT [8:8] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | CMD_COMPLETE | RW1C | RW | 0 | Command Complete<br>In an SD/eMMC Mode, this bit is set when the end bit of a<br>response except for Auto CMD12 and Auto CMD23. This interrupt is not generated when the Response Interrupt<br>Disable in Transfer Mode Register is set to 1.<br>Values:<br>- 0x0 (FALSE): No command complete<br>- 0x1 (TRUE): Command Complete |
| 1 | XFER_COMPLETE | RW1C | RW | 0 | Transfer Complete<br>This bit is set when a read/write transfer and a command<br>with status busy is completed.<br>Values:<br>- 0x0 (FALSE): Not complete<br>- 0x1 (TRUE): Command execution is completed |
| 2 | BGAP_EVENT | RW1C | RW | 0 | Block Gap Event<br>This bit is set when both read/write transaction is stopped at<br>block gap due to a Stop at Block Gap Request.<br>Values:<br>- 0x0 (FALSE): No Block Gap Event<br>- 0x1 (TRUE): Transaction stopped at block gap |
| 3 | DMA_INTERRUPT | RW1C | RW | 0 | DMA Interrupt<br>This bit is set if the Host Controller detects the SDMA Buffer<br>Boundary during transfer. In case of ADMA, by setting the Int<br>field in the descriptor table, the Host controller generates this<br>interrupt. This interrupt is not generated after a Transfer<br>Complete.<br>Values:<br>- 0x0 (FALSE): No DMA Interrupt<br>- 0x1 (TRUE): DMA Interrupt is generated |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 4 | BUF_WR_READY | RW1C | RW | 0 | Buffer Write Ready<br>This bit is set if the Buffer Write Enable changes from 0 to 1.<br>Values:<br>- 0x0 (FALSE): Not ready to write buffer<br>- 0x1 (TRUE): Ready to write buffer |
| 5 | BUF_RD_READY | RW1C | RW | 0 | Buffer Read Ready<br>This bit is set if the Buffer Read Enable changes from 0 to 1.<br>Values:<br>- 0x0 (FALSE): Not ready to read buffer<br>- 0x1 (TRUE): Ready to read buffer |
| 6 | CARD_INSERTION | RW1C | RW | 0 | Card Insertion<br>This bit is set if the Card Inserted in the Present State register changes from 0 to 1.<br>Values:<br>- 0x0 (FALSE): Card state stable or Debouncing<br>- 0x1 (TRUE): Card Inserted |
| 7 | CARD_REMOVAL | RW1C | RW | 0 | Card Removal<br>This bit is set if the Card Inserted in the Present State register changes from 1 to 0.<br>Values:<br>- 0x0 (FALSE): Card state stable or Debouncing<br>- 0x1 (TRUE): Card Removed |
| 8 | CARD_INTERRUPT | R | RW | 0 | Card Interrupt<br>This bit reflects the synchronized value of:<br>- DAT[1] Interrupt Input for SD Mode<br>Values:<br>- 0x0 (FALSE): No Card Interrupt<br>- 0x1 (TRUE): Generate Card Interrupt |
| 13 | FX_EVENT | R | RW | 0 | FX Event<br>This status is set when R[14] of response register is set to 1<br>and Response Type R1/R5 is set to 0 in Transfer Mode<br>register. This interrupt is used with response check function.<br>Values:<br>- 0x0 (FALSE): No Event<br>- 0x1 (TRUE): FX Event is detected |
| 14 | CQE_EVENT | RW1C | RW | 0 | Command Queuing Event<br>This status is set if Command Queuing/Crypto related event<br>has occurred in eMMC/SD mode. Read CQHCI's CQIS/CRNQIS register for more details. In UHS-II Mode,<br>this bit is irrelevant.<br>Values:<br>- 0x0 (FALSE): No Event<br>- 0x1 (TRUE): Command Queuing Event is detected |
| 15 | ERR_INTERRUPT | R | RW | 0 | Error Interrupt<br>If any of the bits in the Error Interrupt Status register are set,<br>then this bit is set.<br>Values:<br>- 0x0 (FALSE): No Error<br>- 0x1 (TRUE): Error |

### 27.3.2.21 SDHC_CORE_ERROR_INT_STAT_R

**Description:** Error Interrupt Status Register
**Address:** 0x40461032
**Offset:** 0x32
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register enables an interrupt when the Error Interrupt Status Enable is enabled and at least one of the statuses is set to 1. Writing to 1 clears the bit and writing to 0 retains the bit unchanged. Signals defined in this register can be enabled by the Error Interrupt Status Enable register, but not by the Error Interrupt Signal Enable register. More than one status can be cleared with a single register write. This register is applicable for an SD/eMMC/UHS-II mode.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | CUR_LMT_ERR [7:7] | DATA_END_BIT_ERR [6:6] | DATA_CRC_ERR [5:5] | DATA_TOUT_ERR [4:4] | CMD_IDX_ERR [3:3] | CMD_END_BIT_ERR [2:2] | CMD_CRC_ERR [1:1] | CMD_TOUT_ERR [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:13] | | | BOOT_ACK_ERR [12:12] | RESP_ERR [11:11] | TUNING_ERR [10:10] | ADMA_ERR [9:9] | AUTO_CMD_ERR [8:8] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | CMD_TOUT_ERR | RW1C | RW | 0 | Command Timeout Error<br>In SD/eMMC Mode,this bit is set only if no response is returned within 64 SD clock cycles from the end bit of the command. If the Host Controller detects a CMD line conflict, along with Command CRC Error bit, this bit is set to 1, without waiting for 64 SD/eMMC card clock cycles.<br>Values:<br>- 0x0 (FALSE): No error<br>- 0x1 (TRUE): Time out |
| 1 | CMD_CRC_ERR | RW1C | RW | 0 | Command CRC Error<br>Command CRC Error is generated in SD/eMMC mode for following two cases.<br>- If a response is returned and the Command Timeout Error is set to 0 (indicating no timeout), this bit is set to 1 when detecting a CRC error in the command response.<br>- The Host Controller detects a CMD line conflict by monitoring the CMD line when a command is issued. If the Host Controller drives the CMD line to 1 level, but detects 0 level on the CMD line at the next SD clock edge, then the Host Controller aborts the command (stop driving CMD line) and set this bit to 1. The Command Timeout Error is also set to 1 to distinguish a CMD line conflict.<br>Values:<br>- 0x0 (FALSE): No error<br>- 0x1 (TRUE): CRC error generated |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 2 | CMD_END_BIT_ERR | RW1C | RW | 0 | Command End Bit Error<br>This bit is set when detecting that the end bit of a command<br>response is 0 in SD/eMMC mode.<br>Values:<br>- 0x0 (FALSE): No error<br>- 0x1 (TRUE): End Bit error generated |
| 3 | CMD_IDX_ERR | RW1C | RW | 0 | Command Index Error<br>This bit is set if a Command Index error occurs in the command respons in SD/eMMC mode.<br>Values:<br>- 0x0 (FALSE): No error<br>- 0x1 (TRUE): Error |
| 4 | DATA_TOUT_ERR | RW1C | RW | 0 | Data Timeout Error<br>This bit is set in SD/eMMC mode when detecting one of the<br>following timeout conditions:<br>- Busy timeout for R1b, R5b type<br>- Busy timeout after Write CRC status<br>- Write CRC Status timeout<br>- Read Data timeout<br>Values:<br>- 0x0 (FALSE): No error<br>- 0x1 (TRUE): Time out |
| 5 | DATA_CRC_ERR | RW1C | RW | 0 | Data CRC Error<br>This error occurs in SD/eMMC mode when detecting CRC<br>error when transferring read data which uses the DAT line,<br>when detecting the Write CRC status having a value of other<br>than 010 or when write CRC status timeout.<br>Values:<br>- 0x0 (FALSE): No error<br>- 0x1 (TRUE): Error |
| 6 | DATA_END_BIT_ERR | RW1C | RW | 0 | Data End Bit Error<br>This error occurs in SD/eMMC mode either when detecting 0<br>at the end bit position of read data that uses the DAT line or<br>at the end bit position of the CRC status.<br>Values:<br>- 0x0 (FALSE): No error<br>- 0x1 (TRUE): Error |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 7 | CUR_LMT_ERR | RW1C | RW | 0 | Current Limit Error<br>By setting the SD Bus Power bit in the Power Control register, the Host Controller is requested to supply power for<br>the SD Bus. If the Host Controller supports the Current Limit<br>function, it can be protected from an illegal card by stopping<br>power supply to the card in which case this bit indicates a<br>failure status. A reading of 1 for this bit means that the Host<br>Controller is not supplying power to the SD card due to some<br>failure. A reading of 0 for this bit means that the Host Controller is supplying power and no error has occurred. The<br>Host Controller may require some sampling time to detect<br>the current limit. DWC_mshc Host Controller does not support this function, this bit is always set to 0.<br>Values:<br>- 0x0 (FALSE): No error<br>- 0x1 (TRUE): Power Fail |
| 8 | AUTO_CMD_ERR | RW1C | RW | 0 | Auto CMD Error<br>This error status is used by Auto CMD12 and Auto CMD23 in<br>SD/eMMC mode. This bit is set when detecting that any of<br>the bits D00 to D05 in Auto CMD Error Status register has<br>changed from 0 to 1. D07 is effective in case of Auto CMD12.<br>Auto CMD Error Status register is valid while this bit is set to<br>1 and may be cleared by clearing of this bit.<br>Values:<br>- 0x0 (FALSE): No error<br>- 0x1 (TRUE): Error |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 9 | ADMA_ERR | RW1C | RW | 0 | ADMA Error<br>This bit is set when the Host Controller detects error during<br>ADMA-based data transfer. The error could be due to following reasons:<br>- Error response received from System bus (Master I/F)<br>- ADMA3,ADMA2 Descriptors invalid<br>- CQE Task or Transfer descriptors invalid<br>When the error occurs, the state of the ADMA is saved in the<br>ADMA Error Status register.<br>In eMMC CQE mode:<br>The Host Controller generates this Interrupt when it detects<br>an invalid descriptor data (Valid=0) at the ST_FDS state.<br>ADMA Error State in the ADMA Error Status indicates that<br>an error has occurred in ST_FDS state. The Host Driver may<br>find that Valid bit is not set at the error descriptor.<br>Values:<br>- 0x0 (FALSE): No error<br>- 0x1 (TRUE): Error |
| 10 | TUNING_ERR | RW1C | RW | 0 | Reserved |
| 11 | RESP_ERR | RW1C | RW | 0 | Response Error<br>Host Controller Version 4.00 supports response error check<br>function to avoid overhead of response error check by Host<br>Driver during DMA execution. If Response Error Check Enable is set to 1 in the Transfer Mode register, Host Controller Checks R1 or R5 response. If an error is detected<br>in a response, this bit is set to 1.This is applicable in SD/eMMC mode.<br>Values:<br>- 0x0 (FALSE): No error<br>- 0x1 (TRUE): Error |
| 12 | BOOT_ACK_ERR | RW1C | RW | 0 | Boot Acknowledgement Error<br>This bit is set when there is a timeout for boot acknowledgement or when detecting boot ack status having<br>a value other than 010. This is applicable only when boot<br>acknowledgement is expected in eMMC mode.<br>In SD mode, this bit is irrelevant.<br>Values:<br>- 0x0 (FALSE): No error<br>- 0x1 (TRUE): Error |

### 27.3.2.22 SDHC_CORE_NORMAL_INT_STAT_EN_R

**Description:** Normal Interrupt Status Enable Register
**Address:** 0x40461034
**Offset:** 0x34
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register enables the Interrupt Status for Normal Interrupt Status register (NORMAL_INT_STAT_R) when NORMAL_INT_STAT_R is set to 1. This register is applicable for an SD/eMMC/UHS-II mode.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | CARD_REMOVAL_STAT_EN [7:7] | CARD_INSERTION_STAT_EN [6:6] | BUF_RD_READY_STAT_EN [5:5] | BUF_WR_READY_STAT_EN [4:4] | DMA_INTERRUPT_STAT_EN [3:3] | BGAP_EVENT_STAT_EN [2:2] | XFER_COMPLETE_STAT_EN [1:1] | CMD_COMPLETE_STAT_EN [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:15] | CQE_EVENT_STAT_EN [14:14] | FX_EVENT_STAT_EN [13:13] | RE_TUNE_EVENT_STAT_EN [12:12] | INT_C_STAT_EN [11:11] | INT_B_STAT_EN [10:10] | INT_A_STAT_EN [9:9] | CARD_INTERRUPT_STAT_EN [8:8] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | CMD_COMPLETE_STAT_EN | RW | R | 0 | Command Complete Status Enable<br>Values:<br>- 0x0 (FALSE): Masked<br>- 0x1 (TRUE): Enabled |
| 1 | XFER_COMPLETE_STAT_EN | RW | R | 0 | Transfer Complete Status Enable<br>Values:<br>- 0x0 (FALSE): Masked<br>- 0x1 (TRUE): Enabled |
| 2 | BGAP_EVENT_STAT_EN | RW | R | 0 | Block Gap Event Status Enable<br>Values:<br>- 0x0 (FALSE): Masked<br>- 0x1 (TRUE): Enabled |
| 3 | DMA_INTERRUPT_STAT_EN | RW | R | 0 | DMA Interrupt Status Enable<br>Values:<br>- 0x0 (FALSE): Masked<br>- 0x1 (TRUE): Enabled |
| 4 | BUF_WR_READY_STAT_EN | RW | R | 0 | Buffer Write Ready Status Enable<br>Values:<br>- 0x0 (FALSE): Masked<br>- 0x1 (TRUE): Enabled |
| 5 | BUF_RD_READY_STAT_EN | RW | R | 0 | Buffer Read Ready Status Enable<br>Values:<br>- 0x0 (FALSE): Masked<br>- 0x1 (TRUE): Enabled |
| 6 | CARD_INSERTION_STAT_EN | RW | R | 0 | Card Insertion Status Enable<br>Values:<br>- 0x0 (FALSE): Masked<br>- 0x1 (TRUE): Enabled |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 7 | CARD_REMOVAL_STAT_EN | RW | R | 0 | Card Removal Status Enable<br>Values:<br>- 0x0 (FALSE): Masked<br>- 0x1 (TRUE): Enabled |
| 8 | CARD_INTERRUPT_STAT_EN | RW | R | 0 | Card Interrupt Status Enable<br>If this bit is set to 0, the Host Controller clears the interrupt<br>request to the System. The Card Interrupt detection is stopped when this bit is cleared and restarted when this bit is<br>set to 1. The Host Driver may clear the Card Interrupt Status<br>Enable before servicing the Card Interrupt and may set this<br>bit again after all interrupt requests from the card are cleared<br>to prevent inadvertent interrupts.<br>Values:<br>- 0x0 (FALSE): Masked<br>- 0x1 (TRUE): Enabled |
| 9 | INT_A_STAT_EN | RW | R | 0 | Reserved: set to 0 |
| 10 | INT_B_STAT_EN | RW | R | 0 | Reserved: set to 0 |
| 11 | INT_C_STAT_EN | RW | R | 0 | Reserved: set to 0 |
| 12 | RE_TUNE_EVENT_STAT_EN | RW | R | 0 | Reserved: set to 0 |
| 13 | FX_EVENT_STAT_EN | RW | R | 0 | FX Event Status Enable<br>This bit is added from Version 4.10.<br>Values:<br>- 0x0 (FALSE): Masked<br>- 0x1 (TRUE): Enabled |
| 14 | CQE_EVENT_STAT_EN | RW | R | 0 | CQE Event Status Enable<br>Values:<br>- 0x0 (FALSE): Masked<br>- 0x1 (TRUE): Enabled |

### 27.3.2.23 SDHC_CORE_ERROR_INT_STAT_EN_R

**Description:** Error Interrupt Status Enable Register
**Address:** 0x40461036
**Offset:** 0x36
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register sets the Interrupt Status for Error Interrupt Status register (ERROR_INT_STAT_R), when ERROR_INT_STAT_EN_R is set to 1. This register is applicable for an SD/eMMC/UHS-II mode.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | CUR_LMT_ERR_STAT_EN [7:7] | DATA_END_BIT_ERR_STAT_EN [6:6] | DATA_CRC_ERR_STAT_EN [5:5] | DATA_TOUT_ERR_STAT_EN [4:4] | CMD_IDX_ERR_STAT_EN [3:3] | CMD_END_BIT_ERR_STAT_EN [2:2] | CMD_CRC_ERR_STAT_EN [1:1] | CMD_TOUT_ERR_STAT_EN [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VENDOR_ERR_STAT_EN3 [15:15] | VENDOR_ERR_STAT_EN2 [14:14] | VENDOR_ERR_STAT_EN1 [13:13] | BOOT_ACK_ERR_STAT_EN [12:12] | RESP_ERR_STAT_EN [11:11] | TUNING_ERR_STAT_EN [10:10] | ADMA_ERR_STAT_EN [9:9] | AUTO_CMD_ERR_STAT_EN [8:8] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | CMD_TOUT_ERR_STAT_EN | RW | R | 0 | Command Timeout Error Status Enable (SD/eMMC Mode only).<br>Values:<br>- 0x0 (FALSE): Masked<br>- 0x1 (TRUE): Enabled |
| 1 | CMD_CRC_ERR_STAT_EN | RW | R | 0 | ommand CRC Error Status Enable (SD/eMMC Mode only)<br>Values:<br>- 0x0 (FALSE): Masked<br>- 0x1 (TRUE): Enabled |
| 2 | CMD_END_BIT_ERR_STAT_EN | RW | R | 0 | Command End Bit Error Status Enable (SD/eMMC Mode only)<br>Values:<br>- 0x0 (FALSE): Masked<br>- 0x1 (TRUE): Enabled |
| 3 | CMD_IDX_ERR_STAT_EN | RW | R | 0 | Command Index Error Status Enable (SD/eMMC Mode only)<br>Values:<br>- 0x0 (FALSE): Masked<br>- 0x1 (TRUE): Enabled |
| 4 | DATA_TOUT_ERR_STAT_EN | RW | R | 0 | Data Timeout Error Status Enable (SD/eMMC Mode only)<br>Values:<br>- 0x0 (FALSE): Masked<br>- 0x1 (TRUE): Enabled |
| 5 | DATA_CRC_ERR_STAT_EN | RW | R | 0 | Data CRC Error Status Enable (SD/eMMC Mode only)<br>Values:<br>- 0x0 (FALSE): Masked<br>- 0x1 (TRUE): Enabled |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 6 | DATA_END_BIT_ERR _STAT_EN | RW | R | 0 | Data End Bit Error Status Enable (SD/eMMC Mode only).<br>Values:<br>- 0x0 (FALSE): Masked<br>- 0x1 (TRUE): Enabled |
| 7 | CUR_LMT_ERR_STAT _EN | RW | R | 0 | Current Limit Error Status Enable<br>Values:<br>- 0x0 (FALSE): Masked<br>- 0x1 (TRUE): Enabled |
| 8 | AUTO_CMD_ERR_STAT _EN | RW | R | 0 | Auto CMD Error Status Enable (SD/eMMC Mode only).<br>Values:<br>- 0x0 (FALSE): Masked<br>- 0x1 (TRUE): Enabled |
| 9 | ADMA_ERR_STAT_EN | RW | R | 0 | ADMA Error Status Enable<br>Values:<br>- 0x0 (FALSE): Masked<br>- 0x1 (TRUE): Enabled |
| 10 | TUNING_ERR_STAT_EN | RW | R | 0 | Tuning Error Status Enable (UHS-I Mode only)<br>Values:<br>- 0x0 (FALSE): Masked<br>- 0x1 (TRUE): Enabled |
| 11 | RESP_ERR_STAT_EN | RW | R | 0 | Response Error Status Enable (SD Mode only)<br>Values:<br>- 0x0 (FALSE): Masked<br>- 0x1 (TRUE): Enabled |
| 12 | BOOT_ACK_ERR_STAT _EN | RW | R | 0 | Boot Acknowledgment Error (eMMC Mode only)<br>Setting this bit to 1 enables setting of Boot Acknowledgment<br>Error in Error Interrupt Status register (ERROR_INT_STAT_R).<br>Values:<br>- 0x0 (FALSE): Masked<br>- 0x1 (TRUE): Enabled |
| 13 | VENDOR_ERR_STAT _EN1 | RW | R | 0 | Reserved: set to 0 |
| 14 | VENDOR_ERR_STAT _EN2 | RW | R | 0 | Reserved: set to 0 |
| 15 | VENDOR_ERR_STAT _EN3 | RW | R | 0 | Reserved: set to 0 |

### 27.3.2.24 SDHC_CORE_NORMAL_INT_SIGNAL_EN_R

**Description:** Normal Interrupt Signal Enable Register
**Address:** 0x40461038
**Offset:** 0x38
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register is used to select the interrupt status that is indicated to the Host System as the interrupt. All these status bits share the same 1-bit interrupt line. Setting any of these bits to 1,
enables interrupt generation. This register is applicable for an SD/eMMC/UHS-II mode.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | CARD_REMOVAL_SIGNAL_EN [7:7] | CARD_INSERTION_SIGNAL_EN [6:6] | BUF_RD_READY_SIGNAL_EN [5:5] | BUF_WR_READY_SIGNAL_EN [4:4] | DMA_INTERRUPT_SIGNAL_EN [3:3] | BGAP_EVENT_SIGNAL_EN [2:2] | XFER_COMPLETE_SIGNAL_EN [1:1] | CMD_COMPLETE_SIGNAL_EN [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:15] | CQE_EVENT_SIGNAL_EN [14:14] | FX_EVENT_SIGNAL_EN [13:13] | RE_TUNE_EVENT_SIGNAL_EN [12:12] | INT_C_SIGNAL_EN [11:11] | INT_B_SIGNAL_EN [10:10] | INT_A_SIGNAL_EN [9:9] | CARD_INTERRUPT_SIGNAL_EN [8:8] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | CMD_COMPLETE_SIGNAL_EN | RW | R | 0 | Command Complete Signal Enable<br>Values:<br>- 0x0 (FALSE): Masked<br>- 0x1 (TRUE): Enabled |
| 1 | XFER_COMPLETE_SIGNAL_EN | RW | R | 0 | Transfer Complete Signal Enable<br>Values:<br>- 0x0 (FALSE): Masked<br>- 0x1 (TRUE): Enabled |
| 2 | BGAP_EVENT_SIGNAL_EN | RW | R | 0 | Block Gap Event Signal Enable<br>Values:<br>- 0x0 (FALSE): Masked<br>- 0x1 (TRUE): Enabled |
| 3 | DMA_INTERRUPT_SIGNAL_EN | RW | R | 0 | DMA Interrupt Signal Enable<br>Values:<br>- 0x0 (FALSE): Masked<br>- 0x1 (TRUE): Enabled |
| 4 | BUF_WR_READY_SIGNAL_EN | RW | R | 0 | Buffer Write Ready Signal Enable<br>Values:<br>- 0x0 (FALSE): Masked<br>- 0x1 (TRUE): Enabled |
| 5 | BUF_RD_READY_SIGNAL_EN | RW | R | 0 | Buffer Read Ready Signal Enable<br>Values:<br>- 0x0 (FALSE): Masked<br>- 0x1 (TRUE): Enabled |
| 6 | CARD_INSERTION_SIGNAL_EN | RW | R | 0 | Card Insertion Signal Enable<br>Values:<br>- 0x0 (FALSE): Masked<br>- 0x1 (TRUE): Enabled |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 7 | CARD_REMOVAL_SIGNAL_EN | RW | R | 0 | Card Removal Signal Enable<br>Values:<br>- 0x0 (FALSE): Masked<br>- 0x1 (TRUE): Enabled |
| 8 | CARD_INTERRUPT_SIGNAL_EN | RW | R | 0 | Card Interrupt Signal Enable<br>Values:<br>- 0x0 (FALSE): Masked<br>- 0x1 (TRUE): Enabled |
| 9 | INT_A_SIGNAL_EN | RW | R | 0 | Reserved: set to 0 |
| 10 | INT_B_SIGNAL_EN | RW | R | 0 | Reserved: set to 0 |
| 11 | INT_C_SIGNAL_EN | RW | R | 0 | Reserved: set to 0 |
| 12 | RE_TUNE_EVENT_SIGNAL_EN | RW | R | 0 | Reserved: set to 0 |
| 13 | FX_EVENT_SIGNAL_EN | RW | R | 0 | FX Event Signal Enable<br>Values:<br>- 0x0 (FALSE): Masked<br>- 0x1 (TRUE): Enabled |
| 14 | CQE_EVENT_SIGNAL_EN | RW | R | 0 | Command Queuing Engine Event Signal Enable<br>Values:<br>- 0x0 (FALSE): Masked<br>- 0x1 (TRUE): Enabled |

### 27.3.2.25 SDHC_CORE_ERROR_INT_SIGNAL_EN_R

**Description:** Error Interrupt Signal Enable Register
**Address:** 0x4046103A
**Offset:** 0x3A
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register is used to select the interrupt status that is notified to the Host System as an interrupt. All these status bits share the same 1-bit interrupt line. Setting any of these bits to 1
enables interrupt generation. This register is applicable for an SD/eMMC/UHS-II mode.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | CUR_LMT_ERR_SIGNAL_EN [7:7] | DATA_END_BIT_ERR_SIGNAL_EN [6:6] | DATA_CRC_ERR_SIGNAL_EN [5:5] | DATA_TOUT_ERR_SIGNAL_EN [4:4] | CMD_IDX_ERR_SIGNAL_EN [3:3] | CMD_END_BIT_ERR_SIGNAL_EN [2:2] | CMD_CRC_ERR_SIGNAL_EN [1:1] | CMD_TOUT_ERR_SIGNAL_EN [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VENDOR_ERR_SIGNAL_EN3 [15:15] | VENDOR_ERR_SIGNAL_EN2 [14:14] | VENDOR_ERR_SIGNAL_EN1 [13:13] | BOOT_ACK_ERR_SIGNAL_EN [12:12] | RESP_ERR_SIGNAL_EN [11:11] | TUNING_ERR_SIGNAL_EN [10:10] | ADMA_ERR_SIGNAL_EN [9:9] | AUTO_CMD_ERR_SIGNAL_EN [8:8] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | CMD_TOUT_ERR_SIGNAL_EN | RW | R | 0 | Command Timeout Error Signal Enable (SD/eMMC Mode only)<br>Values:<br>- 0x0 (FALSE): Masked<br>- 0x1 (TRUE): Enabled |
| 1 | CMD_CRC_ERR_SIGNAL_EN | RW | R | 0 | Command CRC Error Signal Enable (SD/eMMC Mode only)<br>Values:<br>- 0x0 (FALSE): Masked<br>- 0x1 (TRUE): Enabled |
| 2 | CMD_END_BIT_ERR_SIGNAL_EN | RW | R | 0 | Command End Bit Error Signal Enable (SD/eMMC Mode only)<br>Values:<br>- 0x0 (FALSE): Masked<br>- 0x1 (TRUE): Enabled |
| 3 | CMD_IDX_ERR_SIGNAL_EN | RW | R | 0 | Command Index Error Signal Enable (SD/eMMC Mode only)<br>Values:<br>- 0x0 (FALSE): No error<br>- 0x1 (TRUE): Error |
| 4 | DATA_TOUT_ERR_SIGNAL_EN | RW | R | 0 | Data Timeout Error Signal Enable (SD/eMMC Mode only)<br>Values:<br>- 0x0 (FALSE): Masked<br>- 0x1 (TRUE): Enabled |
| 5 | DATA_CRC_ERR_SIGNAL_EN | RW | R | 0 | Data CRC Error Signal Enable (SD/eMMC Mode only)<br>Values:<br>- 0x0 (FALSE): Masked<br>- 0x1 (TRUE): Enabled |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 6 | DATA_END_BIT_ERR_SIGNAL_EN | RW | R | 0 | Data End Bit Error Signal Enable (SD/eMMC Mode only)<br>Values:<br>- 0x0 (FALSE): Masked<br>- 0x1 (TRUE): Enabled |
| 7 | CUR_LMT_ERR_SIGNAL_EN | RW | R | 0 | Current Limit Error Signal Enable<br>Values:<br>- 0x0 (FALSE): Masked<br>- 0x1 (TRUE): Enabled |
| 8 | AUTO_CMD_ERR_SIGNAL_EN | RW | R | 0 | Auto CMD Error Signal Enable (SD/eMMC Mode only)<br>Values:<br>- 0x0 (FALSE): Masked<br>- 0x1 (TRUE): Enabled |
| 9 | ADMA_ERR_SIGNAL_EN | RW | R | 0 | ADMA Error Signal Enable<br>Values:<br>- 0x0 (FALSE): Masked<br>- 0x1 (TRUE): Enabled |
| 10 | TUNING_ERR_SIGNAL_EN | RW | R | 0 | Reserved: set to 0 |
| 11 | RESP_ERR_SIGNAL_EN | RW | R | 0 | Response Error Signal Enable (SD Mode only)<br>Values:<br>- 0x0 (FALSE): Masked<br>- 0x1 (TRUE): Enabled |
| 12 | BOOT_ACK_ERR_SIGNAL_EN | RW | R | 0 | Boot Acknowledgment Error (eMMC Mode only). Setting this bit to 1 enables generating interrupt signal when<br>Boot Acknowledgement Error in Error Interrupt Status register is set.<br>Values:<br>- 0x0 (FALSE): Masked<br>- 0x1 (TRUE): Enabled |
| 13 | VENDOR_ERR_SIGNAL_EN1 | RW | R | 0 | Reserved: set to 0 |
| 14 | VENDOR_ERR_SIGNAL_EN2 | RW | R | 0 | Reserved: set to 0 |
| 15 | VENDOR_ERR_SIGNAL_EN3 | RW | R | 0 | Reserved: set to 0 |

### 27.3.2.26 SDHC_CORE_AUTO_CMD_STAT_R

**Description:** Auto CMD Status Register
**Address:** 0x4046103C
**Offset:** 0x3C
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register is used to indicate the CMD12 response error of Auto CMD12, and the CMD23 response error of Auto CMD23. The Host driver can determine the kind of Auto CMD12/CMD23 errors that can occur in this register. Auto CMD23 errors are indicated in bit 04-01.
This register is valid only when Auto CMD Error is set. This register is applicable for an SD/eMMC
mode.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | CMD_NOT_ISSUED_AUTO_CMD12 [7:7] | None [6:6] | AUTO_CMD_RESP_ERR [5:5] | AUTO_CMD_IDX_ERR [4:4] | AUTO_CMD_EBIT_ERR [3:3] | AUTO_CMD_CRC_ERR [2:2] | AUTO_CMD_TOUT_ERR [1:1] | AUTO_CMD12_NOT_EXEC [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | AUTO_CMD12_NOT_EXEC | R | RW | 0 | Auto CMD12 Not Executed<br>If multiple memory block data transfer is not started due to a<br>command error, this bit is not set because it is not necessary<br>to issue an Auto CMD12. Setting this bit to 1 means that the<br>Host Controller cannot issue Auto CMD12 to stop multiple<br>memory block data transfer, due to some error. If this bit is<br>set to 1, error status bits (D04-D01) is meaningless.<br>This bit is set to 0 when Auto CMD Error is generated by<br>Auto CMD23.<br>Values:<br>- 0x1 (TRUE): Not Executed<br>- 0x0 (FALSE): Executed |
| 1 | AUTO_CMD_TOUT_ERR | R | RW | 0 | Auto CMD Timeout Error<br>This bit is set if no response is returned with 64 SDCLK<br>cycles from the end bit of the command.<br>If this bit is set to 1, error status bits (D04-D01) are meaningless.<br>Values:<br>- 0x1 (TRUE): Time out<br>- 0x0 (FALSE): No Error |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 2 | AUTO_CMD_CRC_ERR | R | RW | 0 | Auto CMD CRC Error<br>This bit is set when detecting a CRC error in the command<br>response.<br>Values:<br>- 0x1 (TRUE): CRC Error Generated<br>- 0x0 (FALSE): No Error |
| 3 | AUTO_CMD_EBIT_ERR | R | RW | 0 | Auto CMD End Bit Error<br>This bit is set when detecting that the end bit of command<br>response is 0.<br>Values:<br>- 0x1 (TRUE): End Bit Error Generated<br>- 0x0 (FALSE): No Error |
| 4 | AUTO_CMD_IDX_ERR | R | RW | 0 | Auto CMD Index Error<br>This bit is set if the command index error occurs in response<br>to a command.<br>Values:<br>- 0x1 (TRUE): Error<br>- 0x0 (FALSE): No Error |
| 5 | AUTO_CMD_RESP_ERR | R | RW | 0 | Auto CMD Response Error<br>This bit is set when Response Error Check Enable in the<br>Transfer Mode register is set to 1 and an error is detected in<br>R1 response of either Auto CMD12 or CMD13. This status is<br>ignored if any bit between D00 to D04 is set to 1.<br>Values:<br>- 0x1 (TRUE): Error<br>- 0x0 (FALSE): No Error |
| 7 | CMD_NOT_ISSUED<br>_AUTO_CMD12 | R | RW | 0 | Command Not Issued By Auto CMD12 Error<br>If this bit is set to 1, CMD_wo_DAT is not executed due to an<br>Auto CMD12 Error (D04-D01) in this register.<br>This bit is set to 0 when Auto CMD Error is generated by<br>Auto CMD23.<br>Values:<br>- 0x1 (TRUE): Not Issued<br>- 0x0 (FALSE): No Error |

### 27.3.2.27 SDHC_CORE_HOST_CTRL2_R

**Description:** Host Control 2 Register
**Address:** 0x4046103E
**Offset:** 0x3E
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register is used to control how the Host Controller operates. This register is applicable for an SD/eMMC/UHS-II mode.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | SAMPLE_CLK_SEL [7:7] | EXEC_TUNING [6:6] | DRV_STRENGTH_SEL [5:4] | | SIGNALING_EN [3:3] | UHS_MODE_SEL [2:0] | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | PRESET_VAL_ENABLE [15:15] | ASYNC_INT_ENABLE [14:14] | ADDRESSING [13:13] | HOST_VER4_ENABLE [12:12] | CMD23_ENABLE [11:11] | ADMA2_LEN_MODE [10:10] | None [9:9] | UHS2_IF_ENABLE [8:8] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:2 | UHS_MODE_SEL | RW | R | 0 | UHS Mode/eMMC Speed Mode Select<br>These bits are used to select UHS mode in the SD mode of<br>operation. In eMMC mode, these bits are used to select<br>eMMC Speed mode.<br>UHS-I Mode:<br>- 0x0: SDR12<br>- 0x1: SDR25<br>- 0x2: SDR50<br>- 0x3: Reserved<br>- 0x4: DDR50<br>- 0x5: Reserved<br>- 0x6: Reserved<br>- 0x7: Reserved<br>eMMC Speed Mode (eMMC mode only):<br>- 0x0: Legacy<br>- 0x1: High Speed SDR<br>- 0x2: Reserved<br>- 0x3: Reserved<br>- 0x4: High Speed DDR<br>- 0x5: Reserved<br>- 0x6: Reserved<br>- 0x7: Reserved |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 3 | SIGNALING_EN | RW | RW | 0 | 1.8V Signaling Enable<br>This bit controls voltage regulator for I/O cell in SD UHS-I mode. Setting this bit from 0 to 1 starts changing the<br>signal voltage from 3.3V to 1.8V. Host Controller clears this<br>bit if switching to 1.8V signaling fails per protocol. The value is reflected on the io_volt_sel output which can then be used to change an external regulator to supply 1.8V instead of 3.3V on the VDDIO pin associated with the CLK/CMD/DAT signals.<br>Note: This bit must be set for all UHS-I speed modes (SDR12/SDR25/SDR50/DDR50).<br>Values:<br>- 0x0 (V_3_3): 3.3V Signalling<br>- 0x1 (V_1_8): 1.8V Signalling |
| 4:5 | DRV_STRENGTH_SEL | RW | RW | 0 | Driver Strength Select<br>These bits are used to select the Host Controller output driver in<br>1.8V signaling UHS-I/eMMC speed modes. The value is reflected on the io_drive_strength[1:0] output.<br>- 0x0 (TYPEB): Driver TYPEB is selected<br>- 0x1 (TYPEA): Driver TYPEA is selected<br>- 0x2 (TYPEC): Driver TYPEC is selected<br>- 0x3 (TYPED): Driver TYPED is selected |
| 6 | EXEC_TUNING | RW | RW | 0 | Reserved: set to 0 |
| 7 | SAMPLE_CLK_SEL | RW | RW | 0 | Reserved: set to 0 |
| 8 | UHS2_IF_ENABLE | RW | R | 0 | Reserved: set to 0 |
| 10 | ADMA2_LEN_MODE | RW | R | 0 | ADMA2 Length Mode<br>This bit selects ADMA2 Length mode to be either 16-bit or<br>26-bit.<br>Values:<br>- 0x0 (FALSE): 16-bit Data Length Mode<br>- 0x1 (TRUE): 26-bit Data Length Mode |
| 11 | CMD23_ENABLE | RW | R | 0 | CMD23 Enable<br>If the card supports CMD23, this bit is set to 1. This bit is<br>used to select Auto CMD23 or Auto CMD12 for ADMA3 data<br>transfer.<br>Values:<br>- 0x0 (FALSE): Auto CMD23 is disabled<br>- 0x1 (TRUE): Auto CMD23 is enabled |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 12 | HOST_VER4_ENABLE | RW | R | 0 | Host Version 4 Enable<br>This bit selects either Version 3.00 compatible mode or Version 4 mode.<br>Functions of following fields are modified for Host Version 4<br>mode:<br>- SDMA Address: SDMA uses ADMA System Address (05Fh-058h) instead of SDMA System Address register<br>(003h-000h)<br>- ADMA2/ADMA3 selection: ADMA3 is selected by DMA<br>select in Host Control 1 register<br>- 32-bit Block Count: SDMA System Address register (003h-000h) is modified to 32-bit Block Count register<br>Note: It is recommended not to program ADMA3 Integrated<br>Descriptor Address registers and<br>Command Queuing registers (if applicable) while operating<br>in Host version less than 4 mode (Host Version 4 Enable =<br>0).<br>Values:<br>- 0x0 (FALSE): Version 3.00 compatible mode<br>- 0x1 (TRUE): Version 4 mode |
| 13 | ADDRESSING | RW | R | 0 | Reserved: set to 0 |
| 14 | ASYNC_INT_ENABLE | RW | R | 0 | Asynchronous Interrupt Enable<br>This bit can be set if a card supports asynchronous interrupts and Asynchronous Interrupt Support is set to 1 in<br>the Capabilities register.<br>Values:<br>- 0x0 (FALSE): Disabled<br>- 0x1 (TRUE): Enabled |
| 15 | PRESET_VAL_ENABLE | RW | R | 0 | Reserved: set to 0 |

### 27.3.2.28 SDHC_CORE_CAPABILITIES1_R

**Description:** Capabilities 1 Register - 0 to 31
**Address:** 0x40461040
**Offset:** 0x40
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register provides the Host Driver with information specific to the Host Controller implementation. The host controller may implement these values as fixed or loaded from the flash
memory during power on initialization. Capabilities register is segregated into two 32-bit registers:
CAPABILITIES1_R and CAPABILITIES2_R. The CAPABILITIES1_R register is the lower part of
Capabilities register.
**Default:** 0x276C6481

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | TOUT_CLK_UNIT [7:7] | None [6:6] | TOUT_CLK_FREQ [5:0] | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | BASE_CLK_FREQ [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | SUS_RES_SUPPORT [23:23] | SDMA_SUPPORT [22:22] | HIGH_SPEED_SUPPORT [21:21] | None [20:20] | ADMA2_SUPPORT [19:19] | EMBEDDED_8_BIT [18:18] | MAX_BLK_LEN [17:16] | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | SLOT_TYPE_R [31:30] | | ASYNC_INT_SUPPORT [29:29] | SYS_ADDR_64_V3 [28:28] | SYS_ADDR_64_V4 [27:27] | VOLT_18 [26:26] | VOLT_30 [25:25] | VOLT_33 [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:5 | TOUT_CLK_FREQ | R | R | 1 | Timeout Clock Frequency<br>This bit shows the base clock frequency used to detect Data<br>Timeout Error. The Timeout Clock unit defines the unit of<br>timeout clock frequency. It can be KHz or MHz.<br>- 0x00 - Get information through another method<br>- 0x01 - 1KHz / 1MHz<br>- 0x02 - 2KHz / 2MHz<br>- 0x03 - 3KHz / 3MHz<br>- .....<br>- 0x3F - 63KHz / 63MHz |
| 7 | TOUT_CLK_UNIT | R | R | 1 | Timeout Clock Unit<br>This bit shows the unit of base clock frequency used to detect Data TImeout Error.<br>Values:<br>- 0x0 (KHZ): KHz<br>- 0x1 (MHZ): MHz |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 8:15 | BASE_CLK_FREQ | R | R | 100 | Base Clock Frequency for SD clock<br>These bits indicate the base (maximum) clock frequency for<br>the SD Clock. The definition of these bits depend on the Host<br>Controller Version.<br>- 6-Bit Base Clock Frequency: This mode is supported by<br>the Host Controller version 1.00 and 2.00. The upper 2 bits are not effective and are always 0. The unit values are 1 MHz. The supported clock range is 10 MHz to 63 MHz.<br>- 0x00 - Get information through another method<br>- 0x01 - 1 MHz<br>- 0x02 - 2 MHz<br>- .....<br>- 0x3F - 63 MHz<br>- 0x40-0xFF - Not Supported<br>- 8-Bit Base Clock Frequency: This mode is supported by<br>the Host Controller version 3.00. The unit values are 1 MHz. The supported clock range is 10 MHz to 255 MHz.<br>- 0x00 - Get information through another method<br>- 0x01 - 1 MHz<br>- 0x02 - 2 MHz<br>- .....<br>- 0xFF - 255 MHz<br>If the frequency is 16.5 MHz, the larger value is set to 0001001b (17 MHz) because the Host Driver uses this value<br>to calculate the clock divider value and it does not exceed<br>the upper limit of the SD Clock frequency. If these bits are all<br>0, the Host system has to get information using a different<br>method. |
| 16:17 | MAX_BLK_LEN | R | R | 0 | Maximum Block Length<br>This bit indicates the maximum block size that the Host driver<br>can read and write to the buffer in the Host Controller. The<br>buffer transfers this block size without wait cycles. The transfer block length is always 512 bytes for the SD Memory<br>irrespective of this bit.<br>Value is fixed to (including the default value):<br>0x0: when MAX_BLK_SIZE=0 indicating 512 Bytes<br>0x1: when MAX_BLK_SIZE=1 indicating 1024 Bytes<br>0x2: Reserved<br>0x3: Reserved |
| 18 | EMBEDDED_8_BIT | R | R | 1 | 8-bit Support for Embedded Device<br>This bit indicates whether the Host Controller is capable of<br>using an 8-bit bus width mode. This bit is not effective when<br>the Slot Type is set to 10b.<br>Values:<br>- 0x0 (FALSE): 8-bit Bus Width not Supported<br>- 0x1 (TRUE): 8-bit Bus Width Supported |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 19 | ADMA2_SUPPORT | R | R | 1 | ADMA2 Support<br>This bit indicates whether the Host Controller is capable of<br>using ADMA2.<br>Values:<br>- 0x0 (FALSE): ADMA2 not Supported<br>- 0x1 (TRUE): ADMA2 Supported |
| 21 | HIGH_SPEED _SUPPORT | R | R | 1 | High Speed Support<br>This bit indicates whether the Host Controller and the Host<br>System supports High Speed mode and they can supply the<br>SD Clock frequency from 25 MHz to 50 MHz.<br>Values:<br>- 0x0 (FALSE): High Speed not Supported<br>- 0x1 (TRUE): High Speed Supported |
| 22 | SDMA_SUPPORT | R | R | 1 | SDMA Support<br>This bit indicates whether the Host Controller is capable of<br>using SDMA to transfer data between the system memory<br>and the Host Controller directly.<br>Values:<br>- 0x0 (FALSE): SDMA not Supported<br>- 0x1 (TRUE): SDMA Supported |
| 23 | SUS_RES_SUPPORT | R | R | 0 | Suspense/Resume Support<br>This bit indicates whether the Host Controller supports Suspend/Resume functionality. If this bit is 0, the Host Driver<br>does not issue either Suspend or Resume commands because the Suspend and Resume mechanism is not supported.<br>Values:<br>- 0x0 (FALSE): Not Supported<br>- 0x1 (TRUE): Supported |
| 24 | VOLT_33 | R | R | 1 | Voltage Support 3.3V<br>Values:<br>- 0x0 (FALSE): 3.3V Not Supported<br>- 0x1 (TRUE): 3.3V Supported |
| 25 | VOLT_30 | R | R | 1 | Voltage Support 3.0V<br>Values:<br>- 0x0 (FALSE): 3.0V Not Supported<br>- 0x1 (TRUE): 3.0V Supported |
| 26 | VOLT_18 | R | R | 1 | Voltage Support 1.8V<br>Values:<br>- 0x0 (FALSE): 1.8V Not Supported<br>- 0x1 (TRUE): 1.8V Supported |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 27 | SYS_ADDR_64_V4 | R | R | 0 | 64-bit System Address Support for V4<br>This bit sets the Host Controller to support 64-bit System<br>Addressing of V4 mode. When this bit is set to 1, full or part<br>of 64-bit address must be used to decode the Host Controller<br>Registers so that Host Controller Registers can be placed<br>above system memory area. 64-bit address decode of Host<br>Controller registers is effective regardless of setting to 64-bit<br>Addressing in Host Control 2.<br>If this bit is set to 1, 64-bit DMA Addressing for version 4 is<br>enabled by setting Host Version 4 Enable (HOST_VER4_ENABLE = 1) and by setting 64-bit Addressing (ADDRESSING =1) in the Host Control 2 register. SDMA can be used and ADMA2 uses 128-bit Descriptor.<br>Values:<br>- 0x0 (FALSE): 64-bit System Address for V4 is Not Supported<br>- 0x1 (TRUE): 64-bit System Address for V4 is Supported |
| 28 | SYS_ADDR_64_V3 | R | R | 0 | 64-bit System Address Support for V3<br>This bit sets the Host controller to support 64-bit System<br>Addressing of V3 mode.<br>SDMA cannot be used in 64-bit Addressing in Version 3<br>Mode.<br>If this bit is set to 1, 64-bit ADMA2 with using 96-bit Descriptor can be enabled by setting Host Version 4 Enable<br>(HOST_VER4_ENABLE = 0) and DMA select (DMA_SEL =<br>11b).<br>Values:<br>- 0x0 (FALSE): 64-bit System Address for V3 is Not Supported<br>- 0x1 (TRUE): 64-bit System Address for V3 is Supported |
| 29 | ASYNC_INT_SUPPORT | R | R | 1 | Asynchronous Interrupt Support (SD Mode only)<br>Values:<br>- 0x0 (FALSE): Asynchronous Interrupt Not Supported<br>- 0x1 (TRUE): Asynchronous Interrupt Supported |
| 30:31 | SLOT_TYPE_R | R | R | 0 | Slot Type<br>These bits indicate usage of a slot by a specific Host System.<br>Values:<br>- 0x0 (REMOVABLE_SLOT): Removable Card Slot<br>- 0x1 (EMBEDDED_SLOT): Embedded Slot for one Device<br>- 0x2 (SHARED_SLOT): Shared Bus Slot (SD mode)<br>- 0x3 (UHS2_EMBEDDED_SLOT): UHS-II Multiple Embedded Devices |

### 27.3.2.29 SDHC_CORE_CAPABILITIES2_R

**Description:** Capabilities Register - 32 to 63
**Address:** 0x40461044
**Offset:** 0x44
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** register provides the Host Driver with information specific to the Host Controller implementation. The host controller may implement these values as fixed or as loaded from flash
memory during power on initialization. Capabilities register is segregated into two 32-bit registers,
namely CAPABILITIES1_R and CAPABILITIES2_R. The CAPABILITIES2_R register is upper part of
Capabilities register.
**Default:** 0x8000077

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:7] | DRV _TYPED [6:6] | DRV _TYPEC [5:5] | DRV _TYPEA [4:4] | UHS2 _SUPPORT [3:3] | DDR50 _SUPPORT [2:2] | SDR104 _SUPPORT [1:1] | SDR50 _SUPPORT [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | RE_TUNING_MODES [15:14] | | USE _TUNING _SDR50 [13:13] | None [12:12] | RETUNE_CNT [11:8] | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | CLK_MUL [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:29] | | | VDD2_18V _SUPPORT [28:28] | ADMA3 _SUPPORT [27:27] | None [26:24] | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | SDR50_SUPPORT | R | R | 1 | SDR50 Support (UHS-I only)<br>Thsi bit indicates that SDR50 is supported. The bit 13 (USE_TUNING_SDR50) indicates whether SDR50 requires<br>tuning or not.<br>Values:<br>- 0x0 (FALSE): SDR50 is not supported<br>- 0x1 (TRUE): SDR50 is supported |
| 1 | SDR104_SUPPORT | R | R | 1 | SDR104 Support (UHS-I only)<br>This bit mentions that SDR104 requires tuning.<br>Values:<br>- 0x0 (FALSE): SDR104 is not supported<br>- 0x1 (TRUE): SDR104 is supported (NOT ACTUALLY SUPPORTED) |
| 2 | DDR50_SUPPORT | R | R | 1 | DDR50 Support (UHS-I only)<br>Values:<br>- 0x0 (FALSE): DDR50 is not supported<br>- 0x1 (TRUE): DDR50 is supported |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 3 | UHS2_SUPPORT | R | R | 0 | UHS-II Support (UHS-II only)<br>This bit indicates whether Host Controller supports UHS-II.<br>Values:<br>- 0x0 (FALSE): UHS-II is not supported<br>- 0x1 (TRUE): UHS-II is supported |
| 4 | DRV_TYPEA | R | R | 1 | Driver Type A Support (UHS-I only)<br>This bit indicates support of Driver Type A for 1.8 Signaling.<br>Values:<br>- 0x0 (FALSE): Driver Type A is not supported<br>- 0x1 (TRUE): Driver Type A is supported |
| 5 | DRV_TYPEC | R | R | 1 | Driver Type C Support (UHS-I only)<br>This bit indicates support of Driver Type C for 1.8 Signaling.<br>Values:<br>- 0x0 (FALSE): Driver Type C is not supported<br>- 0x1 (TRUE): Driver Type C is supported |
| 6 | DRV_TYPED | R | R | 1 | Driver Type D Support (UHS-I only)<br>This bit indicates support of Driver Type D for 1.8 Signaling.<br>Values:<br>- 0x0 (FALSE): Driver Type D is not supported<br>- 0x1 (TRUE): Driver Type D is supported |
| 8:11 | RETUNE_CNT | R | R | 0 | Timer Count for Re-Tuning (UHS-I only)<br>- 0x0: Re-Tuning Timer disabled<br>- 0x1: 1 seconds<br>- 0x2: 2 seconds<br>- 0x3: 4 seconds<br>- .....<br>- 0xB: 1024 seconds<br>- 0xC: Reserved<br>- 0xD: Reserved<br>- 0xE: Reserved<br>- 0xF: Get information from other source |
| 13 | USE_TUNING_SDR50 | R | R | 0 | Use Tuning for SDR50 (UHS-I only)<br>Values:<br>- 0x0 (ZERO): SDR50 does not require tuning<br>- 0x1 (ONE): SDR50 requires tuning |
| 14:15 | RE_TUNING_MODES | R | R | 0 | Re-Tuning Modes (UHS-I only)<br>These bits select the re-tuning method and limit the maximum data length.<br>Values:<br>- 0x0 (MODE1): Timer<br>- 0x1 (MODE2): Timer and Re-Tuning Request (Not supported)<br>- 0x2 (MODE3): Auto Re-Tuning (for transfer)<br>- 0x3 (RSVD_MODE): Reserved |
| 16:23 | CLK_MUL | R | R | 0 | Clock Multiplier<br>These bits indicate the clock multiplier of the programmable<br>clock generator. Setting these bits to 0 means that the Host<br>Controller does not support a programmable clock generator.<br>- 0x0: Clock Multiplier is not Supported<br>- 0x1: Clock Multiplier M = 2<br>- 0x2: Clock Multiplier M = 3<br>- .....<br>- 0xFF: Clock Multiplier M = 256 |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 27 | ADMA3_SUPPORT | R | R | 1 | ADMA3 Support<br>This bit indicates whether the Host Controller is capable of<br>using ADMA3.<br>Values:<br>- 0x0 (FALSE): ADMA3 not Supported<br>- 0x1 (TRUE): ADMA3 Supported |
| 28 | VDD2_18V_SUPPORT | R | R | 0 | 1.8V VDD2 Support<br>This bit indicates support of VDD2 for the Host System.<br>Values:<br>- 0x0 (FALSE): 1.8V VDD2 is not Supported<br>- 0x1 (TRUE): 1.8V VDD2 is Supported |

### 27.3.2.30 SDHC_CORE_CURR_CAPABILITIES1_R

**Description:** Current Capabilities Register - 0 to 31
**Address:** 0x40461048
**Offset:** 0x48
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register indicate the maximum current capability for each voltage, for VDD1. The value is meaningful if the Voltage Support is set in the Capabilities register. If this information is
supplied by the Host System through another method, all the Maximum Current Capabilities registers are set to 0.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | MAX_CUR_33V [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | MAX_CUR_30V [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | MAX_CUR_18V [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | MAX_CUR_33V | R | R | 0 | Maximum Current for 3.3V<br>This bit specifies the Maximum Current for 3.3V VDD1 power<br>supply for the card.<br>- 0: Get information through another method<br>- 1: 4mA<br>- 2: 8mA<br>- 3: 13mA<br>- .....<br>- 255: 1020mA |
| 8:15 | MAX_CUR_30V | R | R | 0 | Maximum Current for 3.0V<br>This bit specifies the Maximum Current for 3.0V VDD1 power<br>supply for the card.<br>- 0: Get information through another method<br>- 1: 4mA<br>- 2: 8mA<br>- 3: 13mA<br>- .....<br>- 255: 1020mA |
| 16:23 | MAX_CUR_18V | R | R | 0 | Maximum Current for 1.8V<br>This bit specifies the Maximum Current for 1.8V VDD1 power<br>supply for the card.<br>- 0: Get information through another method<br>- 1: 4mA<br>- 2: 8mA<br>- 3: 13mA<br>- .....<br>- 255: 1020mA |

### 27.3.2.31 SDHC_CORE_CURR_CAPABILITIES2_R

**Description:** Maximum Current Capabilities Register - 32 to 63
**Address:** 0x4046104C
**Offset:** 0x4C
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register indicates the maximum current capability for each voltage (for VDD2). The value is meaningful if Voltage Support is set in the Capabilities register. If this information is supplied by the Host System through another method, all the Maximum Current Capabilities registers are set to 0.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | MAX_CUR_VDD2_18V [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | MAX_CUR_VDD2_18V | R | R | 0 | Maximum Current for 1.8V VDD2<br>This bit specifies the Maximum Current for 1.8V VDD2 power<br>supply for the UHS-II card.<br>- 0: Get information through another method<br>- 1: 4mA<br>- 2: 8mA<br>- 3: 13mA<br>- .....<br>- 255: 1020mA |

### 27.3.2.32 SDHC_CORE_FORCE_AUTO_CMD_STAT_R

**Description:** Force Event Register for Auto CMD Error Status register
**Address:** 0x40461050
**Offset:** 0x50
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** The register is not a physically implemented but is an address at which the Auto CMD Error Status register can be written.This register is applicable for an SD/eMMC mode.
- 1 : Sets each bit of the Auto CMD Error Status register
- 0 : No effect

**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | FORCE_CMD_NOT_ISSUED_AUTO_CMD12 [7:7] | None [6:6] | FORCE_AUTO_CMD_RESP_ERR [5:5] | FORCE_AUTO_CMD_IDX_ERR [4:4] | FORCE_AUTO_CMD_EBIT_ERR [3:3] | FORCE_AUTO_CMD_CRC_ERR [2:2] | FORCE_AUTO_CMD_TOUT_ERR [1:1] | FORCE_AUTO_CMD12_NOT_EXEC [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | FORCE_AUTO_CMD12_NOT_EXEC | W | R | 0 | Force Event for Auto CMD12 Not Executed<br>Values:<br>- 0x1 (TRUE): Auto CMD12 Not Executed Status is set<br>- 0x0 (FALSE): Not Affected |
| 1 | FORCE_AUTO_CMD_TOUT_ERR | W | R | 0 | Force Event for Auto CMD Timeout Error<br>Values:<br>- 0x1 (TRUE): Auto CMD Timeout Error Status is set<br>- 0x0 (FALSE): Not Affected |
| 2 | FORCE_AUTO_CMD_CRC_ERR | W | R | 0 | Force Event for Auto CMD CRC Error<br>Values:<br>- 0x1 (TRUE): Auto CMD CRC Error Status is set<br>- 0x0 (FALSE): Not Affected |
| 3 | FORCE_AUTO_CMD_EBIT_ERR | W | R | 0 | Force Event for Auto CMD End Bit Error<br>Values:<br>- 0x1 (TRUE): Auto CMD End Bit Error Status is set<br>- 0x0 (FALSE): Not Affected |
| 4 | FORCE_AUTO_CMD_IDX_ERR | W | R | 0 | Force Event for Auto CMD Index Error<br>Values:<br>- 0x1 (TRUE): Auto CMD Index Error Status is set<br>- 0x0 (FALSE): Not Affected |
| 5 | FORCE_AUTO_CMD_RESP_ERR | W | R | 0 | Force Event for Auto CMD Response Error<br>Values:<br>- 0x1 (TRUE): Auto CMD Response Error Status is set<br>- 0x0 (FALSE): Not Affected |
| 7 | FORCE_CMD_NOT_ISSUED_AUTO_CMD12 | W | R | 0 | Force Event for Command Not Issued By Auto CMD12 Error<br>Values:<br>- 0x1 (TRUE): Command Not Issued By Auto CMD12 Error<br>Status is set<br>- 0x0 (FALSE): Not Affected |

### 27.3.2.33 SDHC_CORE_FORCE_ERROR_INT_STAT_R

**Description:** Force Event Register for Error Interrupt Status
**Address:** 0x40461052
**Offset:** 0x52
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register is not physically implemented but is an address at which the Error Interrupt Status register can be written. The effect of a write to this address is reflected in the Error Interrupt Status register if the corresponding bit of the Error Interrupt Status Enable register is set. This register is applicable for an SD/eMMC/UHS-II mode.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | FORCE_CUR_LMT_ERR [7:7] | FORCE_DATA_END_BIT_ERR [6:6] | FORCE_DATA_CRC_ERR [5:5] | FORCE_DATA_TOUT_ERR [4:4] | FORCE_CMD_IDX_ERR [3:3] | FORCE_CMD_END_BIT_ERR [2:2] | FORCE_CMD_CRC_ERR [1:1] | FORCE_CMD_TOUT_ERR [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | FORCE_VENDOR_ERR3 [15:15] | FORCE_VENDOR_ERR2 [14:14] | FORCE_VENDOR_ERR1 [13:13] | FORCE_BOOT_ACK_ERR [12:12] | FORCE_RESP_ERR [11:11] | FORCE_TUNING_ERR [10:10] | FORCE_ADMA_ERR [9:9] | FORCE_AUTO_CMD_ERR [8:8] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | FORCE_CMD_TOUT_ERR | RW | R | 0 | Force Event for Command Timeout Error (SD/eMMC Mode only)<br>Values:<br>- 0x0 (FALSE): Not Affected<br>- 0x1 (TRUE): Command Timeout Error Status is set |
| 1 | FORCE_CMD_CRC_ERR | RW | R | 0 | Force Event for Command CRC Error (SD/eMMC Mode only)<br>Values:<br>- 0x0 (FALSE): Not Affected<br>- 0x1 (TRUE): Command CRC Error Status is set |
| 2 | FORCE_CMD_END_BIT_ERR | RW | R | 0 | Force Event for Command End Bit Error (SD/eMMC Mode only)<br>Values:<br>- 0x0 (FALSE): Not Affected<br>- 0x1 (TRUE): Command End Bit Error Status is set |
| 3 | FORCE_CMD_IDX_ERR | RW | R | 0 | Force Event for Command Index Error (SD/eMMC Mode only)<br>Values:<br>- 0x0 (FALSE): Not Affected<br>- 0x1 (TRUE): Command Index Error Status is set |
| 4 | FORCE_DATA_TOUT_ERR | RW | R | 0 | Force Event for Data Timeout Error (SD/eMMC Mode only)<br>Values:<br>- 0x0 (FALSE): Not Affected<br>- 0x1 (TRUE): Data Timeout Error Status is set |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 5 | FORCE_DATA_CRC _ERR | RW | R | 0 | Force Event for Data CRC Error (SD/eMMC Mode only)<br>Values:<br>- 0x0 (FALSE): Not Affected<br>- 0x1 (TRUE): Data CRC Error Status is set |
| 6 | FORCE_DATA_END_BIT _ERR | RW | R | 0 | Force Event for Data End Bit Error (SD/eMMC Mode only)<br>Values:<br>- 0x0 (FALSE): Not Affected<br>- 0x1 (TRUE): Data End Bit Error Status is set |
| 7 | FORCE_CUR_LMT_ERR | RW | R | 0 | Force Event for Current Limit Error<br>Values:<br>- 0x0 (FALSE): Not Affected<br>- 0x1 (TRUE): Current Limit Error Status is set |
| 8 | FORCE_AUTO_CMD _ERR | RW | R | 0 | Force Event for Auto CMD Error (SD/eMMC Mode only)<br>Values:<br>- 0x0 (FALSE): Not Affected<br>- 0x1 (TRUE): Auto CMD Error Status is set |
| 9 | FORCE_ADMA_ERR | RW | R | 0 | Force Event for ADMA Error<br>Values:<br>- 0x0 (FALSE): Not Affected<br>- 0x1 (TRUE): ADMA Error Status is set |
| 10 | FORCE_TUNING_ERR | RW | R | 0 | Force Event for Tuning Error (UHS-I Mode only)<br>Values:<br>- 0x0 (FALSE): Not Affected<br>- 0x1 (TRUE): Tuning Error Status is set |
| 11 | FORCE_RESP_ERR | RW | R | 0 | Force Event for Response Error (SD Mode only)<br>Values:<br>- 0x0 (FALSE): Not Affected<br>- 0x1 (TRUE): Response Error Status is set |
| 12 | FORCE_BOOT_ACK _ERR | RW | R | 0 | Force Event for Boot Ack error<br>Values:<br>- 0x0 (FALSE): Not Affected<br>- 0x1 (TRUE): Boot ack Error Status is set |
| 13 | FORCE_VENDOR_ERR1 | RW | R | 0 | This bit (FORCE_VENDOR_ERR1) of the FORCE_ERROR_INT_STAT_R register is reserved. It always returns 0. |
| 14 | FORCE_VENDOR_ERR2 | RW | R | 0 | This bit (FORCE_VENDOR_ERR2) of the FORCE_ERROR_INT_STAT_R register is reserved. It always returns 0. |
| 15 | FORCE_VENDOR_ERR3 | RW | R | 0 | This bit (FORCE_VENDOR_ERR3) of the FORCE_ERROR_INT_STAT_R register is reserved. It always returns 0. |

### 27.3.2.34 SDHC_CORE_ADMA_ERR_STAT_R

**Description:** ADMA Error Status Register
**Address:** 0x40461054
**Offset:** 0x54
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register stores the ADMA state during an ADMA error. This register is applicable for an SD/eMMC/UHS-II mode.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:3] | | | | | ADMA_LEN_ERR [2:2] | ADMA_ERR_STATES [1:0] | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:1 | ADMA_ERR_STATES | R | RW | 0 | ADMA Error States<br>These bits indicate the state of ADMA when an error occurs<br>during ADMA data transfer.<br>Values:<br>- 0x0 (ST_STOP): Stop DMA - SYS_ADR register points to<br>a location next to the error descriptor<br>- 0x1 (ST_FDS): Fetch Descriptor - SYS_ADR register points to the error descriptor<br>- 0x2 (UNUSED): Never set this state<br>- 0x3 (ST_TFR): Transfer Data - SYS_ADR register points<br>to a location next to the error descriptor |
| 2 | ADMA_LEN_ERR | R | RW | 0 | ADMA Length Mismatch Error States<br>This error occurs in the following instances:<br>- While the Block Count Enable is being set, the total data<br>length specified by the Descriptor table is different from<br>that specified by the Block Count and Block Length<br>- When the total data length cannot be divided by the block<br>length<br>Values:<br>- 0x0 (NO_ERR): No Error<br>- 0x1 (ERROR): Error |

### 27.3.2.35 SDHC_CORE_ADMA_SA_LOW_R

**Description:** ADMA System Address Register - Low
**Address:** 0x40461058
**Offset:** 0x58
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register holds the lower 32-bit system address for DMA transfer. This register is applicable for an SD/eMMC/UHS-II mode.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | ADMA_SA_LOW [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | ADMA_SA_LOW [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | ADMA_SA_LOW [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | ADMA_SA_LOW [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | ADMA_SA_LOW | RW | RW | 0 | ADMA System Address<br>These bits indicate the lower 32 bits of the ADMA system<br>address.<br>- SDMA: If Host Version 4 Enable is set to 1, this register<br>stores the system address of the data location<br>- ADMA2: This register stores the byte address of the executing command of the descriptor table<br>- ADMA3: This register is set by ADMA3. ADMA2 increments the address of this register that points to the<br>next line, every time a Descriptor line is fetched. |

### 27.3.2.36 SDHC_CORE_ADMA_ID_LOW_R

**Description:** ADMA3 Integrated Descriptor Address Register - Low
**Address:** 0x40461078
**Offset:** 0x78
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register holds the lower 32-bit Integrated Descriptor address.This register is applicable for an SD/eMMC/UHS-II mode.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | ADMA_ID_LOW [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | ADMA_ID_LOW [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | ADMA_ID_LOW [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | ADMA_ID_LOW [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | ADMA_ID_LOW | RW | RW | 0 | ADMA Integrated Descriptor Address<br>These bits indicate the lower 32-bit of the ADMA Integrated<br>Descriptor address. The start address of Integrated Descriptor is set to these register bits. The ADMA3 fetches<br>one Descriptor Address and increments these bits to indicate<br>the next Descriptor address. |

### 27.3.2.37 SDHC_CORE_HOST_CNTRL_VERS_R

**Description:** Host Controller Version
**Address:** 0x404610FE
**Offset:** 0xFE
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register is used to indicate the Host Controller Version number.
**Default:** 0x5

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | SPEC_VERSION_NUM [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VENDOR_VERSION_NUM [15:8] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | SPEC_VERSION_NUM | R | R | 5 | Specification Version Number<br>These bits indicate the Host controller specification version.<br>The upper and lower 4-bits indicate the version.<br>Values<br>0x06-0xFF are reserved.<br>Values:<br>- 0x0 (VER_1_00): SD Host Controller Specification Version 1.00<br>- 0x1 (VER_2_00): SD Host Controller Specification Version 2.00<br>- 0x2 (VER_3_00): SD Host Controller Specification Version 3.00<br>- 0x3 (VER_4_00): SD Host Controller Specification Version 4.00<br>- 0x4 (VER_4_10): SD Host Controller Specification Version 4.10<br>- 0x5 (VER_4_20): SD Host Controller Specification Version 4.20 |
| 8:15 | VENDOR_VERSION_NUM | R | R | 0 | Vendor Version Number<br>This field is reserved for the vendor version number.<br>Host<br>Driver must not use this status. |

### 27.3.2.38 SDHC_CORE_MSHC_VER_ID_R

**Description:** MSHC version
**Address:** 0x40461500
**Offset:** 0x500
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register reflects the current release number of DWC_mshc/DWC_mshc_lite.
**Default:** 0x3137302A

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | MSHC_VER_ID [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | MSHC_VER_ID [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | MSHC_VER_ID [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | MSHC_VER_ID [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | MSHC_VER_ID | R | R | 825700394 | Current release number<br>This field indicates the Synopsys DesignWare Cores DWC_mshc/DWC_mshc_lite current release number that is<br>read by an application.<br>For example, release number '1.60a' is represented in ASCII as 0x313630. Lower 8 bits read from this register can<br>be ignored by the application.<br>An application reading this register in conjunction with the<br>MSHC_VER_TYPE_R register, gathers details of the current<br>release. |

### 27.3.2.39 SDHC_CORE_MSHC_VER_TYPE_R

**Description:** MSHC version type
**Address:** 0x40461504
**Offset:** 0x504
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register reflects the current release type of DWC_mshc/DWC_mshc_lite.
**Default:** 0x67612A2A

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | MSHC_VER_TYPE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | MSHC_VER_TYPE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | MSHC_VER_TYPE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | MSHC_VER_TYPE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | MSHC_VER_TYPE | R | R | 1734421034 | Current release type<br>This field indicates the Synopsys DesignWare Cores DWC_mshc/DWC_mshc_lite current release type that is<br>read by an application.<br>For example, release type is 'ga' is represented in ASCII as<br>0x6761. Lower 16 bits read from this register can be ignored<br>by the application.<br>An application reading this register in conjunction with the<br>MSHC_VER_ID_R register, gathers details of the current<br>release. |

### 27.3.2.40 SDHC_CORE_MSHC_CTRL_R

**Description:** MSHC Control register
**Address:** 0x40461508
**Offset:** 0x508
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register is used to control the operation of MSHC Host Controller.
**Default:** 0x1

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:5] | | | SW_CG _DIS [4:4] | None [3:1] | | | CMD _CONFL ICT _CHECK [0:0] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | CMD_CONFLICT _CHECK | RW | R | 1 | Command conflict check<br>This bit enables command conflict check.<br>Note: DWC_mshc controller monitors the CMD line whenever a command is issued and checks whether the<br>value driven on sd_cmd_out matches the value on sd_cmd_in at next subsequent edge of cclk_tx to determine<br>command conflict error. This bit is cleared only if the feed<br>back delay (including IO Pad delay) is more than (t_card_clk_period - t_setup), where t_setup is the setup<br>time of a flop in DWC_mshc. The I/O pad delay is consistent<br>across CMD and DATA lines, and it is within the value: (2*t_card_clk_period - t_setup)<br>Values:<br>- 0x0 (DISABLE_CMD_CONFLICT_CHK): Disable command conflict check<br>- 0x1 (CMD_CONFLICT_CHK_LAT1): Check for command<br>conflict after 1 card clock cycle |
| 4 | SW_CG_DIS | RW | R | 0 | Internal clock gating disable control<br>This bit must be used to disable IP's internal clock gating<br>when required. when disabled clocks are not gated. Clocks<br>to the core (except hclk) must be stopped when programming this bit.<br>Values:<br>- 0x0 (ENABLE): Internal clock gates are active and clock<br>gating is controlled internally<br>- 0x1 (DISABLE): Internal clock gating is disabled, clocks<br>are not gated internally |

### 27.3.2.41 SDHC_CORE_MBIU_CTRL_R

**Description:** MBIU Control register
**Address:** 0x40461510
**Offset:** 0x510
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register is used to select the valid burst types that the AHB Master bus interface can generate. When more than one bit is set the master selects the burst it prefers among those that are enabled in this register.
**Default:** 0x1

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:4] | | | | BURST_INCR16_EN [3:3] | BURST_INCR8_EN [2:2] | BURST_INCR4_EN [1:1] | UNDEFL_INCR_EN [0:0] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | UNDEFL_INCR_EN | RW | R | 1 | Undefined INCR Burst<br>Controls generation of undefined length INCR transfer on<br>Master interface.<br>Values:<br>- 0x0 (FALSE): Undefined INCR type burst is the least preferred burst on AHB Master I/F<br>- 0x1 (TRUE): Undefined INCR type burst is the most preferred burst on AHB Master I/F |
| 1 | BURST_INCR4_EN | RW | R | 0 | INCR4 Burst<br>Controls generation of INCR4 transfers on Master interface.<br>Values:<br>- 0x0 (FALSE): AHB INCR4 burst type is not generated on<br>Master I/F<br>- 0x1 (TRUE): AHB INCR4 burst type can be generated on<br>Master I/F |
| 2 | BURST_INCR8_EN | RW | R | 0 | INCR8 Burst<br>Controls generation of INCR8 transfers on Master interface.<br>Values:<br>- 0x0 (FALSE): AHB INCR8 burst type is not generated on<br>Master I/F<br>- 0x1 (TRUE): AHB INCR8 burst type can be generated on<br>Master I/F |
| 3 | BURST_INCR16_EN | RW | R | 0 | INCR16 Burst<br>Controls generation of INCR16 transfers on Master interface.<br>Values:<br>- 0x0 (FALSE): AHB INCR16 burst type is not generated on<br>Master I/F<br>- 0x1 (TRUE): AHB INCR16 burst type can be generated<br>on Master I/F |

### 27.3.2.42 SDHC_CORE_EMMC_CTRL_R

**Description:** eMMC Control register
**Address:** 0x4046152C
**Offset:** 0x52C
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register is used to control the eMMC operation.
**Default:** 0xC

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:4] | | | | EMMC_RST_N_OE [3:3] | EMMC_RST_N [2:2] | DISABLE_DATA_CRC_CHK [1:1] | CARD_IS_EMMC [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | CARD_IS_EMMC | RW | R | 0 | eMMC Card present<br>This bit indicates the type of card connected. An application<br>program this bit based on the card connected to SDHC.<br>Values:<br>- 0x1 (EMMC_CARD): Card connected to SDHC is an eMMC card<br>- 0x0 (NON_EMMC_CARD): Card connected to SDHC is<br>a non-eMMC card |
| 1 | DISABLE_DATA_CRC_CHK | RW | R | 0 | Disable Data CRC Check<br>This bit controls masking of CRC16 error for Card Write in<br>eMMC mode. This is useful in bus testing (CMD19) for an<br>eMMC device. In bus testing, an eMMC card does not send<br>CRC status for a block, which may generate CRC error. This<br>CRC error can be masked using this bit during bus testing.<br>Values:<br>- 0x1 (DISABLE): DATA CRC check is disabled<br>- 0x0 (ENABLE): DATA CRC check is enabled |
| 2 | EMMC_RST_N | RW | R | 1 | EMMC Device Reset signal control.<br>This register field controls the card_emmc_reset_n output of SDHC<br>Values:<br>- 0x1 (RST_DEASSERT): Reset to eMMC device is deasserted<br>- 0x0 (RST_ASSERT): Reset to eMMC device asserted<br>(active low) |
| 3 | EMMC_RST_N_OE | RW | R | 1 | Output Enable (OE) control for EMMC Device Reset signal (card_emmc_reset_n).<br>Values:<br>- 0x1 (ENABLE): OE for card_emmc_reset_n is 1<br>- 0x0 (DISABLE): OE for card_emmc_reset_n is 0 |

### 27.3.2.43 SDHC_CORE_BOOT_CTRL_R

**Description:** eMMC Boot Control register
**Address:** 0x4046152E
**Offset:** 0x52E
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register is used to control the eMMC Boot operation.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALIDATE_ BOOT [7:7] | None [6:1] | | | | | | MAN _BOOT_EN [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | BOOT_TOUT_CNT [15:12] | | | | None [11:9] | | | BOOT_ACK _ENABLE [8:8] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | MAN_BOOT_EN | RW | RW | 0 | Mandatory Boot Enable<br>This bit is used to initiate the mandatory boot operation. The<br>application sets this bit along with VALIDATE_BOOT bit.<br>Writing 0 is ignored. The SDHC clears this bit after the boot transfer is completed or terminated.<br>Values:<br>- 0x1 (MAN_BOOT_EN): Mandatory boot enable<br>- 0x0 (MAN_BOOT_DIS): Mandatory boot disable |
| 7 | VALIDATE_BOOT | W | R | 0 | Validate Mandatory Boot Enable bit<br>This bit is used to validate the MAN_BOOT_EN bit.<br>Values:<br>- 0x1 (TRUE): Validate Mandatory boot enable bit<br>- 0x0 (FALSE): Ignore Mandatory boot Enable bit |
| 8 | BOOT_ACK_ENABLE | RW | R | 0 | Boot Acknowledge Enable<br>When this bit set, SDHC checks for boot acknowledge start pattern of 0-1-0 during boot operation. This bit is applicable for both mandatory and alternate boot mode.<br>Values:<br>- 0x1 (TRUE): Boot Ack enable<br>- 0x0 (FALSE): Boot Ack disable |
| 12:15 | BOOT_TOUT_CNT | RW | R | 0 | Boot Ack Timeout Counter Value.<br>This value determines the interval by which boot ack timeout<br>(50 ms) is detected when boot ack is expected during boot<br>operation.<br>- 0xF - Reserved<br>- 0xE - TMCLK x 2^27<br>- .. - .....<br>- 0x1 - TMCLK x 2^14<br>- 0x0 - TMCLK x 2^13 |

### 27.3.2.44 SDHC_CORE_GP_IN_R

**Description:** General Purpose Input register
**Address:** 0x40461530
**Offset:** 0x530
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register is used as a general purpose input register. This register stores all the inputs sampled from input port gp_in.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:1] | | | | | | | GP_IN [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | GP_IN | R | RW | 0 | It reflects the value of gp_in ports.<br>NOT USED - ALWAYS READS 0 |

### 27.3.2.45 SDHC_CORE_GP_OUT_R

**Description:** General Purpose Output register
**Address:** 0x40461534
**Offset:** 0x534
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register is used as a general purpose output register. The contents of this register are reflected on the output port gp_out.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | CARD_CLOCK_OUT_DLY [7:6] | | IO_VOLT_SEL_OE [5:5] | CARD_IF_PWR_EN_OE [4:4] | CARD_CLOCK_OE [3:3] | LED_CTRL_OE [2:2] | CARD_MECH_WRITE_PROT_EN [1:1] | CARD_DETECT_EN [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:10] | | | | | | CARD_CLOCK_IN_DLY [9:8] | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | CARD_DETECT_EN | RW | R | 0 | 0: Force card_detect_n input to 0<br>1: Normal card_detect_n operation allowing card detection from a device pin |
| 1 | CARD_MECH_WRITE_PROT_EN | RW | R | 0 | card_mech_write_prot, despite its name, is an active low signal (per the SD Host Controller Standard spec it is officially called SDWP#). Consider that in the following:<br>0: Force card_mech_write_prot input to 0 internally; this forces write protection to be active<br>1: Allow card_mech_write_prot to work normally per the device's pin state |
| 2 | LED_CTRL_OE | RW | R | 0 | Active high output enable for the LED output signal (led_ctrl) controlled through HOST_CTRL1_R.LED_CTRL:<br>0: disable OE associated with the led_ctrl output<br>1: enable OE associated with the led_ctrl output |
| 3 | CARD_CLOCK_OE | RW | R | 0 | Active high output enable for the card clock output (clk_card) which is gated by CLK_CTRL_R.SD_CLK_EN:<br>0: disable OE to the clk_card output<br>1: enable OE to the clk_card output |
| 4 | CARD_IF_PWR_EN_OE | RW | R | 0 | Active high output enable for the card interface power enable output (card_if_pwr_en) controlled through PWR_CTRL_R.SD_BUS_PWR_VDD1:<br>0: disable OE to the card_if_pwr_en output<br>1: enable OE to the card_if_pwr_en output |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 5 | IO_VOLT_SEL_OE | RW | R | 0 | Active high output enable for the IO voltage selection signal (io_volt_sel) controlled through HOST_CTRL_2.SIGNALING_EN:<br>0: disable OE to the io_volt_sel output<br>1: enable OE to the io_volt_sel output |
| 6:7 | CARD_CLOCK_OUT _DLY | RW | R | 0 | Delay CARD_CLOCK output relative to CMD/DAT to meet output setup/hold times; set according to interface mode:<br>00: SD Default Speed, SD High Speed, SD SDR12, eMMC Legacy<br>01: SD SDR25, SD SDR50, eMMC High Speed SDR<br>10: RESERVED<br>11: SD DDR50, eMMC DDR |
| 8:9 | CARD_CLOCK_IN_DLY | RW | R | 0 | Delay CARD_CLOCK input internally to optimally sample CMD/DAT; set according to interface mode:<br>00: SD Default Speed, SD SDR12, eMMC Legacy<br>01: SD SDR25, SD SDR50<br>10: SD High Speed, eMMC High Speed SDR<br>11: SD DDR50, eMMC DDR |

# 28 SFLASH

**Description** FLASH Supervisory Region
**Base Address** 0x17000000
**Size** 0x8000
**Slave Num** MEMORYMAP

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SFLASH_SI_REVISION_ID | 0x17000001 | FULL | Indicates Silicon Revision ID of the device |
| SFLASH_SILICON_ID | 0x17000002 | FULL | Indicates Silicon ID of the device |
| SFLASH_SFLASH_SVN | 0x170000A8 | FULL | SFLASH Subversion |
| SFLASH_FB_FLAGS | 0x170001FC | FULL | Flash boot flags |
| SFLASH_EPASS_TEMP_TRIM_TEMP_ROOMSORT | 0x1700064E | FULL | On Chip temperature measured using external currents and external ADC at ROOM |
| SFLASH_EPASS_TEMP_TRIM_DIODE_ROOMSORT | 0x17000650 | FULL | Temperature sensor calibration data for VDDA=3.3V, Temperature sensor diode voltage at ROOM |
| SFLASH_EPASS_TEMP_TRIM_VBG_ROOMSORT | 0x17000652 | FULL | Temperature sensor calibration data for VDDA=3.3V, Bandgap voltage at ROOM |
| SFLASH_EPASS_TEMP_TRIM_TEMP_COLDSORT | 0x17000654 | FULL | On Chip temperature measured using external currents and external ADC at COLD |
| SFLASH_EPASS_TEMP_TRIM_DIODE_COLDSORT | 0x17000656 | FULL | Temperature sensor calibration data for VDDA=3.3V, Temperature sensor diode voltage at COLD |
| SFLASH_EPASS_TEMP_TRIM_VBG_COLDSORT | 0x17000658 | FULL | Temperature sensor calibration data for VDDA=3.3V, Bandgap voltage at COLD |
| SFLASH_EPASS_TEMP_TRIM_TEMP_HOTCLASS | 0x1700065A | FULL | On Chip temperature measured using external currents and external ADC at HOT |
| SFLASH_EPASS_TEMP_TRIM_DIODE_HOTCLASS | 0x1700065C | FULL | Temperature sensor calibration data for VDDA=3.3V, Temperature sensor diode voltage at HOT |
| SFLASH_EPASS_TEMP_TRIM_VBG_HOTCLASS | 0x1700065E | FULL | Temperature sensor calibration data for VDDA=3.3V, Bandgap voltage at HOT |
| SFLASH_EPASS_TEMP_TRIM_DIODE_ROOMSORT_5V | 0x1700066A | FULL | Temperature sensor calibration data for VDDA=5V, Temperature sensor diode voltage at ROOM |
| SFLASH_EPASS_TEMP_TRIM_VBG_ROOMSORT_5V | 0x1700066C | FULL | Temperature sensor calibration data for VDDA=5V, Bandgap voltage at ROOM |
| SFLASH_EPASS_TEMP_TRIM_DIODE_COLDSORT_5V | 0x1700066E | FULL | Temperature sensor calibration data for VDDA=5V, Temperature sensor diode voltage at COLD |
| SFLASH_EPASS_TEMP_TRIM_VBG_COLDSORT_5V | 0x17000670 | FULL | Temperature sensor calibration data for VDDA=5V, Bandgap voltage at COLD |
| SFLASH_EPASS_TEMP_TRIM_DIODE_HOTCLASS_5V | 0x17000672 | FULL | Temperature sensor calibration data for VDDA=5V, Temperature sensor diode voltage at HOT |
| SFLASH_EPASS_TEMP_TRIM_VBG_HOTCLASS_5V | 0x17000674 | FULL | Temperature sensor calibration data for VDDA=5V, Bandgap voltage at HOT |
| SFLASH_SRSS_PWR_OFFSET | 0x17000730 | FULL | SRSS_PWR_OFFSET |
| SFLASH_SRSS_PWR_TRIM_HT_PWRSYS_INTERNAL | 0x17000734 | FULL | Trim settings when the supply is intended to come from the internal regulators |
| SFLASH_SRSS_PWR_TRIM_HT_PWRSYS_EXTERNAL | 0x17000738 | FULL | Trim settings for the regulators so they do not interfere with external supply |
| SFLASH_USER_FREE_ROW00 | 0x17000800 | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW01 | 0x17000804 | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW02 | 0x17000808 | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW03 | 0x1700080C | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW04 | 0x17000810 | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW05 | 0x17000814 | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW06 | 0x17000818 | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW07 | 0x1700081C | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW08 | 0x17000820 | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW09 | 0x17000824 | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW010 | 0x17000828 | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW011 | 0x1700082C | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW012 | 0x17000830 | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW013 | 0x17000834 | FULL | USER_FREE_ROW0 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SFLASH_USER_FREE_ROW014 | 0x17000838 | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW015 | 0x1700083C | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW016 | 0x17000840 | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW017 | 0x17000844 | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW018 | 0x17000848 | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW019 | 0x1700084C | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW020 | 0x17000850 | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW021 | 0x17000854 | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW022 | 0x17000858 | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW023 | 0x1700085C | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW024 | 0x17000860 | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW025 | 0x17000864 | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW026 | 0x17000868 | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW027 | 0x1700086C | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW028 | 0x17000870 | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW029 | 0x17000874 | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW030 | 0x17000878 | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW031 | 0x1700087C | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW032 | 0x17000880 | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW033 | 0x17000884 | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW034 | 0x17000888 | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW035 | 0x1700088C | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW036 | 0x17000890 | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW037 | 0x17000894 | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW038 | 0x17000898 | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW039 | 0x1700089C | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW040 | 0x170008A0 | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW041 | 0x170008A4 | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW042 | 0x170008A8 | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW043 | 0x170008AC | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW044 | 0x170008B0 | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW045 | 0x170008B4 | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW046 | 0x170008B8 | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW047 | 0x170008BC | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW048 | 0x170008C0 | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW049 | 0x170008C4 | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW050 | 0x170008C8 | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW051 | 0x170008CC | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW052 | 0x170008D0 | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW053 | 0x170008D4 | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW054 | 0x170008D8 | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW055 | 0x170008DC | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW056 | 0x170008E0 | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW057 | 0x170008E4 | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW058 | 0x170008E8 | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW059 | 0x170008EC | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW060 | 0x170008F0 | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW061 | 0x170008F4 | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW062 | 0x170008F8 | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW063 | 0x170008FC | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW064 | 0x17000900 | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW065 | 0x17000904 | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW066 | 0x17000908 | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW067 | 0x1700090C | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW068 | 0x17000910 | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW069 | 0x17000914 | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW070 | 0x17000918 | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW071 | 0x1700091C | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW072 | 0x17000920 | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW073 | 0x17000924 | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW074 | 0x17000928 | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW075 | 0x1700092C | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW076 | 0x17000930 | FULL | USER_FREE_ROW0 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SFLASH_USER_FREE_ROW077 | 0x17000934 | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW078 | 0x17000938 | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW079 | 0x1700093C | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW080 | 0x17000940 | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW081 | 0x17000944 | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW082 | 0x17000948 | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW083 | 0x1700094C | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW084 | 0x17000950 | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW085 | 0x17000954 | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW086 | 0x17000958 | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW087 | 0x1700095C | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW088 | 0x17000960 | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW089 | 0x17000964 | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW090 | 0x17000968 | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW091 | 0x1700096C | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW092 | 0x17000970 | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW093 | 0x17000974 | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW094 | 0x17000978 | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW095 | 0x1700097C | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW096 | 0x17000980 | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW097 | 0x17000984 | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW098 | 0x17000988 | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW099 | 0x1700098C | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW0100 | 0x17000990 | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW0101 | 0x17000994 | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW0102 | 0x17000998 | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW0103 | 0x1700099C | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW0104 | 0x170009A0 | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW0105 | 0x170009A4 | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW0106 | 0x170009A8 | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW0107 | 0x170009AC | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW0108 | 0x170009B0 | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW0109 | 0x170009B4 | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW0110 | 0x170009B8 | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW0111 | 0x170009BC | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW0112 | 0x170009C0 | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW0113 | 0x170009C4 | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW0114 | 0x170009C8 | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW0115 | 0x170009CC | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW0116 | 0x170009D0 | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW0117 | 0x170009D4 | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW0118 | 0x170009D8 | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW0119 | 0x170009DC | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW0120 | 0x170009E0 | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW0121 | 0x170009E4 | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW0122 | 0x170009E8 | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW0123 | 0x170009EC | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW0124 | 0x170009F0 | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW0125 | 0x170009F4 | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW0126 | 0x170009F8 | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW0127 | 0x170009FC | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW10 | 0x17000A00 | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW11 | 0x17000A04 | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW12 | 0x17000A08 | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW13 | 0x17000A0C | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW14 | 0x17000A10 | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW15 | 0x17000A14 | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW16 | 0x17000A18 | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW17 | 0x17000A1C | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW18 | 0x17000A20 | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW19 | 0x17000A24 | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW110 | 0x17000A28 | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW111 | 0x17000A2C | FULL | USER_FREE_ROW1 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SFLASH_USER_FREE_ROW112 | 0x17000A30 | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW113 | 0x17000A34 | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW114 | 0x17000A38 | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW115 | 0x17000A3C | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW116 | 0x17000A40 | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW117 | 0x17000A44 | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW118 | 0x17000A48 | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW119 | 0x17000A4C | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW120 | 0x17000A50 | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW121 | 0x17000A54 | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW122 | 0x17000A58 | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW123 | 0x17000A5C | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW124 | 0x17000A60 | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW125 | 0x17000A64 | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW126 | 0x17000A68 | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW127 | 0x17000A6C | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW128 | 0x17000A70 | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW129 | 0x17000A74 | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW130 | 0x17000A78 | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW131 | 0x17000A7C | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW132 | 0x17000A80 | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW133 | 0x17000A84 | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW134 | 0x17000A88 | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW135 | 0x17000A8C | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW136 | 0x17000A90 | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW137 | 0x17000A94 | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW138 | 0x17000A98 | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW139 | 0x17000A9C | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW140 | 0x17000AA0 | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW141 | 0x17000AA4 | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW142 | 0x17000AA8 | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW143 | 0x17000AAC | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW144 | 0x17000AB0 | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW145 | 0x17000AB4 | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW146 | 0x17000AB8 | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW147 | 0x17000ABC | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW148 | 0x17000AC0 | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW149 | 0x17000AC4 | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW150 | 0x17000AC8 | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW151 | 0x17000ACC | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW152 | 0x17000AD0 | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW153 | 0x17000AD4 | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW154 | 0x17000AD8 | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW155 | 0x17000ADC | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW156 | 0x17000AE0 | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW157 | 0x17000AE4 | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW158 | 0x17000AE8 | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW159 | 0x17000AEC | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW160 | 0x17000AF0 | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW161 | 0x17000AF4 | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW162 | 0x17000AF8 | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW163 | 0x17000AFC | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW164 | 0x17000B00 | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW165 | 0x17000B04 | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW166 | 0x17000B08 | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW167 | 0x17000B0C | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW168 | 0x17000B10 | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW169 | 0x17000B14 | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW170 | 0x17000B18 | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW171 | 0x17000B1C | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW172 | 0x17000B20 | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW173 | 0x17000B24 | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW174 | 0x17000B28 | FULL | USER_FREE_ROW1 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SFLASH_USER_FREE_ROW175 | 0x17000B2C | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW176 | 0x17000B30 | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW177 | 0x17000B34 | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW178 | 0x17000B38 | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW179 | 0x17000B3C | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW180 | 0x17000B40 | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW181 | 0x17000B44 | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW182 | 0x17000B48 | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW183 | 0x17000B4C | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW184 | 0x17000B50 | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW185 | 0x17000B54 | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW186 | 0x17000B58 | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW187 | 0x17000B5C | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW188 | 0x17000B60 | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW189 | 0x17000B64 | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW190 | 0x17000B68 | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW191 | 0x17000B6C | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW192 | 0x17000B70 | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW193 | 0x17000B74 | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW194 | 0x17000B78 | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW195 | 0x17000B7C | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW196 | 0x17000B80 | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW197 | 0x17000B84 | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW198 | 0x17000B88 | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW199 | 0x17000B8C | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW1100 | 0x17000B90 | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW1101 | 0x17000B94 | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW1102 | 0x17000B98 | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW1103 | 0x17000B9C | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW1104 | 0x17000BA0 | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW1105 | 0x17000BA4 | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW1106 | 0x17000BA8 | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW1107 | 0x17000BAC | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW1108 | 0x17000BB0 | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW1109 | 0x17000BB4 | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW1110 | 0x17000BB8 | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW1111 | 0x17000BBC | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW1112 | 0x17000BC0 | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW1113 | 0x17000BC4 | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW1114 | 0x17000BC8 | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW1115 | 0x17000BCC | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW1116 | 0x17000BD0 | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW1117 | 0x17000BD4 | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW1118 | 0x17000BD8 | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW1119 | 0x17000BDC | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW1120 | 0x17000BE0 | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW1121 | 0x17000BE4 | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW1122 | 0x17000BE8 | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW1123 | 0x17000BEC | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW1124 | 0x17000BF0 | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW1125 | 0x17000BF4 | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW1126 | 0x17000BF8 | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW1127 | 0x17000BFC | FULL | USER_FREE_ROW1 |
| SFLASH_USER_FREE_ROW20 | 0x17000C00 | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW21 | 0x17000C04 | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW22 | 0x17000C08 | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW23 | 0x17000C0C | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW24 | 0x17000C10 | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW25 | 0x17000C14 | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW26 | 0x17000C18 | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW27 | 0x17000C1C | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW28 | 0x17000C20 | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW29 | 0x17000C24 | FULL | USER_FREE_ROW2 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SFLASH_USER_FREE_ROW210 | 0x17000C28 | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW211 | 0x17000C2C | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW212 | 0x17000C30 | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW213 | 0x17000C34 | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW214 | 0x17000C38 | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW215 | 0x17000C3C | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW216 | 0x17000C40 | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW217 | 0x17000C44 | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW218 | 0x17000C48 | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW219 | 0x17000C4C | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW220 | 0x17000C50 | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW221 | 0x17000C54 | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW222 | 0x17000C58 | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW223 | 0x17000C5C | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW224 | 0x17000C60 | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW225 | 0x17000C64 | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW226 | 0x17000C68 | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW227 | 0x17000C6C | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW228 | 0x17000C70 | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW229 | 0x17000C74 | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW230 | 0x17000C78 | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW231 | 0x17000C7C | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW232 | 0x17000C80 | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW233 | 0x17000C84 | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW234 | 0x17000C88 | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW235 | 0x17000C8C | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW236 | 0x17000C90 | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW237 | 0x17000C94 | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW238 | 0x17000C98 | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW239 | 0x17000C9C | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW240 | 0x17000CA0 | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW241 | 0x17000CA4 | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW242 | 0x17000CA8 | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW243 | 0x17000CAC | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW244 | 0x17000CB0 | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW245 | 0x17000CB4 | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW246 | 0x17000CB8 | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW247 | 0x17000CBC | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW248 | 0x17000CC0 | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW249 | 0x17000CC4 | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW250 | 0x17000CC8 | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW251 | 0x17000CCC | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW252 | 0x17000CD0 | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW253 | 0x17000CD4 | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW254 | 0x17000CD8 | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW255 | 0x17000CDC | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW256 | 0x17000CE0 | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW257 | 0x17000CE4 | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW258 | 0x17000CE8 | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW259 | 0x17000CEC | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW260 | 0x17000CF0 | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW261 | 0x17000CF4 | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW262 | 0x17000CF8 | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW263 | 0x17000CFC | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW264 | 0x17000D00 | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW265 | 0x17000D04 | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW266 | 0x17000D08 | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW267 | 0x17000D0C | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW268 | 0x17000D10 | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW269 | 0x17000D14 | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW270 | 0x17000D18 | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW271 | 0x17000D1C | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW272 | 0x17000D20 | FULL | USER_FREE_ROW2 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SFLASH_USER_FREE_ROW273 | 0x17000D24 | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW274 | 0x17000D28 | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW275 | 0x17000D2C | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW276 | 0x17000D30 | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW277 | 0x17000D34 | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW278 | 0x17000D38 | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW279 | 0x17000D3C | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW280 | 0x17000D40 | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW281 | 0x17000D44 | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW282 | 0x17000D48 | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW283 | 0x17000D4C | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW284 | 0x17000D50 | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW285 | 0x17000D54 | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW286 | 0x17000D58 | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW287 | 0x17000D5C | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW288 | 0x17000D60 | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW289 | 0x17000D64 | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW290 | 0x17000D68 | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW291 | 0x17000D6C | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW292 | 0x17000D70 | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW293 | 0x17000D74 | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW294 | 0x17000D78 | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW295 | 0x17000D7C | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW296 | 0x17000D80 | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW297 | 0x17000D84 | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW298 | 0x17000D88 | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW299 | 0x17000D8C | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW2100 | 0x17000D90 | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW2101 | 0x17000D94 | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW2102 | 0x17000D98 | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW2103 | 0x17000D9C | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW2104 | 0x17000DA0 | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW2105 | 0x17000DA4 | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW2106 | 0x17000DA8 | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW2107 | 0x17000DAC | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW2108 | 0x17000DB0 | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW2109 | 0x17000DB4 | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW2110 | 0x17000DB8 | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW2111 | 0x17000DBC | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW2112 | 0x17000DC0 | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW2113 | 0x17000DC4 | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW2114 | 0x17000DC8 | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW2115 | 0x17000DCC | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW2116 | 0x17000DD0 | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW2117 | 0x17000DD4 | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW2118 | 0x17000DD8 | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW2119 | 0x17000DDC | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW2120 | 0x17000DE0 | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW2121 | 0x17000DE4 | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW2122 | 0x17000DE8 | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW2123 | 0x17000DEC | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW2124 | 0x17000DF0 | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW2125 | 0x17000DF4 | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW2126 | 0x17000DF8 | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW2127 | 0x17000DFC | FULL | USER_FREE_ROW2 |
| SFLASH_USER_FREE_ROW30 | 0x17000E00 | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW31 | 0x17000E04 | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW32 | 0x17000E08 | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW33 | 0x17000E0C | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW34 | 0x17000E10 | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW35 | 0x17000E14 | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW36 | 0x17000E18 | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW37 | 0x17000E1C | FULL | USER_FREE_ROW3 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SFLASH_USER_FREE_ROW38 | 0x17000E20 | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW39 | 0x17000E24 | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW310 | 0x17000E28 | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW311 | 0x17000E2C | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW312 | 0x17000E30 | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW313 | 0x17000E34 | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW314 | 0x17000E38 | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW315 | 0x17000E3C | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW316 | 0x17000E40 | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW317 | 0x17000E44 | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW318 | 0x17000E48 | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW319 | 0x17000E4C | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW320 | 0x17000E50 | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW321 | 0x17000E54 | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW322 | 0x17000E58 | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW323 | 0x17000E5C | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW324 | 0x17000E60 | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW325 | 0x17000E64 | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW326 | 0x17000E68 | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW327 | 0x17000E6C | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW328 | 0x17000E70 | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW329 | 0x17000E74 | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW330 | 0x17000E78 | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW331 | 0x17000E7C | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW332 | 0x17000E80 | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW333 | 0x17000E84 | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW334 | 0x17000E88 | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW335 | 0x17000E8C | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW336 | 0x17000E90 | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW337 | 0x17000E94 | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW338 | 0x17000E98 | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW339 | 0x17000E9C | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW340 | 0x17000EA0 | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW341 | 0x17000EA4 | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW342 | 0x17000EA8 | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW343 | 0x17000EAC | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW344 | 0x17000EB0 | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW345 | 0x17000EB4 | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW346 | 0x17000EB8 | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW347 | 0x17000EBC | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW348 | 0x17000EC0 | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW349 | 0x17000EC4 | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW350 | 0x17000EC8 | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW351 | 0x17000ECC | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW352 | 0x17000ED0 | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW353 | 0x17000ED4 | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW354 | 0x17000ED8 | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW355 | 0x17000EDC | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW356 | 0x17000EE0 | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW357 | 0x17000EE4 | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW358 | 0x17000EE8 | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW359 | 0x17000EEC | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW360 | 0x17000EF0 | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW361 | 0x17000EF4 | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW362 | 0x17000EF8 | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW363 | 0x17000EFC | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW364 | 0x17000F00 | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW365 | 0x17000F04 | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW366 | 0x17000F08 | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW367 | 0x17000F0C | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW368 | 0x17000F10 | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW369 | 0x17000F14 | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW370 | 0x17000F18 | FULL | USER_FREE_ROW3 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SFLASH_USER_FREE_ROW371 | 0x17000F1C | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW372 | 0x17000F20 | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW373 | 0x17000F24 | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW374 | 0x17000F28 | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW375 | 0x17000F2C | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW376 | 0x17000F30 | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW377 | 0x17000F34 | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW378 | 0x17000F38 | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW379 | 0x17000F3C | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW380 | 0x17000F40 | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW381 | 0x17000F44 | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW382 | 0x17000F48 | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW383 | 0x17000F4C | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW384 | 0x17000F50 | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW385 | 0x17000F54 | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW386 | 0x17000F58 | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW387 | 0x17000F5C | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW388 | 0x17000F60 | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW389 | 0x17000F64 | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW390 | 0x17000F68 | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW391 | 0x17000F6C | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW392 | 0x17000F70 | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW393 | 0x17000F74 | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW394 | 0x17000F78 | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW395 | 0x17000F7C | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW396 | 0x17000F80 | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW397 | 0x17000F84 | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW398 | 0x17000F88 | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW399 | 0x17000F8C | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW3100 | 0x17000F90 | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW3101 | 0x17000F94 | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW3102 | 0x17000F98 | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW3103 | 0x17000F9C | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW3104 | 0x17000FA0 | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW3105 | 0x17000FA4 | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW3106 | 0x17000FA8 | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW3107 | 0x17000FAC | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW3108 | 0x17000FB0 | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW3109 | 0x17000FB4 | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW3110 | 0x17000FB8 | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW3111 | 0x17000FBC | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW3112 | 0x17000FC0 | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW3113 | 0x17000FC4 | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW3114 | 0x17000FC8 | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW3115 | 0x17000FCC | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW3116 | 0x17000FD0 | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW3117 | 0x17000FD4 | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW3118 | 0x17000FD8 | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW3119 | 0x17000FDC | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW3120 | 0x17000FE0 | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW3121 | 0x17000FE4 | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW3122 | 0x17000FE8 | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW3123 | 0x17000FEC | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW3124 | 0x17000FF0 | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW3125 | 0x17000FF4 | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW3126 | 0x17000FF8 | FULL | USER_FREE_ROW3 |
| SFLASH_USER_FREE_ROW3127 | 0x17000FFC | FULL | USER_FREE_ROW3 |
| SFLASH_SFLASH_UPDATE_MARKER0 | 0x17001800 | FULL | Markers for storing SFLASH programming states |
| SFLASH_SFLASH_UPDATE_MARKER1 | 0x17001804 | FULL | Markers for storing SFLASH programming states |
| SFLASH_NORMAL_ACCESS_RESTRICTIONS | 0x17001A00 | FULL | Indicates access restrictions to be applied on DAP in NORMAL state |
| SFLASH_NORMAL_DEAD_ACCESS_RESTRICTIONS | 0x17001A04 | FULL | Indicates access restrictions to be applied on DAP in NORMAL DEAD state |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SFLASH_FLASH_BOOT_OBJECT_SIZE | 0x17002000 | FULL | Flash Boot - Object Size |
| SFLASH_FLASH_BOOT_APP_ID | 0x17002004 | FULL | Flash Boot - Application ID/Version |
| SFLASH_FLASH_BOOT_BUILD_NUMBER | 0x17002018 | FULL | This field contains the Flashboot internal build number. |
| SFLASH_FLASH_BOOT_FAMILY_ID | 0x1700201C | FULL | Flash Boot - Family ID |
| SFLASH_PUBLIC_KEY0 | 0x17006400 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1 | 0x17006401 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2 | 0x17006402 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3 | 0x17006403 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY4 | 0x17006404 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY5 | 0x17006405 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY6 | 0x17006406 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY7 | 0x17006407 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY8 | 0x17006408 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY9 | 0x17006409 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY10 | 0x1700640A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY11 | 0x1700640B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY12 | 0x1700640C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY13 | 0x1700640D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY14 | 0x1700640E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY15 | 0x1700640F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY16 | 0x17006410 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY17 | 0x17006411 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY18 | 0x17006412 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY19 | 0x17006413 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY20 | 0x17006414 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY21 | 0x17006415 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY22 | 0x17006416 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY23 | 0x17006417 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY24 | 0x17006418 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY25 | 0x17006419 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY26 | 0x1700641A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY27 | 0x1700641B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY28 | 0x1700641C | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SFLASH_PUBLIC_KEY29 | 0x1700641D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY30 | 0x1700641E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY31 | 0x1700641F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY32 | 0x17006420 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY33 | 0x17006421 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY34 | 0x17006422 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY35 | 0x17006423 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY36 | 0x17006424 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY37 | 0x17006425 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY38 | 0x17006426 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY39 | 0x17006427 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY40 | 0x17006428 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY41 | 0x17006429 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY42 | 0x1700642A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY43 | 0x1700642B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY44 | 0x1700642C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY45 | 0x1700642D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY46 | 0x1700642E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY47 | 0x1700642F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY48 | 0x17006430 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY49 | 0x17006431 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY50 | 0x17006432 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY51 | 0x17006433 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY52 | 0x17006434 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY53 | 0x17006435 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY54 | 0x17006436 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY55 | 0x17006437 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY56 | 0x17006438 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY57 | 0x17006439 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY58 | 0x1700643A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY59 | 0x1700643B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY60 | 0x1700643C | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SFLASH_PUBLIC_KEY61 | 0x1700643D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY62 | 0x1700643E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY63 | 0x1700643F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY64 | 0x17006440 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY65 | 0x17006441 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY66 | 0x17006442 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY67 | 0x17006443 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY68 | 0x17006444 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY69 | 0x17006445 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY70 | 0x17006446 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY71 | 0x17006447 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY72 | 0x17006448 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY73 | 0x17006449 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY74 | 0x1700644A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY75 | 0x1700644B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY76 | 0x1700644C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY77 | 0x1700644D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY78 | 0x1700644E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY79 | 0x1700644F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY80 | 0x17006450 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY81 | 0x17006451 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY82 | 0x17006452 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY83 | 0x17006453 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY84 | 0x17006454 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY85 | 0x17006455 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY86 | 0x17006456 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY87 | 0x17006457 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY88 | 0x17006458 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY89 | 0x17006459 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY90 | 0x1700645A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY91 | 0x1700645B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY92 | 0x1700645C | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SFLASH_PUBLIC_KEY93 | 0x1700645D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY94 | 0x1700645E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY95 | 0x1700645F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY96 | 0x17006460 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY97 | 0x17006461 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY98 | 0x17006462 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY99 | 0x17006463 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY100 | 0x17006464 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY101 | 0x17006465 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY102 | 0x17006466 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY103 | 0x17006467 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY104 | 0x17006468 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY105 | 0x17006469 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY106 | 0x1700646A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY107 | 0x1700646B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY108 | 0x1700646C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY109 | 0x1700646D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY110 | 0x1700646E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY111 | 0x1700646F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY112 | 0x17006470 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY113 | 0x17006471 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY114 | 0x17006472 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY115 | 0x17006473 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY116 | 0x17006474 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY117 | 0x17006475 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY118 | 0x17006476 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY119 | 0x17006477 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY120 | 0x17006478 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY121 | 0x17006479 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY122 | 0x1700647A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY123 | 0x1700647B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY124 | 0x1700647C | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SFLASH_PUBLIC_KEY125 | 0x1700647D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY126 | 0x1700647E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY127 | 0x1700647F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY128 | 0x17006480 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY129 | 0x17006481 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY130 | 0x17006482 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY131 | 0x17006483 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY132 | 0x17006484 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY133 | 0x17006485 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY134 | 0x17006486 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY135 | 0x17006487 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY136 | 0x17006488 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY137 | 0x17006489 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY138 | 0x1700648A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY139 | 0x1700648B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY140 | 0x1700648C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY141 | 0x1700648D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY142 | 0x1700648E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY143 | 0x1700648F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY144 | 0x17006490 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY145 | 0x17006491 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY146 | 0x17006492 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY147 | 0x17006493 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY148 | 0x17006494 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY149 | 0x17006495 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY150 | 0x17006496 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY151 | 0x17006497 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY152 | 0x17006498 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY153 | 0x17006499 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY154 | 0x1700649A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY155 | 0x1700649B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY156 | 0x1700649C | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SFLASH_PUBLIC_KEY157 | 0x1700649D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY158 | 0x1700649E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY159 | 0x1700649F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY160 | 0x170064A0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY161 | 0x170064A1 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY162 | 0x170064A2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY163 | 0x170064A3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY164 | 0x170064A4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY165 | 0x170064A5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY166 | 0x170064A6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY167 | 0x170064A7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY168 | 0x170064A8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY169 | 0x170064A9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY170 | 0x170064AA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY171 | 0x170064AB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY172 | 0x170064AC | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY173 | 0x170064AD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY174 | 0x170064AE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY175 | 0x170064AF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY176 | 0x170064B0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY177 | 0x170064B1 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY178 | 0x170064B2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY179 | 0x170064B3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY180 | 0x170064B4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY181 | 0x170064B5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY182 | 0x170064B6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY183 | 0x170064B7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY184 | 0x170064B8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY185 | 0x170064B9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY186 | 0x170064BA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY187 | 0x170064BB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY188 | 0x170064BC | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SFLASH_PUBLIC_KEY189 | 0x170064BD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY190 | 0x170064BE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY191 | 0x170064BF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY192 | 0x170064C0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY193 | 0x170064C1 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY194 | 0x170064C2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY195 | 0x170064C3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY196 | 0x170064C4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY197 | 0x170064C5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY198 | 0x170064C6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY199 | 0x170064C7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY200 | 0x170064C8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY201 | 0x170064C9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY202 | 0x170064CA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY203 | 0x170064CB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY204 | 0x170064CC | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY205 | 0x170064CD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY206 | 0x170064CE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY207 | 0x170064CF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY208 | 0x170064D0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY209 | 0x170064D1 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY210 | 0x170064D2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY211 | 0x170064D3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY212 | 0x170064D4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY213 | 0x170064D5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY214 | 0x170064D6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY215 | 0x170064D7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY216 | 0x170064D8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY217 | 0x170064D9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY218 | 0x170064DA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY219 | 0x170064DB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY220 | 0x170064DC | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SFLASH_PUBLIC_KEY221 | 0x170064DD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY222 | 0x170064DE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY223 | 0x170064DF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY224 | 0x170064E0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY225 | 0x170064E1 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY226 | 0x170064E2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY227 | 0x170064E3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY228 | 0x170064E4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY229 | 0x170064E5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY230 | 0x170064E6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY231 | 0x170064E7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY232 | 0x170064E8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY233 | 0x170064E9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY234 | 0x170064EA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY235 | 0x170064EB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY236 | 0x170064EC | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY237 | 0x170064ED | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY238 | 0x170064EE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY239 | 0x170064EF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY240 | 0x170064F0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY241 | 0x170064F1 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY242 | 0x170064F2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY243 | 0x170064F3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY244 | 0x170064F4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY245 | 0x170064F5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY246 | 0x170064F6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY247 | 0x170064F7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY248 | 0x170064F8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY249 | 0x170064F9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY250 | 0x170064FA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY251 | 0x170064FB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY252 | 0x170064FC | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SFLASH_PUBLIC_KEY253 | 0x170064FD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY254 | 0x170064FE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY255 | 0x170064FF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY256 | 0x17006500 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY257 | 0x17006501 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY258 | 0x17006502 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY259 | 0x17006503 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY260 | 0x17006504 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY261 | 0x17006505 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY262 | 0x17006506 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY263 | 0x17006507 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY264 | 0x17006508 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY265 | 0x17006509 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY266 | 0x1700650A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY267 | 0x1700650B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY268 | 0x1700650C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY269 | 0x1700650D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY270 | 0x1700650E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY271 | 0x1700650F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY272 | 0x17006510 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY273 | 0x17006511 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY274 | 0x17006512 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY275 | 0x17006513 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY276 | 0x17006514 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY277 | 0x17006515 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY278 | 0x17006516 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY279 | 0x17006517 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY280 | 0x17006518 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY281 | 0x17006519 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY282 | 0x1700651A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY283 | 0x1700651B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY284 | 0x1700651C | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SFLASH_PUBLIC_KEY285 | 0x1700651D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY286 | 0x1700651E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY287 | 0x1700651F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY288 | 0x17006520 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY289 | 0x17006521 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY290 | 0x17006522 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY291 | 0x17006523 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY292 | 0x17006524 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY293 | 0x17006525 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY294 | 0x17006526 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY295 | 0x17006527 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY296 | 0x17006528 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY297 | 0x17006529 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY298 | 0x1700652A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY299 | 0x1700652B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY300 | 0x1700652C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY301 | 0x1700652D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY302 | 0x1700652E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY303 | 0x1700652F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY304 | 0x17006530 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY305 | 0x17006531 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY306 | 0x17006532 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY307 | 0x17006533 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY308 | 0x17006534 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY309 | 0x17006535 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY310 | 0x17006536 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY311 | 0x17006537 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY312 | 0x17006538 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY313 | 0x17006539 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY314 | 0x1700653A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY315 | 0x1700653B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY316 | 0x1700653C | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SFLASH_PUBLIC_KEY317 | 0x1700653D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY318 | 0x1700653E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY319 | 0x1700653F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY320 | 0x17006540 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY321 | 0x17006541 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY322 | 0x17006542 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY323 | 0x17006543 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY324 | 0x17006544 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY325 | 0x17006545 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY326 | 0x17006546 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY327 | 0x17006547 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY328 | 0x17006548 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY329 | 0x17006549 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY330 | 0x1700654A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY331 | 0x1700654B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY332 | 0x1700654C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY333 | 0x1700654D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY334 | 0x1700654E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY335 | 0x1700654F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY336 | 0x17006550 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY337 | 0x17006551 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY338 | 0x17006552 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY339 | 0x17006553 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY340 | 0x17006554 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY341 | 0x17006555 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY342 | 0x17006556 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY343 | 0x17006557 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY344 | 0x17006558 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY345 | 0x17006559 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY346 | 0x1700655A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY347 | 0x1700655B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY348 | 0x1700655C | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SFLASH_PUBLIC_KEY349 | 0x1700655D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY350 | 0x1700655E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY351 | 0x1700655F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY352 | 0x17006560 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY353 | 0x17006561 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY354 | 0x17006562 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY355 | 0x17006563 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY356 | 0x17006564 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY357 | 0x17006565 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY358 | 0x17006566 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY359 | 0x17006567 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY360 | 0x17006568 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY361 | 0x17006569 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY362 | 0x1700656A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY363 | 0x1700656B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY364 | 0x1700656C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY365 | 0x1700656D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY366 | 0x1700656E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY367 | 0x1700656F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY368 | 0x17006570 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY369 | 0x17006571 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY370 | 0x17006572 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY371 | 0x17006573 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY372 | 0x17006574 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY373 | 0x17006575 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY374 | 0x17006576 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY375 | 0x17006577 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY376 | 0x17006578 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY377 | 0x17006579 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY378 | 0x1700657A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY379 | 0x1700657B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY380 | 0x1700657C | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SFLASH_PUBLIC_KEY381 | 0x1700657D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY382 | 0x1700657E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY383 | 0x1700657F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY384 | 0x17006580 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY385 | 0x17006581 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY386 | 0x17006582 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY387 | 0x17006583 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY388 | 0x17006584 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY389 | 0x17006585 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY390 | 0x17006586 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY391 | 0x17006587 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY392 | 0x17006588 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY393 | 0x17006589 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY394 | 0x1700658A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY395 | 0x1700658B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY396 | 0x1700658C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY397 | 0x1700658D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY398 | 0x1700658E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY399 | 0x1700658F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY400 | 0x17006590 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY401 | 0x17006591 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY402 | 0x17006592 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY403 | 0x17006593 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY404 | 0x17006594 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY405 | 0x17006595 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY406 | 0x17006596 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY407 | 0x17006597 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY408 | 0x17006598 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY409 | 0x17006599 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY410 | 0x1700659A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY411 | 0x1700659B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY412 | 0x1700659C | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SFLASH_PUBLIC_KEY413 | 0x1700659D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY414 | 0x1700659E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY415 | 0x1700659F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY416 | 0x170065A0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY417 | 0x170065A1 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY418 | 0x170065A2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY419 | 0x170065A3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY420 | 0x170065A4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY421 | 0x170065A5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY422 | 0x170065A6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY423 | 0x170065A7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY424 | 0x170065A8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY425 | 0x170065A9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY426 | 0x170065AA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY427 | 0x170065AB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY428 | 0x170065AC | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY429 | 0x170065AD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY430 | 0x170065AE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY431 | 0x170065AF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY432 | 0x170065B0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY433 | 0x170065B1 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY434 | 0x170065B2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY435 | 0x170065B3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY436 | 0x170065B4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY437 | 0x170065B5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY438 | 0x170065B6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY439 | 0x170065B7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY440 | 0x170065B8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY441 | 0x170065B9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY442 | 0x170065BA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY443 | 0x170065BB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY444 | 0x170065BC | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SFLASH_PUBLIC_KEY445 | 0x170065BD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY446 | 0x170065BE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY447 | 0x170065BF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY448 | 0x170065C0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY449 | 0x170065C1 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY450 | 0x170065C2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY451 | 0x170065C3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY452 | 0x170065C4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY453 | 0x170065C5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY454 | 0x170065C6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY455 | 0x170065C7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY456 | 0x170065C8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY457 | 0x170065C9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY458 | 0x170065CA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY459 | 0x170065CB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY460 | 0x170065CC | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY461 | 0x170065CD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY462 | 0x170065CE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY463 | 0x170065CF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY464 | 0x170065D0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY465 | 0x170065D1 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY466 | 0x170065D2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY467 | 0x170065D3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY468 | 0x170065D4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY469 | 0x170065D5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY470 | 0x170065D6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY471 | 0x170065D7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY472 | 0x170065D8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY473 | 0x170065D9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY474 | 0x170065DA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY475 | 0x170065DB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY476 | 0x170065DC | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SFLASH_PUBLIC_KEY477 | 0x170065DD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY478 | 0x170065DE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY479 | 0x170065DF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY480 | 0x170065E0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY481 | 0x170065E1 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY482 | 0x170065E2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY483 | 0x170065E3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY484 | 0x170065E4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY485 | 0x170065E5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY486 | 0x170065E6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY487 | 0x170065E7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY488 | 0x170065E8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY489 | 0x170065E9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY490 | 0x170065EA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY491 | 0x170065EB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY492 | 0x170065EC | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY493 | 0x170065ED | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY494 | 0x170065EE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY495 | 0x170065EF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY496 | 0x170065F0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY497 | 0x170065F1 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY498 | 0x170065F2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY499 | 0x170065F3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY500 | 0x170065F4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY501 | 0x170065F5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY502 | 0x170065F6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY503 | 0x170065F7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY504 | 0x170065F8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY505 | 0x170065F9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY506 | 0x170065FA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY507 | 0x170065FB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY508 | 0x170065FC | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SFLASH_PUBLIC_KEY509 | 0x170065FD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY510 | 0x170065FE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY511 | 0x170065FF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY512 | 0x17006600 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY513 | 0x17006601 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY514 | 0x17006602 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY515 | 0x17006603 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY516 | 0x17006604 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY517 | 0x17006605 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY518 | 0x17006606 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY519 | 0x17006607 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY520 | 0x17006608 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY521 | 0x17006609 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY522 | 0x1700660A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY523 | 0x1700660B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY524 | 0x1700660C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY525 | 0x1700660D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY526 | 0x1700660E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY527 | 0x1700660F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY528 | 0x17006610 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY529 | 0x17006611 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY530 | 0x17006612 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY531 | 0x17006613 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY532 | 0x17006614 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY533 | 0x17006615 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY534 | 0x17006616 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY535 | 0x17006617 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY536 | 0x17006618 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY537 | 0x17006619 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY538 | 0x1700661A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY539 | 0x1700661B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY540 | 0x1700661C | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SFLASH_PUBLIC_KEY541 | 0x1700661D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY542 | 0x1700661E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY543 | 0x1700661F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY544 | 0x17006620 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY545 | 0x17006621 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY546 | 0x17006622 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY547 | 0x17006623 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY548 | 0x17006624 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY549 | 0x17006625 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY550 | 0x17006626 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY551 | 0x17006627 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY552 | 0x17006628 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY553 | 0x17006629 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY554 | 0x1700662A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY555 | 0x1700662B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY556 | 0x1700662C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY557 | 0x1700662D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY558 | 0x1700662E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY559 | 0x1700662F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY560 | 0x17006630 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY561 | 0x17006631 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY562 | 0x17006632 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY563 | 0x17006633 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY564 | 0x17006634 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY565 | 0x17006635 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY566 | 0x17006636 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY567 | 0x17006637 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY568 | 0x17006638 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY569 | 0x17006639 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY570 | 0x1700663A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY571 | 0x1700663B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY572 | 0x1700663C | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SFLASH_PUBLIC_KEY573 | 0x1700663D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY574 | 0x1700663E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY575 | 0x1700663F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY576 | 0x17006640 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY577 | 0x17006641 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY578 | 0x17006642 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY579 | 0x17006643 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY580 | 0x17006644 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY581 | 0x17006645 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY582 | 0x17006646 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY583 | 0x17006647 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY584 | 0x17006648 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY585 | 0x17006649 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY586 | 0x1700664A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY587 | 0x1700664B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY588 | 0x1700664C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY589 | 0x1700664D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY590 | 0x1700664E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY591 | 0x1700664F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY592 | 0x17006650 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY593 | 0x17006651 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY594 | 0x17006652 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY595 | 0x17006653 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY596 | 0x17006654 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY597 | 0x17006655 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY598 | 0x17006656 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY599 | 0x17006657 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY600 | 0x17006658 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY601 | 0x17006659 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY602 | 0x1700665A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY603 | 0x1700665B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY604 | 0x1700665C | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SFLASH_PUBLIC_KEY605 | 0x1700665D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY606 | 0x1700665E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY607 | 0x1700665F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY608 | 0x17006660 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY609 | 0x17006661 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY610 | 0x17006662 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY611 | 0x17006663 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY612 | 0x17006664 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY613 | 0x17006665 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY614 | 0x17006666 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY615 | 0x17006667 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY616 | 0x17006668 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY617 | 0x17006669 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY618 | 0x1700666A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY619 | 0x1700666B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY620 | 0x1700666C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY621 | 0x1700666D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY622 | 0x1700666E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY623 | 0x1700666F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY624 | 0x17006670 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY625 | 0x17006671 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY626 | 0x17006672 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY627 | 0x17006673 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY628 | 0x17006674 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY629 | 0x17006675 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY630 | 0x17006676 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY631 | 0x17006677 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY632 | 0x17006678 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY633 | 0x17006679 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY634 | 0x1700667A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY635 | 0x1700667B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY636 | 0x1700667C | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SFLASH_PUBLIC_KEY637 | 0x1700667D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY638 | 0x1700667E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY639 | 0x1700667F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY640 | 0x17006680 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY641 | 0x17006681 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY642 | 0x17006682 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY643 | 0x17006683 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY644 | 0x17006684 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY645 | 0x17006685 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY646 | 0x17006686 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY647 | 0x17006687 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY648 | 0x17006688 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY649 | 0x17006689 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY650 | 0x1700668A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY651 | 0x1700668B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY652 | 0x1700668C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY653 | 0x1700668D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY654 | 0x1700668E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY655 | 0x1700668F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY656 | 0x17006690 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY657 | 0x17006691 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY658 | 0x17006692 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY659 | 0x17006693 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY660 | 0x17006694 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY661 | 0x17006695 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY662 | 0x17006696 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY663 | 0x17006697 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY664 | 0x17006698 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY665 | 0x17006699 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY666 | 0x1700669A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY667 | 0x1700669B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY668 | 0x1700669C | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SFLASH_PUBLIC_KEY669 | 0x1700669D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY670 | 0x1700669E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY671 | 0x1700669F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY672 | 0x170066A0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY673 | 0x170066A1 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY674 | 0x170066A2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY675 | 0x170066A3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY676 | 0x170066A4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY677 | 0x170066A5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY678 | 0x170066A6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY679 | 0x170066A7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY680 | 0x170066A8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY681 | 0x170066A9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY682 | 0x170066AA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY683 | 0x170066AB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY684 | 0x170066AC | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY685 | 0x170066AD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY686 | 0x170066AE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY687 | 0x170066AF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY688 | 0x170066B0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY689 | 0x170066B1 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY690 | 0x170066B2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY691 | 0x170066B3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY692 | 0x170066B4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY693 | 0x170066B5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY694 | 0x170066B6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY695 | 0x170066B7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY696 | 0x170066B8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY697 | 0x170066B9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY698 | 0x170066BA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY699 | 0x170066BB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY700 | 0x170066BC | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SFLASH_PUBLIC_KEY701 | 0x170066BD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY702 | 0x170066BE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY703 | 0x170066BF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY704 | 0x170066C0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY705 | 0x170066C1 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY706 | 0x170066C2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY707 | 0x170066C3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY708 | 0x170066C4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY709 | 0x170066C5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY710 | 0x170066C6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY711 | 0x170066C7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY712 | 0x170066C8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY713 | 0x170066C9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY714 | 0x170066CA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY715 | 0x170066CB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY716 | 0x170066CC | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY717 | 0x170066CD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY718 | 0x170066CE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY719 | 0x170066CF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY720 | 0x170066D0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY721 | 0x170066D1 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY722 | 0x170066D2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY723 | 0x170066D3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY724 | 0x170066D4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY725 | 0x170066D5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY726 | 0x170066D6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY727 | 0x170066D7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY728 | 0x170066D8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY729 | 0x170066D9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY730 | 0x170066DA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY731 | 0x170066DB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY732 | 0x170066DC | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SFLASH_PUBLIC_KEY733 | 0x170066DD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY734 | 0x170066DE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY735 | 0x170066DF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY736 | 0x170066E0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY737 | 0x170066E1 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY738 | 0x170066E2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY739 | 0x170066E3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY740 | 0x170066E4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY741 | 0x170066E5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY742 | 0x170066E6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY743 | 0x170066E7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY744 | 0x170066E8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY745 | 0x170066E9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY746 | 0x170066EA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY747 | 0x170066EB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY748 | 0x170066EC | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY749 | 0x170066ED | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY750 | 0x170066EE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY751 | 0x170066EF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY752 | 0x170066F0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY753 | 0x170066F1 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY754 | 0x170066F2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY755 | 0x170066F3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY756 | 0x170066F4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY757 | 0x170066F5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY758 | 0x170066F6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY759 | 0x170066F7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY760 | 0x170066F8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY761 | 0x170066F9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY762 | 0x170066FA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY763 | 0x170066FB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY764 | 0x170066FC | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SFLASH_PUBLIC_KEY765 | 0x170066FD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY766 | 0x170066FE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY767 | 0x170066FF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY768 | 0x17006700 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY769 | 0x17006701 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY770 | 0x17006702 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY771 | 0x17006703 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY772 | 0x17006704 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY773 | 0x17006705 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY774 | 0x17006706 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY775 | 0x17006707 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY776 | 0x17006708 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY777 | 0x17006709 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY778 | 0x1700670A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY779 | 0x1700670B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY780 | 0x1700670C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY781 | 0x1700670D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY782 | 0x1700670E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY783 | 0x1700670F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY784 | 0x17006710 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY785 | 0x17006711 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY786 | 0x17006712 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY787 | 0x17006713 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY788 | 0x17006714 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY789 | 0x17006715 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY790 | 0x17006716 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY791 | 0x17006717 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY792 | 0x17006718 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY793 | 0x17006719 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY794 | 0x1700671A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY795 | 0x1700671B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY796 | 0x1700671C | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SFLASH_PUBLIC_KEY797 | 0x1700671D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY798 | 0x1700671E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY799 | 0x1700671F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY800 | 0x17006720 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY801 | 0x17006721 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY802 | 0x17006722 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY803 | 0x17006723 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY804 | 0x17006724 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY805 | 0x17006725 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY806 | 0x17006726 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY807 | 0x17006727 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY808 | 0x17006728 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY809 | 0x17006729 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY810 | 0x1700672A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY811 | 0x1700672B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY812 | 0x1700672C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY813 | 0x1700672D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY814 | 0x1700672E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY815 | 0x1700672F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY816 | 0x17006730 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY817 | 0x17006731 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY818 | 0x17006732 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY819 | 0x17006733 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY820 | 0x17006734 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY821 | 0x17006735 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY822 | 0x17006736 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY823 | 0x17006737 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY824 | 0x17006738 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY825 | 0x17006739 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY826 | 0x1700673A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY827 | 0x1700673B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY828 | 0x1700673C | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SFLASH_PUBLIC_KEY829 | 0x1700673D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY830 | 0x1700673E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY831 | 0x1700673F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY832 | 0x17006740 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY833 | 0x17006741 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY834 | 0x17006742 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY835 | 0x17006743 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY836 | 0x17006744 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY837 | 0x17006745 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY838 | 0x17006746 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY839 | 0x17006747 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY840 | 0x17006748 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY841 | 0x17006749 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY842 | 0x1700674A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY843 | 0x1700674B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY844 | 0x1700674C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY845 | 0x1700674D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY846 | 0x1700674E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY847 | 0x1700674F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY848 | 0x17006750 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY849 | 0x17006751 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY850 | 0x17006752 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY851 | 0x17006753 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY852 | 0x17006754 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY853 | 0x17006755 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY854 | 0x17006756 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY855 | 0x17006757 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY856 | 0x17006758 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY857 | 0x17006759 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY858 | 0x1700675A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY859 | 0x1700675B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY860 | 0x1700675C | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SFLASH_PUBLIC_KEY861 | 0x1700675D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY862 | 0x1700675E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY863 | 0x1700675F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY864 | 0x17006760 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY865 | 0x17006761 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY866 | 0x17006762 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY867 | 0x17006763 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY868 | 0x17006764 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY869 | 0x17006765 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY870 | 0x17006766 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY871 | 0x17006767 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY872 | 0x17006768 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY873 | 0x17006769 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY874 | 0x1700676A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY875 | 0x1700676B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY876 | 0x1700676C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY877 | 0x1700676D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY878 | 0x1700676E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY879 | 0x1700676F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY880 | 0x17006770 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY881 | 0x17006771 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY882 | 0x17006772 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY883 | 0x17006773 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY884 | 0x17006774 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY885 | 0x17006775 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY886 | 0x17006776 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY887 | 0x17006777 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY888 | 0x17006778 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY889 | 0x17006779 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY890 | 0x1700677A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY891 | 0x1700677B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY892 | 0x1700677C | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SFLASH_PUBLIC_KEY893 | 0x1700677D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY894 | 0x1700677E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY895 | 0x1700677F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY896 | 0x17006780 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY897 | 0x17006781 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY898 | 0x17006782 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY899 | 0x17006783 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY900 | 0x17006784 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY901 | 0x17006785 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY902 | 0x17006786 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY903 | 0x17006787 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY904 | 0x17006788 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY905 | 0x17006789 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY906 | 0x1700678A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY907 | 0x1700678B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY908 | 0x1700678C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY909 | 0x1700678D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY910 | 0x1700678E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY911 | 0x1700678F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY912 | 0x17006790 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY913 | 0x17006791 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY914 | 0x17006792 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY915 | 0x17006793 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY916 | 0x17006794 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY917 | 0x17006795 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY918 | 0x17006796 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY919 | 0x17006797 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY920 | 0x17006798 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY921 | 0x17006799 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY922 | 0x1700679A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY923 | 0x1700679B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY924 | 0x1700679C | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SFLASH_PUBLIC_KEY925 | 0x1700679D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY926 | 0x1700679E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY927 | 0x1700679F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY928 | 0x170067A0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY929 | 0x170067A1 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY930 | 0x170067A2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY931 | 0x170067A3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY932 | 0x170067A4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY933 | 0x170067A5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY934 | 0x170067A6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY935 | 0x170067A7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY936 | 0x170067A8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY937 | 0x170067A9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY938 | 0x170067AA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY939 | 0x170067AB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY940 | 0x170067AC | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY941 | 0x170067AD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY942 | 0x170067AE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY943 | 0x170067AF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY944 | 0x170067B0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY945 | 0x170067B1 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY946 | 0x170067B2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY947 | 0x170067B3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY948 | 0x170067B4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY949 | 0x170067B5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY950 | 0x170067B6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY951 | 0x170067B7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY952 | 0x170067B8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY953 | 0x170067B9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY954 | 0x170067BA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY955 | 0x170067BB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY956 | 0x170067BC | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SFLASH_PUBLIC_KEY957 | 0x170067BD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY958 | 0x170067BE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY959 | 0x170067BF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY960 | 0x170067C0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY961 | 0x170067C1 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY962 | 0x170067C2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY963 | 0x170067C3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY964 | 0x170067C4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY965 | 0x170067C5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY966 | 0x170067C6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY967 | 0x170067C7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY968 | 0x170067C8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY969 | 0x170067C9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY970 | 0x170067CA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY971 | 0x170067CB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY972 | 0x170067CC | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY973 | 0x170067CD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY974 | 0x170067CE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY975 | 0x170067CF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY976 | 0x170067D0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY977 | 0x170067D1 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY978 | 0x170067D2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY979 | 0x170067D3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY980 | 0x170067D4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY981 | 0x170067D5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY982 | 0x170067D6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY983 | 0x170067D7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY984 | 0x170067D8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY985 | 0x170067D9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY986 | 0x170067DA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY987 | 0x170067DB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY988 | 0x170067DC | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SFLASH_PUBLIC_KEY989 | 0x170067DD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY990 | 0x170067DE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY991 | 0x170067DF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY992 | 0x170067E0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY993 | 0x170067E1 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY994 | 0x170067E2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY995 | 0x170067E3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY996 | 0x170067E4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY997 | 0x170067E5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY998 | 0x170067E6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY999 | 0x170067E7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1000 | 0x170067E8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1001 | 0x170067E9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1002 | 0x170067EA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1003 | 0x170067EB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1004 | 0x170067EC | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1005 | 0x170067ED | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1006 | 0x170067EE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1007 | 0x170067EF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1008 | 0x170067F0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1009 | 0x170067F1 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1010 | 0x170067F2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1011 | 0x170067F3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1012 | 0x170067F4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1013 | 0x170067F5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1014 | 0x170067F6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1015 | 0x170067F7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1016 | 0x170067F8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1017 | 0x170067F9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1018 | 0x170067FA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1019 | 0x170067FB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1020 | 0x170067FC | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SFLASH_PUBLIC_KEY1021 | 0x170067FD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1022 | 0x170067FE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1023 | 0x170067FF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1024 | 0x17006800 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1025 | 0x17006801 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1026 | 0x17006802 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1027 | 0x17006803 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1028 | 0x17006804 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1029 | 0x17006805 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1030 | 0x17006806 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1031 | 0x17006807 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1032 | 0x17006808 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1033 | 0x17006809 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1034 | 0x1700680A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1035 | 0x1700680B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1036 | 0x1700680C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1037 | 0x1700680D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1038 | 0x1700680E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1039 | 0x1700680F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1040 | 0x17006810 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1041 | 0x17006811 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1042 | 0x17006812 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1043 | 0x17006813 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1044 | 0x17006814 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1045 | 0x17006815 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1046 | 0x17006816 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1047 | 0x17006817 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1048 | 0x17006818 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1049 | 0x17006819 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1050 | 0x1700681A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1051 | 0x1700681B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1052 | 0x1700681C | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SFLASH_PUBLIC_KEY1053 | 0x1700681D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1054 | 0x1700681E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1055 | 0x1700681F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1056 | 0x17006820 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1057 | 0x17006821 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1058 | 0x17006822 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1059 | 0x17006823 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1060 | 0x17006824 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1061 | 0x17006825 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1062 | 0x17006826 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1063 | 0x17006827 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1064 | 0x17006828 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1065 | 0x17006829 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1066 | 0x1700682A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1067 | 0x1700682B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1068 | 0x1700682C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1069 | 0x1700682D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1070 | 0x1700682E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1071 | 0x1700682F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1072 | 0x17006830 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1073 | 0x17006831 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1074 | 0x17006832 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1075 | 0x17006833 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1076 | 0x17006834 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1077 | 0x17006835 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1078 | 0x17006836 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1079 | 0x17006837 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1080 | 0x17006838 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1081 | 0x17006839 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1082 | 0x1700683A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1083 | 0x1700683B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1084 | 0x1700683C | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SFLASH_PUBLIC_KEY1085 | 0x1700683D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1086 | 0x1700683E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1087 | 0x1700683F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1088 | 0x17006840 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1089 | 0x17006841 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1090 | 0x17006842 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1091 | 0x17006843 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1092 | 0x17006844 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1093 | 0x17006845 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1094 | 0x17006846 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1095 | 0x17006847 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1096 | 0x17006848 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1097 | 0x17006849 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1098 | 0x1700684A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1099 | 0x1700684B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1100 | 0x1700684C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1101 | 0x1700684D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1102 | 0x1700684E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1103 | 0x1700684F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1104 | 0x17006850 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1105 | 0x17006851 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1106 | 0x17006852 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1107 | 0x17006853 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1108 | 0x17006854 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1109 | 0x17006855 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1110 | 0x17006856 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1111 | 0x17006857 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1112 | 0x17006858 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1113 | 0x17006859 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1114 | 0x1700685A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1115 | 0x1700685B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1116 | 0x1700685C | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SFLASH_PUBLIC_KEY1117 | 0x1700685D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1118 | 0x1700685E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1119 | 0x1700685F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1120 | 0x17006860 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1121 | 0x17006861 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1122 | 0x17006862 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1123 | 0x17006863 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1124 | 0x17006864 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1125 | 0x17006865 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1126 | 0x17006866 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1127 | 0x17006867 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1128 | 0x17006868 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1129 | 0x17006869 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1130 | 0x1700686A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1131 | 0x1700686B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1132 | 0x1700686C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1133 | 0x1700686D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1134 | 0x1700686E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1135 | 0x1700686F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1136 | 0x17006870 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1137 | 0x17006871 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1138 | 0x17006872 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1139 | 0x17006873 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1140 | 0x17006874 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1141 | 0x17006875 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1142 | 0x17006876 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1143 | 0x17006877 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1144 | 0x17006878 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1145 | 0x17006879 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1146 | 0x1700687A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1147 | 0x1700687B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1148 | 0x1700687C | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SFLASH_PUBLIC_KEY1149 | 0x1700687D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1150 | 0x1700687E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1151 | 0x1700687F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1152 | 0x17006880 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1153 | 0x17006881 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1154 | 0x17006882 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1155 | 0x17006883 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1156 | 0x17006884 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1157 | 0x17006885 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1158 | 0x17006886 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1159 | 0x17006887 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1160 | 0x17006888 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1161 | 0x17006889 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1162 | 0x1700688A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1163 | 0x1700688B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1164 | 0x1700688C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1165 | 0x1700688D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1166 | 0x1700688E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1167 | 0x1700688F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1168 | 0x17006890 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1169 | 0x17006891 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1170 | 0x17006892 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1171 | 0x17006893 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1172 | 0x17006894 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1173 | 0x17006895 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1174 | 0x17006896 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1175 | 0x17006897 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1176 | 0x17006898 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1177 | 0x17006899 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1178 | 0x1700689A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1179 | 0x1700689B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1180 | 0x1700689C | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SFLASH_PUBLIC_KEY1181 | 0x1700689D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1182 | 0x1700689E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1183 | 0x1700689F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1184 | 0x170068A0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1185 | 0x170068A1 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1186 | 0x170068A2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1187 | 0x170068A3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1188 | 0x170068A4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1189 | 0x170068A5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1190 | 0x170068A6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1191 | 0x170068A7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1192 | 0x170068A8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1193 | 0x170068A9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1194 | 0x170068AA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1195 | 0x170068AB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1196 | 0x170068AC | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1197 | 0x170068AD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1198 | 0x170068AE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1199 | 0x170068AF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1200 | 0x170068B0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1201 | 0x170068B1 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1202 | 0x170068B2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1203 | 0x170068B3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1204 | 0x170068B4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1205 | 0x170068B5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1206 | 0x170068B6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1207 | 0x170068B7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1208 | 0x170068B8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1209 | 0x170068B9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1210 | 0x170068BA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1211 | 0x170068BB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1212 | 0x170068BC | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SFLASH_PUBLIC_KEY1213 | 0x170068BD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1214 | 0x170068BE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1215 | 0x170068BF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1216 | 0x170068C0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1217 | 0x170068C1 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1218 | 0x170068C2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1219 | 0x170068C3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1220 | 0x170068C4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1221 | 0x170068C5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1222 | 0x170068C6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1223 | 0x170068C7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1224 | 0x170068C8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1225 | 0x170068C9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1226 | 0x170068CA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1227 | 0x170068CB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1228 | 0x170068CC | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1229 | 0x170068CD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1230 | 0x170068CE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1231 | 0x170068CF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1232 | 0x170068D0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1233 | 0x170068D1 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1234 | 0x170068D2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1235 | 0x170068D3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1236 | 0x170068D4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1237 | 0x170068D5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1238 | 0x170068D6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1239 | 0x170068D7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1240 | 0x170068D8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1241 | 0x170068D9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1242 | 0x170068DA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1243 | 0x170068DB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1244 | 0x170068DC | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SFLASH_PUBLIC_KEY1245 | 0x170068DD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1246 | 0x170068DE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1247 | 0x170068DF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1248 | 0x170068E0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1249 | 0x170068E1 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1250 | 0x170068E2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1251 | 0x170068E3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1252 | 0x170068E4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1253 | 0x170068E5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1254 | 0x170068E6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1255 | 0x170068E7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1256 | 0x170068E8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1257 | 0x170068E9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1258 | 0x170068EA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1259 | 0x170068EB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1260 | 0x170068EC | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1261 | 0x170068ED | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1262 | 0x170068EE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1263 | 0x170068EF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1264 | 0x170068F0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1265 | 0x170068F1 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1266 | 0x170068F2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1267 | 0x170068F3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1268 | 0x170068F4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1269 | 0x170068F5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1270 | 0x170068F6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1271 | 0x170068F7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1272 | 0x170068F8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1273 | 0x170068F9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1274 | 0x170068FA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1275 | 0x170068FB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1276 | 0x170068FC | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SFLASH_PUBLIC_KEY1277 | 0x170068FD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1278 | 0x170068FE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1279 | 0x170068FF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1280 | 0x17006900 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1281 | 0x17006901 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1282 | 0x17006902 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1283 | 0x17006903 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1284 | 0x17006904 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1285 | 0x17006905 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1286 | 0x17006906 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1287 | 0x17006907 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1288 | 0x17006908 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1289 | 0x17006909 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1290 | 0x1700690A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1291 | 0x1700690B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1292 | 0x1700690C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1293 | 0x1700690D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1294 | 0x1700690E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1295 | 0x1700690F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1296 | 0x17006910 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1297 | 0x17006911 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1298 | 0x17006912 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1299 | 0x17006913 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1300 | 0x17006914 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1301 | 0x17006915 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1302 | 0x17006916 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1303 | 0x17006917 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1304 | 0x17006918 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1305 | 0x17006919 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1306 | 0x1700691A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1307 | 0x1700691B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1308 | 0x1700691C | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SFLASH_PUBLIC_KEY1309 | 0x1700691D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1310 | 0x1700691E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1311 | 0x1700691F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1312 | 0x17006920 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1313 | 0x17006921 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1314 | 0x17006922 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1315 | 0x17006923 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1316 | 0x17006924 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1317 | 0x17006925 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1318 | 0x17006926 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1319 | 0x17006927 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1320 | 0x17006928 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1321 | 0x17006929 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1322 | 0x1700692A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1323 | 0x1700692B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1324 | 0x1700692C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1325 | 0x1700692D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1326 | 0x1700692E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1327 | 0x1700692F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1328 | 0x17006930 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1329 | 0x17006931 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1330 | 0x17006932 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1331 | 0x17006933 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1332 | 0x17006934 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1333 | 0x17006935 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1334 | 0x17006936 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1335 | 0x17006937 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1336 | 0x17006938 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1337 | 0x17006939 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1338 | 0x1700693A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1339 | 0x1700693B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1340 | 0x1700693C | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SFLASH_PUBLIC_KEY1341 | 0x1700693D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1342 | 0x1700693E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1343 | 0x1700693F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1344 | 0x17006940 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1345 | 0x17006941 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1346 | 0x17006942 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1347 | 0x17006943 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1348 | 0x17006944 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1349 | 0x17006945 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1350 | 0x17006946 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1351 | 0x17006947 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1352 | 0x17006948 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1353 | 0x17006949 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1354 | 0x1700694A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1355 | 0x1700694B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1356 | 0x1700694C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1357 | 0x1700694D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1358 | 0x1700694E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1359 | 0x1700694F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1360 | 0x17006950 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1361 | 0x17006951 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1362 | 0x17006952 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1363 | 0x17006953 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1364 | 0x17006954 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1365 | 0x17006955 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1366 | 0x17006956 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1367 | 0x17006957 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1368 | 0x17006958 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1369 | 0x17006959 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1370 | 0x1700695A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1371 | 0x1700695B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1372 | 0x1700695C | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SFLASH_PUBLIC_KEY1373 | 0x1700695D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1374 | 0x1700695E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1375 | 0x1700695F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1376 | 0x17006960 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1377 | 0x17006961 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1378 | 0x17006962 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1379 | 0x17006963 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1380 | 0x17006964 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1381 | 0x17006965 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1382 | 0x17006966 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1383 | 0x17006967 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1384 | 0x17006968 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1385 | 0x17006969 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1386 | 0x1700696A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1387 | 0x1700696B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1388 | 0x1700696C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1389 | 0x1700696D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1390 | 0x1700696E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1391 | 0x1700696F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1392 | 0x17006970 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1393 | 0x17006971 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1394 | 0x17006972 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1395 | 0x17006973 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1396 | 0x17006974 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1397 | 0x17006975 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1398 | 0x17006976 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1399 | 0x17006977 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1400 | 0x17006978 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1401 | 0x17006979 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1402 | 0x1700697A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1403 | 0x1700697B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1404 | 0x1700697C | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SFLASH_PUBLIC_KEY1405 | 0x1700697D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1406 | 0x1700697E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1407 | 0x1700697F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1408 | 0x17006980 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1409 | 0x17006981 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1410 | 0x17006982 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1411 | 0x17006983 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1412 | 0x17006984 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1413 | 0x17006985 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1414 | 0x17006986 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1415 | 0x17006987 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1416 | 0x17006988 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1417 | 0x17006989 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1418 | 0x1700698A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1419 | 0x1700698B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1420 | 0x1700698C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1421 | 0x1700698D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1422 | 0x1700698E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1423 | 0x1700698F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1424 | 0x17006990 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1425 | 0x17006991 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1426 | 0x17006992 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1427 | 0x17006993 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1428 | 0x17006994 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1429 | 0x17006995 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1430 | 0x17006996 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1431 | 0x17006997 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1432 | 0x17006998 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1433 | 0x17006999 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1434 | 0x1700699A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1435 | 0x1700699B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1436 | 0x1700699C | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SFLASH_PUBLIC_KEY1437 | 0x1700699D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1438 | 0x1700699E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1439 | 0x1700699F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1440 | 0x170069A0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1441 | 0x170069A1 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1442 | 0x170069A2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1443 | 0x170069A3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1444 | 0x170069A4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1445 | 0x170069A5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1446 | 0x170069A6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1447 | 0x170069A7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1448 | 0x170069A8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1449 | 0x170069A9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1450 | 0x170069AA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1451 | 0x170069AB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1452 | 0x170069AC | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1453 | 0x170069AD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1454 | 0x170069AE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1455 | 0x170069AF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1456 | 0x170069B0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1457 | 0x170069B1 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1458 | 0x170069B2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1459 | 0x170069B3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1460 | 0x170069B4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1461 | 0x170069B5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1462 | 0x170069B6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1463 | 0x170069B7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1464 | 0x170069B8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1465 | 0x170069B9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1466 | 0x170069BA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1467 | 0x170069BB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1468 | 0x170069BC | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SFLASH_PUBLIC_KEY1469 | 0x170069BD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1470 | 0x170069BE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1471 | 0x170069BF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1472 | 0x170069C0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1473 | 0x170069C1 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1474 | 0x170069C2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1475 | 0x170069C3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1476 | 0x170069C4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1477 | 0x170069C5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1478 | 0x170069C6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1479 | 0x170069C7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1480 | 0x170069C8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1481 | 0x170069C9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1482 | 0x170069CA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1483 | 0x170069CB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1484 | 0x170069CC | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1485 | 0x170069CD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1486 | 0x170069CE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1487 | 0x170069CF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1488 | 0x170069D0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1489 | 0x170069D1 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1490 | 0x170069D2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1491 | 0x170069D3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1492 | 0x170069D4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1493 | 0x170069D5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1494 | 0x170069D6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1495 | 0x170069D7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1496 | 0x170069D8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1497 | 0x170069D9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1498 | 0x170069DA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1499 | 0x170069DB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1500 | 0x170069DC | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SFLASH_PUBLIC_KEY1501 | 0x170069DD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1502 | 0x170069DE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1503 | 0x170069DF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1504 | 0x170069E0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1505 | 0x170069E1 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1506 | 0x170069E2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1507 | 0x170069E3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1508 | 0x170069E4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1509 | 0x170069E5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1510 | 0x170069E6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1511 | 0x170069E7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1512 | 0x170069E8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1513 | 0x170069E9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1514 | 0x170069EA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1515 | 0x170069EB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1516 | 0x170069EC | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1517 | 0x170069ED | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1518 | 0x170069EE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1519 | 0x170069EF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1520 | 0x170069F0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1521 | 0x170069F1 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1522 | 0x170069F2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1523 | 0x170069F3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1524 | 0x170069F4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1525 | 0x170069F5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1526 | 0x170069F6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1527 | 0x170069F7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1528 | 0x170069F8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1529 | 0x170069F9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1530 | 0x170069FA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1531 | 0x170069FB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1532 | 0x170069FC | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SFLASH_PUBLIC_KEY1533 | 0x170069FD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1534 | 0x170069FE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1535 | 0x170069FF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1536 | 0x17006A00 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1537 | 0x17006A01 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1538 | 0x17006A02 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1539 | 0x17006A03 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1540 | 0x17006A04 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1541 | 0x17006A05 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1542 | 0x17006A06 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1543 | 0x17006A07 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1544 | 0x17006A08 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1545 | 0x17006A09 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1546 | 0x17006A0A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1547 | 0x17006A0B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1548 | 0x17006A0C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1549 | 0x17006A0D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1550 | 0x17006A0E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1551 | 0x17006A0F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1552 | 0x17006A10 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1553 | 0x17006A11 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1554 | 0x17006A12 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1555 | 0x17006A13 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1556 | 0x17006A14 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1557 | 0x17006A15 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1558 | 0x17006A16 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1559 | 0x17006A17 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1560 | 0x17006A18 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1561 | 0x17006A19 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1562 | 0x17006A1A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1563 | 0x17006A1B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1564 | 0x17006A1C | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SFLASH_PUBLIC_KEY1565 | 0x17006A1D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1566 | 0x17006A1E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1567 | 0x17006A1F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1568 | 0x17006A20 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1569 | 0x17006A21 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1570 | 0x17006A22 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1571 | 0x17006A23 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1572 | 0x17006A24 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1573 | 0x17006A25 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1574 | 0x17006A26 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1575 | 0x17006A27 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1576 | 0x17006A28 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1577 | 0x17006A29 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1578 | 0x17006A2A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1579 | 0x17006A2B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1580 | 0x17006A2C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1581 | 0x17006A2D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1582 | 0x17006A2E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1583 | 0x17006A2F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1584 | 0x17006A30 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1585 | 0x17006A31 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1586 | 0x17006A32 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1587 | 0x17006A33 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1588 | 0x17006A34 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1589 | 0x17006A35 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1590 | 0x17006A36 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1591 | 0x17006A37 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1592 | 0x17006A38 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1593 | 0x17006A39 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1594 | 0x17006A3A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1595 | 0x17006A3B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1596 | 0x17006A3C | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SFLASH_PUBLIC_KEY1597 | 0x17006A3D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1598 | 0x17006A3E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1599 | 0x17006A3F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1600 | 0x17006A40 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1601 | 0x17006A41 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1602 | 0x17006A42 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1603 | 0x17006A43 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1604 | 0x17006A44 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1605 | 0x17006A45 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1606 | 0x17006A46 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1607 | 0x17006A47 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1608 | 0x17006A48 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1609 | 0x17006A49 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1610 | 0x17006A4A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1611 | 0x17006A4B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1612 | 0x17006A4C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1613 | 0x17006A4D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1614 | 0x17006A4E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1615 | 0x17006A4F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1616 | 0x17006A50 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1617 | 0x17006A51 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1618 | 0x17006A52 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1619 | 0x17006A53 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1620 | 0x17006A54 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1621 | 0x17006A55 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1622 | 0x17006A56 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1623 | 0x17006A57 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1624 | 0x17006A58 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1625 | 0x17006A59 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1626 | 0x17006A5A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1627 | 0x17006A5B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1628 | 0x17006A5C | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SFLASH_PUBLIC_KEY1629 | 0x17006A5D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1630 | 0x17006A5E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1631 | 0x17006A5F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1632 | 0x17006A60 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1633 | 0x17006A61 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1634 | 0x17006A62 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1635 | 0x17006A63 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1636 | 0x17006A64 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1637 | 0x17006A65 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1638 | 0x17006A66 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1639 | 0x17006A67 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1640 | 0x17006A68 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1641 | 0x17006A69 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1642 | 0x17006A6A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1643 | 0x17006A6B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1644 | 0x17006A6C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1645 | 0x17006A6D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1646 | 0x17006A6E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1647 | 0x17006A6F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1648 | 0x17006A70 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1649 | 0x17006A71 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1650 | 0x17006A72 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1651 | 0x17006A73 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1652 | 0x17006A74 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1653 | 0x17006A75 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1654 | 0x17006A76 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1655 | 0x17006A77 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1656 | 0x17006A78 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1657 | 0x17006A79 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1658 | 0x17006A7A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1659 | 0x17006A7B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1660 | 0x17006A7C | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SFLASH_PUBLIC_KEY1661 | 0x17006A7D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1662 | 0x17006A7E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1663 | 0x17006A7F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1664 | 0x17006A80 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1665 | 0x17006A81 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1666 | 0x17006A82 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1667 | 0x17006A83 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1668 | 0x17006A84 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1669 | 0x17006A85 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1670 | 0x17006A86 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1671 | 0x17006A87 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1672 | 0x17006A88 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1673 | 0x17006A89 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1674 | 0x17006A8A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1675 | 0x17006A8B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1676 | 0x17006A8C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1677 | 0x17006A8D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1678 | 0x17006A8E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1679 | 0x17006A8F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1680 | 0x17006A90 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1681 | 0x17006A91 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1682 | 0x17006A92 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1683 | 0x17006A93 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1684 | 0x17006A94 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1685 | 0x17006A95 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1686 | 0x17006A96 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1687 | 0x17006A97 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1688 | 0x17006A98 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1689 | 0x17006A99 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1690 | 0x17006A9A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1691 | 0x17006A9B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1692 | 0x17006A9C | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SFLASH_PUBLIC_KEY1693 | 0x17006A9D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1694 | 0x17006A9E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1695 | 0x17006A9F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1696 | 0x17006AA0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1697 | 0x17006AA1 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1698 | 0x17006AA2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1699 | 0x17006AA3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1700 | 0x17006AA4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1701 | 0x17006AA5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1702 | 0x17006AA6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1703 | 0x17006AA7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1704 | 0x17006AA8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1705 | 0x17006AA9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1706 | 0x17006AAA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1707 | 0x17006AAB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1708 | 0x17006AAC | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1709 | 0x17006AAD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1710 | 0x17006AAE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1711 | 0x17006AAF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1712 | 0x17006AB0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1713 | 0x17006AB1 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1714 | 0x17006AB2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1715 | 0x17006AB3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1716 | 0x17006AB4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1717 | 0x17006AB5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1718 | 0x17006AB6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1719 | 0x17006AB7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1720 | 0x17006AB8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1721 | 0x17006AB9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1722 | 0x17006ABA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1723 | 0x17006ABB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1724 | 0x17006ABC | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SFLASH_PUBLIC_KEY1725 | 0x17006ABD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1726 | 0x17006ABE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1727 | 0x17006ABF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1728 | 0x17006AC0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1729 | 0x17006AC1 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1730 | 0x17006AC2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1731 | 0x17006AC3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1732 | 0x17006AC4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1733 | 0x17006AC5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1734 | 0x17006AC6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1735 | 0x17006AC7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1736 | 0x17006AC8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1737 | 0x17006AC9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1738 | 0x17006ACA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1739 | 0x17006ACB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1740 | 0x17006ACC | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1741 | 0x17006ACD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1742 | 0x17006ACE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1743 | 0x17006ACF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1744 | 0x17006AD0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1745 | 0x17006AD1 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1746 | 0x17006AD2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1747 | 0x17006AD3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1748 | 0x17006AD4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1749 | 0x17006AD5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1750 | 0x17006AD6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1751 | 0x17006AD7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1752 | 0x17006AD8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1753 | 0x17006AD9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1754 | 0x17006ADA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1755 | 0x17006ADB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1756 | 0x17006ADC | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SFLASH_PUBLIC_KEY1757 | 0x17006ADD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1758 | 0x17006ADE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1759 | 0x17006ADF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1760 | 0x17006AE0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1761 | 0x17006AE1 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1762 | 0x17006AE2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1763 | 0x17006AE3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1764 | 0x17006AE4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1765 | 0x17006AE5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1766 | 0x17006AE6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1767 | 0x17006AE7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1768 | 0x17006AE8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1769 | 0x17006AE9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1770 | 0x17006AEA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1771 | 0x17006AEB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1772 | 0x17006AEC | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1773 | 0x17006AED | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1774 | 0x17006AEE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1775 | 0x17006AEF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1776 | 0x17006AF0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1777 | 0x17006AF1 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1778 | 0x17006AF2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1779 | 0x17006AF3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1780 | 0x17006AF4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1781 | 0x17006AF5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1782 | 0x17006AF6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1783 | 0x17006AF7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1784 | 0x17006AF8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1785 | 0x17006AF9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1786 | 0x17006AFA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1787 | 0x17006AFB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1788 | 0x17006AFC | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SFLASH_PUBLIC_KEY1789 | 0x17006AFD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1790 | 0x17006AFE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1791 | 0x17006AFF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1792 | 0x17006B00 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1793 | 0x17006B01 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1794 | 0x17006B02 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1795 | 0x17006B03 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1796 | 0x17006B04 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1797 | 0x17006B05 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1798 | 0x17006B06 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1799 | 0x17006B07 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1800 | 0x17006B08 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1801 | 0x17006B09 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1802 | 0x17006B0A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1803 | 0x17006B0B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1804 | 0x17006B0C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1805 | 0x17006B0D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1806 | 0x17006B0E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1807 | 0x17006B0F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1808 | 0x17006B10 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1809 | 0x17006B11 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1810 | 0x17006B12 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1811 | 0x17006B13 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1812 | 0x17006B14 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1813 | 0x17006B15 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1814 | 0x17006B16 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1815 | 0x17006B17 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1816 | 0x17006B18 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1817 | 0x17006B19 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1818 | 0x17006B1A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1819 | 0x17006B1B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1820 | 0x17006B1C | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SFLASH_PUBLIC_KEY1821 | 0x17006B1D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1822 | 0x17006B1E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1823 | 0x17006B1F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1824 | 0x17006B20 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1825 | 0x17006B21 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1826 | 0x17006B22 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1827 | 0x17006B23 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1828 | 0x17006B24 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1829 | 0x17006B25 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1830 | 0x17006B26 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1831 | 0x17006B27 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1832 | 0x17006B28 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1833 | 0x17006B29 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1834 | 0x17006B2A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1835 | 0x17006B2B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1836 | 0x17006B2C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1837 | 0x17006B2D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1838 | 0x17006B2E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1839 | 0x17006B2F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1840 | 0x17006B30 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1841 | 0x17006B31 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1842 | 0x17006B32 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1843 | 0x17006B33 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1844 | 0x17006B34 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1845 | 0x17006B35 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1846 | 0x17006B36 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1847 | 0x17006B37 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1848 | 0x17006B38 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1849 | 0x17006B39 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1850 | 0x17006B3A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1851 | 0x17006B3B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1852 | 0x17006B3C | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SFLASH_PUBLIC_KEY1853 | 0x17006B3D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1854 | 0x17006B3E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1855 | 0x17006B3F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1856 | 0x17006B40 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1857 | 0x17006B41 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1858 | 0x17006B42 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1859 | 0x17006B43 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1860 | 0x17006B44 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1861 | 0x17006B45 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1862 | 0x17006B46 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1863 | 0x17006B47 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1864 | 0x17006B48 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1865 | 0x17006B49 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1866 | 0x17006B4A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1867 | 0x17006B4B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1868 | 0x17006B4C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1869 | 0x17006B4D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1870 | 0x17006B4E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1871 | 0x17006B4F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1872 | 0x17006B50 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1873 | 0x17006B51 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1874 | 0x17006B52 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1875 | 0x17006B53 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1876 | 0x17006B54 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1877 | 0x17006B55 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1878 | 0x17006B56 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1879 | 0x17006B57 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1880 | 0x17006B58 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1881 | 0x17006B59 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1882 | 0x17006B5A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1883 | 0x17006B5B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1884 | 0x17006B5C | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SFLASH_PUBLIC_KEY1885 | 0x17006B5D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1886 | 0x17006B5E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1887 | 0x17006B5F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1888 | 0x17006B60 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1889 | 0x17006B61 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1890 | 0x17006B62 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1891 | 0x17006B63 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1892 | 0x17006B64 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1893 | 0x17006B65 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1894 | 0x17006B66 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1895 | 0x17006B67 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1896 | 0x17006B68 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1897 | 0x17006B69 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1898 | 0x17006B6A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1899 | 0x17006B6B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1900 | 0x17006B6C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1901 | 0x17006B6D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1902 | 0x17006B6E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1903 | 0x17006B6F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1904 | 0x17006B70 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1905 | 0x17006B71 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1906 | 0x17006B72 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1907 | 0x17006B73 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1908 | 0x17006B74 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1909 | 0x17006B75 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1910 | 0x17006B76 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1911 | 0x17006B77 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1912 | 0x17006B78 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1913 | 0x17006B79 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1914 | 0x17006B7A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1915 | 0x17006B7B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1916 | 0x17006B7C | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SFLASH_PUBLIC_KEY1917 | 0x17006B7D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1918 | 0x17006B7E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1919 | 0x17006B7F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1920 | 0x17006B80 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1921 | 0x17006B81 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1922 | 0x17006B82 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1923 | 0x17006B83 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1924 | 0x17006B84 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1925 | 0x17006B85 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1926 | 0x17006B86 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1927 | 0x17006B87 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1928 | 0x17006B88 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1929 | 0x17006B89 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1930 | 0x17006B8A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1931 | 0x17006B8B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1932 | 0x17006B8C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1933 | 0x17006B8D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1934 | 0x17006B8E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1935 | 0x17006B8F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1936 | 0x17006B90 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1937 | 0x17006B91 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1938 | 0x17006B92 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1939 | 0x17006B93 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1940 | 0x17006B94 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1941 | 0x17006B95 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1942 | 0x17006B96 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1943 | 0x17006B97 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1944 | 0x17006B98 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1945 | 0x17006B99 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1946 | 0x17006B9A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1947 | 0x17006B9B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1948 | 0x17006B9C | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SFLASH_PUBLIC_KEY1949 | 0x17006B9D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1950 | 0x17006B9E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1951 | 0x17006B9F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1952 | 0x17006BA0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1953 | 0x17006BA1 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1954 | 0x17006BA2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1955 | 0x17006BA3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1956 | 0x17006BA4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1957 | 0x17006BA5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1958 | 0x17006BA6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1959 | 0x17006BA7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1960 | 0x17006BA8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1961 | 0x17006BA9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1962 | 0x17006BAA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1963 | 0x17006BAB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1964 | 0x17006BAC | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1965 | 0x17006BAD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1966 | 0x17006BAE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1967 | 0x17006BAF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1968 | 0x17006BB0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1969 | 0x17006BB1 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1970 | 0x17006BB2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1971 | 0x17006BB3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1972 | 0x17006BB4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1973 | 0x17006BB5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1974 | 0x17006BB6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1975 | 0x17006BB7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1976 | 0x17006BB8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1977 | 0x17006BB9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1978 | 0x17006BBA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1979 | 0x17006BBB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1980 | 0x17006BBC | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SFLASH_PUBLIC_KEY1981 | 0x17006BBD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1982 | 0x17006BBE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1983 | 0x17006BBF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1984 | 0x17006BC0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1985 | 0x17006BC1 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1986 | 0x17006BC2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1987 | 0x17006BC3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1988 | 0x17006BC4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1989 | 0x17006BC5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1990 | 0x17006BC6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1991 | 0x17006BC7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1992 | 0x17006BC8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1993 | 0x17006BC9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1994 | 0x17006BCA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1995 | 0x17006BCB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1996 | 0x17006BCC | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1997 | 0x17006BCD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1998 | 0x17006BCE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1999 | 0x17006BCF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2000 | 0x17006BD0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2001 | 0x17006BD1 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2002 | 0x17006BD2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2003 | 0x17006BD3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2004 | 0x17006BD4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2005 | 0x17006BD5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2006 | 0x17006BD6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2007 | 0x17006BD7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2008 | 0x17006BD8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2009 | 0x17006BD9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2010 | 0x17006BDA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2011 | 0x17006BDB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2012 | 0x17006BDC | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SFLASH_PUBLIC_KEY2013 | 0x17006BDD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2014 | 0x17006BDE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2015 | 0x17006BDF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2016 | 0x17006BE0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2017 | 0x17006BE1 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2018 | 0x17006BE2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2019 | 0x17006BE3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2020 | 0x17006BE4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2021 | 0x17006BE5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2022 | 0x17006BE6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2023 | 0x17006BE7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2024 | 0x17006BE8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2025 | 0x17006BE9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2026 | 0x17006BEA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2027 | 0x17006BEB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2028 | 0x17006BEC | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2029 | 0x17006BED | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2030 | 0x17006BEE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2031 | 0x17006BEF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2032 | 0x17006BF0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2033 | 0x17006BF1 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2034 | 0x17006BF2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2035 | 0x17006BF3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2036 | 0x17006BF4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2037 | 0x17006BF5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2038 | 0x17006BF6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2039 | 0x17006BF7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2040 | 0x17006BF8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2041 | 0x17006BF9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2042 | 0x17006BFA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2043 | 0x17006BFB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2044 | 0x17006BFC | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SFLASH_PUBLIC_KEY2045 | 0x17006BFD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2046 | 0x17006BFE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2047 | 0x17006BFF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2048 | 0x17006C00 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2049 | 0x17006C01 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2050 | 0x17006C02 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2051 | 0x17006C03 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2052 | 0x17006C04 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2053 | 0x17006C05 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2054 | 0x17006C06 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2055 | 0x17006C07 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2056 | 0x17006C08 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2057 | 0x17006C09 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2058 | 0x17006C0A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2059 | 0x17006C0B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2060 | 0x17006C0C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2061 | 0x17006C0D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2062 | 0x17006C0E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2063 | 0x17006C0F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2064 | 0x17006C10 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2065 | 0x17006C11 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2066 | 0x17006C12 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2067 | 0x17006C13 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2068 | 0x17006C14 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2069 | 0x17006C15 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2070 | 0x17006C16 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2071 | 0x17006C17 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2072 | 0x17006C18 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2073 | 0x17006C19 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2074 | 0x17006C1A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2075 | 0x17006C1B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2076 | 0x17006C1C | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SFLASH_PUBLIC_KEY2077 | 0x17006C1D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2078 | 0x17006C1E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2079 | 0x17006C1F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2080 | 0x17006C20 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2081 | 0x17006C21 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2082 | 0x17006C22 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2083 | 0x17006C23 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2084 | 0x17006C24 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2085 | 0x17006C25 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2086 | 0x17006C26 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2087 | 0x17006C27 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2088 | 0x17006C28 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2089 | 0x17006C29 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2090 | 0x17006C2A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2091 | 0x17006C2B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2092 | 0x17006C2C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2093 | 0x17006C2D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2094 | 0x17006C2E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2095 | 0x17006C2F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2096 | 0x17006C30 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2097 | 0x17006C31 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2098 | 0x17006C32 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2099 | 0x17006C33 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2100 | 0x17006C34 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2101 | 0x17006C35 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2102 | 0x17006C36 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2103 | 0x17006C37 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2104 | 0x17006C38 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2105 | 0x17006C39 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2106 | 0x17006C3A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2107 | 0x17006C3B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2108 | 0x17006C3C | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SFLASH_PUBLIC_KEY2109 | 0x17006C3D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2110 | 0x17006C3E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2111 | 0x17006C3F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2112 | 0x17006C40 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2113 | 0x17006C41 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2114 | 0x17006C42 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2115 | 0x17006C43 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2116 | 0x17006C44 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2117 | 0x17006C45 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2118 | 0x17006C46 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2119 | 0x17006C47 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2120 | 0x17006C48 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2121 | 0x17006C49 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2122 | 0x17006C4A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2123 | 0x17006C4B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2124 | 0x17006C4C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2125 | 0x17006C4D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2126 | 0x17006C4E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2127 | 0x17006C4F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2128 | 0x17006C50 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2129 | 0x17006C51 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2130 | 0x17006C52 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2131 | 0x17006C53 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2132 | 0x17006C54 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2133 | 0x17006C55 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2134 | 0x17006C56 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2135 | 0x17006C57 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2136 | 0x17006C58 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2137 | 0x17006C59 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2138 | 0x17006C5A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2139 | 0x17006C5B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2140 | 0x17006C5C | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SFLASH_PUBLIC_KEY2141 | 0x17006C5D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2142 | 0x17006C5E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2143 | 0x17006C5F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2144 | 0x17006C60 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2145 | 0x17006C61 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2146 | 0x17006C62 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2147 | 0x17006C63 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2148 | 0x17006C64 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2149 | 0x17006C65 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2150 | 0x17006C66 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2151 | 0x17006C67 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2152 | 0x17006C68 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2153 | 0x17006C69 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2154 | 0x17006C6A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2155 | 0x17006C6B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2156 | 0x17006C6C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2157 | 0x17006C6D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2158 | 0x17006C6E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2159 | 0x17006C6F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2160 | 0x17006C70 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2161 | 0x17006C71 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2162 | 0x17006C72 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2163 | 0x17006C73 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2164 | 0x17006C74 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2165 | 0x17006C75 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2166 | 0x17006C76 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2167 | 0x17006C77 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2168 | 0x17006C78 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2169 | 0x17006C79 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2170 | 0x17006C7A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2171 | 0x17006C7B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2172 | 0x17006C7C | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SFLASH_PUBLIC_KEY2173 | 0x17006C7D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2174 | 0x17006C7E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2175 | 0x17006C7F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2176 | 0x17006C80 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2177 | 0x17006C81 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2178 | 0x17006C82 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2179 | 0x17006C83 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2180 | 0x17006C84 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2181 | 0x17006C85 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2182 | 0x17006C86 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2183 | 0x17006C87 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2184 | 0x17006C88 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2185 | 0x17006C89 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2186 | 0x17006C8A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2187 | 0x17006C8B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2188 | 0x17006C8C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2189 | 0x17006C8D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2190 | 0x17006C8E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2191 | 0x17006C8F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2192 | 0x17006C90 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2193 | 0x17006C91 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2194 | 0x17006C92 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2195 | 0x17006C93 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2196 | 0x17006C94 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2197 | 0x17006C95 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2198 | 0x17006C96 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2199 | 0x17006C97 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2200 | 0x17006C98 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2201 | 0x17006C99 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2202 | 0x17006C9A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2203 | 0x17006C9B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2204 | 0x17006C9C | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SFLASH_PUBLIC_KEY2205 | 0x17006C9D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2206 | 0x17006C9E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2207 | 0x17006C9F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2208 | 0x17006CA0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2209 | 0x17006CA1 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2210 | 0x17006CA2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2211 | 0x17006CA3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2212 | 0x17006CA4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2213 | 0x17006CA5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2214 | 0x17006CA6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2215 | 0x17006CA7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2216 | 0x17006CA8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2217 | 0x17006CA9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2218 | 0x17006CAA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2219 | 0x17006CAB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2220 | 0x17006CAC | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2221 | 0x17006CAD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2222 | 0x17006CAE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2223 | 0x17006CAF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2224 | 0x17006CB0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2225 | 0x17006CB1 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2226 | 0x17006CB2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2227 | 0x17006CB3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2228 | 0x17006CB4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2229 | 0x17006CB5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2230 | 0x17006CB6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2231 | 0x17006CB7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2232 | 0x17006CB8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2233 | 0x17006CB9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2234 | 0x17006CBA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2235 | 0x17006CBB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2236 | 0x17006CBC | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SFLASH_PUBLIC_KEY2237 | 0x17006CBD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2238 | 0x17006CBE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2239 | 0x17006CBF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2240 | 0x17006CC0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2241 | 0x17006CC1 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2242 | 0x17006CC2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2243 | 0x17006CC3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2244 | 0x17006CC4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2245 | 0x17006CC5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2246 | 0x17006CC6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2247 | 0x17006CC7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2248 | 0x17006CC8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2249 | 0x17006CC9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2250 | 0x17006CCA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2251 | 0x17006CCB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2252 | 0x17006CCC | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2253 | 0x17006CCD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2254 | 0x17006CCE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2255 | 0x17006CCF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2256 | 0x17006CD0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2257 | 0x17006CD1 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2258 | 0x17006CD2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2259 | 0x17006CD3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2260 | 0x17006CD4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2261 | 0x17006CD5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2262 | 0x17006CD6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2263 | 0x17006CD7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2264 | 0x17006CD8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2265 | 0x17006CD9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2266 | 0x17006CDA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2267 | 0x17006CDB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2268 | 0x17006CDC | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SFLASH_PUBLIC_KEY2269 | 0x17006CDD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2270 | 0x17006CDE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2271 | 0x17006CDF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2272 | 0x17006CE0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2273 | 0x17006CE1 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2274 | 0x17006CE2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2275 | 0x17006CE3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2276 | 0x17006CE4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2277 | 0x17006CE5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2278 | 0x17006CE6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2279 | 0x17006CE7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2280 | 0x17006CE8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2281 | 0x17006CE9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2282 | 0x17006CEA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2283 | 0x17006CEB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2284 | 0x17006CEC | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2285 | 0x17006CED | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2286 | 0x17006CEE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2287 | 0x17006CEF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2288 | 0x17006CF0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2289 | 0x17006CF1 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2290 | 0x17006CF2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2291 | 0x17006CF3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2292 | 0x17006CF4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2293 | 0x17006CF5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2294 | 0x17006CF6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2295 | 0x17006CF7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2296 | 0x17006CF8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2297 | 0x17006CF9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2298 | 0x17006CFA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2299 | 0x17006CFB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2300 | 0x17006CFC | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SFLASH_PUBLIC_KEY2301 | 0x17006CFD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2302 | 0x17006CFE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2303 | 0x17006CFF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2304 | 0x17006D00 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2305 | 0x17006D01 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2306 | 0x17006D02 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2307 | 0x17006D03 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2308 | 0x17006D04 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2309 | 0x17006D05 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2310 | 0x17006D06 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2311 | 0x17006D07 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2312 | 0x17006D08 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2313 | 0x17006D09 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2314 | 0x17006D0A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2315 | 0x17006D0B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2316 | 0x17006D0C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2317 | 0x17006D0D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2318 | 0x17006D0E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2319 | 0x17006D0F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2320 | 0x17006D10 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2321 | 0x17006D11 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2322 | 0x17006D12 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2323 | 0x17006D13 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2324 | 0x17006D14 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2325 | 0x17006D15 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2326 | 0x17006D16 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2327 | 0x17006D17 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2328 | 0x17006D18 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2329 | 0x17006D19 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2330 | 0x17006D1A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2331 | 0x17006D1B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2332 | 0x17006D1C | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SFLASH_PUBLIC_KEY2333 | 0x17006D1D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2334 | 0x17006D1E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2335 | 0x17006D1F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2336 | 0x17006D20 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2337 | 0x17006D21 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2338 | 0x17006D22 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2339 | 0x17006D23 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2340 | 0x17006D24 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2341 | 0x17006D25 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2342 | 0x17006D26 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2343 | 0x17006D27 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2344 | 0x17006D28 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2345 | 0x17006D29 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2346 | 0x17006D2A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2347 | 0x17006D2B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2348 | 0x17006D2C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2349 | 0x17006D2D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2350 | 0x17006D2E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2351 | 0x17006D2F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2352 | 0x17006D30 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2353 | 0x17006D31 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2354 | 0x17006D32 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2355 | 0x17006D33 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2356 | 0x17006D34 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2357 | 0x17006D35 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2358 | 0x17006D36 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2359 | 0x17006D37 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2360 | 0x17006D38 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2361 | 0x17006D39 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2362 | 0x17006D3A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2363 | 0x17006D3B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2364 | 0x17006D3C | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SFLASH_PUBLIC_KEY2365 | 0x17006D3D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2366 | 0x17006D3E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2367 | 0x17006D3F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2368 | 0x17006D40 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2369 | 0x17006D41 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2370 | 0x17006D42 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2371 | 0x17006D43 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2372 | 0x17006D44 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2373 | 0x17006D45 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2374 | 0x17006D46 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2375 | 0x17006D47 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2376 | 0x17006D48 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2377 | 0x17006D49 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2378 | 0x17006D4A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2379 | 0x17006D4B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2380 | 0x17006D4C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2381 | 0x17006D4D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2382 | 0x17006D4E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2383 | 0x17006D4F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2384 | 0x17006D50 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2385 | 0x17006D51 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2386 | 0x17006D52 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2387 | 0x17006D53 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2388 | 0x17006D54 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2389 | 0x17006D55 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2390 | 0x17006D56 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2391 | 0x17006D57 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2392 | 0x17006D58 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2393 | 0x17006D59 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2394 | 0x17006D5A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2395 | 0x17006D5B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2396 | 0x17006D5C | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SFLASH_PUBLIC_KEY2397 | 0x17006D5D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2398 | 0x17006D5E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2399 | 0x17006D5F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2400 | 0x17006D60 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2401 | 0x17006D61 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2402 | 0x17006D62 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2403 | 0x17006D63 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2404 | 0x17006D64 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2405 | 0x17006D65 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2406 | 0x17006D66 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2407 | 0x17006D67 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2408 | 0x17006D68 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2409 | 0x17006D69 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2410 | 0x17006D6A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2411 | 0x17006D6B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2412 | 0x17006D6C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2413 | 0x17006D6D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2414 | 0x17006D6E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2415 | 0x17006D6F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2416 | 0x17006D70 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2417 | 0x17006D71 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2418 | 0x17006D72 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2419 | 0x17006D73 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2420 | 0x17006D74 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2421 | 0x17006D75 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2422 | 0x17006D76 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2423 | 0x17006D77 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2424 | 0x17006D78 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2425 | 0x17006D79 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2426 | 0x17006D7A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2427 | 0x17006D7B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2428 | 0x17006D7C | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SFLASH_PUBLIC_KEY2429 | 0x17006D7D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2430 | 0x17006D7E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2431 | 0x17006D7F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2432 | 0x17006D80 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2433 | 0x17006D81 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2434 | 0x17006D82 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2435 | 0x17006D83 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2436 | 0x17006D84 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2437 | 0x17006D85 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2438 | 0x17006D86 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2439 | 0x17006D87 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2440 | 0x17006D88 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2441 | 0x17006D89 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2442 | 0x17006D8A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2443 | 0x17006D8B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2444 | 0x17006D8C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2445 | 0x17006D8D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2446 | 0x17006D8E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2447 | 0x17006D8F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2448 | 0x17006D90 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2449 | 0x17006D91 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2450 | 0x17006D92 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2451 | 0x17006D93 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2452 | 0x17006D94 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2453 | 0x17006D95 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2454 | 0x17006D96 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2455 | 0x17006D97 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2456 | 0x17006D98 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2457 | 0x17006D99 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2458 | 0x17006D9A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2459 | 0x17006D9B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2460 | 0x17006D9C | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SFLASH_PUBLIC_KEY2461 | 0x17006D9D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2462 | 0x17006D9E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2463 | 0x17006D9F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2464 | 0x17006DA0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2465 | 0x17006DA1 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2466 | 0x17006DA2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2467 | 0x17006DA3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2468 | 0x17006DA4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2469 | 0x17006DA5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2470 | 0x17006DA6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2471 | 0x17006DA7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2472 | 0x17006DA8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2473 | 0x17006DA9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2474 | 0x17006DAA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2475 | 0x17006DAB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2476 | 0x17006DAC | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2477 | 0x17006DAD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2478 | 0x17006DAE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2479 | 0x17006DAF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2480 | 0x17006DB0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2481 | 0x17006DB1 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2482 | 0x17006DB2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2483 | 0x17006DB3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2484 | 0x17006DB4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2485 | 0x17006DB5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2486 | 0x17006DB6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2487 | 0x17006DB7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2488 | 0x17006DB8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2489 | 0x17006DB9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2490 | 0x17006DBA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2491 | 0x17006DBB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2492 | 0x17006DBC | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SFLASH_PUBLIC_KEY2493 | 0x17006DBD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2494 | 0x17006DBE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2495 | 0x17006DBF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2496 | 0x17006DC0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2497 | 0x17006DC1 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2498 | 0x17006DC2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2499 | 0x17006DC3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2500 | 0x17006DC4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2501 | 0x17006DC5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2502 | 0x17006DC6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2503 | 0x17006DC7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2504 | 0x17006DC8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2505 | 0x17006DC9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2506 | 0x17006DCA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2507 | 0x17006DCB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2508 | 0x17006DCC | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2509 | 0x17006DCD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2510 | 0x17006DCE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2511 | 0x17006DCF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2512 | 0x17006DD0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2513 | 0x17006DD1 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2514 | 0x17006DD2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2515 | 0x17006DD3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2516 | 0x17006DD4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2517 | 0x17006DD5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2518 | 0x17006DD6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2519 | 0x17006DD7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2520 | 0x17006DD8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2521 | 0x17006DD9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2522 | 0x17006DDA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2523 | 0x17006DDB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2524 | 0x17006DDC | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SFLASH_PUBLIC_KEY2525 | 0x17006DDD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2526 | 0x17006DDE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2527 | 0x17006DDF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2528 | 0x17006DE0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2529 | 0x17006DE1 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2530 | 0x17006DE2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2531 | 0x17006DE3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2532 | 0x17006DE4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2533 | 0x17006DE5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2534 | 0x17006DE6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2535 | 0x17006DE7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2536 | 0x17006DE8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2537 | 0x17006DE9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2538 | 0x17006DEA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2539 | 0x17006DEB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2540 | 0x17006DEC | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2541 | 0x17006DED | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2542 | 0x17006DEE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2543 | 0x17006DEF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2544 | 0x17006DF0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2545 | 0x17006DF1 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2546 | 0x17006DF2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2547 | 0x17006DF3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2548 | 0x17006DF4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2549 | 0x17006DF5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2550 | 0x17006DF6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2551 | 0x17006DF7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2552 | 0x17006DF8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2553 | 0x17006DF9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2554 | 0x17006DFA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2555 | 0x17006DFB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2556 | 0x17006DFC | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SFLASH_PUBLIC_KEY2557 | 0x17006DFD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2558 | 0x17006DFE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2559 | 0x17006DFF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2560 | 0x17006E00 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2561 | 0x17006E01 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2562 | 0x17006E02 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2563 | 0x17006E03 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2564 | 0x17006E04 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2565 | 0x17006E05 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2566 | 0x17006E06 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2567 | 0x17006E07 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2568 | 0x17006E08 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2569 | 0x17006E09 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2570 | 0x17006E0A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2571 | 0x17006E0B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2572 | 0x17006E0C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2573 | 0x17006E0D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2574 | 0x17006E0E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2575 | 0x17006E0F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2576 | 0x17006E10 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2577 | 0x17006E11 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2578 | 0x17006E12 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2579 | 0x17006E13 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2580 | 0x17006E14 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2581 | 0x17006E15 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2582 | 0x17006E16 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2583 | 0x17006E17 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2584 | 0x17006E18 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2585 | 0x17006E19 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2586 | 0x17006E1A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2587 | 0x17006E1B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2588 | 0x17006E1C | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SFLASH_PUBLIC_KEY2589 | 0x17006E1D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2590 | 0x17006E1E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2591 | 0x17006E1F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2592 | 0x17006E20 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2593 | 0x17006E21 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2594 | 0x17006E22 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2595 | 0x17006E23 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2596 | 0x17006E24 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2597 | 0x17006E25 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2598 | 0x17006E26 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2599 | 0x17006E27 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2600 | 0x17006E28 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2601 | 0x17006E29 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2602 | 0x17006E2A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2603 | 0x17006E2B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2604 | 0x17006E2C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2605 | 0x17006E2D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2606 | 0x17006E2E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2607 | 0x17006E2F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2608 | 0x17006E30 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2609 | 0x17006E31 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2610 | 0x17006E32 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2611 | 0x17006E33 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2612 | 0x17006E34 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2613 | 0x17006E35 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2614 | 0x17006E36 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2615 | 0x17006E37 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2616 | 0x17006E38 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2617 | 0x17006E39 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2618 | 0x17006E3A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2619 | 0x17006E3B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2620 | 0x17006E3C | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SFLASH_PUBLIC_KEY2621 | 0x17006E3D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2622 | 0x17006E3E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2623 | 0x17006E3F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2624 | 0x17006E40 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2625 | 0x17006E41 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2626 | 0x17006E42 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2627 | 0x17006E43 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2628 | 0x17006E44 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2629 | 0x17006E45 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2630 | 0x17006E46 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2631 | 0x17006E47 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2632 | 0x17006E48 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2633 | 0x17006E49 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2634 | 0x17006E4A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2635 | 0x17006E4B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2636 | 0x17006E4C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2637 | 0x17006E4D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2638 | 0x17006E4E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2639 | 0x17006E4F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2640 | 0x17006E50 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2641 | 0x17006E51 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2642 | 0x17006E52 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2643 | 0x17006E53 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2644 | 0x17006E54 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2645 | 0x17006E55 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2646 | 0x17006E56 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2647 | 0x17006E57 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2648 | 0x17006E58 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2649 | 0x17006E59 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2650 | 0x17006E5A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2651 | 0x17006E5B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2652 | 0x17006E5C | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SFLASH_PUBLIC_KEY2653 | 0x17006E5D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2654 | 0x17006E5E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2655 | 0x17006E5F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2656 | 0x17006E60 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2657 | 0x17006E61 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2658 | 0x17006E62 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2659 | 0x17006E63 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2660 | 0x17006E64 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2661 | 0x17006E65 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2662 | 0x17006E66 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2663 | 0x17006E67 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2664 | 0x17006E68 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2665 | 0x17006E69 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2666 | 0x17006E6A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2667 | 0x17006E6B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2668 | 0x17006E6C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2669 | 0x17006E6D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2670 | 0x17006E6E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2671 | 0x17006E6F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2672 | 0x17006E70 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2673 | 0x17006E71 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2674 | 0x17006E72 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2675 | 0x17006E73 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2676 | 0x17006E74 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2677 | 0x17006E75 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2678 | 0x17006E76 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2679 | 0x17006E77 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2680 | 0x17006E78 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2681 | 0x17006E79 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2682 | 0x17006E7A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2683 | 0x17006E7B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2684 | 0x17006E7C | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SFLASH_PUBLIC_KEY2685 | 0x17006E7D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2686 | 0x17006E7E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2687 | 0x17006E7F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2688 | 0x17006E80 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2689 | 0x17006E81 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2690 | 0x17006E82 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2691 | 0x17006E83 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2692 | 0x17006E84 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2693 | 0x17006E85 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2694 | 0x17006E86 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2695 | 0x17006E87 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2696 | 0x17006E88 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2697 | 0x17006E89 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2698 | 0x17006E8A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2699 | 0x17006E8B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2700 | 0x17006E8C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2701 | 0x17006E8D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2702 | 0x17006E8E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2703 | 0x17006E8F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2704 | 0x17006E90 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2705 | 0x17006E91 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2706 | 0x17006E92 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2707 | 0x17006E93 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2708 | 0x17006E94 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2709 | 0x17006E95 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2710 | 0x17006E96 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2711 | 0x17006E97 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2712 | 0x17006E98 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2713 | 0x17006E99 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2714 | 0x17006E9A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2715 | 0x17006E9B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2716 | 0x17006E9C | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SFLASH_PUBLIC_KEY2717 | 0x17006E9D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2718 | 0x17006E9E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2719 | 0x17006E9F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2720 | 0x17006EA0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2721 | 0x17006EA1 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2722 | 0x17006EA2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2723 | 0x17006EA3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2724 | 0x17006EA4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2725 | 0x17006EA5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2726 | 0x17006EA6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2727 | 0x17006EA7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2728 | 0x17006EA8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2729 | 0x17006EA9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2730 | 0x17006EAA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2731 | 0x17006EAB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2732 | 0x17006EAC | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2733 | 0x17006EAD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2734 | 0x17006EAE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2735 | 0x17006EAF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2736 | 0x17006EB0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2737 | 0x17006EB1 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2738 | 0x17006EB2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2739 | 0x17006EB3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2740 | 0x17006EB4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2741 | 0x17006EB5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2742 | 0x17006EB6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2743 | 0x17006EB7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2744 | 0x17006EB8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2745 | 0x17006EB9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2746 | 0x17006EBA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2747 | 0x17006EBB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2748 | 0x17006EBC | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SFLASH_PUBLIC_KEY2749 | 0x17006EBD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2750 | 0x17006EBE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2751 | 0x17006EBF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2752 | 0x17006EC0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2753 | 0x17006EC1 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2754 | 0x17006EC2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2755 | 0x17006EC3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2756 | 0x17006EC4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2757 | 0x17006EC5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2758 | 0x17006EC6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2759 | 0x17006EC7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2760 | 0x17006EC8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2761 | 0x17006EC9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2762 | 0x17006ECA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2763 | 0x17006ECB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2764 | 0x17006ECC | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2765 | 0x17006ECD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2766 | 0x17006ECE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2767 | 0x17006ECF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2768 | 0x17006ED0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2769 | 0x17006ED1 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2770 | 0x17006ED2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2771 | 0x17006ED3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2772 | 0x17006ED4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2773 | 0x17006ED5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2774 | 0x17006ED6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2775 | 0x17006ED7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2776 | 0x17006ED8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2777 | 0x17006ED9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2778 | 0x17006EDA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2779 | 0x17006EDB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2780 | 0x17006EDC | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SFLASH_PUBLIC_KEY2781 | 0x17006EDD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2782 | 0x17006EDE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2783 | 0x17006EDF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2784 | 0x17006EE0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2785 | 0x17006EE1 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2786 | 0x17006EE2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2787 | 0x17006EE3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2788 | 0x17006EE4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2789 | 0x17006EE5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2790 | 0x17006EE6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2791 | 0x17006EE7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2792 | 0x17006EE8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2793 | 0x17006EE9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2794 | 0x17006EEA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2795 | 0x17006EEB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2796 | 0x17006EEC | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2797 | 0x17006EED | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2798 | 0x17006EEE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2799 | 0x17006EEF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2800 | 0x17006EF0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2801 | 0x17006EF1 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2802 | 0x17006EF2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2803 | 0x17006EF3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2804 | 0x17006EF4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2805 | 0x17006EF5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2806 | 0x17006EF6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2807 | 0x17006EF7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2808 | 0x17006EF8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2809 | 0x17006EF9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2810 | 0x17006EFA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2811 | 0x17006EFB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2812 | 0x17006EFC | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SFLASH_PUBLIC_KEY2813 | 0x17006EFD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2814 | 0x17006EFE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2815 | 0x17006EFF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2816 | 0x17006F00 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2817 | 0x17006F01 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2818 | 0x17006F02 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2819 | 0x17006F03 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2820 | 0x17006F04 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2821 | 0x17006F05 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2822 | 0x17006F06 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2823 | 0x17006F07 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2824 | 0x17006F08 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2825 | 0x17006F09 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2826 | 0x17006F0A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2827 | 0x17006F0B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2828 | 0x17006F0C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2829 | 0x17006F0D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2830 | 0x17006F0E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2831 | 0x17006F0F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2832 | 0x17006F10 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2833 | 0x17006F11 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2834 | 0x17006F12 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2835 | 0x17006F13 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2836 | 0x17006F14 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2837 | 0x17006F15 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2838 | 0x17006F16 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2839 | 0x17006F17 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2840 | 0x17006F18 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2841 | 0x17006F19 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2842 | 0x17006F1A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2843 | 0x17006F1B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2844 | 0x17006F1C | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SFLASH_PUBLIC_KEY2845 | 0x17006F1D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2846 | 0x17006F1E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2847 | 0x17006F1F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2848 | 0x17006F20 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2849 | 0x17006F21 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2850 | 0x17006F22 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2851 | 0x17006F23 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2852 | 0x17006F24 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2853 | 0x17006F25 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2854 | 0x17006F26 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2855 | 0x17006F27 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2856 | 0x17006F28 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2857 | 0x17006F29 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2858 | 0x17006F2A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2859 | 0x17006F2B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2860 | 0x17006F2C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2861 | 0x17006F2D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2862 | 0x17006F2E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2863 | 0x17006F2F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2864 | 0x17006F30 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2865 | 0x17006F31 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2866 | 0x17006F32 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2867 | 0x17006F33 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2868 | 0x17006F34 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2869 | 0x17006F35 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2870 | 0x17006F36 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2871 | 0x17006F37 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2872 | 0x17006F38 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2873 | 0x17006F39 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2874 | 0x17006F3A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2875 | 0x17006F3B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2876 | 0x17006F3C | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SFLASH_PUBLIC_KEY2877 | 0x17006F3D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2878 | 0x17006F3E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2879 | 0x17006F3F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2880 | 0x17006F40 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2881 | 0x17006F41 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2882 | 0x17006F42 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2883 | 0x17006F43 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2884 | 0x17006F44 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2885 | 0x17006F45 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2886 | 0x17006F46 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2887 | 0x17006F47 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2888 | 0x17006F48 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2889 | 0x17006F49 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2890 | 0x17006F4A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2891 | 0x17006F4B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2892 | 0x17006F4C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2893 | 0x17006F4D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2894 | 0x17006F4E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2895 | 0x17006F4F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2896 | 0x17006F50 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2897 | 0x17006F51 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2898 | 0x17006F52 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2899 | 0x17006F53 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2900 | 0x17006F54 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2901 | 0x17006F55 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2902 | 0x17006F56 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2903 | 0x17006F57 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2904 | 0x17006F58 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2905 | 0x17006F59 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2906 | 0x17006F5A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2907 | 0x17006F5B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2908 | 0x17006F5C | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SFLASH_PUBLIC_KEY2909 | 0x17006F5D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2910 | 0x17006F5E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2911 | 0x17006F5F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2912 | 0x17006F60 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2913 | 0x17006F61 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2914 | 0x17006F62 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2915 | 0x17006F63 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2916 | 0x17006F64 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2917 | 0x17006F65 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2918 | 0x17006F66 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2919 | 0x17006F67 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2920 | 0x17006F68 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2921 | 0x17006F69 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2922 | 0x17006F6A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2923 | 0x17006F6B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2924 | 0x17006F6C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2925 | 0x17006F6D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2926 | 0x17006F6E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2927 | 0x17006F6F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2928 | 0x17006F70 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2929 | 0x17006F71 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2930 | 0x17006F72 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2931 | 0x17006F73 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2932 | 0x17006F74 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2933 | 0x17006F75 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2934 | 0x17006F76 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2935 | 0x17006F77 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2936 | 0x17006F78 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2937 | 0x17006F79 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2938 | 0x17006F7A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2939 | 0x17006F7B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2940 | 0x17006F7C | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SFLASH_PUBLIC_KEY2941 | 0x17006F7D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2942 | 0x17006F7E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2943 | 0x17006F7F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2944 | 0x17006F80 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2945 | 0x17006F81 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2946 | 0x17006F82 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2947 | 0x17006F83 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2948 | 0x17006F84 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2949 | 0x17006F85 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2950 | 0x17006F86 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2951 | 0x17006F87 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2952 | 0x17006F88 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2953 | 0x17006F89 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2954 | 0x17006F8A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2955 | 0x17006F8B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2956 | 0x17006F8C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2957 | 0x17006F8D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2958 | 0x17006F8E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2959 | 0x17006F8F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2960 | 0x17006F90 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2961 | 0x17006F91 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2962 | 0x17006F92 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2963 | 0x17006F93 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2964 | 0x17006F94 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2965 | 0x17006F95 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2966 | 0x17006F96 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2967 | 0x17006F97 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2968 | 0x17006F98 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2969 | 0x17006F99 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2970 | 0x17006F9A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2971 | 0x17006F9B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2972 | 0x17006F9C | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SFLASH_PUBLIC_KEY2973 | 0x17006F9D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2974 | 0x17006F9E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2975 | 0x17006F9F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2976 | 0x17006FA0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2977 | 0x17006FA1 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2978 | 0x17006FA2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2979 | 0x17006FA3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2980 | 0x17006FA4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2981 | 0x17006FA5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2982 | 0x17006FA6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2983 | 0x17006FA7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2984 | 0x17006FA8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2985 | 0x17006FA9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2986 | 0x17006FAA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2987 | 0x17006FAB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2988 | 0x17006FAC | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2989 | 0x17006FAD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2990 | 0x17006FAE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2991 | 0x17006FAF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2992 | 0x17006FB0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2993 | 0x17006FB1 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2994 | 0x17006FB2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2995 | 0x17006FB3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2996 | 0x17006FB4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2997 | 0x17006FB5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2998 | 0x17006FB6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2999 | 0x17006FB7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3000 | 0x17006FB8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3001 | 0x17006FB9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3002 | 0x17006FBA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3003 | 0x17006FBB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3004 | 0x17006FBC | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SFLASH_PUBLIC_KEY3005 | 0x17006FBD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3006 | 0x17006FBE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3007 | 0x17006FBF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3008 | 0x17006FC0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3009 | 0x17006FC1 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3010 | 0x17006FC2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3011 | 0x17006FC3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3012 | 0x17006FC4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3013 | 0x17006FC5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3014 | 0x17006FC6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3015 | 0x17006FC7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3016 | 0x17006FC8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3017 | 0x17006FC9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3018 | 0x17006FCA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3019 | 0x17006FCB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3020 | 0x17006FCC | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3021 | 0x17006FCD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3022 | 0x17006FCE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3023 | 0x17006FCF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3024 | 0x17006FD0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3025 | 0x17006FD1 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3026 | 0x17006FD2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3027 | 0x17006FD3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3028 | 0x17006FD4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3029 | 0x17006FD5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3030 | 0x17006FD6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3031 | 0x17006FD7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3032 | 0x17006FD8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3033 | 0x17006FD9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3034 | 0x17006FDA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3035 | 0x17006FDB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3036 | 0x17006FDC | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SFLASH_PUBLIC_KEY3037 | 0x17006FDD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3038 | 0x17006FDE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3039 | 0x17006FDF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3040 | 0x17006FE0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3041 | 0x17006FE1 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3042 | 0x17006FE2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3043 | 0x17006FE3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3044 | 0x17006FE4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3045 | 0x17006FE5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3046 | 0x17006FE6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3047 | 0x17006FE7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3048 | 0x17006FE8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3049 | 0x17006FE9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3050 | 0x17006FEA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3051 | 0x17006FEB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3052 | 0x17006FEC | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3053 | 0x17006FED | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3054 | 0x17006FEE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3055 | 0x17006FEF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3056 | 0x17006FF0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3057 | 0x17006FF1 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3058 | 0x17006FF2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3059 | 0x17006FF3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3060 | 0x17006FF4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3061 | 0x17006FF5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3062 | 0x17006FF6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3063 | 0x17006FF7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3064 | 0x17006FF8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3065 | 0x17006FF9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3066 | 0x17006FFA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3067 | 0x17006FFB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3068 | 0x17006FFC | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SFLASH_PUBLIC_KEY3069 | 0x17006FFD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3070 | 0x17006FFE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3071 | 0x17006FFF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_APP_PROT_SETTINGS0 | 0x17007600 | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS1 | 0x17007604 | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS2 | 0x17007608 | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS3 | 0x1700760C | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS4 | 0x17007610 | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS5 | 0x17007614 | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS6 | 0x17007618 | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS7 | 0x1700761C | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS8 | 0x17007620 | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS9 | 0x17007624 | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS10 | 0x17007628 | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS11 | 0x1700762C | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS12 | 0x17007630 | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS13 | 0x17007634 | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS14 | 0x17007638 | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS15 | 0x1700763C | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS16 | 0x17007640 | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS17 | 0x17007644 | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS18 | 0x17007648 | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS19 | 0x1700764C | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS20 | 0x17007650 | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS21 | 0x17007654 | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS22 | 0x17007658 | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS23 | 0x1700765C | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS24 | 0x17007660 | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS25 | 0x17007664 | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS26 | 0x17007668 | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS27 | 0x1700766C | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS28 | 0x17007670 | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS29 | 0x17007674 | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS30 | 0x17007678 | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS31 | 0x1700767C | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS32 | 0x17007680 | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS33 | 0x17007684 | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS34 | 0x17007688 | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS35 | 0x1700768C | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS36 | 0x17007690 | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS37 | 0x17007694 | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS38 | 0x17007698 | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS39 | 0x1700769C | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS40 | 0x170076A0 | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS41 | 0x170076A4 | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS42 | 0x170076A8 | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS43 | 0x170076AC | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS44 | 0x170076B0 | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS45 | 0x170076B4 | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS46 | 0x170076B8 | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS47 | 0x170076BC | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS48 | 0x170076C0 | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS49 | 0x170076C4 | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS50 | 0x170076C8 | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS51 | 0x170076CC | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS52 | 0x170076D0 | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS53 | 0x170076D4 | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS54 | 0x170076D8 | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS55 | 0x170076DC | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS56 | 0x170076E0 | FULL | Application protection settings (4*128=512 bytes) |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SFLASH_APP_PROT_SETTINGS57 | 0x170076E4 | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS58 | 0x170076E8 | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS59 | 0x170076EC | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS60 | 0x170076F0 | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS61 | 0x170076F4 | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS62 | 0x170076F8 | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS63 | 0x170076FC | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS64 | 0x17007700 | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS65 | 0x17007704 | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS66 | 0x17007708 | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS67 | 0x1700770C | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS68 | 0x17007710 | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS69 | 0x17007714 | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS70 | 0x17007718 | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS71 | 0x1700771C | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS72 | 0x17007720 | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS73 | 0x17007724 | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS74 | 0x17007728 | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS75 | 0x1700772C | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS76 | 0x17007730 | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS77 | 0x17007734 | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS78 | 0x17007738 | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS79 | 0x1700773C | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS80 | 0x17007740 | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS81 | 0x17007744 | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS82 | 0x17007748 | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS83 | 0x1700774C | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS84 | 0x17007750 | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS85 | 0x17007754 | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS86 | 0x17007758 | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS87 | 0x1700775C | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS88 | 0x17007760 | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS89 | 0x17007764 | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS90 | 0x17007768 | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS91 | 0x1700776C | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS92 | 0x17007770 | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS93 | 0x17007774 | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS94 | 0x17007778 | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS95 | 0x1700777C | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS96 | 0x17007780 | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS97 | 0x17007784 | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS98 | 0x17007788 | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS99 | 0x1700778C | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS100 | 0x17007790 | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS101 | 0x17007794 | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS102 | 0x17007798 | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS103 | 0x1700779C | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS104 | 0x170077A0 | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS105 | 0x170077A4 | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS106 | 0x170077A8 | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS107 | 0x170077AC | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS108 | 0x170077B0 | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS109 | 0x170077B4 | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS110 | 0x170077B8 | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS111 | 0x170077BC | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS112 | 0x170077C0 | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS113 | 0x170077C4 | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS114 | 0x170077C8 | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS115 | 0x170077CC | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS116 | 0x170077D0 | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS117 | 0x170077D4 | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS118 | 0x170077D8 | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS119 | 0x170077DC | FULL | Application protection settings (4*128=512 bytes) |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SFLASH_APP_PROT_SETTINGS120 | 0x170077E0 | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS121 | 0x170077E4 | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS122 | 0x170077E8 | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS123 | 0x170077EC | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS124 | 0x170077F0 | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS125 | 0x170077F4 | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS126 | 0x170077F8 | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS127 | 0x170077FC | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_TOC2_OBJECT_SIZE | 0x17007C00 | FULL | Object size in bytes for CRC calculation starting from offset 0x00 |
| SFLASH_TOC2_MAGIC_NUMBER | 0x17007C04 | FULL | Magic number(0x01211220) |
| SFLASH_TOC2_SMIF_CFG_STRUCT_ADDR | 0x17007C08 | FULL | Null terminated table of pointers representing the SMIF configuration structure |
| SFLASH_TOC2_FIRST_USER_APP_ADDR | 0x17007C0C | FULL | Address of First User Application Object |
| SFLASH_TOC2_FIRST_USER_APP_FORMAT | 0x17007C10 | FULL | Format of First User Application Object. 0 - Basic, 1 - Cypress standard & 2 - Simplified |
| SFLASH_TOC2_SECOND_USER_APP_ADDR | 0x17007C14 | FULL | Address of Second User Application Object |
| SFLASH_TOC2_SECOND_USER_APP_FORMAT | 0x17007C18 | FULL | Format of Second User Application Object. 0 - Basic, 1 - Cypress standard & 2 - Simplified |
| SFLASH_TOC2_FIRST_CMX_1_USER_APP_ADDR | 0x17007C1C | FULL | Address of First CM4 or CM7 core1 User Application Object |
| SFLASH_TOC2_SECOND_CMX_1_USER_APP_ADDR | 0x17007C20 | FULL | Address of Second CM4 or CM7 core1 User Application Object |
| SFLASH_TOC2_FIRST_CMX_2_USER_APP_ADDR | 0x17007C24 | FULL | Address of First CM4 or CM7 core2 User Application Object |
| SFLASH_TOC2_SECOND_CMX_2_USER_APP_ADDR | 0x17007C28 | FULL | Address of Second CM4 or CM7 core2 User Application Object |
| SFLASH_TOC2_SECURITY_UPDATES_MARKER | 0x17007CFC | FULL | Marker for Security Updates |
| SFLASH_TOC2_SHASH_OBJECTS | 0x17007D00 | FULL | Number of additional objects to be verified for SECURE_HASH |
| SFLASH_TOC2_SIGNATURE_VERIF_KEY | 0x17007D04 | FULL | Address of signature verification key (0 if none).The object is signature specific key. It is the public key in case of RSA |
| SFLASH_TOC2_APP_PROTECTION_ADDR | 0x17007D08 | FULL | Address of Application Protection |
| SFLASH_TOC2_REVISION | 0x17007DF4 | FULL | Indicates TOC2 Revision. It is not used now. |
| SFLASH_TOC2_FLAGS | 0x17007DF8 | FULL | Controls default configuration |

## 28.1 Register Details

### 28.1.1 SFLASH_SI_REVISION_ID

**Description:** Indicates Silicon Revision ID of the device
**Address:** 0x17000001
**Offset:** 0x1
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Used to store Silicon Revision ID
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | SI_REVISION_ID [7:0] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | SI_REVISION_ID | RW | | X | Silicon Revision ID |

### 28.1.2 SFLASH_SILICON_ID

**Description:** Indicates Silicon ID of the device
**Address:** 0x17000002
**Offset:** 0x2
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Used to store silicon ID
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | ID [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | ID [15:8] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | ID | RW | | X | Silicon ID |

### 28.1.3 SFLASH_SFLASH_SVN

**Description:** SFLASH Subversion
**Address:** 0x170000A8
**Offset:** 0xA8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA32 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA32 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA32 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA32 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | DATA32 | RW | | 0 | SFLASH Subversion |

### 28.1.4 SFLASH_FB_FLAGS

**Description:** Flash boot flags
**Address:** 0x170001FC
**Offset:** 0x1FC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Flash boot flags are used by the flash boot. The default value is 0x0000_0015
**Default:** 0x15

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:6] | | FB_RSA4K_CTL [5:4] | | FB_RSA3K_CTL [3:2] | | FB_PIN_CTL [1:0] | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:1 | FB_PIN_CTL | RW | | 1 | Determines toggling a GPIO pin at the start and end of Flash boot<br>2 = Enable toggling a GPIO pin at the start and end of Flash boot<br>Others = Disable toggling a GPIO pin at the start and end of Flash boot<br>Default value = 1. |
| 2:3 | FB_RSA3K_CTL | RW | | 1 | Determines if RSA-3K is supported.<br>2 = RSA-3K is supported. RSA public key modulo length should be in range 512 to 3072 bit. The field FB_RSA4K_CTL must be set to 0.<br>Others = RSA-3K is not supported. RSA public key modulo length should be in range 512 to 2048 bit.<br>Default value = 1. |
| 4:5 | FB_RSA4K_CTL | RW | | 1 | Determines if RSA-4K is supported.<br>2 = RSA-4K is supported. RSA public key modulo length should be in range 512 to 4096 bit. RSA4K already includes RSA3K option. The field FB_RSA3K_CTL must be set to 0.<br>Others = RSA-4K is not supported.<br>Default value = 1. |

### 28.1.5 SFLASH_EPASS_TEMP_TRIM_TEMP_ROOMSORT

**Description:** On Chip temperature measured using external currents and external ADC at ROOM
**Address:** 0x1700064E
**Offset:** 0x64E
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Temperature calibration data for EPASS Temperature sensor
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA16 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA16 [15:8] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | DATA16 | RW | | X | On Chip temperature measured using external currents and external ADC at ROOM |

### 28.1.6 SFLASH_EPASS_TEMP_TRIM_DIODE_ROOMSORT

**Description:** Temperature sensor calibration data for VDDA=3.3V, Temperature sensor diode voltage at ROOM
**Address:** 0x17000650
**Offset:** 0x650
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Temperature calibration data for EPASS Temperature sensor
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA16 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA16 [15:8] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | DATA16 | RW | | X | Temperature sensor calibration data for VDDA=3.3V, Temperature sensor diode voltage at ROOM |

### 28.1.7 SFLASH_EPASS_TEMP_TRIM_VBG_ROOMSORT

**Description:** Temperature sensor calibration data for VDDA=3.3V, Bandgap voltage at ROOM
**Address:** 0x17000652
**Offset:** 0x652
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Temperature calibration data for EPASS Temperature sensor
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA16 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA16 [15:8] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | DATA16 | RW | | X | Temperature sensor calibration data for VDDA=3.3V, Bandgap voltage at ROOM |

### 28.1.8 SFLASH_EPASS_TEMP_TRIM_TEMP_COLDSORT

**Description:** On Chip temperature measured using external currents and external ADC at COLD
**Address:** 0x17000654
**Offset:** 0x654
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Temperature calibration data for EPASS Temperature sensor
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA16 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA16 [15:8] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | DATA16 | RW | | X | On Chip temperature measured using external currents and external ADC at COLD |

### 28.1.9 SFLASH_EPASS_TEMP_TRIM_DIODE_COLDSORT

**Description:** Temperature sensor calibration data for VDDA=3.3V, Temperature sensor diode voltage at COLD
**Address:** 0x17000656
**Offset:** 0x656
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Temperature calibration data for EPASS Temperature sensor
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA16 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA16 [15:8] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | DATA16 | RW | | X | Temperature sensor calibration data for VDDA=3.3V, Temperature sensor diode voltage at COLD |

### 28.1.10 SFLASH_EPASS_TEMP_TRIM_VBG_COLDSORT

**Description:** Temperature sensor calibration data for VDDA=3.3V, Bandgap voltage at COLD
**Address:** 0x17000658
**Offset:** 0x658
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Temperature calibration data for EPASS Temperature sensor
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA16 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA16 [15:8] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | DATA16 | RW | | X | Temperature sensor calibration data for VDDA=3.3V, Bandgap voltage at COLD |

### 28.1.11 SFLASH_EPASS_TEMP_TRIM_TEMP_HOTCLASS

**Description:** On Chip temperature measured using external currents and external ADC at HOT
**Address:** 0x1700065A
**Offset:** 0x65A
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Temperature calibration data for EPASS Temperature sensor
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA16 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA16 [15:8] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | DATA16 | RW | | X | On Chip temperature measured using external currents and external ADC at HOT |

### 28.1.12 SFLASH_EPASS_TEMP_TRIM_DIODE_HOTCLASS

**Description:** Temperature sensor calibration data for VDDA=3.3V, Temperature sensor diode voltage at HOT
**Address:** 0x1700065C
**Offset:** 0x65C
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Temperature calibration data for EPASS Temperature sensor
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA16 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA16 [15:8] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | DATA16 | RW | | X | Temperature sensor calibration data for VDDA=3.3V, Temperature sensor diode voltage at HOT |

### 28.1.13 SFLASH_EPASS_TEMP_TRIM_VBG_HOTCLASS

**Description:** Temperature sensor calibration data for VDDA=3.3V, Bandgap voltage at HOT
**Address:** 0x1700065E
**Offset:** 0x65E
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Temperature calibration data for EPASS Temperature sensor
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA16 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA16 [15:8] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | DATA16 | RW | | X | Temperature sensor calibration data for VDDA=3.3V, Bandgap voltage at HOT |

### 28.1.14 SFLASH_EPASS_TEMP_TRIM_DIODE_ROOMSORT_5V

**Description:** Temperature sensor calibration data for VDDA=5V, Temperature sensor diode voltage at ROOM
**Address:** 0x1700066A
**Offset:** 0x66A
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Temperature calibration data for EPASS Temperature sensor
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA16 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA16 [15:8] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | DATA16 | RW | | X | Temperature sensor calibration data for VDDA=5V, Temperature sensor diode voltage at ROOM |

### 28.1.15 SFLASH_EPASS_TEMP_TRIM_VBG_ROOMSORT_5V

**Description:** Temperature sensor calibration data for VDDA=5V, Bandgap voltage at ROOM
**Address:** 0x1700066C
**Offset:** 0x66C
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Temperature calibration data for EPASS Temperature sensor
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA16 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA16 [15:8] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | DATA16 | RW | | X | Temperature sensor calibration data for VDDA=5V, Bandgap voltage at ROOM |

### 28.1.16 SFLASH_EPASS_TEMP_TRIM_DIODE_COLDSORT_5V

**Description:** Temperature sensor calibration data for VDDA=5V, Temperature sensor diode voltage at COLD
**Address:** 0x1700066E
**Offset:** 0x66E
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Temperature calibration data for EPASS Temperature sensor
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA16 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA16 [15:8] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | DATA16 | RW | | X | Temperature sensor calibration data for VDDA=5V, Temperature sensor diode voltage at COLD |

### 28.1.17 SFLASH_EPASS_TEMP_TRIM_VBG_COLDSORT_5V

**Description:** Temperature sensor calibration data for VDDA=5V, Bandgap voltage at COLD
**Address:** 0x17000670
**Offset:** 0x670
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Temperature calibration data for EPASS Temperature sensor
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA16 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA16 [15:8] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | DATA16 | RW | | X | Temperature sensor calibration data for VDDA=5V, Bandgap voltage at COLD |

### 28.1.18 SFLASH_EPASS_TEMP_TRIM_DIODE_HOTCLASS_5V

**Description:** Temperature sensor calibration data for VDDA=5V, Temperature sensor diode voltage at HOT
**Address:** 0x17000672
**Offset:** 0x672
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Temperature calibration data for EPASS Temperature sensor
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA16 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA16 [15:8] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | DATA16 | RW | | X | Temperature sensor calibration data for VDDA=5V, Temperature sensor diode voltage at HOT |

### 28.1.19 SFLASH_EPASS_TEMP_TRIM_VBG_HOTCLASS_5V

**Description:** Temperature sensor calibration data for VDDA=5V, Bandgap voltage at HOT
**Address:** 0x17000674
**Offset:** 0x674
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Temperature calibration data for EPASS Temperature sensor
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA16 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA16 [15:8] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | DATA16 | RW | | X | Temperature sensor calibration data for VDDA=5V, Bandgap voltage at HOT |

### 28.1.20 SFLASH_SRSS_PWR_OFFSET

**Description:** SRSS_PWR_OFFSET
**Address:** 0x17000730
**Offset:** 0x730
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:5] | | | PMIC_VADJ_OFFSET [4:0] | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:13] | | | REGHC_TRANS_VADJ_OFFSET [12:8] | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:4 | PMIC_VADJ_OFFSET | RW | | X | Die-specific offset for VADJ when using it for feedback to an external PMIC |
| 8:12 | REGHC_TRANS_VADJ_OFFSET | RW | | X | Die-specific offset for VADJ when using REGHC with external transistor |

### 28.1.21 SFLASH_SRSS_PWR_TRIM_HT_PWRSYS_INTERNAL

**Description:** Trim settings when the supply is intended to come from the internal regulators
**Address:** 0x17000734
**Offset:** 0x734
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x7000010

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:5] | | | ACT_REG_VTRIM [4:0] | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:28] | | | | DPSLP_REG_VTRIM [27:24] | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:4 | ACT_REG_VTRIM | RW | | 16 | Linear Active-Regulator voltage trim. |
| 24:27 | DPSLP_REG_VTRIM | RW | | 7 | Linear DeepSleep-Regulator voltage trim. |

### 28.1.22 SFLASH_SRSS_PWR_TRIM_HT_PWRSYS_EXTERNAL

**Description:** Trim settings for the regulators so they do not interfere with external supply
**Address:** 0x17000738
**Offset:** 0x738
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x700000D

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:5] | | | ACT_REG_VTRIM [4:0] | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:28] | | | | DPSLP_REG_VTRIM [27:24] | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:4 | ACT_REG_VTRIM | RW | | 13 | Linear Active-Regulator voltage trim. |
| 24:27 | DPSLP_REG_VTRIM | RW | | 7 | Linear DeepSleep-Regulator voltage trim. |

### 28.1.23 SFLASH_USER_FREE_ROW0

**Description:** USER_FREE_ROW0
**Address:** 0x17000800
**Offset:** 0x800
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA32 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA32 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA32 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA32 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | DATA32 | RW | | X | N/A |

### 28.1.24 SFLASH_USER_FREE_ROW1

**Description:** USER_FREE_ROW1
**Address:** 0x17000A00
**Offset:** 0xA00
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA32 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA32 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA32 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA32 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | DATA32 | RW | | X | N/A |

### 28.1.25 SFLASH_USER_FREE_ROW2

**Description:** USER_FREE_ROW2
**Address:** 0x17000C00
**Offset:** 0xC00
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA32 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA32 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA32 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA32 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | DATA32 | RW | | X | N/A |

### 28.1.26 SFLASH_USER_FREE_ROW3

**Description:** USER_FREE_ROW3
**Address:** 0x17000E00
**Offset:** 0xE00
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA32 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA32 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA32 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA32 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | DATA32 | RW | | X | N/A |

### 28.1.27 SFLASH_SFLASH_UPDATE_MARKER

**Description:** Markers for storing SFLASH programming states
**Address:** 0x17001800
**Offset:** 0x1800
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA32 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA32 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA32 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA32 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | DATA32 | RW | | X | Marker which indicates SFLASH programming state |

### 28.1.28 SFLASH_NORMAL_ACCESS_RESTRICTIONS

**Description:** Indicates access restrictions to be applied on DAP in NORMAL state
**Address:** 0x17001A00
**Offset:** 0x1A00
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Used during NORMAL state bootup
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DIRECT_EXECUTE_DISABLE [7:7] | SYS_AP_MPU_ENABLE [6:6] | AP_CTL_SYS_DISABLE [5:4] | | AP_CTL_CM4_DISABLE [3:2] | | AP_CTL_CM0_DISABLE [1:0] | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | WORK_FLASH_ALLOWED [15:14] | | SRAM_ALLOWED [13:11] | | | FLASH_ALLOWED [10:8] | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:21] | | | SMIF_XIP_ALLOWED [20:20] | MMIO_ALLOWED [19:18] | | SFLASH_ALLOWED [17:16] | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:1 | AP_CTL_CM0_DISABLE | RW | | X | N/A |
| 2:3 | AP_CTL_CM4_DISABLE | RW | | X | N/A |
| 4:5 | AP_CTL_SYS_DISABLE | RW | | X | N/A |
| 6 | SYS_AP_MPU_ENABLE | RW | | X | N/A |
| 7 | DIRECT_EXECUTE_DISABLE | RW | | X | N/A |
| 8:10 | FLASH_ALLOWED | RW | | X | N/A |
| 11:13 | SRAM_ALLOWED | RW | | X | N/A |
| 14:15 | WORK_FLASH_ALLOWED | RW | | X | N/A |
| 16:17 | SFLASH_ALLOWED | RW | | X | N/A |
| 18:19 | MMIO_ALLOWED | RW | | X | N/A |
| 20 | SMIF_XIP_ALLOWED | RW | | X | N/A |

### 28.1.29 SFLASH_NORMAL_DEAD_ACCESS_RESTRICTIONS

**Description:** Indicates access restrictions to be applied on DAP in NORMAL DEAD state
**Address:** 0x17001A04
**Offset:** 0x1A04
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Used during NORMAL state bootup
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DIRECT_EXECUTE_DISABLE [7:7] | SYS_AP_MPU_ENABLE [6:6] | AP_CTL_SYS_DISABLE [5:4] | | AP_CTL_CM4_DISABLE [3:2] | | AP_CTL_CM0_DISABLE [1:0] | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | WORK_FLASH_ALLOWED [15:14] | | SRAM_ALLOWED [13:11] | | | FLASH_ALLOWED [10:8] | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:21] | | | SMIF_XIP_ALLOWED [20:20] | MMIO_ALLOWED [19:18] | | SFLASH_ALLOWED [17:16] | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:1 | AP_CTL_CM0_DISABLE | RW | | X | N/A |
| 2:3 | AP_CTL_CM4_DISABLE | RW | | X | N/A |
| 4:5 | AP_CTL_SYS_DISABLE | RW | | X | N/A |
| 6 | SYS_AP_MPU_ENABLE | RW | | X | N/A |
| 7 | DIRECT_EXECUTE_DISABLE | RW | | X | N/A |
| 8:10 | FLASH_ALLOWED | RW | | X | N/A |
| 11:13 | SRAM_ALLOWED | RW | | X | N/A |
| 14:15 | WORK_FLASH_ALLOWED | RW | | X | N/A |
| 16:17 | SFLASH_ALLOWED | RW | | X | N/A |
| 18:19 | MMIO_ALLOWED | RW | | X | N/A |
| 20 | SMIF_XIP_ALLOWED | RW | | X | N/A |

### 28.1.30 SFLASH_FLASH_BOOT_OBJECT_SIZE

**Description:** Flash Boot - Object Size
**Address:** 0x17002000
**Offset:** 0x2000
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA32 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA32 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA32 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA32 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | DATA32 | RW | | X | N/A |

### 28.1.31 SFLASH_FLASH_BOOT_APP_ID

**Description:** Flash Boot - Application ID/Version
**Address:** 0x17002004
**Offset:** 0x2004
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | APP_ID [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | APP_ID [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | MINOR_VERSION [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:28] | | | | MAJOR_VERSION [27:24] | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | APP_ID | RW | | X | N/A |
| 16:23 | MINOR_VERSION | RW | | X | N/A |
| 24:27 | MAJOR_VERSION | RW | | X | N/A |

### 28.1.32 SFLASH_FLASH_BOOT_BUILD_NUMBER

**Description:** This field contains the Flashboot internal build number.
**Address:** 0x17002018
**Offset:** 0x2018
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | BUILD_NUMBER_LO [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | BUILD_NUMBER_HI [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | BUILD_NUMBER_RESERVED [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | BUILD_NUMBER_RESERVED [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | BUILD_NUMBER_LO | RW | | X | This field contains the Flashboot internal build number.<br><br>Bits[7:0] - BuildNumber16 [7:0]<br>There is no default value because the Flashboot is always programmed and the version can't be zero |
| 8:15 | BUILD_NUMBER_HI | RW | | X | Bits[15:8]- BuildNumber16 [15:9]<br>There is no default value because the Flashboot is always programmed and the version can't be zero |
| 16:31 | BUILD_NUMBER_RESERVED | RW | | X | Reserved for future use |

### 28.1.33 SFLASH_FLASH_BOOT_FAMILY_ID

**Description:** Flash Boot - Family ID
**Address:** 0x1700201C
**Offset:** 0x201C
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA32 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA32 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA32 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA32 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | DATA32 | RW | | X | N/A |

### 28.1.34 SFLASH_PUBLIC_KEY

**Description:** Public key for signature verification (max RSA key size 4096)
**Address:** 0x17006400
**Offset:** 0x6400
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA [7:0] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | DATA | RW | | X | N/A |

### 28.1.35 SFLASH_APP_PROT_SETTINGS

**Description:** Application protection settings (4*128=512 bytes)
**Address:** 0x17007600
**Offset:** 0x7600
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA32 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA32 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA32 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA32 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | DATA32 | RW | | X | N/A |

### 28.1.36 SFLASH_TOC2_OBJECT_SIZE

**Description:** Object size in bytes for CRC calculation starting from offset 0x00
**Address:** 0x17007C00
**Offset:** 0x7C00
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA32 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA32 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA32 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA32 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | DATA32 | RW | | X | N/A |

### 28.1.37 SFLASH_TOC2_MAGIC_NUMBER

**Description:** Magic number(0x01211220)
**Address:** 0x17007C04
**Offset:** 0x7C04
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA32 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA32 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA32 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA32 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | DATA32 | RW | | X | N/A |

### 28.1.38 SFLASH_TOC2_SMIF_CFG_STRUCT_ADDR

**Description:** Null terminated table of pointers representing the SMIF configuration structure
**Address:** 0x17007C08
**Offset:** 0x7C08
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA32 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA32 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA32 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA32 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | DATA32 | RW | | X | N/A |

### 28.1.39 SFLASH_TOC2_FIRST_USER_APP_ADDR

**Description:** Address of First User Application Object
**Address:** 0x17007C0C
**Offset:** 0x7C0C
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA32 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA32 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA32 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA32 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | DATA32 | RW | | X | N/A |

### 28.1.40 SFLASH_TOC2_FIRST_USER_APP_FORMAT

**Description:** Format of First User Application Object. 0 - Basic, 1 - Cypress standard & 2 - Simplified
**Address:** 0x17007C10
**Offset:** 0x7C10
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA32 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA32 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA32 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA32 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | DATA32 | RW | | X | N/A |

### 28.1.41 SFLASH_TOC2_SECOND_USER_APP_ADDR

**Description:** Address of Second User Application Object
**Address:** 0x17007C14
**Offset:** 0x7C14
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA32 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA32 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA32 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA32 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | DATA32 | RW | | X | N/A |

### 28.1.42 SFLASH_TOC2_SECOND_USER_APP_FORMAT

**Description:** Format of Second User Application Object. 0 - Basic, 1 - Cypress standard & 2 - Simplified
**Address:** 0x17007C18
**Offset:** 0x7C18
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA32 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA32 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA32 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA32 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | DATA32 | RW | | X | N/A |

### 28.1.43 SFLASH_TOC2_FIRST_CMX_1_USER_APP_ADDR

**Description:** Address of First CM4 or CM7 core1 User Application Object
**Address:** 0x17007C1C
**Offset:** 0x7C1C
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA32 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA32 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA32 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA32 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | DATA32 | RW | | X | Address of First CM4 or CM7 core1 User Application Object |

### 28.1.44 SFLASH_TOC2_SECOND_CMX_1_USER_APP_ADDR

**Description:** Address of Second CM4 or CM7 core1 User Application Object
**Address:** 0x17007C20
**Offset:** 0x7C20
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA32 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA32 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA32 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA32 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | DATA32 | RW | | X | N/A |

### 28.1.45 SFLASH_TOC2_FIRST_CMX_2_USER_APP_ADDR

**Description:** Address of First CM4 or CM7 core2 User Application Object
**Address:** 0x17007C24
**Offset:** 0x7C24
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA32 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA32 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA32 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA32 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | DATA32 | RW | | X | N/A |

### 28.1.46 SFLASH_TOC2_SECOND_CMX_2_USER_APP_ADDR

**Description:** Address of Second CM4 or CM7 core2 User Application Object
**Address:** 0x17007C28
**Offset:** 0x7C28
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA32 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA32 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA32 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA32 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | DATA32 | RW | | X | N/A |

### 28.1.47 SFLASH_TOC2_SECURITY_UPDATES_MARKER

**Description:** Marker for Security Updates
**Address:** 0x17007CFC
**Offset:** 0x7CFC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA32 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA32 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA32 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA32 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | DATA32 | RW | | X | This field is valid in flash boot version 3.1.0.554 and later.<br>When marker is set to 0xFEDEEDDF the following PPUs will be configured during boot:<br>- PERI_MS_PPU_FX_PERI_GR2_GROUP (Fixed PPU) - read only for all PCs;<br>- Programmable PPU#11 configured to allow full access for the following region 0x40201000 - 0x4020100C. The HSM may overwrite the default configuration and reconfigure the PPU.<br>- Programmable PPU#12 configured to allow full access for the CPUSS_ECC_CTL register (0x402013C8). The HSM may overwrite the default configuration and reconfigure the PPU.<br>- Programmable PPU#13 configured to allow full access for the following region 0x40201300 - 0x402013C8. The HSM may overwrite the default configuration and reconfigure the PPU. |

### 28.1.48 SFLASH_TOC2_SHASH_OBJECTS

**Description:** Number of additional objects to be verified for SECURE_HASH
**Address:** 0x17007D00
**Offset:** 0x7D00
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA32 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA32 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA32 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA32 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | DATA32 | RW | | X | N/A |

### 28.1.49 SFLASH_TOC2_SIGNATURE_VERIF_KEY

**Description:** Address of signature verification key (0 if none).The object is signature specific key. It is the public key in case of RSA
**Address:** 0x17007D04
**Offset:** 0x7D04
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA32 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA32 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA32 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA32 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | DATA32 | RW | | X | N/A |

### 28.1.50 SFLASH_TOC2_APP_PROTECTION_ADDR

**Description:** Address of Application Protection
**Address:** 0x17007D08
**Offset:** 0x7D08
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA32 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA32 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA32 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA32 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | DATA32 | RW | | X | N/A |

### 28.1.51 SFLASH_TOC2_REVISION

**Description:** Indicates TOC2 Revision. It is not used now.
**Address:** 0x17007DF4
**Offset:** 0x7DF4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA32 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA32 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA32 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA32 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | DATA32 | RW | | X | Indicate TOC2 Revision<br>Value: 0x0000_0000 and 0xFFFF_FFFF - default. |

### 28.1.52 SFLASH_TOC2_FLAGS

**Description:** Controls default configuration
**Address:** 0x17007DF8
**Offset:** 0x7DF8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** If TOC2 is erased (default), Flash boot assumes TOC2_FLAGS = 0x0000_0243
**Default:** 0x243

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | APP_AUTH_CTL [7:7] | SWJ_PINS_CTL [6:5] | | LISTEN_WINDOW [4:2] | | | CLOCK_CONFIG [1:0] | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:11] | | | | | FB_BOOTLOADER_CTL [10:9] | | APP_AUTH_CTL [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:1 | CLOCK_CONFIG | RW | | 3 | Indicates clock frequency configuration. The clock should stay the same after Flash Boot execution.<br>0 = 8 MHz, IMO, no FLL<br>1 = 25 MHz, IMO + FLL<br>2 = 50 MHz, IMO + FLL<br>3 = Use ROM boot clocks configuration (default)<br>Note: the default value is 2 for Flash boot version earlier than 554. |
| 2:4 | LISTEN_WINDOW | RW | | 0 | Determines the Listen window to allow sufficient time to acquire debug port. When CLOCK_CONFIG is set to 3, these window times are calculated assuming ROM boot clock is at 100MHz.<br>0 = 20 ms (Default)<br>1 = 10 ms<br>2 = 1 ms<br>3 = 0 ms (No Listen window)<br>4 = 100 ms |
| 5:6 | SWJ_PINS_CTL | RW | | 2 | Determines if SWJ pins are configured in SWJ mode by Flash boot.<br>Note: SWJ pins may be enabled later in the user code.<br>0 = Do not enable SWJ pins in Flash boot. Listen window is skipped.<br>1 = Do not enable SWJ pins in Flash boot. Listen window is skipped.<br>2 = Enable SWJ pins in Flash boot (default).<br>3 = Do not enable SWJ pins in Flash boot. Listen window is skipped. |
| 7:8 | APP_AUTH_CTL | RW | | 0 | Determines if the application image digital signature verification (authentication) is performed:<br>0 = Authentication is enabled (default).<br>1 = Authentication is disabled.<br>2 = Authentication is enabled (recommended).<br>3 = Authentication is enabled. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 9:10 | FB_BOOTLOADER_CTL | RW | | 1 | Determine if the internal bootloader in Flash boot is disabled:<br>0 = Internal bootloader is disabled.<br>1 = Internal bootloader is launched if the other bootloader conditions are met (default).<br>2 = Internal bootloader is disabled.<br>3 = Internal bootloader is disabled. |

# 29 SMARTIO

**Description** Programmable IO configuration
**Base Address** 0x40320000
**Size** 0x10000
**Slave Num** MMIO3 - 2

## 29.1 PRT 12

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SMARTIO_PRT12_CTL | 0x40320C00 | FULL | Control register |
| SMARTIO_PRT12_SYNC_CTL | 0x40320C10 | FULL | Synchronization control register |
| SMARTIO_PRT12_LUT_SEL0 | 0x40320C20 | FULL | LUT component input selection |
| SMARTIO_PRT12_LUT_SEL1 | 0x40320C24 | FULL | LUT component input selection |
| SMARTIO_PRT12_LUT_SEL2 | 0x40320C28 | FULL | LUT component input selection |
| SMARTIO_PRT12_LUT_SEL3 | 0x40320C2C | FULL | LUT component input selection |
| SMARTIO_PRT12_LUT_SEL4 | 0x40320C30 | FULL | LUT component input selection |
| SMARTIO_PRT12_LUT_SEL5 | 0x40320C34 | FULL | LUT component input selection |
| SMARTIO_PRT12_LUT_SEL6 | 0x40320C38 | FULL | LUT component input selection |
| SMARTIO_PRT12_LUT_SEL7 | 0x40320C3C | FULL | LUT component input selection |
| SMARTIO_PRT12_LUT_CTL0 | 0x40320C40 | FULL | LUT component control register |
| SMARTIO_PRT12_LUT_CTL1 | 0x40320C44 | FULL | LUT component control register |
| SMARTIO_PRT12_LUT_CTL2 | 0x40320C48 | FULL | LUT component control register |
| SMARTIO_PRT12_LUT_CTL3 | 0x40320C4C | FULL | LUT component control register |
| SMARTIO_PRT12_LUT_CTL4 | 0x40320C50 | FULL | LUT component control register |
| SMARTIO_PRT12_LUT_CTL5 | 0x40320C54 | FULL | LUT component control register |
| SMARTIO_PRT12_LUT_CTL6 | 0x40320C58 | FULL | LUT component control register |
| SMARTIO_PRT12_LUT_CTL7 | 0x40320C5C | FULL | LUT component control register |
| SMARTIO_PRT12_DU_SEL | 0x40320CC0 | FULL | Data unit component input selection |
| SMARTIO_PRT12_DU_CTL | 0x40320CC4 | FULL | Data unit component control register |
| SMARTIO_PRT12_DATA | 0x40320CF0 | FULL | Data register |

## 29.2 PRT 13

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SMARTIO_PRT13_CTL | 0x40320D00 | FULL | Control register |
| SMARTIO_PRT13_SYNC_CTL | 0x40320D10 | FULL | Synchronization control register |
| SMARTIO_PRT13_LUT_SEL0 | 0x40320D20 | FULL | LUT component input selection |
| SMARTIO_PRT13_LUT_SEL1 | 0x40320D24 | FULL | LUT component input selection |
| SMARTIO_PRT13_LUT_SEL2 | 0x40320D28 | FULL | LUT component input selection |
| SMARTIO_PRT13_LUT_SEL3 | 0x40320D2C | FULL | LUT component input selection |
| SMARTIO_PRT13_LUT_SEL4 | 0x40320D30 | FULL | LUT component input selection |
| SMARTIO_PRT13_LUT_SEL5 | 0x40320D34 | FULL | LUT component input selection |
| SMARTIO_PRT13_LUT_SEL6 | 0x40320D38 | FULL | LUT component input selection |
| SMARTIO_PRT13_LUT_SEL7 | 0x40320D3C | FULL | LUT component input selection |
| SMARTIO_PRT13_LUT_CTL0 | 0x40320D40 | FULL | LUT component control register |
| SMARTIO_PRT13_LUT_CTL1 | 0x40320D44 | FULL | LUT component control register |
| SMARTIO_PRT13_LUT_CTL2 | 0x40320D48 | FULL | LUT component control register |
| SMARTIO_PRT13_LUT_CTL3 | 0x40320D4C | FULL | LUT component control register |
| SMARTIO_PRT13_LUT_CTL4 | 0x40320D50 | FULL | LUT component control register |
| SMARTIO_PRT13_LUT_CTL5 | 0x40320D54 | FULL | LUT component control register |
| SMARTIO_PRT13_LUT_CTL6 | 0x40320D58 | FULL | LUT component control register |
| SMARTIO_PRT13_LUT_CTL7 | 0x40320D5C | FULL | LUT component control register |
| SMARTIO_PRT13_DU_SEL | 0x40320DC0 | FULL | Data unit component input selection |
| SMARTIO_PRT13_DU_CTL | 0x40320DC4 | FULL | Data unit component control register |
| SMARTIO_PRT13_DATA | 0x40320DF0 | FULL | Data register |

## 29.3 PRT 14

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SMARTIO_PRT14_CTL | 0x40320E00 | FULL | Control register |
| SMARTIO_PRT14_SYNC_CTL | 0x40320E10 | FULL | Synchronization control register |
| SMARTIO_PRT14_LUT_SEL0 | 0x40320E20 | FULL | LUT component input selection |
| SMARTIO_PRT14_LUT_SEL1 | 0x40320E24 | FULL | LUT component input selection |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SMARTIO_PRT14_LUT_SEL2 | 0x40320E28 | FULL | LUT component input selection |
| SMARTIO_PRT14_LUT_SEL3 | 0x40320E2C | FULL | LUT component input selection |
| SMARTIO_PRT14_LUT_SEL4 | 0x40320E30 | FULL | LUT component input selection |
| SMARTIO_PRT14_LUT_SEL5 | 0x40320E34 | FULL | LUT component input selection |
| SMARTIO_PRT14_LUT_SEL6 | 0x40320E38 | FULL | LUT component input selection |
| SMARTIO_PRT14_LUT_SEL7 | 0x40320E3C | FULL | LUT component input selection |
| SMARTIO_PRT14_LUT_CTL0 | 0x40320E40 | FULL | LUT component control register |
| SMARTIO_PRT14_LUT_CTL1 | 0x40320E44 | FULL | LUT component control register |
| SMARTIO_PRT14_LUT_CTL2 | 0x40320E48 | FULL | LUT component control register |
| SMARTIO_PRT14_LUT_CTL3 | 0x40320E4C | FULL | LUT component control register |
| SMARTIO_PRT14_LUT_CTL4 | 0x40320E50 | FULL | LUT component control register |
| SMARTIO_PRT14_LUT_CTL5 | 0x40320E54 | FULL | LUT component control register |
| SMARTIO_PRT14_LUT_CTL6 | 0x40320E58 | FULL | LUT component control register |
| SMARTIO_PRT14_LUT_CTL7 | 0x40320E5C | FULL | LUT component control register |
| SMARTIO_PRT14_DU_SEL | 0x40320EC0 | FULL | Data unit component input selection |
| SMARTIO_PRT14_DU_CTL | 0x40320EC4 | FULL | Data unit component control register |
| SMARTIO_PRT14_DATA | 0x40320EF0 | FULL | Data register |

## 29.4 PRT 15

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SMARTIO_PRT15_CTL | 0x40320F00 | FULL | Control register |
| SMARTIO_PRT15_SYNC_CTL | 0x40320F10 | FULL | Synchronization control register |
| SMARTIO_PRT15_LUT_SEL0 | 0x40320F20 | FULL | LUT component input selection |
| SMARTIO_PRT15_LUT_SEL1 | 0x40320F24 | FULL | LUT component input selection |
| SMARTIO_PRT15_LUT_SEL2 | 0x40320F28 | FULL | LUT component input selection |
| SMARTIO_PRT15_LUT_SEL3 | 0x40320F2C | FULL | LUT component input selection |
| SMARTIO_PRT15_LUT_SEL4 | 0x40320F30 | FULL | LUT component input selection |
| SMARTIO_PRT15_LUT_SEL5 | 0x40320F34 | FULL | LUT component input selection |
| SMARTIO_PRT15_LUT_SEL6 | 0x40320F38 | FULL | LUT component input selection |
| SMARTIO_PRT15_LUT_SEL7 | 0x40320F3C | FULL | LUT component input selection |
| SMARTIO_PRT15_LUT_CTL0 | 0x40320F40 | FULL | LUT component control register |
| SMARTIO_PRT15_LUT_CTL1 | 0x40320F44 | FULL | LUT component control register |
| SMARTIO_PRT15_LUT_CTL2 | 0x40320F48 | FULL | LUT component control register |
| SMARTIO_PRT15_LUT_CTL3 | 0x40320F4C | FULL | LUT component control register |
| SMARTIO_PRT15_LUT_CTL4 | 0x40320F50 | FULL | LUT component control register |
| SMARTIO_PRT15_LUT_CTL5 | 0x40320F54 | FULL | LUT component control register |
| SMARTIO_PRT15_LUT_CTL6 | 0x40320F58 | FULL | LUT component control register |
| SMARTIO_PRT15_LUT_CTL7 | 0x40320F5C | FULL | LUT component control register |
| SMARTIO_PRT15_DU_SEL | 0x40320FC0 | FULL | Data unit component input selection |
| SMARTIO_PRT15_DU_CTL | 0x40320FC4 | FULL | Data unit component control register |
| SMARTIO_PRT15_DATA | 0x40320FF0 | FULL | Data register |

## 29.5 PRT 17

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SMARTIO_PRT17_CTL | 0x40321100 | FULL | Control register |
| SMARTIO_PRT17_SYNC_CTL | 0x40321110 | FULL | Synchronization control register |
| SMARTIO_PRT17_LUT_SEL0 | 0x40321120 | FULL | LUT component input selection |
| SMARTIO_PRT17_LUT_SEL1 | 0x40321124 | FULL | LUT component input selection |
| SMARTIO_PRT17_LUT_SEL2 | 0x40321128 | FULL | LUT component input selection |
| SMARTIO_PRT17_LUT_SEL3 | 0x4032112C | FULL | LUT component input selection |
| SMARTIO_PRT17_LUT_SEL4 | 0x40321130 | FULL | LUT component input selection |
| SMARTIO_PRT17_LUT_SEL5 | 0x40321134 | FULL | LUT component input selection |
| SMARTIO_PRT17_LUT_SEL6 | 0x40321138 | FULL | LUT component input selection |
| SMARTIO_PRT17_LUT_SEL7 | 0x4032113C | FULL | LUT component input selection |
| SMARTIO_PRT17_LUT_CTL0 | 0x40321140 | FULL | LUT component control register |
| SMARTIO_PRT17_LUT_CTL1 | 0x40321144 | FULL | LUT component control register |
| SMARTIO_PRT17_LUT_CTL2 | 0x40321148 | FULL | LUT component control register |
| SMARTIO_PRT17_LUT_CTL3 | 0x4032114C | FULL | LUT component control register |
| SMARTIO_PRT17_LUT_CTL4 | 0x40321150 | FULL | LUT component control register |
| SMARTIO_PRT17_LUT_CTL5 | 0x40321154 | FULL | LUT component control register |
| SMARTIO_PRT17_LUT_CTL6 | 0x40321158 | FULL | LUT component control register |
| SMARTIO_PRT17_LUT_CTL7 | 0x4032115C | FULL | LUT component control register |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SMARTIO_PRT17_DU_SEL | 0x403211C0 | FULL | Data unit component input selection |
| SMARTIO_PRT17_DU_CTL | 0x403211C4 | FULL | Data unit component control register |
| SMARTIO_PRT17_DATA | 0x403211F0 | FULL | Data register |

## 29.6 Register Details

### 29.6.1 PRT

#### 29.6.1.1 SMARTIO_PRT_CTL

**Description:** Control register
**Address:** 0x40320000
**Offset:** 0x0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** Undefined as one or more bit fields have a default value that is undefined

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | BYPASS [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:13] | | | CLOCK_SRC [12:8] | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | ENABLED [31:31] | None [30:26] | | | | | PIPELINE_EN [25:25] | HLD_OVR [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | BYPASS | RW | R | Undefined | Bypass of the programmable IO, one bit for each IO pin: BYPASS[i] is for IO pin i. When ENABLED is '1', this field is used. When ENABLED is '0', this field is NOT used and SMARTIO fabric is always bypassed.<br>'0': No bypass (programmable SMARTIO fabric is exposed).<br>'1': Bypass (programmable SMARTIOIO fabric is hidden). |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 8:12 | CLOCK_SRC | RW | R | 20 | Clock ('clk_fabric') and reset ('rst_fabric_n') source selection:<br>'0': io_data_in[0]/'1'.<br>...<br>'7': io_data_in[7]/'1'.<br>'8': chip_data[0]/'1'.<br>...<br>'15': chip_data[7]/'1'.<br>'16': clk_smartio/rst_sys_act_n. Used for both Active functionality synchronous logic on 'clk_smartio'. This selection is intended for synchronous operation on a PCLK specified clock frequency ('clock_smartio_pos_en'). Note that the fabric's clocked elements are frequency aligned, but NOT phase aligned to 'clk_sys'.<br>'17': clk_smartio/rst_sys_dpslp_n. Used for both DeepSleep functionality synchronous logic on 'clk_smartio' (note that 'clk_smartio' is NOT available in DeepSleep and Hibernate power modes). This selection is intended for synchronous operation on a PCLK specified clock frequency ('clock_smartio_pos_en'). Note that the fabric's clocked elements are frequency aligned, but NOT phase aligned to 'clk_sys'.<br>'18': Same as '17'. Note that the M0S8 SMARTIO version used the Hibernate reset for this value, but the MXS40 SMARTIO version does not support Hibernate functionality.<br>'19': clk_lf/rst_lf_dpslp_n (note that 'clk_lf' is available in DeepSleep power mode). This selection is intended for synchronous operation on'clk_lf'. Note that the fabric's clocked elements are frequency aligned, but NOT phase aligned to other 'clk_lf' clocked elements.<br>'20'-'30': Clock source is constant '0'. Any of these clock sources should be selected when the IP is disabled to ensure low power consumption.<br>'31': asynchronous mode/'1'. Select this when clockless operation is configured.<br><br>NOTE: Two positive edges of the selected clock are required for the block to be enabled (to deactivate reset). In asynchronous (clockless) mode clk_sys is used to enable the block, but is not available for clocking. |
| 24 | HLD_OVR | RW | R | Undefined | IO cell hold override functionality. In DeepSleep power mode, the HSIOM holds the IO cell output and output enable signals if Active functionality is connected to the IO pads. This is undesirable if the SMARTIO is supposed to deliver DeepSleep output functionality on these IO pads. This field is used to control the hold override functionality from the SMARTIO:<br>'0': The HSIOM controls the IO cell hold override functionality ('hsiom_hld_ovr').<br>'1': The SMARTIO controls the IO cel hold override functionality:<br>- In bypass mode (ENABLED is '0' or BYPASS[i] is '1'), the HSIOM control is used.<br>- In NON bypass mode (ENABLED is '1' and BYPASS[i] is '0'), the SMARTIO sets hold override to 'pwr_hld_ovr_hib' to enable SMARTIO functionality in DeepSleep power mode (but disables it in Hibernate or Stop power mode). |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 25 | PIPELINE_EN | RW | R | 1 | Enable for pipeline register:<br>'0': Disabled (register is bypassed).<br>'1': Enabled. |
| 31 | ENABLED | RW | R | 0 | Enable for programmable IO. Should only be set to '1' when the programmable IO is completely configured:<br>'0': Disabled (signals are bypassed; behavior as if BYPASS is 0xFF). When disabled, the fabric (data unit and LUTs) reset is activated.<br><br>If the IP is disabled:<br>- The PIPELINE_EN register field should be set to '1', to ensure low power consumption by preventing combinatorial loops.<br>- The CLOCK_SRC register field should be set to '20'-'30' (clock is constant '0'), to ensure low power consumption.<br><br>'1': Enabled. Once enabled, it takes 3 'clk_fabric' clock cycles till the fabric reset is de-activated and the fabric becomes fully functional. This ensures that the IO pins' input synchronizer states are flushed when the fabric is fully functional. |

### 29.6.1.2 SMARTIO_PRT_SYNC_CTL

**Description:** Synchronization control register
**Address:** 0x40320010
**Offset:** 0x10
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** Undefined as one or more bit fields have a default value that is undefined

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | IO_SYNC_EN [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | CHIP_SYNC_EN [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | IO_SYNC_EN | RW | R | Undefined | Synchronization of the IO pin input signals to 'clk_fabric', one bit for each IO pin: IO_SYNC_EN[i] is for IO pin i.<br>'0': No synchronization.<br>'1': Synchronization. |
| 8:15 | CHIP_SYNC_EN | RW | R | Undefined | Synchronization of the chip input signals to 'clk_fabric', one bit for each input: CHIP_SYNC_EN[i] is for input i.<br>'0': No synchronization.<br>'1': Synchronization. |

### 29.6.1.3 SMARTIO_PRT_LUT_SEL

**Description:** LUT component input selection
**Address:** 0x40320020
**Offset:** 0x20
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:4] | | | | LUT_TR0_SEL [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:12] | | | | LUT_TR1_SEL [11:8] | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:20] | | | | LUT_TR2_SEL [19:16] | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | LUT_TR0_SEL | RW | R | Undefined | LUT input signal 'tr0_in' source selection:<br>'0': Data unit output.<br>'1': LUT 1 output.<br>'2': LUT 2 output.<br>'3': LUT 3 output.<br>'4': LUT 4 output.<br>'5': LUT 5 output.<br>'6': LUT 6 output.<br>'7': LUT 7 output.<br>'8': chip_data[0] (for LUTs 0, 1, 2, 3); chip_data[4] (for LUTs 4, 5, 6, 7).<br>'9': chip_data[1] (for LUTs 0, 1, 2, 3); chip_data[5] (for LUTs 4, 5, 6, 7).<br>'10': chip_data[2] (for LUTs 0, 1, 2, 3); chip_data[6] (for LUTs 4, 5, 6, 7).<br>'11': chip_data[3] (for LUTs 0, 1, 2, 3); chip_data[7] (for LUTs 4, 5, 6, 7).<br>'12': io_data_in[0] (for LUTs 0, 1, 2, 3); io_data_in[4] (for LUTs 4, 5, 6, 7).<br>'13': io_data_in[1] (for LUTs 0, 1, 2, 3); io_data_in[5] (for LUTs 4, 5, 6, 7).<br>'14': io_data_in[2] (for LUTs 0, 1, 2, 3); io_data_in[6] (for LUTs 4, 5, 6, 7).<br>'15': io_data_in[3] (for LUTs 0, 1, 2, 3); io_data_in[7] (for LUTs 4, 5, 6, 7). |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 8:11 | LUT_TR1_SEL | RW | R | Undefined | LUT input signal 'tr1_in' source selection:<br>'0': LUT 0 output.<br>'1': LUT 1 output.<br>'2': LUT 2 output.<br>'3': LUT 3 output.<br>'4': LUT 4 output.<br>'5': LUT 5 output.<br>'6': LUT 6 output.<br>'7': LUT 7 output.<br>'8': chip_data[0] (for LUTs 0, 1, 2, 3); chip_data[4] (for LUTs 4, 5, 6, 7).<br>'9': chip_data[1] (for LUTs 0, 1, 2, 3); chip_data[5] (for LUTs 4, 5, 6, 7).<br>'10': chip_data[2] (for LUTs 0, 1, 2, 3); chip_data[6] (for LUTs 4, 5, 6, 7).<br>'11': chip_data[3] (for LUTs 0, 1, 2, 3); chip_data[7] (for LUTs 4, 5, 6, 7).<br>'12': io_data_in[0] (for LUTs 0, 1, 2, 3); io_data_in[4] (for LUTs 4, 5, 6, 7).<br>'13': io_data_in[1] (for LUTs 0, 1, 2, 3); io_data_in[5] (for LUTs 4, 5, 6, 7).<br>'14': io_data_in[2] (for LUTs 0, 1, 2, 3); io_data_in[6] (for LUTs 4, 5, 6, 7).<br>'15': io_data_in[3] (for LUTs 0, 1, 2, 3); io_data_in[7] (for LUTs 4, 5, 6, 7). |
| 16:19 | LUT_TR2_SEL | RW | R | Undefined | LUT input signal 'tr2_in' source selection. Encoding is the same as for LUT_TR1_SEL. |

### 29.6.1.4 SMARTIO_PRT_LUT_CTL

**Description:** LUT component control register
**Address:** 0x40320040
**Offset:** 0x40
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | LUT [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:10] | | | | | | LUT_OPC [9:8] | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | LUT | RW | R | Undefined | LUT configuration. Depending on the LUT opcode LUT_OPC, the internal state lut_reg (captured in a flip-flop) and the LUT input signals tr0_in, tr1_in, tr2_in, the LUT configuration is used to determine the LUT output signal and the next sequential state (lut_reg). |
| 8:9 | LUT_OPC | RW | R | Undefined | LUT opcode specifies the LUT operation:<br>'0': Combinatoral output, no feedback.<br>tr_out = LUT[{tr2_in, tr1_in, tr0_in}].<br>'1': Combinatorial output, feedback.<br>tr_out = LUT[{lut_reg, tr1_in, tr0_in}].<br>On clock:<br>lut_reg <= tr_in2.<br>'2': Sequential output, no feedback.<br>temp = LUT[{tr2_in, tr1_in, tr0_in}].<br>tr_out = lut_reg.<br>On clock:<br>lut_reg <= temp.<br>'3': Register with asynchronous set and reset.<br>tr_out = lut_reg.<br>enable = (tr2_in ^ LUT[4]) \| LUT[5].<br>set = enable & (tr1_in ^ LUT[2]) & LUT[3].<br>clr = enable & (tr0_in ^ LUT[0]) & LUT[1].<br>Asynchronously (no clock required):<br>lut_reg <= if (clr) '0' else if (set) '1' |

### 29.6.1.5 SMARTIO_PRT_DU_SEL

**Description:** Data unit component input selection
**Address:** 0x403200C0
**Offset:** 0xC0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** Undefined as one or more bit fields have a default value that is undefined

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:4] | | | | DU_TR0_SEL [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:12] | | | | DU_TR1_SEL [11:8] | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:20] | | | | DU_TR2_SEL [19:16] | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:30] | | DU_DATA1_SEL [29:28] | | None [27:26] | | DU_DATA0_SEL [25:24] | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | DU_TR0_SEL | RW | R | Undefined | Data unit input signal 'tr0_in' source selection:<br>'0': Constant '0'.<br>'1': Constant '1'.<br>'2': Data unit output.<br>'10-3': LUT 7 - 0 outputs.<br>Otherwise: Undefined. |
| 8:11 | DU_TR1_SEL | RW | R | Undefined | Data unit input signal 'tr1_in' source selection.<br>Encoding is the same as for DU_TR0_SEL. |
| 16:19 | DU_TR2_SEL | RW | R | Undefined | Data unit input signal 'tr2_in' source selection.<br>Encoding is the same as for DU_TR0_SEL. |
| 24:25 | DU_DATA0_SEL | RW | R | Undefined | Data unit input data 'data0_in' source selection:<br>'0': Constant '0'.<br>'1': chip_data[7:0].<br>'2': io_data_in[7:0].<br>'3': DATA.DATA MMIO register field. |
| 28:29 | DU_DATA1_SEL | RW | R | Undefined | Data unit input data 'data1_in' source selection.<br>Encoding is the same as for DU_DATA0_SEL. |

### 29.6.1.6 SMARTIO_PRT_DU_CTL

**Description:** Data unit component control register
**Address:** 0x403200C4
**Offset:** 0xC4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** Undefined as one or more bit fields have a default value that is undefined

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:3] | | | | | DU_SIZE [2:0] | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:12] | | | | DU_OPC [11:8] | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:2 | DU_SIZE | RW | R | Undefined | Size/width of the data unit data operands (in bits) is DU_SIZE+1. E.g., if DU_SIZE is 7, the width is 8 bits. |
| 8:11 | DU_OPC | RW | R | Undefined | Data unit opcode specifies the data unit operation:<br>'1': INCR<br>'2': DECR<br>'3': INCR_WRAP<br>'4': DECR_WRAP<br>'5': INCR_DECR<br>'6': INCR_DECR_WRAP<br>'7': ROR<br>'8': SHR<br>'9': AND_OR<br>'10': SHR_MAJ3<br>'11': SHR_EQL.<br>Otherwise: Undefined. |

### 29.6.1.7 SMARTIO_PRT_DATA

**Description:** Data register
**Address:** 0x403200F0
**Offset:** 0xF0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** Undefined as one or more bit fields have a default value that is undefined

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | DATA | RW | R | Undefined | Data unit input data source. |

# 30 SMIF

**Description** Serial Memory Interface
**Base Address** 0x40420000
**Size** 0x10000
**Slave Num** MMIO4 - 0

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SMIF0_CTL | 0x40420000 | FULL | Control<br>Note:INT_CLOCK_DL_ENABLED INT_CLOCK_CAPTURE_CYCLE are not available for this register |
| SMIF0_STATUS | 0x40420004 | FULL | Status |
| SMIF0_DELAY_TAP_SEL | 0x40420030 | FULL | Delay Tap Select Register |
| SMIF0_TX_CMD_FIFO_STATUS | 0x40420044 | FULL | Transmitter command FIFO status |
| SMIF0_TX_CMD_FIFO_WR | 0x40420050 | FULL | Transmitter command FIFO write |
| SMIF0_TX_DATA_FIFO_CTL | 0x40420080 | FULL | Transmitter data FIFO control |
| SMIF0_TX_DATA_FIFO_STATUS | 0x40420084 | FULL | Transmitter data FIFO status |
| SMIF0_TX_DATA_FIFO_WR1 | 0x40420090 | FULL | Transmitter data FIFO write |
| SMIF0_TX_DATA_FIFO_WR2 | 0x40420094 | FULL | Transmitter data FIFO write |
| SMIF0_TX_DATA_FIFO_WR4 | 0x40420098 | FULL | Transmitter data FIFO write |
| SMIF0_TX_DATA_FIFO_WR1ODD | 0x4042009C | FULL | Transmitter data FIFO write |
| SMIF0_RX_DATA_MMIO_FIFO_CTL | 0x404200C0 | FULL | Receiver data MMIO FIFO control |
| SMIF0_RX_DATA_MMIO_FIFO_STATUS | 0x404200C4 | FULL | Receiver data MMIO FIFO status |
| SMIF0_RX_DATA_FIFO_STATUS | 0x404200C8 | FULL | Receiver data FIFO status |
| SMIF0_RX_DATA_MMIO_FIFO_RD1 | 0x404200D0 | FULL | Receiver data MMIO FIFO read |
| SMIF0_RX_DATA_MMIO_FIFO_RD2 | 0x404200D4 | FULL | Receiver data MMIO FIFO read |
| SMIF0_RX_DATA_MMIO_FIFO_RD4 | 0x404200D8 | FULL | Receiver data MMIO FIFO read |
| SMIF0_RX_DATA_MMIO_FIFO_RD1_SILENT | 0x404200E0 | FULL | Receiver data MMIO FIFO silent read |
| SMIF0_SLOW_CA_CTL | 0x40420100 | FULL | Slow cache control |
| SMIF0_SLOW_CA_CMD | 0x40420108 | FULL | Slow cache command |
| SMIF0_CRYPTO_CMD | 0x40420200 | FULL | Cryptography Command |
| SMIF0_CRYPTO_INPUT0 | 0x40420220 | FULL | Cryptography input 0 |
| SMIF0_CRYPTO_INPUT1 | 0x40420224 | FULL | Cryptography input 1 |
| SMIF0_CRYPTO_INPUT2 | 0x40420228 | FULL | Cryptography input 2 |
| SMIF0_CRYPTO_INPUT3 | 0x4042022C | FULL | Cryptography input 3 |
| SMIF0_CRYPTO_KEY0 | 0x40420240 | FULL | Cryptography key 0 |
| SMIF0_CRYPTO_KEY1 | 0x40420244 | FULL | Cryptography key 1 |
| SMIF0_CRYPTO_KEY2 | 0x40420248 | FULL | Cryptography key 2 |
| SMIF0_CRYPTO_KEY3 | 0x4042024C | FULL | Cryptography key 3 |
| SMIF0_CRYPTO_OUTPUT0 | 0x40420260 | FULL | Cryptography output 0 |
| SMIF0_CRYPTO_OUTPUT1 | 0x40420264 | FULL | Cryptography output 1 |
| SMIF0_CRYPTO_OUTPUT2 | 0x40420268 | FULL | Cryptography output 2 |
| SMIF0_CRYPTO_OUTPUT3 | 0x4042026C | FULL | Cryptography output 3 |
| SMIF0_INTR | 0x404207C0 | FULL | Interrupt register<br>Note:DL_FAIL DL_WARNING CRC_ERROR FS_STATUS_ERROR are not available for this register |
| SMIF0_INTR_SET | 0x404207C4 | FULL | Interrupt set register<br>Note:DL_FAIL DL_WARNING CRC_ERROR FS_STATUS_ERROR are not available for this register |
| SMIF0_INTR_MASK | 0x404207C8 | FULL | Interrupt mask register<br>Note:DL_FAIL DL_WARNING CRC_ERROR FS_STATUS_ERROR are not available for this register |
| SMIF0_INTR_MASKED | 0x404207CC | FULL | Interrupt masked register<br>Note:DL_FAIL DL_WARNING CRC_ERROR FS_STATUS_ERROR are not available for this register |

## 30.1 DEVICE 0

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SMIF0_DEVICE0_CTL | 0x40420800 | FULL | Control |
| SMIF0_DEVICE0_ADDR | 0x40420808 | FULL | Device region base address |
| SMIF0_DEVICE0_MASK | 0x4042080C | FULL | Device region mask |
| SMIF0_DEVICE0_ADDR_CTL | 0x40420820 | FULL | Address control |
| SMIF0_DEVICE0_RD_CMD_CTL | 0x40420840 | FULL | Read command control |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SMIF0_DEVICE0_RD_ADDR_CTL | 0x40420844 | FULL | Read address control |
| SMIF0_DEVICE0_RD_MODE_CTL | 0x40420848 | FULL | Read mode control |
| SMIF0_DEVICE0_RD_DUMMY_CTL | 0x4042084C | FULL | Read dummy control |
| SMIF0_DEVICE0_RD_DATA_CTL | 0x40420850 | FULL | Read data control |
| SMIF0_DEVICE0_RD_BOUND_CTL | 0x40420858 | FULL | Read boundary control |
| SMIF0_DEVICE0_WR_CMD_CTL | 0x40420860 | FULL | Write command control |
| SMIF0_DEVICE0_WR_ADDR_CTL | 0x40420864 | FULL | Write address control |
| SMIF0_DEVICE0_WR_MODE_CTL | 0x40420868 | FULL | Write mode control |
| SMIF0_DEVICE0_WR_DUMMY_CTL | 0x4042086C | FULL | Write dummy control |
| SMIF0_DEVICE0_WR_DATA_CTL | 0x40420870 | FULL | Write data control |

## 30.2 DEVICE 1

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SMIF0_DEVICE1_CTL | 0x40420880 | FULL | Control |
| SMIF0_DEVICE1_ADDR | 0x40420888 | FULL | Device region base address |
| SMIF0_DEVICE1_MASK | 0x4042088C | FULL | Device region mask |
| SMIF0_DEVICE1_ADDR_CTL | 0x404208A0 | FULL | Address control |
| SMIF0_DEVICE1_RD_CMD_CTL | 0x404208C0 | FULL | Read command control |
| SMIF0_DEVICE1_RD_ADDR_CTL | 0x404208C4 | FULL | Read address control |
| SMIF0_DEVICE1_RD_MODE_CTL | 0x404208C8 | FULL | Read mode control |
| SMIF0_DEVICE1_RD_DUMMY_CTL | 0x404208CC | FULL | Read dummy control |
| SMIF0_DEVICE1_RD_DATA_CTL | 0x404208D0 | FULL | Read data control |
| SMIF0_DEVICE1_RD_BOUND_CTL | 0x404208D8 | FULL | Read boundary control |
| SMIF0_DEVICE1_WR_CMD_CTL | 0x404208E0 | FULL | Write command control |
| SMIF0_DEVICE1_WR_ADDR_CTL | 0x404208E4 | FULL | Write address control |
| SMIF0_DEVICE1_WR_MODE_CTL | 0x404208E8 | FULL | Write mode control |
| SMIF0_DEVICE1_WR_DUMMY_CTL | 0x404208EC | FULL | Write dummy control |
| SMIF0_DEVICE1_WR_DATA_CTL | 0x404208F0 | FULL | Write data control |

## 30.3 Register Details

### 30.3.1 SMIF_CTL

**Description:** Control
**Address:** 0x40420000
**Offset:** 0x0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** The register fields should only be changed when the IP is disabled; i.e. CTL.ENABLED is '0'. The only exception to this rule is the CTL.XIP_MODE field, which can be changed when the IP is enabled.
**Default:** 0x503400

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:7] | DELAY_LINE_SEL [6:5] | | CLOCK_IF_TX_SEL [4:4] | None [3:1] | | | XIP_MODE [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:15] | CLOCK_IF_RX_SEL [14:12] | | | None [11:9] | | | DELAY_TAP_ENABLED [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | SELECT_HOLD_DELAY [23:22] | | SELECT_SETUP_DELAY [21:20] | | None [19:19] | DESELECT_DELAY [18:16] | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | ENABLED [31:31] | None [30:25] | | | | | | BLOCK [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | XIP_MODE | RW | R | 0 | Mode of operation.<br><br>Note: this field should only be changed when the IP is disabled or when STATUS.BUSY is '0' and SW should not be executing from the XIP interface or MMIO interface. |
| | MMIO_MODE | | | 0 | '0': MMIO mode. Individual MMIO accesses to TX and RX FIFOs are used to generate a sequence of SPI transfers. This mode of operation allows for large flexibility in terms of the SPI transfers that can be generated. |
| | XIP_MODE | | | 1 | '1': XIP mode. eXecute-In-Place mode: incoming read and write transfers over the AHB-Lite bus infrastructure are automatically translated in SPI transfers to read data from and write data to a device. This mode of operation allow for efficient device read and write operations. This mode is only supported in SPI_MODE. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 4 | CLOCK_IF_TX_SEL | RW | R | 0 | Specifies device interface transmitter clock options.<br>'0': SDR. Memory interface clock 'spihb_clk_out' is divided (by 2) interface clock 'clk_if', memory interface data signals are driven by divided (by 2) interface clock 'clk_if' with different phase than 'spihb_clk_out'.<br>Results in driving memory interface data signals at falling 'spihb_clk_out' edge.<br>'1': DDR. Memory interface clock 'spihb_clk_out' is divided (by 2) inverted interface clock 'clk_if_inv', memory interface data signals are driven with interface clock 'clk_if'.<br>Results in driving memory interface data signals 90 degrees before rising and falling 'spihb_clk_out' edge. |
| 5:6 | DELAY_LINE_SEL | RW | R | 0 | Specifies the delay line used for RX data capturing with<br>- output / feedback clock based capturing (when CLOCK_IF_RX_SEL = [0..3] and DELAY_TAP_ENABLED = 1)<br>- internal clock based capturing (when CLOCK_IF_RX_SEL = [4..5], INT_CLOCK_CAPTURE_PRESENT = 1 and DELAY_TAP_ENABLED = 1)<br>- RWDS based capturing (when CLOCK_IF_RX_SEL = [6..7]) |
| 8 | DELAY_TAP_ENABLED | RW | R | 0 | Delay Line Tap Enable.<br>'0': Disabled. The delay line tap selections specified in registers DELAY_TAP_SEL or INT_CLOCK_DELAY_TAP_SEL0/1 are not used. The read data is directly captured by the RX data FIFO capture clock as specified by CLOCK_IF_RX_SEL and INT_CLOCK_CAPTURE_CYCLE.<br>'1': Enabled. The delay line tap selections specified in registers DELAY_TAP_SEL or INT_CLOCK_DELAY_TAP_SEL0/1 are used. Note that in RWDS based capture scheme (CLOCK_IF_RX_SEL = [6..7]), DELAY_TAP_ENABLED must be set to '1' as the RWDS based capture scheme requires to use the delay line.<br>If the output / feedback clock based capture scheme (CLOCK_IF_RX_SEL = [0..3]) or the RWDS based capture scheme (CLOCK_IF_RX_SEL = [6..7]) is selected then the register DELAY_TAP_SEL is used to select the capture clock. If the internal clock based capture scheme (CLOCK_IF_RX_SEL = [4..5] and INT_CLOCK_CAPTURE_PRESENT = 1) is selected then the registers INT_CLOCK_DELAY_TAP_SEL0/1 are used to select the capture clock per data bit line (read data is captured by the capture logic and afterwards transferred to the RX data FIFO). |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 12:14 | CLOCK_IF_RX_SEL | RW | R | 3 | Specifies device interface receiver clock 'clk_if_rx' source. MISO data is captured on the rising edge of 'clk_if_rx' in SDR mode and on both edges of 'clk_if_rx' in DDR mode.<br>'0': 'spi_clk_out' (output clock) for SDR capturing with output clock<br>'1': !'spi_clk_out' (output clock) for DDR or SDR capturing with inverted output clock<br>'2': 'spi_clk_in' (feedback clock) for SDR capturing with feedback clock<br>'3': !'spi_clk_in' (feedback clock) for DDR or SDR capturing with inverted feedback clock<br>'4': 'clk_if_tx' (internal clock) for DDR or SDR capturing with internal clock<br>'5': 'clk_if_tx_inv' (internal clock) for DDR or SDR capturing with inverted internal clock<br>'6': 'sphb_rwds_inv' (RWDS / DQS strobe signal driven by memory device) for DDR capturing with RWDS / DQS in Hyperbus / Octal SPI mode or for SDR capturing with falling RWDS / DQS edge in Octal SPI mode<br>'7': 'sphb_rwds' (RWDS / DQS strobe signal driven by memory device) for SDR capturing with rising RWDS / DQS edge in Octal SPI mode |
| 16:18 | DESELECT_DELAY | RW | R | 0 | Specifies the minimum duration of SPI deselection ('spi_select_out[]' is high/'1') in between SPI transfers:<br>'0': 1 memory interface clock cycle.<br>'1': 2 memory interface clock cycles.<br>'2': 3 memory interface clock cycles.<br>'3': 4 memory interface clock cycles.<br>'4': 5 memory interface clock cycles.<br>'5': 6 memory interface clock cycles.<br>'6': 7 memory interface clock cycles.<br>'7': 8 memory interface clock cycles.<br><br>During SPI deselection, 'spi_select_out[]' are '1'/inactive, 'spi_data_out[]' are '1' and 'spi_clk_out' is '0'/inactive. |
| 20:21 | SELECT_SETUP_DELAY | RW | R | 1 | Specifies the duration between 'spi_select_out[]' becomes low/'0') to 1st 'spi_clk_out' edge:<br>'0': 0 memory interface clock cycles + min. duration (see below).<br>'1': 1 memory interface clock cycle + min. duration (see below).<br>'2': 2 memory interface clock cycles + min. duration (see below).<br>'3': 3 memory interface clock cycles + min. duration (see below).<br><br>In addition to the number of cycles selected here there is a min. duration of:<br>- 1 memory interface clock cycle (= 2 clk_if cycle) for SDR timing (CLOCK_IF_TX_SEL = 0)<br>- 1/4 memory interface clock cycle (= 1/2 clk_if cycle) for DDR timing (CLOCK_IF_TX_SEL = 1) |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 22:23 | SELECT_HOLD_DELAY | RW | R | 1 | Specifies the duration between last 'spi_clk_out' edge to 'spi_select_out[]' becomes high/'1'):<br>'0': 0 memory interface clock cycles + min. duration (see below).<br>'1': 1 memory interface clock cycle + min. duration (see below).<br>'2': 2 memory interface clock cycles + min. duration (see below).<br>'3': 3 memory interface clock cycles + min. duration (see below).<br><br>In addition to the number of cycles selected here there is a min. duration of:<br>- 1/2 memory interface clock cycle (= 1 clk_if cycles) for SDR timing (CLOCK_IF_TX_SEL = 0)<br>- 1/4 memory interface clock cycle (= 1/2 clk_if cycle) for DDR timing (CLOCK_IF_TX_SEL = 1) |
| 24 | BLOCK | RW | R | 0 | Specifies what happens for MMIO interface read accesses to an empty RX data FIFO or to a full TX format/data FIFO. Note: the FIFOs can only be accessed in MMIO_MODE.<br><br>This field is not used for test controller accesses. |
| | BUS_ERROR | | | 0 | 0': Generate an AHB-Lite bus error. This option is useful when SW decides to use polling on STATUS.TR_BUSY to determine if a interface transfer is no longer busy (transfer is completed). This option adds SW complexity, but limits the number of AHB-Lite wait states (and limits ISR latency). |
| | WAIT_STATES | | | 1 | 1': Introduce wait states. This setting potentially locks up the AHB-Lite infrastructure and may increase the CPU interrupt latency.This option is useful when SW performs TX/RX data FIFO accesses immediately after a command is setup using the TX format FIFO. This option has low SW complexity, but may result in a significant number of AHB-Lite wait states (and may increase ISR latency). |
| 31 | ENABLED | RW | R | 0 | IP enable:<br>'0': Disabled. All non-retention registers are reset to their default value when the IP is disabled. When the IP is disabled, the XIP accesses produce AHB-Lite bus errors.<br>'1': Enabled.<br><br>Notes:<br>- Before disabling the IP, SW should ensure that the IP is NOT busy (STATUS.BUSY is '0'), otherwise illegal interface transfers may occur.<br>- After CTL.ENABLED is set to 1 it takes up to 20 clk_if cycles until the memory interface registers are realeased from reset. |
| | DISABLED | | | 0 | N/A |
| | ENABLED | | | 1 | N/A |

### 30.3.2 SMIF_STATUS

**Description:** Status
**Address:** 0x40420004
**Offset:** 0x4
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | BUSY [31:31] | None [30:24] | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 31 | BUSY | R | W | 0 | AHB Cache, AXI interface, cryptography, XIP, device interface or any other logic busy in the IP:<br>'0': not busy<br>'1': busy<br>When BUSY is '0', the IP can be safely disabled without:<br>- the potential loss of transient write data.<br>- the potential risk of aborting an inflight SPI device interface transfer.<br>When BUSY is '0', the mode of operation (XIP_MODE or MMIO_MODE) can be safely changed. |

### 30.3.3 SMIF_DELAY_TAP_SEL

**Description:** Delay Tap Select Register
**Address:** 0x40420030
**Offset:** 0x30
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x1

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:5] | | | SEL [4:0] | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:4 | SEL | RW | R | 1 | Delay line tap selection in output / feedback clock based capture scheme (CLOCK_IF_RX_SEL = [0..3]) and RWDS capture scheme (CLOCK_IF_RX_SEL = [6..7]). This is used to shift the strobe signal into the data eye.<br><br>Note: DELAY_TAP_SEL must not be changed while STATUS.BUSY=1. |

### 30.3.4 SMIF_TX_CMD_FIFO_STATUS

**Description:** Transmitter command FIFO status
**Address:** 0x40420044
**Offset:** 0x44
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** The TX command FIFO has 4 entries.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:4] | | | | USED4 [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | USED4 | R | W | 0 | Number of entries that are used in the TX command FIFO (available in both XIP_MODE and MMIO_MODE). Legal range: [0, 8]. |

### 30.3.5 SMIF_TX_CMD_FIFO_WR

**Description:** Transmitter command FIFO write
**Address:** 0x40420050
**Offset:** 0x50
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** A read from this register returns '0'. A write to this register in XIP_MODE results in an AHB-Lite bus error. A write to this register in MMIO_MODE writes the top of the FIFO.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA27 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA27 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA27 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:27] | | | | | DATA27 [26:24] | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:26 | DATA27 | W | R | 0 | Command data. The higher two bits DATA[26:24] specify the specific command<br><br>'0'/TX: A SPI transfer always start with a TX command FIFO entry of the 'TX' format.<br>- DATA[23:20] specifies which of the four devices are selected. DATA[23:20] are directly mapped to 'spi_select_out[3:0]'. Two devices can be selected at the same time in dual-quad mode.<br>- '0': device deselected<br>- '1': device selected<br>- DATA[19] specifies whether this is the last TX Byte; i.e. whether the 'spi_select_out[3:0]' IO output signals are de-activated after the transfer.<br>- '0': not the last TX byte<br>- '1': the last TX byte<br>- DATA[18] specifies the mode of transfer rate:<br>- '0': SDR mode<br>- '1': DDR mode<br>- DATA[17:16] specifies the width of the data transfer:<br>- '0': 1 bit/cycle (single data transfer).<br>- '1': 2 bits/cycle (dual data transfer).<br>- '2': 4 bits/cycle (quad data transfer).<br>- '3': 8 bits/cycle (octal data transfer).<br>- DATA[15:8] specifies the second transmitted Byte. This is only used (and must be specified) for octal data transfer with DDR mode, i.e. when DATA[17:16]='3' and DATA[18]='1'.<br>- DATA[7:0] specifies the transmitted Byte.<br><br>'1'/TX_COUNT: The 'TX_COUNT' command relies on the TX data FIFO to provide the transmitted bytes.<br>- DATA[19] specifies whether this is the last command of a data transfer; i.e. whether the 'spi_select_out[3:0]' IO output signals are de-activated after the transfer.<br>- DATA[18] specifies the mode of transfer rate.<br>- DATA[17:16] specifies the width of the transfer.<br>- DATA[15:0] specifies the number of to be transmitted memory data units (minus 1). '0': 1 unit, '1': 2 units. For SPI (except octal SPI with DDR) one memory data unit is a byte, for octal SPI with DDR and Hyperbus one memory data unit is a 2-byte word.<br>The number of used TX data FIFO entries (in TX_DATA_FIFO_STATUS) = number of memory data units to be transmitted.<br><br>'2'/RX_COUNT: The 'RX_COUNT' command relies on the RX data FIFO to accept the received bytes.<br>- DATA[19] specifies whether this is the last command of a data transfer; i.e. whether the 'spi_select_out[3:0]' IO output signals are de-activated after the transfer.<br>- DATA[18] specifies the mode of transfer rate.<br>- DATA[17:16] specifies the width of the transfer.<br>- DATA[15:0] specifies the number of to be received memory data units (minus 1). '0': 1 unit, '1': 2 units. For SPI (except octal SPI with DDR) one memory data unit is a byte, for octal SPI with DDR and Hyperbus one memory data unit is a 2-byte word.<br>The number of used RX data FIFO entries (in RX_DATA_FIFO_STATUS) = number of memory data units to be received * 8 / data width (1, 2, 4, 8).<br>The number of used RX data MMIO FIFO entries (in RX_DATA_MMIO_FIFO_STATUS) = number of bytes. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| | | | | | (Continuation)<br>'3'/DUMMY_COUNT: The 'DUMMY_COUNT' command conveys dummy cycles. Dummy cycles are used to implement a Turn-Around time in which the SPI master changes from a transmitter driving the data lines to a receiver receiving on the same data lines. The 'DUMMY_COUNT' command is ALWAYS considered to be NOT the last command of a SPI data transfer; i.e. it needs to be followed by another command.<br>- DATA[23] specifies whether RWDS / DQS based capturing is enabled in the last dummy cycle, i.e. this needs to be set to '1' for read transactions to memory device using RWDS / DQS capturing scheme.<br>- DATA[22] specifies whether data learning is enabled. In XIP mode this field is set for read transactions when CTL.INT_CLOCK_DL_ENABLED is '1').<br>- DATA[21] specifies whether the RWDS output signal should be driven starting in the last dummy cycle until DESELECT. This is needed for write transactions with RWDS (e.g. Hyperbus) before a TX_COUNT command.<br>- DATA[20] specifies whether an active RWDS refresh indicator (captured with the previous rising memory clock output) causes to double the number of dummy cycles. This is used for the variable latency in HyperRAM.<br>- DATA[18] specifies the mode of transfer rate. This is used for data learning and RWDS / DQS capturing. In XIP mode the field is taken from DEVICE.RD_DATA_CTL.DDR_MODE.<br>- DATA[17:16] specifies the width of the transfer. This is used for data learning and RWDS / DQS capturing. In XIP mode the field is taken from DEVICE.RD_DATA_CTL.WIDTH.<br>- DATA[15:0] specifies the number of dummy cycles (minus 1). In dummy cycles, the data lines are not driven.<br>Notes:<br>- If CLOCK_IF_TX_SEL = '0' for transmitting command, address and mode fields in SDR mode (driving data between falling edges of spihb_clk_out) and the memory is driving read data in DDR mode (based on memory type and transmitted command), then there must be at least 1 latency / dummy cycle specified (DUMMY_COUNT command must be present) to prevent controller and memory driving data signals at the same time.<br>The same is true for the theoretical (practically irrelevant case) of transmitting at least one of the command, address and mode fields in DDR mode but receiving data from the memory in SDR mode.<br>- When using the RWDS / DQS based capturing scheme (CTL.CLK_IF_RX_SEL=[6,7]), then there is a minimum number of latency / dummy cycles required (DUMMY_COUNT command must be present). For the Hyperbus protocol (DDR_CTL.SIZE3=7) at least 1 latency / dummy cycle has to be specified, for SPI with DQS capturing at least 2 latency / dummy cycles need to be selected (RD_DUMMY_CTL.SIZE5 > 0, exception see following note). |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| | | | | | (Continuation)<br>- In case of falling edge RWDS / DQS capturing (CTL.CLOCK_IF_RX_SEL = '6') and SDR mode, SW should reduce the number of dummy cycles by 1 compared to the latency cycles required by the memory device.<br><br>'4'/DESELECT: The 'DESELECT' command de-activates the 'spi'select_out[3:0] IO output signals. The 'DESELECT' command is ALWAYS considered to be the last command of an SPI data transfer. It is used to finish the last transfer of merged continuous transfers. |

### 30.3.6 SMIF_TX_DATA_FIFO_CTL

**Description:** Transmitter data FIFO control
**Address:** 0x40420080
**Offset:** 0x80
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** The TX data FIFO has 8 entries.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:3] | | | | | TX_TRIGGER_LEVEL [2:0] | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:2 | TX_TRIGGER_LEVEL | RW | R | 0 | Determines when the TX data FIFO 'tr_tx_req' trigger is activated (trigger activation requires MMIO_MODE, the trigger is NOT activated in XIP_MODE):<br>- Trigger is active when TX_DATA_FIFO_STATUS.USED <= TRIGGER_LEVEL. |

### 30.3.7 SMIF_TX_DATA_FIFO_STATUS

**Description:** Transmitter data FIFO status
**Address:** 0x40420084
**Offset:** 0x84
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** The TX data FIFO has 8 entries.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:4] | | | | USED4 [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | USED4 | R | W | 0 | Number of entries that are used in the TX data FIFO (available in both XIP_MODE and MMIO_MODE). Legal range: [0, 8]. |

### 30.3.8 SMIF_TX_DATA_FIFO_WR1

**Description:** Transmitter data FIFO write
**Address:** 0x40420090
**Offset:** 0x90
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** This register provides for single byte writes to the TX FIFO. MMIO register accesses must be 32-bit accesses.
Note: In case octal data transfer width and DDR mode (Hyperbus / Octal SPI) has been selected in TX_COUNT command via TX_CMD_FIFO_WR, i.e. 2 bytes are written in one cycle, the lower byte is written with DATA0 and the upper byte is masked (not written). This register must not be used for a word based memory protocol (Hyperbus / Octal SPI) without write byte masking.

A read from this register returns '0'. A write to this register in XIP_MODE results in an AHB-Lite bus error. A write to this register in MMIO_MODE writes the top entry of the FIFO.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA0 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | DATA0 | W | R | 0 | TX data (written to TX data FIFO). |

### 30.3.9 SMIF_TX_DATA_FIFO_WR2

**Description:** Transmitter data FIFO write
**Address:** 0x40420094
**Offset:** 0x94
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** This register provides for two simultaneous byte writes to the TX FIFO. MMIO register accesses must be 32-bit accesses.
Note:

A read from this register returns '0'. A write to this register in XIP_MODE results in an AHB-Lite bus error. A write to this register in MMIO_MODE writes the top two entries of the FIFO.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA0 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA1 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | DATA0 | W | R | 0 | TX data (written to TX data FIFO, first byte). |
| 8:15 | DATA1 | W | R | 0 | TX data (written to TX data FIFO, second byte). |

### 30.3.10 SMIF_TX_DATA_FIFO_WR4

**Description:** Transmitter data FIFO write
**Address:** 0x40420098
**Offset:** 0x98
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** This register provides for four simultaneous byte writes to the TX FIFO. MMIO register accesses must be 32-bit accesses.

A read from this register returns '0'. A write to this register in XIP_MODE results in an AHB-Lite bus error. A write to this register in MMIO_MODE writes the top four entrues of the FIFO.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA0 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA1 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA2 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA3 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | DATA0 | W | R | 0 | TX data (written to TX data FIFO, first byte). |
| 8:15 | DATA1 | W | R | 0 | TX data (written to TX data FIFO, second byte). |
| 16:23 | DATA2 | W | R | 0 | TX data (written to TX data FIFO, third byte). |
| 24:31 | DATA3 | W | R | 0 | TX data (written to TX data FIFO, fourth byte). |

### 30.3.11 SMIF_TX_DATA_FIFO_WR1ODD

**Description:** Transmitter data FIFO write
**Address:** 0x4042009C
**Offset:** 0x9C
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** This register provides for single byte writes to the TX FIFO for odd byte addresses when using a word based memory protocol (Hyperbus / Octal SPI). MMIO register accesses must be 32-bit accesses.
Note: In case octal data transfer width and DDR mode (Hyperbus / Octal SPI) has been selected in TX_COUNT command via TX_CMD_FIFO_WR, i.e. 2 bytes are written in one cycle, the upper byte is written with DATA0 and the lower byte is masked (not written). This register must not be used for a byte based memory protocol or for a word based memory protocol (Hyperbus / Octal SPI) without write byte masking.

A read from this register returns '0'. A write to this register in XIP_MODE results in an AHB-Lite bus error. A write to this register in MMIO_MODE writes the top entry of the FIFO.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA0 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | DATA0 | W | R | 0 | TX data (written to TX data FIFO). |

### 30.3.12 SMIF_RX_DATA_MMIO_FIFO_CTL

**Description:** Receiver data MMIO FIFO control
**Address:** 0x404200C0
**Offset:** 0xC0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** The RX data MMIO FIFO has 8 entries.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:3] | | | | | RX_TRIGGER_LEVEL [2:0] | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:2 | RX_TRIGGER_LEVEL | RW | R | 0 | Determines when RX data FIFO 'tr_rx_req' trigger is activated (trigger activation requires MMIO_MODE, the trigger is NOT activated in XIP_MODE):<br>- Trigger is active when RX_DATA_MMIO_FIFO_STATUS.USED > TRIGGER_LEVEL. |

### 30.3.13 SMIF_RX_DATA_MMIO_FIFO_STATUS

**Description:** Receiver data MMIO FIFO status
**Address:** 0x404200C4
**Offset:** 0xC4
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** The RX data MMIO FIFO has 8 entries.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:4] | | | | USED4 [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | USED4 | R | W | 0 | Number of entries that are used in the RX data MMIO FIFO (only available in MMIO_MODE). Legal range: [0, 8]. |

### 30.3.14 SMIF_RX_DATA_FIFO_STATUS

**Description:** Receiver data FIFO status
**Address:** 0x404200C8
**Offset:** 0xC8
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** The RX data FIFO has 16 entries.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:5] | | | USED5 [4:0] | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:9] | | | | | | | RX_SR _USED [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:4 | USED5 | R | W | 0 | Number of entries that are used in the RX data FIFO (available in both XIP_MODE and MMIO_MODE). Legal range: [0, 16]. |
| 8 | RX_SR_USED | R | W | 0 | Data available in RX Shift Register, i.e. completely read from RX data FIFO (availabe in both XIP_MODE and MMIO_MODE). |

### 30.3.15 SMIF_RX_DATA_MMIO_FIFO_RD1

**Description:** Receiver data MMIO FIFO read
**Address:** 0x404200D0
**Offset:** 0xD0
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** This register provides a single byte from the RX data MMIO FIFO: a read from this register in MMIO_MODE reads the top entry of the FIFO. MMIO register accesses must be 32-bit accesses.

A write to this register is ignored (no AHB-Lite bus error is generated). A read from this register in XIP_MODE results in an AHB-Lite bus error.

Non test controller read accesses (AHB-Lite bus master identifier is NOT '15') when the RX FIFO is empty behave as specified by CTL.BLOCK and the RX_DATA_FIFO_UNDERFLOW interrupt cause is set to '1'.

Test controller (AHB-Lite bus master identifier is '15') read accesses behave the same as RX_DATA_FIFO_RD1_SILENT read accesses.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA0 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | DATA0 | R | W | 0 | RX data (read from RX data FIFO). |

### 30.3.16 SMIF_RX_DATA_MMIO_FIFO_RD2

**Description:** Receiver data MMIO FIFO read
**Address:** 0x404200D4
**Offset:** 0xD4
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** This register provides two bytes from the RX data MMIO FIFO: a read from this register in MMIO_MODE reads the top two entries of the FIFO. MMIO register accesses must be 32-bit accesses.

A write to this register is ignored (no AHB-Lite bus error is generated). A read from this register in XIP_MODE results in an AHB-Lite bus error.

Non test controller read accesses (AHB-Lite bus master identifier is NOT '15') when the RX FIFO is empty behave as specified by CTL.BLOCK and the RX_DATA_FIFO_UNDERFLOW interrupt cause is set to '1'.

Test controller (AHB-Lite bus master identifier is '15') read accesses ALWAYS result in an AHB-Lite bus error. Test controller read accesses do NOT affect the RX_DATA_FIFO_UNDERFLOW interrupt cause.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA0 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA1 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | DATA0 | R | W | 0 | RX data (read from RX data FIFO, first byte). |
| 8:15 | DATA1 | R | W | 0 | RX data (read from RX data FIFO, second byte). |

### 30.3.17 SMIF_RX_DATA_MMIO_FIFO_RD4

**Description:** Receiver data MMIO FIFO read
**Address:** 0x404200D8
**Offset:** 0xD8
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** This register provides four bytes from the RX data MMIO FIFO: a read from this register in MMIO_MODE reads the top four entries of the FIFO. MMIO register accesses must be 32-bit accesses.

A write to this register is ignored (no AHB-Lite bus error is generated). A read from this register in XIP_MODE results in an AHB-Lite bus error.

Non test controller read accesses (AHB-Lite bus master identifier is NOT '15') when the RX FIFO is empty behave as specified by CTL.BLOCK and the RX_DATA_FIFO_UNDERFLOW interrupt cause is set to '1'.

Test controller (AHB-Lite bus master identifier is '15') read accesses ALWAYS result in an AHB-Lite bus error. Test controller read accesses do NOT affect the RX_DATA_FIFO_UNDERFLOW interrupt cause.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA0 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA1 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA2 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA3 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | DATA0 | R | W | 0 | RX data (read from RX data FIFO, first byte). |
| 8:15 | DATA1 | R | W | 0 | RX data (read from RX data FIFO, second byte). |
| 16:23 | DATA2 | R | W | 0 | RX data (read from RX data FIFO, third byte). |
| 24:31 | DATA3 | R | W | 0 | RX data (read from RX data FIFO, fourth byte). |

### 30.3.18 SMIF_RX_DATA_MMIO_FIFO_RD1_SILENT

**Description:** Receiver data MMIO FIFO silent read
**Address:** 0x404200E0
**Offset:** 0xE0
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** This register is similar to RX_DATA_MMIO_FIFO_RD1, with the exception that the entry is NOT removed from the FIFO. MMIO register accesses must be 32-bit accesses.

A write to this register is ignored (no AHB-Lite bus error is generated). A read from this register in XIP_MODE results in an AHB-Lite bus error.

A read from this register when the RX FIFO is empty results in the return of the value 0xffff_ffff (independent of CTL.BLOCK). Read accesses do NOT affect the RX_DATA_FIFO_UNDERFLOW interrupt cause.

Note: this register is intended to be used by the test controller (AHB-Lite bus master identifier is '15'), but can also be used by other bus masters).
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DATA0 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | DATA0 | R | W | 0 | RX data (read from RX data FIFO). |

### 30.3.19 SMIF_SLOW_CA_CTL

**Description:** Slow cache control
**Address:** 0x40420100
**Offset:** 0x100
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** The slow interface/port is used for the CPUSS CM0+, CRYPTO and DataWire components. Note: cache memory and control information are NOT retained in DeepSleep power mode.
**Default:** 0xC0000000

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:18] | | | | | | WAY [17:16] | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | ENABLED [31:31] | PREF_EN [30:30] | None [29:26] | | | | SET_ADDR [25:24] | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 16:17 | WAY | RW | R | 0 | this is for debug purpose only, and should be hidden to customers in technical document |
| 24:25 | SET_ADDR | RW | R | 0 | this is for debug purpose only, and should be hidden to customers in technical document |
| 30 | PREF_EN | RW | R | 1 | Prefetch enable:<br>'0': Disabled.<br>'1': Enabled.<br><br>Prefetching requires the cache to be enabled; i.e. ENABLED is '1'. |
| 31 | ENABLED | RW | R | 1 | Cache enable:<br>'0': Disabled.<br>'1': Enabled. |

### 30.3.20 SMIF_SLOW_CA_CMD

**Description:** Slow cache command
**Address:** 0x40420108
**Offset:** 0x108
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:1] | | | | | | | INV [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | INV | RW1S | RW1C | 0 | Cache and prefetch buffer invalidation.<br>SW writes a '1' to clear the cache and prefetch buffer. The cache's LRU structure is also reset to its default state.<br>Note,<br>A write access will invalidate the prefetch buffer automatically in hardware.<br>A write access should invalidate both fast and slow caches, by firmware.<br>Note, firmware should invalidate the cache and prefetch buffer only when STATUS.BUSY is '0'. |

### 30.3.21 SMIF_CRYPTO_CMD

**Description:** Cryptography Command
**Address:** 0x40420200
**Offset:** 0x200
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** This register starts an encryption operation.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:1] | | | | | | | START [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | START | RW1S | RW1C | 0 | SW sets this field to '1' to start a AES-128 forward block cipher operation (on the address in CRYPTO_ADDR). HW sets this field to '0' to indicate that the operation has completed. Once completed, the result of the operation can be read from CRYPTO_RESULT0, ..., CRYPTO_RESULT3.<br><br>The operation takes roughly 13 clk_mem clock cycles.<br><br>Note: An operation can only be started in MMIO_MODE. |

### 30.3.22 SMIF_CRYPTO_INPUT0

**Description:** Cryptography input 0
**Address:** 0x40420220
**Offset:** 0x220
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** The CRYPT_INPUT0, ..., CRYPTO_INPUT3 registers provide the plaintext PT[127:0]. The plaintext PT[127:0] is the input to the AES-128 forward block cipher.

These registers are ONLY used in MMIO_MODE. In XIP_MODE, the AHB-Lite bus transfer address CRYPTO_INPUT3, CRYPTO_INPUT2, CRYPTO_INPUT1, A[31:4] and CRYPTO_INPUT0.INPUT[3:0] are used as the plaintext PT[127:0] (the CRYPTO_INPUT0 register is partially used) of the block cipher.

These register should NOT be changed when the IP is busy; i.e. STATUS.BUSY is '1'.
**Default:** Undefined as one or more bit fields have a default value that is undefined

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | INPUT [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | INPUT [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | INPUT [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | INPUT [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | INPUT | RW | R | Undefined | Four Bytes of the plaintext PT[31:0] = CRYPTO_INPUT0.INPUT[31:0]. |

### 30.3.23 SMIF_CRYPTO_INPUT1

**Description:** Cryptography input 1
**Address:** 0x40420224
**Offset:** 0x224
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** Undefined as one or more bit fields have a default value that is undefined

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | INPUT [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | INPUT [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | INPUT [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | INPUT [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | INPUT | RW | R | Undefined | Four Bytes of the plaintext PT[63:32] = CRYPTO_INPUT1.INPUT[31:0]. |

### 30.3.24 SMIF_CRYPTO_INPUT2

**Description:** Cryptography input 2
**Address:** 0x40420228
**Offset:** 0x228
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** Undefined as one or more bit fields have a default value that is undefined

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | INPUT [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | INPUT [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | INPUT [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | INPUT [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | INPUT | RW | R | Undefined | Four Bytes of the plaintext PT[95:64] = CRYPTO_INPUT2.INPUT[31:0]. |

### 30.3.25 SMIF_CRYPTO_INPUT3

**Description:** Cryptography input 3
**Address:** 0x4042022C
**Offset:** 0x22C
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** Undefined as one or more bit fields have a default value that is undefined

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | INPUT [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | INPUT [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | INPUT [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | INPUT [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | INPUT | RW | R | Undefined | Four Bytes of the plaintext PT[127:96] = CRYPTO_INPUT3.INPUT[31:0]. |

### 30.3.26 SMIF_CRYPTO_KEY0

**Description:** Cryptography key 0
**Address:** 0x40420240
**Offset:** 0x240
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** The CRYPTO_KEY3, ..., CRYPTO_KEY0 registers provide the key KEY[127:0]. The key KEY[127:0] is the key of the AES-128 forward block cipher.

SW ALWAYS reads '0' from these registers.

These register should NOT be changed when the IP is busy; i.e. STATUS.BUSY is '1'.
**Default:** Undefined as one or more bit fields have a default value that is undefined

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | KEY [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | KEY [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | KEY [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | KEY [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | KEY | W | R | Undefined | Four Bytes of the key KEY[31:0] = CRYPTO_KEY0.KEY[31:0]. |

### 30.3.27 SMIF_CRYPTO_KEY1

**Description:** Cryptography key 1
**Address:** 0x40420244
**Offset:** 0x244
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** Undefined as one or more bit fields have a default value that is undefined

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | KEY [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | KEY [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | KEY [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | KEY [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | KEY | W | R | Undefined | Four Bytes of the key KEY[63:32] = CRYPTO_KEY1.KEY[31:0]. |

### 30.3.28 SMIF_CRYPTO_KEY2

**Description:** Cryptography key 2
**Address:** 0x40420248
**Offset:** 0x248
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** Undefined as one or more bit fields have a default value that is undefined

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | KEY [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | KEY [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | KEY [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | KEY [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | KEY | W | R | Undefined | Four Bytes of the key KEY[95:64] = CRYPTO_KEY2.KEY[31:0]. |

### 30.3.29 SMIF_CRYPTO_KEY3

**Description:** Cryptography key 3
**Address:** 0x4042024C
**Offset:** 0x24C
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** Undefined as one or more bit fields have a default value that is undefined

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | KEY [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | KEY [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | KEY [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | KEY [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | KEY | W | R | Undefined | Four Bytes of the key KEY[127:96] = CRYPTO_KEY3.KEY[31:0]. |

### 30.3.30 SMIF_CRYPTO_OUTPUT0

**Description:** Cryptography output 0
**Address:** 0x40420260
**Offset:** 0x260
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** The CRYPTO_OUTPUT3, ..., CRYPTO_OUTPUT0 registers provide the ciphertext CT[127:0]. The ciphertext CT[127:0] is the output of the AES-128 forward block cipher. The block cipher use the plaintext PT[127:0] as input (CRYPTO_INPUT3, ..., CRYPTO_INPUT0) and key KEY[127:0] as the key (CRYPTO_KEY3, ..., CRYPTO_KEY0).

These registers are ONLY used in MMIO_MODE. In XIP_MODE, the ciphertext CT[127:0] is used (CRYPTO_OUTPUT3, ..., CRYPTO_OUTPUT0 registers are not used) to XOR the plaintext data PD[127:0] (for write operations) or ciphertext CD[127:0] (for read operations).

These register should NOT be changed when the IP is busy; i.e. STATUS.BUSY is '1'.
**Default:** Undefined as one or more bit fields have a default value that is undefined

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | OUTPUT [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | OUTPUT [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | OUTPUT [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | OUTPUT [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | OUTPUT | RW | A | Undefined | Four Bytes of the ciphertext CT[31:0] = CRYPTO_OUTPUT0.OUTPUT[31:0]. |

### 30.3.31 SMIF_CRYPTO_OUTPUT1

**Description:** Cryptography output 1
**Address:** 0x40420264
**Offset:** 0x264
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** Undefined as one or more bit fields have a default value that is undefined

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | OUTPUT [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | OUTPUT [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | OUTPUT [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | OUTPUT [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | OUTPUT | RW | A | Undefined | Four Bytes of the ciphertext CT[63:32] = CRYPTO_OUTPUT1.OUTPUT[31:0]. |

### 30.3.32 SMIF_CRYPTO_OUTPUT2

**Description:** Cryptography output 2
**Address:** 0x40420268
**Offset:** 0x268
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** Undefined as one or more bit fields have a default value that is undefined

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | OUTPUT [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | OUTPUT [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | OUTPUT [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | OUTPUT [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | OUTPUT | RW | A | Undefined | Four Bytes of the ciphertext CT[95:64] = CRYPTO_OUTPUT2.OUTPUT[31:0]. |

### 30.3.33 SMIF_CRYPTO_OUTPUT3

**Description:** Cryptography output 3
**Address:** 0x4042026C
**Offset:** 0x26C
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** Undefined as one or more bit fields have a default value that is undefined

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | OUTPUT [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | OUTPUT [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | OUTPUT [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | OUTPUT [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | OUTPUT | RW | A | Undefined | Four Bytes of the ciphertext CT[127:96] = CRYPTO_OUTPUT3.OUTPUT[31:0]. |

### 30.3.34 SMIF_INTR

**Description:** Interrupt register
**Address:** 0x404207C0
**Offset:** 0x7C0
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** The IP has a single Active functionality interrupt. The interrupt causes are described in this register. Interrupt causes are only activated when the IP is enabled; i.e. CTL.ENABLED is '1'.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:6] | | RX_DATA_MMIO_FIFO_UNDERFLOW [5:5] | TX_DATA_FIFO_OVERFLOW [4:4] | TX_CMD_FIFO_OVERFLOW [3:3] | XIP_ALIGNMENT_ERROR [2:2] | TR_RX_REQ [1:1] | TR_TX_REQ [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | TR_TX_REQ | RW1C | RW1S | 0 | Activated in MMIO mode, when a TX data FIFO trigger 'tr_tx_req' is activated. |
| 1 | TR_RX_REQ | RW1C | RW1S | 0 | Activated in MMIO mode, when a RX data FIFO trigger 'tr_rx_req' is activated. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 2 | XIP_ALIGNMENT _ERROR | RW1C | RW1S | 0 | Activated in XIP mode, when:<br>- a write transfer is requested<br>and<br>- Dual-Quad SPI mode (selected device's ADDR_CTL.DIV2 is '1') is selected or<br>- Octal SPI DDR mode (selected device's DATA_CTL.DDR_MODE = '1' and DATA_CTL.WIDTH = '3') or Hyperbus mode (selected device's ADDR_CTL.SIZE3 = '7') is selected without memory write byte masking (selected device's WR_DUMMY_CTL.RWDS_EN = '0')<br>and<br>- the AHB-Lite / AXI bus transfer address is not a multiple of '2' or<br>- the requested AHB-Lite / AXI bus transfer size is NOT a multiple of '2'.<br><br>Additionally, it is activated in XIP mode when the selected memory device does not support write byte masking (WR_DUMMY_CTL.RWDS_EN=0) and an AXI transfer occurs with not all of the AXI write strobes ('wstrb') enabled according to the transfer size ('assize').<br><br>Note: In dual-quad SPI mode (ADDR_CTL.DIV is '1'), each memory device contributes a 4-bit nibble for read data or write data. Write accesses are only possible if the request address is a multiple of 2 and the number of requested Bytes is a multiple of 2. Octal SPI DDR mode or Hyperbus mode are 16-bit word based protocols, writing single bytes is only possible when write byte masking is supported (via RWDS). Read accesses are always possible by extending the transfer size and / or aligning the address as needed and discarding the non-relevant byte(s). |
| 3 | TX_CMD_FIFO _OVERFLOW | RW1C | RW1S | 0 | Activated in MMIO mode, on an AHB-Lite write transfer to the TX command FIFO (TX_CMD_FIFO_WR) with not enough free entries available. |
| 4 | TX_DATA_FIFO _OVERFLOW | RW1C | RW1S | 0 | Activated in MMIO mode, on an AHB-Lite write transfer to the TX data FIFO (TX_DATA_FIFO_WR1, TX_DATA_FIFO_WR2, TX_DATA_FIFO_WR4) with not enough free entries available. |
| 5 | RX_DATA_MMIO_FIFO _UNDERFLOW | RW1C | RW1S | 0 | Activated in MMIO mode, on an AHB-Lite read transfer from the RX data MMIO FIFO (RX_DATA_MMIO_FIFO_RD1, RX_DATA_MMIO_FIFO_RD2, RX_DATA_MMIO_FIFO_RD4) with not enough entries available. Only activated for NON test bus controller transfers. |

### 30.3.35 SMIF_INTR_SET

**Description:** Interrupt set register
**Address:** 0x404207C4
**Offset:** 0x7C4
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** When read, this register reflects the interrupt request register. For debug purposes, SW can write a '1' to trigger the cause of an interrupt.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:6] | | RX_DATA_MMIO_FIFO_UNDERFLOW [5:5] | TX_DATA_FIFO_OVERFLOW [4:4] | TX_CMD_FIFO_OVERFLOW [3:3] | XIP_ALIGNMENT_ERROR [2:2] | TR_RX_REQ [1:1] | TR_TX_REQ [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | TR_TX_REQ | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt request register. |
| 1 | TR_RX_REQ | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt request register. |
| 2 | XIP_ALIGNMENT_ERROR | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt request register. |
| 3 | TX_CMD_FIFO_OVERFLOW | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt request register. |
| 4 | TX_DATA_FIFO_OVERFLOW | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt request register. |
| 5 | RX_DATA_MMIO_FIFO_UNDERFLOW | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt request register. |

### 30.3.36 SMIF_INTR_MASK

**Description:** Interrupt mask register
**Address:** 0x404207C8
**Offset:** 0x7C8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:6] | | RX_DATA_MMIO_FIFO_UNDERFLOW [5:5] | TX_DATA_FIFO_OVERFLOW [4:4] | TX_CMD_FIFO_OVERFLOW [3:3] | XIP_ALIGNMENT_ERROR [2:2] | TR_RX_REQ [1:1] | TR_TX_REQ [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | TR_TX_REQ | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |
| 1 | TR_RX_REQ | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |
| 2 | XIP_ALIGNMENT_ERROR | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |
| 3 | TX_CMD_FIFO_OVERFLOW | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |
| 4 | TX_DATA_FIFO_OVERFLOW | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |
| 5 | RX_DATA_MMIO_FIFO_UNDERFLOW | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |

### 30.3.37 SMIF_INTR_MASKED

**Description:** Interrupt masked register
**Address:** 0x404207CC
**Offset:** 0x7CC
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** When read, this register reflects a bitwise and between the interrupt request and mask registers.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:6] | | RX_DATA_MMIO_FIFO_UNDERFLOW [5:5] | TX_DATA_FIFO_OVERFLOW [4:4] | TX_CMD_FIFO_OVERFLOW [3:3] | XIP_ALIGNMENT_ERROR [2:2] | TR_RX_REQ [1:1] | TR_TX_REQ [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | TR_TX_REQ | R | W | 0 | Logical and of corresponding request and mask bits. |
| 1 | TR_RX_REQ | R | W | 0 | Logical and of corresponding request and mask bits. |
| 2 | XIP_ALIGNMENT_ERROR | R | W | 0 | Logical and of corresponding request and mask bits. |
| 3 | TX_CMD_FIFO_OVERFLOW | R | W | 0 | Logical and of corresponding request and mask bits. |
| 4 | TX_DATA_FIFO_OVERFLOW | R | W | 0 | Logical and of corresponding request and mask bits. |
| 5 | RX_DATA_MMIO_FIFO_UNDERFLOW | R | W | 0 | Logical and of corresponding request and mask bits. |

### 30.3.38 DEVICE

#### 30.3.38.1 SMIF_DEVICE_CTL

**Description:** Control
**Address:** 0x40420800
**Offset:** 0x0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register is only used in XIP_MODE (except for the DATA_SEL field, which is used in bot the XIP_MODE and MMIO_MODE).
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:5] | | | CRYPTO_EN [4:4] | None [3:1] | | | WR_EN [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | MERGE_EN [15:15] | MERGE_TIMEOUT [14:12] | | | None [11:10] | | DATA_SEL [9:8] | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | TOTAL_TIMEOUT [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | ENABLED [31:31] | TOTAL_TIMEOUT_EN [30:30] | TOTAL_TIMEOUT [29:24] | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | WR_EN | RW | R | 0 | Write enable:<br>'0': write transfers are not allowed to this device. An attempt to write to this device results in an AHB-Lite bus error.<br>'1': write transfers are allowed to this device. |
| 4 | CRYPTO_EN | RW | R | 0 | Cryptography on read/write accesses:<br>'0': disabled.<br>'1': enabled. |
| 8:9 | DATA_SEL | RW | R | 0 | Specifies the connection of the IP's data lines (spi_data[0], ..., spi_data[7]) to the device's data lines (SI/IO0, SO/IO1, IO2, IO3, IO4, IO5, IO6, IO7):<br>'0': spi_data[0] = IO0, spi_data[1] = IO1, ..., spi_data[7] = IO7. This value is allowed for single, dual, quad, dual quad and octal SPI modes. This value must be used for the first device in dual quad SPI mode. This value must be used for octal SPI mode.<br>'1': spi_data[2] = IO0, spi_data[3] = IO1. This value is only allowed for single and dual SPI modes.<br>'2': spi_data[4] = IO0, spi_data[5] = IO1, ..., spi_data[7] = IO3. This value is only allowed for single, dual, quad and dual quad SPI modes. In dual quad SPI mode, this value must be used for the second device.<br>'3': spi_data[6] = IO0, spi_data[7] = IO1. This value is only allowed for single and dual SPI modes. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 12:14 | MERGE_TIMEOUT | RW | R | 0 | Continuous transfer merge timeout in clk_mem cycles. This limits the standby time of the memory interface, i.e. the time the memory device is selected but no data is transferred.<br>The counting of the merge timeout period is done in the XIP block using clk_mem cycles. It starts when the last TX or RX byte is transferred to or from the data FIFOs.<br>After this period the memory device is deselected. A later transfer, even from a continuous address, starts with the overhead phases (command, address, mode, dummy cycles). |
| | _1_cycle | | | 0 | Timeout after 1 clk_mem cycle.<br>That means transfers will only be merged if the continuous transfer request is already available when the previous transfer is finished. |
| | _16_cycles | | | 1 | Timeout after 2^4 = 16 clk_mem cycles.<br>At a clk_mem frequency of 200MHz this means 80ns. |
| | _256_cycles | | | 2 | Timeout after 2^8 = 256 clk_mem cycles.<br>At a clk_mem frequency of 200MHz this means ~1.3us. |
| | _4096_cycles | | | 3 | Timeout after 2^12 = 4096 clk_mem cycles.<br>At a clk_mem frequency of 200MHz this means ~20us. |
| | _65536_cycles | | | 4 | Timeout after 2^16 = 65536 clk_mem cycles.<br>At a clk_mem frequency of 200MHz this means ~330us. |
| | Reserved5 | | | 5 | N/A |
| | Reserved6 | | | 6 | N/A |
| | Reserved7 | | | 7 | N/A |
| 15 | MERGE_EN | RW | R | 0 | Continous transfer merge enable:<br>'0': Disabled. No merging of transfers is done. Longest possible memory transfer is 16 Byte.<br>'1': Enabled. Merging of continous transfers is done. This skips the overhead (command, address, mode, dummy cycles) for a continuous (linear sequential) transfer. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 16:29 | TOTAL_TIMEOUT | RW | R | 0 | Total transfer timeout in clk_mem cycles.<br>The counting of the total timout period is done in the XIP block using clk_mem cycles. It starts when the first command of a new (not merged) transaction is transferred to the TX command FIFO causing the interface logic to select the memory.<br>After this period the memory device is deselected.<br><br>This feature is needed for RAM devices requiring refresh cycles. The value needs to be derived from the RAMs maximum transaction length time (tCMS) minus the time of transferring 2x16byte data block (data granularity of the XIP ports is 16byte, 1 16byte block transfer outstanding, another available for merging). If the result in negative, MERGE_EN must be set to '0'.<br><br>Example: RAM device tCMS = 4us, interface clock frequency = 100MHz: total transfer timeout is 4us - 2x16x10ns = 3680ns.<br>With clk_mem frequency of 200MHz the TOTAL_TIMEOUT value is 3680/5 = 736.<br><br>Note: In the unlikely case that the total transfer timeout is used (usually for RAM devices) while the page boundary crossing latency generation is enabled via RD_BOUND_CTL.PRESENT (usually for FLASH devices) the additional time needs to taken into account. |
| 30 | TOTAL_TIMEOUT_EN | RW | R | 0 | Total transfer timeout enable.<br>'0': Disabled. There is no limit for the total transfer time. The continuous transfer merge timeout for limiting the idle time of the memory interface still applies.<br>'1': Enabled. The maximum total transfer time is limited by field TOTAL_TIMEOUT. |
| 31 | ENABLED | RW | R | 0 | Device enable:<br>'0': Disabled.<br>'1': Enabled. |

### 30.3.38.2 SMIF_DEVICE_ADDR

**Description:** Device region base address
**Address:** 0x40420808
**Offset:** 0x8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register is only used in XIP_MODE.
**Default:** Undefined as one or more bit fields have a default value that is undefined

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDR [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDR [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | ADDR [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 8:31 | ADDR | RW | A | Undefined | Specifies the base address of the device region. If the device region is 2^m Bytes, ADDR MUST be a multiple of 2^m.<br><br>In dual quad SPI data transfer, the two devices should have the same ADDR and MASK register settings. The device control information (ADDR_CTL, RD_CMD_CTL, etc.) are provided by the MMIO control registers of the device with the lowest index.<br><br>The most significant bit fields are constants and set based on the SMIF_XIP_ADDR parameter. The most significant bits are identified on the SMIF_XIP_MASK parameter. E.g., if SMIF_XIP_MASK is 0xff00:0000 (16 MB XIP memory region), ADDR[31:24] = SMIF_XIP_ADDR[31:24]. |

### 30.3.38.3 SMIF_DEVICE_MASK

**Description:** Device region mask
**Address:** 0x4042080C
**Offset:** 0xC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register is only used in XIP_MODE.
**Default:** Undefined as one or more bit fields have a default value that is undefined

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | MASK [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | MASK [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | MASK [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 8:31 | MASK | RW | A | Undefined | Specifies the size of the device region. All '1' bits are used to compare the incoming transfer request address A[31:0] with the address as specified in ADDR.ADDR: Address A is in the device when (A[31:8] & MASK[31:8]) == ADDR.ADDR[31:8].<br><br>The most significant bit fields are constants and set to'1'. The most significant bits are identified on the SMIF_XIP_MASK parameter. E.g., if SMIF_XIP_MASK is 0xff00:0000 (16 MB XIP memory region), MASK[31:24] = 0xff.<br><br>Note: a transfer request that is not in any device region results in an AHB-Lite bus error. |

### 30.3.38.4 SMIF_DEVICE_ADDR_CTL

**Description:** Address control
**Address:** 0x40420820
**Offset:** 0x20
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register is only used in XIP_MODE.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:3] | | | | | SIZE3 [2:0] | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:9] | | | | | | | DIV2 [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:2 | SIZE3 | RW | R | 0 | Specifies the size of the XIP device address in Bytes:<br>'0': 1 Byte address.<br>'1': 2 Byte address.<br>'2': 3 Byte address.<br>'3': 4 Byte address.<br>'4'-'6': These settings are reserved. Do not use.<br>'7': 4 Byte address (spread over 5 bytes) according to Hyperbus protocol.<br>The lower significant address Bytes of the transfer request are used as XIP address to the external device. Note that for dual quad SPI data transfer, the XIP transfer request address is divided by 2. Therefore, the XIP transfer request address needs to be a multiple of 2. If the address is NOT a multiple of 2, the XIP_ALIGNMENT_ERROR interrupt cause is activated.<br><br>Note: If Hyperbus protocol is selected (SIZE3='7') then the WIDTH field must be set to '3' (octal data transfer) and the DDR_MODE field must be set to '1' (DDR mode) in the read/write command and address control registers, and the PRESENT field in read/write command control registers need be set to '1' (1 command byte). |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 8 | DIV2 | RW | R | 0 | Specifies if the AHB-Lite bus transfer address is divided by 2 or not:<br>'0': No divide by 2.<br>'1': Divide by 2.<br><br>This functionality is used for read and write operation in XIP, dual quad SPI mode; i.e. this DIV2 must be set to '1' in dual quad SPI mode.<br>If DIV2 is set to '1', the memory does not support write masking (WR_DUMMY_CTL.RWDS_EN = '0'), and in this configuration a write transfer is requested and the write transfer request address is NOT a multiple of 2 or the requested number of Bytes to be written is not a multiple of 2, the XIP_ALIGNMENT_ERROR interrupt cause is activated. |

### 30.3.38.5 SMIF_DEVICE_RD_CMD_CTL

**Description:** Read command control
**Address:** 0x40420840
**Offset:** 0x40
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register is only used in XIP_MODE.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | CODE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | CODEH [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:19] | | | | | DDR _MODE [18:18] | WIDTH [17:16] | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | PRESENT2 [31:30] | | None [29:24] | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | CODE | RW | R | 0 | Command byte code. |
| 8:15 | CODEH | RW | R | 0 | Command high byte code.<br>This field specifies the most significant command byte, sent before the least significant command byte (CODE). It is only used when PRESENT2 = '2'. |
| 16:17 | WIDTH | RW | R | 0 | Width of data transfer:<br>'0': 1 bit/cycle (single data transfer).<br>'1': 2 bits/cycle (dual data transfer).<br>'2': 4 bits/cycle (quad data transfer).<br>'3': 8 bits/cycle (octal data transfer). |
| 18 | DDR_MODE | RW | R | 0 | Mode of transfer rate:<br>'0': SDR mode<br>'1': DDR mode |
| 30:31 | PRESENT2 | RW | R | 0 | Presence of command field:<br>'0': not present<br>'1': present (1 Byte)<br>'2': present (2 Byte for OPI)<br><br>Note: For octal data transfer with DDR mode (WIDTH='3' and DDR_MODE='1') either the HB protocol needs to be selected (by ADDR_CTL.SIZE3='7') or this field needs to be set to PRESENT2='2'. |

### 30.3.38.6 SMIF_DEVICE_RD_ADDR_CTL

**Description:** Read address control
**Address:** 0x40420844
**Offset:** 0x44
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register is only used in XIP_MODE.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:19] | | | | | DDR_MODE [18:18] | WIDTH [17:16] | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 16:17 | WIDTH | RW | R | 0 | Width of transfer. |
| 18 | DDR_MODE | RW | R | 0 | Mode of transfer rate. |

### 30.3.38.7 SMIF_DEVICE_RD_MODE_CTL

**Description:** Read mode control
**Address:** 0x40420848
**Offset:** 0x48
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register is only used in XIP_MODE.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | CODE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | CODEH [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:19] | | | | | DDR _MODE [18:18] | WIDTH [17:16] | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | PRESENT2 [31:30] | | None [29:24] | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | CODE | RW | R | 0 | Mode byte code.<br>Note: If a mode field is present (PRESENT='1') for octal data transfer with DDR mode (WIDTH='3' and DDR_MODE='1') the CODE is sent twice. |
| 8:15 | CODEH | RW | R | 0 | Mode high byte code.<br>This field specifies the most significant mode byte, sent before the least significant mode byte (CODE). It is only used when PRESENT2 = '2'. |
| 16:17 | WIDTH | RW | R | 0 | Width of transfer. |
| 18 | DDR_MODE | RW | R | 0 | Mode of transfer rate. |
| 30:31 | PRESENT2 | RW | R | 0 | Presence of mode field:<br>'0': not present<br>'1': present (1 Byte)<br>'2': present (2 Byte for OPI)<br><br>Note: For octal data transfer with DDR mode (WIDTH='3' and DDR_MODE='1') this field needs to be set to PRESENT2='2' to generate a mode field (or to PRESENT2='0'). |

### 30.3.38.8 SMIF_DEVICE_RD_DUMMY_CTL

**Description:** Read dummy control
**Address:** 0x4042084C
**Offset:** 0x4C
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register is only used in XIP_MODE.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:5] | | | SIZE5 [4:0] | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | PRESENT2 [31:30] | | None [29:24] | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:4 | SIZE5 | RW | R | 0 | Number of dummy cycles (minus 1):<br>'0': 1 cycles<br>...<br>'31': 32 cycles.<br><br>Note: this field specifies dummy cycles, not dummy Bytes! |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 30:31 | PRESENT2 | RW | R | 0 | Presence of dummy cycles:<br>'0': not present<br>'1': present<br>'2': present - Dummy cycles are doubled when RWDS refresh indicator is high during CA cycle. (HyperRAM variable latency mode)<br><br>Notes:<br>- If CLOCK_IF_TX_SEL = '0' for transmitting command, address and mode fields in SDR mode (driving data between falling edges of spihb_clk_out) and the memory is driving read data in DDR mode (based on memory type and transmitted command), then there must be at least 1 latency / dummy cycle specified (RD_DUMMY_CTL.PRESENT2 > 0') to prevent controller and memory driving data signals at the same time.<br>The same is true for the theoretical (practically irrelevant case) of transmitting at least one of the command, address and mode fields in DDR mode but receiving data from the memory in SDR mode.<br><br>- When using the RWDS / DQS based capturing scheme (CTL.CLK_IF_RX_SEL=[6,7]), then there is a minimum number of latency / dummy cycles required (RD_DUMMY_CTL.PRESENT2 > 0). For the Hyperbus protocol (DDR_CTL.SIZE3=7) at least 1 latency / dummy cycle has to be specified, for SPI with DQS capturing at least 2 latency / dummy cycles need to be selected (RD_DUMMY_CTL.SIZE5 > 0, exception see following note).<br><br>- In case of falling edge RWDS / DQS capturing (CTL.CLOCK_IF_RX_SEL = '6') and SDR mode, SW should reduce the number of dummy cycles by 1 compared to the latency cycles required by the memory device.<br><br>- For Hyperbus, set RD DUMMY_CTL.SIZE5=initial latency cycles-2 |

### 30.3.38.9 SMIF_DEVICE_RD_DATA_CTL

**Description:** Read data control
**Address:** 0x40420850
**Offset:** 0x50
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register is only used in XIP_MODE.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:19] | | | | | DDR _MODE [18:18] | WIDTH [17:16] | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 16:17 | WIDTH | RW | R | 0 | Width of transfer. |
| 18 | DDR_MODE | RW | R | 0 | Mode of transfer rate. |

### 30.3.38.10 SMIF_DEVICE_RD_BOUND_CTL

**Description:** Read boundary control
**Address:** 0x40420858
**Offset:** 0x58
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register is only used in XIP_MODE.
**Default:** 0x100000

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:5] | | | SIZE5 [4:0] | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:22] | | SUB_PAGE_NR [21:20] | | None [19:18] | | SUB_PAGE_SIZE [17:16] | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | PRESENT [31:31] | None [30:29] | | SUBSEQ_BOUND_EN [28:28] | None [27:24] | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:4 | SIZE5 | RW | R | 0 | Number of base latency cycles (minus 1) used for calculating the number of fist page boundary crossing latency cycles:<br>'0': base_latency = 1 cycles<br>...<br>'31': base_latency = 32 cycles.<br><br>The actual latency cycles when crossing the first page boundary depend on the start address of the transaction and is calculated as follows:<br>if ((page_size - base_latency) < Start_Addr & (sub_page_size - 1))<br>{ ((Start_Addr & (sub_page_size - 1)) - page_size + base_latency) }<br>else<br>{ 0 } |
| 16:17 | SUB_PAGE_SIZE | RW | R | 0 | Specifies the size of a memory sub page 'sub_page_size'.<br>'0': sub_page_size = 8 words = 16 bytes (default).<br>'1': sub_page_size = 16 words = 32 bytes.<br>'2': sub_page_size = 32 words = 64 bytes.<br>'3': sub_page_size = 64 words = 128 bytes. |
| 20:21 | SUB_PAGE_NR | RW | R | 1 | Specifies the number of sub pages per page.<br>'0': 1 sub pages per page, i.e. page_size = sub_page_size<br>'1': 2 sub pages per page, i.e. page_size = 2 x sub_page_size<br>'2': 4 sub pages per page, i.e. page_size = 4 x sub_page_size<br>'3': 8 sub pages per page, i.e. page_size = 8 x sub_page_size |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 28 | SUBSEQ_BOUND_EN | RW | R | 0 | Enable subsequent page boundary latency cycles.<br>'0': Disabled.<br>The page crossing latency cycles are only generated when crossing the first page boundary (i.e. the first time when the SUB_PAGE_NRth sub page boundary is crossed, e.g. with 2 sub pages per page when the 2nd sub page boundary is crossed).<br>'1': Enabled.<br>The page crossing latency cycles are generated when crossing the first and subsequent page boundaries (i.e. every time when a SUB_PAGE_NRth sub page boundary is crossed, e.g. with 2 sub pages per page when the 2nd, 4th, 6th, ... sub page boundary is crossed).<br><br>Note: This only applies when the number of base latency cycles (SIZE5+1) is greater than the size of a page (base_latency > page_size). |
| 31 | PRESENT | RW | R | 0 | Presence of first page boundary latency cycles:<br>'0': not present<br>'1': present |

### 30.3.38.11 SMIF_DEVICE_WR_CMD_CTL

**Description:** Write command control
**Address:** 0x40420860
**Offset:** 0x60
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register is only used in XIP_MODE.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | CODE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | CODEH [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:19] | | | | | DDR _MODE [18:18] | WIDTH [17:16] | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | PRESENT2 [31:30] | | None [29:24] | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | CODE | RW | R | 0 | Command byte code. |
| 8:15 | CODEH | RW | R | 0 | Command high byte code.<br>This field specifies the most significant command byte, sent before the least significant command byte (CODE). It is only used when PRESENT2 = '2'. |
| 16:17 | WIDTH | RW | R | 0 | Width of transfer. |
| 18 | DDR_MODE | RW | R | 0 | Mode of transfer rate. |
| 30:31 | PRESENT2 | RW | R | 0 | Presence of command field:<br>'0': not present<br>'1': present (1 Byte)<br>'2': present (2 Byte for OPI)<br><br>Note: For octal data transfer with DDR mode (WIDTH='3' and DDR_MODE='1') either the HB protocol needs to be selected (by ADDR_CTL.SIZE3='7') or this field needs to be set to PRESENT2='2'. |

### 30.3.38.12 SMIF_DEVICE_WR_ADDR_CTL

**Description:** Write address control
**Address:** 0x40420864
**Offset:** 0x64
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register is only used in XIP_MODE.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:19] | | | | | DDR _MODE [18:18] | WIDTH [17:16] | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 16:17 | WIDTH | RW | R | 0 | Width of transfer. |
| 18 | DDR_MODE | RW | R | 0 | Mode of transfer rate. |

### 30.3.38.13 SMIF_DEVICE_WR_MODE_CTL

**Description:** Write mode control
**Address:** 0x40420868
**Offset:** 0x68
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register is only used in XIP_MODE.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | CODE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | CODEH [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:19] | | | | | DDR _MODE [18:18] | WIDTH [17:16] | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | PRESENT2 [31:30] | | None [29:24] | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | CODE | RW | R | 0 | Mode byte code. |
| 8:15 | CODEH | RW | R | 0 | Mode high byte code.<br>This field specifies the most significant mode byte, sent before the least significant mode byte (CODE). It is only used when PRESENT2 = '2'. |
| 16:17 | WIDTH | RW | R | 0 | Width of transfer. |
| 18 | DDR_MODE | RW | R | 0 | Mode of transfer rate. |
| 30:31 | PRESENT2 | RW | R | 0 | Presence of mode field:<br>'0': not present<br>'1': present (1 Byte)<br>'2': present (2 Byte for OPI)<br><br>Note: For octal data transfer with DDR mode (WIDTH='3' and DDR_MODE='1') this field needs to be set to PRESENT2='2' to generate a mode field (or to PRESENT2='0'). |

### 30.3.38.14 SMIF_DEVICE_WR_DUMMY_CTL

**Description:** Write dummy control
**Address:** 0x4042086C
**Offset:** 0x6C
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register is only used in XIP_MODE.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:5] | | | SIZE5 [4:0] | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:18] | | | | | | RWDS_EN [17:17] | None [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | PRESENT2 [31:30] | | None [29:24] | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:4 | SIZE5 | RW | R | 0 | Number of dummy cycles (minus 1):<br>'0': 1 cycles<br>...<br>'31': 32 cycles. |
| 17 | RWDS_EN | RW | R | 0 | Read-Write-Data-Strobe Enable. Specifies whether the RWDS output signal should be driven starting in the last dummy cycle until DESELECT. This is needed for write transactions with byte masking via RWDS (e.g. Hyperbus).<br>'0': do not drive RWDS output<br>'1': drive RWDS output starting in last dummy cycle until DESELECT<br><br>Note: this field is located in the WR_DUMMY_CTL register (and not in the WR_DATA_CTL register) since the RWDS signal needs to be driven already in the last dummy cycle. |
| 30:31 | PRESENT2 | RW | R | 0 | Presence of dummy cycles:<br>'0': not present<br>'1': present<br>'2': present - Dummy cycles are doubled when RWDS refresh indicator is high during CA cycle. (HyperRAM variable latency mode) |

### 30.3.38.15 SMIF_DEVICE_WR_DATA_CTL

**Description:** Write data control
**Address:** 0x40420870
**Offset:** 0x70
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register is only used in XIP_MODE.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:19] | | | | | DDR _MODE [18:18] | WIDTH [17:16] | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 16:17 | WIDTH | RW | R | 0 | Width of transfer. |
| 18 | DDR_MODE | RW | R | 0 | Mode of transfer rate. |

# 31 SRSS

**Description** SRSS Core Registers (ver3)
**Base Address** 0x40260000
**Size** 0x10000
**Slave Num** MMIO2 - 5

| Register Name | Address | Permission | Description |
|---|---|---|---|
| PWR_LVD_STATUS | 0x40260040 | FULL | High Voltage / Low Voltage Detector (HVLVD) Status Register |
| PWR_LVD_STATUS2 | 0x40260044 | FULL | High Voltage / Low Voltage Detector (HVLVD) Status Register #2 |
| CLK_DSI_SELECT0 | 0x40260100 | FULL | Clock DSI Select Register |
| CLK_DSI_SELECT1 | 0x40260104 | FULL | Clock DSI Select Register |
| CLK_DSI_SELECT2 | 0x40260108 | FULL | Clock DSI Select Register |
| CLK_DSI_SELECT3 | 0x4026010C | FULL | Clock DSI Select Register |
| CLK_DSI_SELECT4 | 0x40260110 | FULL | Clock DSI Select Register |
| CLK_DSI_SELECT5 | 0x40260114 | FULL | Clock DSI Select Register |
| CLK_DSI_SELECT6 | 0x40260118 | FULL | Clock DSI Select Register |
| CLK_OUTPUT_FAST | 0x40260140 | FULL | Fast Clock Output Select Register |
| CLK_OUTPUT_SLOW | 0x40260144 | FULL | Slow Clock Output Select Register |
| CLK_CAL_CNT1 | 0x40260148 | FULL | Clock Calibration Counter 1 |
| CLK_CAL_CNT2 | 0x4026014C | FULL | Clock Calibration Counter 2 |
| SRSS_INTR | 0x40260200 | FULL | SRSS Interrupt Register |
| SRSS_INTR_SET | 0x40260204 | FULL | SRSS Interrupt Set Register |
| SRSS_INTR_MASK | 0x40260208 | FULL | SRSS Interrupt Mask Register |
| SRSS_INTR_MASKED | 0x4026020C | FULL | SRSS Interrupt Masked Register |
| PWR_CTL | 0x40261000 | FULL | Power Mode Control |
| PWR_CTL2 | 0x40261004 | FULL | Power Mode Control 2<br>Note:LINREG_LPMODE RET_REG_DIS NWELL_REG_DIS REFV_OK REFVBUF_LPMODE REFI_LPMODE PORBOD_LPMODE are not available for this register |
| PWR_HIBERNATE | 0x40261008 | FULL | HIBERNATE Mode Register |
| PWR_SSV_CTL | 0x40261018 | FULL | Supply Supervision Control Register |
| PWR_SSV_STATUS | 0x4026101C | FULL | Supply Supervision Status Register |
| PWR_LVD_CTL | 0x40261020 | FULL | High Voltage / Low Voltage Detector (HVLVD) Configuration Register<br>Note:HVLVD1_TRIPSEL HVLVD1_SRCSEL HVLVD1_EN are not available for this register |
| PWR_LVD_CTL2 | 0x40261024 | FULL | High Voltage / Low Voltage Detector (HVLVD) Configuration Register #2 |
| PWR_REGHC_CTL | 0x40261028 | FULL | REGHC Control Register |
| PWR_REGHC_STATUS | 0x4026102C | FULL | REGHC Status Register |
| PWR_REGHC_CTL2 | 0x40261030 | FULL | REGHC Control Register 2 |
| PWR_REGHC_CTL4 | 0x40261038 | FULL | REGHC Control Register 4 |
| PWR_HIB_DATA0 | 0x40261040 | FULL | HIBERNATE Data Register |
| CLK_PATH_SELECT0 | 0x40261200 | FULL | Clock Path Select Register |
| CLK_PATH_SELECT1 | 0x40261204 | FULL | Clock Path Select Register |
| CLK_PATH_SELECT2 | 0x40261208 | FULL | Clock Path Select Register |
| CLK_PATH_SELECT3 | 0x4026120C | FULL | Clock Path Select Register |
| CLK_PATH_SELECT4 | 0x40261210 | FULL | Clock Path Select Register |
| CLK_PATH_SELECT5 | 0x40261214 | FULL | Clock Path Select Register |
| CLK_PATH_SELECT6 | 0x40261218 | FULL | Clock Path Select Register |
| CLK_ROOT_SELECT0 | 0x40261240 | FULL | Clock Root Select Register |
| CLK_ROOT_SELECT1 | 0x40261244 | FULL | Clock Root Select Register |
| CLK_ROOT_SELECT2 | 0x40261248 | FULL | Clock Root Select Register |
| CLK_ROOT_SELECT3 | 0x4026124C | FULL | Clock Root Select Register |
| CLK_ROOT_SELECT4 | 0x40261250 | FULL | Clock Root Select Register |
| CLK_ROOT_SELECT5 | 0x40261254 | FULL | Clock Root Select Register |
| CLK_ROOT_SELECT6 | 0x40261258 | FULL | Clock Root Select Register |
| CLK_ROOT_SELECT7 | 0x4026125C | FULL | Clock Root Select Register |
| CLK_SELECT | 0x40261500 | FULL | Clock selection register |
| CLK_ILO0_CONFIG | 0x40261508 | FULL | ILO0 Configuration |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| CLK_ILO1_CONFIG | 0x4026150C | FULL | ILO1 Configuration |
| CLK_IMO_CONFIG | 0x40261518 | FULL | IMO Configuration |
| CLK_ECO_CONFIG | 0x4026151C | FULL | ECO Configuration Register |
| CLK_ECO_PRESCALE | 0x40261520 | FULL | ECO Prescaler Configuration Register |
| CLK_ECO_STATUS | 0x40261524 | FULL | ECO Status Register |
| CLK_FLL_CONFIG | 0x40261530 | FULL | FLL Configuration Register |
| CLK_FLL_CONFIG2 | 0x40261534 | FULL | FLL Configuration Register 2 |
| CLK_FLL_CONFIG3 | 0x40261538 | FULL | FLL Configuration Register 3 |
| CLK_FLL_CONFIG4 | 0x4026153C | FULL | FLL Configuration Register 4 |
| CLK_FLL_STATUS | 0x40261540 | FULL | FLL Status Register |
| CLK_ECO_CONFIG2 | 0x40261544 | FULL | ECO Configuration Register 2 |
| CLK_PLL_CONFIG0 | 0x40261600 | FULL | PLL Configuration Register |
| CLK_PLL_CONFIG1 | 0x40261604 | FULL | PLL Configuration Register |
| CLK_PLL_STATUS0 | 0x40261640 | FULL | PLL Status Register |
| CLK_PLL_STATUS1 | 0x40261644 | FULL | PLL Status Register |
| CSV_REF_SEL | 0x40261700 | FULL | Select CSV Reference clock for Active domain |
| RES_CAUSE | 0x40261800 | FULL | Reset Cause Observation Register |
| RES_CAUSE2 | 0x40261804 | FULL | Reset Cause Observation Register 2 |
| CLK_TRIM_ILO0_CTL | 0x40263014 | READ | ILO0 Trim Register |
| CLK_TRIM_ILO1_CTL | 0x40263220 | READ | ILO1 Trim Register |

## 31.1 CSV_HF

### 31.1.1 CSV 0

| Register Name | Address | Permission | Description |
|---|---|---|---|
| CSV_HF_CSV0_REF_CTL | 0x40261400 | FULL | Clock Supervision Reference Control |
| CSV_HF_CSV0_REF_LIMIT | 0x40261404 | FULL | Clock Supervision Reference Limits |
| CSV_HF_CSV0_MON_CTL | 0x40261408 | FULL | Clock Supervision Monitor Control |

### 31.1.2 CSV 1

| Register Name | Address | Permission | Description |
|---|---|---|---|
| CSV_HF_CSV1_REF_CTL | 0x40261410 | FULL | Clock Supervision Reference Control |
| CSV_HF_CSV1_REF_LIMIT | 0x40261414 | FULL | Clock Supervision Reference Limits |
| CSV_HF_CSV1_MON_CTL | 0x40261418 | FULL | Clock Supervision Monitor Control |

### 31.1.3 CSV 2

| Register Name | Address | Permission | Description |
|---|---|---|---|
| CSV_HF_CSV2_REF_CTL | 0x40261420 | FULL | Clock Supervision Reference Control |
| CSV_HF_CSV2_REF_LIMIT | 0x40261424 | FULL | Clock Supervision Reference Limits |
| CSV_HF_CSV2_MON_CTL | 0x40261428 | FULL | Clock Supervision Monitor Control |

### 31.1.4 CSV 3

| Register Name | Address | Permission | Description |
|---|---|---|---|
| CSV_HF_CSV3_REF_CTL | 0x40261430 | FULL | Clock Supervision Reference Control |
| CSV_HF_CSV3_REF_LIMIT | 0x40261434 | FULL | Clock Supervision Reference Limits |
| CSV_HF_CSV3_MON_CTL | 0x40261438 | FULL | Clock Supervision Monitor Control |

### 31.1.5 CSV 4

| Register Name | Address | Permission | Description |
|---|---|---|---|
| CSV_HF_CSV4_REF_CTL | 0x40261440 | FULL | Clock Supervision Reference Control |
| CSV_HF_CSV4_REF_LIMIT | 0x40261444 | FULL | Clock Supervision Reference Limits |
| CSV_HF_CSV4_MON_CTL | 0x40261448 | FULL | Clock Supervision Monitor Control |

### 31.1.6 CSV 5

| Register Name | Address | Permission | Description |
|---|---|---|---|
| CSV_HF_CSV5_REF_CTL | 0x40261450 | FULL | Clock Supervision Reference Control |
| CSV_HF_CSV5_REF_LIMIT | 0x40261454 | FULL | Clock Supervision Reference Limits |
| CSV_HF_CSV5_MON_CTL | 0x40261458 | FULL | Clock Supervision Monitor Control |

### 31.1.7 CSV 6

| Register Name | Address | Permission | Description |
|---|---|---|---|
| CSV_HF_CSV6_REF_CTL | 0x40261460 | FULL | Clock Supervision Reference Control |
| CSV_HF_CSV6_REF_LIMIT | 0x40261464 | FULL | Clock Supervision Reference Limits |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| CSV_HF_CSV6_MON_CTL | 0x40261468 | FULL | Clock Supervision Monitor Control |

### 31.1.8 CSV 7

| Register Name | Address | Permission | Description |
|---|---|---|---|
| CSV_HF_CSV7_REF_CTL | 0x40261470 | FULL | Clock Supervision Reference Control |
| CSV_HF_CSV7_REF_LIMIT | 0x40261474 | FULL | Clock Supervision Reference Limits |
| CSV_HF_CSV7_MON_CTL | 0x40261478 | FULL | Clock Supervision Monitor Control |

## 31.2 CSV_REF

### 31.2.1 CSV

| Register Name | Address | Permission | Description |
|---|---|---|---|
| CSV_REF_CSV_REF_CTL | 0x40261710 | FULL | Clock Supervision Reference Control |
| CSV_REF_CSV_REF_LIMIT | 0x40261714 | FULL | Clock Supervision Reference Limits |
| CSV_REF_CSV_MON_CTL | 0x40261718 | FULL | Clock Supervision Monitor Control |

## 31.3 CSV_LF

### 31.3.1 CSV

| Register Name | Address | Permission | Description |
|---|---|---|---|
| CSV_LF_CSV_REF_CTL | 0x40261720 | FULL | Clock Supervision Reference Control |
| CSV_LF_CSV_REF_LIMIT | 0x40261724 | FULL | Clock Supervision Reference Limits |
| CSV_LF_CSV_MON_CTL | 0x40261728 | FULL | Clock Supervision Monitor Control |

## 31.4 CSV_ILO

### 31.4.1 CSV

| Register Name | Address | Permission | Description |
|---|---|---|---|
| CSV_ILO_CSV_REF_CTL | 0x40261730 | FULL | Clock Supervision Reference Control |
| CSV_ILO_CSV_REF_LIMIT | 0x40261734 | FULL | Clock Supervision Reference Limits |
| CSV_ILO_CSV_MON_CTL | 0x40261738 | FULL | Clock Supervision Monitor Control |

## 31.5 CLK_PLL400M 0

| Register Name | Address | Permission | Description |
|---|---|---|---|
| CLK_PLL400M0_CONFIG | 0x40261900 | FULL | 400MHz PLL Configuration Register |
| CLK_PLL400M0_CONFIG2 | 0x40261904 | FULL | 400MHz PLL Configuration Register 2 |
| CLK_PLL400M0_CONFIG3 | 0x40261908 | FULL | 400MHz PLL Configuration Register 3 |
| CLK_PLL400M0_STATUS | 0x4026190C | FULL | 400MHz PLL Status Register |

## 31.6 CLK_PLL400M 1

| Register Name | Address | Permission | Description |
|---|---|---|---|
| CLK_PLL400M1_CONFIG | 0x40261910 | FULL | 400MHz PLL Configuration Register |
| CLK_PLL400M1_CONFIG2 | 0x40261914 | FULL | 400MHz PLL Configuration Register 2 |
| CLK_PLL400M1_CONFIG3 | 0x40261918 | FULL | 400MHz PLL Configuration Register 3 |
| CLK_PLL400M1_STATUS | 0x4026191C | FULL | 400MHz PLL Status Register |

## 31.7 MCWDT 0

| Register Name | Address | Permission | Description |
|---|---|---|---|
| MCWDT0_CPU_SELECT | 0x40268040 | FULL | MCWDT CPU selection register |
| MCWDT0_CTR2_CTL | 0x40268080 | FULL | MCWDT Subcounter 2 Control register |
| MCWDT0_CTR2_CONFIG | 0x40268084 | FULL | MCWDT Subcounter 2 Configuration register |
| MCWDT0_CTR2_CNT | 0x40268088 | FULL | MCWDT Subcounter 2 Count Register |
| MCWDT0_LOCK | 0x40268090 | FULL | MCWDT Lock Register |
| MCWDT0_SERVICE | 0x40268094 | FULL | MCWDT Service Register |
| MCWDT0_INTR | 0x402680A0 | FULL | MCWDT Interrupt Register |
| MCWDT0_INTR_SET | 0x402680A4 | FULL | MCWDT Interrupt Set Register |
| MCWDT0_INTR_MASK | 0x402680A8 | FULL | MCWDT Interrupt Mask Register |
| MCWDT0_INTR_MASKED | 0x402680AC | FULL | MCWDT Interrupt Masked Register |

### 31.7.1 CTR 0

| Register Name | Address | Permission | Description |
|---|---|---|---|
| MCWDT0_CTR0_CTL | 0x40268000 | FULL | MCWDT Subcounter Control Register |
| MCWDT0_CTR0_LOWER_LIMIT | 0x40268004 | FULL | MCWDT Subcounter Lower Limit Register |
| MCWDT0_CTR0_UPPER_LIMIT | 0x40268008 | FULL | MCWDT Subcounter Upper Limit Register |
| MCWDT0_CTR0_WARN_LIMIT | 0x4026800C | FULL | MCWDT Subcounter Warn Limit Register |
| MCWDT0_CTR0_CONFIG | 0x40268010 | FULL | MCWDT Subcounter Configuration Register |
| MCWDT0_CTR0_CNT | 0x40268014 | FULL | MCWDT Subcounter Count Register |

### 31.7.2 CTR 1

| Register Name | Address | Permission | Description |
|---|---|---|---|
| MCWDT0_CTR1_CTL | 0x40268020 | FULL | MCWDT Subcounter Control Register |
| MCWDT0_CTR1_LOWER_LIMIT | 0x40268024 | FULL | MCWDT Subcounter Lower Limit Register |
| MCWDT0_CTR1_UPPER_LIMIT | 0x40268028 | FULL | MCWDT Subcounter Upper Limit Register |
| MCWDT0_CTR1_WARN_LIMIT | 0x4026802C | FULL | MCWDT Subcounter Warn Limit Register |
| MCWDT0_CTR1_CONFIG | 0x40268030 | FULL | MCWDT Subcounter Configuration Register |
| MCWDT0_CTR1_CNT | 0x40268034 | FULL | MCWDT Subcounter Count Register |

## 31.8 MCWDT 1

| Register Name | Address | Permission | Description |
|---|---|---|---|
| MCWDT1_CPU_SELECT | 0x40268140 | FULL | MCWDT CPU selection register |
| MCWDT1_CTR2_CTL | 0x40268180 | FULL | MCWDT Subcounter 2 Control register |
| MCWDT1_CTR2_CONFIG | 0x40268184 | FULL | MCWDT Subcounter 2 Configuration register |
| MCWDT1_CTR2_CNT | 0x40268188 | FULL | MCWDT Subcounter 2 Count Register |
| MCWDT1_LOCK | 0x40268190 | FULL | MCWDT Lock Register |
| MCWDT1_SERVICE | 0x40268194 | FULL | MCWDT Service Register |
| MCWDT1_INTR | 0x402681A0 | FULL | MCWDT Interrupt Register |
| MCWDT1_INTR_SET | 0x402681A4 | FULL | MCWDT Interrupt Set Register |
| MCWDT1_INTR_MASK | 0x402681A8 | FULL | MCWDT Interrupt Mask Register |
| MCWDT1_INTR_MASKED | 0x402681AC | FULL | MCWDT Interrupt Masked Register |

### 31.8.1 CTR 0

| Register Name | Address | Permission | Description |
|---|---|---|---|
| MCWDT1_CTR0_CTL | 0x40268100 | FULL | MCWDT Subcounter Control Register |
| MCWDT1_CTR0_LOWER_LIMIT | 0x40268104 | FULL | MCWDT Subcounter Lower Limit Register |
| MCWDT1_CTR0_UPPER_LIMIT | 0x40268108 | FULL | MCWDT Subcounter Upper Limit Register |
| MCWDT1_CTR0_WARN_LIMIT | 0x4026810C | FULL | MCWDT Subcounter Warn Limit Register |
| MCWDT1_CTR0_CONFIG | 0x40268110 | FULL | MCWDT Subcounter Configuration Register |
| MCWDT1_CTR0_CNT | 0x40268114 | FULL | MCWDT Subcounter Count Register |

### 31.8.2 CTR 1

| Register Name | Address | Permission | Description |
|---|---|---|---|
| MCWDT1_CTR1_CTL | 0x40268120 | FULL | MCWDT Subcounter Control Register |
| MCWDT1_CTR1_LOWER_LIMIT | 0x40268124 | FULL | MCWDT Subcounter Lower Limit Register |
| MCWDT1_CTR1_UPPER_LIMIT | 0x40268128 | FULL | MCWDT Subcounter Upper Limit Register |
| MCWDT1_CTR1_WARN_LIMIT | 0x4026812C | FULL | MCWDT Subcounter Warn Limit Register |
| MCWDT1_CTR1_CONFIG | 0x40268130 | FULL | MCWDT Subcounter Configuration Register |
| MCWDT1_CTR1_CNT | 0x40268134 | FULL | MCWDT Subcounter Count Register |

## 31.9 MCWDT 2

| Register Name | Address | Permission | Description |
|---|---|---|---|
| MCWDT2_CPU_SELECT | 0x40268240 | FULL | MCWDT CPU selection register |
| MCWDT2_CTR2_CTL | 0x40268280 | FULL | MCWDT Subcounter 2 Control register |
| MCWDT2_CTR2_CONFIG | 0x40268284 | FULL | MCWDT Subcounter 2 Configuration register |
| MCWDT2_CTR2_CNT | 0x40268288 | FULL | MCWDT Subcounter 2 Count Register |
| MCWDT2_LOCK | 0x40268290 | FULL | MCWDT Lock Register |
| MCWDT2_SERVICE | 0x40268294 | FULL | MCWDT Service Register |
| MCWDT2_INTR | 0x402682A0 | FULL | MCWDT Interrupt Register |
| MCWDT2_INTR_SET | 0x402682A4 | FULL | MCWDT Interrupt Set Register |
| MCWDT2_INTR_MASK | 0x402682A8 | FULL | MCWDT Interrupt Mask Register |
| MCWDT2_INTR_MASKED | 0x402682AC | FULL | MCWDT Interrupt Masked Register |

### 31.9.1 CTR 0

| Register Name | Address | Permission | Description |
|---|---|---|---|
| MCWDT2_CTR0_CTL | 0x40268200 | FULL | MCWDT Subcounter Control Register |
| MCWDT2_CTR0_LOWER_LIMIT | 0x40268204 | FULL | MCWDT Subcounter Lower Limit Register |
| MCWDT2_CTR0_UPPER_LIMIT | 0x40268208 | FULL | MCWDT Subcounter Upper Limit Register |
| MCWDT2_CTR0_WARN_LIMIT | 0x4026820C | FULL | MCWDT Subcounter Warn Limit Register |
| MCWDT2_CTR0_CONFIG | 0x40268210 | FULL | MCWDT Subcounter Configuration Register |
| MCWDT2_CTR0_CNT | 0x40268214 | FULL | MCWDT Subcounter Count Register |

### 31.9.2 CTR 1

| Register Name | Address | Permission | Description |
|---|---|---|---|
| MCWDT2_CTR1_CTL | 0x40268220 | FULL | MCWDT Subcounter Control Register |
| MCWDT2_CTR1_LOWER_LIMIT | 0x40268224 | FULL | MCWDT Subcounter Lower Limit Register |
| MCWDT2_CTR1_UPPER_LIMIT | 0x40268228 | FULL | MCWDT Subcounter Upper Limit Register |
| MCWDT2_CTR1_WARN_LIMIT | 0x4026822C | FULL | MCWDT Subcounter Warn Limit Register |
| MCWDT2_CTR1_CONFIG | 0x40268230 | FULL | MCWDT Subcounter Configuration Register |
| MCWDT2_CTR1_CNT | 0x40268234 | FULL | MCWDT Subcounter Count Register |

## 31.10 WDT

| Register Name | Address | Permission | Description |
|---|---|---|---|
| WDT_CTL | 0x4026C000 | FULL | WDT Control Register |
| WDT_LOWER_LIMIT | 0x4026C004 | FULL | WDT Lower Limit Register |
| WDT_UPPER_LIMIT | 0x4026C008 | FULL | WDT Upper Limit Register |
| WDT_WARN_LIMIT | 0x4026C00C | FULL | WDT Warn Limit Register |
| WDT_CONFIG | 0x4026C010 | FULL | WDT Configuration Register |
| WDT_CNT | 0x4026C014 | FULL | WDT Count Register |
| WDT_LOCK | 0x4026C040 | FULL | WDT Lock register |
| WDT_SERVICE | 0x4026C044 | FULL | WDT Service register |
| WDT_INTR | 0x4026C050 | FULL | WDT Interrupt Register |
| WDT_INTR_SET | 0x4026C054 | FULL | WDT Interrupt Set Register |
| WDT_INTR_MASK | 0x4026C058 | FULL | WDT Interrupt Mask Register |
| WDT_INTR_MASKED | 0x4026C05C | FULL | WDT Interrupt Masked Register |

## 31.11 Register Details

### 31.11.1 PWR_LVD_STATUS

**Description:** High Voltage / Low Voltage Detector (HVLVD) Status Register
**Address:** 0x40260040
**Offset:** 0x40
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** Real-time status for Voltage Monitoring System
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:1] | | | | | | | HVLVD1_OUT [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | HVLVD1_OUT | R | RW | 0 | HVLVD1 output.<br>0: below voltage threshold<br>1: above voltage threshold |

### 31.11.2 PWR_LVD_STATUS2

**Description:** High Voltage / Low Voltage Detector (HVLVD) Status Register #2
**Address:** 0x40260044
**Offset:** 0x44
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** Real-time status for Voltage Monitoring System
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:1] | | | | | | | HVLVD2_OUT [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | HVLVD2_OUT | R | RW | 0 | HVLVD2 output.<br>0: below voltage threshold<br>1: above voltage threshold |

### 31.11.3 CLK_DSI_SELECT

**Description:** Clock DSI Select Register
**Address:** 0x40260100
**Offset:** 0x100
**Retention:** Retained
**IsDeepSleep:** Yes
**Comment:** Configures DSI mux in clock generation path. Each path has its own copy of this register. See PAS for DSI signal connectivity list.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:5] | | | DSI_MUX [4:0] | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:4 | DSI_MUX | RW | R | 0 | Selects a DSI source or low frequency clock for use in a clock path. The output of this mux can be selected for clock PATH<i> using CLK_PATH_SELECT register. Using the output of this mux as HFCLK source will result in undefined behavior. It can be used to clocks to DSI or as reference inputs for the FLL/PLL, subject to the frequency limits of those circuits. This mux is not glitch free, so do not change the selection while it is an actively selected clock. |
| | DSI_OUT0 | | | 0 | DSI0 - dsi_out[0] |
| | DSI_OUT1 | | | 1 | DSI1 - dsi_out[1] |
| | DSI_OUT2 | | | 2 | DSI2 - dsi_out[2] |
| | DSI_OUT3 | | | 3 | DSI3 - dsi_out[3] |
| | DSI_OUT4 | | | 4 | DSI4 - dsi_out[4] |
| | DSI_OUT5 | | | 5 | DSI5 - dsi_out[5] |
| | DSI_OUT6 | | | 6 | DSI6 - dsi_out[6] |
| | DSI_OUT7 | | | 7 | DSI7 - dsi_out[7] |
| | DSI_OUT8 | | | 8 | DSI8 - dsi_out[8] |
| | DSI_OUT9 | | | 9 | DSI9 - dsi_out[9] |
| | DSI_OUT10 | | | 10 | DSI10 - dsi_out[10] |
| | DSI_OUT11 | | | 11 | DSI11 - dsi_out[11] |
| | DSI_OUT12 | | | 12 | DSI12 - dsi_out[12] |
| | DSI_OUT13 | | | 13 | DSI13 - dsi_out[13] |
| | DSI_OUT14 | | | 14 | DSI14 - dsi_out[14] |
| | DSI_OUT15 | | | 15 | DSI15 - dsi_out[15] |
| | ILO0 | | | 16 | ILO0 - Internal Low-speed Oscillator #0 |
| | WCO | | | 17 | WCO - Watch-Crystal Oscillator |
| | ALTLF | | | 18 | ALTLF - Alternate Low-Frequency Clock |
| | PILO | | | 19 | PILO - Precision Internal Low-speed Oscillator |
| | ILO1 | | | 20 | ILO1 - Internal Low-speed Oscillator #1, if present. |

### 31.11.4 CLK_OUTPUT_FAST

**Description:** Fast Clock Output Select Register
**Address:** 0x40260140
**Offset:** 0x140
**Retention:** Retained
**IsDeepSleep:** Yes
**Comment:** Selects clocks for calibration
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | PATH_SEL0 [7:4] | | | | FAST_SEL0 [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:12] | | | | HFCLK_SEL0 [11:8] | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | PATH_SEL1 [23:20] | | | | FAST_SEL1 [19:16] | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:28] | | | | HFCLK_SEL1 [27:24] | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | FAST_SEL0 | RW | R | 0 | Select signal for fast clock output #0 |
| | NC | | | 0 | Disabled - output is 0. For power savings, clocks are blocked before entering any muxes, including PATH_SEL0 and HFCLK_SEL0. |
| | ECO | | | 1 | External Crystal Oscillator (ECO) |
| | EXTCLK | | | 2 | External clock input (EXTCLK) |
| | ALTHF | | | 3 | Alternate High-Frequency (ALTHF) clock input to SRSS |
| | TIMERCLK | | | 4 | Timer clock. It is grouped with the fast clocks because it may be a gated version of a fast clock, and therefore may have a short high pulse. |
| | PATH_SEL0 | | | 5 | Selects the clock path chosen by PATH_SEL0 field |
| | HFCLK_SEL0 | | | 6 | Selects the output of the HFCLK_SEL0 mux |
| | SLOW_SEL0 | | | 7 | Selects the output of CLK_OUTPUT_SLOW.SLOW_SEL0 |
| 4:7 | PATH_SEL0 | RW | R | 0 | Selects a clock path to use in fast clock output #0 logic.<br>0: FLL output<br>1-15: PLL output on path1-path15 (if available) |
| 8:11 | HFCLK_SEL0 | RW | R | 0 | Selects a HFCLK tree for use in fast clock output #0 |
| 16:19 | FAST_SEL1 | RW | R | 0 | Select signal for fast clock output #1 |
| | NC | | | 0 | Disabled - output is 0. For power savings, clocks are blocked before entering any muxes, including PATH_SEL1 and HFCLK_SEL1. |
| | ECO | | | 1 | External Crystal Oscillator (ECO) |
| | EXTCLK | | | 2 | External clock input (EXTCLK) |
| | ALTHF | | | 3 | Alternate High-Frequency (ALTHF) clock input to SRSS |
| | TIMERCLK | | | 4 | Timer clock. It is grouped with the fast clocks because it may be a gated version of a fast clock, and therefore may have a short high pulse. |
| | PATH_SEL1 | | | 5 | Selects the clock path chosen by PATH_SEL1 field |
| | HFCLK_SEL1 | | | 6 | Selects the output of the HFCLK_SEL1 mux |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| | SLOW_SEL1 | | | 7 | Selects the output of CLK_OUTPUT_SLOW.SLOW_SEL1 |
| 20:23 | PATH_SEL1 | RW | R | 0 | Selects a clock path to use in fast clock output #1 logic.<br>0: FLL output<br>1-15: PLL output on path1-path15 (if available) |
| 24:27 | HFCLK_SEL1 | RW | R | 0 | Selects a HFCLK tree for use in fast clock output #1 logic |

### 31.11.5 CLK_OUTPUT_SLOW

**Description:** Slow Clock Output Select Register
**Address:** 0x40260144
**Offset:** 0x144
**Retention:** Retained
**IsDeepSleep:** Yes
**Comment:** Selects a slow clock for calibration. The outputs of these muxes go into CLK_OUTPUT_FAST.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | SLOW_SEL1 [7:4] | | | | SLOW_SEL0 [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | SLOW_SEL0 | RW | R | 0 | Select signal for slow clock output #0 |
| | NC | | | 0 | Disabled - output is 0. For power savings, clocks are blocked before entering any muxes. |
| | ILO0 | | | 1 | Internal Low Speed Oscillator (ILO0) |
| | WCO | | | 2 | Watch-Crystal Oscillator (WCO) |
| | BAK | | | 3 | Root of the Backup domain clock tree (BAK) |
| | ALTLF | | | 4 | Alternate low-frequency clock input to SRSS (ALTLF) |
| | LFCLK | | | 5 | Root of the low-speed clock tree (LFCLK) |
| | IMO | | | 6 | Internal Main Oscillator (IMO). This is grouped with the slow clocks so it can be observed during DEEPSLEEP entry/exit. |
| | SLPCTRL | | | 7 | Sleep Controller clock (SLPCTRL). This is grouped with the slow clocks so it can be observed during DEEPSLEEP entry/exit. |
| | PILO | | | 8 | Precision Internal Low Speed Oscillator (PILO) |
| | ILO1 | | | 9 | Internal Low Speed Oscillator (ILO1), if present on the product. |
| | ECO_PRESCALER | | | 10 | ECO Prescaler (ECO_PRESCALER) |
| | LPECO | | | 11 | LPECO |
| | LPECO_PRESCALER | | | 12 | LPECO Prescaler (LPECO_PRESCALER) |
| 4:7 | SLOW_SEL1 | RW | R | 0 | Select signal for slow clock output #1 |
| | NC | | | 0 | Disabled - output is 0. For power savings, clocks are blocked before entering any muxes. |
| | ILO0 | | | 1 | Internal Low Speed Oscillator (ILO) |
| | WCO | | | 2 | Watch-Crystal Oscillator (WCO) |
| | BAK | | | 3 | Root of the Backup domain clock tree (BAK) |
| | ALTLF | | | 4 | Alternate low-frequency clock input to SRSS (ALTLF) |
| | LFCLK | | | 5 | Root of the low-speed clock tree (LFCLK) |
| | IMO | | | 6 | Internal Main Oscillator (IMO). This is grouped with the slow clocks so it can be observed during DEEPSLEEP entry/exit. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| | SLPCTRL | | | 7 | Sleep Controller clock (SLPCTRL). This is grouped with the slow clocks so it can be observed during DEEPSLEEP entry/exit. |
| | PILO | | | 8 | Precision Internal Low Speed Oscillator (PILO) |
| | ILO1 | | | 9 | Internal Low Speed Oscillator (ILO1), if present on the product. |
| | ECO_PRESCALER | | | 10 | ECO Prescaler (ECO_PRESCALER) |
| | LPECO | | | 11 | LPECO |
| | LPECO_PRESCALER | | | 12 | LPECO Prescaler (LPECO_PRESCALER) |

### 31.11.6 CLK_CAL_CNT1

**Description:** Clock Calibration Counter 1
**Address:** 0x40260148
**Offset:** 0x148
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x80000000

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | CAL_COUNTER1 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | CAL_COUNTER1 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | CAL_COUNTER1 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | CAL_COUNTER_DONE [31:31] | None [30:24] | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:23 | CAL_COUNTER1 | RW | A | 0 | Down-counter clocked on fast clock output #0 (see CLK_OUTPUT_FAST). This register always reads as zero. Counting starts internally when this register is written with a nonzero value. CAL_COUNTER_DONE goes immediately low to indicate that the counter has started and will be asserted when the counters are done. Do not write this field unless CAL_COUNTER_DONE==1. Both clocks must be running or the measurement will not complete. A stalled counter can be recovered by selecting valid clocks, waiting until the measurement completes, and discarding the first result. |
| 31 | CAL_COUNTER_DONE | R | W | 1 | Status bit indicating that the internal counter #1 is finished counting and CLK_CAL_CNT2.COUNTER stopped counting up |

### 31.11.7 CLK_CAL_CNT2

**Description:** Clock Calibration Counter 2
**Address:** 0x4026014C
**Offset:** 0x14C
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | CAL_COUNTER2 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | CAL_COUNTER2 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | CAL_COUNTER2 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:23 | CAL_COUNTER2 | R | RW | 0 | Up-counter clocked on fast clock output #1 (see CLK_OUTPUT_FAST). When CLK_CAL_CNT1.CAL_COUNTER_DONE==1, the counter is stopped and can be read by SW. Do not read this value unless CAL_COUNTER_DONE==1. The expected final value is related to the ratio of clock frequencies used for the two counters and the value loaded into counter 1: CLK_CAL_CNT2.C OUNTER=(F_cnt2/F_cnt1)*(CLK_CAL_CNT1.COUNTER) |

### 31.11.8 SRSS_INTR

**Description:** SRSS Interrupt Register
**Address:** 0x40260200
**Offset:** 0x200
**Retention:** Retained
**IsDeepSleep:** Yes
**Comment:** Interrupt signal from SRSS includes this register and also BACKUP_INTR, if present.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:6] | | CLK_CAL [5:5] | None [4:3] | | HVLVD2 [2:2] | HVLVD1 [1:1] | None [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 1 | HVLVD1 | RW1C | A | 0 | Interrupt for low voltage detector HVLVD1 |
| 2 | HVLVD2 | RW1C | A | 0 | Interrupt for low voltage detector HVLVD2 |
| 5 | CLK_CAL | RW1C | A | 0 | Clock calibration counter is done. This field is reset during DEEPSLEEP mode. |

### 31.11.9 SRSS_INTR_SET

**Description:** SRSS Interrupt Set Register
**Address:** 0x40260204
**Offset:** 0x204
**Retention:** Retained
**IsDeepSleep:** Yes
**Comment:** Can be used to set interrupts for firmware testing.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:6] | | CLK_CAL [5:5] | None [4:3] | | HVLVD2 [2:2] | HVLVD1 [1:1] | None [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 1 | HVLVD1 | RW1S | A | 0 | Set interrupt for low voltage detector HVLVD1 |
| 2 | HVLVD2 | RW1S | A | 0 | Set interrupt for low voltage detector HVLVD2 |
| 5 | CLK_CAL | RW1S | A | 0 | Set interrupt for clock calibration counter done. This field is reset during DEEPSLEEP mode. |

### 31.11.10 SRSS_INTR_MASK

**Description:** SRSS Interrupt Mask Register
**Address:** 0x40260208
**Offset:** 0x208
**Retention:** Retained
**IsDeepSleep:** Yes
**Comment:** Controls whether interrupt is forwarded to CPU. All masks block the interrupt when 0 and forward the interrupt when 1
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:6] | | CLK_CAL [5:5] | None [4:3] | | HVLVD2 [2:2] | HVLVD1 [1:1] | None [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 1 | HVLVD1 | RW | R | 0 | Mask for low voltage detector HVLVD1 |
| 2 | HVLVD2 | RW | R | 0 | Mask for low voltage detector HVLVD2 |
| 5 | CLK_CAL | RW | R | 0 | Mask for clock calibration done |

### 31.11.11 SRSS_INTR_MASKED

**Description:** SRSS Interrupt Masked Register
**Address:** 0x4026020C
**Offset:** 0x20C
**Retention:** Retained
**IsDeepSleep:** Yes
**Comment:** Bitwise and between the interrupt request and mask registers so firmware can read the status of all mask enabled interrupt causes with a single load operation
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:6] | | CLK_CAL [5:5] | None [4:3] | | HVLVD2 [2:2] | HVLVD1 [1:1] | None [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 1 | HVLVD1 | R | RW | 0 | Logical and of corresponding request and mask bits. |
| 2 | HVLVD2 | R | RW | 0 | Logical and of corresponding request and mask bits. |
| 5 | CLK_CAL | R | RW | 0 | Logical and of corresponding request and mask bits. |

### 31.11.12 PWR_CTL

**Description:** Power Mode Control
**Address:** 0x40261000
**Offset:** 0x1000
**Retention:** Retained
**IsDeepSleep:** Yes
**Comment:** Controls the device power mode options and allows observation of current state.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:6] | | LPM _READY [5:5] | DEBUG _SESSION [4:4] | None [3:2] | | POWER_MODE [1:0] | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:1 | POWER_MODE | R | RW | 0 | Current power mode of the device. Note that this field cannot be read in all power modes on actual silicon. |
| | RESET | | | 0 | System is resetting. |
| | ACTIVE | | | 1 | At least one CPU is running. |
| | SLEEP | | | 2 | No CPUs are running. Peripherals may be running. |
| | DEEPSLEEP | | | 3 | Main high-frequency clock is off; low speed clocks are available. Communication interface clocks may be present. |
| 4 | DEBUG_SESSION | R | RW | 0 | Indicates whether a debug session is active (CDBGPWRUPREQ signal is 1) |
| | NO_SESSION | | | 0 | No debug session active |
| | SESSION_ACTIVE | | | 1 | Debug session is active. Power modes behave differently to keep the debug session active. |
| 5 | LPM_READY | R | RW | 0 | Indicates whether certain low power functions are ready. The low current circuits take longer to startup after XRES, HIBERNATE wakeup, or supply supervision reset wakeup than the normal mode circuits. HIBERNATE mode may be entered regardless of this bit.<br>0: If a low power circuit operation is requested, it will stay in its normal operating mode until it is ready. If DEEPSLEEP is requested by all processors WFI/WFE, the device will instead enter SLEEP. When low power circuits are ready, device will automatically enter the originally requested mode.<br>1: Normal operation. DEEPSLEEP and low power circuits operate as requested in other registers. |

### 31.11.13 PWR_CTL2

**Description:** Power Mode Control 2
**Address:** 0x40261004
**Offset:** 0x1004
**Retention:** Retained
**IsDeepSleep:** Yes
**Comment:** Controls the device power mode options and allows observation of current state.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:5] | | | DPSLP_REG_DIS [4:4] | None [3:2] | | LINREG_OK [1:1] | LINREG_DIS [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:22] | | REFVBUF_OK [21:21] | REFVBUF_DIS [20:20] | None [19:17] | | | REFV_DIS [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | PLL_LS_BYPASS [31:31] | None [30:29] | | BGREF_LPMODE [28:28] | None [27:26] | | REFI_OK [25:25] | REFI_DIS [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | LINREG_DIS | RW | A | 0 | Explicitly disable the linear Core Regulator. Write zero for Traveo II devices. This register is only reset by XRES, HIBERNATE wakeup, or supply supervision reset.<br>0: Linear Core Regulator is not explicitly disabled. Hardware disables it automatically for internal sequences, including for DEEPSLEEP, HIBERNATE, and XRES low power modes.<br>1: Linear Core Regulator is explicitly disabled. Only use this for special cases when another source supplies vccd during ACTIVE and SLEEP modes. This setting is only legal when another source supplies vccd, but there is no special hardware protection for this case. |
| 1 | LINREG_OK | R | RW | 0 | Status of the linear Core Regulator. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 4 | DPSLP_REG_DIS | RW | A | 0 | Explicity disable the DeepSleep regulator, including circuits shared with the Active Regulator. This register must not be set except as part of a Cypress-provided sequence or API, such as the PMIC case described below. This register is only reset by XRES, HIBERNATE wakeup, or supply supervision reset. If the DeepSleep regulator is disabled, it is not supported to enable it again later by clearing this bit.<br>0: DeepSleep Regulator is not explicitly disabled. This is the normal setting, and hardware automatically controls the DeepSleep regulator for most sequences, including for HIBERNATE and XRES low power modes. This setting must be used if the Active Linear Regulator is used, because some circuitry is shared.<br>1: DeepSleep Regulator is explicitly disabled. Only use this for special cases when another source supplies vccdpslp during DEEPSLEEP mode and there is no future intention to use the Active Regulator for ACTIVE/SLEEP modes. For example, this setting is used as part of a Cypress-provided handover sequence to a PMIC that operates in ACTIVE, SLEEP, and DEEPSLEEP and disables both the Active Linear Regulator and DeepSleep Regulator. |
| 16 | REFV_DIS | RW | A | 0 | Disables the voltage reference.<br>PSoC products: This disables the Active voltage reference. Firmware must ensure that LPM_READY==1 and BGREF_LPMODE==1 for at least 1us before disabling the Active Reference. When enabling the Active Reference, use REFV_OK indicator to know when it is ready. This register is only reset by XRES, HIBERNATE wakeup, or supply supervision reset.<br>Traveo II products: Reserved. Write zero. |
| 20 | REFVBUF_DIS | RW | A | 0 | Disable the voltage reference buffer. Firmware should only disable the buffer when there is no connected circuit that is using it. SRSS circuits that require it are the PLL and ECO. A particular product may have circuits outside the SRSS that use the buffer. This register is only reset by XRES, HIBERNATE wakeup, or supply supervision reset. |
| 21 | REFVBUF_OK | R | RW | 0 | Indicates that the voltage reference buffer is ready. Due to synchronization delays, it may take two IMO clock cycles for hardware to clear this bit after asserting REFVBUF_DIS=1. |
| 24 | REFI_DIS | RW | A | 0 | Reserved. Write zero. |
| 25 | REFI_OK | R | RW | 0 | Indicates that the current reference is ready. Due to synchronization delays, it may take two IMO clock cycles for hardware to clear this bit after asserting REFI_DIS=1. |
| 28 | BGREF_LPMODE | RW | A | 0 | Control the circuit-level power mode of the Bandgap Reference circuits.<br>0: Bandgap Reference circuits operate in higher current mode.<br>1: Bandgap Reference circuits operate in low power. Refer to documentation for restrictions.<br><br>HT-variant: This register will not set unless CLK_ILO0_CONFIG.ILO0_ENABLE==1. When disabling low power operation, keep ILO0 enabled for at least 5 cycles after clearing this bit to allow for internal synchronization. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 31 | PLL_LS_BYPASS | RW | R | 0 | Bypass level shifter inside the PLL. Unused, if no PLL is present in the product.<br>0: Do not bypass the level shifter. This setting is ok for all operational modes and vccd target voltage.<br>1: Bypass the level shifter. This may reduce jitter on the PLL output clock, but can only be used when vccd is targeted to 1.1V nominal. Otherwise, it can result in clock degradation and static current. |

### 31.11.14 PWR_HIBERNATE

**Description:** HIBERNATE Mode Register
**Address:** 0x40261008
**Offset:** 0x1008
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register controls entry/exit from HIBERNATE power mode. This register is implemented in the unregulated voltage domain. This register and PWR_HIB_DATA registers are the only ones that continue to retain information during HIBERNATE mode. Three identical writes are required to enter HIBERNATE mode. Ensure changes settle after the third write by reading this register.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | TOKEN [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | UNLOCK [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | POLARITY_HIBPIN [23:20] | | | | MASK _HIBWDT [19:19] | MASK _HIBA LARM [18:18] | FREEZE [17:17] | None [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | HIBERNATE [31:31] | HIBERNATE _DISABLE [30:30] | None [29:28] | | MASK_HIBPIN [27:24] | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | TOKEN | RW | A | 0 | Contains a 8-bit token that is retained through a HIBERNATE/WAKEUP sequence that can be used by firmware to differentiate WAKEUP from a general RESET event. Note that waking up from HIBERNATE using XRES will reset this register. |
| 8:15 | UNLOCK | RW | A | 0 | This byte must be set to 0x3A for FREEZE or HIBERNATE fields to operate. Any other value in this register will cause FREEZE/HIBERNATE to have no effect, except as noted in the FREEZE description. |
| 17 | FREEZE | RW | A | 0 | Firmware sets this bit to freeze the configuration, mode and state of all GPIOs and SIOs in the system. When entering HIBERNATE mode, the first write instructs DEEPSLEEP peripherals that they cannot ignore the upcoming freeze command. This occurs even in the illegal condition where UNLOCK is not set. If UNLOCK and HIBERNATE are properly set, the IOs actually freeze on the second write. Supply supervision is disabled during HIBERNATE mode. HIBERNATE peripherals ignore resets (excluding XRES) while FREEZE==1. |
| 18 | MASK_HIBALARM | RW | A | 0 | When set, HIBERNATE will wakeup for a RTC interrupt |
| 19 | MASK_HIBWDT | RW | A | 0 | When set, HIBERNATE will wakeup for WDT interrupt |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 20:23 | POLARITY_HIBPIN | RW | A | 0 | Each bit sets the active polarity of the corresponding wakeup pin.<br>0: Pin input of 0 will wakeup the part from HIBERNATE<br>1: Pin input of 1 will wakeup the part from HIBERNATE |
| 24:27 | MASK_HIBPIN | RW | A | 0 | When set, HIBERNATE will wakeup if the corresponding pin input matches the POLARITY_HIBPIN setting. Each bit corresponds to one of the wakeup pins. |
| 30 | HIBERNATE_DISABLE | RW1S | R | 0 | Hibernate disable bit.<br>0: Normal operation, HIBERNATE works as described<br>1: Further writes to this register are ignored<br>Note: This bit is a write-once bit until the next reset. Avoid changing any other bits in this register while disabling HIBERNATE mode. Also, it is recommended to clear the UNLOCK code, if it was previously written.. |
| 31 | HIBERNATE | RW | A | 0 | Firmware sets this bit to enter HIBERNATE mode. The system will enter HIBERNATE mode immediately after writing to this bit and will wakeup only in response to XRES or WAKEUP event. Both UNLOCK and FREEZE must have been set correctly in a previous write operations. Otherwise, it will not enter HIBERNATE. External supplies must have been stable for 250us before entering HIBERNATE mode. |

### 31.11.15 PWR_SSV_CTL

**Description:** Supply Supervision Control Register
**Address:** 0x40261018
**Offset:** 0x1018
**Retention:** Retained
**IsDeepSleep:** Yes
**Comment:** Controls for brownout and over-voltage detectors. Fields *_VSEL and *_ACTION are only reset by XRES/POR/BOD/OVD/OCD/HIBERNATE. Fields *_ENABLE are reset by all resets.
**Default:** 0x8080808

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | BODVDDA_ACTION [7:6] | | None [5:5] | BODVDDA_VSEL [4:4] | BODVDDD_ENABLE [3:3] | None [2:1] | | BODVDDD_VSEL [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:12] | | | | BODVCCD_ENABLE [11:11] | None [10:9] | | BODVDDA_ENABLE [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | OVDVDDA_ACTION [23:22] | | None [21:21] | OVDVDDA_VSEL [20:20] | OVDVDDD_ENABLE [19:19] | None [18:17] | | OVDVDDD_VSEL [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:28] | | | | OVDVCCD_ENABLE [27:27] | None [26:25] | | OVDVDDA_ENABLE [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | BODVDDD_VSEL | RW | A | 0 | Selects the voltage threshold for BOD on vddd. The BOD does not reliably monitor the supply during the transition.<br>0: vddd<2.7V<br>1: vddd<3.0V |
| 3 | BODVDDD_ENABLE | RW | A | 1 | Enable for BOD on vddd. This cannot be disabled during normal operation. |
| 4 | BODVDDA_VSEL | RW | A | 0 | Selects the voltage threshold for BOD on vdda. Ensure BODVDDA_ENABLE==0 before changing this setting to prevent false triggers.<br>0: vdda<2.7V<br>1: vdda<3.0V |
| 6:7 | BODVDDA_ACTION | RW | A | 0 | Action taken when the BOD on vdda triggers. |
| | NOTHING | | | 0 | No action |
| | FAULT | | | 1 | Generate a fault |
| | RESET | | | 2 | Reset the chip |
| 8 | BODVDDA_ENABLE | RW | A | 0 | Enable for BOD on vdda. BODVDDA_ACTION will be triggered when the BOD is disabled. If no action is desired when disabling, firmware must first write BODVDDA_ACTION=NOTHING in a separate write cycle. |
| 11 | BODVCCD_ENABLE | RW | A | 1 | Enable for BOD on vccd. This cannot be disabled during normal operation. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 16 | OVDVDDD_VSEL | RW | A | 0 | Selects the voltage threshold for OVD on vddd. The OVD does not reliably monitor the supply during the transition.<br>0: vddd>5.5V<br>1: vddd>5.0V |
| 19 | OVDVDDD_ENABLE | RW | A | 1 | Enable for OVD on vddd. This cannot be disabled during normal operation. |
| 20 | OVDVDDA_VSEL | RW | A | 0 | Selects the voltage threshold for OVD on vdda. Ensure OVDVDDA_ENABLE==0 before changing this setting to prevent false triggers<br>0: vddd>5.5V<br>1: vddd>5.0V |
| 22:23 | OVDVDDA_ACTION | RW | A | 0 | Action taken when the OVD on vdda triggers. |
| | NOTHING | | | 0 | No action |
| | FAULT | | | 1 | Generate a fault |
| | RESET | | | 2 | Reset the chip |
| 24 | OVDVDDA_ENABLE | RW | A | 0 | Enable for OVD on vdda. |
| 27 | OVDVCCD_ENABLE | RW | A | 1 | Enable for OVD on vccd. This cannot be disabled during normal operation. |

### 31.11.16 PWR_SSV_STATUS

**Description:** Supply Supervision Status Register
**Address:** 0x4026101C
**Offset:** 0x101C
**Retention:** Retained
**IsDeepSleep:** Yes
**Comment:** Status for brownout and over-voltage detectors.
**Default:** 0x30505

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:3] | | | | | BODVCCD_OK [2:2] | BODVDDA_OK [1:1] | BODVDDD_OK [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:11] | | | | | OVDVCCD_OK [10:10] | OVDVDDA_OK [9:9] | OVDVDDD_OK [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:18] | | | | | | OCD_DPSLP_REG_OK [17:17] | OCD_ACT_LINREG_OK [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | BODVDDD_OK | R | RW | 1 | BOD indicates vddd is ok. This will always read 1, because a detected brownout will reset the chip. |
| 1 | BODVDDA_OK | R | RW | 0 | BOD indicates vdda is ok. |
| 2 | BODVCCD_OK | R | RW | 1 | BOD indicates vccd is ok. This will always read 1, because a detected brownout will reset the chip. |
| 8 | OVDVDDD_OK | R | RW | 1 | OVD indicates vddd is ok. This will always read 1, because a detected over-voltage condition will reset the chip. |
| 9 | OVDVDDA_OK | R | RW | 0 | OVD indicates vdda is ok. |
| 10 | OVDVCCD_OK | R | RW | 1 | OVD indicates vccd is ok. This will always read 1, because a detected over-over-voltage condition will reset the chip. |
| 16 | OCD_ACT_LINREG_OK | R | RW | 1 | OCD indicates the current drawn from the linear Active Regulator is ok. This will always read 1, because a detected over-current condition will reset the chip. |
| 17 | OCD_DPSLP_REG_OK | R | RW | 1 | OCD indicates the current drawn from the linear DeepSleep Regulator is ok. This will always read 1, because a detected over-current condition will reset the chip. |

### 31.11.17 PWR_LVD_CTL

**Description:** High Voltage / Low Voltage Detector (HVLVD) Configuration Register
**Address:** 0x40261020
**Offset:** 0x1020
**Retention:** Retained
**IsDeepSleep:** Yes
**Comment:** Trim and configuration bits for Voltage Monitoring System.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | HVLVD1_EN_HT [15:15] | HVLVD1_DPSLP_EN_HT [14:14] | None [13:13] | HVLVD1_TRIPSEL_HT [12:8] | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:19] | | | | | HVLVD1_ACTION [18:18] | HVLVD1_EDGE_SEL [17:16] | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 8:12 | HVLVD1_TRIPSEL_HT | RW | R | 0 | Threshold selection for HVLVD1 for HT products. Detector accuracy is +/-4 percent of the nominal values listed below. Disable the detector (HVLVD1_EN=0) before changing the threshold. NOTE: When increasing the trip selection bits, the user must increase by one binary unit in 10us cycle, otherwise there is the potential to generate an HV OVD reset.<br>0: rise 2.825V (nom), fall=2.8V (nom)<br>1: rise 2.925V (nom), fall=2.9V (nom)<br>2: rise 3.025V (nom), fall=3.0V (nom)<br>3: rise 3.125V (nom), fall=3.1V (nom)<br>4: rise 3.225V (nom), fall=3.2V (nom)<br>5: rise 3.325V (nom), fall=3.3V (nom)<br>6: rise 3.425V (nom), fall=3.4V (nom)<br>7: rise 3.525V (nom), fall=3.5V (nom)<br>8: rise 3.625V (nom), fall=3.6V (nom)<br>9: rise 3.725V (nom), fall=3.7V (nom)<br>10: rise 3.825V (nom), fall=3.8V (nom)<br>11: rise 3.925V (nom), fall=3.9V (nom)<br>12: rise 4.025V (nom), fall=4.0V (nom)<br>13: rise 4.125V (nom), fall=4.1V (nom)<br>14: rise 4.225V (nom), fall=4.2V (nom)<br>15: rise 4.325V (nom), fall=4.3V (nom)<br>16: rise 4.425V (nom), fall=4.4V (nom)<br>17: rise 4.525V (nom), fall=4.5V (nom)<br>18: rise 4.625V (nom), fall=4.6V (nom)<br>19: rise 4.725V (nom), fall=4.7V (nom)<br>20: rise 4.825V (nom), fall=4.8V (nom)<br>21: rise 4.925V (nom), fall=4.9V (nom)<br>22: rise 5.025V (nom), fall=5.0V (nom)<br>23: rise 5.125V (nom), fall=5.1V (nom)<br>24: rise 5.225V (nom), fall=5.2V (nom)<br>25: rise 5.325V (nom), fall=5.3V (nom)<br>others: reserved |
| 14 | HVLVD1_DPSLP_EN_HT | RW | R | 0 | Keep HVLVD1 voltage monitor enabled during DEEPSLEEP mode. This field is only used when HVLVD1_EN_HT==1. |
| 15 | HVLVD1_EN_HT | RW | R | 0 | Enable HVLVD1 voltage monitor. This detector monitors vddd only. Do not change other HVLVD1 settings when enabled. |
| 16:17 | HVLVD1_EDGE_SEL | RW | R | 0 | Sets which edge(s) will trigger an action when the threshold is crossed. |
| | DISABLE | | | 0 | Disabled |
| | RISING | | | 1 | Rising edge |
| | FALLING | | | 2 | Falling edge |
| | BOTH | | | 3 | Both rising and falling edges |
| 18 | HVLVD1_ACTION | RW | R | 0 | Action taken when the threshold is crossed in the programmed directions(s) |
| | INTERRUPT | | | 0 | Generate an interrupt |
| | FAULT | | | 1 | Generate a fault |

### 31.11.18 PWR_LVD_CTL2

**Description:** High Voltage / Low Voltage Detector (HVLVD) Configuration Register #2
**Address:** 0x40261024
**Offset:** 0x1024
**Retention:** Retained
**IsDeepSleep:** Yes
**Comment:** Trim and configuration bits for Voltage Monitoring System.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | HVLVD2_EN_HT [15:15] | HVLVD2_DPSLP_EN_HT [14:14] | None [13:13] | HVLVD2_TRIPSEL_HT [12:8] | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:19] | | | | | HVLVD2_ACTION [18:18] | HVLVD2_EDGE_SEL [17:16] | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 8:12 | HVLVD2_TRIPSEL_HT | RW | R | 0 | Threshold selection for HVLVD2 for HT products. Detector accuracy is +/-4 percent of the nominal values listed below. Disable the detector (HVLVD1_EN=0) before changing the threshold. NOTE: When increasing the trip selection bits, the user must increase by one binary unit in 10us cycle, otherwise there is the potential to generate an HV OVD reset.<br>0: rise 2.825V (nom), fall=2.8V (nom)<br>1: rise 2.925V (nom), fall=2.9V (nom)<br>2: rise 3.025V (nom), fall=3.0V (nom)<br>3: rise 3.125V (nom), fall=3.1V (nom)<br>4: rise 3.225V (nom), fall=3.2V (nom)<br>5: rise 3.325V (nom), fall=3.3V (nom)<br>6: rise 3.425V (nom), fall=3.4V (nom)<br>7: rise 3.525V (nom), fall=3.5V (nom)<br>8: rise 3.625V (nom), fall=3.6V (nom)<br>9: rise 3.725V (nom), fall=3.7V (nom)<br>10: rise 3.825V (nom), fall=3.8V (nom)<br>11: rise 3.925V (nom), fall=3.9V (nom)<br>12: rise 4.025V (nom), fall=4.0V (nom)<br>13: rise 4.125V (nom), fall=4.1V (nom)<br>14: rise 4.225V (nom), fall=4.2V (nom)<br>15: rise 4.325V (nom), fall=4.3V (nom)<br>16: rise 4.425V (nom), fall=4.4V (nom)<br>17: rise 4.525V (nom), fall=4.5V (nom)<br>18: rise 4.625V (nom), fall=4.6V (nom)<br>19: rise 4.725V (nom), fall=4.7V (nom)<br>20: rise 4.825V (nom), fall=4.8V (nom)<br>21: rise 4.925V (nom), fall=4.9V (nom)<br>22: rise 5.025V (nom), fall=5.0V (nom)<br>23: rise 5.125V (nom), fall=5.1V (nom)<br>24: rise 5.225V (nom), fall=5.2V (nom)<br>25: rise 5.325V (nom), fall=5.3V (nom)<br>others: reserved |
| 14 | HVLVD2_DPSLP_EN_HT | RW | R | 0 | Keep HVLVD2 voltage monitor enabled during DEEPSLEEP mode. This field is only used when HVLVD1_EN_HT==1. |
| 15 | HVLVD2_EN_HT | RW | R | 0 | Enable HVLVD2 voltage monitor. This detector monitors vddd only. Do not change other HVLVD2 settings when enabled. |
| 16:17 | HVLVD2_EDGE_SEL | RW | R | 0 | Sets which edge(s) will trigger an action when the threshold is crossed. |
| | DISABLE | | | 0 | Disabled |
| | RISING | | | 1 | Rising edge |
| | FALLING | | | 2 | Falling edge |
| | BOTH | | | 3 | Both rising and falling edges |
| 18 | HVLVD2_ACTION | RW | R | 0 | Action taken when the threshold is crossed in the programmed directions(s) |
| | INTERRUPT | | | 0 | Generate an interrupt |
| | FAULT | | | 1 | Generate a fault |

### 31.11.19 PWR_REGHC_CTL

**Description:** REGHC Control Register
**Address:** 0x40261028
**Offset:** 0x1028
**Retention:** Retained
**IsDeepSleep:** Yes
**Comment:** Control for the high-current regulator. This regulator requires external components. See datasheet. This register is only reset by HV resets (XRES, POR, BOD, OVD, OCD, HIBERNATE wakeup).
**Default:** 0x40000104

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | REGHC_VADJ [7:4] | | | | REGHC_PMIC_DRV_VOUT [3:2] | | None [1:1] | REGHC_MODE [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:15] | REGHC_PMIC_RADJ [14:12] | | | REGHC_PMIC_USE_RADJ [11:11] | REGHC_PMIC_USE_LINREG [10:10] | None [9:9] | REGHC_VADJ [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | REGHC_PMIC_STATUS_WAIT [23:20] | | | | REGHC_PMIC_STATUS_POLARITY [19:19] | REGHC_PMIC_STATUS_INEN [18:18] | REGHC_PMIC_CTL_POLARITY [17:17] | REGHC_PMIC_CTL_OUTEN [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | REGHC_CONFIGURED [31:31] | REGHC_TRANS_USE_OCD [30:30] | REGHC_PMIC_STATUS_WAIT [29:24] | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | REGHC_MODE | RW | A | 0 | REGHC control mode:<br>0: external transistor connected,<br>1: external PMIC connected |
| 2:3 | REGHC_PMIC_DRV_VOUT | RW | A | 1 | Setting for DRV_VOUT pin for PMIC mode. See REGHC_VADJ for calculation of vadj.<br>2'b00: DRV_VOUT=vccd*0.9/vadj;<br>2'b01: DRV_VOUT=vccd*0.8/vadj;<br>2'b10: DRV_VOUT=vccd*0.6/vadj;<br>2'b11: DRV_VOUT=vccd |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 4:8 | REGHC_VADJ | RW | A | 16 | Regulator output trim according to the formula vadj=(1.020V + REGHC_VADJ*0.005V) plus an offset described below. For example, 0x1A=>1.15V (nominal).<br><br>For transistor mode, REGHC will dynamically adjust DRV_VOUT so the supply targets the vadj voltage. Adjust for die to die variation by adding the signed offset value in SFLASH SRSS_PWR_OFFSET.REGHC_TRANS_VADJ_OFFSET.<br><br>Note: SRSS_PWR_OFFSET.REGHC_TRANS_VADJ_OFFSET value is calculated using the default value of the REGHC_VADJ: 0x10 (1.1V) and applies to the full range of REGHC target voltages.<br><br>For PMIC mode, adjust for die to die variation by adding the signed offset value in SFLASH SRSS_PWR_OFFSET.PMIC_VADJ_OFFSET to the nominal calculated code. For PMIC mode, also see REGHC_PMIC_DRV_VOUT. |
| 10 | REGHC_PMIC_USE_LINREG | RW | A | 0 | For REGHC external PMIC mode, controls whether hardware sequencer keeps the internal Active Linear Regulator enabled to improve supply supervision of vccd. When using this feature, if the PMIC fails to keep vccd above the internal regulator target, then the internal regulator will attempt to recover vccd. If the regulator current is too high, the regulator triggers an over-current detector (OCD) reset.<br>0: Internal Active Linear Regulator disabled after PMIC enabled. OCD is disabled.;<br>1: Internal Active Linear Regulator kept enabled. See datasheet for minimum PMIC vccd input to prevent OCD. |
| 11 | REGHC_PMIC_USE_RADJ | RW | A | 0 | Controls whether hardware sequencer enables reset voltage adjustment circuit when enabling a PMIC. |
| 12:14 | REGHC_PMIC_RADJ | RW | A | 0 | Reset voltage adjustment for PMIC as a factor (Vfbk/Vref) where Vfbk is the feedback voltage and Vref is the PMIC internal reference. The reset voltage adjustment circuit is enabled by the hardware sequencer if REGHC_PMIC_USE_RADJ=1. PMIC have Vref of 0.8V or 0.9V, and the resulting reset voltage (Vreset) are precalculated in the table below:<br>3'b000: Vfbk/Vref=1.0000, Vreset=.800V@(Vref=0.8V), .900V@(Vref=0.9V);<br>3'b001: Vfbk/Vref=1.0556, Vreset=.844V@(Vref=0.8V), .950V@(Vref=0.9V);<br>3'b010: Vfbk/Vref=1.1111, Vreset=.889V@(Vref=0.8V), 1.000V@(Vref=0.9V);<br>3'b011: Vfbk/Vref=1.1250, Vreset=.900V@(Vref=0.8V), 1.013V@(Vref=0.9V);<br>3'b100: Vfbk/Vref=1.1667, Vreset=.933V@(Vref=0.8V), 1.050V@(Vref=0.9V);<br>3'b101: Vfbk/Vref=1.1875, Vreset=.950V@(Vref=0.8V), 1.069V@(Vref=0.9V);<br>3'b110: Vfbk/Vref=1.2500, Vreset=1.000V@(Vref=0.8V), 1.125V@(Vref=0.9V);<br>3'b111: Vfbk/Vref=1.3125, Vreset=1.050V@(Vref=0.8V), 1.181V@(Vref=0.9V); |
| 16 | REGHC_PMIC_CTL_OUTEN | RW | A | 0 | Output enable for PMIC enable pin. Set this bit high to enable the driver on this pin. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 17 | REGHC_PMIC_CTL _POLARITY | RW | A | 0 | Polarity used to enable the PMIC. The sequencer uses REGHC_PMIC_CTL_POLARITY to enable the PMIC, and it uses the complement to disable the PMIC. |
| 18 | REGHC_PMIC_STATUS _INEN | RW | A | 0 | Input buffer enable for PMIC status input. Set this bit high to enable the input receiver. |
| 19 | REGHC_PMIC_STATUS _POLARITY | RW | A | 0 | The polarity used to trigger a reset action based on the PMIC status input. The reset system triggers a reset when the unmasked PMIC status matches this value. |
| 20:29 | REGHC_PMIC_STATUS _WAIT | RW | A | 0 | Wait count in 4us steps after PMIC status ok. This is used by the hardware sequencer to allow additional settling time before disabling the internal regulator. The LSB is 32 IMO periods which results in a nominal LSB step of 4us. |
| 30 | REGHC_TRANS_USE _OCD | RW | A | 1 | Reserved. Always write high. |
| 31 | REGHC_CONFIGURED | RW1S | A | 0 | Indicates the REGHC has been configured. This is used to know if REGHC should be enabled in response to a debug power up request. It is recommended to not change REGHC settings after REGHC_CONFIGURED is set high, because it can cause failure if REGHC is enabled or transitioning. |

### 31.11.20 PWR_REGHC_STATUS

**Description:** REGHC Status Register
**Address:** 0x4026102C
**Offset:** 0x102C
**Retention:** Retained
**IsDeepSleep:** Yes
**Comment:** Status register for REGHC.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:3] | | | | | REGHC _CKT_OK [2:2] | REGHC _OCD_OK [1:1] | REGHC _ENABLED [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:13] | | | REGHC _PMIC _STATUS _OK [12:12] | None [11:10] | | REGHC _OV_OUT [9:9] | REGHC _UV_OUT [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | REGHC _SEQ _BUSY [31:31] | None [30:24] | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | REGHC_ENABLED | R | RW | 0 | Indicates the state of the REGHC enable/disable sequencer. This bit is only valid when REGHC_SEQ_BUSY==0.<br>0: REGHC sequencer indicates REGHC is disabled.<br>1: REGHC sequencer indicates REGHC is enabled. |
| 1 | REGHC_OCD_OK | R | RW | 0 | Indicates the over-current detector is operating and the current drawn from REGHC is within limits. OCD is only a choice for transistor mode, and it is disabled for PMIC mode.<br>0: Current measurement exceeds limit or detector is OFF,<br>1: Current measurement within limit |
| 2 | REGHC_CKT_OK | R | RW | 0 | Indicates the REGHC circuit is enabled and operating. It does not indicate that the voltage and current are within required limits for robust operation.<br>0: REGHC circuit is not ready. This can occur if the REGHC circuit is disabled or if it was recently enabled.<br>1: REGHC circuit is enabled and operating. |
| 8 | REGHC_UV_OUT | R | RW | 0 | Reserved |
| 9 | REGHC_OV_OUT | R | RW | 0 | Reserved |
| 12 | REGHC_PMIC_STATUS _OK | R | RW | 0 | Indicates the PMIC status is ok. This includes polarity adjustment according to REGHC_PMIC_STATUS_POLARITY.<br>0: PMIC status is not ok or PMIC input buffer is disabled (REGHC_PMIC_STATUS_INEN==0);<br>1: PMIC status input buffer is enabled and indicates ok |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 31 | REGHC_SEQ_BUSY | R | RW | 0 | Indicates the REGHC enable/disable sequencer is busy transitioning to/from REGHC.<br>0: Sequencer is not busy;<br>1: Sequencer is busy either enabling or disabling REGHC. |

### 31.11.21 PWR_REGHC_CTL2

**Description:** REGHC Control Register 2
**Address:** 0x40261030
**Offset:** 0x1030
**Retention:** Retained
**IsDeepSleep:** Yes
**Comment:** Control for the high-current regulator. This regulator requires external components. See datasheet. This register is only reset by HV resets (XRES, POR, BOD, OVD, OCD, HIBERNATE wakeup).
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | REGHC_PMIC_STATUS_TIMEOUT [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | REGHC_EN [31:31] | None [30:24] | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | REGHC_PMIC_STATUS_TIMEOUT | RW | A | 0 | Timeout while waiting for REGHC_PMIC_STATUS_OK==1 when switching to PMIC.<br>0: disables timeout.<br>>0: enables timeout of REGHC_PMIC_STATUS_TIMEOUT*128us (nominal, clocked by IMO). Timeout expiration triggers reset. |
| 31 | REGHC_EN | RW | A | 0 | Enable REGHC. This bit will not set if REGHC_CONFIGURED==0. Use PWR_REGHC_STATUS.ENABLED to know the actual status of REGHC. It will differ from this bit in the following cases:<br>A) Do not enter DEEPSLEEP while the sequencer is busy (see PWR_REGHC_STATUS.REGHC_SEQ_BUSY). The hardware sequencer disables REGHC during DEEPSLEEP entry and enables it upon wakeup.<br>B) The debugger requests the chip remain powered up. Hardware prevents REGHC from disabling when this bit is cleared. Hardware does not automatically enable REGHC in response to debugger power up request. If this bit is low when the debugger deasserts the power up request, the hardware sequencer will disable REGHC. |

### 31.11.22 PWR_REGHC_CTL4

**Description:** REGHC Control Register 4
**Address:** 0x40261038
**Offset:** 0x1038
**Retention:** Retained
**IsDeepSleep:** Yes
**Comment:** Control for the high-current regulator. This regulator requires external components. See datasheet. This register is only reset by HV resets (XRES, POR, BOD, OVD, OCD, HIBERNATE wakeup). Do not change this register after setting PWR_REGHC_CTL.REGHC_CONFIGURED.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | REGHC_PMIC_DPSLP [31:31] | REGHC_PMIC_VADJ_DIS [30:30] | None [29:24] | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 30 | REGHC_PMIC_VADJ_DIS | RW | A | 0 | When operating in PMIC mode, disables the VADJ circuitry. This can be used to decrease current consumption if the entire feedback network is outside the device.<br>0: Device generates VADJ when PMIC is enabled. This allows the feedback loop to compensate for voltage drops in the PCB and package.<br>1: Device does not generate VADJ, and it must not be part of the PMIC feedback loop. This reduces current by turning off the internal resistor divider that generates VADJ. This setting is ineffective when REGHC_PMIC_RADJ_EN==1, and VADJ is generated in that case when PMIC is enabled. |
| 31 | REGHC_PMIC_DPSLP | RW | A | 0 | When operating in PMIC mode, configures PMIC behavior during DEEPSLEEP.<br>0: Device operates from internal regulators during DEEPSLEEP. If PMIC is enabled at the beginning of the DEEPSLEEP transition, hardware changes to the internal regulators and disables the PMIC.<br>1: DEEPSLEEP transition does not change PMIC enable. |

### 31.11.23 PWR_HIB_DATA

**Description:** HIBERNATE Data Register
**Address:** 0x40261040
**Offset:** 0x1040
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register can retain information during HIBERNATE mode.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | HIB_DATA [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | HIB_DATA [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | HIB_DATA [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | HIB_DATA [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | HIB_DATA | RW | A | 0 | Additional data that is retained through a HIBERNATE/WAKEUP sequence that can be used by firmware for any application-specific purpose. Note that waking up from HIBERNATE using XRES will reset this register. |

### 31.11.24 CLK_PATH_SELECT

**Description:** Clock Path Select Register
**Address:** 0x40261200
**Offset:** 0x1200
**Retention:** Retained
**IsDeepSleep:** Yes
**Comment:** Selects a source for clock path. The output of this mux can be used as the root of a clock tree. If there is a PLL on the path, this mux output is the PLL reference clock. The related PLL register contains a mux to select whether the clock path uses the PLL output or is bypassed to the PLL reference clock.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:3] | | | | | PATH_MUX [2:0] | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:2 | PATH_MUX | RW | R | 0 | Selects a source for clock PATH<i>. Note that not all products support all clock sources. Selecting a clock source that is not supported will result in undefined behavior. It takes four cycles of the originally selected clock to switch away from it. Do not disable the original clock during this time. |
| | IMO | | | 0 | IMO - Internal R/C Oscillator |
| | EXTCLK | | | 1 | EXTCLK - External Clock Pin |
| | ECO | | | 2 | ECO - External-Crystal Oscillator |
| | ALTHF | | | 3 | ALTHF - Alternate High-Frequency clock input (product-specific clock) |
| | DSI_MUX | | | 4 | DSI_MUX - Output of DSI mux for this path. Using a DSI source directly as root of HFCLK will result in undefined behavior. |
| | LPECO | | | 5 | LPECO - Low-Power External-Crystal Oscillator |

### 31.11.25 CLK_ROOT_SELECT

**Description:** Clock Root Select Register
**Address:** 0x40261240
**Offset:** 0x1240
**Retention:** Retained
**IsDeepSleep:** Yes
**Comment:** Selects a root for a HF clock tree and DSI input. There is a copy of this register for each clock root.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:6] | | ROOT_DIV [5:4] | | ROOT_MUX [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:9] | | | | | | | DIRECT _MUX [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | ENABLE [31:31] | None [30:24] | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | ROOT_MUX | RW | R | 0 | Selects a clock path as the root of HFCLK<k> and for SRSS DSI input <k>. Use CLK_PATH_SELECT[i] to configure the desired path. Some paths may have FLL or PLL available (product-specific), and the control and bypass mux selections of these are in other registers. Configure the FLL using CLK_FLL_CONFIG register. Configure a PLL using the related CLK_PLL_CONFIG[k] register. Note that not all products support all clock sources. Selecting a clock source that is not supported will result in undefined behavior. It takes four cycles of the originally selected clock to switch away from it. Do not disable the original clock during this time. |
| | PATH0 | | | 0 | Select PATH0 (can be configured for FLL) |
| | PATH1 | | | 1 | Select PATH1 (can be configured for PLL0, if available in the product) |
| | PATH2 | | | 2 | Select PATH2 (can be configured for PLL1, if available in the product) |
| | PATH3 | | | 3 | Select PATH3 (can be configured for PLL2, if available in the product) |
| | PATH4 | | | 4 | Select PATH4 (can be configured for PLL3, if available in the product) |
| | PATH5 | | | 5 | Select PATH5 (can be configured for PLL4, if available in the product) |
| | PATH6 | | | 6 | Select PATH6 (can be configured for PLL5, if available in the product) |
| | PATH7 | | | 7 | Select PATH7 (can be configured for PLL6, if available in the product) |
| | PATH8 | | | 8 | Select PATH8 (can be configured for PLL7, if available in the product) |
| | PATH9 | | | 9 | Select PATH9 (can be configured for PLL8, if available in the product) |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| | PATH10 | | | 10 | Select PATH10 (can be configured for PLL9, if available in the product) |
| | PATH11 | | | 11 | Select PATH11 (can be configured for PLL10, if available in the product) |
| | PATH12 | | | 12 | Select PATH12 (can be configured for PLL11, if available in the product) |
| | PATH13 | | | 13 | Select PATH13 (can be configured for PLL12, if available in the product) |
| | PATH14 | | | 14 | Select PATH14 (can be configured for PLL13, if available in the product) |
| | PATH15 | | | 15 | Select PATH15 (can be configured for PLL14, if available in the product) |
| 4:5 | ROOT_DIV | RW | R | 0 | Selects predivider value for this clock root and DSI input. This divider is after DIRECT_MUX. For products with DSI, the output of this mux is routed to DSI for use as a signal. For products with clock supervision, the output of this mux is the monitored clock for CSV_HF<k>. |
| | NO_DIV | | | 0 | Transparent mode, feed through selected clock source w/o dividing. |
| | DIV_BY_2 | | | 1 | Divide selected clock source by 2 |
| | DIV_BY_4 | | | 2 | Divide selected clock source by 4 |
| | DIV_BY_8 | | | 3 | Divide selected clock source by 8 |
| 8 | DIRECT_MUX | RW | A | MASK_DIRECTMUX_DEF | Direct selection mux that allows IMO to bypass most of the clock mux structure. For products with multiple regulators, this mux can be used to reduce current without requiring significant reconfiguration of the clocking network. The default value of HFCLK<0>==ROOT_MUX, and the default value for other clock trees is product-specific. |
| | IMO | | | 0 | Select IMO |
| | ROOT_MUX | | | 1 | Select ROOT_MUX selection |
| 31 | ENABLE | RW | A | 0 | Enable for this clock root. All clock roots default to disabled (ENABLE==0) except HFCLK0, which cannot be disabled. |

### 31.11.26 CLK_SELECT

**Description:** Clock selection register
**Address:** 0x40261500
**Offset:** 0x1500
**Retention:** Retained
**IsDeepSleep:** Yes
**Comment:** Clock source selection register.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:3] | | | | | LFCLK_SEL [2:0] | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | PUMP_ENABLE [15:15] | PUMP_DIV [14:12] | | | PUMP_SEL [11:8] | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:2 | LFCLK_SEL | RW | A | 0 | Select source for LFCLK. Note that not all products support all clock sources. Selecting a clock source that is not supported will result in undefined behavior. Writes to this field are ignored unless the WDT is unlocked using WDT_LOCK register. It takes four cycles of the originally selected clock to switch away from it. Do not disable the original clock during this time. |
| | ILO0 | | | 0 | ILO0 - Internal Low-speed Oscillator #0. |
| | WCO | | | 1 | WCO - Watch-Crystal Oscillator. Requires Backup domain to be present and properly configured (including external watch crystal, if used). |
| | ALTLF | | | 2 | ALTLF - Alternate Low-Frequency Clock. Capability is product-specific |
| | PILO | | | 3 | PILO - Precision ILO. If present, it works in DEEPSLEEP and higher modes. Does not work in HIBERNATE mode. |
| | ILO1 | | | 4 | ILO1 - Internal Low-speed Oscillator #1, if present. |
| | ECO_PRESCALER | | | 5 | ECO_PRESCALER - External-Crystal Oscillator after prescaling, if present. Does not work in DEEPSLEEP or HIBERNATE modes. Intended for applications that operate in ACTIVE/SLEEP modes only. This option is only valid when ECO is present in the product. |
| | LPECO_PRESCALER | | | 6 | LPECO_PRESCALER - Low-Power External-Crystal Oscillator after prescaling, if present. This choice works in ACTIVE/SLEEP/DEEPSLEEP modes. This option is only valid when LPECO is present in the product. |
| 8:11 | PUMP_SEL | RW | R | 0 | Reserved. Not used the product. |
| 12:14 | PUMP_DIV | RW | R | 0 | Reserved. Not used in the product. |
| | NO_DIV | | | 0 | N/A |
| | DIV_BY_2 | | | 1 | N/A |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| | DIV_BY_4 | | | 2 | N/A |
| | DIV_BY_8 | | | 3 | N/A |
| | DIV_BY_16 | | | 4 | N/A |
| 15 | PUMP_ENABLE | RW | R | 0 | Reserved. Not used in the product. |

### 31.11.27 CLK_ILO0_CONFIG

**Description:** ILO0 Configuration
**Address:** 0x40261508
**Offset:** 0x1508
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Configuration register for ILO0. ILO0 configuration and trims are reset by XRES, HIBERNATE, and power-related resets, unless otherwise noted.
**Default:** 0x80000000

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:1] | | | | | | | ILO0_BACKUP [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | ENABLE [31:31] | ILO0_MON_ENABLE [30:30] | None [29:24] | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | ILO0_BACKUP | RW | A | 0 | This register indicates that ILO0 should stay enabled during XRES and HIBERNATE modes. If backup voltage domain is implemented on the product, this bit also indicates if ILO0 should stay enabled through power-related resets on other supplies, e.g.. BOD on VDDD/VCCD. Writes to this field are ignored unless the WDT is unlocked using WDT_LOCK register. This register is reset when the backup logic resets.<br>0: ILO0 turns off during XRES, HIBERNATE, and power-related resets. ILO0 configuration and trims are reset by these events.<br>1: ILO0 stays enabled, as described above. ILO0 configuration and trims are not reset by these events. |
| 30 | ILO0_MON_ENABLE | RW | A | 0 | Reserved. Always write a zero. Writes to this field are ignored unless the WDT is unlocked using WDT_LOCK register. |
| 31 | ENABLE | RW | A | 1 | Master enable for ILO. Writes to this field are ignored unless the WDT is unlocked using WDT_LOCK register.<br><br>HT-variant: This register will not clear unless PWR_CTL2.BGREF_LPMODE==0. After enabling, the first ILO0 cycle occurs within 12us and is +/-10 percent accuracy. Thereafter, ILO0 is +/-5 percent accurate. |

### 31.11.28 CLK_ILO1_CONFIG

**Description:** ILO1 Configuration
**Address:** 0x4026150C
**Offset:** 0x150C
**Retention:** Retained
**IsDeepSleep:** Yes
**Comment:** Configuration register for ILO1.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | ENABLE [31:31] | ILO1_MON_ENABLE [30:30] | None [29:24] | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 30 | ILO1_MON_ENABLE | RW | R | 0 | Reserved. Always write a zero. |
| 31 | ENABLE | RW | R | 0 | Master enable for ILO1.<br><br>HT-variant: After enabling, the first ILO1 cycle occurs within 12us and is +/-10 percent accuracy. Thereafter, ILO1 is +/-5 percent accurate. |

### 31.11.29 CLK_IMO_CONFIG

**Description:** IMO Configuration
**Address:** 0x40261518
**Offset:** 0x1518
**Retention:** Retained
**IsDeepSleep:** Yes
**Comment:** Internal high speed R/C oscillator configuration register. Note that this oscillator comes up active on power up. The oscillator provides the primary system clock (HFCLK) on power up until firmware configures differently. This oscillator is also used before system start to count out power up delays. This is done in fast IMO (FIMO) mode that does not require any external references and runs at a fixed 12MHz.
**Default:** 0x80000000

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | ENABLE [31:31] | None [30:24] | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 31 | ENABLE | RW | R | 1 | Master enable for IMO oscillator. This bit must be high at all times for all functions to work properly. Hardware will automatically disable the IMO during DEEPSLEEP, HIBERNATE, and XRES. |

### 31.11.30 CLK_ECO_CONFIG

**Description:** ECO Configuration Register
**Address:** 0x4026151C
**Offset:** 0x151C
**Retention:** Retained
**IsDeepSleep:** Yes
**Comment:** Internal high speed oscillator configuration register for External-Crystal.
**Default:** 0x2

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:2] | | | | | | AGC_EN [1:1] | None [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | ECO_EN [31:31] | None [30:29] | | ECO_DIV_ENABLE [28:28] | ECO_DIV_DISABLE [27:27] | None [26:24] | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 1 | AGC_EN | RW | R | 1 | Automatic Gain Control (AGC) enable. When set, the oscillation amplitude is controlled to the level selected by CLK_ECO_CONFIG2.ATRIM. When low, the amplitude is not explicitly controlled and can be as high as the vddd supply. WARNING: use care when disabling AGC because driving a crystal beyond its rated limit can permanently damage the crystal. |
| 27 | ECO_DIV_DISABLE | RW | RW1C | 0 | ECO prescaler disable command (mutually exclusive with ECO_DIV_ENABLE). SW sets this field to '1' and HW sets this field to '0'.<br><br>HW sets ECO_DIV_DISABLE field to '0' immediately and HW sets CLK_ECO_PRESCALE.ECO_DIV_EN field to '0' immediately. |
| 28 | ECO_DIV_ENABLE | RW | RW1C | 0 | ECO prescaler enable command (mutually exclusive with ECO_DIV_DISABLE). ECO Prescaler only works in ACTIVE and SLEEP modes. SW sets this field to '1' to enable the divider and HW sets this field to '0' to indicate that divider enabling has completed. When the divider is enabled, its integer and fractional counters are initialized to '0'. If a divider is to be re-enabled using different integer and fractional divider values, the SW should follow these steps:<br>0: Disable the divider using the ECO_DIV_DISABLE field.<br>1: Configure CLK_ECO_PRESCALE registers.<br>2: Enable the divider using the ECO_DIV_ENABLE field.<br><br>HW sets the ECO_DIV_ENABLE field to '0' when the enabling is performed and HW set CLK_ECO_PRESCALER.ENABLED to '1' when the enabling is performed. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 31 | ECO_EN | RW | R | 0 | Master enable for ECO oscillator. Configure the settings in CLK_ECO_CONFIG2 to work with the selected crystal, before enabling ECO. |

### 31.11.31 CLK_ECO_PRESCALE

**Description:** ECO Prescaler Configuration Register
**Address:** 0x40261520
**Offset:** 0x1520
**Retention:** Retained
**IsDeepSleep:** Yes
**Comment:** Fractional prescaler value to bring down the average ECO frequency to 32768 Hz if used as LFCLK. Do not change divider settings while ECO prescaler is enabled or enabling.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:1] | | | | | | | ECO_DIV_ENABLED [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | ECO_FRAC_DIV [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | ECO_INT_DIV [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:26] | | | | | | ECO_INT_DIV [25:24] | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | ECO_DIV_ENABLED | R | RW | 0 | ECO prescaler enabled. HW sets this field to '1' as a result of an CLK_ECO_CONFIG.ECO_DIV_ENABLE command. HW sets this field to '0' as a result on a CLK_ECO_CONFIG.ECO_DIV_DISABLE command. |
| 8:15 | ECO_FRAC_DIV | RW | R | 0 | 8-bit fractional value, sufficient to get prescaler output within the +/-65ppm calibration range. Subtract one from the desired divide value when writing this field. For example, to divide by 1, write ECO_FRAC_DIV=0. Do not change this setting when ECO Prescaler is enabled. |
| 16:25 | ECO_INT_DIV | RW | R | 0 | 10-bit integer value allows for ECO frequencies up to 33.55MHz. Subtract one from the desired divide value when writing this field. For example, to divide by 1, write ECO_INT_DIV=0. Do not change this setting when ECO Prescaler is enabled. |

### 31.11.32 CLK_ECO_STATUS

**Description:** ECO Status Register
**Address:** 0x40261524
**Offset:** 0x1524
**Retention:** Retained
**IsDeepSleep:** Yes
**Comment:** Status indications for external crystal oscillator (ECO).
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:2] | | | | | | ECO_READY [1:1] | ECO_OK [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | ECO_OK | R | W | 0 | Indicates the ECO internal oscillator circuit has sufficient amplitude. It may not meet the PPM accuracy or duty cycle spec. |
| 1 | ECO_READY | R | W | 0 | Indicates the ECO internal oscillator circuit has had enough time to fully stabilize. This is the output of a counter since ECO was enabled, and it does not check the ECO output. It is recommended to also confirm ECO_OK==1. |

### 31.11.33 CLK_FLL_CONFIG

**Description:** FLL Configuration Register
**Address:** 0x40261530
**Offset:** 0x1530
**Retention:** Retained
**IsDeepSleep:** Yes
**Comment:** This register contains frequency lock loop (FLL) configuration. FLL circuit settings should not be changed while it is a selected clock (connected to logic). This prevents clock glitches that can crash the logic. Deselect the FLL using .BYPASS_SEL=FLL_REF
**Default:** 0x1000000

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | FLL_MULT [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | FLL_MULT [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:18] | | | | | | FLL_MULT [17:16] | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | FLL_ENABLE [31:31] | None [30:25] | | | | | | FLL_OUTPUT_DIV [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:17 | FLL_MULT | RW | R | 0 | Multiplier to determine CCO frequency in multiples of the frequency of the selected reference clock (Fref).<br><br>Ffll = (FLL_MULT) * (Fref / REFERENCE_DIV) / (OUTPUT_DIV+1) |
| 24 | FLL_OUTPUT_DIV | RW | R | 1 | Control bits for Output divider. Set the divide value before enabling the FLL, and do not change it while FLL is enabled.<br>0: no division<br>1: divide by 2 |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 31 | FLL_ENABLE | RW | R | 0 | Master enable for FLL. The FLL requires firmware sequencing when enabling and disabling. Hardware handles sequencing automatically when entering/exiting DEEPSLEEP.<br><br>To enable the FLL, use the following sequence:<br>1) Configure FLL and CCO settings. Do not modify CLK_FLL_CONFIG3.BYPASS_SEL (must be AUTO) or CLK_FLL_CONFIG.FLL_ENABLE (must be 0).<br>2) Enable the CCO by writing CLK_FLL_CONFIG4.CCO_ENABLE=1<br>3) Wait until CLK_FLL_STATUS.CCO_READY==1.<br>4) Ensure the reference clock has stabilized.<br>5) Write FLL_ENABLE=1.<br>6) Optionally wait until CLK_FLL_STATUS.LOCKED==1. The hardware automatically changes to the FLL output when LOCKED==1.<br><br>To disable the FLL, use the following sequence:<br>1) Write CLK_FLL_CONFIG3.BYPASS_SEL=FLL_REF.<br>2) Read CLK_FLL_CONFIG3.BYPASS_SEL to ensure the write completes (read is not optional).<br>3) Wait at least ten cycles of either FLL reference clock or FLL output clock, whichever is slower. It is recommended to use a HW counter (e.g. clock calibration counter, event generator) running on the slower clock.<br>4) Disable FLL with FLL_ENABLE=0.<br>5) Disable the CCO by writing CLK_FLL_CONFIG4.CCO_ENABLE=0.<br>6) Write CLK_FLL_CONFIG3.BYPASS_SEL=AUTO.<br>7) Read CLK_FLL_CONFIG3.BYPASS_SEL to ensure the write completes (read is not optional).<br>8) Wait three cycles of FLL reference clock. It is recommended to use a HW counter (e.g. clock calibration counter, event generator) running on the reference clock.<br><br>0: Block is powered off<br>1: Block is powered on |

### 31.11.34 CLK_FLL_CONFIG2

**Description:** FLL Configuration Register 2
**Address:** 0x40261534
**Offset:** 0x1534
**Retention:** Retained
**IsDeepSleep:** Yes
**Comment:** This register contains frequency lock loop (FLL) configuration. FLL circuit settings should not be changed while it is a selected clock (connected to logic). This prevents clock glitches that can crash the logic. Deselect the FLL using .BYPASS_SEL=FLL_REF
**Default:** 0x20001

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | FLL_REF_DIV [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:13] | | | FLL_REF_DIV [12:8] | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | LOCK_TOL [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | UPDATE_TOL [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:12 | FLL_REF_DIV | RW | R | 1 | Control bits for reference divider. Set the divide value before enabling the FLL, and do not change it while FLL is enabled.<br>0: illegal (undefined behavior)<br>1: divide by 1<br>...<br>8191: divide by 8191 |
| 16:23 | LOCK_TOL | RW | R | 2 | Lock tolerance sets the error threshold for when the FLL output is considered locked to the reference input. A high tolerance can be used to lock more quickly or allow less accuracy. The tolerance is the allowed difference between the count value for the ideal formula and the measured value.<br>0: tolerate error of 1 count value<br>1: tolerate error of 2 count values<br>...<br>255: tolerate error of 256 count values |
| 24:31 | UPDATE_TOL | RW | R | 0 | Update tolerance sets the error threshold for when the FLL will update the CCO frequency settings. The update tolerance is the allowed difference between the count value for the ideal formula and the measured value. UPDATE_TOL should be less than LOCK_TOL. |

### 31.11.35 CLK_FLL_CONFIG3

**Description:** FLL Configuration Register 3
**Address:** 0x40261538
**Offset:** 0x1538
**Retention:** Retained
**IsDeepSleep:** Yes
**Comment:** This register contains frequency lock loop (FLL) configuration. Do not change settings while the FLL is running, except BYPASS_SEL.
**Default:** 0x2800

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | FLL_LF_PGAIN [7:4] | | | | FLL_LF_IGAIN [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | SETTLING_COUNT [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:21] | | | SETTLING_COUNT [20:16] | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:30] | | BYPASS_SEL [29:28] | | None [27:24] | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | FLL_LF_IGAIN | RW | R | 0 | FLL Loop Filter Gain Setting #1. The proportional gain is the sum of FLL_LF_IGAIN and FLL_LF_PGAIN.<br>0: 1/256<br>1: 1/128<br>2: 1/64<br>3: 1/32<br>4: 1/16<br>5: 1/8<br>6: 1/4<br>7: 1/2<br>8: 1.0<br>9: 2.0<br>10: 4.0<br>11: 8.0<br>>=12: illegal |
| 4:7 | FLL_LF_PGAIN | RW | R | 0 | FLL Loop Filter Gain Setting #2. The proportional gain is the sum of FLL_LF_IGAIN and FLL_LF_PGAIN.<br>0: 1/256<br>1: 1/128<br>2: 1/64<br>3: 1/32<br>4: 1/16<br>5: 1/8<br>6: 1/4<br>7: 1/2<br>8: 1.0<br>9: 2.0<br>10: 4.0<br>11: 8.0<br>>=12: illegal |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 8:20 | SETTLING_COUNT | RW | R | 40 | Number of undivided reference clock cycles to wait after changing the CCO trim until the loop measurement restarts. A delay allows the CCO output to settle and gives a more accurate measurement. The default is tuned to an 8MHz reference clock since the IMO is expected to be the most common use case.<br>0: no settling time<br>1: wait one reference clock cycle<br>...<br>8191: wait 8191 reference clock cycles |
| 28:29 | BYPASS_SEL | RW | R | 0 | Bypass mux located just after FLL output. This register can be written while the FLL is enabled. When changing BYPASS_SEL, do not turn off the reference clock or CCO clock for five cycles (whichever is slower). In case of disabling FLL(FLL_ENABLE=0), additional five cycles are required. Refer to FLL disable sequence for more details in CLK_FLL_CONFIG->FLL_ENABLE. Whenever BYPASS_SEL is changed, it is required to read CLK_FLL_CONFIG3 to ensure the change takes effect. |
| | AUTO | | | 0 | Automatic using lock indicator. When unlocked, automatically selects FLL reference input (bypass mode). When locked, automatically selects FLL output. This can allow some processing to occur while the FLL is locking, such as after DEEPSLEEP wakeup. It is incompatible with clock supervision, because the frequency changes based on the lock signal. |
| | LOCKED_OR_NOTHING | | | 1 | Similar to AUTO, except the clock is gated off when unlocked. This is compatible with clock supervision, because the supervisors allow no clock during startup (until a timeout occurs), and the clock targets the proper frequency whenever it is running. |
| | FLL_REF | | | 2 | Select FLL reference input (bypass mode). Ignores lock indicator |
| | FLL_OUT | | | 3 | Select FLL output. Ignores lock indicator. |

### 31.11.36 CLK_FLL_CONFIG4

**Description:** FLL Configuration Register 4
**Address:** 0x4026153C
**Offset:** 0x153C
**Retention:** Retained
**IsDeepSleep:** Yes
**Comment:** This register contains frequency lock loop (FLL) configuration. Do not change settings while the FLL is running.
**Default:** 0xFF

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | CCO_LIMIT [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:11] | | | | | CCO_RANGE [10:8] | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | CCO_FREQ [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | CCO_ENABLE [31:31] | CCO_HW_UPDATE_DIS [30:30] | None [29:25] | | | | | CCO_FREQ [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | CCO_LIMIT | RW | R | 255 | Maximum CCO offset allowed (used to prevent FLL dynamics from selecting an CCO frequency that the logic cannot support) |
| 8:10 | CCO_RANGE | RW | R | 0 | Frequency range of CCO |
| | RANGE0 | | | 0 | Target frequency is in range [48, 64) MHz |
| | RANGE1 | | | 1 | Target frequency is in range [64, 85) MHz |
| | RANGE2 | | | 2 | Target frequency is in range [85, 113) MHz |
| | RANGE3 | | | 3 | Target frequency is in range [113, 150) MHz |
| | RANGE4 | | | 4 | Target frequency is in range [150, 200] MHz |
| 16:24 | CCO_FREQ | RW | RW | 0 | CCO frequency code. This is updated by HW when the FLL is enabled. It can be manually updated to use the CCO in an open loop configuration. The meaning of each frequency code depends on the range. |
| 30 | CCO_HW_UPDATE_DIS | RW | R | 0 | Disable CCO frequency update by FLL hardware<br>0: Hardware update of CCO settings is allowed. Use this setting for normal FLL operation.<br>1: Hardware update of CCO settings is disabled. Use this setting for open-loop FLL operation. |
| 31 | CCO_ENABLE | RW | R | 0 | Enable the CCO. It is required to enable the CCO before using the FLL.<br>0: Block is powered off<br>1: Block is powered on |

### 31.11.37 CLK_FLL_STATUS

**Description:** FLL Status Register
**Address:** 0x40261540
**Offset:** 0x1540
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** This register indicates status for the FLL. This register is synchronized during an AHB read transaction. This causes a number wait-states to be inserted in the transaction depending on the frequency ratio between system and FLL frequency.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:3] | | | | | CCO_READY [2:2] | UNLOCK_OCCURRED [1:1] | LOCKED [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | LOCKED | R | W | 0 | FLL Lock Indicator |
| 1 | UNLOCK_OCCURRED | RW1C | A | 0 | This bit sets whenever the FLL is enabled and goes out of lock. This bit stays set until cleared by firmware. |
| 2 | CCO_READY | R | RW | 0 | This indicates that the CCO is internally settled and ready to use. |

### 31.11.38 CLK_ECO_CONFIG2

**Description:** ECO Configuration Register 2
**Address:** 0x40261544
**Offset:** 0x1544
**Retention:** Retained
**IsDeepSleep:** Yes
**Comment:** Internal high speed oscillator configuration register for External-Crystal.
**Default:** 0x3

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | ATRIM [7:4] | | | | None [3:3] | WDTRIM [2:0] | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:15] | GTRIM [14:12] | | | RTRIM [11:10] | | FTRIM [9:8] | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:2 | WDTRIM | RW | R | 3 | Watch Dog Trim. Sets the minimum oscillation amplitude (Vp) for the crystal drive level. The minimum amplitude detector output is readable in CLK_ECO_STATUS.ECO_OK.<br>0x0: Vp > 0.05V<br>0x1: Vp > 0.10V<br>0x2: Vp > 0.15V<br>0x3: Vp > 0.20V<br>0x4: Vp > 0.25V<br>0x5: Vp > 0.30V<br>0x6: Vp > 0.35V<br>0x7: Vp > 0.40V |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 4:7 | ATRIM | RW | R | 0 | Amplitude trim. Sets maximum oscillation amplitude (Vp) to set the crystal drive level when ECO_CONFIG.AGC_EN=1. When AGC_EN=0, most values of this register are unused, except as noted. WARNING: use care when setting this field because driving a crystal beyond its rated limit can permanently damage the crystal.<br>0x0: Vp < 0.35V<br>0x1: Vp < 0.40V<br>0x2: Vp < 0.45V<br>0x3: Vp < 0.50V<br>0x4: Vp < 0.55V<br>0x5: Vp < 0.60V<br>0x6: Vp < 0.65V<br>0x7: Vp < 0.70V<br>0x8: Vp < 0.75V<br>0x9: Vp < 0.80V<br>0xA: Vp < 0.85V<br>0xB: Vp < 0.90V<br>0xC: Vp < 0.95V<br>0xD: Vp < 1.00V<br>0xE: Vp < 1.05V<br>0xF: Vp < 1.10V when AGC_EN=1. When AGC_EN=0, this setting enables maximum swing between vddd and vssd. |
| 8:9 | FTRIM | RW | R | 0 | Filter Trim - 3rd harmonic oscillation |
| 10:11 | RTRIM | RW | R | 0 | Feedback resistor Trim |
| 12:14 | GTRIM | RW | R | 0 | Gain Trim - Startup time. |

### 31.11.39 CLK_PLL_CONFIG

**Description:** PLL Configuration Register
**Address:** 0x40261600
**Offset:** 0x1600
**Retention:** Retained
**IsDeepSleep:** Yes
**Comment:** This register contains PLL configuration. There is a copy of this register for each PLL. PLL circuit settings should not be changed while it is a selected clock (connected to logic). This prevents clock glitches that can crash the logic.
**Default:** 0x20116

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:7] | FEEDBACK_DIV [6:0] | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:13] | | | REFERENCE_DIV [12:8] | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:21] | | | OUTPUT_DIV [20:16] | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | ENABLE [31:31] | None [30:30] | BYPASS_SEL [29:28] | | PLL_LF_MODE [27:27] | LOCK_DELAY [26:25] | | None [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:6 | FEEDBACK_DIV | RW | R | 22 | Control bits for feedback divider. Set the divide value before enabling the PLL, and do not change it while PLL is enabled.<br>0-21: illegal (undefined behavior)<br>22: divide by 22<br>...<br>112: divide by 112<br>>112: illegal (undefined behavior) |
| 8:12 | REFERENCE_DIV | RW | R | 1 | Control bits for reference divider. Set the divide value before enabling the PLL, and do not change it while PLL is enabled.<br>0: illegal (undefined behavior)<br>1: divide by 1<br>...<br>20: divide by 20<br>others: illegal (undefined behavior) |
| 16:20 | OUTPUT_DIV | RW | R | 2 | Control bits for Output divider. Set the divide value before enabling the PLL, and do not change it while PLL is enabled.<br>0: illegal (undefined behavior)<br>1: illegal (undefined behavior)<br>2: divide by 2. Suitable for direct usage as HFCLK source.<br>...<br>16: divide by 16. Suitable for direct usage as HFCLK source.<br>>16: illegal (undefined behavior) |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 25:26 | LOCK_DELAY | RW | R | 0 | Configures the sensitivity of the lock detection logic.<br>0: normal operation<br>1: reduced sensitivity to allow tracking a modulating reference clock. When this option is selected, configure fVCO=320MHz. The PLL can track the a reference clock frequency that modulates within +/-4 percent at a rate of fREF/1000 MHz.<br>2,3: reserved (do not use) |
| 27 | PLL_LF_MODE | RW | R | 0 | VCO frequency range selection. Configure this bit according to the targeted VCO frequency. Do not change this setting while the PLL is enabled.<br>0: VCO frequency is [200MHz, 400MHz]<br>1: VCO frequency is [170MHz, 200MHz) |
| 28:29 | BYPASS_SEL | RW | R | 0 | Bypass mux located just after PLL output. This selection is glitch-free and can be changed while the PLL is running. When changing BYPASS_SEL, do not turn off the reference clock or PLL clock for five cycles (whichever is slower). |
| | AUTO | | | 0 | Automatic using lock indicator. When unlocked, automatically selects PLL reference input (bypass mode). When locked, automatically selects PLL output. If ENABLE=0, automatically selects PLL reference input. |
| | LOCKED_OR_NOTHING | | | 1 | Similar to AUTO, except the clock is gated off when unlocked. This is compatible with clock supervision, because the supervisors allow no clock during startup (until a timeout occurs), and the clock targets the proper frequency whenever it is running. If ENABLE=0, no clock is output. |
| | PLL_REF | | | 2 | Select PLL reference input (bypass mode). Ignores lock indicator |
| | PLL_OUT | | | 3 | Select PLL output. Ignores lock indicator. If ENABLE=0, no clock is output. |
| 31 | ENABLE | RW | R | 0 | Master enable for PLL. Setup FEEDBACK_DIV, REFERENCE_DIV, and OUTPUT_DIV at least one cycle before setting ENABLE=1.<br><br>Fpll = (FEEDBACK_DIV) * (Fref / REFERENCE_DIV) / (OUTPUT_DIV)<br><br>0: Block is disabled. When the PLL disables, hardware controls the bypass mux as described in BYPASS_SEL, before disabling the PLL circuit.<br>1: Block is enabled |

### 31.11.40 CLK_PLL_STATUS

**Description:** PLL Status Register
**Address:** 0x40261640
**Offset:** 0x1640
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register indicates status for the PLL. There is a copy of this register for each PLL. This register is synchronized during an AHB read transaction. This causes a number wait-states to be inserted in the transaction depending on the frequency ration between system and PLL frequency.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:2] | | | | | | UNLOCK_OCCURRED [1:1] | LOCKED [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | LOCKED | R | W | 0 | PLL Lock Indicator |
| 1 | UNLOCK_OCCURRED | RW1C | A | 0 | This bit sets whenever the PLL Lock bit goes low, and stays set until cleared by firmware. |

### 31.11.41 CSV_REF_SEL

**Description:** Select CSV Reference clock for Active domain
**Address:** 0x40261700
**Offset:** 0x1700
**Retention:** Retained
**IsDeepSleep:** Yes
**Comment:** Selects a source to be used as the Reference clock for CSV in the Active domain. (matching CLK_PATH_SELECT.PATH_MUX)
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:3] | | | | | REF_MUX [2:0] | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:2 | REF_MUX | RW | R | 0 | Selects a source for clock clk_ref_hf. Note that not all products support all clock sources. Selecting a clock source that is not supported will result in undefined behavior. It takes four cycles of the originally selected clock to switch away from it. Do not disable the original clock during this time. |
| | IMO | | | 0 | IMO - Internal R/C Oscillator |
| | EXTCLK | | | 1 | EXTCLK - External Clock Pin |
| | ECO | | | 2 | ECO - External-Crystal Oscillator |
| | ALTHF | | | 3 | ALTHF - Alternate High-Frequency clock input (product-specific clock) |

### 31.11.42 RES_CAUSE

**Description:** Reset Cause Observation Register
**Address:** 0x40261800
**Offset:** 0x1800
**Retention:** Retained
**IsDeepSleep:** Yes
**Comment:** Indicates the cause for reset(s) that occurred in the system. All bits in this register assert when the corresponding reset cause occurs and must be cleared by firmware. Low-voltage cause bits are reset whenever the low-voltage supply is initialized, including XRES, POR, brown-out, and during Hibernate wakeup. HT products also clear low-voltage cause bits for over-voltage, over-current, and WDT resets. Refer to the reset source documentation to understand what reset source behavior for different configuration or modes.
**Default:** 0x40000000

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | RESET_MCWDT2 [7:7] | RESET_MCWDT1 [6:6] | RESET_MCWDT0 [5:5] | RESET_SOFT [4:4] | RESET_TC_DBGRESET [3:3] | RESET_DPSLP_FAULT [2:2] | RESET_ACT_FAULT [1:1] | RESET_WDT [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:9] | | | | | | | RESET_MCWDT3 [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | RESET_OCD_ACT_LINREG [23:23] | RESET_OVD_VCCD [22:22] | RESET_OVD_VDDA [21:21] | RESET_OVD_VDDD [20:20] | RESET_BOD_VCCD [19:19] | RESET_BOD_VDDA [18:18] | RESET_BOD_VDDD [17:17] | RESET_XRES [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:31] | RESET_POR_VDDD [30:30] | RESET_STRUCT_XRES [29:29] | RESET_PXRES [28:28] | None [27:27] | RESET_PMIC [26:26] | RESET_OCD_REGHC [25:25] | RESET_OCD_DPSLP_LINREG [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | RESET_WDT | RW1C | A | 0 | A basic WatchDog Timer (WDT) reset has occurred since last power cycle. ULP products: This is a low-voltage cause bit that hardware clears when the low-voltage supply is initialized (see comments above).<br><br>For products that support high-voltage cause detection, this bit blocks recording of other high-voltage cause bits, except RESET_PORVDDD. Hardware clears this bit during POR. This bit is not blocked by other HV cause bits. |
| 1 | RESET_ACT_FAULT | RW1C | A | 0 | Fault logging system requested a reset from its Active logic. This is a low-voltage cause bit that hardware clears when the low-voltage supply is initialized (see comments above). |
| 2 | RESET_DPSLP_FAULT | RW1C | A | 0 | Fault logging system requested a reset from its DeepSleep logic. This is a low-voltage cause bit that hardware clears when the low-voltage supply is initialized (see comments above). |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 3 | RESET_TC_DBGRESET | RW1C | A | 0 | Test controller or debugger asserted reset. Only resets debug domain. This is a low-voltage cause bit that hardware clears when the low-voltage supply is initialized (see comments above). |
| 4 | RESET_SOFT | RW1C | A | 0 | A CPU requested a system reset through it's SYSRESETREQ. This can be done via a debugger probe or in firmware. This is a low-voltage cause bit that hardware clears when the low-voltage supply is initialized (see comments above). |
| 5 | RESET_MCWDT0 | RW1C | A | 0 | Multi-Counter Watchdog timer reset #0. This is a low-voltage cause bit that hardware clears when the low-voltage supply is initialized (see comments above). |
| 6 | RESET_MCWDT1 | RW1C | A | 0 | Multi-Counter Watchdog timer reset #1. This is a low-voltage cause bit that hardware clears when the low-voltage supply is initialized (see comments above). |
| 7 | RESET_MCWDT2 | RW1C | A | 0 | Multi-Counter Watchdog timer reset #2. This is a low-voltage cause bit that hardware clears when the low-voltage supply is initialized (see comments above). |
| 8 | RESET_MCWDT3 | RW1C | A | 0 | Multi-Counter Watchdog timer reset #3. This is a low-voltage cause bit that hardware clears when the low-voltage supply is initialized (see comments above). |
| 16 | RESET_XRES | RW1C | A | 0 | External XRES pin was asserted. This is a high-voltage cause bit that blocks recording of other high-voltage cause bits, except RESET_PORVDDD. Hardware clears this bit during POR. This bit is not blocked by other HV cause bits. |
| 17 | RESET_BODVDDD | RW1C | A | 0 | External VDDD supply crossed brown-out limit. Note that this cause will only be observable as long as the VDDD supply does not go below the POR (power on reset) detection limit. Below this limit it is not possible to reliably retain information in the device. This is a high-voltage cause bit that blocks recording of other high-voltage cause bits, except RESET_PORVDDD. Hardware clears this bit during POR. |
| 18 | RESET_BODVDDA | RW1C | A | 0 | External VDDA supply crossed the brown-out limit. This is a high-voltage cause bit that blocks recording of other high-voltage cause bits, except RESET_PORVDDD. Hardware clears this bit during POR. |
| 19 | RESET_BODVCCD | RW1C | A | 0 | Internal VCCD core supply crossed the brown-out limit. Note that this detector will detect gross issues with the internal core supply, but may not catch all brown-out conditions. Functional and timing supervision (CSV, WDT) is provided to create fully failsafe internal crash detection. This is a high-voltage cause bit that blocks recording of other high-voltage cause bits, except RESET_PORVDDD. Hardware clears this bit during POR. |
| 20 | RESET_OVDVDDD | RW1C | A | 0 | Overvoltage detection on the external VDDD supply. This is a high-voltage cause bit that blocks recording of other high-voltage cause bits, except RESET_PORVDDD. Hardware clears this bit during POR. |
| 21 | RESET_OVDVDDA | RW1C | A | 0 | Overvoltage detection on the external VDDA supply. This is a high-voltage cause bit that blocks recording of other high-voltage cause bits, except RESET_PORVDDD. Hardware clears this bit during POR. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 22 | RESET_OVDVCCD | RW1C | A | 0 | Overvoltage detection on the internal core VCCD supply. This is a high-voltage cause bit that blocks recording of other high-voltage cause bits, except RESET_PORVDDD. Hardware clears this bit during POR. |
| 23 | RESET_OCD_ACT _LINREG | RW1C | A | 0 | Overcurrent detection on the internal VCCD supply when supplied by the ACTIVE power mode linear regulator. This is a high-voltage cause bit that blocks recording of other high-voltage cause bits, except RESET_PORVDDD. Hardware clears this bit during POR. |
| 24 | RESET_OCD_DPSLP _LINREG | RW1C | A | 0 | Overcurrent detection on the internal VCCD supply when supplied by the DEEPSLEEP power mode linear regulator. This is a high-voltage cause bit that blocks recording of other high-voltage cause bits, except RESET_PORVDDD. Hardware clears this bit during POR. |
| 25 | RESET_OCD_REGHC | RW1C | A | 0 | Overcurrent detection from REGHC (if present). If REGHC is not present, hardware will never set this bit. This is a high-voltage cause bit that blocks recording of other high-voltage cause bits, except RESET_PORVDDD. Hardware clears this bit during POR. |
| 26 | RESET_PMIC | RW1C | A | 0 | PMIC status triggered a reset. If PMIC control is not present, hardware will never set this bit. This is a high-voltage cause bit that blocks recording of other high-voltage cause bits, except RESET_PORVDDD. Hardware clears this bit during POR. |
| 28 | RESET_PXRES | RW1C | A | 0 | PXRES triggered. This is a high-voltage cause bit that blocks recording of other high-voltage cause bits, except RESET_PORVDDD. Hardware clears this bit during POR. This bit is not blocked by other HV cause bits. |
| 29 | RESET_STRUCT_XRES | RW1C | A | 0 | Structural reset was asserted. This is a high-voltage cause bit that blocks recording of other high-voltage cause bits, except RESET_PORVDDD. Hardware clears this bit during POR. This bit is not blocked by other HV cause bits. |
| 30 | RESET_PORVDDD | RW1C | A | 1 | Indicator that a POR occurred. This is a high-voltage cause bit, and hardware clears the other bits when this one is set. It does not block further recording of other high-voltage causes. |

### 31.11.43 RES_CAUSE2

**Description:** Reset Cause Observation Register 2
**Address:** 0x40261804
**Offset:** 0x1804
**Retention:** Retained
**IsDeepSleep:** Yes
**Comment:** Indicates the cause for the latest reset(s) that occurred in the system. Note that resets due to power up and brown-outs below state retention voltages in regulated and unregulated domains cannot be distinguished from each other. All bits in this register assert when the corresponding reset cause occurs and must be cleared by firmware. These bits are cleared by hardware only during XRES, POR or after a detected brown-out.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | RESET_CSV_HF [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | RESET_CSV_HF [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:17] | | | | | | | RESET_CSV_REF [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | RESET_CSV_HF | RW1C | A | 0 | Clock supervision logic requested a reset due to loss or frequency violation of a high-frequency clock. Each bit index K corresponds to a HFCLK<K>. Unimplemented clock bits return zero. |
| 16 | RESET_CSV_REF | RW1C | A | 0 | Clock supervision logic requested a reset due to loss or frequency violation of the reference clock source that is used to monitor the other HF clock sources. |

### 31.11.44 CLK_TRIM_ILO0_CTL

**Description:** ILO0 Trim Register
**Address:** 0x40263014
**Offset:** 0x3014
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Trims ILO frequency. Determined during manufacturing sort/class, but may be updated in the field to calibrate voltage and temperature conditions. This register is protected by WDT_CTL.WDT_LOCK. ILO0 configuration and trims are reset by XRES and power-related resets, unless configured otherwise.
**Default:** 0x52C

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:6] | | ILO0_FTRIM [5:0] | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:12] | | | | ILO0_MONTRIM [11:8] | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:5 | ILO0_FTRIM | RW | A | 44 | ILO0 frequency trims. LSB step size is 1.5 percent (typical) of the frequency. |
| 8:11 | ILO0_MONTRIM | RW | A | 5 | ILO0 internal monitor trim. |

### 31.11.45 CLK_TRIM_ILO1_CTL

**Description:** ILO1 Trim Register
**Address:** 0x40263220
**Offset:** 0x3220
**Retention:** Retained
**IsDeepSleep:** Yes
**Comment:** Trims ILO frequency. Determined during manufacturing sort/class, but may be updated in the field to calibrate voltage and temperature conditions.
**Default:** 0x52C

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:6] | | ILO1_FTRIM [5:0] | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:12] | | | | ILO1_MONTRIM [11:8] | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:5 | ILO1_FTRIM | RW | R | 44 | ILO1 frequency trims. LSB step size is 1.5 percent (typical) of the frequency. |
| 8:11 | ILO1_MONTRIM | RW | R | 5 | ILO1 internal monitor trim. |

### 31.11.46 CSV_HF

### 31.11.46.1 CSV

#### 31.11.46.1.1 CSV_HF_CSV_REF_CTL

**Description:** Clock Supervision Reference Control
**Address:** 0x40261400
**Offset:** 0x0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Controls clock supervision for a clock tree.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | STARTUP [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | STARTUP [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | CSV_EN [31:31] | CSV _ACTION [30:30] | None [29:24] | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | STARTUP | RW | R | 0 | Startup delay time -1 (in reference clock cycles), after enable or DeepSleep wakeup, from reference clock start to monitored clock start.<br>At a minimum (both clocks running): STARTUP >= (PERIOD +3) * FREQ_RATIO - UPPER, with FREQ_RATIO = (Reference frequency / Monitored frequency)<br>On top of that the actual clock startup delay and the margin for accuracy of both clocks must be added. |
| 30 | CSV_ACTION | RW | R | 0 | Specifies the action taken when an anomaly is detected on the monitored clock. CSV in DeepSleep domain always do a Fault report (which also wakes up the system). |
| | FAULT | | | 0 | Do a Fault report. |
| | RESET | | | 1 | Cause a power reset. This should only be used for clk_hf0. |
| 31 | CSV_EN | RW | R | 0 | Enables clock supervision, both frequency and loss. CSV in Active domain: Clock supervision is reset during DeepSleep and Hibernate modes. When enabled it begins operating automatically after a DeepSleep wakeup, but it must be reconfigured after Hibernate wakeup.<br>CSV in DeepSleep domain: Clock supervision is reset during Hibernate mode. It must be reconfigured after Hibernate wakeup.<br><br>A CSV error detection is reported to the Fault structure, or instead it can generate a power reset. |

### 31.11.46.1.2 CSV_HF_CSV_REF_LIMIT

**Description:** Clock Supervision Reference Limits
**Address:** 0x40261404
**Offset:** 0x4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | LOWER [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | LOWER [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | UPPER [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | UPPER [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | LOWER | RW | R | 0 | Cycle time lower limit. Set the lower limit -1, in reference clock cycles, before the next monitored clock event is allowed to happen. If a monitored clock event happens before this limit is reached a CSV error is detected.<br>LOWER must be at least 1 less than UPPER. In case the clocks are asynchronous LOWER must be at least 3 less than UPPER. |
| 16:31 | UPPER | RW | R | 0 | Cycle time upper limit. Set the upper limit -1, in reference clock cycles, before (or same time) the next monitored clock event must happen. If a monitored clock event does not happen before this limit is reached, or does not happen at all (clock loss), a CSV error is detected. |

### 31.11.46.1.3 CSV_HF_CSV_MON_CTL

**Description:** Clock Supervision Monitor Control
**Address:** 0x40261408
**Offset:** 0x8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | PERIOD [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | PERIOD [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | PERIOD | RW | R | 0 | Period time. Set the Period -1, in monitored clock cycles, before the next monitored clock event happens.<br>PERIOD <= (UPPER+1) / FREQ_RATIO -1, with FREQ_RATIO = (Reference frequency / Monitored frequency)<br>In case the clocks are asynchronous: PERIOD <= UPPER / FREQ_RATIO -1<br>Additionally margin must be added for accuracy of both clocks. |

### 31.11.47 CSV_REF

#### 31.11.47.1 CSV

#### 31.11.47.1.1 CSV_REF_CSV_REF_CTL

**Description:** Clock Supervision Reference Control
**Address:** 0x40261710
**Offset:** 0x0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Controls clock supervision for a clock tree.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | STARTUP [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | STARTUP [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | CSV_EN [31:31] | CSV _ACTION [30:30] | None [29:24] | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | STARTUP | RW | R | 0 | Startup delay time -1 (in reference clock cycles), after enable or DeepSleep wakeup, from reference clock start to monitored clock start.<br>At a minimum (both clocks running): STARTUP >= (PERIOD +3) * FREQ_RATIO - UPPER, with FREQ_RATIO = (Reference frequency / Monitored frequency)<br>On top of that the actual clock startup delay and the margin for accuracy of both clocks must be added. |
| 30 | CSV_ACTION | RW | R | 0 | Specifies the action taken when an anomaly is detected on the monitored clock. CSV in DeepSleep domain always do a Fault report (which also wakes up the system). |
| | FAULT | | | 0 | Do a Fault report. |
| | RESET | | | 1 | Cause a power reset. This should only be used for clk_hf0. |
| 31 | CSV_EN | RW | R | 0 | Enables clock supervision, both frequency and loss. CSV in Active domain: Clock supervision is reset during DeepSleep and Hibernate modes. When enabled it begins operating automatically after a DeepSleep wakeup, but it must be reconfigured after Hibernate wakeup.<br>CSV in DeepSleep domain: Clock supervision is reset during Hibernate mode. It must be reconfigured after Hibernate wakeup.<br><br>A CSV error detection is reported to the Fault structure, or instead it can generate a power reset. |

### 31.11.47.1.2 CSV_REF_CSV_REF_LIMIT

**Description:** Clock Supervision Reference Limits
**Address:** 0x40261714
**Offset:** 0x4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | LOWER [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | LOWER [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | UPPER [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | UPPER [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | LOWER | RW | R | 0 | Cycle time lower limit. Set the lower limit -1, in reference clock cycles, before the next monitored clock event is allowed to happen. If a monitored clock event happens before this limit is reached a CSV error is detected.<br>LOWER must be at least 1 less than UPPER. In case the clocks are asynchronous LOWER must be at least 3 less than UPPER. |
| 16:31 | UPPER | RW | R | 0 | Cycle time upper limit. Set the upper limit -1, in reference clock cycles, before (or same time) the next monitored clock event must happen. If a monitored clock event does not happen before this limit is reached, or does not happen at all (clock loss), a CSV error is detected. |

### 31.11.47.1.3 CSV_REF_CSV_MON_CTL

**Description:** Clock Supervision Monitor Control
**Address:** 0x40261718
**Offset:** 0x8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | PERIOD [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | PERIOD [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | PERIOD | RW | R | 0 | Period time. Set the Period -1, in monitored clock cycles, before the next monitored clock event happens.<br>PERIOD <= (UPPER+1) / FREQ_RATIO -1, with FREQ_RATIO = (Reference frequency / Monitored frequency)<br>In case the clocks are asynchronous: PERIOD <= UPPER / FREQ_RATIO -1<br>Additionally margin must be added for accuracy of both clocks. |

### 31.11.48 CSV_LF

### 31.11.48.1 CSV

#### 31.11.48.1.1 CSV_LF_CSV_REF_CTL

**Description:** Clock Supervision Reference Control
**Address:** 0x40261720
**Offset:** 0x0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Controls clock supervision for a clock tree.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | STARTUP [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | CSV_EN [31:31] | None [30:24] | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | STARTUP | RW | R | 0 | Startup delay time -1 (in reference clock cycles), after enable, from reference clock start to monitored clock start.<br>At a minimum (both clocks running): STARTUP >= (PERIOD +3) * FREQ_RATIO - UPPER, with FREQ_RATIO = (Reference frequency / Monitored frequency)<br>On top of that the actual clock startup delay and the margin for accuracy of both clocks must be added. |
| 31 | CSV_EN | RW | R | 0 | Enables clock supervision, both frequency and loss.<br>CSV in Active domain: Clock supervision is reset during DeepSleep and Hibernate modes. When enabled it begins operating automatically after a DeepSleep wakeup, but it must be reconfigured after Hibernate wakeup.<br>CSV in DeepSleep domain: Clock supervision is reset during Hibernate mode. It must be reconfigured after Hibernate wakeup.<br>CSV in Backup domain: Clock supervision operates during Hibernate mode, can be configured to wake from Hibernate, and continues operating during reboot.<br><br>A CSV error detection is reported to the Fault structure. |

### 31.11.48.1.2 CSV_LF_CSV_REF_LIMIT

**Description:** Clock Supervision Reference Limits
**Address:** 0x40261724
**Offset:** 0x4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | LOWER [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | UPPER [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | LOWER | RW | R | 0 | Cycle time lower limit. Set the lower limit -1, in reference clock cycles, before the next monitored clock event is allowed to happen. If a monitored clock event happens before this limit is reached a CSV error is detected.<br>LOWER must be at least 1 less than UPPER. In case the clocks are asynchronous LOWER must be at least 3 less than UPPER. |
| 16:23 | UPPER | RW | R | 0 | Cycle time upper limit. Set the upper limit -1, in reference clock cycles, before (or same time) the next monitored clock event must happen. If a monitored clock event does not happen before this limit is reached, or does not happen at all (clock loss), a CSV error is detected. |

### 31.11.48.1.3 CSV_LF_CSV_MON_CTL

**Description:** Clock Supervision Monitor Control
**Address:** 0x40261728
**Offset:** 0x8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | PERIOD [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | PERIOD | RW | R | 0 | Period time. Set the Period -1, in monitored clock cycles, before the next monitored clock event happens.<br>PERIOD <= (UPPER+1) / FREQ_RATIO -1, with FREQ_RATIO = (Reference frequency / Monitored frequency)<br>In case the clocks are asynchronous: PERIOD <= UPPER / FREQ_RATIO -1<br>Additionally margin must be added for accuracy of both clocks. |

### 31.11.49 CSV_ILO

### 31.11.49.1 CSV

#### 31.11.49.1.1 CSV_ILO_CSV_REF_CTL

**Description:** Clock Supervision Reference Control
**Address:** 0x40261730
**Offset:** 0x0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Controls clock supervision for a clock tree.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | STARTUP [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | CSV_EN [31:31] | None [30:24] | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | STARTUP | RW | R | 0 | Startup delay time -1 (in reference clock cycles), after enable, from reference clock start to monitored clock start.<br>At a minimum (both clocks running): STARTUP >= (PERIOD +3) * FREQ_RATIO - UPPER, with FREQ_RATIO = (Reference frequency / Monitored frequency)<br>On top of that the actual clock startup delay and the margin for accuracy of both clocks must be added. |
| 31 | CSV_EN | RW | R | 0 | Enables clock supervision, both frequency and loss.<br>CSV in Active domain: Clock supervision is reset during DeepSleep and Hibernate modes. When enabled it begins operating automatically after a DeepSleep wakeup, but it must be reconfigured after Hibernate wakeup.<br>CSV in DeepSleep domain: Clock supervision is reset during Hibernate mode. It must be reconfigured after Hibernate wakeup.<br>CSV in Backup domain: Clock supervision operates during Hibernate mode, can be configured to wake from Hibernate, and continues operating during reboot.<br><br>A CSV error detection is reported to the Fault structure. |

### 31.11.49.1.2 CSV_ILO_CSV_REF_LIMIT

**Description:** Clock Supervision Reference Limits
**Address:** 0x40261734
**Offset:** 0x4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | LOWER [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | UPPER [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | LOWER | RW | R | 0 | Cycle time lower limit. Set the lower limit -1, in reference clock cycles, before the next monitored clock event is allowed to happen. If a monitored clock event happens before this limit is reached a CSV error is detected.<br>LOWER must be at least 1 less than UPPER. In case the clocks are asynchronous LOWER must be at least 3 less than UPPER. |
| 16:23 | UPPER | RW | R | 0 | Cycle time upper limit. Set the upper limit -1, in reference clock cycles, before (or same time) the next monitored clock event must happen. If a monitored clock event does not happen before this limit is reached, or does not happen at all (clock loss), a CSV error is detected. |

### 31.11.49.1.3 CSV_ILO_CSV_MON_CTL

**Description:** Clock Supervision Monitor Control
**Address:** 0x40261738
**Offset:** 0x8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | PERIOD [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | PERIOD | RW | R | 0 | Period time. Set the Period -1, in monitored clock cycles, before the next monitored clock event happens.<br>PERIOD <= (UPPER+1) / FREQ_RATIO -1, with FREQ_RATIO = (Reference frequency / Monitored frequency)<br>In case the clocks are asynchronous: PERIOD <= UPPER / FREQ_RATIO -1<br>Additionally margin must be added for accuracy of both clocks. |

### 31.11.50 CLK_PLL400M

#### 31.11.50.1 CLK_PLL400M_CONFIG

**Description:** 400MHz PLL Configuration Register
**Address:** 0x40261900
**Offset:** 0x0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register contains PLL configuration for 400MHz PLL. There is a copy of this register for each 400MHz PLL. Configuration settings should not be changed while it is a selected clock (connected to logic). This prevents clock glitches that can crash the logic.
**Default:** 0x20116

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | FEEDBACK_DIV [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:13] | | | REFERENCE_DIV [12:8] | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:21] | | | OUTPUT_DIV [20:16] | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | ENABLE [31:31] | None [30:30] | BYPASS_SEL [29:28] | | None [27:27] | LOCK_DELAY [26:25] | | None [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | FEEDBACK_DIV | RW | R | 22 | Control bits for feedback divider. Set the divide value before enabling the PLL, and do not change it while PLL is enabled.<br>0-15: illegal (undefined behavior)<br>16: divide by 16<br>...<br>200: divide by 200<br>>200: illegal (undefined behavior)<br><br>When using fractional mode, the jitter specs are met over the restricted range of 27 to 47, inclusive. |
| 8:12 | REFERENCE_DIV | RW | R | 1 | Control bits for reference divider. Set the divide value before enabling the PLL, and do not change it while PLL is enabled.<br>0: illegal (undefined behavior)<br>1: divide by 1<br>...<br>16: divide by 16<br>others: illegal (undefined behavior)<br><br>When using fractional mode, the jitter specs are met over the restricted range of 1 to 4, inclusive. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 16:20 | OUTPUT_DIV | RW | R | 2 | Control bits for Output divider. Set the divide value before enabling the PLL, and do not change it while PLL is enabled.<br>0: illegal (undefined behavior)<br>1: illegal (undefined behavior)<br>2: divide by 2. Suitable for direct usage as HFCLK source.<br>...<br>16: divide by 16. Suitable for direct usage as HFCLK source.<br>>16: illegal (undefined behavior) |
| 25:26 | LOCK_DELAY | RW | R | 0 | Configures the sensitivity of the lock detection logic, according to the intended operating mode:<br>0: Integer divider without spreading;<br>1: Fractional division or spreading.<br>2,3: reserved (do not use) |
| 28:29 | BYPASS_SEL | RW | R | 0 | Bypass mux located just after PLL output. This selection is glitch-free and can be changed while the PLL is running. When changing BYPASS_SEL, do not turn off the reference clock or PLL clock for five cycles (whichever is slower). |
| | AUTO | | | 0 | Automatic using lock indicator. When unlocked, automatically selects PLL reference input (bypass mode). When locked, automatically selects PLL output. If ENABLE=0, automatically selects PLL reference input. |
| | LOCKED_OR_NOTHING | | | 1 | Similar to AUTO, except the clock is gated off when unlocked. This is compatible with clock supervision, because the supervisors allow no clock during startup (until a timeout occurs), and the clock targets the proper frequency whenever it is running. If ENABLE=0, no clock is output. |
| | PLL_REF | | | 2 | Select PLL reference input (bypass mode). Ignores lock indicator |
| | PLL_OUT | | | 3 | Select PLL output. Ignores lock indicator. If ENABLE=0, no clock is output. |
| 31 | ENABLE | RW | R | 0 | Master enable for PLL. Setup FEEDBACK_DIV, REFERENCE_DIV, and OUTPUT_DIV at least one cycle before setting ENABLE=1.<br><br>fOUT = (FEEDBACK_DIV + FRAC_EN*FRAC_DIV/2^24) * (fREF / REFERENCE_DIV) / (OUTPUT_DIV)<br><br>0: Block is disabled. When the PLL disables, hardware controls the bypass mux as described in BYPASS_SEL, before disabling the PLL circuit.<br>1: Block is enabled |

### 31.11.50.2 CLK_PLL400M_CONFIG2

**Description:** 400MHz PLL Configuration Register 2
**Address:** 0x40261904
**Offset:** 0x4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register contains additional PLL configuration for 400MHz fractional PLLs. There is a copy of this register for each 400MHz PLL. Configure this register before enabling the PLL, and do not change any settings (except FRAC_DIV) while PLL ENABLE==1.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | FRAC_DIV [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | FRAC_DIV [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | FRAC_DIV [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | FRAC_EN [31:31] | FRAC_DITHER_EN [30:28] | | | None [27:24] | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:23 | FRAC_DIV | RW | A | 0 | Control bits for fractional divider. This value is interpreted as a fraction of the PFD frequency, i.e. fPFD * (FRAC_DIV/2^24). This field can be dynamically updated within the 1000ppm control limit. It takes up to 115 AHB cycles to transfer the setting to the PLL, and writes that occur faster may be silently ignored and require the application to write again after the previous update has finished. Reading the register returns the accepted value. The PLL will start targeting the new value, but it may take significant time (milliseconds) to stabilize at the new average value. Do not change the FRAC_DIV setting while the PLL is initially locking. |
| 28:30 | FRAC_DITHER_EN | RW | R | 0 | Enables dithering during fractional operation.<br>3'b000: disables dithering;<br>3'b001: enables dithering;<br>others: reserved |
| 31 | FRAC_EN | RW | R | 0 | Enables fractional division mode. When using fractional division mode, see CLK_PLL400M_CONFIG.LOCK_DELAY for an additional configuration requirement. |

### 31.11.50.3 CLK_PLL400M_CONFIG3

**Description:** 400MHz PLL Configuration Register 3
**Address:** 0x40261908
**Offset:** 0x8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register contains additional PLL configuration for 400MHz fractional PLLs. There is a copy of this register for each 400MHz PLL. There is a copy of this register for each 400MHz PLL. Configure this register before enabling the PLL, and do not change any settings while PLL ENABLE==1.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | SSCG_DEPTH [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:10] | | | | | | SSCG_DEPTH [9:8] | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:19] | | | | | SSCG_RATE [18:16] | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | SSCG_EN [31:31] | None [30:29] | | SSCG_MODE [28:28] | None [27:25] | | | SSCG_DITHER_EN [24:24] |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:9 | SSCG_DEPTH | RW | R | 0 | Control bits for SSCG modulation depth as a percentage of the non-modulated clock. The following choices are supported, and all others are reserved:<br>10'h029: -0.5 percent (down-spread),<br>10'h052: -1 percent (down-spread),<br>10'h0a4: -2 percent (down-spread),<br>10'h0f6: -3 percent (down-spread) |
| 16:18 | SSCG_RATE | RW | R | 0 | Control bits for SSCG modulation rate as a factor of fPFD clock frequency. Audio applications should choose a setting that results in a modulation rate that is greater than 20kHz, so fPFD/512 or fPFD/256 is recommended.<br>0: Modulation rate = fPFD/4096,<br>1: Modulation rate = fPFD/2048,<br>2: Modulation rate = fPFD/1024,<br>3: Modulation rate = fPFD/512,<br>4: Modulation rate = fPFD/256 (limited to 8MHz only), others: reserved |
| 24 | SSCG_DITHER_EN | RW | R | 0 | Reserved. Setting is not used internally. |
| 28 | SSCG_MODE | RW | R | 0 | Reserved. Write zero always. |
| 31 | SSCG_EN | RW | R | 0 | Enables spreading mode. When using spreading, see CLK_PLL400M_CONFIG.LOCK_DELAY for an additional configuration requirement. |

### 31.11.50.4 CLK_PLL400M_STATUS

**Description:** 400MHz PLL Status Register
**Address:** 0x4026190C
**Offset:** 0xC
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** This register indicates status for a PLL400M. There is a copy of this register for each PLL400M. This register is synchronized during an AHB read transaction. This causes a number wait-states to be inserted in the transaction depending on the frequency ration between system and PLL frequency.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:2] | | | | | | UNLOCK_OCCURRED [1:1] | LOCKED [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | LOCKED | R | W | 0 | PLL Lock Indicator |
| 1 | UNLOCK_OCCURRED | RW1C | A | 0 | This bit sets whenever the PLL Lock bit goes low, and stays set until cleared by firmware. |

## 31.11.51 MCWDT

### 31.11.51.1 MCWDT_CPU_SELECT

**Description:** MCWDT CPU selection register
**Address:** 0x40268040
**Offset:** 0x40
**Retention:** Retained
**IsDeepSleep:** Yes
**Comment:** Assigns this MCWDT to a CPU.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:2] | | | | | | CPU_SEL [1:0] | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:1 | CPU_SEL | RW | R | 0 | Assigns this MCWDT to a CPU. This selects which CPU SLEEPDEEP signal is used for SLEEPDEEP_PAUSE. |

### 31.11.51.2 MCWDT_CTR2_CTL

**Description:** MCWDT Subcounter 2 Control register
**Address:** 0x40268080
**Offset:** 0x80
**Retention:** Retained
**IsDeepSleep:** Yes
**Comment:** Control register for MCWDT subcounter 2. Writes are ignored when locked (i.e. corresponding LOCK.MCWDT_LOCK<>0). This register may be written while the counter is running, but new values may take up to 2 clk_lf cycles to take effect.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:1] | | | | | | | ENABLED [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | ENABLE [31:31] | None [30:24] | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | ENABLED | R | RW | 0 | Indicates actual state of this subcounter. May lag ENABLE by up to two clk_lf cycles. |
| 31 | ENABLE | RW | R | 0 | Enable subcounter. May take up to 2 clk_lf cycles to take effect. When ENABLE changes from 1->0, the counter is cleared.<br>0: Counter is disabled (not clocked)<br>1: Counter is enabled (counting up) |

### 31.11.51.3 MCWDT_CTR2_CONFIG

**Description:** MCWDT Subcounter 2 Configuration register
**Address:** 0x40268084
**Offset:** 0x84
**Retention:** Retained
**IsDeepSleep:** Yes
**Comment:** Configuration for MCWDT subcounter 2. Writes are ignored when locked (i.e. corresponding LOCK.MCWDT_LOCK<>0). This register may be written while the counter is running, but new values may take up to 2 clk_lf cycles to take effect. Before changing the limit, it is recommended to set the service bit for this subcounter and wait until it reads back low. This prevents possible unintended actions caused by synchronization delays.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:1] | | | | | | | ACTION [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:21] | | | BITS [20:16] | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | DEBUG_RUN [31:31] | SLEEPDEEP_PAUSE [30:30] | None [29:29] | DEBUG_TRIGGER_EN [28:28] | None [27:24] | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | ACTION | RW | R | 0 | Action taken when the specified BIT toggles.<br>Action will be triggered on the same edge where BITS to observe toggle. |
| | NOTHING | | | 0 | Do nothing |
| | INT | | | 1 | Trigger an interrupt |
| 16:20 | BITS | RW | R | 0 | Bit to observe for a toggle:<br>0: Do ACTION after CNT[0] toggles (i.e. every tick)<br>.<br>31: Do ACTION after CNT[31] toggles (i.e. every 2^31 ticks) |
| 28 | DEBUG_TRIGGER_EN | RW | R | 0 | Enables the trigger input for this MCWDT to pause the counter during debug mode. To pause at a breakpoint while debugging, configure the trigger matrix to connect the related CPU halted signal to the trigger input for this MCWDT, and then set this bit. It takes up to two clk_lf cycles for the trigger signal to be processed. Triggers that are less than two clk_lf cycles may be missed. Synchronization errors can accumulate each time it is halted.<br>0: Pauses the counter whenever a debug probe is connected.<br>1: Pauses the counter whenever a debug probe is connected and the trigger input is high. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 30 | SLEEPDEEP_PAUSE | RW | R | 0 | Pauses/runs this counter when the corresponding processor is in SLEEPDEEP. Note it may take up to two clk_lf cycles for the counter to pause and up to two clk_lf cycles for it to unpause, due to internal synchronization.<br>0: Counter runs normally regardless of processor mode.<br>1: Counter pauses when corresponding processor is in SLEEPDEEP. |
| 31 | DEBUG_RUN | RW | R | 0 | Pauses/runs this counter while a debugger is connected. Other behaviors are unchanged during debugging, including service, configuration updates and enable/disable. Note it may take up to two clk_lf cycles for the counter to pause and another two cycles to unpause, due to internal synchronization.<br>0: When debugger connected, counter pauses incrementing as configured in DEBUG_TRIGGER_EN.<br><br>1: When debugger connected, counter increments normally, but reset generation is blocked. |

### 31.11.51.4 MCWDT_CTR2_CNT

**Description:** MCWDT Subcounter 2 Count Register
**Address:** 0x40268088
**Offset:** 0x88
**Retention:** Retained
**IsDeepSleep:** Yes
**Comment:** Count value for this MCWDT subcounter 2. Writes are ignored when this subcounter is enabled or when it is locked (i.e. corresponding LOCK.MCWDT_LOCK<>0).
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | CNT2 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | CNT2 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | CNT2 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | CNT2 [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | CNT2 | RW | A | 0 | Current value of subcounter 2 for this MCWDT. This field may lag the actual count value by up to one clk_lf cycle, due to internal synchronization. When this subcounter is disabled and unlocked, the count value can be written for verification and debugging purposes. Software writes are always ignored when the subcounter is enabled. This register retains information during DeepSleep mode if SLEEPDEEP_PAUSE == 1. |

### 31.11.51.5 MCWDT_LOCK

**Description:** MCWDT Lock Register
**Address:** 0x40268090
**Offset:** 0x90
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Lock or unlock the respective configuration registers of subcounters 0/1/2 of this MCWDT.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:2] | | | | | | MCWDT_LOCK [1:0] | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:1 | MCWDT_LOCK | RW | A | 0 | Prohibits writing control and configuration registers related to this MCWDT when not equal 0 (as specified in the other register descriptions). Requires at least two different writes to unlock.<br>Note that this field is 2 bits to force multiple writes only. Each MCWDT has a separate local lock. |
| | NO_CHG | | | 0 | No effect |
| | CLR0 | | | 1 | Clears bit 0 |
| | CLR1 | | | 2 | Clears bit 1 |
| | SET01 | | | 3 | Sets both bits 0 and 1 |

### 31.11.51.6 MCWDT_SERVICE

**Description:** MCWDT Service Register
**Address:** 0x40268094
**Offset:** 0x94
**Retention:** Retained
**IsDeepSleep:** Yes
**Comment:** Control the behavior of the Watchdog counters. Writes to this register are ignored when LOCK.MCWDT_LOCK<>0. All fields in this register can be used while counter is in operation.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:2] | | | | | | CTR1 _SERVICE [1:1] | CTR0 _SERVICE [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | CTR0_SERVICE | RW1S | RW1C | 0 | Services subcounter 0. This resets the count value for subcounter 0 to zero. This may take up to three clk_lf cycles to take effect. Hardware clears this bit, after necessary synchronization. To ensure a pending CTR0_SERVICE write is reflected, firmware should wait until this bit reads low before attempting to write CTR0_SERVICE=1. If subcounter 0 is disabled, CTR0_SERVICE will not trigger a LOWER_ACTION and will not clear a preloaded count value. |
| 1 | CTR1_SERVICE | RW1S | RW1C | 0 | Services subcounter 1. This resets the count value for subcounter 1 to zero. This may take up to three clk_lf cycles to take effect. Hardware clears this bit, after necessary synchronization. To ensure a pending CTR1_SERVICE write is reflected, firmware should wait until this bit reads low before attempting to write CTR1_SERVICE=1. If subcounter 1 is disabled, CTR1_SERVICE will not trigger a LOWER_ACTION and will not clear a preloaded count value. |

### 31.11.51.7 MCWDT_INTR

**Description:** MCWDT Interrupt Register
**Address:** 0x402680A0
**Offset:** 0xA0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Interrupt status register for MCWDT subcounters.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:3] | | | | | CTR2_INT [2:2] | CTR1_INT [1:1] | CTR0_INT [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | CTR0_INT | RW1C | A | 0 | MCWDT Interrupt Request for sub-counter 0. This bit is set by hardware as configured by this registers. This bit must be cleared by firmware. |
| 1 | CTR1_INT | RW1C | A | 0 | MCWDT Interrupt Request for sub-counter 1. This bit is set by hardware as configured by this registers. This bit must be cleared by firmware. |
| 2 | CTR2_INT | RW1C | A | 0 | MCWDT Interrupt Request for sub-counter 2. This bit is set by hardware as configured by this registers. This bit must be cleared by firmware. |

### 31.11.51.8 MCWDT_INTR_SET

**Description:** MCWDT Interrupt Set Register
**Address:** 0x402680A4
**Offset:** 0xA4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register can be used to trigger an interrupt for firmware testing.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:3] | | | | | CTR2_INT [2:2] | CTR1_INT [1:1] | CTR0_INT [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | CTR0_INT | RW1S | A | 0 | Set interrupt for MCWDT_INT0 |
| 1 | CTR1_INT | RW1S | A | 0 | Set interrupt for MCWDT_INT1 |
| 2 | CTR2_INT | RW1S | A | 0 | Set interrupt for MCWDT_INT2 |

### 31.11.51.9 MCWDT_INTR_MASK

**Description:** MCWDT Interrupt Mask Register
**Address:** 0x402680A8
**Offset:** 0xA8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** This register controls whether a subcounter interrupt is forwarded to the corresponding processor. All masks block the interrupt when 0 and forward the interrupt when 1.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:3] | | | | | CTR2_INT [2:2] | CTR1_INT [1:1] | CTR0_INT [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | CTR0_INT | RW | R | 0 | Interrupt Mask for sub-counter 0 for warning interrupt. The bit controls if the interrupt is forwarded to the CPU. The interrupt is blocked when the value of the bit is 0. The interrupt is forwarded if the value of the bit is 1. |
| 1 | CTR1_INT | RW | R | 0 | Interrupt Mask for sub-counter 1 for warning interrupt. The bit controls if the interrupt is forwarded to the CPU. The interrupt is blocked when the value of the bit is 0. The interrupt is forwarded if the value of the bit is 1. |
| 2 | CTR2_INT | RW | R | 0 | Interrupt Mask for sub-counter 2. The bit controls if the interrupt is forwarded to the CPU. The interrupt is blocked when the value of the bit is 0. The interrupt is forwarded if the value of the bit is 1. |

### 31.11.51.10 MCWDT_INTR_MASKED

**Description:** MCWDT Interrupt Masked Register
**Address:** 0x402680AC
**Offset:** 0xAC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Bitwise AND between the interrupt request and mask registers so firmware can read the status of all mask enabled interrupt causes with a single load operation. Each available MCWDT has a copy of this register.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:3] | | | | | CTR2_INT [2:2] | CTR1_INT [1:1] | CTR0_INT [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | CTR0_INT | R | RW | 0 | Logical and of corresponding request and mask bits. |
| 1 | CTR1_INT | R | RW | 0 | Logical and of corresponding request and mask bits. |
| 2 | CTR2_INT | R | RW | 0 | Logical and of corresponding request and mask bits. |

### 31.11.51.11 CTR

#### 31.11.51.11.1 MCWDT_CTR_CTL

**Description:** MCWDT Subcounter Control Register
**Address:** 0x40268000
**Offset:** 0x0
**Retention:** Retained
**IsDeepSleep:** Yes
**Comment:** Control register for this MCWDT subcounter. Writes are ignored when locked (i.e. corresponding MCWDT[i]_LOCK.WDT_LOCK<>0). This register may be written while the counter is running, but new values may take up to 2 clk_lf cycles to take effect.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:1] | | | | | | | ENABLED [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | ENABLE [31:31] | None [30:24] | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | ENABLED | R | RW | 0 | Indicates actual state of this subcounter. May lag ENABLE by up to two clk_lf cycles. |
| 31 | ENABLE | RW | R | 0 | Enable subcounter. May take up to 2 clk_lf cycles to take effect. When ENABLE changes from 1->0, the counter is cleared.<br>0: Counter is disabled (not clocked)<br>1: Counter is enabled (counting up) |

### 31.11.51.11.2 MCWDT_CTR_LOWER_LIMIT

**Description:** MCWDT Subcounter Lower Limit Register
**Address:** 0x40268004
**Offset:** 0x4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Lower limit for this MCWDT subcounter. Writes are ignored when locked (i.e. corresponding MCWDT[i]_LOCK.WDT_LOCK<>0). This register may be written while the counter is running, but new values may take up to 2 clk_lf cycles to take effect. Before changing the limit, it is recommended to set the service bit for this subcounter within the configured limits. This prevents possible unintended actions caused by the updated limits.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | LOWER_LIMIT [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | LOWER_LIMIT [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | LOWER_LIMIT | RW | R | 0 | Lower limit for this MCWDT subcounter. See LOWER_ACTION. |

### 31.11.51.11.3 MCWDT_CTR_UPPER_LIMIT

**Description:** MCWDT Subcounter Upper Limit Register
**Address:** 0x40268008
**Offset:** 0x8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Upper limit for this MCWDT subcounter. Writes are ignored when locked (i.e. corresponding MCWDT[i]_LOCK.WDT_LOCK<>0). This register may be written while the counter is running, but new values may take up to 2 clk_lf cycles to take effect. Before changing the limit, it is recommended to set the service bit for this subcounter within the configured limits. This prevents possible unintended actions caused by the updated limits.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | UPPER_LIMIT [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | UPPER_LIMIT [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | UPPER_LIMIT | RW | R | 0 | Upper limit for this MCWDT subcounter. See UPPER_ACTION. |

### 31.11.51.11.4 MCWDT_CTR_WARN_LIMIT

**Description:** MCWDT Subcounter Warn Limit Register
**Address:** 0x4026800C
**Offset:** 0xC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Warn limit for this MCWDT subcounter. Writes are ignored when locked (i.e. corresponding MCWDT[i]_LOCK.WDT_LOCK<>0). This register may be written while the counter is running, but new values may take up to 2 clk_lf cycles to take effect. Before changing the limit, it is recommended to set the service bit for this subcounter within the configured limits. This prevents possible unintended actions caused by the updated limits.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | WARN_LIMIT [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | WARN_LIMIT [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | WARN_LIMIT | RW | R | 0 | Warn limit for this MCWDT subcounter. See WARN_ACTION. |

### 31.11.51.11.5 MCWDT_CTR_CONFIG

**Description:** MCWDT Subcounter Configuration Register
**Address:** 0x40268010
**Offset:** 0x10
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Configuration for this MCWDT subcounter. Writes are ignored when locked (i.e. corresponding MCWDT[i]_LOCK.WDT_LOCK<>0). This register may be written while the counter is running, but new values may take up to 2 clk_lf cycles to take effect. MCWDT always reports the first fault that occurs across subcounter #0 and subcounter #1 for this MCWDT, but may not report additional faults that occur while the first is being processed.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:6] | | UPPER_ACTION [5:4] | | None [3:2] | | LOWER_ACTION [1:0] | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:13] | | | AUTO _SERVICE [12:12] | None [11:9] | | | WARN _ACTION [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | DEBUG _RUN [31:31] | SLEEPDEEP _PAUSE [30:30] | None [29:29] | DEBUG _TRIGGER _EN [28:28] | None [27:24] | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:1 | LOWER_ACTION | RW | R | 0 | Action taken if this watchdog is serviced before LOWER_LIMIT is reached. LOWER_ACTION is ignored (i.e. treated as NOTHING) when a debugger is connected and/or when the corresponding processor is in SLEEPDEEP. |
| | NOTHING | | | 0 | Do nothing |
| | FAULT | | | 1 | Trigger a fault. It can take up to 3 clk_lf cycles for the fault to be transferred to the fault manager.<br>For LOWER_LIMIT >= 1: The action is triggered on same edge when it meets this condition.<br>For LOWER_LIMIT == 0: No action is triggered. |
| | FAULT_THEN_RESET | | | 2 | Trigger a fault. Further, trigger a system-wide reset if the fault is not serviced and the watchdog is not cleared within 6 clk_lf cycles. It can take up to 3 clk_lf cycles for the fault to be transferred to the fault manager, which gives at least 3 clk_lf cycles for software to respond.<br>For LOWER_LIMIT >= 1: The action is triggered on same edge when it meets this condition.<br>For LOWER_LIMIT == 0: No action is triggered. |
| 4:5 | UPPER_ACTION | RW | R | 0 | Action taken if this watchdog is not serviced before UPPER_LIMIT is reached. The counter stops counting when UPPER_LIMIT is reached, regardless of UPPER_ACTION setting. UPPER_ACTION is ignored (i.e. treated as NOTHING) when a debugger is connected. |
| | NOTHING | | | 0 | Do nothing |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| | FAULT | | | 1 | Trigger a fault.<br>For UPPER_LIMIT >= 2: The action is triggered on same edge when it meets this condition.<br>For UPPER_LIMIT < 2: The action may take up to one extra clk_lf cycle to trigger. |
| | FAULT_THEN_RESET | | | 2 | Trigger a fault. Further, trigger a system-wide reset if the fault is not serviced and the watchdog is not cleared within 6 clk_lf cycles. It can take up to 3 clk_lf cycles for the fault to be transferred to the fault manager, which gives at least 3 clk_lf cycles for software to respond.<br>For UPPER_LIMIT >= 2: The action is triggered on same edge when it meets this condition.<br>For UPPER_LIMIT < 2: The action may take up to one extra clk_lf cycle to trigger. |
| 8 | WARN_ACTION | RW | R | 0 | Action taken when the count value reaches WARN_LIMIT. The minimum setting to achieve a periodic interrupt is WARN_LIMIT==1. A setting of zero will trigger once but not periodically.<br>For WARN_LIMIT >= 2: The action is triggered on same edge when it meets this condition.<br>For WARN_LIMIT == [0,1] : The action may take up to one extra clk_lf cycle to trigger. |
| | NOTHING | | | 0 | Do nothing |
| | INT | | | 1 | Trigger an interrupt. |
| 12 | AUTO_SERVICE | RW | R | 0 | Automatically service when the count value reaches WARN_LIMIT. This allows creation of a periodic interrupt if this counter is not needed as a watchdog. This field is ignored when LOWER_ACTION<>NOTHING or when UPPER_ACTION<>NOTHING. |
| 28 | DEBUG_TRIGGER_EN | RW | R | 0 | Enables the trigger input for this MCWDT to pause the counter during debug mode. To pause at a breakpoint while debugging, configure the trigger matrix to connect the related CPU halted signal to the trigger input for this MCWDT, and then set this bit. It takes up to two clk_lf cycles for the trigger signal to be processed. Triggers that are less than two clk_lf cycles may be missed. Synchronization errors can accumulate each time it is halted.<br>0: Pauses the counter whenever a debug probe is connected.<br>1: Pauses the counter whenever a debug probe is connected and the trigger input is high. |
| 30 | SLEEPDEEP_PAUSE | RW | R | 0 | Pauses/runs this counter when the corresponding processor is in SLEEPDEEP. Note it may take up to two clk_lf cycles for the counter to pause and up to two clk_lf cycles for it to unpause, due to internal synchronization. After wakeup, the LOWER_ACTION is ignored until after the first service. This prevents an unintentional trigger of the LOWER_ACTION before the firmware realigns the servicing period. After the first service, LOWER_ACTION behaves as configured.<br>0: Counter runs normally regardless of processor mode.<br>1: Counter pauses when corresponding processor is in SLEEPDEEP. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 31 | DEBUG_RUN | RW | R | 0 | Pauses/runs this counter while a debugger is connected. Other behaviors are unchanged during debugging, including service, configuration updates and enable/disable. Note it may take up to two clk_lf cycles for the counter to pause, due to internal synchronization.<br><br>When (DEBUG_RUN==1 or DEBUG_TRIGGER_EN==0) and the debugger is connected for at least two clk_lf cycles, the LOWER_ACTION is ignored until after the first service after the debugger is disconnected. After the debugger is disconnected, the LOWER_ACTION is ignored until after the first service. This prevents an unintentional trigger of the LOWER_ACTION before the firmware realigns the servicing period. After the first service, LOWER_ACTION behaves as configured. If the debugger is disconnected before two clk_lf cycles, the LOWER_ACTION may or may not be ignored.<br><br>0: When debugger connected, counter pauses incrementing as configured in DEBUG_TRIGGER_EN.<br><br>1: When debugger connected, counter increments normally, but reset generation is blocked. To block LOWER_ACTION fault generation, write DEBUG_TRIGGER_EN==0. |

### 31.11.51.11.6 MCWDT_CTR_CNT

**Description:** MCWDT Subcounter Count Register
**Address:** 0x40268014
**Offset:** 0x14
**Retention:** Retained
**IsDeepSleep:** Yes
**Comment:** Count value for this MCWDT subcounter. Writes are ignored when this subcounter is enabled or when it is locked (i.e. corresponding MCWDT[i]_LOCK.WDT_LOCK<>0).
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | CNT [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | CNT [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | CNT | RW | A | 0 | Current value of subcounter for this MCWDT. This field may lag the actual count value by up to one clk_lf cycle, due to internal synchronization. When this subcounter is disabled and unlocked, the count value can be written for verification and debugging purposes. Software writes are always ignored when the subcounter is enabled.This register retains information during DeepSleep mode if SLEEPDEEP_PAUSE == 1. |

### 31.11.52 WDT

#### 31.11.52.1 WDT_CTL

**Description:** WDT Control Register
**Address:** 0x4026C000
**Offset:** 0x0
**Retention:** Retained
**IsDeepSleep:** Yes
**Comment:** Control register for watchdog. Writes are ignored when locked (i.e. Corresponding LOCK.WDT_LOCK<>0).
**Default:** 0x80000001

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:1] | | | | | | | ENABLED [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | ENABLE [31:31] | None [30:24] | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | ENABLED | R | RW | 1 | Indicates actual state of watchdog. May lag ENABLE by up to three clk_ilo0 cycles. |
| 31 | ENABLE | RW | A | 1 | Enable watchdog. May take up to three clk_ilo0 cycles to take effect. When ENABLE changes from 1->0, the counter is cleared. Do not enter DEEPSLEEP or HIBERNATE mode if ENABLE<>ENABLED. This can be done by waiting until ENABLE==ENABLED whenever ENABLE is changed.<br>0: Counter is disabled (not clocked).<br>1: Counter is enabled (counting up) |

### 31.11.52.2 WDT_LOWER_LIMIT

**Description:** WDT Lower Limit Register
**Address:** 0x4026C004
**Offset:** 0x4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Lower limit for watchdog. Writes are ignored when locked (i.e. Corresponding LOCK.WDT_LOCK<>0) or when enabled (i.e. ENABLE==1 and ENABLED==1). This register is implemented in vddd domain. This register retains information during HIBERNATE mode.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | LOWER_LIMIT [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | LOWER_LIMIT [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | LOWER_LIMIT [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | LOWER_LIMIT [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | LOWER_LIMIT | RW | A | 0 | Lower limit for watchdog. See LOWER_ACTION. |

### 31.11.52.3 WDT_UPPER_LIMIT

**Description:** WDT Upper Limit Register
**Address:** 0x4026C008
**Offset:** 0x8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Upper limit for watchdog. Writes are ignored when locked (i.e. Corresponding LOCK.WDT_LOCK<>0) or when enabled (i.e. ENABLE==1 and ENABLED==1). This register is implemented in vddd domain. This register retains information during HIBERNATE mode.
**Default:** 0x8000

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | UPPER_LIMIT [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | UPPER_LIMIT [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | UPPER_LIMIT [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | UPPER_LIMIT [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | UPPER_LIMIT | RW | A | 32768 | Upper limit for watchdog. See UPPER_ACTION. |

### 31.11.52.4 WDT_WARN_LIMIT

**Description:** WDT Warn Limit Register
**Address:** 0x4026C00C
**Offset:** 0xC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Warn limit for watchdog. Writes are ignored when locked (i.e. Corresponding LOCK.WDT_LOCK<>0) or when enabled (i.e. ENABLE==1 and ENABLED==1). This register is implemented in vddd domain. This register retains information during HIBERNATE mode.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | WARN_LIMIT [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | WARN_LIMIT [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | WARN_LIMIT [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | WARN_LIMIT [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | WARN_LIMIT | RW | A | 0 | Warn limit for watchdog. See WARN_ACTION. |

### 31.11.52.5 WDT_CONFIG

**Description:** WDT Configuration Register
**Address:** 0x4026C010
**Offset:** 0x10
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Configuration for watchdog. Writes are ignored when locked (i.e. Corresponding LOCK.WDT_LOCK<>0) or when enabled (i.e. ENABLE==1 and ENABLED==1). This register is implemented in vddd domain. This register retains information during HIBERNATE mode.
**Default:** 0x10

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:5] | | | UPPER_ACTION [4:4] | None [3:1] | | | LOWER_ACTION [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:13] | | | AUTO_SERVICE [12:12] | None [11:9] | | | WARN_ACTION [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | DEBUG_RUN [31:31] | HIB_PAUSE [30:30] | DPSLP_PAUSE [29:29] | DEBUG_TRIGGER_EN [28:28] | None [27:24] | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | LOWER_ACTION | RW | A | 0 | Action taken if this watchdog is serviced before LOWER_LIMIT is reached. LOWER_ACTION is ignored (i.e. treated as NOTHING) when a debugger is connected and/or when the chip is in DEEPSLEEP/HIBERNATE modes.<br>For LOWER_LIMIT >= 1: The action is triggered on same edge when it meets this condition.<br>For LOWER_LIMIT == 0: No action is triggered. |
| | NOTHING | | | 0 | Do nothing |
| | RESET | | | 1 | Trigger a reset. |
| 4 | UPPER_ACTION | RW | A | 1 | Action taken if this watchdog is not serviced before UPPER_LIMIT is reached. The counter stops counting when UPPER_LIMIT is reached, regardless of UPPER_ACTION setting. UPPER_ACTION is ignored (i.e. treated as NOTHING) when a debugger is connected.<br>For UPPER_LIMIT >= 2: The action is triggered on same edge when it meets this condition.<br>For UPPER_LIMIT < 2: The action may take up to one extra clk_ilo0 cycle to trigger. |
| | NOTHING | | | 0 | Do nothing |
| | RESET | | | 1 | Trigger a reset. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 8 | WARN_ACTION | RW | A | 0 | Action taken when the count value reaches WARN_LIMIT. The minimum setting to achieve a periodic interrupt is WARN_LIMIT==1. A setting of zero will trigger once but not periodically.<br>For WARN_LIMIT >= 2: The action is triggered on same edge when it meets this condition.<br>For WARN_LIMIT < 2 : The action may take up to one extra clk_ilo0 cycle to trigger. |
| | NOTHING | | | 0 | Do nothing |
| | INT | | | 1 | Trigger an interrupt. |
| 12 | AUTO_SERVICE | RW | A | 0 | Automatically service when the count value reaches WARN_LIMIT. This allows creation of a periodic interrupt if this counter is not needed as a watchdog. This field is ignored when LOWER_ACTION<>NOTHING or when UPPER_ACTION<>NOTHING. |
| 28 | DEBUG_TRIGGER_EN | RW | A | 0 | Enables the trigger input for WDT to pause the counter during debug mode. To pause at a breakpoint while debugging, configure the trigger matrix to connect the related CPU halted signal to the trigger input for this WDT, and then set this bit. It takes up to two clk_ilo0 cycles for the trigger signal to be processed. Triggers that are less than two clk_ilo0 cycles may be missed. Synchronization error can accumulate each time it is halted.<br>0: Pauses the counter whenever a debug probe is connected.<br>1: Pauses the counter whenever a debug probe is connected and the trigger input is high. |
| 29 | DPSLP_PAUSE | RW | A | 0 | Pauses/runs this counter when the system is in DEEPSLEEP. Note it may take up to two clk_ilo0 cycles for the counter to pause, due to internal synchronization. During DEEPSLEEP wakeup, the pause request is removed when clk_hf0 starts clocking, and then it may take up to two clk_ilo0 cycles for the counter to start. After wakeup, the LOWER_ACTION is ignored until after the first service. This prevents an unintentional trigger of the LOWER_ACTION before the firmware realigns the servicing period. After the first service, LOWER_ACTION behaves as configured.<br>0: Counter behaves normally during DEEPSLEEP.<br>1: Counter pauses during DEEPSLEEP. |
| 30 | HIB_PAUSE | RW | A | 0 | Pauses/runs this counter when the system is in HIBERNATE. Note it may take up to two clk_ilo0 cycles for the counter to pause, due to internal synchronization. After wakeup, the LOWER_ACTION is ignored until after the first service. This prevents an unintentional trigger of the LOWER_ACTION before the firmware realigns the servicing period. After the first service, LOWER_ACTION behaves as configured.<br>0: Counter behaves normally during HIBERNATE.<br>1: Counter pauses during HIBERNATE. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 31 | DEBUG_RUN | RW | A | 0 | Pauses/runs this counter while a debugger is connected. Other behaviors are unchanged during debugging, including service, configuration updates and enable/disable. Note it may take up to two clk_ilo0 cycles for the counter to pause and another two cycles to unpause, due to internal synchronization. If the debugger is connected for at least two clk_ilo0 cycles, the LOWER_ACTION is ignored until after the first service after the debugger is disconnected. This prevents an unintentional trigger of the LOWER_ACTION before the firmware realigns the servicing period. After the first service, LOWER_ACTION behaves as configured. If the debugger is disconnected before two clk_ilo0 cycles, the LOWER_ACTION may or may not be ignored.<br>0: When debugger connected, counter pauses incrementing as configured in DEBUG_TRIGGER_EN.<br>1: When debugger connected, counter increments normally, but reset generation is blocked. |

### 31.11.52.6 WDT_CNT

**Description:** WDT Count Register
**Address:** 0x4026C014
**Offset:** 0x14
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Count value for watchdog. Writes are ignored when locked (i.e. Corresponding LOCK.WDT_LOCK<>0) or when enabled (i.e. ENABLE==1 and ENABLED==1). This register is implemented in vddd domain. This register retains information during HIBERNATE mode.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | CNT [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | CNT [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | CNT [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | CNT [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | CNT | RW | A | 0 | Current value of subcounter for this WDT. This field may lag the actual count value by up to one clk_ilo0 cycle, due to internal synchronization. When this subcounter is disabled and unlocked, the count value can be written for verification and debugging purposes. Software writes are always ignored when the subcounter is enabled. This register retains information during DeepSleep or Hiberbate mode if DPSLP_PAUSE == 1 or HIB_PAUSE == 1. |

### 31.11.52.7 WDT_LOCK

**Description:** WDT Lock register
**Address:** 0x4026C040
**Offset:** 0x40
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Lock or unlock the registers in this WDT
**Default:** 0x3

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:2] | | | | | | WDT_LOCK [1:0] | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:1 | WDT_LOCK | RW | A | 3 | Prohibits writing control and configuration registers related to this WDT when not equal 0 (as specified in the other register descriptions). Requires at least two different writes to unlock.<br>Note that this field is 2 bits to force multiple writes only. This register also locks the clk_ilo0 settings. |
| | NO_CHG | | | 0 | No effect |
| | CLR0 | | | 1 | Clears bit 0 |
| | CLR1 | | | 2 | Clears bit 1 |
| | SET01 | | | 3 | Sets both bits 0 and 1 |

### 31.11.52.8 WDT_SERVICE

**Description:** WDT Service register
**Address:** 0x4026C044
**Offset:** 0x44
**Retention:** Retained
**IsDeepSleep:** Yes
**Comment:** Control the behavior of the Watchdog counters. Writes to this register are ignored when LOCK.WDT_LOCK<>0. All fields in this register can be used while counter is in operation.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:1] | | | | | | | SERVICE [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | SERVICE | RW1S | RW1C | 0 | Services the watchdog. This resets the count value to zero. This may take up to three clk_ilo0 cycle to take effect. Hardware clears this bit, after necessary synchronization. To ensure a pending SERVICE write is reflected, firmware should wait until this bit reads low before attempting to write SERVICE=1. If WDT is disabled, SERVICE will not trigger a LOWER_ACTION and will not clear a preloaded count value. |

### 31.11.52.9 WDT_INTR

**Description:** WDT Interrupt Register
**Address:** 0x4026C050
**Offset:** 0x50
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** Interrupt signal from WDT
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:1] | | | | | | | WDT [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | WDT | RW1C | A | 0 | WDT Interrupt Request. This bit is set as configured by WDT action and limits. Due to internal synchronization, it takes up to 8 SYSCLK cycles to update after a W1C or reading this register and during this time AHB bus is stalled. |

### 31.11.52.10 WDT_INTR_SET

**Description:** WDT Interrupt Set Register
**Address:** 0x4026C054
**Offset:** 0x54
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Can be used to set interrupts for firmware testing.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:1] | | | | | | | WDT [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | WDT | RW1S | A | 0 | Set interrupt.<br>Due to internal synchronization, it takes up to 8 SYSCLK cycles to update after a W1S or reading from this register and during this time AHB bus is stalled. |

### 31.11.52.11 WDT_INTR_MASK

**Description:** WDT Interrupt Mask Register
**Address:** 0x4026C058
**Offset:** 0x58
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Controls whether interrupt is forwarded to CPU. All masks block the interrupt when 0 and forward the interrupt when 1
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:1] | | | | | | | WDT [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | WDT | RW | R | 0 | Mask for watchdog timer. Clearing this bit will not forward the interrupt to the CPU. |

### 31.11.52.12 WDT_INTR_MASKED

**Description:** WDT Interrupt Masked Register
**Address:** 0x4026C05C
**Offset:** 0x5C
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** Bitwise AND between the interrupt request and mask registers so firmware can read the status of all mask enabled interrupt causes with a single load operation
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:1] | | | | | | | WDT [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | WDT | R | RW | 0 | Logical and of corresponding request and mask bits. Due to internal synchronization, it takes up to 8 SYSCLK cycles to read from this register. During this time AHB bus is stalled. |

# 32 SYSAP

**Description** System debug Access Port (SYSAP) registers
**Base Address** 0xE0000000
**Size** 0x20000000
**Slave Num** SYSTEM

## 32.1 ROMTABLE

| Register Name | Address | Permission | Description |
|---|---|---|---|
| SYSAP_ROMTABLE_DID | 0xF1000FCC | FULL | Device Type Identifier register. |
| SYSAP_ROMTABLE_PID4 | 0xF1000FD0 | FULL | Peripheral Identification Register 4. |
| SYSAP_ROMTABLE_PID5 | 0xF1000FD4 | FULL | Peripheral Identification Register 5. |
| SYSAP_ROMTABLE_PID6 | 0xF1000FD8 | FULL | Peripheral Identification Register 6. |
| SYSAP_ROMTABLE_PID7 | 0xF1000FDC | FULL | Peripheral Identification Register 7. |
| SYSAP_ROMTABLE_PID0 | 0xF1000FE0 | FULL | Peripheral Identification Register 0. |
| SYSAP_ROMTABLE_PID1 | 0xF1000FE4 | FULL | Peripheral Identification Register 1. |
| SYSAP_ROMTABLE_PID2 | 0xF1000FE8 | FULL | Peripheral Identification Register 2. |
| SYSAP_ROMTABLE_PID3 | 0xF1000FEC | FULL | Peripheral Identification Register 3. |
| SYSAP_ROMTABLE_CID0 | 0xF1000FF0 | FULL | Component Identification Register 0. |
| SYSAP_ROMTABLE_CID1 | 0xF1000FF4 | FULL | Component Identification Register 1. |
| SYSAP_ROMTABLE_CID2 | 0xF1000FF8 | FULL | Component Identification Register 2. |
| SYSAP_ROMTABLE_CID3 | 0xF1000FFC | FULL | Component Identification Register 3. |

## 32.2 Register Details

### 32.2.1 ROMTABLE

#### 32.2.1.1 SYSAP_ROMTABLE_DID

**Description:** Device Type Identifier register.
**Address:** 0xF1000FCC
**Offset:** 0xFCC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x1

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 1 | . |

### 32.2.1.2 SYSAP_ROMTABLE_PID4

**Description:** Peripheral Identification Register 4.
**Address:** 0xF1000FD0
**Offset:** 0xFD0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** Undefined as one or more bit fields have a default value that is undefined

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNT [7:4] | | | | JEP_CONTINUATION [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | JEP_CONTINUATION | R | R | Undefined | JEP106 continuation code. This value is product specific and specified as part of the product definition in the CPUSS.JEPCONTINUATION parameter. |
| 4:7 | COUNT | R | R | 0 | Size of ROM Table is 2^COUNT * 4 KByte. |

### 32.2.1.3 SYSAP_ROMTABLE_PID5

**Description:** Peripheral Identification Register 5.
**Address:** 0xF1000FD4
**Offset:** 0xFD4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 0 | . |

### 32.2.1.4 SYSAP_ROMTABLE_PID6

**Description:** Peripheral Identification Register 6.
**Address:** 0xF1000FD8
**Offset:** 0xFD8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 0 | . |

### 32.2.1.5 SYSAP_ROMTABLE_PID7

**Description:** Peripheral Identification Register 7.
**Address:** 0xF1000FDC
**Offset:** 0xFDC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 0 | . |

### 32.2.1.6 SYSAP_ROMTABLE_PID0

**Description:** Peripheral Identification Register 0.
**Address:** 0xF1000FE0
**Offset:** 0xFE0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** Undefined as one or more bit fields have a default value that is undefined

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | PN_MIN [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | PN_MIN | R | R | Undefined | JEP106 part number. 4 lsbs of CPUSS.PARTNUMBER parameter. |

### 32.2.1.7 SYSAP_ROMTABLE_PID1

**Description:** Peripheral Identification Register 1.
**Address:** 0xF1000FE4
**Offset:** 0xFE4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** Undefined as one or more bit fields have a default value that is undefined

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | JEPID_MIN [7:4] | | | | PN_MAJ [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | PN_MAJ | R | R | Undefined | JEP106 part number. 4 msbs of CPUSS.PARTNUMBER parameter. |
| 4:7 | JEPID_MIN | R | R | Undefined | JEP106 vendor id. 4 lsbs of CPUSS.JEPID parameter. |

### 32.2.1.8 SYSAP_ROMTABLE_PID2

**Description:** Peripheral Identification Register 2.
**Address:** 0xF1000FE8
**Offset:** 0xFE8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** Undefined as one or more bit fields have a default value that is undefined

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | REV [7:4] | | | | None [3:3] | JEPID_MAJ [2:0] | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:2 | JEPID_MAJ | R | R | Undefined | JEP106 vendor id. 4 msbs of CPUSS.JEPID parameter. |
| 4:7 | REV | R | R | Undefined | Major REVision number (chip specific). Identifies the design iteration of the component. For first tape out: 0x1. This field is incremented on subsequent tape outs. |

### 32.2.1.9 SYSAP_ROMTABLE_PID3

**Description:** Peripheral Identification Register 3.
**Address:** 0xF1000FEC
**Offset:** 0xFEC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** Undefined as one or more bit fields have a default value that is undefined

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | REV_AND [7:4] | | | | CM [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:3 | CM | R | R | 0 | N/A |
| 4:7 | REV_AND | R | R | Undefined | Minor REVision number (chip specific). For first tape out: 0x1. This field is is incremented on subsequent tape outs. |

### 32.2.1.10 SYSAP_ROMTABLE_CID0

**Description:** Component Identification Register 0.
**Address:** 0xF1000FF0
**Offset:** 0xFF0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xD

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 13 | Component identification byte 0 of 4-byte component identification 0xB105:100D. |

### 32.2.1.11 SYSAP_ROMTABLE_CID1

**Description:** Component Identification Register 1.
**Address:** 0xF1000FF4
**Offset:** 0xFF4
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x10

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 16 | Component identification byte 1 of 4-byte component identification 0xB105:100D. Component class: 'ROM Table'. |

### 32.2.1.12 SYSAP_ROMTABLE_CID2

**Description:** Component Identification Register 2.
**Address:** 0xF1000FF8
**Offset:** 0xFF8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x5

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 5 | Component identification byte 2 of 4-byte component identification 0xB105:100D. |

### 32.2.1.13 SYSAP_ROMTABLE_CID3

**Description:** Component Identification Register 3.
**Address:** 0xF1000FFC
**Offset:** 0xFFC
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xB1

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | VALUE [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:31 | VALUE | R | R | 177 | Component identification byte 3 of 4-byte component identification 0xB105:100D. |

# 33 TCPWM

## 33.1 TCPWM 0

**Description** Timer/Counter/PWM
**Base Address** 0x40380000
**Size** 0x20000
**Slave Num** MMIO3 - 3

### 33.1.1 GRP 0

#### 33.1.1.1 CNT 0

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM0_GRP0_CNT0_CTRL | 0x40380000 | FULL | Counter control register<br>Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM0_GRP0_CNT0_STATUS | 0x40380004 | FULL | Counter status register<br>Note:DT_CNT_H is not available for this register |
| TCPWM0_GRP0_CNT0_COUNTER | 0x40380008 | FULL | Counter count register |
| TCPWM0_GRP0_CNT0_CC0 | 0x40380010 | FULL | Counter compare/capture 0 register |
| TCPWM0_GRP0_CNT0_CC0_BUFF | 0x40380014 | FULL | Counter buffered compare/capture 0 register |
| TCPWM0_GRP0_CNT0_CC1 | 0x40380018 | FULL | Counter compare/capture 1 register |
| TCPWM0_GRP0_CNT0_CC1_BUFF | 0x4038001C | FULL | Counter buffered compare/capture 1 register |
| TCPWM0_GRP0_CNT0_PERIOD | 0x40380020 | FULL | Counter period register |
| TCPWM0_GRP0_CNT0_PERIOD_BUFF | 0x40380024 | FULL | Counter buffered period register |
| TCPWM0_GRP0_CNT0_DT | 0x40380030 | FULL | Counter PWM dead time register<br>Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM0_GRP0_CNT0_TR_CMD | 0x40380040 | FULL | Counter trigger command register |
| TCPWM0_GRP0_CNT0_TR_IN_SEL0 | 0x40380044 | FULL | Counter input trigger selection register 0 |
| TCPWM0_GRP0_CNT0_TR_IN_SEL1 | 0x40380048 | FULL | Counter input trigger selection register 1 |
| TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL | 0x4038004C | FULL | Counter input trigger edge selection register |
| TCPWM0_GRP0_CNT0_TR_PWM_CTRL | 0x40380050 | FULL | Counter trigger PWM control register |
| TCPWM0_GRP0_CNT0_TR_OUT_SEL | 0x40380054 | FULL | Counter output trigger selection register |
| TCPWM0_GRP0_CNT0_INTR | 0x40380070 | FULL | Interrupt request register |
| TCPWM0_GRP0_CNT0_INTR_SET | 0x40380074 | FULL | Interrupt set request register |
| TCPWM0_GRP0_CNT0_INTR_MASK | 0x40380078 | FULL | Interrupt mask register |
| TCPWM0_GRP0_CNT0_INTR_MASKED | 0x4038007C | FULL | Interrupt masked request register |

#### 33.1.1.2 CNT 1

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM0_GRP0_CNT1_CTRL | 0x40380080 | FULL | Counter control register<br>Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM0_GRP0_CNT1_STATUS | 0x40380084 | FULL | Counter status register<br>Note:DT_CNT_H is not available for this register |
| TCPWM0_GRP0_CNT1_COUNTER | 0x40380088 | FULL | Counter count register |
| TCPWM0_GRP0_CNT1_CC0 | 0x40380090 | FULL | Counter compare/capture 0 register |
| TCPWM0_GRP0_CNT1_CC0_BUFF | 0x40380094 | FULL | Counter buffered compare/capture 0 register |
| TCPWM0_GRP0_CNT1_CC1 | 0x40380098 | FULL | Counter compare/capture 1 register |
| TCPWM0_GRP0_CNT1_CC1_BUFF | 0x4038009C | FULL | Counter buffered compare/capture 1 register |
| TCPWM0_GRP0_CNT1_PERIOD | 0x403800A0 | FULL | Counter period register |
| TCPWM0_GRP0_CNT1_PERIOD_BUFF | 0x403800A4 | FULL | Counter buffered period register |
| TCPWM0_GRP0_CNT1_DT | 0x403800B0 | FULL | Counter PWM dead time register<br>Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM0_GRP0_CNT1_TR_CMD | 0x403800C0 | FULL | Counter trigger command register |
| TCPWM0_GRP0_CNT1_TR_IN_SEL0 | 0x403800C4 | FULL | Counter input trigger selection register 0 |
| TCPWM0_GRP0_CNT1_TR_IN_SEL1 | 0x403800C8 | FULL | Counter input trigger selection register 1 |
| TCPWM0_GRP0_CNT1_TR_IN_EDGE_SEL | 0x403800CC | FULL | Counter input trigger edge selection register |
| TCPWM0_GRP0_CNT1_TR_PWM_CTRL | 0x403800D0 | FULL | Counter trigger PWM control register |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM0_GRP0_CNT1_TR_OUT_SEL | 0x403800D4 | FULL | Counter output trigger selection register |
| TCPWM0_GRP0_CNT1_INTR | 0x403800F0 | FULL | Interrupt request register |
| TCPWM0_GRP0_CNT1_INTR_SET | 0x403800F4 | FULL | Interrupt set request register |
| TCPWM0_GRP0_CNT1_INTR_MASK | 0x403800F8 | FULL | Interrupt mask register |
| TCPWM0_GRP0_CNT1_INTR_MASKED | 0x403800FC | FULL | Interrupt masked request register |

#### 33.1.1.3 CNT 2

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM0_GRP0_CNT2_CTRL | 0x40380100 | FULL | Counter control register<br>Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM0_GRP0_CNT2_STATUS | 0x40380104 | FULL | Counter status register<br>Note:DT_CNT_H is not available for this register |
| TCPWM0_GRP0_CNT2_COUNTER | 0x40380108 | FULL | Counter count register |
| TCPWM0_GRP0_CNT2_CC0 | 0x40380110 | FULL | Counter compare/capture 0 register |
| TCPWM0_GRP0_CNT2_CC0_BUFF | 0x40380114 | FULL | Counter buffered compare/capture 0 register |
| TCPWM0_GRP0_CNT2_CC1 | 0x40380118 | FULL | Counter compare/capture 1 register |
| TCPWM0_GRP0_CNT2_CC1_BUFF | 0x4038011C | FULL | Counter buffered compare/capture 1 register |
| TCPWM0_GRP0_CNT2_PERIOD | 0x40380120 | FULL | Counter period register |
| TCPWM0_GRP0_CNT2_PERIOD_BUFF | 0x40380124 | FULL | Counter buffered period register |
| TCPWM0_GRP0_CNT2_DT | 0x40380130 | FULL | Counter PWM dead time register<br>Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM0_GRP0_CNT2_TR_CMD | 0x40380140 | FULL | Counter trigger command register |
| TCPWM0_GRP0_CNT2_TR_IN_SEL0 | 0x40380144 | FULL | Counter input trigger selection register 0 |
| TCPWM0_GRP0_CNT2_TR_IN_SEL1 | 0x40380148 | FULL | Counter input trigger selection register 1 |
| TCPWM0_GRP0_CNT2_TR_IN_EDGE_SEL | 0x4038014C | FULL | Counter input trigger edge selection register |
| TCPWM0_GRP0_CNT2_TR_PWM_CTRL | 0x40380150 | FULL | Counter trigger PWM control register |
| TCPWM0_GRP0_CNT2_TR_OUT_SEL | 0x40380154 | FULL | Counter output trigger selection register |
| TCPWM0_GRP0_CNT2_INTR | 0x40380170 | FULL | Interrupt request register |
| TCPWM0_GRP0_CNT2_INTR_SET | 0x40380174 | FULL | Interrupt set request register |
| TCPWM0_GRP0_CNT2_INTR_MASK | 0x40380178 | FULL | Interrupt mask register |
| TCPWM0_GRP0_CNT2_INTR_MASKED | 0x4038017C | FULL | Interrupt masked request register |

### 33.1.2 GRP 1

#### 33.1.2.1 CNT 0

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM0_GRP1_CNT0_CTRL | 0x40388000 | FULL | Counter control register |
| TCPWM0_GRP1_CNT0_STATUS | 0x40388004 | FULL | Counter status register |
| TCPWM0_GRP1_CNT0_COUNTER | 0x40388008 | FULL | Counter count register |
| TCPWM0_GRP1_CNT0_CC0 | 0x40388010 | FULL | Counter compare/capture 0 register |
| TCPWM0_GRP1_CNT0_CC0_BUFF | 0x40388014 | FULL | Counter buffered compare/capture 0 register |
| TCPWM0_GRP1_CNT0_CC1 | 0x40388018 | FULL | Counter compare/capture 1 register |
| TCPWM0_GRP1_CNT0_CC1_BUFF | 0x4038801C | FULL | Counter buffered compare/capture 1 register |
| TCPWM0_GRP1_CNT0_PERIOD | 0x40388020 | FULL | Counter period register |
| TCPWM0_GRP1_CNT0_PERIOD_BUFF | 0x40388024 | FULL | Counter buffered period register |
| TCPWM0_GRP1_CNT0_LINE_SEL | 0x40388028 | FULL | Counter line selection register |
| TCPWM0_GRP1_CNT0_LINE_SEL_BUFF | 0x4038802C | FULL | Counter buffered line selection register |
| TCPWM0_GRP1_CNT0_DT | 0x40388030 | FULL | Counter PWM dead time register |
| TCPWM0_GRP1_CNT0_TR_CMD | 0x40388040 | FULL | Counter trigger command register |
| TCPWM0_GRP1_CNT0_TR_IN_SEL0 | 0x40388044 | FULL | Counter input trigger selection register 0 |
| TCPWM0_GRP1_CNT0_TR_IN_SEL1 | 0x40388048 | FULL | Counter input trigger selection register 1 |
| TCPWM0_GRP1_CNT0_TR_IN_EDGE_SEL | 0x4038804C | FULL | Counter input trigger edge selection register |
| TCPWM0_GRP1_CNT0_TR_PWM_CTRL | 0x40388050 | FULL | Counter trigger PWM control register |
| TCPWM0_GRP1_CNT0_TR_OUT_SEL | 0x40388054 | FULL | Counter output trigger selection register |
| TCPWM0_GRP1_CNT0_INTR | 0x40388070 | FULL | Interrupt request register |
| TCPWM0_GRP1_CNT0_INTR_SET | 0x40388074 | FULL | Interrupt set request register |
| TCPWM0_GRP1_CNT0_INTR_MASK | 0x40388078 | FULL | Interrupt mask register |
| TCPWM0_GRP1_CNT0_INTR_MASKED | 0x4038807C | FULL | Interrupt masked request register |

#### 33.1.2.2 CNT 1

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM0_GRP1_CNT1_CTRL | 0x40388080 | FULL | Counter control register |
| TCPWM0_GRP1_CNT1_STATUS | 0x40388084 | FULL | Counter status register |
| TCPWM0_GRP1_CNT1_COUNTER | 0x40388088 | FULL | Counter count register |
| TCPWM0_GRP1_CNT1_CC0 | 0x40388090 | FULL | Counter compare/capture 0 register |
| TCPWM0_GRP1_CNT1_CC0_BUFF | 0x40388094 | FULL | Counter buffered compare/capture 0 register |
| TCPWM0_GRP1_CNT1_CC1 | 0x40388098 | FULL | Counter compare/capture 1 register |
| TCPWM0_GRP1_CNT1_CC1_BUFF | 0x4038809C | FULL | Counter buffered compare/capture 1 register |
| TCPWM0_GRP1_CNT1_PERIOD | 0x403880A0 | FULL | Counter period register |
| TCPWM0_GRP1_CNT1_PERIOD_BUFF | 0x403880A4 | FULL | Counter buffered period register |
| TCPWM0_GRP1_CNT1_LINE_SEL | 0x403880A8 | FULL | Counter line selection register |
| TCPWM0_GRP1_CNT1_LINE_SEL_BUFF | 0x403880AC | FULL | Counter buffered line selection register |
| TCPWM0_GRP1_CNT1_DT | 0x403880B0 | FULL | Counter PWM dead time register |
| TCPWM0_GRP1_CNT1_TR_CMD | 0x403880C0 | FULL | Counter trigger command register |
| TCPWM0_GRP1_CNT1_TR_IN_SEL0 | 0x403880C4 | FULL | Counter input trigger selection register 0 |
| TCPWM0_GRP1_CNT1_TR_IN_SEL1 | 0x403880C8 | FULL | Counter input trigger selection register 1 |
| TCPWM0_GRP1_CNT1_TR_IN_EDGE_SEL | 0x403880CC | FULL | Counter input trigger edge selection register |
| TCPWM0_GRP1_CNT1_TR_PWM_CTRL | 0x403880D0 | FULL | Counter trigger PWM control register |
| TCPWM0_GRP1_CNT1_TR_OUT_SEL | 0x403880D4 | FULL | Counter output trigger selection register |
| TCPWM0_GRP1_CNT1_INTR | 0x403880F0 | FULL | Interrupt request register |
| TCPWM0_GRP1_CNT1_INTR_SET | 0x403880F4 | FULL | Interrupt set request register |
| TCPWM0_GRP1_CNT1_INTR_MASK | 0x403880F8 | FULL | Interrupt mask register |
| TCPWM0_GRP1_CNT1_INTR_MASKED | 0x403880FC | FULL | Interrupt masked request register |

#### 33.1.2.3 CNT 2

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM0_GRP1_CNT2_CTRL | 0x40388100 | FULL | Counter control register |
| TCPWM0_GRP1_CNT2_STATUS | 0x40388104 | FULL | Counter status register |
| TCPWM0_GRP1_CNT2_COUNTER | 0x40388108 | FULL | Counter count register |
| TCPWM0_GRP1_CNT2_CC0 | 0x40388110 | FULL | Counter compare/capture 0 register |
| TCPWM0_GRP1_CNT2_CC0_BUFF | 0x40388114 | FULL | Counter buffered compare/capture 0 register |
| TCPWM0_GRP1_CNT2_CC1 | 0x40388118 | FULL | Counter compare/capture 1 register |
| TCPWM0_GRP1_CNT2_CC1_BUFF | 0x4038811C | FULL | Counter buffered compare/capture 1 register |
| TCPWM0_GRP1_CNT2_PERIOD | 0x40388120 | FULL | Counter period register |
| TCPWM0_GRP1_CNT2_PERIOD_BUFF | 0x40388124 | FULL | Counter buffered period register |
| TCPWM0_GRP1_CNT2_LINE_SEL | 0x40388128 | FULL | Counter line selection register |
| TCPWM0_GRP1_CNT2_LINE_SEL_BUFF | 0x4038812C | FULL | Counter buffered line selection register |
| TCPWM0_GRP1_CNT2_DT | 0x40388130 | FULL | Counter PWM dead time register |
| TCPWM0_GRP1_CNT2_TR_CMD | 0x40388140 | FULL | Counter trigger command register |
| TCPWM0_GRP1_CNT2_TR_IN_SEL0 | 0x40388144 | FULL | Counter input trigger selection register 0 |
| TCPWM0_GRP1_CNT2_TR_IN_SEL1 | 0x40388148 | FULL | Counter input trigger selection register 1 |
| TCPWM0_GRP1_CNT2_TR_IN_EDGE_SEL | 0x4038814C | FULL | Counter input trigger edge selection register |
| TCPWM0_GRP1_CNT2_TR_PWM_CTRL | 0x40388150 | FULL | Counter trigger PWM control register |
| TCPWM0_GRP1_CNT2_TR_OUT_SEL | 0x40388154 | FULL | Counter output trigger selection register |
| TCPWM0_GRP1_CNT2_INTR | 0x40388170 | FULL | Interrupt request register |
| TCPWM0_GRP1_CNT2_INTR_SET | 0x40388174 | FULL | Interrupt set request register |
| TCPWM0_GRP1_CNT2_INTR_MASK | 0x40388178 | FULL | Interrupt mask register |
| TCPWM0_GRP1_CNT2_INTR_MASKED | 0x4038817C | FULL | Interrupt masked request register |

### 33.1.3 GRP 2

#### 33.1.3.1 CNT 0

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM0_GRP2_CNT0_CTRL | 0x40390000 | FULL | Counter control register<br>Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM0_GRP2_CNT0_STATUS | 0x40390004 | FULL | Counter status register<br>Note:DT_CNT_H is not available for this register |
| TCPWM0_GRP2_CNT0_COUNTER | 0x40390008 | FULL | Counter count register |
| TCPWM0_GRP2_CNT0_CC0 | 0x40390010 | FULL | Counter compare/capture 0 register |
| TCPWM0_GRP2_CNT0_CC0_BUFF | 0x40390014 | FULL | Counter buffered compare/capture 0 register |
| TCPWM0_GRP2_CNT0_CC1 | 0x40390018 | FULL | Counter compare/capture 1 register |
| TCPWM0_GRP2_CNT0_CC1_BUFF | 0x4039001C | FULL | Counter buffered compare/capture 1 register |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM0_GRP2_CNT0_PERIOD | 0x40390020 | FULL | Counter period register |
| TCPWM0_GRP2_CNT0_PERIOD_BUFF | 0x40390024 | FULL | Counter buffered period register |
| TCPWM0_GRP2_CNT0_DT | 0x40390030 | FULL | Counter PWM dead time register<br>Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM0_GRP2_CNT0_TR_CMD | 0x40390040 | FULL | Counter trigger command register |
| TCPWM0_GRP2_CNT0_TR_IN_SEL0 | 0x40390044 | FULL | Counter input trigger selection register 0 |
| TCPWM0_GRP2_CNT0_TR_IN_SEL1 | 0x40390048 | FULL | Counter input trigger selection register 1 |
| TCPWM0_GRP2_CNT0_TR_IN_EDGE_SEL | 0x4039004C | FULL | Counter input trigger edge selection register |
| TCPWM0_GRP2_CNT0_TR_PWM_CTRL | 0x40390050 | FULL | Counter trigger PWM control register |
| TCPWM0_GRP2_CNT0_TR_OUT_SEL | 0x40390054 | FULL | Counter output trigger selection register |
| TCPWM0_GRP2_CNT0_INTR | 0x40390070 | FULL | Interrupt request register |
| TCPWM0_GRP2_CNT0_INTR_SET | 0x40390074 | FULL | Interrupt set request register |
| TCPWM0_GRP2_CNT0_INTR_MASK | 0x40390078 | FULL | Interrupt mask register |
| TCPWM0_GRP2_CNT0_INTR_MASKED | 0x4039007C | FULL | Interrupt masked request register |

### 33.1.3.2 CNT 1

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM0_GRP2_CNT1_CTRL | 0x40390080 | FULL | Counter control register<br>Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM0_GRP2_CNT1_STATUS | 0x40390084 | FULL | Counter status register<br>Note:DT_CNT_H is not available for this register |
| TCPWM0_GRP2_CNT1_COUNTER | 0x40390088 | FULL | Counter count register |
| TCPWM0_GRP2_CNT1_CC0 | 0x40390090 | FULL | Counter compare/capture 0 register |
| TCPWM0_GRP2_CNT1_CC0_BUFF | 0x40390094 | FULL | Counter buffered compare/capture 0 register |
| TCPWM0_GRP2_CNT1_CC1 | 0x40390098 | FULL | Counter compare/capture 1 register |
| TCPWM0_GRP2_CNT1_CC1_BUFF | 0x4039009C | FULL | Counter buffered compare/capture 1 register |
| TCPWM0_GRP2_CNT1_PERIOD | 0x403900A0 | FULL | Counter period register |
| TCPWM0_GRP2_CNT1_PERIOD_BUFF | 0x403900A4 | FULL | Counter buffered period register |
| TCPWM0_GRP2_CNT1_DT | 0x403900B0 | FULL | Counter PWM dead time register<br>Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM0_GRP2_CNT1_TR_CMD | 0x403900C0 | FULL | Counter trigger command register |
| TCPWM0_GRP2_CNT1_TR_IN_SEL0 | 0x403900C4 | FULL | Counter input trigger selection register 0 |
| TCPWM0_GRP2_CNT1_TR_IN_SEL1 | 0x403900C8 | FULL | Counter input trigger selection register 1 |
| TCPWM0_GRP2_CNT1_TR_IN_EDGE_SEL | 0x403900CC | FULL | Counter input trigger edge selection register |
| TCPWM0_GRP2_CNT1_TR_PWM_CTRL | 0x403900D0 | FULL | Counter trigger PWM control register |
| TCPWM0_GRP2_CNT1_TR_OUT_SEL | 0x403900D4 | FULL | Counter output trigger selection register |
| TCPWM0_GRP2_CNT1_INTR | 0x403900F0 | FULL | Interrupt request register |
| TCPWM0_GRP2_CNT1_INTR_SET | 0x403900F4 | FULL | Interrupt set request register |
| TCPWM0_GRP2_CNT1_INTR_MASK | 0x403900F8 | FULL | Interrupt mask register |
| TCPWM0_GRP2_CNT1_INTR_MASKED | 0x403900FC | FULL | Interrupt masked request register |

### 33.1.3.3 CNT 2

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM0_GRP2_CNT2_CTRL | 0x40390100 | FULL | Counter control register<br>Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM0_GRP2_CNT2_STATUS | 0x40390104 | FULL | Counter status register<br>Note:DT_CNT_H is not available for this register |
| TCPWM0_GRP2_CNT2_COUNTER | 0x40390108 | FULL | Counter count register |
| TCPWM0_GRP2_CNT2_CC0 | 0x40390110 | FULL | Counter compare/capture 0 register |
| TCPWM0_GRP2_CNT2_CC0_BUFF | 0x40390114 | FULL | Counter buffered compare/capture 0 register |
| TCPWM0_GRP2_CNT2_CC1 | 0x40390118 | FULL | Counter compare/capture 1 register |
| TCPWM0_GRP2_CNT2_CC1_BUFF | 0x4039011C | FULL | Counter buffered compare/capture 1 register |
| TCPWM0_GRP2_CNT2_PERIOD | 0x40390120 | FULL | Counter period register |
| TCPWM0_GRP2_CNT2_PERIOD_BUFF | 0x40390124 | FULL | Counter buffered period register |
| TCPWM0_GRP2_CNT2_DT | 0x40390130 | FULL | Counter PWM dead time register<br>Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM0_GRP2_CNT2_TR_CMD | 0x40390140 | FULL | Counter trigger command register |
| TCPWM0_GRP2_CNT2_TR_IN_SEL0 | 0x40390144 | FULL | Counter input trigger selection register 0 |
| TCPWM0_GRP2_CNT2_TR_IN_SEL1 | 0x40390148 | FULL | Counter input trigger selection register 1 |
| TCPWM0_GRP2_CNT2_TR_IN_EDGE_SEL | 0x4039014C | FULL | Counter input trigger edge selection register |
| TCPWM0_GRP2_CNT2_TR_PWM_CTRL | 0x40390150 | FULL | Counter trigger PWM control register |
| TCPWM0_GRP2_CNT2_TR_OUT_SEL | 0x40390154 | FULL | Counter output trigger selection register |
| TCPWM0_GRP2_CNT2_INTR | 0x40390170 | FULL | Interrupt request register |
| TCPWM0_GRP2_CNT2_INTR_SET | 0x40390174 | FULL | Interrupt set request register |
| TCPWM0_GRP2_CNT2_INTR_MASK | 0x40390178 | FULL | Interrupt mask register |
| TCPWM0_GRP2_CNT2_INTR_MASKED | 0x4039017C | FULL | Interrupt masked request register |

## 33.2 TCPWM 1

**Description** Timer/Counter/PWM
**Base Address** 0x40580000
**Size** 0x20000
**Slave Num** MMIO5 - 5

### 33.2.1 GRP 0

#### 33.2.1.1 CNT 0

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT0_CTRL | 0x40580000 | FULL | Counter control register<br>Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM1_GRP0_CNT0_STATUS | 0x40580004 | FULL | Counter status register<br>Note:DT_CNT_H is not available for this register |
| TCPWM1_GRP0_CNT0_COUNTER | 0x40580008 | FULL | Counter count register |
| TCPWM1_GRP0_CNT0_CC0 | 0x40580010 | FULL | Counter compare/capture 0 register |
| TCPWM1_GRP0_CNT0_CC0_BUFF | 0x40580014 | FULL | Counter buffered compare/capture 0 register |
| TCPWM1_GRP0_CNT0_CC1 | 0x40580018 | FULL | Counter compare/capture 1 register |
| TCPWM1_GRP0_CNT0_CC1_BUFF | 0x4058001C | FULL | Counter buffered compare/capture 1 register |
| TCPWM1_GRP0_CNT0_PERIOD | 0x40580020 | FULL | Counter period register |
| TCPWM1_GRP0_CNT0_PERIOD_BUFF | 0x40580024 | FULL | Counter buffered period register |
| TCPWM1_GRP0_CNT0_DT | 0x40580030 | FULL | Counter PWM dead time register<br>Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM1_GRP0_CNT0_TR_CMD | 0x40580040 | FULL | Counter trigger command register |
| TCPWM1_GRP0_CNT0_TR_IN_SEL0 | 0x40580044 | FULL | Counter input trigger selection register 0 |
| TCPWM1_GRP0_CNT0_TR_IN_SEL1 | 0x40580048 | FULL | Counter input trigger selection register 1 |
| TCPWM1_GRP0_CNT0_TR_IN_EDGE_SEL | 0x4058004C | FULL | Counter input trigger edge selection register |
| TCPWM1_GRP0_CNT0_TR_PWM_CTRL | 0x40580050 | FULL | Counter trigger PWM control register |
| TCPWM1_GRP0_CNT0_TR_OUT_SEL | 0x40580054 | FULL | Counter output trigger selection register |
| TCPWM1_GRP0_CNT0_INTR | 0x40580070 | FULL | Interrupt request register |
| TCPWM1_GRP0_CNT0_INTR_SET | 0x40580074 | FULL | Interrupt set request register |
| TCPWM1_GRP0_CNT0_INTR_MASK | 0x40580078 | FULL | Interrupt mask register |
| TCPWM1_GRP0_CNT0_INTR_MASKED | 0x4058007C | FULL | Interrupt masked request register |

#### 33.2.1.2 CNT 1

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT1_CTRL | 0x40580080 | FULL | Counter control register<br>Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM1_GRP0_CNT1_STATUS | 0x40580084 | FULL | Counter status register<br>Note:DT_CNT_H is not available for this register |
| TCPWM1_GRP0_CNT1_COUNTER | 0x40580088 | FULL | Counter count register |
| TCPWM1_GRP0_CNT1_CC0 | 0x40580090 | FULL | Counter compare/capture 0 register |
| TCPWM1_GRP0_CNT1_CC0_BUFF | 0x40580094 | FULL | Counter buffered compare/capture 0 register |
| TCPWM1_GRP0_CNT1_CC1 | 0x40580098 | FULL | Counter compare/capture 1 register |
| TCPWM1_GRP0_CNT1_CC1_BUFF | 0x4058009C | FULL | Counter buffered compare/capture 1 register |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT1_PERIOD | 0x405800A0 | FULL | Counter period register |
| TCPWM1_GRP0_CNT1_PERIOD_BUFF | 0x405800A4 | FULL | Counter buffered period register |
| TCPWM1_GRP0_CNT1_DT | 0x405800B0 | FULL | Counter PWM dead time register<br>Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM1_GRP0_CNT1_TR_CMD | 0x405800C0 | FULL | Counter trigger command register |
| TCPWM1_GRP0_CNT1_TR_IN_SEL0 | 0x405800C4 | FULL | Counter input trigger selection register 0 |
| TCPWM1_GRP0_CNT1_TR_IN_SEL1 | 0x405800C8 | FULL | Counter input trigger selection register 1 |
| TCPWM1_GRP0_CNT1_TR_IN_EDGE_SEL | 0x405800CC | FULL | Counter input trigger edge selection register |
| TCPWM1_GRP0_CNT1_TR_PWM_CTRL | 0x405800D0 | FULL | Counter trigger PWM control register |
| TCPWM1_GRP0_CNT1_TR_OUT_SEL | 0x405800D4 | FULL | Counter output trigger selection register |
| TCPWM1_GRP0_CNT1_INTR | 0x405800F0 | FULL | Interrupt request register |
| TCPWM1_GRP0_CNT1_INTR_SET | 0x405800F4 | FULL | Interrupt set request register |
| TCPWM1_GRP0_CNT1_INTR_MASK | 0x405800F8 | FULL | Interrupt mask register |
| TCPWM1_GRP0_CNT1_INTR_MASKED | 0x405800FC | FULL | Interrupt masked request register |

### 33.2.1.3 CNT 2

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT2_CTRL | 0x40580100 | FULL | Counter control register<br>Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM1_GRP0_CNT2_STATUS | 0x40580104 | FULL | Counter status register<br>Note:DT_CNT_H is not available for this register |
| TCPWM1_GRP0_CNT2_COUNTER | 0x40580108 | FULL | Counter count register |
| TCPWM1_GRP0_CNT2_CC0 | 0x40580110 | FULL | Counter compare/capture 0 register |
| TCPWM1_GRP0_CNT2_CC0_BUFF | 0x40580114 | FULL | Counter buffered compare/capture 0 register |
| TCPWM1_GRP0_CNT2_CC1 | 0x40580118 | FULL | Counter compare/capture 1 register |
| TCPWM1_GRP0_CNT2_CC1_BUFF | 0x4058011C | FULL | Counter buffered compare/capture 1 register |
| TCPWM1_GRP0_CNT2_PERIOD | 0x40580120 | FULL | Counter period register |
| TCPWM1_GRP0_CNT2_PERIOD_BUFF | 0x40580124 | FULL | Counter buffered period register |
| TCPWM1_GRP0_CNT2_DT | 0x40580130 | FULL | Counter PWM dead time register<br>Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM1_GRP0_CNT2_TR_CMD | 0x40580140 | FULL | Counter trigger command register |
| TCPWM1_GRP0_CNT2_TR_IN_SEL0 | 0x40580144 | FULL | Counter input trigger selection register 0 |
| TCPWM1_GRP0_CNT2_TR_IN_SEL1 | 0x40580148 | FULL | Counter input trigger selection register 1 |
| TCPWM1_GRP0_CNT2_TR_IN_EDGE_SEL | 0x4058014C | FULL | Counter input trigger edge selection register |
| TCPWM1_GRP0_CNT2_TR_PWM_CTRL | 0x40580150 | FULL | Counter trigger PWM control register |
| TCPWM1_GRP0_CNT2_TR_OUT_SEL | 0x40580154 | FULL | Counter output trigger selection register |
| TCPWM1_GRP0_CNT2_INTR | 0x40580170 | FULL | Interrupt request register |
| TCPWM1_GRP0_CNT2_INTR_SET | 0x40580174 | FULL | Interrupt set request register |
| TCPWM1_GRP0_CNT2_INTR_MASK | 0x40580178 | FULL | Interrupt mask register |
| TCPWM1_GRP0_CNT2_INTR_MASKED | 0x4058017C | FULL | Interrupt masked request register |

### 33.2.1.4 CNT 3

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT3_CTRL | 0x40580180 | FULL | Counter control register<br>Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM1_GRP0_CNT3_STATUS | 0x40580184 | FULL | Counter status register<br>Note:DT_CNT_H is not available for this register |
| TCPWM1_GRP0_CNT3_COUNTER | 0x40580188 | FULL | Counter count register |
| TCPWM1_GRP0_CNT3_CC0 | 0x40580190 | FULL | Counter compare/capture 0 register |
| TCPWM1_GRP0_CNT3_CC0_BUFF | 0x40580194 | FULL | Counter buffered compare/capture 0 register |
| TCPWM1_GRP0_CNT3_CC1 | 0x40580198 | FULL | Counter compare/capture 1 register |
| TCPWM1_GRP0_CNT3_CC1_BUFF | 0x4058019C | FULL | Counter buffered compare/capture 1 register |
| TCPWM1_GRP0_CNT3_PERIOD | 0x405801A0 | FULL | Counter period register |
| TCPWM1_GRP0_CNT3_PERIOD_BUFF | 0x405801A4 | FULL | Counter buffered period register |
| TCPWM1_GRP0_CNT3_DT | 0x405801B0 | FULL | Counter PWM dead time register<br>Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT3_TR_CMD | 0x405801C0 | FULL | Counter trigger command register |
| TCPWM1_GRP0_CNT3_TR_IN_SEL0 | 0x405801C4 | FULL | Counter input trigger selection register 0 |
| TCPWM1_GRP0_CNT3_TR_IN_SEL1 | 0x405801C8 | FULL | Counter input trigger selection register 1 |
| TCPWM1_GRP0_CNT3_TR_IN_EDGE_SEL | 0x405801CC | FULL | Counter input trigger edge selection register |
| TCPWM1_GRP0_CNT3_TR_PWM_CTRL | 0x405801D0 | FULL | Counter trigger PWM control register |
| TCPWM1_GRP0_CNT3_TR_OUT_SEL | 0x405801D4 | FULL | Counter output trigger selection register |
| TCPWM1_GRP0_CNT3_INTR | 0x405801F0 | FULL | Interrupt request register |
| TCPWM1_GRP0_CNT3_INTR_SET | 0x405801F4 | FULL | Interrupt set request register |
| TCPWM1_GRP0_CNT3_INTR_MASK | 0x405801F8 | FULL | Interrupt mask register |
| TCPWM1_GRP0_CNT3_INTR_MASKED | 0x405801FC | FULL | Interrupt masked request register |

### 33.2.1.5 CNT 4

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT4_CTRL | 0x40580200 | FULL | Counter control register<br>Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM1_GRP0_CNT4_STATUS | 0x40580204 | FULL | Counter status register<br>Note:DT_CNT_H is not available for this register |
| TCPWM1_GRP0_CNT4_COUNTER | 0x40580208 | FULL | Counter count register |
| TCPWM1_GRP0_CNT4_CC0 | 0x40580210 | FULL | Counter compare/capture 0 register |
| TCPWM1_GRP0_CNT4_CC0_BUFF | 0x40580214 | FULL | Counter buffered compare/capture 0 register |
| TCPWM1_GRP0_CNT4_CC1 | 0x40580218 | FULL | Counter compare/capture 1 register |
| TCPWM1_GRP0_CNT4_CC1_BUFF | 0x4058021C | FULL | Counter buffered compare/capture 1 register |
| TCPWM1_GRP0_CNT4_PERIOD | 0x40580220 | FULL | Counter period register |
| TCPWM1_GRP0_CNT4_PERIOD_BUFF | 0x40580224 | FULL | Counter buffered period register |
| TCPWM1_GRP0_CNT4_DT | 0x40580230 | FULL | Counter PWM dead time register<br>Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM1_GRP0_CNT4_TR_CMD | 0x40580240 | FULL | Counter trigger command register |
| TCPWM1_GRP0_CNT4_TR_IN_SEL0 | 0x40580244 | FULL | Counter input trigger selection register 0 |
| TCPWM1_GRP0_CNT4_TR_IN_SEL1 | 0x40580248 | FULL | Counter input trigger selection register 1 |
| TCPWM1_GRP0_CNT4_TR_IN_EDGE_SEL | 0x4058024C | FULL | Counter input trigger edge selection register |
| TCPWM1_GRP0_CNT4_TR_PWM_CTRL | 0x40580250 | FULL | Counter trigger PWM control register |
| TCPWM1_GRP0_CNT4_TR_OUT_SEL | 0x40580254 | FULL | Counter output trigger selection register |
| TCPWM1_GRP0_CNT4_INTR | 0x40580270 | FULL | Interrupt request register |
| TCPWM1_GRP0_CNT4_INTR_SET | 0x40580274 | FULL | Interrupt set request register |
| TCPWM1_GRP0_CNT4_INTR_MASK | 0x40580278 | FULL | Interrupt mask register |
| TCPWM1_GRP0_CNT4_INTR_MASKED | 0x4058027C | FULL | Interrupt masked request register |

### 33.2.1.6 CNT 5

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT5_CTRL | 0x40580280 | FULL | Counter control register<br>Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM1_GRP0_CNT5_STATUS | 0x40580284 | FULL | Counter status register<br>Note:DT_CNT_H is not available for this register |
| TCPWM1_GRP0_CNT5_COUNTER | 0x40580288 | FULL | Counter count register |
| TCPWM1_GRP0_CNT5_CC0 | 0x40580290 | FULL | Counter compare/capture 0 register |
| TCPWM1_GRP0_CNT5_CC0_BUFF | 0x40580294 | FULL | Counter buffered compare/capture 0 register |
| TCPWM1_GRP0_CNT5_CC1 | 0x40580298 | FULL | Counter compare/capture 1 register |
| TCPWM1_GRP0_CNT5_CC1_BUFF | 0x4058029C | FULL | Counter buffered compare/capture 1 register |
| TCPWM1_GRP0_CNT5_PERIOD | 0x405802A0 | FULL | Counter period register |
| TCPWM1_GRP0_CNT5_PERIOD_BUFF | 0x405802A4 | FULL | Counter buffered period register |
| TCPWM1_GRP0_CNT5_DT | 0x405802B0 | FULL | Counter PWM dead time register<br>Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM1_GRP0_CNT5_TR_CMD | 0x405802C0 | FULL | Counter trigger command register |
| TCPWM1_GRP0_CNT5_TR_IN_SEL0 | 0x405802C4 | FULL | Counter input trigger selection register 0 |
| TCPWM1_GRP0_CNT5_TR_IN_SEL1 | 0x405802C8 | FULL | Counter input trigger selection register 1 |
| TCPWM1_GRP0_CNT5_TR_IN_EDGE_SEL | 0x405802CC | FULL | Counter input trigger edge selection register |
| TCPWM1_GRP0_CNT5_TR_PWM_CTRL | 0x405802D0 | FULL | Counter trigger PWM control register |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT5_TR_OUT_SEL | 0x405802D4 | FULL | Counter output trigger selection register |
| TCPWM1_GRP0_CNT5_INTR | 0x405802F0 | FULL | Interrupt request register |
| TCPWM1_GRP0_CNT5_INTR_SET | 0x405802F4 | FULL | Interrupt set request register |
| TCPWM1_GRP0_CNT5_INTR_MASK | 0x405802F8 | FULL | Interrupt mask register |
| TCPWM1_GRP0_CNT5_INTR_MASKED | 0x405802FC | FULL | Interrupt masked request register |

### 33.2.1.7 CNT 6

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT6_CTRL | 0x40580300 | FULL | Counter control register<br>Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM1_GRP0_CNT6_STATUS | 0x40580304 | FULL | Counter status register<br>Note:DT_CNT_H is not available for this register |
| TCPWM1_GRP0_CNT6_COUNTER | 0x40580308 | FULL | Counter count register |
| TCPWM1_GRP0_CNT6_CC0 | 0x40580310 | FULL | Counter compare/capture 0 register |
| TCPWM1_GRP0_CNT6_CC0_BUFF | 0x40580314 | FULL | Counter buffered compare/capture 0 register |
| TCPWM1_GRP0_CNT6_CC1 | 0x40580318 | FULL | Counter compare/capture 1 register |
| TCPWM1_GRP0_CNT6_CC1_BUFF | 0x4058031C | FULL | Counter buffered compare/capture 1 register |
| TCPWM1_GRP0_CNT6_PERIOD | 0x40580320 | FULL | Counter period register |
| TCPWM1_GRP0_CNT6_PERIOD_BUFF | 0x40580324 | FULL | Counter buffered period register |
| TCPWM1_GRP0_CNT6_DT | 0x40580330 | FULL | Counter PWM dead time register<br>Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM1_GRP0_CNT6_TR_CMD | 0x40580340 | FULL | Counter trigger command register |
| TCPWM1_GRP0_CNT6_TR_IN_SEL0 | 0x40580344 | FULL | Counter input trigger selection register 0 |
| TCPWM1_GRP0_CNT6_TR_IN_SEL1 | 0x40580348 | FULL | Counter input trigger selection register 1 |
| TCPWM1_GRP0_CNT6_TR_IN_EDGE_SEL | 0x4058034C | FULL | Counter input trigger edge selection register |
| TCPWM1_GRP0_CNT6_TR_PWM_CTRL | 0x40580350 | FULL | Counter trigger PWM control register |
| TCPWM1_GRP0_CNT6_TR_OUT_SEL | 0x40580354 | FULL | Counter output trigger selection register |
| TCPWM1_GRP0_CNT6_INTR | 0x40580370 | FULL | Interrupt request register |
| TCPWM1_GRP0_CNT6_INTR_SET | 0x40580374 | FULL | Interrupt set request register |
| TCPWM1_GRP0_CNT6_INTR_MASK | 0x40580378 | FULL | Interrupt mask register |
| TCPWM1_GRP0_CNT6_INTR_MASKED | 0x4058037C | FULL | Interrupt masked request register |

### 33.2.1.8 CNT 7

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT7_CTRL | 0x40580380 | FULL | Counter control register<br>Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM1_GRP0_CNT7_STATUS | 0x40580384 | FULL | Counter status register<br>Note:DT_CNT_H is not available for this register |
| TCPWM1_GRP0_CNT7_COUNTER | 0x40580388 | FULL | Counter count register |
| TCPWM1_GRP0_CNT7_CC0 | 0x40580390 | FULL | Counter compare/capture 0 register |
| TCPWM1_GRP0_CNT7_CC0_BUFF | 0x40580394 | FULL | Counter buffered compare/capture 0 register |
| TCPWM1_GRP0_CNT7_CC1 | 0x40580398 | FULL | Counter compare/capture 1 register |
| TCPWM1_GRP0_CNT7_CC1_BUFF | 0x4058039C | FULL | Counter buffered compare/capture 1 register |
| TCPWM1_GRP0_CNT7_PERIOD | 0x405803A0 | FULL | Counter period register |
| TCPWM1_GRP0_CNT7_PERIOD_BUFF | 0x405803A4 | FULL | Counter buffered period register |
| TCPWM1_GRP0_CNT7_DT | 0x405803B0 | FULL | Counter PWM dead time register<br>Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM1_GRP0_CNT7_TR_CMD | 0x405803C0 | FULL | Counter trigger command register |
| TCPWM1_GRP0_CNT7_TR_IN_SEL0 | 0x405803C4 | FULL | Counter input trigger selection register 0 |
| TCPWM1_GRP0_CNT7_TR_IN_SEL1 | 0x405803C8 | FULL | Counter input trigger selection register 1 |
| TCPWM1_GRP0_CNT7_TR_IN_EDGE_SEL | 0x405803CC | FULL | Counter input trigger edge selection register |
| TCPWM1_GRP0_CNT7_TR_PWM_CTRL | 0x405803D0 | FULL | Counter trigger PWM control register |
| TCPWM1_GRP0_CNT7_TR_OUT_SEL | 0x405803D4 | FULL | Counter output trigger selection register |
| TCPWM1_GRP0_CNT7_INTR | 0x405803F0 | FULL | Interrupt request register |
| TCPWM1_GRP0_CNT7_INTR_SET | 0x405803F4 | FULL | Interrupt set request register |
| TCPWM1_GRP0_CNT7_INTR_MASK | 0x405803F8 | FULL | Interrupt mask register |
| TCPWM1_GRP0_CNT7_INTR_MASKED | 0x405803FC | FULL | Interrupt masked request register |

### 33.2.1.9 CNT 8

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT8_CTRL | 0x40580400 | FULL | Counter control register<br>Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM1_GRP0_CNT8_STATUS | 0x40580404 | FULL | Counter status register<br>Note:DT_CNT_H is not available for this register |
| TCPWM1_GRP0_CNT8_COUNTER | 0x40580408 | FULL | Counter count register |
| TCPWM1_GRP0_CNT8_CC0 | 0x40580410 | FULL | Counter compare/capture 0 register |
| TCPWM1_GRP0_CNT8_CC0_BUFF | 0x40580414 | FULL | Counter buffered compare/capture 0 register |
| TCPWM1_GRP0_CNT8_CC1 | 0x40580418 | FULL | Counter compare/capture 1 register |
| TCPWM1_GRP0_CNT8_CC1_BUFF | 0x4058041C | FULL | Counter buffered compare/capture 1 register |
| TCPWM1_GRP0_CNT8_PERIOD | 0x40580420 | FULL | Counter period register |
| TCPWM1_GRP0_CNT8_PERIOD_BUFF | 0x40580424 | FULL | Counter buffered period register |
| TCPWM1_GRP0_CNT8_DT | 0x40580430 | FULL | Counter PWM dead time register<br>Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM1_GRP0_CNT8_TR_CMD | 0x40580440 | FULL | Counter trigger command register |
| TCPWM1_GRP0_CNT8_TR_IN_SEL0 | 0x40580444 | FULL | Counter input trigger selection register 0 |
| TCPWM1_GRP0_CNT8_TR_IN_SEL1 | 0x40580448 | FULL | Counter input trigger selection register 1 |
| TCPWM1_GRP0_CNT8_TR_IN_EDGE_SEL | 0x4058044C | FULL | Counter input trigger edge selection register |
| TCPWM1_GRP0_CNT8_TR_PWM_CTRL | 0x40580450 | FULL | Counter trigger PWM control register |
| TCPWM1_GRP0_CNT8_TR_OUT_SEL | 0x40580454 | FULL | Counter output trigger selection register |
| TCPWM1_GRP0_CNT8_INTR | 0x40580470 | FULL | Interrupt request register |
| TCPWM1_GRP0_CNT8_INTR_SET | 0x40580474 | FULL | Interrupt set request register |
| TCPWM1_GRP0_CNT8_INTR_MASK | 0x40580478 | FULL | Interrupt mask register |
| TCPWM1_GRP0_CNT8_INTR_MASKED | 0x4058047C | FULL | Interrupt masked request register |

### 33.2.1.10 CNT 9

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT9_CTRL | 0x40580480 | FULL | Counter control register<br>Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM1_GRP0_CNT9_STATUS | 0x40580484 | FULL | Counter status register<br>Note:DT_CNT_H is not available for this register |
| TCPWM1_GRP0_CNT9_COUNTER | 0x40580488 | FULL | Counter count register |
| TCPWM1_GRP0_CNT9_CC0 | 0x40580490 | FULL | Counter compare/capture 0 register |
| TCPWM1_GRP0_CNT9_CC0_BUFF | 0x40580494 | FULL | Counter buffered compare/capture 0 register |
| TCPWM1_GRP0_CNT9_CC1 | 0x40580498 | FULL | Counter compare/capture 1 register |
| TCPWM1_GRP0_CNT9_CC1_BUFF | 0x4058049C | FULL | Counter buffered compare/capture 1 register |
| TCPWM1_GRP0_CNT9_PERIOD | 0x405804A0 | FULL | Counter period register |
| TCPWM1_GRP0_CNT9_PERIOD_BUFF | 0x405804A4 | FULL | Counter buffered period register |
| TCPWM1_GRP0_CNT9_DT | 0x405804B0 | FULL | Counter PWM dead time register<br>Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM1_GRP0_CNT9_TR_CMD | 0x405804C0 | FULL | Counter trigger command register |
| TCPWM1_GRP0_CNT9_TR_IN_SEL0 | 0x405804C4 | FULL | Counter input trigger selection register 0 |
| TCPWM1_GRP0_CNT9_TR_IN_SEL1 | 0x405804C8 | FULL | Counter input trigger selection register 1 |
| TCPWM1_GRP0_CNT9_TR_IN_EDGE_SEL | 0x405804CC | FULL | Counter input trigger edge selection register |
| TCPWM1_GRP0_CNT9_TR_PWM_CTRL | 0x405804D0 | FULL | Counter trigger PWM control register |
| TCPWM1_GRP0_CNT9_TR_OUT_SEL | 0x405804D4 | FULL | Counter output trigger selection register |
| TCPWM1_GRP0_CNT9_INTR | 0x405804F0 | FULL | Interrupt request register |
| TCPWM1_GRP0_CNT9_INTR_SET | 0x405804F4 | FULL | Interrupt set request register |
| TCPWM1_GRP0_CNT9_INTR_MASK | 0x405804F8 | FULL | Interrupt mask register |
| TCPWM1_GRP0_CNT9_INTR_MASKED | 0x405804FC | FULL | Interrupt masked request register |

### 33.2.1.11 CNT 10

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT10_CTRL | 0x40580500 | FULL | Counter control register<br>Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM1_GRP0_CNT10_STATUS | 0x40580504 | FULL | Counter status register<br>Note:DT_CNT_H is not available for this register |
| TCPWM1_GRP0_CNT10_COUNTER | 0x40580508 | FULL | Counter count register |
| TCPWM1_GRP0_CNT10_CC0 | 0x40580510 | FULL | Counter compare/capture 0 register |
| TCPWM1_GRP0_CNT10_CC0_BUFF | 0x40580514 | FULL | Counter buffered compare/capture 0 register |
| TCPWM1_GRP0_CNT10_CC1 | 0x40580518 | FULL | Counter compare/capture 1 register |
| TCPWM1_GRP0_CNT10_CC1_BUFF | 0x4058051C | FULL | Counter buffered compare/capture 1 register |
| TCPWM1_GRP0_CNT10_PERIOD | 0x40580520 | FULL | Counter period register |
| TCPWM1_GRP0_CNT10_PERIOD_BUFF | 0x40580524 | FULL | Counter buffered period register |
| TCPWM1_GRP0_CNT10_DT | 0x40580530 | FULL | Counter PWM dead time register<br>Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM1_GRP0_CNT10_TR_CMD | 0x40580540 | FULL | Counter trigger command register |
| TCPWM1_GRP0_CNT10_TR_IN_SEL0 | 0x40580544 | FULL | Counter input trigger selection register 0 |
| TCPWM1_GRP0_CNT10_TR_IN_SEL1 | 0x40580548 | FULL | Counter input trigger selection register 1 |
| TCPWM1_GRP0_CNT10_TR_IN_EDGE_SEL | 0x4058054C | FULL | Counter input trigger edge selection register |
| TCPWM1_GRP0_CNT10_TR_PWM_CTRL | 0x40580550 | FULL | Counter trigger PWM control register |
| TCPWM1_GRP0_CNT10_TR_OUT_SEL | 0x40580554 | FULL | Counter output trigger selection register |
| TCPWM1_GRP0_CNT10_INTR | 0x40580570 | FULL | Interrupt request register |
| TCPWM1_GRP0_CNT10_INTR_SET | 0x40580574 | FULL | Interrupt set request register |
| TCPWM1_GRP0_CNT10_INTR_MASK | 0x40580578 | FULL | Interrupt mask register |
| TCPWM1_GRP0_CNT10_INTR_MASKED | 0x4058057C | FULL | Interrupt masked request register |

### 33.2.1.12 CNT 11

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT11_CTRL | 0x40580580 | FULL | Counter control register<br>Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM1_GRP0_CNT11_STATUS | 0x40580584 | FULL | Counter status register<br>Note:DT_CNT_H is not available for this register |
| TCPWM1_GRP0_CNT11_COUNTER | 0x40580588 | FULL | Counter count register |
| TCPWM1_GRP0_CNT11_CC0 | 0x40580590 | FULL | Counter compare/capture 0 register |
| TCPWM1_GRP0_CNT11_CC0_BUFF | 0x40580594 | FULL | Counter buffered compare/capture 0 register |
| TCPWM1_GRP0_CNT11_CC1 | 0x40580598 | FULL | Counter compare/capture 1 register |
| TCPWM1_GRP0_CNT11_CC1_BUFF | 0x4058059C | FULL | Counter buffered compare/capture 1 register |
| TCPWM1_GRP0_CNT11_PERIOD | 0x405805A0 | FULL | Counter period register |
| TCPWM1_GRP0_CNT11_PERIOD_BUFF | 0x405805A4 | FULL | Counter buffered period register |
| TCPWM1_GRP0_CNT11_DT | 0x405805B0 | FULL | Counter PWM dead time register<br>Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM1_GRP0_CNT11_TR_CMD | 0x405805C0 | FULL | Counter trigger command register |
| TCPWM1_GRP0_CNT11_TR_IN_SEL0 | 0x405805C4 | FULL | Counter input trigger selection register 0 |
| TCPWM1_GRP0_CNT11_TR_IN_SEL1 | 0x405805C8 | FULL | Counter input trigger selection register 1 |
| TCPWM1_GRP0_CNT11_TR_IN_EDGE_SEL | 0x405805CC | FULL | Counter input trigger edge selection register |
| TCPWM1_GRP0_CNT11_TR_PWM_CTRL | 0x405805D0 | FULL | Counter trigger PWM control register |
| TCPWM1_GRP0_CNT11_TR_OUT_SEL | 0x405805D4 | FULL | Counter output trigger selection register |
| TCPWM1_GRP0_CNT11_INTR | 0x405805F0 | FULL | Interrupt request register |
| TCPWM1_GRP0_CNT11_INTR_SET | 0x405805F4 | FULL | Interrupt set request register |
| TCPWM1_GRP0_CNT11_INTR_MASK | 0x405805F8 | FULL | Interrupt mask register |
| TCPWM1_GRP0_CNT11_INTR_MASKED | 0x405805FC | FULL | Interrupt masked request register |

### 33.2.1.13 CNT 12

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT12_CTRL | 0x40580600 | FULL | Counter control register<br>Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT12_STATUS | 0x40580604 | FULL | Counter status register<br>Note:DT_CNT_H is not available for this register |
| TCPWM1_GRP0_CNT12_COUNTER | 0x40580608 | FULL | Counter count register |
| TCPWM1_GRP0_CNT12_CC0 | 0x40580610 | FULL | Counter compare/capture 0 register |
| TCPWM1_GRP0_CNT12_CC0_BUFF | 0x40580614 | FULL | Counter buffered compare/capture 0 register |
| TCPWM1_GRP0_CNT12_CC1 | 0x40580618 | FULL | Counter compare/capture 1 register |
| TCPWM1_GRP0_CNT12_CC1_BUFF | 0x4058061C | FULL | Counter buffered compare/capture 1 register |
| TCPWM1_GRP0_CNT12_PERIOD | 0x40580620 | FULL | Counter period register |
| TCPWM1_GRP0_CNT12_PERIOD_BUFF | 0x40580624 | FULL | Counter buffered period register |
| TCPWM1_GRP0_CNT12_DT | 0x40580630 | FULL | Counter PWM dead time register<br>Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM1_GRP0_CNT12_TR_CMD | 0x40580640 | FULL | Counter trigger command register |
| TCPWM1_GRP0_CNT12_TR_IN_SEL0 | 0x40580644 | FULL | Counter input trigger selection register 0 |
| TCPWM1_GRP0_CNT12_TR_IN_SEL1 | 0x40580648 | FULL | Counter input trigger selection register 1 |
| TCPWM1_GRP0_CNT12_TR_IN_EDGE_SEL | 0x4058064C | FULL | Counter input trigger edge selection register |
| TCPWM1_GRP0_CNT12_TR_PWM_CTRL | 0x40580650 | FULL | Counter trigger PWM control register |
| TCPWM1_GRP0_CNT12_TR_OUT_SEL | 0x40580654 | FULL | Counter output trigger selection register |
| TCPWM1_GRP0_CNT12_INTR | 0x40580670 | FULL | Interrupt request register |
| TCPWM1_GRP0_CNT12_INTR_SET | 0x40580674 | FULL | Interrupt set request register |
| TCPWM1_GRP0_CNT12_INTR_MASK | 0x40580678 | FULL | Interrupt mask register |
| TCPWM1_GRP0_CNT12_INTR_MASKED | 0x4058067C | FULL | Interrupt masked request register |

### 33.2.1.14 CNT 13

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT13_CTRL | 0x40580680 | FULL | Counter control register<br>Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM1_GRP0_CNT13_STATUS | 0x40580684 | FULL | Counter status register<br>Note:DT_CNT_H is not available for this register |
| TCPWM1_GRP0_CNT13_COUNTER | 0x40580688 | FULL | Counter count register |
| TCPWM1_GRP0_CNT13_CC0 | 0x40580690 | FULL | Counter compare/capture 0 register |
| TCPWM1_GRP0_CNT13_CC0_BUFF | 0x40580694 | FULL | Counter buffered compare/capture 0 register |
| TCPWM1_GRP0_CNT13_CC1 | 0x40580698 | FULL | Counter compare/capture 1 register |
| TCPWM1_GRP0_CNT13_CC1_BUFF | 0x4058069C | FULL | Counter buffered compare/capture 1 register |
| TCPWM1_GRP0_CNT13_PERIOD | 0x405806A0 | FULL | Counter period register |
| TCPWM1_GRP0_CNT13_PERIOD_BUFF | 0x405806A4 | FULL | Counter buffered period register |
| TCPWM1_GRP0_CNT13_DT | 0x405806B0 | FULL | Counter PWM dead time register<br>Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM1_GRP0_CNT13_TR_CMD | 0x405806C0 | FULL | Counter trigger command register |
| TCPWM1_GRP0_CNT13_TR_IN_SEL0 | 0x405806C4 | FULL | Counter input trigger selection register 0 |
| TCPWM1_GRP0_CNT13_TR_IN_SEL1 | 0x405806C8 | FULL | Counter input trigger selection register 1 |
| TCPWM1_GRP0_CNT13_TR_IN_EDGE_SEL | 0x405806CC | FULL | Counter input trigger edge selection register |
| TCPWM1_GRP0_CNT13_TR_PWM_CTRL | 0x405806D0 | FULL | Counter trigger PWM control register |
| TCPWM1_GRP0_CNT13_TR_OUT_SEL | 0x405806D4 | FULL | Counter output trigger selection register |
| TCPWM1_GRP0_CNT13_INTR | 0x405806F0 | FULL | Interrupt request register |
| TCPWM1_GRP0_CNT13_INTR_SET | 0x405806F4 | FULL | Interrupt set request register |
| TCPWM1_GRP0_CNT13_INTR_MASK | 0x405806F8 | FULL | Interrupt mask register |
| TCPWM1_GRP0_CNT13_INTR_MASKED | 0x405806FC | FULL | Interrupt masked request register |

### 33.2.1.15 CNT 14

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT14_CTRL | 0x40580700 | FULL | Counter control register<br>Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM1_GRP0_CNT14_STATUS | 0x40580704 | FULL | Counter status register<br>Note:DT_CNT_H is not available for this register |
| TCPWM1_GRP0_CNT14_COUNTER | 0x40580708 | FULL | Counter count register |
| TCPWM1_GRP0_CNT14_CC0 | 0x40580710 | FULL | Counter compare/capture 0 register |
| TCPWM1_GRP0_CNT14_CC0_BUFF | 0x40580714 | FULL | Counter buffered compare/capture 0 register |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT14_CC1 | 0x40580718 | FULL | Counter compare/capture 1 register |
| TCPWM1_GRP0_CNT14_CC1_BUFF | 0x4058071C | FULL | Counter buffered compare/capture 1 register |
| TCPWM1_GRP0_CNT14_PERIOD | 0x40580720 | FULL | Counter period register |
| TCPWM1_GRP0_CNT14_PERIOD_BUFF | 0x40580724 | FULL | Counter buffered period register |
| TCPWM1_GRP0_CNT14_DT | 0x40580730 | FULL | Counter PWM dead time register Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM1_GRP0_CNT14_TR_CMD | 0x40580740 | FULL | Counter trigger command register |
| TCPWM1_GRP0_CNT14_TR_IN_SEL0 | 0x40580744 | FULL | Counter input trigger selection register 0 |
| TCPWM1_GRP0_CNT14_TR_IN_SEL1 | 0x40580748 | FULL | Counter input trigger selection register 1 |
| TCPWM1_GRP0_CNT14_TR_IN_EDGE_SEL | 0x4058074C | FULL | Counter input trigger edge selection register |
| TCPWM1_GRP0_CNT14_TR_PWM_CTRL | 0x40580750 | FULL | Counter trigger PWM control register |
| TCPWM1_GRP0_CNT14_TR_OUT_SEL | 0x40580754 | FULL | Counter output trigger selection register |
| TCPWM1_GRP0_CNT14_INTR | 0x40580770 | FULL | Interrupt request register |
| TCPWM1_GRP0_CNT14_INTR_SET | 0x40580774 | FULL | Interrupt set request register |
| TCPWM1_GRP0_CNT14_INTR_MASK | 0x40580778 | FULL | Interrupt mask register |
| TCPWM1_GRP0_CNT14_INTR_MASKED | 0x4058077C | FULL | Interrupt masked request register |

### 33.2.1.16 CNT 15

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT15_CTRL | 0x40580780 | FULL | Counter control register Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM1_GRP0_CNT15_STATUS | 0x40580784 | FULL | Counter status register Note:DT_CNT_H is not available for this register |
| TCPWM1_GRP0_CNT15_COUNTER | 0x40580788 | FULL | Counter count register |
| TCPWM1_GRP0_CNT15_CC0 | 0x40580790 | FULL | Counter compare/capture 0 register |
| TCPWM1_GRP0_CNT15_CC0_BUFF | 0x40580794 | FULL | Counter buffered compare/capture 0 register |
| TCPWM1_GRP0_CNT15_CC1 | 0x40580798 | FULL | Counter compare/capture 1 register |
| TCPWM1_GRP0_CNT15_CC1_BUFF | 0x4058079C | FULL | Counter buffered compare/capture 1 register |
| TCPWM1_GRP0_CNT15_PERIOD | 0x405807A0 | FULL | Counter period register |
| TCPWM1_GRP0_CNT15_PERIOD_BUFF | 0x405807A4 | FULL | Counter buffered period register |
| TCPWM1_GRP0_CNT15_DT | 0x405807B0 | FULL | Counter PWM dead time register Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM1_GRP0_CNT15_TR_CMD | 0x405807C0 | FULL | Counter trigger command register |
| TCPWM1_GRP0_CNT15_TR_IN_SEL0 | 0x405807C4 | FULL | Counter input trigger selection register 0 |
| TCPWM1_GRP0_CNT15_TR_IN_SEL1 | 0x405807C8 | FULL | Counter input trigger selection register 1 |
| TCPWM1_GRP0_CNT15_TR_IN_EDGE_SEL | 0x405807CC | FULL | Counter input trigger edge selection register |
| TCPWM1_GRP0_CNT15_TR_PWM_CTRL | 0x405807D0 | FULL | Counter trigger PWM control register |
| TCPWM1_GRP0_CNT15_TR_OUT_SEL | 0x405807D4 | FULL | Counter output trigger selection register |
| TCPWM1_GRP0_CNT15_INTR | 0x405807F0 | FULL | Interrupt request register |
| TCPWM1_GRP0_CNT15_INTR_SET | 0x405807F4 | FULL | Interrupt set request register |
| TCPWM1_GRP0_CNT15_INTR_MASK | 0x405807F8 | FULL | Interrupt mask register |
| TCPWM1_GRP0_CNT15_INTR_MASKED | 0x405807FC | FULL | Interrupt masked request register |

### 33.2.1.17 CNT 16

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT16_CTRL | 0x40580800 | FULL | Counter control register Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM1_GRP0_CNT16_STATUS | 0x40580804 | FULL | Counter status register Note:DT_CNT_H is not available for this register |
| TCPWM1_GRP0_CNT16_COUNTER | 0x40580808 | FULL | Counter count register |
| TCPWM1_GRP0_CNT16_CC0 | 0x40580810 | FULL | Counter compare/capture 0 register |
| TCPWM1_GRP0_CNT16_CC0_BUFF | 0x40580814 | FULL | Counter buffered compare/capture 0 register |
| TCPWM1_GRP0_CNT16_CC1 | 0x40580818 | FULL | Counter compare/capture 1 register |
| TCPWM1_GRP0_CNT16_CC1_BUFF | 0x4058081C | FULL | Counter buffered compare/capture 1 register |
| TCPWM1_GRP0_CNT16_PERIOD | 0x40580820 | FULL | Counter period register |
| TCPWM1_GRP0_CNT16_PERIOD_BUFF | 0x40580824 | FULL | Counter buffered period register |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT16_DT | 0x40580830 | FULL | Counter PWM dead time register<br>Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM1_GRP0_CNT16_TR_CMD | 0x40580840 | FULL | Counter trigger command register |
| TCPWM1_GRP0_CNT16_TR_IN_SEL0 | 0x40580844 | FULL | Counter input trigger selection register 0 |
| TCPWM1_GRP0_CNT16_TR_IN_SEL1 | 0x40580848 | FULL | Counter input trigger selection register 1 |
| TCPWM1_GRP0_CNT16_TR_IN_EDGE_SEL | 0x4058084C | FULL | Counter input trigger edge selection register |
| TCPWM1_GRP0_CNT16_TR_PWM_CTRL | 0x40580850 | FULL | Counter trigger PWM control register |
| TCPWM1_GRP0_CNT16_TR_OUT_SEL | 0x40580854 | FULL | Counter output trigger selection register |
| TCPWM1_GRP0_CNT16_INTR | 0x40580870 | FULL | Interrupt request register |
| TCPWM1_GRP0_CNT16_INTR_SET | 0x40580874 | FULL | Interrupt set request register |
| TCPWM1_GRP0_CNT16_INTR_MASK | 0x40580878 | FULL | Interrupt mask register |
| TCPWM1_GRP0_CNT16_INTR_MASKED | 0x4058087C | FULL | Interrupt masked request register |

### 33.2.1.18 CNT 17

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT17_CTRL | 0x40580880 | FULL | Counter control register<br>Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM1_GRP0_CNT17_STATUS | 0x40580884 | FULL | Counter status register<br>Note:DT_CNT_H is not available for this register |
| TCPWM1_GRP0_CNT17_COUNTER | 0x40580888 | FULL | Counter count register |
| TCPWM1_GRP0_CNT17_CC0 | 0x40580890 | FULL | Counter compare/capture 0 register |
| TCPWM1_GRP0_CNT17_CC0_BUFF | 0x40580894 | FULL | Counter buffered compare/capture 0 register |
| TCPWM1_GRP0_CNT17_CC1 | 0x40580898 | FULL | Counter compare/capture 1 register |
| TCPWM1_GRP0_CNT17_CC1_BUFF | 0x4058089C | FULL | Counter buffered compare/capture 1 register |
| TCPWM1_GRP0_CNT17_PERIOD | 0x405808A0 | FULL | Counter period register |
| TCPWM1_GRP0_CNT17_PERIOD_BUFF | 0x405808A4 | FULL | Counter buffered period register |
| TCPWM1_GRP0_CNT17_DT | 0x405808B0 | FULL | Counter PWM dead time register<br>Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM1_GRP0_CNT17_TR_CMD | 0x405808C0 | FULL | Counter trigger command register |
| TCPWM1_GRP0_CNT17_TR_IN_SEL0 | 0x405808C4 | FULL | Counter input trigger selection register 0 |
| TCPWM1_GRP0_CNT17_TR_IN_SEL1 | 0x405808C8 | FULL | Counter input trigger selection register 1 |
| TCPWM1_GRP0_CNT17_TR_IN_EDGE_SEL | 0x405808CC | FULL | Counter input trigger edge selection register |
| TCPWM1_GRP0_CNT17_TR_PWM_CTRL | 0x405808D0 | FULL | Counter trigger PWM control register |
| TCPWM1_GRP0_CNT17_TR_OUT_SEL | 0x405808D4 | FULL | Counter output trigger selection register |
| TCPWM1_GRP0_CNT17_INTR | 0x405808F0 | FULL | Interrupt request register |
| TCPWM1_GRP0_CNT17_INTR_SET | 0x405808F4 | FULL | Interrupt set request register |
| TCPWM1_GRP0_CNT17_INTR_MASK | 0x405808F8 | FULL | Interrupt mask register |
| TCPWM1_GRP0_CNT17_INTR_MASKED | 0x405808FC | FULL | Interrupt masked request register |

### 33.2.1.19 CNT 18

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT18_CTRL | 0x40580900 | FULL | Counter control register<br>Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM1_GRP0_CNT18_STATUS | 0x40580904 | FULL | Counter status register<br>Note:DT_CNT_H is not available for this register |
| TCPWM1_GRP0_CNT18_COUNTER | 0x40580908 | FULL | Counter count register |
| TCPWM1_GRP0_CNT18_CC0 | 0x40580910 | FULL | Counter compare/capture 0 register |
| TCPWM1_GRP0_CNT18_CC0_BUFF | 0x40580914 | FULL | Counter buffered compare/capture 0 register |
| TCPWM1_GRP0_CNT18_CC1 | 0x40580918 | FULL | Counter compare/capture 1 register |
| TCPWM1_GRP0_CNT18_CC1_BUFF | 0x4058091C | FULL | Counter buffered compare/capture 1 register |
| TCPWM1_GRP0_CNT18_PERIOD | 0x40580920 | FULL | Counter period register |
| TCPWM1_GRP0_CNT18_PERIOD_BUFF | 0x40580924 | FULL | Counter buffered period register |
| TCPWM1_GRP0_CNT18_DT | 0x40580930 | FULL | Counter PWM dead time register<br>Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM1_GRP0_CNT18_TR_CMD | 0x40580940 | FULL | Counter trigger command register |
| TCPWM1_GRP0_CNT18_TR_IN_SEL0 | 0x40580944 | FULL | Counter input trigger selection register 0 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT18_TR_IN_SEL1 | 0x40580948 | FULL | Counter input trigger selection register 1 |
| TCPWM1_GRP0_CNT18_TR_IN_EDGE_SEL | 0x4058094C | FULL | Counter input trigger edge selection register |
| TCPWM1_GRP0_CNT18_TR_PWM_CTRL | 0x40580950 | FULL | Counter trigger PWM control register |
| TCPWM1_GRP0_CNT18_TR_OUT_SEL | 0x40580954 | FULL | Counter output trigger selection register |
| TCPWM1_GRP0_CNT18_INTR | 0x40580970 | FULL | Interrupt request register |
| TCPWM1_GRP0_CNT18_INTR_SET | 0x40580974 | FULL | Interrupt set request register |
| TCPWM1_GRP0_CNT18_INTR_MASK | 0x40580978 | FULL | Interrupt mask register |
| TCPWM1_GRP0_CNT18_INTR_MASKED | 0x4058097C | FULL | Interrupt masked request register |

### 33.2.1.20 CNT 19

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT19_CTRL | 0x40580980 | FULL | Counter control register<br>Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM1_GRP0_CNT19_STATUS | 0x40580984 | FULL | Counter status register<br>Note:DT_CNT_H is not available for this register |
| TCPWM1_GRP0_CNT19_COUNTER | 0x40580988 | FULL | Counter count register |
| TCPWM1_GRP0_CNT19_CC0 | 0x40580990 | FULL | Counter compare/capture 0 register |
| TCPWM1_GRP0_CNT19_CC0_BUFF | 0x40580994 | FULL | Counter buffered compare/capture 0 register |
| TCPWM1_GRP0_CNT19_CC1 | 0x40580998 | FULL | Counter compare/capture 1 register |
| TCPWM1_GRP0_CNT19_CC1_BUFF | 0x4058099C | FULL | Counter buffered compare/capture 1 register |
| TCPWM1_GRP0_CNT19_PERIOD | 0x405809A0 | FULL | Counter period register |
| TCPWM1_GRP0_CNT19_PERIOD_BUFF | 0x405809A4 | FULL | Counter buffered period register |
| TCPWM1_GRP0_CNT19_DT | 0x405809B0 | FULL | Counter PWM dead time register<br>Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM1_GRP0_CNT19_TR_CMD | 0x405809C0 | FULL | Counter trigger command register |
| TCPWM1_GRP0_CNT19_TR_IN_SEL0 | 0x405809C4 | FULL | Counter input trigger selection register 0 |
| TCPWM1_GRP0_CNT19_TR_IN_SEL1 | 0x405809C8 | FULL | Counter input trigger selection register 1 |
| TCPWM1_GRP0_CNT19_TR_IN_EDGE_SEL | 0x405809CC | FULL | Counter input trigger edge selection register |
| TCPWM1_GRP0_CNT19_TR_PWM_CTRL | 0x405809D0 | FULL | Counter trigger PWM control register |
| TCPWM1_GRP0_CNT19_TR_OUT_SEL | 0x405809D4 | FULL | Counter output trigger selection register |
| TCPWM1_GRP0_CNT19_INTR | 0x405809F0 | FULL | Interrupt request register |
| TCPWM1_GRP0_CNT19_INTR_SET | 0x405809F4 | FULL | Interrupt set request register |
| TCPWM1_GRP0_CNT19_INTR_MASK | 0x405809F8 | FULL | Interrupt mask register |
| TCPWM1_GRP0_CNT19_INTR_MASKED | 0x405809FC | FULL | Interrupt masked request register |

### 33.2.1.21 CNT 20

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT20_CTRL | 0x40580A00 | FULL | Counter control register<br>Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM1_GRP0_CNT20_STATUS | 0x40580A04 | FULL | Counter status register<br>Note:DT_CNT_H is not available for this register |
| TCPWM1_GRP0_CNT20_COUNTER | 0x40580A08 | FULL | Counter count register |
| TCPWM1_GRP0_CNT20_CC0 | 0x40580A10 | FULL | Counter compare/capture 0 register |
| TCPWM1_GRP0_CNT20_CC0_BUFF | 0x40580A14 | FULL | Counter buffered compare/capture 0 register |
| TCPWM1_GRP0_CNT20_CC1 | 0x40580A18 | FULL | Counter compare/capture 1 register |
| TCPWM1_GRP0_CNT20_CC1_BUFF | 0x40580A1C | FULL | Counter buffered compare/capture 1 register |
| TCPWM1_GRP0_CNT20_PERIOD | 0x40580A20 | FULL | Counter period register |
| TCPWM1_GRP0_CNT20_PERIOD_BUFF | 0x40580A24 | FULL | Counter buffered period register |
| TCPWM1_GRP0_CNT20_DT | 0x40580A30 | FULL | Counter PWM dead time register<br>Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM1_GRP0_CNT20_TR_CMD | 0x40580A40 | FULL | Counter trigger command register |
| TCPWM1_GRP0_CNT20_TR_IN_SEL0 | 0x40580A44 | FULL | Counter input trigger selection register 0 |
| TCPWM1_GRP0_CNT20_TR_IN_SEL1 | 0x40580A48 | FULL | Counter input trigger selection register 1 |
| TCPWM1_GRP0_CNT20_TR_IN_EDGE_SEL | 0x40580A4C | FULL | Counter input trigger edge selection register |
| TCPWM1_GRP0_CNT20_TR_PWM_CTRL | 0x40580A50 | FULL | Counter trigger PWM control register |
| TCPWM1_GRP0_CNT20_TR_OUT_SEL | 0x40580A54 | FULL | Counter output trigger selection register |
| TCPWM1_GRP0_CNT20_INTR | 0x40580A70 | FULL | Interrupt request register |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT20_INTR_SET | 0x40580A74 | FULL | Interrupt set request register |
| TCPWM1_GRP0_CNT20_INTR_MASK | 0x40580A78 | FULL | Interrupt mask register |
| TCPWM1_GRP0_CNT20_INTR_MASKED | 0x40580A7C | FULL | Interrupt masked request register |

### 33.2.1.22 CNT 21

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT21_CTRL | 0x40580A80 | FULL | Counter control register<br>Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM1_GRP0_CNT21_STATUS | 0x40580A84 | FULL | Counter status register<br>Note:DT_CNT_H is not available for this register |
| TCPWM1_GRP0_CNT21_COUNTER | 0x40580A88 | FULL | Counter count register |
| TCPWM1_GRP0_CNT21_CC0 | 0x40580A90 | FULL | Counter compare/capture 0 register |
| TCPWM1_GRP0_CNT21_CC0_BUFF | 0x40580A94 | FULL | Counter buffered compare/capture 0 register |
| TCPWM1_GRP0_CNT21_CC1 | 0x40580A98 | FULL | Counter compare/capture 1 register |
| TCPWM1_GRP0_CNT21_CC1_BUFF | 0x40580A9C | FULL | Counter buffered compare/capture 1 register |
| TCPWM1_GRP0_CNT21_PERIOD | 0x40580AA0 | FULL | Counter period register |
| TCPWM1_GRP0_CNT21_PERIOD_BUFF | 0x40580AA4 | FULL | Counter buffered period register |
| TCPWM1_GRP0_CNT21_DT | 0x40580AB0 | FULL | Counter PWM dead time register<br>Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM1_GRP0_CNT21_TR_CMD | 0x40580AC0 | FULL | Counter trigger command register |
| TCPWM1_GRP0_CNT21_TR_IN_SEL0 | 0x40580AC4 | FULL | Counter input trigger selection register 0 |
| TCPWM1_GRP0_CNT21_TR_IN_SEL1 | 0x40580AC8 | FULL | Counter input trigger selection register 1 |
| TCPWM1_GRP0_CNT21_TR_IN_EDGE_SEL | 0x40580ACC | FULL | Counter input trigger edge selection register |
| TCPWM1_GRP0_CNT21_TR_PWM_CTRL | 0x40580AD0 | FULL | Counter trigger PWM control register |
| TCPWM1_GRP0_CNT21_TR_OUT_SEL | 0x40580AD4 | FULL | Counter output trigger selection register |
| TCPWM1_GRP0_CNT21_INTR | 0x40580AF0 | FULL | Interrupt request register |
| TCPWM1_GRP0_CNT21_INTR_SET | 0x40580AF4 | FULL | Interrupt set request register |
| TCPWM1_GRP0_CNT21_INTR_MASK | 0x40580AF8 | FULL | Interrupt mask register |
| TCPWM1_GRP0_CNT21_INTR_MASKED | 0x40580AFC | FULL | Interrupt masked request register |

### 33.2.1.23 CNT 22

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT22_CTRL | 0x40580B00 | FULL | Counter control register<br>Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM1_GRP0_CNT22_STATUS | 0x40580B04 | FULL | Counter status register<br>Note:DT_CNT_H is not available for this register |
| TCPWM1_GRP0_CNT22_COUNTER | 0x40580B08 | FULL | Counter count register |
| TCPWM1_GRP0_CNT22_CC0 | 0x40580B10 | FULL | Counter compare/capture 0 register |
| TCPWM1_GRP0_CNT22_CC0_BUFF | 0x40580B14 | FULL | Counter buffered compare/capture 0 register |
| TCPWM1_GRP0_CNT22_CC1 | 0x40580B18 | FULL | Counter compare/capture 1 register |
| TCPWM1_GRP0_CNT22_CC1_BUFF | 0x40580B1C | FULL | Counter buffered compare/capture 1 register |
| TCPWM1_GRP0_CNT22_PERIOD | 0x40580B20 | FULL | Counter period register |
| TCPWM1_GRP0_CNT22_PERIOD_BUFF | 0x40580B24 | FULL | Counter buffered period register |
| TCPWM1_GRP0_CNT22_DT | 0x40580B30 | FULL | Counter PWM dead time register<br>Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM1_GRP0_CNT22_TR_CMD | 0x40580B40 | FULL | Counter trigger command register |
| TCPWM1_GRP0_CNT22_TR_IN_SEL0 | 0x40580B44 | FULL | Counter input trigger selection register 0 |
| TCPWM1_GRP0_CNT22_TR_IN_SEL1 | 0x40580B48 | FULL | Counter input trigger selection register 1 |
| TCPWM1_GRP0_CNT22_TR_IN_EDGE_SEL | 0x40580B4C | FULL | Counter input trigger edge selection register |
| TCPWM1_GRP0_CNT22_TR_PWM_CTRL | 0x40580B50 | FULL | Counter trigger PWM control register |
| TCPWM1_GRP0_CNT22_TR_OUT_SEL | 0x40580B54 | FULL | Counter output trigger selection register |
| TCPWM1_GRP0_CNT22_INTR | 0x40580B70 | FULL | Interrupt request register |
| TCPWM1_GRP0_CNT22_INTR_SET | 0x40580B74 | FULL | Interrupt set request register |
| TCPWM1_GRP0_CNT22_INTR_MASK | 0x40580B78 | FULL | Interrupt mask register |
| TCPWM1_GRP0_CNT22_INTR_MASKED | 0x40580B7C | FULL | Interrupt masked request register |

### 33.2.1.24 CNT 23

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT23_CTRL | 0x40580B80 | FULL | Counter control register<br>Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM1_GRP0_CNT23_STATUS | 0x40580B84 | FULL | Counter status register<br>Note:DT_CNT_H is not available for this register |
| TCPWM1_GRP0_CNT23_COUNTER | 0x40580B88 | FULL | Counter count register |
| TCPWM1_GRP0_CNT23_CC0 | 0x40580B90 | FULL | Counter compare/capture 0 register |
| TCPWM1_GRP0_CNT23_CC0_BUFF | 0x40580B94 | FULL | Counter buffered compare/capture 0 register |
| TCPWM1_GRP0_CNT23_CC1 | 0x40580B98 | FULL | Counter compare/capture 1 register |
| TCPWM1_GRP0_CNT23_CC1_BUFF | 0x40580B9C | FULL | Counter buffered compare/capture 1 register |
| TCPWM1_GRP0_CNT23_PERIOD | 0x40580BA0 | FULL | Counter period register |
| TCPWM1_GRP0_CNT23_PERIOD_BUFF | 0x40580BA4 | FULL | Counter buffered period register |
| TCPWM1_GRP0_CNT23_DT | 0x40580BB0 | FULL | Counter PWM dead time register<br>Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM1_GRP0_CNT23_TR_CMD | 0x40580BC0 | FULL | Counter trigger command register |
| TCPWM1_GRP0_CNT23_TR_IN_SEL0 | 0x40580BC4 | FULL | Counter input trigger selection register 0 |
| TCPWM1_GRP0_CNT23_TR_IN_SEL1 | 0x40580BC8 | FULL | Counter input trigger selection register 1 |
| TCPWM1_GRP0_CNT23_TR_IN_EDGE_SEL | 0x40580BCC | FULL | Counter input trigger edge selection register |
| TCPWM1_GRP0_CNT23_TR_PWM_CTRL | 0x40580BD0 | FULL | Counter trigger PWM control register |
| TCPWM1_GRP0_CNT23_TR_OUT_SEL | 0x40580BD4 | FULL | Counter output trigger selection register |
| TCPWM1_GRP0_CNT23_INTR | 0x40580BF0 | FULL | Interrupt request register |
| TCPWM1_GRP0_CNT23_INTR_SET | 0x40580BF4 | FULL | Interrupt set request register |
| TCPWM1_GRP0_CNT23_INTR_MASK | 0x40580BF8 | FULL | Interrupt mask register |
| TCPWM1_GRP0_CNT23_INTR_MASKED | 0x40580BFC | FULL | Interrupt masked request register |

### 33.2.1.25 CNT 24

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT24_CTRL | 0x40580C00 | FULL | Counter control register<br>Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM1_GRP0_CNT24_STATUS | 0x40580C04 | FULL | Counter status register<br>Note:DT_CNT_H is not available for this register |
| TCPWM1_GRP0_CNT24_COUNTER | 0x40580C08 | FULL | Counter count register |
| TCPWM1_GRP0_CNT24_CC0 | 0x40580C10 | FULL | Counter compare/capture 0 register |
| TCPWM1_GRP0_CNT24_CC0_BUFF | 0x40580C14 | FULL | Counter buffered compare/capture 0 register |
| TCPWM1_GRP0_CNT24_CC1 | 0x40580C18 | FULL | Counter compare/capture 1 register |
| TCPWM1_GRP0_CNT24_CC1_BUFF | 0x40580C1C | FULL | Counter buffered compare/capture 1 register |
| TCPWM1_GRP0_CNT24_PERIOD | 0x40580C20 | FULL | Counter period register |
| TCPWM1_GRP0_CNT24_PERIOD_BUFF | 0x40580C24 | FULL | Counter buffered period register |
| TCPWM1_GRP0_CNT24_DT | 0x40580C30 | FULL | Counter PWM dead time register<br>Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM1_GRP0_CNT24_TR_CMD | 0x40580C40 | FULL | Counter trigger command register |
| TCPWM1_GRP0_CNT24_TR_IN_SEL0 | 0x40580C44 | FULL | Counter input trigger selection register 0 |
| TCPWM1_GRP0_CNT24_TR_IN_SEL1 | 0x40580C48 | FULL | Counter input trigger selection register 1 |
| TCPWM1_GRP0_CNT24_TR_IN_EDGE_SEL | 0x40580C4C | FULL | Counter input trigger edge selection register |
| TCPWM1_GRP0_CNT24_TR_PWM_CTRL | 0x40580C50 | FULL | Counter trigger PWM control register |
| TCPWM1_GRP0_CNT24_TR_OUT_SEL | 0x40580C54 | FULL | Counter output trigger selection register |
| TCPWM1_GRP0_CNT24_INTR | 0x40580C70 | FULL | Interrupt request register |
| TCPWM1_GRP0_CNT24_INTR_SET | 0x40580C74 | FULL | Interrupt set request register |
| TCPWM1_GRP0_CNT24_INTR_MASK | 0x40580C78 | FULL | Interrupt mask register |
| TCPWM1_GRP0_CNT24_INTR_MASKED | 0x40580C7C | FULL | Interrupt masked request register |

### 33.2.1.26 CNT 25

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT25_CTRL | 0x40580C80 | FULL | Counter control register<br>Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT25_STATUS | 0x40580C84 | FULL | Counter status register<br>Note:DT_CNT_H is not available for this register |
| TCPWM1_GRP0_CNT25_COUNTER | 0x40580C88 | FULL | Counter count register |
| TCPWM1_GRP0_CNT25_CC0 | 0x40580C90 | FULL | Counter compare/capture 0 register |
| TCPWM1_GRP0_CNT25_CC0_BUFF | 0x40580C94 | FULL | Counter buffered compare/capture 0 register |
| TCPWM1_GRP0_CNT25_CC1 | 0x40580C98 | FULL | Counter compare/capture 1 register |
| TCPWM1_GRP0_CNT25_CC1_BUFF | 0x40580C9C | FULL | Counter buffered compare/capture 1 register |
| TCPWM1_GRP0_CNT25_PERIOD | 0x40580CA0 | FULL | Counter period register |
| TCPWM1_GRP0_CNT25_PERIOD_BUFF | 0x40580CA4 | FULL | Counter buffered period register |
| TCPWM1_GRP0_CNT25_DT | 0x40580CB0 | FULL | Counter PWM dead time register<br>Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM1_GRP0_CNT25_TR_CMD | 0x40580CC0 | FULL | Counter trigger command register |
| TCPWM1_GRP0_CNT25_TR_IN_SEL0 | 0x40580CC4 | FULL | Counter input trigger selection register 0 |
| TCPWM1_GRP0_CNT25_TR_IN_SEL1 | 0x40580CC8 | FULL | Counter input trigger selection register 1 |
| TCPWM1_GRP0_CNT25_TR_IN_EDGE_SEL | 0x40580CCC | FULL | Counter input trigger edge selection register |
| TCPWM1_GRP0_CNT25_TR_PWM_CTRL | 0x40580CD0 | FULL | Counter trigger PWM control register |
| TCPWM1_GRP0_CNT25_TR_OUT_SEL | 0x40580CD4 | FULL | Counter output trigger selection register |
| TCPWM1_GRP0_CNT25_INTR | 0x40580CF0 | FULL | Interrupt request register |
| TCPWM1_GRP0_CNT25_INTR_SET | 0x40580CF4 | FULL | Interrupt set request register |
| TCPWM1_GRP0_CNT25_INTR_MASK | 0x40580CF8 | FULL | Interrupt mask register |
| TCPWM1_GRP0_CNT25_INTR_MASKED | 0x40580CFC | FULL | Interrupt masked request register |

### 33.2.1.27 CNT 26

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT26_CTRL | 0x40580D00 | FULL | Counter control register<br>Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM1_GRP0_CNT26_STATUS | 0x40580D04 | FULL | Counter status register<br>Note:DT_CNT_H is not available for this register |
| TCPWM1_GRP0_CNT26_COUNTER | 0x40580D08 | FULL | Counter count register |
| TCPWM1_GRP0_CNT26_CC0 | 0x40580D10 | FULL | Counter compare/capture 0 register |
| TCPWM1_GRP0_CNT26_CC0_BUFF | 0x40580D14 | FULL | Counter buffered compare/capture 0 register |
| TCPWM1_GRP0_CNT26_CC1 | 0x40580D18 | FULL | Counter compare/capture 1 register |
| TCPWM1_GRP0_CNT26_CC1_BUFF | 0x40580D1C | FULL | Counter buffered compare/capture 1 register |
| TCPWM1_GRP0_CNT26_PERIOD | 0x40580D20 | FULL | Counter period register |
| TCPWM1_GRP0_CNT26_PERIOD_BUFF | 0x40580D24 | FULL | Counter buffered period register |
| TCPWM1_GRP0_CNT26_DT | 0x40580D30 | FULL | Counter PWM dead time register<br>Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM1_GRP0_CNT26_TR_CMD | 0x40580D40 | FULL | Counter trigger command register |
| TCPWM1_GRP0_CNT26_TR_IN_SEL0 | 0x40580D44 | FULL | Counter input trigger selection register 0 |
| TCPWM1_GRP0_CNT26_TR_IN_SEL1 | 0x40580D48 | FULL | Counter input trigger selection register 1 |
| TCPWM1_GRP0_CNT26_TR_IN_EDGE_SEL | 0x40580D4C | FULL | Counter input trigger edge selection register |
| TCPWM1_GRP0_CNT26_TR_PWM_CTRL | 0x40580D50 | FULL | Counter trigger PWM control register |
| TCPWM1_GRP0_CNT26_TR_OUT_SEL | 0x40580D54 | FULL | Counter output trigger selection register |
| TCPWM1_GRP0_CNT26_INTR | 0x40580D70 | FULL | Interrupt request register |
| TCPWM1_GRP0_CNT26_INTR_SET | 0x40580D74 | FULL | Interrupt set request register |
| TCPWM1_GRP0_CNT26_INTR_MASK | 0x40580D78 | FULL | Interrupt mask register |
| TCPWM1_GRP0_CNT26_INTR_MASKED | 0x40580D7C | FULL | Interrupt masked request register |

### 33.2.1.28 CNT 27

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT27_CTRL | 0x40580D80 | FULL | Counter control register<br>Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM1_GRP0_CNT27_STATUS | 0x40580D84 | FULL | Counter status register<br>Note:DT_CNT_H is not available for this register |
| TCPWM1_GRP0_CNT27_COUNTER | 0x40580D88 | FULL | Counter count register |
| TCPWM1_GRP0_CNT27_CC0 | 0x40580D90 | FULL | Counter compare/capture 0 register |
| TCPWM1_GRP0_CNT27_CC0_BUFF | 0x40580D94 | FULL | Counter buffered compare/capture 0 register |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT27_CC1 | 0x40580D98 | FULL | Counter compare/capture 1 register |
| TCPWM1_GRP0_CNT27_CC1_BUFF | 0x40580D9C | FULL | Counter buffered compare/capture 1 register |
| TCPWM1_GRP0_CNT27_PERIOD | 0x40580DA0 | FULL | Counter period register |
| TCPWM1_GRP0_CNT27_PERIOD_BUFF | 0x40580DA4 | FULL | Counter buffered period register |
| TCPWM1_GRP0_CNT27_DT | 0x40580DB0 | FULL | Counter PWM dead time register<br>Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM1_GRP0_CNT27_TR_CMD | 0x40580DC0 | FULL | Counter trigger command register |
| TCPWM1_GRP0_CNT27_TR_IN_SEL0 | 0x40580DC4 | FULL | Counter input trigger selection register 0 |
| TCPWM1_GRP0_CNT27_TR_IN_SEL1 | 0x40580DC8 | FULL | Counter input trigger selection register 1 |
| TCPWM1_GRP0_CNT27_TR_IN_EDGE_SEL | 0x40580DCC | FULL | Counter input trigger edge selection register |
| TCPWM1_GRP0_CNT27_TR_PWM_CTRL | 0x40580DD0 | FULL | Counter trigger PWM control register |
| TCPWM1_GRP0_CNT27_TR_OUT_SEL | 0x40580DD4 | FULL | Counter output trigger selection register |
| TCPWM1_GRP0_CNT27_INTR | 0x40580DF0 | FULL | Interrupt request register |
| TCPWM1_GRP0_CNT27_INTR_SET | 0x40580DF4 | FULL | Interrupt set request register |
| TCPWM1_GRP0_CNT27_INTR_MASK | 0x40580DF8 | FULL | Interrupt mask register |
| TCPWM1_GRP0_CNT27_INTR_MASKED | 0x40580DFC | FULL | Interrupt masked request register |

### 33.2.1.29 CNT 28

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT28_CTRL | 0x40580E00 | FULL | Counter control register<br>Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM1_GRP0_CNT28_STATUS | 0x40580E04 | FULL | Counter status register<br>Note:DT_CNT_H is not available for this register |
| TCPWM1_GRP0_CNT28_COUNTER | 0x40580E08 | FULL | Counter count register |
| TCPWM1_GRP0_CNT28_CC0 | 0x40580E10 | FULL | Counter compare/capture 0 register |
| TCPWM1_GRP0_CNT28_CC0_BUFF | 0x40580E14 | FULL | Counter buffered compare/capture 0 register |
| TCPWM1_GRP0_CNT28_CC1 | 0x40580E18 | FULL | Counter compare/capture 1 register |
| TCPWM1_GRP0_CNT28_CC1_BUFF | 0x40580E1C | FULL | Counter buffered compare/capture 1 register |
| TCPWM1_GRP0_CNT28_PERIOD | 0x40580E20 | FULL | Counter period register |
| TCPWM1_GRP0_CNT28_PERIOD_BUFF | 0x40580E24 | FULL | Counter buffered period register |
| TCPWM1_GRP0_CNT28_DT | 0x40580E30 | FULL | Counter PWM dead time register<br>Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM1_GRP0_CNT28_TR_CMD | 0x40580E40 | FULL | Counter trigger command register |
| TCPWM1_GRP0_CNT28_TR_IN_SEL0 | 0x40580E44 | FULL | Counter input trigger selection register 0 |
| TCPWM1_GRP0_CNT28_TR_IN_SEL1 | 0x40580E48 | FULL | Counter input trigger selection register 1 |
| TCPWM1_GRP0_CNT28_TR_IN_EDGE_SEL | 0x40580E4C | FULL | Counter input trigger edge selection register |
| TCPWM1_GRP0_CNT28_TR_PWM_CTRL | 0x40580E50 | FULL | Counter trigger PWM control register |
| TCPWM1_GRP0_CNT28_TR_OUT_SEL | 0x40580E54 | FULL | Counter output trigger selection register |
| TCPWM1_GRP0_CNT28_INTR | 0x40580E70 | FULL | Interrupt request register |
| TCPWM1_GRP0_CNT28_INTR_SET | 0x40580E74 | FULL | Interrupt set request register |
| TCPWM1_GRP0_CNT28_INTR_MASK | 0x40580E78 | FULL | Interrupt mask register |
| TCPWM1_GRP0_CNT28_INTR_MASKED | 0x40580E7C | FULL | Interrupt masked request register |

### 33.2.1.30 CNT 29

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT29_CTRL | 0x40580E80 | FULL | Counter control register<br>Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM1_GRP0_CNT29_STATUS | 0x40580E84 | FULL | Counter status register<br>Note:DT_CNT_H is not available for this register |
| TCPWM1_GRP0_CNT29_COUNTER | 0x40580E88 | FULL | Counter count register |
| TCPWM1_GRP0_CNT29_CC0 | 0x40580E90 | FULL | Counter compare/capture 0 register |
| TCPWM1_GRP0_CNT29_CC0_BUFF | 0x40580E94 | FULL | Counter buffered compare/capture 0 register |
| TCPWM1_GRP0_CNT29_CC1 | 0x40580E98 | FULL | Counter compare/capture 1 register |
| TCPWM1_GRP0_CNT29_CC1_BUFF | 0x40580E9C | FULL | Counter buffered compare/capture 1 register |
| TCPWM1_GRP0_CNT29_PERIOD | 0x40580EA0 | FULL | Counter period register |
| TCPWM1_GRP0_CNT29_PERIOD_BUFF | 0x40580EA4 | FULL | Counter buffered period register |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT29_DT | 0x40580EB0 | FULL | Counter PWM dead time register<br>Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM1_GRP0_CNT29_TR_CMD | 0x40580EC0 | FULL | Counter trigger command register |
| TCPWM1_GRP0_CNT29_TR_IN_SEL0 | 0x40580EC4 | FULL | Counter input trigger selection register 0 |
| TCPWM1_GRP0_CNT29_TR_IN_SEL1 | 0x40580EC8 | FULL | Counter input trigger selection register 1 |
| TCPWM1_GRP0_CNT29_TR_IN_EDGE_SEL | 0x40580ECC | FULL | Counter input trigger edge selection register |
| TCPWM1_GRP0_CNT29_TR_PWM_CTRL | 0x40580ED0 | FULL | Counter trigger PWM control register |
| TCPWM1_GRP0_CNT29_TR_OUT_SEL | 0x40580ED4 | FULL | Counter output trigger selection register |
| TCPWM1_GRP0_CNT29_INTR | 0x40580EF0 | FULL | Interrupt request register |
| TCPWM1_GRP0_CNT29_INTR_SET | 0x40580EF4 | FULL | Interrupt set request register |
| TCPWM1_GRP0_CNT29_INTR_MASK | 0x40580EF8 | FULL | Interrupt mask register |
| TCPWM1_GRP0_CNT29_INTR_MASKED | 0x40580EFC | FULL | Interrupt masked request register |

### 33.2.1.31 CNT 30

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT30_CTRL | 0x40580F00 | FULL | Counter control register<br>Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM1_GRP0_CNT30_STATUS | 0x40580F04 | FULL | Counter status register<br>Note:DT_CNT_H is not available for this register |
| TCPWM1_GRP0_CNT30_COUNTER | 0x40580F08 | FULL | Counter count register |
| TCPWM1_GRP0_CNT30_CC0 | 0x40580F10 | FULL | Counter compare/capture 0 register |
| TCPWM1_GRP0_CNT30_CC0_BUFF | 0x40580F14 | FULL | Counter buffered compare/capture 0 register |
| TCPWM1_GRP0_CNT30_CC1 | 0x40580F18 | FULL | Counter compare/capture 1 register |
| TCPWM1_GRP0_CNT30_CC1_BUFF | 0x40580F1C | FULL | Counter buffered compare/capture 1 register |
| TCPWM1_GRP0_CNT30_PERIOD | 0x40580F20 | FULL | Counter period register |
| TCPWM1_GRP0_CNT30_PERIOD_BUFF | 0x40580F24 | FULL | Counter buffered period register |
| TCPWM1_GRP0_CNT30_DT | 0x40580F30 | FULL | Counter PWM dead time register<br>Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM1_GRP0_CNT30_TR_CMD | 0x40580F40 | FULL | Counter trigger command register |
| TCPWM1_GRP0_CNT30_TR_IN_SEL0 | 0x40580F44 | FULL | Counter input trigger selection register 0 |
| TCPWM1_GRP0_CNT30_TR_IN_SEL1 | 0x40580F48 | FULL | Counter input trigger selection register 1 |
| TCPWM1_GRP0_CNT30_TR_IN_EDGE_SEL | 0x40580F4C | FULL | Counter input trigger edge selection register |
| TCPWM1_GRP0_CNT30_TR_PWM_CTRL | 0x40580F50 | FULL | Counter trigger PWM control register |
| TCPWM1_GRP0_CNT30_TR_OUT_SEL | 0x40580F54 | FULL | Counter output trigger selection register |
| TCPWM1_GRP0_CNT30_INTR | 0x40580F70 | FULL | Interrupt request register |
| TCPWM1_GRP0_CNT30_INTR_SET | 0x40580F74 | FULL | Interrupt set request register |
| TCPWM1_GRP0_CNT30_INTR_MASK | 0x40580F78 | FULL | Interrupt mask register |
| TCPWM1_GRP0_CNT30_INTR_MASKED | 0x40580F7C | FULL | Interrupt masked request register |

### 33.2.1.32 CNT 31

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT31_CTRL | 0x40580F80 | FULL | Counter control register<br>Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM1_GRP0_CNT31_STATUS | 0x40580F84 | FULL | Counter status register<br>Note:DT_CNT_H is not available for this register |
| TCPWM1_GRP0_CNT31_COUNTER | 0x40580F88 | FULL | Counter count register |
| TCPWM1_GRP0_CNT31_CC0 | 0x40580F90 | FULL | Counter compare/capture 0 register |
| TCPWM1_GRP0_CNT31_CC0_BUFF | 0x40580F94 | FULL | Counter buffered compare/capture 0 register |
| TCPWM1_GRP0_CNT31_CC1 | 0x40580F98 | FULL | Counter compare/capture 1 register |
| TCPWM1_GRP0_CNT31_CC1_BUFF | 0x40580F9C | FULL | Counter buffered compare/capture 1 register |
| TCPWM1_GRP0_CNT31_PERIOD | 0x40580FA0 | FULL | Counter period register |
| TCPWM1_GRP0_CNT31_PERIOD_BUFF | 0x40580FA4 | FULL | Counter buffered period register |
| TCPWM1_GRP0_CNT31_DT | 0x40580FB0 | FULL | Counter PWM dead time register<br>Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM1_GRP0_CNT31_TR_CMD | 0x40580FC0 | FULL | Counter trigger command register |
| TCPWM1_GRP0_CNT31_TR_IN_SEL0 | 0x40580FC4 | FULL | Counter input trigger selection register 0 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT31_TR_IN_SEL1 | 0x40580FC8 | FULL | Counter input trigger selection register 1 |
| TCPWM1_GRP0_CNT31_TR_IN_EDGE_SEL | 0x40580FCC | FULL | Counter input trigger edge selection register |
| TCPWM1_GRP0_CNT31_TR_PWM_CTRL | 0x40580FD0 | FULL | Counter trigger PWM control register |
| TCPWM1_GRP0_CNT31_TR_OUT_SEL | 0x40580FD4 | FULL | Counter output trigger selection register |
| TCPWM1_GRP0_CNT31_INTR | 0x40580FF0 | FULL | Interrupt request register |
| TCPWM1_GRP0_CNT31_INTR_SET | 0x40580FF4 | FULL | Interrupt set request register |
| TCPWM1_GRP0_CNT31_INTR_MASK | 0x40580FF8 | FULL | Interrupt mask register |
| TCPWM1_GRP0_CNT31_INTR_MASKED | 0x40580FFC | FULL | Interrupt masked request register |

### 33.2.1.33 CNT 32

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT32_CTRL | 0x40581000 | FULL | Counter control register<br>Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM1_GRP0_CNT32_STATUS | 0x40581004 | FULL | Counter status register<br>Note:DT_CNT_H is not available for this register |
| TCPWM1_GRP0_CNT32_COUNTER | 0x40581008 | FULL | Counter count register |
| TCPWM1_GRP0_CNT32_CC0 | 0x40581010 | FULL | Counter compare/capture 0 register |
| TCPWM1_GRP0_CNT32_CC0_BUFF | 0x40581014 | FULL | Counter buffered compare/capture 0 register |
| TCPWM1_GRP0_CNT32_CC1 | 0x40581018 | FULL | Counter compare/capture 1 register |
| TCPWM1_GRP0_CNT32_CC1_BUFF | 0x4058101C | FULL | Counter buffered compare/capture 1 register |
| TCPWM1_GRP0_CNT32_PERIOD | 0x40581020 | FULL | Counter period register |
| TCPWM1_GRP0_CNT32_PERIOD_BUFF | 0x40581024 | FULL | Counter buffered period register |
| TCPWM1_GRP0_CNT32_DT | 0x40581030 | FULL | Counter PWM dead time register<br>Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM1_GRP0_CNT32_TR_CMD | 0x40581040 | FULL | Counter trigger command register |
| TCPWM1_GRP0_CNT32_TR_IN_SEL0 | 0x40581044 | FULL | Counter input trigger selection register 0 |
| TCPWM1_GRP0_CNT32_TR_IN_SEL1 | 0x40581048 | FULL | Counter input trigger selection register 1 |
| TCPWM1_GRP0_CNT32_TR_IN_EDGE_SEL | 0x4058104C | FULL | Counter input trigger edge selection register |
| TCPWM1_GRP0_CNT32_TR_PWM_CTRL | 0x40581050 | FULL | Counter trigger PWM control register |
| TCPWM1_GRP0_CNT32_TR_OUT_SEL | 0x40581054 | FULL | Counter output trigger selection register |
| TCPWM1_GRP0_CNT32_INTR | 0x40581070 | FULL | Interrupt request register |
| TCPWM1_GRP0_CNT32_INTR_SET | 0x40581074 | FULL | Interrupt set request register |
| TCPWM1_GRP0_CNT32_INTR_MASK | 0x40581078 | FULL | Interrupt mask register |
| TCPWM1_GRP0_CNT32_INTR_MASKED | 0x4058107C | FULL | Interrupt masked request register |

### 33.2.1.34 CNT 33

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT33_CTRL | 0x40581080 | FULL | Counter control register<br>Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM1_GRP0_CNT33_STATUS | 0x40581084 | FULL | Counter status register<br>Note:DT_CNT_H is not available for this register |
| TCPWM1_GRP0_CNT33_COUNTER | 0x40581088 | FULL | Counter count register |
| TCPWM1_GRP0_CNT33_CC0 | 0x40581090 | FULL | Counter compare/capture 0 register |
| TCPWM1_GRP0_CNT33_CC0_BUFF | 0x40581094 | FULL | Counter buffered compare/capture 0 register |
| TCPWM1_GRP0_CNT33_CC1 | 0x40581098 | FULL | Counter compare/capture 1 register |
| TCPWM1_GRP0_CNT33_CC1_BUFF | 0x4058109C | FULL | Counter buffered compare/capture 1 register |
| TCPWM1_GRP0_CNT33_PERIOD | 0x405810A0 | FULL | Counter period register |
| TCPWM1_GRP0_CNT33_PERIOD_BUFF | 0x405810A4 | FULL | Counter buffered period register |
| TCPWM1_GRP0_CNT33_DT | 0x405810B0 | FULL | Counter PWM dead time register<br>Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM1_GRP0_CNT33_TR_CMD | 0x405810C0 | FULL | Counter trigger command register |
| TCPWM1_GRP0_CNT33_TR_IN_SEL0 | 0x405810C4 | FULL | Counter input trigger selection register 0 |
| TCPWM1_GRP0_CNT33_TR_IN_SEL1 | 0x405810C8 | FULL | Counter input trigger selection register 1 |
| TCPWM1_GRP0_CNT33_TR_IN_EDGE_SEL | 0x405810CC | FULL | Counter input trigger edge selection register |
| TCPWM1_GRP0_CNT33_TR_PWM_CTRL | 0x405810D0 | FULL | Counter trigger PWM control register |
| TCPWM1_GRP0_CNT33_TR_OUT_SEL | 0x405810D4 | FULL | Counter output trigger selection register |
| TCPWM1_GRP0_CNT33_INTR | 0x405810F0 | FULL | Interrupt request register |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT33_INTR_SET | 0x405810F4 | FULL | Interrupt set request register |
| TCPWM1_GRP0_CNT33_INTR_MASK | 0x405810F8 | FULL | Interrupt mask register |
| TCPWM1_GRP0_CNT33_INTR_MASKED | 0x405810FC | FULL | Interrupt masked request register |

### 33.2.1.35 CNT 34

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT34_CTRL | 0x40581100 | FULL | Counter control register<br>Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM1_GRP0_CNT34_STATUS | 0x40581104 | FULL | Counter status register<br>Note:DT_CNT_H is not available for this register |
| TCPWM1_GRP0_CNT34_COUNTER | 0x40581108 | FULL | Counter count register |
| TCPWM1_GRP0_CNT34_CC0 | 0x40581110 | FULL | Counter compare/capture 0 register |
| TCPWM1_GRP0_CNT34_CC0_BUFF | 0x40581114 | FULL | Counter buffered compare/capture 0 register |
| TCPWM1_GRP0_CNT34_CC1 | 0x40581118 | FULL | Counter compare/capture 1 register |
| TCPWM1_GRP0_CNT34_CC1_BUFF | 0x4058111C | FULL | Counter buffered compare/capture 1 register |
| TCPWM1_GRP0_CNT34_PERIOD | 0x40581120 | FULL | Counter period register |
| TCPWM1_GRP0_CNT34_PERIOD_BUFF | 0x40581124 | FULL | Counter buffered period register |
| TCPWM1_GRP0_CNT34_DT | 0x40581130 | FULL | Counter PWM dead time register<br>Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM1_GRP0_CNT34_TR_CMD | 0x40581140 | FULL | Counter trigger command register |
| TCPWM1_GRP0_CNT34_TR_IN_SEL0 | 0x40581144 | FULL | Counter input trigger selection register 0 |
| TCPWM1_GRP0_CNT34_TR_IN_SEL1 | 0x40581148 | FULL | Counter input trigger selection register 1 |
| TCPWM1_GRP0_CNT34_TR_IN_EDGE_SEL | 0x4058114C | FULL | Counter input trigger edge selection register |
| TCPWM1_GRP0_CNT34_TR_PWM_CTRL | 0x40581150 | FULL | Counter trigger PWM control register |
| TCPWM1_GRP0_CNT34_TR_OUT_SEL | 0x40581154 | FULL | Counter output trigger selection register |
| TCPWM1_GRP0_CNT34_INTR | 0x40581170 | FULL | Interrupt request register |
| TCPWM1_GRP0_CNT34_INTR_SET | 0x40581174 | FULL | Interrupt set request register |
| TCPWM1_GRP0_CNT34_INTR_MASK | 0x40581178 | FULL | Interrupt mask register |
| TCPWM1_GRP0_CNT34_INTR_MASKED | 0x4058117C | FULL | Interrupt masked request register |

### 33.2.1.36 CNT 35

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT35_CTRL | 0x40581180 | FULL | Counter control register<br>Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM1_GRP0_CNT35_STATUS | 0x40581184 | FULL | Counter status register<br>Note:DT_CNT_H is not available for this register |
| TCPWM1_GRP0_CNT35_COUNTER | 0x40581188 | FULL | Counter count register |
| TCPWM1_GRP0_CNT35_CC0 | 0x40581190 | FULL | Counter compare/capture 0 register |
| TCPWM1_GRP0_CNT35_CC0_BUFF | 0x40581194 | FULL | Counter buffered compare/capture 0 register |
| TCPWM1_GRP0_CNT35_CC1 | 0x40581198 | FULL | Counter compare/capture 1 register |
| TCPWM1_GRP0_CNT35_CC1_BUFF | 0x4058119C | FULL | Counter buffered compare/capture 1 register |
| TCPWM1_GRP0_CNT35_PERIOD | 0x405811A0 | FULL | Counter period register |
| TCPWM1_GRP0_CNT35_PERIOD_BUFF | 0x405811A4 | FULL | Counter buffered period register |
| TCPWM1_GRP0_CNT35_DT | 0x405811B0 | FULL | Counter PWM dead time register<br>Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM1_GRP0_CNT35_TR_CMD | 0x405811C0 | FULL | Counter trigger command register |
| TCPWM1_GRP0_CNT35_TR_IN_SEL0 | 0x405811C4 | FULL | Counter input trigger selection register 0 |
| TCPWM1_GRP0_CNT35_TR_IN_SEL1 | 0x405811C8 | FULL | Counter input trigger selection register 1 |
| TCPWM1_GRP0_CNT35_TR_IN_EDGE_SEL | 0x405811CC | FULL | Counter input trigger edge selection register |
| TCPWM1_GRP0_CNT35_TR_PWM_CTRL | 0x405811D0 | FULL | Counter trigger PWM control register |
| TCPWM1_GRP0_CNT35_TR_OUT_SEL | 0x405811D4 | FULL | Counter output trigger selection register |
| TCPWM1_GRP0_CNT35_INTR | 0x405811F0 | FULL | Interrupt request register |
| TCPWM1_GRP0_CNT35_INTR_SET | 0x405811F4 | FULL | Interrupt set request register |
| TCPWM1_GRP0_CNT35_INTR_MASK | 0x405811F8 | FULL | Interrupt mask register |
| TCPWM1_GRP0_CNT35_INTR_MASKED | 0x405811FC | FULL | Interrupt masked request register |

### 33.2.1.37 CNT 36

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT36_CTRL | 0x40581200 | FULL | Counter control register<br>Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM1_GRP0_CNT36_STATUS | 0x40581204 | FULL | Counter status register<br>Note:DT_CNT_H is not available for this register |
| TCPWM1_GRP0_CNT36_COUNTER | 0x40581208 | FULL | Counter count register |
| TCPWM1_GRP0_CNT36_CC0 | 0x40581210 | FULL | Counter compare/capture 0 register |
| TCPWM1_GRP0_CNT36_CC0_BUFF | 0x40581214 | FULL | Counter buffered compare/capture 0 register |
| TCPWM1_GRP0_CNT36_CC1 | 0x40581218 | FULL | Counter compare/capture 1 register |
| TCPWM1_GRP0_CNT36_CC1_BUFF | 0x4058121C | FULL | Counter buffered compare/capture 1 register |
| TCPWM1_GRP0_CNT36_PERIOD | 0x40581220 | FULL | Counter period register |
| TCPWM1_GRP0_CNT36_PERIOD_BUFF | 0x40581224 | FULL | Counter buffered period register |
| TCPWM1_GRP0_CNT36_DT | 0x40581230 | FULL | Counter PWM dead time register<br>Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM1_GRP0_CNT36_TR_CMD | 0x40581240 | FULL | Counter trigger command register |
| TCPWM1_GRP0_CNT36_TR_IN_SEL0 | 0x40581244 | FULL | Counter input trigger selection register 0 |
| TCPWM1_GRP0_CNT36_TR_IN_SEL1 | 0x40581248 | FULL | Counter input trigger selection register 1 |
| TCPWM1_GRP0_CNT36_TR_IN_EDGE_SEL | 0x4058124C | FULL | Counter input trigger edge selection register |
| TCPWM1_GRP0_CNT36_TR_PWM_CTRL | 0x40581250 | FULL | Counter trigger PWM control register |
| TCPWM1_GRP0_CNT36_TR_OUT_SEL | 0x40581254 | FULL | Counter output trigger selection register |
| TCPWM1_GRP0_CNT36_INTR | 0x40581270 | FULL | Interrupt request register |
| TCPWM1_GRP0_CNT36_INTR_SET | 0x40581274 | FULL | Interrupt set request register |
| TCPWM1_GRP0_CNT36_INTR_MASK | 0x40581278 | FULL | Interrupt mask register |
| TCPWM1_GRP0_CNT36_INTR_MASKED | 0x4058127C | FULL | Interrupt masked request register |

### 33.2.1.38 CNT 37

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT37_CTRL | 0x40581280 | FULL | Counter control register<br>Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM1_GRP0_CNT37_STATUS | 0x40581284 | FULL | Counter status register<br>Note:DT_CNT_H is not available for this register |
| TCPWM1_GRP0_CNT37_COUNTER | 0x40581288 | FULL | Counter count register |
| TCPWM1_GRP0_CNT37_CC0 | 0x40581290 | FULL | Counter compare/capture 0 register |
| TCPWM1_GRP0_CNT37_CC0_BUFF | 0x40581294 | FULL | Counter buffered compare/capture 0 register |
| TCPWM1_GRP0_CNT37_CC1 | 0x40581298 | FULL | Counter compare/capture 1 register |
| TCPWM1_GRP0_CNT37_CC1_BUFF | 0x4058129C | FULL | Counter buffered compare/capture 1 register |
| TCPWM1_GRP0_CNT37_PERIOD | 0x405812A0 | FULL | Counter period register |
| TCPWM1_GRP0_CNT37_PERIOD_BUFF | 0x405812A4 | FULL | Counter buffered period register |
| TCPWM1_GRP0_CNT37_DT | 0x405812B0 | FULL | Counter PWM dead time register<br>Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM1_GRP0_CNT37_TR_CMD | 0x405812C0 | FULL | Counter trigger command register |
| TCPWM1_GRP0_CNT37_TR_IN_SEL0 | 0x405812C4 | FULL | Counter input trigger selection register 0 |
| TCPWM1_GRP0_CNT37_TR_IN_SEL1 | 0x405812C8 | FULL | Counter input trigger selection register 1 |
| TCPWM1_GRP0_CNT37_TR_IN_EDGE_SEL | 0x405812CC | FULL | Counter input trigger edge selection register |
| TCPWM1_GRP0_CNT37_TR_PWM_CTRL | 0x405812D0 | FULL | Counter trigger PWM control register |
| TCPWM1_GRP0_CNT37_TR_OUT_SEL | 0x405812D4 | FULL | Counter output trigger selection register |
| TCPWM1_GRP0_CNT37_INTR | 0x405812F0 | FULL | Interrupt request register |
| TCPWM1_GRP0_CNT37_INTR_SET | 0x405812F4 | FULL | Interrupt set request register |
| TCPWM1_GRP0_CNT37_INTR_MASK | 0x405812F8 | FULL | Interrupt mask register |
| TCPWM1_GRP0_CNT37_INTR_MASKED | 0x405812FC | FULL | Interrupt masked request register |

### 33.2.1.39 CNT 38

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT38_CTRL | 0x40581300 | FULL | Counter control register<br>Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT38_STATUS | 0x40581304 | FULL | Counter status register<br>Note:DT_CNT_H is not available for this register |
| TCPWM1_GRP0_CNT38_COUNTER | 0x40581308 | FULL | Counter count register |
| TCPWM1_GRP0_CNT38_CC0 | 0x40581310 | FULL | Counter compare/capture 0 register |
| TCPWM1_GRP0_CNT38_CC0_BUFF | 0x40581314 | FULL | Counter buffered compare/capture 0 register |
| TCPWM1_GRP0_CNT38_CC1 | 0x40581318 | FULL | Counter compare/capture 1 register |
| TCPWM1_GRP0_CNT38_CC1_BUFF | 0x4058131C | FULL | Counter buffered compare/capture 1 register |
| TCPWM1_GRP0_CNT38_PERIOD | 0x40581320 | FULL | Counter period register |
| TCPWM1_GRP0_CNT38_PERIOD_BUFF | 0x40581324 | FULL | Counter buffered period register |
| TCPWM1_GRP0_CNT38_DT | 0x40581330 | FULL | Counter PWM dead time register<br>Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM1_GRP0_CNT38_TR_CMD | 0x40581340 | FULL | Counter trigger command register |
| TCPWM1_GRP0_CNT38_TR_IN_SEL0 | 0x40581344 | FULL | Counter input trigger selection register 0 |
| TCPWM1_GRP0_CNT38_TR_IN_SEL1 | 0x40581348 | FULL | Counter input trigger selection register 1 |
| TCPWM1_GRP0_CNT38_TR_IN_EDGE_SEL | 0x4058134C | FULL | Counter input trigger edge selection register |
| TCPWM1_GRP0_CNT38_TR_PWM_CTRL | 0x40581350 | FULL | Counter trigger PWM control register |
| TCPWM1_GRP0_CNT38_TR_OUT_SEL | 0x40581354 | FULL | Counter output trigger selection register |
| TCPWM1_GRP0_CNT38_INTR | 0x40581370 | FULL | Interrupt request register |
| TCPWM1_GRP0_CNT38_INTR_SET | 0x40581374 | FULL | Interrupt set request register |
| TCPWM1_GRP0_CNT38_INTR_MASK | 0x40581378 | FULL | Interrupt mask register |
| TCPWM1_GRP0_CNT38_INTR_MASKED | 0x4058137C | FULL | Interrupt masked request register |

### 33.2.1.40 CNT 39

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT39_CTRL | 0x40581380 | FULL | Counter control register<br>Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM1_GRP0_CNT39_STATUS | 0x40581384 | FULL | Counter status register<br>Note:DT_CNT_H is not available for this register |
| TCPWM1_GRP0_CNT39_COUNTER | 0x40581388 | FULL | Counter count register |
| TCPWM1_GRP0_CNT39_CC0 | 0x40581390 | FULL | Counter compare/capture 0 register |
| TCPWM1_GRP0_CNT39_CC0_BUFF | 0x40581394 | FULL | Counter buffered compare/capture 0 register |
| TCPWM1_GRP0_CNT39_CC1 | 0x40581398 | FULL | Counter compare/capture 1 register |
| TCPWM1_GRP0_CNT39_CC1_BUFF | 0x4058139C | FULL | Counter buffered compare/capture 1 register |
| TCPWM1_GRP0_CNT39_PERIOD | 0x405813A0 | FULL | Counter period register |
| TCPWM1_GRP0_CNT39_PERIOD_BUFF | 0x405813A4 | FULL | Counter buffered period register |
| TCPWM1_GRP0_CNT39_DT | 0x405813B0 | FULL | Counter PWM dead time register<br>Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM1_GRP0_CNT39_TR_CMD | 0x405813C0 | FULL | Counter trigger command register |
| TCPWM1_GRP0_CNT39_TR_IN_SEL0 | 0x405813C4 | FULL | Counter input trigger selection register 0 |
| TCPWM1_GRP0_CNT39_TR_IN_SEL1 | 0x405813C8 | FULL | Counter input trigger selection register 1 |
| TCPWM1_GRP0_CNT39_TR_IN_EDGE_SEL | 0x405813CC | FULL | Counter input trigger edge selection register |
| TCPWM1_GRP0_CNT39_TR_PWM_CTRL | 0x405813D0 | FULL | Counter trigger PWM control register |
| TCPWM1_GRP0_CNT39_TR_OUT_SEL | 0x405813D4 | FULL | Counter output trigger selection register |
| TCPWM1_GRP0_CNT39_INTR | 0x405813F0 | FULL | Interrupt request register |
| TCPWM1_GRP0_CNT39_INTR_SET | 0x405813F4 | FULL | Interrupt set request register |
| TCPWM1_GRP0_CNT39_INTR_MASK | 0x405813F8 | FULL | Interrupt mask register |
| TCPWM1_GRP0_CNT39_INTR_MASKED | 0x405813FC | FULL | Interrupt masked request register |

### 33.2.1.41 CNT 40

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT40_CTRL | 0x40581400 | FULL | Counter control register<br>Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM1_GRP0_CNT40_STATUS | 0x40581404 | FULL | Counter status register<br>Note:DT_CNT_H is not available for this register |
| TCPWM1_GRP0_CNT40_COUNTER | 0x40581408 | FULL | Counter count register |
| TCPWM1_GRP0_CNT40_CC0 | 0x40581410 | FULL | Counter compare/capture 0 register |
| TCPWM1_GRP0_CNT40_CC0_BUFF | 0x40581414 | FULL | Counter buffered compare/capture 0 register |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT40_CC1 | 0x40581418 | FULL | Counter compare/capture 1 register |
| TCPWM1_GRP0_CNT40_CC1_BUFF | 0x4058141C | FULL | Counter buffered compare/capture 1 register |
| TCPWM1_GRP0_CNT40_PERIOD | 0x40581420 | FULL | Counter period register |
| TCPWM1_GRP0_CNT40_PERIOD_BUFF | 0x40581424 | FULL | Counter buffered period register |
| TCPWM1_GRP0_CNT40_DT | 0x40581430 | FULL | Counter PWM dead time register Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM1_GRP0_CNT40_TR_CMD | 0x40581440 | FULL | Counter trigger command register |
| TCPWM1_GRP0_CNT40_TR_IN_SEL0 | 0x40581444 | FULL | Counter input trigger selection register 0 |
| TCPWM1_GRP0_CNT40_TR_IN_SEL1 | 0x40581448 | FULL | Counter input trigger selection register 1 |
| TCPWM1_GRP0_CNT40_TR_IN_EDGE_SEL | 0x4058144C | FULL | Counter input trigger edge selection register |
| TCPWM1_GRP0_CNT40_TR_PWM_CTRL | 0x40581450 | FULL | Counter trigger PWM control register |
| TCPWM1_GRP0_CNT40_TR_OUT_SEL | 0x40581454 | FULL | Counter output trigger selection register |
| TCPWM1_GRP0_CNT40_INTR | 0x40581470 | FULL | Interrupt request register |
| TCPWM1_GRP0_CNT40_INTR_SET | 0x40581474 | FULL | Interrupt set request register |
| TCPWM1_GRP0_CNT40_INTR_MASK | 0x40581478 | FULL | Interrupt mask register |
| TCPWM1_GRP0_CNT40_INTR_MASKED | 0x4058147C | FULL | Interrupt masked request register |

### 33.2.1.42 CNT 41

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT41_CTRL | 0x40581480 | FULL | Counter control register Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM1_GRP0_CNT41_STATUS | 0x40581484 | FULL | Counter status register Note:DT_CNT_H is not available for this register |
| TCPWM1_GRP0_CNT41_COUNTER | 0x40581488 | FULL | Counter count register |
| TCPWM1_GRP0_CNT41_CC0 | 0x40581490 | FULL | Counter compare/capture 0 register |
| TCPWM1_GRP0_CNT41_CC0_BUFF | 0x40581494 | FULL | Counter buffered compare/capture 0 register |
| TCPWM1_GRP0_CNT41_CC1 | 0x40581498 | FULL | Counter compare/capture 1 register |
| TCPWM1_GRP0_CNT41_CC1_BUFF | 0x4058149C | FULL | Counter buffered compare/capture 1 register |
| TCPWM1_GRP0_CNT41_PERIOD | 0x405814A0 | FULL | Counter period register |
| TCPWM1_GRP0_CNT41_PERIOD_BUFF | 0x405814A4 | FULL | Counter buffered period register |
| TCPWM1_GRP0_CNT41_DT | 0x405814B0 | FULL | Counter PWM dead time register Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM1_GRP0_CNT41_TR_CMD | 0x405814C0 | FULL | Counter trigger command register |
| TCPWM1_GRP0_CNT41_TR_IN_SEL0 | 0x405814C4 | FULL | Counter input trigger selection register 0 |
| TCPWM1_GRP0_CNT41_TR_IN_SEL1 | 0x405814C8 | FULL | Counter input trigger selection register 1 |
| TCPWM1_GRP0_CNT41_TR_IN_EDGE_SEL | 0x405814CC | FULL | Counter input trigger edge selection register |
| TCPWM1_GRP0_CNT41_TR_PWM_CTRL | 0x405814D0 | FULL | Counter trigger PWM control register |
| TCPWM1_GRP0_CNT41_TR_OUT_SEL | 0x405814D4 | FULL | Counter output trigger selection register |
| TCPWM1_GRP0_CNT41_INTR | 0x405814F0 | FULL | Interrupt request register |
| TCPWM1_GRP0_CNT41_INTR_SET | 0x405814F4 | FULL | Interrupt set request register |
| TCPWM1_GRP0_CNT41_INTR_MASK | 0x405814F8 | FULL | Interrupt mask register |
| TCPWM1_GRP0_CNT41_INTR_MASKED | 0x405814FC | FULL | Interrupt masked request register |

### 33.2.1.43 CNT 42

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT42_CTRL | 0x40581500 | FULL | Counter control register Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM1_GRP0_CNT42_STATUS | 0x40581504 | FULL | Counter status register Note:DT_CNT_H is not available for this register |
| TCPWM1_GRP0_CNT42_COUNTER | 0x40581508 | FULL | Counter count register |
| TCPWM1_GRP0_CNT42_CC0 | 0x40581510 | FULL | Counter compare/capture 0 register |
| TCPWM1_GRP0_CNT42_CC0_BUFF | 0x40581514 | FULL | Counter buffered compare/capture 0 register |
| TCPWM1_GRP0_CNT42_CC1 | 0x40581518 | FULL | Counter compare/capture 1 register |
| TCPWM1_GRP0_CNT42_CC1_BUFF | 0x4058151C | FULL | Counter buffered compare/capture 1 register |
| TCPWM1_GRP0_CNT42_PERIOD | 0x40581520 | FULL | Counter period register |
| TCPWM1_GRP0_CNT42_PERIOD_BUFF | 0x40581524 | FULL | Counter buffered period register |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT42_DT | 0x40581530 | FULL | Counter PWM dead time register<br>Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM1_GRP0_CNT42_TR_CMD | 0x40581540 | FULL | Counter trigger command register |
| TCPWM1_GRP0_CNT42_TR_IN_SEL0 | 0x40581544 | FULL | Counter input trigger selection register 0 |
| TCPWM1_GRP0_CNT42_TR_IN_SEL1 | 0x40581548 | FULL | Counter input trigger selection register 1 |
| TCPWM1_GRP0_CNT42_TR_IN_EDGE_SEL | 0x4058154C | FULL | Counter input trigger edge selection register |
| TCPWM1_GRP0_CNT42_TR_PWM_CTRL | 0x40581550 | FULL | Counter trigger PWM control register |
| TCPWM1_GRP0_CNT42_TR_OUT_SEL | 0x40581554 | FULL | Counter output trigger selection register |
| TCPWM1_GRP0_CNT42_INTR | 0x40581570 | FULL | Interrupt request register |
| TCPWM1_GRP0_CNT42_INTR_SET | 0x40581574 | FULL | Interrupt set request register |
| TCPWM1_GRP0_CNT42_INTR_MASK | 0x40581578 | FULL | Interrupt mask register |
| TCPWM1_GRP0_CNT42_INTR_MASKED | 0x4058157C | FULL | Interrupt masked request register |

### 33.2.1.44 CNT 43

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT43_CTRL | 0x40581580 | FULL | Counter control register<br>Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM1_GRP0_CNT43_STATUS | 0x40581584 | FULL | Counter status register<br>Note:DT_CNT_H is not available for this register |
| TCPWM1_GRP0_CNT43_COUNTER | 0x40581588 | FULL | Counter count register |
| TCPWM1_GRP0_CNT43_CC0 | 0x40581590 | FULL | Counter compare/capture 0 register |
| TCPWM1_GRP0_CNT43_CC0_BUFF | 0x40581594 | FULL | Counter buffered compare/capture 0 register |
| TCPWM1_GRP0_CNT43_CC1 | 0x40581598 | FULL | Counter compare/capture 1 register |
| TCPWM1_GRP0_CNT43_CC1_BUFF | 0x4058159C | FULL | Counter buffered compare/capture 1 register |
| TCPWM1_GRP0_CNT43_PERIOD | 0x405815A0 | FULL | Counter period register |
| TCPWM1_GRP0_CNT43_PERIOD_BUFF | 0x405815A4 | FULL | Counter buffered period register |
| TCPWM1_GRP0_CNT43_DT | 0x405815B0 | FULL | Counter PWM dead time register<br>Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM1_GRP0_CNT43_TR_CMD | 0x405815C0 | FULL | Counter trigger command register |
| TCPWM1_GRP0_CNT43_TR_IN_SEL0 | 0x405815C4 | FULL | Counter input trigger selection register 0 |
| TCPWM1_GRP0_CNT43_TR_IN_SEL1 | 0x405815C8 | FULL | Counter input trigger selection register 1 |
| TCPWM1_GRP0_CNT43_TR_IN_EDGE_SEL | 0x405815CC | FULL | Counter input trigger edge selection register |
| TCPWM1_GRP0_CNT43_TR_PWM_CTRL | 0x405815D0 | FULL | Counter trigger PWM control register |
| TCPWM1_GRP0_CNT43_TR_OUT_SEL | 0x405815D4 | FULL | Counter output trigger selection register |
| TCPWM1_GRP0_CNT43_INTR | 0x405815F0 | FULL | Interrupt request register |
| TCPWM1_GRP0_CNT43_INTR_SET | 0x405815F4 | FULL | Interrupt set request register |
| TCPWM1_GRP0_CNT43_INTR_MASK | 0x405815F8 | FULL | Interrupt mask register |
| TCPWM1_GRP0_CNT43_INTR_MASKED | 0x405815FC | FULL | Interrupt masked request register |

### 33.2.1.45 CNT 44

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT44_CTRL | 0x40581600 | FULL | Counter control register<br>Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM1_GRP0_CNT44_STATUS | 0x40581604 | FULL | Counter status register<br>Note:DT_CNT_H is not available for this register |
| TCPWM1_GRP0_CNT44_COUNTER | 0x40581608 | FULL | Counter count register |
| TCPWM1_GRP0_CNT44_CC0 | 0x40581610 | FULL | Counter compare/capture 0 register |
| TCPWM1_GRP0_CNT44_CC0_BUFF | 0x40581614 | FULL | Counter buffered compare/capture 0 register |
| TCPWM1_GRP0_CNT44_CC1 | 0x40581618 | FULL | Counter compare/capture 1 register |
| TCPWM1_GRP0_CNT44_CC1_BUFF | 0x4058161C | FULL | Counter buffered compare/capture 1 register |
| TCPWM1_GRP0_CNT44_PERIOD | 0x40581620 | FULL | Counter period register |
| TCPWM1_GRP0_CNT44_PERIOD_BUFF | 0x40581624 | FULL | Counter buffered period register |
| TCPWM1_GRP0_CNT44_DT | 0x40581630 | FULL | Counter PWM dead time register<br>Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM1_GRP0_CNT44_TR_CMD | 0x40581640 | FULL | Counter trigger command register |
| TCPWM1_GRP0_CNT44_TR_IN_SEL0 | 0x40581644 | FULL | Counter input trigger selection register 0 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT44_TR_IN_SEL1 | 0x40581648 | FULL | Counter input trigger selection register 1 |
| TCPWM1_GRP0_CNT44_TR_IN_EDGE_SEL | 0x4058164C | FULL | Counter input trigger edge selection register |
| TCPWM1_GRP0_CNT44_TR_PWM_CTRL | 0x40581650 | FULL | Counter trigger PWM control register |
| TCPWM1_GRP0_CNT44_TR_OUT_SEL | 0x40581654 | FULL | Counter output trigger selection register |
| TCPWM1_GRP0_CNT44_INTR | 0x40581670 | FULL | Interrupt request register |
| TCPWM1_GRP0_CNT44_INTR_SET | 0x40581674 | FULL | Interrupt set request register |
| TCPWM1_GRP0_CNT44_INTR_MASK | 0x40581678 | FULL | Interrupt mask register |
| TCPWM1_GRP0_CNT44_INTR_MASKED | 0x4058167C | FULL | Interrupt masked request register |

### 33.2.1.46 CNT 45

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT45_CTRL | 0x40581680 | FULL | Counter control register<br>Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM1_GRP0_CNT45_STATUS | 0x40581684 | FULL | Counter status register<br>Note:DT_CNT_H is not available for this register |
| TCPWM1_GRP0_CNT45_COUNTER | 0x40581688 | FULL | Counter count register |
| TCPWM1_GRP0_CNT45_CC0 | 0x40581690 | FULL | Counter compare/capture 0 register |
| TCPWM1_GRP0_CNT45_CC0_BUFF | 0x40581694 | FULL | Counter buffered compare/capture 0 register |
| TCPWM1_GRP0_CNT45_CC1 | 0x40581698 | FULL | Counter compare/capture 1 register |
| TCPWM1_GRP0_CNT45_CC1_BUFF | 0x4058169C | FULL | Counter buffered compare/capture 1 register |
| TCPWM1_GRP0_CNT45_PERIOD | 0x405816A0 | FULL | Counter period register |
| TCPWM1_GRP0_CNT45_PERIOD_BUFF | 0x405816A4 | FULL | Counter buffered period register |
| TCPWM1_GRP0_CNT45_DT | 0x405816B0 | FULL | Counter PWM dead time register<br>Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM1_GRP0_CNT45_TR_CMD | 0x405816C0 | FULL | Counter trigger command register |
| TCPWM1_GRP0_CNT45_TR_IN_SEL0 | 0x405816C4 | FULL | Counter input trigger selection register 0 |
| TCPWM1_GRP0_CNT45_TR_IN_SEL1 | 0x405816C8 | FULL | Counter input trigger selection register 1 |
| TCPWM1_GRP0_CNT45_TR_IN_EDGE_SEL | 0x405816CC | FULL | Counter input trigger edge selection register |
| TCPWM1_GRP0_CNT45_TR_PWM_CTRL | 0x405816D0 | FULL | Counter trigger PWM control register |
| TCPWM1_GRP0_CNT45_TR_OUT_SEL | 0x405816D4 | FULL | Counter output trigger selection register |
| TCPWM1_GRP0_CNT45_INTR | 0x405816F0 | FULL | Interrupt request register |
| TCPWM1_GRP0_CNT45_INTR_SET | 0x405816F4 | FULL | Interrupt set request register |
| TCPWM1_GRP0_CNT45_INTR_MASK | 0x405816F8 | FULL | Interrupt mask register |
| TCPWM1_GRP0_CNT45_INTR_MASKED | 0x405816FC | FULL | Interrupt masked request register |

### 33.2.1.47 CNT 46

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT46_CTRL | 0x40581700 | FULL | Counter control register<br>Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM1_GRP0_CNT46_STATUS | 0x40581704 | FULL | Counter status register<br>Note:DT_CNT_H is not available for this register |
| TCPWM1_GRP0_CNT46_COUNTER | 0x40581708 | FULL | Counter count register |
| TCPWM1_GRP0_CNT46_CC0 | 0x40581710 | FULL | Counter compare/capture 0 register |
| TCPWM1_GRP0_CNT46_CC0_BUFF | 0x40581714 | FULL | Counter buffered compare/capture 0 register |
| TCPWM1_GRP0_CNT46_CC1 | 0x40581718 | FULL | Counter compare/capture 1 register |
| TCPWM1_GRP0_CNT46_CC1_BUFF | 0x4058171C | FULL | Counter buffered compare/capture 1 register |
| TCPWM1_GRP0_CNT46_PERIOD | 0x40581720 | FULL | Counter period register |
| TCPWM1_GRP0_CNT46_PERIOD_BUFF | 0x40581724 | FULL | Counter buffered period register |
| TCPWM1_GRP0_CNT46_DT | 0x40581730 | FULL | Counter PWM dead time register<br>Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM1_GRP0_CNT46_TR_CMD | 0x40581740 | FULL | Counter trigger command register |
| TCPWM1_GRP0_CNT46_TR_IN_SEL0 | 0x40581744 | FULL | Counter input trigger selection register 0 |
| TCPWM1_GRP0_CNT46_TR_IN_SEL1 | 0x40581748 | FULL | Counter input trigger selection register 1 |
| TCPWM1_GRP0_CNT46_TR_IN_EDGE_SEL | 0x4058174C | FULL | Counter input trigger edge selection register |
| TCPWM1_GRP0_CNT46_TR_PWM_CTRL | 0x40581750 | FULL | Counter trigger PWM control register |
| TCPWM1_GRP0_CNT46_TR_OUT_SEL | 0x40581754 | FULL | Counter output trigger selection register |
| TCPWM1_GRP0_CNT46_INTR | 0x40581770 | FULL | Interrupt request register |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT46_INTR_SET | 0x40581774 | FULL | Interrupt set request register |
| TCPWM1_GRP0_CNT46_INTR_MASK | 0x40581778 | FULL | Interrupt mask register |
| TCPWM1_GRP0_CNT46_INTR_MASKED | 0x4058177C | FULL | Interrupt masked request register |

### 33.2.1.48 CNT 47

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT47_CTRL | 0x40581780 | FULL | Counter control register<br>Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM1_GRP0_CNT47_STATUS | 0x40581784 | FULL | Counter status register<br>Note:DT_CNT_H is not available for this register |
| TCPWM1_GRP0_CNT47_COUNTER | 0x40581788 | FULL | Counter count register |
| TCPWM1_GRP0_CNT47_CC0 | 0x40581790 | FULL | Counter compare/capture 0 register |
| TCPWM1_GRP0_CNT47_CC0_BUFF | 0x40581794 | FULL | Counter buffered compare/capture 0 register |
| TCPWM1_GRP0_CNT47_CC1 | 0x40581798 | FULL | Counter compare/capture 1 register |
| TCPWM1_GRP0_CNT47_CC1_BUFF | 0x4058179C | FULL | Counter buffered compare/capture 1 register |
| TCPWM1_GRP0_CNT47_PERIOD | 0x405817A0 | FULL | Counter period register |
| TCPWM1_GRP0_CNT47_PERIOD_BUFF | 0x405817A4 | FULL | Counter buffered period register |
| TCPWM1_GRP0_CNT47_DT | 0x405817B0 | FULL | Counter PWM dead time register<br>Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM1_GRP0_CNT47_TR_CMD | 0x405817C0 | FULL | Counter trigger command register |
| TCPWM1_GRP0_CNT47_TR_IN_SEL0 | 0x405817C4 | FULL | Counter input trigger selection register 0 |
| TCPWM1_GRP0_CNT47_TR_IN_SEL1 | 0x405817C8 | FULL | Counter input trigger selection register 1 |
| TCPWM1_GRP0_CNT47_TR_IN_EDGE_SEL | 0x405817CC | FULL | Counter input trigger edge selection register |
| TCPWM1_GRP0_CNT47_TR_PWM_CTRL | 0x405817D0 | FULL | Counter trigger PWM control register |
| TCPWM1_GRP0_CNT47_TR_OUT_SEL | 0x405817D4 | FULL | Counter output trigger selection register |
| TCPWM1_GRP0_CNT47_INTR | 0x405817F0 | FULL | Interrupt request register |
| TCPWM1_GRP0_CNT47_INTR_SET | 0x405817F4 | FULL | Interrupt set request register |
| TCPWM1_GRP0_CNT47_INTR_MASK | 0x405817F8 | FULL | Interrupt mask register |
| TCPWM1_GRP0_CNT47_INTR_MASKED | 0x405817FC | FULL | Interrupt masked request register |

### 33.2.1.49 CNT 48

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT48_CTRL | 0x40581800 | FULL | Counter control register<br>Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM1_GRP0_CNT48_STATUS | 0x40581804 | FULL | Counter status register<br>Note:DT_CNT_H is not available for this register |
| TCPWM1_GRP0_CNT48_COUNTER | 0x40581808 | FULL | Counter count register |
| TCPWM1_GRP0_CNT48_CC0 | 0x40581810 | FULL | Counter compare/capture 0 register |
| TCPWM1_GRP0_CNT48_CC0_BUFF | 0x40581814 | FULL | Counter buffered compare/capture 0 register |
| TCPWM1_GRP0_CNT48_CC1 | 0x40581818 | FULL | Counter compare/capture 1 register |
| TCPWM1_GRP0_CNT48_CC1_BUFF | 0x4058181C | FULL | Counter buffered compare/capture 1 register |
| TCPWM1_GRP0_CNT48_PERIOD | 0x40581820 | FULL | Counter period register |
| TCPWM1_GRP0_CNT48_PERIOD_BUFF | 0x40581824 | FULL | Counter buffered period register |
| TCPWM1_GRP0_CNT48_DT | 0x40581830 | FULL | Counter PWM dead time register<br>Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM1_GRP0_CNT48_TR_CMD | 0x40581840 | FULL | Counter trigger command register |
| TCPWM1_GRP0_CNT48_TR_IN_SEL0 | 0x40581844 | FULL | Counter input trigger selection register 0 |
| TCPWM1_GRP0_CNT48_TR_IN_SEL1 | 0x40581848 | FULL | Counter input trigger selection register 1 |
| TCPWM1_GRP0_CNT48_TR_IN_EDGE_SEL | 0x4058184C | FULL | Counter input trigger edge selection register |
| TCPWM1_GRP0_CNT48_TR_PWM_CTRL | 0x40581850 | FULL | Counter trigger PWM control register |
| TCPWM1_GRP0_CNT48_TR_OUT_SEL | 0x40581854 | FULL | Counter output trigger selection register |
| TCPWM1_GRP0_CNT48_INTR | 0x40581870 | FULL | Interrupt request register |
| TCPWM1_GRP0_CNT48_INTR_SET | 0x40581874 | FULL | Interrupt set request register |
| TCPWM1_GRP0_CNT48_INTR_MASK | 0x40581878 | FULL | Interrupt mask register |
| TCPWM1_GRP0_CNT48_INTR_MASKED | 0x4058187C | FULL | Interrupt masked request register |

### 33.2.1.50 CNT 49

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT49_CTRL | 0x40581880 | FULL | Counter control register<br>Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM1_GRP0_CNT49_STATUS | 0x40581884 | FULL | Counter status register<br>Note:DT_CNT_H is not available for this register |
| TCPWM1_GRP0_CNT49_COUNTER | 0x40581888 | FULL | Counter count register |
| TCPWM1_GRP0_CNT49_CC0 | 0x40581890 | FULL | Counter compare/capture 0 register |
| TCPWM1_GRP0_CNT49_CC0_BUFF | 0x40581894 | FULL | Counter buffered compare/capture 0 register |
| TCPWM1_GRP0_CNT49_CC1 | 0x40581898 | FULL | Counter compare/capture 1 register |
| TCPWM1_GRP0_CNT49_CC1_BUFF | 0x4058189C | FULL | Counter buffered compare/capture 1 register |
| TCPWM1_GRP0_CNT49_PERIOD | 0x405818A0 | FULL | Counter period register |
| TCPWM1_GRP0_CNT49_PERIOD_BUFF | 0x405818A4 | FULL | Counter buffered period register |
| TCPWM1_GRP0_CNT49_DT | 0x405818B0 | FULL | Counter PWM dead time register<br>Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM1_GRP0_CNT49_TR_CMD | 0x405818C0 | FULL | Counter trigger command register |
| TCPWM1_GRP0_CNT49_TR_IN_SEL0 | 0x405818C4 | FULL | Counter input trigger selection register 0 |
| TCPWM1_GRP0_CNT49_TR_IN_SEL1 | 0x405818C8 | FULL | Counter input trigger selection register 1 |
| TCPWM1_GRP0_CNT49_TR_IN_EDGE_SEL | 0x405818CC | FULL | Counter input trigger edge selection register |
| TCPWM1_GRP0_CNT49_TR_PWM_CTRL | 0x405818D0 | FULL | Counter trigger PWM control register |
| TCPWM1_GRP0_CNT49_TR_OUT_SEL | 0x405818D4 | FULL | Counter output trigger selection register |
| TCPWM1_GRP0_CNT49_INTR | 0x405818F0 | FULL | Interrupt request register |
| TCPWM1_GRP0_CNT49_INTR_SET | 0x405818F4 | FULL | Interrupt set request register |
| TCPWM1_GRP0_CNT49_INTR_MASK | 0x405818F8 | FULL | Interrupt mask register |
| TCPWM1_GRP0_CNT49_INTR_MASKED | 0x405818FC | FULL | Interrupt masked request register |

### 33.2.1.51 CNT 50

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT50_CTRL | 0x40581900 | FULL | Counter control register<br>Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM1_GRP0_CNT50_STATUS | 0x40581904 | FULL | Counter status register<br>Note:DT_CNT_H is not available for this register |
| TCPWM1_GRP0_CNT50_COUNTER | 0x40581908 | FULL | Counter count register |
| TCPWM1_GRP0_CNT50_CC0 | 0x40581910 | FULL | Counter compare/capture 0 register |
| TCPWM1_GRP0_CNT50_CC0_BUFF | 0x40581914 | FULL | Counter buffered compare/capture 0 register |
| TCPWM1_GRP0_CNT50_CC1 | 0x40581918 | FULL | Counter compare/capture 1 register |
| TCPWM1_GRP0_CNT50_CC1_BUFF | 0x4058191C | FULL | Counter buffered compare/capture 1 register |
| TCPWM1_GRP0_CNT50_PERIOD | 0x40581920 | FULL | Counter period register |
| TCPWM1_GRP0_CNT50_PERIOD_BUFF | 0x40581924 | FULL | Counter buffered period register |
| TCPWM1_GRP0_CNT50_DT | 0x40581930 | FULL | Counter PWM dead time register<br>Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM1_GRP0_CNT50_TR_CMD | 0x40581940 | FULL | Counter trigger command register |
| TCPWM1_GRP0_CNT50_TR_IN_SEL0 | 0x40581944 | FULL | Counter input trigger selection register 0 |
| TCPWM1_GRP0_CNT50_TR_IN_SEL1 | 0x40581948 | FULL | Counter input trigger selection register 1 |
| TCPWM1_GRP0_CNT50_TR_IN_EDGE_SEL | 0x4058194C | FULL | Counter input trigger edge selection register |
| TCPWM1_GRP0_CNT50_TR_PWM_CTRL | 0x40581950 | FULL | Counter trigger PWM control register |
| TCPWM1_GRP0_CNT50_TR_OUT_SEL | 0x40581954 | FULL | Counter output trigger selection register |
| TCPWM1_GRP0_CNT50_INTR | 0x40581970 | FULL | Interrupt request register |
| TCPWM1_GRP0_CNT50_INTR_SET | 0x40581974 | FULL | Interrupt set request register |
| TCPWM1_GRP0_CNT50_INTR_MASK | 0x40581978 | FULL | Interrupt mask register |
| TCPWM1_GRP0_CNT50_INTR_MASKED | 0x4058197C | FULL | Interrupt masked request register |

### 33.2.1.52 CNT 51

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT51_CTRL | 0x40581980 | FULL | Counter control register<br>Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT51_STATUS | 0x40581984 | FULL | Counter status register<br>Note:DT_CNT_H is not available for this register |
| TCPWM1_GRP0_CNT51_COUNTER | 0x40581988 | FULL | Counter count register |
| TCPWM1_GRP0_CNT51_CC0 | 0x40581990 | FULL | Counter compare/capture 0 register |
| TCPWM1_GRP0_CNT51_CC0_BUFF | 0x40581994 | FULL | Counter buffered compare/capture 0 register |
| TCPWM1_GRP0_CNT51_CC1 | 0x40581998 | FULL | Counter compare/capture 1 register |
| TCPWM1_GRP0_CNT51_CC1_BUFF | 0x4058199C | FULL | Counter buffered compare/capture 1 register |
| TCPWM1_GRP0_CNT51_PERIOD | 0x405819A0 | FULL | Counter period register |
| TCPWM1_GRP0_CNT51_PERIOD_BUFF | 0x405819A4 | FULL | Counter buffered period register |
| TCPWM1_GRP0_CNT51_DT | 0x405819B0 | FULL | Counter PWM dead time register<br>Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM1_GRP0_CNT51_TR_CMD | 0x405819C0 | FULL | Counter trigger command register |
| TCPWM1_GRP0_CNT51_TR_IN_SEL0 | 0x405819C4 | FULL | Counter input trigger selection register 0 |
| TCPWM1_GRP0_CNT51_TR_IN_SEL1 | 0x405819C8 | FULL | Counter input trigger selection register 1 |
| TCPWM1_GRP0_CNT51_TR_IN_EDGE_SEL | 0x405819CC | FULL | Counter input trigger edge selection register |
| TCPWM1_GRP0_CNT51_TR_PWM_CTRL | 0x405819D0 | FULL | Counter trigger PWM control register |
| TCPWM1_GRP0_CNT51_TR_OUT_SEL | 0x405819D4 | FULL | Counter output trigger selection register |
| TCPWM1_GRP0_CNT51_INTR | 0x405819F0 | FULL | Interrupt request register |
| TCPWM1_GRP0_CNT51_INTR_SET | 0x405819F4 | FULL | Interrupt set request register |
| TCPWM1_GRP0_CNT51_INTR_MASK | 0x405819F8 | FULL | Interrupt mask register |
| TCPWM1_GRP0_CNT51_INTR_MASKED | 0x405819FC | FULL | Interrupt masked request register |

### 33.2.1.53 CNT 52

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT52_CTRL | 0x40581A00 | FULL | Counter control register<br>Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM1_GRP0_CNT52_STATUS | 0x40581A04 | FULL | Counter status register<br>Note:DT_CNT_H is not available for this register |
| TCPWM1_GRP0_CNT52_COUNTER | 0x40581A08 | FULL | Counter count register |
| TCPWM1_GRP0_CNT52_CC0 | 0x40581A10 | FULL | Counter compare/capture 0 register |
| TCPWM1_GRP0_CNT52_CC0_BUFF | 0x40581A14 | FULL | Counter buffered compare/capture 0 register |
| TCPWM1_GRP0_CNT52_CC1 | 0x40581A18 | FULL | Counter compare/capture 1 register |
| TCPWM1_GRP0_CNT52_CC1_BUFF | 0x40581A1C | FULL | Counter buffered compare/capture 1 register |
| TCPWM1_GRP0_CNT52_PERIOD | 0x40581A20 | FULL | Counter period register |
| TCPWM1_GRP0_CNT52_PERIOD_BUFF | 0x40581A24 | FULL | Counter buffered period register |
| TCPWM1_GRP0_CNT52_DT | 0x40581A30 | FULL | Counter PWM dead time register<br>Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM1_GRP0_CNT52_TR_CMD | 0x40581A40 | FULL | Counter trigger command register |
| TCPWM1_GRP0_CNT52_TR_IN_SEL0 | 0x40581A44 | FULL | Counter input trigger selection register 0 |
| TCPWM1_GRP0_CNT52_TR_IN_SEL1 | 0x40581A48 | FULL | Counter input trigger selection register 1 |
| TCPWM1_GRP0_CNT52_TR_IN_EDGE_SEL | 0x40581A4C | FULL | Counter input trigger edge selection register |
| TCPWM1_GRP0_CNT52_TR_PWM_CTRL | 0x40581A50 | FULL | Counter trigger PWM control register |
| TCPWM1_GRP0_CNT52_TR_OUT_SEL | 0x40581A54 | FULL | Counter output trigger selection register |
| TCPWM1_GRP0_CNT52_INTR | 0x40581A70 | FULL | Interrupt request register |
| TCPWM1_GRP0_CNT52_INTR_SET | 0x40581A74 | FULL | Interrupt set request register |
| TCPWM1_GRP0_CNT52_INTR_MASK | 0x40581A78 | FULL | Interrupt mask register |
| TCPWM1_GRP0_CNT52_INTR_MASKED | 0x40581A7C | FULL | Interrupt masked request register |

### 33.2.1.54 CNT 53

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT53_CTRL | 0x40581A80 | FULL | Counter control register<br>Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM1_GRP0_CNT53_STATUS | 0x40581A84 | FULL | Counter status register<br>Note:DT_CNT_H is not available for this register |
| TCPWM1_GRP0_CNT53_COUNTER | 0x40581A88 | FULL | Counter count register |
| TCPWM1_GRP0_CNT53_CC0 | 0x40581A90 | FULL | Counter compare/capture 0 register |
| TCPWM1_GRP0_CNT53_CC0_BUFF | 0x40581A94 | FULL | Counter buffered compare/capture 0 register |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT53_CC1 | 0x40581A98 | FULL | Counter compare/capture 1 register |
| TCPWM1_GRP0_CNT53_CC1_BUFF | 0x40581A9C | FULL | Counter buffered compare/capture 1 register |
| TCPWM1_GRP0_CNT53_PERIOD | 0x40581AA0 | FULL | Counter period register |
| TCPWM1_GRP0_CNT53_PERIOD_BUFF | 0x40581AA4 | FULL | Counter buffered period register |
| TCPWM1_GRP0_CNT53_DT | 0x40581AB0 | FULL | Counter PWM dead time register<br>Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM1_GRP0_CNT53_TR_CMD | 0x40581AC0 | FULL | Counter trigger command register |
| TCPWM1_GRP0_CNT53_TR_IN_SEL0 | 0x40581AC4 | FULL | Counter input trigger selection register 0 |
| TCPWM1_GRP0_CNT53_TR_IN_SEL1 | 0x40581AC8 | FULL | Counter input trigger selection register 1 |
| TCPWM1_GRP0_CNT53_TR_IN_EDGE_SEL | 0x40581ACC | FULL | Counter input trigger edge selection register |
| TCPWM1_GRP0_CNT53_TR_PWM_CTRL | 0x40581AD0 | FULL | Counter trigger PWM control register |
| TCPWM1_GRP0_CNT53_TR_OUT_SEL | 0x40581AD4 | FULL | Counter output trigger selection register |
| TCPWM1_GRP0_CNT53_INTR | 0x40581AF0 | FULL | Interrupt request register |
| TCPWM1_GRP0_CNT53_INTR_SET | 0x40581AF4 | FULL | Interrupt set request register |
| TCPWM1_GRP0_CNT53_INTR_MASK | 0x40581AF8 | FULL | Interrupt mask register |
| TCPWM1_GRP0_CNT53_INTR_MASKED | 0x40581AFC | FULL | Interrupt masked request register |

### 33.2.1.55 CNT 54

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT54_CTRL | 0x40581B00 | FULL | Counter control register<br>Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM1_GRP0_CNT54_STATUS | 0x40581B04 | FULL | Counter status register<br>Note:DT_CNT_H is not available for this register |
| TCPWM1_GRP0_CNT54_COUNTER | 0x40581B08 | FULL | Counter count register |
| TCPWM1_GRP0_CNT54_CC0 | 0x40581B10 | FULL | Counter compare/capture 0 register |
| TCPWM1_GRP0_CNT54_CC0_BUFF | 0x40581B14 | FULL | Counter buffered compare/capture 0 register |
| TCPWM1_GRP0_CNT54_CC1 | 0x40581B18 | FULL | Counter compare/capture 1 register |
| TCPWM1_GRP0_CNT54_CC1_BUFF | 0x40581B1C | FULL | Counter buffered compare/capture 1 register |
| TCPWM1_GRP0_CNT54_PERIOD | 0x40581B20 | FULL | Counter period register |
| TCPWM1_GRP0_CNT54_PERIOD_BUFF | 0x40581B24 | FULL | Counter buffered period register |
| TCPWM1_GRP0_CNT54_DT | 0x40581B30 | FULL | Counter PWM dead time register<br>Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM1_GRP0_CNT54_TR_CMD | 0x40581B40 | FULL | Counter trigger command register |
| TCPWM1_GRP0_CNT54_TR_IN_SEL0 | 0x40581B44 | FULL | Counter input trigger selection register 0 |
| TCPWM1_GRP0_CNT54_TR_IN_SEL1 | 0x40581B48 | FULL | Counter input trigger selection register 1 |
| TCPWM1_GRP0_CNT54_TR_IN_EDGE_SEL | 0x40581B4C | FULL | Counter input trigger edge selection register |
| TCPWM1_GRP0_CNT54_TR_PWM_CTRL | 0x40581B50 | FULL | Counter trigger PWM control register |
| TCPWM1_GRP0_CNT54_TR_OUT_SEL | 0x40581B54 | FULL | Counter output trigger selection register |
| TCPWM1_GRP0_CNT54_INTR | 0x40581B70 | FULL | Interrupt request register |
| TCPWM1_GRP0_CNT54_INTR_SET | 0x40581B74 | FULL | Interrupt set request register |
| TCPWM1_GRP0_CNT54_INTR_MASK | 0x40581B78 | FULL | Interrupt mask register |
| TCPWM1_GRP0_CNT54_INTR_MASKED | 0x40581B7C | FULL | Interrupt masked request register |

### 33.2.1.56 CNT 55

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT55_CTRL | 0x40581B80 | FULL | Counter control register<br>Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM1_GRP0_CNT55_STATUS | 0x40581B84 | FULL | Counter status register<br>Note:DT_CNT_H is not available for this register |
| TCPWM1_GRP0_CNT55_COUNTER | 0x40581B88 | FULL | Counter count register |
| TCPWM1_GRP0_CNT55_CC0 | 0x40581B90 | FULL | Counter compare/capture 0 register |
| TCPWM1_GRP0_CNT55_CC0_BUFF | 0x40581B94 | FULL | Counter buffered compare/capture 0 register |
| TCPWM1_GRP0_CNT55_CC1 | 0x40581B98 | FULL | Counter compare/capture 1 register |
| TCPWM1_GRP0_CNT55_CC1_BUFF | 0x40581B9C | FULL | Counter buffered compare/capture 1 register |
| TCPWM1_GRP0_CNT55_PERIOD | 0x40581BA0 | FULL | Counter period register |
| TCPWM1_GRP0_CNT55_PERIOD_BUFF | 0x40581BA4 | FULL | Counter buffered period register |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT55_DT | 0x40581BB0 | FULL | Counter PWM dead time register<br>Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM1_GRP0_CNT55_TR_CMD | 0x40581BC0 | FULL | Counter trigger command register |
| TCPWM1_GRP0_CNT55_TR_IN_SEL0 | 0x40581BC4 | FULL | Counter input trigger selection register 0 |
| TCPWM1_GRP0_CNT55_TR_IN_SEL1 | 0x40581BC8 | FULL | Counter input trigger selection register 1 |
| TCPWM1_GRP0_CNT55_TR_IN_EDGE_SEL | 0x40581BCC | FULL | Counter input trigger edge selection register |
| TCPWM1_GRP0_CNT55_TR_PWM_CTRL | 0x40581BD0 | FULL | Counter trigger PWM control register |
| TCPWM1_GRP0_CNT55_TR_OUT_SEL | 0x40581BD4 | FULL | Counter output trigger selection register |
| TCPWM1_GRP0_CNT55_INTR | 0x40581BF0 | FULL | Interrupt request register |
| TCPWM1_GRP0_CNT55_INTR_SET | 0x40581BF4 | FULL | Interrupt set request register |
| TCPWM1_GRP0_CNT55_INTR_MASK | 0x40581BF8 | FULL | Interrupt mask register |
| TCPWM1_GRP0_CNT55_INTR_MASKED | 0x40581BFC | FULL | Interrupt masked request register |

### 33.2.1.57 CNT 56

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT56_CTRL | 0x40581C00 | FULL | Counter control register<br>Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM1_GRP0_CNT56_STATUS | 0x40581C04 | FULL | Counter status register<br>Note:DT_CNT_H is not available for this register |
| TCPWM1_GRP0_CNT56_COUNTER | 0x40581C08 | FULL | Counter count register |
| TCPWM1_GRP0_CNT56_CC0 | 0x40581C10 | FULL | Counter compare/capture 0 register |
| TCPWM1_GRP0_CNT56_CC0_BUFF | 0x40581C14 | FULL | Counter buffered compare/capture 0 register |
| TCPWM1_GRP0_CNT56_CC1 | 0x40581C18 | FULL | Counter compare/capture 1 register |
| TCPWM1_GRP0_CNT56_CC1_BUFF | 0x40581C1C | FULL | Counter buffered compare/capture 1 register |
| TCPWM1_GRP0_CNT56_PERIOD | 0x40581C20 | FULL | Counter period register |
| TCPWM1_GRP0_CNT56_PERIOD_BUFF | 0x40581C24 | FULL | Counter buffered period register |
| TCPWM1_GRP0_CNT56_DT | 0x40581C30 | FULL | Counter PWM dead time register<br>Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM1_GRP0_CNT56_TR_CMD | 0x40581C40 | FULL | Counter trigger command register |
| TCPWM1_GRP0_CNT56_TR_IN_SEL0 | 0x40581C44 | FULL | Counter input trigger selection register 0 |
| TCPWM1_GRP0_CNT56_TR_IN_SEL1 | 0x40581C48 | FULL | Counter input trigger selection register 1 |
| TCPWM1_GRP0_CNT56_TR_IN_EDGE_SEL | 0x40581C4C | FULL | Counter input trigger edge selection register |
| TCPWM1_GRP0_CNT56_TR_PWM_CTRL | 0x40581C50 | FULL | Counter trigger PWM control register |
| TCPWM1_GRP0_CNT56_TR_OUT_SEL | 0x40581C54 | FULL | Counter output trigger selection register |
| TCPWM1_GRP0_CNT56_INTR | 0x40581C70 | FULL | Interrupt request register |
| TCPWM1_GRP0_CNT56_INTR_SET | 0x40581C74 | FULL | Interrupt set request register |
| TCPWM1_GRP0_CNT56_INTR_MASK | 0x40581C78 | FULL | Interrupt mask register |
| TCPWM1_GRP0_CNT56_INTR_MASKED | 0x40581C7C | FULL | Interrupt masked request register |

### 33.2.1.58 CNT 57

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT57_CTRL | 0x40581C80 | FULL | Counter control register<br>Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM1_GRP0_CNT57_STATUS | 0x40581C84 | FULL | Counter status register<br>Note:DT_CNT_H is not available for this register |
| TCPWM1_GRP0_CNT57_COUNTER | 0x40581C88 | FULL | Counter count register |
| TCPWM1_GRP0_CNT57_CC0 | 0x40581C90 | FULL | Counter compare/capture 0 register |
| TCPWM1_GRP0_CNT57_CC0_BUFF | 0x40581C94 | FULL | Counter buffered compare/capture 0 register |
| TCPWM1_GRP0_CNT57_CC1 | 0x40581C98 | FULL | Counter compare/capture 1 register |
| TCPWM1_GRP0_CNT57_CC1_BUFF | 0x40581C9C | FULL | Counter buffered compare/capture 1 register |
| TCPWM1_GRP0_CNT57_PERIOD | 0x40581CA0 | FULL | Counter period register |
| TCPWM1_GRP0_CNT57_PERIOD_BUFF | 0x40581CA4 | FULL | Counter buffered period register |
| TCPWM1_GRP0_CNT57_DT | 0x40581CB0 | FULL | Counter PWM dead time register<br>Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM1_GRP0_CNT57_TR_CMD | 0x40581CC0 | FULL | Counter trigger command register |
| TCPWM1_GRP0_CNT57_TR_IN_SEL0 | 0x40581CC4 | FULL | Counter input trigger selection register 0 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT57_TR_IN_SEL1 | 0x40581CC8 | FULL | Counter input trigger selection register 1 |
| TCPWM1_GRP0_CNT57_TR_IN_EDGE_SEL | 0x40581CCC | FULL | Counter input trigger edge selection register |
| TCPWM1_GRP0_CNT57_TR_PWM_CTRL | 0x40581CD0 | FULL | Counter trigger PWM control register |
| TCPWM1_GRP0_CNT57_TR_OUT_SEL | 0x40581CD4 | FULL | Counter output trigger selection register |
| TCPWM1_GRP0_CNT57_INTR | 0x40581CF0 | FULL | Interrupt request register |
| TCPWM1_GRP0_CNT57_INTR_SET | 0x40581CF4 | FULL | Interrupt set request register |
| TCPWM1_GRP0_CNT57_INTR_MASK | 0x40581CF8 | FULL | Interrupt mask register |
| TCPWM1_GRP0_CNT57_INTR_MASKED | 0x40581CFC | FULL | Interrupt masked request register |

### 33.2.1.59 CNT 58

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT58_CTRL | 0x40581D00 | FULL | Counter control register<br>Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM1_GRP0_CNT58_STATUS | 0x40581D04 | FULL | Counter status register<br>Note:DT_CNT_H is not available for this register |
| TCPWM1_GRP0_CNT58_COUNTER | 0x40581D08 | FULL | Counter count register |
| TCPWM1_GRP0_CNT58_CC0 | 0x40581D10 | FULL | Counter compare/capture 0 register |
| TCPWM1_GRP0_CNT58_CC0_BUFF | 0x40581D14 | FULL | Counter buffered compare/capture 0 register |
| TCPWM1_GRP0_CNT58_CC1 | 0x40581D18 | FULL | Counter compare/capture 1 register |
| TCPWM1_GRP0_CNT58_CC1_BUFF | 0x40581D1C | FULL | Counter buffered compare/capture 1 register |
| TCPWM1_GRP0_CNT58_PERIOD | 0x40581D20 | FULL | Counter period register |
| TCPWM1_GRP0_CNT58_PERIOD_BUFF | 0x40581D24 | FULL | Counter buffered period register |
| TCPWM1_GRP0_CNT58_DT | 0x40581D30 | FULL | Counter PWM dead time register<br>Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM1_GRP0_CNT58_TR_CMD | 0x40581D40 | FULL | Counter trigger command register |
| TCPWM1_GRP0_CNT58_TR_IN_SEL0 | 0x40581D44 | FULL | Counter input trigger selection register 0 |
| TCPWM1_GRP0_CNT58_TR_IN_SEL1 | 0x40581D48 | FULL | Counter input trigger selection register 1 |
| TCPWM1_GRP0_CNT58_TR_IN_EDGE_SEL | 0x40581D4C | FULL | Counter input trigger edge selection register |
| TCPWM1_GRP0_CNT58_TR_PWM_CTRL | 0x40581D50 | FULL | Counter trigger PWM control register |
| TCPWM1_GRP0_CNT58_TR_OUT_SEL | 0x40581D54 | FULL | Counter output trigger selection register |
| TCPWM1_GRP0_CNT58_INTR | 0x40581D70 | FULL | Interrupt request register |
| TCPWM1_GRP0_CNT58_INTR_SET | 0x40581D74 | FULL | Interrupt set request register |
| TCPWM1_GRP0_CNT58_INTR_MASK | 0x40581D78 | FULL | Interrupt mask register |
| TCPWM1_GRP0_CNT58_INTR_MASKED | 0x40581D7C | FULL | Interrupt masked request register |

### 33.2.1.60 CNT 59

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT59_CTRL | 0x40581D80 | FULL | Counter control register<br>Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM1_GRP0_CNT59_STATUS | 0x40581D84 | FULL | Counter status register<br>Note:DT_CNT_H is not available for this register |
| TCPWM1_GRP0_CNT59_COUNTER | 0x40581D88 | FULL | Counter count register |
| TCPWM1_GRP0_CNT59_CC0 | 0x40581D90 | FULL | Counter compare/capture 0 register |
| TCPWM1_GRP0_CNT59_CC0_BUFF | 0x40581D94 | FULL | Counter buffered compare/capture 0 register |
| TCPWM1_GRP0_CNT59_CC1 | 0x40581D98 | FULL | Counter compare/capture 1 register |
| TCPWM1_GRP0_CNT59_CC1_BUFF | 0x40581D9C | FULL | Counter buffered compare/capture 1 register |
| TCPWM1_GRP0_CNT59_PERIOD | 0x40581DA0 | FULL | Counter period register |
| TCPWM1_GRP0_CNT59_PERIOD_BUFF | 0x40581DA4 | FULL | Counter buffered period register |
| TCPWM1_GRP0_CNT59_DT | 0x40581DB0 | FULL | Counter PWM dead time register<br>Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM1_GRP0_CNT59_TR_CMD | 0x40581DC0 | FULL | Counter trigger command register |
| TCPWM1_GRP0_CNT59_TR_IN_SEL0 | 0x40581DC4 | FULL | Counter input trigger selection register 0 |
| TCPWM1_GRP0_CNT59_TR_IN_SEL1 | 0x40581DC8 | FULL | Counter input trigger selection register 1 |
| TCPWM1_GRP0_CNT59_TR_IN_EDGE_SEL | 0x40581DCC | FULL | Counter input trigger edge selection register |
| TCPWM1_GRP0_CNT59_TR_PWM_CTRL | 0x40581DD0 | FULL | Counter trigger PWM control register |
| TCPWM1_GRP0_CNT59_TR_OUT_SEL | 0x40581DD4 | FULL | Counter output trigger selection register |
| TCPWM1_GRP0_CNT59_INTR | 0x40581DF0 | FULL | Interrupt request register |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT59_INTR_SET | 0x40581DF4 | FULL | Interrupt set request register |
| TCPWM1_GRP0_CNT59_INTR_MASK | 0x40581DF8 | FULL | Interrupt mask register |
| TCPWM1_GRP0_CNT59_INTR_MASKED | 0x40581DFC | FULL | Interrupt masked request register |

### 33.2.1.61 CNT 60

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT60_CTRL | 0x40581E00 | FULL | Counter control register<br>Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM1_GRP0_CNT60_STATUS | 0x40581E04 | FULL | Counter status register<br>Note:DT_CNT_H is not available for this register |
| TCPWM1_GRP0_CNT60_COUNTER | 0x40581E08 | FULL | Counter count register |
| TCPWM1_GRP0_CNT60_CC0 | 0x40581E10 | FULL | Counter compare/capture 0 register |
| TCPWM1_GRP0_CNT60_CC0_BUFF | 0x40581E14 | FULL | Counter buffered compare/capture 0 register |
| TCPWM1_GRP0_CNT60_CC1 | 0x40581E18 | FULL | Counter compare/capture 1 register |
| TCPWM1_GRP0_CNT60_CC1_BUFF | 0x40581E1C | FULL | Counter buffered compare/capture 1 register |
| TCPWM1_GRP0_CNT60_PERIOD | 0x40581E20 | FULL | Counter period register |
| TCPWM1_GRP0_CNT60_PERIOD_BUFF | 0x40581E24 | FULL | Counter buffered period register |
| TCPWM1_GRP0_CNT60_DT | 0x40581E30 | FULL | Counter PWM dead time register<br>Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM1_GRP0_CNT60_TR_CMD | 0x40581E40 | FULL | Counter trigger command register |
| TCPWM1_GRP0_CNT60_TR_IN_SEL0 | 0x40581E44 | FULL | Counter input trigger selection register 0 |
| TCPWM1_GRP0_CNT60_TR_IN_SEL1 | 0x40581E48 | FULL | Counter input trigger selection register 1 |
| TCPWM1_GRP0_CNT60_TR_IN_EDGE_SEL | 0x40581E4C | FULL | Counter input trigger edge selection register |
| TCPWM1_GRP0_CNT60_TR_PWM_CTRL | 0x40581E50 | FULL | Counter trigger PWM control register |
| TCPWM1_GRP0_CNT60_TR_OUT_SEL | 0x40581E54 | FULL | Counter output trigger selection register |
| TCPWM1_GRP0_CNT60_INTR | 0x40581E70 | FULL | Interrupt request register |
| TCPWM1_GRP0_CNT60_INTR_SET | 0x40581E74 | FULL | Interrupt set request register |
| TCPWM1_GRP0_CNT60_INTR_MASK | 0x40581E78 | FULL | Interrupt mask register |
| TCPWM1_GRP0_CNT60_INTR_MASKED | 0x40581E7C | FULL | Interrupt masked request register |

### 33.2.1.62 CNT 61

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT61_CTRL | 0x40581E80 | FULL | Counter control register<br>Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM1_GRP0_CNT61_STATUS | 0x40581E84 | FULL | Counter status register<br>Note:DT_CNT_H is not available for this register |
| TCPWM1_GRP0_CNT61_COUNTER | 0x40581E88 | FULL | Counter count register |
| TCPWM1_GRP0_CNT61_CC0 | 0x40581E90 | FULL | Counter compare/capture 0 register |
| TCPWM1_GRP0_CNT61_CC0_BUFF | 0x40581E94 | FULL | Counter buffered compare/capture 0 register |
| TCPWM1_GRP0_CNT61_CC1 | 0x40581E98 | FULL | Counter compare/capture 1 register |
| TCPWM1_GRP0_CNT61_CC1_BUFF | 0x40581E9C | FULL | Counter buffered compare/capture 1 register |
| TCPWM1_GRP0_CNT61_PERIOD | 0x40581EA0 | FULL | Counter period register |
| TCPWM1_GRP0_CNT61_PERIOD_BUFF | 0x40581EA4 | FULL | Counter buffered period register |
| TCPWM1_GRP0_CNT61_DT | 0x40581EB0 | FULL | Counter PWM dead time register<br>Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM1_GRP0_CNT61_TR_CMD | 0x40581EC0 | FULL | Counter trigger command register |
| TCPWM1_GRP0_CNT61_TR_IN_SEL0 | 0x40581EC4 | FULL | Counter input trigger selection register 0 |
| TCPWM1_GRP0_CNT61_TR_IN_SEL1 | 0x40581EC8 | FULL | Counter input trigger selection register 1 |
| TCPWM1_GRP0_CNT61_TR_IN_EDGE_SEL | 0x40581ECC | FULL | Counter input trigger edge selection register |
| TCPWM1_GRP0_CNT61_TR_PWM_CTRL | 0x40581ED0 | FULL | Counter trigger PWM control register |
| TCPWM1_GRP0_CNT61_TR_OUT_SEL | 0x40581ED4 | FULL | Counter output trigger selection register |
| TCPWM1_GRP0_CNT61_INTR | 0x40581EF0 | FULL | Interrupt request register |
| TCPWM1_GRP0_CNT61_INTR_SET | 0x40581EF4 | FULL | Interrupt set request register |
| TCPWM1_GRP0_CNT61_INTR_MASK | 0x40581EF8 | FULL | Interrupt mask register |
| TCPWM1_GRP0_CNT61_INTR_MASKED | 0x40581EFC | FULL | Interrupt masked request register |

### 33.2.1.63 CNT 62

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT62_CTRL | 0x40581F00 | FULL | Counter control register<br>Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM1_GRP0_CNT62_STATUS | 0x40581F04 | FULL | Counter status register<br>Note:DT_CNT_H is not available for this register |
| TCPWM1_GRP0_CNT62_COUNTER | 0x40581F08 | FULL | Counter count register |
| TCPWM1_GRP0_CNT62_CC0 | 0x40581F10 | FULL | Counter compare/capture 0 register |
| TCPWM1_GRP0_CNT62_CC0_BUFF | 0x40581F14 | FULL | Counter buffered compare/capture 0 register |
| TCPWM1_GRP0_CNT62_CC1 | 0x40581F18 | FULL | Counter compare/capture 1 register |
| TCPWM1_GRP0_CNT62_CC1_BUFF | 0x40581F1C | FULL | Counter buffered compare/capture 1 register |
| TCPWM1_GRP0_CNT62_PERIOD | 0x40581F20 | FULL | Counter period register |
| TCPWM1_GRP0_CNT62_PERIOD_BUFF | 0x40581F24 | FULL | Counter buffered period register |
| TCPWM1_GRP0_CNT62_DT | 0x40581F30 | FULL | Counter PWM dead time register<br>Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM1_GRP0_CNT62_TR_CMD | 0x40581F40 | FULL | Counter trigger command register |
| TCPWM1_GRP0_CNT62_TR_IN_SEL0 | 0x40581F44 | FULL | Counter input trigger selection register 0 |
| TCPWM1_GRP0_CNT62_TR_IN_SEL1 | 0x40581F48 | FULL | Counter input trigger selection register 1 |
| TCPWM1_GRP0_CNT62_TR_IN_EDGE_SEL | 0x40581F4C | FULL | Counter input trigger edge selection register |
| TCPWM1_GRP0_CNT62_TR_PWM_CTRL | 0x40581F50 | FULL | Counter trigger PWM control register |
| TCPWM1_GRP0_CNT62_TR_OUT_SEL | 0x40581F54 | FULL | Counter output trigger selection register |
| TCPWM1_GRP0_CNT62_INTR | 0x40581F70 | FULL | Interrupt request register |
| TCPWM1_GRP0_CNT62_INTR_SET | 0x40581F74 | FULL | Interrupt set request register |
| TCPWM1_GRP0_CNT62_INTR_MASK | 0x40581F78 | FULL | Interrupt mask register |
| TCPWM1_GRP0_CNT62_INTR_MASKED | 0x40581F7C | FULL | Interrupt masked request register |

### 33.2.1.64 CNT 63

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT63_CTRL | 0x40581F80 | FULL | Counter control register<br>Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM1_GRP0_CNT63_STATUS | 0x40581F84 | FULL | Counter status register<br>Note:DT_CNT_H is not available for this register |
| TCPWM1_GRP0_CNT63_COUNTER | 0x40581F88 | FULL | Counter count register |
| TCPWM1_GRP0_CNT63_CC0 | 0x40581F90 | FULL | Counter compare/capture 0 register |
| TCPWM1_GRP0_CNT63_CC0_BUFF | 0x40581F94 | FULL | Counter buffered compare/capture 0 register |
| TCPWM1_GRP0_CNT63_CC1 | 0x40581F98 | FULL | Counter compare/capture 1 register |
| TCPWM1_GRP0_CNT63_CC1_BUFF | 0x40581F9C | FULL | Counter buffered compare/capture 1 register |
| TCPWM1_GRP0_CNT63_PERIOD | 0x40581FA0 | FULL | Counter period register |
| TCPWM1_GRP0_CNT63_PERIOD_BUFF | 0x40581FA4 | FULL | Counter buffered period register |
| TCPWM1_GRP0_CNT63_DT | 0x40581FB0 | FULL | Counter PWM dead time register<br>Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM1_GRP0_CNT63_TR_CMD | 0x40581FC0 | FULL | Counter trigger command register |
| TCPWM1_GRP0_CNT63_TR_IN_SEL0 | 0x40581FC4 | FULL | Counter input trigger selection register 0 |
| TCPWM1_GRP0_CNT63_TR_IN_SEL1 | 0x40581FC8 | FULL | Counter input trigger selection register 1 |
| TCPWM1_GRP0_CNT63_TR_IN_EDGE_SEL | 0x40581FCC | FULL | Counter input trigger edge selection register |
| TCPWM1_GRP0_CNT63_TR_PWM_CTRL | 0x40581FD0 | FULL | Counter trigger PWM control register |
| TCPWM1_GRP0_CNT63_TR_OUT_SEL | 0x40581FD4 | FULL | Counter output trigger selection register |
| TCPWM1_GRP0_CNT63_INTR | 0x40581FF0 | FULL | Interrupt request register |
| TCPWM1_GRP0_CNT63_INTR_SET | 0x40581FF4 | FULL | Interrupt set request register |
| TCPWM1_GRP0_CNT63_INTR_MASK | 0x40581FF8 | FULL | Interrupt mask register |
| TCPWM1_GRP0_CNT63_INTR_MASKED | 0x40581FFC | FULL | Interrupt masked request register |

### 33.2.1.65 CNT 64

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT64_CTRL | 0x40582000 | FULL | Counter control register<br>Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT64_STATUS | 0x40582004 | FULL | Counter status register<br>Note:DT_CNT_H is not available for this register |
| TCPWM1_GRP0_CNT64_COUNTER | 0x40582008 | FULL | Counter count register |
| TCPWM1_GRP0_CNT64_CC0 | 0x40582010 | FULL | Counter compare/capture 0 register |
| TCPWM1_GRP0_CNT64_CC0_BUFF | 0x40582014 | FULL | Counter buffered compare/capture 0 register |
| TCPWM1_GRP0_CNT64_CC1 | 0x40582018 | FULL | Counter compare/capture 1 register |
| TCPWM1_GRP0_CNT64_CC1_BUFF | 0x4058201C | FULL | Counter buffered compare/capture 1 register |
| TCPWM1_GRP0_CNT64_PERIOD | 0x40582020 | FULL | Counter period register |
| TCPWM1_GRP0_CNT64_PERIOD_BUFF | 0x40582024 | FULL | Counter buffered period register |
| TCPWM1_GRP0_CNT64_DT | 0x40582030 | FULL | Counter PWM dead time register<br>Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM1_GRP0_CNT64_TR_CMD | 0x40582040 | FULL | Counter trigger command register |
| TCPWM1_GRP0_CNT64_TR_IN_SEL0 | 0x40582044 | FULL | Counter input trigger selection register 0 |
| TCPWM1_GRP0_CNT64_TR_IN_SEL1 | 0x40582048 | FULL | Counter input trigger selection register 1 |
| TCPWM1_GRP0_CNT64_TR_IN_EDGE_SEL | 0x4058204C | FULL | Counter input trigger edge selection register |
| TCPWM1_GRP0_CNT64_TR_PWM_CTRL | 0x40582050 | FULL | Counter trigger PWM control register |
| TCPWM1_GRP0_CNT64_TR_OUT_SEL | 0x40582054 | FULL | Counter output trigger selection register |
| TCPWM1_GRP0_CNT64_INTR | 0x40582070 | FULL | Interrupt request register |
| TCPWM1_GRP0_CNT64_INTR_SET | 0x40582074 | FULL | Interrupt set request register |
| TCPWM1_GRP0_CNT64_INTR_MASK | 0x40582078 | FULL | Interrupt mask register |
| TCPWM1_GRP0_CNT64_INTR_MASKED | 0x4058207C | FULL | Interrupt masked request register |

### 33.2.1.66 CNT 65

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT65_CTRL | 0x40582080 | FULL | Counter control register<br>Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM1_GRP0_CNT65_STATUS | 0x40582084 | FULL | Counter status register<br>Note:DT_CNT_H is not available for this register |
| TCPWM1_GRP0_CNT65_COUNTER | 0x40582088 | FULL | Counter count register |
| TCPWM1_GRP0_CNT65_CC0 | 0x40582090 | FULL | Counter compare/capture 0 register |
| TCPWM1_GRP0_CNT65_CC0_BUFF | 0x40582094 | FULL | Counter buffered compare/capture 0 register |
| TCPWM1_GRP0_CNT65_CC1 | 0x40582098 | FULL | Counter compare/capture 1 register |
| TCPWM1_GRP0_CNT65_CC1_BUFF | 0x4058209C | FULL | Counter buffered compare/capture 1 register |
| TCPWM1_GRP0_CNT65_PERIOD | 0x405820A0 | FULL | Counter period register |
| TCPWM1_GRP0_CNT65_PERIOD_BUFF | 0x405820A4 | FULL | Counter buffered period register |
| TCPWM1_GRP0_CNT65_DT | 0x405820B0 | FULL | Counter PWM dead time register<br>Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM1_GRP0_CNT65_TR_CMD | 0x405820C0 | FULL | Counter trigger command register |
| TCPWM1_GRP0_CNT65_TR_IN_SEL0 | 0x405820C4 | FULL | Counter input trigger selection register 0 |
| TCPWM1_GRP0_CNT65_TR_IN_SEL1 | 0x405820C8 | FULL | Counter input trigger selection register 1 |
| TCPWM1_GRP0_CNT65_TR_IN_EDGE_SEL | 0x405820CC | FULL | Counter input trigger edge selection register |
| TCPWM1_GRP0_CNT65_TR_PWM_CTRL | 0x405820D0 | FULL | Counter trigger PWM control register |
| TCPWM1_GRP0_CNT65_TR_OUT_SEL | 0x405820D4 | FULL | Counter output trigger selection register |
| TCPWM1_GRP0_CNT65_INTR | 0x405820F0 | FULL | Interrupt request register |
| TCPWM1_GRP0_CNT65_INTR_SET | 0x405820F4 | FULL | Interrupt set request register |
| TCPWM1_GRP0_CNT65_INTR_MASK | 0x405820F8 | FULL | Interrupt mask register |
| TCPWM1_GRP0_CNT65_INTR_MASKED | 0x405820FC | FULL | Interrupt masked request register |

### 33.2.1.67 CNT 66

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT66_CTRL | 0x40582100 | FULL | Counter control register<br>Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM1_GRP0_CNT66_STATUS | 0x40582104 | FULL | Counter status register<br>Note:DT_CNT_H is not available for this register |
| TCPWM1_GRP0_CNT66_COUNTER | 0x40582108 | FULL | Counter count register |
| TCPWM1_GRP0_CNT66_CC0 | 0x40582110 | FULL | Counter compare/capture 0 register |
| TCPWM1_GRP0_CNT66_CC0_BUFF | 0x40582114 | FULL | Counter buffered compare/capture 0 register |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT66_CC1 | 0x40582118 | FULL | Counter compare/capture 1 register |
| TCPWM1_GRP0_CNT66_CC1_BUFF | 0x4058211C | FULL | Counter buffered compare/capture 1 register |
| TCPWM1_GRP0_CNT66_PERIOD | 0x40582120 | FULL | Counter period register |
| TCPWM1_GRP0_CNT66_PERIOD_BUFF | 0x40582124 | FULL | Counter buffered period register |
| TCPWM1_GRP0_CNT66_DT | 0x40582130 | FULL | Counter PWM dead time register Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM1_GRP0_CNT66_TR_CMD | 0x40582140 | FULL | Counter trigger command register |
| TCPWM1_GRP0_CNT66_TR_IN_SEL0 | 0x40582144 | FULL | Counter input trigger selection register 0 |
| TCPWM1_GRP0_CNT66_TR_IN_SEL1 | 0x40582148 | FULL | Counter input trigger selection register 1 |
| TCPWM1_GRP0_CNT66_TR_IN_EDGE_SEL | 0x4058214C | FULL | Counter input trigger edge selection register |
| TCPWM1_GRP0_CNT66_TR_PWM_CTRL | 0x40582150 | FULL | Counter trigger PWM control register |
| TCPWM1_GRP0_CNT66_TR_OUT_SEL | 0x40582154 | FULL | Counter output trigger selection register |
| TCPWM1_GRP0_CNT66_INTR | 0x40582170 | FULL | Interrupt request register |
| TCPWM1_GRP0_CNT66_INTR_SET | 0x40582174 | FULL | Interrupt set request register |
| TCPWM1_GRP0_CNT66_INTR_MASK | 0x40582178 | FULL | Interrupt mask register |
| TCPWM1_GRP0_CNT66_INTR_MASKED | 0x4058217C | FULL | Interrupt masked request register |

### 33.2.1.68 CNT 67

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT67_CTRL | 0x40582180 | FULL | Counter control register Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM1_GRP0_CNT67_STATUS | 0x40582184 | FULL | Counter status register Note:DT_CNT_H is not available for this register |
| TCPWM1_GRP0_CNT67_COUNTER | 0x40582188 | FULL | Counter count register |
| TCPWM1_GRP0_CNT67_CC0 | 0x40582190 | FULL | Counter compare/capture 0 register |
| TCPWM1_GRP0_CNT67_CC0_BUFF | 0x40582194 | FULL | Counter buffered compare/capture 0 register |
| TCPWM1_GRP0_CNT67_CC1 | 0x40582198 | FULL | Counter compare/capture 1 register |
| TCPWM1_GRP0_CNT67_CC1_BUFF | 0x4058219C | FULL | Counter buffered compare/capture 1 register |
| TCPWM1_GRP0_CNT67_PERIOD | 0x405821A0 | FULL | Counter period register |
| TCPWM1_GRP0_CNT67_PERIOD_BUFF | 0x405821A4 | FULL | Counter buffered period register |
| TCPWM1_GRP0_CNT67_DT | 0x405821B0 | FULL | Counter PWM dead time register Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM1_GRP0_CNT67_TR_CMD | 0x405821C0 | FULL | Counter trigger command register |
| TCPWM1_GRP0_CNT67_TR_IN_SEL0 | 0x405821C4 | FULL | Counter input trigger selection register 0 |
| TCPWM1_GRP0_CNT67_TR_IN_SEL1 | 0x405821C8 | FULL | Counter input trigger selection register 1 |
| TCPWM1_GRP0_CNT67_TR_IN_EDGE_SEL | 0x405821CC | FULL | Counter input trigger edge selection register |
| TCPWM1_GRP0_CNT67_TR_PWM_CTRL | 0x405821D0 | FULL | Counter trigger PWM control register |
| TCPWM1_GRP0_CNT67_TR_OUT_SEL | 0x405821D4 | FULL | Counter output trigger selection register |
| TCPWM1_GRP0_CNT67_INTR | 0x405821F0 | FULL | Interrupt request register |
| TCPWM1_GRP0_CNT67_INTR_SET | 0x405821F4 | FULL | Interrupt set request register |
| TCPWM1_GRP0_CNT67_INTR_MASK | 0x405821F8 | FULL | Interrupt mask register |
| TCPWM1_GRP0_CNT67_INTR_MASKED | 0x405821FC | FULL | Interrupt masked request register |

### 33.2.1.69 CNT 68

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT68_CTRL | 0x40582200 | FULL | Counter control register Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM1_GRP0_CNT68_STATUS | 0x40582204 | FULL | Counter status register Note:DT_CNT_H is not available for this register |
| TCPWM1_GRP0_CNT68_COUNTER | 0x40582208 | FULL | Counter count register |
| TCPWM1_GRP0_CNT68_CC0 | 0x40582210 | FULL | Counter compare/capture 0 register |
| TCPWM1_GRP0_CNT68_CC0_BUFF | 0x40582214 | FULL | Counter buffered compare/capture 0 register |
| TCPWM1_GRP0_CNT68_CC1 | 0x40582218 | FULL | Counter compare/capture 1 register |
| TCPWM1_GRP0_CNT68_CC1_BUFF | 0x4058221C | FULL | Counter buffered compare/capture 1 register |
| TCPWM1_GRP0_CNT68_PERIOD | 0x40582220 | FULL | Counter period register |
| TCPWM1_GRP0_CNT68_PERIOD_BUFF | 0x40582224 | FULL | Counter buffered period register |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT68_DT | 0x40582230 | FULL | Counter PWM dead time register<br>Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM1_GRP0_CNT68_TR_CMD | 0x40582240 | FULL | Counter trigger command register |
| TCPWM1_GRP0_CNT68_TR_IN_SEL0 | 0x40582244 | FULL | Counter input trigger selection register 0 |
| TCPWM1_GRP0_CNT68_TR_IN_SEL1 | 0x40582248 | FULL | Counter input trigger selection register 1 |
| TCPWM1_GRP0_CNT68_TR_IN_EDGE_SEL | 0x4058224C | FULL | Counter input trigger edge selection register |
| TCPWM1_GRP0_CNT68_TR_PWM_CTRL | 0x40582250 | FULL | Counter trigger PWM control register |
| TCPWM1_GRP0_CNT68_TR_OUT_SEL | 0x40582254 | FULL | Counter output trigger selection register |
| TCPWM1_GRP0_CNT68_INTR | 0x40582270 | FULL | Interrupt request register |
| TCPWM1_GRP0_CNT68_INTR_SET | 0x40582274 | FULL | Interrupt set request register |
| TCPWM1_GRP0_CNT68_INTR_MASK | 0x40582278 | FULL | Interrupt mask register |
| TCPWM1_GRP0_CNT68_INTR_MASKED | 0x4058227C | FULL | Interrupt masked request register |

### 33.2.1.70 CNT 69

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT69_CTRL | 0x40582280 | FULL | Counter control register<br>Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM1_GRP0_CNT69_STATUS | 0x40582284 | FULL | Counter status register<br>Note:DT_CNT_H is not available for this register |
| TCPWM1_GRP0_CNT69_COUNTER | 0x40582288 | FULL | Counter count register |
| TCPWM1_GRP0_CNT69_CC0 | 0x40582290 | FULL | Counter compare/capture 0 register |
| TCPWM1_GRP0_CNT69_CC0_BUFF | 0x40582294 | FULL | Counter buffered compare/capture 0 register |
| TCPWM1_GRP0_CNT69_CC1 | 0x40582298 | FULL | Counter compare/capture 1 register |
| TCPWM1_GRP0_CNT69_CC1_BUFF | 0x4058229C | FULL | Counter buffered compare/capture 1 register |
| TCPWM1_GRP0_CNT69_PERIOD | 0x405822A0 | FULL | Counter period register |
| TCPWM1_GRP0_CNT69_PERIOD_BUFF | 0x405822A4 | FULL | Counter buffered period register |
| TCPWM1_GRP0_CNT69_DT | 0x405822B0 | FULL | Counter PWM dead time register<br>Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM1_GRP0_CNT69_TR_CMD | 0x405822C0 | FULL | Counter trigger command register |
| TCPWM1_GRP0_CNT69_TR_IN_SEL0 | 0x405822C4 | FULL | Counter input trigger selection register 0 |
| TCPWM1_GRP0_CNT69_TR_IN_SEL1 | 0x405822C8 | FULL | Counter input trigger selection register 1 |
| TCPWM1_GRP0_CNT69_TR_IN_EDGE_SEL | 0x405822CC | FULL | Counter input trigger edge selection register |
| TCPWM1_GRP0_CNT69_TR_PWM_CTRL | 0x405822D0 | FULL | Counter trigger PWM control register |
| TCPWM1_GRP0_CNT69_TR_OUT_SEL | 0x405822D4 | FULL | Counter output trigger selection register |
| TCPWM1_GRP0_CNT69_INTR | 0x405822F0 | FULL | Interrupt request register |
| TCPWM1_GRP0_CNT69_INTR_SET | 0x405822F4 | FULL | Interrupt set request register |
| TCPWM1_GRP0_CNT69_INTR_MASK | 0x405822F8 | FULL | Interrupt mask register |
| TCPWM1_GRP0_CNT69_INTR_MASKED | 0x405822FC | FULL | Interrupt masked request register |

### 33.2.1.71 CNT 70

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT70_CTRL | 0x40582300 | FULL | Counter control register<br>Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM1_GRP0_CNT70_STATUS | 0x40582304 | FULL | Counter status register<br>Note:DT_CNT_H is not available for this register |
| TCPWM1_GRP0_CNT70_COUNTER | 0x40582308 | FULL | Counter count register |
| TCPWM1_GRP0_CNT70_CC0 | 0x40582310 | FULL | Counter compare/capture 0 register |
| TCPWM1_GRP0_CNT70_CC0_BUFF | 0x40582314 | FULL | Counter buffered compare/capture 0 register |
| TCPWM1_GRP0_CNT70_CC1 | 0x40582318 | FULL | Counter compare/capture 1 register |
| TCPWM1_GRP0_CNT70_CC1_BUFF | 0x4058231C | FULL | Counter buffered compare/capture 1 register |
| TCPWM1_GRP0_CNT70_PERIOD | 0x40582320 | FULL | Counter period register |
| TCPWM1_GRP0_CNT70_PERIOD_BUFF | 0x40582324 | FULL | Counter buffered period register |
| TCPWM1_GRP0_CNT70_DT | 0x40582330 | FULL | Counter PWM dead time register<br>Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM1_GRP0_CNT70_TR_CMD | 0x40582340 | FULL | Counter trigger command register |
| TCPWM1_GRP0_CNT70_TR_IN_SEL0 | 0x40582344 | FULL | Counter input trigger selection register 0 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT70_TR_IN_SEL1 | 0x40582348 | FULL | Counter input trigger selection register 1 |
| TCPWM1_GRP0_CNT70_TR_IN_EDGE_SEL | 0x4058234C | FULL | Counter input trigger edge selection register |
| TCPWM1_GRP0_CNT70_TR_PWM_CTRL | 0x40582350 | FULL | Counter trigger PWM control register |
| TCPWM1_GRP0_CNT70_TR_OUT_SEL | 0x40582354 | FULL | Counter output trigger selection register |
| TCPWM1_GRP0_CNT70_INTR | 0x40582370 | FULL | Interrupt request register |
| TCPWM1_GRP0_CNT70_INTR_SET | 0x40582374 | FULL | Interrupt set request register |
| TCPWM1_GRP0_CNT70_INTR_MASK | 0x40582378 | FULL | Interrupt mask register |
| TCPWM1_GRP0_CNT70_INTR_MASKED | 0x4058237C | FULL | Interrupt masked request register |

### 33.2.1.72 CNT 71

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT71_CTRL | 0x40582380 | FULL | Counter control register<br>Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM1_GRP0_CNT71_STATUS | 0x40582384 | FULL | Counter status register<br>Note:DT_CNT_H is not available for this register |
| TCPWM1_GRP0_CNT71_COUNTER | 0x40582388 | FULL | Counter count register |
| TCPWM1_GRP0_CNT71_CC0 | 0x40582390 | FULL | Counter compare/capture 0 register |
| TCPWM1_GRP0_CNT71_CC0_BUFF | 0x40582394 | FULL | Counter buffered compare/capture 0 register |
| TCPWM1_GRP0_CNT71_CC1 | 0x40582398 | FULL | Counter compare/capture 1 register |
| TCPWM1_GRP0_CNT71_CC1_BUFF | 0x4058239C | FULL | Counter buffered compare/capture 1 register |
| TCPWM1_GRP0_CNT71_PERIOD | 0x405823A0 | FULL | Counter period register |
| TCPWM1_GRP0_CNT71_PERIOD_BUFF | 0x405823A4 | FULL | Counter buffered period register |
| TCPWM1_GRP0_CNT71_DT | 0x405823B0 | FULL | Counter PWM dead time register<br>Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM1_GRP0_CNT71_TR_CMD | 0x405823C0 | FULL | Counter trigger command register |
| TCPWM1_GRP0_CNT71_TR_IN_SEL0 | 0x405823C4 | FULL | Counter input trigger selection register 0 |
| TCPWM1_GRP0_CNT71_TR_IN_SEL1 | 0x405823C8 | FULL | Counter input trigger selection register 1 |
| TCPWM1_GRP0_CNT71_TR_IN_EDGE_SEL | 0x405823CC | FULL | Counter input trigger edge selection register |
| TCPWM1_GRP0_CNT71_TR_PWM_CTRL | 0x405823D0 | FULL | Counter trigger PWM control register |
| TCPWM1_GRP0_CNT71_TR_OUT_SEL | 0x405823D4 | FULL | Counter output trigger selection register |
| TCPWM1_GRP0_CNT71_INTR | 0x405823F0 | FULL | Interrupt request register |
| TCPWM1_GRP0_CNT71_INTR_SET | 0x405823F4 | FULL | Interrupt set request register |
| TCPWM1_GRP0_CNT71_INTR_MASK | 0x405823F8 | FULL | Interrupt mask register |
| TCPWM1_GRP0_CNT71_INTR_MASKED | 0x405823FC | FULL | Interrupt masked request register |

### 33.2.1.73 CNT 72

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT72_CTRL | 0x40582400 | FULL | Counter control register<br>Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM1_GRP0_CNT72_STATUS | 0x40582404 | FULL | Counter status register<br>Note:DT_CNT_H is not available for this register |
| TCPWM1_GRP0_CNT72_COUNTER | 0x40582408 | FULL | Counter count register |
| TCPWM1_GRP0_CNT72_CC0 | 0x40582410 | FULL | Counter compare/capture 0 register |
| TCPWM1_GRP0_CNT72_CC0_BUFF | 0x40582414 | FULL | Counter buffered compare/capture 0 register |
| TCPWM1_GRP0_CNT72_CC1 | 0x40582418 | FULL | Counter compare/capture 1 register |
| TCPWM1_GRP0_CNT72_CC1_BUFF | 0x4058241C | FULL | Counter buffered compare/capture 1 register |
| TCPWM1_GRP0_CNT72_PERIOD | 0x40582420 | FULL | Counter period register |
| TCPWM1_GRP0_CNT72_PERIOD_BUFF | 0x40582424 | FULL | Counter buffered period register |
| TCPWM1_GRP0_CNT72_DT | 0x40582430 | FULL | Counter PWM dead time register<br>Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM1_GRP0_CNT72_TR_CMD | 0x40582440 | FULL | Counter trigger command register |
| TCPWM1_GRP0_CNT72_TR_IN_SEL0 | 0x40582444 | FULL | Counter input trigger selection register 0 |
| TCPWM1_GRP0_CNT72_TR_IN_SEL1 | 0x40582448 | FULL | Counter input trigger selection register 1 |
| TCPWM1_GRP0_CNT72_TR_IN_EDGE_SEL | 0x4058244C | FULL | Counter input trigger edge selection register |
| TCPWM1_GRP0_CNT72_TR_PWM_CTRL | 0x40582450 | FULL | Counter trigger PWM control register |
| TCPWM1_GRP0_CNT72_TR_OUT_SEL | 0x40582454 | FULL | Counter output trigger selection register |
| TCPWM1_GRP0_CNT72_INTR | 0x40582470 | FULL | Interrupt request register |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT72_INTR_SET | 0x40582474 | FULL | Interrupt set request register |
| TCPWM1_GRP0_CNT72_INTR_MASK | 0x40582478 | FULL | Interrupt mask register |
| TCPWM1_GRP0_CNT72_INTR_MASKED | 0x4058247C | FULL | Interrupt masked request register |

### 33.2.1.74 CNT 73

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT73_CTRL | 0x40582480 | FULL | Counter control register<br>Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM1_GRP0_CNT73_STATUS | 0x40582484 | FULL | Counter status register<br>Note:DT_CNT_H is not available for this register |
| TCPWM1_GRP0_CNT73_COUNTER | 0x40582488 | FULL | Counter count register |
| TCPWM1_GRP0_CNT73_CC0 | 0x40582490 | FULL | Counter compare/capture 0 register |
| TCPWM1_GRP0_CNT73_CC0_BUFF | 0x40582494 | FULL | Counter buffered compare/capture 0 register |
| TCPWM1_GRP0_CNT73_CC1 | 0x40582498 | FULL | Counter compare/capture 1 register |
| TCPWM1_GRP0_CNT73_CC1_BUFF | 0x4058249C | FULL | Counter buffered compare/capture 1 register |
| TCPWM1_GRP0_CNT73_PERIOD | 0x405824A0 | FULL | Counter period register |
| TCPWM1_GRP0_CNT73_PERIOD_BUFF | 0x405824A4 | FULL | Counter buffered period register |
| TCPWM1_GRP0_CNT73_DT | 0x405824B0 | FULL | Counter PWM dead time register<br>Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM1_GRP0_CNT73_TR_CMD | 0x405824C0 | FULL | Counter trigger command register |
| TCPWM1_GRP0_CNT73_TR_IN_SEL0 | 0x405824C4 | FULL | Counter input trigger selection register 0 |
| TCPWM1_GRP0_CNT73_TR_IN_SEL1 | 0x405824C8 | FULL | Counter input trigger selection register 1 |
| TCPWM1_GRP0_CNT73_TR_IN_EDGE_SEL | 0x405824CC | FULL | Counter input trigger edge selection register |
| TCPWM1_GRP0_CNT73_TR_PWM_CTRL | 0x405824D0 | FULL | Counter trigger PWM control register |
| TCPWM1_GRP0_CNT73_TR_OUT_SEL | 0x405824D4 | FULL | Counter output trigger selection register |
| TCPWM1_GRP0_CNT73_INTR | 0x405824F0 | FULL | Interrupt request register |
| TCPWM1_GRP0_CNT73_INTR_SET | 0x405824F4 | FULL | Interrupt set request register |
| TCPWM1_GRP0_CNT73_INTR_MASK | 0x405824F8 | FULL | Interrupt mask register |
| TCPWM1_GRP0_CNT73_INTR_MASKED | 0x405824FC | FULL | Interrupt masked request register |

### 33.2.1.75 CNT 74

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT74_CTRL | 0x40582500 | FULL | Counter control register<br>Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM1_GRP0_CNT74_STATUS | 0x40582504 | FULL | Counter status register<br>Note:DT_CNT_H is not available for this register |
| TCPWM1_GRP0_CNT74_COUNTER | 0x40582508 | FULL | Counter count register |
| TCPWM1_GRP0_CNT74_CC0 | 0x40582510 | FULL | Counter compare/capture 0 register |
| TCPWM1_GRP0_CNT74_CC0_BUFF | 0x40582514 | FULL | Counter buffered compare/capture 0 register |
| TCPWM1_GRP0_CNT74_CC1 | 0x40582518 | FULL | Counter compare/capture 1 register |
| TCPWM1_GRP0_CNT74_CC1_BUFF | 0x4058251C | FULL | Counter buffered compare/capture 1 register |
| TCPWM1_GRP0_CNT74_PERIOD | 0x40582520 | FULL | Counter period register |
| TCPWM1_GRP0_CNT74_PERIOD_BUFF | 0x40582524 | FULL | Counter buffered period register |
| TCPWM1_GRP0_CNT74_DT | 0x40582530 | FULL | Counter PWM dead time register<br>Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM1_GRP0_CNT74_TR_CMD | 0x40582540 | FULL | Counter trigger command register |
| TCPWM1_GRP0_CNT74_TR_IN_SEL0 | 0x40582544 | FULL | Counter input trigger selection register 0 |
| TCPWM1_GRP0_CNT74_TR_IN_SEL1 | 0x40582548 | FULL | Counter input trigger selection register 1 |
| TCPWM1_GRP0_CNT74_TR_IN_EDGE_SEL | 0x4058254C | FULL | Counter input trigger edge selection register |
| TCPWM1_GRP0_CNT74_TR_PWM_CTRL | 0x40582550 | FULL | Counter trigger PWM control register |
| TCPWM1_GRP0_CNT74_TR_OUT_SEL | 0x40582554 | FULL | Counter output trigger selection register |
| TCPWM1_GRP0_CNT74_INTR | 0x40582570 | FULL | Interrupt request register |
| TCPWM1_GRP0_CNT74_INTR_SET | 0x40582574 | FULL | Interrupt set request register |
| TCPWM1_GRP0_CNT74_INTR_MASK | 0x40582578 | FULL | Interrupt mask register |
| TCPWM1_GRP0_CNT74_INTR_MASKED | 0x4058257C | FULL | Interrupt masked request register |

### 33.2.1.76 CNT 75

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT75_CTRL | 0x40582580 | FULL | Counter control register<br>Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM1_GRP0_CNT75_STATUS | 0x40582584 | FULL | Counter status register<br>Note:DT_CNT_H is not available for this register |
| TCPWM1_GRP0_CNT75_COUNTER | 0x40582588 | FULL | Counter count register |
| TCPWM1_GRP0_CNT75_CC0 | 0x40582590 | FULL | Counter compare/capture 0 register |
| TCPWM1_GRP0_CNT75_CC0_BUFF | 0x40582594 | FULL | Counter buffered compare/capture 0 register |
| TCPWM1_GRP0_CNT75_CC1 | 0x40582598 | FULL | Counter compare/capture 1 register |
| TCPWM1_GRP0_CNT75_CC1_BUFF | 0x4058259C | FULL | Counter buffered compare/capture 1 register |
| TCPWM1_GRP0_CNT75_PERIOD | 0x405825A0 | FULL | Counter period register |
| TCPWM1_GRP0_CNT75_PERIOD_BUFF | 0x405825A4 | FULL | Counter buffered period register |
| TCPWM1_GRP0_CNT75_DT | 0x405825B0 | FULL | Counter PWM dead time register<br>Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM1_GRP0_CNT75_TR_CMD | 0x405825C0 | FULL | Counter trigger command register |
| TCPWM1_GRP0_CNT75_TR_IN_SEL0 | 0x405825C4 | FULL | Counter input trigger selection register 0 |
| TCPWM1_GRP0_CNT75_TR_IN_SEL1 | 0x405825C8 | FULL | Counter input trigger selection register 1 |
| TCPWM1_GRP0_CNT75_TR_IN_EDGE_SEL | 0x405825CC | FULL | Counter input trigger edge selection register |
| TCPWM1_GRP0_CNT75_TR_PWM_CTRL | 0x405825D0 | FULL | Counter trigger PWM control register |
| TCPWM1_GRP0_CNT75_TR_OUT_SEL | 0x405825D4 | FULL | Counter output trigger selection register |
| TCPWM1_GRP0_CNT75_INTR | 0x405825F0 | FULL | Interrupt request register |
| TCPWM1_GRP0_CNT75_INTR_SET | 0x405825F4 | FULL | Interrupt set request register |
| TCPWM1_GRP0_CNT75_INTR_MASK | 0x405825F8 | FULL | Interrupt mask register |
| TCPWM1_GRP0_CNT75_INTR_MASKED | 0x405825FC | FULL | Interrupt masked request register |

### 33.2.1.77 CNT 76

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT76_CTRL | 0x40582600 | FULL | Counter control register<br>Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM1_GRP0_CNT76_STATUS | 0x40582604 | FULL | Counter status register<br>Note:DT_CNT_H is not available for this register |
| TCPWM1_GRP0_CNT76_COUNTER | 0x40582608 | FULL | Counter count register |
| TCPWM1_GRP0_CNT76_CC0 | 0x40582610 | FULL | Counter compare/capture 0 register |
| TCPWM1_GRP0_CNT76_CC0_BUFF | 0x40582614 | FULL | Counter buffered compare/capture 0 register |
| TCPWM1_GRP0_CNT76_CC1 | 0x40582618 | FULL | Counter compare/capture 1 register |
| TCPWM1_GRP0_CNT76_CC1_BUFF | 0x4058261C | FULL | Counter buffered compare/capture 1 register |
| TCPWM1_GRP0_CNT76_PERIOD | 0x40582620 | FULL | Counter period register |
| TCPWM1_GRP0_CNT76_PERIOD_BUFF | 0x40582624 | FULL | Counter buffered period register |
| TCPWM1_GRP0_CNT76_DT | 0x40582630 | FULL | Counter PWM dead time register<br>Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM1_GRP0_CNT76_TR_CMD | 0x40582640 | FULL | Counter trigger command register |
| TCPWM1_GRP0_CNT76_TR_IN_SEL0 | 0x40582644 | FULL | Counter input trigger selection register 0 |
| TCPWM1_GRP0_CNT76_TR_IN_SEL1 | 0x40582648 | FULL | Counter input trigger selection register 1 |
| TCPWM1_GRP0_CNT76_TR_IN_EDGE_SEL | 0x4058264C | FULL | Counter input trigger edge selection register |
| TCPWM1_GRP0_CNT76_TR_PWM_CTRL | 0x40582650 | FULL | Counter trigger PWM control register |
| TCPWM1_GRP0_CNT76_TR_OUT_SEL | 0x40582654 | FULL | Counter output trigger selection register |
| TCPWM1_GRP0_CNT76_INTR | 0x40582670 | FULL | Interrupt request register |
| TCPWM1_GRP0_CNT76_INTR_SET | 0x40582674 | FULL | Interrupt set request register |
| TCPWM1_GRP0_CNT76_INTR_MASK | 0x40582678 | FULL | Interrupt mask register |
| TCPWM1_GRP0_CNT76_INTR_MASKED | 0x4058267C | FULL | Interrupt masked request register |

### 33.2.1.78 CNT 77

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT77_CTRL | 0x40582680 | FULL | Counter control register<br>Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT77_STATUS | 0x40582684 | FULL | Counter status register<br>Note:DT_CNT_H is not available for this register |
| TCPWM1_GRP0_CNT77_COUNTER | 0x40582688 | FULL | Counter count register |
| TCPWM1_GRP0_CNT77_CC0 | 0x40582690 | FULL | Counter compare/capture 0 register |
| TCPWM1_GRP0_CNT77_CC0_BUFF | 0x40582694 | FULL | Counter buffered compare/capture 0 register |
| TCPWM1_GRP0_CNT77_CC1 | 0x40582698 | FULL | Counter compare/capture 1 register |
| TCPWM1_GRP0_CNT77_CC1_BUFF | 0x4058269C | FULL | Counter buffered compare/capture 1 register |
| TCPWM1_GRP0_CNT77_PERIOD | 0x405826A0 | FULL | Counter period register |
| TCPWM1_GRP0_CNT77_PERIOD_BUFF | 0x405826A4 | FULL | Counter buffered period register |
| TCPWM1_GRP0_CNT77_DT | 0x405826B0 | FULL | Counter PWM dead time register<br>Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM1_GRP0_CNT77_TR_CMD | 0x405826C0 | FULL | Counter trigger command register |
| TCPWM1_GRP0_CNT77_TR_IN_SEL0 | 0x405826C4 | FULL | Counter input trigger selection register 0 |
| TCPWM1_GRP0_CNT77_TR_IN_SEL1 | 0x405826C8 | FULL | Counter input trigger selection register 1 |
| TCPWM1_GRP0_CNT77_TR_IN_EDGE_SEL | 0x405826CC | FULL | Counter input trigger edge selection register |
| TCPWM1_GRP0_CNT77_TR_PWM_CTRL | 0x405826D0 | FULL | Counter trigger PWM control register |
| TCPWM1_GRP0_CNT77_TR_OUT_SEL | 0x405826D4 | FULL | Counter output trigger selection register |
| TCPWM1_GRP0_CNT77_INTR | 0x405826F0 | FULL | Interrupt request register |
| TCPWM1_GRP0_CNT77_INTR_SET | 0x405826F4 | FULL | Interrupt set request register |
| TCPWM1_GRP0_CNT77_INTR_MASK | 0x405826F8 | FULL | Interrupt mask register |
| TCPWM1_GRP0_CNT77_INTR_MASKED | 0x405826FC | FULL | Interrupt masked request register |

### 33.2.1.79 CNT 78

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT78_CTRL | 0x40582700 | FULL | Counter control register<br>Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM1_GRP0_CNT78_STATUS | 0x40582704 | FULL | Counter status register<br>Note:DT_CNT_H is not available for this register |
| TCPWM1_GRP0_CNT78_COUNTER | 0x40582708 | FULL | Counter count register |
| TCPWM1_GRP0_CNT78_CC0 | 0x40582710 | FULL | Counter compare/capture 0 register |
| TCPWM1_GRP0_CNT78_CC0_BUFF | 0x40582714 | FULL | Counter buffered compare/capture 0 register |
| TCPWM1_GRP0_CNT78_CC1 | 0x40582718 | FULL | Counter compare/capture 1 register |
| TCPWM1_GRP0_CNT78_CC1_BUFF | 0x4058271C | FULL | Counter buffered compare/capture 1 register |
| TCPWM1_GRP0_CNT78_PERIOD | 0x40582720 | FULL | Counter period register |
| TCPWM1_GRP0_CNT78_PERIOD_BUFF | 0x40582724 | FULL | Counter buffered period register |
| TCPWM1_GRP0_CNT78_DT | 0x40582730 | FULL | Counter PWM dead time register<br>Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM1_GRP0_CNT78_TR_CMD | 0x40582740 | FULL | Counter trigger command register |
| TCPWM1_GRP0_CNT78_TR_IN_SEL0 | 0x40582744 | FULL | Counter input trigger selection register 0 |
| TCPWM1_GRP0_CNT78_TR_IN_SEL1 | 0x40582748 | FULL | Counter input trigger selection register 1 |
| TCPWM1_GRP0_CNT78_TR_IN_EDGE_SEL | 0x4058274C | FULL | Counter input trigger edge selection register |
| TCPWM1_GRP0_CNT78_TR_PWM_CTRL | 0x40582750 | FULL | Counter trigger PWM control register |
| TCPWM1_GRP0_CNT78_TR_OUT_SEL | 0x40582754 | FULL | Counter output trigger selection register |
| TCPWM1_GRP0_CNT78_INTR | 0x40582770 | FULL | Interrupt request register |
| TCPWM1_GRP0_CNT78_INTR_SET | 0x40582774 | FULL | Interrupt set request register |
| TCPWM1_GRP0_CNT78_INTR_MASK | 0x40582778 | FULL | Interrupt mask register |
| TCPWM1_GRP0_CNT78_INTR_MASKED | 0x4058277C | FULL | Interrupt masked request register |

### 33.2.1.80 CNT 79

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT79_CTRL | 0x40582780 | FULL | Counter control register<br>Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM1_GRP0_CNT79_STATUS | 0x40582784 | FULL | Counter status register<br>Note:DT_CNT_H is not available for this register |
| TCPWM1_GRP0_CNT79_COUNTER | 0x40582788 | FULL | Counter count register |
| TCPWM1_GRP0_CNT79_CC0 | 0x40582790 | FULL | Counter compare/capture 0 register |
| TCPWM1_GRP0_CNT79_CC0_BUFF | 0x40582794 | FULL | Counter buffered compare/capture 0 register |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT79_CC1 | 0x40582798 | FULL | Counter compare/capture 1 register |
| TCPWM1_GRP0_CNT79_CC1_BUFF | 0x4058279C | FULL | Counter buffered compare/capture 1 register |
| TCPWM1_GRP0_CNT79_PERIOD | 0x405827A0 | FULL | Counter period register |
| TCPWM1_GRP0_CNT79_PERIOD_BUFF | 0x405827A4 | FULL | Counter buffered period register |
| TCPWM1_GRP0_CNT79_DT | 0x405827B0 | FULL | Counter PWM dead time register<br>Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM1_GRP0_CNT79_TR_CMD | 0x405827C0 | FULL | Counter trigger command register |
| TCPWM1_GRP0_CNT79_TR_IN_SEL0 | 0x405827C4 | FULL | Counter input trigger selection register 0 |
| TCPWM1_GRP0_CNT79_TR_IN_SEL1 | 0x405827C8 | FULL | Counter input trigger selection register 1 |
| TCPWM1_GRP0_CNT79_TR_IN_EDGE_SEL | 0x405827CC | FULL | Counter input trigger edge selection register |
| TCPWM1_GRP0_CNT79_TR_PWM_CTRL | 0x405827D0 | FULL | Counter trigger PWM control register |
| TCPWM1_GRP0_CNT79_TR_OUT_SEL | 0x405827D4 | FULL | Counter output trigger selection register |
| TCPWM1_GRP0_CNT79_INTR | 0x405827F0 | FULL | Interrupt request register |
| TCPWM1_GRP0_CNT79_INTR_SET | 0x405827F4 | FULL | Interrupt set request register |
| TCPWM1_GRP0_CNT79_INTR_MASK | 0x405827F8 | FULL | Interrupt mask register |
| TCPWM1_GRP0_CNT79_INTR_MASKED | 0x405827FC | FULL | Interrupt masked request register |

### 33.2.1.81 CNT 80

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT80_CTRL | 0x40582800 | FULL | Counter control register<br>Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM1_GRP0_CNT80_STATUS | 0x40582804 | FULL | Counter status register<br>Note:DT_CNT_H is not available for this register |
| TCPWM1_GRP0_CNT80_COUNTER | 0x40582808 | FULL | Counter count register |
| TCPWM1_GRP0_CNT80_CC0 | 0x40582810 | FULL | Counter compare/capture 0 register |
| TCPWM1_GRP0_CNT80_CC0_BUFF | 0x40582814 | FULL | Counter buffered compare/capture 0 register |
| TCPWM1_GRP0_CNT80_CC1 | 0x40582818 | FULL | Counter compare/capture 1 register |
| TCPWM1_GRP0_CNT80_CC1_BUFF | 0x4058281C | FULL | Counter buffered compare/capture 1 register |
| TCPWM1_GRP0_CNT80_PERIOD | 0x40582820 | FULL | Counter period register |
| TCPWM1_GRP0_CNT80_PERIOD_BUFF | 0x40582824 | FULL | Counter buffered period register |
| TCPWM1_GRP0_CNT80_DT | 0x40582830 | FULL | Counter PWM dead time register<br>Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM1_GRP0_CNT80_TR_CMD | 0x40582840 | FULL | Counter trigger command register |
| TCPWM1_GRP0_CNT80_TR_IN_SEL0 | 0x40582844 | FULL | Counter input trigger selection register 0 |
| TCPWM1_GRP0_CNT80_TR_IN_SEL1 | 0x40582848 | FULL | Counter input trigger selection register 1 |
| TCPWM1_GRP0_CNT80_TR_IN_EDGE_SEL | 0x4058284C | FULL | Counter input trigger edge selection register |
| TCPWM1_GRP0_CNT80_TR_PWM_CTRL | 0x40582850 | FULL | Counter trigger PWM control register |
| TCPWM1_GRP0_CNT80_TR_OUT_SEL | 0x40582854 | FULL | Counter output trigger selection register |
| TCPWM1_GRP0_CNT80_INTR | 0x40582870 | FULL | Interrupt request register |
| TCPWM1_GRP0_CNT80_INTR_SET | 0x40582874 | FULL | Interrupt set request register |
| TCPWM1_GRP0_CNT80_INTR_MASK | 0x40582878 | FULL | Interrupt mask register |
| TCPWM1_GRP0_CNT80_INTR_MASKED | 0x4058287C | FULL | Interrupt masked request register |

### 33.2.1.82 CNT 81

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT81_CTRL | 0x40582880 | FULL | Counter control register<br>Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM1_GRP0_CNT81_STATUS | 0x40582884 | FULL | Counter status register<br>Note:DT_CNT_H is not available for this register |
| TCPWM1_GRP0_CNT81_COUNTER | 0x40582888 | FULL | Counter count register |
| TCPWM1_GRP0_CNT81_CC0 | 0x40582890 | FULL | Counter compare/capture 0 register |
| TCPWM1_GRP0_CNT81_CC0_BUFF | 0x40582894 | FULL | Counter buffered compare/capture 0 register |
| TCPWM1_GRP0_CNT81_CC1 | 0x40582898 | FULL | Counter compare/capture 1 register |
| TCPWM1_GRP0_CNT81_CC1_BUFF | 0x4058289C | FULL | Counter buffered compare/capture 1 register |
| TCPWM1_GRP0_CNT81_PERIOD | 0x405828A0 | FULL | Counter period register |
| TCPWM1_GRP0_CNT81_PERIOD_BUFF | 0x405828A4 | FULL | Counter buffered period register |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT81_DT | 0x405828B0 | FULL | Counter PWM dead time register<br>Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM1_GRP0_CNT81_TR_CMD | 0x405828C0 | FULL | Counter trigger command register |
| TCPWM1_GRP0_CNT81_TR_IN_SEL0 | 0x405828C4 | FULL | Counter input trigger selection register 0 |
| TCPWM1_GRP0_CNT81_TR_IN_SEL1 | 0x405828C8 | FULL | Counter input trigger selection register 1 |
| TCPWM1_GRP0_CNT81_TR_IN_EDGE_SEL | 0x405828CC | FULL | Counter input trigger edge selection register |
| TCPWM1_GRP0_CNT81_TR_PWM_CTRL | 0x405828D0 | FULL | Counter trigger PWM control register |
| TCPWM1_GRP0_CNT81_TR_OUT_SEL | 0x405828D4 | FULL | Counter output trigger selection register |
| TCPWM1_GRP0_CNT81_INTR | 0x405828F0 | FULL | Interrupt request register |
| TCPWM1_GRP0_CNT81_INTR_SET | 0x405828F4 | FULL | Interrupt set request register |
| TCPWM1_GRP0_CNT81_INTR_MASK | 0x405828F8 | FULL | Interrupt mask register |
| TCPWM1_GRP0_CNT81_INTR_MASKED | 0x405828FC | FULL | Interrupt masked request register |

### 33.2.1.83 CNT 82

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT82_CTRL | 0x40582900 | FULL | Counter control register<br>Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM1_GRP0_CNT82_STATUS | 0x40582904 | FULL | Counter status register<br>Note:DT_CNT_H is not available for this register |
| TCPWM1_GRP0_CNT82_COUNTER | 0x40582908 | FULL | Counter count register |
| TCPWM1_GRP0_CNT82_CC0 | 0x40582910 | FULL | Counter compare/capture 0 register |
| TCPWM1_GRP0_CNT82_CC0_BUFF | 0x40582914 | FULL | Counter buffered compare/capture 0 register |
| TCPWM1_GRP0_CNT82_CC1 | 0x40582918 | FULL | Counter compare/capture 1 register |
| TCPWM1_GRP0_CNT82_CC1_BUFF | 0x4058291C | FULL | Counter buffered compare/capture 1 register |
| TCPWM1_GRP0_CNT82_PERIOD | 0x40582920 | FULL | Counter period register |
| TCPWM1_GRP0_CNT82_PERIOD_BUFF | 0x40582924 | FULL | Counter buffered period register |
| TCPWM1_GRP0_CNT82_DT | 0x40582930 | FULL | Counter PWM dead time register<br>Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM1_GRP0_CNT82_TR_CMD | 0x40582940 | FULL | Counter trigger command register |
| TCPWM1_GRP0_CNT82_TR_IN_SEL0 | 0x40582944 | FULL | Counter input trigger selection register 0 |
| TCPWM1_GRP0_CNT82_TR_IN_SEL1 | 0x40582948 | FULL | Counter input trigger selection register 1 |
| TCPWM1_GRP0_CNT82_TR_IN_EDGE_SEL | 0x4058294C | FULL | Counter input trigger edge selection register |
| TCPWM1_GRP0_CNT82_TR_PWM_CTRL | 0x40582950 | FULL | Counter trigger PWM control register |
| TCPWM1_GRP0_CNT82_TR_OUT_SEL | 0x40582954 | FULL | Counter output trigger selection register |
| TCPWM1_GRP0_CNT82_INTR | 0x40582970 | FULL | Interrupt request register |
| TCPWM1_GRP0_CNT82_INTR_SET | 0x40582974 | FULL | Interrupt set request register |
| TCPWM1_GRP0_CNT82_INTR_MASK | 0x40582978 | FULL | Interrupt mask register |
| TCPWM1_GRP0_CNT82_INTR_MASKED | 0x4058297C | FULL | Interrupt masked request register |

### 33.2.1.84 CNT 83

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT83_CTRL | 0x40582980 | FULL | Counter control register<br>Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM1_GRP0_CNT83_STATUS | 0x40582984 | FULL | Counter status register<br>Note:DT_CNT_H is not available for this register |
| TCPWM1_GRP0_CNT83_COUNTER | 0x40582988 | FULL | Counter count register |
| TCPWM1_GRP0_CNT83_CC0 | 0x40582990 | FULL | Counter compare/capture 0 register |
| TCPWM1_GRP0_CNT83_CC0_BUFF | 0x40582994 | FULL | Counter buffered compare/capture 0 register |
| TCPWM1_GRP0_CNT83_CC1 | 0x40582998 | FULL | Counter compare/capture 1 register |
| TCPWM1_GRP0_CNT83_CC1_BUFF | 0x4058299C | FULL | Counter buffered compare/capture 1 register |
| TCPWM1_GRP0_CNT83_PERIOD | 0x405829A0 | FULL | Counter period register |
| TCPWM1_GRP0_CNT83_PERIOD_BUFF | 0x405829A4 | FULL | Counter buffered period register |
| TCPWM1_GRP0_CNT83_DT | 0x405829B0 | FULL | Counter PWM dead time register<br>Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM1_GRP0_CNT83_TR_CMD | 0x405829C0 | FULL | Counter trigger command register |
| TCPWM1_GRP0_CNT83_TR_IN_SEL0 | 0x405829C4 | FULL | Counter input trigger selection register 0 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP0_CNT83_TR_IN_SEL1 | 0x405829C8 | FULL | Counter input trigger selection register 1 |
| TCPWM1_GRP0_CNT83_TR_IN_EDGE_SEL | 0x405829CC | FULL | Counter input trigger edge selection register |
| TCPWM1_GRP0_CNT83_TR_PWM_CTRL | 0x405829D0 | FULL | Counter trigger PWM control register |
| TCPWM1_GRP0_CNT83_TR_OUT_SEL | 0x405829D4 | FULL | Counter output trigger selection register |
| TCPWM1_GRP0_CNT83_INTR | 0x405829F0 | FULL | Interrupt request register |
| TCPWM1_GRP0_CNT83_INTR_SET | 0x405829F4 | FULL | Interrupt set request register |
| TCPWM1_GRP0_CNT83_INTR_MASK | 0x405829F8 | FULL | Interrupt mask register |
| TCPWM1_GRP0_CNT83_INTR_MASKED | 0x405829FC | FULL | Interrupt masked request register |

### 33.2.2 GRP 1

#### 33.2.2.1 CNT 0

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP1_CNT0_CTRL | 0x40588000 | FULL | Counter control register |
| TCPWM1_GRP1_CNT0_STATUS | 0x40588004 | FULL | Counter status register |
| TCPWM1_GRP1_CNT0_COUNTER | 0x40588008 | FULL | Counter count register |
| TCPWM1_GRP1_CNT0_CC0 | 0x40588010 | FULL | Counter compare/capture 0 register |
| TCPWM1_GRP1_CNT0_CC0_BUFF | 0x40588014 | FULL | Counter buffered compare/capture 0 register |
| TCPWM1_GRP1_CNT0_CC1 | 0x40588018 | FULL | Counter compare/capture 1 register |
| TCPWM1_GRP1_CNT0_CC1_BUFF | 0x4058801C | FULL | Counter buffered compare/capture 1 register |
| TCPWM1_GRP1_CNT0_PERIOD | 0x40588020 | FULL | Counter period register |
| TCPWM1_GRP1_CNT0_PERIOD_BUFF | 0x40588024 | FULL | Counter buffered period register |
| TCPWM1_GRP1_CNT0_LINE_SEL | 0x40588028 | FULL | Counter line selection register |
| TCPWM1_GRP1_CNT0_LINE_SEL_BUFF | 0x4058802C | FULL | Counter buffered line selection register |
| TCPWM1_GRP1_CNT0_DT | 0x40588030 | FULL | Counter PWM dead time register |
| TCPWM1_GRP1_CNT0_TR_CMD | 0x40588040 | FULL | Counter trigger command register |
| TCPWM1_GRP1_CNT0_TR_IN_SEL0 | 0x40588044 | FULL | Counter input trigger selection register 0 |
| TCPWM1_GRP1_CNT0_TR_IN_SEL1 | 0x40588048 | FULL | Counter input trigger selection register 1 |
| TCPWM1_GRP1_CNT0_TR_IN_EDGE_SEL | 0x4058804C | FULL | Counter input trigger edge selection register |
| TCPWM1_GRP1_CNT0_TR_PWM_CTRL | 0x40588050 | FULL | Counter trigger PWM control register |
| TCPWM1_GRP1_CNT0_TR_OUT_SEL | 0x40588054 | FULL | Counter output trigger selection register |
| TCPWM1_GRP1_CNT0_INTR | 0x40588070 | FULL | Interrupt request register |
| TCPWM1_GRP1_CNT0_INTR_SET | 0x40588074 | FULL | Interrupt set request register |
| TCPWM1_GRP1_CNT0_INTR_MASK | 0x40588078 | FULL | Interrupt mask register |
| TCPWM1_GRP1_CNT0_INTR_MASKED | 0x4058807C | FULL | Interrupt masked request register |

#### 33.2.2.2 CNT 1

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP1_CNT1_CTRL | 0x40588080 | FULL | Counter control register |
| TCPWM1_GRP1_CNT1_STATUS | 0x40588084 | FULL | Counter status register |
| TCPWM1_GRP1_CNT1_COUNTER | 0x40588088 | FULL | Counter count register |
| TCPWM1_GRP1_CNT1_CC0 | 0x40588090 | FULL | Counter compare/capture 0 register |
| TCPWM1_GRP1_CNT1_CC0_BUFF | 0x40588094 | FULL | Counter buffered compare/capture 0 register |
| TCPWM1_GRP1_CNT1_CC1 | 0x40588098 | FULL | Counter compare/capture 1 register |
| TCPWM1_GRP1_CNT1_CC1_BUFF | 0x4058809C | FULL | Counter buffered compare/capture 1 register |
| TCPWM1_GRP1_CNT1_PERIOD | 0x405880A0 | FULL | Counter period register |
| TCPWM1_GRP1_CNT1_PERIOD_BUFF | 0x405880A4 | FULL | Counter buffered period register |
| TCPWM1_GRP1_CNT1_LINE_SEL | 0x405880A8 | FULL | Counter line selection register |
| TCPWM1_GRP1_CNT1_LINE_SEL_BUFF | 0x405880AC | FULL | Counter buffered line selection register |
| TCPWM1_GRP1_CNT1_DT | 0x405880B0 | FULL | Counter PWM dead time register |
| TCPWM1_GRP1_CNT1_TR_CMD | 0x405880C0 | FULL | Counter trigger command register |
| TCPWM1_GRP1_CNT1_TR_IN_SEL0 | 0x405880C4 | FULL | Counter input trigger selection register 0 |
| TCPWM1_GRP1_CNT1_TR_IN_SEL1 | 0x405880C8 | FULL | Counter input trigger selection register 1 |
| TCPWM1_GRP1_CNT1_TR_IN_EDGE_SEL | 0x405880CC | FULL | Counter input trigger edge selection register |
| TCPWM1_GRP1_CNT1_TR_PWM_CTRL | 0x405880D0 | FULL | Counter trigger PWM control register |
| TCPWM1_GRP1_CNT1_TR_OUT_SEL | 0x405880D4 | FULL | Counter output trigger selection register |
| TCPWM1_GRP1_CNT1_INTR | 0x405880F0 | FULL | Interrupt request register |
| TCPWM1_GRP1_CNT1_INTR_SET | 0x405880F4 | FULL | Interrupt set request register |
| TCPWM1_GRP1_CNT1_INTR_MASK | 0x405880F8 | FULL | Interrupt mask register |
| TCPWM1_GRP1_CNT1_INTR_MASKED | 0x405880FC | FULL | Interrupt masked request register |

#### 33.2.2.3 CNT 2

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP1_CNT2_CTRL | 0x40588100 | FULL | Counter control register |
| TCPWM1_GRP1_CNT2_STATUS | 0x40588104 | FULL | Counter status register |
| TCPWM1_GRP1_CNT2_COUNTER | 0x40588108 | FULL | Counter count register |
| TCPWM1_GRP1_CNT2_CC0 | 0x40588110 | FULL | Counter compare/capture 0 register |
| TCPWM1_GRP1_CNT2_CC0_BUFF | 0x40588114 | FULL | Counter buffered compare/capture 0 register |
| TCPWM1_GRP1_CNT2_CC1 | 0x40588118 | FULL | Counter compare/capture 1 register |
| TCPWM1_GRP1_CNT2_CC1_BUFF | 0x4058811C | FULL | Counter buffered compare/capture 1 register |
| TCPWM1_GRP1_CNT2_PERIOD | 0x40588120 | FULL | Counter period register |
| TCPWM1_GRP1_CNT2_PERIOD_BUFF | 0x40588124 | FULL | Counter buffered period register |
| TCPWM1_GRP1_CNT2_LINE_SEL | 0x40588128 | FULL | Counter line selection register |
| TCPWM1_GRP1_CNT2_LINE_SEL_BUFF | 0x4058812C | FULL | Counter buffered line selection register |
| TCPWM1_GRP1_CNT2_DT | 0x40588130 | FULL | Counter PWM dead time register |
| TCPWM1_GRP1_CNT2_TR_CMD | 0x40588140 | FULL | Counter trigger command register |
| TCPWM1_GRP1_CNT2_TR_IN_SEL0 | 0x40588144 | FULL | Counter input trigger selection register 0 |
| TCPWM1_GRP1_CNT2_TR_IN_SEL1 | 0x40588148 | FULL | Counter input trigger selection register 1 |
| TCPWM1_GRP1_CNT2_TR_IN_EDGE_SEL | 0x4058814C | FULL | Counter input trigger edge selection register |
| TCPWM1_GRP1_CNT2_TR_PWM_CTRL | 0x40588150 | FULL | Counter trigger PWM control register |
| TCPWM1_GRP1_CNT2_TR_OUT_SEL | 0x40588154 | FULL | Counter output trigger selection register |
| TCPWM1_GRP1_CNT2_INTR | 0x40588170 | FULL | Interrupt request register |
| TCPWM1_GRP1_CNT2_INTR_SET | 0x40588174 | FULL | Interrupt set request register |
| TCPWM1_GRP1_CNT2_INTR_MASK | 0x40588178 | FULL | Interrupt mask register |
| TCPWM1_GRP1_CNT2_INTR_MASKED | 0x4058817C | FULL | Interrupt masked request register |

### 33.2.2.4 CNT 3

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP1_CNT3_CTRL | 0x40588180 | FULL | Counter control register |
| TCPWM1_GRP1_CNT3_STATUS | 0x40588184 | FULL | Counter status register |
| TCPWM1_GRP1_CNT3_COUNTER | 0x40588188 | FULL | Counter count register |
| TCPWM1_GRP1_CNT3_CC0 | 0x40588190 | FULL | Counter compare/capture 0 register |
| TCPWM1_GRP1_CNT3_CC0_BUFF | 0x40588194 | FULL | Counter buffered compare/capture 0 register |
| TCPWM1_GRP1_CNT3_CC1 | 0x40588198 | FULL | Counter compare/capture 1 register |
| TCPWM1_GRP1_CNT3_CC1_BUFF | 0x4058819C | FULL | Counter buffered compare/capture 1 register |
| TCPWM1_GRP1_CNT3_PERIOD | 0x405881A0 | FULL | Counter period register |
| TCPWM1_GRP1_CNT3_PERIOD_BUFF | 0x405881A4 | FULL | Counter buffered period register |
| TCPWM1_GRP1_CNT3_LINE_SEL | 0x405881A8 | FULL | Counter line selection register |
| TCPWM1_GRP1_CNT3_LINE_SEL_BUFF | 0x405881AC | FULL | Counter buffered line selection register |
| TCPWM1_GRP1_CNT3_DT | 0x405881B0 | FULL | Counter PWM dead time register |
| TCPWM1_GRP1_CNT3_TR_CMD | 0x405881C0 | FULL | Counter trigger command register |
| TCPWM1_GRP1_CNT3_TR_IN_SEL0 | 0x405881C4 | FULL | Counter input trigger selection register 0 |
| TCPWM1_GRP1_CNT3_TR_IN_SEL1 | 0x405881C8 | FULL | Counter input trigger selection register 1 |
| TCPWM1_GRP1_CNT3_TR_IN_EDGE_SEL | 0x405881CC | FULL | Counter input trigger edge selection register |
| TCPWM1_GRP1_CNT3_TR_PWM_CTRL | 0x405881D0 | FULL | Counter trigger PWM control register |
| TCPWM1_GRP1_CNT3_TR_OUT_SEL | 0x405881D4 | FULL | Counter output trigger selection register |
| TCPWM1_GRP1_CNT3_INTR | 0x405881F0 | FULL | Interrupt request register |
| TCPWM1_GRP1_CNT3_INTR_SET | 0x405881F4 | FULL | Interrupt set request register |
| TCPWM1_GRP1_CNT3_INTR_MASK | 0x405881F8 | FULL | Interrupt mask register |
| TCPWM1_GRP1_CNT3_INTR_MASKED | 0x405881FC | FULL | Interrupt masked request register |

### 33.2.2.5 CNT 4

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP1_CNT4_CTRL | 0x40588200 | FULL | Counter control register |
| TCPWM1_GRP1_CNT4_STATUS | 0x40588204 | FULL | Counter status register |
| TCPWM1_GRP1_CNT4_COUNTER | 0x40588208 | FULL | Counter count register |
| TCPWM1_GRP1_CNT4_CC0 | 0x40588210 | FULL | Counter compare/capture 0 register |
| TCPWM1_GRP1_CNT4_CC0_BUFF | 0x40588214 | FULL | Counter buffered compare/capture 0 register |
| TCPWM1_GRP1_CNT4_CC1 | 0x40588218 | FULL | Counter compare/capture 1 register |
| TCPWM1_GRP1_CNT4_CC1_BUFF | 0x4058821C | FULL | Counter buffered compare/capture 1 register |
| TCPWM1_GRP1_CNT4_PERIOD | 0x40588220 | FULL | Counter period register |
| TCPWM1_GRP1_CNT4_PERIOD_BUFF | 0x40588224 | FULL | Counter buffered period register |
| TCPWM1_GRP1_CNT4_LINE_SEL | 0x40588228 | FULL | Counter line selection register |
| TCPWM1_GRP1_CNT4_LINE_SEL_BUFF | 0x4058822C | FULL | Counter buffered line selection register |
| TCPWM1_GRP1_CNT4_DT | 0x40588230 | FULL | Counter PWM dead time register |
| TCPWM1_GRP1_CNT4_TR_CMD | 0x40588240 | FULL | Counter trigger command register |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP1_CNT4_TR_IN_SEL0 | 0x40588244 | FULL | Counter input trigger selection register 0 |
| TCPWM1_GRP1_CNT4_TR_IN_SEL1 | 0x40588248 | FULL | Counter input trigger selection register 1 |
| TCPWM1_GRP1_CNT4_TR_IN_EDGE_SEL | 0x4058824C | FULL | Counter input trigger edge selection register |
| TCPWM1_GRP1_CNT4_TR_PWM_CTRL | 0x40588250 | FULL | Counter trigger PWM control register |
| TCPWM1_GRP1_CNT4_TR_OUT_SEL | 0x40588254 | FULL | Counter output trigger selection register |
| TCPWM1_GRP1_CNT4_INTR | 0x40588270 | FULL | Interrupt request register |
| TCPWM1_GRP1_CNT4_INTR_SET | 0x40588274 | FULL | Interrupt set request register |
| TCPWM1_GRP1_CNT4_INTR_MASK | 0x40588278 | FULL | Interrupt mask register |
| TCPWM1_GRP1_CNT4_INTR_MASKED | 0x4058827C | FULL | Interrupt masked request register |

### 33.2.2.6 CNT 5

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP1_CNT5_CTRL | 0x40588280 | FULL | Counter control register |
| TCPWM1_GRP1_CNT5_STATUS | 0x40588284 | FULL | Counter status register |
| TCPWM1_GRP1_CNT5_COUNTER | 0x40588288 | FULL | Counter count register |
| TCPWM1_GRP1_CNT5_CC0 | 0x40588290 | FULL | Counter compare/capture 0 register |
| TCPWM1_GRP1_CNT5_CC0_BUFF | 0x40588294 | FULL | Counter buffered compare/capture 0 register |
| TCPWM1_GRP1_CNT5_CC1 | 0x40588298 | FULL | Counter compare/capture 1 register |
| TCPWM1_GRP1_CNT5_CC1_BUFF | 0x4058829C | FULL | Counter buffered compare/capture 1 register |
| TCPWM1_GRP1_CNT5_PERIOD | 0x405882A0 | FULL | Counter period register |
| TCPWM1_GRP1_CNT5_PERIOD_BUFF | 0x405882A4 | FULL | Counter buffered period register |
| TCPWM1_GRP1_CNT5_LINE_SEL | 0x405882A8 | FULL | Counter line selection register |
| TCPWM1_GRP1_CNT5_LINE_SEL_BUFF | 0x405882AC | FULL | Counter buffered line selection register |
| TCPWM1_GRP1_CNT5_DT | 0x405882B0 | FULL | Counter PWM dead time register |
| TCPWM1_GRP1_CNT5_TR_CMD | 0x405882C0 | FULL | Counter trigger command register |
| TCPWM1_GRP1_CNT5_TR_IN_SEL0 | 0x405882C4 | FULL | Counter input trigger selection register 0 |
| TCPWM1_GRP1_CNT5_TR_IN_SEL1 | 0x405882C8 | FULL | Counter input trigger selection register 1 |
| TCPWM1_GRP1_CNT5_TR_IN_EDGE_SEL | 0x405882CC | FULL | Counter input trigger edge selection register |
| TCPWM1_GRP1_CNT5_TR_PWM_CTRL | 0x405882D0 | FULL | Counter trigger PWM control register |
| TCPWM1_GRP1_CNT5_TR_OUT_SEL | 0x405882D4 | FULL | Counter output trigger selection register |
| TCPWM1_GRP1_CNT5_INTR | 0x405882F0 | FULL | Interrupt request register |
| TCPWM1_GRP1_CNT5_INTR_SET | 0x405882F4 | FULL | Interrupt set request register |
| TCPWM1_GRP1_CNT5_INTR_MASK | 0x405882F8 | FULL | Interrupt mask register |
| TCPWM1_GRP1_CNT5_INTR_MASKED | 0x405882FC | FULL | Interrupt masked request register |

### 33.2.2.7 CNT 6

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP1_CNT6_CTRL | 0x40588300 | FULL | Counter control register |
| TCPWM1_GRP1_CNT6_STATUS | 0x40588304 | FULL | Counter status register |
| TCPWM1_GRP1_CNT6_COUNTER | 0x40588308 | FULL | Counter count register |
| TCPWM1_GRP1_CNT6_CC0 | 0x40588310 | FULL | Counter compare/capture 0 register |
| TCPWM1_GRP1_CNT6_CC0_BUFF | 0x40588314 | FULL | Counter buffered compare/capture 0 register |
| TCPWM1_GRP1_CNT6_CC1 | 0x40588318 | FULL | Counter compare/capture 1 register |
| TCPWM1_GRP1_CNT6_CC1_BUFF | 0x4058831C | FULL | Counter buffered compare/capture 1 register |
| TCPWM1_GRP1_CNT6_PERIOD | 0x40588320 | FULL | Counter period register |
| TCPWM1_GRP1_CNT6_PERIOD_BUFF | 0x40588324 | FULL | Counter buffered period register |
| TCPWM1_GRP1_CNT6_LINE_SEL | 0x40588328 | FULL | Counter line selection register |
| TCPWM1_GRP1_CNT6_LINE_SEL_BUFF | 0x4058832C | FULL | Counter buffered line selection register |
| TCPWM1_GRP1_CNT6_DT | 0x40588330 | FULL | Counter PWM dead time register |
| TCPWM1_GRP1_CNT6_TR_CMD | 0x40588340 | FULL | Counter trigger command register |
| TCPWM1_GRP1_CNT6_TR_IN_SEL0 | 0x40588344 | FULL | Counter input trigger selection register 0 |
| TCPWM1_GRP1_CNT6_TR_IN_SEL1 | 0x40588348 | FULL | Counter input trigger selection register 1 |
| TCPWM1_GRP1_CNT6_TR_IN_EDGE_SEL | 0x4058834C | FULL | Counter input trigger edge selection register |
| TCPWM1_GRP1_CNT6_TR_PWM_CTRL | 0x40588350 | FULL | Counter trigger PWM control register |
| TCPWM1_GRP1_CNT6_TR_OUT_SEL | 0x40588354 | FULL | Counter output trigger selection register |
| TCPWM1_GRP1_CNT6_INTR | 0x40588370 | FULL | Interrupt request register |
| TCPWM1_GRP1_CNT6_INTR_SET | 0x40588374 | FULL | Interrupt set request register |
| TCPWM1_GRP1_CNT6_INTR_MASK | 0x40588378 | FULL | Interrupt mask register |
| TCPWM1_GRP1_CNT6_INTR_MASKED | 0x4058837C | FULL | Interrupt masked request register |

### 33.2.2.8 CNT 7

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP1_CNT7_CTRL | 0x40588380 | FULL | Counter control register |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP1_CNT7_STATUS | 0x40588384 | FULL | Counter status register |
| TCPWM1_GRP1_CNT7_COUNTER | 0x40588388 | FULL | Counter count register |
| TCPWM1_GRP1_CNT7_CC0 | 0x40588390 | FULL | Counter compare/capture 0 register |
| TCPWM1_GRP1_CNT7_CC0_BUFF | 0x40588394 | FULL | Counter buffered compare/capture 0 register |
| TCPWM1_GRP1_CNT7_CC1 | 0x40588398 | FULL | Counter compare/capture 1 register |
| TCPWM1_GRP1_CNT7_CC1_BUFF | 0x4058839C | FULL | Counter buffered compare/capture 1 register |
| TCPWM1_GRP1_CNT7_PERIOD | 0x405883A0 | FULL | Counter period register |
| TCPWM1_GRP1_CNT7_PERIOD_BUFF | 0x405883A4 | FULL | Counter buffered period register |
| TCPWM1_GRP1_CNT7_LINE_SEL | 0x405883A8 | FULL | Counter line selection register |
| TCPWM1_GRP1_CNT7_LINE_SEL_BUFF | 0x405883AC | FULL | Counter buffered line selection register |
| TCPWM1_GRP1_CNT7_DT | 0x405883B0 | FULL | Counter PWM dead time register |
| TCPWM1_GRP1_CNT7_TR_CMD | 0x405883C0 | FULL | Counter trigger command register |
| TCPWM1_GRP1_CNT7_TR_IN_SEL0 | 0x405883C4 | FULL | Counter input trigger selection register 0 |
| TCPWM1_GRP1_CNT7_TR_IN_SEL1 | 0x405883C8 | FULL | Counter input trigger selection register 1 |
| TCPWM1_GRP1_CNT7_TR_IN_EDGE_SEL | 0x405883CC | FULL | Counter input trigger edge selection register |
| TCPWM1_GRP1_CNT7_TR_PWM_CTRL | 0x405883D0 | FULL | Counter trigger PWM control register |
| TCPWM1_GRP1_CNT7_TR_OUT_SEL | 0x405883D4 | FULL | Counter output trigger selection register |
| TCPWM1_GRP1_CNT7_INTR | 0x405883F0 | FULL | Interrupt request register |
| TCPWM1_GRP1_CNT7_INTR_SET | 0x405883F4 | FULL | Interrupt set request register |
| TCPWM1_GRP1_CNT7_INTR_MASK | 0x405883F8 | FULL | Interrupt mask register |
| TCPWM1_GRP1_CNT7_INTR_MASKED | 0x405883FC | FULL | Interrupt masked request register |

### 33.2.2.9 CNT 8

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP1_CNT8_CTRL | 0x40588400 | FULL | Counter control register |
| TCPWM1_GRP1_CNT8_STATUS | 0x40588404 | FULL | Counter status register |
| TCPWM1_GRP1_CNT8_COUNTER | 0x40588408 | FULL | Counter count register |
| TCPWM1_GRP1_CNT8_CC0 | 0x40588410 | FULL | Counter compare/capture 0 register |
| TCPWM1_GRP1_CNT8_CC0_BUFF | 0x40588414 | FULL | Counter buffered compare/capture 0 register |
| TCPWM1_GRP1_CNT8_CC1 | 0x40588418 | FULL | Counter compare/capture 1 register |
| TCPWM1_GRP1_CNT8_CC1_BUFF | 0x4058841C | FULL | Counter buffered compare/capture 1 register |
| TCPWM1_GRP1_CNT8_PERIOD | 0x40588420 | FULL | Counter period register |
| TCPWM1_GRP1_CNT8_PERIOD_BUFF | 0x40588424 | FULL | Counter buffered period register |
| TCPWM1_GRP1_CNT8_LINE_SEL | 0x40588428 | FULL | Counter line selection register |
| TCPWM1_GRP1_CNT8_LINE_SEL_BUFF | 0x4058842C | FULL | Counter buffered line selection register |
| TCPWM1_GRP1_CNT8_DT | 0x40588430 | FULL | Counter PWM dead time register |
| TCPWM1_GRP1_CNT8_TR_CMD | 0x40588440 | FULL | Counter trigger command register |
| TCPWM1_GRP1_CNT8_TR_IN_SEL0 | 0x40588444 | FULL | Counter input trigger selection register 0 |
| TCPWM1_GRP1_CNT8_TR_IN_SEL1 | 0x40588448 | FULL | Counter input trigger selection register 1 |
| TCPWM1_GRP1_CNT8_TR_IN_EDGE_SEL | 0x4058844C | FULL | Counter input trigger edge selection register |
| TCPWM1_GRP1_CNT8_TR_PWM_CTRL | 0x40588450 | FULL | Counter trigger PWM control register |
| TCPWM1_GRP1_CNT8_TR_OUT_SEL | 0x40588454 | FULL | Counter output trigger selection register |
| TCPWM1_GRP1_CNT8_INTR | 0x40588470 | FULL | Interrupt request register |
| TCPWM1_GRP1_CNT8_INTR_SET | 0x40588474 | FULL | Interrupt set request register |
| TCPWM1_GRP1_CNT8_INTR_MASK | 0x40588478 | FULL | Interrupt mask register |
| TCPWM1_GRP1_CNT8_INTR_MASKED | 0x4058847C | FULL | Interrupt masked request register |

### 33.2.2.10 CNT 9

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP1_CNT9_CTRL | 0x40588480 | FULL | Counter control register |
| TCPWM1_GRP1_CNT9_STATUS | 0x40588484 | FULL | Counter status register |
| TCPWM1_GRP1_CNT9_COUNTER | 0x40588488 | FULL | Counter count register |
| TCPWM1_GRP1_CNT9_CC0 | 0x40588490 | FULL | Counter compare/capture 0 register |
| TCPWM1_GRP1_CNT9_CC0_BUFF | 0x40588494 | FULL | Counter buffered compare/capture 0 register |
| TCPWM1_GRP1_CNT9_CC1 | 0x40588498 | FULL | Counter compare/capture 1 register |
| TCPWM1_GRP1_CNT9_CC1_BUFF | 0x4058849C | FULL | Counter buffered compare/capture 1 register |
| TCPWM1_GRP1_CNT9_PERIOD | 0x405884A0 | FULL | Counter period register |
| TCPWM1_GRP1_CNT9_PERIOD_BUFF | 0x405884A4 | FULL | Counter buffered period register |
| TCPWM1_GRP1_CNT9_LINE_SEL | 0x405884A8 | FULL | Counter line selection register |
| TCPWM1_GRP1_CNT9_LINE_SEL_BUFF | 0x405884AC | FULL | Counter buffered line selection register |
| TCPWM1_GRP1_CNT9_DT | 0x405884B0 | FULL | Counter PWM dead time register |
| TCPWM1_GRP1_CNT9_TR_CMD | 0x405884C0 | FULL | Counter trigger command register |
| TCPWM1_GRP1_CNT9_TR_IN_SEL0 | 0x405884C4 | FULL | Counter input trigger selection register 0 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP1_CNT9_TR_IN_SEL1 | 0x405884C8 | FULL | Counter input trigger selection register 1 |
| TCPWM1_GRP1_CNT9_TR_IN_EDGE_SEL | 0x405884CC | FULL | Counter input trigger edge selection register |
| TCPWM1_GRP1_CNT9_TR_PWM_CTRL | 0x405884D0 | FULL | Counter trigger PWM control register |
| TCPWM1_GRP1_CNT9_TR_OUT_SEL | 0x405884D4 | FULL | Counter output trigger selection register |
| TCPWM1_GRP1_CNT9_INTR | 0x405884F0 | FULL | Interrupt request register |
| TCPWM1_GRP1_CNT9_INTR_SET | 0x405884F4 | FULL | Interrupt set request register |
| TCPWM1_GRP1_CNT9_INTR_MASK | 0x405884F8 | FULL | Interrupt mask register |
| TCPWM1_GRP1_CNT9_INTR_MASKED | 0x405884FC | FULL | Interrupt masked request register |

#### 33.2.2.11 CNT 10

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP1_CNT10_CTRL | 0x40588500 | FULL | Counter control register |
| TCPWM1_GRP1_CNT10_STATUS | 0x40588504 | FULL | Counter status register |
| TCPWM1_GRP1_CNT10_COUNTER | 0x40588508 | FULL | Counter count register |
| TCPWM1_GRP1_CNT10_CC0 | 0x40588510 | FULL | Counter compare/capture 0 register |
| TCPWM1_GRP1_CNT10_CC0_BUFF | 0x40588514 | FULL | Counter buffered compare/capture 0 register |
| TCPWM1_GRP1_CNT10_CC1 | 0x40588518 | FULL | Counter compare/capture 1 register |
| TCPWM1_GRP1_CNT10_CC1_BUFF | 0x4058851C | FULL | Counter buffered compare/capture 1 register |
| TCPWM1_GRP1_CNT10_PERIOD | 0x40588520 | FULL | Counter period register |
| TCPWM1_GRP1_CNT10_PERIOD_BUFF | 0x40588524 | FULL | Counter buffered period register |
| TCPWM1_GRP1_CNT10_LINE_SEL | 0x40588528 | FULL | Counter line selection register |
| TCPWM1_GRP1_CNT10_LINE_SEL_BUFF | 0x4058852C | FULL | Counter buffered line selection register |
| TCPWM1_GRP1_CNT10_DT | 0x40588530 | FULL | Counter PWM dead time register |
| TCPWM1_GRP1_CNT10_TR_CMD | 0x40588540 | FULL | Counter trigger command register |
| TCPWM1_GRP1_CNT10_TR_IN_SEL0 | 0x40588544 | FULL | Counter input trigger selection register 0 |
| TCPWM1_GRP1_CNT10_TR_IN_SEL1 | 0x40588548 | FULL | Counter input trigger selection register 1 |
| TCPWM1_GRP1_CNT10_TR_IN_EDGE_SEL | 0x4058854C | FULL | Counter input trigger edge selection register |
| TCPWM1_GRP1_CNT10_TR_PWM_CTRL | 0x40588550 | FULL | Counter trigger PWM control register |
| TCPWM1_GRP1_CNT10_TR_OUT_SEL | 0x40588554 | FULL | Counter output trigger selection register |
| TCPWM1_GRP1_CNT10_INTR | 0x40588570 | FULL | Interrupt request register |
| TCPWM1_GRP1_CNT10_INTR_SET | 0x40588574 | FULL | Interrupt set request register |
| TCPWM1_GRP1_CNT10_INTR_MASK | 0x40588578 | FULL | Interrupt mask register |
| TCPWM1_GRP1_CNT10_INTR_MASKED | 0x4058857C | FULL | Interrupt masked request register |

#### 33.2.2.12 CNT 11

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP1_CNT11_CTRL | 0x40588580 | FULL | Counter control register |
| TCPWM1_GRP1_CNT11_STATUS | 0x40588584 | FULL | Counter status register |
| TCPWM1_GRP1_CNT11_COUNTER | 0x40588588 | FULL | Counter count register |
| TCPWM1_GRP1_CNT11_CC0 | 0x40588590 | FULL | Counter compare/capture 0 register |
| TCPWM1_GRP1_CNT11_CC0_BUFF | 0x40588594 | FULL | Counter buffered compare/capture 0 register |
| TCPWM1_GRP1_CNT11_CC1 | 0x40588598 | FULL | Counter compare/capture 1 register |
| TCPWM1_GRP1_CNT11_CC1_BUFF | 0x4058859C | FULL | Counter buffered compare/capture 1 register |
| TCPWM1_GRP1_CNT11_PERIOD | 0x405885A0 | FULL | Counter period register |
| TCPWM1_GRP1_CNT11_PERIOD_BUFF | 0x405885A4 | FULL | Counter buffered period register |
| TCPWM1_GRP1_CNT11_LINE_SEL | 0x405885A8 | FULL | Counter line selection register |
| TCPWM1_GRP1_CNT11_LINE_SEL_BUFF | 0x405885AC | FULL | Counter buffered line selection register |
| TCPWM1_GRP1_CNT11_DT | 0x405885B0 | FULL | Counter PWM dead time register |
| TCPWM1_GRP1_CNT11_TR_CMD | 0x405885C0 | FULL | Counter trigger command register |
| TCPWM1_GRP1_CNT11_TR_IN_SEL0 | 0x405885C4 | FULL | Counter input trigger selection register 0 |
| TCPWM1_GRP1_CNT11_TR_IN_SEL1 | 0x405885C8 | FULL | Counter input trigger selection register 1 |
| TCPWM1_GRP1_CNT11_TR_IN_EDGE_SEL | 0x405885CC | FULL | Counter input trigger edge selection register |
| TCPWM1_GRP1_CNT11_TR_PWM_CTRL | 0x405885D0 | FULL | Counter trigger PWM control register |
| TCPWM1_GRP1_CNT11_TR_OUT_SEL | 0x405885D4 | FULL | Counter output trigger selection register |
| TCPWM1_GRP1_CNT11_INTR | 0x405885F0 | FULL | Interrupt request register |
| TCPWM1_GRP1_CNT11_INTR_SET | 0x405885F4 | FULL | Interrupt set request register |
| TCPWM1_GRP1_CNT11_INTR_MASK | 0x405885F8 | FULL | Interrupt mask register |
| TCPWM1_GRP1_CNT11_INTR_MASKED | 0x405885FC | FULL | Interrupt masked request register |

### 33.2.3 GRP 2

#### 33.2.3.1 CNT 0

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP2_CNT0_CTRL | 0x40590000 | FULL | Counter control register<br>Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM1_GRP2_CNT0_STATUS | 0x40590004 | FULL | Counter status register<br>Note:DT_CNT_H is not available for this register |
| TCPWM1_GRP2_CNT0_COUNTER | 0x40590008 | FULL | Counter count register |
| TCPWM1_GRP2_CNT0_CC0 | 0x40590010 | FULL | Counter compare/capture 0 register |
| TCPWM1_GRP2_CNT0_CC0_BUFF | 0x40590014 | FULL | Counter buffered compare/capture 0 register |
| TCPWM1_GRP2_CNT0_CC1 | 0x40590018 | FULL | Counter compare/capture 1 register |
| TCPWM1_GRP2_CNT0_CC1_BUFF | 0x4059001C | FULL | Counter buffered compare/capture 1 register |
| TCPWM1_GRP2_CNT0_PERIOD | 0x40590020 | FULL | Counter period register |
| TCPWM1_GRP2_CNT0_PERIOD_BUFF | 0x40590024 | FULL | Counter buffered period register |
| TCPWM1_GRP2_CNT0_DT | 0x40590030 | FULL | Counter PWM dead time register<br>Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM1_GRP2_CNT0_TR_CMD | 0x40590040 | FULL | Counter trigger command register |
| TCPWM1_GRP2_CNT0_TR_IN_SEL0 | 0x40590044 | FULL | Counter input trigger selection register 0 |
| TCPWM1_GRP2_CNT0_TR_IN_SEL1 | 0x40590048 | FULL | Counter input trigger selection register 1 |
| TCPWM1_GRP2_CNT0_TR_IN_EDGE_SEL | 0x4059004C | FULL | Counter input trigger edge selection register |
| TCPWM1_GRP2_CNT0_TR_PWM_CTRL | 0x40590050 | FULL | Counter trigger PWM control register |
| TCPWM1_GRP2_CNT0_TR_OUT_SEL | 0x40590054 | FULL | Counter output trigger selection register |
| TCPWM1_GRP2_CNT0_INTR | 0x40590070 | FULL | Interrupt request register |
| TCPWM1_GRP2_CNT0_INTR_SET | 0x40590074 | FULL | Interrupt set request register |
| TCPWM1_GRP2_CNT0_INTR_MASK | 0x40590078 | FULL | Interrupt mask register |
| TCPWM1_GRP2_CNT0_INTR_MASKED | 0x4059007C | FULL | Interrupt masked request register |

### 33.2.3.2 CNT 1

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP2_CNT1_CTRL | 0x40590080 | FULL | Counter control register<br>Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM1_GRP2_CNT1_STATUS | 0x40590084 | FULL | Counter status register<br>Note:DT_CNT_H is not available for this register |
| TCPWM1_GRP2_CNT1_COUNTER | 0x40590088 | FULL | Counter count register |
| TCPWM1_GRP2_CNT1_CC0 | 0x40590090 | FULL | Counter compare/capture 0 register |
| TCPWM1_GRP2_CNT1_CC0_BUFF | 0x40590094 | FULL | Counter buffered compare/capture 0 register |
| TCPWM1_GRP2_CNT1_CC1 | 0x40590098 | FULL | Counter compare/capture 1 register |
| TCPWM1_GRP2_CNT1_CC1_BUFF | 0x4059009C | FULL | Counter buffered compare/capture 1 register |
| TCPWM1_GRP2_CNT1_PERIOD | 0x405900A0 | FULL | Counter period register |
| TCPWM1_GRP2_CNT1_PERIOD_BUFF | 0x405900A4 | FULL | Counter buffered period register |
| TCPWM1_GRP2_CNT1_DT | 0x405900B0 | FULL | Counter PWM dead time register<br>Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM1_GRP2_CNT1_TR_CMD | 0x405900C0 | FULL | Counter trigger command register |
| TCPWM1_GRP2_CNT1_TR_IN_SEL0 | 0x405900C4 | FULL | Counter input trigger selection register 0 |
| TCPWM1_GRP2_CNT1_TR_IN_SEL1 | 0x405900C8 | FULL | Counter input trigger selection register 1 |
| TCPWM1_GRP2_CNT1_TR_IN_EDGE_SEL | 0x405900CC | FULL | Counter input trigger edge selection register |
| TCPWM1_GRP2_CNT1_TR_PWM_CTRL | 0x405900D0 | FULL | Counter trigger PWM control register |
| TCPWM1_GRP2_CNT1_TR_OUT_SEL | 0x405900D4 | FULL | Counter output trigger selection register |
| TCPWM1_GRP2_CNT1_INTR | 0x405900F0 | FULL | Interrupt request register |
| TCPWM1_GRP2_CNT1_INTR_SET | 0x405900F4 | FULL | Interrupt set request register |
| TCPWM1_GRP2_CNT1_INTR_MASK | 0x405900F8 | FULL | Interrupt mask register |
| TCPWM1_GRP2_CNT1_INTR_MASKED | 0x405900FC | FULL | Interrupt masked request register |

### 33.2.3.3 CNT 2

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP2_CNT2_CTRL | 0x40590100 | FULL | Counter control register<br>Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP2_CNT2_STATUS | 0x40590104 | FULL | Counter status register<br>Note:DT_CNT_H is not available for this register |
| TCPWM1_GRP2_CNT2_COUNTER | 0x40590108 | FULL | Counter count register |
| TCPWM1_GRP2_CNT2_CC0 | 0x40590110 | FULL | Counter compare/capture 0 register |
| TCPWM1_GRP2_CNT2_CC0_BUFF | 0x40590114 | FULL | Counter buffered compare/capture 0 register |
| TCPWM1_GRP2_CNT2_CC1 | 0x40590118 | FULL | Counter compare/capture 1 register |
| TCPWM1_GRP2_CNT2_CC1_BUFF | 0x4059011C | FULL | Counter buffered compare/capture 1 register |
| TCPWM1_GRP2_CNT2_PERIOD | 0x40590120 | FULL | Counter period register |
| TCPWM1_GRP2_CNT2_PERIOD_BUFF | 0x40590124 | FULL | Counter buffered period register |
| TCPWM1_GRP2_CNT2_DT | 0x40590130 | FULL | Counter PWM dead time register<br>Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM1_GRP2_CNT2_TR_CMD | 0x40590140 | FULL | Counter trigger command register |
| TCPWM1_GRP2_CNT2_TR_IN_SEL0 | 0x40590144 | FULL | Counter input trigger selection register 0 |
| TCPWM1_GRP2_CNT2_TR_IN_SEL1 | 0x40590148 | FULL | Counter input trigger selection register 1 |
| TCPWM1_GRP2_CNT2_TR_IN_EDGE_SEL | 0x4059014C | FULL | Counter input trigger edge selection register |
| TCPWM1_GRP2_CNT2_TR_PWM_CTRL | 0x40590150 | FULL | Counter trigger PWM control register |
| TCPWM1_GRP2_CNT2_TR_OUT_SEL | 0x40590154 | FULL | Counter output trigger selection register |
| TCPWM1_GRP2_CNT2_INTR | 0x40590170 | FULL | Interrupt request register |
| TCPWM1_GRP2_CNT2_INTR_SET | 0x40590174 | FULL | Interrupt set request register |
| TCPWM1_GRP2_CNT2_INTR_MASK | 0x40590178 | FULL | Interrupt mask register |
| TCPWM1_GRP2_CNT2_INTR_MASKED | 0x4059017C | FULL | Interrupt masked request register |

### 33.2.3.4 CNT 3

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP2_CNT3_CTRL | 0x40590180 | FULL | Counter control register<br>Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM1_GRP2_CNT3_STATUS | 0x40590184 | FULL | Counter status register<br>Note:DT_CNT_H is not available for this register |
| TCPWM1_GRP2_CNT3_COUNTER | 0x40590188 | FULL | Counter count register |
| TCPWM1_GRP2_CNT3_CC0 | 0x40590190 | FULL | Counter compare/capture 0 register |
| TCPWM1_GRP2_CNT3_CC0_BUFF | 0x40590194 | FULL | Counter buffered compare/capture 0 register |
| TCPWM1_GRP2_CNT3_CC1 | 0x40590198 | FULL | Counter compare/capture 1 register |
| TCPWM1_GRP2_CNT3_CC1_BUFF | 0x4059019C | FULL | Counter buffered compare/capture 1 register |
| TCPWM1_GRP2_CNT3_PERIOD | 0x405901A0 | FULL | Counter period register |
| TCPWM1_GRP2_CNT3_PERIOD_BUFF | 0x405901A4 | FULL | Counter buffered period register |
| TCPWM1_GRP2_CNT3_DT | 0x405901B0 | FULL | Counter PWM dead time register<br>Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM1_GRP2_CNT3_TR_CMD | 0x405901C0 | FULL | Counter trigger command register |
| TCPWM1_GRP2_CNT3_TR_IN_SEL0 | 0x405901C4 | FULL | Counter input trigger selection register 0 |
| TCPWM1_GRP2_CNT3_TR_IN_SEL1 | 0x405901C8 | FULL | Counter input trigger selection register 1 |
| TCPWM1_GRP2_CNT3_TR_IN_EDGE_SEL | 0x405901CC | FULL | Counter input trigger edge selection register |
| TCPWM1_GRP2_CNT3_TR_PWM_CTRL | 0x405901D0 | FULL | Counter trigger PWM control register |
| TCPWM1_GRP2_CNT3_TR_OUT_SEL | 0x405901D4 | FULL | Counter output trigger selection register |
| TCPWM1_GRP2_CNT3_INTR | 0x405901F0 | FULL | Interrupt request register |
| TCPWM1_GRP2_CNT3_INTR_SET | 0x405901F4 | FULL | Interrupt set request register |
| TCPWM1_GRP2_CNT3_INTR_MASK | 0x405901F8 | FULL | Interrupt mask register |
| TCPWM1_GRP2_CNT3_INTR_MASKED | 0x405901FC | FULL | Interrupt masked request register |

### 33.2.3.5 CNT 4

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP2_CNT4_CTRL | 0x40590200 | FULL | Counter control register<br>Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM1_GRP2_CNT4_STATUS | 0x40590204 | FULL | Counter status register<br>Note:DT_CNT_H is not available for this register |
| TCPWM1_GRP2_CNT4_COUNTER | 0x40590208 | FULL | Counter count register |
| TCPWM1_GRP2_CNT4_CC0 | 0x40590210 | FULL | Counter compare/capture 0 register |
| TCPWM1_GRP2_CNT4_CC0_BUFF | 0x40590214 | FULL | Counter buffered compare/capture 0 register |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP2_CNT4_CC1 | 0x40590218 | FULL | Counter compare/capture 1 register |
| TCPWM1_GRP2_CNT4_CC1_BUFF | 0x4059021C | FULL | Counter buffered compare/capture 1 register |
| TCPWM1_GRP2_CNT4_PERIOD | 0x40590220 | FULL | Counter period register |
| TCPWM1_GRP2_CNT4_PERIOD_BUFF | 0x40590224 | FULL | Counter buffered period register |
| TCPWM1_GRP2_CNT4_DT | 0x40590230 | FULL | Counter PWM dead time register Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM1_GRP2_CNT4_TR_CMD | 0x40590240 | FULL | Counter trigger command register |
| TCPWM1_GRP2_CNT4_TR_IN_SEL0 | 0x40590244 | FULL | Counter input trigger selection register 0 |
| TCPWM1_GRP2_CNT4_TR_IN_SEL1 | 0x40590248 | FULL | Counter input trigger selection register 1 |
| TCPWM1_GRP2_CNT4_TR_IN_EDGE_SEL | 0x4059024C | FULL | Counter input trigger edge selection register |
| TCPWM1_GRP2_CNT4_TR_PWM_CTRL | 0x40590250 | FULL | Counter trigger PWM control register |
| TCPWM1_GRP2_CNT4_TR_OUT_SEL | 0x40590254 | FULL | Counter output trigger selection register |
| TCPWM1_GRP2_CNT4_INTR | 0x40590270 | FULL | Interrupt request register |
| TCPWM1_GRP2_CNT4_INTR_SET | 0x40590274 | FULL | Interrupt set request register |
| TCPWM1_GRP2_CNT4_INTR_MASK | 0x40590278 | FULL | Interrupt mask register |
| TCPWM1_GRP2_CNT4_INTR_MASKED | 0x4059027C | FULL | Interrupt masked request register |

### 33.2.3.6 CNT 5

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP2_CNT5_CTRL | 0x40590280 | FULL | Counter control register Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM1_GRP2_CNT5_STATUS | 0x40590284 | FULL | Counter status register Note:DT_CNT_H is not available for this register |
| TCPWM1_GRP2_CNT5_COUNTER | 0x40590288 | FULL | Counter count register |
| TCPWM1_GRP2_CNT5_CC0 | 0x40590290 | FULL | Counter compare/capture 0 register |
| TCPWM1_GRP2_CNT5_CC0_BUFF | 0x40590294 | FULL | Counter buffered compare/capture 0 register |
| TCPWM1_GRP2_CNT5_CC1 | 0x40590298 | FULL | Counter compare/capture 1 register |
| TCPWM1_GRP2_CNT5_CC1_BUFF | 0x4059029C | FULL | Counter buffered compare/capture 1 register |
| TCPWM1_GRP2_CNT5_PERIOD | 0x405902A0 | FULL | Counter period register |
| TCPWM1_GRP2_CNT5_PERIOD_BUFF | 0x405902A4 | FULL | Counter buffered period register |
| TCPWM1_GRP2_CNT5_DT | 0x405902B0 | FULL | Counter PWM dead time register Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM1_GRP2_CNT5_TR_CMD | 0x405902C0 | FULL | Counter trigger command register |
| TCPWM1_GRP2_CNT5_TR_IN_SEL0 | 0x405902C4 | FULL | Counter input trigger selection register 0 |
| TCPWM1_GRP2_CNT5_TR_IN_SEL1 | 0x405902C8 | FULL | Counter input trigger selection register 1 |
| TCPWM1_GRP2_CNT5_TR_IN_EDGE_SEL | 0x405902CC | FULL | Counter input trigger edge selection register |
| TCPWM1_GRP2_CNT5_TR_PWM_CTRL | 0x405902D0 | FULL | Counter trigger PWM control register |
| TCPWM1_GRP2_CNT5_TR_OUT_SEL | 0x405902D4 | FULL | Counter output trigger selection register |
| TCPWM1_GRP2_CNT5_INTR | 0x405902F0 | FULL | Interrupt request register |
| TCPWM1_GRP2_CNT5_INTR_SET | 0x405902F4 | FULL | Interrupt set request register |
| TCPWM1_GRP2_CNT5_INTR_MASK | 0x405902F8 | FULL | Interrupt mask register |
| TCPWM1_GRP2_CNT5_INTR_MASKED | 0x405902FC | FULL | Interrupt masked request register |

### 33.2.3.7 CNT 6

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP2_CNT6_CTRL | 0x40590300 | FULL | Counter control register Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM1_GRP2_CNT6_STATUS | 0x40590304 | FULL | Counter status register Note:DT_CNT_H is not available for this register |
| TCPWM1_GRP2_CNT6_COUNTER | 0x40590308 | FULL | Counter count register |
| TCPWM1_GRP2_CNT6_CC0 | 0x40590310 | FULL | Counter compare/capture 0 register |
| TCPWM1_GRP2_CNT6_CC0_BUFF | 0x40590314 | FULL | Counter buffered compare/capture 0 register |
| TCPWM1_GRP2_CNT6_CC1 | 0x40590318 | FULL | Counter compare/capture 1 register |
| TCPWM1_GRP2_CNT6_CC1_BUFF | 0x4059031C | FULL | Counter buffered compare/capture 1 register |
| TCPWM1_GRP2_CNT6_PERIOD | 0x40590320 | FULL | Counter period register |
| TCPWM1_GRP2_CNT6_PERIOD_BUFF | 0x40590324 | FULL | Counter buffered period register |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP2_CNT6_DT | 0x40590330 | FULL | Counter PWM dead time register<br>Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM1_GRP2_CNT6_TR_CMD | 0x40590340 | FULL | Counter trigger command register |
| TCPWM1_GRP2_CNT6_TR_IN_SEL0 | 0x40590344 | FULL | Counter input trigger selection register 0 |
| TCPWM1_GRP2_CNT6_TR_IN_SEL1 | 0x40590348 | FULL | Counter input trigger selection register 1 |
| TCPWM1_GRP2_CNT6_TR_IN_EDGE_SEL | 0x4059034C | FULL | Counter input trigger edge selection register |
| TCPWM1_GRP2_CNT6_TR_PWM_CTRL | 0x40590350 | FULL | Counter trigger PWM control register |
| TCPWM1_GRP2_CNT6_TR_OUT_SEL | 0x40590354 | FULL | Counter output trigger selection register |
| TCPWM1_GRP2_CNT6_INTR | 0x40590370 | FULL | Interrupt request register |
| TCPWM1_GRP2_CNT6_INTR_SET | 0x40590374 | FULL | Interrupt set request register |
| TCPWM1_GRP2_CNT6_INTR_MASK | 0x40590378 | FULL | Interrupt mask register |
| TCPWM1_GRP2_CNT6_INTR_MASKED | 0x4059037C | FULL | Interrupt masked request register |

### 33.2.3.8 CNT 7

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP2_CNT7_CTRL | 0x40590380 | FULL | Counter control register<br>Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM1_GRP2_CNT7_STATUS | 0x40590384 | FULL | Counter status register<br>Note:DT_CNT_H is not available for this register |
| TCPWM1_GRP2_CNT7_COUNTER | 0x40590388 | FULL | Counter count register |
| TCPWM1_GRP2_CNT7_CC0 | 0x40590390 | FULL | Counter compare/capture 0 register |
| TCPWM1_GRP2_CNT7_CC0_BUFF | 0x40590394 | FULL | Counter buffered compare/capture 0 register |
| TCPWM1_GRP2_CNT7_CC1 | 0x40590398 | FULL | Counter compare/capture 1 register |
| TCPWM1_GRP2_CNT7_CC1_BUFF | 0x4059039C | FULL | Counter buffered compare/capture 1 register |
| TCPWM1_GRP2_CNT7_PERIOD | 0x405903A0 | FULL | Counter period register |
| TCPWM1_GRP2_CNT7_PERIOD_BUFF | 0x405903A4 | FULL | Counter buffered period register |
| TCPWM1_GRP2_CNT7_DT | 0x405903B0 | FULL | Counter PWM dead time register<br>Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM1_GRP2_CNT7_TR_CMD | 0x405903C0 | FULL | Counter trigger command register |
| TCPWM1_GRP2_CNT7_TR_IN_SEL0 | 0x405903C4 | FULL | Counter input trigger selection register 0 |
| TCPWM1_GRP2_CNT7_TR_IN_SEL1 | 0x405903C8 | FULL | Counter input trigger selection register 1 |
| TCPWM1_GRP2_CNT7_TR_IN_EDGE_SEL | 0x405903CC | FULL | Counter input trigger edge selection register |
| TCPWM1_GRP2_CNT7_TR_PWM_CTRL | 0x405903D0 | FULL | Counter trigger PWM control register |
| TCPWM1_GRP2_CNT7_TR_OUT_SEL | 0x405903D4 | FULL | Counter output trigger selection register |
| TCPWM1_GRP2_CNT7_INTR | 0x405903F0 | FULL | Interrupt request register |
| TCPWM1_GRP2_CNT7_INTR_SET | 0x405903F4 | FULL | Interrupt set request register |
| TCPWM1_GRP2_CNT7_INTR_MASK | 0x405903F8 | FULL | Interrupt mask register |
| TCPWM1_GRP2_CNT7_INTR_MASKED | 0x405903FC | FULL | Interrupt masked request register |

### 33.2.3.9 CNT 8

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP2_CNT8_CTRL | 0x40590400 | FULL | Counter control register<br>Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM1_GRP2_CNT8_STATUS | 0x40590404 | FULL | Counter status register<br>Note:DT_CNT_H is not available for this register |
| TCPWM1_GRP2_CNT8_COUNTER | 0x40590408 | FULL | Counter count register |
| TCPWM1_GRP2_CNT8_CC0 | 0x40590410 | FULL | Counter compare/capture 0 register |
| TCPWM1_GRP2_CNT8_CC0_BUFF | 0x40590414 | FULL | Counter buffered compare/capture 0 register |
| TCPWM1_GRP2_CNT8_CC1 | 0x40590418 | FULL | Counter compare/capture 1 register |
| TCPWM1_GRP2_CNT8_CC1_BUFF | 0x4059041C | FULL | Counter buffered compare/capture 1 register |
| TCPWM1_GRP2_CNT8_PERIOD | 0x40590420 | FULL | Counter period register |
| TCPWM1_GRP2_CNT8_PERIOD_BUFF | 0x40590424 | FULL | Counter buffered period register |
| TCPWM1_GRP2_CNT8_DT | 0x40590430 | FULL | Counter PWM dead time register<br>Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM1_GRP2_CNT8_TR_CMD | 0x40590440 | FULL | Counter trigger command register |
| TCPWM1_GRP2_CNT8_TR_IN_SEL0 | 0x40590444 | FULL | Counter input trigger selection register 0 |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP2_CNT8_TR_IN_SEL1 | 0x40590448 | FULL | Counter input trigger selection register 1 |
| TCPWM1_GRP2_CNT8_TR_IN_EDGE_SEL | 0x4059044C | FULL | Counter input trigger edge selection register |
| TCPWM1_GRP2_CNT8_TR_PWM_CTRL | 0x40590450 | FULL | Counter trigger PWM control register |
| TCPWM1_GRP2_CNT8_TR_OUT_SEL | 0x40590454 | FULL | Counter output trigger selection register |
| TCPWM1_GRP2_CNT8_INTR | 0x40590470 | FULL | Interrupt request register |
| TCPWM1_GRP2_CNT8_INTR_SET | 0x40590474 | FULL | Interrupt set request register |
| TCPWM1_GRP2_CNT8_INTR_MASK | 0x40590478 | FULL | Interrupt mask register |
| TCPWM1_GRP2_CNT8_INTR_MASKED | 0x4059047C | FULL | Interrupt masked request register |

### 33.2.3.10 CNT 9

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP2_CNT9_CTRL | 0x40590480 | FULL | Counter control register<br>Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM1_GRP2_CNT9_STATUS | 0x40590484 | FULL | Counter status register<br>Note:DT_CNT_H is not available for this register |
| TCPWM1_GRP2_CNT9_COUNTER | 0x40590488 | FULL | Counter count register |
| TCPWM1_GRP2_CNT9_CC0 | 0x40590490 | FULL | Counter compare/capture 0 register |
| TCPWM1_GRP2_CNT9_CC0_BUFF | 0x40590494 | FULL | Counter buffered compare/capture 0 register |
| TCPWM1_GRP2_CNT9_CC1 | 0x40590498 | FULL | Counter compare/capture 1 register |
| TCPWM1_GRP2_CNT9_CC1_BUFF | 0x4059049C | FULL | Counter buffered compare/capture 1 register |
| TCPWM1_GRP2_CNT9_PERIOD | 0x405904A0 | FULL | Counter period register |
| TCPWM1_GRP2_CNT9_PERIOD_BUFF | 0x405904A4 | FULL | Counter buffered period register |
| TCPWM1_GRP2_CNT9_DT | 0x405904B0 | FULL | Counter PWM dead time register<br>Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM1_GRP2_CNT9_TR_CMD | 0x405904C0 | FULL | Counter trigger command register |
| TCPWM1_GRP2_CNT9_TR_IN_SEL0 | 0x405904C4 | FULL | Counter input trigger selection register 0 |
| TCPWM1_GRP2_CNT9_TR_IN_SEL1 | 0x405904C8 | FULL | Counter input trigger selection register 1 |
| TCPWM1_GRP2_CNT9_TR_IN_EDGE_SEL | 0x405904CC | FULL | Counter input trigger edge selection register |
| TCPWM1_GRP2_CNT9_TR_PWM_CTRL | 0x405904D0 | FULL | Counter trigger PWM control register |
| TCPWM1_GRP2_CNT9_TR_OUT_SEL | 0x405904D4 | FULL | Counter output trigger selection register |
| TCPWM1_GRP2_CNT9_INTR | 0x405904F0 | FULL | Interrupt request register |
| TCPWM1_GRP2_CNT9_INTR_SET | 0x405904F4 | FULL | Interrupt set request register |
| TCPWM1_GRP2_CNT9_INTR_MASK | 0x405904F8 | FULL | Interrupt mask register |
| TCPWM1_GRP2_CNT9_INTR_MASKED | 0x405904FC | FULL | Interrupt masked request register |

### 33.2.3.11 CNT 10

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP2_CNT10_CTRL | 0x40590500 | FULL | Counter control register<br>Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM1_GRP2_CNT10_STATUS | 0x40590504 | FULL | Counter status register<br>Note:DT_CNT_H is not available for this register |
| TCPWM1_GRP2_CNT10_COUNTER | 0x40590508 | FULL | Counter count register |
| TCPWM1_GRP2_CNT10_CC0 | 0x40590510 | FULL | Counter compare/capture 0 register |
| TCPWM1_GRP2_CNT10_CC0_BUFF | 0x40590514 | FULL | Counter buffered compare/capture 0 register |
| TCPWM1_GRP2_CNT10_CC1 | 0x40590518 | FULL | Counter compare/capture 1 register |
| TCPWM1_GRP2_CNT10_CC1_BUFF | 0x4059051C | FULL | Counter buffered compare/capture 1 register |
| TCPWM1_GRP2_CNT10_PERIOD | 0x40590520 | FULL | Counter period register |
| TCPWM1_GRP2_CNT10_PERIOD_BUFF | 0x40590524 | FULL | Counter buffered period register |
| TCPWM1_GRP2_CNT10_DT | 0x40590530 | FULL | Counter PWM dead time register<br>Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM1_GRP2_CNT10_TR_CMD | 0x40590540 | FULL | Counter trigger command register |
| TCPWM1_GRP2_CNT10_TR_IN_SEL0 | 0x40590544 | FULL | Counter input trigger selection register 0 |
| TCPWM1_GRP2_CNT10_TR_IN_SEL1 | 0x40590548 | FULL | Counter input trigger selection register 1 |
| TCPWM1_GRP2_CNT10_TR_IN_EDGE_SEL | 0x4059054C | FULL | Counter input trigger edge selection register |
| TCPWM1_GRP2_CNT10_TR_PWM_CTRL | 0x40590550 | FULL | Counter trigger PWM control register |
| TCPWM1_GRP2_CNT10_TR_OUT_SEL | 0x40590554 | FULL | Counter output trigger selection register |
| TCPWM1_GRP2_CNT10_INTR | 0x40590570 | FULL | Interrupt request register |

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP2_CNT10_INTR_SET | 0x40590574 | FULL | Interrupt set request register |
| TCPWM1_GRP2_CNT10_INTR_MASK | 0x40590578 | FULL | Interrupt mask register |
| TCPWM1_GRP2_CNT10_INTR_MASKED | 0x4059057C | FULL | Interrupt masked request register |

### 33.2.3.12 CNT 11

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP2_CNT11_CTRL | 0x40590580 | FULL | Counter control register<br>Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM1_GRP2_CNT11_STATUS | 0x40590584 | FULL | Counter status register<br>Note:DT_CNT_H is not available for this register |
| TCPWM1_GRP2_CNT11_COUNTER | 0x40590588 | FULL | Counter count register |
| TCPWM1_GRP2_CNT11_CC0 | 0x40590590 | FULL | Counter compare/capture 0 register |
| TCPWM1_GRP2_CNT11_CC0_BUFF | 0x40590594 | FULL | Counter buffered compare/capture 0 register |
| TCPWM1_GRP2_CNT11_CC1 | 0x40590598 | FULL | Counter compare/capture 1 register |
| TCPWM1_GRP2_CNT11_CC1_BUFF | 0x4059059C | FULL | Counter buffered compare/capture 1 register |
| TCPWM1_GRP2_CNT11_PERIOD | 0x405905A0 | FULL | Counter period register |
| TCPWM1_GRP2_CNT11_PERIOD_BUFF | 0x405905A4 | FULL | Counter buffered period register |
| TCPWM1_GRP2_CNT11_DT | 0x405905B0 | FULL | Counter PWM dead time register<br>Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM1_GRP2_CNT11_TR_CMD | 0x405905C0 | FULL | Counter trigger command register |
| TCPWM1_GRP2_CNT11_TR_IN_SEL0 | 0x405905C4 | FULL | Counter input trigger selection register 0 |
| TCPWM1_GRP2_CNT11_TR_IN_SEL1 | 0x405905C8 | FULL | Counter input trigger selection register 1 |
| TCPWM1_GRP2_CNT11_TR_IN_EDGE_SEL | 0x405905CC | FULL | Counter input trigger edge selection register |
| TCPWM1_GRP2_CNT11_TR_PWM_CTRL | 0x405905D0 | FULL | Counter trigger PWM control register |
| TCPWM1_GRP2_CNT11_TR_OUT_SEL | 0x405905D4 | FULL | Counter output trigger selection register |
| TCPWM1_GRP2_CNT11_INTR | 0x405905F0 | FULL | Interrupt request register |
| TCPWM1_GRP2_CNT11_INTR_SET | 0x405905F4 | FULL | Interrupt set request register |
| TCPWM1_GRP2_CNT11_INTR_MASK | 0x405905F8 | FULL | Interrupt mask register |
| TCPWM1_GRP2_CNT11_INTR_MASKED | 0x405905FC | FULL | Interrupt masked request register |

### 33.2.3.13 CNT 12

| Register Name | Address | Permission | Description |
|---|---|---|---|
| TCPWM1_GRP2_CNT12_CTRL | 0x40590600 | FULL | Counter control register<br>Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM1_GRP2_CNT12_STATUS | 0x40590604 | FULL | Counter status register<br>Note:DT_CNT_H is not available for this register |
| TCPWM1_GRP2_CNT12_COUNTER | 0x40590608 | FULL | Counter count register |
| TCPWM1_GRP2_CNT12_CC0 | 0x40590610 | FULL | Counter compare/capture 0 register |
| TCPWM1_GRP2_CNT12_CC0_BUFF | 0x40590614 | FULL | Counter buffered compare/capture 0 register |
| TCPWM1_GRP2_CNT12_CC1 | 0x40590618 | FULL | Counter compare/capture 1 register |
| TCPWM1_GRP2_CNT12_CC1_BUFF | 0x4059061C | FULL | Counter buffered compare/capture 1 register |
| TCPWM1_GRP2_CNT12_PERIOD | 0x40590620 | FULL | Counter period register |
| TCPWM1_GRP2_CNT12_PERIOD_BUFF | 0x40590624 | FULL | Counter buffered period register |
| TCPWM1_GRP2_CNT12_DT | 0x40590630 | FULL | Counter PWM dead time register<br>Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM1_GRP2_CNT12_TR_CMD | 0x40590640 | FULL | Counter trigger command register |
| TCPWM1_GRP2_CNT12_TR_IN_SEL0 | 0x40590644 | FULL | Counter input trigger selection register 0 |
| TCPWM1_GRP2_CNT12_TR_IN_SEL1 | 0x40590648 | FULL | Counter input trigger selection register 1 |
| TCPWM1_GRP2_CNT12_TR_IN_EDGE_SEL | 0x4059064C | FULL | Counter input trigger edge selection register |
| TCPWM1_GRP2_CNT12_TR_PWM_CTRL | 0x40590650 | FULL | Counter trigger PWM control register |
| TCPWM1_GRP2_CNT12_TR_OUT_SEL | 0x40590654 | FULL | Counter output trigger selection register |
| TCPWM1_GRP2_CNT12_INTR | 0x40590670 | FULL | Interrupt request register |
| TCPWM1_GRP2_CNT12_INTR_SET | 0x40590674 | FULL | Interrupt set request register |
| TCPWM1_GRP2_CNT12_INTR_MASK | 0x40590678 | FULL | Interrupt mask register |
| TCPWM1_GRP2_CNT12_INTR_MASKED | 0x4059067C | FULL | Interrupt masked request register |

## 33.3 Register Details

### 33.3.1 GRP

### 33.3.1.1 CNT

#### 33.3.1.1.1 TCPWM_GRP_CNT_CTRL

**Description:** Counter control register
**Address:** 0x40380000
**Offset:** 0x0
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xF0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | CC1_MATCH_DOWN_EN [7:7] | CC1_MATCH_UP_EN [6:6] | CC0_MATCH_DOWN_EN [5:5] | CC0_MATCH_UP_EN [4:4] | AUTO_RELOAD_LINE_SEL [3:3] | AUTO_RELOAD_PERIOD [2:2] | AUTO_RELOAD_CC1 [1:1] | AUTO_RELOAD_CC0 [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:14] | | PWM_DISABLE_MODE [13:12] | | None [11:11] | PWM_SYNC_KILL [10:10] | PWM_STOP_ON_KILL [9:9] | PWM_IMM_KILL [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:22] | | QUAD_ENCODING_MODE [21:20] | | None [19:19] | ONE_SHOT [18:18] | UP_DOWN_MODE [17:16] | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | ENABLED [31:31] | DBG_FREEZE_EN [30:30] | None [29:27] | | | MODE [26:24] | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | AUTO_RELOAD_CC0 | RW | R | 0 | Specifies switching of the CC0 and buffered CC0 values. This field has a function in TIMER, QUAD (QUAD_RANGE0_CMP, QUAD_RANGE1_CMP range modes), SR, PWM, PWM_DT and PWM_PR modes.<br>Timer, QUAD, SR modes:<br>'0': never switch.<br>'1': switch on a compare match 0 event.<br>PWM, PWM_DT, PWM_PR modes:<br>'0: never switch.<br>'1': switch on a terminal count event with an actively pending switch event. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 1 | AUTO_RELOAD_CC1 | RW | R | 0 | Specifies switching of the CC1 and buffered CC1 values. This field has a function in TIMER, QUAD (QUAD_RANGE0_CMP, QUAD_RANGE1_CMP range modes), SR, PWM, PWM_DT and PWM_PR modes.<br>Timer, QUAD, SR modes:<br>'0': never switch.<br>'1': switch on a compare match 1 event.<br>PWM, PWM_DT, PWM_PR modes:<br>'0: never switch.<br>'1': switch on a terminal count event with an actively pending switch event. |
| 2 | AUTO_RELOAD _PERIOD | RW | R | 0 | Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes.<br>'0': never switch.<br>'1': switch on a terminal count event with and actively pending switch event.<br><br>In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function.<br>'0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event.<br>'1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff. |
| 3 | AUTO_RELOAD_LINE _SEL | RW | R | 0 | Specifies switching of the LINE_SEL and LINE_BUFF_SEL values. This field has a function in PWM and PWM_PR modes.<br>'0': never switch.<br>'1': switch on a terminal count event with and actively pending switch event. |
| 4 | CC0_MATCH_UP_EN | RW | R | 1 | Enables / disables the compare match 0 event generation (COUNTER equals CC0 register) when counting up (STATUS.DOWN = 0) in CNT_UPDN1/2 mode.<br>'0': compare match 0 event generation disabled when counting up<br>'1': compare match 0 event generation enabled when counting up<br><br>This field has a function in PWM and PWM_DT modes only. |
| 5 | CC0_MATCH_DOWN_EN | RW | R | 1 | Enables / disables the compare match 0 event generation (COUNTER equals CC0 register) when counting down (STATUS.DOWN = 1) in CNT_UPDN1/2 mode.<br>'0': compare match 0 event generation disabled when counting down<br>'1': compare match 0 event generation enabled when counting down<br><br>This field has a function in PWM and PWM_DT modes only. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 6 | CC1_MATCH_UP_EN | RW | R | 1 | Enables / disables the compare match 1 event generation (COUNTER equals CC0 register) when counting up (STATUS.DOWN = 0) in CNT_UPDN1/2 mode.<br>'0': compare match 1 event generation disabled when counting up<br>'1': compare match 1 event generation enabled when counting up<br><br>This field has a function in PWM and PWM_DT modes only. |
| 7 | CC1_MATCH_DOWN_EN | RW | R | 1 | Enables / disables the compare match 1 event generation (COUNTER equals CC0 register) when counting down (STATUS.DOWN = 1) in CNT_UPDN1/2 mode.<br>'0': compare match 1 event generation disabled when counting down<br>'1': compare match 1 event generation enabled when counting down<br><br>This field has a function in PWM and PWM_DT modes only. |
| 8 | PWM_IMM_KILL | RW | R | 0 | Specifies whether the kill event immediately deactivates the 'dt_line_out' and 'dt_line_compl_out' signals or with the next module clock ('active count' pre-scaled 'clk_counter').<br>'0': synchronous kill activation. Deactivates the 'dt_line_out' and 'dt_line_compl_out' signals with the next module clock ('active count' pre-scaled 'clk_counter').<br>'1': immediate kill activation. Immediately deactivates the 'dt_line_out' and 'dt_line_compl_out' signals.<br><br>This field has a function in PWM, PWM_DT and PWM_PR modes only. |
| 9 | PWM_STOP_ON_KILL | RW | R | 0 | Specifies whether the counter stops on a kill events:<br>'0': kill event does NOT stop counter.<br>'1': kill event stops counter.<br><br>This field has a function in PWM, PWM_DT and PWM_PR modes only. |
| 10 | PWM_SYNC_KILL | RW | R | 0 | Specifies asynchronous/synchronous kill behavior:<br>'1': synchronous kill mode: the kill event disables the 'dt_line_out' and 'dt_line_compl_out' signals till the next terminal count event (synchronous kill). In synchronous kill mode, STOP_EDGE should be RISING_EDGE.<br>'0': asynchronous kill mode: the kill event only disables the 'dt_line_out' and 'dt_line_compl_out' signals when present. In asynchronous kill mode, STOP_EDGE should be NO_EDGE_DET.<br><br>This field has a function in PWM and PWM_DT modes only. This field is only used when PWM_STOP_ON_KILL is '0'. |
| 12:13 | PWM_DISABLE_MODE | RW | R | 0 | Specifies the behavior of the PWM outputs 'line_out' and 'line_compl_out' while the TCPWM counter is disabled (CTL.ENABLED='0') or stopped.<br><br>Note: The output signal of this selection can be further modified by the immediate kill logic and line_out polarity settings (CTRL.QUAD_ENCODING_MODE). |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| | Z | | | 0 | When the counter is disabled the PWM outputs 'line_out' and 'line_compl_out' are NOT driven by the TCPWM. Instead the port default level configuration applies, e.g. 'Z' (high impedance).<br>Note: This is realized by driving the TCPWM output 'line_out_en' to 0.<br><br>When the counter is stopped upon a stop event the PWM outputs are deactivated (to the polarity defined by CTL.QUAD_ENCODING_MODE). |
| | RETAIN | | | 1 | When the counter is disabled the PWM outputs 'line_out' and 'line_compl_out' are driven by the TCPWM.<br>When the counter is disabled or stopped upon a stop event the PWM outputs are retained (keep their previous levels).<br>While the counter is disabled or stopped the PWM outputs can be changed via LINE_SEL (when parameter GRP_SMC_PRESENT = 1). |
| | L | | | 2 | When the counter is disabled the PWM outputs 'line_out' and 'line_compl_out' are driven by the TCPWM.<br>When the counter is disabled or stopped upon a stop event the PWM output 'line_out' is driven as a fixed '0' and the PWM output 'line_compl_out' is driven as a fixed '1'. |
| | H | | | 3 | When the counter is disabled the PWM outputs 'line_out' and 'line_compl_out' are driven by the TCPWM.<br>When the counter is disabled or stopped upon a stop event the PWM output 'line_out' is driven as a fixed '1' and the PWM output 'line_compl_out' is driven as a fixed '0'. |
| 16:17 | UP_DOWN_MODE | RW | R | 0 | Determines counter direction.<br><br>In QUAD mode this field acts as QUAD_RANGE_MODE field selecting between different counter range, reload value and compare / capture behavior. |
| | COUNT_UP | | | 0 | Count up (to PERIOD). An overflow event is generated when the counter changes from a state in which COUNTER equals PERIOD. A terminal count event is generated when the counter changes from a state in which COUNTER equals PERIOD. |
| | COUNT_DOWN | | | 1 | Count down (to '0'). An underflow event is generated when the counter changes from a state in which COUNTER equals '0'. A terminal count event is generated when the counter changes from a state in which COUNTER equals '0'. |
| | COUNT_UPDN1 | | | 2 | Count up (to PERIOD), then count down (to '0'). An overflow event is generated when the counter changes from a state in which COUNTER equals PERIOD. An underflow event is generated when the counter changes from a state in which COUNTER equals '0'. A terminal count event is generated when the counter changes from a state in which COUNTER equals '0'. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| | COUNT_UPDN2 | | | 3 | Count up (to PERIOD), then count down (to '0'). An overflow event is generated when the counter changes from a state in which COUNTER equals PERIOD. An underflow event is generated when the counter changes from a state in which COUNTER equals '0'. A terminal count event is generated when the counter changes from a state in which COUNTER equals '0' AND when the counter changes from a state in which COUNTER equals PERIOD (this counter direction can be used for PWM functionality with asymmetrical updates). |
| | QUAD_RANGE0 | | | 0 | In QUAD mode this setting selects the QUAD_RANGE0 mode with the following behavior:<br>- COUNTER range is between 0x0000 and 0xFFFF / 0xFFFFFFFF (for GRP_CNT_WIDTH = 16 / 32)<br>- on reload / index event:<br>- CC0 is copied to CC0_BUFF<br>- COUNTER is copied to CC0<br>- COUNTER is set to midpoint (0x8000 / 0x80000000)<br>- tc and cc0_match events are generated<br>- when COUNTER is 0x0000 or 0xFFFF / 0xFFFFFFFF:<br>- CC0 is copied to CC0_BUFF<br>- COUNTER (0x0000 or 0xFFFF / 0xFFFFFFFF) is copied to CC0<br>- COUNTER is set to midpoint (0x8000 / 0x80000000)<br>- cc0_match event is generated |
| | QUAD_RANGE0_CMP | | | 1 | In QUAD mode this setting selects the QUAD_RANGE0_CMP mode with the following behavior:<br>- COUNTER range is between 0x0000 and 0xFFFF / 0xFFFFFFFF (for GRP_CNT_WIDTH = 16 / 32)<br>- the capture0 event acts as 2nd reload / index event<br>- on reload / index event:<br>- COUNTER is set to midpoint (0x8000 / 0x80000000)<br>- when 'capture on index' is selected (AUTO_RELOAD_PERIOD=0):<br>- tc event is generated<br>- PERIOD is copied to PERIOD_BUFF<br>- COUNTER is copied to PERIOD<br>- when COUNTER is 0x0000 or 0xFFFF / 0xFFFFFFFF:<br>- COUNTER is set to midpoint (0x8000 / 0x80000000)<br>- when 'capture on wrap-around' is selected (AUTO_RELOAD_PERIOD=1):<br>- tc event is generated<br>- PERIOD is copied to PERIOD_BUFF<br>- COUNTER (0x0000 or 0xFFFF / 0xFFFFFFFF) is copied to PERIOD<br>- 1 or 2 compare functions (depending on CC1_PRESENT) available<br><br>This mode is to a certain extend backward compatible with previous TCPWM quadrature behavior but allows a compare function during quadrature decoding using the CC0/CC_BUFF registers and the cc0_match event. Because of that the PERIOD/PERIOD_BUFF registers are used instead of CC0/CC_BUFF registers to capture COUNTER at reload / index event or wrap-around. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| | QUAD_RANGE1_CAPT | | | 2 | In QUAD mode this setting selects the QUAD_RANGE1_CAPT mode with the following behavior:<br>- COUNTER range is between 0x0000 and PERIOD<br>- on reload / index event:<br>- COUNTER is set to 0x0000<br>- tc event is generated<br>- when COUNTER is 0x0000 and decrementing:<br>- COUNTER is set to PERIOD<br>- tc event is generated<br>- when COUNTER equals PERIOD and is incrementing:<br>- COUNTER is set to 0x0000<br>- tc event is generated<br>- 1 or 2 capture functions (depending on CC1_PRESENT) available<br>- on capture0 / capture1 event:<br>- CC0 / CC1 is copied to CC0_BUFF / CC1_BUFF<br>- COUNTER value is copied to CC0<br><br>It allows that the COUNTER register reflects the current angle position of the rotary encoder, i.e. no MOD or SUB calculations need to be done in SW on the COUNTER value to get the current angle position. This allows a DMA copy of the angle position from the COUNTER register. However, a disadvantage of this mode is that fast sequences of tc interrupts can occur (when encoder moves back and forth around start position). It is recommended to not use the tc interrupt in this mode. |
| | QUAD_RANGE1_CMP | | | 3 | In QUAD mode this setting selects the QUAD_RANGE1_CMP mode.<br>The behavior is the same as for QUAD_RANGE1_CAPT mode described above with the only difference that 1 or 2 compare functions (depending on CC1_PRESENT) are available instead of 1 or 2 capture functions. |
| 18 | ONE_SHOT | RW | R | 0 | When '0', counter runs continuous. When '1', counter is turned off by hardware when a terminal count event is generated. |
| 20:21 | QUAD_ENCODING_MODE | RW | R | 0 | In QUAD mode this field selects the quadrature encoding mode (X1/X2/X4) or the Up / Down rotary counting mode.<br>In PWM, PWM_DT and PWM_PR modes, these two bits can be used to invert 'dt_line_out' and 'dt_line_compl_out'. Inversion is the last step in generation of 'dt_line_out' and 'dt_line_compl_out'; i.e. a disabled output line 'dt_line_out' has the value QUAD_ENCODING_MODE[0] and a disabled output line 'dt_line_compl_out' has the value QUAD_ENCODING_MODE[1]. |
| | X1 | | | 0 | X1 encoding (QUAD mode)<br>This encoding is identical with an up / down counting functionality of the following way: Rising edges of input phiA increment or decrement the counter depending on the state of input phiB (direction input). |
| | X2 | | | 1 | X2 encoding (QUAD mode) |
| | X4 | | | 2 | X4 encoding (QUAD mode) |
| | UP_DOWN | | | 3 | Up / Down rotary counting mode. Input phiA increments the counter, input phiB decrements the counter. The trigger edge detection settings apply. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| | INV_OUT | | | 1 | When bit 0 is '1', QUADRATURE_ENCODING_MODE[0] inverts 'dt_line_out' (PWM/PWM_DT modes) |
| | INV_COMPL_OUT | | | 2 | When bit 1 is '1', QUADRATURE_ENCODING_MODE[1] inverts 'dt_line_compl_out' (PWM/PWM_DT modes) |
| 24:26 | MODE | RW | R | 0 | Counter mode. |
| | TIMER | | | 0 | Timer mode |
| | Reserved1 | | | 1 | N/A |
| | CAPTURE | | | 2 | Capture mode |
| | QUAD | | | 3 | Quadrature mode<br><br>Different encoding modes can be selected by QUAD_ENCODING_MODE including up/down count functionality.<br>Different counter range, reload value and capture behavior can be selected by QUAD_RANGE_MODE (overloaded field UP_DOWN_MODE). |
| | PWM | | | 4 | Pulse width modulation (PWM) mode |
| | PWM_DT | | | 5 | PWM with deadtime insertion mode |
| | PWM_PR | | | 6 | Pseudo random pulse width modulation |
| | SR | | | 7 | Shift register mode. |
| 30 | DBG_FREEZE_EN | RW | R | 0 | Specifies the counter behavior in debug mode.<br>'0': The counter operation continues in debug mode.<br>'1': The counter operation freezes in debug mode. |
| 31 | ENABLED | RW | R | 0 | Counter enable.<br>'0': counter disabled.<br>'1': counter enabled.<br>Counter static configuration information (e.g. CTRL.MODE, all TR_IN_SEL, TR_IN_EDGE_SEL, TR_PWM_CTRL and TR_OUT_SEL register fields) should only be modified when the counter is disabled.<br>When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes:<br>- the associated counter triggers in the CMD register are set to '0'.<br>- the counter's interrupt cause fields in counter's INTR register.<br>- the counter's status fields in counter's STATUS register..<br>- the counter's trigger outputs ('tr_out0' and tr_out1').<br>- the counter's line outputs ('line_out' and 'line_compl_out'). |

#### 33.3.1.1.2 TCPWM_GRP_CNT_STATUS

**Description:** Counter status register
**Address:** 0x40380004
**Offset:** 0x4
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** When the counter is disabled (CTRL.ENABLED = 0), then the STATUS.TR_* bit fields are typically reset to their default values. However, there are exceptions possible in the following cases, based on the selected input trigger via TR_IN_SEL*.*_SEL:
- If a constant '0' is selected, then a '0' is read.
- If a constant '1' is selected, then a '1' is read.
- If a general purpose trigger input 'tr_all_cnt_in' is selected which is also selected by another counter and that counter is enabled, then the actual level of the selected trigger is read.

**Default:** 0x20

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | TR_STOP [7:7] | TR _RELOAD [6:6] | TR_COUNT [5:5] | TR _CAPTUR E0 [4:4] | None [3:1] | | | DOWN [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | RUNNING [15:15] | None [14:12] | | | LINE _COMPL _OUT [11:11] | LINE_OUT [10:10] | TR _CAPTUR E1 [9:9] | TR_START [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | DT_CNT_L [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | DT_CNT_H [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | DOWN | R | RW | 0 | When '0', counter is counting up. When '1', counter is counting down. In QUAD mode, this field indicates the direction of the latest counter change: '0' when last incremented and '1' when last decremented. |
| 4 | TR_CAPTURE0 | R | RW | 0 | Indicates the actual level of the selected capture 0 trigger. |
| 5 | TR_COUNT | R | RW | 1 | Indicates the actual level of the selected count trigger. |
| 6 | TR_RELOAD | R | RW | 0 | Indicates the actual level of the selected reload trigger. |
| 7 | TR_STOP | R | RW | 0 | Indicates the actual level of the selected stop trigger. |
| 8 | TR_START | R | RW | 0 | Indicates the actual level of the selected start trigger. |
| 9 | TR_CAPTURE1 | R | RW | 0 | Indicates the actual level of the selected capture 1 trigger. |
| 10 | LINE_OUT | R | RW | 0 | Indicates the actual level of the PWM line output signal. |
| 11 | LINE_COMPL_OUT | R | RW | 0 | Indicates the actual level of the complementary PWM line output signal. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 15 | RUNNING | R | RW | 0 | When '0', the counter is NOT running. When '1', the counter is running.<br><br>This field is used to indicate that the counter is running after a start/reload event and that the counter is stopped after a stop event.<br>When a running counter operation is paused in debug state (see CTRL.DBG_PAUSE) then the RUNNING bit is still '1'. |
| 16:23 | DT_CNT_L | R | RW | 0 | Generic 8-bit counter field. In PWM_DT mode, this counter is used for dead time insertion (8bit dead time counter or low byte of 16-bit dead time counter).<br>In all other modes, this counter is used for pre-scaling the selected counter clock. PWM_DT mode can NOT use prescaled clock functionality. |
| 24:31 | DT_CNT_H | R | RW | 0 | High byte of 16-bit dead time counter. In PWM_DT mode, this counter is used for dead time insertion.<br>In all other modes, this field has no effect.<br><br>Note: This field only exists when parameter GRP_AMC_PRESENT for advanced motor control is set to 1. Otherwise the dead time is only 8bit wide and the only the field DT_CNT_L is used as dead time counter. |

#### 33.3.1.1.3 TCPWM_GRP_CNT_COUNTER

**Description:** Counter count register
**Address:** 0x40380008
**Offset:** 0x8
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNTER [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | COUNTER [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | COUNTER | RW | RW | 0 | 16-bit / 32-bit counter value. It is advised to not write to this field when the counter is running. |

#### 33.3.1.1.4 TCPWM_GRP_CNT_CC0

**Description:** Counter compare/capture 0 register
**Address:** 0x40380010
**Offset:** 0x10
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xFFFFFFFF

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | CC [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | CC [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | CC | RW | RW | 65535 | In CAPTURE mode, captures the counter value. In other modes, compared to counter value. |

#### 33.3.1.1.5 TCPWM_GRP_CNT_CC0_BUFF

**Description:** Counter buffered compare/capture 0 register
**Address:** 0x40380014
**Offset:** 0x14
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xFFFFFFFF

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | CC [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | CC [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | CC | RW | RW | 65535 | Additional buffer for counter CC register. |

#### 33.3.1.1.6 TCPWM_GRP_CNT_CC1

**Description:** Counter compare/capture 1 register
**Address:** 0x40380018
**Offset:** 0x18
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xFFFFFFFF

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | CC [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | CC [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | CC | RW | RW | 65535 | In CAPTURE mode, captures the counter value. In other modes, compared to counter value. |

#### 33.3.1.1.7 TCPWM_GRP_CNT_CC1_BUFF

**Description:** Counter buffered compare/capture 1 register
**Address:** 0x4038001C
**Offset:** 0x1C
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xFFFFFFFF

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | CC [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | CC [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | CC | RW | RW | 65535 | Additional buffer for counter CC1 register. |

#### 33.3.1.1.8 TCPWM_GRP_CNT_PERIOD

**Description:** Counter period register
**Address:** 0x40380020
**Offset:** 0x20
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xFFFFFFFF

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | PERIOD [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | PERIOD [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | PERIOD | RW | RW | 65535 | Period value: upper value of the counter. When the counter should count for n cycles, this field should be set to n-1. |

#### 33.3.1.1.9 TCPWM_GRP_CNT_PERIOD_BUFF

**Description:** Counter buffered period register
**Address:** 0x40380024
**Offset:** 0x24
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0xFFFFFFFF

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | PERIOD [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | PERIOD [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:15 | PERIOD | RW | RW | 65535 | Additional buffer for counter PERIOD register.<br><br>In PWM_PR mode PEROD_BUFF defines the LFSR polynomial. Each bit represents a tap of the shift register which can be feed back to the MSB via an XOR tree.<br>Examples for GRP_CNT_WIDTH = 16:<br>- Maximum length 16bit LFSR<br>- polynomial x^16 + x^14 + x^13 + x^11 + 1<br>- taps 0,2,3,5 -> PERIOD = 0x002d<br>- period is 2^16-1 = 65535 cycles<br>- Maximum length 8bit LFSR:<br>- polynomial x^8 + x^6 + x^5 + x^4 + 1<br>- taps 8,10,11,12 (realized in 8 MSBs of 16bit LFSR)<br>- period is 2^8-1 = 255 cycles<br><br>In SR mode PERIOD_BUFF defines which tap of the shift register generates the PWM output signals. For a delay of n cycles (from capture event to PWM output) the bit CNT_WIDTH-n should be set to '1'. For a shift register function only one tap should be use, i.e. a one-hot value must be written to PERIOD_BUFF. If multiple bits in PERIOD_BUFF are set then the taps are XOR combined. |

### 33.3.1.1.10 TCPWM_GRP_CNT_LINE_SEL

**Description:** Counter line selection register
**Address:** 0x40380028
**Offset:** 0x28
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x32

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:7] | COMPL_OUT_SEL [6:4] | | | None [3:3] | OUT_SEL [2:0] | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:2 | OUT_SEL | RW | RW | 2 | Selects the source for the output signal 'line_out'. Default setting is the PWM signal 'line'. Other settings are useful for Stepper Motor Control.<br>This field has a function in PWM and PWM_PR modes only.<br><br>Note: The output signal of this selection can be further modified by the stop / kill logic and line_out polarity setting (CTRL.QUAD_ENCODING_MODE[0]). |
| | L | | | 0 | fixed '0' |
| | H | | | 1 | fixed '1' |
| | PWM | | | 2 | PWM signal 'line' |
| | PWM_INV | | | 3 | inverted PWM signal 'line' |
| | Z | | | 4 | The output 'line_out' is not driven by the TCPWM. Instead the port default level configuration applies, e.g. 'Z' (high impedance).<br><br>Note: This is realized by driving the output 'line_out_en' to 0. |
| | Reserved5 | | | 5 | N/A |
| | Reserved6 | | | 6 | N/A |
| | Reserved7 | | | 7 | N/A |
| 4:6 | COMPL_OUT_SEL | RW | RW | 3 | Selects the source for the output signal 'line_compl_out'. Default setting is the inverted PWM signal 'line'. Other settings are useful for Stepper Motor Control.<br>This field has a function in PWM and PWM_PR modes only.<br><br>Note: The output signal of this selection can be further modified by the stop / kill logic and line_compl_out polarity setting (CTRL.QUAD_ENCODING_MODE[1]). |
| | L | | | 0 | fixed '0' |
| | H | | | 1 | fixed '1' |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| | PWM | | | 2 | PWM signal 'line' |
| | PWM_INV | | | 3 | inverted PWM signal 'line' |
| | Z | | | 4 | The output 'line_compl_out' is not driven by the TCPWM. Instead the port default level configuration applies, e.g. 'Z' (high impedance).<br><br>Note: This is realized by driving the output 'line_compl_out_en' to 0. |
| | Reserved5 | | | 5 | N/A |
| | Reserved6 | | | 6 | N/A |
| | Reserved7 | | | 7 | N/A |

### 33.3.1.1.11 TCPWM_GRP_CNT_LINE_SEL_BUFF

**Description:** Counter buffered line selection register
**Address:** 0x4038002C
**Offset:** 0x2C
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x32

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:7] | COMPL_OUT_SEL [6:4] | | | None [3:3] | OUT_SEL [2:0] | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:2 | OUT_SEL | RW | RW | 2 | Buffer for LINE_SEL.OUT_SEL.<br>Can be exchanged with LINE_SEL.LINE_OUT_SEL on a terminal count event with an actively pending switch event.<br><br>This field has a function in PWM and PWM_PR modes only. |
| 4:6 | COMPL_OUT_SEL | RW | RW | 3 | Buffer for LINE_SEL.COMPL.OUT_SEL.<br>Can be exchanged with LINE_SEL.LINE_COMPL_OUT_SEL on a terminal count event with an actively pending switch event.<br><br>This field has a function in PWM and PWM_PR modes only. |

#### 33.3.1.1.12 TCPWM_GRP_CNT_DT

**Description:** Counter PWM dead time register
**Address:** 0x40380030
**Offset:** 0x30
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DT_LINE_OUT_L [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | DT_LINE_OUT_H [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | DT_LINE_COMPL_OUT [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | DT_LINE_COMPL_OUT [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:7 | DT_LINE_OUT_L | RW | R | 0 | In PWM_DT mode, this field is used to determine the low byte of the dead time before activating the PWM line output signal 'line_out': amount of dead time cycles in the counter clock domain.<br>In all other modes, the lower 3 bits of this field determine pre-scaling of the selected counter clock.<br><br>Note: This field determines the low byte of the 16-bit dead time before activating 'line_out' when parameter GRP_AMC_PRESENT for advanced motor control is set to 1. Otherwise the dead time is only 8 bit wide and the same dead time specified by this DT_LINE_OUT_L field is used before activating 'line_out' and 'line_compl_out'. |
| | DIVBY1 | | | 0 | Divide by 1 (other-than-PWM_DT mode) |
| | DIVBY2 | | | 1 | Divide by 2 (other-than-PWM_DT mode) |
| | DIVBY4 | | | 2 | Divide by 4 (other-than-PWM_DT mode) |
| | DIVBY8 | | | 3 | Divide by 8 (other-than-PWM_DT mode) |
| | DIVBY16 | | | 4 | Divide by 16 (other-than-PWM_DT mode) |
| | DIVBY32 | | | 5 | Divide by 32 (other-than-PWM_DT mode) |
| | DIVBY64 | | | 6 | Divide by 64 (other-than-PWM_DT mode) |
| | DIVBY128 | | | 7 | Divide by 128 (other-than-PWM_DT mode) |
| 8:15 | DT_LINE_OUT_H | RW | R | 0 | In PWM_DT mode, this field is used to determine the high byte of the dead time before activating the PWM line output signal 'line_out': amount of dead time cycles in the counter clock domain.<br>In all other modes, this field has no effect.<br><br>Note: This field only exists when parameter GRP_AMC_PRESENT for advanced motor control is set to 1. Otherwise the dead time is only 8 bit wide and the same dead time specified by field DT_LINE_OUT_L is used before activating 'line_out' and 'line_compl_out'. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 16:31 | DT_LINE_COMPL_OUT | RW | R | 0 | In PWM_DT mode, this field is used to determine the dead time before activating the complementary PWM line output signal 'line_compl_out': amount of dead time cycles in the counter clock domain.<br>In all other modes, this field has no effect.<br><br>Note: This field only exists when parameter GRP_AMC_PRESENT for advanced motor control is set to 1. Otherwise the dead time is only 8 bit wide and the same dead time specified by field DT_LINE_OUT_L is used before activating 'line_out' and 'line_compl_out'. |

#### 33.3.1.1.13 TCPWM_GRP_CNT_TR_CMD

**Description:** Counter trigger command register
**Address:** 0x40380040
**Offset:** 0x40
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** Enables software controlled operation for this counter.
Note: Synchronized operation on multiple counters can be done using trigger multipliers.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:6] | | CAPTURE1 [5:5] | START [4:4] | STOP [3:3] | RELOAD [2:2] | None [1:1] | CAPTURE0 [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | CAPTURE0 | RW1S | RW1C | 0 | SW capture 0 trigger. When written with '1', a capture 0 trigger is generated and the HW sets the field to '0' when the SW trigger has taken effect. It should be noted that the HW operates on the counter frequency. If the counter is disabled through CTRL.ENABLED, the field is immediately set to '0'. |
| 2 | RELOAD | RW1S | RW1C | 0 | SW reload trigger. For HW behavior, see COUNTER_CAPTURE0 field. |
| 3 | STOP | RW1S | RW1C | 0 | SW stop trigger. For HW behavior, see COUNTER_CAPTURE0 field. |
| 4 | START | RW1S | RW1C | 0 | SW start trigger. For HW behavior, see COUNTER_CAPTURE0 field. |
| 5 | CAPTURE1 | RW1S | RW1C | 0 | SW capture 1 trigger. For HW behavior, see COUNTER_CAPTURE0 field. |

### 33.3.1.1.14 TCPWM_GRP_CNT_TR_IN_SEL0

**Description:** Counter input trigger selection register 0
**Address:** 0x40380044
**Offset:** 0x44
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Used to select triggers for specific counter events.
**Default:** 0x100

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:5] | | | CAPTURE0_SEL [4:0] | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:13] | | | COUNT_SEL [12:8] | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:21] | | | RELOAD_SEL [20:16] | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:29] | | | STOP_SEL [28:24] | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:4 | CAPTURE0_SEL | RW | R | 0 | Selects one of the up to 256 input triggers as a capture0 trigger. Input trigger 0 is always '0' and input trigger 1 is always '1'. If existing, the one-to-one trigger inputs 'tr_one_cnt_in' (different to each counter) are selected by setting 2 and above. The settings above are used for the general purpose trigger inputs 'tr_all_cnt_in' connected to all counters selected.<br>In the PWM, PWM_DT and PWM_PR modes this trigger is used to switch the values if the compare and period registers with their buffer counterparts. |
| 8:12 | COUNT_SEL | RW | R | 1 | Selects one of the 256 input triggers as a count trigger.<br><br>In QUAD mode, this is the first phase (phi A). Default setting selects input trigger 1, which is always '1'.<br><br>Note: In the modes: TIMER, CAPTURE, PWM, PWM_DT, and SR, If the counter is externally triggered ( COUNT_SEL > 1), an external trigger will be required for each TR_CMD to execute. For example, a write to TR_CMD.START will not start the counter until the trigger selected by COUNT_SEL asserts. The next trigger will increment the counter since the counter is now running. This goes for all TR_CMD fields. |
| 16:20 | RELOAD_SEL | RW | R | 0 | Selects one of the 256 input triggers as a reload trigger.<br>In QUAD mode, this is the index or revolution pulse. In these modes, it will update the counter with 0x8000 (counter midpoint) or 0x0000 depending on the QUAD_RANGE_MODE. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 24:28 | STOP_SEL | RW | R | 0 | Selects one of the 256 input triggers as a stop trigger. In PWM, PWM_DT and PWM_PR modes, this is the kill trigger. In these modes, the kill trigger is used to either temporarily block the PWM outputs (PWM_STOP_ON_KILL is '0') or stop the functionality (PWM_STOP_ON_KILL is '1'). For the PWM and PWM_DT modes, the blocking of the output signals can be asynchronous (STOP_EDGE should be NO_EDGE_DET) in which case the blocking is as long as the trigger is '1' or synchronous (STOP_EDGE should be RISING_EDGE) in which case it extends till the next terminal count event. |

### 33.3.1.1.15 TCPWM_GRP_CNT_TR_IN_SEL1

**Description:** Counter input trigger selection register 1
**Address:** 0x40380048
**Offset:** 0x48
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Used to select triggers for specific counter events.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:5] | | | START_SEL [4:0] | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:13] | | | CAPTURE1_SEL [12:8] | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:4 | START_SEL | RW | R | 0 | Selects one of the 256 input triggers as a start trigger. In QUAD mode, this is the second phase (phi B). |
| 8:12 | CAPTURE1_SEL | RW | R | 0 | Selects one of the 256 input triggers as a capture 1 trigger. |

### 33.3.1.1.16 TCPWM_GRP_CNT_TR_IN_EDGE_SEL

**Description:** Counter input trigger edge selection register
**Address:** 0x4038004C
**Offset:** 0x4C
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Used to determine edge detection for specific counter triggers. Events will only take effect on enabled counters.
**Default:** 0xFFF

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | STOP_EDGE [7:6] | | RELOAD_EDGE [5:4] | | COUNT_EDGE [3:2] | | CAPTURE0_EDGE [1:0] | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:12] | | | | CAPTURE1_EDGE [11:10] | | START_EDGE [9:8] | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:1 | CAPTURE0_EDGE | RW | R | 3 | A capture 0 event will copy the counter value into the CC0 register. |
| | RISING_EDGE | | | 0 | Rising edge. Any rising edge generates an event. |
| | FALLING_EDGE | | | 1 | Falling edge. Any falling edge generates an event. |
| | ANY_EDGE | | | 2 | Rising AND falling edge. Any odd amount of edges generates an event. |
| | NO_EDGE_DET | | | 3 | No edge detection, use trigger as is. |
| 2:3 | COUNT_EDGE | RW | R | 3 | A counter event will increase or decrease the counter by '1'. |
| | RISING_EDGE | | | 0 | Rising edge. Any rising edge generates an event. |
| | FALLING_EDGE | | | 1 | Falling edge. Any falling edge generates an event. |
| | ANY_EDGE | | | 2 | Rising AND falling edge. Any odd amount of edges generates an event. |
| | NO_EDGE_DET | | | 3 | No edge detection, use trigger as is. |
| 4:5 | RELOAD_EDGE | RW | R | 3 | A reload event will initialize the counter. When counting up, the counter is initialized to '0'. When counting down, the counter is initialized with PERIOD. |
| | RISING_EDGE | | | 0 | Rising edge. Any rising edge generates an event. |
| | FALLING_EDGE | | | 1 | Falling edge. Any falling edge generates an event. |
| | ANY_EDGE | | | 2 | Rising AND falling edge. Any odd amount of edges generates an event. |
| | NO_EDGE_DET | | | 3 | No edge detection, use trigger as is. |
| 6:7 | STOP_EDGE | RW | R | 3 | A stop event, will stop the counter; i.e. it will no longer be running. Stopping will NOT disable the counter. |
| | RISING_EDGE | | | 0 | Rising edge. Any rising edge generates an event. |
| | FALLING_EDGE | | | 1 | Falling edge. Any falling edge generates an event. |
| | ANY_EDGE | | | 2 | Rising AND falling edge. Any odd amount of edges generates an event. |
| | NO_EDGE_DET | | | 3 | No edge detection, use trigger as is. |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 8:9 | START_EDGE | RW | R | 3 | A start event will start the counter; i.e. the counter will become running. Starting does NOT enable the counter. A start event will not initialize the counter whereas the reload event does. |
| | RISING_EDGE | | | 0 | Rising edge. Any rising edge generates an event. |
| | FALLING_EDGE | | | 1 | Falling edge. Any falling edge generates an event. |
| | ANY_EDGE | | | 2 | Rising AND falling edge. Any odd amount of edges generates an event. |
| | NO_EDGE_DET | | | 3 | No edge detection, use trigger as is. |
| 10:11 | CAPTURE1_EDGE | RW | R | 3 | A capture 1 event will copy the counter value into the CC1 register. |
| | RISING_EDGE | | | 0 | Rising edge. Any rising edge generates an event. |
| | FALLING_EDGE | | | 1 | Falling edge. Any falling edge generates an event. |
| | ANY_EDGE | | | 2 | Rising AND falling edge. Any odd amount of edges generates an event. |
| | NO_EDGE_DET | | | 3 | No edge detection, use trigger as is. |

### 33.3.1.1.17 TCPWM_GRP_CNT_TR_PWM_CTRL

**Description:** Counter trigger PWM control register
**Address:** 0x40380050
**Offset:** 0x50
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Used to control counter 'line_out', 'dt_line_out' and 'dt_line_compl_out' output signals.
**Default:** 0xFF

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | CC1_MATCH_MODE [7:6] | | UNDERFLOW_MODE [5:4] | | OVERFLOW_MODE [3:2] | | CC0_MATCH_MODE [1:0] | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:1 | CC0_MATCH_MODE | RW | R | 3 | Determines the effect of a compare match 0 event (COUNTER equals CC0 register) on the 'line_out' output signals. Note that INVERT is especially useful for center aligned pulse width modulation.<br>To generate a duty cycle of 0 percent, the counter CC0 register should be set to '0'. For a 100 percent duty cycle, the counter CC0 register should be set to larger than the counter PERIOD register. |
| | SET | | | 0 | Set to '1' |
| | CLEAR | | | 1 | Set to '0' |
| | INVERT | | | 2 | Invert |
| | NO_CHANGE | | | 3 | No Change |
| 2:3 | OVERFLOW_MODE | RW | R | 3 | Determines the effect of a counter overflow event (COUNTER reaches PERIOD) on the 'line_out' output signals. |
| | SET | | | 0 | Set to '1' |
| | CLEAR | | | 1 | Set to '0' |
| | INVERT | | | 2 | Invert |
| | NO_CHANGE | | | 3 | No Change |
| 4:5 | UNDERFLOW_MODE | RW | R | 3 | Determines the effect of a counter underflow event (COUNTER reaches '0') on the 'line_out' output signals. |
| | SET | | | 0 | Set to '1' |
| | CLEAR | | | 1 | Set to '0' |
| | INVERT | | | 2 | Invert |
| | NO_CHANGE | | | 3 | No Change |
| 6:7 | CC1_MATCH_MODE | RW | R | 3 | Determines the effect of a compare match 1 event (COUNTER equals CC1 register) on the 'line_out' output signals. |
| | SET | | | 0 | Set to '1' |
| | CLEAR | | | 1 | Set to '0' |
| | INVERT | | | 2 | Invert |

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| | NO_CHANGE | | | 3 | No Change |

### 33.3.1.1.18 TCPWM_GRP_CNT_TR_OUT_SEL

**Description:** Counter output trigger selection register
**Address:** 0x40380054
**Offset:** 0x54
**Retention:** Retained
**IsDeepSleep:** No
**Comment:** Used to select internal events for output trigger generation.
**Default:** 0x32

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:7] | OUT1 [6:4] | | | None [3:3] | OUT0 [2:0] | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0:2 | OUT0 | RW | R | 2 | Selects one of the internal events to generate the output trigger 0. Default setting selects the terminal count event. |
| | OVERFLOW | | | 0 | Overflow event |
| | UNDERFLOW | | | 1 | Underflow event |
| | TC | | | 2 | Terminal count event (default selection) |
| | CC0_MATCH | | | 3 | Compare match 0 event |
| | CC1_MATCH | | | 4 | Compare match 1 event |
| | LINE_OUT | | | 5 | PWM output signal 'line_out' |
| | Reserved6 | | | 6 | N/A |
| | Disabled | | | 7 | Output trigger disabled. |
| 4:6 | OUT1 | RW | R | 3 | Selects one of the internal events to generate the output trigger 1. Default setting selects the compare match 0 event. |
| | OVERFLOW | | | 0 | Overflow event |
| | UNDERFLOW | | | 1 | Underflow event |
| | TC | | | 2 | Terminal count event |
| | CC0_MATCH | | | 3 | Compare match 0 event (default selection) |
| | CC1_MATCH | | | 4 | Compare match 1 event |
| | LINE_OUT | | | 5 | PWM output signal 'line_out' |
| | Reserved6 | | | 6 | N/A |
| | Disabled | | | 7 | Output trigger disabled. |

#### 33.3.1.1.19 TCPWM_GRP_CNT_INTR

**Description:** Interrupt request register
**Address:** 0x40380070
**Offset:** 0x70
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** The register fields are not retained. This is to ensure that they come up as '0' after coming out of DeepSleep system power mode. HW clears the interrupt causes to '0', when the counter is disabled.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:3] | | | | | CC1 _MATCH [2:2] | CC0 _MATCH [1:1] | TC [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | TC | RW1C | RW1S | 0 | Terminal count event. Set to '1', when event is detected. Write with '1' to clear bit. |
| 1 | CC0_MATCH | RW1C | RW1S | 0 | Counter matches CC0 register event. Set to '1', when event is detected. Write with '1' to clear bit. |
| 2 | CC1_MATCH | RW1C | RW1S | 0 | Counter matches CC1 register event. Set to '1', when event is detected. Write with '1' to clear bit. |

#### 33.3.1.1.20 TCPWM_GRP_CNT_INTR_SET

**Description:** Interrupt set request register
**Address:** 0x40380074
**Offset:** 0x74
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** When read, this register reflects the interrupt request register.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:3] | | | | | CC1 _MATCH [2:2] | CC0 _MATCH [1:1] | TC [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | TC | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt request register. |
| 1 | CC0_MATCH | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt request register. |
| 2 | CC1_MATCH | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt request register. |

#### 33.3.1.1.21 TCPWM_GRP_CNT_INTR_MASK

**Description:** Interrupt mask register
**Address:** 0x40380078
**Offset:** 0x78
**Retention:** Retained
**IsDeepSleep:** No
**Comment:**
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:3] | | | | | CC1 _MATCH [2:2] | CC0 _MATCH [1:1] | TC [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | TC | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |
| 1 | CC0_MATCH | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |
| 2 | CC1_MATCH | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |

#### 33.3.1.1.22 TCPWM_GRP_CNT_INTR_MASKED

**Description:** Interrupt masked request register
**Address:** 0x4038007C
**Offset:** 0x7C
**Retention:** Not Retained
**IsDeepSleep:** No
**Comment:** When read, this register reflects a bitwise AND between the interrupt request and mask registers.
**Default:** 0x0

**Bit-field Table**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | None [7:3] | | | | | CC1 _MATCH [2:2] | CC0 _MATCH [1:1] | TC [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Name | None [31:24] | | | | | | | |

**Bit-fields**

| Bits | Name | SW | HW | Default or Enum | Description |
|---|---|---|---|---|---|
| 0 | TC | R | W | 0 | Logical and of corresponding request and mask bits. |
| 1 | CC0_MATCH | R | W | 0 | Logical and of corresponding request and mask bits. |
| 2 | CC1_MATCH | R | W | 0 | Logical and of corresponding request and mask bits. |

# References

[1] 002-24001: TRAVEO™ T2G body controller high MCU architecture reference manual.

# Revision history

| Document revision | Date | Description of changes |
|---|---|---|
| ** | 2018-07-25 | Specification for new silicon. |
| *A | 2018-09-26 | Minor issues fixed in generation of HTML. |
| *B | 2019-05-16 | Instance table is created for each IP and the Instance number is picked from the parameter section of the<br>XML.<br>Links are created for the REGISTER table with offset from the base.<br>All registers are displayed (same instance of the same IP).<br>All bit-fields per register are rendered based on parameterization<br>Logs captures the following three details:<br>a. IP and its respective instances<br>b. IP wise Hidden registers<br>c. IP wise Populated registers<br>Optimization of HTML:<br>a. Stable "File Header" which was earlier moving along with the contents<br>b. Color codes for the navigation pane<br>c. Links to the REGISTER definition from the register table |
| *C | 2019-09-17 | 1. All the instances of all the IPs are supported now.<br>2. Look and feel of the UI has been changed to make it more user friendly:<br>a. Distributed into 3 panes:<br>i. Sections<br>ii. Registers<br>iii. Content<br>b. Default page with right fragment opens up with the references, notes, and registers structure with respective links on the Contents pane.<br>c. Registers pane provide global search operation after feeding first 3 characters when ONLY at home.<br>d. On the Sections pane, user must select the **MMIO > IP > Instance** etc.<br>e. Registers pane provides Search options for the selected instance.<br>f. Once a particular instance is chosen, the Registers pane provides a list of registers. User can select one of these registers and observe the register structure on the Contents pane.<br>3. Instance table, register name and offsets have been removed, as they are no longer needed.<br>4. All hidden registers and sections are not visible (similar to earlier versions).<br>5. There is no PDF associated with HTML as earlier.<br>Known Issues:<br>1. There is no way to print any content as of now.<br>2. There could be a slight misalignment on the content pane based on the screen size. |

## Revision history

| Document revision | Date | Description of changes |
|---|---|---|
| *D | 2020-03-05 | 1. Extensive search options using address or register or bit fields.<br>Search option is supported for "Registers", register "Addresses" and register "Bit Fields" using prefixes "reg:" or "add:" or "bit:" respectively.<br>2. Buttons "Home", and "Up" included.<br>3. Register Structure with links, all homepage notes are moved down.<br>4. Some fixes which were present in the previous revision in spec system.<br>Missing contents due to parser errors (CDT#343334).<br>5. Print options for the selected registers.<br>6. HTML is supported only on Chrome, Mozilla Firefox, Opera, UC Browser and Microsoft Edge browsers.<br>(No support for any other OS/Mobiles etc.)<br>7. Issue of content overlap while re-sizing after "restore down" option is fixed.<br>Known Issues:<br>1. Whole HTML print option not available. |
| *E | 2020-08-07 | 1. Based on Rev_D of Silicon tape out.<br>2. SW Access note enhanced.<br>3. Added HW access note for registers behavior. |
| *F | 2020-09-23 | 1. ES100 Release.<br>2. Sflash additions.<br>3. eFuse corrections etc. |
| *G | 2021-10-01 | 1. Refer to Registers TRM difference log with respect to previous revision for details.<br>2. Addition of PASS/ADC registers for Temperature sensor control and trimming.<br>3. Sflash TOC2 updates for flash boot.<br>4. Minor description updates to some registers.<br>5. Addition of marker for security enhancement.<br>6. Removal of not needed registers. |
| *H | 2023-02-08 | 1. Register retentions flag updated where ever applicable.<br>2. Other errata fixes, updates and corrections. |
| *I | 2024-12-23 | • Register retentions flag updated wherever applicable.<br>• Other errata fixes, updates and corrections. |
| *J | 2026-08-28 | • New registers added<br>• Register retentions flag updated where ever applicable<br>• Other errata fixes, updates and corrections |

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Edition: 2026-08-28

Published by
Infineon Technologies AG
Am Campeon 1-15
85579 Neubiberg, Germany

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Document reference:
002-24402 Rev. *J

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