

Sl. No.	Section	Subsection	Change Description	Current Spec *G content	New Spec *H content	Reason for change	Customer Impact
1	6. Protection Unit	6.4.7 PPU 6.4.7.2 ECC Error Injection	Added Note	-	Note: Depending on the application and use case, there may be a need to protect ECC error injection from non-authorized use. For more details, contact Infineon support.	Improvement	None
2	7 Direct memory access	7.1.6.2 ECC for P-DMA channel configuration SRAMs	Added note	-	Note: Depending on the application and use case there may be a need to protect ECC error injection from nonauthorized use. For more details, contact Infineon support.	Add information	None
3	8 Code flash	8.2.2.5 Code flash ECC Error injection	Added Note	-	Note: Depending on the application and use case, there may be a need to protect ECC error injection from non-authorized use. For more details, contact Infineon support.	Improvement	None
4	8 Code flash	8.2.2.7 Cache ECC Error injection	Added Note	-	Note: Depending on the application and use case, there may be a need to protect ECC error injection from non-authorized use. For more details, contact Infineon support.	Improvement	None
5	8 Code flash	8.2.4.1 Dual bank mode and remap functionality Table 8-11	Added Note	-	Note: Access to any code flash banks (in both Single Bank mode and Dual Bank mode), while an SFLASH row is being written, can result in a BUS error.	Improvement	None
6	8 Code flash	8.3.1 SROM APIs	Updated description	To execute the SROM APIs, it is recommended to use the core M0+ through inter-processor communicatio	To execute the SROM APIs, it is necessary to use the core M0+ through inter-processor communicatio	Improvement	None
7	9 Work flash	9.2.2.2 Work flash ECC Work flash ECC	Added Note	-	Note: Depending on the application and use case, there may be a need to protect ECC error injection from non-authorized use. For more details, contact Infineon support.	Improvement	None
8	9 Work flash	9.3.2 SROM APIs	Updated description	To execute the SROM APIs, it is recommended to use the core M0+ through inter-processor communication.	To execute the SROM APIs, it is necessary to use the core M0+ through inter-processor communication.	Improvement	None
9	10 SRAM interface	-	Sentence change	SRAM controllers are implemented in the TRAVEO™ T2G family device for the on-chip SRAM memory interface. The SRAMs are accessible by CPUs. CPUs can also execute code out from these SRAMs.	SRAM controllers are implemented in the TRAVEO™ T2G family device for the on-chip SRAM memory interface. CPUs can access the SRAMs and can also execute code out of these SRAMs.	Description change	None
10	10 SRAM interface	10.3 ECC Details 10.3.3 ECC Error Injection	Added Note	-	Note: Depending on the application and use case, there may be a need to protect ECC error injection from non-authorized use. For more details, contact Infineon support.	Improvement	None
11	11. BootROM	11.3.4.5 Security Enhancement PPU Configuration in Sflash Table 11-3	Added TRAVEO T2G Cluster Entry	-	Added TRAVEO™ T2G Cluster Entry	Specification change	Middle
12	11. BootROM	11.3.4.5 Security Enhancement PPU Configuration in Sflash	Added Note	-	Note: Depending on the application and use case, there may be a need to protect ECC error injection from non-authorized use. For more details, contact Infineon support.	Improvement	None
13	11. BootROM	11.4.2 eFuse Bits Table 11-6	Changed description	Critical Object Hash FACTORY_HASH: SHA-256 SECURE_HASH: SHA-256 SECURE_HASH_ZEROES: SHA-256	Critical Object Hash FACTORY_HASH: SHAKE-128 SECURE_HASH: SHAKE-128 SECURE_HASH_ZEROES: SECURE_HASH	Fixing	None
14	19. Reset system	19.1.7 Internal system reset	Update	-	Note that you must write 0x5FA to the VECTKEY field at the same time you write to the SYSRESETREQ bit of the AIRCR registers; otherwise, the processor ignores the write.	Correction	None
15	20. Watchdog timer	20.3.1 Overview	Updated description	the counter increments to the 32-bit boundary and then wraps around to '0' and counts up.	the counter stops counting.	Updating	None
16	22.6 Digital Output Driver	Table 22-5	DS_TRM[2:0] 101 111 changed description	101: 40ohm, 1.8-V memory 111: 25ohm, 1.8-V memory	101: 40ohm, 3.3-V memory 111: 25ohm, 3.3-V memory	Correction	None
17	23. CAN FD Controller	24.4.8.4 ECC Error Injection	Added Note	-	Note: Depending on the application and use case, there may be a need to protect ECC error injection from non-authorized use. For more details, contact Infineon support.	Improvement	None
18	24. Serial Communications Block (SCB)	24.2.4 Clock and Reset Interface	Added clock relationship	-	CLK_PERI>=CLK_SYS(CLK_GR6)=CLK_AHB=CLK_SCB(PCLK_SCB_CLOCK)	Improvement	None
19	24. Serial Communications Block (SCB)	24.4.5.3 Oversampling and Bit Rate SPI Master Mode	Default value	Note: The SCBx_SPI_CTRL.LATE_MISO_SAMPLE is set to '0' by default.	Note: The SCBx_SPI_CTRL.LATE_MISO_SAMPLE is set to '1' by default.	correction	None
20	24. Serial Communications Block (SCB)	24.6.6.2 Oversampling and Bit Rate	Added description	-	"I2C Master Clock Synchronization" description	Improvement	None
21	25. Timer, Counter, and PWM	Table 25-2. Handling Input Trigger Multiplexers	Change and delete the Input Trigger	(Input Trigger Selection) (Input Trigger) 2 HSIOM column ACT#2 3 HSIOM column ACT#3 4 PASS (programmable analog subsystem), through 1:1 trigger mux #0,	(Input Trigger Selection) (Input Trigger) 2 HSIOM column TCx_y_TR0 / TCx_M_y_TR0 / TCx_H_y_TR0 3 HSIOM column TCx_y_TR1 / TCx_M_y_TR1 / TCx_H_y_TR1 4 PASS (programmable analog subsystem), through 1:1 trigger mux #x	Fixing	Yes

22	25. Timer, Counter, and PWM	Table 25-2. Handling Input Trigger Multiplexers	Change and delete the Input Trigger Source	<p>(Input Trigger Selection) 4 sheet tab</p> <p>(Input Trigger Source) Refer to the product "triggersOnetoOne". Not all counters will have this input trigger.</p> <p>Refer to the trigger mux 5 block.</p> <p>...</p> <p>31 block.</p> <p>Refer to the trigger mux</p>	<p>(Input Trigger Selection) 4 one-to-one" datasheet.</p> <p>(Input Trigger Source) Refer to the "Triggers" section in the device datasheet.</p> <p>Refer to the trigger mux 5 block in the device datasheet.</p> <p>...</p> <p>31 block in the device datasheet.</p> <p>Refer to the trigger mux</p>	Fixing	Yes
23	25. Timer, Counter, and PWM	Table 25-2. Handling Input Trigger Multiplexers	Change the note	The input triggers can be generated by different sources. While the general-purpose trigger inputs (tr_all_cnt_in[0] to tr_all_cnt_in[26]) are only from the trigger multiplexer block (see the Trigger Multiplexer chapter on page 503), the one-to-one input triggers can also be generated by external GPIO input pins.	The input triggers can be generated by different sources. While the general-purpose trigger inputs (tr_all_cnt_in[0] to tr_all_cnt_in[26]) are only from the trigger multiplexer block (see the Trigger Multiplexer chapter on page 583), the one-to-one input triggers can also be generated by external GPIO input pins.	Fixing	None
24	33. Nonvolatile Memory Programming	System Calls	Updated the note: specific system calls shall not be triggered during non blocking program/erase on Flash Bank0/Bank 1	Note only mentions about Bank 0 Note only mentions about ReadSWPU/WriteSWPU	Updated the note to also mention about Bank 1 Added other affected system calls	enhancement	Yes, Minor
25	33. Nonvolatile Memory Programming	List of system calls	Removed CM0+, CM4, DAP from the column Normal for system call TransitionToRMA	Support for the bus masters in Normal was mentioned for TransitionToRMA	Removed CM0+, CM4, DAP from the column Normal for TransitionToRMA	enhancement	None
26	34. Flash Boot	34.2.1.1 Cy_FB_VerifyApplication	Added note	-	Note: This function internally enables the power control of crypto engine and configure registers or memories needed to perform authentication of user application. Additionally, the function also disables the power control of crypto engine after an authentication is performed. This means existing configurations related to crypto (for example, configured by HSM software) is overwritten after calling this function and therefore must be handled again after every instance the function is called.	Fixing	None