**S72VS-R MCP**

# 256 Mb (16M x 16 bit), 1.8V Burst Mode Flash DDR DRAM on Split Bus

## Features

- Power supply voltage of 1.7V to 1.95V
- Burst Speeds
  - Flash = 83 MHz or 108 MHz
  - DDR DRAM = 166 MHz
- Packages
  - 8.0 × 8.0 mm, 133-ball MCP
- Operating Temperature
  - Wireless, –25 °C to +85 °C
  - Industrial, –40 °C to +85 °C

## General Description

This document contains information on the S72VS-R MCP stacked products. Refer to the S29VS/XS-R datasheet (002-00833) for full electrical specifications of the Flash memory component.

The S72VS Series is a product line of stacked products (MCPs), and consists of:

- S29VS family Address-Data Multiplexed Flash memory die
- DDR DRAM

The products covered by this document are listed in the below tables below.

| Flash Density | DRAM Density (256 Mb) |
|---|---|
| 256 Mb | S72VS256RE0 |

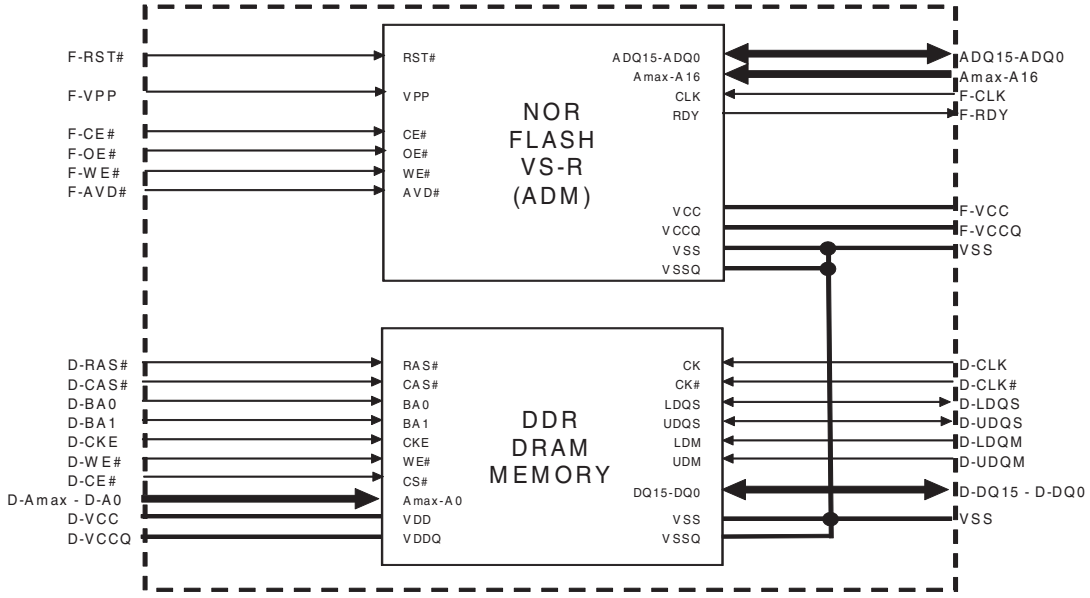
## DDR Specification Reference

| Density | Reference Name | Document Identification Number |
|---|---|---|
| 256 Mb | 256 Mb (16M x 16 bit) DDR DRAM | SDM256D166D1R/D3R |

## Electronic Serial Number

For applicable devices, the Factory Secured Silicon Area contains a random, 128-bit ESN, stored in the address range 000000h-000007h.

## Product Block Diagram

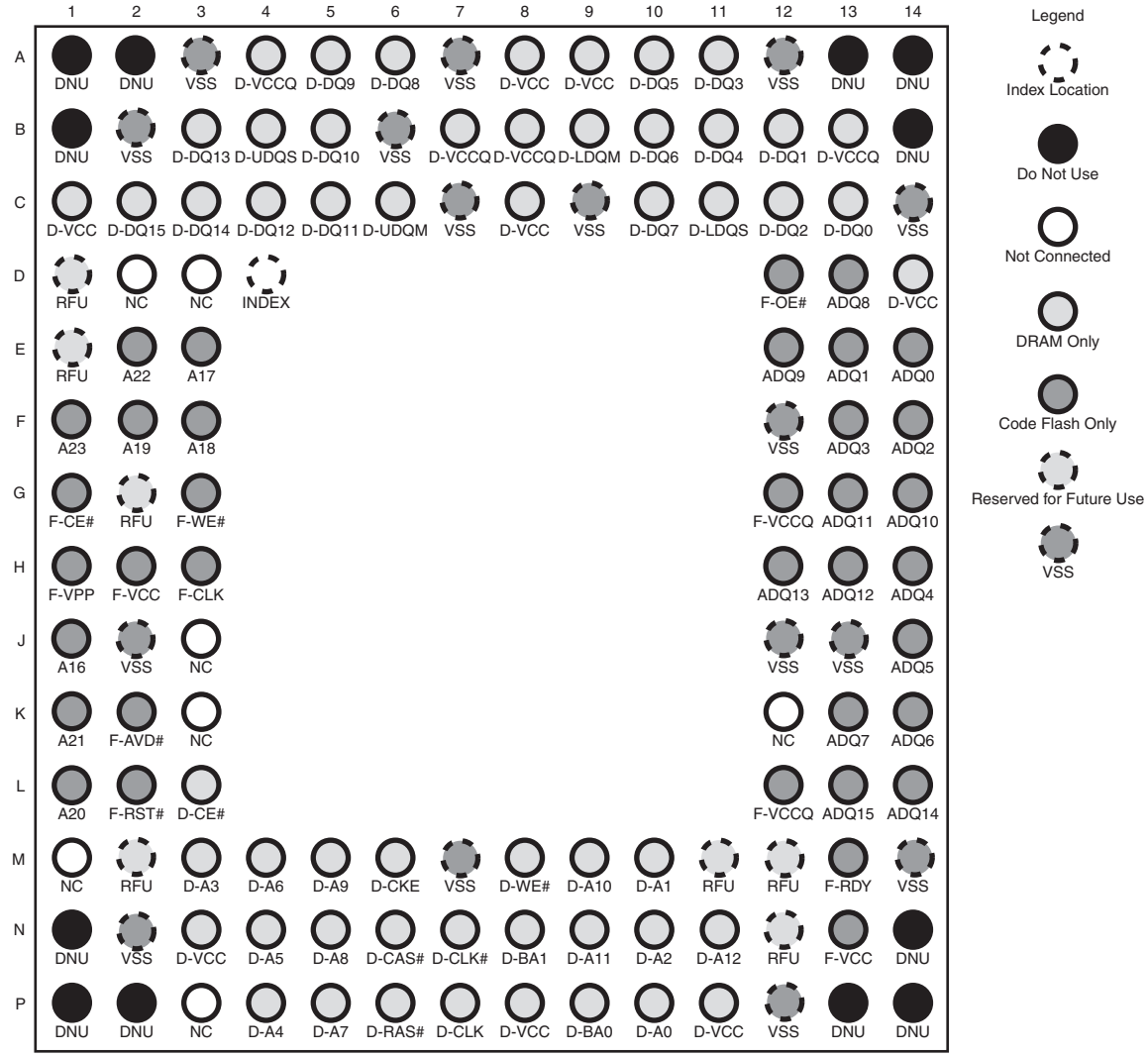



**Notes**

1. Amax indicates highest address bit for memory component:
   a. Amax = A23 for VS256R.
   b. Amax = A12 for 256 Mb DDR DRAM.

## Connection Diagrams

**Figure 1. 133-ball Fine-Pitch Ball Grid Array MCP**




| MCP | Flash Amax | DDR DRAM Density | D-Amax |
|---|---|---|---|
| S72VS256RE0 | A23 | 256 Mb | D-A12 |

## Input/Output Description

**Table 1. Input/Output Description**

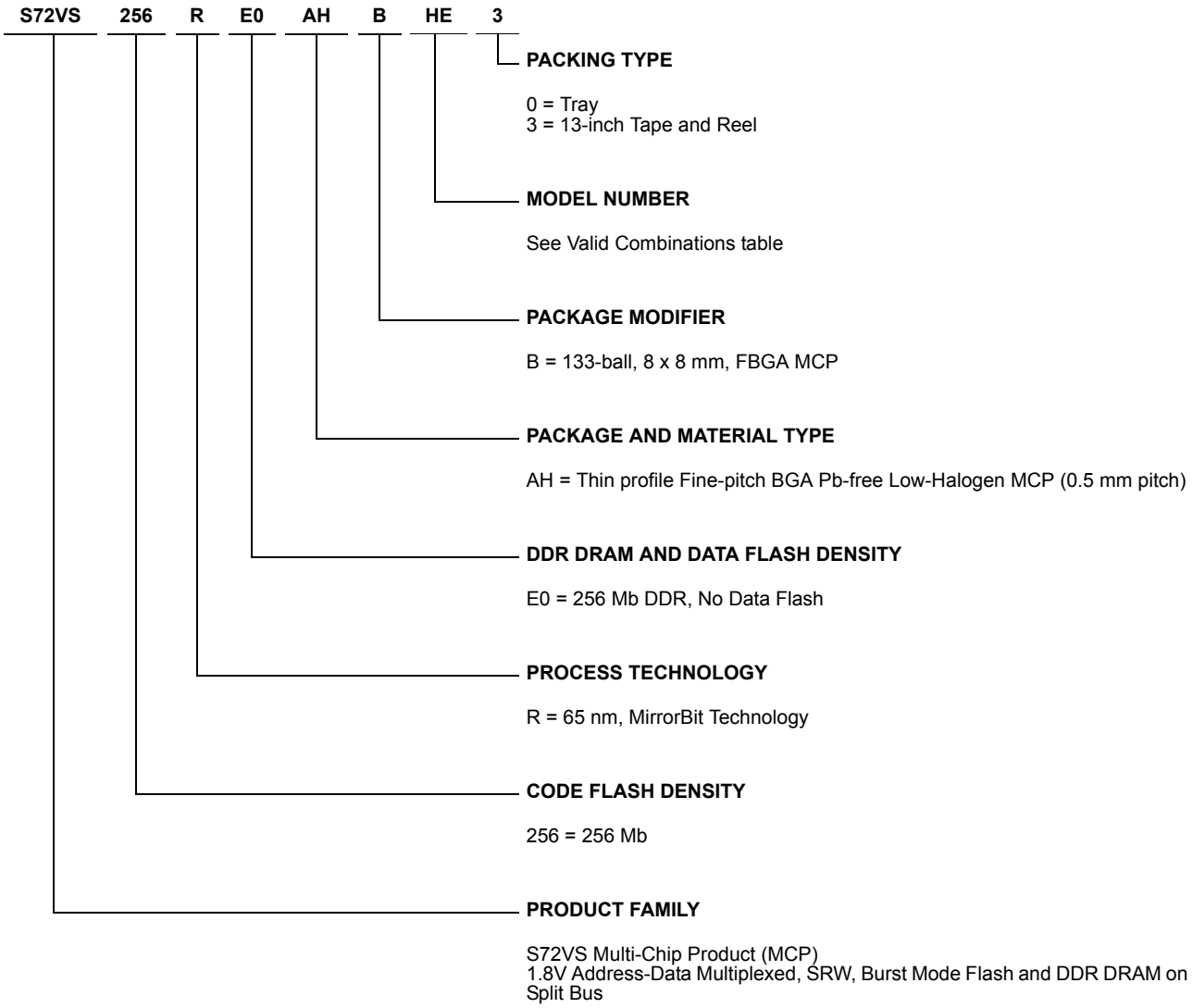
| Symbol | Description | Flash | RAM |
|---|---|---|---|
| Amax – A16 | Flash Address inputs | X | – |
| ADQ15 – ADQ0 | Flash multiplexed Address and Data | X | – |
| F-CE# | Flash Chip-enable input. | X | – |
| F-OE# | Flash Output Enable input. Asynchronous relative to CLK for Burst mode. | X | – |
| F-WE# | Flash Write Enable input | X | – |
| F-VCC | Flash device power supply (1.7 V to 1.95 V) | X | – |
| F-VCCQ | Flash Input/Output Buffer power supply | X | – |
| VSS | Ground | X | X |
| F-RDY | Flash ready output. Indicates the status of the Burst read. $V_{OL}$ = data invalid. $V_{OH}$ = data valid. | X | – |
| F-CLK | Flash Clock. The first rising edge of CLK in conjunction with AVD# low latches the address input and activates burst mode operation. After the initial word is output, subsequent rising edges of CLK increment the internal address counter. CLK should remain low during asynchronous access. | X | – |
| F-AVD# | Flash Address Valid input. Indicates to device that the valid address is present on the address inputs. $V_{IL}$ = for asynchronous mode, indicates valid address; for burst mode, causes starting address to be latched on rising edge of CLK. $V_{IH}$= device ignores address inputs | X | – |
| F-RST# | Flash hardware reset input. $V_{IL}$= device resets and returns to reading array data | X | – |
| F-VPP | Flash accelerated input. At $V_{HH}$, accelerates programming; automatically places device in unlock bypass mode. At $V_{IL}$, disables all program and erase functions. Should be at $V_{IH}$ for all other conditions. | X | – |
| D-Amax – D-A0 | DRAM Address inputs. | – | X |
| D-DQ15 – D-DQ0 | DRAM Data input/output | – | X |
| D-CLK | DRAM System Clock | – | X |
| D-CE# | DRAM Chip Select | – | X |
| D-CKE | DRAM Clock Enable | – | X |
| D-BA1 – BA0 | DRAM Bank Select | – | X |
| D-RAS# | DRAM Row Address Strobe | – | X |
| D-CAS# | DRAM Column Address Strobe | – | X |
| D-UDQM – D-LDQM | DRAM Data Input Mask | – | X |
| D-WE# | DRAM Write Enable input | – | X |
| D-VCCQ | DRAM Input/Output Buffer power supply | – | X |
| D-VCC | DRAM device power supply | – | X |
| D-UDQS | DRAM Upper Data Strobe, output with read data and input with write data | – | X |
| D-LDQS | DRAM Lower Data Strobe, output with read data and input with write data | – | X |
| D-CLK# | DDR Clock for negative edge of CLK | – | X |

**Table 1. Input/Output Description** (Continued)

| Symbol | Description | Flash | RAM |
|---|---|---|---|
| RFU | Reserved for Future Use. No device internal signal is currently connected to the package connector but there is potential future use for the connector for a signal. It is recommended to not use RFU connectors for PCB routing channels so that the PCB may take advantage of future enhanced features in compatible footprint devices. | – | – |
| NC | Not Connected. No device internal signal is connected to the package connector nor is there any future plan to use the connector for a signal. The connection may safely be used for routing space for a signal on a Printed Circuit Board (PCB). | – | – |
| DNU | Do Not Use. A device internal signal may be connected to the package connector. The connection may be used by Spansion for test or other purposes and is not intended for connection to any host system signal. Any DNU signal related function will be inactive when the signal is at $V_{IL}$. The signal has an internal pull-down resistor and may be left unconnected in the host system or may be tied to $V_{SS}$. Do not use these connections for PCB signal routing channels. Do not connect any host system signal to these connections. | – | – |

## Ordering Information

The order number (Valid Combination) is formed by the following:




### Valid Combinations

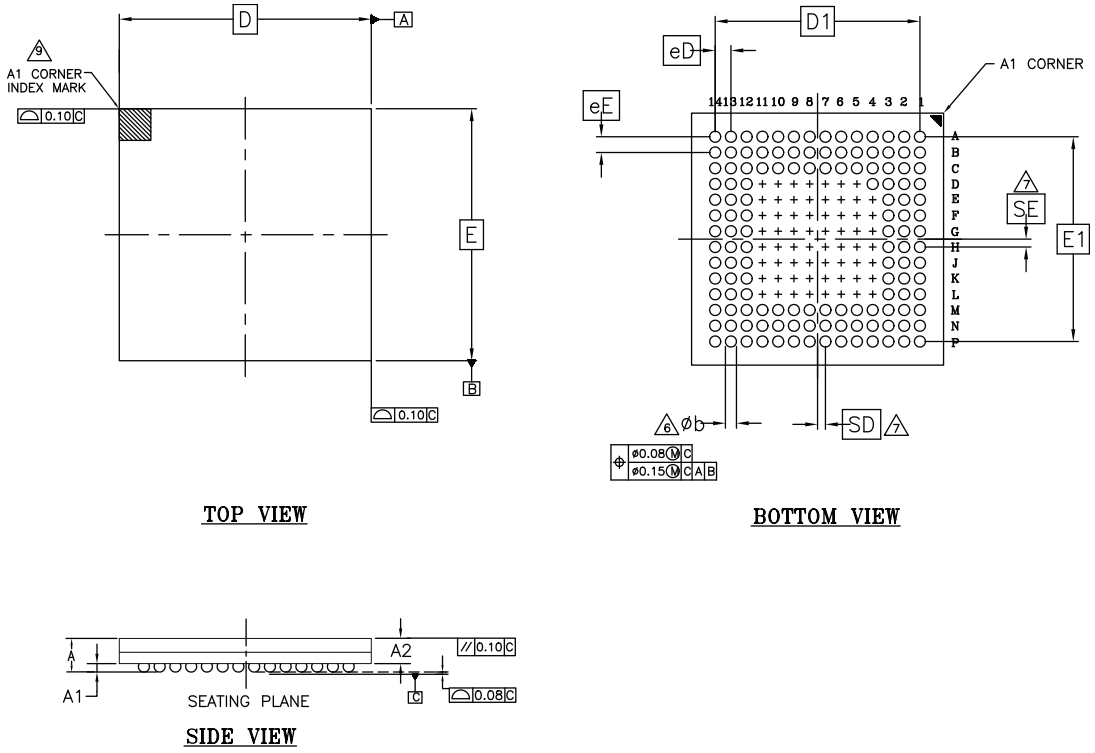
Valid Combinations list configurations planned to be supported in volume for this device. Consult your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

| Base OPN | Package | Model Number | Packing Type | Flash Boot | Temp Range | Electronic Serial Number | Flash Density | DDR DRAM Density | Flash Speed (MHz) | DRAM Speed (MHz) | DRAM Specification | Package |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| S72VS256RE0 | AHB | H1 | 0, 3[2] | Top | Wireless | Yes | 256 Mb | 256 Mb | 108 | 166 | SDM256D166D 1R | 8.0 x 8.0 mm 133-ball MCP (RSC133) |
| | | J1 | | Bottom | | No | | | | | | |
| | | HH | | Top | Industrial | Yes | | | | | SDM256D166D 3R | |
| | | JH | | Bottom | | Yes | | | | | | |

**Note**
2. Packing Type 0 is standard. Specify other options as required.
3. BGA package marking omits leading “S” and packing type designator from ordering part number.

## Physical Dimensions

**Figure 2. RSC133—133-ball Fine-Pitch Ball Grid Array (FBGA) 8.0 x 8.0 mm**




| PACKAGE | RSC 133 | | | NOTE |
|---|---|---|---|---|
| JEDEC | N/A | | | |
| D X E | 8.00mm X 8.00mm PACKAGE | | | |
| SYMBOL | MIN. | NOM. | MAX. | |
| A | – | – | 1.00 | PROFILE |
| A1 | 0.18 | – | – | BALL HEIGHT |
| A2 | 0.62 | – | 0.74 | BODY THICKNESS |
| D | 8.00 BSC | | | BODY SIZE |
| E | 8.00 BSC | | | BODY SIZE |
| D1 | 6.50 BSC | | | MATRIX FOOTPRINT |
| E1 | 6.50 BSC | | | MATRIX FOOTPRINT |
| MD | 14 | | | MATRIX SIZE D DIRECTION |
| ME | 14 | | | MATRIX SIZE E DIRECTION |
| n | 133 | | | BALL COUNT |
| ø b | 0.25 | 0.30 | 0.35 | BALL DIAMETER |
| e | 0.50 BSC | | | BALL PITCH |
| SE/SD | 0.25 BSC | | | SOLDER BALL PLACEMENT |
| | | | | |
| | D5–D11, E4–E11, F4–F11, G4–G11 H4–H11, J4–J11, K4–K11, L4–L11 | | | DEPOPULATED SOLDER BALL |

**NOTES:**

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M–1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JEP95, SECTION 4.3, SPP–010.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   n IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

3643/16-038.63/12.16.09

# Revision History

## Document History Page

| Document Title: S72VS-R MCP, 256 Mb (16M x 16 bit), 1.8V Burst Mode Flash DDR DRAM on Split Bus<br>Document Number: 002-00773 | | | | |
|---|---|---|---|---|
| **Revision** | **ECN** | **Orig. of Change** | **Submission Date** | **Description of Change** |
| ** | — | — | 07/21/2010 | Initial release |
| *A | — | — | 08/24/2010 | Global: Added information for OPN S72VS256RE0AHBH1 |
| *B | — | — | 12/10/2010 | Global: Updated 256 Mb DRAM specification reference |
| *C | — | — | 03/18/2011 | Global: Added OPN S72VS256RE0AHBJ1 |
| *D | — | — | 10/05/2011 | Ordering Information: Replaced Product Selector Guide section<br>Valid Combinations:<br>Made a separate section<br>Added OPNs: S72VS256RE0AHBHH/JH |
| *E | — | — | 04/17/2012 | Ordering Information: Added ESN support for S72VS256RE0AHBH1 |
| *F | 5185100 | TOCU | 03/22/2016 | Updated to Cypress template.<br>Removed any occurrence of 128 Mb and 8M in the document. |

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