S71WS-P

1.8 Volt-only Flash with CellularRAM

Features

- Power supply voltage of 1.7 to 1.95V
- Flash access time: 80 ns, 20 ns
- Flash burst frequencies: 80 MHz, 104 MHz
- pSRAM Access time: 70 ns, 20 ns
- pSRAM burst frequency: 104 MHz
- Package:
  – 8.0 × 11.6 mm MCP
- Operating Temperature
  – –25 °C to +85 °C (wireless)

The S71WS series is a product line of stacked packages and consists of:

- One S29WS256P NOR flash memory die
- CellularRAM die

The products covered by this document are listed in the table below.

Device	CellularRAM Density (Mb)
	64 Mb
S29WS256P	S71WS256PC0

Note:
For a full list of OPNs, please contact the local sales representative or refer to the Ordering Information valid combinations tables.

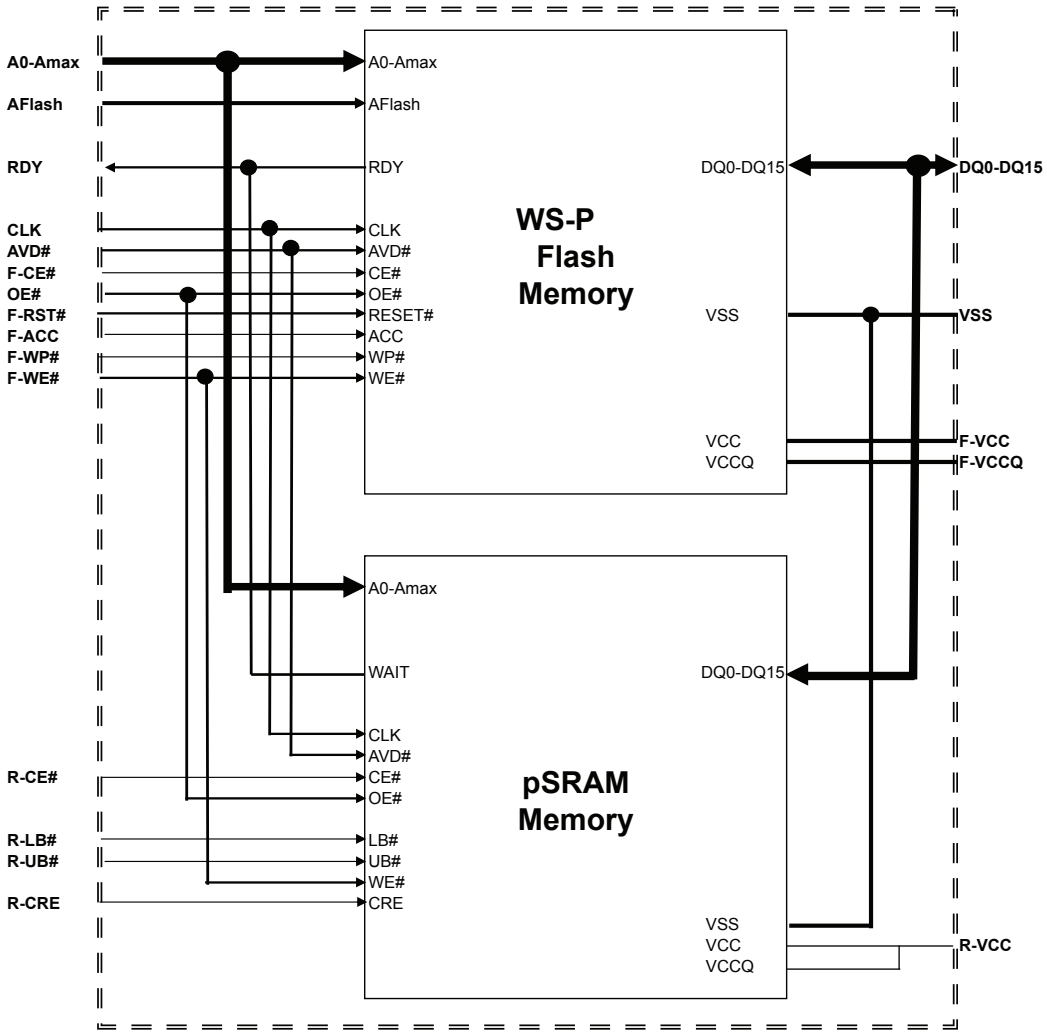
For detailed specifications, please refer to the individual data sheets.

Document	Cypress Document Number
S29WS512/256/128P datasheet	002-01747
64M CellularRAM PN: SWM064D133S1R	SWM064D133S1R

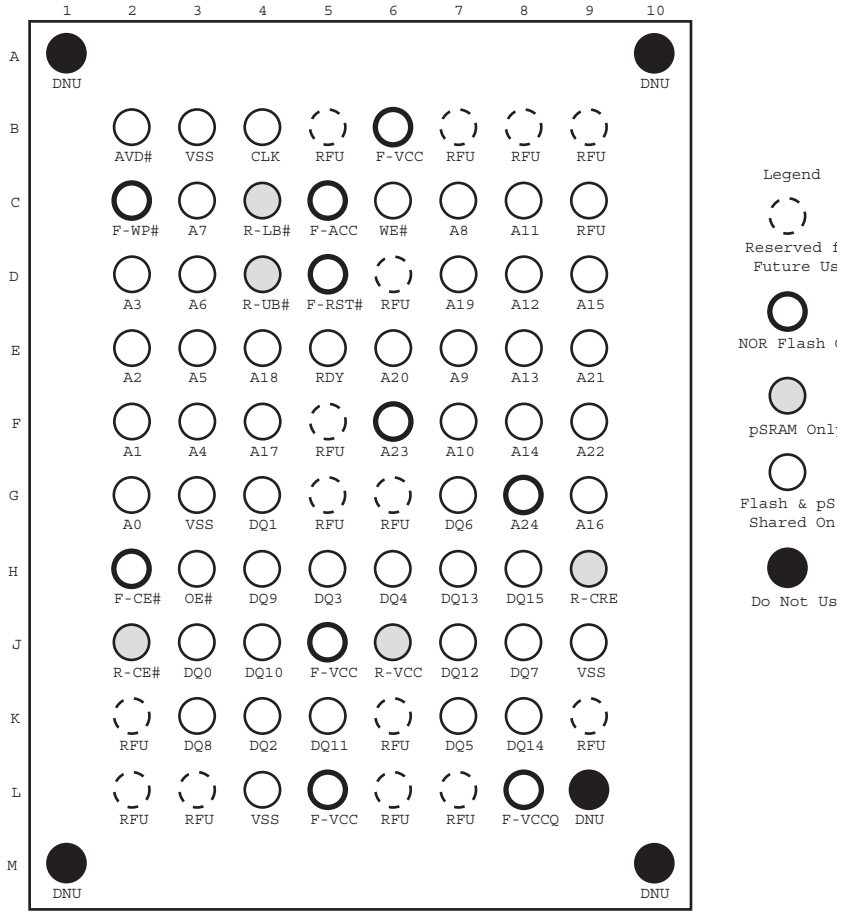
1. Product Selector Guide

Device	Model Number	Flash Density (Mb)	CellularRAM Density (Mb)	Flash Speed (MHz)	CellularRAM Speed (MHz)	CellularRAM Supplier	Package
S71WS256PC0HH3	YL	256	64	104	104	SWM064D133S1R	84 ball MCP 8x11.6x1.2 mm
S71WS256PC0HH3	YR			80			

2. MCP Block Diagram



3. Connection Diagrams



Note:

1. *V_{CC} pins must ramp simultaneously.*

MCP	Flash-only Addresses	Shared Addresses
S71WS256PC0	A23–A22	A21–A0

3.1 Special Handling Instructions For FBGA Package

Special handling is required for Flash Memory products in FBGA packages.

Flash memory devices in FBGA packages may be damaged if exposed to ultrasonic cleaning methods. The package and/or data integrity may be compromised if the package body is exposed to temperatures above 150°C for prolonged periods of time.

3.2 Look-ahead Ballout for Future Designs

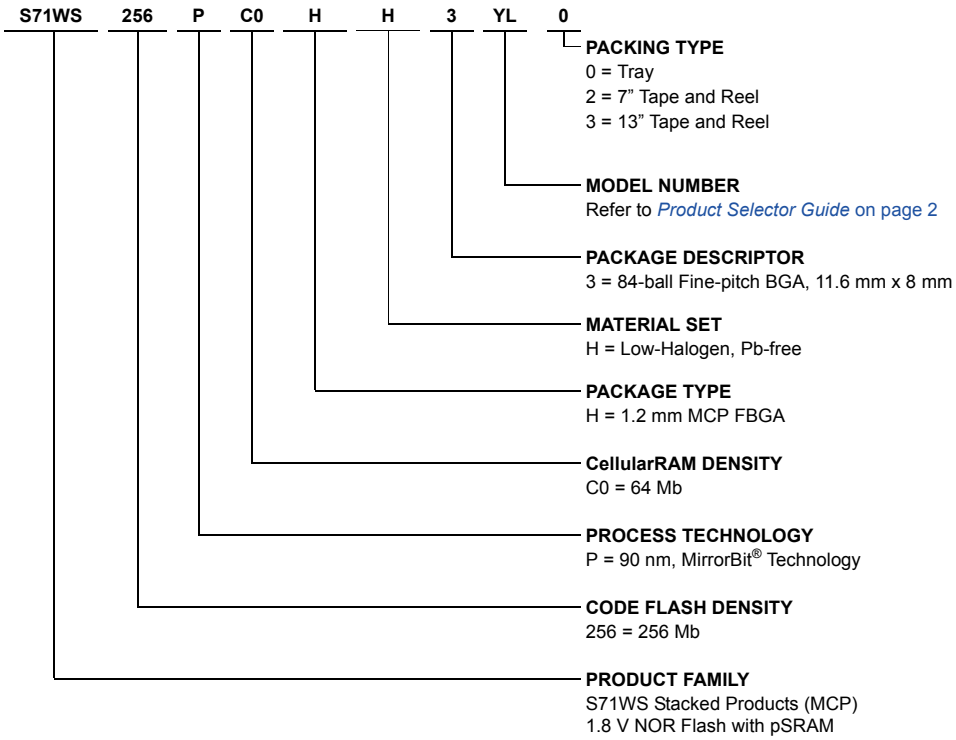
Please refer to the Design-in Scalable Wireless Solutions with Cypress Products application note (publication number: Design_Scalable_Wireless). Contact your local Cypress sales representative for more details.

3.3 NOR Flash and pSRAM Input/Output Descriptions

Signal	Description	Flash	pSRAM
Amax-A0	NOR Flash Address inputs	X	X
DQ15-DQ0	Flash Data input/output	X	X
F-CE#	NOR Flash Chip-enable input #1. Asynchronous relative to CLK for Burst Mode.	X	
OE#	Output Enable input. Asynchronous relative to CLK for Burst mode.	X	X
WE#	Write Enable input.	X	X
F-V_{CC}	NOR Flash device power supply (1.7 V - 1.95 V).	X	
F-V_{CCQ}	Input/Output Buffer power supply.	X	
V_{SS}	Ground	X	X
RFU	Reserved for Future Use. No device internal signal is currently connected to the package connector but there is potential future use for the connector for a signal. It is recommended to not use RFU connectors for PCB routing channels so that the PCB may take advantage of future enhanced features in compatible footprint devices.		
RDY	Flash ready output. Indicates the status of the Burst read. V_{OL} = data valid. The Flash RDY pin is shared with the WAIT pin of the pSRAM.	X	X
CLK	NOR Flash Clock, shared with CLK of burst-mode pSRAM.. The first rising edge of CLK in conjunction with AVD# low latches the address input and activates burst mode operation. After the initial word is output, subsequent rising edges of CLK increment the internal address counter. CLK should remain low during asynchronous access.	X	X
AVD#	NOR Flash Address Valid input. Shared with AVD# of burst-mode pSRAM. Indicates to device that the valid address is present on the address inputs. V_{IL} = for asynchronous mode, indicates valid address; for burst mode, causes starting address to be latched on rising edge of CLK. V_{IH}= device ignores address inputs	X	X
F-RST#	NOR Flash hardware reset input. V_{IL}= device resets and returns to reading array data	X	
F-WP#	NOR Flash hardware write protect input. V_{IL} = disables program and erase functions in the four outermost sectors.	X	
F-ACC	NOR Flash accelerated input. At V_{HH}, accelerates programming; automatically places device in unlock bypass mode. At V_{IL}, disables all program and erase functions. Should be at V_{IH} for all other conditions.	X	
R-CE#	Chip-enable input for pSRAM		X
R-CRE	Control Register Enable (pSRAM). For CellularRAM only.		X
R-VCC	pSRAM Power Supply		X
R-UB#	Upper Byte Control (pSRAM)		X
R-LB#	Lower Byte Control (pSRAM)		X
DNU	Do Not Use. A device internal signal may be connected to the package connector. The connection may be used by Cypress for test or other purposes and is not intended for connection to any host system signal. Any DNU signal related function will be inactive when the signal is at V_{IL}. The signal has an internal pull-down resistor and may be left unconnected in the host system or may be tied to V_{SS}. Do not use these connections for PCB signal routing channels. Do not connect any host system signal to these connections. Note: Some customers prefer being able to tie DNU signals to V_{SS} on the PCB.		

4. Ordering Information

The order number is formed by a valid combinations of the following:



4.1 Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

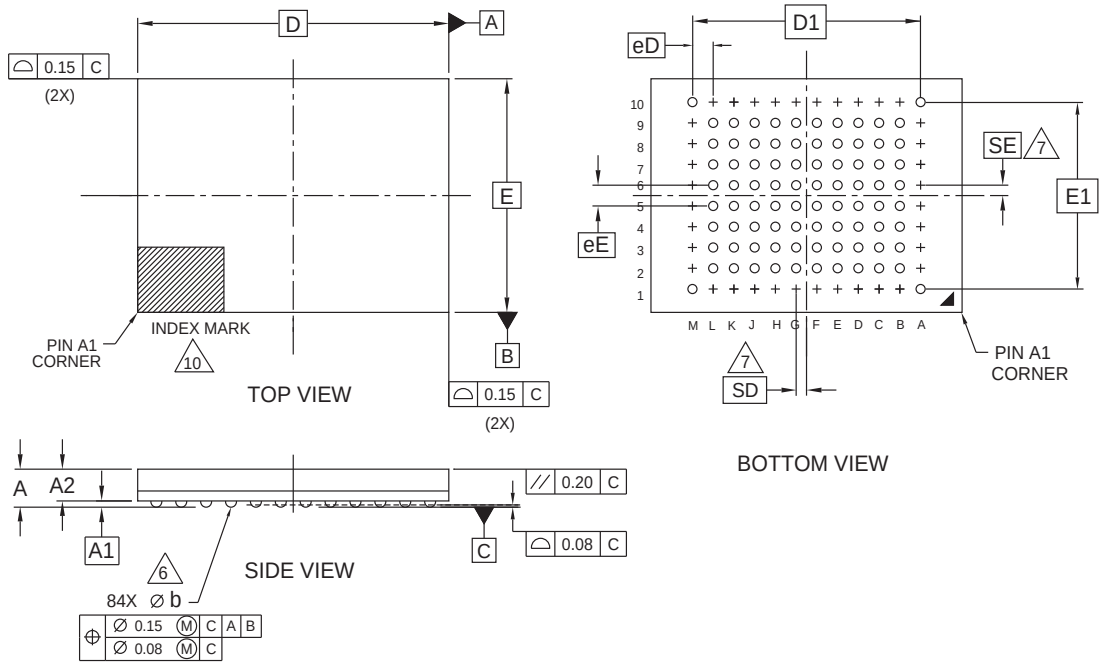
Valid Combination						
Product Family	**Code Flash Denisty (Mb)**	**Process Technology**	**CellularRAM Density**	**Package Type / Material**	**Model Number Combo**	**Packing Type**
S71WS	256	P	C0	HH3	YL, YR	0, 2, 3 (Note 1)

Notes:

1. *Packing Type 0 is standard. Specify other options as required.*
2. *BGA package marking omits leading S and packing type designator from ordering part number.*

5. Physical Dimensions

5.1 TLA084— 84-ball Fine Pitch Ball Grid Array (FBGA) 8 x 11.6 mm Package



PACKAGE	TLA 084			
JEDEC	N/A			
D x E	11.60 mm x 8.00 mm PACKAGE			
SYMBOL	MIN	NOM	MAX	NOTE
A	---	---	1.20	PROFILE
A1	0.17	---	---	BALL HEIGHT
A2	0.81	---	0.97	BODY THICKNESS
D		11.60 BSC.		BODY SIZE
E		8.00 BSC.		BODY SIZE
D1		8.80 BSC.		MATRIX FOOTPRINT
E1		7.20 BSC.		MATRIX FOOTPRINT
MD		12		MATRIX SIZE D DIRECTION
ME		10		MATRIX SIZE E DIRECTION
n		84		BALL COUNT
Ø b	0.35	0.40	0.45	BALL DIAMETER
eE		0.80 BSC.		BALL PITCH
eD		0.80 BSC		BALL PITCH
SD / SE		0.40 BSC.		SOLDER BALL PLACEMENT
		A2,A3,A4,A5,A6,A7,A8,A9 B1,B10,C1,C10,D1,D10, E1,E10,F1,F10,G1,G10, H1,H10,J1,J10,K1,K10,L1,L10, M2,M3,M4,M5,M6,M7,M8,M9		DEPOPULATED SOLDER BALLS

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JESD 95-1, SPP-010.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.

   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.

   n IS THE NUMBER OF POPULTED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.

6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.

   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. N/A
10. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

3372-2 \ 16-038.22a

6. Revision History

Spansion Publication Number: S71WS-P_00

Section	Description
Revision 01 (February 21, 2006 to August 17 2012)	
	Initial Release
	Added the S71WS512PC0
	Added the S71WS512PD0 108MHz OPN
	Added the S71WS256PD0 MCP
	Added the S71WS256PC0 MCP
	Added new CellularRAM Type 3
	Revised Valid Combination table
	Revised Product Selector Guide
	Added S71WS128PC0 MCP offering
	Added the S71WS512PD0JF4 OPN
	Added the S71WS512PD0HF3SR OPN
	Added 80 MHz S71WS128PC0 to Valid Combinations
	Added 54 MHz and Asynchronous S71WS512PC0 MCP
	Revised Valid Combinations
	Add 104 MHz, 80 Mhz and 66 MHz S71WS256PC, S71WS256PD and S71WS128PC MCP products
	Removed the S71WS512PD0JF MCP
	Added package TSB084
	Added OPNs S71WS128PB0HF3SR/SV
	Added low-Halogen options for S71WS128PB0, S71WS128PC0, S71WS256PC0, S71WS256PD0, and S71WS512PD0
	Added 64M CellularRAM Type 2
	Updated 128M CellularRAM Type 2 PID
	Removed 128M/64M CellularRAM Type 3 OPNs and PIDs
	Added CellularRAM Type 3 and associated OPNs
	Added CellularRAM PN: SWM128D104R1R and associated OPNs
	Changed Flash Page Access time to 20 ns
	In Features, changed max Flash burst frequency from 108 MHz to 104 MHz
	Removed OPNs S71WS512PD0HH3HL, S71WS256PD0HH3HL, S71WS256PD0HH3HR
	Added MCP OPNs S71WS256PC0HH3YR0/L0 and CellularRAM OPN SWM064D133S1R
	Added MCP OPNs S71WS128PB0HH3RL0/RR0/RV0 for new 32 Mb CellularRAM OPN SWM032D133S1R
	Removed all OPNs except S71WS512PD0HH3YL/YR/YV, S71WS256PC0HH3YR/YL and S71WS128PB0HH3RL/RR/RV
	Removed TSB084 drawing
	Removed all OPNs and corresponding references, except S71WS256PC0HH3YR/YL

Document History Page

Document Title: S71WS-P 1.8 Volt-only Flash with CellularRAM Document Number: 001-98532				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	–	WIOB	02/21/2006 to 08/17/12	Initial Release Added the S71WS512PC0 Added the S71WS512PD0 108MHz OPN Added the S71WS256PD0 MCP Added the S71WS256PC0 MCP Added new CellularRAM Type 3 Revised Valid Combination table Revised Product Selector Guide Added S71WS128PC0 MCP offering Added the S71WS512PD0JF4 OPN Added the S71WS512PD0HF3SR OPN Added 80 MHz S71WS128PC0 to Valid Combinations Added 54 MHz and Asynchronous S71WS512PC0 MCP Revised Valid Combinations Add 104 MHz, 80 Mhz and 66 MHz S71WS256PC, S71WS256PD and S71WS128PC MCP products Removed the S71WS512PD0JF MCP Added package TSB084 Added OPNs S71WS128PB0HF3SR/SV Added low-Halogen options for S71WS128PB0, S71WS128PC0, S71WS256PC0, S71WS256PD0, and S71WS512PD0 Added 64M CellularRAM Type 2 Updated 128M CellularRAM Type 2 PID Removed 128M/64M CellularRAM Type 3 OPNs and PIDs Added CellularRAM Type 3 and associated OPNs Added CellularRAM PN: SWM128D104R1R and associated OPNs Changed Flash Page Access time to 20 ns In Features, changed max Flash burst frequency from 108 MHz to 104 MHz Removed OPNs S71WS512PD0HH3HL, S71WS256PD0HH3HL, S71WS256PD0HH3HR Added MCP OPNs S71WS256PC0HH3YR0/L0 and CellularRAM OPN SWM064D133S1R Added MCP OPNs S71WS128PB0HH3RL0/RR0/RV0 for new 32 Mb CellularRAM OPN SWM032D133S1R Removed all OPNs except S71WS512PD0HH3YL/YR/YV, S71WS256PC0HH3YR/YL and S71WS128PB0HH3RL/RR/RV Removed TSB084 drawing Removed all OPNs and corresponding references, except S71WS256PC0HH3YR/YL
*A	4965208	WIOB	10/15/2015	Updated to Cypress template.

Document History Page (Continued)

Document Title: S71WS-P 1.8 Volt-only Flash with CellularRAM Document Number: 001-98532				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
*B	5162276	PSR	03/04/2016	Updated *Features* on page 1: Replaced “S29WS-P” with “S29WS256P”. Updated table for detailed specifications: Replaced “S29WS-P” with “S29WS512/256/128P datasheet” in “Document” column. Replaced “Publication Identification Number (PID)” with “Cypress Document Number” in column heading and replaced “S29WS-P_00” with “002-01747” in the same column. Updated to new template.
*C	5963292	AESATMP8	11/10/2017	Updated logo and Copyright.

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