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S6J34x8/9/A

32-bit Microcontroller

S6J3400 Series Hardware Manual Traveo™ Family

Document Number: 002-09919 Rev. *F

Cypress Semiconductor
An Infineon Technologies Company
198 Champion Court
San Jose, CA 95134-1709

www.cypress.com

www.infineon.com

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Preface



Thank you for your continued use of Cypress semiconductor products.
Read this manual and "Data Sheet" thoroughly before using products in this family.

Purpose of this manual and intended readers

This manual explains the functions and operations of this family and describes how it is used. The manual is intended for engineers engaged in the actual development of products using this family.

** This manual explains the configuration and operation of the peripheral functions, but does not cover the specifics of each device in the family.*

Users should refer to the respective data sheets of devices for device-specific details.

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CHAPTER 1: Overview



This chapter explains the product overview.

1. Overview
2. Document definition
3. Register attribute
4. Vocabulary

CODE: OVERVIEW-S6J3400-E1.1

1. Overview

S6J3400 is a microcontroller series which is to be applied to automotive systems representative of a body control unit.

2. Document Definition

The related documents of S6J3400 are the followings.

Table 2-1 Related Documents

Document Type	Definition	Primary User	Document Code
Datasheet	The function and its characteristics are specified quantitatively.	Investigator and Hardware Engineer	001-97829
S6J3400 Hardware Manual	The function and its operation of S6J3400 series are described.	Software Engineer	002-09919
Traveo™ Platform Hardware Manual	The function and its operation of CPU core platform are described.	Software Engineer	002-07884
Application Note	The reference software, sample application, the reference board design and so on are explained.	Software and Hardware Engineer	Under consideration

Note:

- Refer all documents for the system development.
- "Primary user" is a most likely an engineer for whom the document is the most useful.
- The description of the datasheet and the S6J3400 Hardware Manual should precede the duplicated description of Traveo™ Platform Hardware Manual.
- Traveo™ Platform Hardware Manual is expected to be used as dictionary of platform specification.

3. Register Attribute

3.1. Read and Write

Refer the table with the following definition.

Table 3-1 Register Attribute of Read and Write

Attribute	Definition
R	It can be read.
R0	"0" is to be read.
R1	"1" is to be read.
RX	The read value is undefined.
W	It can be written.
W0	"0" must be written.
W1	"1" must be written.
WX	Writing doesn't affect the operation.
"/" (slash)	The read value is same as the written value.
"," (comma)	The read value is different from the written value.

■ Example

R/W : The written value is to be read.

R, W0 : "0" must be written, and the read value is different from the written value.

Note:

- The register attribute of a status register which has its clear register and set register is conveniently described to be R/W though the written value cannot be read directly. In this case R/W has a meaning that the controlled value is to be read.
- A register attribute does not necessarily describe a prohibited operation of the register. Any prohibited operations should be referred within the line of the register description as well. See every description of the register specification together with every note.

3.2. Protection

Refer the table with the following definition.

Table 3-2 Register Attribute of Protection

Attribute	Definition
RP	It can be read at the supervisor mode.
WP	It can be written at the supervisor mode.
WS	It can be written after cancelling the sequence protection.
WPS	It can be written after cancelling the sequence protection at the supervisor mode.

3.3. Register Information

You can also see register information in a table as below.

BIT_OFFSET	The bit offset (Ex. 31,30,29,,,0)
BIT_NAME	The bit name
ACCESS_TYPE	The allowed access defined 3.1
PROT_TYPE	The allowed access defined 3.2
INITIAL_VALUE	The initial value

4. Vocabulary

A/D converter	Analog digital converter	
ADC	Analog digital converter	
AHB	Advanced high performance bus	
AMBATM	Advanced microcontroller bus architecture	
APB	Advanced peripheral bus	
ATCM	TCM-A port	
AXI	Advanced extensible interface	
B0TCM	TCM B0 port	
B1TCM	TCM B1 port	
BBU	Bit banding unit	
BDR	Boot description record	
CAN	Control area network	
CD	Clock domain	
CPU	Central processing unit	
CR	CR Oscillator	
CRC	Cyclic redundancy check	
CSV	Clock supervisor	
DAP	Debug access port	
DED	Dual error detection	
DMA	Direct memory access	
DMAC	DMA controller	
ECC	Error correction code	
ETM	Embedded trace macro	
EXT-IRC	External interrupt controller	
FIQ	Fast interrupt request	
FPU	Floating point unit	
FRT	Free run timer	
GPIO	General purpose I/O	
HPM	High performance matrix	
HW-WDT	Hardware watchdog timer	
I/O	Input or output	
ICU	Input capture unit	
IPCU	Inter-processor communication unit	
IRC	Interrupt controller	
IRQ	Interrupt request	
ISR	Interrupt service routine	
JTAG	Joint test action group	
LLPP	Low latency peripheral port	
LVD	Low voltage detector	
MCU	Microcontroller unit	
MFS	Multi-function serial interface	
NF	Noise filter	
NMI	Non maskable interrupt	
OCU	Output compare unit	

OSC	Oscillator	
PLL	Phase locked loop	
PONR	Power on reset	
PPC	Port pin configuration	
PSS	Power saving state	
PWM	Pulse width modulation	
RAM	Random access memory	
RIC	Resource input configuration	
ROM	Read only memory	
RTC	Real time clock	
RVD	Low voltage detection and reset for RAM retention	
SCT	Source clock timer	
SEC	Single error correction	
SEDED	Single error correction and dual error detection	
SHE	Secure Hardware Extension	
SRAM	Static RAM	
SW-WDT	Software watchdog timer	
SYSC	System controller	
TCFLASH	FLASH connected to TCM	
TCM	Tightly coupled memory	
TCRAM	RAM connected to TCM	
TPU	Timing protection unit	
UDC	Up-down counter	
VIC	Vectored interrupt controller	
WDR	Watchdog description record	
WDT	Watchdog timer	
WorkFLASH	Work FLASH memory	

CHAPTER 2: Function List



This chapter explains the functions.

1. Function list
2. Optional function

CODE: FUNCTIONLIST-S6J3400-E1.1

1. Function list

The table shows the functions which are implemented in S6J3400 series.

Table 1-1. Function List

Function	Description			Remark
	S6J34xxJxx	S6J34xxHxx	S6J34xxFxx	
CPU core	Arm® Cortex® R5F			
FPU	Available			
PPU	Available			
MPU	Available			
TPU	Available			
Endian	Little endian			
Core clock frequency	132MHz			See the AC specification on the datasheet
HPM bus frequency	33MHz			See the AC specification on the datasheet
LLPM bus frequency	33MHz			See the AC specification on the datasheet
Resource clock frequency	40MHz (Max)			
Embedded CR oscillation	Slow clock: 100kHz, Fast clock: 4MHz (Center frequency)			See the AC specification on the datasheet
PLL	PLL0			
SSCG PLL	SSCG0			
Clock supervisor	Available			
DMA	1 instance 16 ch 128 DMA client interfaces			
Boot-ROM	16 Kbyte			
JTAG	Available			
Data cache	16Kbyte			
Instruction cache	16Kbyte			
Program FLASH	Option			See 2.1
Work FLASH	112Kbyte			
TC-RAM	Option			See 2.1
System SRAM	Option			See 2.1
Backup area in System SRAM	Option			See 2.1
Security (SHE)	Option			See 2.1
Low latency interrupt	Available			
Power domain	3 domains			
Power supply	5.0V +/- 0.5V or 3.3V +/- 0.3V			See the AC specification on the datasheet
Embedded LDO power supply for 5.0V	Available			
Low voltage detection of external power supply	Available			

Function	Description			Remark
	S6J34xxJxx	S6J34xxHxx	S6J34xxFxx	
Low voltage detection of internal LDO output	Available			
Hardware watchdog timer	Available			
Software watchdog timer	Available			
Package	Option			See 2.1
AUTOSAR	AUTOSAR 4.0.3			
General Purpose I/O	Option			See 2.2
Up/down counter (QPRC)	2 ch			
I/O timer	FRT 8ch x ICU 12ch x OCU 12ch			memory size digit from 8 to A
32bit Reload timer	6 ch			
Real time clock	Available			Automatic calibration
Base timer	64ch	60ch	48ch	with output pin or input pin
	64ch	55ch	40ch	with output pin
	64ch	57ch	30ch	with input pin
12bit-A/D converter	64ch 32ch+32ch	56ch 24ch+32ch	35ch 15ch+20ch	See 2.2
Partial Wake Up	analog input 8ch	analog input 8ch	analog input 7ch	Trigger 1ch
CRC	4 ch			
Programmable CRC	1 ch			
Source clock timer	4 ch			
NMI	Available			
External interrupt	32 ch			See the AC specification on the datasheet
Internal interrupt	256 vectors			
Multi-function serial interface	14ch	13ch	13ch	memory size digit from 8 to A See the AC specification on the datasheet
	14ch	13ch	12ch	with CS pin See the AC specification on the datasheet
CAN-FD	6 ch			
CAN-FD RAM (ECC supported)	16KB/ch It is equivalent to 192 message buffer per channel of CAN module			
BUS DIAGNOSIS FUNCTION	Available			
BASE TIMER SIMULTANEOUS OPERATION	1 ch			

Note:

- The options are described in 2. Optional FunctionOptional .

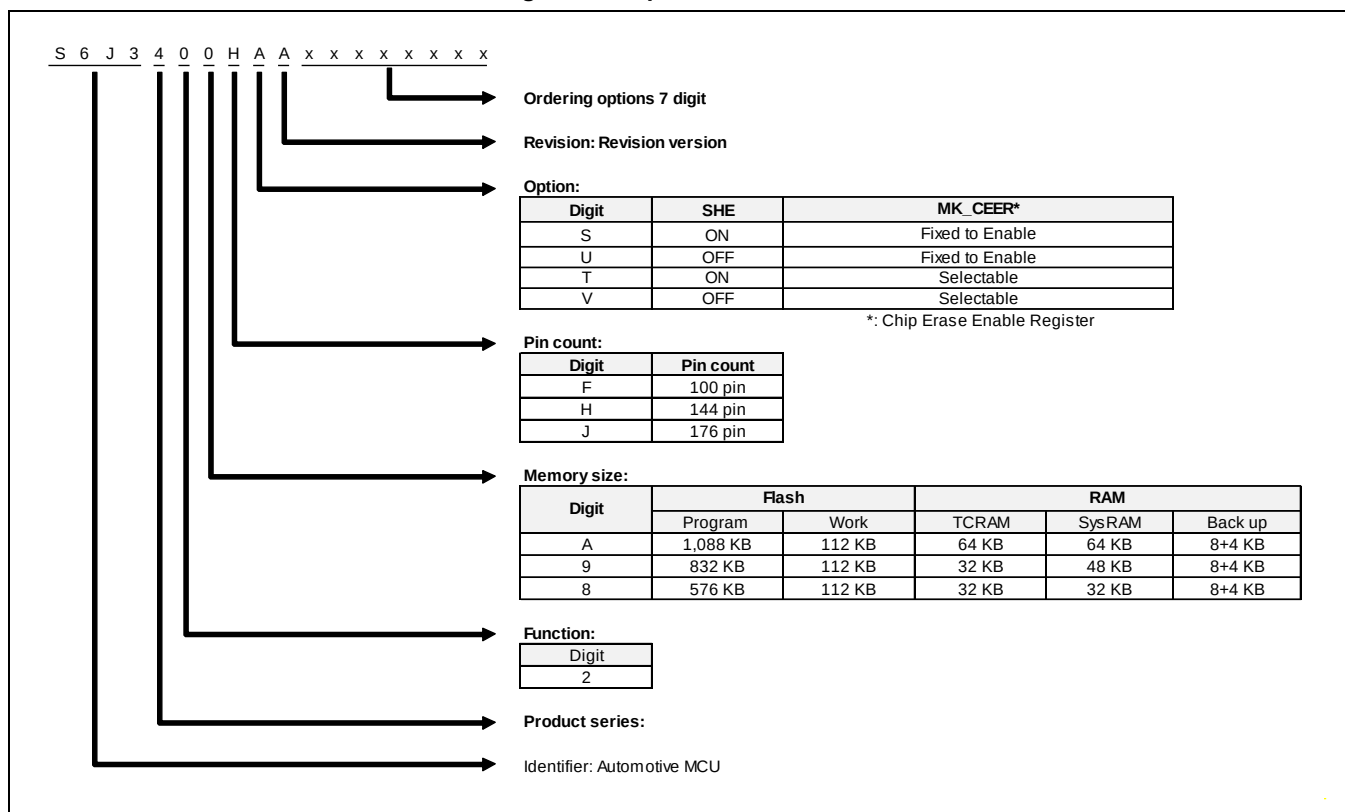
- *The described specifications in the table which are related the electric characteristics only show the typical values. They don't necessarily include the width of characteristics, errors, and so on. They should be seen in the datasheet in detailed.*

2. Optional Function

2.1. Basic Option

The figure shows the optional function and the part number relations of the series.

Figure 2-1. Optional Function



Note:

- This table only shows the relations between the optional function and the part numbers. That is, all products are not necessarily available for orders. See the order number on the datasheet, and confirm actual availabilities of products.

2.2. ID

See the ID specification on the Datasheet in detail.

2.3. Restriction

Some functions have restrictions which depend on package pin counts.

Table 2-1. Restrictions on Package Pin Counts

Function	LQFP144	LQFP100
Analog input port (12bit-ADC)	AN001 to 002, AN007, AN012, AN015 to 016, AN023 to 024 (56 ports)	AN001 to 002, AN004, AN006 to 007, AN009, AN011 to 012, AN015 to 016, AN018, AN020, AN023 to 024, AN026, AN029, AN031, AN101, AN103 to 105, AN115 to 117, AN122, AN124, AN126, AN130 to 131 (35 ports)
General purpose I/O	P002, P004, P011, P014, P025 to 026, P102, P104, P110 to 111, P116, P121, P124 to 125, P200 to 201, P216 to 217, P221, P303, P310 to 311, P316, P320, P325 to 326, P328 to 329, P410, P412, P415, P419	P000, P002 to P004, P008 to P009, P011, P014, P017 to 019, P023 to 026, P030, P101 to 102, P104, P110 to 111, P113, P115 to 116, P118, P120 to 121, P124 to 125, P127, P129, P200 to 201, P203, P206, P208, P210, P212, P216 to 219, P221, P230 to 231, P300, P303, P306, P308, P310 to 312, P316 to 320, P325 to 326, P328 to 330, P403 to 404, P406 to 408, P410 to 412, P414 to 415, P417 to 419, P421
Base timer	TIOA0/1/2/3_1 TIOA14/15/16/17/18_0 TIOA21/25/26/27_1 TIOA51/57/58/59/61_0 TIOB56/57/58/59/60/61/62_0	TIOA0/1_0 TIOA0/1/2/3/5_1 TIOA9/10/13_1 TIOA7/8/14/15/16/17/18/19_0 TIOB0/4/5/8/10/12_0 TIOB14/15/19/22/23_0 TIOA21/26/27/28_0 TIOA21/23/25/26/27/28_1 TIOA49/51/53/56/57/58/59/60_0 TIOA61/62/63_0 TIOB24/25/29/33/35/37/38_0 TIOB43/44/46/47/48/49_0 TIOB51/53/56/57/58/59/60_0 TIOB61/62/63_0
FRT	TEXT10_0	TEXT0/2/3/10_0, TEXT1/4_1

Function	LQFP144	LQFP100
External interrupt	INT10/13/15_0, INT23/25/26_1, INT1_2	INT6/9/10_0, INT12/13/14/15_0, INT0/5_1, INT11/12/13/15/16/19_1, INT20/22/23/25/26/27_1, INT31_1, INT1/4/5_2, INT11/12_2
Partial wake up	PWUTRG_0	PWU_AN7 PWUTRG_0
CAN-FD	-	TX0_0, RX1_1, TX1_1 TX2_1
Multi-function serial	SCS21_1, SCS23_0, SCS23_1, SCS40_1, SCS41_1, SCS52_0, SIN6_1, SOT6_1, SCS70_1, SCS72_1, SCS110_0, SIN12_0, SIN12_1, SOT12_1, SCK13_0, SIN13_0, SOT13_0, SCS130_0	SCS0_0, SCK2_0, SIN2_0, SIN2_1, SOT2_1, SCS21_0, SCS21_1, SCS22_0, SCS22_1, SCS23_0, SCS23_1, SCS30_0, SIN4_0, SIN4_1, SOT4_1, SCS40_1, SCS41_0, SCS41_1, SCS42_0, SCS43_0, SCS43_1, SCS50_1, SCS52_0, SIN6_1, SOT6_1, SCS60_2, SCS61_0, SCK7_1, SIN7_0, SIN7_2, SOT7_1, SCS70_1, SCS71_0, SCS71_1, SCS72_1, SCS73_0, SIN8_0, SCS83_0, SCK9_0, SOT9_0, SCS90_1, SCS101_0, SCS102_0, SCS103_0, SOT11_1, SCS110_0, SCK12_0, SIN12_0, SIN12_1, SOT12_1, SCS120_1, SCK13_0, SIN13_0, SOT13_0, SCS130_0
I ² C	SCL13_0, SDA13_0	SCL2_0, SCL9_0, SDA9_0, SCL12_0, SCL13_0, SDA13_0
Input capture	-	IN2/3_0, IN0/2_1, IN0/2_2, IN19/20_0, IN16/20_1
Output compare	-	OUT1/2/3_0, OUT2/5_1, OUT19/20/21_0

Function	LQFP144	LQFP100
Quad position & revolution counter	-	AIN8_0, AIN8_1, ZIN8_0
Reload timer	-	TOT2_0, TOT3_0, TOT16_0, TOT17_0
Trace	-	TRACECTL_0, TRACEDATA0/1/3/4/5/7_0

Note:

- See multiplexed functions on pin assignment sheet.
- The optional restriction will be added without notification.

CHAPTER 3: Product Description



This chapter explains the function feature.

1. Overview
2. Product description
3. Note

CODE: PRODUCT-S6J3400-E3

1. Overview

This chapter explains the product features of S6J3400 series. The description of this chapter should precede the duplicated description on Traveo™ Platform Hardware Manual.

■ Option Features

See the common information of the option features on the Hardware Manual of Traveo™ Platform.

In the case of option of default and LP-Type, S6J3400 select the LP-Type.

In the case of options that do not include the LP-Type, S6J3400 select the default.

2. Product Description

The table shows features.

Table 2-1. Features and Description

Feature	Description
Technology	40nm CMOS technology with embedded FLASH Fully automotive qualified according to ISO/TS 16949 and AEC-Q100
Functional Safety	The product series has some functional safety features suited for ASIL-B application.
Peripherals	See the chapter of "Function List" on this manual.
Power Domain (PD)	See the Traveo™ Platform Hardware Manual and the chapter of "State Transition" on this manual in detail.
Debug and Trace	See the Traveo™ Platform Hardware Manual in detail. - Standard 5-pin JTAG interface - SWD (Serial Wire Debug) interface 16kB Embedded Trace Buffer 8-bit trace support.
System Control	See the Traveo™ Platform Hardware Manual in detail. Main and sub oscillator is available. - A wide range of 3.6 - 16MHz is available for main oscillator 32KHz is available for sub oscillator Sub clock is enable/disable by register settings
Clock	See the Traveo™ Platform Hardware Manual in detail. CLK_CLKO (Clock Output Function) is supported.
Embedded CR oscillation	See the Traveo™ Platform Hardware Manual in detail. Stabilization time is as followings. 30us for 4MHz (Fast clock) 20us for 100kHz (Slow clock)
Clock Supervisor	See the Traveo™ Platform Hardware Manual in detail. This product series doesn't support clock supervisor output port. (Related register and internal circuit is implemented.)
Reset	RSTX pin + MD pin simultaneous assert INITX (Same as INITX pin input) - Occurrence factor: Simultaneously inputting "L" level to RSTX pin and inputting "L" level to MD pin - Release factor: Inputting "H" level to RSTX pin See the Traveo™ Platform Hardware Manual in detail. Following resets are not mounted on this device. - SRSTX (and nSRST pin)
Hardware watchdog	See the Traveo™ Platform Hardware Manual in detail. Hardware watchdog function stops during PSS mode. In the related register of HWDG_CFG, the bit ALLOWSTOPCLK is always read as 1 (HWDG_CFG.ALLOWSTOPCLK=1). The product series doesn't support Watchdog Counter Monitor Output port. (Related register and internal circuit is implemented.).
Software watchdog	See the Traveo™ Platform Hardware Manual in detail. The product series doesn't support Watchdog Counter Monitor Output port. (Related register and internal circuit is implemented.).

Feature	Description
Standby mode	See the Traveo™ Platform Hardware Manual in detail. Standby mode with 5V (or 3.3V) single power supply is available.
Partial wakeup	Partial wakeup function is mounted. This mode is one of the PSS modes.
PLL / SSCG PLL	See the Traveo™ Platform Hardware Manual in detail. Use case assumption is following. - PLL ➤ Peripherals ➤ Trace clock - SSCG ➤ CPU core ➤ Peripherals
External Interrupts	Sensitive: H level, L level, pos-edge, neg-edge, both-edge
NMI	Sensitive: L level 1 NMI pin.
Memory Protection	16 region MPU inside CPU core (see the Cortex™-R5 Revision:r1p2 Technical Reference Manual) 8 region MPU for SHE (see Memory Protection Unit for AXI of SHE in Traveo™ Platform Hardware Manual) 16 region MPU for DMA controller (see MPU16 AHB in Traveo™ Platform Hardware Manual) To configure Lock or Unlock for both MPUXn_UNLOCK and MPUHn_UNLOCK. - Lock: 0x112ABB56 - Unlock: 0xACCABB56
Peripheral Protection	See the Traveo™ Platform Hardware Manual in detail. Protected peripherals are described in the base address map.
Internal Memories System SRAM	See the Traveo™ Platform Hardware Manual in detail. Max memory size is smaller than the above value on some product type. Please see the " Optional Function " of the chapter of "Function List" on this manual.
Internal Memories TCRAM	See the Traveo™ Platform Hardware Manual in detail. Max memory size is smaller than the above value on some product type. Please see the " Optional Function " of the chapter of "Function List" on this manual.
Internal Memories Backup area in System SRAM	Up to 64kByte Backup area can only be operated in RUN mode (normal operation mode). In other mode the memory content should be retained, but it cannot be operated. SLEEP control for Backup area is not supported and cannot be used.

Feature	Description
Embedded Program/Work Flash Memory	Embedded Program Flash can be accessed with 0wait cycle if CPU frequency is 80MHz or less. 0-wait-cycle: 80MHz or less. 1-wait-cycle: 132MHz or less. Work Flash can be accessed with 0-wait-cycle if CPU frequency is 12.5MHz or less. 6-wait-cycle: 80MHz or less. 10-wait-cycle: 132MHz or less. The wait-cycle setting see the Traveo™ Platform Hardware Manual in details. The maximum frequency should be referred in datasheet. Erase suspend is supported. Reading and writing to the other sector are possible when Flash Erase is suspended. Serial Flash programing and Parallel Flash programing are supported. Margin mode is not supported.
Internal Power Domain	PD1: Always ON PD2: Cortex R5F platform/ additional peripherals PD4: Backup RAM in Always On domain * The chapter of the "Block Diagram" on this manual explains in detailed.
Power Supply	External 5V (or 3.3V) is required. Built in LDO provides internal voltage. There are constraints of power on/off sequence.
Low Voltage Detection	LVD for external voltage is supported. LVD for internal voltage is supported. See the specification of the detected level on the datasheet.
Low voltage detection for RAM retention (RVD)	RVD for RAM retention is effective during the standby mode only. That is, it is only for the retention RAM that the function is available.
Resource inter-connect	The output signal of some resources can be inputted to the other resource.
I/O Ports	5V general purpose I/O Multi input level and multi output drivability Pull-up, pull-down function is available. Resource input and output is multiplexed. +B input is allowed many pins.
A/D Converter	12bit resolution, 2 unit 64 channels of analog input for TEQFP176 56 channels of analog input for LQFP144 35 channel of analog input for LQFP100 External trigger and timer trigger are available. The description of the A/D converter function should be referred in the S6J3400 Hardware Manual.
CRC	4 CRC calculators (CRC32, CCITT)
Programmable CRC	DMA support

Feature	Description
Base Timer	16-bit PWM Timer 16-bit PPG Timer 16/32-bit Reload Timer 16/32-bit PWC Timer.
Base Timer Simultaneous Operation	16-bit Global Timer 1ch
Reload Timer	32-bit Reload Timer
I/O Timer	32-bit Freerun Timer 32-bit Input Capture 32-bit Output Compare
QPRC (Quad Precision Counter)	Quad Position & Revolution Counter 16-bit position counter
Multi-Functional Serial (MFS)	UART mode CSIO (SPI) mode LIN mode I ² C mode Only 2 ports of MFS have the dedicated I/O for I ² C. See the datasheet in detailed. The I ² C is not designed to be hot swappable. CTS/RTS is not mounted (hardware flow control is not supported for this series.) This model does not support Wake Up Function.
CAN-FD	Flexible data rate is supported. 16KB/ch of message RAM is available. The clock output from CAN pre-scaler is supplied to every CAN. ECC error generation function of the message RAM is not supported for this device. Therefore, CAN FD ECC Error Insertion Control Register (FDFECCR) is not writeable.
Real Time Clock (RTC) with auto-calibration	See the Traveo™ Platform Hardware Manual in detailed.
SHE	See the Traveo™ Platform Hardware Manual in detailed.
Source Clock Timer	See the Traveo™ Platform Hardware Manual in detailed.
BUS DIAGNOSIS FUNCTION	The bus diagnosis function prevents an LSI malfunction by checking data that was output on a bus during access to each resource.

2.1. Reset Signal

The following table shows the reset signal of each function.

See the chapter of "Reset" in Traveo™ Platform Hardware Manual for details of reset signal "RSTX_*".

Table 2-2. The Reset Signal of Each Function.

Functions	CHAPTER	Reset signal	Remark
Base Timer	CHAPTER 16	RSTX_PD2	
Base Timer I/O Selection Function	CHAPTER 17	RSTX_PD2	
Base Timer Simultaneous Operation	CHAPTER 18	RSTX_PD2	
32-Bit Free-Run Timer	CHAPTER 19	RSTX_PD2	
32-Bit Input Capture	CHAPTER 20	RSTX_PD2	
32-bit Reload Timer	CHAPTER 21	RSTX_PD2	
I/O Port	CHAPTER 22	RSTX_PD2	for I/O Controller
		RSTX_IO_5V	for I/O
12/10/8-Bit Analog to Digital Converter	CHAPTER 23	RSTX_PD2	for Unit0
		RSTX_PD1	for Unit1
Partial Wakeup Control	CHAPTER 24	RSTX_PD1	
Programmable CRC	CHAPTER 25	RSTX_PD2	
Clock Monitor	CHAPTER 26	RSTX_PD1	
Bus Diagnosis Function	CHAPTER 27	RSTX_PD2	
CAN FD Controller	Traveo™ Platform Hardware Manual	RSTX_PD2	
Multi-function Serial Interface	Traveo™ Platform Hardware Manual	RSTX_PD2	
32-bit Output Compare	Traveo™ Platform Hardware Manual	RSTX_PD2	
QPRC (Quadrature Position/Revolution Counter)	Traveo™ Platform Hardware Manual	RSTX_PD2	

3. Note

3.1. Status Flag Clear

Note that the hardware operation of a write access to a register which has status flags may be later than program operations of software. The delay results from the fact that the write accesses and their signals are operated through multiple buses.

For example, when a software program intends to return from interrupt software routine (ISR) after clearing the interrupt flag, the return instruction may practically be executed before the completion of the write access as for hardware operation. That is, the CPU execution may immediately jump to the ISR again after returning from the ISR because the flag is not cleared.

To avoid such a phenomenon, the execution of Data Memory Barrier (DMB) instruction between the write access and the return instruction is recommended for the program. The return instruction is never executed before the completion of DMB execution.

It should be considered that the method takes a number of execution cycles and that it may cause some influence to application performance. For example, one time of the DMB execution is enough after a number of continuous flag clear operations.

3.2. Error Response

Error response is generated when access occurs to the following register and bit offset.

Function	Register	Bit Offset	Access	Error Type
12/10/8-BIT ANALOG TO DIGITAL CONVERTER	ADC12Bn_CHSTAT0 to 31	Whole register	Write(B,H,W)	Bus error
	ADC12Bn_CD0 to 31	Whole register	Write(B,H,W)	Bus error
	ADC12Bn_CDONEIRQ0	Whole register	Write(B,H,W)	Bus error
	ADC12Bn_GRPIRQ0	Whole register	Write(B,H,W)	Bus error
	ADC12Bn_RCIRQ0	Whole register	Write(B,H,W)	Bus error
	ADC12Bn_PCIRQ0	Whole register	Write(B,H,W)	Bus error
	ADC12Bn_TRGST0	Whole register	Write(B,H,W)	Bus error
	ADC12Bn_RCOTF0	Whole register	Write(B,H,W)	Bus error
	ADC12Bn_TRGOR0	Whole register	Write(B,H,W)	Bus error
	ADC12Bn_MCSTAT0 to 3	Whole register	Write(B,H,W)	Bus error
	(Other reserved area)	(Other reserved area)	Read / Write(B,H,W)	Bus error

3.3. Register Initial Value

The table shows initial value of Register bit which is uniquely specified for the product series.

Register	Bit	Initial Value	Description
SYSC0_APPLVDCFGR	LVDL1S	0	-
SYSC0_APPLVDCFGR	LVDL1V	000	-
SYSC0_APPLVDCFGR	LVDL1E	1	-
SYSC0_APPLVDCFGR	Bit22	0	-

Register	Bit	Initial Value	Description
SYSC0_APPLVDCFGR	Bit19 to Bit17	000	-
SYSC0_APPLVDCFGR	Bit16	0	-
SYSC0_APPLVDCFGR	LVDH1S	0	LVDH1 need to be used as Reset function. LVDH1S must not be changed by Initial value.
SYSC0_APPLVDCFGR	LVDH1V	111	-
SYSC0_APPLVDCFGR	LVDH1E	1	-
SYSC0_APPLVDCFGR	LVDH2S	0	-
SYSC0_APPLVDCFGR	LVDH2V	000	-
SYSC0_APPLVDCFGR	LVDH2E	0	-
SYSC0_STSLVDCFGR	LVDL1R	1	-
SYSC0_STSLVDCFGR	LVDL1S	0	-
SYSC0_STSLVDCFGR	LVDL1V	000	-
SYSC0_STSLVDCFGR	LVDL1E	1	-
SYSC0_STSLVDCFGR	Bit23	0	-
SYSC0_STSLVDCFGR	Bit22	0	-
SYSC0_STSLVDCFGR	Bit19 to Bit17	000	-
SYSC0_STSLVDCFGR	Bit16	0	-
SYSC0_STSLVDCFGR	LVDH1R	1	-
SYSC0_STSLVDCFGR	LVDH1S	0	LVDH1 need to be used as Reset function. LVDH1S must not be changed by Initial value.
SYSC0_STSLVDCFGR	LVDH1V	111	-
SYSC0_STSLVDCFGR	LVDH1E	1	-
SYSC0_STSLVDCFGR	LVDH2R	0	-
SYSC0_STSLVDCFGR	LVDH2S	0	-
SYSC0_STSLVDCFGR	LVDH2V	000	-
SYSC0_STSLVDCFGR	LVDH2E	0	-
SYSC0_PSSLVDCFGR	LVDL1S	0	1 should be written only if LVDL1V is changed from initial value.
SYSC0_PSSLVDCFGR	LVDL1V	000	-
SYSC0_PSSLVDCFGR	LVDL1E	1	-
SYSC0_PSSLVDCFGR	Bit22	0	Reserved
SYSC0_PSSLVDCFGR	Bit19 to Bit17	000	Reserved
SYSC0_PSSLVDCFGR	Bit16	0	Reserved
SYSC0_PSSLVDCFGR	LVDH1S	0	LVDH1 need to be used as Reset function. LVDH1S must not be changed by Initial value.
SYSC0_PSSLVDCFGR	LVDH1V	111	-
SYSC0_PSSLVDCFGR	LVDH1E	1	-
SYSC0_PSSLVDCFGR	LVDH2S	0	Reserved
SYSC0_PSSLVDCFGR	LVDH2V	000	Reserved
SYSC0_PSSLVDCFGR	LVDH2E	0	Reserved
SYSC0_RUNLVDCFGR	LVDL1S	0	1 should be written only if LVDL1V is changed from initial value.
SYSC0_RUNLVDCFGR	LVDL1V	000	-
SYSC0_RUNLVDCFGR	LVDL1E	1	-
SYSC0_RUNLVDCFGR	Bit22	0	Reserved
SYSC0_RUNLVDCFGR	Bit19 to Bit17	000	Reserved

Register	Bit	Initial Value	Description
SYSC0_RUNLVDCFGR	Bit16	0	Reserved
SYSC0_RUNLVDCFGR	LVDH1S	0	LVDH1 need to be used as Reset function. LVDH1S must not be changed by Initial value
SYSC0_RUNLVDCFGR	LVDH1V	111	-
SYSC0_RUNLVDCFGR	LVDH1E	1	-
SYSC0_RUNLVDCFGR	LVDH2S	0	Reserved
SYSC0_RUNLVDCFGR	LVDH2V	000	Reserved
SYSC0_RUNLVDCFGR	LVDH2E	0	Reserved
SYSC0_SPESPSWCFGR0	-	0x00000000	Writing doesn't affect anything.
SYSC0_SPESPSWCFGR1	-	0x11000001	Writing doesn't affect anything.
SYSC0_SPEWPSWCFGR0	-	0x00000000	Writing doesn't affect anything.
SYSC0_SPEWPSWCFGR1	-	0x11000001	Writing doesn't affect anything.

Notes:

- SYSC0_SPESPSWCFGR0 and 1, and SYSC0_SPEWPSWCFGR0 and 1 are not software configurable registers but hardware specific registers for the system.

3.4. Restriction

Function	Related Register and Configuration	Restriction	Remark
Interrupt Controller	IRC0_IRQS8 to IRC0_IRQS15 IRC0_IRQR8 to IRC0_IRQR15 IRC0_IRQSIS8 to IRC0_IRQSIS15 IRC0_IRQCES8 to IRC0_IRQCES15 IRC0_IRQCEC8 to IRC0_IRQCEC15 IRC0_IRQCE8 to IRC0_IRQCE15 IRC0_IRQHS8 to IRC0_IRQHS15 IRC0_IRQRS8 to IRC0_IRQRS15 IRC0_IRQPS8 to IRC0_IRQPS15	Not support these registers because 256 interrupt vectors.	-
Profile update	System Status Register (SYSC0_SYSSTS) PSSSTS0 bit RUNSTS0 bit PSSDF0 bit RUNDFO bit	Before profile update, confirm the status is not updating by STS0 bit. After profile update, confirm the profile update completion by DF0 bit and the software go ahead with next handling.	-
Low Power Consumption	MCG_IRSR0 IRQ_PW bit	This model does not support IRQ_PW bit in MCG_IRSR0 register. This bit is always read to 0.	-
	SYSC0_STSLVDCFGR LVDH1S bit	Set SYSC0_STSLVDCFGR.LVDH1S = 0. LVDH1 need to be used as Reset function.	-
	SYSC0_SPECFGR EXVRSTCNT bit	Set SYSC0_SPECFGR.EXVRSTCNT = 0. External power supply control need to be reset by LVDH1.	-

Function	Related Register and Configuration	Restriction	Remark
Low Power Consumption	SYSC0_PSSCKSRER	Do not disable FastCR (4MHz) in PSS mode (PD2: ON/OFF). If FastCR disable, please see the "5. Precautions for Using this Device" of chapter 24.	-
Main clock division	SYSC_MOSCCNTR DIV2SEL bit	Set SYSC_MOSCCNTR.DIV2SEL=1. Main clock pulse that is no division in chip deforms easily by noise. It causes running out of control.	-
Main clock fast clock input enable	SYSC_MOSCCNTR FCIMEN bit	Set SYSC_MOSCCNTR.FCIMEN=0. Main clock needs setting to 0 to oscillate.	-
Reset	-	All RAM data (include TCRAM, System RAM, Backup RAM) are not guaranteed after release of RSTX pin input reset.	-
	SYSC_RSTCAUSEUR SWDR bit	SWDR (Software Watchdog Reset Detection) flag of SYSC_RSTCAUSEUR (User Reset Factor Register) is set when a reset from one of the following reset is asserted in PSS mode (PD2:OFF).. In this case please ignore SWDR = 1. - RAM retention low-voltage detection reset (RVD) - INITX (INITX) - Illegal mode detection reset (IMR) - Internal power supply low-voltage detection reset (LVDL1R) - External power supply low-voltage detection reset (LVDH1R) - Hardware watchdog reset (HWDR)	-
Clock system	SYSC_CKOTCNTR CKSEL bit	Do not set SYSC_CKOTCNTR.CKSEL[3:0] = 0011. Sub clock do not use to the source clocks.	-
Partial Wakeup Control	-	This function have restriction. Please see the "5. Precautions for Using this Device" of chapter 24.	-
Real Time Clock	-	All RTC registers are not initialized by RSTX(external reset), and there are possibilities that the RTC registers are overwritten. The RTC registers need setting after release of RSTX again.	-

Function	Related Register and Configuration	Restriction	Remark
Security	TCFCFG0_CSWP0.SWP0 to SWP31 bit TCFCFG0_CSWP1to8.SWP0 to SWP31 bit	In order to write successfully any sector of Code Flash, all Sectors must have their SWP (TCFCFG0_CSWP0.SWP0 to SWP31 , TCFCFG0_CSWP1.SWP0 to SWP31) set to 1.	-

CHAPTER 4: Block Diagram



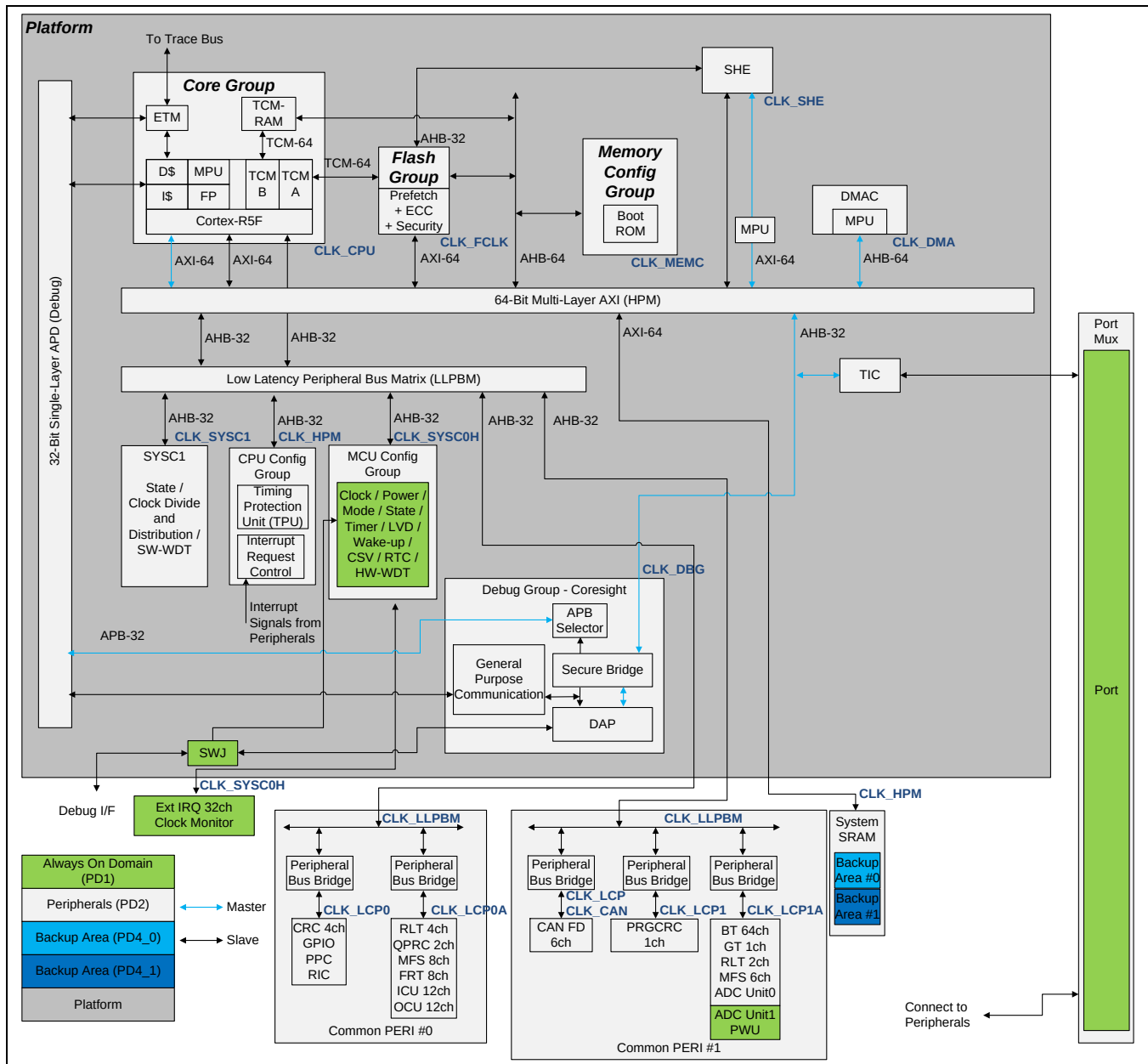
This chapter explains the block diagram.

1. Block diagram
2. Note

CODE: BLOCK_DIAGRAM-S6J3400-E1

1. Block Diagram

Figure 1-1



2. Note

No description.

CHAPTER 5: Clock Configuration



This chapter explains the clock configuration.

1. Overview
2. Operation
3. Remark

CODE: CLOCKCFG-S6J3400-E1.1

1. Overview

This chapter describes clock selection and configuration of each function.

See the chapter of the “Clock System” in Traveo™ Platform Hardware Manual before referring this chapter.

2. Operation

The source clock of each function should be selected as following table.

Table 2-1. Clock Function

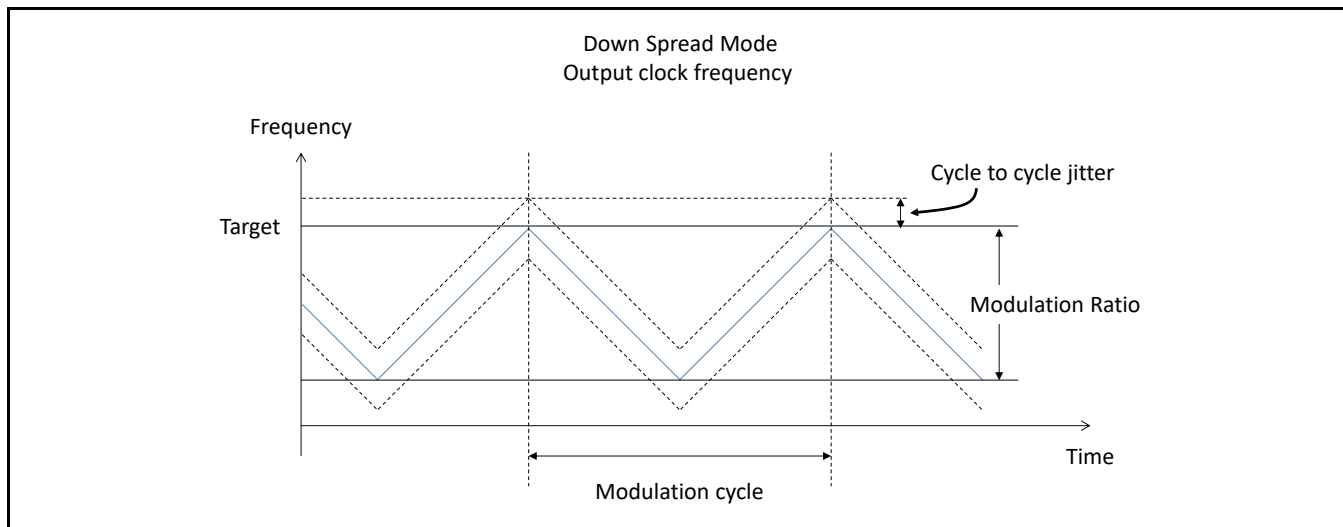
Function	Clock Name	Source Clock System	Configuration
CPU	CLK_CPU	SSCG0	See Traveo™ Platform Hardware Manual
FLASH	CLK_FCLK	SSCG0	See Traveo™ Platform Hardware Manual
HPM	CLK_HPM	SSCG0	See Traveo™ Platform Hardware Manual
DMA	CLK_DMA	SSCG0	See Traveo™ Platform Hardware Manual
LLPBM	CLK_LLPCM	SSCG0	See Traveo™ Platform Hardware Manual
MCU configuration	CLK_SYSC0H CLK_COMH	SSCG0	See Traveo™ Platform Hardware Manual
CAN	CLK_CAN	PLL0	See Traveo™ Platform Hardware Manual
CoreSight	CLK_TRC	PLL0	See Traveo™ Platform Hardware Manual
Hardware watchdog timer	CLK_HWWDT	Internal CR oscillator (High frequency)	See Traveo™ Platform Hardware Manual
		Internal CR oscillator (Low frequency)	See Traveo™ Platform Hardware Manual
Software watchdog timer	CLK_SWWDT	Main clock	See Traveo™ Platform Hardware Manual
		Sub clock	See Traveo™ Platform Hardware Manual
		Internal CR oscillator (High frequency)	See Traveo™ Platform Hardware Manual
		Internal CR oscillator (Low frequency)	See Traveo™ Platform Hardware Manual
Real time clock	CLK_RTC	Main clock	See Traveo™ Platform Hardware Manual
		Sub clock	See Traveo™ Platform Hardware Manual
		Internal CR oscillator (Low frequency)	See Traveo™ Platform Hardware Manual
CRC, GPIO, PPC, RIC in Common PERI #0	CLK_LCP0	SSCG0	See Traveo™ Platform Hardware Manual
RLT, QPRC, MFS, FRT, ICU, OCU in Common PERI #0	CLK_LCP0A	SSCG0	See Traveo™ Platform Hardware Manual
		PLL0	See Traveo™ Platform Hardware Manual
PRGCRC in Common PERI #1	CLK_LCP1	SSCG0	See Traveo™ Platform Hardware Manual
BT, GT, RLT, MFS, ADC in Common PERI #1	CLK_LCP1A	SSCG0	See Traveo™ Platform Hardware Manual
		PLL0	See Traveo™ Platform Hardware Manual

2.1. Spread Spectrum Clock Generator (SSCG)

Target frequency of SSCG should be referred in Datasheet.

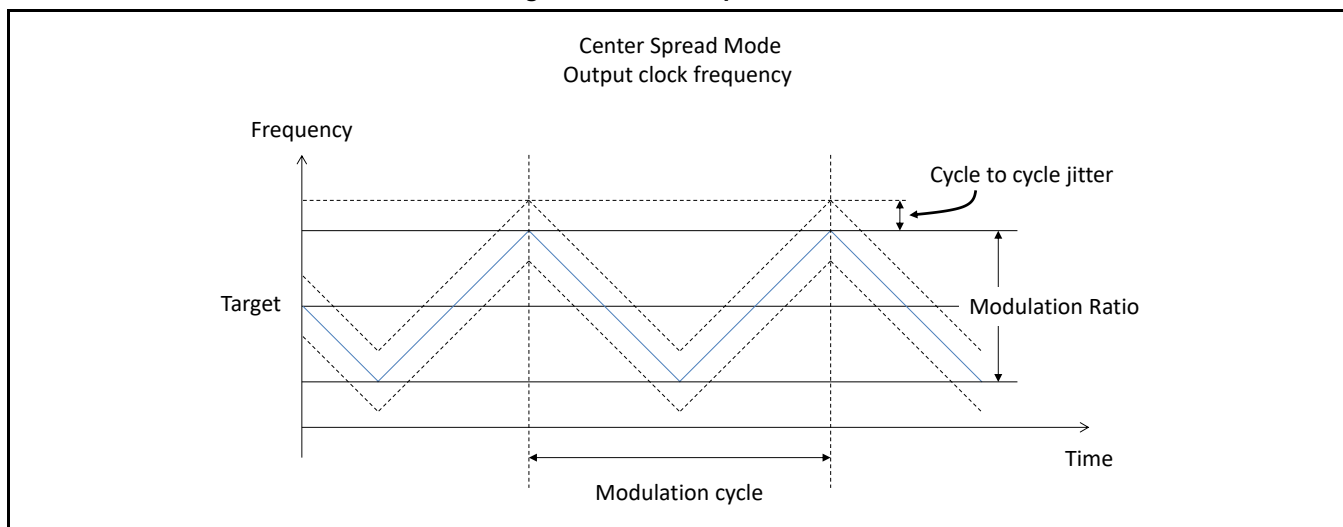
Down Spread Mode

Figure 2-1 Down Spread Mode



Center Spread Mode

Figure 2-2 Center Spread Mode



3. Remark

See the “Clock System” in Traveo™ Platform Hardware Manual before referring this chapter.

Notes:

- If you want to know a combination of a peripheral function and its source clock, you need to see the group name from the table of base address map on this manual at first.
- The group name and its clock source are described in the chapter of “Platform Overview” Configuration and “Clock System”. See Traveo™ Platform Hardware Manual.
- Clock frequency can be seen in datasheet of S6J3400 series.
- Each clock need to keep the specific ratio for CLK_CPU as following table.
- In case of CLK_LCP0A and CLK_LCP1A with PLL0, not need to keep this specific ratio between CLK_CPU and CLK_LCP0A, CLK_LCP1A.

The table shows the possible setting for CLK_CPU = 132 MHz, 80 MHz, 40 MHz.

Table 2-2. Clock CPU Setting

Clock	CLK_CPU : CLOCK		
	≤ 132MHz	≤ 80MHz	≤ 40MHz
CLK_FCLK	1:2n	1:n	1:n
CLK_LCP			
CLK_ATB			
CLK_DBG			
CLK_HPM/DMA/MEMC/SHE	1:4n	1:2n	
CLK_SYS1			
CLK_LCP0			
CLK_LCP0A			
CLK_LCP1			
CLK_LCP1A			
CLK_SYSC0H/COMH			

n: Same divide number

Table 2-3. Clock CPU Setting

	CLK_CPU = 132 MHz		CLK_CPU = 80 MHz		CLK_CPU = 40 MHz		
	n=1	n=2	n=1	n=2	n=1	n=2	n=4
CLK_FCLK	66 MHz	33 MHz	80 MHz	40 MHz	40 MHz	20 MHz	10 MHz
CLK_LCP	66 MHz	33 MHz	80 MHz	40 MHz	40 MHz	20 MHz	10 MHz
CLK_ATB	66 MHz	33 MHz	40 MHz	20 MHz	40 MHz	20 MHz	10 MHz
CLK_DBG	66 MHz	33 MHz	40 MHz	20 MHz	40 MHz	20 MHz	10 MHz
CLK_HPM/DMA/MEMC/SHE	33 MHz	16.5 MHz	40 MHz	20 MHz	40 MHz	20 MHz	10 MHz
CLK_SYS1	33 MHz	16.5 MHz	40 MHz	20 MHz	40 MHz	20 MHz	10 MHz
CLK_LCP0	33 MHz	16.5 MHz	40 MHz	20 MHz	40 MHz	20 MHz	10 MHz
CLK_LCP0A	33 MHz	16.5 MHz	40 MHz	20 MHz	40 MHz	20 MHz	10 MHz
CLK_LCP1	33 MHz	16.5 MHz	40 MHz	20 MHz	40 MHz	20 MHz	10 MHz
CLK_LCP1A	33 MHz	16.5 MHz	40 MHz	20 MHz	40 MHz	20 MHz	10 MHz
CLK_SYSC0H/COMH	33 MHz	16.5 MHz	40 MHz	20 MHz	40 MHz	20 MHz	10 MHz

CHAPTER 6: Operation Mode



This chapter explains operation mode.

1. Overview
2. Configuration
3. Registers

CODE: MODE-S6J3400-E1.1

1. Overview

This section gives a description of operation mode.

The mode controller determines the operation mode of MCU. It supports,

- User mode
- Serial programming mode (with synchronous communication)
- Serial programming mode (with asynchronous communication)
- JTAG boundary scan mode

2. Configuration

Operation Mode	PORT		
	MODE	P020(SOT0)	P022(SIN0)
User Mode	1	-	-
Serial Programming Mode (Sync)	0	1	0
Serial Programming Mode (Async)	0	1	1
JTAG Boundary Scan Mode	0	0	0

Note:

- User mode can be applied to Software debugging using JTAG interface with ICE.
- As for serial programming, see the chapter of “Serial Programming” on this manual.

3. Registers

See Traveo™ Platform Hardware Manual.

CHAPTER 7: Memory and Base Address Map



This chapter explains the memory map and the base address map of registers.

1. Overview
2. Memory map
3. Base address map

CODE: MEMORYMAP-S6J3400-E1.3

1. Overview

When MPU attribute of Cortex-R5F is configured as "Normal", store buffer inside Cortex-R5F can operate and write data can be merged. To avoid influence of this data merger, MPU attribute "Device" or "Strongly Ordered" should be used.

MPU attribute "Device" or "Strongly Ordered" must be used for areas below, to avoid this influence.

- Peripheral area [B000_0000 ~ B7FF_FFFF]
- Peripheral area [B800_0000 ~ BFFF_FFFF]
- Error Config area (ERRCFG) [FFFE_E000 ~ FFFE_FFFF]

MPU attribute "Device" or "Strongly Ordered" is required for accesses to areas below, in particular situation.

- FLASH Memory (when writing commands)

2. Memory Map

START Address	END Address	Group	Part
0000_0000	0000_FFFF	Internal area for CR5 Complex	TCRAM 64KB@Max
0001_0000	007F_FFFF		Reserved
0080_0000	009E_FFFF		Reserved
009F_0000	009F_FFFF		TCFLASH 64KB (Small sector 8KB x 8)
00A0_0000	00AF_FFFF		TCFLASH 1MB@Max
00B0_0000	00FF_FFFF		Reserved
0100_0000	019E_FFFF		Reserved
019F_0000	019F_FFFF		AXI_FLASH 64KB (Small sector 8KB x 8)
01A0_0000	01AF_FFFF		AXI_FLASH 1MB@Max
01B0_0000	01FF_FFFF		Reserved
0200_0000	0200_FFFF	Shared Flash and memory area	System SRAM 64KB@Max
0201_0000	027F_FFFF		Reserved
0280_0000	0280_0FFF		Reserved
0280_1000	03FF_FFFF		Reserved
0400_0000	05FF_FFFF		AXI_SLAVE_CORE0
0600_0000	07FF_FFFF		Reserved
0800_0000	09FF_FFFF		Reserved
0A00_0000	0BFF_FFFF		Reserved
0C00_0000	0DFF_FFFF		Reserved
0E00_0000	0E01_BFFF		WORK_FLASH 112KB (mirror area 1)
0E01_C000	0E1F_FFFF		Reserved
0E20_0000	0E21_BFFF		WORK_FLASH 112KB (mirror area 3)
0E21_C000	0E2F_FFFF		Reserved
0E30_0000	0E31_BFFF		WORK_FLASH 112KB (mirror area 4)
0E31_C000	0E3F_FFFF		Reserved
0E40_0000	0E7F_FFFF		Reserved
0E80_0000	0E80_FFFF		System SRAM 64KB@Max (mirror) (Covers 0200_0000 -- 0200_FFFF)
0E81_0000	0EFF_FFFF		Reserved
0F00_0000	0FFF_FFFF		Reserved
1000_0000	1FFF_FFFF	Reserved	Reserved
2000_0000	2FFF_FFFF	Reserved	Reserved
3000_0000	3FFF_FFFF	Reserved	Reserved
4000_0000	4FFF_FFFF	Reserved	Reserved
5000_0000	501F_FFFF	Reserved	Reserved
5020_0000	5020_03FF	Reserved	Reserved
5020_0400	5020_3FFF	Reserved	Reserved
5020_4000	5020_43FF	Reserved	Reserved
5020_4400	5021_3FFF	Reserved	Reserved
5021_4000	5021_43FF	Reserved	Reserved
5021_4400	5021_47FF	Reserved	Reserved
5021_4800	503F_FFFF	Reserved	Reserved

START Address	END Address	Group	Part
5040_0000	504F_FFFF	Reserved	Reserved
5050_0000	5FFF_FFFF	Reserved	Reserved
6000_0000	7FFF_FFFF	Reserved	Reserved
8000_0000	8FFF_FFFF	Reserved	Reserved
9000_0000	9FFF_FFFF	Reserved	Reserved
A000_0000	A010_7FFF	Reserved	Reserved
A010_8000	A010_80FF	System SRAM	System SRAM registers (mirror)
A010_8100	A041_1FFF	Reserved	Reserved
A041_2000	A041_20FF	MEM Config Group	Wflash Control Status Register (mirror)
A041_2100	A118_FFFF	Reserved	Reserved
A119_0000	A11F_FFFF	Bit RMW alias	Bit RMW alias for MEMC (mirror) (Covers B041_2000 -- B041_FFFF)
A120_0000	AFFF_FFFF	Reserved	Reserved
B000_0000	B7FF_FFFF	Peripheral area	Peripheral area
B800_0000	B802_87FF	Peripheral area	Peripheral area
B802_8800	BFFF_FFFF	Reserved	Reserved
C000_0000	EFFF_FFFF	Reserved	Reserved
F000_0000	FFFE_DFFF	BootROM/ERRCFG area	Reserved
FFFE_E000	FFFE_EFFF		ERRCFG
FFFE_F000	FFFE_FFFF		ERRCFG
FFFF_0000	FFFF_FFFF		BootROM

Memory Map of System SRAM

Part Number	Backup Area (PD4_0)		Backup Area (PD4_1)		Non backup Area (PD2)		Remarks
	START Address	END Address	START Address	END Address	START Address	END Address	
S6J34x8xxA	0200_0000	0200_1FFF	0200_2000	0200_2FFF	0200_3000	0200_7FFF	32KB
S6J34x9xxA	0200_0000	0200_1FFF	0200_2000	0200_2FFF	0200_3000	0200_BFFF	48KB
S6J34xAxxA	0200_0000	0200_1FFF	0200_2000	0200_2FFF	0200_3000	0200_FFFF	64KB

Memory Map of TCRAM

Part Number	START Address	END Address	Remarks
S6J34x8xxA	0000_0000	0000_7FFF	32KB
S6J34x9xxA	0000_0000	0000_7FFF	32KB
S6J34xAxxA	0000_0000	0000_FFFF	64KB

3. Base Address Map

An address of a certain register can be specified as below.

- Base address

Look for the base address X of the function from the base address map below.

- Offset address

Look for the offset address Y of the register from the offset address list which is described in the chapter of the function. Each function chapter has offset address list or its information.

- Specify

The register address can be specified as $X + Y$.

Note:

- Address area of not-implemented function is not supported. See the chapter of function list.

START Address	END Address	Group	Function	PPU_No
B000_0000	B00F_FFFF	Reserved	Reserved	-
B010_0000	B010_03FF	Reserved	Reserved	-
B010_0400	B010_0FFF	Reserved	Reserved	-
B010_1000	B010_13FF	Reserved	Reserved	-
B010_1400	B010_7FFF	Reserved	Reserved	-
B010_8000	B010_80FF	System SRAM	System SRAM registers	2
B010_8100	B01F_FFFF	Reserved	Reserved	-
B020_0000	B02F_FFFF	Reserved	Reserved	-
B030_0000	B030_7FFF	SYSC1	System Controller #1	4
B030_8000	B03F_FFFF	SYSC1	SWDT	5
B040_0000	B040_7FFF	CPU Config Group	IRC0	21
B040_8000	B040_FFFF	CPU Config Group	TPU0	19
B041_0000	B041_0FFF	CPU Config Group	TCRAM Control Status Register	16
B041_1000	B041_1FFF	CPU Config Group	TCFlash Control Status Register	17
B041_2000	B041_20FF	MEM Config Group	Wflash Control Status Register	18
B041_2100	B04F_FFFF	Reserved	Reserved	-
B050_0000	B050_0FFF	Debug Group	DAP ROM table	-
B050_1000	B050_1FFF	Debug Group	ETB	-
B050_2000	B050_2FFF	Debug Group	CTI #4	-
B050_3000	B050_3FFF	Debug Group	TPIU	-
B050_4000	B057_FFFF	Debug Group	TRACE FUNNEL	-
B058_0000	B058_FFFF	Debug Group	CR5_RomTable	-
B059_0000	B059_1FFF	Debug Group	CORE0	-
B059_2000	B059_7FFF	Reserved	Reserved	-
B059_8000	B059_8FFF	Debug Group	CTI #0	-
B059_9000	B059_BFFF	Reserved	Reserved	-
B059_C000	B059_CFFF	Debug Group	ETM0	-
B059_D000	B05B_FFFF	Reserved	Reserved	-

START Address	END Address	Group	Function	PPU_No
B05C_0000		Debug Group	Security Checker	-
	B05F_FFFF	Reserved	Reserved	-
B060_0000	B060_007F	MCU Config Group	Protection register area	51
B060_0080	B060_00FF	MCU Config Group	RUN profile register area	51
B060_0100	B060_017F	MCU Config Group	PSS profile register area	51
B060_0180	B060_01FF	MCU Config Group	APP profile register area	51
B060_0200	B060_027F	MCU Config Group	STS profile register area	51
B060_0280	B060_02FF	MCU Config Group	System register area	51
B060_0300	B060_037F	MCU Config Group	CSV	51
B060_0380	B060_03FF	MCU Config Group	RESET	51
B060_0400	B060_047F	MCU Config Group	SCT (Fast CR)	34
B060_0480	B060_04FF	MCU Config Group	SCT (Slow CR)	33
B060_0500	B060_057F	MCU Config Group	SCT (Main clock)	35
B060_0580	B060_05FF	MCU Config Group	SCT (Sub clock)	36
B060_0600	B060_067F	MCU Config Group	Clock System	51
B060_0680	B060_06FF	MCU Config Group	Special register area	51
B060_0700	B060_07FF	MCU Config Group	Debug register area	51
B060_0800	B060_BFFF	MCU Config Group	MODEC	55
B060_C000	B060_FFFF	MCU Config Group	HWDT	52
B061_0000	B061_7FFF	Reserved	Reserved	-
B061_8000	B061_FFFF	MCU Config Group	RTC	32
B062_0000	B063_FFFF	MCU Config Group	Ext-IRQ	53
B064_0000	B064_0FFF	Reserved	Reserved	-
B064_1000	B064_1FFF	Reserved	Reserved	-
B064_2000	B064_2FFF	Reserved	Reserved	-
B064_3000	B064_3FFF	MCU Config Group	Clock Monitor	-
B064_4000	B065_FFFF	Reserved	Reserved	-
B066_0000	B067_FFFF	Reserved	Reserved	-
B068_0000	B068_7FFF	Reserved	Reserved	-
B068_8000	B068_83FF	Reserved	Reserved	-
B068_8400	B068_87FF	MCU Config Group	CR_CALIBRATION	38
B068_8800	B068_8BFF	MCU Config Group	MCG_IRS	42
B068_8C00	B068_FFFF	MCU Config Group	CAN_PRESCALER	43
B069_0000	B06A_7FFF	Reserved	Reserved	-
B06A_8000	B06B_FFFF	Reserved	Reserved	-
B06C_0000	B06F_FFFF	Reserved	Reserved	-
B070_0000	B07F_FFFF	Reserved	Reserved	-
B080_0000	B0FF_FFFF	Bit RMW alias	Bit RMW alias for MCU Config (Covers B060_0000 -- B06F_FFFF)	-
B100_0000	B10F_FFFF	Bit RMW alias	Bit RMW alias for SYSC1 (Covers B030_0000 -- B031_FFFF)	-
B110_0000	B118_FFFF	Bit RMW alias	Bit RMW alias for CPU Config (Covers B040_0000 -- B041_1FFF)	-

START Address	END Address	Group	Function	PPU_No
B119_0000	B11F_FFFF	Bit RMW alias	Bit RMW alias for MEMC (Covers B041_2000 -- B041_FFFF)	-
B120_0000	B1FF_FFFF	Reserved	Reserved	-
B200_0000	B20F_FFFF	SHE Group	SHE configuration registers (1MB)	63
B210_0000	B3FF_FFFF	Reserved	Reserved	-
B400_0000	B46F_FFFF	Reserved	Reserved	-
B470_0000	B470_3FFF	CPU Config Group	DMAC #0 registers	64
B470_4000	B470_7FFF	Reserved	Reserved	-
B470_8000	B470_FFFF	Reserved	Reserved	-
B471_0000	B471_0FFF	CPU Config Group	MPU for DMAC #0	66
B471_1000	B471_1FFF	Reserved	Reserved	-
B471_2000	B471_3FFF	Reserved	Reserved	-
B471_4000	B471_4FFF	CPU Config Group	DMA Complex #0 registers (Additional registers, RLTs)	68
B471_5000	B471_5FFF	Reserved	Reserved	-
B471_6000	B471_7FFF	Reserved	Reserved	-
B471_8000	B471_83FF	Common PERI #0	CRC #0	70
B471_8400	B471_87FF	Common PERI #0	CRC #1	71
B471_8800	B471_8BFF	Common PERI #0	CRC #2	72
B471_8C00	B471_8FFF	Common PERI #0	CRC #3	73
B471_9000	B471_9FFF	Common PERI #0	Bus Diagnosis	271
B471_A000	B473_7FFF	Reserved	Reserved	-
B473_8000	B473_FFFF	Common PERI #0	GPIO	74
B474_0000	B474_7FFF	Common PERI #0	PPC	75
B474_8000	B474_FFFF	Common PERI #0	RIC	76
B475_0000	B475_7FFF	CPU Config Group	PPU	-
B475_8000	B478_FFFF	Reserved	Reserved	-
B479_0000	B47F_FFFF	Reserved	Reserved	-
B480_0000	B480_03FF	Common PERI #0	M.F.Serial ch.0	176
B480_0400	B480_07FF	Common PERI #0	M.F.Serial ch.1	177
B480_0800	B480_0BFF	Common PERI #0	M.F.Serial ch.2	178
B480_0C00	B480_0FFF	Common PERI #0	M.F.Serial ch.3	179
B480_1000	B480_13FF	Common PERI #0	M.F.Serial ch.4	180
B480_1400	B480_17FF	Common PERI #0	M.F.Serial ch.5	181
B480_1800	B480_1BFF	Common PERI #0	M.F.Serial ch.6	182
B480_1C00	B480_1FFF	Common PERI #0	M.F.Serial ch.7	183
B480_2000	B480_7FFF	Reserved	Reserved	-
B480_8000	B480_83FF	Common PERI #1	Base Timer ch.0	88
B480_8400	B480_87FF	Common PERI #1	Base Timer ch.1	89
B480_8800	B480_8BFF	Common PERI #1	Base Timer ch.2	90
B480_8C00	B480_8FFF	Common PERI #1	Base Timer ch.3	91
B480_9000	B480_93FF	Common PERI #1	Base Timer ch.4	92
B480_9400	B480_97FF	Common PERI #1	Base Timer ch.5	93
B480_9800	B480_9BFF	Common PERI #1	Base Timer ch.6	94

CHAPTER 7:Memory and Base Address Map

START Address	END Address	Group	Function	PPU_No
B480_9C00	B480_9FFF	Common PERI #1	Base Timer ch.7	95
B480_A000	B480_A3FF	Common PERI #1	Base Timer ch.8	96
B480_A400	B480_A7FF	Common PERI #1	Base Timer ch.9	97
B480_A800	B480_ABFF	Common PERI #1	Base Timer ch.10	98
B480_AC00	B480_AFFF	Common PERI #1	Base Timer ch.11	99
B480_B000	B480_FFFF	Reserved	Reserved	-
B481_0000	B481_03FF	Common PERI #0	Reload Timer ch.0	128
B481_0400	B481_07FF	Common PERI #0	Reload Timer ch.1	129
B481_0800	B481_0BFF	Common PERI #0	Reload Timer ch.2	130
B481_0C00	B481_0FFF	Common PERI #0	Reload Timer ch.3	131
B481_1000	B481_7FFF	Reserved	Reserved	-
B481_8000	B481_FFFF	Reserved	Reserved	-
B482_0000	B482_03FF	Common PERI #0	FRT ch.0	208
B482_0400	B482_07FF	Common PERI #0	FRT ch.1	209
B482_0800	B482_0BFF	Common PERI #0	FRT ch.2	210
B482_0C00	B482_0FFF	Common PERI #0	FRT ch.3	211
B482_1000	B482_13FF	Common PERI #0	FRT ch.4	212
B482_1400	B482_7FFF	Reserved	Reserved	-
B482_8000	B482_83FF	Common PERI #0	Input Capture ch.0 / ch.1	224
B482_8400	B482_87FF	Common PERI #0	Input Capture ch.2 / ch.3	225
B482_8800	B482_8BFF	Common PERI #0	Input Capture ch.4 / ch.5	226
B482_8C00	B482_FFFF	Reserved	Reserved	-
B483_0000	B483_03FF	Common PERI #0	Output Compare ch.0 / ch.1	240
B483_0400	B483_07FF	Common PERI #0	Output Compare ch.2 / ch.3	241
B483_0800	B483_0BFF	Common PERI #0	Output Compare ch.4 / ch.5	242
B483_0C00	B483_FBFF	Reserved	Reserved	-
B483_FC00	B483_FFFF	Common PERI #0	Reload Timer Simultaneous Soft Start for ch.0/1/2/3	80
B484_0000	B484_5FFF	Reserved	Reserved	-
B484_6000	B484_63FF	Common PERI #1	Base Timer ch.24	290
B484_6400	B484_67FF	Common PERI #1	Base Timer ch.25	291
B484_6800	B484_6BFF	Common PERI #1	Base Timer ch.26	292
B484_6C00	B484_6FFF	Common PERI #1	Base Timer ch.27	293
B484_7000	B484_73FF	Common PERI #1	Base Timer ch.28	294
B484_7400	B484_77FF	Common PERI #1	Base Timer ch.29	295
B484_7800	B484_7BFF	Common PERI #1	Base Timer ch.30	296
B484_7C00	B484_7FFF	Common PERI #1	Base Timer ch.31	297
B484_8000	B484_83FF	Common PERI #1	Base Timer ch.32	298
B484_8400	B484_87FF	Common PERI #1	Base Timer ch.33	299
B484_8800	B484_8BFF	Common PERI #1	Base Timer ch.34	300
B484_8C00	B484_8FFF	Common PERI #1	Base Timer ch.35	301
B484_9000	B484_93FF	Common PERI #1	Base Timer ch.36	302
B484_9400	B484_97FF	Common PERI #1	Base Timer ch.37	303
B484_9800	B484_9BFF	Common PERI #1	Base Timer ch.38	304

START Address	END Address	Group	Function	PPU_No
B484_9C00	B484_9FFF	Common PERI #1	Base Timer ch.39	305
B484_A000	B484_A3FF	Common PERI #1	Base Timer ch.40	306
B484_A400	B484_A7FF	Common PERI #1	Base Timer ch.41	307
B484_A800	B484_ABFF	Common PERI #1	Base Timer ch.42	308
B484_AC00	B484_AFFF	Common PERI #1	Base Timer ch.43	309
B484_B000	B484_B3FF	Common PERI #1	Base Timer ch.44	310
B484_B400	B484_B7FF	Common PERI #1	Base Timer ch.45	311
B484_B800	B484_BBFF	Common PERI #1	Base Timer ch.46	312
B484_BC00	B484_BFFF	Common PERI #1	Base Timer ch.47	313
B484_C000	B484_C3FF	Common PERI #1	Base Timer ch.48	314
B484_C400	B484_C7FF	Common PERI #1	Base Timer ch.49	315
B484_C800	B484_CBFF	Common PERI #1	Base Timer ch.50	316
B484_CC00	B484_CFFF	Common PERI #1	Base Timer ch.51	317
B484_D000	B484_D3FF	Common PERI #1	Base Timer ch.52	318
B484_D400	B484_D7FF	Common PERI #1	Base Timer ch.53	319
B484_D800	B484_DBFF	Common PERI #1	Base Timer ch.54	320
B484_DC00	B484_DFFF	Common PERI #1	Base Timer ch.55	321
B484_E000	B484_E3FF	Common PERI #1	Base Timer ch.56	322
B484_E400	B484_E7FF	Common PERI #1	Base Timer ch.57	323
B484_E800	B484_EBFF	Common PERI #1	Base Timer ch.58	324
B484_EC00	B484_EFFF	Common PERI #1	Base Timer ch.59	325
B484_F000	B484_F3FF	Common PERI #1	Base Timer ch.60	326
B484_F400	B484_F7FF	Common PERI #1	Base Timer ch.61	327
B484_F800	B484_FBFF	Common PERI #1	Base Timer ch.62	328
B484_FC00	B484_FFFF	Common PERI #1	Base Timer ch.63	329
B485_0000	B485_03FF	Reserved	Reserved	-
B485_0400	B485_07FF	Reserved	Reserved	-
B485_0800	B487_FFFF	Reserved	Reserved	-
B488_0000	B488_03FF	Common PERI #1	M.F.Serial ch.8	184
B488_0400	B488_07FF	Common PERI #1	M.F.Serial ch.9	185
B488_0800	B488_0BFF	Common PERI #1	M.F.Serial ch.10	186
B488_0C00	B488_0FFF	Common PERI #1	M.F.Serial ch.11	187
B488_1000	B488_13FF	Common PERI #1	M.F.Serial ch.12	188
B488_1400	B488_17FF	Common PERI #1	M.F.Serial ch.13	189
B488_1800	B488_7FFF	Reserved	Reserved	-
B488_8000	B488_83FF	Common PERI #1	Base Timer ch.12	100
B488_8400	B488_87FF	Common PERI #1	Base Timer ch.13	101
B488_8800	B488_8BFF	Common PERI #1	Base Timer ch.14	102
B488_8C00	B488_8FFF	Common PERI #1	Base Timer ch.15	103
B488_9000	B488_93FF	Common PERI #1	Base Timer ch.16	104
B488_9400	B488_97FF	Common PERI #1	Base Timer ch.17	105
B488_9800	B488_9BFF	Common PERI #1	Base Timer ch.18	106
B488_9C00	B488_9FFF	Common PERI #1	Base Timer ch.19	107

START Address	END Address	Group	Function	PPU_No
B488_A000	B488_A3FF	Common PERI #1	Base Timer ch.20	108
B488_A400	B488_A7FF	Common PERI #1	Base Timer ch.21	109
B488_A800	B488_ABFF	Common PERI #1	Base Timer ch.22	110
B488_AC00	B488_AFFF	Common PERI #1	Base Timer ch.23	111
B488_B000	B488_B3FF	Common PERI #1	Global Timer	334
B488_B400	B488_FFFF	Reserved	Reserved	-
B489_0000	B489_03FF	Common PERI #1	Reload Timer ch.16	144
B489_0400	B489_07FF	Common PERI #1	Reload Timer ch.17	145
B489_0800	B489_7FFF	Reserved	Reserved	-
B489_8000	B489_83FF	Common PERI #0	QPRC ch.8	200
B489_8400	B489_87FF	Common PERI #0	QPRC ch.9	201
B489_8800	B489_FFFF	Reserved	Reserved	-
B48A_0000	B48A_03FF	Common PERI #0	FRT ch.8	216
B48A_0400	B48A_07FF	Common PERI #0	FRT ch.9	217
B48A_0800	B48A_0BFF	Common PERI #0	FRT ch.10	218
B48A_0C00	B48A_7FFF	Reserved	Reserved	-
B48A_8000	B48A_83FF	Common PERI #0	Input Capture ch.16 / ch.17	232
B48A_8400	B48A_87FF	Common PERI #0	Input Capture ch.18 / ch.19	233
B48A_8800	B48A_8BFF	Common PERI #0	Input Capture ch.20 / ch.21	234
B48A_8C00	B48A_FFFF	Reserved	Reserved	-
B48B_0000	B48B_03FF	Common PERI #0	Output Compare ch.16 / ch.17	248
B48B_0400	B48B_07FF	Common PERI #0	Output Compare ch.18 / ch.19	249
B48B_0800	B48B_0BFF	Common PERI #0	Output Compare ch.20 / ch.21	250
B48B_0C00	B48B_FBFF	Reserved	Reserved	-
B48B_FC00	B48B_FFFF	Common PERI #1	Reload Timer Simultaneous Soft Start for ch.16/17	81
B48C_0000	B48C_03FF	Common PERI #1	ADC12B0	330
B48C_0400	B48C_07FF	Common PERI #1	ADC12B1	331
B48C_0800	B48C_0BFF	Common PERI #1	Partial Wake Up	332
B48C_0C00	B48C_5FFF	Reserved	Reserved	-
B48C_6000	B48C_FFFF	Reserved	Reserved	-
B48D_0000	B48D_FFFF	Reserved	Reserved	-
B48E_0000	B48F_FFFF	Reserved	Reserved	-
B490_0000	B490_FFFF	Common PERI #1	CAN_FD ch.0	256
B491_0000	B491_FFFF	Common PERI #1	CAN_FD ch.1	257
B492_0000	B492_FFFF	Common PERI #1	CAN_FD ch.2	258
B493_0000	B493_FFFF	Common PERI #1	CAN_FD ch.3	259
B494_0000	B494_FFFF	Common PERI #1	CAN_FD ch.4	260
B495_0000	B495_FFFF	Common PERI #1	CAN_FD ch.8	333
B496_0000	B497_FFFF	Reserved	Reserved	-
B498_0000	B4BF_FFFF	Reserved	Reserved	-
B4C0_0000	B4FF_FFFF	Bit RMW alias	Bit RMW alias for Common PERI #1 (Covers B490_0000 -- B497_FFFF)	-
B500_0000	B5FF_FFFF	Reserved	Reserved	-

START Address	END Address	Group	Function	PPU_No
B600_0000	B6FF_FFFF	Reserved	Reserved	-
B700_0000	B70B_FFFF	Bit RMW alias	Bit RMW alias for CPU Config Group (Covers B470_0000 -- B471_7FFF)	-
B70C_0000	B727_FFFF	Bit RMW alias	Bit RMW alias for Common PERI #0 (Covers B471_8000 -- B474_FFFF)	-
B728_0000	B747_FFFF	Bit RMW alias	Bit RMW alias for CPU Config Group (Covers B475_0000 -- B478_FFFF)	-
B748_0000	B77F_FFFF	Bit RMW alias	Bit RMW alias for Common PERI #0 (Covers B479_0000 -- B47F_FFFF)	-
B780_0000	B783_FFFF	Bit RMW alias	Bit RMW alias for Common PERI #0 (Covers B480_0000 -- B480_7FFF)	-
B784_0000	B787_FFFF	Bit RMW alias	Bit RMW alias for Common PERI #1 (Covers B480_8000 -- B480_FFFF)	-
B788_0000	B7A2_FFFF	Bit RMW alias	Bit RMW alias for Common PERI #0 (Covers B481_0000 -- B484_5FFF)	-
B7A3_0000	B7A8_1FFF	Bit RMW alias	Bit RMW alias for Common PERI #1 (Covers B484_6000 -- B485_03FF)	-
B7A8_2000	B7BF_FFFF	Bit RMW alias	Bit RMW alias for Common PERI #0 (Covers B485_0400 -- B487_FFFF)	-
B7C0_0000	B7CB_FFFF	Bit RMW alias	Bit RMW alias for Common PERI #1 (Covers B488_0000 -- B489_7FFF)	-
B7CC_0000	B7DF_DFFF	Bit RMW alias	Bit RMW alias for Common PERI #0 (Covers B489_8000 -- B48B_FBFF)	-
B7DF_E000	B7FF_FFFF	Bit RMW alias	Bit RMW alias for Common PERI #1 (Covers B48B_FC00 -- B48F_FFFF)	-
B800_0000	B801_7FFF	Reserved	Reserved	-
B801_8000	B801_83FF	Common PERI #1	PRGCRC	356
B801_8400	BFFF_FFFF	Reserved	Reserved	-
C000_0000	FFFE_DFFF	Reserved	Reserved	-
FFFE_E000	FFFE_E3FF	ERRCFG	IRC0 (IRC0_NMIVASBR)	-
FFFE_E400	FFFE_F7FF	Reserved	Reserved	-
FFFE_F800	FFFE_FBFF	ERRCFG	IRC (IRC_NMIVASBR) Mirror *	-
FFFE_FC00	FFFE_FFFF	ERRCFG	BootROM I/F	20

CHAPTER 8: IRQ Map / NMI Map



This chapter explains IRQ Map and NMI Map .

1. IRQ Map
2. NMI Map

CODE: IRQMAP-S6J3400-E1.1

1. IRQ Map

This section shows list of interrupt vector.

This list shows the assignments of interrupt vectors / interrupt control registers.

IRQ No.	Detail	IRQ Priority Register	Vector Address Register
0	Reserved		
1	System Control Status	IRC0_IRQPL0 : IRQPL1	IRC0_IRQVA1
2	HW-WDT Pre-warning	IRC0_IRQPL0 : IRQPL2	IRC0_IRQVA2
3	SW-WDT Pre-warning	IRC0_IRQPL0 : IRQPL3	IRC0_IRQVA3
4 to 7	Reserved		
8	TCFLASH RDY, Hang up, Single Bit Error	IRC0_IRQPL2 : IRQPL8	IRC0_IRQVA8
9	Reserved		
10	Work FLASH Hang up	IRC0_IRQPL2 : IRQPL10	IRC0_IRQVA10
11 to 13	Reserved		
14	System SRAM Single Bit Error(include backup area)	IRC0_IRQPL3 : IRQPL14	IRC0_IRQVA14
15	CAN FD RAM(ch.0 to ch.4, ch.8) Single Bit Error	IRC0_IRQPL3 : IRQPL15	IRC0_IRQVA15
16	IRC Vector Address RAM Single Bit Error	IRC0_IRQPL4 : IRQPL16	IRC0_IRQVA16
17 to 19	Reserved		
20	Work FLASH RDY, Write Enable Release, Single Bit Error	IRC0_IRQPL5 : IRQPL20	IRC0_IRQVA20
21 to 23	Reserved		
24	External Interrupt Request ch.0 / ch.16	IRC0_IRQPL6 : IRQPL24	IRC0_IRQVA24
25	External Interrupt Request ch.1 / ch.17	IRC0_IRQPL6 : IRQPL25	IRC0_IRQVA25
26	External Interrupt Request ch.2 / ch.18	IRC0_IRQPL6 : IRQPL26	IRC0_IRQVA26
27	External Interrupt Request ch.3 / ch.19	IRC0_IRQPL6 : IRQPL27	IRC0_IRQVA27
28	External Interrupt Request ch.4 / ch.20	IRC0_IRQPL7 : IRQPL28	IRC0_IRQVA28
29	External Interrupt Request ch.5 / ch.21	IRC0_IRQPL7 : IRQPL29	IRC0_IRQVA29
30	External Interrupt Request ch.6 / ch.22	IRC0_IRQPL7 : IRQPL30	IRC0_IRQVA30
31	External Interrupt Request ch.7 / ch.23	IRC0_IRQPL7 : IRQPL31	IRC0_IRQVA31
32	External Interrupt Request ch.8 / ch.24	IRC0_IRQPL8 : IRQPL32	IRC0_IRQVA32
33	External Interrupt Request ch.9 / ch.25	IRC0_IRQPL8 : IRQPL33	IRC0_IRQVA33
34	External Interrupt Request ch.10 / ch.26	IRC0_IRQPL8 : IRQPL34	IRC0_IRQVA34
35	External Interrupt Request ch.11 / ch.27	IRC0_IRQPL8 : IRQPL35	IRC0_IRQVA35
36	External Interrupt Request ch.12 / ch.28	IRC0_IRQPL9 : IRQPL36	IRC0_IRQVA36
37	External Interrupt Request ch.13 / ch.29	IRC0_IRQPL9 : IRQPL37	IRC0_IRQVA37
38	External Interrupt Request ch.14 / ch.30	IRC0_IRQPL9 : IRQPL38	IRC0_IRQVA38
39	External Interrupt Request ch.15 / ch.31	IRC0_IRQPL9 : IRQPL39	IRC0_IRQVA39
40	CAN FD ch.0 (OR-ed of all factors)	IRC0_IRQPL10 : IRQPL40	IRC0_IRQVA40
41	CAN FD ch.1 (OR-ed of all factors)	IRC0_IRQPL10 : IRQPL41	IRC0_IRQVA41
42	CAN FD ch.2 (OR-ed of all factors)	IRC0_IRQPL10 : IRQPL42	IRC0_IRQVA42
43	CAN FD ch.3 (OR-ed of all factors)	IRC0_IRQPL10 : IRQPL43	IRC0_IRQVA43
44	CAN FD ch.4 (OR-ed of all factors)	IRC0_IRQPL11 : IRQPL44	IRC0_IRQVA44
45	CAN FD ch.8 (OR-ed of all factors)	IRC0_IRQPL11 : IRQPL45	IRC0_IRQVA45
46	MFS RX ch.0	IRC0_IRQPL11 : IRQPL46	IRC0_IRQVA46

IRQ No.	Detail	IRQ Priority Register	Vector Address Register
47	MFS TX ch.0	IRC0_IRQPL11 : IRQPL47	IRC0_IRQVA47
48	MFS RX ch.1	IRC0_IRQPL12 : IRQPL48	IRC0_IRQVA48
49	MFS TX ch.1	IRC0_IRQPL12 : IRQPL49	IRC0_IRQVA49
50	MFS RX ch.2	IRC0_IRQPL12 : IRQPL50	IRC0_IRQVA50
51	MFS TX ch.2	IRC0_IRQPL12 : IRQPL51	IRC0_IRQVA51
52	MFS RX ch.3	IRC0_IRQPL13 : IRQPL52	IRC0_IRQVA52
53	MFS TX ch.3	IRC0_IRQPL13 : IRQPL53	IRC0_IRQVA53
54	MFS RX ch.4	IRC0_IRQPL13 : IRQPL54	IRC0_IRQVA54
55	MFS TX ch.4	IRC0_IRQPL13 : IRQPL55	IRC0_IRQVA55
56	MFS RX ch.5	IRC0_IRQPL14 : IRQPL56	IRC0_IRQVA56
57	MFS TX ch.5	IRC0_IRQPL14 : IRQPL57	IRC0_IRQVA57
58	MFS RX ch.6	IRC0_IRQPL14 : IRQPL58	IRC0_IRQVA58
59	MFS TX ch.6	IRC0_IRQPL14 : IRQPL59	IRC0_IRQVA59
60	MFS RX ch.7	IRC0_IRQPL15 : IRQPL60	IRC0_IRQVA60
61	MFS TX ch.7	IRC0_IRQPL15 : IRQPL61	IRC0_IRQVA61
62	MFS RX ch.8	IRC0_IRQPL15 : IRQPL62	IRC0_IRQVA62
63	MFS TX ch.8	IRC0_IRQPL15 : IRQPL63	IRC0_IRQVA63
64	MFS RX ch.9	IRC0_IRQPL16 : IRQPL64	IRC0_IRQVA64
65	MFS TX ch.9	IRC0_IRQPL16 : IRQPL65	IRC0_IRQVA65
66	MFS RX ch.10	IRC0_IRQPL16 : IRQPL66	IRC0_IRQVA66
67	MFS TX ch.10	IRC0_IRQPL16 : IRQPL67	IRC0_IRQVA67
68	MFS RX ch.11	IRC0_IRQPL17 : IRQPL68	IRC0_IRQVA68
69	MFS TX ch.11	IRC0_IRQPL17 : IRQPL69	IRC0_IRQVA69
70	MFS RX ch.12	IRC0_IRQPL17 : IRQPL70	IRC0_IRQVA70
71	MFS TX ch.12	IRC0_IRQPL17 : IRQPL71	IRC0_IRQVA71
72	MFS RX ch.13	IRC0_IRQPL18 : IRQPL72	IRC0_IRQVA72
73	MFS TX ch.13	IRC0_IRQPL18 : IRQPL73	IRC0_IRQVA73
74 to 90	Reserved		
91	SHE Error	RC0_IRQPL22 : IRQPL91	IRC0_IRQVA91
92	SHE	RC0_IRQPL23 : IRQPL92	IRC0_IRQVA92
93 to 94	Reserved		
95	TCRAM diag	RC0_IRQPL23 : IRQPL95	IRC0_IRQVA95
96	Reserved		
97	Global Timer (Compare Clear Interrupt)	RC0_IRQPL24 : IRQPL97	IRC0_IRQVA97
98	RTC	RC0_IRQPL24 : IRQPL98	IRC0_IRQVA98
99	CR CARIBRATION	RC0_IRQPL24 : IRQPL99	IRC0_IRQVA99
100	Base Timer ch.0/8/9/10/11	IRC0_IRQPL25 : IRQPL100	IRC0_IRQVA100
101	Base Timer ch.1	IRC0_IRQPL25 : IRQPL101	IRC0_IRQVA101
102	Base Timer ch.2	IRC0_IRQPL25 : IRQPL102	IRC0_IRQVA102
103	Base Timer ch.3	IRC0_IRQPL25 : IRQPL103	IRC0_IRQVA103
104	Base Timer ch.4	IRC0_IRQPL26 : IRQPL104	IRC0_IRQVA104

IRQ No.	Detail	IRQ Priority Register	Vector Address Register
105	Base Timer ch.5	IRC0_IRQPL26 : IRQPL105	IRC0_IRQVA105
106	Base Timer ch.6	IRC0_IRQPL26 : IRQPL106	IRC0_IRQVA106
107	Base Timer ch.7	IRC0_IRQPL26 : IRQPL107	IRC0_IRQVA107
108	Base Timer ch.12/20/21/22/23	IRC0_IRQPL27 : IRQPL108	IRC0_IRQVA108
109	Base Timer ch.13	IRC0_IRQPL27 : IRQPL109	IRC0_IRQVA109
110	Base Timer ch.14	IRC0_IRQPL27 : IRQPL110	IRC0_IRQVA110
111	Base Timer ch.15	IRC0_IRQPL27 : IRQPL111	IRC0_IRQVA111
112	Base Timer ch.16	IRC0_IRQPL28 : IRQPL112	IRC0_IRQVA112
113	Base Timer ch.17	IRC0_IRQPL28 : IRQPL113	IRC0_IRQVA113
114	Base Timer ch.18	IRC0_IRQPL28 : IRQPL114	IRC0_IRQVA114
115	Base Timer ch.19	IRC0_IRQPL28 : IRQPL115	IRC0_IRQVA115
116	Base Timer ch.24/32/33/34/35	IRC0_IRQPL29 : IRQPL116	IRC0_IRQVA116
117	Base Timer ch.25	IRC0_IRQPL29 : IRQPL117	IRC0_IRQVA117
118	Base Timer ch.26	IRC0_IRQPL29 : IRQPL118	IRC0_IRQVA118
119	Base Timer ch.27	IRC0_IRQPL29 : IRQPL119	IRC0_IRQVA119
120	Base Timer ch.28	IRC0_IRQPL30 : IRQPL120	IRC0_IRQVA120
121	Base Timer ch.29	IRC0_IRQPL30 : IRQPL121	IRC0_IRQVA121
122	Base Timer ch.30	IRC0_IRQPL30 : IRQPL122	IRC0_IRQVA122
123	Base Timer ch.31	IRC0_IRQPL30 : IRQPL123	IRC0_IRQVA123
124	Base Timer ch.36/44/45/46/47	IRC0_IRQPL31 : IRQPL124	IRC0_IRQVA124
125	Base Timer ch.37	IRC0_IRQPL31 : IRQPL125	IRC0_IRQVA125
126	Base Timer ch.38	IRC0_IRQPL31 : IRQPL126	IRC0_IRQVA126
127	Base Timer ch.39	IRC0_IRQPL31 : IRQPL127	IRC0_IRQVA127
128	Base Timer ch.40	IRC0_IRQPL32 : IRQPL128	IRC0_IRQVA128
129	Base Timer ch.41	IRC0_IRQPL32 : IRQPL129	IRC0_IRQVA129
130	Base Timer ch.42	IRC0_IRQPL32 : IRQPL130	IRC0_IRQVA130
131	Base Timer ch.43	IRC0_IRQPL32 : IRQPL131	IRC0_IRQVA131
132	Base Timer ch.48/56/57/58/59	IRC0_IRQPL33 : IRQPL132	IRC0_IRQVA132
133	Base Timer ch.49	IRC0_IRQPL33 : IRQPL133	IRC0_IRQVA133
134	Base Timer ch.50	IRC0_IRQPL33 : IRQPL134	IRC0_IRQVA134
135	Base Timer ch.51	IRC0_IRQPL33 : IRQPL135	IRC0_IRQVA135
136	Base Timer ch.52	IRC0_IRQPL34 : IRQPL136	IRC0_IRQVA136
137	Base Timer ch.53	IRC0_IRQPL34 : IRQPL137	IRC0_IRQVA137
138	Base Timer ch.54	IRC0_IRQPL34 : IRQPL138	IRC0_IRQVA138
139	Base Timer ch.55	IRC0_IRQPL34 : IRQPL139	IRC0_IRQVA139
140	Base Timer ch.60	IRC0_IRQPL35 : IRQPL140	IRC0_IRQVA140
141	Base Timer ch.61	IRC0_IRQPL35 : IRQPL141	IRC0_IRQVA141
142	Base Timer ch.62	IRC0_IRQPL35 : IRQPL142	IRC0_IRQVA142
143	Base Timer ch.63	IRC0_IRQPL35 : IRQPL143	IRC0_IRQVA143
144	Reload Timer ch.0	IRC0_IRQPL36 : IRQPL144	IRC0_IRQVA144

IRQ No.	Detail	IRQ Priority Register	Vector Address Register
145	Reload Timer ch.1	IRC0_IRQPL36 : IRQPL145	IRC0_IRQVA145
146	Reload Timer ch.2	IRC0_IRQPL36 : IRQPL146	IRC0_IRQVA146
147	Reload Timer ch.3	IRC0_IRQPL36 : IRQPL147	IRC0_IRQVA147
148	Reload Timer ch.16	IRC0_IRQPL37 : IRQPL148	IRC0_IRQVA148
149	Reload Timer ch.17	IRC0_IRQPL37 : IRQPL149	IRC0_IRQVA149
150	FRT ch.0	IRC0_IRQPL37 : IRQPL150	IRC0_IRQVA150
151	FRT ch.1	IRC0_IRQPL37 : IRQPL151	IRC0_IRQVA151
152	FRT ch.2	IRC0_IRQPL38 : IRQPL152	IRC0_IRQVA152
153	FRT ch.3	IRC0_IRQPL38 : IRQPL153	IRC0_IRQVA153
154	FRT ch.4	IRC0_IRQPL38 : IRQPL154	IRC0_IRQVA154
155	Reserved		
156	FRT ch.8	IRC0_IRQPL39 : IRQPL156	IRC0_IRQVA156
157	FRT ch.9	IRC0_IRQPL39 : IRQPL157	IRC0_IRQVA157
158	FRT ch.10	IRC0_IRQPL39 : IRQPL158	IRC0_IRQVA158
159 to 161	Reserved		
162	IRQ0 of Input Capture 0 (ch.0)	IRC0_IRQPL40 : IRQPL162	IRC0_IRQVA162
163	IRQ0 of Input Capture 1 (ch.2)	IRC0_IRQPL40 : IRQPL163	IRC0_IRQVA163
164	IRQ0 of Input Capture 2 (ch.4)	IRC0_IRQPL41 : IRQPL164	IRC0_IRQVA164
165	IRQ0 of Input Capture 8 (ch.16)	IRC0_IRQPL41 : IRQPL165	IRC0_IRQVA165
166	IRQ0 of Input Capture 9 (ch.18)	IRC0_IRQPL41 : IRQPL166	IRC0_IRQVA166
167	IRQ0 of Input Capture 10 (ch.20)	IRC0_IRQPL41 : IRQPL167	IRC0_IRQVA167
168	IRQ1 of Input Capture 0 (ch.1)	IRC0_IRQPL42 : IRQPL168	IRC0_IRQVA168
169	IRQ1 of Input Capture 1 (ch.3)	IRC0_IRQPL42 : IRQPL169	IRC0_IRQVA169
170	IRQ1 of Input Capture 2 (ch.5)	IRC0_IRQPL42 : IRQPL170	IRC0_IRQVA170
171	IRQ1 of Input Capture 8 (ch.17)	IRC0_IRQPL42 : IRQPL171	IRC0_IRQVA171
172	IRQ1 of Input Capture 9 (ch.19)	IRC0_IRQPL43 : IRQPL172	IRC0_IRQVA172
173	IRQ1 of Input Capture 10 (ch.21)	IRC0_IRQPL43 : IRQPL173	IRC0_IRQVA173
174	IRQ0 of Output Compare 0 (ch.0)	IRC0_IRQPL43 : IRQPL174	IRC0_IRQVA174
175	IRQ0 of Output Compare 1 (ch.2)	IRC0_IRQPL43 : IRQPL175	IRC0_IRQVA175
176	IRQ0 of Output Compare 2 (ch.4)	IRC0_IRQPL44 : IRQPL176	IRC0_IRQVA176
177	Reserved		
178	IRQ0 of Output Compare 8 (ch.16)	IRC0_IRQPL44 : IRQPL178	IRC0_IRQVA178
179	IRQ0 of Output Compare 9 (ch.18)	IRC0_IRQPL44 : IRQPL179	IRC0_IRQVA179
180	IRQ0 of Output Compare 10 (ch.20)	IRC0_IRQPL45 : IRQPL180	IRC0_IRQVA180
181	IRQ1 of Output Compare 0 (ch.1)	IRC0_IRQPL45 : IRQPL181	IRC0_IRQVA181
182	IRQ1 of Output Compare 1 (ch.3)	IRC0_IRQPL45 : IRQPL182	IRC0_IRQVA182
183	IRQ1 of Output Compare 2 (ch.5)	IRC0_IRQPL45 : IRQPL183	IRC0_IRQVA183
184	Reserved		
185	IRQ1 of Output Compare 8 (ch.17)	IRC0_IRQPL46 : IRQPL185	IRC0_IRQVA185
186	IRQ1 of Output Compare 9 (ch.19)	IRC0_IRQPL46 : IRQPL186	IRC0_IRQVA186

IRQ No.	Detail	IRQ Priority Register	Vector Address Register
187	IRQ1 of Output Compare 10 (ch.21)	IRC0_IRQPL46 : IRQPL187	IRC0_IRQVA187
188	QPRC ch.8	IRC0_IRQPL47 : IRQPL188	IRC0_IRQVA188
189	QPRC ch.9	IRC0_IRQPL47 : IRQPL189	IRC0_IRQVA189
190	ADC12B0 Conversion Done	IRC0_IRQPL47 : IRQPL190	IRC0_IRQVA190
191	ADC12B0 Group interrupt	IRC0_IRQPL47 : IRQPL191	IRC0_IRQVA191
192	ADC12B0 pulse detection function	IRC0_IRQPL48 : IRQPL192	IRC0_IRQVA192
193	ADC12B0 RCO	IRC0_IRQPL48 : IRQPL193	IRC0_IRQVA193
194	ADC12B1 Conversion Done	IRC0_IRQPL48 : IRQPL194	IRC0_IRQVA194
195	ADC12B1 Group interrupt	IRC0_IRQPL48 : IRQPL195	IRC0_IRQVA195
196	ADC12B1 pulse detection function	IRC0_IRQPL49 : IRQPL196	IRC0_IRQVA196
197	ADC12B1 RCO	IRC0_IRQPL49 : IRQPL197	IRC0_IRQVA197
198	DMA Error	IRC0_IRQPL49 : IRQPL198	IRC0_IRQVA198
199	DMAC Completion ch.0	IRC0_IRQPL49 : IRQPL199	IRC0_IRQVA199
200	DMAC Completion ch.1	IRC0_IRQPL50 : IRQPL200	IRC0_IRQVA200
201	DMAC Completion ch.2	IRC0_IRQPL50 : IRQPL201	IRC0_IRQVA201
202	DMAC Completion ch.3	IRC0_IRQPL50 : IRQPL202	IRC0_IRQVA202
203	DMAC Completion ch.4	IRC0_IRQPL50 : IRQPL203	IRC0_IRQVA203
204	DMAC Completion ch.5	IRC0_IRQPL51 : IRQPL204	IRC0_IRQVA204
205	DMAC Completion ch.6	IRC0_IRQPL51 : IRQPL205	IRC0_IRQVA205
206	DMAC Completion ch.7	IRC0_IRQPL51 : IRQPL206	IRC0_IRQVA206
207	DMAC Completion ch.8	IRC0_IRQPL51 : IRQPL207	IRC0_IRQVA207
208	DMAC Completion ch.9	IRC0_IRQPL52 : IRQPL208	IRC0_IRQVA208
209	DMAC Completion ch.10	IRC0_IRQPL52 : IRQPL209	IRC0_IRQVA209
210	DMAC Completion ch.11	IRC0_IRQPL52 : IRQPL210	IRC0_IRQVA210
211	DMAC Completion ch.12	IRC0_IRQPL52 : IRQPL211	IRC0_IRQVA211
212	DMAC Completion ch.13	IRC0_IRQPL53 : IRQPL212	IRC0_IRQVA212
213	DMAC Completion ch.14	IRC0_IRQPL53 : IRQPL213	IRC0_IRQVA213
214	DMAC Completion ch.15	IRC0_IRQPL53 : IRQPL214	IRC0_IRQVA214
215	DMAC RLT(ch.0,1,2,3 OR-ed)	IRC0_IRQPL53 : IRQPL215	IRC0_IRQVA215
216	SCT RC IRQ	IRC0_IRQPL54 : IRQPL216	IRC0_IRQVA216
217	SCT SRC IRQ	IRC0_IRQPL54 : IRQPL217	IRC0_IRQVA217
218	SCT Main OSC IRQ	IRC0_IRQPL54 : IRQPL218	IRC0_IRQVA218
219	SCT Sub OSC IRQ	IRC0_IRQPL54 : IRQPL219	IRC0_IRQVA219
220	CR5 Performance Monitor Unit IRQ	IRC0_IRQPL55 : IRQPL220	IRC0_IRQVA220
221	RPGCRC	IRC0_IRQPL55 : IRQPL221	IRC0_IRQVA221
222	MFS ch.0 Error (Tx/Rx error, Status OR-ed)	IRC0_IRQPL55 : IRQPL222	IRC0_IRQVA222
223	MFS ch.1 Error (Tx/Rx error, Status OR-ed)	IRC0_IRQPL55 : IRQPL223	IRC0_IRQVA223
224	MFS ch.2 Error (Tx/Rx error, Status OR-ed)	IRC0_IRQPL56 : IRQPL224	IRC0_IRQVA224
225	MFS ch.3 Error (Tx/Rx error, Status OR-ed)	IRC0_IRQPL56 : IRQPL225	IRC0_IRQVA225
226	MFS ch.4 Error (Tx/Rx error, Status OR-ed)	IRC0_IRQPL56 : IRQPL226	IRC0_IRQVA226

IRQ No.	Detail	IRQ Priority Register	Vector Address Register
227	MFS ch.5 Error (Tx/Rx error, Status OR-ed)	IRC0_IRQPL56 : IRQPL227	IRC0_IRQVA227
228	MFS ch.6 Error (Tx/Rx error, Status OR-ed)	IRC0_IRQPL57 : IRQPL228	IRC0_IRQVA228
229	MFS ch.7 Error (Tx/Rx error, Status OR-ed)	IRC0_IRQPL57 : IRQPL229	IRC0_IRQVA229
230	MFS ch.8 Error (Tx/Rx error, Status OR-ed)	IRC0_IRQPL57 : IRQPL230	IRC0_IRQVA230
231	MFS ch.9 Error (Tx/Rx error, Status OR-ed)	IRC0_IRQPL57 : IRQPL231	IRC0_IRQVA231
232	MFS ch.10 Error (Tx/Rx error, Status OR-ed)	IRC0_IRQPL58 : IRQPL232	IRC0_IRQVA232
233	MFS ch.11 Error (Tx/Rx error, Status OR-ed)	IRC0_IRQPL58 : IRQPL233	IRC0_IRQVA233
234	MFS ch.12 Error (Tx/Rx error, Status OR-ed)	IRC0_IRQPL58 : IRQPL234	IRC0_IRQVA234
235	MFS ch.13 Error (Tx/Rx error, Status OR-ed)	IRC0_IRQPL58 : IRQPL235	IRC0_IRQVA235
236 to 255	Reserved		

2. NMI Map

This section shows NMI map.

NMI No.	Detail	Priority Level	IRQ/NMI Vector Address
0	NMIX pin(Ext-IRC)	IRC0_NMIPL0 : NMIPL0	IRC0_NMIVA0
1 to 3	Reserved		
4	LVDs IRQ	IRC0_NMIPL1 : NMIPL4	IRC0_NMIVA4
5	CSV, Profile	IRC0_NMIPL1 : NMIPL5	IRC0_NMIVA5
6	HW-WDT	IRC0_NMIPL1 : NMIPL6	IRC0_NMIVA6
7	SW-WDT	IRC0_NMIPL1 : NMIPL7	IRC0_NMIVA7
8	IRC 2-bit ECC err detection	IRC0_NMIPL2 : NMIPL8	IRC0_NMIVA8
9 to 11	Reserved		
12	CAN-FD RAMs 2-bit ECC error detection	IRC0_NMIPL3 : NMIPL12	IRC0_NMIVA12
13	DMAC MPU #0 protection violation	IRC0_NMIPL3 : NMIPL13	IRC0_NMIVA13
14	Reserved		
15	SHE MPU	IRC0_NMIPL3 : NMIPL15	IRC0_NMIVA15
16 to 17	Reserved		
18	TPU protection violation	IRC0_NMIPL4 : NMIPL18	IRC0_NMIVA18
19 to 23	Reserved		
24	Bus diagnosis error detection	IRC0_NMIPL6 : NMIPL24	IRC0_NMIVA24
25 to 31	Reserved		

CHAPTER 9: DMA Channel Activation Factors



This chapter explains the DMA channel activation factors.

1.Factors list

CODE: DMAFACT-S6J3400-E1

1. Factors list

Client Number	Peripheral Functions						Enable Setting of IRQ Request	Remarks
	Combination. 0	Combination. 1	Combination. 2	Combination. 3	Combination. 4	Combination. 5		
0 to 8	Reserved						-	
9	WORK FLASH	-	-	-	-	-	Unnecessary	*2
10	Ext IRQ 0	Ext IRQ 8	Ext IRQ 16	Ext IRQ 24	-	-	Unnecessary	*1
11	Ext IRQ 1	Ext IRQ 9	Ext IRQ 17	Ext IRQ 25	-	-	Unnecessary	*1
12	Ext IRQ 2	Ext IRQ 10	Ext IRQ 18	Ext IRQ 26	-	-	Unnecessary	*1
13	Ext IRQ 3	Ext IRQ 11	Ext IRQ 19	Ext IRQ 27	-	-	Unnecessary	*1
14	Ext IRQ 4	Ext IRQ 12	Ext IRQ 20	Ext IRQ 28	-	-	Unnecessary	*1
15	Ext IRQ 5	Ext IRQ 13	Ext IRQ 21	Ext IRQ 29	-	-	Unnecessary	*1
16	Ext IRQ 6	Ext IRQ 14	Ext IRQ 22	Ext IRQ 30	-	-	Unnecessary	*1
17	Ext IRQ 7	Ext IRQ 15	Ext IRQ 23	Ext IRQ 31	-	-	Unnecessary	*1
18	MFS ch.0 RX	-	-	-	-	-	Necessary	*4
19	MFS ch.0 TX	-	-	-	-	-	Necessary	*4
20	MFS ch.1 RX	-	-	-	-	-	Necessary	*4
21	MFS ch.1 TX	-	-	-	-	-	Necessary	*4
22	MFS ch.2 RX	-	-	-	-	-	Necessary	*4
23	MFS ch.2 TX	-	-	-	-	-	Necessary	*4
24	MFS ch.3 RX	-	-	-	-	-	Necessary	*4
25	MFS ch.3 TX	-	-	-	-	-	Necessary	*4
26	MFS ch.4 RX	-	-	-	-	-	Necessary	*4
27	MFS ch.4 TX	-	-	-	-	-	Necessary	*4
28	MFS ch.5 RX	-	-	-	-	-	Necessary	*4
29	MFS ch.5 TX	-	-	-	-	-	Necessary	*4
30	MFS ch.6 RX	-	-	-	-	-	Necessary	*4
31	MFS ch.6 TX	-	-	-	-	-	Necessary	*4
32	MFS ch.7 RX	-	-	-	-	-	Necessary	*4

Client Number	Peripheral Functions						Enable Setting of IRQ Request	Remarks
	Combination. 0	Combination. 1	Combination. 2	Combination. 3	Combination. 4	Combination. 5		
33	MFS ch.7 TX	-	-	-	-	-	Necessary	*4
34	MFS ch.8 RX	-	-	-	-	-	Necessary	*4
35	MFS ch.8 TX	-	-	-	-	-	Necessary	*4
36	MFS ch.9 RX	-	-	-	-	-	Necessary	*4
37	MFS ch.9 TX	-	-	-	-	-	Necessary	*4
38	MFS ch.10 RX	-	-	-	-	-	Necessary	*4
39	MFS ch.10 TX	-	-	-	-	-	Necessary	*4
40	MFS ch.11 RX	-	-	-	-	-	Necessary	*4
41	MFS ch.11 TX	-	-	-	-	-	Necessary	*4
42	MFS ch.12 RX	-	-	-	-	-	Necessary	*4
43	MFS ch.12 TX	-	-	-	-	-	Necessary	*4
44	MFS ch.13 RX	-	-	-	-	-	Necessary	*4
45	MFS ch.13 TX	-	-	-	-	-	Necessary	*4
46 to 49	Reserved						-	
50	-	-	-	-	-	-	-	
51	-	-	-	-	-	-	-	
52	-	-	-	-	-	-	-	
53	-	-	-	-	-	-	-	
54	-	-	-	-	-	-	-	
55	-	-	-	-	-	-	-	
56	Base Timer ch.0-0	Base Timer ch.0-1	Base Timer ch.24-0	Base Timer ch.24-1	Base Timer ch.48-0	Base Timer ch.48-1	Necessary	*1, *3
57	Base Timer ch.1-0	Base Timer ch.1-1	Base Timer ch.25-0	Base Timer ch.25-1	Base Timer ch.49-0	Base Timer ch.49-1	Necessary	*1, *3
58	Base Timer ch.2-0	Base Timer ch.2-1	Base Timer ch.26-0	Base Timer ch.26-1	Base Timer ch.50-0	Base Timer ch.50-1	Necessary	*1, *3
59	Base Timer ch.3-0	Base Timer ch.3-1	Base Timer ch.27-0	Base Timer ch.27-1	Base Timer ch.51-0	Base Timer ch.51-1	Necessary	*1, *3
60	Base Timer ch.4-0	Base Timer ch.4-1	Base Timer ch.28-0	Base Timer ch.28-1	Base Timer ch.52-0	Base Timer ch.52-1	Necessary	*1, *3

Client Number	Peripheral Functions						Enable Setting of IRQ Request	Remarks
	Combination. 0	Combination. 1	Combination. 2	Combination. 3	Combination. 4	Combination. 5		
61	Base Timer ch.5-0	Base Timer ch.5-1	Base Timer ch.29-0	Base Timer ch.29-1	Base Timer ch.53-0	Base Timer ch.53-1	Necessary	*1, *3
62	Base Timer ch.6-0	Base Timer ch.6-1	Base Timer ch.30-0	Base Timer ch.30-1	Base Timer ch.54-0	Base Timer ch.54-1	Necessary	*1, *3
63	Base Timer ch.7-0	Base Timer ch.7-1	Base Timer ch.31-0	Base Timer ch.31-1	Base Timer ch.55-0	Base Timer ch.55-1	Necessary	*1, *3
64	Base Timer ch.8-0	Base Timer ch.8-1	Base Timer ch.32-0	Base Timer ch.32-1	Base Timer ch.56-0	Base Timer ch.56-1	Necessary	*1, *3
65	Base Timer ch.9-0	Base Timer ch.9-1	Base Timer ch.33-0	Base Timer ch.33-1	Base Timer ch.57-0	Base Timer ch.57-1	Necessary	*1, *3
66	Base Timer ch.10-0	Base Timer ch.10-1	Base Timer ch.34-0	Base Timer ch.34-1	Base Timer ch.58-0	Base Timer ch.58-1	Necessary	*1, *3
67	Base Timer ch.11-0	Base Timer ch.11-1	Base Timer ch.35-0	Base Timer ch.35-1	Base Timer ch.59-0	Base Timer ch.59-1	Necessary	*1, *3
68	Base Timer ch.12-0	Base Timer ch.12-1	Base Timer ch.36-0	Base Timer ch.36-1	Base Timer ch.60-0	Base Timer ch.60-1	Necessary	*1, *3
69	Base Timer ch.13-0	Base Timer ch.13-1	Base Timer ch.37-0	Base Timer ch.37-1	Base Timer ch.61-0	Base Timer ch.61-1	Necessary	*1, *3
70	Base Timer ch.14-0	Base Timer ch.14-1	Base Timer ch.38-0	Base Timer ch.38-1	Base Timer ch.62-0	Base Timer ch.62-1	Necessary	*1, *3
71	Base Timer ch.15-0	Base Timer ch.15-1	Base Timer ch.39-0	Base Timer ch.39-1	Base Timer ch.63-0	Base Timer ch.63-1	Necessary	*1, *3
72	Base Timer ch.16-0	Base Timer ch.16-1	Base Timer ch.40-0	Base Timer ch.40-1	-	-	Necessary	*1, *3
73	Base Timer ch.17-0	Base Timer ch.17-1	Base Timer ch.41-0	Base Timer ch.41-1	-	-	Necessary	*1, *3
74	Base Timer ch.18-0	Base Timer ch.18-1	Base Timer ch.42-0	Base Timer ch.42-1	-	-	Necessary	*1, *3
75	Base Timer ch.19-0	Base Timer ch.19-1	Base Timer ch.43-0	Base Timer ch.43-1	-	-	Necessary	*1, *3
76	Base Timer ch.20-0	Base Timer ch.20-1	Base Timer ch.44-0	Base Timer ch.44-1	-	-	Necessary	*1, *3
77	Base Timer ch.21-0	Base Timer ch.21-1	Base Timer ch.45-0	Base Timer ch.45-1	-	-	Necessary	*1, *3
78	Base Timer ch.22-0	Base Timer ch.22-1	Base Timer ch.46-0	Base Timer ch.46-1	-	-	Necessary	*1, *3
79	Base Timer ch.23-0	Base Timer ch.23-1	Base Timer ch.47-0	Base Timer ch.47-1	-	-	Necessary	*1, *3
80	FRT ch.0 Match	FRT ch.0 Zero	FRT ch.2 Match	FRT ch.2 Zero	FRT ch.4 Match	FRT ch.4 Zero	Necessary	*1, *3
81	FRT ch.1 Match	FRT ch.1 Zero	FRT ch.3 Match	FRT ch.3 Zero	-	-	Necessary	*1, *3
82	FRT ch.8 Match	FRT ch.8 Zero	FRT ch.10 Match	FRT ch.10 Zero	-	-	Necessary	*1, *3

Client Number	Peripheral Functions						Enable Setting of IRQ Request	Remarks
	Combination. 0	Combination. 1	Combination. 2	Combination. 3	Combination. 4	Combination. 5		
83	FRT ch.9 Match	FRT ch.9 Zero	-	-	-	-	Necessary	*1, *3
84	IRQ0 of ICU pair0 (ch.0)	IRQ0 of ICU pair1 (ch.2)	IRQ0 of ICU pair2 (ch.4)	-	-	-	Necessary	*1, *3
85	IRQ0 of ICU pair8 (ch.16)	IRQ0 of ICU pair9 (ch.18)	IRQ0 of ICU pair10 (ch.20)	-	-	-	Necessary	*1, *3
86	IRQ1 of ICU pair0 (ch.1)	IRQ1 of ICU pair1 (ch.3)	IRQ1 of ICU pair2 (ch.5)	-	-	-	Necessary	*1, *3
87	IRQ1 of ICU pair8 (ch.17)	IRQ1 of ICU pair9 (ch.19)	IRQ1 of ICU pair10 (ch.21)	-	-	-	Necessary	*1, *3
88	IRQ0 of OCU pair0 (ch.0)	IRQ0 of OCU pair1 (ch.2)	IRQ0 of OCU pair2 (ch.4)	-	-	-	Necessary	*1, *3
89	IRQ0 of OCU pair8 (ch.16)	IRQ0 of OCU pair9 (ch.18)	IRQ0 of OCU pair10 (ch.20)	-	-	-	Necessary	*1, *3
90	IRQ1 of OCU pair0 (ch.1)	IRQ1 of OCU pair1 (ch.3)	IRQ1 of OCU pair2 (ch.5)	-	-	-	Necessary	*1, *3
91	IRQ1 of OCU pair8 (ch.17)	IRQ1 of OCU pair9 (ch.19)	IRQ1 of OCU pair10 (ch.21)	-	-	-	Necessary	*1, *3
92	Reload Timer ch.0	Reload Timer ch.2	Reload Timer ch.16	-	-	-	Unnecessary	*1
93	Reload Timer ch.1	Reload Timer ch.3	Reload Timer ch.17	-	-	-	Unnecessary	*1
94	DMAC #0 Reload Timer 0	DMAC #0 Reload Timer 1	DMAC #0 Reload Timer 2	DMAC #0 Reload Timer 3	-	-	Unnecessary	*1
95	ADC12B0-0	-	-	-	-	-	Unnecessary	
96	ADC12B0-1	-	-	-	-	-	Unnecessary	
97	ADC12B0-2	-	-	-	-	-	Unnecessary	
98	ADC12B0-3	-	-	-	-	-	Unnecessary	
99	ADC12B1-0	-	-	-	-	-	Unnecessary	
100	ADC12B1-1	-	-	-	-	-	Unnecessary	
101	ADC12B1-2	-	-	-	-	-	Unnecessary	
102	ADC12B1-3	-	-	-	-	-	Unnecessary	
103	PRGCRC	-	-	-	-	-	Unnecessary	
104 to 127	Reserved						-	

- *1: For assignment of source, see the chapter of "I/O Port" on this manual.
- *2: DSTP_ACK function is set by DMAi_CMCICm:BEHSTPACK.
- *3: The interrupt factor flags of peripheral function are cleared automatically by acceptance of DMA transfer request.
- *4: The interrupt factor flags of peripheral function are cleared automatically after DMA transfer is started.

CHAPTER 10: Port Description



This chapter explains port functions.

1. Port description list
2. Remark

CODE: PORT_DESCRIPTION-S6J3400-E2

1. Port Description List

The table shows the port function of description which is supported. The port function which is not described in the table is not supported for the product.

Port Name	Description	Pin No. of Package			Remark
		LQFP 100	LQFP 144	TEQFP 176	
MD	Mode pin	83	117	145	
RSTX	External reset input pin	89	123	151	
NMIX	Non-maskable interrupt input pin	68	95	115	
X0	Main clock oscillation input pin	84	118	146	
X1	Main clock oscillation output pin	85	119	147	
X0A	Sub clock oscillation input pin	88	122	150	
X1A	Sub clock oscillation output pin	87	121	149	
INT0_0	External interrupt ch.0 input pin (0)	56	80	99	
INT0_1	External interrupt ch.0 input pin (1)	-	9	11	
INT0_2	External interrupt ch.0 input pin (2)	2	3	3	
INT1_0	External interrupt ch.1 input pin (0)	69	97	117	
INT1_1	External interrupt ch.1 input pin (1)	14	23	29	
INT1_2	External interrupt ch.1 input pin (2)	-	-	13	
INT2_0	External interrupt ch.2 input pin (0)	94	128	156	
INT2_1	External interrupt ch.2 input pin (1)	22	33	41	
INT2_2	External interrupt ch.2 input pin (2)	8	12	15	
INT3_0	External interrupt ch.3 input pin (0)	13	20	24	
INT3_1	External interrupt ch.3 input pin (1)	23	34	42	
INT4_0	External interrupt ch.4 input pin (0)	15	24	30	
INT4_1	External interrupt ch.4 input pin (1)	33	46	57	
INT4_2	External interrupt ch.4 input pin (2)	-	15	19	
INT5_0	External interrupt ch.5 input pin (0)	39	56	70	
INT5_1	External interrupt ch.5 input pin (1)	-	47	58	
INT5_2	External interrupt ch.5 input pin (2)	-	53	67	
INT6_0	External interrupt ch.6 input pin (0)	-	66	82	
INT6_1	External interrupt ch.6 input pin (1)	41	58	74	
INT7_0	External interrupt ch.7 input pin (0)	53	77	96	
INT7_1	External interrupt ch.7 input pin (1)	44	63	79	
INT8_0	External interrupt ch.8 input pin (0)	63	87	106	
INT8_1	External interrupt ch.8 input pin (1)	58	82	101	
INT8_2	External interrupt ch.8 input pin (2)	11	18	22	
INT9_0	External interrupt ch.9 input pin (0)	-	105	128	
INT9_1	External interrupt ch.9 input pin (1)	60	84	103	
INT10_0	External interrupt ch.10 input pin (0)	-	-	139	
INT10_1	External interrupt ch.10 input pin (1)	71	101	123	
INT11_0	External interrupt ch.11 input pin (0)	95	131	159	
INT11_1	External interrupt ch.11 input pin (1)	-	104	127	

Port Name	Description	Pin No. of Package			Remark
		LQFP 100	LQFP 144	TEQFP 176	
INT11_2	External interrupt ch.11 input pin (2)	-	26	32	
INT12_0	External interrupt ch.12 input pin (0)	-	134	162	
INT12_1	External interrupt ch.12 input pin (1)	-	106	129	
INT12_2	External interrupt ch.12 input pin (2)	-	143	175	
INT12_3	External interrupt ch.12 input pin (3)	20	31	39	
INT13_0	External interrupt ch.13 input pin (0)	-	-	169	
INT13_1	External interrupt ch.13 input pin (1)	-	136	165	
INT13_2	External interrupt ch.13 input pin (2)	29	41	51	
INT14_0	External interrupt ch.14 input pin (0)	-	141	172	
INT14_1	External interrupt ch.14 input pin (1)	97	137	167	
INT15_0	External interrupt ch.15 input pin (0)	-	-	120	
INT15_1	External interrupt ch.15 input pin (1)	-	140	171	
INT15_2	External interrupt ch.15 input pin (2)	36	51	63	
INT16_0	External interrupt ch.16 input pin (0)	3	5	7	
INT16_1	External interrupt ch.16 input pin (1)	-	59	75	
INT17_0	External interrupt ch.17 input pin (0)	10	14	18	
INT17_1	External interrupt ch.17 input pin (1)	59	83	102	
INT18_0	External interrupt ch.18 input pin (0)	19	30	37	
INT18_1	External interrupt ch.18 input pin (1)	4	6	8	
INT19_0	External interrupt ch.19 input pin (0)	24	35	43	
INT19_1	External interrupt ch.19 input pin (1)	-	88	107	
INT20_0	External interrupt ch.20 input pin (0)	27	38	46	
INT20_1	External interrupt ch.20 input pin (1)	-	90	109	
INT21_0	External interrupt ch.21 input pin (0)	33	46	57	
INT22_0	External interrupt ch.22 input pin (0)	38	54	68	
INT22_1	External interrupt ch.22 input pin (1)	-	21	25	
INT23_0	External interrupt ch.23 input pin (0)	42	60	76	
INT23_1	External interrupt ch.23 input pin (1)	-	-	48	
INT24_0	External interrupt ch.24 input pin (0)	43	61	77	
INT24_1	External interrupt ch.24 input pin (1)	66	93	113	
INT25_0	External interrupt ch.25 input pin (0)	52	76	94	
INT25_1	External interrupt ch.25 input pin (1)	-	-	64	
INT26_0	External interrupt ch.26 input pin (0)	65	92	111	
INT26_1	External interrupt ch.26 input pin (1)	-	-	143	
INT27_0	External interrupt ch.27 input pin (0)	70	99	119	
INT27_1	External interrupt ch.27 input pin (1)	-	98	118	
INT28_0	External interrupt ch.28 input pin (0)	73	103	125	
INT28_1	External interrupt ch.28 input pin (1)	74	107	131	
INT29_0	External interrupt ch.29 input pin (0)	82	115	141	
INT30_0	External interrupt ch.30 input pin (0)	98	139	170	
INT30_1	External interrupt ch.30 input pin (1)	96	135	163	

Port Name	Description	Pin No. of Package			Remark
		LQFP 100	LQFP 144	TEQFP 176	
INT31_0	External interrupt ch.31 input pin (0)	99	142	174	
INT31_1	External interrupt ch.31 input pin (1)	-	143	175	
ADTG0_0	ADC unit0 external trigger input pin (0)	59	83	102	
ADTG0_1	ADC unit0 external trigger input pin (1)	46	67	83	
ADTG1_0	ADC unit1 external trigger input pin (0)	60	84	103	
ADTG1_1	ADC unit1 external trigger input pin (1)	38	54	68	
AN000	ADC unit0 ch.0 analog input pin	27	38	46	
AN001	ADC unit0 ch.1 analog input pin	-	-	47	
AN002	ADC unit0 ch.2 analog input pin	-	-	48	
AN003	ADC unit0 ch.3 analog input pin	28	39	49	
AN004	ADC unit0 ch.4 analog input pin	-	40	50	
AN005	ADC unit0 ch.5 analog input pin	29	41	51	
AN006	ADC unit0 ch.6 analog input pin	-	45	55	
AN007	ADC unit0 ch.7 analog input pin	-	-	56	
AN008	ADC unit0 ch.8 analog input pin	33	46	57	
AN009	ADC unit0 ch.9 analog input pin	-	47	58	
AN010	ADC unit0 ch.10 analog input pin	34	48	59	
AN011	ADC unit0 ch.11 analog input pin	-	49	60	
AN012	ADC unit0 ch.12 analog input pin	-	-	61	
AN013	ADC unit0 ch.13 analog input pin	35	50	62	
AN014	ADC unit0 ch.14 analog input pin	36	51	63	
AN015	ADC unit0 ch.15 analog input pin	-	-	64	
AN016	ADC unit0 ch.16 analog input pin	-	-	65	
AN017	ADC unit0 ch.17 analog input pin	37	52	66	
AN018	ADC unit0 ch.18 analog input pin	-	53	67	
AN019	ADC unit0 ch.19 analog input pin	38	54	68	
AN020	ADC unit0 ch.20 analog input pin	-	55	69	
AN021	ADC unit0 ch.21 analog input pin	39	56	70	
AN022	ADC unit0 ch.22 analog input pin	40	57	71	
AN023	ADC unit0 ch.23 analog input pin	-	-	72	
AN024	ADC unit0 ch.24 analog input pin	-	-	73	
AN025	ADC unit0 ch.25 analog input pin	41	58	74	
AN026	ADC unit0 ch.26 analog input pin	-	59	75	
AN027	ADC unit0 ch.27 analog input pin	42	60	76	
AN028	ADC unit0 ch.28 analog input pin	43	61	77	
AN029	ADC unit0 ch.29 analog input pin	-	62	78	
AN030	ADC unit0 ch.30 analog input pin	44	63	79	
AN031	ADC unit0 ch.31 analog input pin	-	64	80	
AN100	ADC unit1 ch.0 analog input pin	45	65	81	
AN101	ADC unit1 ch.1 analog input pin	-	66	82	
AN102	ADC unit1 ch.2 analog input pin	46	67	83	

Port Name	Description	Pin No. of Package			Remark
		LQFP 100	LQFP 144	TEQFP 176	
AN103	ADC unit1 ch.3 analog input pin	-	68	84	
AN104	ADC unit1 ch.4 analog input pin	-	74	92	
AN105	ADC unit1 ch.5 analog input pin	-	75	93	
AN106	ADC unit1 ch.6 analog input pin	52	76	94	
AN107	ADC unit1 ch.7 analog input pin	53	77	96	
AN108	ADC unit1 ch.8 analog input pin	54	78	97	
AN109	ADC unit1 ch.9 analog input pin	55	79	98	
AN110	ADC unit1 ch.10 analog input pin	56	80	99	
AN111	ADC unit1 ch.11 analog input pin	57	81	100	
AN112	ADC unit1 ch.12 analog input pin	61	85	104	
AN113	ADC unit1 ch.13 analog input pin	62	86	105	
AN114	ADC unit1 ch.14 analog input pin	63	87	106	
AN115	ADC unit1 ch.15 analog input pin	-	88	107	
AN116	ADC unit1 ch.16 analog input pin	-	89	108	
AN117	ADC unit1 ch.17 analog input pin	-	90	109	
AN118	ADC unit1 ch.18 analog input pin	64	91	110	
AN119	ADC unit1 ch.19 analog input pin	65	92	111	
AN120	ADC unit1 ch.20 analog input pin	66	93	113	
AN121	ADC unit1 ch.21 analog input pin	67	94	114	
AN122	ADC unit1 ch.22 analog input pin	-	96	116	
AN123	ADC unit1 ch.23 analog input pin	69	97	117	
AN124	ADC unit1 ch.24 analog input pin	-	98	118	
AN125	ADC unit1 ch.25 analog input pin	70	99	119	
AN126	ADC unit1 ch.26 analog input pin	-	100	122	
AN127	ADC unit1 ch.27 analog input pin	71	101	123	
AN128	ADC unit1 ch.28 analog input pin	72	102	124	
AN129	ADC unit1 ch.29 analog input pin	73	103	125	
AN130	ADC unit1 ch.30 analog input pin	-	104	127	
AN131	ADC unit1 ch.31 analog input pin	-	106	129	
PWU_AN0	Partial wakeup ADC analog 0 input pin	54	78	97	
PWU_AN1	Partial wakeup ADC analog 1 input pin	55	79	98	
PWU_AN2	Partial wakeup ADC analog 2 input pin	56	80	99	
PWU_AN3	Partial wakeup ADC analog 3 input pin	57	81	100	
PWU_AN4	Partial wakeup ADC analog 4 input pin	61	85	104	
PWU_AN5	Partial wakeup ADC analog 5 input pin	62	86	105	
PWU_AN6	Partial wakeup ADC analog 6 input pin	63	87	106	
PWU_AN7	Partial wakeup ADC analog 7 input pin	-	88	107	
PWUTRG_0	Partial wakeup trigger output pin (0)	-	88	107	
PWUTRG_1	Partial wakeup trigger output pin (1)	74	107	131	
RX0_0	CAN ch.0 reception data input pin (0)	69	97	117	
RX0_1	CAN ch.0 reception data input pin (1)	63	87	106	

Port Name	Description	Pin No. of Package			Remark
		LQFP 100	LQFP 144	TEQFP 176	
RX0_2	CAN ch.0 reception data input pin (2)	56	80	99	
TX0_0	CAN ch.0 transmission data output pin (0)	-	96	116	
TX0_1	CAN ch.0 transmission data output pin (1)	62	86	105	
TX0_2	CAN ch.0 transmission data output pin (2)	55	79	98	
RX1_0	CAN ch.1 reception data input pin (0)	94	128	156	
RX1_1	CAN ch.1 reception data input pin (1)	-	105	128	
RX1_2	CAN ch.1 reception data input pin (2)	22	33	41	
TX1_0	CAN ch.1 transmission data output pin (0)	93	127	155	
TX1_1	CAN ch.1 transmission data output pin (1)	-	104	127	
TX1_2	CAN ch.1 transmission data output pin (2)	21	32	40	
RX2_0	CAN ch.2 reception data input pin (0)	53	77	96	
RX2_1	CAN ch.2 reception data input pin (1)	95	131	159	
TX2_0	CAN ch.2 transmission data output pin (0)	52	76	94	
TX2_1	CAN ch.2 transmission data output pin (1)	-	132	160	
RX3_0	CAN ch.3 reception data input pin (0)	10	14	18	
TX3_0	CAN ch.3 transmission data output pin (0)	9	13	17	
RX4_0	CAN ch.4 reception data input pin (0)	43	61	77	
TX4_0	CAN ch.4 transmission data output pin (0)	42	60	76	
RX8_0	CAN ch.8 reception data input pin (0)	73	103	125	
TX8_0	CAN ch.8 transmission data output pin (0)	72	102	124	
SCK0_0	Multi-function serial ch.0 clock I/O pin (0)	12	19	23	
SIN0_0	Multi-function serial ch.0 serial data input pin (0)	13	20	24	
SOT0_0	Multi-function serial ch.0 serial data output pin (0)	11	18	22	
SCS0_0	Multi-function serial ch.0 serial chip select 0 I/O pin (0)	-	21	25	
SCS0_1	Multi-function serial ch.0 serial chip select 0 I/O pin (1)	14	23	29	
SCK1_0	Multi-function serial ch.1 clock I/O pin (0)	18	28	34	
SIN1_0	Multi-function serial ch.1 serial data input pin (0)	15	24	30	
SOT1_0	Multi-function serial ch.1 serial data output pin (0)	16	25	31	
SCS1_0	Multi-function serial ch.1 serial chip select 0 I/O pin (0)	17	27	33	
SCK2_0	Multi-function serial ch.2 clock I/O pin (0)	-	136	165	
SCK2_1	Multi-function serial ch.2 clock I/O pin (1)	99	142	174	
SIN2_0	Multi-function serial ch.2 serial data input pin (0)	-	134	162	
SIN2_1	Multi-function serial ch.2 serial data input pin (1)	-	143	175	
SIN2_2	Multi-function serial ch.2 serial data input pin (2)	98	139	170	
SOT2_0	Multi-function serial ch.2 serial data output pin (0)	96	135	163	
SOT2_1	Multi-function serial ch.2 serial data output pin (1)	-	2	2	
SCS20_0	Multi-function serial ch.2 serial chip select 0 I/O pin (0)	97	137	167	
SCS20_1	Multi-function serial ch.2 serial chip select 0 I/O pin (1)	2	3	3	
SCS21_0	Multi-function serial ch.2 serial chip select 1 output pin (0)	-	138	168	
SCS21_1	Multi-function serial ch.2 serial chip select 1 output pin (1)	-	-	4	
SCS22_0	Multi-function serial ch.2 serial chip select 2 output pin (0)	-	141	172	
SCS22_1	Multi-function serial ch.2 serial chip select 2 output pin (1)	-	4	5	

Port Name	Description	Pin No. of Package			Remark
		LQFP 100	LQFP 144	TEQFP 176	
SCS23_0	Multi-function serial ch.2 serial chip select 3 output pin (0)	-	-	173	
SCS23_1	Multi-function serial ch.2 serial chip select 3 output pin (1)	-	-	6	
SCK3_0	Multi-function serial ch.3 clock I/O pin (0)	5	7	9	
SIN3_0	Multi-function serial ch.3 serial data input pin (0)	3	5	7	
SOT3_0	Multi-function serial ch.3 serial data output pin (0)	4	6	8	
SCS30_0	Multi-function serial ch.3 serial chip select 0 I/O pin (0)	-	8	10	
SCS30_1	Multi-function serial ch.3 serial chip select 0 I/O pin (1)	2	3	3	
SCK4_0	Multi-function serial ch.4 clock I/O pin (0)	44	63	79	
SCK4_1	Multi-function serial ch.4 clock I/O pin (1)	12	19	23	
SIN4_0	Multi-function serial ch.4 serial data input pin (0)	-	66	82	
SIN4_1	Multi-function serial ch.4 serial data input pin (1)	-	21	25	
SIN4_2	Multi-function serial ch.4 serial data input pin (2)	43	61	77	
SOT4_0	Multi-function serial ch.4 serial data output pin (0)	45	65	81	
SOT4_1	Multi-function serial ch.4 serial data output pin (1)	-	22	26	
SCS40_0	Multi-function serial ch.4 serial chip select 0 I/O pin (0)	46	67	83	
SCS40_1	Multi-function serial ch.4 serial chip select 0 I/O pin (1)	-	-	27	
SCS41_0	Multi-function serial ch.4 serial chip select 1 output pin (0)	-	68	84	
SCS41_1	Multi-function serial ch.4 serial chip select 1 output pin (1)	-	-	28	
SCS42_0	Multi-function serial ch.4 serial chip select 2 output pin (0)	-	64	80	
SCS42_1	Multi-function serial ch.4 serial chip select 2 output pin (1)	14	23	29	
SCS43_0	Multi-function serial ch.4 serial chip select 3 output pin (0)	-	62	78	
SCS43_1	Multi-function serial ch.4 serial chip select 3 output pin (1)	-	26	32	
SCK5_0	Multi-function serial ch.5 clock I/O pin (0)	57	81	100	
SCK5_1	Multi-function serial ch.5 clock I/O pin (1)	60	84	103	
SIN5_0	Multi-function serial ch.5 serial data input pin (0)	53	77	96	
SIN5_1	Multi-function serial ch.5 serial data input pin (1)	58	82	101	
SOT5_0	Multi-function serial ch.5 serial data output pin (0)	56	80	99	
SOT5_1	Multi-function serial ch.5 serial data output pin (1)	59	83	102	
SCS50_0	Multi-function serial ch.5 serial chip select 0 I/O pin (0)	55	79	98	
SCS50_1	Multi-function serial ch.5 serial chip select 0 I/O pin (1)	-	68	84	
SCS51_0	Multi-function serial ch.5 serial chip select 1 output pin (0)	54	78	97	
SCS52_0	Multi-function serial ch.5 serial chip select 2 output pin (0)	-	-	95	
SCS53_0	Multi-function serial ch.5 serial chip select 3 output pin (0)	52	76	94	
SCK6_0	Multi-function serial ch.6 clock I/O pin (0)	41	58	74	
SCK6_1	Multi-function serial ch.6 clock I/O pin (1)	82	115	141	
SIN6_0	Multi-function serial ch.6 serial data input pin (0)	39	56	70	
SIN6_1	Multi-function serial ch.6 serial data input pin (1)	-	-	143	
SOT6_0	Multi-function serial ch.6 serial data output pin (0)	40	57	71	
SOT6_1	Multi-function serial ch.6 serial data output pin (1)	-	-	142	
SCS60_0	Multi-function serial ch.6 serial chip select 0 I/O pin (0)	34	48	59	
SCS60_1	Multi-function serial ch.6 serial chip select 0 I/O pin (1)	87	121	149	
SCS60_2	Multi-function serial ch.6 serial chip select 0 I/O pin (2)	-	116	144	
SCS61_0	Multi-function serial ch.6 serial chip select 1 output pin (0)	-	49	60	

Port Name	Description	Pin No. of Package			Remark
		LQFP 100	LQFP 144	TEQFP 176	
SCS61_1	Multi-function serial ch.6 serial chip select 1 output pin (1)	88	122	150	
SCS62_0	Multi-function serial ch.6 serial chip select 2 output pin (0)	35	50	62	
SCS62_1	Multi-function serial ch.6 serial chip select 2 output pin (1)	93	127	155	
SCS63_0	Multi-function serial ch.6 serial chip select 3 output pin (0)	36	51	63	
SCS63_1	Multi-function serial ch.6 serial chip select 3 output pin (1)	94	128	156	
SCK7_0	Multi-function serial ch.7 clock I/O pin (0)	72	102	124	
SCK7_1	Multi-function serial ch.7 clock I/O pin (1)	-	133	161	
SIN7_0	Multi-function serial ch.7 serial data input pin (0)	-	106	129	
SIN7_1	Multi-function serial ch.7 serial data input pin (1)	98	139	170	
SIN7_2	Multi-function serial ch.7 serial data input pin (2)	-	104	127	
SIN7_3	Multi-function serial ch.7 serial data input pin (3)	70	99	119	
SOT7_0	Multi-function serial ch.7 serial data output pin (0)	71	101	123	
SOT7_1	Multi-function serial ch.7 serial data output pin (1)	-	140	171	
SCS70_0	Multi-function serial ch.7 serial chip select 0 I/O pin (0)	73	103	125	
SCS70_1	Multi-function serial ch.7 serial chip select 0 I/O pin (1)	-	-	164	
SCS71_0	Multi-function serial ch.7 serial chip select 1 output pin (0)	-	100	122	
SCS71_1	Multi-function serial ch.7 serial chip select 1 output pin (1)	-	136	165	
SCS72_0	Multi-function serial ch.7 serial chip select 2 output pin (0)	69	97	117	
SCS72_1	Multi-function serial ch.7 serial chip select 2 output pin (1)	-	-	166	
SCS73_0	Multi-function serial ch.7 serial chip select 3 output pin (0)	-	96	116	
SCS73_1	Multi-function serial ch.7 serial chip select 3 output pin (1)	97	137	167	
SCK8_0	Multi-function serial ch.8 clock I/O pin (0)	7	11	14	
SIN8_0	Multi-function serial ch.8 serial data input pin (0)	-	9	11	
SIN8_1	Multi-function serial ch.8 serial data input pin (1)	4	6	8	
SIN8_2	Multi-function serial ch.8 serial data input pin (2)	10	14	18	
SOT8_0	Multi-function serial ch.8 serial data output pin (0)	6	10	12	
SCS80_0	Multi-function serial ch.8 serial chip select 0 I/O pin (0)	8	12	15	
SCS81_0	Multi-function serial ch.8 serial chip select 1 output pin (0)	9	13	17	
SCS82_0	Multi-function serial ch.8 serial chip select 2 output pin (0)	10	14	18	
SCS83_0	Multi-function serial ch.8 serial chip select 3 output pin (0)	-	15	19	
SCS83_1	Multi-function serial ch.8 serial chip select 3 output pin (1)	3	5	7	
SCK9_0	Multi-function serial ch.9 clock I/O pin (0)	-	133	161	
SCK9_1	Multi-function serial ch.9 clock I/O pin (1)	93	127	155	
SIN9_0	Multi-function serial ch.9 serial data input pin (0)	95	131	159	
SOT9_0	Multi-function serial ch.9 serial data output pin (0)	-	132	160	
SOT9_1	Multi-function serial ch.9 serial data output pin (1)	94	128	156	
SCS90_0	Multi-function serial ch.9 serial chip select 0 I/O pin (0)	94	128	156	
SCS90_1	Multi-function serial ch.9 serial chip select 0 I/O pin (1)	-	130	158	
SCK10_0	Multi-function serial ch.10 clock I/O pin (0)	61	85	104	
SIN10_0	Multi-function serial ch.10 serial data input pin (0)	63	87	106	
SOT10_0	Multi-function serial ch.10 serial data output pin (0)	62	86	105	
SCS100_0	Multi-function serial ch.10 serial chip select 0 I/O pin (0)	64	91	110	
SCS100_1	Multi-function serial ch.10 serial chip select 0 I/O pin (1)	67	94	114	

Port Name	Description	Pin No. of Package			Remark
		LQFP 100	LQFP 144	TEQFP 176	
SCS101_0	Multi-function serial ch.10 serial chip select 1 output pin (0)	-	90	109	
SCS101_1	Multi-function serial ch.10 serial chip select 1 output pin (1)	66	93	113	
SCS102_0	Multi-function serial ch.10 serial chip select 2 output pin (0)	-	89	108	
SCS102_1	Multi-function serial ch.10 serial chip select 2 output pin (1)	65	92	111	
SCS103_0	Multi-function serial ch.10 serial chip select 3 output pin (0)	-	88	107	
SCK11_0	Multi-function serial ch.11 clock I/O pin (0)	24	35	43	
SIN11_0	Multi-function serial ch.11 serial data input pin (0)	22	33	41	
SIN11_1	Multi-function serial ch.11 serial data input pin (1)	24	35	43	
SOT11_0	Multi-function serial ch.11 serial data output pin (0)	23	34	42	
SOT11_1	Multi-function serial ch.11 serial data output pin (1)	-	40	50	
SCS110_0	Multi-function serial ch.11 serial chip select 0 I/O pin (0)	-	-	47	
SCS110_1	Multi-function serial ch.11 serial chip select 0 I/O pin (1)	20	31	39	
SCK12_0	Multi-function serial ch.12 clock I/O pin (0)	-	40	50	
SCK12_1	Multi-function serial ch.12 clock I/O pin (1)	5	7	9	
SCK12_2	Multi-function serial ch.12 clock I/O pin (2)	33	46	57	
SIN12_0	Multi-function serial ch.12 serial data input pin (0)	-	-	48	
SIN12_1	Multi-function serial ch.12 serial data input pin (1)	-	-	13	
SIN12_2	Multi-function serial ch.12 serial data input pin (2)	27	38	46	
SOT12_0	Multi-function serial ch.12 serial data output pin (0)	28	39	49	
SOT12_1	Multi-function serial ch.12 serial data output pin (1)	-	-	16	
SCS120_0	Multi-function serial ch.12 serial chip select 0 I/O pin (0)	29	41	51	
SCS120_1	Multi-function serial ch.12 serial chip select 0 I/O pin (1)	-	8	10	
SCK13_0	Multi-function serial ch.13 clock I/O pin (0)	-	-	66	
SIN13_0	Multi-function serial ch.13 serial data input pin (0)	-	-	64	
SOT13_0	Multi-function serial ch.13 serial data output pin (0)	-	-	65	
SCS130_0	Multi-function serial ch.13 serial chip select 0 I/O pin (0)	-	-	61	
SCL0_0	I ² C ch.0 clock I/O pin (0)	12	19	23	
SDA0_0	I ² C ch.0 serial data I/O pin (0)	11	18	22	
SCL1_0	I ² C ch.1 clock I/O pin (0)	18	28	34	
SDA1_0	I ² C ch.1 serial data I/O pin (0)	16	25	31	
SCL2_0	I ² C ch.2 clock I/O pin (0)	-	136	165	
SCL2_1	I ² C ch.2 clock I/O pin (1)	99	142	174	
SDA2_0	I ² C ch.2 serial data I/O pin (0)	96	135	163	
SCL3_0	I ² C ch.3 clock I/O pin (0)	5	7	9	
SDA3_0	I ² C ch.3 serial data I/O pin (0)	4	6	8	
SCL4_0	I ² C ch.4 clock I/O pin (0)	44	63	79	
SDA4_0	I ² C ch.4 serial data I/O pin (0)	45	65	81	
SCL5_0	I ² C ch.5 clock I/O pin (0)	57	81	100	
SDA5_0	I ² C ch.5 serial data I/O pin (0)	56	80	99	
SCL6_0	I ² C ch.6 clock I/O pin (0)	41	58	74	
SDA6_0	I ² C ch.6 serial data I/O pin (0)	40	57	71	
SCL7_0	I ² C ch.7 clock I/O pin (0)	72	102	124	

Port Name	Description	Pin No. of Package			Remark
		LQFP 100	LQFP 144	TEQFP 176	
SDA7_0	I ² C ch.7 serial data I/O pin (0)	71	101	123	
SCL8_0	I ² C ch.8 clock I/O pin (0)	7	11	14	
SDA8_0	I ² C ch.8 serial data I/O pin (0)	6	10	12	
SCL9_0	I ² C ch.9 clock I/O pin (0)	-	133	161	
SCL9_1	I ² C ch.9 clock I/O pin (1)	93	127	155	
SDA9_0	I ² C ch.9 serial data I/O pin (0)	-	132	160	
SDA9_1	I ² C ch.9 serial data I/O pin (1)	94	128	156	
SCL10_0	I ² C ch.10 clock I/O pin (0)	61	85	104	
SDA10_0	I ² C ch.10 serial data I/O pin (0)	62	86	105	
SCL11_0	I ² C ch.11 clock I/O pin (0)	24	35	43	
SDA11_0	I ² C ch.11 serial data I/O pin (0)	23	34	42	
SCL12_0	I ² C ch.12 clock I/O pin (0)	-	40	50	
SCL12_1	I ² C ch.12 clock I/O pin (1)	33	46	57	
SDA12_0	I ² C ch.12 serial data I/O pin (0)	28	39	49	
SCL13_0	I ² C ch.13 clock I/O pin (0)	-	-	66	
SDA13_0	I ² C ch.13 serial data I/O pin (0)	-	-	65	
TEXT0_0	Free-run timer ch.0 clock input pin (0)	-	17	21	
TEXT0_1	Free-run timer ch.0 clock input pin (1)	14	23	29	
TEXT1_0	Free-run timer ch.1 clock input pin (0)	11	18	22	
TEXT1_1	Free-run timer ch.1 clock input pin (1)	-	53	67	
TEXT2_0	Free-run timer ch.2 clock input pin (0)	-	74	92	
TEXT2_1	Free-run timer ch.2 clock input pin (1)	38	54	68	
TEXT3_0	Free-run timer ch.3 clock input pin (0)	-	75	93	
TEXT3_1	Free-run timer ch.3 clock input pin (1)	43	61	77	
TEXT4_0	Free-run timer ch.4 clock input pin (0)	66	93	113	
TEXT4_1	Free-run timer ch.4 clock input pin (1)	-	62	78	
TEXT8_0	Free-run timer ch.8 clock input pin (0)	67	94	114	
TEXT8_1	Free-run timer ch.8 clock input pin (1)	44	63	79	
TEXT9_0	Free-run timer ch.9 clock input pin (0)	41	58	74	
TEXT10_0	Free-run timer ch.10 clock input pin (0)	-	-	73	
IN0_0	Input capture ch.0 input pin (0)	93	127	155	
IN0_1	Input capture ch.0 input pin (1)	-	98	118	
IN0_2	Input capture ch.0 input pin (2)	-	66	82	
IN1_0	Input capture ch.1 input pin (0)	94	128	156	
IN1_1	Input capture ch.1 input pin (1)	70	99	119	
IN1_2	Input capture ch.1 input pin (2)	46	67	83	
IN2_0	Input capture ch.2 input pin (0)	-	129	157	
IN2_1	Input capture ch.2 input pin (1)	-	100	122	
IN2_2	Input capture ch.2 input pin (2)	-	68	84	
IN2_3	Input capture ch.2 input pin (3)	96	135	163	
IN3_0	Input capture ch.3 input pin (0)	-	130	158	

Port Name	Description	Pin No. of Package			Remark
		LQFP 100	LQFP 144	TEQFP 176	
IN3_1	Input capture ch.3 input pin (1)	71	101	123	
IN3_2	Input capture ch.3 input pin (2)	58	82	101	
IN4_0	Input capture ch.4 input pin (0)	95	131	159	
IN4_1	Input capture ch.4 input pin (1)	72	102	124	
IN4_2	Input capture ch.4 input pin (2)	59	83	102	
IN5_0	Input capture ch.5 input pin (0)	98	139	170	
IN5_1	Input capture ch.5 input pin (1)	73	103	125	
IN5_2	Input capture ch.5 input pin (2)	60	84	103	
IN16_0	Input capture ch.16 input pin (0)	3	5	7	
IN16_1	Input capture ch.16 input pin (1)	-	55	69	
IN16_2	Input capture ch.16 input pin (2)	52	76	94	
IN17_0	Input capture ch.17 input pin (0)	4	6	8	
IN17_1	Input capture ch.17 input pin (1)	39	56	70	
IN17_2	Input capture ch.17 input pin (2)	53	77	96	
IN18_0	Input capture ch.18 input pin (0)	5	7	9	
IN18_1	Input capture ch.18 input pin (1)	40	57	71	
IN18_2	Input capture ch.18 input pin (2)	54	78	97	
IN19_0	Input capture ch.19 input pin (0)	-	8	10	
IN19_1	Input capture ch.19 input pin (1)	41	58	74	
IN19_2	Input capture ch.19 input pin (2)	55	79	98	
IN20_0	Input capture ch.20 input pin (0)	-	9	11	
IN20_1	Input capture ch.20 input pin (1)	-	59	75	
IN20_2	Input capture ch.20 input pin (2)	56	80	99	
IN21_0	Input capture ch.21 input pin (0)	6	10	12	
IN21_1	Input capture ch.21 input pin (1)	42	60	76	
IN21_2	Input capture ch.21 input pin (2)	57	81	100	
OUT0_0	Output compare ch.0 output pin (0)	63	87	106	
OUT0_1	Output compare ch.0 output pin (1)	15	24	30	
OUT1_0	Output compare ch.1 output pin (0)	-	88	107	
OUT1_1	Output compare ch.1 output pin (1)	16	25	31	
OUT2_0	Output compare ch.2 output pin (0)	-	89	108	
OUT2_1	Output compare ch.2 output pin (1)	-	26	32	
OUT2_2	Output compare ch.2 output pin (2)	12	19	23	
OUT3_0	Output compare ch.3 output pin (0)	-	90	109	
OUT3_1	Output compare ch.3 output pin (1)	17	27	33	
OUT4_0	Output compare ch.4 output pin (0)	64	91	110	
OUT4_1	Output compare ch.4 output pin (1)	18	28	34	
OUT5_0	Output compare ch.5 output pin (0)	7	11	14	
OUT5_1	Output compare ch.5 output pin (1)	-	29	35	
OUT5_2	Output compare ch.5 output pin (2)	13	20	24	
OUT16_0	Output compare ch.16 output pin (0)	8	12	15	

Port Name	Description	Pin No. of Package			Remark
		LQFP 100	LQFP 144	TEQFP 176	
OUT16_1	Output compare ch.16 output pin (1)	19	30	37	
OUT17_0	Output compare ch.17 output pin (0)	9	13	17	
OUT17_1	Output compare ch.17 output pin (1)	20	31	39	
OUT18_0	Output compare ch.18 output pin (0)	10	14	18	
OUT18_1	Output compare ch.18 output pin (1)	21	32	40	
OUT19_0	Output compare ch.19 output pin (0)	-	15	19	
OUT19_1	Output compare ch.19 output pin (1)	22	33	41	
OUT20_0	Output compare ch.20 output pin (0)	-	16	20	
OUT20_1	Output compare ch.20 output pin (1)	23	34	42	
OUT21_0	Output compare ch.21 output pin (0)	-	17	21	
OUT21_1	Output compare ch.21 output pin (1)	24	35	43	
TIOA0_0	Base timer ch.0 TIOA output pin (0)	-	8	10	
TIOA0_1	Base timer ch.0 TIOA output pin (1)	-	-	4	
TIOA1_0	Base timer ch.1 TIOA I/O pin (0)	-	9	11	
TIOA1_1	Base timer ch.1 TIOA I/O pin (1)	-	-	6	
TIOB0_0	Base timer ch.0 TIOB input pin (0)	-	17	21	
TIOB1_0	Base timer ch.1 TIOB input pin (0)	11	18	22	
TIOA2_0	Base timer ch.2 TIOA output pin (0)	6	10	12	
TIOA2_1	Base timer ch.2 TIOA output pin (1)	-	-	13	
TIOA3_0	Base timer ch.3 TIOA I/O pin (0)	7	11	14	
TIOA3_1	Base timer ch.3 TIOA I/O pin (1)	-	-	16	
TIOB2_0	Base timer ch.2 TIOB input pin (0)	12	19	23	
TIOB3_0	Base timer ch.3 TIOB input pin (0)	13	20	24	
TIOA4_0	Base timer ch.4 TIOA output pin (0)	8	12	15	
TIOA4_1	Base timer ch.4 TIOA output pin (1)	14	23	29	
TIOA5_0	Base timer ch.5 TIOA I/O pin (0)	9	13	17	
TIOA5_1	Base timer ch.5 TIOA I/O pin (1)	-	40	50	
TIOB4_0	Base timer ch.4 TIOB input pin (0)	-	21	25	
TIOB5_0	Base timer ch.5 TIOB input pin (0)	-	22	26	
TIOA6_0	Base timer ch.6 TIOA output pin (0)	10	14	18	
TIOA6_1	Base timer ch.6 TIOA output pin (1)	29	41	51	
TIOA7_0	Base timer ch.7 TIOA I/O pin (0)	-	15	19	
TIOA7_1	Base timer ch.7 TIOA I/O pin (1)	72	102	124	
TIOB6_0	Base timer ch.6 TIOB input pin (0)	14	23	29	
TIOB7_0	Base timer ch.7 TIOB input pin (0)	15	24	30	
TIOA8_0	Base timer ch.8 TIOA output pin (0)	-	16	20	
TIOA8_1	Base timer ch.8 TIOA output pin (1)	73	103	125	
TIOA9_0	Base timer ch.9 TIOA I/O pin (0)	20	31	39	
TIOA9_1	Base timer ch.9 TIOA I/O pin (1)	-	104	127	
TIOB8_0	Base timer ch.8 TIOB input pin (0)	-	26	32	
TIOB9_0	Base timer ch.9 TIOB input pin (0)	19	30	37	

Port Name	Description	Pin No. of Package			Remark
		LQFP 100	LQFP 144	TEQFP 176	
TIOA10_0	Base timer ch.10 TIOA output pin (0)	22	33	41	
TIOA10_1	Base timer ch.10 TIOA output pin (1)	-	105	128	
TIOA11_0	Base timer ch.11 TIOA I/O pin (0)	23	34	42	
TIOA11_1	Base timer ch.11 TIOA I/O pin (1)	35	50	62	
TIOB10_0	Base timer ch.10 TIOB input pin (0)	-	45	55	
TIOB11_0	Base timer ch.11 TIOB input pin (0)	33	46	57	
TIOA12_0	Base timer ch.12 TIOA output pin (0)	24	35	43	
TIOA12_1	Base timer ch.12 TIOA output pin (1)	36	51	63	
TIOA13_0	Base timer ch.13 TIOA I/O pin (0)	28	39	49	
TIOA13_1	Base timer ch.13 TIOA I/O pin (1)	-	68	84	
TIOB12_0	Base timer ch.12 TIOB input pin (0)	-	47	58	
TIOB13_0	Base timer ch.13 TIOB input pin (0)	34	48	59	
TIOA14_0	Base timer ch.14 TIOA output pin (0)	-	-	61	
TIOA14_1	Base timer ch.14 TIOA output pin (1)	58	82	101	
TIOA15_0	Base timer ch.15 TIOA I/O pin (0)	-	-	64	
TIOA15_1	Base timer ch.15 TIOA I/O pin (1)	59	83	102	
TIOB14_0	Base timer ch.14 TIOB input pin (0)	-	74	92	
TIOB15_0	Base timer ch.15 TIOB input pin (0)	-	75	93	
TIOA16_0	Base timer ch.16 TIOA output pin (0)	-	-	65	
TIOA16_1	Base timer ch.16 TIOA output pin (1)	60	84	103	
TIOA17_0	Base timer ch.17 TIOA I/O pin (0)	-	-	72	
TIOA17_1	Base timer ch.17 TIOA I/O pin (1)	57	81	100	
TIOB16_0	Base timer ch.16 TIOB input pin (0)	52	76	94	
TIOB17_0	Base timer ch.17 TIOB input pin (0)	56	80	99	
TIOA18_0	Base timer ch.18 TIOA output pin (0)	-	-	73	
TIOA18_1	Base timer ch.18 TIOA output pin (1)	64	91	110	
TIOA19_0	Base timer ch.19 TIOA I/O pin (0)	-	64	80	
TIOA19_1	Base timer ch.19 TIOA I/O pin (1)	65	92	111	
TIOB18_0	Base timer ch.18 TIOB input pin (0)	69	97	117	
TIOB19_0	Base timer ch.19 TIOB input pin (0)	-	59	75	
TIOA20_0	Base timer ch.20 TIOA output pin (0)	45	65	81	
TIOA20_1	Base timer ch.20 TIOA output pin (1)	66	93	113	
TIOA21_0	Base timer ch.21 TIOA I/O pin (0)	-	66	82	
TIOA21_1	Base timer ch.21 TIOA I/O pin (1)	-	-	126	
TIOB20_0	Base timer ch.20 TIOB input pin (0)	42	60	76	
TIOB21_0	Base timer ch.21 TIOB input pin (0)	43	61	77	
TIOA22_0	Base timer ch.22 TIOA output pin (0)	46	67	83	
TIOA22_1	Base timer ch.22 TIOA output pin (1)	98	139	170	
TIOA23_0	Base timer ch.23 TIOA I/O pin (0)	61	85	104	
TIOA23_1	Base timer ch.23 TIOA I/O pin (1)	-	140	171	
TIOB22_0	Base timer ch.22 TIOB input pin (0)	-	62	78	

Port Name	Description	Pin No. of Package			Remark
		LQFP 100	LQFP 144	TEQFP 176	
TIOB23_0	Base timer ch.23 TIOB input pin (0)	-	141	172	
TIOA24_0	Base timer ch.24 TIOA output pin (0)	62	86	105	
TIOA24_1	Base timer ch.24 TIOA output pin (1)	96	135	163	
TIOA25_0	Base timer ch.25 TIOA I/O pin (0)	63	87	106	
TIOA25_1	Base timer ch.25 TIOA I/O pin (1)	-	-	166	
TIOB24_0	Base timer ch.24 TIOB input pin (0)	-	136	165	
TIOB25_0	Base timer ch.25 TIOB input pin (0)	-	100	122	
TIOA26_0	Base timer ch.26 TIOA output pin (0)	-	88	107	
TIOA26_1	Base timer ch.26 TIOA output pin (1)	-	-	169	
TIOA27_0	Base timer ch.27 TIOA I/O pin (0)	-	89	108	
TIOA27_1	Base timer ch.27 TIOA I/O pin (1)	-	-	173	
TIOB26_0	Base timer ch.26 TIOB input pin (0)	71	101	123	
TIOB27_0	Base timer ch.27 TIOB input pin (0)	72	102	124	
TIOA28_0	Base timer ch.28 TIOA output pin (0)	-	90	109	
TIOA28_1	Base timer ch.28 TIOA output pin (1)	-	98	118	
TIOA29_0	Base timer ch.29 TIOA I/O pin (0)	67	94	114	
TIOA29_1	Base timer ch.29 TIOA I/O pin (1)	70	99	119	
TIOB28_0	Base timer ch.28 TIOB input pin (0)	73	103	125	
TIOB29_0	Base timer ch.29 TIOB input pin (0)	-	104	127	
TIOA30_0	Base timer ch.30 TIOA output pin (0)	16	25	31	
TIOA31_0	Base timer ch.31 TIOA I/O pin (0)	17	27	33	
TIOB30_0	Base timer ch.30 TIOB input pin (0)	18	28	34	
TIOB31_0	Base timer ch.31 TIOB input pin (0)	21	32	40	
TIOA32_0	Base timer ch.32 TIOA output pin (0)	29	41	51	
TIOA33_0	Base timer ch.33 TIOA I/O pin (0)	27	38	46	
TIOB32_0	Base timer ch.32 TIOB input pin (0)	35	50	62	
TIOB33_0	Base timer ch.33 TIOB input pin (0)	-	49	60	
TIOA34_0	Base timer ch.34 TIOA output pin (0)	36	51	63	
TIOA35_0	Base timer ch.35 TIOA I/O pin (0)	37	52	66	
TIOB34_0	Base timer ch.34 TIOB input pin (0)	38	54	68	
TIOB35_0	Base timer ch.35 TIOB input pin (0)	-	53	67	
TIOA36_0	Base timer ch.36 TIOA output pin (0)	41	58	74	
TIOA37_0	Base timer ch.37 TIOA I/O pin (0)	40	57	71	
TIOB36_0	Base timer ch.36 TIOB input pin (0)	39	56	70	
TIOB37_0	Base timer ch.37 TIOB input pin (0)	-	55	69	
TIOA38_0	Base timer ch.38 TIOA output pin (0)	44	63	79	
TIOA39_0	Base timer ch.39 TIOA I/O pin (0)	53	77	96	
TIOB38_0	Base timer ch.38 TIOB input pin (0)	-	68	84	
TIOB39_0	Base timer ch.39 TIOB input pin (0)	54	78	97	
TIOA40_0	Base timer ch.40 TIOA output pin (0)	55	79	98	
TIOA41_0	Base timer ch.41 TIOA I/O pin (0)	58	82	101	

Port Name	Description	Pin No. of Package			Remark
		LQFP 100	LQFP 144	TEQFP 176	
TIOB40_0	Base timer ch.40 TIOB input pin (0)	59	83	102	
TIOB41_0	Base timer ch.41 TIOB input pin (0)	60	84	103	
TIOA42_0	Base timer ch.42 TIOA output pin (0)	64	91	110	
TIOA43_0	Base timer ch.43 TIOA I/O pin (0)	65	92	111	
TIOB42_0	Base timer ch.42 TIOB input pin (0)	66	93	113	
TIOB43_0	Base timer ch.43 TIOB input pin (0)	-	96	116	
TIOA44_0	Base timer ch.44 TIOA output pin (0)	70	99	119	
TIOA45_0	Base timer ch.45 TIOA I/O pin (0)	74	107	131	
TIOB44_0	Base timer ch.44 TIOB input pin (0)	-	98	118	
TIOB45_0	Base timer ch.45 TIOB input pin (0)	82	115	141	
TIOA46_0	Base timer ch.46 TIOA output pin (0)	93	127	155	
TIOA47_0	Base timer ch.47 TIOA I/O pin (0)	94	128	156	
TIOB46_0	Base timer ch.46 TIOB input pin (0)	-	129	157	
TIOB47_0	Base timer ch.47 TIOB input pin (0)	-	130	158	
TIOA48_0	Base timer ch.48 TIOA output pin (0)	95	131	159	
TIOA49_0	Base timer ch.49 TIOA I/O pin (0)	-	132	160	
TIOB48_0	Base timer ch.48 TIOB input pin (0)	-	133	161	
TIOB49_0	Base timer ch.49 TIOB input pin (0)	-	134	162	
TIOA50_0	Base timer ch.50 TIOA output pin (0)	96	135	163	
TIOA51_0	Base timer ch.51 TIOA I/O pin (0)	-	-	164	
TIOB50_0	Base timer ch.50 TIOB input pin (0)	97	137	167	
TIOB51_0	Base timer ch.51 TIOB input pin (0)	-	138	168	
TIOA52_0	Base timer ch.52 TIOA output pin (0)	98	139	170	
TIOA53_0	Base timer ch.53 TIOA I/O pin (0)	-	140	171	
TIOB52_0	Base timer ch.52 TIOB input pin (0)	99	142	174	
TIOB53_0	Base timer ch.53 TIOB input pin (0)	-	143	175	
TIOA54_0	Base timer ch.54 TIOA output pin (0)	2	3	3	
TIOA55_0	Base timer ch.55 TIOA I/O pin (0)	3	5	7	
TIOB54_0	Base timer ch.54 TIOB input pin (0)	4	6	8	
TIOB55_0	Base timer ch.55 TIOB input pin (0)	5	7	9	
TIOA56_0	Base timer ch.56 TIOA output pin (0)	-	29	35	
TIOA57_0	Base timer ch.57 TIOA I/O pin (0)	-	-	36	
TIOB56_0	Base timer ch.56 TIOB input pin (0)	-	-	47	
TIOB57_0	Base timer ch.57 TIOB input pin (0)	-	-	48	
TIOA58_0	Base timer ch.58 TIOA output pin (0)	-	-	90	
TIOA59_0	Base timer ch.59 TIOA I/O pin (0)	-	-	120	
TIOB58_0	Base timer ch.58 TIOB input pin (0)	-	-	91	
TIOB59_0	Base timer ch.59 TIOB input pin (0)	-	-	121	
TIOA60_0	Base timer ch.60 TIOA output pin (0)	-	106	129	
TIOA61_0	Base timer ch.61 TIOA I/O pin (0)	-	-	139	
TIOB60_0	Base timer ch.60 TIOB input pin (0)	-	-	130	

Port Name	Description	Pin No. of Package			Remark
		LQFP 100	LQFP 144	TEQFP 176	
TIOB61_0	Base timer ch.61 TIOB input pin (0)	-	-	140	
TIOA62_0	Base timer ch.62 TIOA output pin (0)	-	116	144	
TIOA63_0	Base timer ch.63 TIOA I/O pin (0)	-	2	2	
TIOB62_0	Base timer ch.62 TIOB input pin (0)	-	-	143	
TIOB63_0	Base timer ch.63 TIOB input pin (0)	-	4	5	
AIN8_0	Quad Position & Revolution Counter ch.8 AIN input pin (0)	-	2	2	
AIN8_1	Quad Position & Revolution Counter ch.8 AIN input pin (1)	-	59	75	
AIN8_2	Quad Position & Revolution Counter ch.8 AIN input pin (2)	6	10	12	
BIN8_0	Quad Position & Revolution Counter ch.8 BIN input pin (0)	2	3	3	
BIN8_1	Quad Position & Revolution Counter ch.8 BIN input pin (1)	42	60	76	
BIN8_2	Quad Position & Revolution Counter ch.8 BIN input pin (2)	7	11	14	
ZIN8_0	Quad Position & Revolution Counter ch.8 ZIN input pin (0)	-	4	5	
ZIN8_1	Quad Position & Revolution Counter ch.8 ZIN input pin (1)	43	61	77	
ZIN8_2	Quad Position & Revolution Counter ch.8 ZIN input pin (2)	8	12	15	
AIN9_0	Quad Position & Revolution Counter ch.9 AIN input pin (0)	3	5	7	
AIN9_1	Quad Position & Revolution Counter ch.9 AIN input pin (1)	54	78	97	
BIN9_0	Quad Position & Revolution Counter ch.9 BIN input pin (0)	4	6	8	
BIN9_1	Quad Position & Revolution Counter ch.9 BIN input pin (1)	55	79	98	
ZIN9_0	Quad Position & Revolution Counter ch.9 ZIN input pin (0)	5	7	9	
ZIN9_1	Quad Position & Revolution Counter ch.9 ZIN input pin (1)	56	80	99	
TIN0_0	Reload timer ch.0 event input pin (0)	21	32	40	
TIN0_1	Reload timer ch.0 event input pin (1)	52	76	94	
TOT0_0	Reload timer ch.0 output pin (0)	22	33	41	
TOT0_1	Reload timer ch.0 output pin (1)	54	78	97	
TIN1_0	Reload timer ch.1 event input pin (0)	23	34	42	
TIN1_1	Reload timer ch.1 event input pin (1)	57	81	100	
TOT1_0	Reload timer ch.1 output pin (0)	24	35	43	
TOT1_1	Reload timer ch.1 output pin (1)	61	85	104	
TIN2_0	Reload timer ch.2 event input pin (0)	28	39	49	
TIN2_1	Reload timer ch.2 event input pin (1)	62	86	105	
TOT2_0	Reload timer ch.2 output pin (0)	-	40	50	
TOT2_1	Reload timer ch.2 output pin (1)	63	87	106	
TIN3_0	Reload timer ch.3 event input pin (0)	29	41	51	
TIN3_1	Reload timer ch.3 event input pin (1)	64	91	110	
TOT3_0	Reload timer ch.3 output pin (0)	-	45	55	
TOT3_1	Reload timer ch.3 output pin (1)	65	92	111	
TIN16_0	Reload timer ch.16 event input pin (0)	33	46	57	
TIN16_1	Reload timer ch.16 event input pin (1)	66	93	113	
TOT16_0	Reload timer ch.16 output pin (0)	-	47	58	
TOT16_1	Reload timer ch.16 output pin (1)	67	94	114	
TIN17_0	Reload timer ch.17 event input pin (0)	34	48	59	
TIN17_1	Reload timer ch.17 event input pin (1)	69	97	117	

Port Name	Description	Pin No. of Package			Remark
		LQFP 100	LQFP 144	TEQFP 176	
TOT17_0	Reload timer ch.17 output pin (0)	-	49	60	
TOT17_1	Reload timer ch.17 output pin (1)	70	99	119	
WOT	RTC overflow output pin	82	115	141	
CLK_CLKO	Clock monitor output pin	27	38	46	
TRACECLK_0	Trace clock output pin (0)	99	142	174	
TRACECLK_1	Trace clock output pin (1)	74	107	131	
TRACECTL_0	Trace control output pin (0)	-	143	175	
TRACECTL_1	Trace control output pin (1)	73	103	125	
TRACEDATA0_0	Trace data 0 output pin (0)	-	129	157	
TRACEDATA0_1	Trace data 0 output pin (1)	72	102	124	
TRACEDATA1_0	Trace data 1 output pin (0)	-	130	158	
TRACEDATA1_1	Trace data 1 output pin (1)	71	101	123	
TRACEDATA2_0	Trace data 2 output pin (0)	95	131	159	
TRACEDATA2_1	Trace data 2 output pin (1)	70	99	119	
TRACEDATA3_0	Trace data 3 output pin (0)	-	132	160	
TRACEDATA3_1	Trace data 3 output pin (1)	69	97	117	
TRACEDATA4_0	Trace data 4 output pin (0)	-	133	161	
TRACEDATA4_1	Trace data 4 output pin (1)	67	94	114	
TRACEDATA5_0	Trace data 5 output pin (0)	-	134	162	
TRACEDATA5_1	Trace data 5 output pin (1)	66	93	113	
TRACEDATA6_0	Trace data 6 output pin (0)	96	135	163	
TRACEDATA6_1	Trace data 6 output pin (1)	65	92	111	
TRACEDATA7_0	Trace data 7 output pin (0)	-	136	165	
TRACEDATA7_1	Trace data 7 output pin (1)	64	91	110	
TRST	JTAG test reset input pin	81	114	138	
TCK	JTAG test clock input pin	78	111	135	
TDI	JTAG test data input pin	80	113	137	
TDO	JTAG test data output pin	77	110	134	
TMS	JTAG test mode state input pin	79	112	136	
P000	General-purpose I/O port	-	2	2	
P001	General-purpose I/O port	2	3	3	
P002	General-purpose I/O port	-	-	4	
P003	General-purpose I/O port	-	4	5	
P004	General-purpose I/O port	-	-	6	
P005	General-purpose I/O port	3	5	7	
P006	General-purpose I/O port	4	6	8	
P007	General-purpose I/O port	5	7	9	
P008	General-purpose I/O port	-	8	10	
P009	General-purpose I/O port	-	9	11	
P010	General-purpose I/O port	6	10	12	
P011	General-purpose I/O port	-	-	13	

Port Name	Description	Pin No. of Package			Remark
		LQFP 100	LQFP 144	TEQFP 176	
P012	General-purpose I/O port	7	11	14	
P013	General-purpose I/O port	8	12	15	
P014	General-purpose I/O port	-	-	16	
P015	General-purpose I/O port	9	13	17	
P016	General-purpose I/O port	10	14	18	
P017	General-purpose I/O port	-	15	19	
P018	General-purpose I/O port	-	16	20	
P019	General-purpose I/O port	-	17	21	
P020	General-purpose I/O port	11	18	22	
P021	General-purpose I/O port	12	19	23	
P022	General-purpose I/O port	13	20	24	
P023	General-purpose I/O port	-	21	25	
P024	General-purpose I/O port	-	22	26	
P025	General-purpose I/O port	-	-	27	
P026	General-purpose I/O port	-	-	28	
P027	General-purpose I/O port	14	23	29	
P028	General-purpose I/O port	15	24	30	
P029	General-purpose I/O port	16	25	31	
P030	General-purpose I/O port	-	26	32	
P031	General-purpose I/O port	17	27	33	
P100	General-purpose I/O port	18	28	34	
P101	General-purpose I/O port	-	29	35	
P102	General-purpose I/O port	-	-	36	
P103	General-purpose I/O port	19	30	37	
P104	General-purpose I/O port	-	-	38	
P105	General-purpose I/O port	20	31	39	
P106	General-purpose I/O port	21	32	40	
P107	General-purpose I/O port	22	33	41	
P108	General-purpose I/O port	23	34	42	
P109	General-purpose I/O port	24	35	43	
P110	General-purpose I/O port	-	-	47	
P111	General-purpose I/O port	-	-	48	
P112	General-purpose I/O port	28	39	49	
P113	General-purpose I/O port	-	40	50	
P114	General-purpose I/O port	29	41	51	
P115	General-purpose I/O port	-	45	55	
P116	General-purpose I/O port	-	-	56	
P117	General-purpose I/O port	33	46	57	
P118	General-purpose I/O port	-	47	58	
P119	General-purpose I/O port	34	48	59	
P120	General-purpose I/O port	-	49	60	

Port Name	Description	Pin No. of Package			Remark
		LQFP 100	LQFP 144	TEQFP 176	
P121	General-purpose I/O port	-	-	61	
P122	General-purpose I/O port	35	50	62	
P123	General-purpose I/O port	36	51	63	
P124	General-purpose I/O port	-	-	64	
P125	General-purpose I/O port	-	-	65	
P126	General-purpose I/O port	37	52	66	
P127	General-purpose I/O port	-	53	67	
P128	General-purpose I/O port	38	54	68	
P129	General-purpose I/O port	-	55	69	
P130	General-purpose I/O port	39	56	70	
P131	General-purpose I/O port	40	57	71	
P200	General-purpose I/O port	-	-	72	
P201	General-purpose I/O port	-	-	73	
P202	General-purpose I/O port	41	58	74	
P203	General-purpose I/O port	-	59	75	
P204	General-purpose I/O port	42	60	76	
P205	General-purpose I/O port	43	61	77	
P206	General-purpose I/O port	-	62	78	
P207	General-purpose I/O port	44	63	79	
P208	General-purpose I/O port	-	64	80	
P209	General-purpose I/O port	45	65	81	
P210	General-purpose I/O port	-	66	82	
P211	General-purpose I/O port	46	67	83	
P212	General-purpose I/O port	-	68	84	
P213	General-purpose I/O port	58	82	101	
P214	General-purpose I/O port	59	83	102	
P215	General-purpose I/O port	60	84	103	
P216	General-purpose I/O port	-	-	90	
P217	General-purpose I/O port	-	-	91	
P218	General-purpose I/O port	-	74	92	
P219	General-purpose I/O port	-	75	93	
P220	General-purpose I/O port	52	76	94	
P221	General-purpose I/O port	-	-	95	
P222	General-purpose I/O port	53	77	96	
P223	General-purpose I/O port	54	78	97	
P224	General-purpose I/O port	55	79	98	
P225	General-purpose I/O port	56	80	99	
P226	General-purpose I/O port	57	81	100	
P227	General-purpose I/O port	61	85	104	
P228	General-purpose I/O port	62	86	105	
P229	General-purpose I/O port	63	87	106	

Port Name	Description	Pin No. of Package			Remark
		LQFP 100	LQFP 144	TEQFP 176	
P230	General-purpose I/O port	-	88	107	
P231	General-purpose I/O port	-	89	108	
P300	General-purpose I/O port	-	90	109	
P301	General-purpose I/O port	64	91	110	
P302	General-purpose I/O port	65	92	111	
P303	General-purpose I/O port	-	-	112	
P304	General-purpose I/O port	66	93	113	
P305	General-purpose I/O port	67	94	114	
P306	General-purpose I/O port	-	96	116	
P307	General-purpose I/O port	69	97	117	
P308	General-purpose I/O port	-	98	118	
P309	General-purpose I/O port	70	99	119	
P310	General-purpose I/O port	-	-	120	
P311	General-purpose I/O port	-	-	121	
P312	General-purpose I/O port	-	100	122	
P313	General-purpose I/O port	71	101	123	
P314	General-purpose I/O port	72	102	124	
P315	General-purpose I/O port	73	103	125	
P316	General-purpose I/O port	-	-	126	
P317	General-purpose I/O port	-	104	127	
P318	General-purpose I/O port	-	105	128	
P319	General-purpose I/O port	-	106	129	
P320	General-purpose I/O port	-	-	130	
P321	General-purpose I/O port	74	107	131	
P322	General-purpose output port	77	110	134	
P323	General-purpose output port	80	113	137	
P324	General-purpose output port	81	114	138	
P325	General-purpose I/O port	-	-	139	
P326	General-purpose I/O port	-	-	140	
P327	General-purpose I/O port	82	115	141	
P328	General-purpose I/O port	-	-	142	
P329	General-purpose I/O port	-	-	143	
P330	General-purpose I/O port	-	116	144	
P331	General-purpose I/O port	87	121	149	
P400	General-purpose I/O port	88	122	150	
P401	General-purpose I/O port	93	127	155	
P402	General-purpose I/O port	94	128	156	
P403	General-purpose I/O port	-	129	157	
P404	General-purpose I/O port	-	130	158	
P405	General-purpose I/O port	95	131	159	
P406	General-purpose I/O port	-	132	160	

Port Name	Description	Pin No. of Package			Remark
		LQFP 100	LQFP 144	TEQFP 176	
P407	General-purpose I/O port	-	133	161	
P408	General-purpose I/O port	-	134	162	
P409	General-purpose I/O port	96	135	163	
P410	General-purpose I/O port	-	-	164	
P411	General-purpose I/O port	-	136	165	
P412	General-purpose I/O port	-	-	166	
P413	General-purpose I/O port	97	137	167	
P414	General-purpose I/O port	-	138	168	
P415	General-purpose I/O port	-	-	169	
P416	General-purpose I/O port	98	139	170	
P417	General-purpose I/O port	-	140	171	
P418	General-purpose I/O port	-	141	172	
P419	General-purpose I/O port	-	-	173	
P420	General-purpose I/O port	99	142	174	
P421	General-purpose I/O port	-	143	175	
P422	General-purpose I/O port	27	38	46	
AVCC0	Analog power supply pin for A/D converter unit 0	32	44	54	
AVCC1	Analog power supply pin for A/D converter unit 1	49	71	87	
AVSS0	GND pin for A/D converter unit 0	31	43	53	
AVSS1	GND pin for A/D converter unit 1	48	70	86	
AVRH0	Upper-limit reference voltage pin for A/D converter unit 0	30	42	52	
AVRH1	Upper-limit reference voltage pin for A/D converter unit 1	47	69	85	
AVRL0	Lower-limit reference voltage pin for A/D converter unit 0	31	43	53	
AVRL1	Lower-limit reference voltage pin for A/D converter unit 1	48	70	86	
C	External capacity connection output pin	92	126	154	
VCC	Power supply pin	25	36	44	
		50	72	88	
		76	109	133	
		90	124	152	
		100	144	176	
VSS	GND pin	1	1	1	
		26	37	45	
		51	73	89	
		75	108	132	
		86	120	148	
		91	125	153	

2. Remark

Note:

- *The port description list shows the port function of description which is mounted and supported on the product. The function which is not described in this table is not supported and assured.*
- *See the chapter of “Function List” on this manual as well.*
- *PWU function have restriction. Please see Note in the “5. Precautions for Using this Device” of chapter 24.*

CHAPTER 11: Port Configuration



This chapter explains the port configuration.

1. Overview
2. Configuration and Block Diagram
3. Operation
4. Registers
5. Precautions

CODE: PORT_CONFIGURATION-S6J3400-E2.1

1. Overview

This chapter explains the particular port configuration of the product PKG pins.

The microcontroller has various functions such as general purpose I/O ports, input or output timers, analog input ports and so on. Some of these functions are multiplexed implemented in a pin, and the assignment to a pin is particular for the product.

A port configuration is to determine which function and which input/output direction is applied to a port.

"3. Operation" of this chapter describes following.

- The particular port configurations of the resource input configuration register (RIC)
- The port output function configuration
- The analog I/O setting
- The input level setting
- The output drive capacity setting

See the common information of the registers on I/O Port.

2. Configuration and Block Diagram

See the “2. Configuration and Block Diagrams” of Chapter 22.

3. Operation

The relation between configuration and operation is described.

3.1. Resource Input Configuration

The resource input configuration (RIC) is a function to select input from an external or output from another internal resource as resource input. A resource which supports either a port input relocation or a resource inputs.

Register (Offset)	Resource	RESSEL[3:0] /PORTSEL L[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN002 (0x0004)	SCL0	RESSEL (0-7)	80ns noise filter disable	80ns noise filter enable	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN003 (0x0006)	SDA0	RESSEL (0-7)	80ns noise filter disable	80ns noise filter enable	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN004 (0x0008)	MFS0_TRIGGER	RESSEL (0-7)	TOT0	TOT1	TOT2	TOT3	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL L[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN005 (0x000A)	SCS0	RESSEL (0-7)	-	-	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	P023	P027	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN009 (0x0012)	SCL1	RESSEL (0-7)	80ns noise filter disable	80ns noise filter enable	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN010 (0x0014)	SDA1	RESSEL (0-7)	80ns noise filter disable	80ns noise filter enable	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN011 (0x0016)	MFS1_TRI GGER	RESSEL (0-7)	TOT0	TOT1	TOT2	TOT3	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN014 (0x001C)	SIN2	RESSEL (0-7)	-	-	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	P408	P421	P416	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL L[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN015 (0x001E)	SCK2	RESSEL (0-7)	-	-	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	P411	P420	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN016 (0x0020)	SCL2	RESSEL (0-7)	80ns noise filter disable	80ns noise filter enable	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	P411	P420	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN017 (0x0022)	SDA2	RESSEL (0-7)	80ns noise filter disable	80ns noise filter enable	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN018 (0x0024)	MFS2_TRI GGER	RESSEL (0-7)	TOT0	TOT1	TOT2	TOT3	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN019 (0x0026)	SCS20	RESSEL (0-7)	-	-	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	P413	P001	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL L[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN023 (0x002E)	SCL3	RESSEL (0-7)	80ns noise filter disable	80ns noise filter enable	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN024 (0x0030)	SDA3	RESSEL (0-7)	80ns noise filter disable	80ns noise filter enable	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN025 (0x0032)	MFS3_TRI GGER	RESSEL (0-7)	TOT0	TOT1	TOT2	TOT3	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN026 (0x0034)	SCS30	RESSEL (0-7)	-	-	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	P008	P001	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN028 (0x0038)	SIN4	RESSEL (0-7)	-	-	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	P210	P023	P205	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL L[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN029 (0x003A)	SCK4	RESSEL (0-7)	-	-	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	P207	P021	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN030 (0x003C)	SCL4	RESSEL (0-7)	80ns noise filter disable	80ns noise filter enable	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN031 (0x003E)	SDA4	RESSEL (0-7)	80ns noise filter disable	80ns noise filter enable	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN032 (0x0040)	MFS4_TRI GGER	RESSEL (0-7)	TOT0	TOT1	TOT2	TOT3	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN033 (0x0042)	SCS40	RESSEL (0-7)	-	-	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	P211	P025	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL L[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN035 (0x0046)	SIN5	RESSEL (0-7)	-	-	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	P222	P213	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN036 (0x0048)	SCK5	RESSEL (0-7)	-	-	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	P226	P215	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN037 (0x004A)	SCL5	RESSEL (0-7)	80ns noise filter disable	80ns noise filter enable	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN038 (0x004C)	SDA5	RESSEL (0-7)	80ns noise filter disable	80ns noise filter enable	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN039 (0x004E)	MFS5_TRI GGER	RESSEL (0-7)	TOT0	TOT1	TOT2	TOT3	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL L[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN040 (0x0050)	SCS50	RESSEL (0-7)	-	-	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	P224	P212	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN042 (0x0054)	SIN6	RESSEL (0-7)	-	-	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	P130	P329	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN043 (0x0056)	SCK6	RESSEL (0-7)	-	-	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	P202	P327	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN044 (0x0058)	SCL6	RESSEL (0-7)	80ns noise filter disable	80ns noise filter enable	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN045 (0x005A)	SDA6	RESSEL (0-7)	80ns noise filter disable	80ns noise filter enable	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL L[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN046 (0x005C)	MFS6_TRI GGER	RESSEL (0-7)	TOT0	TOT1	TOT2	TOT3	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN047 (0x005E)	SCS60	RESSEL (0-7)	-	-	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	P119	P331	P330	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN049 (0x0062)	SIN7	RESSEL (0-7)	-	-	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	P319	P416	P317	P309	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN050 (0x0064)	SCK7	RESSEL (0-7)	-	-	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	P314	P407	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN051 (0x0066)	SCL7	RESSEL (0-7)	80ns noise filter disable	80ns noise filter enable	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL L[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN052 (0x0068)	SDA7	RESSEL (0-7)	80ns noise filter disable	80ns noise filter enable	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN053 (0x006A)	MFS7_TRI GGER	RESSEL (0-7)	TOT0	TOT1	TOT2	TOT3	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN054 (0x006C)	SCS70	RESSEL (0-7)	-	-	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	P315	P410	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN056 (0x0070)	SIN8	RESSEL (0-7)	-	-	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	P009	P006	P016	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN058 (0x0074)	SCL8	RESSEL (0-7)	80ns noise filter disable	80ns noise filter enable	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL L[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN059 (0x0076)	SDA8	RESSEL (0-7)	80ns noise filter disable	80ns noise filter enable	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN060 (0x0078)	MFS8_TRI GGER	RESSEL (0-7)	TOT16	TOT17	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN064 (0x0080)	SCK9	RESSEL (0-7)	-	-	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	P407	P401	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN065 (0x0082)	SCL9	RESSEL (0-7)	80ns noise filter disable	80ns noise filter enable	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	P407	P401	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN066 (0x0084)	SDA9	RESSEL (0-7)	80ns noise filter disable	80ns noise filter enable	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	P406	P402	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL L[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN067 (0x0086)	MFS9_TRI GGER	RESSEL (0-7)	TOT16	TOT17	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN068 (0x0088)	SCS90	RESSEL (0-7)	-	-	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	P402	P404	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN072 (0x0090)	SCL10	RESSEL (0-7)	80ns noise filter disable	80ns noise filter enable	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN073 (0x0092)	SDA10	RESSEL (0-7)	80ns noise filter disable	80ns noise filter enable	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN074 (0x0094)	MFS10_T RIGGER	RESSEL (0-7)	TOT16	TOT17	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL L[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN075 (0x0096)	SCS100	RESSEL (0-7)	-	-	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	P301	P305	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN077 (0x009A)	SIN11	RESSEL (0-7)	-	-	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	P107	P109	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN079 (0x009E)	SCL11	RESSEL (0-7)	80ns noise filter disable	80ns noise filter enable	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN080 (0x00A0)	SDA11	RESSEL (0-7)	80ns noise filter disable	80ns noise filter enable	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN081 (0x00A2)	MFS11_T RIGGER	RESSEL (0-7)	TOT16	TOT17	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL L[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN082 (0x00A4)	SCS110	RESSEL (0-7)	-	-	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	P110	P105	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN084 (0x00A8)	SIN12	RESSEL (0-7)	-	-	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	P111	P011	P422	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN085 (0x00AA)	SCK12	RESSEL (0-7)	-	-	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	P113	P007	P117	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN086 (0x00AC)	SCL12	RESSEL (0-7)	80ns noise filter disable	80ns noise filter enable	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	P113	P117	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN087 (0x00AE)	SDA12	RESSEL (0-7)	80ns noise filter disable	80ns noise filter enable	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL L[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN088 (0x00B0)	MFS12_T RIGGER	RESSEL (0-7)	TOT16	TOT17	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN089 (0x00B2)	SCS120	RESSEL (0-7)	-	-	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	P114	P008	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN093 (0x00BA)	SCL13	RESSEL (0-7)	80ns noise filter disable	80ns noise filter enable	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN094 (0x00BC)	SDA13	RESSEL (0-7)	80ns noise filter disable	80ns noise filter enable	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN095 (0x00BE)	MFS13_T RIGGER	RESSEL (0-7)	TOT16	TOT17	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3:0] /PORTSEL[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN210 (0x01A4)	RX0	RESSEL (0-7)	PORT_PIN	CAN0_RX _AND_TX	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	P307	P229	P225	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN211 (0x01A6)	RX1	RESSEL (0-7)	PORT_PIN	CAN1_RX _AND_TX	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	P402	P318	P107	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN212 (0x01A8)	RX2	RESSEL (0-7)	PORT_PIN	CAN2_RX _AND_TX	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	P222	P405	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN213 (0x01AA)	RX3	RESSEL (0-7)	PORT_PIN	CAN3_RX _AND_TX	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN214 (0x01AC)	RX4	RESSEL (0-7)	PORT_PIN	CAN4_RX _AND_TX	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN218 (0x01B4)	RX8	RESSEL (0-7)	PORT_P N	CAN8_RX _AND_TX	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN219 (0x01B6)	TIN0	RESSEL (0-7)	PORT_P N	TOT3	RLT3_UFS ET	TOT1	TIOA0	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	P106	P220	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN220 (0x01B8)	TIN1	RESSEL (0-7)	PORT_P N	TOT0	RLT0_UFS ET	TOT2	TIOA2	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	P108	P226	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN221 (0x01BA)	TIN2	RESSEL (0-7)	PORT_P N	TOT1	RLT1_UFS ET	TOT3	TIOA4	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	P112	P228	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN222 (0x01BC)	TIN3	RESSEL (0-7)	PORT_P N	TOT2	RLT2_UFS ET	TOT0	TIOA6	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	P114	P301	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL L[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN235 (0x01D6)	TIN16	RESSEL (0-7)	PORT_P IN	TOT17	RLT17_U FSET	-	TIOA8	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	P117	P304	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN236 (0x01D8)	TIN17	RESSEL (0-7)	PORT_P IN	TOT16	RLT16_U FSET	-	TIOA10	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	P119	P307	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN251 (0x01F6)	INT0	RESSEL (0-7)	-	-	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	P225	P009	P001	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN252 (0x01F8)	INT1	RESSEL (0-7)	-	-	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	P307	P027	P011	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN253 (0x01FA)	INT2	RESSEL (0-7)	-	-	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	P402	P107	P013	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL L[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN254 (0x01FC)	INT3	RESSEL (0-7)	-	-	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	P022	P108	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN255 (0x01FE)	INT4	RESSEL (0-7)	-	-	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	P028	P117	P017	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN256 (0x0200)	INT5	RESSEL (0-7)	-	-	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	P130	P118	P127	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN257 (0x0202)	INT6	RESSEL (0-7)	-	-	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	P210	P202	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN258 (0x0204)	INT7	RESSEL (0-7)	-	-	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	P222	P207	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL L[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN259 (0x0206)	INT8	RESSEL (0-7)	-	-	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	P229	P213	P020	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN260 (0x0208)	INT9	RESSEL (0-7)	-	-	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	P318	P215	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN261 (0x020A)	INT10	RESSEL (0-7)	-	-	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	P325	P313	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN262 (0x020C)	INT11	RESSEL (0-7)	-	-	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	P405	P317	P030	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN263 (0x020E)	INT12	RESSEL (0-7)	-	-	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	P408	P319	P421	P105	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL L[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN264 (0x0210)	INT13	RESSEL (0-7)	-	-	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	P415	P411	P114	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN265 (0x0212)	INT14	RESSEL (0-7)	-	-	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	P418	P413	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN266 (0x0214)	INT15	RESSEL (0-7)	-	-	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	P310	P417	P123	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN267 (0x0216)	INT16	RESSEL (0-7)	-	-	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	P005	P203	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN268 (0x0218)	INT17	RESSEL (0-7)	-	-	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	P016	P214	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL L[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN269 (0x021A)	INT18	RESSEL (0-7)	-	-	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	P103	P006	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN270 (0x021C)	INT19	RESSEL (0-7)	-	-	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	P109	P230	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN271 (0x021E)	INT20	RESSEL (0-7)	-	-	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	P422	P300	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN273 (0x0222)	INT22	RESSEL (0-7)	-	-	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	P128	P023	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN274 (0x0224)	INT23	RESSEL (0-7)	-	-	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	P204	P111	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL L[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN275 (0x0226)	INT24	RESSEL (0-7)	-	-	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	P205	P304	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN276 (0x0228)	INT25	RESSEL (0-7)	-	-	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	P220	P124	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN277 (0x022A)	INT26	RESSEL (0-7)	-	-	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	P302	P329	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN278 (0x022C)	INT27	RESSEL (0-7)	-	-	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	P309	P308	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN279 (0x022E)	INT28	RESSEL (0-7)	-	-	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	P315	P321	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL L[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN281 (0x0232)	INT30	RESSEL (0-7)	-	-	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	P416	P409	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN282 (0x0234)	INT31	RESSEL (0-7)	-	-	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	P420	P421	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN283 (0x0236)	TEXT0	RESSEL (0-7)	PORT_P N	TOT0	TOT1	TIOA1	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	P019	P027	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN284 (0x0238)	TEXT1	RESSEL (0-7)	PORT_P N	TOT0	TOT2	TIOA3	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	P020	P127	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN285 (0x023A)	TEXT2	RESSEL (0-7)	PORT_P N	TOT0	TOT3	TIOA5	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	P218	P128	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN286 (0x023C)	TEXT3	RESSEL (0-7)	PORT_P N	TOT0	TOT1	TIOA7	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	P219	P205	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN287 (0x023E)	TEXT4	RESSEL (0-7)	PORT_P N	TOT0	TOT2	TIOA9	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	P304	P206	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN291 (0x0246)	TEXT8	RESSEL (0-7)	PORT_P N	RLT0_UFS ET	RLT1_UFS ET	TIOA17	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	P305	P207	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN292 (0x0248)	TEXT9	RESSEL (0-7)	PORT_P N	RLT0_UFS ET	RLT2_UFS ET	TIOA19	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN293 (0x024A)	TEXT10	RESSEL (0-7)	PORT_P N	RLT0_UFS ET	RLT3_UFS ET	TIOA21	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN299 (0x0256)	OCU0	RESSEL (0-7)	FRT0	FRT1	FRT2	FRT3	FRT4	FRT8	FRT9	FRT10
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
	OCU1	RESSEL (0-7)	FRT0	FRT1	FRT2	FRT3	FRT4	FRT8	FRT9	FRT10
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN300 (0x0258)	OCU0_MOD	RESSEL (0-7)	set1	set0	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN301 (0x025A)	OCU1_MOD	RESSEL (0-7)	set1	set0	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL L[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN302 (0x025C)	OCU2	RESSEL (0-7)	FRT1	FRT2	FRT3	FRT4	FRT8	FRT9	FRT10	FRT0
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
	OCU3	RESSEL (0-7)	FRT1	FRT2	FRT3	FRT4	FRT8	FRT9	FRT10	FRT0
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN303 (0x025E)	OCU2_MO D	RESSEL (0-7)	set1	set0	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN304 (0x0260)	OCU3_MO D	RESSEL (0-7)	set1	set0	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL L[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN305 (0x0262)	OCU4	RESSEL (0-7)	FRT2	FRT3	FRT4	FRT8	FRT9	FRT10	FRT0	FRT1
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
	OCU5	RESSEL (0-7)	FRT2	FRT3	FRT4	FRT8	FRT9	FRT10	FRT0	FRT1
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN306 (0x0264)	OCU4_MO D	RESSEL (0-7)	set1	set0	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN307 (0x0266)	OCU5_MO D	RESSEL (0-7)	set1	set0	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL L[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN323 (0x0286)	OCU16	RESSEL (0-7)	FRT8	FRT9	FRT10	FRT0	FRT1	FRT2	FRT3	FRT4
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
	OCU17	RESSEL (0-7)	FRT8	FRT9	FRT10	FRT0	FRT1	FRT2	FRT3	FRT4
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN324 (0x0288)	OCU16_M OD	RESSEL (0-7)	set1	set0	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN325 (0x028A)	OCU17_M OD	RESSEL (0-7)	set1	set0	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL L[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN326 (0x028C)	OCU18	RESSEL (0-7)	FRT9	FRT10	FRT0	FRT1	FRT2	FRT3	FRT4	FRT8
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
	OCU19	RESSEL (0-7)	FRT9	FRT10	FRT0	FRT1	FRT2	FRT3	FRT4	FRT8
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN327 (0x028E)	OCU18_M OD	RESSEL (0-7)	set1	set0	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN328 (0x0290)	OCU19_M OD	RESSEL (0-7)	set1	set0	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL L[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN329 (0x0292)	OCU20	RESSEL (0-7)	FRT10	FRT0	FRT1	FRT2	FRT3	FRT4	FRT8	FRT9
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
	OCU21	RESSEL (0-7)	FRT10	FRT0	FRT1	FRT2	FRT3	FRT4	FRT8	FRT9
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN330 (0x0294)	OCU20_M OD	RESSEL (0-7)	set1	set0	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN331 (0x0296)	OCU21_M OD	RESSEL (0-7)	set1	set0	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN347 (0x02B6)	IN0	RESSEL (0-7)	PORT_PI N	MFS0_LS YN	-	TOT0	TOT1	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	P401	P308	P210	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3:0] /PORTSEL[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN348 (0x02B8)	IN1	RESSEL (0-7)	PORT_PIN	MFS1_LSYN	-	TOT0	TOT2	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	P402	P309	P211	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN349 (0x02BA)	ICU0	RESSEL (0-7)	FRT0	FRT1	FRT2	FRT3	FRT4	FRT8	FRT9	FRT10
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
	ICU1	RESSEL (0-7)	FRT0	FRT1	FRT2	FRT3	FRT4	FRT8	FRT9	FRT10
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN350 (0x02BC)	IN2	RESSEL (0-7)	PORT_PIN	MFS2_LSYN	-	TOT0	TOT3	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	P403	P312	P212	P409	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN351 (0x02BE)	IN3	RESSEL (0-7)	PORT_PIN	MFS3_LSYN	-	TOT0	TOT1	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	P404	P313	P213	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL L[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN352 (0x02C0)	ICU2	RESSEL (0-7)	FRT1	FRT2	FRT3	FRT4	FRT8	FRT9	FRT10	FRT0
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
	ICU3	RESSEL (0-7)	FRT1	FRT2	FRT3	FRT4	FRT8	FRT9	FRT10	FRT0
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN353 (0x02C2)	IN4	RESSEL (0-7)	PORT_P IN	MFS4_L SYN	-	TOT0	TOT2	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	P405	P314	P214	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN354 (0x02C4)	IN5	RESSEL (0-7)	PORT_P IN	MFS5_L SYN	-	TOT0	TOT3	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	P416	P315	P215	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3:0] /PORTSEL[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN355 (0x02C6)	ICU4	RESSEL (0-7)	FRT2	FRT3	FRT4	FRT8	FRT9	FRT10	FRT0	FRT1
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
	ICU5	RESSEL (0-7)	FRT2	FRT3	FRT4	FRT8	FRT9	FRT10	FRT0	FRT1
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN371 (0x02E6)	IN16	RESSEL (0-7)	PORT_P IN	MFS6_L SYN	-	TOT0	TOT1	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	P005	P129	P220	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN372 (0x02E8)	IN17	RESSEL (0-7)	PORT_P IN	MFS7_L SYN	-	TOT0	TOT2	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	P006	P130	P222	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL L[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN373 (0x02EA)	ICU16	RESSEL (0-7)	FRT8	FRT9	FRT10	FRT0	FRT1	FRT2	FRT3	FRT4
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
	ICU17	RESSEL (0-7)	FRT8	FRT9	FRT10	FRT0	FRT1	FRT2	FRT3	FRT4
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN374 (0x02EC)	IN18	RESSEL (0-7)	PORT_PI N	MFS8_LS YN	MFS12_L SYN	TOT0	TOT3	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	P007	P131	P223	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN375 (0x02EE)	IN19	RESSEL (0-7)	PORT_PI N	MFS9_LS YN	MFS13_L SYN	TOT0	TOT1	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	P008	P202	P224	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3:0] /PORTSEL[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN376 (0x02F0)	ICU18	RESSEL (0-7)	FRT9	FRT10	FRT0	FRT1	FRT2	FRT3	FRT4	FRT8
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
	ICU19	RESSEL (0-7)	FRT9	FRT10	FRT0	FRT1	FRT2	FRT3	FRT4	FRT8
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN377 (0x02F2)	IN20	RESSEL (0-7)	PORT_PIN	MFS10_LSYN	-	TOT0	TOT2	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	P009	P203	P225	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN378 (0x02F4)	IN21	RESSEL (0-7)	PORT_PIN	MFS11_LSYN	-	TOT0	TOT3	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	P010	P204	P226	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL L[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN379 (0x02F6)	ICU20	RESSEL (0-7)	FRT10	FRT0	FRT1	FRT2	FRT3	FRT4	FRT8	FRT9
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
	ICU21	RESSEL (0-7)	FRT10	FRT0	FRT1	FRT2	FRT3	FRT4	FRT8	FRT9
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN419 (0x0346)	AIN8	RESSEL (0-7)	PORT_P N	TOT0	TIOA0	TIOA1	TIOA2	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	P000	P203	P010	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN420 (0x0348)	BIN8	RESSEL (0-7)	PORT_P N	TOT1	TIOA1	TIOA2	TIOA0	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	P001	P204	P012	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN421 (0x034A)	ZIN8	RESSEL (0-7)	PORT_P N	TOT2	TIOA2	TIOA0	TIOA1	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	P003	P205	P013	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3:0] /PORTSEL[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN422 (0x034C)	AIN9	RESSEL (0-7)	PORT_PIN	TOT1	TIOA3	TIOA4	TIOA5	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	P005	P223	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN423 (0x034E)	BIN9	RESSEL (0-7)	PORT_PIN	TOT2	TIOA4	TIOA5	TIOA3	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	P006	P224	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN424 (0x0350)	ZIN9	RESSEL (0-7)	PORT_PIN	TOT3	TIOA5	TIOA3	TIOA4	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	P007	P225	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN443 (0x0376)	TIOB0	RESSEL (0-7)	PORT_PIN	TOT0	RLT0_UFSET	TOT1	RLT1_UFSET	FRT0_MTSF	OUT0	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN444 (0x0378)	TIOA1	RESSEL (0-7)	PORT_PIN	TOT0	RLT0_UFSET	TOT1	RLT1_UFSET	FRT0_MTSF	OUT0	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	P009	P004	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL L[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN445 (0x037A)	TIOB1	RESSEL (0-7)	PORT_P N	TOT0	RLT0_UFS ET	TOT1	RLT1_U FSET	FRT0_M TSF	OUT0	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN446 (0x037C)	TIOB2	RESSEL (0-7)	PORT_P N	TOT0	RLT0_UFS ET	TOT2	RLT2_U FSET	FRT1_M TSF	OUT1	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN447 (0x037E)	TIOA3	RESSEL (0-7)	PORT_P N	TOT0	RLT0_UFS ET	TOT2	RLT2_U FSET	FRT1_M TSF	OUT1	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	P012	P014	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN448 (0x0380)	TIOB3	RESSEL (0-7)	PORT_P N	TOT0	RLT0_UFS ET	TOT2	RLT2_U FSET	FRT1_M TSF	OUT1	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN449 (0x0382)	TIOB4	RESSEL (0-7)	PORT_P N	TOT0	RLT0_UFS ET	TOT3	RLT3_U FSET	FRT2_M TSF	OUT2	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3:0] /PORTSEL[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN450 (0x0384)	TIOA5	RESSEL (0-7)	PORT_PIN	TOT0	RLT0_UFSET	TOT3	RLT3_UFSET	FRT2_MTSF	OUT2	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	P015	P113	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN451 (0x0386)	TIOB5	RESSEL (0-7)	PORT_PIN	TOT0	RLT0_UFSET	TOT3	RLT3_UFSET	FRT2_MTSF	OUT2	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN452 (0x0388)	TIOB6	RESSEL (0-7)	PORT_PIN	TOT0	RLT0_UFSET	TOT16	RLT16_UFSET	FRT3_MTSF	OUT3	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN453 (0x038A)	TIOA7	RESSEL (0-7)	PORT_PIN	TOT0	RLT0_UFSET	TOT16	RLT16_UFSET	FRT3_MTSF	OUT3	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	P017	P314	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN454 (0x038C)	TIOB7	RESSEL (0-7)	PORT_PIN	TOT0	RLT0_UFSET	TOT16	RLT16_UFSET	FRT3_MTSF	OUT3	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL L[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN455 (0x038E)	TIOB8	RESSEL (0-7)	PORT_P N	TOT0	RLT0_UFS ET	TOT17	RLT17_ UFSET	FRT4_M TSF	OUT4	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN456 (0x0390)	TIOA9	RESSEL (0-7)	PORT_P N	TOT0	RLT0_UFS ET	TOT17	RLT17_ UFSET	FRT4_M TSF	OUT4	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	P105	P317	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN457 (0x0392)	TIOB9	RESSEL (0-7)	PORT_P N	TOT0	RLT0_UFS ET	TOT17	RLT17_ UFSET	FRT4_M TSF	OUT4	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN458 (0x0394)	TIOB10	RESSEL (0-7)	PORT_P N	TOT16	RLT16_UF SET	TOT0	RLT0_U FSET	FRT0_M TSF	OUT5	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN459 (0x0396)	TIOA11	RESSEL (0-7)	PORT_P N	TOT16	RLT16_UF SET	TOT0	RLT0_U FSET	FRT0_M TSF	OUT5	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	P108	P122	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL L[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN460 (0x0398)	TIOB11	RESSEL (0-7)	PORT_P N	TOT16	RLT16_U FSET	TOT0	RLT0_U FSET	FRT0_M TSF	OUT5	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN461 (0x039A)	TIOB12	RESSEL (0-7)	PORT_P N	TOT16	RLT16_U FSET	TOT1	RLT1_U FSET	FRT8_M TSF	OUT0	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN462 (0x039C)	TIOA13	RESSEL (0-7)	PORT_P N	TOT16	RLT16_U FSET	TOT1	RLT1_U FSET	FRT8_M TSF	OUT0	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	P112	P212	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN463 (0x039E)	TIOB13	RESSEL (0-7)	PORT_P N	TOT16	RLT16_U FSET	TOT1	RLT1_U FSET	FRT8_M TSF	OUT0	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN464 (0x03A0)	TIOB14	RESSEL (0-7)	PORT_P N	TOT16	RLT16_U FSET	TOT2	RLT2_U FSET	FRT9_M TSF	OUT1	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN465 (0x03A2)	TIOA15	RESSEL (0-7)	PORT_PIN	TOT16	RLT16_UF SET	TOT2	RLT2_U FSET	FRT9_M TSF	OUT1	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	P124	P214	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN466 (0x03A4)	TIOB15	RESSEL (0-7)	PORT_PIN	TOT16	RLT16_UF SET	TOT2	RLT2_U FSET	FRT9_M TSF	OUT1	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN467 (0x03A6)	TIOB16	RESSEL (0-7)	PORT_PIN	TOT16	RLT16_UF SET	TOT3	RLT3_U FSET	FRT10_ MTSF	OUT16	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN468 (0x03A8)	TIOA17	RESSEL (0-7)	PORT_PIN	TOT16	RLT16_UF SET	TOT3	RLT3_U FSET	FRT10_ MTSF	OUT16	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	P200	P226	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN469 (0x03AA)	TIOB17	RESSEL (0-7)	PORT_PIN	TOT16	RLT16_UF SET	TOT3	RLT3_U FSET	FRT10_ MTSF	OUT16	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3:0] /PORTSEL[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN470 (0x03AC)	TIOB18	RESSEL (0-7)	PORT_PIN	TOT16	RLT16_UFSET	TOT17	RLT17_UFSET	FRT8_MTSF	OUT17	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN471 (0x03AE)	TIOA19	RESSEL (0-7)	PORT_PIN	TOT16	RLT16_UFSET	TOT17	RLT17_UFSET	FRT8_MTSF	OUT17	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	P208	P302	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN472 (0x03B0)	TIOB19	RESSEL (0-7)	PORT_PIN	TOT16	RLT16_UFSET	TOT17	RLT17_UFSET	FRT8_MTSF	OUT17	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN473 (0x03B2)	TIOB20	RESSEL (0-7)	PORT_PIN	TOT0	RLT0_UFSET	TOT1	RLT1_UFSET	FRT9_MTSF	OUT18	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN474 (0x03B4)	TIOA21	RESSEL (0-7)	PORT_PIN	TOT0	RLT0_UFSET	TOT1	RLT1_UFSET	FRT9_MTSF	OUT18	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	P210	P316	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN475 (0x03B6)	TIOB21	RESSEL (0-7)	PORT_PIN	TOT0	RLT0_UFS ET	TOT1	RLT1_U FSET	FRT9_M TSF	OUT18	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN476 (0x03B8)	TIOB22	RESSEL (0-7)	PORT_PIN	TOT0	RLT0_UFS ET	TOT2	RLT2_U FSET	FRT10_ MTSF	OUT19	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN477 (0x03BA)	TIOA23	RESSEL (0-7)	PORT_PIN	TOT0	RLT0_UFS ET	TOT2	RLT2_U FSET	FRT10_ MTSF	OUT19	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	P227	P417	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN478 (0x03BC)	TIOB23	RESSEL (0-7)	PORT_PIN	TOT0	RLT0_UFS ET	TOT2	RLT2_U FSET	FRT10_ MTSF	OUT19	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN479 (0x03BE)	TIOB24	RESSEL (0-7)	PORT_PIN	TOT0	RLT0_UFS ET	TOT3	RLT3_U FSET	FRT0_M TSF	OUT20	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL L[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN480 (0x03C0)	TIOA25	RESSEL (0-7)	PORT_P N	TOT0	RLT0_UFS ET	TOT3	RLT3_U FSET	FRT0_M TSF	OUT20	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	P229	P412	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN481 (0x03C2)	TIOB25	RESSEL (0-7)	PORT_P N	TOT0	RLT0_UFS ET	TOT3	RLT3_U FSET	FRT0_M TSF	OUT20	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN482 (0x03C4)	TIOB26	RESSEL (0-7)	PORT_P N	TOT0	RLT0_UFS ET	TOT16	RLT16_ UFSET	FRT1_M TSF	OUT21	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN483 (0x03C6)	TIOA27	RESSEL (0-7)	PORT_P N	TOT0	RLT0_UFS ET	TOT16	RLT16_ UFSET	FRT1_M TSF	OUT21	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	P231	P419	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN484 (0x03C8)	TIOB27	RESSEL (0-7)	PORT_P N	TOT0	RLT0_UFS ET	TOT16	RLT16_ UFSET	FRT1_M TSF	OUT21	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN485 (0x03CA)	TIOB28	RESSEL (0-7)	PORT_P N	TOT0	RLT0_UFS ET	TOT17	RLT17_ UFSET	FRT2_M TSF	OUT0	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN486 (0x03CC)	TIOA29	RESSEL (0-7)	PORT_P N	TOT0	RLT0_UFS ET	TOT17	RLT17_ UFSET	FRT2_M TSF	OUT0	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	P305	P309	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN487 (0x03CE)	TIOB29	RESSEL (0-7)	PORT_P N	TOT0	RLT0_UFS ET	TOT17	RLT17_ UFSET	FRT2_M TSF	OUT0	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN488 (0x03D0)	TIOB30	RESSEL (0-7)	PORT_P N	TOT16	RLT16_UF SET	TOT0	RLT0_U FSET	FRT3_M TSF	OUT1	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN489 (0x03D2)	TIOA31	RESSEL (0-7)	PORT_P N	TOT16	RLT16_UF SET	TOT0	RLT0_U FSET	FRT3_M TSF	OUT1	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL L[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN490 (0x03D4)	TIOB31	RESSEL (0-7)	PORT_P N	TOT16	RLT16_U FSET	TOT0	RLT0_U FSET	FRT3_M TSF	OUT1	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN491 (0x03D6)	TIOB32	RESSEL (0-7)	PORT_P N	TOT16	RLT16_U FSET	TOT1	RLT1_U FSET	FRT4_M TSF	OUT2	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN492 (0x03D8)	TIOA33	RESSEL (0-7)	PORT_P N	TOT16	RLT16_U FSET	TOT1	RLT1_U FSET	FRT4_M TSF	OUT2	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN493 (0x03DA)	TIOB33	RESSEL (0-7)	PORT_P N	TOT16	RLT16_U FSET	TOT1	RLT1_U FSET	FRT4_M TSF	OUT2	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN494 (0x03DC)	TIOB34	RESSEL (0-7)	PORT_P N	TOT16	RLT16_U FSET	TOT2	RLT2_U FSET	FRT0_M TSF	OUT3	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN495 (0x03DE)	TIOA35	RESSEL (0-7)	PORT_P N	TOT16	RLT16_U FSET	TOT2	RLT2_U FSET	FRT0_M TSF	OUT3	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN496 (0x03E0)	TIOB35	RESSEL (0-7)	PORT_P N	TOT16	RLT16_U FSET	TOT2	RLT2_U FSET	FRT0_M TSF	OUT3	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN497 (0x03E2)	TIOB36	RESSEL (0-7)	PORT_P N	TOT16	RLT16_U FSET	TOT3	RLT3_U FSET	FRT8_M TSF	OUT4	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN498 (0x03E4)	TIOA37	RESSEL (0-7)	PORT_P N	TOT16	RLT16_U FSET	TOT3	RLT3_U FSET	FRT8_M TSF	OUT4	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN499 (0x03E6)	TIOB37	RESSEL (0-7)	PORT_P N	TOT16	RLT16_U FSET	TOT3	RLT3_U FSET	FRT8_M TSF	OUT4	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL L[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN500 (0x03E8)	TIOB38	RESSEL (0-7)	PORT_P N	TOT16	RLT16_UF SET	TOT17	RLT17_ UFSET	FRT9_M TSF	OUT5	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN501 (0x03EA)	TIOA39	RESSEL (0-7)	PORT_P N	TOT16	RLT16_UF SET	TOT17	RLT17_ UFSET	FRT9_M TSF	OUT5	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN502 (0x03EC)	TIOB39	RESSEL (0-7)	PORT_P N	TOT16	RLT16_UF SET	TOT17	RLT17_ UFSET	FRT9_M TSF	OUT5	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN503 (0x03EE)	TIOB40	RESSEL (0-7)	PORT_P N	TOT0	RLT0_UFS ET	TOT1	RLT1_U FSET	FRT10_ MTSF	OUT0	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN504 (0x03F0)	TIOA41	RESSEL (0-7)	PORT_P N	TOT0	RLT0_UFS ET	TOT1	RLT1_U FSET	FRT10_ MTSF	OUT0	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL L[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN505 (0x03F2)	TIOB41	RESSEL (0-7)	PORT_P N	TOT0	RLT0_UFS ET	TOT1	RLT1_U FSET	FRT10_ MTSF	OUT0	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN506 (0x03F4)	TIOB42	RESSEL (0-7)	PORT_P N	TOT0	RLT0_UFS ET	TOT2	RLT2_U FSET	FRT8_M TSF	OUT1	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN507 (0x03F6)	TIOA43	RESSEL (0-7)	PORT_P N	TOT0	RLT0_UFS ET	TOT2	RLT2_U FSET	FRT8_M TSF	OUT1	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN508 (0x03F8)	TIOB43	RESSEL (0-7)	PORT_P N	TOT0	RLT0_UFS ET	TOT2	RLT2_U FSET	FRT8_M TSF	OUT1	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN509 (0x03FA)	TIOB44	RESSEL (0-7)	PORT_P N	TOT0	RLT0_UFS ET	TOT3	RLT3_U FSET	FRT9_M TSF	OUT16	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL L[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN510 (0x03FC)	TIOA45	RESSEL (0-7)	PORT_P N	TOT0	RLT0_UFS ET	TOT3	RLT3_U FSET	FRT9_M TSF	OUT16	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN511 (0x03FE)	TIOB45	RESSEL (0-7)	PORT_P N	TOT0	RLT0_UFS ET	TOT3	RLT3_U FSET	FRT9_M TSF	OUT16	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN512 (0x0400)	TIOB46	RESSEL (0-7)	PORT_P N	TOT0	RLT0_UFS ET	TOT16	RLT16_ UFSET	FRT10_ MTSF	OUT17	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN513 (0x0402)	TIOA47	RESSEL (0-7)	PORT_P N	TOT0	RLT0_UFS ET	TOT16	RLT16_ UFSET	FRT10_ MTSF	OUT17	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN514 (0x0404)	TIOB47	RESSEL (0-7)	PORT_P N	TOT0	RLT0_UFS ET	TOT16	RLT16_ UFSET	FRT10_ MTSF	OUT17	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN515 (0x0406)	TIOB48	RESSEL (0-7)	PORT_P N	TOT0	RLT0_UFS ET	TOT17	RLT17_ UFSET	FRT0_M TSF	OUT18	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN516 (0x0408)	TIOA49	RESSEL (0-7)	PORT_P N	TOT0	RLT0_UFS ET	TOT17	RLT17_ UFSET	FRT0_M TSF	OUT18	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN517 (0x040A)	TIOB49	RESSEL (0-7)	PORT_P N	TOT0	RLT0_UFS ET	TOT17	RLT17_ UFSET	FRT0_M TSF	OUT18	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN518 (0x040C)	TIOB50	RESSEL (0-7)	PORT_P N	TOT16	RLT16_UF SET	TOT0	RLT0_U FSET	FRT1_M TSF	OUT19	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN519 (0x040E)	TIOA51	RESSEL (0-7)	PORT_P N	TOT16	RLT16_UF SET	TOT0	RLT0_U FSET	FRT1_M TSF	OUT19	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL L[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN520 (0x0410)	TIOB51	RESSEL (0-7)	PORT_P N	TOT16	RLT16_U FSET	TOT0	RLT0_U FSET	FRT1_M TSF	OUT19	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN521 (0x0412)	TIOB52	RESSEL (0-7)	PORT_P N	TOT16	RLT16_U FSET	TOT1	RLT1_U FSET	FRT2_M TSF	OUT20	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN522 (0x0414)	TIOA53	RESSEL (0-7)	PORT_P N	TOT16	RLT16_U FSET	TOT1	RLT1_U FSET	FRT2_M TSF	OUT20	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN523 (0x0416)	TIOB53	RESSEL (0-7)	PORT_P N	TOT16	RLT16_U FSET	TOT1	RLT1_U FSET	FRT2_M TSF	OUT20	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN524 (0x0418)	TIOB54	RESSEL (0-7)	PORT_P N	TOT16	RLT16_U FSET	TOT2	RLT2_U FSET	FRT3_M TSF	OUT21	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN525 (0x041A)	TIOA55	RESSEL (0-7)	PORT_P N	TOT16	RLT16_U FSET	TOT2	RLT2_U FSET	FRT3_M TSF	OUT21	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN526 (0x041C)	TIOB55	RESSEL (0-7)	PORT_P N	TOT16	RLT16_U FSET	TOT2	RLT2_U FSET	FRT3_M TSF	OUT21	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN527 (0x041E)	TIOB56	RESSEL (0-7)	PORT_P N	TOT16	RLT16_U FSET	TOT3	RLT3_U FSET	FRT4_M TSF	OUT0	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN528 (0x0420)	TIOA57	RESSEL (0-7)	PORT_P N	TOT16	RLT16_U FSET	TOT3	RLT3_U FSET	FRT4_M TSF	OUT0	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN529 (0x0422)	TIOB57	RESSEL (0-7)	PORT_P N	TOT16	RLT16_U FSET	TOT3	RLT3_U FSET	FRT4_M TSF	OUT0	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL L[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN530 (0x0424)	TIOB58	RESSEL (0-7)	PORT_P N	TOT16	RLT16_UF SET	TOT17	RLT17_ UFSET	FRT0_M TSF	OUT1	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN531 (0x0426)	TIOA59	RESSEL (0-7)	PORT_P N	TOT16	RLT16_UF SET	TOT17	RLT17_ UFSET	FRT0_M TSF	OUT1	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN532 (0x0428)	TIOB59	RESSEL (0-7)	PORT_P N	TOT16	RLT16_UF SET	TOT17	RLT17_ UFSET	FRT0_M TSF	OUT1	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN533 (0x042A)	TIOB60	RESSEL (0-7)	PORT_P N	TOT0	RLT0_UFS ET	TOT1	RLT1_U FSET	FRT8_M TSF	OUT2	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN534 (0x042C)	TIOA61	RESSEL (0-7)	PORT_P N	TOT0	RLT0_UFS ET	TOT1	RLT1_U FSET	FRT8_M TSF	OUT2	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN535 (0x042E)	TIOB61	RESSEL (0-7)	PORT_PIN	TOT0	RLT0_UFS ET	TOT1	RLT1_U FSET	FRT8_M TSF	OUT2	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN536 (0x0430)	TIOB62	RESSEL (0-7)	PORT_PIN	TOT0	RLT0_UFS ET	TOT2	RLT2_U FSET	FRT9_M TSF	OUT3	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN537 (0x0432)	TIOA63	RESSEL (0-7)	PORT_PIN	TOT0	RLT0_UFS ET	TOT2	RLT2_U FSET	FRT9_M TSF	OUT3	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN538 (0x0434)	TIOB63	RESSEL (0-7)	PORT_PIN	TOT0	RLT0_UFS ET	TOT2	RLT2_U FSET	FRT9_M TSF	OUT3	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN539 (0x0436)	ADTG0	RESSEL (0-7)	-	-	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	P214	P211	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL L[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN540 (0x0438)	ADTG1	RESSEL (0-7)	-	-	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	P215	P128	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN541 (0x043A)	ADC0_HW TRG0	RESSEL (0-7)	PORT_PIN(ADTG0)	RLT0_UFS ET	RLT1_UFS ET	OUT0	OUT1	bt_adto_000_a	bt_adto_000_b	bt_adto_000_c
		RESSEL (8-15)	bt_adto_000_d	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN542 (0x043C)	bt_adto_000_a	RESSEL (0-7)	BT0_ADT O	BT1_ADT O	BT2_ADT O	BT3_ADT O	BT4_ADT O	BT5_ADT O	BT6_ADT O	BT7_ADT O
		RESSEL (8-15)	BT8_ADT O	BT9_ADT O	BT10_ADT O	BT11_A DTO	BT12_A DTO	BT13_A DTO	BT14_A DTO	BT15_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN543 (0x043E)	bt_adto_000_b	RESSEL (0-7)	BT16_ADT O	BT17_ADT O	BT18_ADT O	BT19_A DTO	BT20_A DTO	BT21_A DTO	BT22_A DTO	BT23_A DTO
		RESSEL (8-15)	BT24_ADT O	BT25_ADT O	BT26_ADT O	BT27_A DTO	BT28_A DTO	BT29_A DTO	BT30_A DTO	BT31_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN544 (0x0440)	bt_adto_000_c	RESSEL (0-7)	BT32_ADT O	BT33_ADT O	BT34_ADT O	BT35_A DTO	BT36_A DTO	BT37_A DTO	BT38_A DTO	BT39_A DTO
		RESSEL (8-15)	BT40_ADT O	BT41_ADT O	BT42_ADT O	BT43_A DTO	BT44_A DTO	BT45_A DTO	BT46_A DTO	BT47_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN545 (0x0442)	bt_adto_0 00_d	RESSEL (0-7)	BT48_ADT O	BT49_ADT O	BT50_ADT O	BT51_A DTO	BT52_A DTO	BT53_A DTO	BT54_A DTO	BT55_A DTO
		RESSEL (8-15)	BT56_ADT O	BT57_ADT O	BT58_ADT O	BT59_A DTO	BT60_A DTO	BT61_A DTO	BT62_A DTO	BT63_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN546 (0x0444)	ADC0_HW TRG1	RESSEL (0-7)	PORT_P N(ADTG0)	RLT1_UFS ET	RLT2_UFS ET	OUT1	OUT2	bt_adto_ 001_a	bt_adto_ 001_b	bt_adto_ 001_c
		RESSEL (8-15)	bt_adto_0 01_d	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN547 (0x0446)	bt_adto_0 01_a	RESSEL (0-7)	BT0_ADT O	BT1_ADT O	BT2_ADT O	BT3_AD TO	BT4_AD TO	BT5_AD TO	BT6_AD TO	BT7_AD TO
		RESSEL (8-15)	BT8_ADT O	BT9_ADT O	BT10_ADT O	BT11_A DTO	BT12_A DTO	BT13_A DTO	BT14_A DTO	BT15_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN548 (0x0448)	bt_adto_0 01_b	RESSEL (0-7)	BT16_ADT O	BT17_ADT O	BT18_ADT O	BT19_A DTO	BT20_A DTO	BT21_A DTO	BT22_A DTO	BT23_A DTO
		RESSEL (8-15)	BT24_ADT O	BT25_ADT O	BT26_ADT O	BT27_A DTO	BT28_A DTO	BT29_A DTO	BT30_A DTO	BT31_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN549 (0x044A)	bt_adto_0 01_c	RESSEL (0-7)	BT32_ADT O	BT33_ADT O	BT34_ADT O	BT35_A DTO	BT36_A DTO	BT37_A DTO	BT38_A DTO	BT39_A DTO
		RESSEL (8-15)	BT40_ADT O	BT41_ADT O	BT42_ADT O	BT43_A DTO	BT44_A DTO	BT45_A DTO	BT46_A DTO	BT47_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN550 (0x044C)	bt_adto_0 01_d	RESSEL (0-7)	BT48_ADT O	BT49_ADT O	BT50_ADT O	BT51_A DTO	BT52_A DTO	BT53_A DTO	BT54_A DTO	BT55_A DTO
		RESSEL (8-15)	BT56_ADT O	BT57_ADT O	BT58_ADT O	BT59_A DTO	BT60_A DTO	BT61_A DTO	BT62_A DTO	BT63_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN551 (0x044E)	ADC0_HW TRG2	RESSEL (0-7)	PORT_PIN(ADTG0)	RLT2_UFS ET	RLT3_UFS ET	OUT2	OUT3	bt_adto_002_a	bt_adto_002_b	bt_adto_002_c
		RESSEL (8-15)	bt_adto_002_d	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN552 (0x0450)	bt_adto_0 02_a	RESSEL (0-7)	BT0_ADT O	BT1_ADT O	BT2_ADT O	BT3_AD TO	BT4_AD TO	BT5_AD TO	BT6_AD TO	BT7_AD TO
		RESSEL (8-15)	BT8_ADT O	BT9_ADT O	BT10_ADT O	BT11_A DTO	BT12_A DTO	BT13_A DTO	BT14_A DTO	BT15_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN553 (0x0452)	bt_adto_0 02_b	RESSEL (0-7)	BT16_ADT O	BT17_ADT O	BT18_ADT O	BT19_A DTO	BT20_A DTO	BT21_A DTO	BT22_A DTO	BT23_A DTO
		RESSEL (8-15)	BT24_ADT O	BT25_ADT O	BT26_ADT O	BT27_A DTO	BT28_A DTO	BT29_A DTO	BT30_A DTO	BT31_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN554 (0x0454)	bt_adto_0 02_c	RESSEL (0-7)	BT32_ADT O	BT33_ADT O	BT34_ADT O	BT35_A DTO	BT36_A DTO	BT37_A DTO	BT38_A DTO	BT39_A DTO
		RESSEL (8-15)	BT40_ADT O	BT41_ADT O	BT42_ADT O	BT43_A DTO	BT44_A DTO	BT45_A DTO	BT46_A DTO	BT47_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN555 (0x0456)	bt_adto_0 02_d	RESSEL (0-7)	BT48_ADT O	BT49_ADT O	BT50_ADT O	BT51_A DTO	BT52_A DTO	BT53_A DTO	BT54_A DTO	BT55_A DTO
		RESSEL (8-15)	BT56_ADT O	BT57_ADT O	BT58_ADT O	BT59_A DTO	BT60_A DTO	BT61_A DTO	BT62_A DTO	BT63_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN556 (0x0458)	ADC0_HW TRG3	RESSEL (0-7)	PORT_P N(ADTG0)	RLT3_UFS ET	RLT16_UF SET	OUT3	OUT4	bt_adto_ 003_a	bt_adto_ 003_b	bt_adto_ 003_c
		RESSEL (8-15)	bt_adto_0 03_d	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN557 (0x045A)	bt_adto_0 03_a	RESSEL (0-7)	BT0_ADT O	BT1_ADT O	BT2_ADT O	BT3_AD TO	BT4_AD TO	BT5_AD TO	BT6_AD TO	BT7_AD TO
		RESSEL (8-15)	BT8_ADT O	BT9_ADT O	BT10_ADT O	BT11_A DTO	BT12_A DTO	BT13_A DTO	BT14_A DTO	BT15_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN558 (0x045C)	bt_adto_0 03_b	RESSEL (0-7)	BT16_ADT O	BT17_ADT O	BT18_ADT O	BT19_A DTO	BT20_A DTO	BT21_A DTO	BT22_A DTO	BT23_A DTO
		RESSEL (8-15)	BT24_ADT O	BT25_ADT O	BT26_ADT O	BT27_A DTO	BT28_A DTO	BT29_A DTO	BT30_A DTO	BT31_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN559 (0x045E)	bt_adto_0 03_c	RESSEL (0-7)	BT32_ADT O	BT33_ADT O	BT34_ADT O	BT35_A DTO	BT36_A DTO	BT37_A DTO	BT38_A DTO	BT39_A DTO
		RESSEL (8-15)	BT40_ADT O	BT41_ADT O	BT42_ADT O	BT43_A DTO	BT44_A DTO	BT45_A DTO	BT46_A DTO	BT47_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL L[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN560 (0x0460)	bt_adto_0 03_d	RESSEL (0-7)	BT48_ADT O	BT49_ADT O	BT50_ADT O	BT51_A DTO	BT52_A DTO	BT53_A DTO	BT54_A DTO	BT55_A DTO
		RESSEL (8-15)	BT56_ADT O	BT57_ADT O	BT58_ADT O	BT59_A DTO	BT60_A DTO	BT61_A DTO	BT62_A DTO	BT63_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN561 (0x0462)	ADC0_HW TRG4	RESSEL (0-7)	PORT_PIN(ADTG0)	RLT16_UF SET	RLT17_UF SET	OUT4	OUT5	bt_adto_004_a	bt_adto_004_b	bt_adto_004_c
		RESSEL (8-15)	bt_adto_004_d	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN562 (0x0464)	bt_adto_0 04_a	RESSEL (0-7)	BT0_ADT O	BT1_ADT O	BT2_ADT O	BT3_AD TO	BT4_AD TO	BT5_AD TO	BT6_AD TO	BT7_AD TO
		RESSEL (8-15)	BT8_ADT O	BT9_ADT O	BT10_ADT O	BT11_A DTO	BT12_A DTO	BT13_A DTO	BT14_A DTO	BT15_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN563 (0x0466)	bt_adto_0 04_b	RESSEL (0-7)	BT16_ADT O	BT17_ADT O	BT18_ADT O	BT19_A DTO	BT20_A DTO	BT21_A DTO	BT22_A DTO	BT23_A DTO
		RESSEL (8-15)	BT24_ADT O	BT25_ADT O	BT26_ADT O	BT27_A DTO	BT28_A DTO	BT29_A DTO	BT30_A DTO	BT31_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN564 (0x0468)	bt_adto_0 04_c	RESSEL (0-7)	BT32_ADT O	BT33_ADT O	BT34_ADT O	BT35_A DTO	BT36_A DTO	BT37_A DTO	BT38_A DTO	BT39_A DTO
		RESSEL (8-15)	BT40_ADT O	BT41_ADT O	BT42_ADT O	BT43_A DTO	BT44_A DTO	BT45_A DTO	BT46_A DTO	BT47_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN565 (0x046A)	bt_adto_0 04_d	RESSEL (0-7)	BT48_ADT O	BT49_ADT O	BT50_ADT O	BT51_A DTO	BT52_A DTO	BT53_A DTO	BT54_A DTO	BT55_A DTO
		RESSEL (8-15)	BT56_ADT O	BT57_ADT O	BT58_ADT O	BT59_A DTO	BT60_A DTO	BT61_A DTO	BT62_A DTO	BT63_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN566 (0x046C)	ADC0_HW TRG5	RESSEL (0-7)	PORT_P N(ADTG0)	RLT17_UF SET	RLT0_UFS ET	OUT5	OUT0	bt_adto_ 005_a	bt_adto_ 005_b	bt_adto_ 005_c
		RESSEL (8-15)	bt_adto_0 05_d	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN567 (0x046E)	bt_adto_0 05_a	RESSEL (0-7)	BT0_ADT O	BT1_ADT O	BT2_ADT O	BT3_AD TO	BT4_AD TO	BT5_AD TO	BT6_AD TO	BT7_AD TO
		RESSEL (8-15)	BT8_ADT O	BT9_ADT O	BT10_ADT O	BT11_A DTO	BT12_A DTO	BT13_A DTO	BT14_A DTO	BT15_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN568 (0x0470)	bt_adto_0 05_b	RESSEL (0-7)	BT16_ADT O	BT17_ADT O	BT18_ADT O	BT19_A DTO	BT20_A DTO	BT21_A DTO	BT22_A DTO	BT23_A DTO
		RESSEL (8-15)	BT24_ADT O	BT25_ADT O	BT26_ADT O	BT27_A DTO	BT28_A DTO	BT29_A DTO	BT30_A DTO	BT31_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN569 (0x0472)	bt_adto_0 05_c	RESSEL (0-7)	BT32_ADT O	BT33_ADT O	BT34_ADT O	BT35_A DTO	BT36_A DTO	BT37_A DTO	BT38_A DTO	BT39_A DTO
		RESSEL (8-15)	BT40_ADT O	BT41_ADT O	BT42_ADT O	BT43_A DTO	BT44_A DTO	BT45_A DTO	BT46_A DTO	BT47_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL L[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN570 (0x0474)	bt_adto_0 05_d	RESSEL (0-7)	BT48_ADT O	BT49_ADT O	BT50_ADT O	BT51_A DTO	BT52_A DTO	BT53_A DTO	BT54_A DTO	BT55_A DTO
		RESSEL (8-15)	BT56_ADT O	BT57_ADT O	BT58_ADT O	BT59_A DTO	BT60_A DTO	BT61_A DTO	BT62_A DTO	BT63_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN571 (0x0476)	ADC0_HW TRG6	RESSEL (0-7)	PORT_P N(ADTG0)	RLT0_UFS ET	RLT1_UFS ET	OUT0	OUT1	bt_adto_ 006_a	bt_adto_ 006_b	bt_adto_ 006_c
		RESSEL (8-15)	bt_adto_0 06_d	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN572 (0x0478)	bt_adto_0 06_a	RESSEL (0-7)	BT0_ADT O	BT1_ADT O	BT2_ADT O	BT3_AD TO	BT4_AD TO	BT5_AD TO	BT6_AD TO	BT7_AD TO
		RESSEL (8-15)	BT8_ADT O	BT9_ADT O	BT10_ADT O	BT11_A DTO	BT12_A DTO	BT13_A DTO	BT14_A DTO	BT15_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN573 (0x047A)	bt_adto_0 06_b	RESSEL (0-7)	BT16_ADT O	BT17_ADT O	BT18_ADT O	BT19_A DTO	BT20_A DTO	BT21_A DTO	BT22_A DTO	BT23_A DTO
		RESSEL (8-15)	BT24_ADT O	BT25_ADT O	BT26_ADT O	BT27_A DTO	BT28_A DTO	BT29_A DTO	BT30_A DTO	BT31_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN574 (0x047C)	bt_adto_0 06_c	RESSEL (0-7)	BT32_ADT O	BT33_ADT O	BT34_ADT O	BT35_A DTO	BT36_A DTO	BT37_A DTO	BT38_A DTO	BT39_A DTO
		RESSEL (8-15)	BT40_ADT O	BT41_ADT O	BT42_ADT O	BT43_A DTO	BT44_A DTO	BT45_A DTO	BT46_A DTO	BT47_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN575 (0x047E)	bt_adto_0 06_d	RESSEL (0-7)	BT48_ADT O	BT49_ADT O	BT50_ADT O	BT51_A DTO	BT52_A DTO	BT53_A DTO	BT54_A DTO	BT55_A DTO
		RESSEL (8-15)	BT56_ADT O	BT57_ADT O	BT58_ADT O	BT59_A DTO	BT60_A DTO	BT61_A DTO	BT62_A DTO	BT63_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN576 (0x0480)	ADC0_HW TRG7	RESSEL (0-7)	PORT_P N(ADTG0)	RLT1_UFS ET	RLT2_UFS ET	OUT1	OUT16	bt_adto_ 007_a	bt_adto_ 007_b	bt_adto_ 007_c
		RESSEL (8-15)	bt_adto_0 07_d	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN577 (0x0482)	bt_adto_0 07_a	RESSEL (0-7)	BT0_ADT O	BT1_ADT O	BT2_ADT O	BT3_AD TO	BT4_AD TO	BT5_AD TO	BT6_AD TO	BT7_AD TO
		RESSEL (8-15)	BT8_ADT O	BT9_ADT O	BT10_ADT O	BT11_A DTO	BT12_A DTO	BT13_A DTO	BT14_A DTO	BT15_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN578 (0x0484)	bt_adto_0 07_b	RESSEL (0-7)	BT16_ADT O	BT17_ADT O	BT18_ADT O	BT19_A DTO	BT20_A DTO	BT21_A DTO	BT22_A DTO	BT23_A DTO
		RESSEL (8-15)	BT24_ADT O	BT25_ADT O	BT26_ADT O	BT27_A DTO	BT28_A DTO	BT29_A DTO	BT30_A DTO	BT31_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN579 (0x0486)	bt_adto_0 07_c	RESSEL (0-7)	BT32_ADT O	BT33_ADT O	BT34_ADT O	BT35_A DTO	BT36_A DTO	BT37_A DTO	BT38_A DTO	BT39_A DTO
		RESSEL (8-15)	BT40_ADT O	BT41_ADT O	BT42_ADT O	BT43_A DTO	BT44_A DTO	BT45_A DTO	BT46_A DTO	BT47_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL L[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN580 (0x0488)	bt_adto_0 07_d	RESSEL (0-7)	BT48_ADT O	BT49_ADT O	BT50_ADT O	BT51_A DTO	BT52_A DTO	BT53_A DTO	BT54_A DTO	BT55_A DTO
		RESSEL (8-15)	BT56_ADT O	BT57_ADT O	BT58_ADT O	BT59_A DTO	BT60_A DTO	BT61_A DTO	BT62_A DTO	BT63_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN581 (0x048A)	ADC0_HW TRG8	RESSEL (0-7)	PORT_PIN(ADTG0)	RLT2_UFS ET	RLT3_UFS ET	OUT16	OUT17	bt_adto_008_a	bt_adto_008_b	bt_adto_008_c
		RESSEL (8-15)	bt_adto_008_d	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN582 (0x048C)	bt_adto_0 08_a	RESSEL (0-7)	BT0_ADT O	BT1_ADT O	BT2_ADT O	BT3_AD TO	BT4_AD TO	BT5_AD TO	BT6_AD TO	BT7_AD TO
		RESSEL (8-15)	BT8_ADT O	BT9_ADT O	BT10_ADT O	BT11_A DTO	BT12_A DTO	BT13_A DTO	BT14_A DTO	BT15_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN583 (0x048E)	bt_adto_0 08_b	RESSEL (0-7)	BT16_ADT O	BT17_ADT O	BT18_ADT O	BT19_A DTO	BT20_A DTO	BT21_A DTO	BT22_A DTO	BT23_A DTO
		RESSEL (8-15)	BT24_ADT O	BT25_ADT O	BT26_ADT O	BT27_A DTO	BT28_A DTO	BT29_A DTO	BT30_A DTO	BT31_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN584 (0x0490)	bt_adto_0 08_c	RESSEL (0-7)	BT32_ADT O	BT33_ADT O	BT34_ADT O	BT35_A DTO	BT36_A DTO	BT37_A DTO	BT38_A DTO	BT39_A DTO
		RESSEL (8-15)	BT40_ADT O	BT41_ADT O	BT42_ADT O	BT43_A DTO	BT44_A DTO	BT45_A DTO	BT46_A DTO	BT47_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN585 (0x0492)	bt_adto_0 08_d	RESSEL (0-7)	BT48_ADT O	BT49_ADT O	BT50_ADT O	BT51_A DTO	BT52_A DTO	BT53_A DTO	BT54_A DTO	BT55_A DTO
		RESSEL (8-15)	BT56_ADT O	BT57_ADT O	BT58_ADT O	BT59_A DTO	BT60_A DTO	BT61_A DTO	BT62_A DTO	BT63_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN586 (0x0494)	ADC0_HW TRG9	RESSEL (0-7)	PORT_P N(ADTG0)	RLT3_UFS ET	RLT16_UF SET	OUT17	OUT18	bt_adto_ 009_a	bt_adto_ 009_b	bt_adto_ 009_c
		RESSEL (8-15)	bt_adto_0 09_d	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN587 (0x0496)	bt_adto_0 09_a	RESSEL (0-7)	BT0_ADT O	BT1_ADT O	BT2_ADT O	BT3_AD TO	BT4_AD TO	BT5_AD TO	BT6_AD TO	BT7_AD TO
		RESSEL (8-15)	BT8_ADT O	BT9_ADT O	BT10_ADT O	BT11_A DTO	BT12_A DTO	BT13_A DTO	BT14_A DTO	BT15_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN588 (0x0498)	bt_adto_0 09_b	RESSEL (0-7)	BT16_ADT O	BT17_ADT O	BT18_ADT O	BT19_A DTO	BT20_A DTO	BT21_A DTO	BT22_A DTO	BT23_A DTO
		RESSEL (8-15)	BT24_ADT O	BT25_ADT O	BT26_ADT O	BT27_A DTO	BT28_A DTO	BT29_A DTO	BT30_A DTO	BT31_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN589 (0x049A)	bt_adto_0 09_c	RESSEL (0-7)	BT32_ADT O	BT33_ADT O	BT34_ADT O	BT35_A DTO	BT36_A DTO	BT37_A DTO	BT38_A DTO	BT39_A DTO
		RESSEL (8-15)	BT40_ADT O	BT41_ADT O	BT42_ADT O	BT43_A DTO	BT44_A DTO	BT45_A DTO	BT46_A DTO	BT47_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL L[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN590 (0x049C)	bt_adto_0 09_d	RESSEL (0-7)	BT48_ADT O	BT49_ADT O	BT50_ADT O	BT51_A DTO	BT52_A DTO	BT53_A DTO	BT54_A DTO	BT55_A DTO
		RESSEL (8-15)	BT56_ADT O	BT57_ADT O	BT58_ADT O	BT59_A DTO	BT60_A DTO	BT61_A DTO	BT62_A DTO	BT63_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN591 (0x049E)	ADC0_HW TRG10	RESSEL (0-7)	PORT_PIN(ADTG0)	RLT16_UF SET	RLT17_UF SET	OUT18	OUT19	bt_adto_010_a	bt_adto_010_b	bt_adto_010_c
		RESSEL (8-15)	bt_adto_010_d	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN592 (0x04A0)	bt_adto_0 10_a	RESSEL (0-7)	BT0_ADT O	BT1_ADT O	BT2_ADT O	BT3_AD TO	BT4_AD TO	BT5_AD TO	BT6_AD TO	BT7_AD TO
		RESSEL (8-15)	BT8_ADT O	BT9_ADT O	BT10_ADT O	BT11_A DTO	BT12_A DTO	BT13_A DTO	BT14_A DTO	BT15_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN593 (0x04A2)	bt_adto_0 10_b	RESSEL (0-7)	BT16_ADT O	BT17_ADT O	BT18_ADT O	BT19_A DTO	BT20_A DTO	BT21_A DTO	BT22_A DTO	BT23_A DTO
		RESSEL (8-15)	BT24_ADT O	BT25_ADT O	BT26_ADT O	BT27_A DTO	BT28_A DTO	BT29_A DTO	BT30_A DTO	BT31_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN594 (0x04A4)	bt_adto_0 10_c	RESSEL (0-7)	BT32_ADT O	BT33_ADT O	BT34_ADT O	BT35_A DTO	BT36_A DTO	BT37_A DTO	BT38_A DTO	BT39_A DTO
		RESSEL (8-15)	BT40_ADT O	BT41_ADT O	BT42_ADT O	BT43_A DTO	BT44_A DTO	BT45_A DTO	BT46_A DTO	BT47_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN595 (0x04A6)	bt_adto_0 10_d	RESSEL (0-7)	BT48_ADT O	BT49_ADT O	BT50_ADT O	BT51_A DTO	BT52_A DTO	BT53_A DTO	BT54_A DTO	BT55_A DTO
		RESSEL (8-15)	BT56_ADT O	BT57_ADT O	BT58_ADT O	BT59_A DTO	BT60_A DTO	BT61_A DTO	BT62_A DTO	BT63_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN596 (0x04A8)	ADC0_HW TRG11	RESSEL (0-7)	PORT_PI N(ADTG0)	RLT17_UF SET	RLT0_UFS ET	OUT19	OUT20	bt_adto_ 011_a	bt_adto_ 011_b	bt_adto_ 011_c
		RESSEL (8-15)	bt_adto_01 1_d	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN597 (0x04AA)	bt_adto_01 1_a	RESSEL (0-7)	BT0_ADT O	BT1_ADT O	BT2_ADT O	BT3_AD TO	BT4_AD TO	BT5_AD TO	BT6_AD TO	BT7_AD TO
		RESSEL (8-15)	BT8_ADT O	BT9_ADT O	BT10_ADT O	BT11_A DTO	BT12_A DTO	BT13_A DTO	BT14_A DTO	BT15_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN598 (0x04AC)	bt_adto_01 1_b	RESSEL (0-7)	BT16_ADT O	BT17_ADT O	BT18_ADT O	BT19_A DTO	BT20_A DTO	BT21_A DTO	BT22_A DTO	BT23_A DTO
		RESSEL (8-15)	BT24_ADT O	BT25_ADT O	BT26_ADT O	BT27_A DTO	BT28_A DTO	BT29_A DTO	BT30_A DTO	BT31_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN599 (0x04AE)	bt_adto_01 1_c	RESSEL (0-7)	BT32_ADT O	BT33_ADT O	BT34_ADT O	BT35_A DTO	BT36_A DTO	BT37_A DTO	BT38_A DTO	BT39_A DTO
		RESSEL (8-15)	BT40_ADT O	BT41_ADT O	BT42_ADT O	BT43_A DTO	BT44_A DTO	BT45_A DTO	BT46_A DTO	BT47_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL L[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN600 (0x04B0)	bt_adto_01 1_d	RESSEL (0-7)	BT48_ADT O	BT49_ADT O	BT50_ADT O	BT51_A DTO	BT52_A DTO	BT53_A DTO	BT54_A DTO	BT55_A DTO
		RESSEL (8-15)	BT56_ADT O	BT57_ADT O	BT58_ADT O	BT59_A DTO	BT60_A DTO	BT61_A DTO	BT62_A DTO	BT63_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN601 (0x04B2)	ADC0_HW TRG12	RESSEL (0-7)	PORT_PIN(ADTG0)	RLT0_UFS ET	RLT1_UFS ET	OUT20	OUT21	bt_adto_012_a	bt_adto_012_b	bt_adto_012_c
		RESSEL (8-15)	bt_adto_012_d	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN602 (0x04B4)	bt_adto_0 12_a	RESSEL (0-7)	BT0_ADT O	BT1_ADT O	BT2_ADT O	BT3_AD TO	BT4_AD TO	BT5_AD TO	BT6_AD TO	BT7_AD TO
		RESSEL (8-15)	BT8_ADT O	BT9_ADT O	BT10_ADT O	BT11_A DTO	BT12_A DTO	BT13_A DTO	BT14_A DTO	BT15_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN603 (0x04B6)	bt_adto_0 12_b	RESSEL (0-7)	BT16_ADT O	BT17_ADT O	BT18_ADT O	BT19_A DTO	BT20_A DTO	BT21_A DTO	BT22_A DTO	BT23_A DTO
		RESSEL (8-15)	BT24_ADT O	BT25_ADT O	BT26_ADT O	BT27_A DTO	BT28_A DTO	BT29_A DTO	BT30_A DTO	BT31_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN604 (0x04B8)	bt_adto_0 12_c	RESSEL (0-7)	BT32_ADT O	BT33_ADT O	BT34_ADT O	BT35_A DTO	BT36_A DTO	BT37_A DTO	BT38_A DTO	BT39_A DTO
		RESSEL (8-15)	BT40_ADT O	BT41_ADT O	BT42_ADT O	BT43_A DTO	BT44_A DTO	BT45_A DTO	BT46_A DTO	BT47_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN605 (0x04BA)	bt_adto_0 12_d	RESSEL (0-7)	BT48_ADT O	BT49_ADT O	BT50_ADT O	BT51_A DTO	BT52_A DTO	BT53_A DTO	BT54_A DTO	BT55_A DTO
		RESSEL (8-15)	BT56_ADT O	BT57_ADT O	BT58_ADT O	BT59_A DTO	BT60_A DTO	BT61_A DTO	BT62_A DTO	BT63_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN606 (0x04BC)	ADC0_HW TRG13	RESSEL (0-7)	PORT_P N(ADTG0)	RLT1_UFS ET	RLT2_UFS ET	OUT21	OUT0	bt_adto_ 013_a	bt_adto_ 013_b	bt_adto_ 013_c
		RESSEL (8-15)	bt_adto_0 13_d	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN607 (0x04BE)	bt_adto_0 13_a	RESSEL (0-7)	BT0_ADT O	BT1_ADT O	BT2_ADT O	BT3_AD TO	BT4_AD TO	BT5_AD TO	BT6_AD TO	BT7_AD TO
		RESSEL (8-15)	BT8_ADT O	BT9_ADT O	BT10_ADT O	BT11_A DTO	BT12_A DTO	BT13_A DTO	BT14_A DTO	BT15_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN608 (0x04C0)	bt_adto_0 13_b	RESSEL (0-7)	BT16_ADT O	BT17_ADT O	BT18_ADT O	BT19_A DTO	BT20_A DTO	BT21_A DTO	BT22_A DTO	BT23_A DTO
		RESSEL (8-15)	BT24_ADT O	BT25_ADT O	BT26_ADT O	BT27_A DTO	BT28_A DTO	BT29_A DTO	BT30_A DTO	BT31_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN609 (0x04C2)	bt_adto_0 13_c	RESSEL (0-7)	BT32_ADT O	BT33_ADT O	BT34_ADT O	BT35_A DTO	BT36_A DTO	BT37_A DTO	BT38_A DTO	BT39_A DTO
		RESSEL (8-15)	BT40_ADT O	BT41_ADT O	BT42_ADT O	BT43_A DTO	BT44_A DTO	BT45_A DTO	BT46_A DTO	BT47_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN610 (0x04C4)	bt_adto_0 13_d	RESSEL (0-7)	BT48_ADT O	BT49_ADT O	BT50_ADT O	BT51_A DTO	BT52_A DTO	BT53_A DTO	BT54_A DTO	BT55_A DTO
		RESSEL (8-15)	BT56_ADT O	BT57_ADT O	BT58_ADT O	BT59_A DTO	BT60_A DTO	BT61_A DTO	BT62_A DTO	BT63_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN611 (0x04C6)	ADC0_HW TRG14	RESSEL (0-7)	PORT_PIN(ADTG0)	RLT2_UFS ET	RLT3_UFS ET	OUT0	OUT1	bt_adto_014_a	bt_adto_014_b	bt_adto_014_c
		RESSEL (8-15)	bt_adto_014_d	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN612 (0x04C8)	bt_adto_0 14_a	RESSEL (0-7)	BT0_ADT O	BT1_ADT O	BT2_ADT O	BT3_AD TO	BT4_AD TO	BT5_AD TO	BT6_AD TO	BT7_AD TO
		RESSEL (8-15)	BT8_ADT O	BT9_ADT O	BT10_ADT O	BT11_A DTO	BT12_A DTO	BT13_A DTO	BT14_A DTO	BT15_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN613 (0x04CA)	bt_adto_0 14_b	RESSEL (0-7)	BT16_ADT O	BT17_ADT O	BT18_ADT O	BT19_A DTO	BT20_A DTO	BT21_A DTO	BT22_A DTO	BT23_A DTO
		RESSEL (8-15)	BT24_ADT O	BT25_ADT O	BT26_ADT O	BT27_A DTO	BT28_A DTO	BT29_A DTO	BT30_A DTO	BT31_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN614 (0x04CC)	bt_adto_0 14_c	RESSEL (0-7)	BT32_ADT O	BT33_ADT O	BT34_ADT O	BT35_A DTO	BT36_A DTO	BT37_A DTO	BT38_A DTO	BT39_A DTO
		RESSEL (8-15)	BT40_ADT O	BT41_ADT O	BT42_ADT O	BT43_A DTO	BT44_A DTO	BT45_A DTO	BT46_A DTO	BT47_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN615 (0x04CE)	bt_adto_0 14_d	RESSEL (0-7)	BT48_ADT O	BT49_ADT O	BT50_ADT O	BT51_A DTO	BT52_A DTO	BT53_A DTO	BT54_A DTO	BT55_A DTO
		RESSEL (8-15)	BT56_ADT O	BT57_ADT O	BT58_ADT O	BT59_A DTO	BT60_A DTO	BT61_A DTO	BT62_A DTO	BT63_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN616 (0x04D0)	ADC0_HW TRG15	RESSEL (0-7)	PORT_P N(ADTG0)	RLT3_UFS ET	RLT16_UF SET	OUT1	OUT2	bt_adto_ 015_a	bt_adto_ 015_b	bt_adto_ 015_c
		RESSEL (8-15)	bt_adto_0 15_d	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN617 (0x04D2)	bt_adto_0 15_a	RESSEL (0-7)	BT0_ADT O	BT1_ADT O	BT2_ADT O	BT3_AD TO	BT4_AD TO	BT5_AD TO	BT6_AD TO	BT7_AD TO
		RESSEL (8-15)	BT8_ADT O	BT9_ADT O	BT10_ADT O	BT11_A DTO	BT12_A DTO	BT13_A DTO	BT14_A DTO	BT15_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN618 (0x04D4)	bt_adto_0 15_b	RESSEL (0-7)	BT16_ADT O	BT17_ADT O	BT18_ADT O	BT19_A DTO	BT20_A DTO	BT21_A DTO	BT22_A DTO	BT23_A DTO
		RESSEL (8-15)	BT24_ADT O	BT25_ADT O	BT26_ADT O	BT27_A DTO	BT28_A DTO	BT29_A DTO	BT30_A DTO	BT31_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN619 (0x04D6)	bt_adto_0 15_c	RESSEL (0-7)	BT32_ADT O	BT33_ADT O	BT34_ADT O	BT35_A DTO	BT36_A DTO	BT37_A DTO	BT38_A DTO	BT39_A DTO
		RESSEL (8-15)	BT40_ADT O	BT41_ADT O	BT42_ADT O	BT43_A DTO	BT44_A DTO	BT45_A DTO	BT46_A DTO	BT47_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN620 (0x04D8)	bt_adto_0 15_d	RESSEL (0-7)	BT48_ADT O	BT49_ADT O	BT50_ADT O	BT51_A DTO	BT52_A DTO	BT53_A DTO	BT54_A DTO	BT55_A DTO
		RESSEL (8-15)	BT56_ADT O	BT57_ADT O	BT58_ADT O	BT59_A DTO	BT60_A DTO	BT61_A DTO	BT62_A DTO	BT63_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN621 (0x04DA)	ADC0_HW TRG16	RESSEL (0-7)	PORT_PIN(ADTG0)	RLT16_UF SET	RLT17_UF SET	OUT2	OUT3	bt_adto_016_a	bt_adto_016_b	bt_adto_016_c
		RESSEL (8-15)	bt_adto_016_d	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN622 (0x04DC)	bt_adto_0 16_a	RESSEL (0-7)	BT0_ADT O	BT1_ADT O	BT2_ADT O	BT3_AD TO	BT4_AD TO	BT5_AD TO	BT6_AD TO	BT7_AD TO
		RESSEL (8-15)	BT8_ADT O	BT9_ADT O	BT10_ADT O	BT11_A DTO	BT12_A DTO	BT13_A DTO	BT14_A DTO	BT15_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN623 (0x04DE)	bt_adto_0 16_b	RESSEL (0-7)	BT16_ADT O	BT17_ADT O	BT18_ADT O	BT19_A DTO	BT20_A DTO	BT21_A DTO	BT22_A DTO	BT23_A DTO
		RESSEL (8-15)	BT24_ADT O	BT25_ADT O	BT26_ADT O	BT27_A DTO	BT28_A DTO	BT29_A DTO	BT30_A DTO	BT31_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN624 (0x04E0)	bt_adto_0 16_c	RESSEL (0-7)	BT32_ADT O	BT33_ADT O	BT34_ADT O	BT35_A DTO	BT36_A DTO	BT37_A DTO	BT38_A DTO	BT39_A DTO
		RESSEL (8-15)	BT40_ADT O	BT41_ADT O	BT42_ADT O	BT43_A DTO	BT44_A DTO	BT45_A DTO	BT46_A DTO	BT47_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN625 (0x04E2)	bt_adto_0 16_d	RESSEL (0-7)	BT48_ADT O	BT49_ADT O	BT50_ADT O	BT51_A DTO	BT52_A DTO	BT53_A DTO	BT54_A DTO	BT55_A DTO
		RESSEL (8-15)	BT56_ADT O	BT57_ADT O	BT58_ADT O	BT59_A DTO	BT60_A DTO	BT61_A DTO	BT62_A DTO	BT63_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN626 (0x04E4)	ADC0_HW TRG17	RESSEL (0-7)	PORT_P N(ADTG0)	RLT17_UF SET	RLT0_UFS ET	OUT3	OUT4	bt_adto_ 017_a	bt_adto_ 017_b	bt_adto_ 017_c
		RESSEL (8-15)	bt_adto_0 17_d	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN627 (0x04E6)	bt_adto_0 17_a	RESSEL (0-7)	BT0_ADT O	BT1_ADT O	BT2_ADT O	BT3_AD TO	BT4_AD TO	BT5_AD TO	BT6_AD TO	BT7_AD TO
		RESSEL (8-15)	BT8_ADT O	BT9_ADT O	BT10_ADT O	BT11_A DTO	BT12_A DTO	BT13_A DTO	BT14_A DTO	BT15_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN628 (0x04E8)	bt_adto_0 17_b	RESSEL (0-7)	BT16_ADT O	BT17_ADT O	BT18_ADT O	BT19_A DTO	BT20_A DTO	BT21_A DTO	BT22_A DTO	BT23_A DTO
		RESSEL (8-15)	BT24_ADT O	BT25_ADT O	BT26_ADT O	BT27_A DTO	BT28_A DTO	BT29_A DTO	BT30_A DTO	BT31_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN629 (0x04EA)	bt_adto_0 17_c	RESSEL (0-7)	BT32_ADT O	BT33_ADT O	BT34_ADT O	BT35_A DTO	BT36_A DTO	BT37_A DTO	BT38_A DTO	BT39_A DTO
		RESSEL (8-15)	BT40_ADT O	BT41_ADT O	BT42_ADT O	BT43_A DTO	BT44_A DTO	BT45_A DTO	BT46_A DTO	BT47_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3:0] /PORTSEL[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN630 (0x04EC)	bt_adto_0 17_d	RESSEL (0-7)	BT48_ADT O	BT49_ADT O	BT50_ADT O	BT51_A DTO	BT52_A DTO	BT53_A DTO	BT54_A DTO	BT55_A DTO
		RESSEL (8-15)	BT56_ADT O	BT57_ADT O	BT58_ADT O	BT59_A DTO	BT60_A DTO	BT61_A DTO	BT62_A DTO	BT63_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN631 (0x04EE)	ADC0_HW TRG18	RESSEL (0-7)	PORT_PIN(ADTG0)	RLT0_UFS ET	RLT1_UFS ET	OUT4	OUT5	bt_adto_018_a	bt_adto_018_b	bt_adto_018_c
		RESSEL (8-15)	bt_adto_018_d	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN632 (0x04F0)	bt_adto_0 18_a	RESSEL (0-7)	BT0_ADT O	BT1_ADT O	BT2_ADT O	BT3_AD TO	BT4_AD TO	BT5_AD TO	BT6_AD TO	BT7_AD TO
		RESSEL (8-15)	BT8_ADT O	BT9_ADT O	BT10_ADT O	BT11_A DTO	BT12_A DTO	BT13_A DTO	BT14_A DTO	BT15_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN633 (0x04F2)	bt_adto_0 18_b	RESSEL (0-7)	BT16_ADT O	BT17_ADT O	BT18_ADT O	BT19_A DTO	BT20_A DTO	BT21_A DTO	BT22_A DTO	BT23_A DTO
		RESSEL (8-15)	BT24_ADT O	BT25_ADT O	BT26_ADT O	BT27_A DTO	BT28_A DTO	BT29_A DTO	BT30_A DTO	BT31_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN634 (0x04F4)	bt_adto_0 18_c	RESSEL (0-7)	BT32_ADT O	BT33_ADT O	BT34_ADT O	BT35_A DTO	BT36_A DTO	BT37_A DTO	BT38_A DTO	BT39_A DTO
		RESSEL (8-15)	BT40_ADT O	BT41_ADT O	BT42_ADT O	BT43_A DTO	BT44_A DTO	BT45_A DTO	BT46_A DTO	BT47_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN635 (0x04F6)	bt_adto_0 18_d	RESSEL (0-7)	BT48_ADT O	BT49_ADT O	BT50_ADT O	BT51_A DTO	BT52_A DTO	BT53_A DTO	BT54_A DTO	BT55_A DTO
		RESSEL (8-15)	BT56_ADT O	BT57_ADT O	BT58_ADT O	BT59_A DTO	BT60_A DTO	BT61_A DTO	BT62_A DTO	BT63_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN636 (0x04F8)	ADC0_HW TRG19	RESSEL (0-7)	PORT_P N(ADTG0)	RLT1_UFS ET	RLT2_UFS ET	OUT5	OUT0	bt_adto_ 019_a	bt_adto_ 019_b	bt_adto_ 019_c
		RESSEL (8-15)	bt_adto_0 19_d	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN637 (0x04FA)	bt_adto_0 19_a	RESSEL (0-7)	BT0_ADT O	BT1_ADT O	BT2_ADT O	BT3_AD TO	BT4_AD TO	BT5_AD TO	BT6_AD TO	BT7_AD TO
		RESSEL (8-15)	BT8_ADT O	BT9_ADT O	BT10_ADT O	BT11_A DTO	BT12_A DTO	BT13_A DTO	BT14_A DTO	BT15_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN638 (0x04FC)	bt_adto_0 19_b	RESSEL (0-7)	BT16_ADT O	BT17_ADT O	BT18_ADT O	BT19_A DTO	BT20_A DTO	BT21_A DTO	BT22_A DTO	BT23_A DTO
		RESSEL (8-15)	BT24_ADT O	BT25_ADT O	BT26_ADT O	BT27_A DTO	BT28_A DTO	BT29_A DTO	BT30_A DTO	BT31_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN639 (0x04FE)	bt_adto_0 19_c	RESSEL (0-7)	BT32_ADT O	BT33_ADT O	BT34_ADT O	BT35_A DTO	BT36_A DTO	BT37_A DTO	BT38_A DTO	BT39_A DTO
		RESSEL (8-15)	BT40_ADT O	BT41_ADT O	BT42_ADT O	BT43_A DTO	BT44_A DTO	BT45_A DTO	BT46_A DTO	BT47_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL L[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN640 (0x0500)	bt_adto_0 19_d	RESSEL (0-7)	BT48_ADT O	BT49_ADT O	BT50_ADT O	BT51_A DTO	BT52_A DTO	BT53_A DTO	BT54_A DTO	BT55_A DTO
		RESSEL (8-15)	BT56_ADT O	BT57_ADT O	BT58_ADT O	BT59_A DTO	BT60_A DTO	BT61_A DTO	BT62_A DTO	BT63_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN641 (0x0502)	ADC0_HW TRG20	RESSEL (0-7)	PORT_P N(ADTG0)	RLT2_UFS ET	RLT3_UFS ET	OUT0	OUT1	bt_adto_ 020_a	bt_adto_ 020_b	bt_adto_ 020_c
		RESSEL (8-15)	bt_adto_0 20_d	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN642 (0x0504)	bt_adto_0 20_a	RESSEL (0-7)	BT0_ADT O	BT1_ADT O	BT2_ADT O	BT3_AD TO	BT4_AD TO	BT5_AD TO	BT6_AD TO	BT7_AD TO
		RESSEL (8-15)	BT8_ADT O	BT9_ADT O	BT10_ADT O	BT11_A DTO	BT12_A DTO	BT13_A DTO	BT14_A DTO	BT15_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN643 (0x0506)	bt_adto_0 20_b	RESSEL (0-7)	BT16_ADT O	BT17_ADT O	BT18_ADT O	BT19_A DTO	BT20_A DTO	BT21_A DTO	BT22_A DTO	BT23_A DTO
		RESSEL (8-15)	BT24_ADT O	BT25_ADT O	BT26_ADT O	BT27_A DTO	BT28_A DTO	BT29_A DTO	BT30_A DTO	BT31_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN644 (0x0508)	bt_adto_0 20_c	RESSEL (0-7)	BT32_ADT O	BT33_ADT O	BT34_ADT O	BT35_A DTO	BT36_A DTO	BT37_A DTO	BT38_A DTO	BT39_A DTO
		RESSEL (8-15)	BT40_ADT O	BT41_ADT O	BT42_ADT O	BT43_A DTO	BT44_A DTO	BT45_A DTO	BT46_A DTO	BT47_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN645 (0x050A)	bt_adto_0 20_d	RESSEL (0-7)	BT48_ADT O	BT49_ADT O	BT50_ADT O	BT51_A DTO	BT52_A DTO	BT53_A DTO	BT54_A DTO	BT55_A DTO
		RESSEL (8-15)	BT56_ADT O	BT57_ADT O	BT58_ADT O	BT59_A DTO	BT60_A DTO	BT61_A DTO	BT62_A DTO	BT63_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN646 (0x050C)	ADC0_HW TRG21	RESSEL (0-7)	PORT_P N(ADTG0)	RLT3_UFS ET	RLT16_UF SET	OUT1	OUT16	bt_adto_ 021_a	bt_adto_ 021_b	bt_adto_ 021_c
		RESSEL (8-15)	bt_adto_0 21_d	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN647 (0x050E)	bt_adto_0 21_a	RESSEL (0-7)	BT0_ADT O	BT1_ADT O	BT2_ADT O	BT3_AD TO	BT4_AD TO	BT5_AD TO	BT6_AD TO	BT7_AD TO
		RESSEL (8-15)	BT8_ADT O	BT9_ADT O	BT10_ADT O	BT11_A DTO	BT12_A DTO	BT13_A DTO	BT14_A DTO	BT15_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN648 (0x0510)	bt_adto_0 21_b	RESSEL (0-7)	BT16_ADT O	BT17_ADT O	BT18_ADT O	BT19_A DTO	BT20_A DTO	BT21_A DTO	BT22_A DTO	BT23_A DTO
		RESSEL (8-15)	BT24_ADT O	BT25_ADT O	BT26_ADT O	BT27_A DTO	BT28_A DTO	BT29_A DTO	BT30_A DTO	BT31_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN649 (0x0512)	bt_adto_0 21_c	RESSEL (0-7)	BT32_ADT O	BT33_ADT O	BT34_ADT O	BT35_A DTO	BT36_A DTO	BT37_A DTO	BT38_A DTO	BT39_A DTO
		RESSEL (8-15)	BT40_ADT O	BT41_ADT O	BT42_ADT O	BT43_A DTO	BT44_A DTO	BT45_A DTO	BT46_A DTO	BT47_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL L[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN650 (0x0514)	bt_adto_0 21_d	RESSEL (0-7)	BT48_ADT O	BT49_ADT O	BT50_ADT O	BT51_A DTO	BT52_A DTO	BT53_A DTO	BT54_A DTO	BT55_A DTO
		RESSEL (8-15)	BT56_ADT O	BT57_ADT O	BT58_ADT O	BT59_A DTO	BT60_A DTO	BT61_A DTO	BT62_A DTO	BT63_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN651 (0x0516)	ADC0_HW TRG22	RESSEL (0-7)	PORT_PIN(ADTG0)	RLT16_UF SET	RLT17_UF SET	OUT16	OUT17	bt_adto_022_a	bt_adto_022_b	bt_adto_022_c
		RESSEL (8-15)	bt_adto_022_d	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN652 (0x0518)	bt_adto_0 22_a	RESSEL (0-7)	BT0_ADT O	BT1_ADT O	BT2_ADT O	BT3_AD TO	BT4_AD TO	BT5_AD TO	BT6_AD TO	BT7_AD TO
		RESSEL (8-15)	BT8_ADT O	BT9_ADT O	BT10_ADT O	BT11_A DTO	BT12_A DTO	BT13_A DTO	BT14_A DTO	BT15_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN653 (0x051A)	bt_adto_0 22_b	RESSEL (0-7)	BT16_ADT O	BT17_ADT O	BT18_ADT O	BT19_A DTO	BT20_A DTO	BT21_A DTO	BT22_A DTO	BT23_A DTO
		RESSEL (8-15)	BT24_ADT O	BT25_ADT O	BT26_ADT O	BT27_A DTO	BT28_A DTO	BT29_A DTO	BT30_A DTO	BT31_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN654 (0x051C)	bt_adto_0 22_c	RESSEL (0-7)	BT32_ADT O	BT33_ADT O	BT34_ADT O	BT35_A DTO	BT36_A DTO	BT37_A DTO	BT38_A DTO	BT39_A DTO
		RESSEL (8-15)	BT40_ADT O	BT41_ADT O	BT42_ADT O	BT43_A DTO	BT44_A DTO	BT45_A DTO	BT46_A DTO	BT47_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN655 (0x051E)	bt_adto_0 22_d	RESSEL (0-7)	BT48_ADT O	BT49_ADT O	BT50_ADT O	BT51_A DTO	BT52_A DTO	BT53_A DTO	BT54_A DTO	BT55_A DTO
		RESSEL (8-15)	BT56_ADT O	BT57_ADT O	BT58_ADT O	BT59_A DTO	BT60_A DTO	BT61_A DTO	BT62_A DTO	BT63_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN656 (0x0520)	ADC0_HW TRG23	RESSEL (0-7)	PORT_P N(ADTG0)	RLT17_UF SET	RLT0_UFS ET	OUT17	OUT18	bt_adto_ 023_a	bt_adto_ 023_b	bt_adto_ 023_c
		RESSEL (8-15)	bt_adto_0 23_d	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN657 (0x0522)	bt_adto_0 23_a	RESSEL (0-7)	BT0_ADT O	BT1_ADT O	BT2_ADT O	BT3_AD TO	BT4_AD TO	BT5_AD TO	BT6_AD TO	BT7_AD TO
		RESSEL (8-15)	BT8_ADT O	BT9_ADT O	BT10_ADT O	BT11_A DTO	BT12_A DTO	BT13_A DTO	BT14_A DTO	BT15_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN658 (0x0524)	bt_adto_0 23_b	RESSEL (0-7)	BT16_ADT O	BT17_ADT O	BT18_ADT O	BT19_A DTO	BT20_A DTO	BT21_A DTO	BT22_A DTO	BT23_A DTO
		RESSEL (8-15)	BT24_ADT O	BT25_ADT O	BT26_ADT O	BT27_A DTO	BT28_A DTO	BT29_A DTO	BT30_A DTO	BT31_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN659 (0x0526)	bt_adto_0 23_c	RESSEL (0-7)	BT32_ADT O	BT33_ADT O	BT34_ADT O	BT35_A DTO	BT36_A DTO	BT37_A DTO	BT38_A DTO	BT39_A DTO
		RESSEL (8-15)	BT40_ADT O	BT41_ADT O	BT42_ADT O	BT43_A DTO	BT44_A DTO	BT45_A DTO	BT46_A DTO	BT47_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL L[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN660 (0x0528)	bt_adto_0 23_d	RESSEL (0-7)	BT48_ADT O	BT49_ADT O	BT50_ADT O	BT51_A DTO	BT52_A DTO	BT53_A DTO	BT54_A DTO	BT55_A DTO
		RESSEL (8-15)	BT56_ADT O	BT57_ADT O	BT58_ADT O	BT59_A DTO	BT60_A DTO	BT61_A DTO	BT62_A DTO	BT63_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN661 (0x052A)	ADC0_HW TRG24	RESSEL (0-7)	PORT_P N(ADTG0)	RLT0_UFS ET	RLT1_UFS ET	OUT18	OUT19	bt_adto_ 024_a	bt_adto_ 024_b	bt_adto_ 024_c
		RESSEL (8-15)	bt_adto_0 24_d	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN662 (0x052C)	bt_adto_0 24_a	RESSEL (0-7)	BT0_ADT O	BT1_ADT O	BT2_ADT O	BT3_AD TO	BT4_AD TO	BT5_AD TO	BT6_AD TO	BT7_AD TO
		RESSEL (8-15)	BT8_ADT O	BT9_ADT O	BT10_ADT O	BT11_A DTO	BT12_A DTO	BT13_A DTO	BT14_A DTO	BT15_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN663 (0x052E)	bt_adto_0 24_b	RESSEL (0-7)	BT16_ADT O	BT17_ADT O	BT18_ADT O	BT19_A DTO	BT20_A DTO	BT21_A DTO	BT22_A DTO	BT23_A DTO
		RESSEL (8-15)	BT24_ADT O	BT25_ADT O	BT26_ADT O	BT27_A DTO	BT28_A DTO	BT29_A DTO	BT30_A DTO	BT31_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN664 (0x0530)	bt_adto_0 24_c	RESSEL (0-7)	BT32_ADT O	BT33_ADT O	BT34_ADT O	BT35_A DTO	BT36_A DTO	BT37_A DTO	BT38_A DTO	BT39_A DTO
		RESSEL (8-15)	BT40_ADT O	BT41_ADT O	BT42_ADT O	BT43_A DTO	BT44_A DTO	BT45_A DTO	BT46_A DTO	BT47_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN665 (0x0532)	bt_adto_0 24_d	RESSEL (0-7)	BT48_ADT O	BT49_ADT O	BT50_ADT O	BT51_A DTO	BT52_A DTO	BT53_A DTO	BT54_A DTO	BT55_A DTO
		RESSEL (8-15)	BT56_ADT O	BT57_ADT O	BT58_ADT O	BT59_A DTO	BT60_A DTO	BT61_A DTO	BT62_A DTO	BT63_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN666 (0x0534)	ADC0_HW TRG25	RESSEL (0-7)	PORT_P N(ADTG0)	RLT1_UFS ET	RLT2_UFS ET	OUT19	OUT20	bt_adto_ 025_a	bt_adto_ 025_b	bt_adto_ 025_c
		RESSEL (8-15)	bt_adto_0 25_d	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN667 (0x0536)	bt_adto_0 25_a	RESSEL (0-7)	BT0_ADT O	BT1_ADT O	BT2_ADT O	BT3_AD TO	BT4_AD TO	BT5_AD TO	BT6_AD TO	BT7_AD TO
		RESSEL (8-15)	BT8_ADT O	BT9_ADT O	BT10_ADT O	BT11_A DTO	BT12_A DTO	BT13_A DTO	BT14_A DTO	BT15_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN668 (0x0538)	bt_adto_0 25_b	RESSEL (0-7)	BT16_ADT O	BT17_ADT O	BT18_ADT O	BT19_A DTO	BT20_A DTO	BT21_A DTO	BT22_A DTO	BT23_A DTO
		RESSEL (8-15)	BT24_ADT O	BT25_ADT O	BT26_ADT O	BT27_A DTO	BT28_A DTO	BT29_A DTO	BT30_A DTO	BT31_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN669 (0x053A)	bt_adto_0 25_c	RESSEL (0-7)	BT32_ADT O	BT33_ADT O	BT34_ADT O	BT35_A DTO	BT36_A DTO	BT37_A DTO	BT38_A DTO	BT39_A DTO
		RESSEL (8-15)	BT40_ADT O	BT41_ADT O	BT42_ADT O	BT43_A DTO	BT44_A DTO	BT45_A DTO	BT46_A DTO	BT47_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL L[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN670 (0x053C)	bt_adto_0 25_d	RESSEL (0-7)	BT48_ADT O	BT49_ADT O	BT50_ADT O	BT51_A DTO	BT52_A DTO	BT53_A DTO	BT54_A DTO	BT55_A DTO
		RESSEL (8-15)	BT56_ADT O	BT57_ADT O	BT58_ADT O	BT59_A DTO	BT60_A DTO	BT61_A DTO	BT62_A DTO	BT63_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN671 (0x053E)	ADC0_HW TRG26	RESSEL (0-7)	PORT_P N(ADTG0)	RLT2_UFS ET	RLT3_UFS ET	OUT20	OUT21	bt_adto_ 026_a	bt_adto_ 026_b	bt_adto_ 026_c
		RESSEL (8-15)	bt_adto_0 26_d	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN672 (0x0540)	bt_adto_0 26_a	RESSEL (0-7)	BT0_ADT O	BT1_ADT O	BT2_ADT O	BT3_AD TO	BT4_AD TO	BT5_AD TO	BT6_AD TO	BT7_AD TO
		RESSEL (8-15)	BT8_ADT O	BT9_ADT O	BT10_ADT O	BT11_A DTO	BT12_A DTO	BT13_A DTO	BT14_A DTO	BT15_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN673 (0x0542)	bt_adto_0 26_b	RESSEL (0-7)	BT16_ADT O	BT17_ADT O	BT18_ADT O	BT19_A DTO	BT20_A DTO	BT21_A DTO	BT22_A DTO	BT23_A DTO
		RESSEL (8-15)	BT24_ADT O	BT25_ADT O	BT26_ADT O	BT27_A DTO	BT28_A DTO	BT29_A DTO	BT30_A DTO	BT31_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN674 (0x0544)	bt_adto_0 26_c	RESSEL (0-7)	BT32_ADT O	BT33_ADT O	BT34_ADT O	BT35_A DTO	BT36_A DTO	BT37_A DTO	BT38_A DTO	BT39_A DTO
		RESSEL (8-15)	BT40_ADT O	BT41_ADT O	BT42_ADT O	BT43_A DTO	BT44_A DTO	BT45_A DTO	BT46_A DTO	BT47_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN675 (0x0546)	bt_adto_0 26_d	RESSEL (0-7)	BT48_ADT O	BT49_ADT O	BT50_ADT O	BT51_A DTO	BT52_A DTO	BT53_A DTO	BT54_A DTO	BT55_A DTO
		RESSEL (8-15)	BT56_ADT O	BT57_ADT O	BT58_ADT O	BT59_A DTO	BT60_A DTO	BT61_A DTO	BT62_A DTO	BT63_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN676 (0x0548)	ADC0_HW TRG27	RESSEL (0-7)	PORT_P N(ADTG0)	RLT3_UFS ET	RLT16_UF SET	OUT21	OUT0	bt_adto_ 027_a	bt_adto_ 027_b	bt_adto_ 027_c
		RESSEL (8-15)	bt_adto_0 27_d	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN677 (0x054A)	bt_adto_0 27_a	RESSEL (0-7)	BT0_ADT O	BT1_ADT O	BT2_ADT O	BT3_AD TO	BT4_AD TO	BT5_AD TO	BT6_AD TO	BT7_AD TO
		RESSEL (8-15)	BT8_ADT O	BT9_ADT O	BT10_ADT O	BT11_A DTO	BT12_A DTO	BT13_A DTO	BT14_A DTO	BT15_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN678 (0x054C)	bt_adto_0 27_b	RESSEL (0-7)	BT16_ADT O	BT17_ADT O	BT18_ADT O	BT19_A DTO	BT20_A DTO	BT21_A DTO	BT22_A DTO	BT23_A DTO
		RESSEL (8-15)	BT24_ADT O	BT25_ADT O	BT26_ADT O	BT27_A DTO	BT28_A DTO	BT29_A DTO	BT30_A DTO	BT31_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN679 (0x054E)	bt_adto_0 27_c	RESSEL (0-7)	BT32_ADT O	BT33_ADT O	BT34_ADT O	BT35_A DTO	BT36_A DTO	BT37_A DTO	BT38_A DTO	BT39_A DTO
		RESSEL (8-15)	BT40_ADT O	BT41_ADT O	BT42_ADT O	BT43_A DTO	BT44_A DTO	BT45_A DTO	BT46_A DTO	BT47_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL L[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN680 (0x0550)	bt_adto_0 27_d	RESSEL (0-7)	BT48_ADT O	BT49_ADT O	BT50_ADT O	BT51_A DTO	BT52_A DTO	BT53_A DTO	BT54_A DTO	BT55_A DTO
		RESSEL (8-15)	BT56_ADT O	BT57_ADT O	BT58_ADT O	BT59_A DTO	BT60_A DTO	BT61_A DTO	BT62_A DTO	BT63_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN681 (0x0552)	ADC0_HW TRG28	RESSEL (0-7)	PORT_PIN(ADTG0)	RLT16_UF SET	RLT17_UF SET	OUT0	OUT1	bt_adto_028_a	bt_adto_028_b	bt_adto_028_c
		RESSEL (8-15)	bt_adto_028_d	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN682 (0x0554)	bt_adto_0 28_a	RESSEL (0-7)	BT0_ADT O	BT1_ADT O	BT2_ADT O	BT3_AD TO	BT4_AD TO	BT5_AD TO	BT6_AD TO	BT7_AD TO
		RESSEL (8-15)	BT8_ADT O	BT9_ADT O	BT10_ADT O	BT11_A DTO	BT12_A DTO	BT13_A DTO	BT14_A DTO	BT15_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN683 (0x0556)	bt_adto_0 28_b	RESSEL (0-7)	BT16_ADT O	BT17_ADT O	BT18_ADT O	BT19_A DTO	BT20_A DTO	BT21_A DTO	BT22_A DTO	BT23_A DTO
		RESSEL (8-15)	BT24_ADT O	BT25_ADT O	BT26_ADT O	BT27_A DTO	BT28_A DTO	BT29_A DTO	BT30_A DTO	BT31_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN684 (0x0558)	bt_adto_0 28_c	RESSEL (0-7)	BT32_ADT O	BT33_ADT O	BT34_ADT O	BT35_A DTO	BT36_A DTO	BT37_A DTO	BT38_A DTO	BT39_A DTO
		RESSEL (8-15)	BT40_ADT O	BT41_ADT O	BT42_ADT O	BT43_A DTO	BT44_A DTO	BT45_A DTO	BT46_A DTO	BT47_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN685 (0x055A)	bt_adto_0 28_d	RESSEL (0-7)	BT48_ADT O	BT49_ADT O	BT50_ADT O	BT51_A DTO	BT52_A DTO	BT53_A DTO	BT54_A DTO	BT55_A DTO
		RESSEL (8-15)	BT56_ADT O	BT57_ADT O	BT58_ADT O	BT59_A DTO	BT60_A DTO	BT61_A DTO	BT62_A DTO	BT63_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN686 (0x055C)	ADC0_HW TRG29	RESSEL (0-7)	PORT_P N(ADTG0)	RLT17_UF SET	RLT0_UFS ET	OUT1	OUT2	bt_adto_ 029_a	bt_adto_ 029_b	bt_adto_ 029_c
		RESSEL (8-15)	bt_adto_0 29_d	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN687 (0x055E)	bt_adto_0 29_a	RESSEL (0-7)	BT0_ADT O	BT1_ADT O	BT2_ADT O	BT3_AD TO	BT4_AD TO	BT5_AD TO	BT6_AD TO	BT7_AD TO
		RESSEL (8-15)	BT8_ADT O	BT9_ADT O	BT10_ADT O	BT11_A DTO	BT12_A DTO	BT13_A DTO	BT14_A DTO	BT15_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN688 (0x0560)	bt_adto_0 29_b	RESSEL (0-7)	BT16_ADT O	BT17_ADT O	BT18_ADT O	BT19_A DTO	BT20_A DTO	BT21_A DTO	BT22_A DTO	BT23_A DTO
		RESSEL (8-15)	BT24_ADT O	BT25_ADT O	BT26_ADT O	BT27_A DTO	BT28_A DTO	BT29_A DTO	BT30_A DTO	BT31_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN689 (0x0562)	bt_adto_0 29_c	RESSEL (0-7)	BT32_ADT O	BT33_ADT O	BT34_ADT O	BT35_A DTO	BT36_A DTO	BT37_A DTO	BT38_A DTO	BT39_A DTO
		RESSEL (8-15)	BT40_ADT O	BT41_ADT O	BT42_ADT O	BT43_A DTO	BT44_A DTO	BT45_A DTO	BT46_A DTO	BT47_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL L[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN690 (0x0564)	bt_adto_0 29_d	RESSEL (0-7)	BT48_ADT O	BT49_ADT O	BT50_ADT O	BT51_A DTO	BT52_A DTO	BT53_A DTO	BT54_A DTO	BT55_A DTO
		RESSEL (8-15)	BT56_ADT O	BT57_ADT O	BT58_ADT O	BT59_A DTO	BT60_A DTO	BT61_A DTO	BT62_A DTO	BT63_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN691 (0x0566)	ADC0_HW TRG30	RESSEL (0-7)	PORT_PIN(ADTG0)	RLT0_UFS ET	RLT1_UFS ET	OUT2	OUT3	bt_adto_030_a	bt_adto_030_b	bt_adto_030_c
		RESSEL (8-15)	bt_adto_030_d	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN692 (0x0568)	bt_adto_0 30_a	RESSEL (0-7)	BT0_ADT O	BT1_ADT O	BT2_ADT O	BT3_AD TO	BT4_AD TO	BT5_AD TO	BT6_AD TO	BT7_AD TO
		RESSEL (8-15)	BT8_ADT O	BT9_ADT O	BT10_ADT O	BT11_A DTO	BT12_A DTO	BT13_A DTO	BT14_A DTO	BT15_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN693 (0x056A)	bt_adto_0 30_b	RESSEL (0-7)	BT16_ADT O	BT17_ADT O	BT18_ADT O	BT19_A DTO	BT20_A DTO	BT21_A DTO	BT22_A DTO	BT23_A DTO
		RESSEL (8-15)	BT24_ADT O	BT25_ADT O	BT26_ADT O	BT27_A DTO	BT28_A DTO	BT29_A DTO	BT30_A DTO	BT31_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN694 (0x056C)	bt_adto_0 30_c	RESSEL (0-7)	BT32_ADT O	BT33_ADT O	BT34_ADT O	BT35_A DTO	BT36_A DTO	BT37_A DTO	BT38_A DTO	BT39_A DTO
		RESSEL (8-15)	BT40_ADT O	BT41_ADT O	BT42_ADT O	BT43_A DTO	BT44_A DTO	BT45_A DTO	BT46_A DTO	BT47_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN695 (0x056E)	bt_adto_0 30_d	RESSEL (0-7)	BT48_ADT O	BT49_ADT O	BT50_ADT O	BT51_A DTO	BT52_A DTO	BT53_A DTO	BT54_A DTO	BT55_A DTO
		RESSEL (8-15)	BT56_ADT O	BT57_ADT O	BT58_ADT O	BT59_A DTO	BT60_A DTO	BT61_A DTO	BT62_A DTO	BT63_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN696 (0x0570)	ADC0_HW TRG31	RESSEL (0-7)	PORT_P N(ADTG0)	RLT1_UFS ET	RLT2_UFS ET	OUT3	OUT4	bt_adto_ 031_a	bt_adto_ 031_b	bt_adto_ 031_c
		RESSEL (8-15)	bt_adto_0 31_d	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN697 (0x0572)	bt_adto_0 31_a	RESSEL (0-7)	BT0_ADT O	BT1_ADT O	BT2_ADT O	BT3_AD TO	BT4_AD TO	BT5_AD TO	BT6_AD TO	BT7_AD TO
		RESSEL (8-15)	BT8_ADT O	BT9_ADT O	BT10_ADT O	BT11_A DTO	BT12_A DTO	BT13_A DTO	BT14_A DTO	BT15_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN698 (0x0574)	bt_adto_0 31_b	RESSEL (0-7)	BT16_ADT O	BT17_ADT O	BT18_ADT O	BT19_A DTO	BT20_A DTO	BT21_A DTO	BT22_A DTO	BT23_A DTO
		RESSEL (8-15)	BT24_ADT O	BT25_ADT O	BT26_ADT O	BT27_A DTO	BT28_A DTO	BT29_A DTO	BT30_A DTO	BT31_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN699 (0x0576)	bt_adto_0 31_c	RESSEL (0-7)	BT32_ADT O	BT33_ADT O	BT34_ADT O	BT35_A DTO	BT36_A DTO	BT37_A DTO	BT38_A DTO	BT39_A DTO
		RESSEL (8-15)	BT40_ADT O	BT41_ADT O	BT42_ADT O	BT43_A DTO	BT44_A DTO	BT45_A DTO	BT46_A DTO	BT47_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL L[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN700 (0x0578)	bt_adto_0 31_d	RESSEL (0-7)	BT48_ADT O	BT49_ADT O	BT50_ADT O	BT51_A DTO	BT52_A DTO	BT53_A DTO	BT54_A DTO	BT55_A DTO
		RESSEL (8-15)	BT56_ADT O	BT57_ADT O	BT58_ADT O	BT59_A DTO	BT60_A DTO	BT61_A DTO	BT62_A DTO	BT63_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN701 (0x057A)	ADC1_HW TRG0	RESSEL (0-7)	PORT_P N(ADTG0)	RLT0_UFS ET	RLT1_UFS ET	OUT4	OUT5	bt_adto_ 100_a	bt_adto_ 100_b	bt_adto_ 100_c
		RESSEL (8-15)	bt_adto_1 00_d	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN702 (0x057C)	bt_adto_1 00_a	RESSEL (0-7)	BT0_ADT O	BT1_ADT O	BT2_ADT O	BT3_AD TO	BT4_AD TO	BT5_AD TO	BT6_AD TO	BT7_AD TO
		RESSEL (8-15)	BT8_ADT O	BT9_ADT O	BT10_ADT O	BT11_A DTO	BT12_A DTO	BT13_A DTO	BT14_A DTO	BT15_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN703 (0x057E)	bt_adto_1 00_b	RESSEL (0-7)	BT16_ADT O	BT17_ADT O	BT18_ADT O	BT19_A DTO	BT20_A DTO	BT21_A DTO	BT22_A DTO	BT23_A DTO
		RESSEL (8-15)	BT24_ADT O	BT25_ADT O	BT26_ADT O	BT27_A DTO	BT28_A DTO	BT29_A DTO	BT30_A DTO	BT31_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN704 (0x0580)	bt_adto_1 00_c	RESSEL (0-7)	BT32_ADT O	BT33_ADT O	BT34_ADT O	BT35_A DTO	BT36_A DTO	BT37_A DTO	BT38_A DTO	BT39_A DTO
		RESSEL (8-15)	BT40_ADT O	BT41_ADT O	BT42_ADT O	BT43_A DTO	BT44_A DTO	BT45_A DTO	BT46_A DTO	BT47_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN705 (0x0582)	bt_adto_1 00_d	RESSEL (0-7)	BT48_ADT O	BT49_ADT O	BT50_ADT O	BT51_A DTO	BT52_A DTO	BT53_A DTO	BT54_A DTO	BT55_A DTO
		RESSEL (8-15)	BT56_ADT O	BT57_ADT O	BT58_ADT O	BT59_A DTO	BT60_A DTO	BT61_A DTO	BT62_A DTO	BT63_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN706 (0x0584)	ADC1_HW TRG1	RESSEL (0-7)	PORT_P N(ADTG0)	RLT1_UFS ET	RLT2_UFS ET	OUT5	OUT0	bt_adto_ 101_a	bt_adto_ 101_b	bt_adto_ 101_c
		RESSEL (8-15)	bt_adto_1 01_d	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN707 (0x0586)	bt_adto_1 01_a	RESSEL (0-7)	BT0_ADT O	BT1_ADT O	BT2_ADT O	BT3_AD TO	BT4_AD TO	BT5_AD TO	BT6_AD TO	BT7_AD TO
		RESSEL (8-15)	BT8_ADT O	BT9_ADT O	BT10_ADT O	BT11_A DTO	BT12_A DTO	BT13_A DTO	BT14_A DTO	BT15_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN708 (0x0588)	bt_adto_1 01_b	RESSEL (0-7)	BT16_ADT O	BT17_ADT O	BT18_ADT O	BT19_A DTO	BT20_A DTO	BT21_A DTO	BT22_A DTO	BT23_A DTO
		RESSEL (8-15)	BT24_ADT O	BT25_ADT O	BT26_ADT O	BT27_A DTO	BT28_A DTO	BT29_A DTO	BT30_A DTO	BT31_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN709 (0x058A)	bt_adto_1 01_c	RESSEL (0-7)	BT32_ADT O	BT33_ADT O	BT34_ADT O	BT35_A DTO	BT36_A DTO	BT37_A DTO	BT38_A DTO	BT39_A DTO
		RESSEL (8-15)	BT40_ADT O	BT41_ADT O	BT42_ADT O	BT43_A DTO	BT44_A DTO	BT45_A DTO	BT46_A DTO	BT47_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL L[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN710 (0x058C)	bt_adto_1 01_d	RESSEL (0-7)	BT48_ADT O	BT49_ADT O	BT50_ADT O	BT51_A DTO	BT52_A DTO	BT53_A DTO	BT54_A DTO	BT55_A DTO
		RESSEL (8-15)	BT56_ADT O	BT57_ADT O	BT58_ADT O	BT59_A DTO	BT60_A DTO	BT61_A DTO	BT62_A DTO	BT63_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN711 (0x058E)	ADC1_HW TRG2	RESSEL (0-7)	PORT_PIN(ADTG0)	RLT2_UFS ET	RLT3_UFS ET	OUT0	OUT1	bt_adto_102_a	bt_adto_102_b	bt_adto_102_c
		RESSEL (8-15)	bt_adto_102_d	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN712 (0x0590)	bt_adto_1 02_a	RESSEL (0-7)	BT0_ADT O	BT1_ADT O	BT2_ADT O	BT3_AD TO	BT4_AD TO	BT5_AD TO	BT6_AD TO	BT7_AD TO
		RESSEL (8-15)	BT8_ADT O	BT9_ADT O	BT10_ADT O	BT11_A DTO	BT12_A DTO	BT13_A DTO	BT14_A DTO	BT15_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN713 (0x0592)	bt_adto_1 02_b	RESSEL (0-7)	BT16_ADT O	BT17_ADT O	BT18_ADT O	BT19_A DTO	BT20_A DTO	BT21_A DTO	BT22_A DTO	BT23_A DTO
		RESSEL (8-15)	BT24_ADT O	BT25_ADT O	BT26_ADT O	BT27_A DTO	BT28_A DTO	BT29_A DTO	BT30_A DTO	BT31_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN714 (0x0594)	bt_adto_1 02_c	RESSEL (0-7)	BT32_ADT O	BT33_ADT O	BT34_ADT O	BT35_A DTO	BT36_A DTO	BT37_A DTO	BT38_A DTO	BT39_A DTO
		RESSEL (8-15)	BT40_ADT O	BT41_ADT O	BT42_ADT O	BT43_A DTO	BT44_A DTO	BT45_A DTO	BT46_A DTO	BT47_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN715 (0x0596)	bt_adto_1 02_d	RESSEL (0-7)	BT48_ADT O	BT49_ADT O	BT50_ADT O	BT51_A DTO	BT52_A DTO	BT53_A DTO	BT54_A DTO	BT55_A DTO
		RESSEL (8-15)	BT56_ADT O	BT57_ADT O	BT58_ADT O	BT59_A DTO	BT60_A DTO	BT61_A DTO	BT62_A DTO	BT63_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN716 (0x0598)	ADC1_HW TRG3	RESSEL (0-7)	PORT_P N(ADTG0)	RLT3_UFS ET	RLT16_UF SET	OUT1	OUT16	bt_adto_ 103_a	bt_adto_ 103_b	bt_adto_ 103_c
		RESSEL (8-15)	bt_adto_1 03_d	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN717 (0x059A)	bt_adto_1 03_a	RESSEL (0-7)	BT0_ADT O	BT1_ADT O	BT2_ADT O	BT3_AD TO	BT4_AD TO	BT5_AD TO	BT6_AD TO	BT7_AD TO
		RESSEL (8-15)	BT8_ADT O	BT9_ADT O	BT10_ADT O	BT11_A DTO	BT12_A DTO	BT13_A DTO	BT14_A DTO	BT15_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN718 (0x059C)	bt_adto_1 03_b	RESSEL (0-7)	BT16_ADT O	BT17_ADT O	BT18_ADT O	BT19_A DTO	BT20_A DTO	BT21_A DTO	BT22_A DTO	BT23_A DTO
		RESSEL (8-15)	BT24_ADT O	BT25_ADT O	BT26_ADT O	BT27_A DTO	BT28_A DTO	BT29_A DTO	BT30_A DTO	BT31_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN719 (0x059E)	bt_adto_1 03_c	RESSEL (0-7)	BT32_ADT O	BT33_ADT O	BT34_ADT O	BT35_A DTO	BT36_A DTO	BT37_A DTO	BT38_A DTO	BT39_A DTO
		RESSEL (8-15)	BT40_ADT O	BT41_ADT O	BT42_ADT O	BT43_A DTO	BT44_A DTO	BT45_A DTO	BT46_A DTO	BT47_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN720 (0x05A0)	bt_adto_1 03_d	RESSEL (0-7)	BT48_ADT O	BT49_ADT O	BT50_ADT O	BT51_A DTO	BT52_A DTO	BT53_A DTO	BT54_A DTO	BT55_A DTO
		RESSEL (8-15)	BT56_ADT O	BT57_ADT O	BT58_ADT O	BT59_A DTO	BT60_A DTO	BT61_A DTO	BT62_A DTO	BT63_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN721 (0x05A2)	ADC1_HW TRG4	RESSEL (0-7)	PORT_PIN(ADTG0)	RLT16_UF SET	RLT17_UF SET	OUT16	OUT17	bt_adto_104_a	bt_adto_104_b	bt_adto_104_c
		RESSEL (8-15)	bt_adto_104_d	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN722 (0x05A4)	bt_adto_1 04_a	RESSEL (0-7)	BT0_ADT O	BT1_ADT O	BT2_ADT O	BT3_AD TO	BT4_AD TO	BT5_AD TO	BT6_AD TO	BT7_AD TO
		RESSEL (8-15)	BT8_ADT O	BT9_ADT O	BT10_ADT O	BT11_A DTO	BT12_A DTO	BT13_A DTO	BT14_A DTO	BT15_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN723 (0x05A6)	bt_adto_1 04_b	RESSEL (0-7)	BT16_ADT O	BT17_ADT O	BT18_ADT O	BT19_A DTO	BT20_A DTO	BT21_A DTO	BT22_A DTO	BT23_A DTO
		RESSEL (8-15)	BT24_ADT O	BT25_ADT O	BT26_ADT O	BT27_A DTO	BT28_A DTO	BT29_A DTO	BT30_A DTO	BT31_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN724 (0x05A8)	bt_adto_1 04_c	RESSEL (0-7)	BT32_ADT O	BT33_ADT O	BT34_ADT O	BT35_A DTO	BT36_A DTO	BT37_A DTO	BT38_A DTO	BT39_A DTO
		RESSEL (8-15)	BT40_ADT O	BT41_ADT O	BT42_ADT O	BT43_A DTO	BT44_A DTO	BT45_A DTO	BT46_A DTO	BT47_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN725 (0x05AA)	bt_adto_1 04_d	RESSEL (0-7)	BT48_ADT O	BT49_ADT O	BT50_ADT O	BT51_A DTO	BT52_A DTO	BT53_A DTO	BT54_A DTO	BT55_A DTO
		RESSEL (8-15)	BT56_ADT O	BT57_ADT O	BT58_ADT O	BT59_A DTO	BT60_A DTO	BT61_A DTO	BT62_A DTO	BT63_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN726 (0x05AC)	ADC1_HW TRG5	RESSEL (0-7)	PORT_P N(ADTG0)	RLT17_UF SET	RLT0_UFS ET	OUT17	OUT18	bt_adto_ 105_a	bt_adto_ 105_b	bt_adto_ 105_c
		RESSEL (8-15)	bt_adto_1 05_d	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN727 (0x05AE)	bt_adto_1 05_a	RESSEL (0-7)	BT0_ADT O	BT1_ADT O	BT2_ADT O	BT3_AD TO	BT4_AD TO	BT5_AD TO	BT6_AD TO	BT7_AD TO
		RESSEL (8-15)	BT8_ADT O	BT9_ADT O	BT10_ADT O	BT11_A DTO	BT12_A DTO	BT13_A DTO	BT14_A DTO	BT15_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN728 (0x05B0)	bt_adto_1 05_b	RESSEL (0-7)	BT16_ADT O	BT17_ADT O	BT18_ADT O	BT19_A DTO	BT20_A DTO	BT21_A DTO	BT22_A DTO	BT23_A DTO
		RESSEL (8-15)	BT24_ADT O	BT25_ADT O	BT26_ADT O	BT27_A DTO	BT28_A DTO	BT29_A DTO	BT30_A DTO	BT31_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN729 (0x05B2)	bt_adto_1 05_c	RESSEL (0-7)	BT32_ADT O	BT33_ADT O	BT34_ADT O	BT35_A DTO	BT36_A DTO	BT37_A DTO	BT38_A DTO	BT39_A DTO
		RESSEL (8-15)	BT40_ADT O	BT41_ADT O	BT42_ADT O	BT43_A DTO	BT44_A DTO	BT45_A DTO	BT46_A DTO	BT47_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3:0] /PORTSEL[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN730 (0x05B4)	bt_adto_1 05_d	RESSEL (0-7)	BT48_ADT O	BT49_ADT O	BT50_ADT O	BT51_A DTO	BT52_A DTO	BT53_A DTO	BT54_A DTO	BT55_A DTO
		RESSEL (8-15)	BT56_ADT O	BT57_ADT O	BT58_ADT O	BT59_A DTO	BT60_A DTO	BT61_A DTO	BT62_A DTO	BT63_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN731 (0x05B6)	ADC1_HW TRG6	RESSEL (0-7)	PORT_PIN(ADTG0)	RLT0_UFS ET	RLT1_UFS ET	OUT18	OUT19	bt_adto_106_a	bt_adto_106_b	bt_adto_106_c
		RESSEL (8-15)	bt_adto_106_d	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN732 (0x05B8)	bt_adto_1 06_a	RESSEL (0-7)	BT0_ADT O	BT1_ADT O	BT2_ADT O	BT3_AD TO	BT4_AD TO	BT5_AD TO	BT6_AD TO	BT7_AD TO
		RESSEL (8-15)	BT8_ADT O	BT9_ADT O	BT10_ADT O	BT11_A DTO	BT12_A DTO	BT13_A DTO	BT14_A DTO	BT15_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN733 (0x05BA)	bt_adto_1 06_b	RESSEL (0-7)	BT16_ADT O	BT17_ADT O	BT18_ADT O	BT19_A DTO	BT20_A DTO	BT21_A DTO	BT22_A DTO	BT23_A DTO
		RESSEL (8-15)	BT24_ADT O	BT25_ADT O	BT26_ADT O	BT27_A DTO	BT28_A DTO	BT29_A DTO	BT30_A DTO	BT31_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN734 (0x05BC)	bt_adto_1 06_c	RESSEL (0-7)	BT32_ADT O	BT33_ADT O	BT34_ADT O	BT35_A DTO	BT36_A DTO	BT37_A DTO	BT38_A DTO	BT39_A DTO
		RESSEL (8-15)	BT40_ADT O	BT41_ADT O	BT42_ADT O	BT43_A DTO	BT44_A DTO	BT45_A DTO	BT46_A DTO	BT47_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN735 (0x05BE)	bt_adto_1 06_d	RESSEL (0-7)	BT48_ADT O	BT49_ADT O	BT50_ADT O	BT51_A DTO	BT52_A DTO	BT53_A DTO	BT54_A DTO	BT55_A DTO
		RESSEL (8-15)	BT56_ADT O	BT57_ADT O	BT58_ADT O	BT59_A DTO	BT60_A DTO	BT61_A DTO	BT62_A DTO	BT63_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN736 (0x05C0)	ADC1_HW TRG7	RESSEL (0-7)	PORT_P N(ADTG0)	RLT1_UFS ET	RLT2_UFS ET	OUT19	OUT20	bt_adto_ 107_a	bt_adto_ 107_b	bt_adto_ 107_c
		RESSEL (8-15)	bt_adto_1 07_d	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN737 (0x05C2)	bt_adto_1 07_a	RESSEL (0-7)	BT0_ADT O	BT1_ADT O	BT2_ADT O	BT3_AD TO	BT4_AD TO	BT5_AD TO	BT6_AD TO	BT7_AD TO
		RESSEL (8-15)	BT8_ADT O	BT9_ADT O	BT10_ADT O	BT11_A DTO	BT12_A DTO	BT13_A DTO	BT14_A DTO	BT15_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN738 (0x05C4)	bt_adto_1 07_b	RESSEL (0-7)	BT16_ADT O	BT17_ADT O	BT18_ADT O	BT19_A DTO	BT20_A DTO	BT21_A DTO	BT22_A DTO	BT23_A DTO
		RESSEL (8-15)	BT24_ADT O	BT25_ADT O	BT26_ADT O	BT27_A DTO	BT28_A DTO	BT29_A DTO	BT30_A DTO	BT31_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN739 (0x05C6)	bt_adto_1 07_c	RESSEL (0-7)	BT32_ADT O	BT33_ADT O	BT34_ADT O	BT35_A DTO	BT36_A DTO	BT37_A DTO	BT38_A DTO	BT39_A DTO
		RESSEL (8-15)	BT40_ADT O	BT41_ADT O	BT42_ADT O	BT43_A DTO	BT44_A DTO	BT45_A DTO	BT46_A DTO	BT47_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3:0] /PORTSEL[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN740 (0x05C8)	bt_adto_1 07_d	RESSEL (0-7)	BT48_ADT O	BT49_ADT O	BT50_ADT O	BT51_A DTO	BT52_A DTO	BT53_A DTO	BT54_A DTO	BT55_A DTO
		RESSEL (8-15)	BT56_ADT O	BT57_ADT O	BT58_ADT O	BT59_A DTO	BT60_A DTO	BT61_A DTO	BT62_A DTO	BT63_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN741 (0x05CA)	ADC1_HW TRG8	RESSEL (0-7)	PORT_PIN(ADTG0)	RLT2_UFS ET	RLT3_UFS ET	OUT20	OUT21	bt_adto_108_a	bt_adto_108_b	bt_adto_108_c
		RESSEL (8-15)	bt_adto_108_d	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN742 (0x05CC)	bt_adto_1 08_a	RESSEL (0-7)	BT0_ADT O	BT1_ADT O	BT2_ADT O	BT3_AD TO	BT4_AD TO	BT5_AD TO	BT6_AD TO	BT7_AD TO
		RESSEL (8-15)	BT8_ADT O	BT9_ADT O	BT10_ADT O	BT11_A DTO	BT12_A DTO	BT13_A DTO	BT14_A DTO	BT15_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN743 (0x05CE)	bt_adto_1 08_b	RESSEL (0-7)	BT16_ADT O	BT17_ADT O	BT18_ADT O	BT19_A DTO	BT20_A DTO	BT21_A DTO	BT22_A DTO	BT23_A DTO
		RESSEL (8-15)	BT24_ADT O	BT25_ADT O	BT26_ADT O	BT27_A DTO	BT28_A DTO	BT29_A DTO	BT30_A DTO	BT31_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN744 (0x05D0)	bt_adto_1 08_c	RESSEL (0-7)	BT32_ADT O	BT33_ADT O	BT34_ADT O	BT35_A DTO	BT36_A DTO	BT37_A DTO	BT38_A DTO	BT39_A DTO
		RESSEL (8-15)	BT40_ADT O	BT41_ADT O	BT42_ADT O	BT43_A DTO	BT44_A DTO	BT45_A DTO	BT46_A DTO	BT47_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN745 (0x05D2)	bt_adto_1 08_d	RESSEL (0-7)	BT48_ADT O	BT49_ADT O	BT50_ADT O	BT51_A DTO	BT52_A DTO	BT53_A DTO	BT54_A DTO	BT55_A DTO
		RESSEL (8-15)	BT56_ADT O	BT57_ADT O	BT58_ADT O	BT59_A DTO	BT60_A DTO	BT61_A DTO	BT62_A DTO	BT63_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN746 (0x05D4)	ADC1_HW TRG9	RESSEL (0-7)	PORT_P N(ADTG0)	RLT3_UFS ET	RLT16_UF SET	OUT21	OUT0	bt_adto_ 109_a	bt_adto_ 109_b	bt_adto_ 109_c
		RESSEL (8-15)	bt_adto_1 09_d	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN747 (0x05D6)	bt_adto_1 09_a	RESSEL (0-7)	BT0_ADT O	BT1_ADT O	BT2_ADT O	BT3_AD TO	BT4_AD TO	BT5_AD TO	BT6_AD TO	BT7_AD TO
		RESSEL (8-15)	BT8_ADT O	BT9_ADT O	BT10_ADT O	BT11_A DTO	BT12_A DTO	BT13_A DTO	BT14_A DTO	BT15_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN748 (0x05D8)	bt_adto_1 09_b	RESSEL (0-7)	BT16_ADT O	BT17_ADT O	BT18_ADT O	BT19_A DTO	BT20_A DTO	BT21_A DTO	BT22_A DTO	BT23_A DTO
		RESSEL (8-15)	BT24_ADT O	BT25_ADT O	BT26_ADT O	BT27_A DTO	BT28_A DTO	BT29_A DTO	BT30_A DTO	BT31_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN749 (0x05DA)	bt_adto_1 09_c	RESSEL (0-7)	BT32_ADT O	BT33_ADT O	BT34_ADT O	BT35_A DTO	BT36_A DTO	BT37_A DTO	BT38_A DTO	BT39_A DTO
		RESSEL (8-15)	BT40_ADT O	BT41_ADT O	BT42_ADT O	BT43_A DTO	BT44_A DTO	BT45_A DTO	BT46_A DTO	BT47_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN750 (0x05DC)	bt_adto_1 09_d	RESSEL (0-7)	BT48_ADT O	BT49_ADT O	BT50_ADT O	BT51_A DTO	BT52_A DTO	BT53_A DTO	BT54_A DTO	BT55_A DTO
		RESSEL (8-15)	BT56_ADT O	BT57_ADT O	BT58_ADT O	BT59_A DTO	BT60_A DTO	BT61_A DTO	BT62_A DTO	BT63_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN751 (0x05DE)	ADC1_HW TRG10	RESSEL (0-7)	PORT_PIN(ADTG0)	RLT16_UF SET	RLT17_UF SET	OUT0	OUT1	bt_adto_110_a	bt_adto_110_b	bt_adto_110_c
		RESSEL (8-15)	bt_adto_110_d	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN752 (0x05E0)	bt_adto_11 0_a	RESSEL (0-7)	BT0_ADT O	BT1_ADT O	BT2_ADT O	BT3_AD TO	BT4_AD TO	BT5_AD TO	BT6_AD TO	BT7_AD TO
		RESSEL (8-15)	BT8_ADT O	BT9_ADT O	BT10_ADT O	BT11_A DTO	BT12_A DTO	BT13_A DTO	BT14_A DTO	BT15_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN753 (0x05E2)	bt_adto_11 0_b	RESSEL (0-7)	BT16_ADT O	BT17_ADT O	BT18_ADT O	BT19_A DTO	BT20_A DTO	BT21_A DTO	BT22_A DTO	BT23_A DTO
		RESSEL (8-15)	BT24_ADT O	BT25_ADT O	BT26_ADT O	BT27_A DTO	BT28_A DTO	BT29_A DTO	BT30_A DTO	BT31_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN754 (0x05E4)	bt_adto_11 0_c	RESSEL (0-7)	BT32_ADT O	BT33_ADT O	BT34_ADT O	BT35_A DTO	BT36_A DTO	BT37_A DTO	BT38_A DTO	BT39_A DTO
		RESSEL (8-15)	BT40_ADT O	BT41_ADT O	BT42_ADT O	BT43_A DTO	BT44_A DTO	BT45_A DTO	BT46_A DTO	BT47_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN755 (0x05E6)	bt_adto_11 0_d	RESSEL (0-7)	BT48_ADT O	BT49_ADT O	BT50_ADT O	BT51_A DTO	BT52_A DTO	BT53_A DTO	BT54_A DTO	BT55_A DTO
		RESSEL (8-15)	BT56_ADT O	BT57_ADT O	BT58_ADT O	BT59_A DTO	BT60_A DTO	BT61_A DTO	BT62_A DTO	BT63_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN756 (0x05E8)	ADC1_HW TRG11	RESSEL (0-7)	PORT_PI N(ADTG0)	RLT17_UF SET	RLT0_UFS ET	OUT1	OUT2	bt_adto_ 111_a	bt_adto_ 111_b	bt_adto_ 111_c
		RESSEL (8-15)	bt_adto_11 1_d	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN757 (0x05EA)	bt_adto_11 1_a	RESSEL (0-7)	BT0_ADT O	BT1_ADT O	BT2_ADT O	BT3_AD TO	BT4_AD TO	BT5_AD TO	BT6_AD TO	BT7_AD TO
		RESSEL (8-15)	BT8_ADT O	BT9_ADT O	BT10_ADT O	BT11_A DTO	BT12_A DTO	BT13_A DTO	BT14_A DTO	BT15_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN758 (0x05EC)	bt_adto_11 1_b	RESSEL (0-7)	BT16_ADT O	BT17_ADT O	BT18_ADT O	BT19_A DTO	BT20_A DTO	BT21_A DTO	BT22_A DTO	BT23_A DTO
		RESSEL (8-15)	BT24_ADT O	BT25_ADT O	BT26_ADT O	BT27_A DTO	BT28_A DTO	BT29_A DTO	BT30_A DTO	BT31_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN759 (0x05EE)	bt_adto_11 1_c	RESSEL (0-7)	BT32_ADT O	BT33_ADT O	BT34_ADT O	BT35_A DTO	BT36_A DTO	BT37_A DTO	BT38_A DTO	BT39_A DTO
		RESSEL (8-15)	BT40_ADT O	BT41_ADT O	BT42_ADT O	BT43_A DTO	BT44_A DTO	BT45_A DTO	BT46_A DTO	BT47_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL L[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN760 (0x05F0)	bt_adto_11 1_d	RESSEL (0-7)	BT48_ADT O	BT49_ADT O	BT50_ADT O	BT51_A DTO	BT52_A DTO	BT53_A DTO	BT54_A DTO	BT55_A DTO
		RESSEL (8-15)	BT56_ADT O	BT57_ADT O	BT58_ADT O	BT59_A DTO	BT60_A DTO	BT61_A DTO	BT62_A DTO	BT63_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN761 (0x05F2)	ADC1_HW TRG12	RESSEL (0-7)	PORT_PIN(ADTG0)	RLT0_UFS ET	RLT1_UFS ET	OUT2	OUT3	bt_adto_112_a	bt_adto_112_b	bt_adto_112_c
		RESSEL (8-15)	bt_adto_112_d	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN762 (0x05F4)	bt_adto_11 2_a	RESSEL (0-7)	BT0_ADT O	BT1_ADT O	BT2_ADT O	BT3_AD TO	BT4_AD TO	BT5_AD TO	BT6_AD TO	BT7_AD TO
		RESSEL (8-15)	BT8_ADT O	BT9_ADT O	BT10_ADT O	BT11_A DTO	BT12_A DTO	BT13_A DTO	BT14_A DTO	BT15_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN763 (0x05F6)	bt_adto_11 2_b	RESSEL (0-7)	BT16_ADT O	BT17_ADT O	BT18_ADT O	BT19_A DTO	BT20_A DTO	BT21_A DTO	BT22_A DTO	BT23_A DTO
		RESSEL (8-15)	BT24_ADT O	BT25_ADT O	BT26_ADT O	BT27_A DTO	BT28_A DTO	BT29_A DTO	BT30_A DTO	BT31_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN764 (0x05F8)	bt_adto_11 2_c	RESSEL (0-7)	BT32_ADT O	BT33_ADT O	BT34_ADT O	BT35_A DTO	BT36_A DTO	BT37_A DTO	BT38_A DTO	BT39_A DTO
		RESSEL (8-15)	BT40_ADT O	BT41_ADT O	BT42_ADT O	BT43_A DTO	BT44_A DTO	BT45_A DTO	BT46_A DTO	BT47_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN765 (0x05FA)	bt_adto_11 2_d	RESSEL (0-7)	BT48_ADT O	BT49_ADT O	BT50_ADT O	BT51_A DTO	BT52_A DTO	BT53_A DTO	BT54_A DTO	BT55_A DTO
		RESSEL (8-15)	BT56_ADT O	BT57_ADT O	BT58_ADT O	BT59_A DTO	BT60_A DTO	BT61_A DTO	BT62_A DTO	BT63_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN766 (0x05FC)	ADC1_HW TRG13	RESSEL (0-7)	PORT_P N(ADTG0)	RLT1_UFS ET	RLT2_UFS ET	OUT3	OUT4	bt_adto_ 113_a	bt_adto_ 113_b	bt_adto_ 113_c
		RESSEL (8-15)	bt_adto_11 3_d	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN767 (0x05FE)	bt_adto_11 3_a	RESSEL (0-7)	BT0_ADT O	BT1_ADT O	BT2_ADT O	BT3_AD TO	BT4_AD TO	BT5_AD TO	BT6_AD TO	BT7_AD TO
		RESSEL (8-15)	BT8_ADT O	BT9_ADT O	BT10_ADT O	BT11_A DTO	BT12_A DTO	BT13_A DTO	BT14_A DTO	BT15_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN768 (0x0600)	bt_adto_11 3_b	RESSEL (0-7)	BT16_ADT O	BT17_ADT O	BT18_ADT O	BT19_A DTO	BT20_A DTO	BT21_A DTO	BT22_A DTO	BT23_A DTO
		RESSEL (8-15)	BT24_ADT O	BT25_ADT O	BT26_ADT O	BT27_A DTO	BT28_A DTO	BT29_A DTO	BT30_A DTO	BT31_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN769 (0x0602)	bt_adto_11 3_c	RESSEL (0-7)	BT32_ADT O	BT33_ADT O	BT34_ADT O	BT35_A DTO	BT36_A DTO	BT37_A DTO	BT38_A DTO	BT39_A DTO
		RESSEL (8-15)	BT40_ADT O	BT41_ADT O	BT42_ADT O	BT43_A DTO	BT44_A DTO	BT45_A DTO	BT46_A DTO	BT47_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL L[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN770 (0x0604)	bt_adto_11 3_d	RESSEL (0-7)	BT48_ADT O	BT49_ADT O	BT50_ADT O	BT51_A DTO	BT52_A DTO	BT53_A DTO	BT54_A DTO	BT55_A DTO
		RESSEL (8-15)	BT56_ADT O	BT57_ADT O	BT58_ADT O	BT59_A DTO	BT60_A DTO	BT61_A DTO	BT62_A DTO	BT63_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN771 (0x0606)	ADC1_HW TRG14	RESSEL (0-7)	PORT_PIN(ADTG0)	RLT2_UFS ET	RLT3_UFS ET	OUT4	OUT5	bt_adto_114_a	bt_adto_114_b	bt_adto_114_c
		RESSEL (8-15)	bt_adto_114_d	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN772 (0x0608)	bt_adto_11 4_a	RESSEL (0-7)	BT0_ADT O	BT1_ADT O	BT2_ADT O	BT3_AD TO	BT4_AD TO	BT5_AD TO	BT6_AD TO	BT7_AD TO
		RESSEL (8-15)	BT8_ADT O	BT9_ADT O	BT10_ADT O	BT11_A DTO	BT12_A DTO	BT13_A DTO	BT14_A DTO	BT15_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN773 (0x060A)	bt_adto_11 4_b	RESSEL (0-7)	BT16_ADT O	BT17_ADT O	BT18_ADT O	BT19_A DTO	BT20_A DTO	BT21_A DTO	BT22_A DTO	BT23_A DTO
		RESSEL (8-15)	BT24_ADT O	BT25_ADT O	BT26_ADT O	BT27_A DTO	BT28_A DTO	BT29_A DTO	BT30_A DTO	BT31_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN774 (0x060C)	bt_adto_11 4_c	RESSEL (0-7)	BT32_ADT O	BT33_ADT O	BT34_ADT O	BT35_A DTO	BT36_A DTO	BT37_A DTO	BT38_A DTO	BT39_A DTO
		RESSEL (8-15)	BT40_ADT O	BT41_ADT O	BT42_ADT O	BT43_A DTO	BT44_A DTO	BT45_A DTO	BT46_A DTO	BT47_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN775 (0x060E)	bt_adto_11 4_d	RESSEL (0-7)	BT48_ADT O	BT49_ADT O	BT50_ADT O	BT51_A DTO	BT52_A DTO	BT53_A DTO	BT54_A DTO	BT55_A DTO
		RESSEL (8-15)	BT56_ADT O	BT57_ADT O	BT58_ADT O	BT59_A DTO	BT60_A DTO	BT61_A DTO	BT62_A DTO	BT63_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN776 (0x0610)	ADC1_HW TRG15	RESSEL (0-7)	PORT_P N(ADTG0)	RLT3_UFS ET	RLT16_UF SET	OUT5	OUT0	bt_adto_ 115_a	bt_adto_ 115_b	bt_adto_ 115_c
		RESSEL (8-15)	bt_adto_11 5_d	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN777 (0x0612)	bt_adto_11 5_a	RESSEL (0-7)	BT0_ADT O	BT1_ADT O	BT2_ADT O	BT3_AD TO	BT4_AD TO	BT5_AD TO	BT6_AD TO	BT7_AD TO
		RESSEL (8-15)	BT8_ADT O	BT9_ADT O	BT10_ADT O	BT11_A DTO	BT12_A DTO	BT13_A DTO	BT14_A DTO	BT15_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN778 (0x0614)	bt_adto_11 5_b	RESSEL (0-7)	BT16_ADT O	BT17_ADT O	BT18_ADT O	BT19_A DTO	BT20_A DTO	BT21_A DTO	BT22_A DTO	BT23_A DTO
		RESSEL (8-15)	BT24_ADT O	BT25_ADT O	BT26_ADT O	BT27_A DTO	BT28_A DTO	BT29_A DTO	BT30_A DTO	BT31_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN779 (0x0616)	bt_adto_11 5_c	RESSEL (0-7)	BT32_ADT O	BT33_ADT O	BT34_ADT O	BT35_A DTO	BT36_A DTO	BT37_A DTO	BT38_A DTO	BT39_A DTO
		RESSEL (8-15)	BT40_ADT O	BT41_ADT O	BT42_ADT O	BT43_A DTO	BT44_A DTO	BT45_A DTO	BT46_A DTO	BT47_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN780 (0x0618)	bt_adto_11 5_d	RESSEL (0-7)	BT48_ADT O	BT49_ADT O	BT50_ADT O	BT51_A DTO	BT52_A DTO	BT53_A DTO	BT54_A DTO	BT55_A DTO
		RESSEL (8-15)	BT56_ADT O	BT57_ADT O	BT58_ADT O	BT59_A DTO	BT60_A DTO	BT61_A DTO	BT62_A DTO	BT63_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN781 (0x061A)	ADC1_HW TRG16	RESSEL (0-7)	PORT_PIN(ADTG0)	RLT16_UF SET	RLT17_UF SET	OUT0	OUT1	bt_adto_116_a	bt_adto_116_b	bt_adto_116_c
		RESSEL (8-15)	bt_adto_116_d	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN782 (0x061C)	bt_adto_11 6_a	RESSEL (0-7)	BT0_ADT O	BT1_ADT O	BT2_ADT O	BT3_AD TO	BT4_AD TO	BT5_AD TO	BT6_AD TO	BT7_AD TO
		RESSEL (8-15)	BT8_ADT O	BT9_ADT O	BT10_ADT O	BT11_A DTO	BT12_A DTO	BT13_A DTO	BT14_A DTO	BT15_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN783 (0x061E)	bt_adto_11 6_b	RESSEL (0-7)	BT16_ADT O	BT17_ADT O	BT18_ADT O	BT19_A DTO	BT20_A DTO	BT21_A DTO	BT22_A DTO	BT23_A DTO
		RESSEL (8-15)	BT24_ADT O	BT25_ADT O	BT26_ADT O	BT27_A DTO	BT28_A DTO	BT29_A DTO	BT30_A DTO	BT31_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN784 (0x0620)	bt_adto_11 6_c	RESSEL (0-7)	BT32_ADT O	BT33_ADT O	BT34_ADT O	BT35_A DTO	BT36_A DTO	BT37_A DTO	BT38_A DTO	BT39_A DTO
		RESSEL (8-15)	BT40_ADT O	BT41_ADT O	BT42_ADT O	BT43_A DTO	BT44_A DTO	BT45_A DTO	BT46_A DTO	BT47_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN785 (0x0622)	bt_adto_11 6_d	RESSEL (0-7)	BT48_ADT O	BT49_ADT O	BT50_ADT O	BT51_A DTO	BT52_A DTO	BT53_A DTO	BT54_A DTO	BT55_A DTO
		RESSEL (8-15)	BT56_ADT O	BT57_ADT O	BT58_ADT O	BT59_A DTO	BT60_A DTO	BT61_A DTO	BT62_A DTO	BT63_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN786 (0x0624)	ADC1_HW TRG17	RESSEL (0-7)	PORT_P N(ADTG0)	RLT17_UF SET	RLT0_UFS ET	OUT1	OUT16	bt_adto_ 117_a	bt_adto_ 117_b	bt_adto_ 117_c
		RESSEL (8-15)	bt_adto_11 7_d	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN787 (0x0626)	bt_adto_11 7_a	RESSEL (0-7)	BT0_ADT O	BT1_ADT O	BT2_ADT O	BT3_AD TO	BT4_AD TO	BT5_AD TO	BT6_AD TO	BT7_AD TO
		RESSEL (8-15)	BT8_ADT O	BT9_ADT O	BT10_ADT O	BT11_A DTO	BT12_A DTO	BT13_A DTO	BT14_A DTO	BT15_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN788 (0x0628)	bt_adto_11 7_b	RESSEL (0-7)	BT16_ADT O	BT17_ADT O	BT18_ADT O	BT19_A DTO	BT20_A DTO	BT21_A DTO	BT22_A DTO	BT23_A DTO
		RESSEL (8-15)	BT24_ADT O	BT25_ADT O	BT26_ADT O	BT27_A DTO	BT28_A DTO	BT29_A DTO	BT30_A DTO	BT31_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN789 (0x062A)	bt_adto_11 7_c	RESSEL (0-7)	BT32_ADT O	BT33_ADT O	BT34_ADT O	BT35_A DTO	BT36_A DTO	BT37_A DTO	BT38_A DTO	BT39_A DTO
		RESSEL (8-15)	BT40_ADT O	BT41_ADT O	BT42_ADT O	BT43_A DTO	BT44_A DTO	BT45_A DTO	BT46_A DTO	BT47_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL L[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN790 (0x062C)	bt_adto_11 7_d	RESSEL (0-7)	BT48_ADT O	BT49_ADT O	BT50_ADT O	BT51_A DTO	BT52_A DTO	BT53_A DTO	BT54_A DTO	BT55_A DTO
		RESSEL (8-15)	BT56_ADT O	BT57_ADT O	BT58_ADT O	BT59_A DTO	BT60_A DTO	BT61_A DTO	BT62_A DTO	BT63_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN791 (0x062E)	ADC1_HW TRG18	RESSEL (0-7)	PORT_PIN(ADTG0)	RLT0_UFS ET	RLT1_UFS ET	OUT16	OUT17	bt_adto_118_a	bt_adto_118_b	bt_adto_118_c
		RESSEL (8-15)	bt_adto_118_d	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN792 (0x0630)	bt_adto_11 8_a	RESSEL (0-7)	BT0_ADT O	BT1_ADT O	BT2_ADT O	BT3_AD TO	BT4_AD TO	BT5_AD TO	BT6_AD TO	BT7_AD TO
		RESSEL (8-15)	BT8_ADT O	BT9_ADT O	BT10_ADT O	BT11_A DTO	BT12_A DTO	BT13_A DTO	BT14_A DTO	BT15_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN793 (0x0632)	bt_adto_11 8_b	RESSEL (0-7)	BT16_ADT O	BT17_ADT O	BT18_ADT O	BT19_A DTO	BT20_A DTO	BT21_A DTO	BT22_A DTO	BT23_A DTO
		RESSEL (8-15)	BT24_ADT O	BT25_ADT O	BT26_ADT O	BT27_A DTO	BT28_A DTO	BT29_A DTO	BT30_A DTO	BT31_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN794 (0x0634)	bt_adto_11 8_c	RESSEL (0-7)	BT32_ADT O	BT33_ADT O	BT34_ADT O	BT35_A DTO	BT36_A DTO	BT37_A DTO	BT38_A DTO	BT39_A DTO
		RESSEL (8-15)	BT40_ADT O	BT41_ADT O	BT42_ADT O	BT43_A DTO	BT44_A DTO	BT45_A DTO	BT46_A DTO	BT47_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN795 (0x0636)	bt_adto_11 8_d	RESSEL (0-7)	BT48_ADT O	BT49_ADT O	BT50_ADT O	BT51_A DTO	BT52_A DTO	BT53_A DTO	BT54_A DTO	BT55_A DTO
		RESSEL (8-15)	BT56_ADT O	BT57_ADT O	BT58_ADT O	BT59_A DTO	BT60_A DTO	BT61_A DTO	BT62_A DTO	BT63_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN796 (0x0638)	ADC1_HW TRG19	RESSEL (0-7)	PORT_PI N(ADTG0)	RLT1_UFS ET	RLT2_UFS ET	OUT17	OUT18	bt_adto_ 119_a	bt_adto_ 119_b	bt_adto_ 119_c
		RESSEL (8-15)	bt_adto_11 9_d	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN797 (0x063A)	bt_adto_11 9_a	RESSEL (0-7)	BT0_ADT O	BT1_ADT O	BT2_ADT O	BT3_AD TO	BT4_AD TO	BT5_AD TO	BT6_AD TO	BT7_AD TO
		RESSEL (8-15)	BT8_ADT O	BT9_ADT O	BT10_ADT O	BT11_A DTO	BT12_A DTO	BT13_A DTO	BT14_A DTO	BT15_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN798 (0x063C)	bt_adto_11 9_b	RESSEL (0-7)	BT16_ADT O	BT17_ADT O	BT18_ADT O	BT19_A DTO	BT20_A DTO	BT21_A DTO	BT22_A DTO	BT23_A DTO
		RESSEL (8-15)	BT24_ADT O	BT25_ADT O	BT26_ADT O	BT27_A DTO	BT28_A DTO	BT29_A DTO	BT30_A DTO	BT31_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN799 (0x063E)	bt_adto_11 9_c	RESSEL (0-7)	BT32_ADT O	BT33_ADT O	BT34_ADT O	BT35_A DTO	BT36_A DTO	BT37_A DTO	BT38_A DTO	BT39_A DTO
		RESSEL (8-15)	BT40_ADT O	BT41_ADT O	BT42_ADT O	BT43_A DTO	BT44_A DTO	BT45_A DTO	BT46_A DTO	BT47_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL L[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN800 (0x0640)	bt_adto_11 9_d	RESSEL (0-7)	BT48_ADT O	BT49_ADT O	BT50_ADT O	BT51_A DTO	BT52_A DTO	BT53_A DTO	BT54_A DTO	BT55_A DTO
		RESSEL (8-15)	BT56_ADT O	BT57_ADT O	BT58_ADT O	BT59_A DTO	BT60_A DTO	BT61_A DTO	BT62_A DTO	BT63_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN801 (0x0642)	ADC1_HW TRG20	RESSEL (0-7)	PORT_PIN(ADTG0)	RLT2_UFS ET	RLT3_UFS ET	OUT18	OUT19	bt_adto_120_a	bt_adto_120_b	bt_adto_120_c
		RESSEL (8-15)	bt_adto_120_d	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN802 (0x0644)	bt_adto_1 20_a	RESSEL (0-7)	BT0_ADT O	BT1_ADT O	BT2_ADT O	BT3_AD TO	BT4_AD TO	BT5_AD TO	BT6_AD TO	BT7_AD TO
		RESSEL (8-15)	BT8_ADT O	BT9_ADT O	BT10_ADT O	BT11_A DTO	BT12_A DTO	BT13_A DTO	BT14_A DTO	BT15_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN803 (0x0646)	bt_adto_1 20_b	RESSEL (0-7)	BT16_ADT O	BT17_ADT O	BT18_ADT O	BT19_A DTO	BT20_A DTO	BT21_A DTO	BT22_A DTO	BT23_A DTO
		RESSEL (8-15)	BT24_ADT O	BT25_ADT O	BT26_ADT O	BT27_A DTO	BT28_A DTO	BT29_A DTO	BT30_A DTO	BT31_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN804 (0x0648)	bt_adto_1 20_c	RESSEL (0-7)	BT32_ADT O	BT33_ADT O	BT34_ADT O	BT35_A DTO	BT36_A DTO	BT37_A DTO	BT38_A DTO	BT39_A DTO
		RESSEL (8-15)	BT40_ADT O	BT41_ADT O	BT42_ADT O	BT43_A DTO	BT44_A DTO	BT45_A DTO	BT46_A DTO	BT47_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN805 (0x064A)	bt_adto_1 20_d	RESSEL (0-7)	BT48_ADT O	BT49_ADT O	BT50_ADT O	BT51_A DTO	BT52_A DTO	BT53_A DTO	BT54_A DTO	BT55_A DTO
		RESSEL (8-15)	BT56_ADT O	BT57_ADT O	BT58_ADT O	BT59_A DTO	BT60_A DTO	BT61_A DTO	BT62_A DTO	BT63_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN806 (0x064C)	ADC1_HW TRG21	RESSEL (0-7)	PORT_P N(ADTG0)	RLT3_UFS ET	RLT16_UF SET	OUT19	OUT20	bt_adto_ 121_a	bt_adto_ 121_b	bt_adto_ 121_c
		RESSEL (8-15)	bt_adto_1 21_d	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN807 (0x064E)	bt_adto_1 21_a	RESSEL (0-7)	BT0_ADT O	BT1_ADT O	BT2_ADT O	BT3_AD TO	BT4_AD TO	BT5_AD TO	BT6_AD TO	BT7_AD TO
		RESSEL (8-15)	BT8_ADT O	BT9_ADT O	BT10_ADT O	BT11_A DTO	BT12_A DTO	BT13_A DTO	BT14_A DTO	BT15_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN808 (0x0650)	bt_adto_1 21_b	RESSEL (0-7)	BT16_ADT O	BT17_ADT O	BT18_ADT O	BT19_A DTO	BT20_A DTO	BT21_A DTO	BT22_A DTO	BT23_A DTO
		RESSEL (8-15)	BT24_ADT O	BT25_ADT O	BT26_ADT O	BT27_A DTO	BT28_A DTO	BT29_A DTO	BT30_A DTO	BT31_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN809 (0x0652)	bt_adto_1 21_c	RESSEL (0-7)	BT32_ADT O	BT33_ADT O	BT34_ADT O	BT35_A DTO	BT36_A DTO	BT37_A DTO	BT38_A DTO	BT39_A DTO
		RESSEL (8-15)	BT40_ADT O	BT41_ADT O	BT42_ADT O	BT43_A DTO	BT44_A DTO	BT45_A DTO	BT46_A DTO	BT47_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL L[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN810 (0x0654)	bt_adto_1 21_d	RESSEL (0-7)	BT48_ADT O	BT49_ADT O	BT50_ADT O	BT51_A DTO	BT52_A DTO	BT53_A DTO	BT54_A DTO	BT55_A DTO
		RESSEL (8-15)	BT56_ADT O	BT57_ADT O	BT58_ADT O	BT59_A DTO	BT60_A DTO	BT61_A DTO	BT62_A DTO	BT63_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN811 (0x0656)	ADC1_HW TRG22	RESSEL (0-7)	PORT_PIN(ADTG0)	RLT16_UF SET	RLT17_UF SET	OUT20	OUT21	bt_adto_122_a	bt_adto_122_b	bt_adto_122_c
		RESSEL (8-15)	bt_adto_122_d	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN812 (0x0658)	bt_adto_1 22_a	RESSEL (0-7)	BT0_ADT O	BT1_ADT O	BT2_ADT O	BT3_AD TO	BT4_AD TO	BT5_AD TO	BT6_AD TO	BT7_AD TO
		RESSEL (8-15)	BT8_ADT O	BT9_ADT O	BT10_ADT O	BT11_A DTO	BT12_A DTO	BT13_A DTO	BT14_A DTO	BT15_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN813 (0x065A)	bt_adto_1 22_b	RESSEL (0-7)	BT16_ADT O	BT17_ADT O	BT18_ADT O	BT19_A DTO	BT20_A DTO	BT21_A DTO	BT22_A DTO	BT23_A DTO
		RESSEL (8-15)	BT24_ADT O	BT25_ADT O	BT26_ADT O	BT27_A DTO	BT28_A DTO	BT29_A DTO	BT30_A DTO	BT31_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN814 (0x065C)	bt_adto_1 22_c	RESSEL (0-7)	BT32_ADT O	BT33_ADT O	BT34_ADT O	BT35_A DTO	BT36_A DTO	BT37_A DTO	BT38_A DTO	BT39_A DTO
		RESSEL (8-15)	BT40_ADT O	BT41_ADT O	BT42_ADT O	BT43_A DTO	BT44_A DTO	BT45_A DTO	BT46_A DTO	BT47_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN815 (0x065E)	bt_adto_1 22_d	RESSEL (0-7)	BT48_ADT O	BT49_ADT O	BT50_ADT O	BT51_A DTO	BT52_A DTO	BT53_A DTO	BT54_A DTO	BT55_A DTO
		RESSEL (8-15)	BT56_ADT O	BT57_ADT O	BT58_ADT O	BT59_A DTO	BT60_A DTO	BT61_A DTO	BT62_A DTO	BT63_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN816 (0x0660)	ADC1_HW TRG23	RESSEL (0-7)	PORT_PIN(ADTG0)	RLT17_UF SET	RLT0_UFS ET	OUT21	OUT0	bt_adto_123_a	bt_adto_123_b	bt_adto_123_c
		RESSEL (8-15)	bt_adto_123_d	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN817 (0x0662)	bt_adto_1 23_a	RESSEL (0-7)	BT0_ADT O	BT1_ADT O	BT2_ADT O	BT3_ADT O	BT4_ADT O	BT5_ADT O	BT6_ADT O	BT7_ADT O
		RESSEL (8-15)	BT8_ADT O	BT9_ADT O	BT10_ADT O	BT11_A DTO	BT12_A DTO	BT13_A DTO	BT14_A DTO	BT15_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN818 (0x0664)	bt_adto_1 23_b	RESSEL (0-7)	BT16_ADT O	BT17_ADT O	BT18_ADT O	BT19_A DTO	BT20_A DTO	BT21_A DTO	BT22_A DTO	BT23_A DTO
		RESSEL (8-15)	BT24_ADT O	BT25_ADT O	BT26_ADT O	BT27_A DTO	BT28_A DTO	BT29_A DTO	BT30_A DTO	BT31_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN819 (0x0666)	bt_adto_1 23_c	RESSEL (0-7)	BT32_ADT O	BT33_ADT O	BT34_ADT O	BT35_A DTO	BT36_A DTO	BT37_A DTO	BT38_A DTO	BT39_A DTO
		RESSEL (8-15)	BT40_ADT O	BT41_ADT O	BT42_ADT O	BT43_A DTO	BT44_A DTO	BT45_A DTO	BT46_A DTO	BT47_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3:0] /PORTSEL[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN820 (0x0668)	bt_adto_1 23_d	RESSEL (0-7)	BT48_ADT O	BT49_ADT O	BT50_ADT O	BT51_A DTO	BT52_A DTO	BT53_A DTO	BT54_A DTO	BT55_A DTO
		RESSEL (8-15)	BT56_ADT O	BT57_ADT O	BT58_ADT O	BT59_A DTO	BT60_A DTO	BT61_A DTO	BT62_A DTO	BT63_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN821 (0x066A)	ADC1_HW TRG24	RESSEL (0-7)	PORT_PIN(ADTG0)	RLT0_UFS ET	RLT1_UFS ET	OUT0	OUT1	bt_adto_124_a	bt_adto_124_b	bt_adto_124_c
		RESSEL (8-15)	bt_adto_124_d	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN822 (0x066C)	bt_adto_1 24_a	RESSEL (0-7)	BT0_ADT O	BT1_ADT O	BT2_ADT O	BT3_AD TO	BT4_AD TO	BT5_AD TO	BT6_AD TO	BT7_AD TO
		RESSEL (8-15)	BT8_ADT O	BT9_ADT O	BT10_ADT O	BT11_A DTO	BT12_A DTO	BT13_A DTO	BT14_A DTO	BT15_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN823 (0x066E)	bt_adto_1 24_b	RESSEL (0-7)	BT16_ADT O	BT17_ADT O	BT18_ADT O	BT19_A DTO	BT20_A DTO	BT21_A DTO	BT22_A DTO	BT23_A DTO
		RESSEL (8-15)	BT24_ADT O	BT25_ADT O	BT26_ADT O	BT27_A DTO	BT28_A DTO	BT29_A DTO	BT30_A DTO	BT31_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN824 (0x0670)	bt_adto_1 24_c	RESSEL (0-7)	BT32_ADT O	BT33_ADT O	BT34_ADT O	BT35_A DTO	BT36_A DTO	BT37_A DTO	BT38_A DTO	BT39_A DTO
		RESSEL (8-15)	BT40_ADT O	BT41_ADT O	BT42_ADT O	BT43_A DTO	BT44_A DTO	BT45_A DTO	BT46_A DTO	BT47_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN825 (0x0672)	bt_adto_1 24_d	RESSEL (0-7)	BT48_ADT O	BT49_ADT O	BT50_ADT O	BT51_A DTO	BT52_A DTO	BT53_A DTO	BT54_A DTO	BT55_A DTO
		RESSEL (8-15)	BT56_ADT O	BT57_ADT O	BT58_ADT O	BT59_A DTO	BT60_A DTO	BT61_A DTO	BT62_A DTO	BT63_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN826 (0x0674)	ADC1_HW TRG25	RESSEL (0-7)	PORT_P N(ADTG0)	RLT1_UFS ET	RLT2_UFS ET	OUT1	OUT2	bt_adto_ 125_a	bt_adto_ 125_b	bt_adto_ 125_c
		RESSEL (8-15)	bt_adto_1 25_d	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN827 (0x0676)	bt_adto_1 25_a	RESSEL (0-7)	BT0_ADT O	BT1_ADT O	BT2_ADT O	BT3_AD TO	BT4_AD TO	BT5_AD TO	BT6_AD TO	BT7_AD TO
		RESSEL (8-15)	BT8_ADT O	BT9_ADT O	BT10_ADT O	BT11_A DTO	BT12_A DTO	BT13_A DTO	BT14_A DTO	BT15_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN828 (0x0678)	bt_adto_1 25_b	RESSEL (0-7)	BT16_ADT O	BT17_ADT O	BT18_ADT O	BT19_A DTO	BT20_A DTO	BT21_A DTO	BT22_A DTO	BT23_A DTO
		RESSEL (8-15)	BT24_ADT O	BT25_ADT O	BT26_ADT O	BT27_A DTO	BT28_A DTO	BT29_A DTO	BT30_A DTO	BT31_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN829 (0x067A)	bt_adto_1 25_c	RESSEL (0-7)	BT32_ADT O	BT33_ADT O	BT34_ADT O	BT35_A DTO	BT36_A DTO	BT37_A DTO	BT38_A DTO	BT39_A DTO
		RESSEL (8-15)	BT40_ADT O	BT41_ADT O	BT42_ADT O	BT43_A DTO	BT44_A DTO	BT45_A DTO	BT46_A DTO	BT47_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN830 (0x067C)	bt_adto_1 25_d	RESSEL (0-7)	BT48_ADT O	BT49_ADT O	BT50_ADT O	BT51_A DTO	BT52_A DTO	BT53_A DTO	BT54_A DTO	BT55_A DTO
		RESSEL (8-15)	BT56_ADT O	BT57_ADT O	BT58_ADT O	BT59_A DTO	BT60_A DTO	BT61_A DTO	BT62_A DTO	BT63_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN831 (0x067E)	ADC1_HW TRG26	RESSEL (0-7)	PORT_PIN(ADTG0)	RLT2_UFS ET	RLT3_UFS ET	OUT2	OUT3	bt_adto_126_a	bt_adto_126_b	bt_adto_126_c
		RESSEL (8-15)	bt_adto_126_d	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN832 (0x0680)	bt_adto_1 26_a	RESSEL (0-7)	BT0_ADT O	BT1_ADT O	BT2_ADT O	BT3_AD TO	BT4_AD TO	BT5_AD TO	BT6_AD TO	BT7_AD TO
		RESSEL (8-15)	BT8_ADT O	BT9_ADT O	BT10_ADT O	BT11_A DTO	BT12_A DTO	BT13_A DTO	BT14_A DTO	BT15_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN833 (0x0682)	bt_adto_1 26_b	RESSEL (0-7)	BT16_ADT O	BT17_ADT O	BT18_ADT O	BT19_A DTO	BT20_A DTO	BT21_A DTO	BT22_A DTO	BT23_A DTO
		RESSEL (8-15)	BT24_ADT O	BT25_ADT O	BT26_ADT O	BT27_A DTO	BT28_A DTO	BT29_A DTO	BT30_A DTO	BT31_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN834 (0x0684)	bt_adto_1 26_c	RESSEL (0-7)	BT32_ADT O	BT33_ADT O	BT34_ADT O	BT35_A DTO	BT36_A DTO	BT37_A DTO	BT38_A DTO	BT39_A DTO
		RESSEL (8-15)	BT40_ADT O	BT41_ADT O	BT42_ADT O	BT43_A DTO	BT44_A DTO	BT45_A DTO	BT46_A DTO	BT47_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN835 (0x0686)	bt_adto_1 26_d	RESSEL (0-7)	BT48_ADT O	BT49_ADT O	BT50_ADT O	BT51_A DTO	BT52_A DTO	BT53_A DTO	BT54_A DTO	BT55_A DTO
		RESSEL (8-15)	BT56_ADT O	BT57_ADT O	BT58_ADT O	BT59_A DTO	BT60_A DTO	BT61_A DTO	BT62_A DTO	BT63_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN836 (0x0688)	ADC1_HW TRG27	RESSEL (0-7)	PORT_P N(ADTG0)	RLT3_UFS ET	RLT16_UF SET	OUT3	OUT4	bt_adto_ 127_a	bt_adto_ 127_b	bt_adto_ 127_c
		RESSEL (8-15)	bt_adto_1 27_d	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN837 (0x068A)	bt_adto_1 27_a	RESSEL (0-7)	BT0_ADT O	BT1_ADT O	BT2_ADT O	BT3_AD TO	BT4_AD TO	BT5_AD TO	BT6_AD TO	BT7_AD TO
		RESSEL (8-15)	BT8_ADT O	BT9_ADT O	BT10_ADT O	BT11_A DTO	BT12_A DTO	BT13_A DTO	BT14_A DTO	BT15_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN838 (0x068C)	bt_adto_1 27_b	RESSEL (0-7)	BT16_ADT O	BT17_ADT O	BT18_ADT O	BT19_A DTO	BT20_A DTO	BT21_A DTO	BT22_A DTO	BT23_A DTO
		RESSEL (8-15)	BT24_ADT O	BT25_ADT O	BT26_ADT O	BT27_A DTO	BT28_A DTO	BT29_A DTO	BT30_A DTO	BT31_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN839 (0x068E)	bt_adto_1 27_c	RESSEL (0-7)	BT32_ADT O	BT33_ADT O	BT34_ADT O	BT35_A DTO	BT36_A DTO	BT37_A DTO	BT38_A DTO	BT39_A DTO
		RESSEL (8-15)	BT40_ADT O	BT41_ADT O	BT42_ADT O	BT43_A DTO	BT44_A DTO	BT45_A DTO	BT46_A DTO	BT47_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL L[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN840 (0x0690)	bt_adto_1 27_d	RESSEL (0-7)	BT48_ADT O	BT49_ADT O	BT50_ADT O	BT51_A DTO	BT52_A DTO	BT53_A DTO	BT54_A DTO	BT55_A DTO
		RESSEL (8-15)	BT56_ADT O	BT57_ADT O	BT58_ADT O	BT59_A DTO	BT60_A DTO	BT61_A DTO	BT62_A DTO	BT63_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN841 (0x0692)	ADC1_HW TRG28	RESSEL (0-7)	PORT_PIN(ADTG0)	RLT16_UF SET	RLT17_UF SET	OUT4	OUT5	bt_adto_128_a	bt_adto_128_b	bt_adto_128_c
		RESSEL (8-15)	bt_adto_128_d	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN842 (0x0694)	bt_adto_1 28_a	RESSEL (0-7)	BT0_ADT O	BT1_ADT O	BT2_ADT O	BT3_AD TO	BT4_AD TO	BT5_AD TO	BT6_AD TO	BT7_AD TO
		RESSEL (8-15)	BT8_ADT O	BT9_ADT O	BT10_ADT O	BT11_A DTO	BT12_A DTO	BT13_A DTO	BT14_A DTO	BT15_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN843 (0x0696)	bt_adto_1 28_b	RESSEL (0-7)	BT16_ADT O	BT17_ADT O	BT18_ADT O	BT19_A DTO	BT20_A DTO	BT21_A DTO	BT22_A DTO	BT23_A DTO
		RESSEL (8-15)	BT24_ADT O	BT25_ADT O	BT26_ADT O	BT27_A DTO	BT28_A DTO	BT29_A DTO	BT30_A DTO	BT31_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN844 (0x0698)	bt_adto_1 28_c	RESSEL (0-7)	BT32_ADT O	BT33_ADT O	BT34_ADT O	BT35_A DTO	BT36_A DTO	BT37_A DTO	BT38_A DTO	BT39_A DTO
		RESSEL (8-15)	BT40_ADT O	BT41_ADT O	BT42_ADT O	BT43_A DTO	BT44_A DTO	BT45_A DTO	BT46_A DTO	BT47_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN845 (0x069A)	bt_adto_1 28_d	RESSEL (0-7)	BT48_ADT O	BT49_ADT O	BT50_ADT O	BT51_A DTO	BT52_A DTO	BT53_A DTO	BT54_A DTO	BT55_A DTO
		RESSEL (8-15)	BT56_ADT O	BT57_ADT O	BT58_ADT O	BT59_A DTO	BT60_A DTO	BT61_A DTO	BT62_A DTO	BT63_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN846 (0x069C)	ADC1_HW TRG29	RESSEL (0-7)	PORT_PIN(ADTG0)	RLT17_UF SET	RLT0_UFS ET	OUT5	OUT0	bt_adto_129_a	bt_adto_129_b	bt_adto_129_c
		RESSEL (8-15)	bt_adto_129_d	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN847 (0x069E)	bt_adto_1 29_a	RESSEL (0-7)	BT0_ADT O	BT1_ADT O	BT2_ADT O	BT3_ADT O	BT4_ADT O	BT5_ADT O	BT6_ADT O	BT7_ADT O
		RESSEL (8-15)	BT8_ADT O	BT9_ADT O	BT10_ADT O	BT11_A DTO	BT12_A DTO	BT13_A DTO	BT14_A DTO	BT15_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN848 (0x06A0)	bt_adto_1 29_b	RESSEL (0-7)	BT16_ADT O	BT17_ADT O	BT18_ADT O	BT19_A DTO	BT20_A DTO	BT21_A DTO	BT22_A DTO	BT23_A DTO
		RESSEL (8-15)	BT24_ADT O	BT25_ADT O	BT26_ADT O	BT27_A DTO	BT28_A DTO	BT29_A DTO	BT30_A DTO	BT31_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN849 (0x06A2)	bt_adto_1 29_c	RESSEL (0-7)	BT32_ADT O	BT33_ADT O	BT34_ADT O	BT35_A DTO	BT36_A DTO	BT37_A DTO	BT38_A DTO	BT39_A DTO
		RESSEL (8-15)	BT40_ADT O	BT41_ADT O	BT42_ADT O	BT43_A DTO	BT44_A DTO	BT45_A DTO	BT46_A DTO	BT47_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3:0] /PORTSEL[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN850 (0x06A4)	bt_adto_1 29_d	RESSEL (0-7)	BT48_ADT O	BT49_ADT O	BT50_ADT O	BT51_A DTO	BT52_A DTO	BT53_A DTO	BT54_A DTO	BT55_A DTO
		RESSEL (8-15)	BT56_ADT O	BT57_ADT O	BT58_ADT O	BT59_A DTO	BT60_A DTO	BT61_A DTO	BT62_A DTO	BT63_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN851 (0x06A6)	ADC1_HW TRG30	RESSEL (0-7)	PORT_PIN(ADTG0)	RLT0_UFS ET	RLT1_UFS ET	OUT0	OUT1	bt_adto_130_a	bt_adto_130_b	bt_adto_130_c
		RESSEL (8-15)	bt_adto_130_d	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN852 (0x06A8)	bt_adto_1 30_a	RESSEL (0-7)	BT0_ADT O	BT1_ADT O	BT2_ADT O	BT3_AD TO	BT4_AD TO	BT5_AD TO	BT6_AD TO	BT7_AD TO
		RESSEL (8-15)	BT8_ADT O	BT9_ADT O	BT10_ADT O	BT11_A DTO	BT12_A DTO	BT13_A DTO	BT14_A DTO	BT15_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN853 (0x06AA)	bt_adto_1 30_b	RESSEL (0-7)	BT16_ADT O	BT17_ADT O	BT18_ADT O	BT19_A DTO	BT20_A DTO	BT21_A DTO	BT22_A DTO	BT23_A DTO
		RESSEL (8-15)	BT24_ADT O	BT25_ADT O	BT26_ADT O	BT27_A DTO	BT28_A DTO	BT29_A DTO	BT30_A DTO	BT31_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN854 (0x06AC)	bt_adto_1 30_c	RESSEL (0-7)	BT32_ADT O	BT33_ADT O	BT34_ADT O	BT35_A DTO	BT36_A DTO	BT37_A DTO	BT38_A DTO	BT39_A DTO
		RESSEL (8-15)	BT40_ADT O	BT41_ADT O	BT42_ADT O	BT43_A DTO	BT44_A DTO	BT45_A DTO	BT46_A DTO	BT47_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN855 (0x06AE)	bt_adto_1 30_d	RESSEL (0-7)	BT48_ADT O	BT49_ADT O	BT50_ADT O	BT51_A DTO	BT52_A DTO	BT53_A DTO	BT54_A DTO	BT55_A DTO
		RESSEL (8-15)	BT56_ADT O	BT57_ADT O	BT58_ADT O	BT59_A DTO	BT60_A DTO	BT61_A DTO	BT62_A DTO	BT63_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN856 (0x06B0)	ADC1_HW TRG31	RESSEL (0-7)	PORT_P N(ADTG0)	RLT1_UFS ET	RLT2_UFS ET	OUT1	OUT16	bt_adto_ 131_a	bt_adto_ 131_b	bt_adto_ 131_c
		RESSEL (8-15)	bt_adto_1 31_d	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN857 (0x06B2)	bt_adto_1 31_a	RESSEL (0-7)	BT0_ADT O	BT1_ADT O	BT2_ADT O	BT3_AD TO	BT4_AD TO	BT5_AD TO	BT6_AD TO	BT7_AD TO
		RESSEL (8-15)	BT8_ADT O	BT9_ADT O	BT10_ADT O	BT11_A DTO	BT12_A DTO	BT13_A DTO	BT14_A DTO	BT15_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN858 (0x06B4)	bt_adto_1 31_b	RESSEL (0-7)	BT16_ADT O	BT17_ADT O	BT18_ADT O	BT19_A DTO	BT20_A DTO	BT21_A DTO	BT22_A DTO	BT23_A DTO
		RESSEL (8-15)	BT24_ADT O	BT25_ADT O	BT26_ADT O	BT27_A DTO	BT28_A DTO	BT29_A DTO	BT30_A DTO	BT31_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN859 (0x06B6)	bt_adto_1 31_c	RESSEL (0-7)	BT32_ADT O	BT33_ADT O	BT34_ADT O	BT35_A DTO	BT36_A DTO	BT37_A DTO	BT38_A DTO	BT39_A DTO
		RESSEL (8-15)	BT40_ADT O	BT41_ADT O	BT42_ADT O	BT43_A DTO	BT44_A DTO	BT45_A DTO	BT46_A DTO	BT47_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL L[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN860 (0x06B8)	bt_adto_1 31_d	RESSEL (0-7)	BT48_ADT O	BT49_ADT O	BT50_ADT O	BT51_A DTO	BT52_A DTO	BT53_A DTO	BT54_A DTO	BT55_A DTO
		RESSEL (8-15)	BT56_ADT O	BT57_ADT O	BT58_ADT O	BT59_A DTO	BT60_A DTO	BT61_A DTO	BT62_A DTO	BT63_A DTO
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN861 (0x06BA)	DMA[10]	RESSEL (0-7)	Ext_IRQ_0	Ext_IRQ_8	Ext_IRQ_1 6	Ext_IRQ _24	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN862 (0x06BC)	DMA[11]	RESSEL (0-7)	Ext_IRQ_1	Ext_IRQ_9	Ext_IRQ_1 7	Ext_IRQ _25	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN863 (0x06BE)	DMA[12]	RESSEL (0-7)	Ext_IRQ_2	Ext_IRQ_1 0	Ext_IRQ_1 8	Ext_IRQ _26	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN864 (0x06C0)	DMA[13]	RESSEL (0-7)	Ext_IRQ_3	Ext_IRQ_1 1	Ext_IRQ_1 9	Ext_IRQ _27	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL L[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN865 (0x06C2)	DMA[14]	RESSEL (0-7)	Ext_IRQ_4	Ext_IRQ_1 2	Ext_IRQ_2 0	Ext_IRQ _28	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN866 (0x06C4)	DMA[15]	RESSEL (0-7)	Ext_IRQ_5	Ext_IRQ_1 3	Ext_IRQ_2 1	Ext_IRQ _29	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN867 (0x06C6)	DMA[16]	RESSEL (0-7)	Ext_IRQ_6	Ext_IRQ_1 4	Ext_IRQ_2 2	Ext_IRQ _30	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN868 (0x06C8)	DMA[17]	RESSEL (0-7)	Ext_IRQ_7	Ext_IRQ_1 5	Ext_IRQ_2 3	Ext_IRQ _31	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN869 (0x06CA)	DMA[56]	RESSEL (0-7)	BT0_IRQ- 0	BT0_IRQ- 1	BT24_IRQ -0	BT24_IR Q-1	BT48_IR Q-0	BT48_IR Q-1	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL L[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN870 (0x06CC)	DMA[57]	RESSEL (0-7)	BT1_IRQ- 0	BT1_IRQ- 1	BT25_IRQ -0	BT25_IR Q-1	BT49_IR Q-0	BT49_IR Q-1	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN871 (0x06CE)	DMA[58]	RESSEL (0-7)	BT2_IRQ- 0	BT2_IRQ- 1	BT26_IRQ -0	BT26_IR Q-1	BT50_IR Q-0	BT50_IR Q-1	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN872 (0x06D0)	DMA[59]	RESSEL (0-7)	BT3_IRQ- 0	BT3_IRQ- 1	BT27_IRQ -0	BT27_IR Q-1	BT51_IR Q-0	BT51_IR Q-1	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN873 (0x06D2)	DMA[60]	RESSEL (0-7)	BT4_IRQ- 0	BT4_IRQ- 1	BT28_IRQ -0	BT28_IR Q-1	BT52_IR Q-0	BT52_IR Q-1	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN874 (0x06D4)	DMA[61]	RESSEL (0-7)	BT5_IRQ- 0	BT5_IRQ- 1	BT29_IRQ -0	BT29_IR Q-1	BT53_IR Q-0	BT53_IR Q-1	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL L[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN875 (0x06D6)	DMA[62]	RESSEL (0-7)	BT6_IRQ- 0	BT6_IRQ- 1	BT30_IRQ -0	BT30_IR Q-1	BT54_IR Q-0	BT54_IR Q-1	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN876 (0x06D8)	DMA[63]	RESSEL (0-7)	BT7_IRQ- 0	BT7_IRQ- 1	BT31_IRQ -0	BT31_IR Q-1	BT55_IR Q-0	BT55_IR Q-1	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN877 (0x06DA)	DMA[64]	RESSEL (0-7)	BT8_IRQ- 0	BT8_IRQ- 1	BT32_IRQ -0	BT32_IR Q-1	BT56_IR Q-0	BT56_IR Q-1	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN878 (0x06DC)	DMA[65]	RESSEL (0-7)	BT9_IRQ- 0	BT9_IRQ- 1	BT33_IRQ -0	BT33_IR Q-1	BT57_IR Q-0	BT57_IR Q-1	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN879 (0x06DE)	DMA[66]	RESSEL (0-7)	BT10_IRQ -0	BT10_IRQ -1	BT34_IRQ -0	BT34_IR Q-1	BT58_IR Q-0	BT58_IR Q-1	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL L[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN880 (0x06E0)	DMA[67]	RESSEL (0-7)	BT11_IRQ -0	BT11_IRQ -1	BT35_IRQ -0	BT35_IR Q-1	BT59_IRQ Q-0	BT59_IR Q-1	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN881 (0x06E2)	DMA[68]	RESSEL (0-7)	BT12_IRQ -0	BT12_IRQ -1	BT36_IRQ -0	BT36_IR Q-1	BT60_IRQ Q-0	BT60_IR Q-1	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN882 (0x06E4)	DMA[69]	RESSEL (0-7)	BT13_IRQ -0	BT13_IRQ -1	BT37_IRQ -0	BT37_IR Q-1	BT61_IRQ Q-0	BT61_IR Q-1	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN883 (0x06E6)	DMA[70]	RESSEL (0-7)	BT14_IRQ -0	BT14_IRQ -1	BT38_IRQ -0	BT38_IR Q-1	BT62_IRQ Q-0	BT62_IR Q-1	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN884 (0x06E8)	DMA[71]	RESSEL (0-7)	BT15_IRQ -0	BT15_IRQ -1	BT39_IRQ -0	BT39_IR Q-1	BT63_IRQ Q-0	BT63_IR Q-1	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL L[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN885 (0x06EA)	DMA[72]	RESSEL (0-7)	BT16_IRQ -0	BT16_IRQ -1	BT40_IRQ -0	BT40_IRQ Q-1	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN886 (0x06EC)	DMA[73]	RESSEL (0-7)	BT17_IRQ -0	BT17_IRQ -1	BT41_IRQ -0	BT41_IRQ Q-1	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN887 (0x06EE)	DMA[74]	RESSEL (0-7)	BT18_IRQ -0	BT18_IRQ -1	BT42_IRQ -0	BT42_IRQ Q-1	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN888 (0x06F0)	DMA[75]	RESSEL (0-7)	BT19_IRQ -0	BT19_IRQ -1	BT43_IRQ -0	BT43_IRQ Q-1	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN889 (0x06F2)	DMA[76]	RESSEL (0-7)	BT20_IRQ -0	BT20_IRQ -1	BT44_IRQ -0	BT44_IRQ Q-1	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL L[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN890 (0x06F4)	DMA[77]	RESSEL (0-7)	BT21_IRQ -0	BT21_IRQ -1	BT45_IRQ -0	BT45_IRQ Q-1	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN891 (0x06F6)	DMA[78]	RESSEL (0-7)	BT22_IRQ -0	BT22_IRQ -1	BT46_IRQ -0	BT46_IRQ Q-1	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN892 (0x06F8)	DMA[79]	RESSEL (0-7)	BT23_IRQ -0	BT23_IRQ -1	BT47_IRQ -0	BT47_IRQ Q-1	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN893 (0x06FA)	DMA[80]	RESSEL (0-7)	FRT0_Mat ch	FRT0_Zer o	FRT2_Mat ch	FRT2_Z ero	FRT4_M atch	FRT4_Z ero	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN894 (0x06FC)	DMA[81]	RESSEL (0-7)	FRT1_Mat ch	FRT1_Zer o	FRT3_Mat ch	FRT3_Z ero	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN895 (0x06FE)	DMA[82]	RESSEL (0-7)	FRT8_Mat ch	FRT8_Zer o	FRT10_M atch	FRT10_ Zero	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN896 (0x0700)	DMA[83]	RESSEL (0-7)	FRT9_Mat ch	FRT9_Zer o	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN897 (0x0702)	DMA[84]	RESSEL (0-7)	ICU0_IRQ 0	ICU2_IRQ 0	ICU4_IRQ 0	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN898 (0x0704)	DMA[85]	RESSEL (0-7)	ICU16_IR Q0	ICU18_IR Q0	ICU20_IR Q0	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN899 (0x0706)	DMA[86]	RESSEL (0-7)	ICU1_IRQ 1	ICU3_IRQ 1	ICU5_IRQ 1	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL L[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN900 (0x0708)	DMA[87]	RESSEL (0-7)	ICU17_IR Q1	ICU19_IR Q1	ICU21_IR Q1	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN901 (0x070A)	DMA[88]	RESSEL (0-7)	OCU0_IR Q0	OCU2_IR Q0	OCU4_IR Q0	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN902 (0x070C)	DMA[89]	RESSEL (0-7)	OCU16_IR Q0	OCU18_IR Q0	OCU20_IR Q0	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN903 (0x070E)	DMA[90]	RESSEL (0-7)	OCU1_IR Q1	OCU3_IR Q1	OCU5_IR Q1	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN904 (0x0710)	DMA[91]	RESSEL (0-7)	OCU17_IR Q1	OCU19_IR Q1	OCU21_IR Q1	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL L[3:0]	Source for Resource Input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RIC_RE SIN905 (0x0712)	DMA[92]	RESSEL (0-7)	RLT0_IRQ	RLT2_IRQ	RLT16_IRQ	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN906 (0x0714)	DMA[93]	RESSEL (0-7)	RLT1_IRQ	RLT3_IRQ	RLT17_IRQ	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
RIC_RE SIN907 (0x0716)	DMA[94]	RESSEL (0-7)	DMAC_RL T0	DMAC_RL T1	DMAC_RL T2	DMAC_ RLT3	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Note:

- If *BTx_ADTO* is used by *ADCx_HWTRGx*, set by the two *RIC_RESIN* (Resource Input Setting Register).
Select the *bt_adto_xxx_x* by *ADCx_HWTRGx* and then, select the *BTx_ADTO* by *bt_adto_xxx_x*.
- When both *GPIO_PORTEN.GPORTEN* and *PPC_PCFGR.PIE* are configured as 0, the input signal is disconnected and external interrupt cannot be detected. During disconnecting, I/O internally outputs "low" to internal logic, and if *ELVR* is configured as low-level-detection, falling-edge-detection, or both-edge-detection it will be detected as external interrupt with *EIRR*=1.
- *OCUx_MODn* is described as *MODn* pin in *Traveo™ Platform hardware manual*.

3.2. Port output function configuration

The port output function configuration (POF) is a function to select a function to output to a port.

A resource which supports a port output relocation has its PPC_PCFG.POF to configure resource output.

Register (Offset)	Port	Resource Functional Outputs							
		POF=0	POF=1	POF=2	POF=3	POF=4	POF=5	POF=6	POF=7
PPC_PCFG R000 (0x0000)	P000	GPIO_POD R0:POD00	-	-	SOT2	-	-	-	TIOA63
PPC_PCFG R001 (0x0002)	P001	GPIO_POD R0:POD01	-	SCS30	SCS20	-	-	-	TIOA54
PPC_PCFG R002 (0x0004)	P002	GPIO_POD R0:POD02	TIOA0	-	SCS21	-	-	-	-
PPC_PCFG R003 (0x0006)	P003	GPIO_POD R0:POD03	-	-	SCS22	-	-	-	-
PPC_PCFG R004 (0x0008)	P004	GPIO_POD R0:POD04	TIOA1	-	SCS23	-	-	-	-
PPC_PCFG R005 (0x000A)	P005	GPIO_POD R0:POD05	-	SCS83	-	-	-	-	TIOA55
PPC_PCFG R006 (0x000C)	P006	GPIO_POD R0:POD06	-	SOT3	-	-	-	SDA3	-
PPC_PCFG R007 (0x000E)	P007	GPIO_POD R0:POD07	-	SCK3	SCK12	-	-	SCL3	-
PPC_PCFG R008 (0x0010)	P008	GPIO_POD R0:POD08	TIOA0	SCS30	SCS120	-	-	-	-
PPC_PCFG R009 (0x0012)	P009	GPIO_POD R0:POD09	TIOA1	-	-	-	-	-	-
PPC_PCFG R010 (0x0014)	P010	GPIO_POD R0:POD10	TIOA2	SOT8	-	-	-	SDA8	-
PPC_PCFG R011 (0x0016)	P011	GPIO_POD R0:POD11	TIOA2	-	-	-	-	-	-
PPC_PCFG R012 (0x0018)	P012	GPIO_POD R0:POD12	TIOA3	SCK8	-	OUT5	-	SCL8	-

Register (Offset)	Port	Resource Functional Outputs							
		POF=0	POF=1	POF=2	POF=3	POF=4	POF=5	POF=6	POF=7
PPC_PCFG R013 (0x001A)	P013	GPIO_POD R0:POD13	TIOA4	SCS80	-	OUT16	-	-	-
PPC_PCFG R014 (0x001C)	P014	GPIO_POD R0:POD14	TIOA3	-	SOT12	-	-	-	-
PPC_PCFG R015 (0x001E)	P015	GPIO_POD R0:POD15	TIOA5	SCS81	-	OUT17	TX3	-	-
PPC_PCFG R016 (0x0020)	P016	GPIO_POD R0:POD16	TIOA6	SCS82	-	OUT18	-	-	-
PPC_PCFG R017 (0x0022)	P017	GPIO_POD R0:POD17	TIOA7	SCS83	-	OUT19	-	-	-
PPC_PCFG R018 (0x0024)	P018	GPIO_POD R0:POD18	TIOA8	-	-	OUT20	-	-	-
PPC_PCFG R019 (0x0026)	P019	GPIO_POD R0:POD19	-	-	-	OUT21	-	-	-
PPC_PCFG R020 (0x0028)	P020	GPIO_POD R0:POD20	-	SOT0	-	-	-	SDA0	-
PPC_PCFG R021 (0x002A)	P021	GPIO_POD R0:POD21	-	SCK0	SCK4	OUT2	-	SCL0	-
PPC_PCFG R022 (0x002C)	P022	GPIO_POD R0:POD22	-	-	-	OUT5	-	-	-
PPC_PCFG R023 (0x002E)	P023	GPIO_POD R0:POD23	-	SCS0	-	-	-	-	-
PPC_PCFG R024 (0x0030)	P024	GPIO_POD R0:POD24	-	-	SOT4	-	-	-	-
PPC_PCFG R025 (0x0032)	P025	GPIO_POD R0:POD25	-	-	SCS40	-	-	-	-
PPC_PCFG R026 (0x0034)	P026	GPIO_POD R0:POD26	-	-	SCS41	-	-	-	-
PPC_PCFG R027 (0x0036)	P027	GPIO_POD R0:POD27	TIOA4	SCS0	SCS42	-	-	-	-

Register (Offset)	Port	Resource Functional Outputs							
		POF=0	POF=1	POF=2	POF=3	POF=4	POF=5	POF=6	POF=7
PPC_PCFG R028 (0x0038)	P028	GPIO_POD R0:POD28	-	-	-	OUT0	-	-	-
PPC_PCFG R029 (0x003A)	P029	GPIO_POD R0:POD29	-	SOT1	-	OUT1	-	SDA1	TIOA30
PPC_PCFG R030 (0x003C)	P030	GPIO_POD R0:POD30	-	-	SCS43	OUT2	-	-	-
PPC_PCFG R031 (0x003E)	P031	GPIO_POD R0:POD31	-	SCS1	-	OUT3	-	-	TIOA31
PPC_PCFG R100 (0x0040)	P100	GPIO_POD R1:POD00	-	SCK1	-	OUT4	-	SCL1	-
PPC_PCFG R101 (0x0042)	P101	GPIO_POD R1:POD01	-	-	-	OUT5	-	-	TIOA56
PPC_PCFG R102 (0x0044)	P102	GPIO_POD R1:POD02	-	-	-	-	-	-	TIOA57
PPC_PCFG R103 (0x0046)	P103	GPIO_POD R1:POD03	-	-	-	OUT16	-	-	-
PPC_PCFG R104 (0x0048)	P104	GPIO_POD R1:POD04	-	-	-	-	-	-	-
PPC_PCFG R105 (0x004A)	P105	GPIO_POD R1:POD05	TIOA9	-	SCS110	OUT17	-	-	-
PPC_PCFG R106 (0x004C)	P106	GPIO_POD R1:POD06	-	-	-	OUT18	TX1	-	-
PPC_PCFG R107 (0x004E)	P107	GPIO_POD R1:POD07	TIOA10	-	-	OUT19	-	-	TOT0
PPC_PCFG R108 (0x0050)	P108	GPIO_POD R1:POD08	TIOA11	SOT11	-	OUT20	-	SDA11	-
PPC_PCFG R109 (0x0052)	P109	GPIO_POD R1:POD09	TIOA12	SCK11	-	OUT21	-	SCL11	TOT1
PPC_PCFG R110 (0x0054)	P110	GPIO_POD R1:POD10	-	SCS110	-	-	-	-	-

Register (Offset)	Port	Resource Functional Outputs							
		POF=0	POF=1	POF=2	POF=3	POF=4	POF=5	POF=6	POF=7
PPC_PCFG R111 (0x0056)	P111	GPIO_POD R1:POD11	-	-	-	-	-	-	-
PPC_PCFG R112 (0x0058)	P112	GPIO_POD R1:POD12	TIOA13	SOT12	-	-	-	SDA12	-
PPC_PCFG R113 (0x005A)	P113	GPIO_POD R1:POD13	TIOA5	SCK12	SOT11	-	-	SCL12	TOT2
PPC_PCFG R114 (0x005C)	P114	GPIO_POD R1:POD14	TIOA6	SCS120	-	-	-	-	TIOA32
PPC_PCFG R115 (0x005E)	P115	GPIO_POD R1:POD15	-	-	-	-	-	-	TOT3
PPC_PCFG R116 (0x0060)	P116	GPIO_POD R1:POD16	-	-	-	-	-	-	-
PPC_PCFG R117 (0x0062)	P117	GPIO_POD R1:POD17	-	-	SCK12	-	-	SCL12	-
PPC_PCFG R118 (0x0064)	P118	GPIO_POD R1:POD18	-	-	-	-	-	-	TOT16
PPC_PCFG R119 (0x0066)	P119	GPIO_POD R1:POD19	-	SCS60	-	-	-	-	-
PPC_PCFG R120 (0x0068)	P120	GPIO_POD R1:POD20	-	SCS61	-	-	-	-	TOT17
PPC_PCFG R121 (0x006A)	P121	GPIO_POD R1:POD21	TIOA14	SCS130	-	-	-	-	-
PPC_PCFG R122 (0x006C)	P122	GPIO_POD R1:POD22	TIOA11	SCS62	-	-	-	-	-
PPC_PCFG R123 (0x006E)	P123	GPIO_POD R1:POD23	TIOA12	SCS63	-	-	-	-	TIOA34
PPC_PCFG R124 (0x0070)	P124	GPIO_POD R1:POD24	TIOA15	-	-	-	-	-	-
PPC_PCFG R125 (0x0072)	P125	GPIO_POD R1:POD25	TIOA16	SOT13	-	-	-	SDA13	-

Register (Offset)	Port	Resource Functional Outputs							
		POF=0	POF=1	POF=2	POF=3	POF=4	POF=5	POF=6	POF=7
PPC_PCFG R126 (0x0074)	P126	GPIO_POD R1:POD26	-	SCK13	-	-	-	SCL13	TIOA35
PPC_PCFG R127 (0x0076)	P127	GPIO_POD R1:POD27	-	-	-	-	-	-	-
PPC_PCFG R128 (0x0078)	P128	GPIO_POD R1:POD28	-	-	-	-	-	-	-
PPC_PCFG R129 (0x007A)	P129	GPIO_POD R1:POD29	-	-	-	-	-	-	-
PPC_PCFG R130 (0x007C)	P130	GPIO_POD R1:POD30	-	-	-	-	-	-	-
PPC_PCFG R131 (0x007E)	P131	GPIO_POD R1:POD31	-	SOT6	-	-	-	SDA6	TIOA37
PPC_PCFG R200 (0x0080)	P200	GPIO_POD R2:POD00	TIOA17	-	-	-	-	-	-
PPC_PCFG R201 (0x0082)	P201	GPIO_POD R2:POD01	TIOA18	-	-	-	-	-	-
PPC_PCFG R202 (0x0084)	P202	GPIO_POD R2:POD02	-	SCK6	-	-	-	SCL6	TIOA36
PPC_PCFG R203 (0x0086)	P203	GPIO_POD R2:POD03	-	-	-	-	-	-	-
PPC_PCFG R204 (0x0088)	P204	GPIO_POD R2:POD04	-	-	-	-	TX4	-	-
PPC_PCFG R205 (0x008A)	P205	GPIO_POD R2:POD05	-	-	-	-	-	-	-
PPC_PCFG R206 (0x008C)	P206	GPIO_POD R2:POD06	-	SCS43	-	-	-	-	-
PPC_PCFG R207 (0x008E)	P207	GPIO_POD R2:POD07	-	SCK4	SCL4	-	-	-	TIOA38
PPC_PCFG R208 (0x0090)	P208	GPIO_POD R2:POD08	TIOA19	SCS42	-	-	-	-	-

Register (Offset)	Port	Resource Functional Outputs							
		POF=0	POF=1	POF=2	POF=3	POF=4	POF=5	POF=6	POF=7
PPC_PCFG R209 (0x0092)	P209	GPIO_POD R2:POD09	TIOA20	SOT4	SDA4	-	-	-	-
PPC_PCFG R210 (0x0094)	P210	GPIO_POD R2:POD10	TIOA21	-	-	-	-	-	-
PPC_PCFG R211 (0x0096)	P211	GPIO_POD R2:POD11	TIOA22	SCS40	-	-	-	-	-
PPC_PCFG R212 (0x0098)	P212	GPIO_POD R2:POD12	TIOA13	SCS41	SCS50	-	-	-	-
PPC_PCFG R213 (0x009A)	P213	GPIO_POD R2:POD13	TIOA14	-	-	-	-	-	TIOA41
PPC_PCFG R214 (0x009C)	P214	GPIO_POD R2:POD14	TIOA15	-	SOT5	-	-	-	-
PPC_PCFG R215 (0x009E)	P215	GPIO_POD R2:POD15	TIOA16	-	SCK5	-	-	-	-
PPC_PCFG R216 (0x00A0)	P216	GPIO_POD R2:POD16	-	-	-	-	-	-	TIOA58
PPC_PCFG R217 (0x00A2)	P217	GPIO_POD R2:POD17	-	-	-	-	-	-	-
PPC_PCFG R218 (0x00A4)	P218	GPIO_POD R2:POD18	-	-	-	-	-	-	-
PPC_PCFG R219 (0x00A6)	P219	GPIO_POD R2:POD19	-	-	-	-	-	-	-
PPC_PCFG R220 (0x00A8)	P220	GPIO_POD R2:POD20	-	SCS53	-	-	TX2	-	-
PPC_PCFG R221 (0x00AA)	P221	GPIO_POD R2:POD21	-	SCS52	-	-	-	-	-
PPC_PCFG R222 (0x00AC)	P222	GPIO_POD R2:POD22	-	-	-	-	-	-	TIOA39
PPC_PCFG R223 (0x00AE)	P223	GPIO_POD R2:POD23	-	SCS51	-	-	-	-	TOT0

Register (Offset)	Port	Resource Functional Outputs							
		POF=0	POF=1	POF=2	POF=3	POF=4	POF=5	POF=6	POF=7
PPC_PCFG R224 (0x00B0)	P224	GPIO_POD R2:POD24	-	SCS50	-	-	TX0	-	TIOA40
PPC_PCFG R225 (0x00B2)	P225	GPIO_POD R2:POD25	-	SOT5	-	-	-	SDA5	-
PPC_PCFG R226 (0x00B4)	P226	GPIO_POD R2:POD26	TIOA17	SCK5	-	-	-	SCL5	-
PPC_PCFG R227 (0x00B6)	P227	GPIO_POD R2:POD27	TIOA23	SCK10	-	-	-	SCL10	TOT1
PPC_PCFG R228 (0x00B8)	P228	GPIO_POD R2:POD28	TIOA24	SOT10	-	-	TX0	SDA10	-
PPC_PCFG R229 (0x00BA)	P229	GPIO_POD R2:POD29	TIOA25	-	-	OUT0	-	-	TOT2
PPC_PCFG R230 (0x00BC)	P230	GPIO_POD R2:POD30	TIOA26	SCS103	-	OUT1	-	-	-
PPC_PCFG R231 (0x00BE)	P231	GPIO_POD R2:POD31	TIOA27	SCS102	-	OUT2	-	-	-
PPC_PCFG R300 (0x00C0)	P300	GPIO_POD R3:POD00	TIOA28	SCS101	-	OUT3	-	-	-
PPC_PCFG R301 (0x00C2)	P301	GPIO_POD R3:POD01	TIOA18	SCS100	-	OUT4	TRACEDA TA7	-	TIOA42
PPC_PCFG R302 (0x00C4)	P302	GPIO_POD R3:POD02	TIOA19	-	SCS102	TRACEDA TA6	-	TOT3	TIOA43
PPC_PCFG R303 (0x00C6)	P303	GPIO_POD R3:POD03	-	-	-	-	-	-	-
PPC_PCFG R304 (0x00C8)	P304	GPIO_POD R3:POD04	TIOA20	-	SCS101	TRACEDA TA5	-	-	-
PPC_PCFG R305 (0x00CA)	P305	GPIO_POD R3:POD05	TIOA29	-	SCS100	TRACEDA TA4	-	-	TOT16
PPC_PCFG R306 (0x00CC)	P306	GPIO_POD R3:POD06	-	SCS73	-	-	TX0	-	-

Register (Offset)	Port	Resource Functional Outputs							
		POF=0	POF=1	POF=2	POF=3	POF=4	POF=5	POF=6	POF=7
PPC_PCFG R307 (0x00CE)	P307	GPIO_POD R3:POD07	-	SCS72	-	TRACEDA TA3	-	-	-
PPC_PCFG R308 (0x00D0)	P308	GPIO_POD R3:POD08	TIOA28	-	-	-	-	-	-
PPC_PCFG R309 (0x00D2)	P309	GPIO_POD R3:POD09	TIOA29	-	-	TRACEDA TA2	-	TOT17	TIOA44
PPC_PCFG R310 (0x00D4)	P310	GPIO_POD R3:POD10	-	-	-	-	-	-	TIOA59
PPC_PCFG R311 (0x00D6)	P311	GPIO_POD R3:POD11	-	-	-	-	-	-	-
PPC_PCFG R312 (0x00D8)	P312	GPIO_POD R3:POD12	-	SCS71	-	-	-	-	-
PPC_PCFG R313 (0x00DA)	P313	GPIO_POD R3:POD13	-	SOT7	SDA7	TRACEDA TA1	-	-	-
PPC_PCFG R314 (0x00DC)	P314	GPIO_POD R3:POD14	TIOA7	SCK7	SCL7	TRACEDA TA0	TX8	-	-
PPC_PCFG R315 (0x00DE)	P315	GPIO_POD R3:POD15	TIOA8	SCS70	-	TRACECT L	-	-	-
PPC_PCFG R316 (0x00E0)	P316	GPIO_POD R3:POD16	TIOA21	-	-	-	-	-	-
PPC_PCFG R317 (0x00E2)	P317	GPIO_POD R3:POD17	TIOA9	-	-	-	TX1	-	-
PPC_PCFG R318 (0x00E4)	P318	GPIO_POD R3:POD18	TIOA10	-	-	-	-	-	-
PPC_PCFG R319 (0x00E6)	P319	GPIO_POD R3:POD19	-	-	-	-	-	-	TIOA60
PPC_PCFG R320 (0x00E8)	P320	GPIO_POD R3:POD20	-	-	-	PWUTRG _0	-	-	-
PPC_PCFG R321 (0x00EA)	P321	GPIO_POD R3:POD21	-	-	-	PWUTRG _1	TRACECL K	-	TIOA45

Register (Offset)	Port	Resource Functional Outputs							
		POF=0	POF=1	POF=2	POF=3	POF=4	POF=5	POF=6	POF=7
PPC_PCFG R322 (0x00EC)	TDO	TDO	GPIO_POD R3:POD22	-	-	-	-	-	-
PPC_PCFG R323 (0x00EE)	TDI	TDI	GPIO_POD R3:POD23	-	-	-	-	-	-
PPC_PCFG R324 (0x00F0)	TRST	TRST	GPIO_POD R3:POD24	-	-	-	-	-	-
PPC_PCFG R325 (0x00F2)	P325	GPIO_POD R3:POD25	-	-	-	-	-	-	TIOA61
PPC_PCFG R326 (0x00F4)	P326	GPIO_POD R3:POD26	-	-	-	-	-	-	-
PPC_PCFG R327 (0x00F6)	P327	GPIO_POD R3:POD27	-	-	SCK6	WOT	-	-	-
PPC_PCFG R328 (0x00F8)	P328	GPIO_POD R3:POD28	-	-	SOT6	-	-	-	-
PPC_PCFG R329 (0x00FA)	P329	GPIO_POD R3:POD29	-	-	-	-	-	-	-
PPC_PCFG R330 (0x00FC)	P330	GPIO_POD R3:POD30	-	-	SCS60	-	-	-	TIOA62
PPC_PCFG R331 (0x00FE)	P331	GPIO_POD R3:POD31	-	-	SCS60	-	-	-	-
PPC_PCFG R400 (0x0100)	P400	GPIO_POD R4:POD00	-	-	SCS61	-	-	-	-
PPC_PCFG R401 (0x0102)	P401	GPIO_POD R4:POD01	-	-	SCS62	SCK9	TX1	SCL9	TIOA46
PPC_PCFG R402 (0x0104)	P402	GPIO_POD R4:POD02	-	SCS90	SCS63	SOT9	-	SDA9	TIOA47
PPC_PCFG R403 (0x0106)	P403	GPIO_POD R4:POD03	-	-	-	TRACEDA TA0	-	-	-
PPC_PCFG R404 (0x0108)	P404	GPIO_POD R4:POD04	-	-	SCS90	TRACEDA TA1	-	-	-

Register (Offset)	Port	Resource Functional Outputs							
		POF=0	POF=1	POF=2	POF=3	POF=4	POF=5	POF=6	POF=7
PPC_PCFG R405 (0x010A)	P405	GPIO_POD R4:POD05	-	-	-	TRACEDA TA2	-	-	TIOA48
PPC_PCFG R406 (0x010C)	P406	GPIO_POD R4:POD06	-	SOT9	SDA9	TRACEDA TA3	TX2	-	TIOA49
PPC_PCFG R407 (0x010E)	P407	GPIO_POD R4:POD07	-	SCK9	SCK7	TRACEDA TA4	-	SCL9	-
PPC_PCFG R408 (0x0110)	P408	GPIO_POD R4:POD08	-	-	-	TRACEDA TA5	-	-	-
PPC_PCFG R409 (0x0112)	P409	GPIO_POD R4:POD09	TIOA24	SOT2	SDA2	TRACEDA TA6	-	-	TIOA50
PPC_PCFG R410 (0x0114)	P410	GPIO_POD R4:POD10	-	-	SCS70	-	-	-	TIOA51
PPC_PCFG R411 (0x0116)	P411	GPIO_POD R4:POD11	-	SCK2	SCS71	TRACEDA TA7	-	SCL2	-
PPC_PCFG R412 (0x0118)	P412	GPIO_POD R4:POD12	TIOA25	-	SCS72	-	-	-	-
PPC_PCFG R413 (0x011A)	P413	GPIO_POD R4:POD13	-	SCS20	SCS73	-	-	-	-
PPC_PCFG R414 (0x011C)	P414	GPIO_POD R4:POD14	-	-	SCS21	-	-	-	-
PPC_PCFG R415 (0x011E)	P415	GPIO_POD R4:POD15	TIOA26	-	-	-	-	-	-
PPC_PCFG R416 (0x0120)	P416	GPIO_POD R4:POD16	TIOA22	-	-	-	-	-	TIOA52
PPC_PCFG R417 (0x0122)	P417	GPIO_POD R4:POD17	TIOA23	-	SOT7	-	-	-	TIOA53
PPC_PCFG R418 (0x0124)	P418	GPIO_POD R4:POD18	-	-	SCS22	-	-	-	-
PPC_PCFG R419 (0x0126)	P419	GPIO_POD R4:POD19	TIOA27	-	SCS23	-	-	-	-

Register (Offset)	Port	Resource Functional Outputs							
		POF=0	POF=1	POF=2	POF=3	POF=4	POF=5	POF=6	POF=7
PPC_PCFG R420 (0x0128)	P420	GPIO_POD R4:POD20	-	-	SCK2	TRACECL K	-	-	SCL2
PPC_PCFG R421 (0x012A)	P421	GPIO_POD R4:POD21	-	-	-	TRACECT L	-	-	-
PPC_PCFG R422 (0x012C)	P422	GPIO_POD R4:POD22	-	-	-	CLK_CLK O	-	-	TIOA33

Note:

- The hyphen indicates that setting is prohibited.
- If the in/out function on ports is used, set the register of PPC_PCFGR(Port Setting Register) and RIC_RESIN(Resource Input Setting Register).

3.3. The Analog I/O Setting

If analog terminals assignment of the ADC is used, must set the following before using ADC.

- The PPC_PCFGR:PIE register of target port makes disable digital input to set to 0.
- The corresponding POF should be set to 0.
- The GPIO_DDR register of target port makes input control to set to 0.
- The PPC_PCFGR:PDE/PUE register of target port makes disable Pull-Up/Pull-Down to set to 0.

3.4. Input Level Setting

This section shows the I/O port input level settings.

Pin No. of Package			Port Name	Value of PPC_PCFG:PI[1:0]				Remark
LQFP 100	LQFP 144	TEQFP 176		2'b00	2'b01	2'b10	2'b11	
-	2	2	P000	CMOS-hys	Automotive	-	-	
2	3	3	P001	CMOS-hys	Automotive	-	-	
-	-	4	P002	CMOS-hys	Automotive	-	-	
-	4	5	P003	CMOS-hys	Automotive	-	-	
-	-	6	P004	CMOS-hys	Automotive	-	-	
3	5	7	P005	CMOS-hys	Automotive	-	-	
4	6	8	P006	CMOS-hys	Automotive	-	-	
5	7	9	P007	CMOS-hys	Automotive	-	-	
-	8	10	P008	CMOS-hys	Automotive	-	-	
-	9	11	P009	CMOS-hys	Automotive	-	-	
6	10	12	P010	CMOS-hys	Automotive	-	-	
-	-	13	P011	CMOS-hys	Automotive	-	-	
7	11	14	P012	CMOS-hys	Automotive	-	-	
8	12	15	P013	CMOS-hys	Automotive	-	-	
-	-	16	P014	CMOS-hys	Automotive	-	-	
9	13	17	P015	CMOS-hys	Automotive	-	-	
10	14	18	P016	CMOS-hys	Automotive	-	-	
-	15	19	P017	CMOS-hys	Automotive	-	-	
-	16	20	P018	CMOS-hys	Automotive	-	-	
-	17	21	P019	CMOS-hys	Automotive	-	-	
11	18	22	P020	CMOS-hys	Automotive	-	-	
12	19	23	P021	CMOS-hys	Automotive	-	-	
13	20	24	P022	CMOS-hys	Automotive	-	-	
-	21	25	P023	CMOS-hys	Automotive	-	-	
-	22	26	P024	CMOS-hys	Automotive	-	-	
-	-	27	P025	CMOS-hys	Automotive	-	-	
-	-	28	P026	CMOS-hys	Automotive	-	-	
14	23	29	P027	CMOS-hys	Automotive	-	-	
15	24	30	P028	CMOS-hys	Automotive	-	-	
16	25	31	P029	CMOS-hys	Automotive	-	-	
-	26	32	P030	CMOS-hys	Automotive	-	-	
17	27	33	P031	CMOS-hys	Automotive	-	-	
18	28	34	P100	CMOS-hys	Automotive	-	-	
-	29	35	P101	CMOS-hys	Automotive	-	-	
-	-	36	P102	CMOS-hys	Automotive	-	-	
19	30	37	P103	CMOS-hys	Automotive	-	-	
-	-	38	P104	CMOS-hys	Automotive	-	-	

Pin No. of Package			Port Name	Value of PPC_PCFG:PIL[1:0]				Remark
LQFP 100	LQFP 144	TEQFP 176		2'b00	2'b01	2'b10	2'b11	
20	31	39	P105	CMOS-hys	Automotive	-	-	
21	32	40	P106	CMOS-hys	Automotive	-	-	
22	33	41	P107	CMOS-hys	Automotive	-	-	
23	34	42	P108	CMOS-hys	Automotive	-	-	
24	35	43	P109	CMOS-hys	Automotive	-	-	
27	38	46	P422	CMOS-hys	Automotive	-	-	
-	-	47	P110	CMOS-hys	Automotive	-	-	
-	-	48	P111	CMOS-hys	Automotive	-	-	
28	39	49	P112	CMOS-hys	Automotive	-	-	
-	40	50	P113	CMOS-hys	Automotive	-	-	
29	41	51	P114	CMOS-hys	Automotive	-	-	
-	45	55	P115	CMOS-hys	Automotive	-	-	
-	-	56	P116	CMOS-hys	Automotive	-	-	
33	46	57	P117	CMOS-hys	Automotive	-	-	
-	47	58	P118	CMOS-hys	Automotive	-	-	
34	48	59	P119	CMOS-hys	Automotive	-	-	
-	49	60	P120	CMOS-hys	Automotive	-	-	
-	-	61	P121	CMOS-hys	Automotive	-	-	
35	50	62	P122	CMOS-hys	Automotive	-	-	
36	51	63	P123	CMOS-hys	Automotive	-	-	
-	-	64	P124	CMOS-hys	Automotive	-	-	
-	-	65	P125	CMOS-hys	Automotive	-	-	
37	52	66	P126	CMOS-hys	Automotive	-	-	
-	53	67	P127	CMOS-hys	Automotive	-	-	
38	54	68	P128	CMOS-hys	Automotive	-	-	
-	55	69	P129	CMOS-hys	Automotive	-	-	
39	56	70	P130	CMOS-hys	Automotive	-	-	
40	57	71	P131	CMOS-hys	Automotive	-	-	
-	-	72	P200	CMOS-hys	Automotive	-	-	
-	-	73	P201	CMOS-hys	Automotive	-	-	
41	58	74	P202	CMOS-hys	Automotive	-	-	
-	59	75	P203	CMOS-hys	Automotive	-	-	
42	60	76	P204	CMOS-hys	Automotive	-	-	
43	61	77	P205	CMOS-hys	Automotive	-	-	
-	62	78	P206	CMOS-hys	Automotive	-	-	
44	63	79	P207	CMOS-hys	Automotive	-	-	
-	64	80	P208	CMOS-hys	Automotive	-	-	
45	65	81	P209	CMOS-hys	Automotive	-	-	
-	66	82	P210	CMOS-hys	Automotive	-	-	
46	67	83	P211	CMOS-hys	Automotive	-	-	
-	68	84	P212	CMOS-hys	Automotive	-	-	

Pin No. of Package			Port Name	Value of PPC_PCFG:R:PIL[1:0]				Remark
LQFP 100	LQFP 144	TEQFP 176		2'b00	2'b01	2'b10	2'b11	
-	-	90	P216	CMOS-hys	Automotive	-	-	
-	-	91	P217	CMOS-hys	Automotive	-	-	
-	74	92	P218	CMOS-hys	Automotive	-	-	
-	75	93	P219	CMOS-hys	Automotive	-	-	
52	76	94	P220	CMOS-hys	Automotive	-	-	
-	-	95	P221	CMOS-hys	Automotive	-	-	
53	77	96	P222	CMOS-hys	Automotive	-	-	
54	78	97	P223	CMOS-hys	Automotive	-	-	
55	79	98	P224	CMOS-hys	Automotive	-	-	
56	80	99	P225	CMOS-hys	Automotive	-	-	
57	81	100	P226	CMOS-hys	Automotive	-	-	
58	82	101	P213	CMOS-hys	Automotive	-	-	
59	83	102	P214	CMOS-hys	Automotive	-	-	
60	84	103	P215	CMOS-hys	Automotive	-	-	
61	85	104	P227	CMOS-hys	Automotive	-	-	
62	86	105	P228	CMOS-hys	Automotive	-	-	
63	87	106	P229	CMOS-hys	Automotive	-	-	
-	88	107	P230	CMOS-hys	Automotive	-	-	
-	89	108	P231	CMOS-hys	Automotive	-	-	
-	90	109	P300	CMOS-hys	Automotive	-	-	
64	91	110	P301	CMOS-hys	Automotive	-	-	
65	92	111	P302	CMOS-hys	Automotive	-	-	
-	-	112	P303	CMOS-hys	Automotive	-	-	
66	93	113	P304	CMOS-hys	Automotive	-	-	
67	94	114	P305	CMOS-hys	Automotive	-	-	
-	96	116	P306	CMOS-hys	Automotive	-	-	
69	97	117	P307	CMOS-hys	Automotive	-	-	
-	98	118	P308	CMOS-hys	Automotive	-	-	
70	99	119	P309	CMOS-hys	Automotive	-	-	
-	-	120	P310	CMOS-hys	Automotive	-	-	
-	-	121	P311	CMOS-hys	Automotive	-	-	
-	100	122	P312	CMOS-hys	Automotive	-	-	
71	101	123	P313	CMOS-hys	Automotive	-	-	
72	102	124	P314	CMOS-hys	Automotive	-	-	
73	103	125	P315	CMOS-hys	Automotive	-	-	
-	-	126	P316	CMOS-hys	Automotive	-	-	
-	104	127	P317	CMOS-hys	Automotive	-	-	
-	105	128	P318	CMOS-hys	Automotive	-	-	
-	106	129	P319	CMOS-hys	Automotive	-	-	
-	-	130	P320	CMOS-hys	Automotive	-	-	
74	107	131	P321	CMOS-hys	Automotive	-	-	

Pin No. of Package			Port Name	Value of PPC_PCFGR:PIL[1:0]				Remark
LQFP 100	LQFP 144	TEQFP 176		2'b00	2'b01	2'b10	2'b11	
77	110	134	TDO/P322	-	-	-	-	Output only
78	111	135	TCK	-	-	-	-	TTL input only
79	112	136	TMS	-	-	-	-	TTL input only
80	113	137	TDI/P323	-	-	-	-	TTL input only
81	114	138	TRST/P324	-	-	-	-	TTL input only
-	-	139	P325	CMOS-hys	Automotive	-	-	
-	-	140	P326	CMOS-hys	Automotive	-	-	
82	115	141	P327	CMOS-hys	Automotive	-	-	
-	-	142	P328	CMOS-hys	Automotive	-	-	
-	-	143	P329	CMOS-hys	Automotive	-	-	
-	116	144	P330	CMOS-hys	Automotive	-	-	
87	121	149	P331	CMOS-hys	Automotive	-	-	
88	122	150	P400	CMOS-hys	Automotive	-	-	
93	127	155	P401	CMOS-hys	Automotive	-	-	
94	128	156	P402	CMOS-hys	Automotive	-	-	
-	129	157	P403	CMOS-hys	Automotive	-	-	
-	130	158	P404	CMOS-hys	Automotive	-	-	
95	131	159	P405	CMOS-hys	Automotive	-	-	
-	132	160	P406	CMOS-hys	Automotive	-	-	
-	133	161	P407	CMOS-hys	Automotive	-	-	
-	134	162	P408	CMOS-hys	Automotive	-	-	
96	135	163	P409	CMOS-hys	Automotive	-	-	
-	-	164	P410	CMOS-hys	Automotive	-	-	
-	136	165	P411	CMOS-hys	Automotive	-	-	
-	-	166	P412	CMOS-hys	Automotive	-	-	
97	137	167	P413	CMOS-hys	Automotive	-	-	
-	138	168	P414	CMOS-hys	Automotive	-	-	
-	-	169	P415	CMOS-hys	Automotive	-	-	
98	139	170	P416	CMOS-hys	Automotive	-	-	
-	140	171	P417	CMOS-hys	Automotive	-	-	
-	141	172	P418	CMOS-hys	Automotive	-	-	
-	-	173	P419	CMOS-hys	Automotive	-	-	
99	142	174	P420	CMOS-hys	Automotive	-	-	
-	143	175	P421	CMOS-hys	Automotive	-	-	

Note:

- The hyphen of "Value of PPC_PCFGR:PIL[1:0]" indicates that setting is prohibited except for the initial values(PIL[1:0]=00).
- "CMOS-hys" is CMOS hysteresis input level.
- "Automotive" is Automotive hysteresis input level.
- To get detailed information about the input level, see the DC characteristics of the Datasheet.

3.5. Output Drive Capacity Setting

This section shows the I/O port output drive capacity settings.

Pin No. of Package			Port name	Value of PPC_PCFGR:ODR[1:0]				Remark
LQFP 100	LQFP 144	TEQFP 176		2'b00	2'b01	2'b10	2'b11	
-	2	2	P000	1mA	2mA	-	5mA	
2	3	3	P001	1mA	2mA	-	5mA	
-	-	4	P002	1mA	2mA	-	5mA	
-	4	5	P003	1mA	2mA	-	5mA	
-	-	6	P004	1mA	2mA	-	5mA	
3	5	7	P005	1mA	2mA	-	5mA	
4	6	8	P006	1mA	2mA	-	5mA	*1
5	7	9	P007	1mA	2mA	-	5mA	*1
-	8	10	P008	1mA	2mA	-	5mA	
-	9	11	P009	1mA	2mA	-	5mA	
6	10	12	P010	1mA	2mA	-	5mA	*2
-	-	13	P011	1mA	2mA	-	5mA	
7	11	14	P012	1mA	2mA	-	5mA	*2
8	12	15	P013	1mA	2mA	-	5mA	
-	-	16	P014	1mA	2mA	-	5mA	
9	13	17	P015	1mA	2mA	-	5mA	
10	14	18	P016	1mA	2mA	-	5mA	
-	15	19	P017	1mA	2mA	-	5mA	
-	16	20	P018	1mA	2mA	-	5mA	
-	17	21	P019	1mA	2mA	-	5mA	
11	18	22	P020	1mA	2mA	-	5mA	*2
12	19	23	P021	1mA	2mA	-	5mA	*2
13	20	24	P022	1mA	2mA	-	5mA	
-	21	25	P023	1mA	2mA	-	5mA	
-	22	26	P024	1mA	2mA	-	5mA	
-	-	27	P025	1mA	2mA	-	5mA	
-	-	28	P026	1mA	2mA	-	5mA	
14	23	29	P027	1mA	2mA	-	5mA	
15	24	30	P028	1mA	2mA	-	5mA	
16	25	31	P029	1mA	2mA	-	5mA	*2
-	26	32	P030	1mA	2mA	-	5mA	
17	27	33	P031	1mA	2mA	-	5mA	
18	28	34	P100	1mA	2mA	-	5mA	*2
-	29	35	P101	1mA	2mA	-	5mA	
-	-	36	P102	1mA	2mA	-	5mA	
19	30	37	P103	1mA	2mA	-	5mA	
-	-	38	P104	1mA	2mA	-	5mA	

Pin No. of Package			Port name	Value of PPC_PCFGR:ODR[1:0]				Remark
LQFP 100	LQFP 144	TEQFP 176		2'b00	2'b01	2'b10	2'b11	
20	31	39	P105	1mA	2mA	-	5mA	
21	32	40	P106	1mA	2mA	-	5mA	
22	33	41	P107	1mA	2mA	-	5mA	
23	34	42	P108	1mA	2mA	-	5mA	*2
24	35	43	P109	1mA	2mA	-	5mA	*2
27	38	46	P422	1mA	2mA	-	5mA	
-	-	47	P110	1mA	2mA	-	5mA	
-	-	48	P111	1mA	2mA	-	5mA	
28	39	49	P112	1mA	2mA	-	5mA	*2
-	40	50	P113	1mA	2mA	-	5mA	*2
29	41	51	P114	1mA	2mA	-	5mA	
-	45	55	P115	1mA	2mA	-	5mA	
-	-	56	P116	1mA	2mA	-	5mA	
33	46	57	P117	1mA	2mA	-	5mA	*2
-	47	58	P118	1mA	2mA	-	5mA	
34	48	59	P119	1mA	2mA	-	5mA	
-	49	60	P120	1mA	2mA	-	5mA	
-	-	61	P121	1mA	2mA	-	5mA	
35	50	62	P122	1mA	2mA	-	5mA	
36	51	63	P123	1mA	2mA	-	5mA	
-	-	64	P124	1mA	2mA	-	5mA	
-	-	65	P125	1mA	2mA	-	5mA	*2
37	52	66	P126	1mA	2mA	-	5mA	*2
-	53	67	P127	1mA	2mA	-	5mA	
38	54	68	P128	1mA	2mA	-	5mA	
-	55	69	P129	1mA	2mA	-	5mA	
39	56	70	P130	1mA	2mA	-	5mA	
40	57	71	P131	1mA	2mA	-	5mA	*2
-	-	72	P200	1mA	2mA	-	5mA	
-	-	73	P201	1mA	2mA	-	5mA	
41	58	74	P202	1mA	2mA	-	5mA	*2
-	59	75	P203	1mA	2mA	-	5mA	
42	60	76	P204	1mA	2mA	-	5mA	
43	61	77	P205	1mA	2mA	-	5mA	
-	62	78	P206	1mA	2mA	-	5mA	
44	63	79	P207	1mA	2mA	-	5mA	*2
-	64	80	P208	1mA	2mA	-	5mA	
45	65	81	P209	1mA	2mA	-	5mA	*2
-	66	82	P210	1mA	2mA	-	5mA	
46	67	83	P211	1mA	2mA	-	5mA	
-	68	84	P212	1mA	2mA	-	5mA	

Pin No. of Package			Port name	Value of PPC_PCFGR:ODR[1:0]				Remark
LQFP 100	LQFP 144	TEQFP 176		2'b00	2'b01	2'b10	2'b11	
-	-	90	P216	1mA	2mA	-	5mA	
-	-	91	P217	1mA	2mA	-	5mA	
-	74	92	P218	1mA	2mA	-	5mA	
-	75	93	P219	1mA	2mA	-	5mA	
52	76	94	P220	1mA	2mA	-	5mA	
-	-	95	P221	1mA	2mA	-	5mA	
53	77	96	P222	1mA	2mA	-	5mA	
54	78	97	P223	1mA	2mA	-	5mA	
55	79	98	P224	1mA	2mA	-	5mA	
56	80	99	P225	1mA	2mA	-	5mA	*1
57	81	100	P226	1mA	2mA	-	5mA	*1
58	82	101	P213	1mA	2mA	-	5mA	
59	83	102	P214	1mA	2mA	-	5mA	
60	84	103	P215	1mA	2mA	-	5mA	
61	85	104	P227	1mA	2mA	-	5mA	*2
62	86	105	P228	1mA	2mA	-	5mA	*2
63	87	106	P229	1mA	2mA	-	5mA	
-	88	107	P230	1mA	2mA	-	5mA	
-	89	108	P231	1mA	2mA	-	5mA	
-	90	109	P300	1mA	2mA	-	5mA	
64	91	110	P301	1mA	2mA	-	5mA	
65	92	111	P302	1mA	2mA	-	5mA	
-	-	112	P303	1mA	2mA	-	5mA	
66	93	113	P304	1mA	2mA	-	5mA	
67	94	114	P305	1mA	2mA	-	5mA	
-	96	116	P306	1mA	2mA	-	5mA	
69	97	117	P307	1mA	2mA	-	5mA	
-	98	118	P308	1mA	2mA	-	5mA	
70	99	119	P309	1mA	2mA	-	5mA	
-	-	120	P310	1mA	2mA	-	5mA	
-	-	121	P311	1mA	2mA	-	5mA	
-	100	122	P312	1mA	2mA	-	5mA	
71	101	123	P313	1mA	2mA	-	5mA	*2
72	102	124	P314	1mA	2mA	-	5mA	*2
73	103	125	P315	1mA	2mA	-	5mA	
-	-	126	P316	1mA	2mA	-	5mA	
-	104	127	P317	1mA	2mA	-	5mA	
-	105	128	P318	1mA	2mA	-	5mA	
-	106	129	P319	1mA	2mA	-	5mA	
-	-	130	P320	1mA	2mA	-	5mA	
74	107	131	P321	1mA	2mA	-	5mA	

Pin No. of Package			Port name	Value of PPC_PCFGR:ODR[1:0]				Remark
LQFP 100	LQFP 144	TEQFP 176		2'b00	2'b01	2'b10	2'b11	
77	110	134	TDO/P322	1mA	2mA	-	5mA	*3
78	111	135	TCK	-	-	-	-	Input only
79	112	136	TMS	-	-	-	5mA	*4
80	113	137	TDI/P323	1mA	2mA	-	5mA	
81	114	138	TRST/P324	1mA	2mA	-	5mA	
-	-	139	P325	1mA	2mA	-	5mA	
-	-	140	P326	1mA	2mA	-	5mA	
82	115	141	P327	1mA	2mA	-	5mA	
-	-	142	P328	1mA	2mA	-	5mA	
-	-	143	P329	1mA	2mA	-	5mA	
-	116	144	P330	1mA	2mA	-	5mA	
87	121	149	P331	1mA	2mA	-	5mA	
88	122	150	P400	1mA	2mA	-	5mA	
93	127	155	P401	1mA	2mA	-	5mA	*2
94	128	156	P402	1mA	2mA	-	5mA	*2
-	129	157	P403	1mA	2mA	-	5mA	
-	130	158	P404	1mA	2mA	-	5mA	
95	131	159	P405	1mA	2mA	-	5mA	
-	132	160	P406	1mA	2mA	-	5mA	*2
-	133	161	P407	1mA	2mA	-	5mA	*2
-	134	162	P408	1mA	2mA	-	5mA	
96	135	163	P409	1mA	2mA	-	5mA	*2
-	-	164	P410	1mA	2mA	-	5mA	
-	136	165	P411	1mA	2mA	-	5mA	*2
-	-	166	P412	1mA	2mA	-	5mA	
97	137	167	P413	1mA	2mA	-	5mA	
-	138	168	P414	1mA	2mA	-	5mA	
-	-	169	P415	1mA	2mA	-	5mA	
98	139	170	P416	1mA	2mA	-	5mA	
-	140	171	P417	1mA	2mA	-	5mA	
-	141	172	P418	1mA	2mA	-	5mA	
-	-	173	P419	1mA	2mA	-	5mA	
99	142	174	P420	1mA	2mA	-	5mA	*2
-	143	175	P421	1mA	2mA	-	5mA	

Note:

- The hyphen of "Value of PPC_PCFGR:ODR[1:0]" indicates that setting is prohibited except for the initial values(ODR[1:0]=00).
- *1 When the PPC_PCFGR:POF[2:0] value setting is "3"(SDA or SCL function setting), the output drive capacity is "I²C" regardless of the ODR setting. Then, the port status is to be the Open Drain, and IOL is to be 3mA.

- *2 When the `PPC_PCFGR:POF[2:0]` value setting is "3"(SDA or SCL function setting), the port status is to be the Pseudo Open Drain, and IOL is to be the configured value for ODR.
- *3 When the `PPC_PCFGR:POF[2:0]` value setting is "0"(TDO function setting), the output drive capacity is 5mA regardless of the ODR setting.
- *4 When the `PPC_PCFGR:POF[2:0]` value setting is "0"(TMS(SWD) function setting), the output drive capacity is 5mA regardless of the ODR setting.
- To get detailed information about the drive capability, see the DC characteristics of the Datasheet.

3.6. Port Status

3.6.1. Hi-z Control

Traveo™ Platform hardware manual has description of System Special Setting Register (SYSC0_SPECFGR).

The [bit23] PSSPADCTRL: PSS-time port configuring bit should be configured as below.

- 0: Do not perform Hi-z control.
- 1: Perform Hi-z control.

Note:

- At RUN mode, if configured as Hi-z control, it doesn't affect the port status immediately, but after executing WFI instruction to update the profile registers, then it turns out Hi-z status during PSS mode.
- As opposite control from PSS to RUN, the port status of Hi-z will automatically be released without reconfiguration of SYSC0_SPECFGR.PSSPADCTRL = 0.

3.6.2. Port Status Hold during PSS Mode

All of the GPIO area can be kept the port status during PSS mode by System Special Setting Register (SYSC0_SPECFGR).

The [bit31] to [bit24] HOLDIO_PD_x: HOLD data latch bit should be configured as below.

- 0: Do not retain control.
- 1: Retain control.

Note:

- During MCU RUN mode, I/O port status will be latched immediately after SYSC0_SPECFGR.HOLDIO_PD_x= 1 (Retain control) configured.
- After SYSC0_SPECFGR.HOLDIO_PD_x= 1, the status of followings will be latched. Please note that PID is not included, that is, input data cannot be latched.
 - PPC_PCFGRI_{ij} POD, POE, PIL, PUE, PDE, ODR, NFE, and POF. (excluding PID: Input data cannot be latched)
 - RIC_RESIN_x.PORTSEL and RESSEL
- At turning from MCU PSS mode to RUN, the latched status will not be released automatically. Configuration SYSC0_SPECFGR.HOLDIO_PD_x = 0 should be necessary for releasing the status.

3.7. Function Port Group

A port group specifies an I/O port combination for a peripheral function. A peripheral function has some port groups and should be configured and used within a port group of them which is defined in the following table in order to satisfy AC specification.

Do not take a port combination which is not described in the following table as s port group.

Function	Port Group
Multi-Function Serial Ch.0	Group1 - SCK0_0 - SIN0_0 - SOT0_0 - SCS0_0/SCS0_1
Multi-Function Serial Ch.1	Group1 - SCK1_0 - SIN1_0 - SOT1_0 - SCS1_0
Multi-Function Serial Ch.2	Group1 - SCK2_0 - SIN2_0 - SOT2_0 - SCS20_0 - SCS21_0 - SCS22_0 - SCS23_0 Group2 - SCK2_1 - SIN2_0/SIN2_1/SIN2_2 - SOT2_0/SOT2_1 - SCS20_0/SCS20_1 - SCS21_0/SCS21_1 - SCS22_0/SCS22_1 - SCS23_0/SCS23_1
Multi-Function Serial Ch.3	Group1 - SCK3_0 - SIN3_0 - SOT3_0 - SCS30_0/SCS30_1

Function	Port Group
Multi-Function Serial Ch.4	Group1 - SCK4_0 - SIN4_0/SIN4_2 - SOT4_0 - SCS40_0 - SCS41_0 - SCS42_0 - SCS43_0
	Group2 - SCK4_1 - SIN4_1 - SOT4_1 - SCS40_1 - SCS41_1 - SCS42_1 - SCS43_1
Multi-Function Serial Ch.5	Group1 - SCK5_0/SCK5_1 - SIN5_0/SIN5_1 - SOT5_0/SOT5_1 - SCS50_0 - SCS51_0 - SCS52_0 - SCS53_0
Multi-Function Serial Ch.6	Group1 - SCK6_0 - SIN6_0 - SOT6_0 - SCS60_0 - SCS61_0 - SCS62_0 - SCS63_0
	Group2 - SCK6_1 - SIN6_1 - SOT6_1 - SCS60_1/SCS60_2 - SCS61_1 - SCS62_1 - SCS63_1

Function	Port Group
Multi-Function Serial Ch.7	Group1 - SCK7_0 - SIN7_0/SIN7_2/SIN7_3 - SOT7_0 - SCS70_0 - SCS71_0 - SCS72_0 - SCS73_0 Group2 - SCK7_1 - SIN7_1 - SOT7_1 - SCS70_1 - SCS71_1 - SCS72_1 - SCS73_1
Multi-Function Serial Ch.8	Group1 - SCK8_0 - SIN8_0/SIN8_1/SIN8_2 - SOT8_0 - SCS80_0 - SCS81_0 - SCS82_0 - SCS83_0/SCS83_1
Multi-Function Serial Ch.9	Group1 - SCK9_0/SCK9_1 - SIN9_0 - SOT9_0/SOT9_1 - SCS90_0/SCS90_1
Multi-Function Serial Ch.10	Group1 - SCK10_0 - SIN10_0 - SOT10_0 - SCS100_0/SCS100_1 - SCS101_0/SCS101_1 - SCS102_0/SCS102_1 - SCS103_0
Multi-Function Serial Ch.11	Group1 - SCK11_0 - SIN11_0 - SOT11_0/SOT11_1 - SCS110_0/SCS110_1

Function	Port Group
Multi-Function Serial Ch.12	Group1 - SCK12_0/SCK12_2 - SIN12_0/SIN12_2 - SOT12_0 - SCS120_0
	Group2 - SCK12_1 - SIN12_1 - SOT12_1 - SCS120_1
Multi-Function Serial Ch.13	Group1 - SCK13_0 - SIN13_0 - SOT13_0 - SCS130_0

3.8. Key Code Register

The write access to I/O Port register is protected by Key Code Register.

Table 3-1 Relationship between I/O Port Register and Key Code Register

I/O Port Register	Key Code Register	Remark
Data Direction Register (GPIO_DDRI)	GPIO Key Code Register (GPIO_KEYCDR)	-
Data Direction Set Register (GPIO_DDSDRI)	GPIO Key Code Register (GPIO_KEYCDR)	-
Data Direction Clear Register (GPIO_DDCRI)	GPIO Key Code Register (GPIO_KEYCDR)	-
Port Output Data Register (GPIO_PODRI)	-	-
Port Output Set Register (GPIO_POSRI)	-	-
Port Output Clear Register (GPIO_POCRI)	-	-
Port Input Enable Register (GPIO_PORTEN)	GPIO Key Code Register (GPIO_KEYCDR)	-
Port Input Data Register (GPIO_PIDRI)	-	-
GPIO Key Code Register (GPIO_KEYCDR)	-	-
Port Setting Register (PPC_PCFGRIj)	PPC Key Code Register (PPC_KEYCDR)	-
PPC Key Code Register (PPC_KEYCDR)	-	-
Resource Input Setting Register (RIC_RESINn)	RIC Key Code Register (RIC_KEYCDR)	-
RIC Key Code Register (RIC_KEYCDR)	-	-

4. Registers

See the common information of the registers on I/O Port.

5. Precautions

5.1. Noise Filter

Each GPIO has the noise filter for noise removal from external input. Also, some resources have additional dedicated noise filter for resource input. See the following Configuration and Diagram.

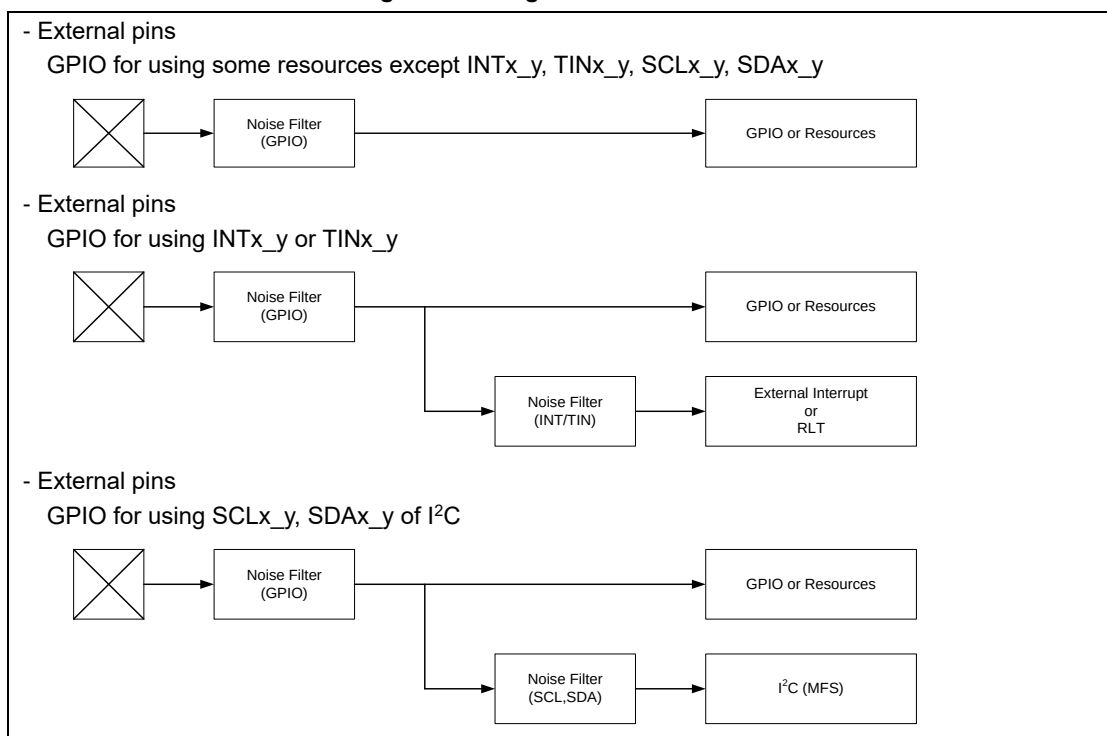
Table 5-1: Configuration for Noise Filter

Noise Filter for Resource	PPC_PCFGRIij: NFE	EICxx_NFER: NFE _n	RLTn_TMCSR: NFE	RIC_RESINn: RESSEL
GPIO	Enable/Disable	- *1	- *1	- *1
External interrupt (INT)	Disable *2	Enable/Disable	- *1	- *1
Reload Timer input (TIN)	Disable *2	- *1	Enable/Disable	- *1
I ² C interface (SCL, SDA)	Disable *2	- *1	- *1	Enable/Disable

*1: It is unrelated to register's setting.

*2: When selecting a Noise Filter other than for GPIO, set the Port Setting Register (PPC_PCFGRIij: NFE) to Disable.

Figure 5-1: Diagram of Noise Filter



5.2. I²C setting

For I²C fast-mode output pins "P006 (SDA3_0), P007 (SCL3_0), P225 (SDA5_0), P226 (SCL5_0)" to output Hi-Z after reset, the registers must be set in the following order.

- (1) Set the MD (Operation Mode Setting Bits) of the SMR (Serial Mode Register) to I²C mode.
- (2) Set the POF (Port Output Function Selection Bit) of the PPC_PCFGRIjj (Port Setting Register) to I²C.

If not set in the above order, the MCU will output "H" level before outputting Hi-Z to each port.

CHAPTER 12: State Transition



This chapter explains the state transition.

1. Overview
2. Diagram of State transition
3. Fetching the Operation Mode
4. Changes to PSS and RUN

CODE: STATE_TRANSITION-S6J3400-E1

1. Overview

This section gives a brief overview of State transition

Refer to the chapter of "Low-power Consumption" in Traveo™ Platform Hardware Manual for the detailed information for performing a change state.

2. Diagram of State Transition

This section shows diagram of state transitions.

The device state transitions for this series are shown below.

Figure 2-1 Diagram of Device State Transitions

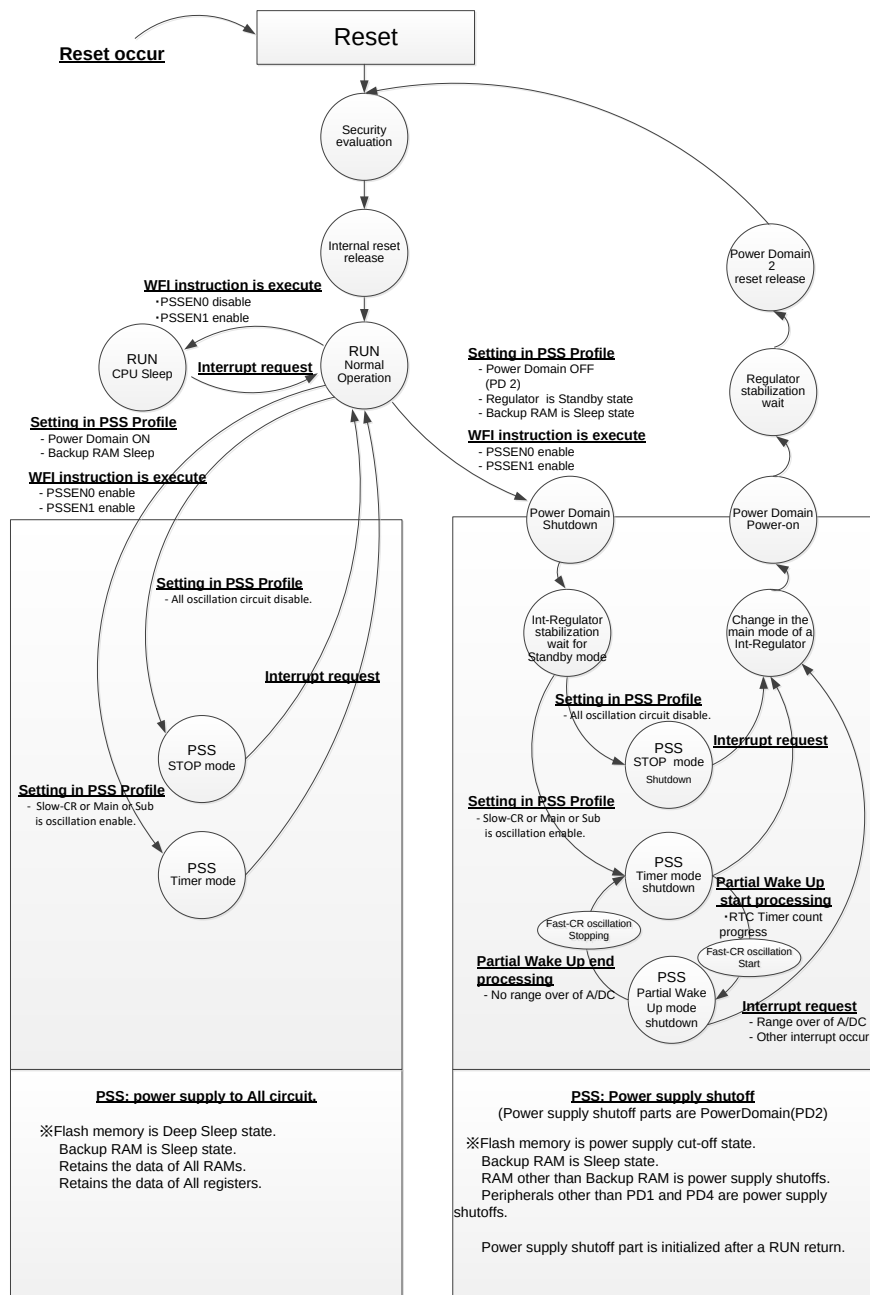


Figure 2-2 RUN/PSS State Definitions

S6J3400 supports only the below defined operating state.

Internal state and a frequency definition

		RUN Normal Operation	RUN CPU Sleep	PSS Timer mode	PSS STOP mode	PSS PWU mode Shutdown	PSS Timer mode shutdown	PSS STOP mode Shutdown
Clocks	CLK_CPU	Customer any Frequency	←	Prohibition of an oscillation	Prohibition of an oscillation	Prohibition of an oscillation	Prohibition of an oscillation	Prohibition of an oscillation
	CLK_FCLK							
	CLK_ATB							
	CLK_DBG			Customer any Frequency	Prohibition of an oscillation	Customer any Frequency	Prohibition of an oscillation	Prohibition of an oscillation
	CLK_HPM							
	CLK_DMA							
	CLK_MEMC			Prohibition of an oscillation	Prohibition of an oscillation	Prohibition of an oscillation	Prohibition of an oscillation	Prohibition of an oscillation
	CLK_SYSC1							
	CLK_TRC							
	CLK_SYSC0H							
	CLK_COMH							
	CLK_LLFBM							
	CLK_LCP							
	CLK_LCP0							
	CLK_LCP0A							
	CLK_LCP1							
	CLK_LCP1A							
oscillation state of a source clock	Slow-CR	100KHz	←	100KHz / disable	Prohibition of an oscillation	100KHz	100KHz / disable	Prohibition of an oscillation
	Fast-CR	4MHz	←	4MHz / disable	Prohibition of an oscillation	4MHz / disable (Fast-CR is unrelated to the PSS profile to oscillate.)	4MHz / disable	Prohibition of an oscillation
	Main oscillator	4MHz~16MHz	←	4~16MHz / disable	Prohibition of an oscillation	Prohibition of an oscillation	4~16MHz / disable	Prohibition of an oscillation
	Sub oscillator	32KHz	←	32KHz / disable	Prohibition of an oscillation	Prohibition of an oscillation	32KHz / disable	Prohibition of an oscillation
	PLL	Customer any Frequency	←	Prohibition of an oscillation				
	SSCG_PLL	Customer any Frequency	←					

The macro operating state in each mode, and the state of the power domain.

		RUN Normal Operation	RUN CPU Sleep	PSS Timer mode	PSS STOP mode	PSS PWU mode Shutdown	PSS Timer mode shutdown	PSS STOP mode Shutdown
CPU(PD2)	-	enable	disable	disable	disable	Power down	Power down	Power down
FLASH(PD2)	-	Operation	NOP	Deep Sleep	Deep Sleep	Power down	Power down	Power down
Backup RAM(PD4)	-	Operation	NOP	NOP	NOP	NOP	NOP	NOP
Int-Regulator	-	Main mode	Main mode	Main mode	Main mode	Standby mode	Standby mode	Standby mode
Power Domain	PD2	ON	ON	ON	ON	OFF	OFF	OFF
	PD4	ON	ON	ON	ON	ON	ON	ON

The conditions for changing in each state.

		RUN Normal Operation	RUN CPU Sleep	PSS Timer mode	PSS STOP mode	PSS PWU mode Shutdown	PSS Timer mode shutdown	PSS STOP mode Shutdown
Setup for changes	PSSSEN0	-	disable	enable	enable	enable	enable	enable
	PSSSEN1	-	enable	enable	enable	enable	enable	enable
Changes start command		-	Execution of a WFI command.					

Note:

- Do not disable FastCR (4MHz) in PSS mode (PD2: ON/OFF). If FastCR disable, Please see Note in the "5. Precautions for Using this Device" of chapter 24.

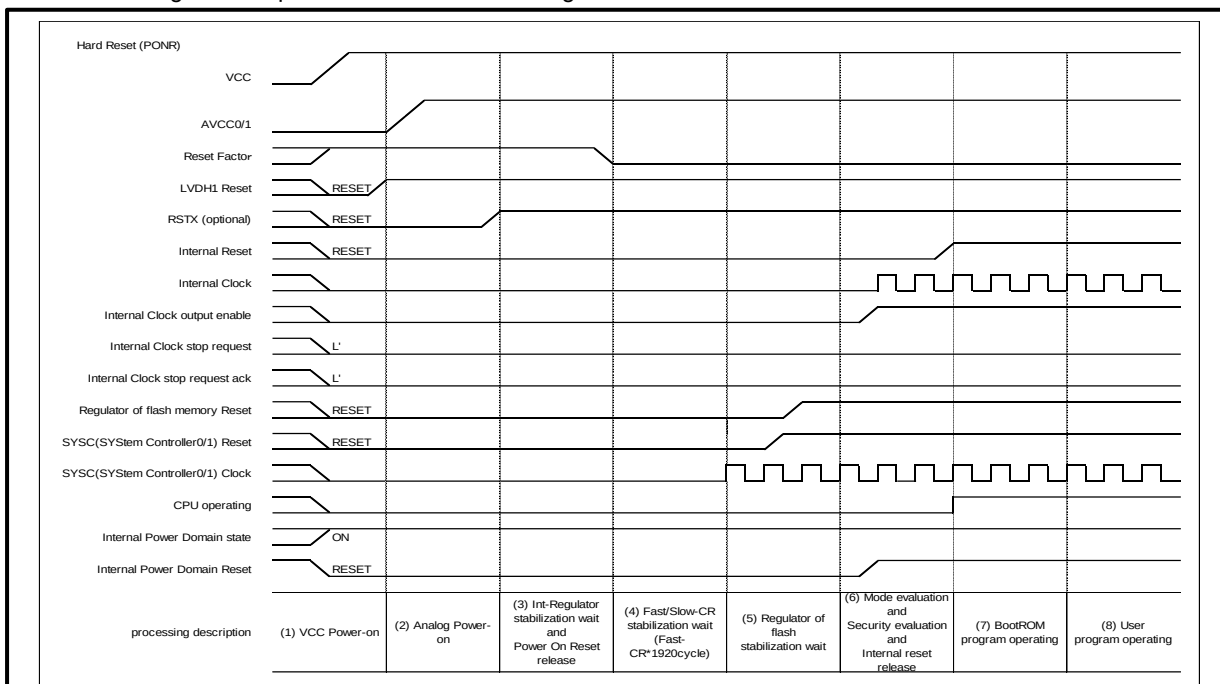
3. Fetching the Operation Mode

This section describes the Fetching the Operation Mode.

The operation mode is fetched by sampling the RST (Reset).

The following shows an operation sequence from an occurrence of reset cause to the determination of an operation mode.

Figure3-1 Operation Mode Fetch Timing Chart of PONR



S6J3400 guarantees that

- 1) Each power supply is stable before reset release for that domain
- 2) Isolation is valid before each pair of adjacent supplies is stable during power-up sequence

Power-up sequence defined in S6J3400 datasheet.

- 1) Each power supply is stable before reset release for that domain

Below table describes reset asserted until stabilization of each supply:

#	Power supply	Reset	Who must monitor the supply?	Corr. phase in POR release diagram (sheet "POR diagram")	Explanation of Reset
1	VCC	LVDH1 reset	CY MCU	(1)	VCC is monitored by LVDH1 which issues & releases reset above minimum operation voltage
2	VDD (internal 1.2V)	POR	CY MCU	(3)	VDD rises above minimum operation voltage during Int-Regulator stabilization wait shown in (3) in sheet POR Diagram
3	AVCC0/1	LVDH1 reset or RSTX	CY MCU or User	(1)	LVDH1 can monitor AVCC0/1 only if it's shorted with VCC on the board. Otherwise, this supply has to be monitored on the board and RSTX has to be issued to inactivate the domain until the supply is stable.

2) Isolation is valid before each pair of adjacent supplies is stable during power-up sequence

Below table describes isolation available for each adjacent supply pair:

#	From	To	Isolation method	Isolator assert timing (sheet "POR diagram")	Isolator release timing (sheet "POR diagram")
1	VCC	VDD	POR & LVDH1 initialize both domains until VCC stabilization	(1) POR assertion	(2) LVDH1 release
2	AVCC0/1	VDD	LVDH1 reset (if AVCC0/1 shorted w/ VCC on board) or RSTX, etc. (otherwise) works as isolation until AVCC0/1 powers up and user inverts the bit in software	(1) POR assertion or RSTX etc. assertion	(1) LVDH1 or RSTX etc. release
3	VDD	VCC	POR initialized both domains until VDD stabilization	(1) POR assertion	(3) POR release
4	VDD	AVCC0/1	POR initialized both domains until VDD stabilization	(1) POR assertion	(3) POR release

Existing power supply pairs (# in parenthesis = corresp. entry in above table):

From \ To	To			
		VCC	VDD	AVCC0/1
	VCC		x (1)	
	VDD	x (3)		x (4)
	AVCC0/1		x (2)	

VCC interacts only with regulated domain

VDD interacts with Always-ON domain I/Os

AVCC0/1 powers analog SWs & A/D in VDD domain

Figure3-2 Operation Mode Fetch Timing Chart of Other Reset

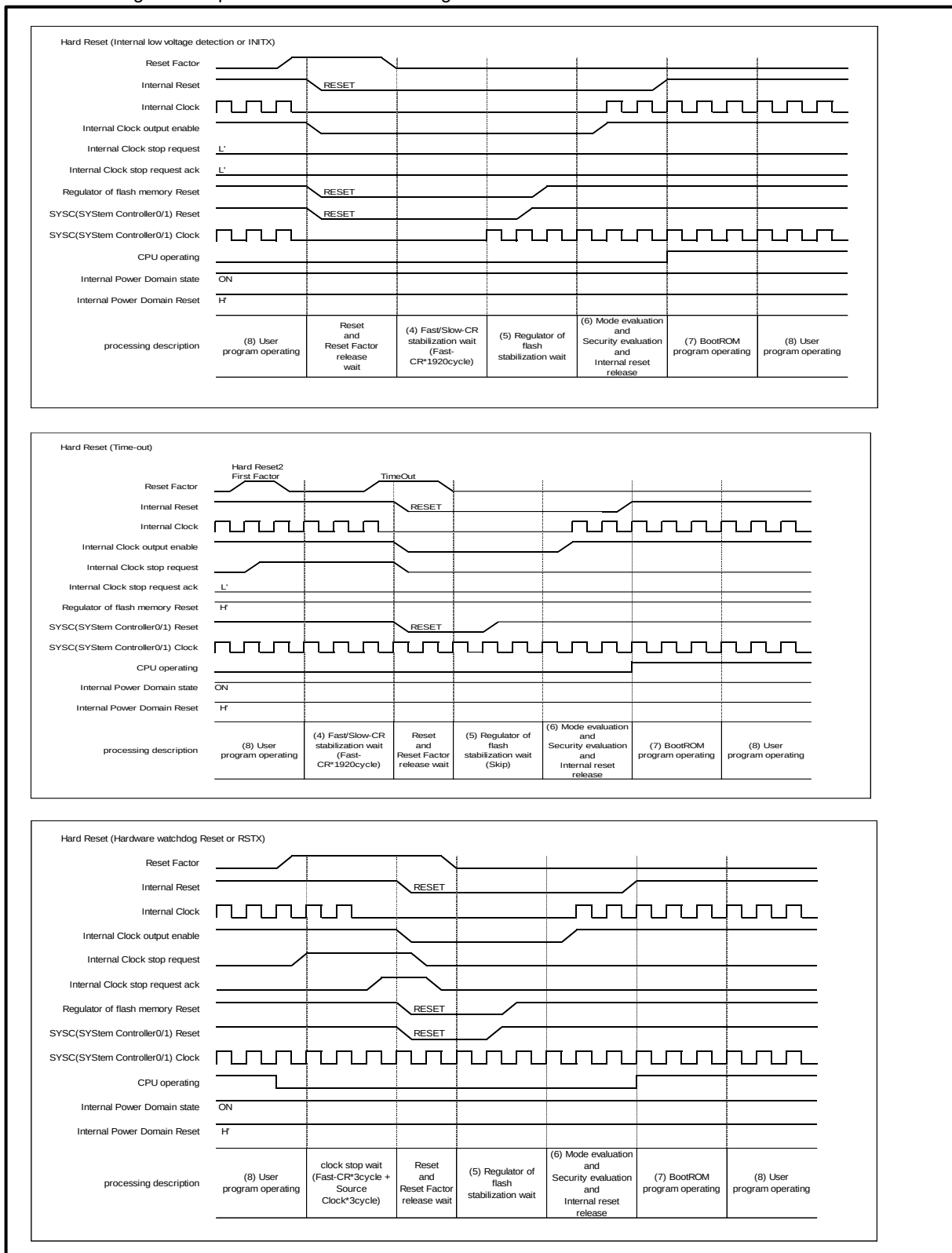
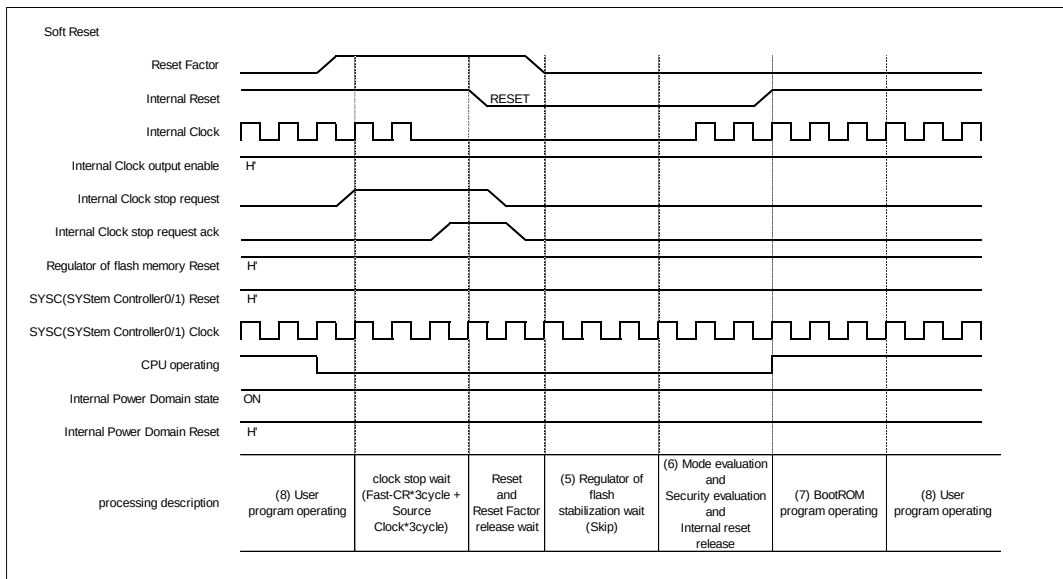
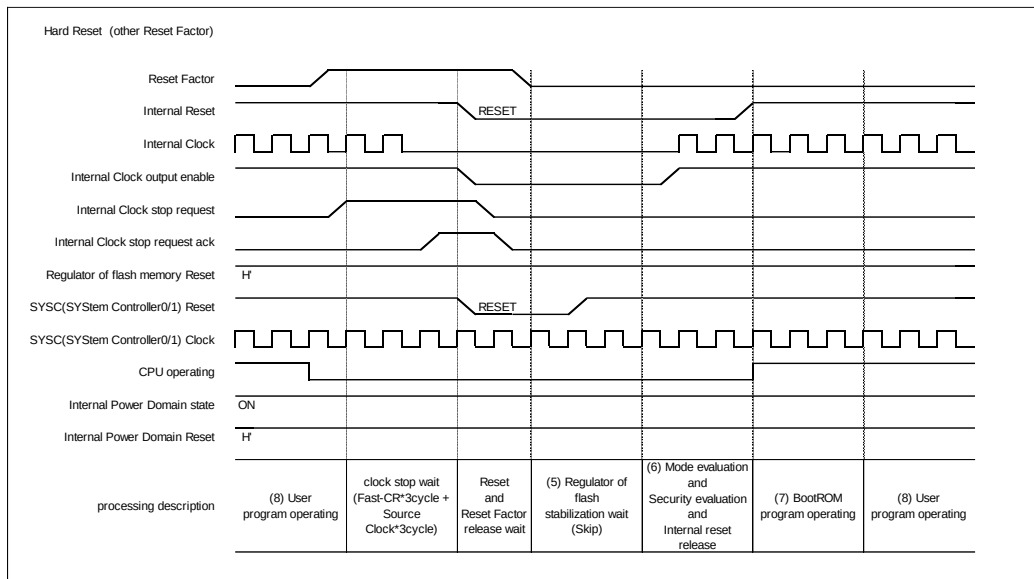


Figure3-3 Operation Mode Fetch Timing Chart of Other Reset



4. Changes to PSS and RUN

This section shows the sequence which changes to PSS and RUN.

Figure4-1 Changes to PSS Timing Chart

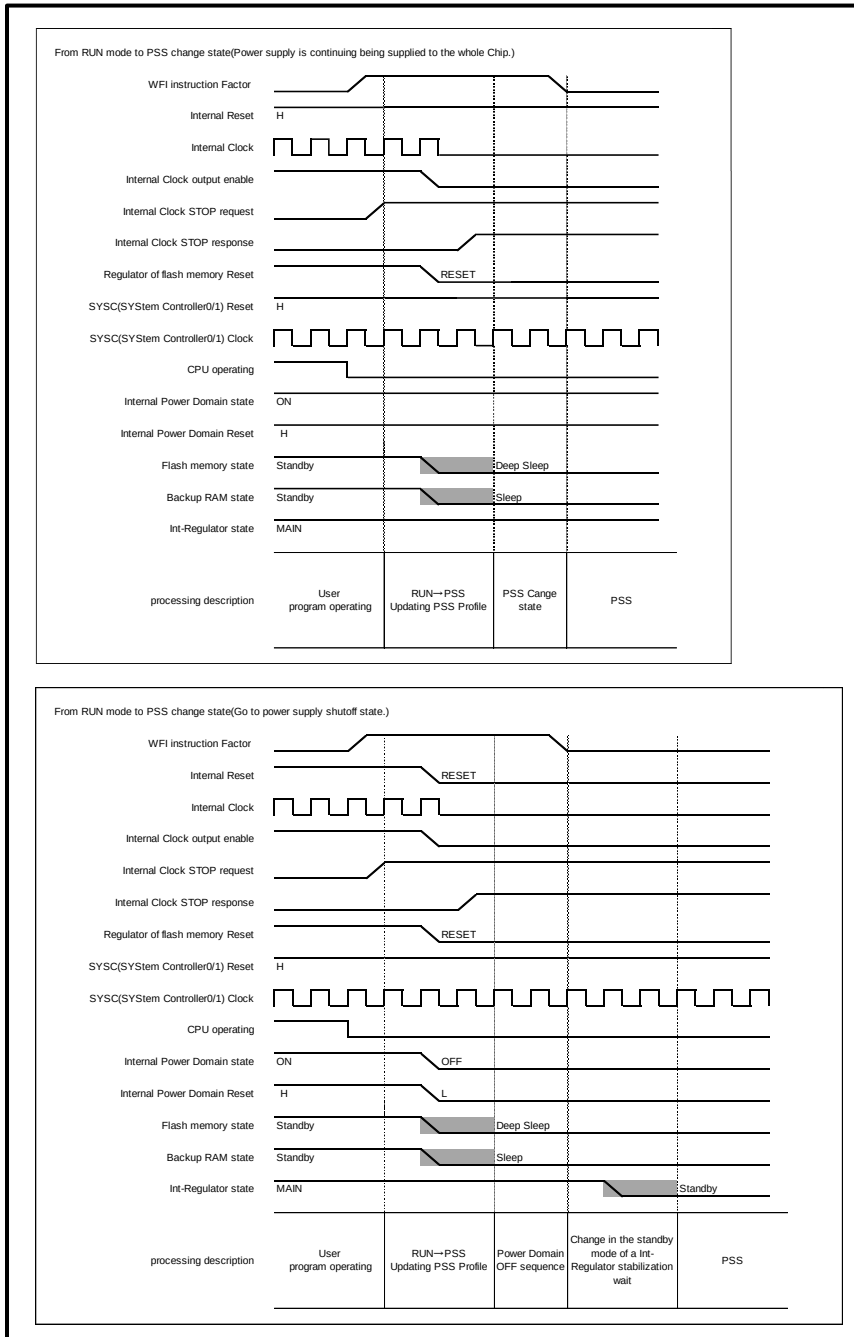


Figure4-2 Changes to PSS Timing Chart

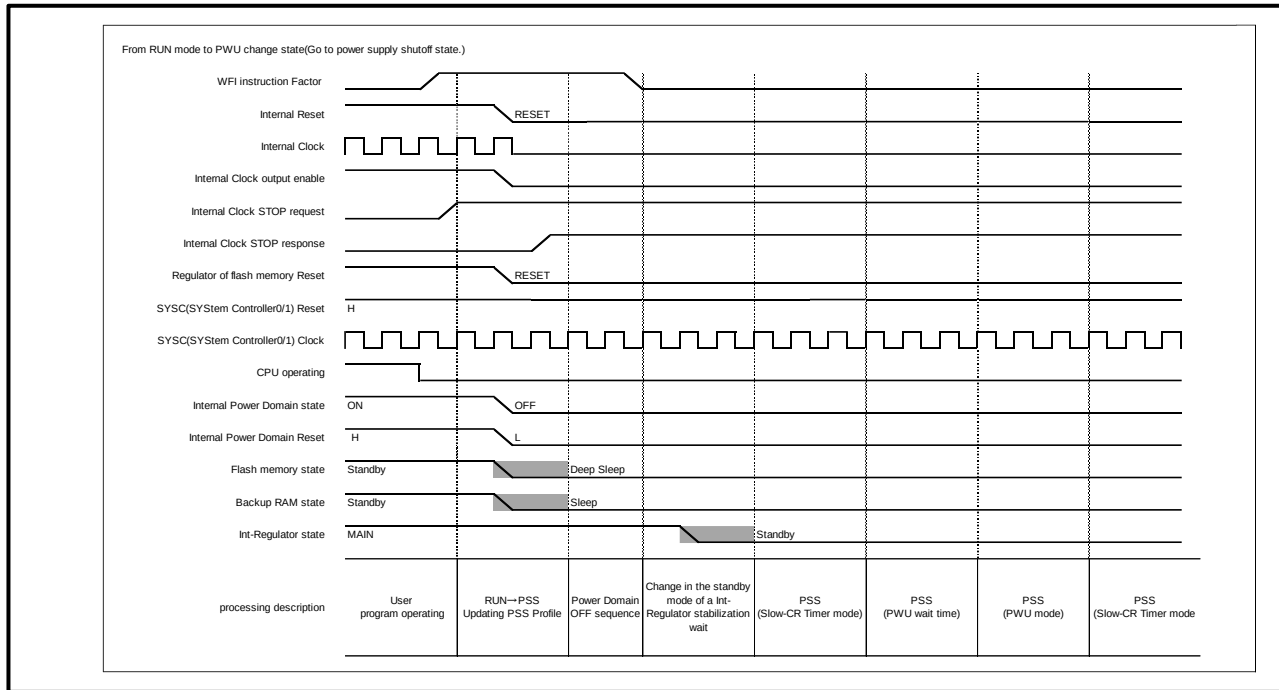
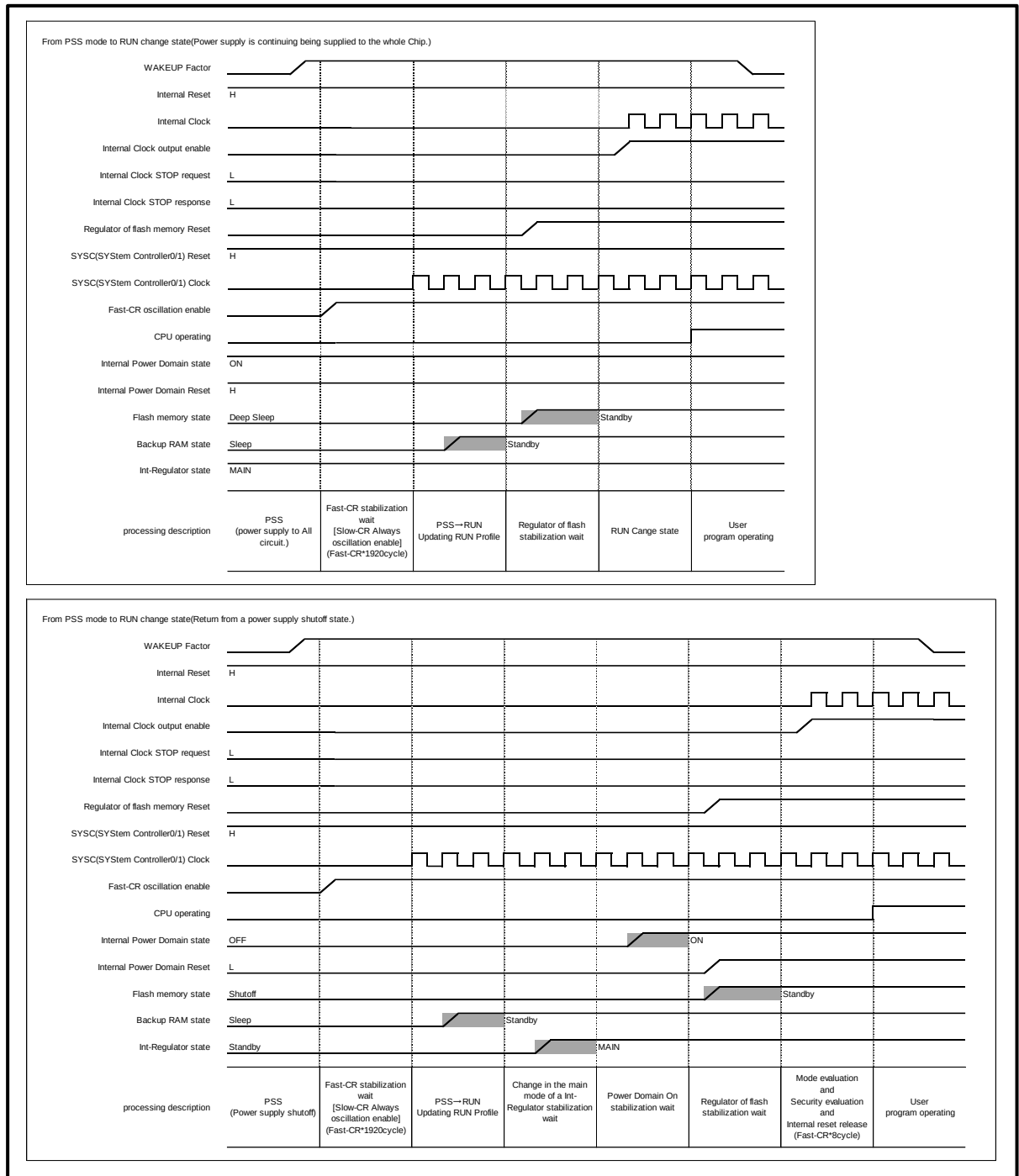


Figure4-3 Changes to RUN Timing Chart



CHAPTER 13: Pin Status in Each CPU State



This chapter explains pin status in each cpu state.

1. Pin Status in Each CPU State
2. Note

CODE: PIN_STATUS-S6J3400-E2

This section shows the pin status in each cpu state.

Legend
 HI-Z - Output is HI-Z.
 Input blocked - Input is actually disconnected.

- 280

2. Note

No description.

CHAPTER 14: Low Voltage Detection



This chapter explains the function of low voltage detection.

1. Overview
2. Configuration of supervised power domain
3. Registers

CODE: LVD-S6J3400-E2

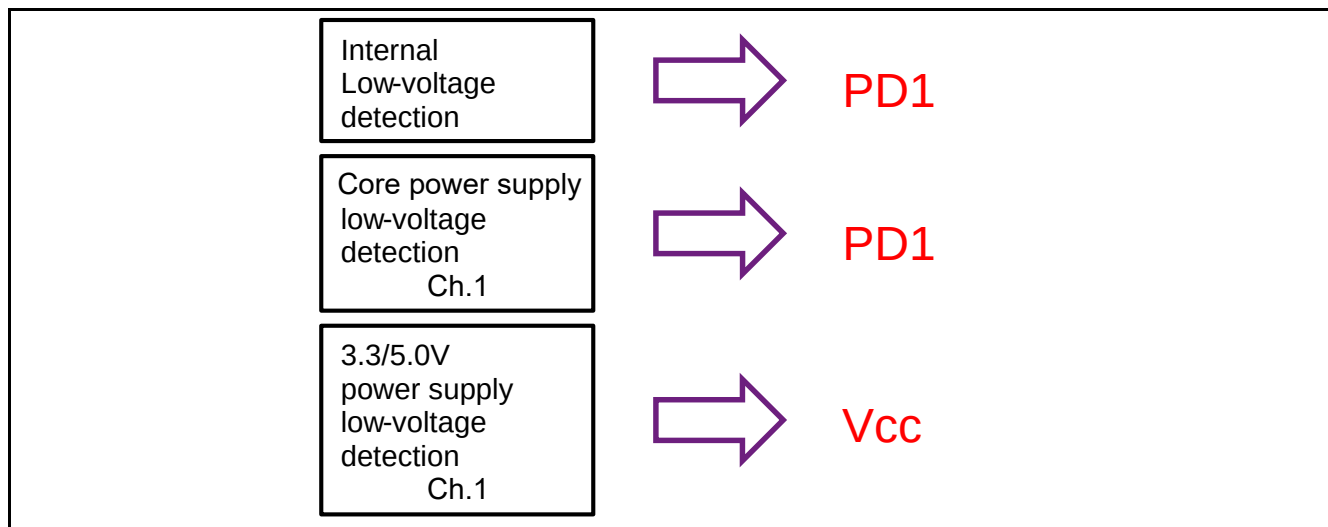
1. Overview

The low voltage detection and its supervised target are described here.

See the standard information and specification of Traveo™ Platform Hardware Manual.

2. Configuration of Supervised Power Domain

Figure 2-1 Supervised Power Domain



Note:

- PD stands for "power domain".
- The internal low-voltage detection is used for the power-on-reset function.
- PD1 includes PD2 and PD4 so the both can be supervised by means of PD1 supervision.
- Although 2 channels (ch.1 and ch.2) are described for core power supply low-voltage detection in specification of Traveo™ Platform Hardware Manual, this model has only 1 channel (ch.1).
- Although 2 channels (ch.1 and ch.2) are described for 3.3/5.0V power supply low-voltage detection in specification of Traveo™ Platform Hardware Manual, this model has only 1 channel (ch.1).

3. Registers

See the RUN/PSS/APP/STS Low-voltage Detection setting Register on Traveo™ Platform Hardware Manual.

Here, configurable value and its operation are described.

Note:

- *LVDH1 reset does not clear the LVDH1S, LVDH1V, LVDH1E configured value. The following factors clear the value to initial value.*
 - *Power-on reset.*
 - *LVDL0(RAM maintenance low voltage detection reset).*
 - *LVDL1(Internal low voltage detection reset).*
 - *Illegal mode detection reset.*
 - *INITX (RSTX pin + MD pin simultaneous assert reset).*

[Bit30] LVDL1S Internal low-voltage detection voltage operation selection bit

Bit 30	Description
0	Reset (Initial value)
1	Interrupt

Note:

- *LVDL1V will be initial value with reset. If LVDL1V is changed from initial value, LVDL1S should be configured as interrupt.*

[Bit27:25] LVDL1V Internal low-voltage detection voltage setting bits

Bit 27:25	Voltage [V]	Guaranteed MCU Operation Voltage Range
000 *	0.875(Initial value)	No
001 *	0.95	
010	Reserved	
011	Reserved	
100	Reserved	
101	Reserved	
110	Reserved	
111	Reserved	

*: This LVD cannot be used to reliably generate a reset before voltage dips below minimum guaranteed MCU operation voltage, as these detection levels are below the minimum guaranteed MCU operation voltage.

Note:

- *LVDL1V will be initial value with reset. If LVDL1V is changed from initial value, LVDL1S should be configured as interrupt.*

[Bit24] LVDL1E Internal low-voltage detection operation enable bit

Bit 24	Description
0	STOP operation
1	Enable operation (Initial value)

Note:

- LVDL1 corresponds to 1.2V power supply low-voltage detection ch.1

[Bit14] LVDH1S External low-voltage detection voltage operation selection bit

Bit 14	Description
0	Reset (Initial value)
1	Interrupt

Note:

- Set SYSC0_STSLVDCFG.LVDH1S = 0
- LVDH1 need to be used as Reset function.

[Bit11:9] LVDH1V External low-voltage detection voltage setting bits

Bit 11:9	Voltage [V]	Guaranteed MCU Operation Voltage Range
000 *	2.7	No
001	2.8	Yes
010	3.6	
011	3.8	
100	4.0	
101	4.2	
110 *	2.5	No
111 *	2.6(Initial value)	

*: These LVD settings cannot be used to reliably generate a reset before voltage dips below minimum guaranteed MCU operation voltage, as these detection levels are below the minimum guaranteed MCU operation voltage (2.7V).

[Bit8] LVDH1E External low-voltage detection operation enable bit

Bit 8	Description
0	STOP operation
1	Enable operation (Initial value)

Note:

- LVDH1 corresponds to 3.3/5.0V power supply low-voltage detection ch.1

CHAPTER 15: Serial Programming



This chapter explains serial programming.

1. Overview
2. Memory Map
3. Flash Sector Configuration
4. Port Configuration
5. Operation
6. Note.

CODE: SERIAL_PRG-S6J3400-E1

1. Overview

This chapter describes the FLASH serial programming. Please refer Traveo™ Platform Hardware Manual if necessary.

2. Memory Map

See the chapter of “Memory and Base Address Map” on this hardware manual.

3. Flash Sector Configuration

See the chapter of “TCFLASH” and “WorkFLASH” of Traveo™ Platform Hardware Manual.

4. Port Configuration

Table 4-1: Port Configuration and Usage

Port Name	Configuration	Remark
MODE	Pull-down	-
RSTX	Reset input	-
X0	Oscillation input	-
X1	Oscillation output	-
P022/SIN0_0	Pull-up: Clock asynchronous mode Pull-down: Clock synchronous mode Used for a serial input function after reset operation.	-
P020/SOT0_0	Pull-up: necessary until reset release. Used for a serial output function after reset operation.	-
P021/SCK0_0	Used for synchronous mode.	-

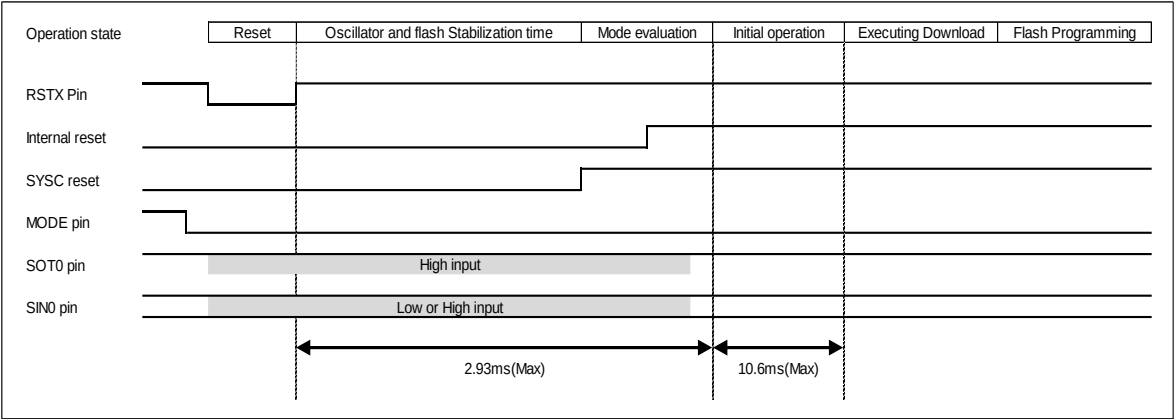
Note:

- See the chapter of “Port Description” on this manual” for Port name.
- See the “Pin Assignment” in Datasheet.

5. Operation

5.1. Timing Chart

Figure 5-1. Timing Chart



5.2. RAM Executing Communication Protocol

5.2.1. Command Format

5.2.1.1 Download Command

Byte Position	Byte Value	Explanation
1	00H	Download command
2	XXH	Download start address (A7-A0)
3	XXH	Download start address (A15-A8)
4	XXH	Download start address (A23-A16)
5	XXH	Download start address (A31-A24)
6	XXH	Download count number (BC7-BC0)
7	XXH	Download count number (BC15-BC8)
8	XXH	Download count number (BC23-BC16)
9	XXH	Download count number (BC31-BC24)
10	XXH	Sum value of download command(*1)

(*1) The SUM value is calculated in 8-bits, and the overflow of simple addition is ignored.

5.2.1.2 Executing Command

Byte Position	Byte Value	Explanation
1	C0H	Executing command
2	00H	Dummy data (For adjusting of command length)
3	00H	Dummy data (For adjusting of command length)
4	00H	Dummy data (For adjusting of command length)
5	00H	Dummy data (For adjusting of command length)
6	00H	Dummy data (For adjusting of command length)
7	00H	Dummy data (For adjusting of command length)
8	00H	Dummy data (For adjusting of command length)
9	00H	Dummy data (For adjusting of command length)
10	C0H	SUM value of executing command

5.2.1.3 Reset Command

Byte Position	Byte Value	Explanation
1	18H	Reset command

5.2.1.4 Full Chip Erase Command

Word Position	Word Value	Explanation
1	C0356EA5H	Key0
2	2E830596H	Key1
3	01A00000H	Key2

Word Position	Word Value	Explanation
4	F3A033EDH	Key3
5	370E6A51H	Key4
6	B0412000H	Key5
7	00000002H	Key6
8	AA805510H	Key7

5.2.2. Command Sequence

5.2.2.1 Download Command Sequence

Byte Count	Host(Tool) ⇒ Micom	Micom ⇒ Host(Tool)	
1 Byte	Receipt of down load command (00H)		
4 Byte	Receipt of download start address		
4 Byte	Receipt of download byte number		
1 Byte	SUM value of command		
1 Byte		Command response	
		Normal end	: 01H
		SUM malfunction	: X2H
		Command malfunction	: X4H
N Byte	Receipt of download data	Data input procedure(Little Endian)	
		D7~D0	
		D15~D8	
		D23~D16	
		D31~D24	
1 Byte	SUM value of download data (*1)		
1 Byte		Download processing response	
		Busy	: 00H
		Normal end	: 01H
		SUM malfunction	: 02H

(*1) About downloaded N byte data, SUM value is calculated in 8-bits, and the overflow of simple addition is ignored.

5.2.2.2 Executing Command Sequence

Byte Count	Host(Tool) ⇒ Micom	Micom ⇒ Host(Tool)	
1 Byte	Receipt of executing command (C0H)		
8 Byte	Receipt of dummy data (00H)		
1 Byte	SUM value of the command (C0H)		
(1 Byte)		Command response	
		(when SUM value is malfunction) (*1)	
		SUM malfunction	: C2H

(*1) Only when the SUM malfunction occurs, command response is returned. Command response is not returned except the SUM malfunction occurs. After receiving executing command, it jumps to the download start address specified by the download command if the SUM is not malfunctioning.

5.2.2.3 Reset Command Sequence

Byte count	Host(Tool) ⇒ Micom	Micom ⇒ Host(Tool)	
1 Byte	Download Command (18H)		
1 Byte		Command response (*1) Normal end	: 11H

(*1) Response of reset command is always normal end. (11H)

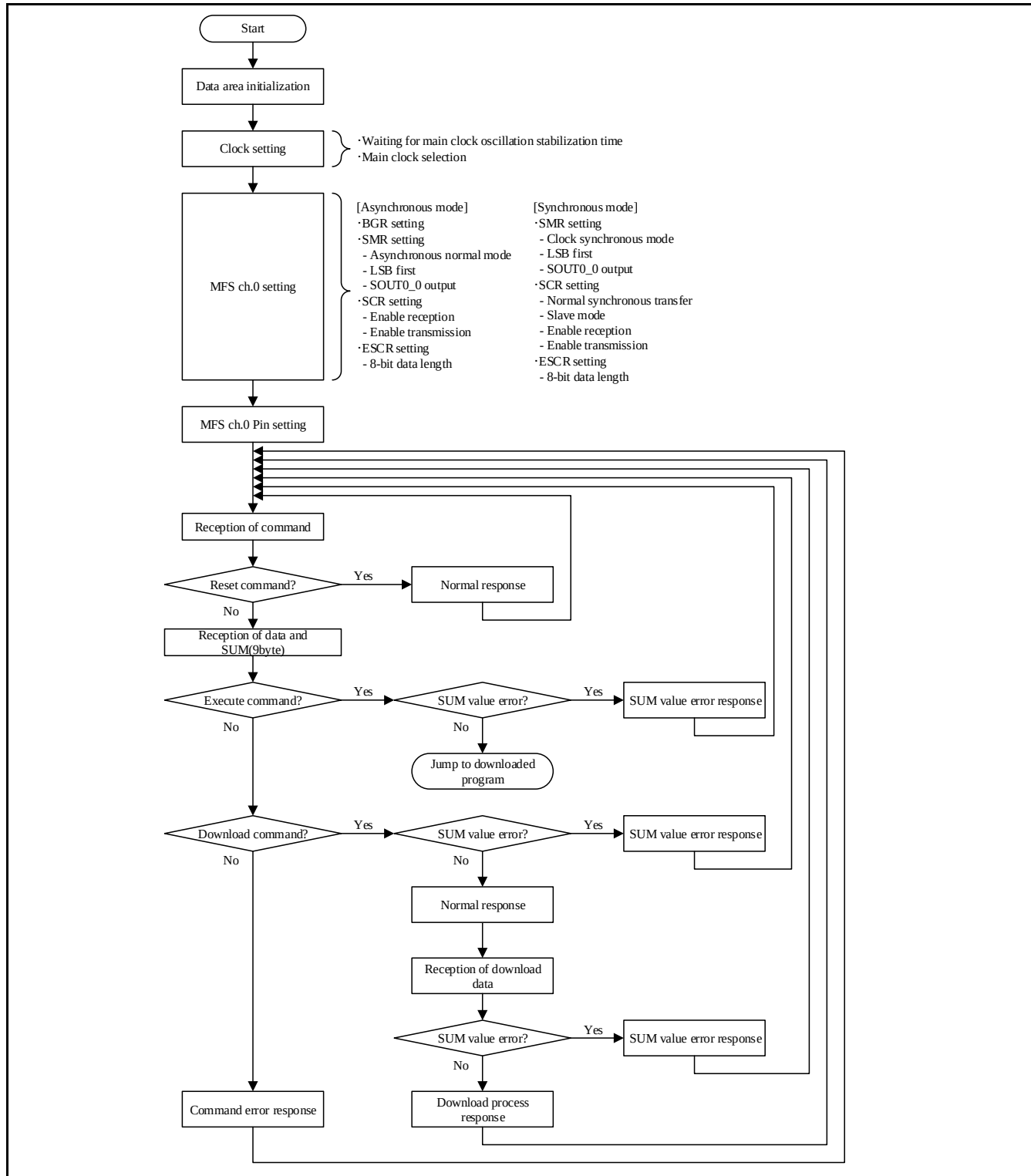
5.2.2.4 Full Chip Erase Command Sequence

Byte count	Host(Tool) ⇒ Micom	Micom ⇒ Host(Tool)	
1-32 Byte	Key0-7Receive	-	
4 Byte	-	Command response (*1) Normal end	: 12345678H
4 Byte	-	Command response (*1) Normal end	: BABEFACEH

(*1) Command response is returned only when it is normal end. In other cases, hard reset is operated and command response is not returned.

5.3. Operation Flow

Figure 5-2: Operation Flow Chart



6. Note.

See Traveo™ Platform Hardware Manual.

CHAPTER 16: Base Timer



This chapter explains the functions and operations of the Base Timer.

1. Overview of the Base Timer
2. Block Diagrams of the Base Timer
3. Operations of the Base Timer
4. 32-Bit Mode Operation
5. Debug Mode
6. Interrupts from the Base Timer
7. Start of DMA Controller (DMAC)
8. Registers of the Base Timer
9. Notes on Using the Base Timer
10. Base Timer Description by Function Mode

CODE:BT-S6J3400-E3

1. Overview of the Base Timer

Only one of the following timer functions can be selected for the Base Timer in the FMD2 to FMD0 bit settings in the Timer Control Register (TMCR): Reset mode, 16-bit PWM Timer, 16-bit PPG Timer, 16/32-bit Reload Timer, and 16/32-bit PWC Timer. This section provides an overview of the various selectable timers.

Relationship Between Mode Settings and Various Timer Functions

FMD2 to FMD0 Bit Settings in the Timer Control Register (TMCR)	Function
000	Reset mode
001	16-bit PWM Timer
010	16-bit PPG Timer
011	16/32-bit Reload Timer
100	16/32-bit PWC Timer

Reset Mode

Reset mode is the state in which the Base Timer macros have been reset (to the initial values in each register). To use another timer function or switch the T32 bit setting, first enter this mode and then set the other timer function or the T32 bit. However, after a macro reset, it is possible to set a timer function and the T32 bit without entering this mode.

16-Bit PWM Timer

The 16-bit PWM Timer operates in 16-bit periods.

This timer consists of a 17-bit down counter that takes into account the start delay period, a 16-bit data register with a cycle setting buffer, a 16-bit compare register with a duty setting buffer, a Start Delay Value Setting Register (PSDR), an ADC Trigger Value Setting Register (ADTR), and a pin controller.

The down counter will be described in 16 bit formats when the 16-bit PWM Timer is irrelevant to the start delay control.

The registers with buffers store the cycle and duty data, enabling rewriting while the timer is operating.

The counter clock of the 17-bit down counter can be selected from 12 types of internal clocks (internal clock divided by 1/2/4/8/16/32/64/128/256/512/1024/2048) and 3 types of external clocks (rising-edge, falling-edge, and both-edges detection).

One-shot mode and continuous mode can be selected. In one-shot mode, counting stops when an underflow occurs. In continuous mode, counting is repeated following a reload.

The start of the 16-bit PWM Timer can be selected from a software trigger and 3 types of external events (rising-edge, falling-edge, and both-edges detection).

The start delay function can delay the PWM control start time after trigger input.

An ADC trigger signal is output when the ADC Trigger Value Setting Register (ADTR) matches the count value of the 16-bit down counter.

The external timer match starting can start a timer, when a match of the value set as the External Timer Compare Data Register (ETCDR) and an external timer value is detected.

16-Bit PPG Timer

This timer consists of a 16-bit down counter, a 16-bit data register for the "H" width setting, a 16-bit data register for the "L" width setting, and a pin controller.

The count clock of the 16-bit down counter can be selected from 12 types of internal clocks (internal clock divided by 1/2/4/8/16/32/64/128/256/512/1024/2048) and 3 types of external clocks (rising-edge, falling-edge, and both-edges detection).

One-shot mode and continuous mode can be selected. In one-shot mode, counting stops when an underflow occurs. In continuous mode, counting is repeated following a reload.

The start of the 16-bit PPG Timer can be selected from a software trigger and 3 types of external events (rising-edge, falling-edge, and both-edges detection).

The external timer match starting can start a timer, when a match of the value set as the External Timer Compare Data Register (ETCDR) and an external timer value is detected.

16/32-Bit Reload Timer

This timer consists of a 16-bit down counter, a 16-bit reload register, and a pin controller.

The count clock of the 16-bit down counter can be selected from 12 types of internal clocks (internal clock divided by 1/2/4/8/16/32/64/128/256/512/1024/2048) and 3 types of external clocks (rising-edge, falling-edge, and both-edges detection).

One-shot mode and continuous mode can be selected. In one-shot mode, counting stops when an underflow occurs. In continuous mode, counting is repeated following a reload.

An external factor pin can be selected as a trigger input function or a gate function when the 16/32-bit Reload Timer is operating.

If the trigger input function is selected, the start of the 16/32-bit Reload Timer can be selected from a software trigger and 3 types of external events (rising-edge, falling-edge, and both-edges detection).

If the gate function is selected, the 16/32-bit Reload Timer counts only while a valid level is being input to the external factor pin.

The external timer match starting can start a timer, when a match of the value set as the External Timer Compare Data Register (ETCDR) and an external timer value is detected.

16/32-Bit PWC Timer

This timer consists of a 16-bit up counter, measurement input pins, and a control register.

With the input of external pulses, the timer measures the time between events.

The reference count clock can be selected from 12 types of internal clocks (divided by 1/2/4/8/16/32/64/128/256/512/1024/2048).

The supported measurement modes:

- "H" pulse width (rising to falling) / "L" pulse width (falling to rising)

- Rising cycle (rising to rising) / falling cycle (falling to falling)
- Edge-to-edge measurement (rising or falling to falling or rising)

An interrupt request can be generated at the measurement end time.

The measurement is 1-time only or continuous. Either can be selected.

2. Block Diagrams of the Base Timer

Figure 2-1 to Figure 2-4 are block diagrams of the Base Timer in each mode.

Figure 2-1 Block Diagram of the 16-Bit PWM Timer

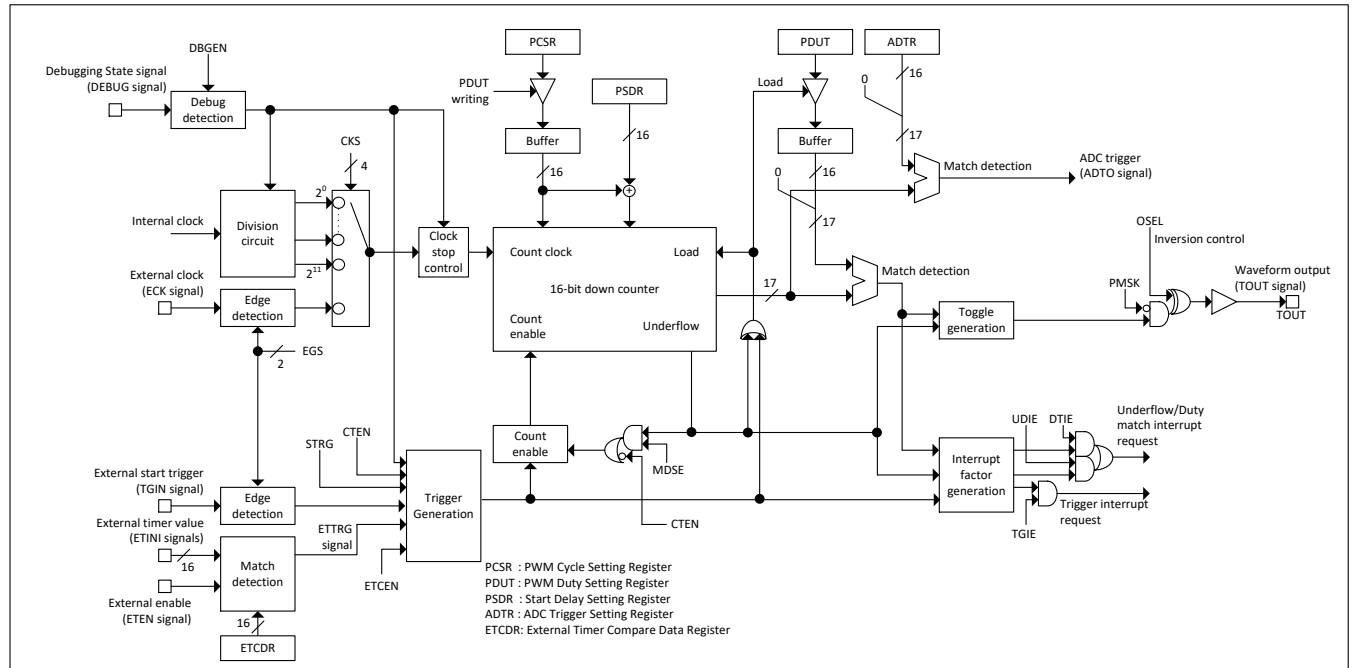


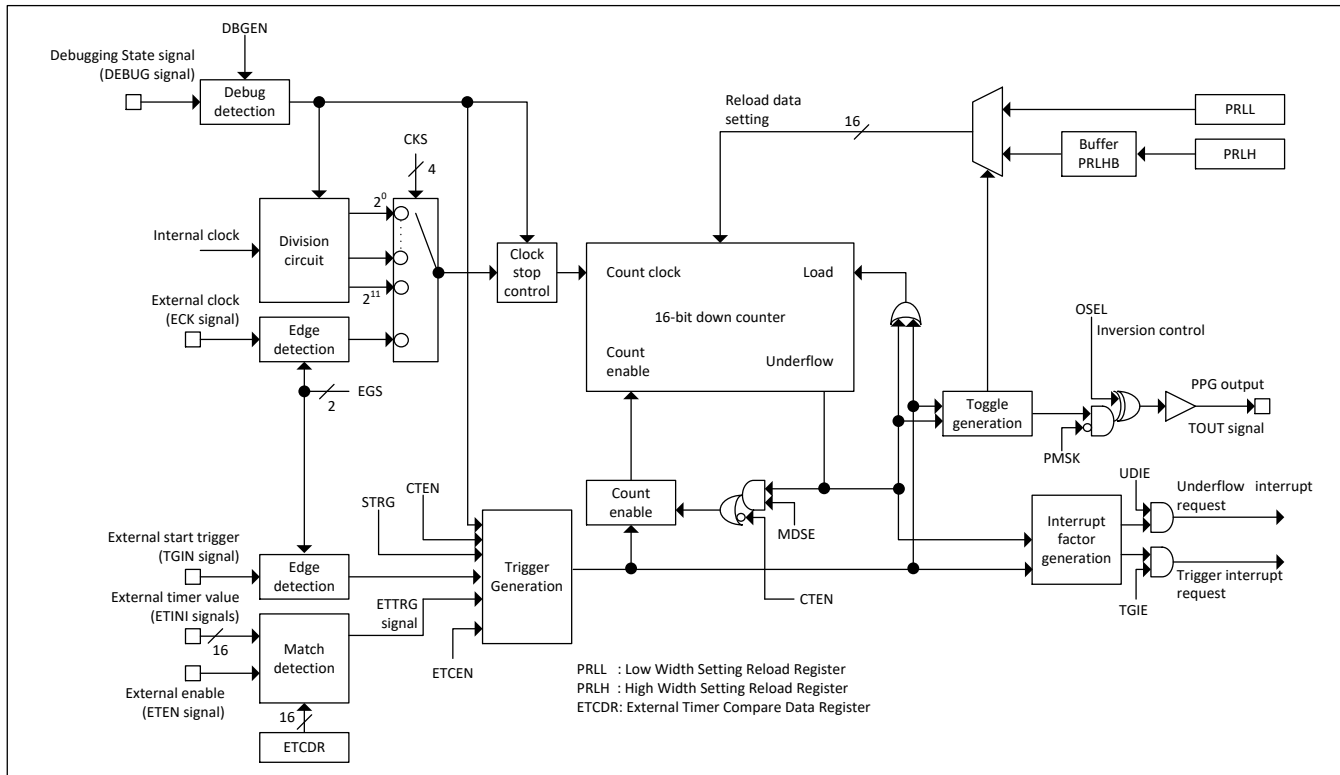
Figure 2-2 Block Diagram of the 16-Bit PPG Timer

Figure 2-3 Block Diagram of the 16/32-Bit Reload Timer (ch1, ch0)

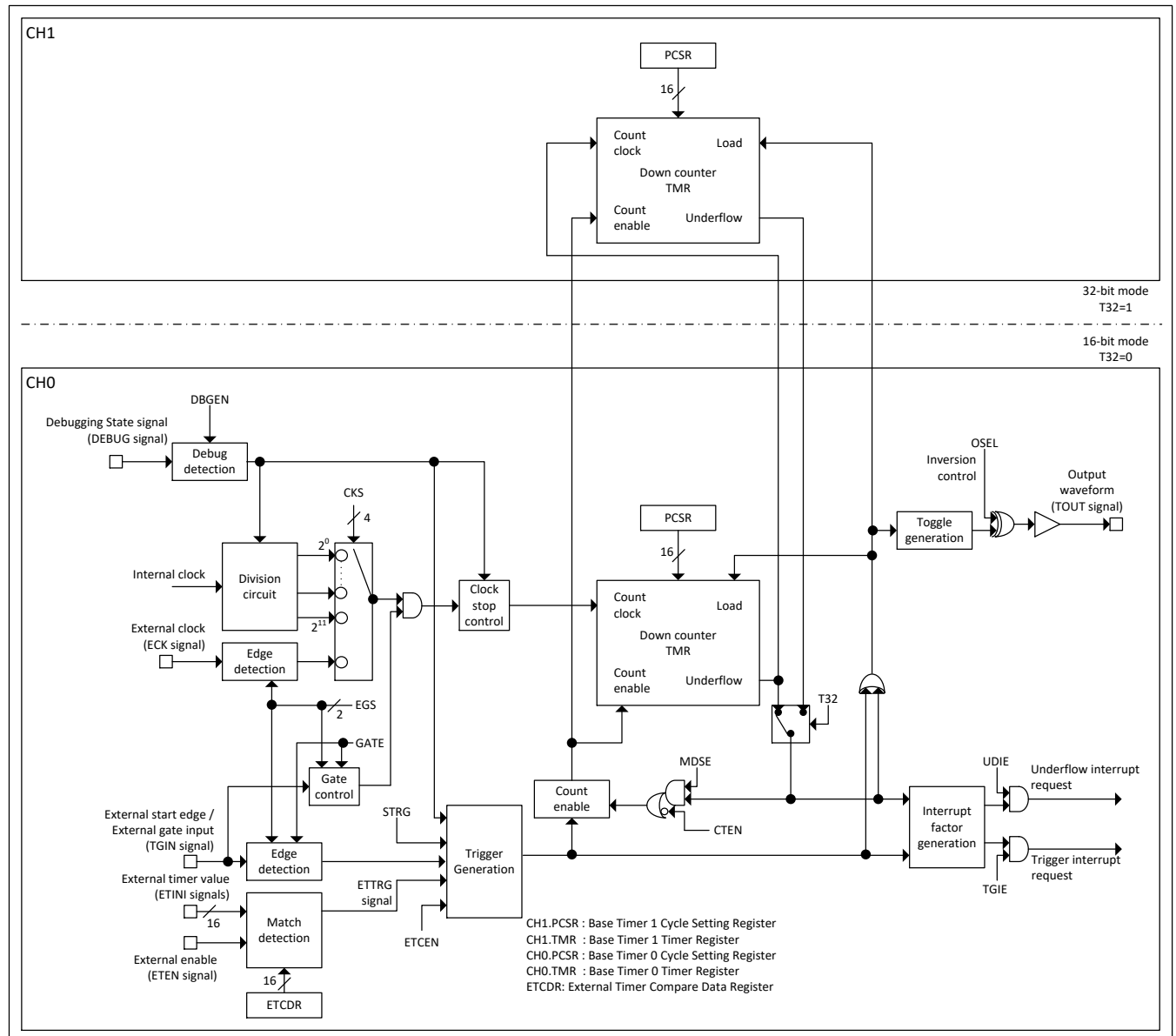
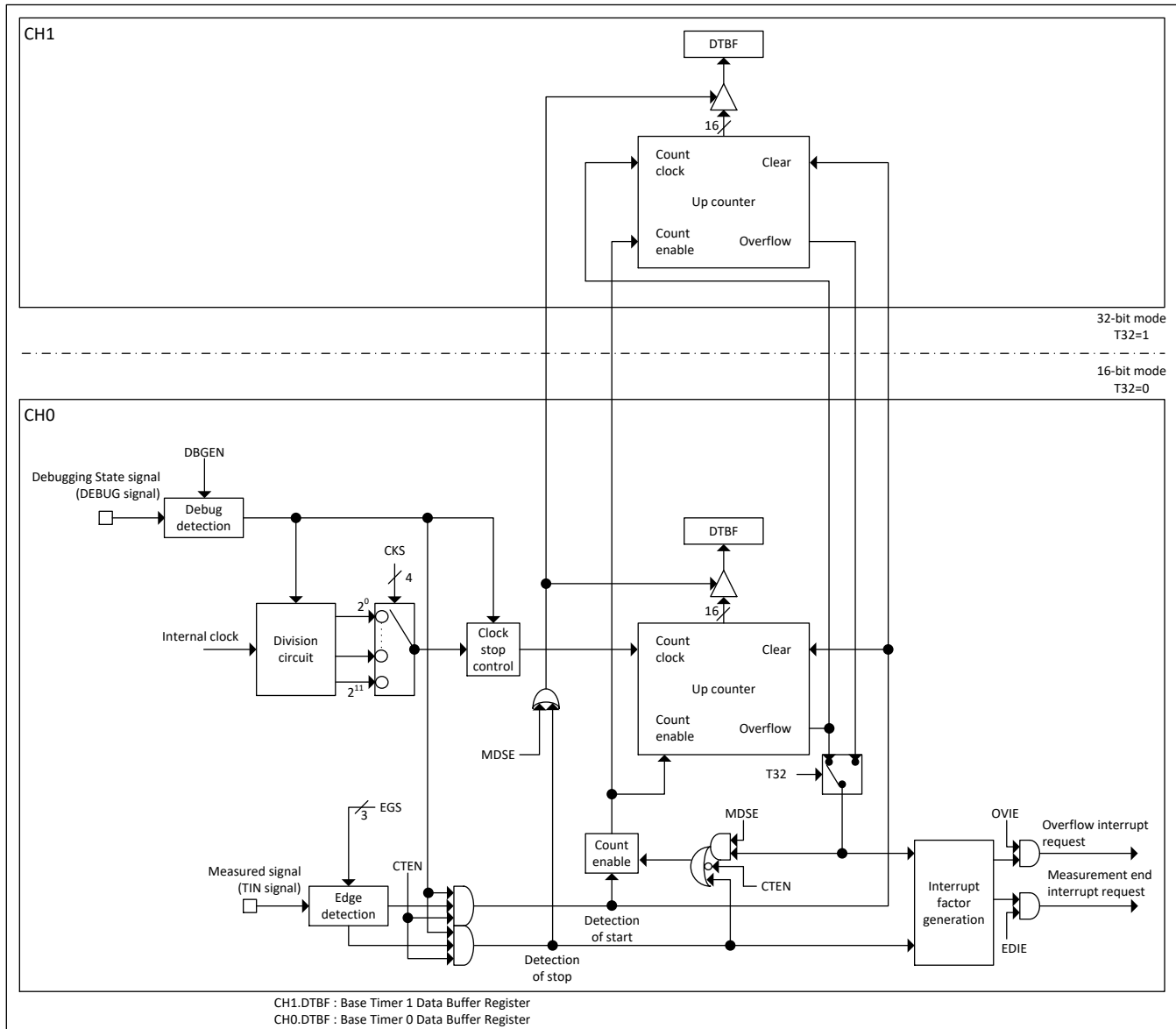


Figure 2-4 Block Diagram of the 16/32-Bit PWC Timer (ch1, ch0)

3. Operations of the Base Timer

This section explains the operations of the Base Timer.

Operations of Base Timer

Reset Mode

Reset mode is the state in which the Base Timer macros have been reset (to the initial values in each register). To use another timer function or switch the T32 bit setting, first enter this mode and then set the other timer function or the T32 bit. However, after a macro reset, it is possible to set a timer function and the T32 bit without entering this mode. If this mode is set for the even-numbered channel when 32-bit mode is set, the odd-numbered channel is reset at the same time, so Reset mode need not be set for the odd-numbered channel.

16-Bit PWM Timer

The 16-bit PWM Timer starts counting down from the set cycle value upon trigger activation. In the beginning the output level is "L". If the 16-bit down counter matches the set value in the duty setting register, the output is inverted to the "H" level. Then, the output is inverted to the "L" level again when the counter underflows. Thus, this timer can generate a waveform with an arbitrary cycle and duty.

16-Bit PPG Timer

The 16-bit PPG Timer starts counting down from the set value in the Low Width Setting Reload Register (PRL) upon trigger activation. In the beginning the output level is "L". The output is inverted to the "H" level when the counter underflows. Subsequently, the counter starts counting down from the set value in the High Width Setting Reload Register (PRLH). The output is inverted to the "L" level when the counter underflows. Thus, this timer can generate a waveform with an arbitrary "L" width and "H" width.

16-Bit Reload Timer

The 16-bit Reload Timer starts counting down from the set cycle value upon trigger activation. An interrupt flag is set to "1" when the 16-bit down counter underflows. The output level is defined by the MDSE bit setting - the polarity of the output is toggled each time an underflow is detected, or, the output is set to "H" when counting starts and switches to "L" when an underflow is detected.

32-Bit Reload Timer

With the same basic operation as the 16-bit Reload Timer, this timer uses two channels, an even-numbered channel and an odd-numbered channel, to operate as a 32-bit Reload Timer. The even-numbered channel performs the lower 16-bit timer operations, and the odd-numbered channel performs the upper 16-bit timer operations. The interrupt controller and output waveform control conform to the settings of only the even-numbered channel. To set a cycle, write it first to the upper register (odd-numbered channel) and then to the lower register (even-numbered channel).

To read the timer value, read it first from the lower register (even-numbered channel) and then from the upper register (odd-numbered channel).

16-Bit PWC Timer

The PWC Timer starts the 16-bit up counter upon detection of the measurement start edge, and stops the counter upon the detection of a measurement end edge. The resulting count value will be stored as the measured pulse width in the Data Buffer Register (DTBF).

32-Bit PWC Timer

With the same basic operation as the 16-bit PWC Timer, this timer uses two channels, an even-numbered channel and an odd-numbered channel, to operate as a 32-bit PWC Timer. The even-numbered channel performs the lower 16-bit count operations, and the odd-numbered channel performs the upper 16-bit count operations. The interrupt controller conforms to the settings of only the even-numbered channel. To read a measurement value or count value, read it first from the lower register (even-numbered channel) and then from the upper register (odd-numbered channel).

4. 32-Bit Mode Operation

The Reload Timer and PWC are capable of 32-bit mode operation using two channels. This section shows the basic functions/operations of the 32-bit mode function.

32-Bit Mode Function

This function realizes the operation of the 32-bit data Reload Timer or 32-bit data PWC Timer by using two Base Timer channels. The value of the timer or counter in operation can also be read when the lower 16-bit timer or counter value of the even-numbered channel is read. This is because the upper 16-bit timer or counter value of the odd-numbered channel is also fetched at the time.

32-Bit Mode Settings

First, reset the state by setting the FMD2 to FMD0 bits in the TMCR register of the even-numbered channel to "000" for Reset mode. Then, in the same way as in 16-bit mode, make Reload Timer or PWC Timer selection and operation settings. To set 32-bit operation mode at this time, write "1" to the T32 bit in the TMCR register. Keep the T32 bit of the odd-numbered channel at "0". There is no need to set the odd-numbered channel to Reset mode. For the Reload Timer, set the upper 16-bit reload value of the 32 bits in the Cycle Setting Register (PCSR) of the odd-numbered channel. Then, set the lower 16-bit reload value in the Cycle Setting Register (PCSR) of the even-numbered channel.

After the writing of the T32 bit, the change to 32-bit operation mode is reflected immediately, so change the settings for both channels while the counter is in a stopped state.

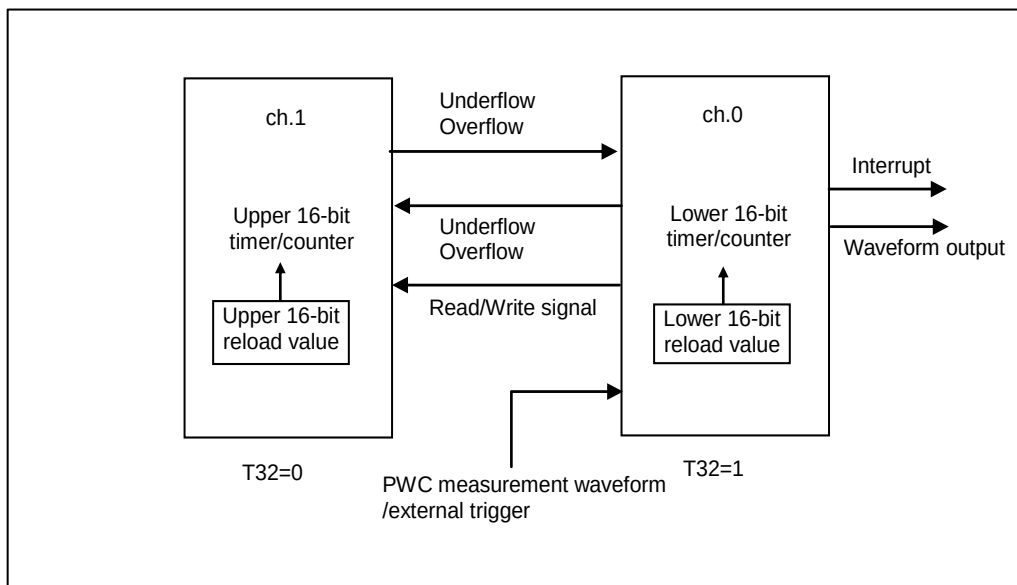
To change from 32-bit mode to 16-bit mode, set the FMD2 to FMD0 bits in the TMCR register of the even-numbered channel to "000" for Reset mode. This resets the states of both the even-numbered and odd-numbered channels. As a result, the settings for 16-bit mode can be made for each of the channels.

32-Bit Mode Operation

After 32-bit mode is set, if the Reload Timer or PWC Timer is started with even-numbered channel control, the even-numbered channel timer/counter performs the lower 16-bit operations. The odd-numbered channel timer/counter performs the upper 16-bit operations.

Operation in 32-bit mode conforms to the settings made for the even-numbered channel. Thus, the settings made for the odd-numbered channel (excluding those in the Cycle Setting Register (PCSR) at the Reload Timer time) are ignored. The timer start, waveform output, and interrupt signals of the even-numbered channel are valid. (The corresponding signals for the odd-numbered channel will be masked to "L".)

Figure 4-1 shows the configuration of ch.0 and ch.1.

Figure 4-1 Configuration of 32-Bit Mode Operation (for ch.0 and ch.1)

5. Debug Mode

If it goes into a Debug mode, operation of the Base Timer can be stopped and debugged.

If all the following conditions are satisfied, it will go into the Debug mode.

- The debug enable bit (DBGEN) of the Base Timer Debug Register (BT_DEBUG) is "1".
- The debug signal (DEBUG) is active.

It becomes the following operation when it goes into the Debug mode.

- The prescaler stop.
- The timer stop.
- The output waveform stop.
 - It holds the output value at the time of the stop.
- The trigger is ignored in PWM Timer, PPG Timer or Reload timer.
- The measurement edge is ignored in PWC Timer.

It becomes the following operation when it restores from the Debug mode.

- The prescaler is resumed from the stopped value.
- The timer is resumed from the stopped value.
- The output waveform resumes the output from the stopped state.

Note:

- *Register access is possible in the Debug mode.*
- *When the processor is in the debug state, the debug signal (DEBUG) becomes active.*
For the definition of debug state, refer to Section 12.8 of the Arm Cortex-R5 Technical Reference Manual.

6. Interrupts from the Base Timer

This section shows a list summarizing the interrupt request flags, interrupt enable bits, and interrupt factors in each function of the Base Timer.

Interrupt Controller Bits and Interrupt Factors of Each Function

Table 6-1 shows the interrupt controller bits and interrupt factors of each function.

Table 6-1 Interrupt Controller Bits and Interrupt Factors in Each Mode

	Status Control Register (STC)			
	Interrupt Request Flag Bit	Interrupt Request Enable Bit	Interrupt Factor	Interrupt Factor Output Signal
PWM Timer Function	UDIR : bit0	UDIE : bit4	Detection of underflow	IRQ0
	DTIR : bit1	DTIE : bit5	Detection of duty match	
	TGIR : bit2	TGIE : bit6	Detection of timer activation trigger	IRQ1
PPG Timer Function	UDIR : bit0	UDIE : bit4	Detection of underflow	IRQ0
	TGIR : bit2	TGIE : bit6	Detection of timer activation trigger	IRQ1
Reload Timer Function	UDIR : bit0	UDIE : bit4	Detection of underflow	IRQ0
	TGIR : bit2	TGIE : bit6	Detection of timer activation trigger	IRQ1
PWC Timer Function	OVIR : bit0	OVIE : bit4	Detection of overflow	IRQ0
	EDIR : bit2	EDIE : bit6	Detection of measurement end	IRQ1

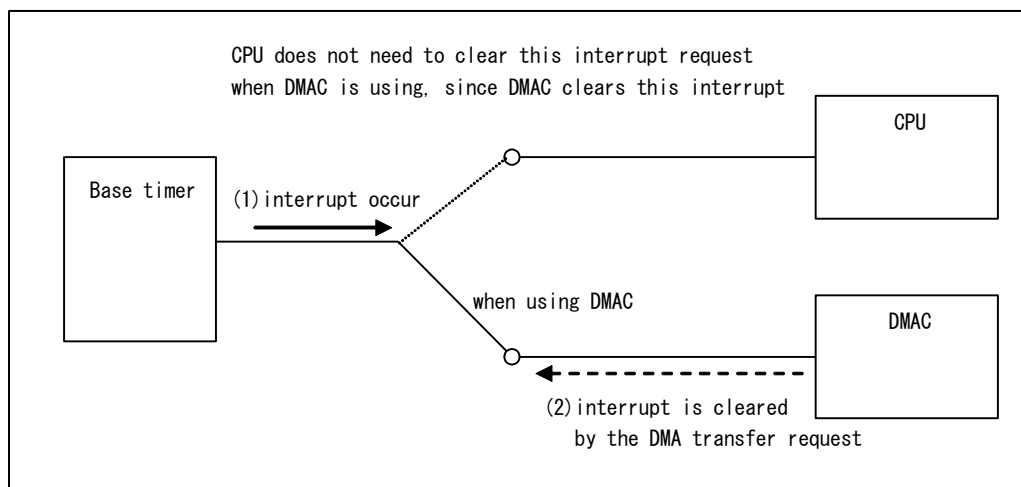
7. Start of DMA Controller (DMAC)

The generation of a Base Timer interrupt request can be used to start the DMAC.

DMA Transfer Operation Using Base Timer Interrupt Factor

The generation of a Base Timer interrupt factor can be used to start the DMAC. Figure 7-1 shows an overview of DMAC start with the Base Timer.

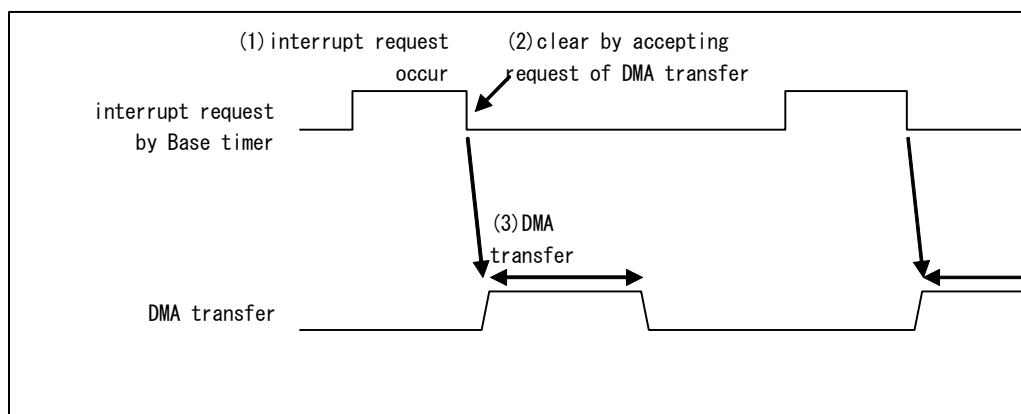
Figure 7-1 Overview of DMAC Start with the Base Timer



Configure the DMAC before starting it with the Base Timer. For details on DMAC settings, see the chapter of "DMA Controller" in Traveo™ Platform hardware manual and "6. Interrupts from the Base Timer" on this manual.

Figure 7-2 shows an example of a DMA transfer operation with a Base Timer interrupt request.

Figure 7-2 DMA Transfer Operation Example



8. Registers of the Base Timer

This section lists the registers of each mode of the Base Timer.

List of Registers when 16-Bit PWM Timer is Selected

Table 8-1 List of Registers When the 16-Bit PWM Timer Is Selected

Abbreviated Register Name	Register Name	Reference
TMCR	Timer Control Register	10.1.9
TMCR2	Timer Control Register 2	10.1.9
STC	Status Control Register	10.1.9
STCC	Status Control Clear Register	10.1.9
STCS	Status Control Set Register	10.1.9
PCSR	PWM Cycle Setting Register	10.1.10
PDUT	PWM Duty Setting Register	10.1.11
TMR	Timer Register	10.1.12
PSDR	Start Delay Value Setting Register	10.1.13
ADTR	ADC Trigger Value Setting Register	10.1.14
BT_DEBUG	Base Timer Debug Register	10.1.15
ETCDR	External Timer Compare Data Register	10.1.16

List of Registers when 16-Bit PPG Timer is Selected

Table 8-2 List of Registers When the 16-Bit PPG Timer Is Selected

Abbreviated Register Name	Register Name	Reference
TMCR	Timer Control Register	10.2.7
TMCR2	Timer Control Register 2	10.2.7
STC	Status Control Register	10.2.7
STCC	Status Control Clear Register	10.2.7
STCS	Status Control Set Register	10.2.7
PRLL	Low Width Setting Reload Register	10.2.8
PRLH	High Width Setting Reload Register	10.2.9
TMR	Timer Register	10.2.10
BT_DEBUG	Base Timer Debug Register	10.2.11
ETCDR	External Timer Compare Data Register	10.2.12

List of Registers when Reload Timer is Selected

Table 8-3 List of Registers When the Reload Timer Is Selected

Abbreviated Register Name	Register Name	Reference
TMCR	Timer Control Register	10.3.4
TMCR2	Timer Control Register 2	10.3.4
STC	Status Control Register	10.3.4
STCC	Status Control Clear Register	10.3.4

Abbreviated Register Name	Register Name	Reference
STCS	Status Control Set Register	10.3.4
PCSR	Cycle Setting Register	10.3.5
TMR	Timer Register	10.3.6
BT_DEBUG	Base Timer Debug Register	10.2.11
ETCDR	External Timer Compare Data Register	10.2.12

List of Registers when PWC Timer is Selected

Table 8-4 List of Registers When the PWC Timer Is Selected

Abbreviated Register Name	Register Name	Reference
TMCR	Timer Control Register	10.4.2
TMCR2	Timer Control Register 2	10.4.2
STC	Status Control Register	10.4.2
STCC	Status Control Clear Register	10.4.2
STCS	Status Control Set Register	10.4.2
DTBF	Data Buffer Register	10.4.3
BT_DEBUG	Base Timer Debug Register	10.2.11

Table 8-5 Offset Addresses

CH No.	Offset_Address (Common PERI #1)	CH No.	Offset_Address (Common PERI #1)	CH No.	Offset_Address (Common PERI #1)
24	0x0084_6000	12	0x0088_8000	0	0x0080_8000
25	0x0084_6400	13	0x0088_8400	1	0x0080_8400
26	0x0084_6800	14	0x0088_8800	2	0x0080_8800
27	0x0084_6C00	15	0x0088_8C00	3	0x0080_8C00
28	0x0084_7000	16	0x0088_9000	4	0x0080_9000
29	0x0084_7400	17	0x0088_9400	5	0x0080_9400
30	0x0084_7800	18	0x0088_9800	6	0x0080_9800
31	0x0084_7C00	19	0x0088_9C00	7	0x0080_9C00
32	0x0084_8000	20	0x0088_A000	8	0x0080_A000
33	0x0084_8400	21	0x0088_A400	9	0x0080_A400
34	0x0084_8800	22	0x0088_A800	10	0x0080_A800
35	0x0084_8C00	23	0x0088_AC00	11	0x0080_AC00

CH No.	Offset_Address (Common PERI #1)	CH No.	Offset_Address (Common PERI #1)	CH No.	Offset_Address (Common PERI #1)
60	0x0084_F000	48	0x0084_C000	36	0x0084_9000
61	0x0084_F400	49	0x0084_C400	37	0x0084_9400
62	0x0084_F800	50	0x0084_C800	38	0x0084_9800
63	0x0084_FC00	51	0x0084_CC00	39	0x0084_9C00
-	-	52	0x0084_D000	40	0x0084_A000
-	-	53	0x0084_D400	41	0x0084_A400
-	-	54	0x0084_D800	42	0x0084_A800
-	-	55	0x0084_DC00	43	0x0084_AC00
-	-	56	0x0084_E000	44	0x0084_B000
-	-	57	0x0084_E400	45	0x0084_B400
-	-	58	0x0084_E800	46	0x0084_B800
-	-	59	0x0084_EC00	47	0x0084_BC00

Table 8-6 Register Map (Channel No.: 0) (12) (24) (36) (48) (60)

Offset	Register Name/Initial Value			
	+3	+2	+1	+0
0x0000_0000	Reserved 00000000_00000000		BTxx_PCSR/ BTxx_PCSR/ BTxx_PRLL / Reserved XXXXXXXX_XXXXXXXX	
0x0000_0004	Reserved 00000000_00000000		Reserved/ BTxx_PDUT/ BTxx_PRLH/ BTxx_DTBF XXXXXXXX_XXXXXXXX / 00000000_00000000 (BTxx_DTBF)	
0x0000_0008	Reserved/ BTxx_TMR/ Reserved/ Reserved 00000000_00000000		BTxx_TMR/ BTxx_TMR/ BTxx_TMR/ Reserved 00000000_00000000 XXXXXXXX_XXXXXXXX*1	
0x0000_000C	Reserved 00000000_00000000		BTxx_TMCR 00000000_00000000	
0x0000_0010	Reserved 00000000_00000000		BTxx_TMCR2 00000000	BTxx_STC 00000000
0x0000_0014	Reserved 00000000_00000000		Reserved 00000000	BTxx_STCC 00000000
0x0000_0018	Reserved 00000000_00000000		Reserved 00000000	BTxx_STCS 00000000
0x0000_001C	Reserved 00000000_00000000		Reserved/ BTxx_PSDR/ Reserved/ Reserved 00000000_00000000	
0x0000_0020	Reserved 00000000_00000000		Reserved/ BTxx_ADTR/ Reserved/ Reserved 00000000_00000000	

Offset	Register Name/Initial Value			
	+3	+2	+1	+0
0x0000_0024	Reserved 00000000_00000000		BT_DEBUG 00000000	
0x0000_0028	Reserved 00000000_00000000_00000000_00000000			
0x0000_002C	Reserved 00000000_00000000		ETCDR/ ETCDR / ETCDR/ Reserved 01111111_11111111 / 00000000_00000000 (Reserved)	
0x0000_0030	Reserved 11111111_11111111		Reserved 11111111	BT_BTSELmn*2 11110000
0x0000_0034	Reserved 11111111_11111111		BT_BTSSSRn*3 11111111_11111111	
0x0000_0038	Reserved 11111111_11111111		BT_BTTRRn*3 11110000_00000000	

*1 The initial value is XXXXXXXX_XXXXXXX only during reload timer operation.

*2 mn = 01, 1213, 2425, 3637, 4849 and 6061

*3 n = 0, 12, 24, 36, 48 and 60

The "****/****/****/****" expression in each table corresponds to the reload/PWM/PPG/PWC timer, respectively.

Table 8-7 Register Map (Channel No.: 1, 3, 5, 7, 9, and 11) (13, 15, 17, 19, 21, and 23) (25, 27, 29, 31, 33, and 35) (37, 39, 41, 43, 45, and 47) (49, 51, 53, 55, 57, and 59) (61 and 63)

Offset	Register Name/Initial Value			
	+3	+2	+1	+0
0x0000_0000	Reserved 00000000_00000000		BTxx_PCSR/ BTxx_PCSR/ BTxx_PRL / Reserved XXXXXXXX_XXXXXXXX	
0x0000_0004	Reserved 00000000_00000000		Reserved/ BTxx_PDUT/ BTxx_PRLH/ BTxx_DTB XXXXXXXX_XXXXXXXX / 00000000_00000000 (BTxx_DTB)	
0x0000_0008	Reserved/ BTxx_TMR/ Reserved/ Reserved 00000000_00000000		BTxx_TMR/ BTxx_TMR/ BTxx_TMR / Reserved 00000000_00000000 / XXXXXXXX_XXXXXXX*1	
0x0000_000C	Reserved 00000000_00000000		BTxx_TMCR 00000000_00000000	
0x0000_0010	Reserved 00000000_00000000		BTxx_TMCR2 00000000	BTxx_STC 00000000

Offset	Register Name/Initial Value			
	+3	+2	+1	+0
0x0000_0014	Reserved 00000000_00000000		Reserved 00000000	BTxx_STCC 00000000
0x0000_0018	Reserved 00000000_00000000		Reserved 00000000	BTxx_STCS 00000000
0x0000_001C	Reserved 00000000_00000000		Reserved/ BTxx_PSDR/ Reserved/ Reserved 00000000_00000000	
0x0000_0020	Reserved 00000000_00000000		Reserved/ BTxx_ADTR/ Reserved/ Reserved 00000000_00000000	
0x0000_0024	Reserved 00000000_00000000		BT_DEBUG 00000000	
0x0000_0028	Reserved 00000000_00000000_00000000_00000000			
0x0000_002C	Reserved 00000000_00000000		ETCDR/ ETCDR / ETCDR/ Reserved 01111111_11111111 / 00000000_00000000 (Reserved)	

*1 The initial value is XXXXXXXX_XXXXXXX only during reload timer operation.

The "*/*/*/*/" expression in each table corresponds to the reload/PWM/PPG/PWC timer, respectively.

Table 8-8 Register Map (Channel No.: 2, 4, 6, 8, and 10) (14, 16, 18, 20, and 22) (26, 28, 30, 32, and 34) (38, 40, 42, 44, and 46) (50, 52, 54, 56, and 58) (62)

Offset	Register Name/Initial Value			
	+3	+2	+1	+0
0x0000_0000	Reserved 00000000_00000000		BTxx_PCSR/ BTxx_PCSR/ BTxx_PRL / Reserved XXXXXXXX_XXXXXXXX	
0x0000_0004	Reserved 00000000_00000000		Reserved/ BTxx_PDUT/ BTxx_PRLH/ BTxx_DTB XXXXXXXX_XXXXXXXX / 00000000_00000000 (BTxx_DTB)	
0x0000_0008	Reserved/ BTxx_TMR/ Reserved/ Reserved 00000000_00000000		BTxx_TMR/ BTxx_TMR/ BTxx_TMR / Reserved 00000000_00000000 / XXXXXXXX_XXXXXXX*1	
0x0000_000C	Reserved 00000000_00000000		BTxx_TMCR 00000000_00000000	
0x0000_0010	Reserved 00000000_00000000		BTxx_TMCR2 00000000	BTxx_STC 00000000
0x0000_0014	Reserved 00000000_00000000		Reserved 00000000	BTxx_STCC 00000000
0x0000_0018	Reserved 00000000_00000000		Reserved 00000000	BTxx_STCS 00000000
0x0000_001C	Reserved 00000000_00000000		Reserved/ BTxx_PSDR/ Reserved/ Reserved 00000000_00000000	
0x0000_0020	Reserved 00000000_00000000		Reserved/ BTxx_ADTR/ Reserved/ Reserved 00000000_00000000	
0x0000_0024	Reserved 00000000_00000000		BT_DEBUG 00000000	
0x0000_0028	Reserved 00000000_00000000_00000000_00000000			
0x0000_002C	Reserved 00000000_00000000		ETCDR/ ETCDR / ETCDR/ Reserved 01111111_11111111 / 00000000_00000000 (Reserved)	
0x0000_0030	Reserved 11111111_11111111		Reserved 11111111	BT_BTSELmn*2 11110000

*1 The initial value is XXXXXXXX_XXXXXXX only during reload timer operation.

*2 mn = 23, 45, 67, 89, 1011, 1415, 1617, 1819, 2021, 2223, 2627, 2829, 3031, 3233, 3435, 3839, 4041, 4243, 4445, 4647, 5051, 5253, 5455, 5657, 5859 and 6263

The "****/****/****/****" expression in each table corresponds to the reload/PWM/PPG/PWC timer, respectively.

9. Notes on Using the Base Timer

This section explains precautions on use of the Base Timer.

Notes to observe when accessing register

Status Control Register (STC) Access

- To clear a specific bit in this register, write "1" to the corresponding bit in the Status Control Clear Register (STCC).
- To set a specific bit in this register, write "1" to the corresponding bit in the Status Control Set Register (STCS).
- Direct writing to this register is possible only during writing to all bits.

Notes to observe on configuration using program, common to use of timers

- Rewriting of the following bits in the TMCR2 register and TMCR register during operation is prohibited. Be sure that such rewriting is done either before the timer starts or after it stops.

Bit	Bit Name	Description
[TMCR2 bit0], [TMCR bit14,13,12]	CKS3 to CKS0	Clock selection bits
[bit10,9,8]	EGS2, EGS1, EGS0	Measurement edge selection bits
[bit7]	T32	32-bit timer selection bit (when the Reload Timer and PWC function are selected)
[bit6,5,4]	FMD2 to FMD0	Timer function selection bits
[bit2]	MDSE	Measurement mode (single/continuous) selection bit

- All the registers of the Base Timer are initialized when the FMD2 to FMD0 bits in the TMCR register are set to "000" for Reset mode. For this reason, all the registers must be reconfigured.
- The settings for bits other than the FMD2 to FMD0 bits in the TMCR register are ignored and initialized when the FMD2 to FMD0 bits in the TMCR register are set to "000" for Reset mode.

Notes on using the 16-bit PWM/PPG/Reload Timer

- If the interrupt request flag set timing and clear timing overlap, the flag set has priority, and the clear operation is disabled.
- If the load timing and count timing overlap, the load operation has priority for the down counter.
- After configuring the timer function with the FMD2 to FMD0 bits in the TMCR register, set the cycle, duty, "H" width, and "L" width.
- If the Base Timer is configured in one-shot mode and is restarted when count end is detected, the counter will reload the count value and restart.

Notes on using the PWC Timer

- If "1" is written to the count start enable bit (CTEN), the counter is cleared. Thus, any data in the counter before the start is enabled is invalid.
- If the PWC mode setting (FMD2 to FMD0 = "100") and the measurement start setting (CTEN="1") are set simultaneously after a system reset assertion or upon leaving Reset mode, the PWC Timer operation may vary due to the state of the immediately preceding measurement signal.
- When operating in continuous measurement mode, if a measurement start edge is detected at the same time that the Base Timer has been restarted, the timer starts counting immediately from 0x0001.
- If a restart is performed after a count operation begins, operations such as the following may occur, depending on the timing the restart has been performed.
 - For a restart at the same time as a measurement end edge in pulse-width single measurement mode

The restart is performed and the measurement start edge wait state begins, but the measurement end flag (EDIR) is set to "1".

- For a restart at the same time as a measurement end edge in pulse-width continuous measurement mode

The restart is performed and the measurement start edge wait state begins, but the measurement end flag (EDIR) is set to "1" and the measurement results at that point are transferred to DTBF.

Note the operation of the flag when using the interrupt controller, etc. at the restart time during operation as described above.

10. Base Timer Description by Function Mode

This section explains each function of the Base Timer.

Functions of the Base Timer

10.1 PWM Timer Function

10.2 PPG Timer Function

10.3 Reload Timer Function

10.4 PWC Timer Function

10.1. PWM Timer Function

Only one of the following timer functions can be selected for the Base Timer in the FMD2 to FMD0 bit settings in the Timer Control Register (TMCR): 16-bit PWM Timer, 16-bit PPG Timer, 16/32-bit Reload Timer, and 16/32-bit PWC Timer. This section explains the timer function with the PWM setting.

10.1.1 16-Bit PWM Timer Operation

10.1.2 One-Shot Operation

10.1.3 Start Delay Function

10.1.4 ADC Trigger Output Timing

10.1.5 External Timer Match Starting

10.1.6 Interrupt Factors and Timing Chart

10.1.7 Output Waveform

10.1.9 Timer Control Registers (TMCR, TMCR2), Status Control Register (STC), Status Control Clear Register (STCC), and Status Control Set Register (STCS)

10.1.10 PWM Cycle Setting Register (PCSR)

10.1.11 PWM Duty Setting Register (PDUT)

10.1.12 Timer Register (TMR)

10.1.13 Start Delay Value Setting Register (PSDR)

10.1.14 ADC Trigger Value Setting Register (ADTR)

10.1.15 Base Timer Debug Register (BT_DEBUG)

10.1.16 External Timer Compare Data Register (ETCDR)

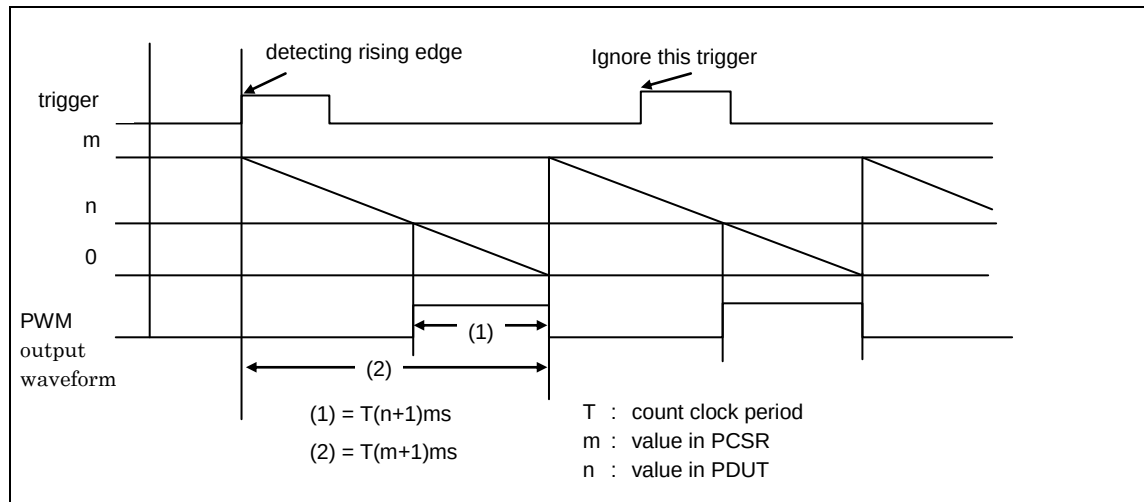
10.1.1. 16-Bit PWM Timer Operation

In PWM operation, waveforms of the set cycle can be output either singly or continuously upon the detection of a trigger. The cycle of the output pulse can be controlled through PCSR value changes. The duty ratio can be controlled through PDUT value changes. After writing data to PCSR, be sure to write to PDUT.

Continuous Operation

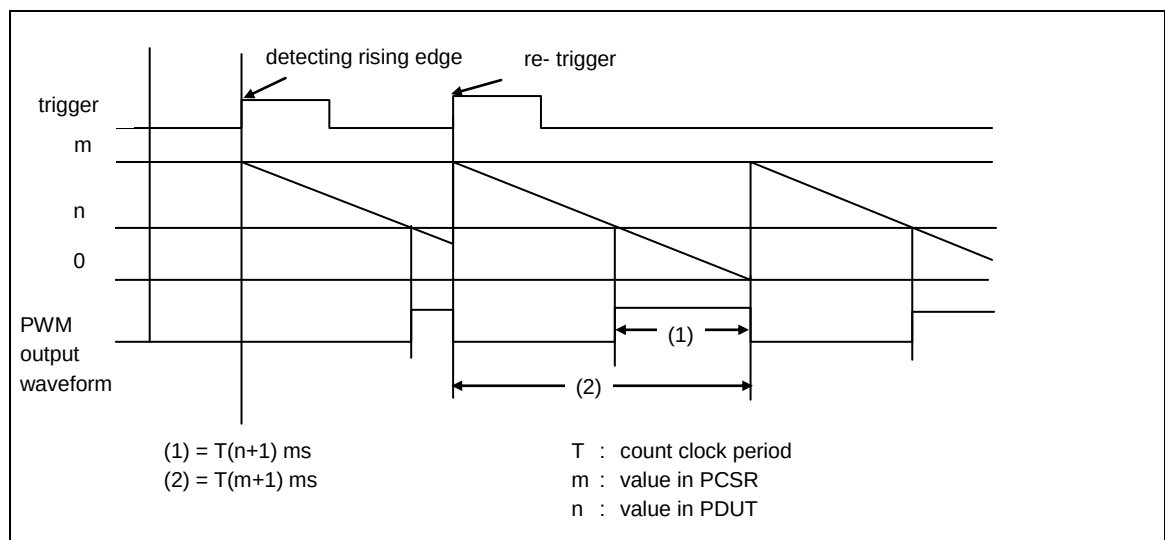
When Restart is Disabled (RTGEN="0")

Figure 10-1 PWM Operation Timing Chart (When Restart Is Disabled)



When Restart is Enabled (RTGEN="1")

Figure 10-2 PWM Operation Timing Chart (When Restart Is Enabled)



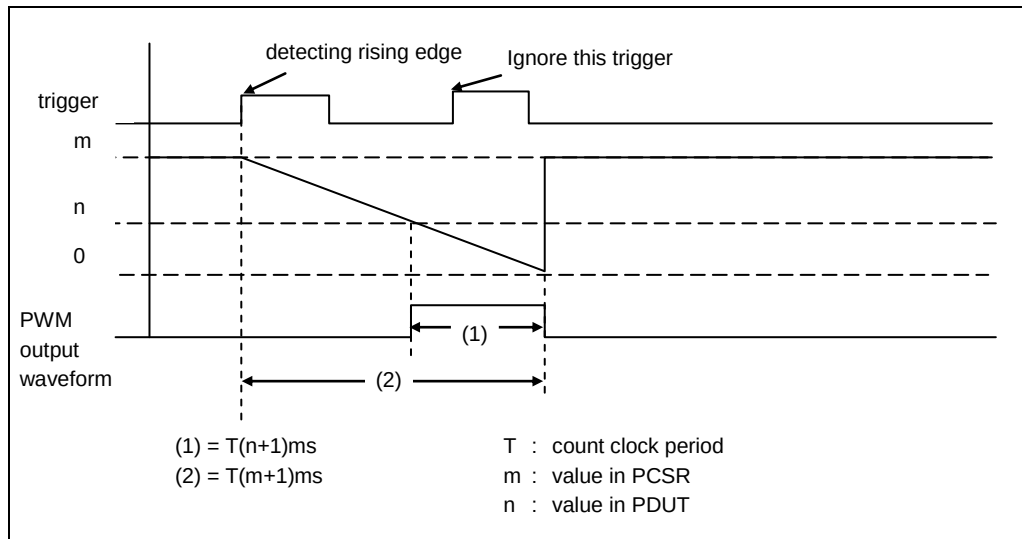
10.1.2. One-Shot Operation

In one-shot operation, a trigger can cause the output of a single pulse of any width. If restart is enabled, the counter is reloaded when an edge is detected during operation.

One-Shot Operation

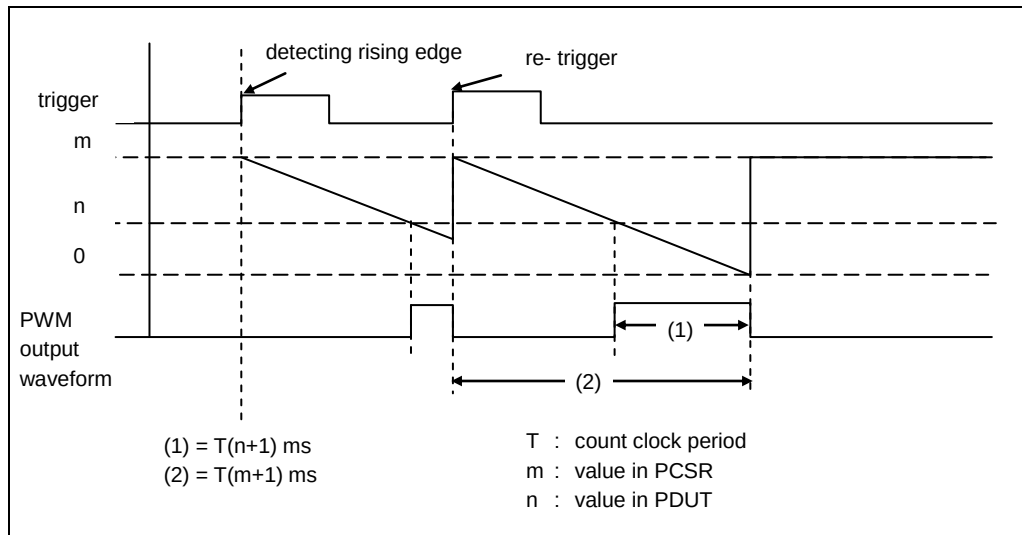
When Restart is Disabled (RTGEN="0")

Figure 10-3 One-Shot Operation Timing Chart (Trigger Restart Disabled)



When Restart is Enabled (RTGEN="1")

Figure 10-4 One-Shot Operation Timing Chart (Trigger Restart Enabled)



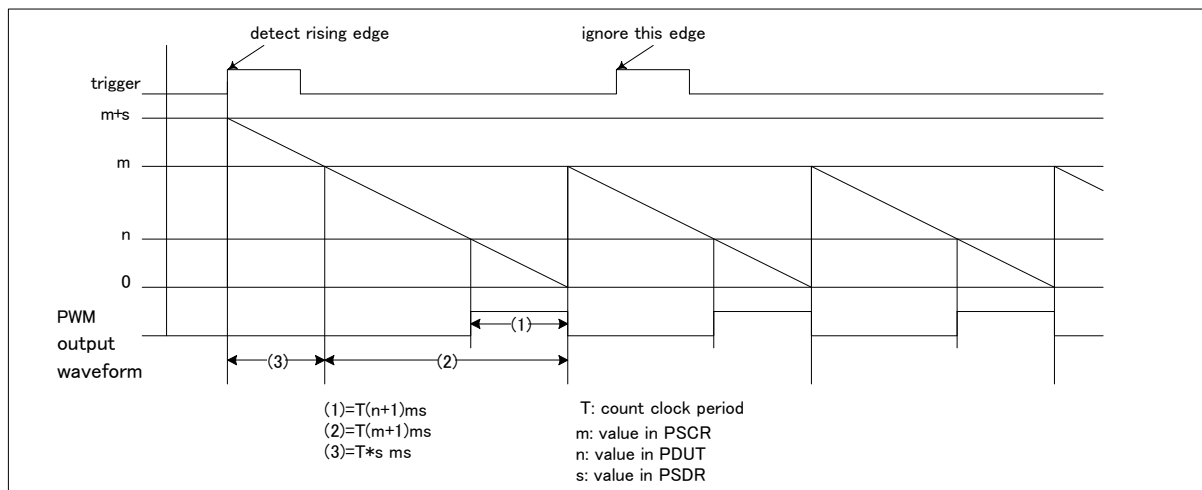
10.1.3. Start Delay Function

The start delay function can delay the time when PWM control starts after a trigger input.

Start Delay Operation in Continuous Operation

When Restart is Disabled (RTGEN="0")

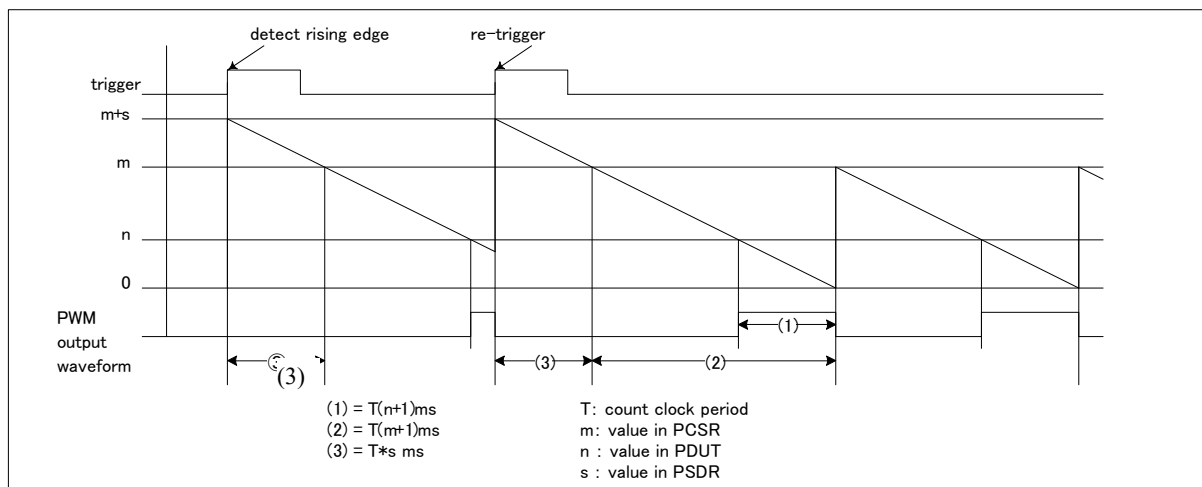
Figure 10-5 Start Delay Operation in Continuous Operation (Trigger Restart Disabled)



No PWM waveform is output during the start delay period ((3) above).

When Restart is Enabled (RTGEN="1")

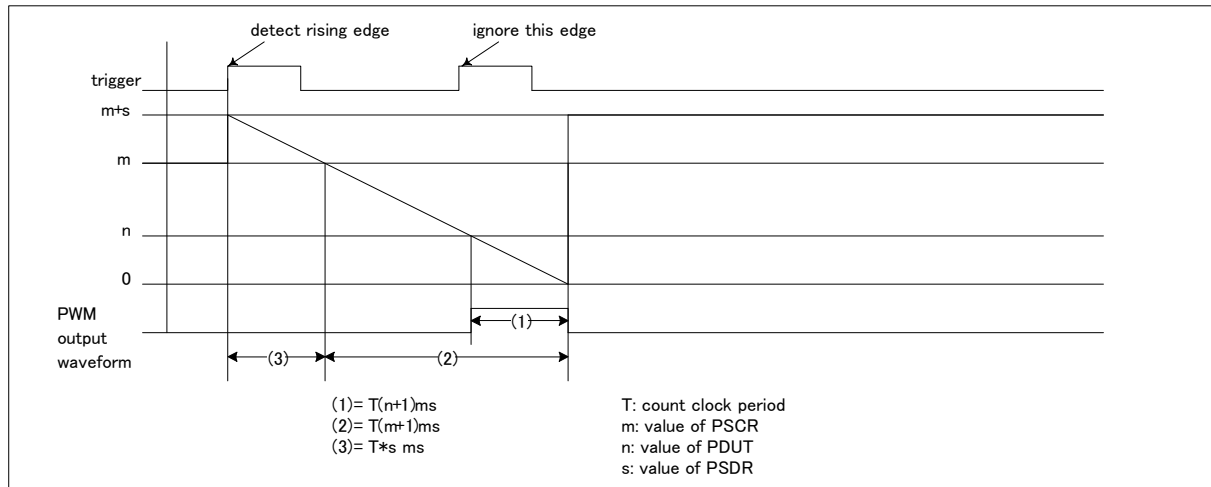
Figure 10-6 Start Delay Operation in Continuous Operation (Trigger Restart Enabled)



No PWM waveform is output during the start delay period ((3) above).

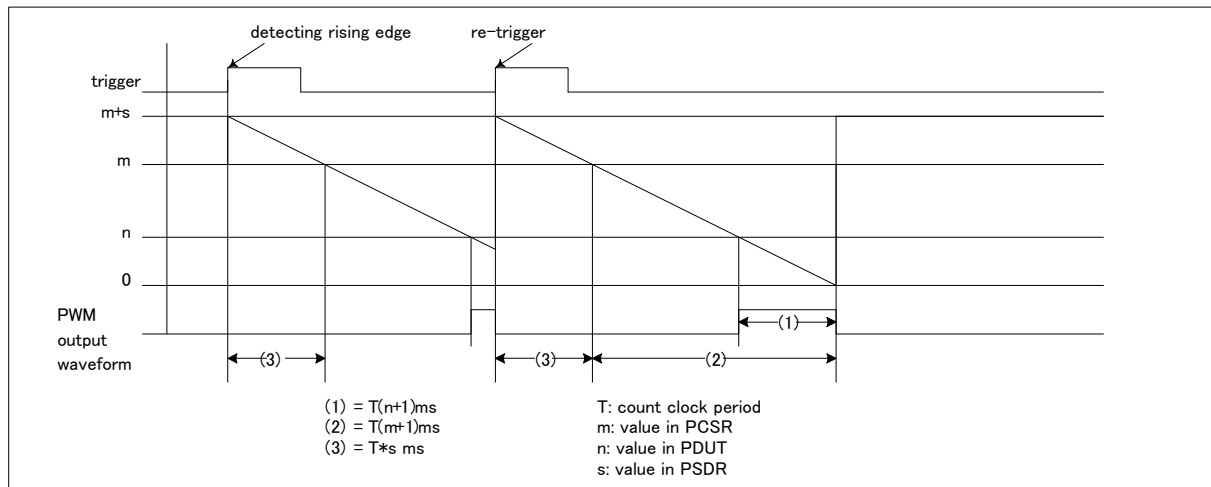
Start Delay Operation in One-Shot Operation

When Restart is Disabled (RTGEN="0")

Figure 10-7 Start Delay Operation in One-Shot Operation (Trigger Restart Disabled)


No PWM waveform is output during the start delay period ((3) above).

When Restart is Enabled (RTGEN="1")

Figure 10-8 Start Delay Operation in One-Shot Operation (Trigger Restart Enabled)


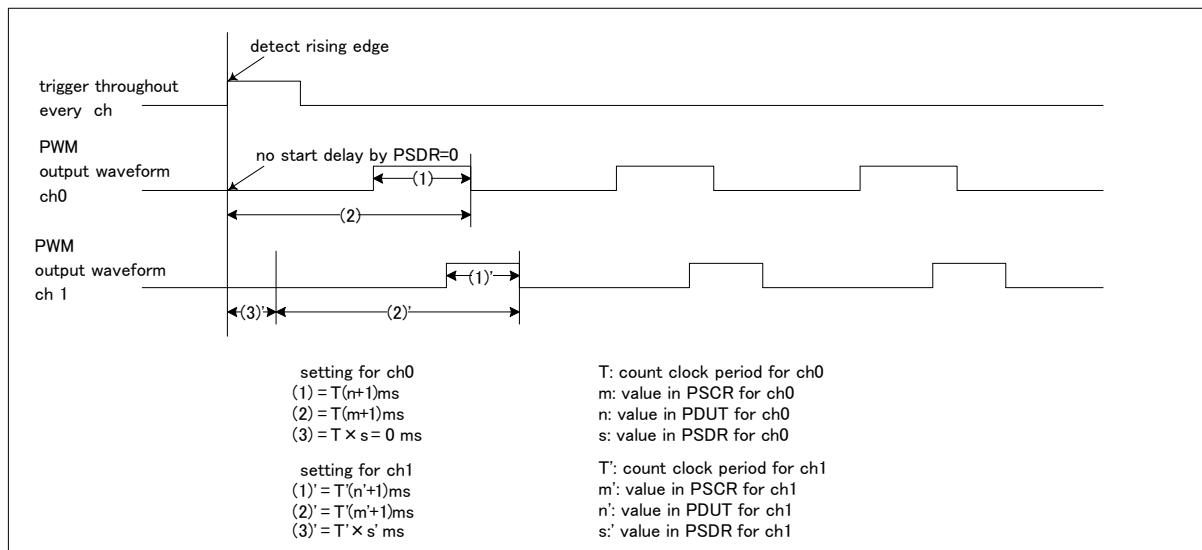
No PWM waveform is output during the start delay period ((3) above).

Start Delay Operation with Multiple Channels interlocked

The trigger can be controlled to interlock several channels in a specific phase relationship.

When Restart is Disabled (RTGEN="0")

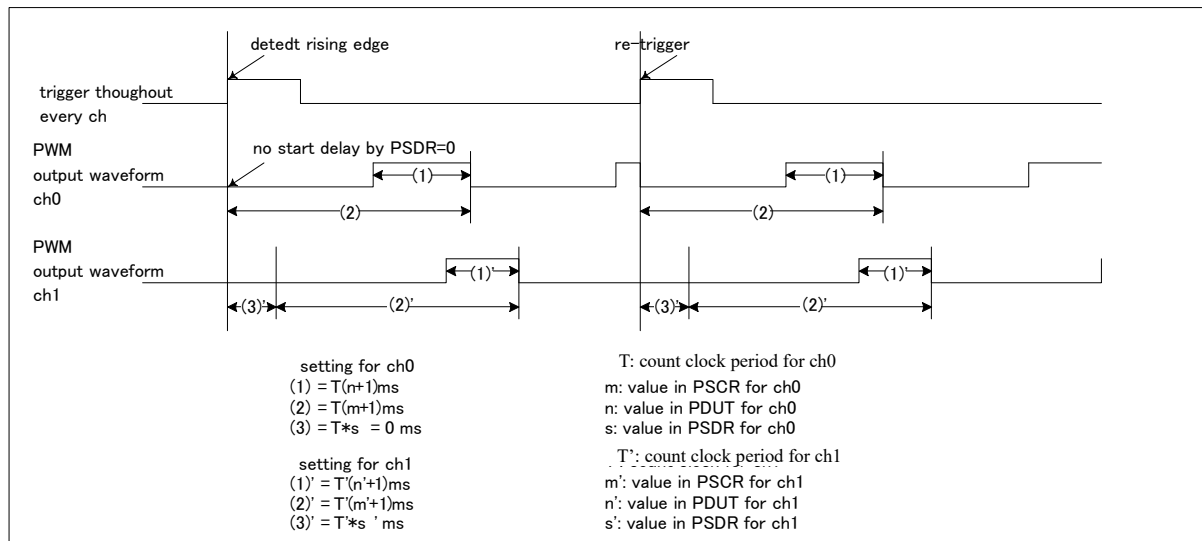
Figure 10-9 Start Delay Operation in Continuous Operation with Multiple Channels Interlocked (Trigger Restart Disabled)



No PWM waveform is output during the start delay period ((3) above).

When Restart is Enabled (RTGEN="1")

Figure 10-10 Start Delay Operation in Continuous Operation with Multiple Channels Interlocked (Trigger Restart Enabled)



No PWM waveform is output during the start delay period ((3) above).

10.1.4. ADC Trigger Output Timing

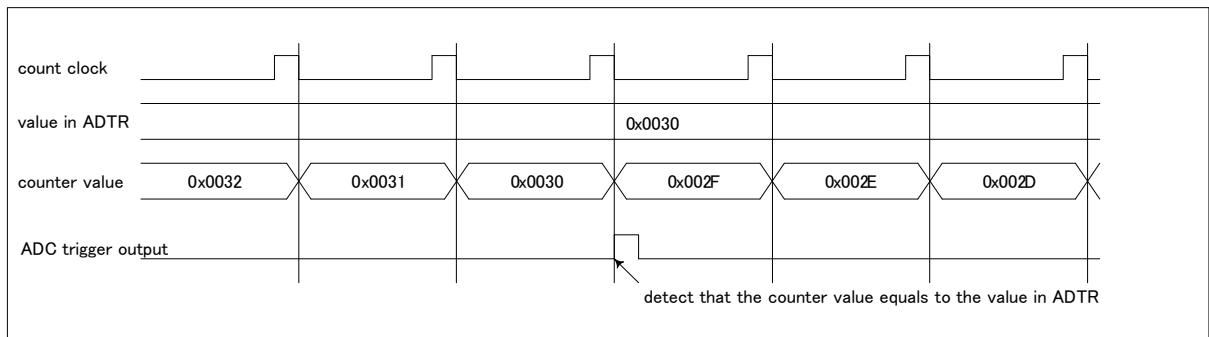
This section explains the ADC trigger output timing.

ADC Trigger Output Timing

ADC trigger is output when the 16-bit down counter is compared with the ADTR register and they match.

Figure 10-11 shows a timing chart of ADC trigger output when ADTR is 0x0030.

Figure 10-11 Timing Chart of ADC Trigger Output



10.1.5. External Timer Match Starting

If the external timer match starting function is used, the 16/17-bit down counter can start in synchronization with an external timer.

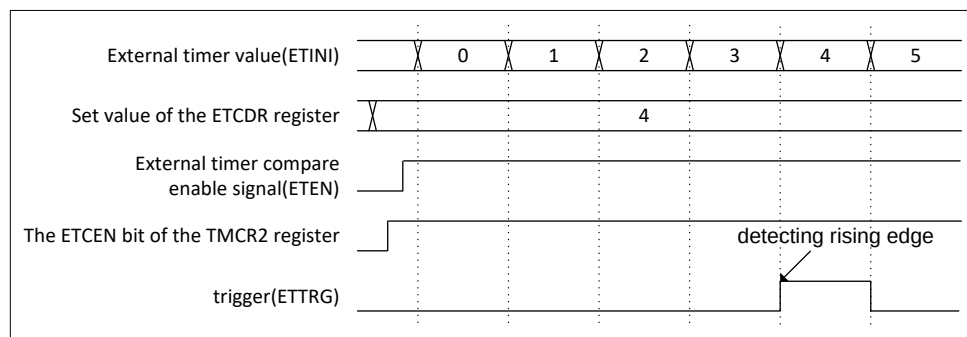
If all the following conditions are satisfied, starting by an external timer is performed.

- The CTEN bit of the TMCR register is "1".
- The ETCEN bit of the TMCR2 register is "1".
- The external timer compare enable signal (ETEN) is active.

When timer is running, the restart by the external timer match starting does not occur. If performing external timer match starting again, perform the following processings.

1. The CTEN bit of the TMCR register is set to "0".
2. The CTEN bit of the TMCR register is set to "1" again.

Figure 10-12 Example of External Timer Match Starting Operation (ETCDR=4)



10.1.6. Interrupt Factors and Timing Chart

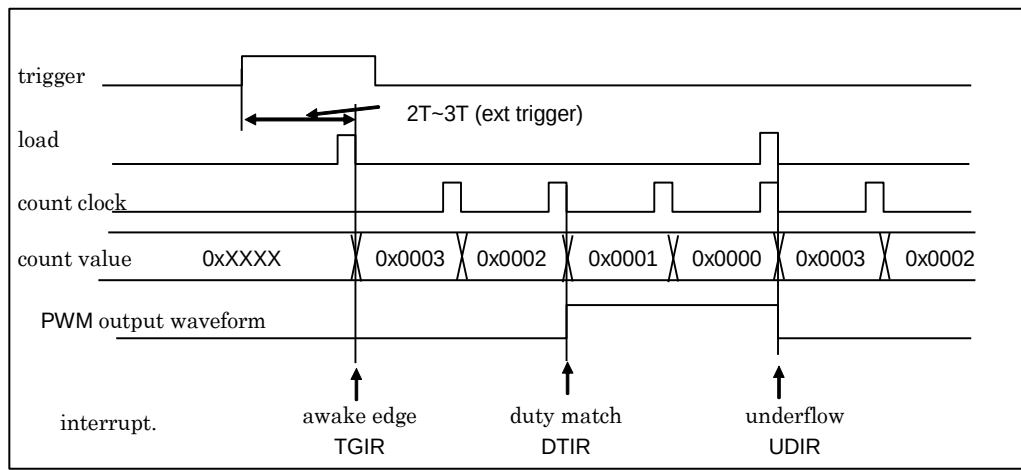
This section shows interrupt factors and a timing chart.

Interrupt Factors and Timing Chart (PWM Output: Normal Polarity)

The time required for a counter value to be loaded following the input of a trigger is, for software triggers T, and for external triggers 2T to 3T (T: internal clock cycle).

Figure 10-13 shows the interrupt factors and a timing chart where the cycle setting value is 3 and the duty value is 1.

Figure 10-13 PWM Timer Interrupt Factors and Timing Chart



10.1.7. Output Waveform

This section shows PWM output.

Output methods for All "L" or All "H" in PWM Output

Figure 10-14 shows an output method where the PWM output is all "L". Figure 10-15 shows an output method where it is all "H".

Figure 10-14 Example Where PWM Output Is All "L" Level (TMCR.OSEL="0")

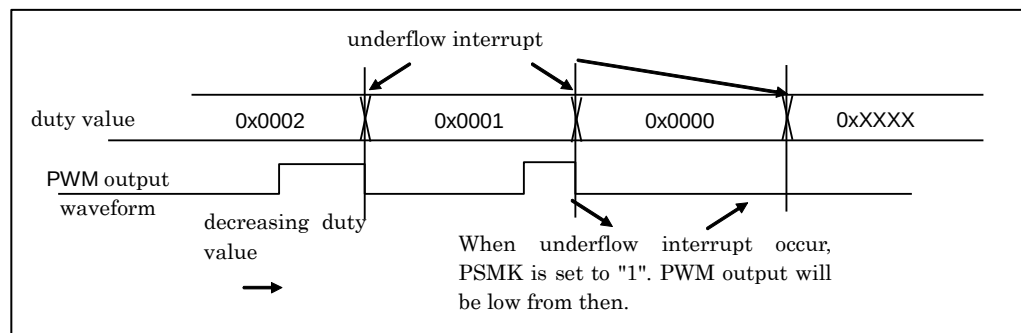
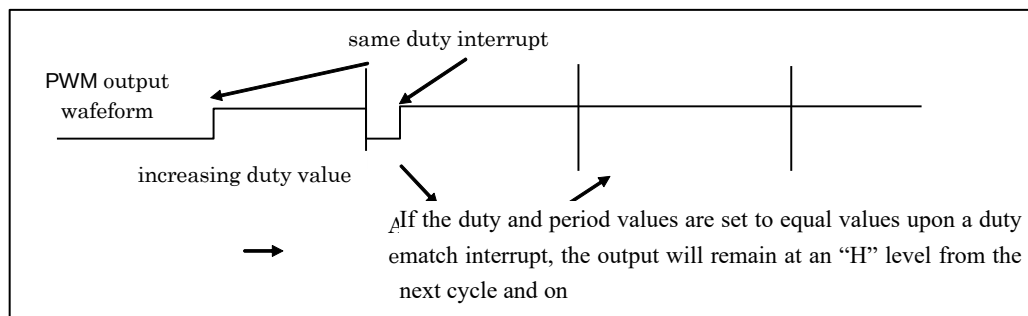


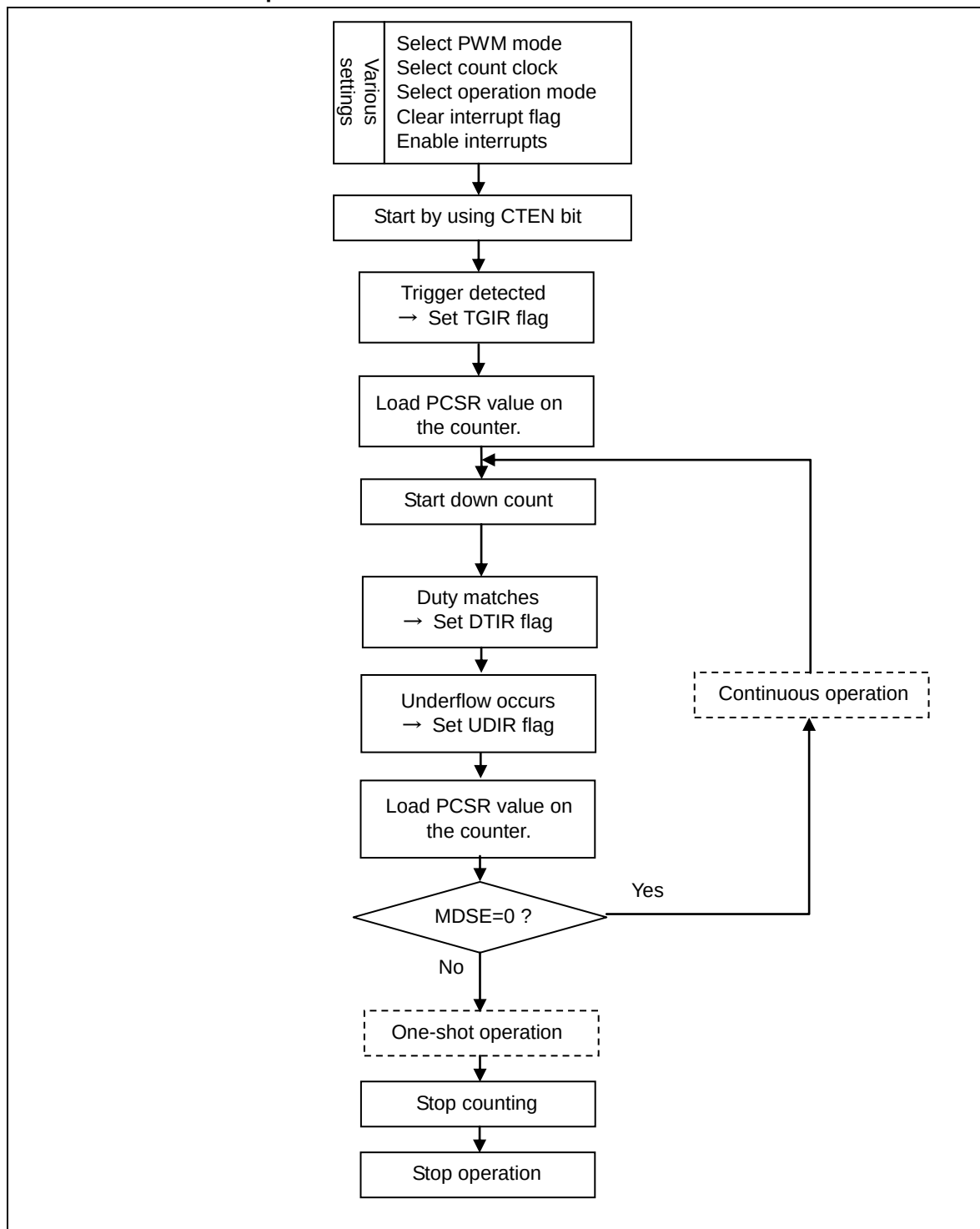
Figure 10-15 Example Where PWM Output Is All "H" Level (TMCR.OSEL="0")



10.1.8. PWM Timer Operation Flow

This section shows the PWM Timer operation flow.

PWM Timer Operation Flow



10.1.9. Timer Control Registers (TMCR, TMCR2), Status Control Register (STC), Status Control Clear Register (STCC), and Status Control Set Register (STCS)

The Timer Control Register (TMCR) controls the PWM Timer. Note that there are bits that cannot be rewritten during PWM Timer operation.

For details on writing to the Status Control Register (STC), see "9.Notes on Using the Base Timer".

10.1.9.1 Timer Control Register (Upper Byte of TMCR)

bit	15	14	13	12	11	10	9	8
Field	Reserved	CKS2	CKS1	CKS0	RTGEN	PMSK	EGS1	EGS0
R/W Attribute	R0,W0	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Protection Attribute	-							
Initial Value	0	0	0	0	0	0	0	0

[bit15] Reserved: Reserved Bit

The read value is "0".

If writing to this bit, write "0".

[TMCR2:bit0,bit14:12] CKS3 to CKS0: Count Clock Selection Bits

- These bits select a count clock for the 17-bit down counter.
- Any modification to the count clock is reflected immediately after the setting is changed. Therefore, modify CKS3 to CKS0 while counting is stopped (CTEN="0"). However, note that the bits can be modified at the same time as "1" is written to the count operation enable bit (CTEN).

CKS3	CKS2	CKS1	CKS0	Description
0	0	0	0	Internal clock
0	0	0	1	Internal clock divided by 4
0	0	1	0	Internal clock divided by 16
0	0	1	1	Internal clock divided by 128
0	1	0	0	Internal clock divided by 256
0	1	0	1	External clock (rising-edge event)
0	1	1	0	External clock (falling-edge event)
0	1	1	1	External clock (both-edges event)
1	0	0	0	Internal clock divided by 512
1	0	0	1	Internal clock divided by 1024
1	0	1	0	Internal clock divided by 2048
1	0	1	1	Internal clock divided by 2
1	1	0	0	Internal clock divided by 8
1	1	0	1	Internal clock divided by 32
1	1	1	0	Internal clock divided by 64
1	1	1	1	Setting prohibited

[bit11] RTGEN: Restart Enable Bit

This bit enables restart by a software trigger or trigger input.

Bit	Description
0	Disable restart.
1	Enable restart.

[bit10] PMSK: Pulse Output Mask Bit

- This bit controls the output waveform level of the PWM output waveform.
- When the bit is "0", the PWM waveform is output as is.
- When the bit is "1", PWM output is masked to "L" output regardless of the cycle or duty setting value.

Note:

- If the output polarity specification bit (OSEL) in the Timer Control Register (lower byte of TMCR) is set for inverted output, setting the PMSK bit to "1" results in masking to "H" output.

Bit	Description
0	Normal output
1	Fixed at "L" output

[bit9:8] EGS1 to EGS0: Trigger Input Edge Selection Bits

- These bits select the valid edge for an input waveform as an external start factor, and they set trigger conditions.
- For the initial value or the "00" setting, no valid edge is selected for an input waveform, so no external waveform causes a start.

Note:

- If "1" is written to the STRG bit, the software trigger becomes valid regardless of the EGS1 and EGS0 settings.

- Modify EGS1 and EGS0 while counting is stopped (CTEN="0"). However, note that the bits can be modified at the same time as "1" is written to the CTEN bit.

EGS1	EGS0	Description
0	0	Trigger input invalid
0	1	Rising edge
1	0	Falling edge
1	1	Both edges

10.1.9.2 Timer Control Register (Lower Byte of TMCR)

bit	7	6	5	4	3	2	1	0
Field	Reserved	FMD2	FMD1	FMD0	OSEL	MDSE	CTEN	STRG
R/W Attribute	R0,W0	R/W	R/W	R/W	R/W	R/W	R/W	R0,W
Protection Attribute	-							
Initial Value	0	0	0	0	0	0	0	0

[bit7] Reserved: Reserved Bit

The read value is "0".

If writing to this bit, write "0".

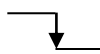
[bit6:4] FMD2 to FMD0: Timer Function Selection Bits

- These bits select the timer function.
- If "001" is set in the FMD2 to FMD0 bits, the PWM function is selected.
- Modify these bits while the timer is stopped (CTEN="0"). However, note that the bits can be modified at the same time as "1" is written to the CTEN bit.

FMD2	FMD1	FMD0	Description
0	0	0	Reset mode
0	0	1	16-bit PWM Timer
0	1	0	16-bit PPG Timer
0	1	1	16/32-bit Reload Timer
1	0	0	16/32-bit PWC Timer
1	0	1	Setting prohibited
1	1	0	
1	1	1	

[bit3] OSEL: Output Polarity Specification Bit

- This bit sets the PWM output polarity.

Polarity	After Reset	Duty Match	Underflow
Normal	"L" output		
Inverse	"H" output		

Bit	Description
0	Normal polarity
1	Inverse polarity

[bit2] MDSE: Mode Selection Bit

- This bit selects either operation for continuous pulse output or one-shot operation for single-pulse output.
- Modify the bit while the timer is stopped (CTEN="0"). However, note that the bits can be modified at the same time as "1" is written to the CTEN bit.

Bit	Description
0	Continuous operation
1	One-shot operation

[bit1] CTEN: Count Operation Enable Bit

- This bit enables operation of the down counter.
- If "0" is written to this bit when counter operation is enabled (CTEN bit is "1"), the counter stops.

Bit	Description
0	Stop operation.
1	Enable operation.

[bit0] STRG: Software Trigger Bit

- If "1" is written to the STRG bit when the CTEN bit is "1", a software trigger is applied.
- The read value of the STRG bit is always "0".

Notes:

- Even if "1" is written to the CTEN and STRG bits at the same time, a software trigger is applied.
- If "1" is written to the STRG bit, the software trigger becomes valid regardless of the EGS1 and EGS0 settings.

Bit	Description
0	Invalid
1	Startup by software

10.1.9.3 Timer Control Register 2 (TMCR2)

bit	7	6	5	4	3	2	1	0
Field	Reserved						ETCEN	CKS3
R/W Attribute	R0,W0						R/W	R/W
Protection Attribute	-							
Initial Value	000000						0	0

[bit7:2] Reserved: Reserved Bits

The read value is "0".

If writing to this bit, write "0".

[bit1] ETCEN: External Timer Compare Enable Bit

It is the bit which enables match detection of an external timer value and the ETCDR register value.

Bit	Description
0	Match detection disable
1	Match detection enable

[bit0] CKS3: Count Clock Selection Bit

See "Count clock selection bits" in "10.1.9Timer Control Registers (TMCR, TMCR2), Status Control Register (STC), Status Control Clear Register (STCC), and Status Control Set Register (STCS)".

10.1.9.4 Status Control Register (STC)

bit	7	6	5	4	3	2	1	0
Field	Reserved	TGIE	DTIE	UDIE	Reserved	TGIR	DTIR	UDIR
R/W Attribute	R0,W0	R/W	R/W	R/W	R0,W0	R,WX	R,WX	R,WX
Protection Attribute	-							
Initial Value	0	0	0	0	0	0	0	0

[bit7] Reserved: Reserved Bit

The read value is "0".

If writing to this bit, write "0".

[bit6] TGIE: Trigger Interrupt Request Enable Bit

- This bit controls interrupt requests of the trigger interrupt request bit (bit2 TGIR).
- If the TGIE bit is enabled and the TGIR bit is set to "1", an interrupt request is issued to the CPU.
- Writing "1" to the STCC.TGIEC bit clears this bit.
- Writing "1" to the STCS.TGIES bit sets this bit.

Bit	Description
0	Disable interrupt requests.
1	Enable interrupt requests.

[bit5] DTIE: Duty Match Interrupt Request Enable Bit

- This bit controls interrupt requests of the duty match interrupt request bit (bit1 DTIR).
- If the DTIE bit is enabled and the DTIR bit is set to "1", an interrupt request is issued to the CPU.
- Writing "1" to the STCC.DTIEC bit clears this bit.
- Writing "1" to the STCS.DTIES bit sets this bit.

Bit	Description
0	Disable interrupt requests.
1	Enable interrupt requests.

[bit4] UDIE: Underflow Interrupt Request Enable Bit

- This bit controls interrupt requests of the underflow interrupt request bit (bit0 UDIR).
- If the UDIE bit is enabled and the UDIR bit is set to "1", an interrupt request is issued to the CPU.
- Writing "1" to the STCC.UDIEC bit clears this bit.
- Writing "1" to the STCS.UDIES bit sets this bit.

Bit	Description
0	Disable interrupt requests.
1	Enable interrupt requests.

[bit3] Reserved: Reserved Bit

The read value is "0".

If writing to this bit, write "0".

[bit2] TGIR: Trigger Interrupt Request Bit

- The TGIR bit is set to "1" when a software trigger or trigger input is detected.
- Writing "1" to the STCC.TGIRC bit clears this bit.
- This bit is read-only. Writing data to this bit has no effect on operation.

Bit	Description
0	The interrupt factor is cleared.
1	Detect the interrupt factor.

[bit1] DTIR: Duty Match Interrupt Request Bit

- The DTIR bit is set to "1" when the count value matches the duty setting value.
- Writing "1" to the STCC.DTIRC bit clears this bit.
- This bit is read-only. Writing data to this bit has no effect on operation.

Bit	Description
0	The interrupt factor is cleared.
1	Detect the interrupt factor.

[bit0] UDIR: Underflow Interrupt Request Bit

- The UDIR bit is set to "1" when the count value underflows from 0x0000 to 0xFFFF.
- Writing "1" to the STCC.UDIRC bit clears this bit.
- This bit is read-only. Writing data to this bit has no effect on operation.

Bit	Description
0	The interrupt factor is cleared.
1	Detect the interrupt factor.

10.1.9.5 Status Control Clear Register (STCC)

bit	7	6	5	4	3	2	1	0
Field	Reserved	TGIEC	DTIEC	UDIEC	Reserved	TGIRC	DTIRC	UDIRC
R/W Attribute	R0,W0	R0,W	R0,W	R0,W	R0,W0	R0,W	R0,W	R0,W
Protection Attribute	-							
Initial Value	0	0	0	0	0	0	0	0

[bit7] Reserved: Reserved Bit

The read value is "0".

If writing to this bit, write "0".

[bit6] TGIEC: Trigger Interrupt Request Enable Clear Bit

- If "1" is written to this bit, the STC.TGIE bit is cleared to "0".
- The read value of this bit is always "0".

Bit	Description
0	Invalid
1	Clear the TGIE bit.

[bit5] DTIEC: Duty Match Interrupt Request Enable Clear Bit

- If "1" is written to this bit, the STC.DTIE bit is cleared to "0".
- The read value of this bit is always "0".

Bit	Description
0	Invalid
1	Clear the DTIE bit.

[bit4] UDIEC: Underflow Interrupt Request Enable Clear Bit

- If "1" is written to this bit, the STC.UDIE bit is cleared to "0".
- The read value of this bit is always "0".

Bit	Description
0	Invalid
1	Clear the UDIE bit.

[bit3] Reserved: Reserved Bit

The read value is "0".

If writing to this bit, write "0".

[bit2] TGIRC: Trigger Interrupt Request Clear Bit

- If "1" is written to this bit, the STC.TGIR bit is cleared to "0".
- The read value of this bit is always "0".

Bit	Description
0	Invalid
1	Clear the TGIR bit.

[bit1] DTIRC: Duty Match Interrupt Request Clear Bit

- If "1" is written to this bit, the STC.DTIR bit is cleared to "0".
- The read value of this bit is always "0".

Bit	Description
0	Invalid
1	Clear the DTIR bit.

[bit0] UDIRC: Underflow Interrupt Request Clear Bit

- If "1" is written to this bit, the STC.UDIR bit is cleared to "0".
- The read value of this bit is always "0".

Bit	Description
0	Invalid
1	Clear the UDIR bit.

10.1.9.6 Status Control Set Register (STCS)

bit	7	6	5	4	3	2	1	0
Field	Reserved	TGIES	DTIES	UDIES	Reserved			
R/W Attribute	R0,W0	R0,W	R0,W	R0,W	R0,W0			
Protection Attribute	-							
Initial Value	0	0	0	0	0000			

[bit7] Reserved: Reserved Bit

The read value is "0".

If writing to this bit, write "0".

[bit6] TGIES: Trigger Interrupt Request Enable Set Bit

- If "1" is written to this bit, the STC.TGIE bit is set to "1".
- The read value of this bit is always "0".

Bit	Description
0	Invalid
1	Set the TGIE bit.

[bit5] DTIES: Duty Match Interrupt Request Enable Set Bit

- If "1" is written to this bit, the STC.DTIE bit is set to "1".
- The read value of this bit is always "0".

Bit	Description
0	Invalid
1	Set the DTIE bit.

[bit4] UDIES: Underflow Interrupt Request Enable Set Bit

- If "1" is written to this bit, the STC.UDIE bit is set to "1".
- The read value of this bit is always "0".

Bit	Description
0	Invalid
1	Set the UDIE bit.

[bit3-0] Reserved: Reserved Bits

The read value is "0".

If writing to this bit, write "0".

10.1.10. PWM Cycle Setting Register (PCSR)

The PWM Cycle Setting Register (PCSR) is a register with a buffer for setting a cycle. There is a transfer to the Timer Register (TMR) at the start time and at the underflow time.

bit	15	8
Field	PCSR[15:8]	
R/W Attribute	R/W	
Protection Attribute	-	
Initial Value	XXXX XXXX	

bit	7	0
Field	PCSR[7:0]	
R/W Attribute	R/W	
Protection Attribute	-	
Initial Value	XXXX XXXX	

These bits compose the register with a buffer for setting a cycle. There is a transfer to the Timer Register (TMR) at the start time and at the underflow time.

When initializing and rewriting the Cycle Setting Register (PCSR), be sure to write to the duty setting register after writing to the Cycle Setting Register (PCSR).

- Use 16- or 32-bit data access for the PCSR register.
- After configuring the PWM function with the FMD2 to FMD0 bits in the TMCR register, set a cycle in the PCSR register.

10.1.11. PWM Duty Setting Register (PDUT)

The PWM Duty Setting Register (PDUT) is a register with a buffer for setting a duty. An underflow causes a buffer transfer.

bit	15	8
Field	PDUT[15:8]	
R/W Attribute	R/W	
Protection Attribute	-	
Initial Value	XXXX XXXX	

bit	7	0
Field	PDUT[7:0]	
R/W Attribute	R/W	
Protection Attribute	-	
Initial Value	XXXX XXXX	

These bits compose the register with a buffer for setting a duty. An underflow causes a transfer from the buffer.

If the set values of the Cycle Setting Register (PCSR) and duty setting register are the same value, the output for normal polarity is all "H", and the output for inverse polarity is all "L".

If PCSR < PDUT in the set values, the output for normal polarity is all "L", and the output for inverse polarity is all "H".

- Use 16- or 32-bit data access for the PDUT register.
- After configuring the PWM function with the FMD2 to FMD0 bits in the TMCR register, set a duty in the PDUT register.

10.1.12. Timer Register (TMR)

The Timer Register (TMR) can read the value of the 17-bit down counter.

Bit	31	24
Field	Reserved	
R/W Attribute	R0,W0	
Protection Attribute	-	
Initial Value	0000 0000	

bit	23	17	16
Field	Reserved		TMR[16]
R/W Attribute	R0,W0		R,WX
Protection Attribute	-		
Initial Value	00000000		0

Bit	15	8
Field	TMR[15:8]	
R/W Attribute	R,WX	
Protection Attribute	-	
Initial Value	0000 0000	

Bit	7	0
Field	TMR[7:0]	
R/W Attribute	R,WX	
Protection Attribute	-	
Initial Value	0000 0000	

[bit31:17] Reserved: Reserved Bits

The read value is "0".

[bit16:0] TMR16 to TMR0: Timer Value Data Bits

The Timer Register (TMR) can read the value of the 17-bit down counter that takes into account the start delay period.

- During trigger input, a value of "start delay period (PSDR) + PWM cycle (PCSR)" is reloaded into the TMR register.
- A value of "PWM cycle (PCSR)" is reloaded into the TMR register when an underflow occurs.
- Use 32-bit data access for the TMR register.

10.1.13. Start Delay Value Setting Register (PSDR)

The Start Delay Value Setting Register (PSDR) sets a start delay value for the start delay function.

bit	15	8
Field	PSDR[15:8]	
R/W Attribute	R/W	
Protection Attribute	-	
Initial Value	0000 0000	

bit	7	0
Field	PSDR[7:0]	
R/W Attribute	R/W	
Protection Attribute	-	
Initial Value	0000 0000	

The PSDR[15:0] bits set a start delay value to delay the start of the PWM Timer after trigger input.

- To not use the start delay function, set the PSDR[15:0] bits to 0x0000.
- No PWM waveform is output during start delay control period after trigger input.
- After configuring the PWM function with the FMD2 to FMD0 bits in the TMCR register, set a cycle in the PSDR register.
- Use 16- or 32-bit data access for the PSDR register.
- Any modification to the PSDR[15:0] bits is reflected immediately after the setting is changed. Set the PSDR[15:0] bits while counting is stopped (TMCR:CTEN="0").

10.1.14. ADC Trigger Value Setting Register (ADTR)

The ADC Trigger Value Setting Register (ADTR) sets the time for ADC trigger output.

bit	15	8
Field	ADTR[15:8]	
R/W Attribute	R/W	
Protection Attribute	-	
Initial Value	00000 0000	

bit	7	0
Field	ADTR[7:0]	
R/W Attribute	R/W	
Protection Attribute	-	
Initial Value	0000 0000	

The ADC trigger is output when the 16-bit down counter is compared with the ADTR[15:0] bits and they match.

- For the ADTR register, set a value equal to or less than the PCSR[15:0] bits in the PCSR register.
- Use 16- or 32-bit data access for the ADTR register.
- After configuring the PWM function with the FMD2 to FMD0 bits in the TMCR register, set a cycle in the ADTR register.

10.1.15. Base Timer Debug Register (BT_DEBUG)

The Base Timer Debug Register (BT_DEBUG) performs enable/disable setting of debug.

bit	15	8
Field	Reserved	
R/W Attribute	R0,W0	
Protection Attribute	-	
Initial Value	0000 0000	

bit	7	1	0
Field	Reserved		DBGEN
R/W Attribute	R0,W0		R/W
Protection Attribute	-		
Initial Value	0000000		0

[bit15:1] Reserved: Reserved Bits

The read value is "0".

If writing to this bit, write "0".

[bit0] DBGEN: Debug Enable Bit

- It is the bit which permits stopping operation of a Base Timer with the debug signal (DEBUG).

Bit	Description
0	Disable
1	Enable

10.1.16. External Timer Compare Data Register (ETCDR)

The External Timer Compare Data Register (ETCDR) is the register which sets the value which is started by an external timer.

bit	15	8
Field	ETCDR[15:8]	
R/W Attribute	R/W	
Protection Attribute	-	
Initial Value	01111111	

bit	7	0
Field	ETCDR[7:0]	
R/W Attribute	R/W	
Protection Attribute	-	
Initial Value	11111111	

It is a register compared with an external timer signal (ETINI). Refer to "10.1.5 External Timer Match Starting" for details.

- Use 16- or 32-bit data access for the ETCDR register.

10.2. PPG Timer Function

Only one of the following timer functions can be selected for the Base Timer in the FMD2 to FMD0 bit settings in the Timer Control Register (TMCR): 16-bit PWM Timer, 16-bit PPG Timer, 16/32-bit Reload Timer, and 16/32-bit PWC Timer. This section explains the timer function with the PPG setting.

10.2.1 16-Bit PPG Timer Operation

10.2.2 Continuous Operation

10.2.3 One-Shot Operation

10.2.4 External Timer Match Starting

10.2.5 Interrupt Factors and Timing Chart

10.2.6 PPG Timer Operation Flow

10.2.7 Timer Control Registers (TMCR, TMCR2), Status Control Register (STC), Status Control Clear Register (STCC), and Status Control Set Register (STCS)

10.2.8 Low Width Setting Reload Register (PRL)

10.2.9 High Width Setting Reload Register (PRLH)

10.2.10 Timer Register (TMR)

10.2.11 Base Timer Debug Register (BT_DEBUG)

10.2.12 External Timer Compare Data Register (ETCDR)

10.2.1. 16-Bit PPG Timer Operation

PPG Timer operation can control output pulses by using the "L" width and "H" width settings for the output pulses in the respective reload registers.

Overview of Operation

There are two 16-bit reload registers for the "L" width and "H" width settings and one buffer for the "H" width setting (PRLH, PRLH, and PRLHB).

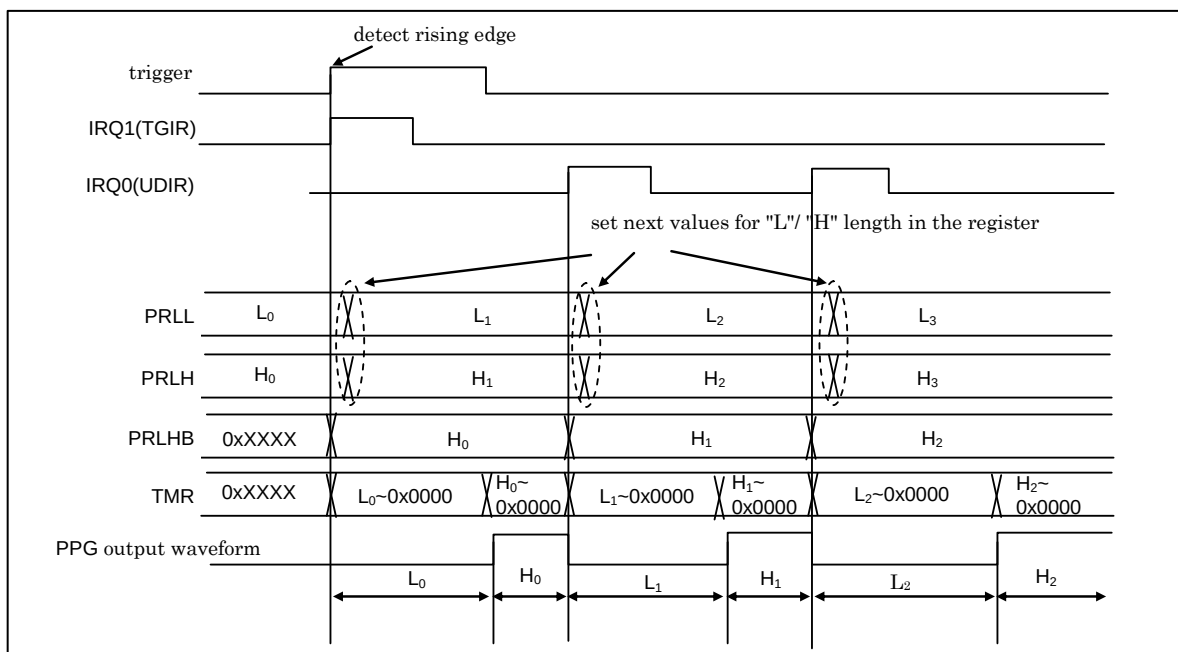
An activation trigger first causes loading of the set value of PRLH into the 16-bit down counter. At the same time, the set value of PRLH is transferred to PRLHB. The PPG output level changes to "L", and the counter counts down each count clock. The detection of an underflow causes reloading of the PRLHB value into the counter, inverts the PPG output waveform and continues counting down each count clock. The detection of another underflow causes inversion of the PPG output waveform, reloading of the set value of PRLH into the counter, and transfer of the set value of PRLH to PRLHB.

The pulse output by the output waveform from this operation has an "L" width and "H" width corresponding to each reload register value.

Timing of Writing to Reload Registers

Data is written to the reload registers PRLH and PRLH when an activation trigger is detected, and also before the next cycle change occurs following an underflow interrupt factor (UDIR) being asserted to "1".

The data that is set at this time is the settings for the next cycle. The set data in PRLH and PRLH is automatically transferred to TMR and PRLHB, respectively, when an activation trigger is detected or when an underflow occurs at the "H" width count end time. The data transferred to PRLHB is automatically reloaded into TMR when an underflow occurs at the "L" width count end time.



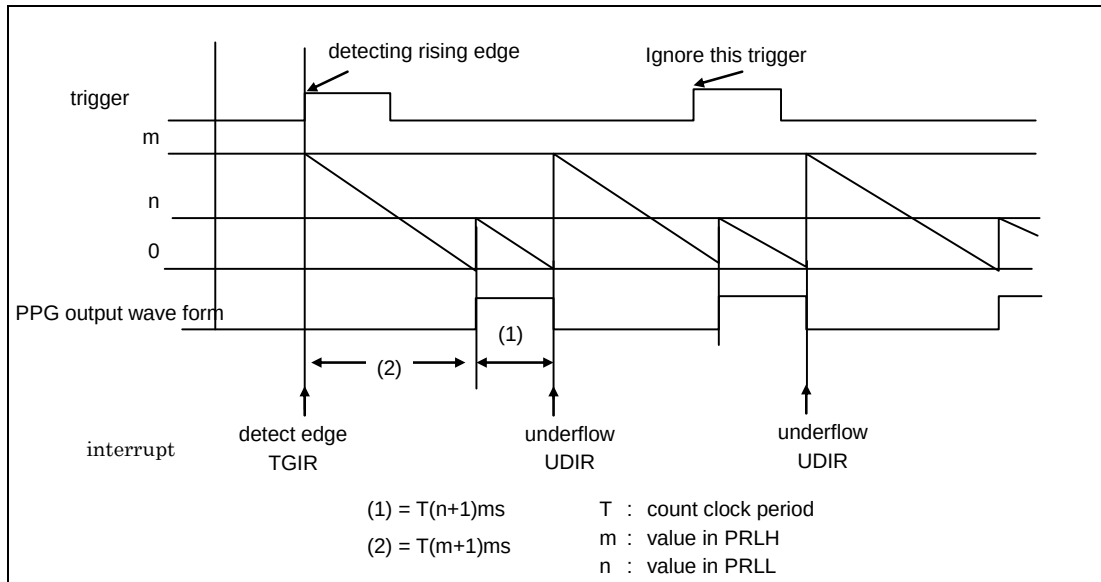
10.2.2. Continuous Operation

In continuous operation, pulses can be output continuously through updating of the "L" width and "H" width at the set timing for each interrupt factor. If restart is enabled, the counter is reloaded when an edge is detected during operation.

Continuous Operation

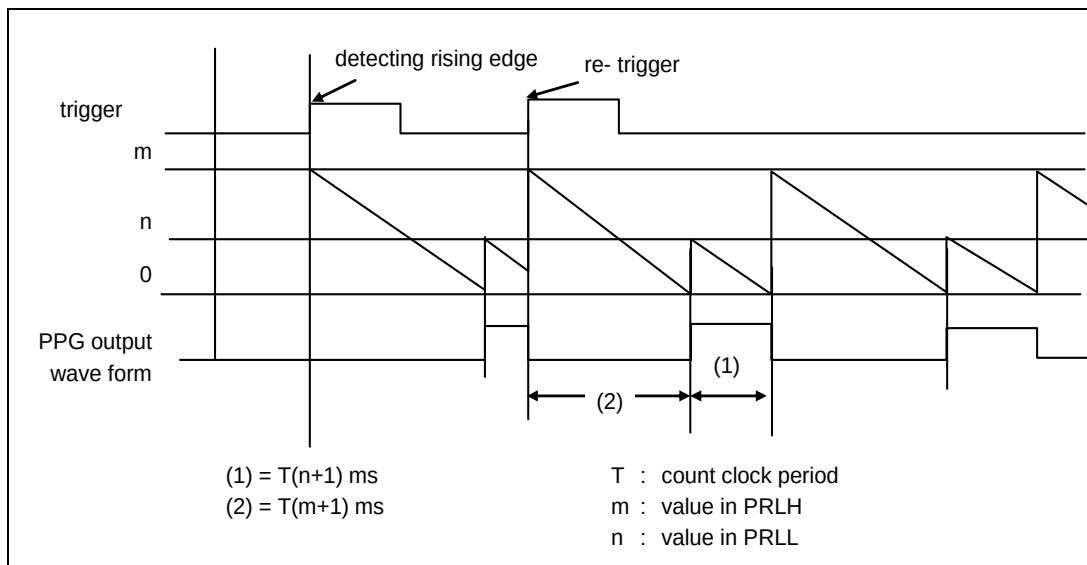
When Restart is Disabled (RTGEN="0")

Figure 10-16 PPG Operation Timing Chart (When Restart Is Disabled)



When Restart is Enabled (RTGEN="1")

Figure 10-17 PPG Operation Timing Chart (When Restart Is Enabled)



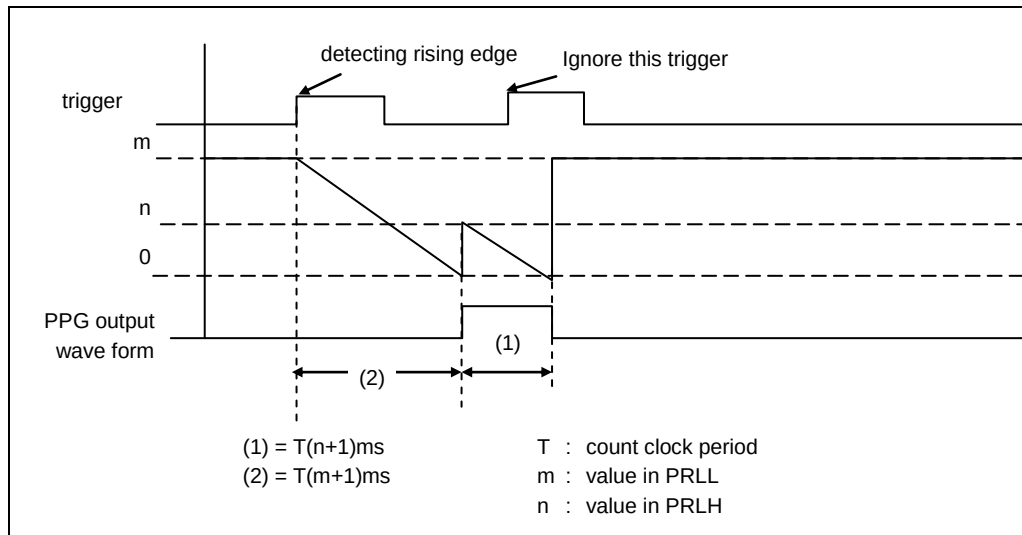
10.2.3. One-Shot Operation

In one-shot operation, a trigger can cause the output of a single pulse of any width. If restart is enabled, the counter is reloaded when an edge is detected during operation.

One-Shot Operation

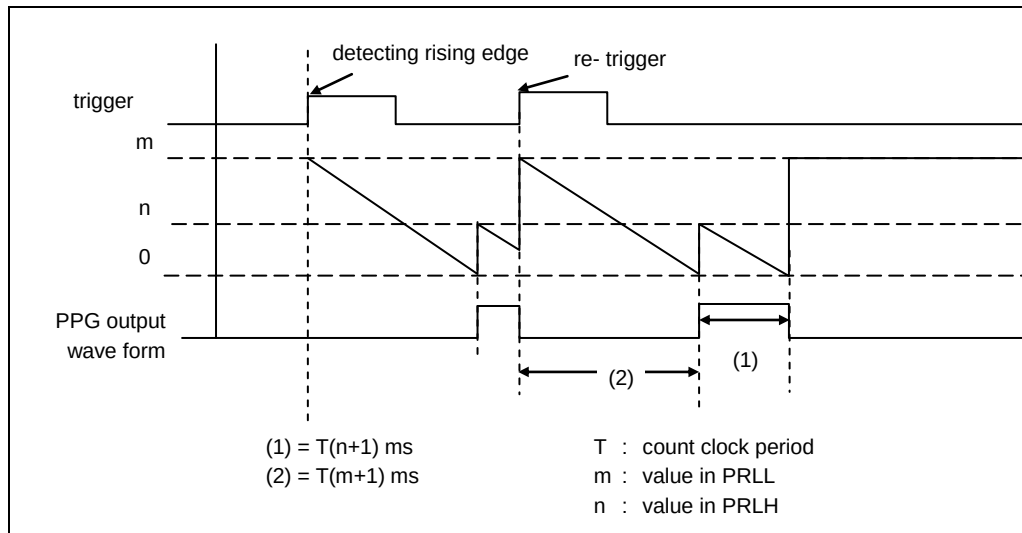
When Restart is Disabled (RTGEN="0")

Figure 10-18 One-Shot Operation Timing Chart (Trigger Restart Disabled)



When Restart is Enabled (RTGEN="1")

Figure 10-19 One-Shot Operation Timing Chart (Trigger Restart Enabled)



Relationship Between Reload Value and Pulse Width

The output pulse width is the following value: 1 is added to the value written to the 16-bit reload register, and the sum is multiplied by the cycles of the count clock. Therefore, when the value of the reload register is 0x0000, the pulse width is equal to 1 count clock cycle. Similarly, when the value of the reload register is 0xFFFF, the pulse width is equal to 65536 count clock cycles. The pulse width calculation formula is as follows.

$$PL = T \times (L + 1)$$

$$PH = T \times (H + 1)$$

PL: "L" pulse width

PH: "H" pulse width

T: Count clock cycle

L: PRLl value

H: PRLH value

10.2.4. External Timer Match Starting

If the external timer match starting function is used, the 16/17-bit down counter can start in synchronization with an external timer.

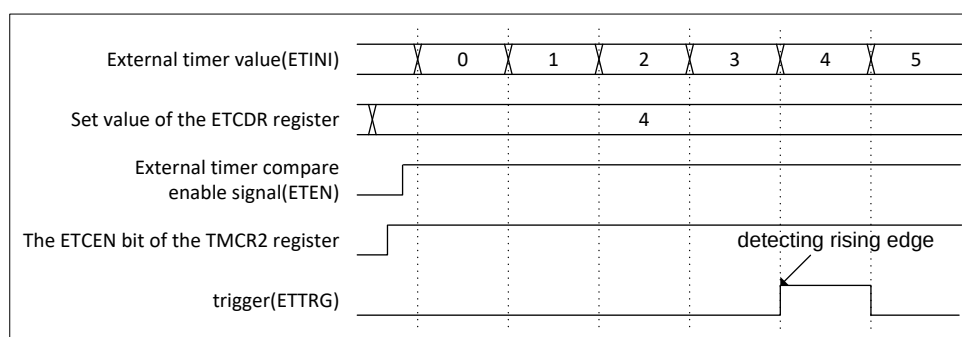
If all the following conditions are satisfied, starting by an external timer is performed.

- The CTEN bit of the TMCR register is "1".
- The ETCEN bit of the TMCR2 register is "1".
- The external timer compare enable signal (ETEN) is active.

When timer is running, the restart by the external timer match starting does not occur. If performing external timer match starting again, perform the following processings.

1. The CTEN bit of the TMCR register is set to "0".
2. The CTEN bit of the TMCR register is set to "1" again.

Figure 10-20 The Example of External Timer Match Starting Operation (ETCDR=4)



10.2.5. Interrupt Factors and Timing Chart

This section shows interrupt factors and a timing chart.

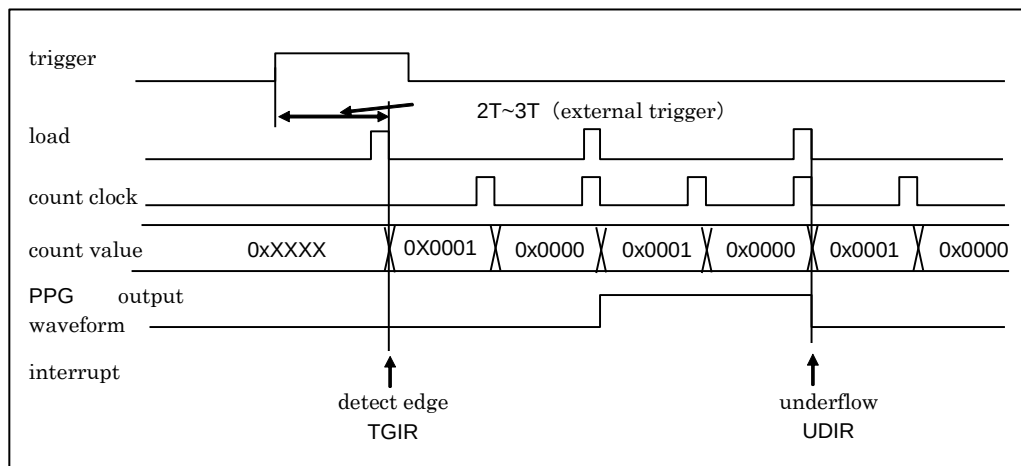
Interrupt Factors and Timing Chart (PPG Output: Normal Polarity)

For the period from trigger application until the loading of a counter value, the required software trigger time is T , and the required external trigger time is $2T$ to $3T$ (T : Internal clock cycle).

An interrupt factor is generated when a PPG activation trigger is detected or when an underflow is detected at the "H" level output time.

Figure 10-21 shows the interrupt factors and a timing chart where the "L" width setting value is 1 and the "H" width setting value is 1.

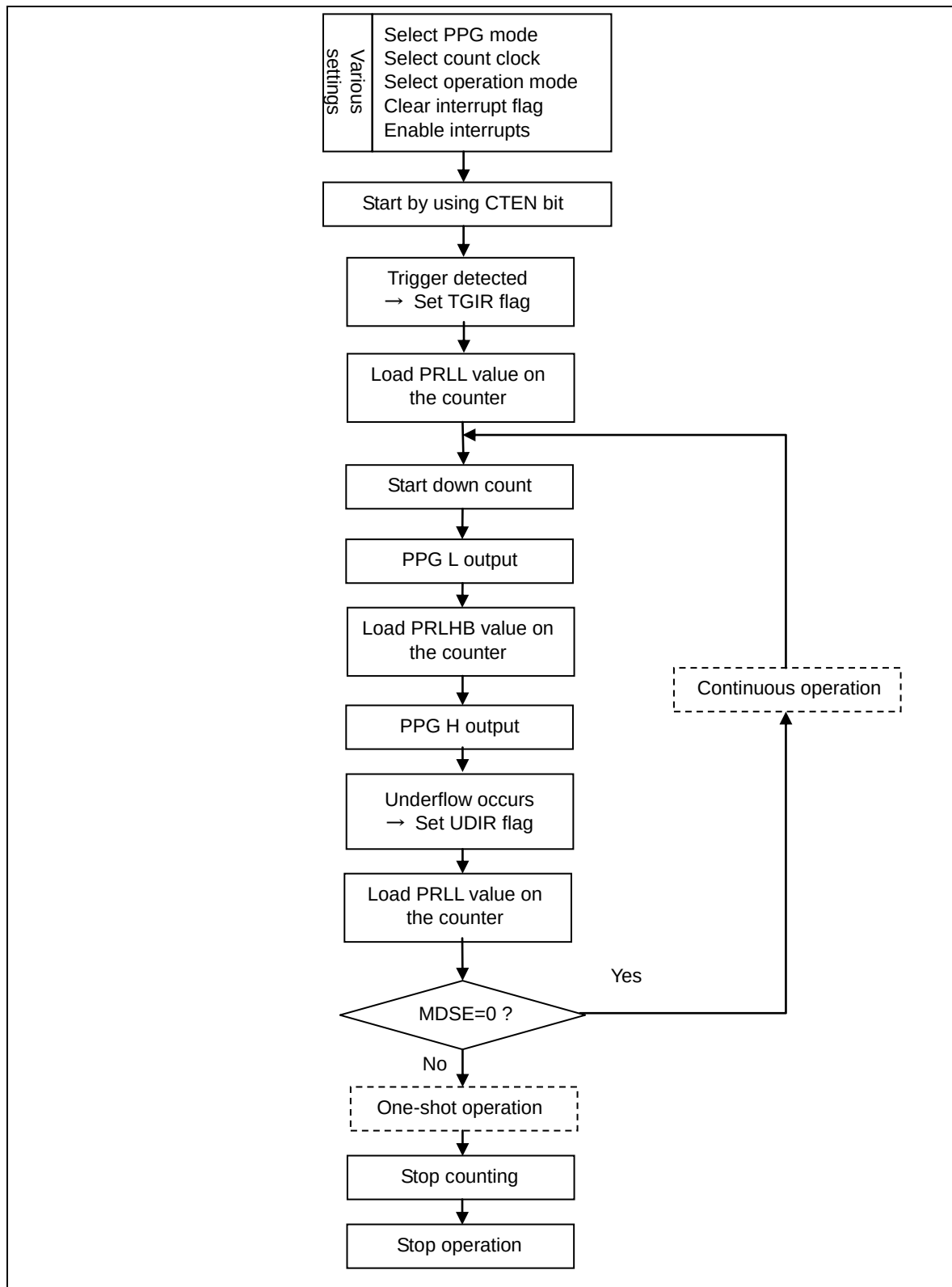
Figure 10-21 PPG Timer Interrupt Factors and Timing Chart



10.2.6. PPG Timer Operation Flow

This section shows the PPG Timer operation flow.

PPG Timer Operation Flow



10.2.7. Timer Control Registers (TMCR, TMCR2), Status Control Register (STC), Status Control Clear Register (STCC), and Status Control Set Register (STCS)

For details on writing to the Status Control Register (STC), see "9. Notes on Using the Base Timer".

10.2.7.1 Timer Control Register (Upper Byte of TMCR)

bit	15	14	13	12	11	10	9	8
Field	Reserved	CKS2	CKS1	CKS0	RTGEN	PMSK	EGS1	EGS0
R/W Attribute	R0,W0	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Protection Attribute	-							
Initial Value	0	0	0	0	0	0	0	0

[bit15] Reserved: Reserved Bit

The read value is "0".

If writing to this bit, write "0".

[TMCR2:bit0,bit14:12] CKS3 to CKS0: Count Clock Selection Bits

- These bits select a count clock for the 16-bit down counter.
- Any modification to the count clock is reflected immediately after the setting is changed. Therefore, modify CKS3 to CKS0 while counting is stopped (CTEN="0"). However, note that the bits can be modified at the same time as "1" is written to the CTEN bit.

CKS3	CKS2	CKS1	CKS0	Description
0	0	0	0	Internal clock
0	0	0	1	Internal clock divided by 4
0	0	1	0	Internal clock divided by 16
0	0	1	1	Internal clock divided by 128
0	1	0	0	Internal clock divided by 256
0	1	0	1	External clock (rising-edge event)
0	1	1	0	External clock (falling-edge event)
0	1	1	1	External clock (both-edges event)
1	0	0	0	Internal clock divided by 512
1	0	0	1	Internal clock divided by 1024
1	0	1	0	Internal clock divided by 2048
1	0	1	1	Internal clock divided by 2
1	1	0	0	Internal clock divided by 8
1	1	0	1	Internal clock divided by 32
1	1	1	0	Internal clock divided by 64
1	1	1	1	Setting prohibited

[bit11] RTGEN: Restart Enable Bit

This bit enables restart by a software trigger or trigger input.

Bit	Description
0	Disable restart.
1	Enable restart.

[bit10] PMSK: Pulse Output Mask Bit

- This bit controls the output waveform level of the PPG output waveform.
- When the bit is "0", the PPG waveform is output as is.
- When the bit is "1", PPG output is masked to "L" output regardless of the cycle or duty setting value.

Note:

- If the output polarity specification bit (OSEL) in the Timer Control Register (lower byte of TMCR) is set for inverted output, setting the PMSK bit to "1" results in masking to "H" output.

Bit	Description
0	Normal output
1	Fixed at "L" output

[bit9:8] EGS1 to EGS0: Trigger Input Edge Selection Bits

- These bits select the valid edge for an input waveform as an external start factor, and they set trigger conditions.
- For the initial value or the "00" setting, no valid edge is selected for an input waveform, so no external waveform causes a start.

Note:

- If "1" is written to the STRG bit, the software trigger becomes valid regardless of the EGS1 and EGS0 settings.
- Modify EGS1 and EGS0 while counting is stopped (CTEN="0"). However, note that the bits can be modified at the same time as "1" is written to the CTEN bit.

EGS1	EGS0	Description
0	0	Trigger input invalid
0	1	Rising edge
1	0	Falling edge
1	1	Both edges

10.2.7.2 Timer Control Register (Lower Byte of TMCR)

bit	7	6	5	4	3	2	1	0
Field	Reserved	FMD2	FMD1	FMD0	OSEL	MDSE	CTEN	STRG
R/W Attribute	R0,W0	R/W	R/W	R/W	R/W	R/W	R/W	R0,W
Protection Attribute	-							
Initial Value	0	0	0	0	0	0	0	0

[bit7] Reserved: Reserved Bit

The read value is "0".

If writing to this bit, write "0".

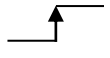
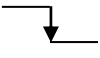
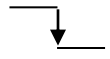
[bit6:4] FMD2 to FMD0: Timer Function Selection Bits

- These bits select the timer function.
- If "010" is set in the FMD2 to FMD0 bits, the PPG function is selected.
- Modify these bits while the timer is stopped (CTEN="0"). However, note that the bits can be modified at the same time as "1" is written to the CTEN bit.

FMD2	FMD1	FMD0	Description
0	0	0	Reset mode
0	0	1	16-bit PWM Timer
0	1	0	16-bit PPG Timer
0	1	1	16/32-bit Reload Timer
1	0	0	16/32-bit PWC Timer
1	0	1	Setting prohibited
1	1	0	
1	1	1	

[bit3] OSEL: Output Polarity Specification Bit

- This bit sets the PPG output polarity.

Polarity	After Reset	"L" Width Count End	"H" Width Count End
Normal	"L" output		
Inverse	"H" output		

Bit	Description
0	Normal polarity
1	Inverse polarity

[bit2] MDSE: Mode Selection Bit

- This bit selects either operation for continuous pulse output or one-shot operation for single-pulse output.
- Modify the bit while the timer is stopped (CTEN="0"). However, note that the bits can be modified at the same time as "1" is written to the CTEN bit.

Bit	Description
0	Continuous operation
1	One-shot operation

[bit1] CTEN: Count Operation Enable Bit

- This bit enables operation of the down counter.
- If "0" is written to this bit when counter operation is enabled (CTEN bit is "1"), the counter stops.

Bit	Description
0	Stop operation.
1	Enable operation.

[bit0] STRG: Software Trigger Bit

- If "1" is written to the STRG bit when the CTEN bit is "1", a software trigger is applied.
- The read value of the STRG bit is always "0".

Notes:

- Even if "1" is written to the CTEN and STRG bits at the same time, a software trigger is applied.
- If "1" is written to the STRG bit, the software trigger becomes valid regardless of the EGS1 and EGS0 settings.

Bit	Description
0	Invalid
1	Startup by software

10.2.7.3 Timer Control Register 2 (TMCR2)

bit	7	6	5	4	3	2	1	0
Field	Reserved						ETCEN	CKS3
R/W Attribute	R0,W0						R/W	R/W
Protection Attribute	-							
Initial Value	000000						0	0

[bit7:2] Reserved: Reserved Bits

The read value is "0".

If writing to this bit, write "0".

[bit1] ETCEN: External Timer Compare Enable Bit

It is the bit which enables match detection of an external timer value and the ETCDR register value.

Bit	Description
0	Match detection disable
1	Match detection enable

[bit0] CKS3: Count Clock Selection Bit

See "Count clock selection bits" in "10.2.7 Timer Control Registers (TMCR, TMCR2), Status Control Register (STC), Status Control Clear Register (STCC), and Status Control Set Register (STCS)".

10.2.7.4 Status Control Register (STC)

bit	7	6	5	4	3	2	1	0
Field	Reserved	TGIE	Reserved	UDIE	Reserved	TGIR	Reserved	UDIR
R/W Attribute	R0,W0	R/W	R0,W0	R/W	R0,W0	R,WX	R0,W0	R,WX
Protection Attribute	-							
Initial Value	0	0	0	0	0	0	0	0

[bit7] Reserved: Reserved Bit

The read value is "0".

If writing to this bit, write "0".

[bit6] TGIE: Trigger Interrupt Request Enable Bit

- This bit controls interrupt requests of the trigger interrupt request bit (bit2 TGIR).
- If the TGIE bit is enabled and the TGIR bit is set to "1", an interrupt request is issued to the CPU.
- Writing "1" to the STCC.TGIEC bit clears this bit.
- Writing "1" to the STCS.TGIES bit sets this bit.

Bit	Description
0	Disable interrupt requests.
1	Enable interrupt requests.

[bit5] Reserved: Reserved Bit

The read value is "0".

If writing to this bit, write "0".

[bit4] UDIE: Underflow Interrupt Request Enable Bit

- This bit controls interrupt requests of the underflow interrupt request bit (bit0 UDIR).
- If the UDIE bit is enabled and the UDIR bit is set to "1", an interrupt request is issued to the CPU.
- Writing "1" to the STCC.UDIEC bit clears this bit.
- Writing "1" to the STCS.UDIES bit sets this bit.

Bit	Description
0	Disable interrupt requests.
1	Enable interrupt requests.

[bit3] Reserved: Reserved Bit

The read value is "0".

If writing to this bit, write "0".

[bit2] TGIR: Trigger Interrupt Request Bit

- The TGIR bit is set to "1" when a software trigger or trigger input is detected.
- Writing "1" to the STCC.TGIRC bit clears this bit.
- This bit is read-only. Writing data to this bit has no effect on operation.

Bit	Description
0	The interrupt factor is cleared.
1	Detect the interrupt factor.

[bit1] Reserved: Reserved Bit

The read value is "0".

If writing to this bit, write "0".

[bit0] UDIR: Underflow Interrupt Request Bit

- During counting from the set "H" width value, the UDIR bit is set to "1" when the count value underflows and changes from 0x0000 to 0xFFFF.
- Writing "1" to the STCC.UDIRC bit clears this bit.
- This bit is read-only. Writing data to this bit has no effect on operation.

Bit	Description
0	The interrupt factor is cleared.
1	Detect the interrupt factor.

10.2.7.5 Status Control Clear Register (STCC)

bit	7	6	5	4	3	2	1	0
Field	Reserved	TGIEC	Reserved	UDIEC	Reserved	TGIRC	Reserved	UDIRC
R/W Attribute	R0,W0	R0,W	R0,W0	R0,W	R0,W0	R0,W	R0,W0	R0,W
Protection Attribute	-							
Initial Value	0	0	0	0	0	0	0	0

[bit7] Reserved: Reserved Bit

The read value is "0".

If writing to this bit, write "0".

[bit6] TGIEC: Trigger Interrupt Request Enable Clear Bit

- If "1" is written to this bit, the STC.TGIE bit is cleared to "0".
- The read value of this bit is always "0".

Bit	Description
0	Invalid
1	Clear the TGIE bit.

[bit5] Reserved: Reserved Bit

The read value is "0".

If writing to this bit, write "0".

[bit4] UDIEC: Underflow Interrupt Request Enable Clear Bit

- If "1" is written to this bit, the STC.UDIE bit is cleared to "0".
- The read value of this bit is always "0".

Bit	Description
0	Invalid
1	Clear the UDIE bit.

[bit3] Reserved: Reserved Bit

The read value is "0".

If writing to this bit, write "0".

[bit2] TGIRC: Trigger Interrupt Request Clear Bit

- If "1" is written to this bit, the STC.TGIR bit is cleared to "0".
- The read value of this bit is always "0".

Bit	Description
0	Invalid
1	Clear the TGIR bit.

[bit1] Reserved: Reserved Bit

The read value is "0".

If writing to this bit, write "0".

[bit0] UDIRC: Underflow Interrupt Request Clear Bit

- If "1" is written to this bit, the STC.UDIR bit is cleared to "0".
- The read value of this bit is always "0".

Bit	Description
0	Invalid
1	Clear the UDIR bit.

10.2.7.6 Status Control Set Register (STCS)

bit	7	6	5	4	3	2	1	0
Field	Reserved	TGIES	Reserved	UDIES	Reserved			
R/W Attribute	R0,W0	R0,W	R0,W0	R0,W	R0,W0			
Protection Attribute	-							
Initial Value	0	0	0	0	0000			

[bit7] Reserved: Reserved Bit

The read value is "0".

If writing to this bit, write "0".

[bit6] TGIES: Trigger Interrupt Request Enable Set Bit

- If "1" is written to this bit, the STC.TGIE bit is set to "1".
- The read value of this bit is always "0".

Bit	Description
0	Invalid
1	Set the TGIE bit.

[bit5] Reserved: Reserved Bit

The read value is "0".

If writing to this bit, write "0".

[bit4] UDIES: Underflow Interrupt Request Enable Set Bit

- If "1" is written to this bit, the STC.UDIE bit is set to "1".
- The read value of this bit is always "0".

Bit	Description
0	Invalid
1	Set the UDIE bit.

[bit3:0] Reserved: Reserved Bits

The read value is "0".

If writing to this bit, write "0".

10.2.8. Low Width Setting Reload Register (PRL)

The Low Width Setting Reload Register (PRL) is the register used to set the "L" width of the PPG output waveform. An underflow at the activation trigger detection time or after the end of "H" width counting causes a transfer to the Timer Register (TMR).

bit	15	8
Field	PRL[15:8]	
R/W Attribute	R/W	
Protection Attribute	-	
Initial Value	XXXXXXXX	

bit	7	0
Field	PRL[7:0]	
R/W Attribute	R/W	
Protection Attribute	-	
Initial Value	XXXXXXXX	

These bits compose the register used to set the "L" width of the PPG output waveform. An underflow at the activation trigger detection time or "H" width count end time causes a transfer to the Timer Register (TMR).

- Use 16- or 32-bit data access for the PRL register.
- After configuring the PPG function with the FMD2 to FMD0 bits in the TMCR register, set the "L" width in the PRL register.

10.2.9. High Width Setting Reload Register (PRLH)

The High Width Setting Reload Register (PRLH) is the register with a buffer used to set the "H" width of the PPG output waveform. An underflow when an activation trigger is detected or after "H" width counting ends causes a transfer from PRLH to the buffer register. An underflow at the "L" width count end time causes a transfer from the buffer register to the Timer Register (TMR).

bit	15	8
Field	PRLH[15:8]	
R/W Attribute	R/W	
Protection Attribute	-	
Initial Value	XXXXXXXX	

bit	7	0
Field	PRLH[7:0]	
R/W Attribute	R/W	
Protection Attribute	-	
Initial Value	XXXXXXXX	

These bits compose the register used to set the "H" width of the PPG output waveform. An underflow at the activation trigger detection time or "H" width count end time causes a transfer from PRLH to the buffer register. An underflow at the "L" width count end time causes a transfer from the buffer register to the Timer Register (TMR).

- Use 16- or 32-bit data access for the PRLH register.
- After configuring the PPG function with the FMD2 to FMD0 bits in the TMCR register, set the "H" width in the PRLH register.

10.2.10. Timer Register (TMR)

The Timer Register (TMR) can read the value of the 16-bit down counter.

bit	15	8
Field	TMR[15:8]	
R/W Attribute	R,WX	
Protection Attribute	-	
Initial Value	00000000	

bit	7	0
Field	TMR[7:0]	
R/W Attribute	R,WX	
Protection Attribute	-	
Initial Value	00000000	

The Timer Register (TMR) can read the value of the 16-bit down counter.

- Use 16- or 32-bit data access for the TMR register.

10.2.11. Base Timer Debug Register (BT_DEBUG)

The Base Timer Debug Register (BT_DEBUG) performs enable/disable setting of debug.

bit	15	8
Field	Reserved	
R/W Attribute	R0,W0	
Protection Attribute	-	
Initial Value	00000000	

bit	7	0
Field	Reserved	DBGEN
R/W Attribute	R0,W0	R/W
Protection Attribute	-	
Initial Value	00000000	0

[bit15:1] Reserved: Reserved Bits

The read value is "0".

If writing to this bit, write "0".

[bit0] DBGEN: Debug Enable Bit

- It is the bit which permits stopping operation of a Base Timer with the debug signal (DEBUG).

Bit	Description
0	Disable
1	Enable

10.2.12. External Timer Compare Data Register (ETCDR)

The External Timer Compare Data Register (ETCDR) is the register which sets the value which is started by an external timer.

bit	15	8
Field	ETCDR[15:8]	
R/W Attribute	R/W	
Protection Attribute	-	
Initial Value	01111111	

bit	7	0
Field	ETCDR[7:0]	
R/W Attribute	R/W	
Protection Attribute	-	
Initial Value	11111111	

It is a register compared with an external timer signal (ETINI). Refer to "10.2.4 External Timer Match Starting" for details.

- Use 16- or 32-bit data access for the ETCDR register.

10.3. Reload Timer Function

Only one of the following timer functions can be selected for the Base Timer in the FMD2 to FMD0 bit settings in the Timer Control Register (TMCR): 16-bit PWM Timer, 16-bit PPG Timer, 16/32-bit Reload Timer, and 16/32-bit PWC Timer. This section explains the timer function with the Reload Timer setting.

10.3.1 Operations of 16-Bit Reload Timer

10.3.2 External Timer Match Starting

10.3.3 Reload Timer Operation Flow

10.3.4 Timer Control Registers (TMCR, TMCR2), Status Control Register (STC), Status Control Clear Register (STCC), and Status Control Set Register (STCS)

10.3.5 Cycle Setting Register (PCSR)

10.3.6 Timer Register (TMR)

10.3.7 Base Timer Debug Register (BT_DEBUG)

10.3.8 External Timer Compare Data Register (ETCDR)

10.3.1. Operations of 16-Bit Reload Timer

The Reload Timer operates by performing a countdown from the set value in the Cycle Setting Register (PCSR), in synchronization with the count clock. When the count value becomes "0", the counting ends, or the timer automatically loads the cycle setting to continue operating until the countdown is stopped.

Count Operation when Internal Clock is Selected

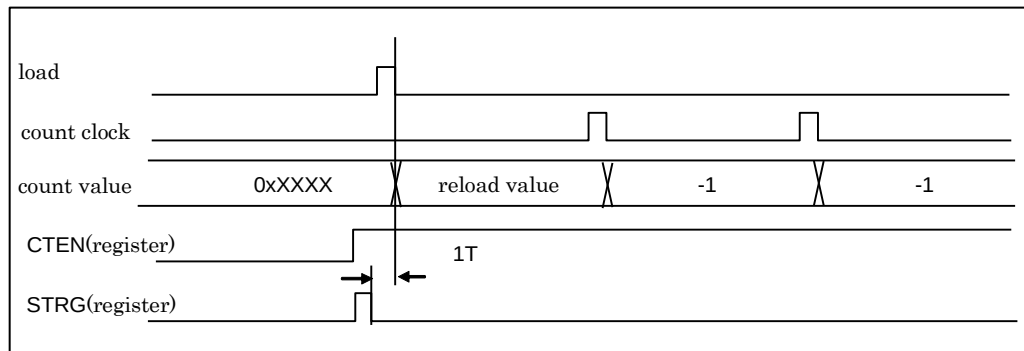
In order to start a count operation and enable counting at the same time, write "1" to both the CTEN bit and STRG bit in the Timer Control Register (TMCR). In a state where the timer has started (CTEN="1"), trigger input with the STRG bit is always enabled regardless of the operation mode.

With count operation enabled, the start of the timer by a software trigger or external trigger results in the Cycle Setting Register (PCSR) value being loaded into the counter and a countdown being started.

The time required from the generation of a counter start trigger until the loading of Cycle Setting Register (PCSR) data into the counter is 1T (T: Internal clock cycle).

Figure 10-22 shows the start and operation of the counter using a software trigger.

Figure 10-22 Count Operation When the Internal Clock Is Selected



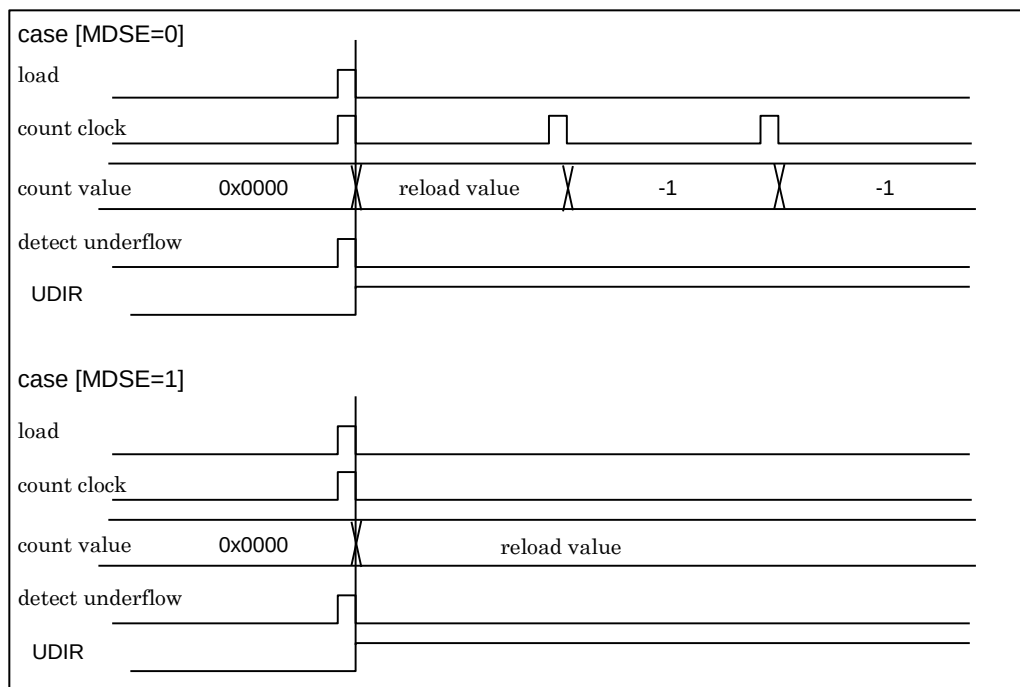
Underflow Operation

If the counter value changes from 0x0000 to 0xFFFF, an underflow has occurred. Therefore, an underflow occurs at the count of [set value of Cycle Setting Register (PCSR) + 1].

The Cycle Setting Register (PCSR) contents are loaded into the counter when an underflow occurs. If the MDSE bit in the Timer Control Register (TMCR) is "0", the count operation continues. If the MDSE bit is "1", the count operation stops with the loaded counter value unchanged.

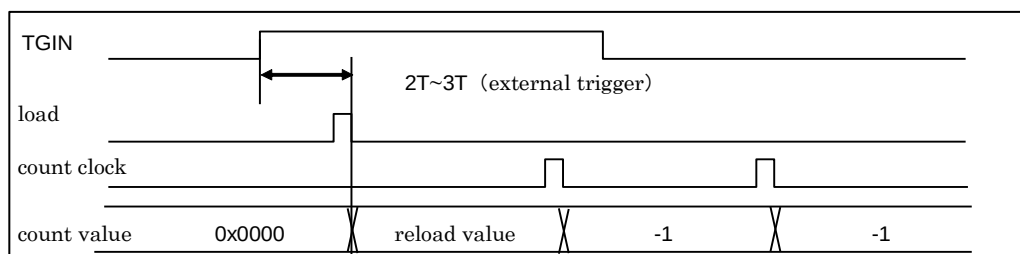
The UDIR bit in the Status Control Register (STC) is set to "1" by an underflow. If the UDIE bit is "1" at this time, an interrupt request is generated.

Figure 10-23 shows an underflow operation timing chart.

Figure 10-23 Underflow Operation Timing Chart**Operation of Input Pin Function**

If the trigger input function (TMCR2.GATE="0") is selected, the TGIN pin can be used as trigger input. When a valid edge is input to the TGIN pin, the Cycle Setting Register (PCSR) contents are loaded into the counter, and a count operation begins. For the period from trigger application until the loading of a counter value, the required time is $2T$ to $3T$ (T : internal clock cycle).

Figure 10-24 shows trigger input operation where the valid edge specification is a rising edge.

Figure 10-24 Trigger Input Operation (TMCR2.GATE="0")

If the gate function (TMCR2.GATE="1") is selected, the TGIN pin can be used as the gate function.

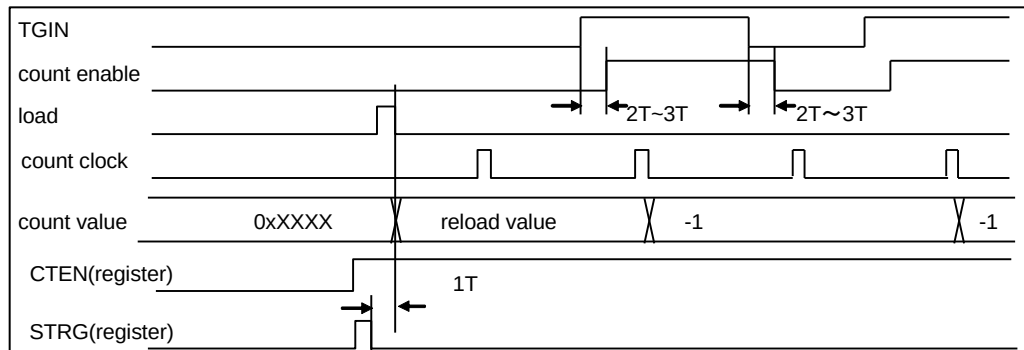
With count operations enabled (TMCR.CTEN="1"), the start of the timer by a software trigger (TMCR.STRG="1") results in the Cycle Setting Register (PCSR) value being loaded into the counter. The count clock counts down only while a valid level is being input to the TGIN pin.

In order to synchronize the signal that is input from the TGIN pin, the time required from the input of a valid level until count enable becomes effective is $2T$ to $3T$ at the start and end of the count operation (T : internal clock cycle).

The gate function and trigger input function are controlled exclusively. Therefore, activation by an external event cannot be used when the gate function is in use.

Figure 10-25 shows gate function operation where the valid level is "H".

Figure 10-25 Gate Function Operation (TMCR2.GATE="1")

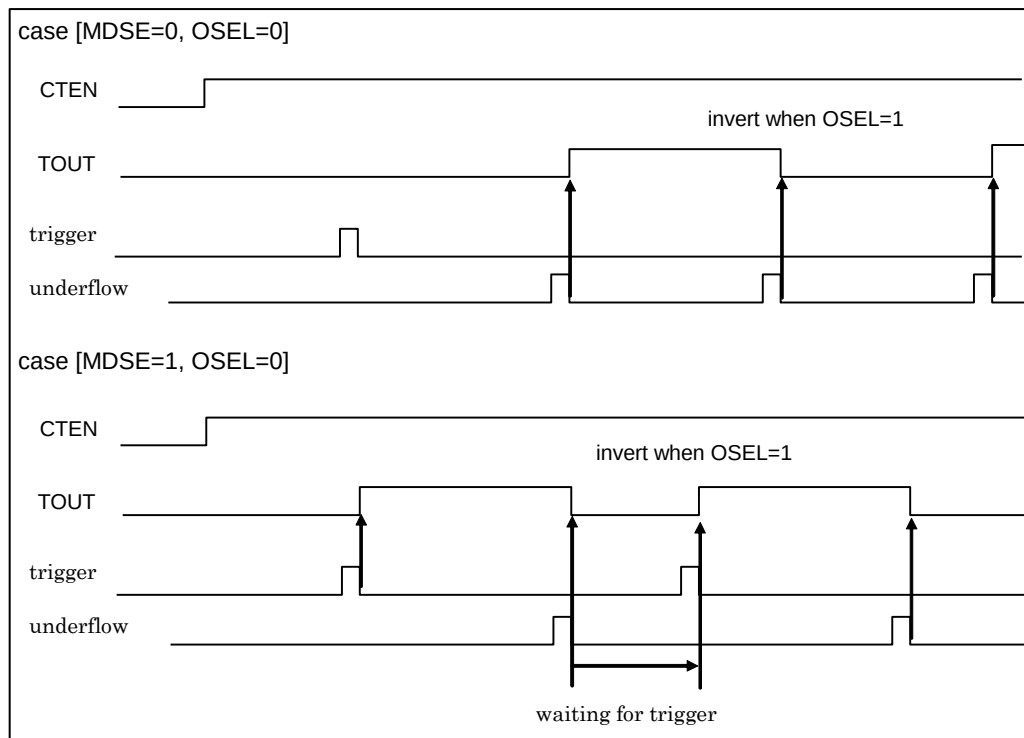


Operation of Output Pin Function

The TOUT output pin functions as toggle output in reload mode and as pulse output in one-shot mode. The toggle output is inverted by an underflow. The pulse output indicates that counting is in progress. The OSEL bit in the Timer Control Register (TMCR) can set the output polarity. If OSEL is "0", the initial value is "0" for toggle output, and "1" is output during counting for one-shot pulse output. If OSEL is "1", the output waveform is inverted.

Figure 10-26 shows an output pin function operation timing chart.

Figure 10-26 Output Pin Function Operation Timing Chart



10.3.2. External Timer Match Starting

If the external timer match starting function is used, the 16/17-bit down counter can start in synchronization with an external timer.

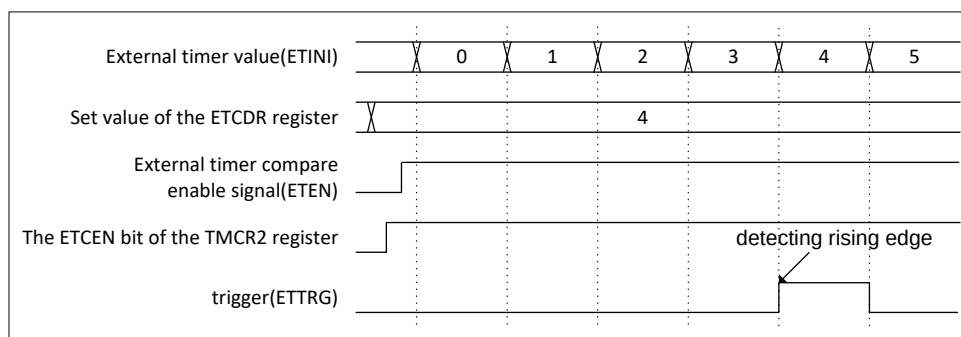
If all the following conditions are satisfied, starting by an external timer is performed.

- The CTEN bit of the TMCR register is "1."
- The ETCEN bit of the TMCR2 register is "1."
- The external timer compare enable signal (ETEN) is active.

When timer is running, the restart by the external timer match starting does not occur. If performing external timer match starting again, perform the following processings.

1. The CTEN bit of the TMCR register is set to "0".
2. The CTEN bit of the TMCR register is set to "1" again.

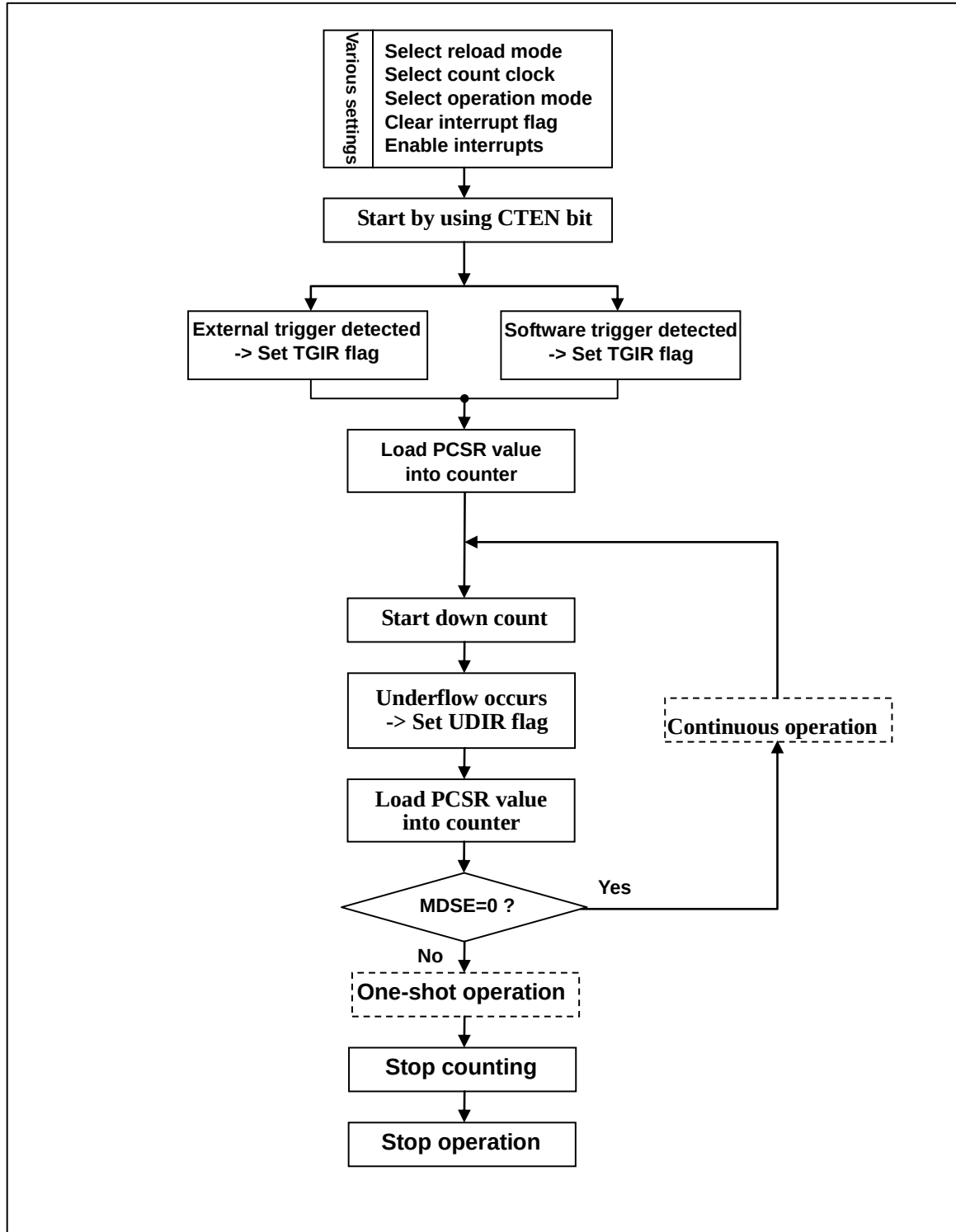
Figure 10-27 The Example of External Timer Match Starting Operation (ETCDR=4)



10.3.3. Reload Timer Operation Flow

This section shows the Reload Timer operation flow.

Reload Timer Operation Flow



10.3.4. Timer Control Registers (TMCR, TMCR2), Status Control Register (STC), Status Control Clear Register (STCC), and Status Control Set Register (STCS)

The Timer Control Register (TMCR) controls timer operation.

For details on writing to the Status Control Register (STC), see "9. Notes on Using the Base Timer".

10.3.4.1 Timer Control Register (Upper Byte of TMCR)

bit	15	14	13	12	11	10	9	8
Field	Reserved	CKS2	CKS1	CKS0	Reserved		EGS1	EGS0
R/W Attribute	R0,W0	R/W	R/W	R/W	R0,W0		R/W	R/W
Protection Attribute	-							
Initial Value	0	0	0	0	0		0	0

[bit15] Reserved: Reserved Bit

The read value is "0".

If writing to this bit, write "0".

[TMCR2:bit0,bit14:12] CKS3 to CKS0: Count Clock Selection Bits

- These bits select a count clock for the 16-bit down counter.
- Any modification to the count clock is reflected immediately after the setting is changed. Therefore, modify CKS3 to CKS0 while counting is stopped (CTEN="0"). However, note that the bits can be modified at the same time as "1" is written to the CTEN bit.

CKS3	CKS2	CKS1	CKS0	Description
0	0	0	0	Internal clock
0	0	0	1	Internal clock divided by 4
0	0	1	0	Internal clock divided by 16
0	0	1	1	Internal clock divided by 128
0	1	0	0	Internal clock divided by 256
0	1	0	1	External clock (rising-edge event)
0	1	1	0	External clock (falling-edge event)
0	1	1	1	External clock (both-edges event)
1	0	0	0	Internal clock divided by 512
1	0	0	1	Internal clock divided by 1024
1	0	1	0	Internal clock divided by 2048
1	0	1	1	Internal clock divided by 2
1	1	0	0	Internal clock divided by 8
1	1	0	1	Internal clock divided by 32
1	1	1	0	Internal clock divided by 64
1	1	1	1	Setting prohibited

[bit11:10] Reserved: Reserved Bits

The read value is "0".

If writing to this bit, write "0".

[bit9:8] EGS1, EGS0: Trigger Input Edge and Gate Function Level Selection Bits

- Trigger input selected (TMCR2.GATE="0")
 - These bits select the valid edge for an input waveform as an external start factor, and they set trigger conditions.
 - For the initial value or the "00" setting, no valid edge is selected for an input waveform, so no external waveform causes a start.
- Gate function selected (TMCR2.GATE="1")
 - These bits select a valid level corresponding to an input waveform as an external count factor, and the down counter counts down only while the selected level is valid.

Note:

- If "1" is written to the STRG bit, the software trigger becomes valid regardless of the EGS1 and EGS0 settings.

- Modify EGS1 and EGS0 while counting is stopped (CTEN="0"). However, note that the bits can be modified at the same time as "1" is written to the CTEN bit.

EGS1	EGS0	Description	
		Trigger Input Selected (TMCR2.GATE="0")	Gate Function Selected (TMCR2.GATE="1")
0	0	Trigger input invalid	"L" level
0	1	External trigger(rising edge)	"H" level
1	0	External trigger(falling edge)	"L" level
1	1	External trigger(both edges)	"H" level

10.3.4.2 Timer Control Register (Lower Byte of TMCR)

bit	7	6	5	4	3	2	1	0
Field	T32	FMD2	FMD1	FMD0	OSEL	MDSE	CTEN	STRG
R/W Attribute	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R0,W
Protection Attribute	-							
Initial Value	0	0	0	0	0	0	0	0

[bit7] T32: 32-Bit Timer Selection Bit

- This bit selects the 32-bit timer function.
- If the Reload Timer function is selected with "011" set in the FMD2 to FMD0 bits, setting the T32 bit to "1" results in operation in 32-bit timer mode.
- Modify these bits while the timer is stopped (CTEN="0"). However, note that the bit can be modified at the same time as "1" is written to the CTEN bit. (See "4. 32-Bit Mode Operation")

Bit	Description
0	16-bit timer mode
1	32-bit timer mode

[bit6:4] FMD2 to FMD0: Timer Function Selection Bits

- These bits select the timer function.
- If "011" is set in the FMD2 to FMD0 bits, the Reload Timer function is selected.
- Modify these bits while the timer is stopped (CTEN="0"). However, note that the bits can be modified at the same time as "1" is written to the CTEN bit.

FMD2	FMD1	FMD0	Description
0	0	0	Reset mode
0	0	1	16-bit PWM Timer
0	1	0	16-bit PPG Timer
0	1	1	16/32-bit Reload Timer
1	0	0	16/32-bit PWC Timer
Other than above			Setting prohibited

[bit3] OSEL: Output Polarity Specification Bit

- This bit selects either normal or inverse output as the timer output level.
- When combined with the mode selection bit (bit2 MDSE), this bit generates an output waveform as follows.

MDSE	OSEL	Output Waveform
0	0	Toggle output with "L" at count start time
0	1	Toggle output with "H" at count start time
1	0	Rectangular output of "H" during counting
1	1	Rectangular output of "L" during counting

Bit	Description
0	Normal polarity
1	Inverse polarity

[bit2] MDSE: Mode Selection Bit

- If the MDSE bit is set to "0", reload mode is selected. The Cycle Setting Register (PCSR) value is loaded into the counter at the same time that the count value underflows from 0x0000 to 0xFFFF, and the count operation continues.
- If the MDSE bit is set to "1", one-shot mode is selected. When the count value underflows from 0x0000 to 0xFFFF, operation stops.
- Modify these bits while the timer is stopped (CTEN="0"). However, note that the bits can be modified at the same time as "1" is written to the CTEN bit.

Bit	Description
0	Reload mode
1	One-shot mode

[bit1] CTEN: Timer Enable Bit

- This bit enables operation of the down counter.
- If "0" is written to this bit when counter operation is enabled (CTEN bit is "1"), the counter stops.

Bit	Description
0	Stop operation.
1	Enable operation.

[bit0] STRG: Software Trigger Bit

- If "1" is written to the STRG bit when the CTEN bit is "1", a software trigger is applied.
- The read value of the STRG bit is always "0".

Notes:

- Even if "1" is written to the CTEN and STRG bits at the same time, a software trigger is applied.
- If "1" is written to the STRG bit, the software trigger becomes valid regardless of the EGS1 and EGS0 settings.

Bit	Description
0	Invalid
1	Startup by software

10.3.4.3 Timer Control Register 2 (TMCR2)

bit	7	6	5	4	3	2	1	0
Field	GATE	Reserved					ETCEN	CKS3
R/W Attribute	R/W	R0,W0					R/W	R/W
Protection Attribute	-							
Initial Value	0	00000					0	0

[bit7] GATE: Gate Input Enable Bit

This bit selects whether to use the external factor pin for the trigger input function or gate function during Reload Timer operation.

- Trigger input function: A countdown begins when a valid edge is input to the external factor pin.
- Gate function: A countdown is performed only while a valid level is being input to the external factor pin.

After configuring the Reload Timer function with the FMD2 to FMD0 bits in the TMCR register, set the GATE bit.

Bit	Description
0	Trigger input function
1	Gate function

[bit6:2] Reserved: Reserved Bits

The read value is "0".

If writing to this bit, write "0".

[bit1] ETCEN: External Timer Compare Enable Bit

It is the bit which enables match detection of an external timer value and the ETCDR register value.

Bit	Description
0	Match detection disable
1	Match detection enable

[bit0] CKS3: Count Clock Selection Bit

See "Count clock selection bits" in "10.3.4 Timer Control Registers (TMCR, TMCR2), Status Control Register (STC), Status Control Clear Register (STCC), and Status Control Set Register (STCS)"

10.3.4.4 Status Control Register (STC)

bit	7	6	5	4	3	2	1	0
Field	Reserved	TGIE	Reserved	UDIE	Reserved	TGIR	Reserved	UDIR
R/W Attribute	R0,W0	R/W	R0,W0	R/W	R0,W0	R,WX	R0,W0	R,WX
Protection Attribute	-							
Initial Value	0	0	0	0	0	0	0	0

[bit7] Reserved: Reserved Bit

The read value is "0".

If writing to this bit, write "0".

[bit6] TGIE: Trigger Interrupt Request Enable Bit

- This bit controls interrupt requests of the trigger interrupt request bit (bit2 TGIR).
- If the TGIE bit is enabled and the TGIR bit is set to "1", an interrupt request is issued to the CPU.
- Writing "1" to the STCC.TGIEC bit clears this bit.
- Writing "1" to the STCS.TGIES bit sets this bit.

Bit	Description
0	Disable interrupt requests.
1	Enable interrupt requests.

[bit5] Reserved: Reserved Bit

The read value is "0".

If writing to this bit, write "0".

[bit4] UDIE: Underflow Interrupt Request Enable Bit

- This bit controls interrupt requests of the underflow interrupt request bit (bit0 UDIR).
- If the UDIE bit is enabled and the UDIR bit is set to "1", an interrupt request is issued to the CPU.
- Writing "1" to the STCC.UDIEC bit clears this bit.
- Writing "1" to the STCS.UDIES bit sets this bit.

Bit	Description
0	Disable interrupt requests.
1	Enable interrupt requests.

[bit3] Reserved: Reserved Bit

The read value is "0".

If writing to this bit, write "0".

[bit2] TGIR: Trigger Interrupt Request Bit

- The TGIR bit is set to "1" when a software trigger or trigger input is detected.
- Writing "1" to the STCC.TGIRC bit clears this bit.
- This bit is read-only. Writing data to this bit has no effect on operation.

Bit	Description
0	The interrupt factor is cleared.
1	Detect the interrupt factor.

[bit1] Reserved: Reserved Bit

The read value is "0".

If writing to this bit, write "0".

[bit0] UDIR: Underflow Interrupt Request Bit

- The UDIR bit is set to "1" when the count value underflows and changes from 0x0000 to 0xFFFF.
- Writing "1" to the STCC.UDIRC bit clears this bit.
- This bit is read-only. Writing data to this bit has no effect on operation.

Bit	Description
0	The interrupt factor is cleared.
1	Detect the interrupt factor.

10.3.4.5 Status Control Clear Register (STCC)

bit	7	6	5	4	3	2	1	0
Field	Reserved	TGIEC	Reserved	UDIEC	Reserved	TGIRC	Reserved	UDIRC
R/W Attribute	R0,W0	R0,W	R0,W0	R0,W	R0,W0	R0,W	R0,W0	R0,W
Protection Attribute	-							
Initial Value	0	0	0	0	0	0	0	0

[bit7] Reserved: Reserved Bit

The read value is "0".

If writing to this bit, write "0".

[bit6] TGIEC: Trigger Interrupt Request Enable Clear Bit

- If "1" is written to this bit, the STC.TGIE bit is cleared to "0".
- The read value of this bit is always "0".

Bit	Description
0	Invalid
1	Clear the TGIE bit.

[bit5] Reserved: Reserved Bit

The read value is "0".

If writing to this bit, write "0".

[bit4] UDIEC: Underflow Interrupt Request Enable Clear Bit

- If "1" is written to this bit, the STC.UDIE bit is cleared to "0".
- The read value of this bit is always "0".

Bit	Description
0	Invalid
1	Clear the UDIE bit.

[bit3] Reserved: Reserved Bit

The read value is "0".

If writing to this bit, write "0".

[bit2] TGIRC: Trigger Interrupt Request Clear Bit

- If "1" is written to this bit, the STC.TGIR bit is cleared to "0".
- The read value of this bit is always "0".

Bit	Description
0	Invalid
1	Clear the TGIR bit.

[bit1] Reserved: Reserved Bit

The read value is "0".

If writing to this bit, write "0".

[bit0] UDIRC: Underflow Interrupt Request Clear Bit

- If "1" is written to this bit, the STC.UDIR bit is cleared to "0".
- The read value of this bit is always "0".

Bit	Description
0	Invalid
1	Clear the UDIR bit.

10.3.4.6 Status Control Set Register (STCS)

bit	7	6	5	4	3	2	1	0
Field	Reserved	TGIES	Reserved	UDIES	Reserved			
R/W Attribute	R0,W0	R0,W	R0,W0	R0,W	R0,W0			
Protection Attribute	-							
Initial Value	0	0	0	0	0000			

[bit7] Reserved: Reserved Bit

The read value is "0".

If writing to this bit, write "0".

[bit6] TGIES: Trigger Interrupt Request Enable Set Bit

- If "1" is written to this bit, the STC:TGIE bit is set to "1".
- The read value of this bit is always "0".

Bit	Description
0	Invalid
1	Set the TGIE bit.

[bit5] Reserved: Reserved Bit

The read value is "0".

If writing to this bit, write "0".

[bit4] UDIES: Underflow Interrupt Request Enable Set Bit

- If "1" is written to this bit, the STC:UDIE bit is set to "1".
- The read value of this bit is always "0".

Bit	Description
0	Invalid
1	Set the UDIE bit.

[bit3:0] Reserved: Reserved Bits

The read value is "0".

If writing to this bit, write "0".

10.3.5. Cycle Setting Register (PCSR)

The Cycle Setting Register (PCSR) is a register that retains the initial count value. In 32-bit mode, if this is an even-numbered channel, this will display the initial value of the lower 16-bit count. If this is an odd-numbered channel, this will display the initial value of the upper 16-bit count. The initial value at the reset time is undefined. Be sure to access this register with 16- or 32-bit data transfer instructions.

bit	15	14	13	12	11	10	9	8
Field	PCSR[15:8]							
R/W Attribute	R/W							
Protection Attribute	-							
Initial Value	XXXXXXXX							

bit	7	6	5	4	3	2	1	0
Field	PCSR[7:0]							
R/W Attribute	R/W							
Protection Attribute	-							
Initial Value	XXXXXXXX							

These bits compose the register used to set a cycle. An underflow causes a transfer to the Timer Register.

- Use 16- or 32-bit data access for the PCSR register.
- After configuring the Reload Timer function with the FMD2 to FMD0 bits in the TMCR register, set a cycle in the PCSR register.
- To write data to the PCSR register in 32-bit mode, access first the upper 16-bit data (data for the odd-numbered channel) and then the lower 16-bit data (data for the even-numbered channel).

10.3.6. Timer Register (TMR)

The Timer Register (TMR) is a register that can read the count value of a timer. In 32-bit mode, if this is an even-numbered channel, this will display the value of the lower 16-bit count. If this is an odd-numbered channel, this will display the value of the upper 16-bit count. The initial value is undefined.

Be sure to read this register with 16- or 32-bit data transfer instructions.

bit	15	14	13	12	11	10	9	8
Field	TMR[15:8]							
R/W Attribute	R,WX							
Protection Attribute	-							
Initial Value	XXXXXXXX							

bit	7	6	5	4	3	2	1	0
Field	TMR[7:0]							
R/W Attribute	R,WX							
Protection Attribute	-							
Initial Value	XXXXXXXX							

The Timer Register (TMR) can read the value of the 16-bit down counter.

- Use 16- or 32-bit data access for the TMR register.
- To read the TMR register in 32-bit mode, access first the lower 16-bit data (data for the even-numbered channel) and then the upper 16-bit data (data for the odd-numbered channel).

10.3.7. Base Timer Debug Register (BT_DEBUG)

The Base Timer Debug Register (BT_DEBUG) performs enable/disable setting of debug.

bit	15	14	13	12	11	10	9	8
Field	Reserved							
R/W Attribute	R0,W0							
Protection Attribute	-							
Initial Value	00000000							

bit	7	6	5	4	3	2	1	0
Field	Reserved							DBGEN
R/W Attribute	R0,W0							R/W
Protection Attribute	-							
Initial Value	00000000							0

[bit15:1] Reserved: Reserved Bits

The read value is "0".

If writing to this bit, write "0".

[bit0] DBGEN: Debug Enable Bit

- It is the bit which permits stopping operation of a Base Timer with the debug signal (DEBUG).

Bit	Description
0	Disable
1	Enable

10.3.8. External Timer Compare Data Register (ETCDR)

The External Timer Compare Data Register (ETCDR) is the register which sets the value which is started by an external timer.

bit	15	14	13	12	11	10	9	8
Field	ETCDR[15:8]							
R/W Attribute	R/W							
Protection Attribute	-							
Initial Value	01111111							

bit	7	6	5	4	3	2	1	0
Field	ETCDR[7:0]							
R/W Attribute	R/W							
Protection Attribute	-							
Initial Value	11111111							

It is a register compared with an external timer signal (ETINI). Refer to "10.3.2 External Timer Match Starting" for details.

- Use 16- or 32-bit data access for the ETCDR register.

10.4. PWC Timer Function

Only one of the following timer functions can be selected for the Base Timer in the FMD2 to FMD0 bit settings in the Timer Control Register (TMCR): 16-bit PWM Timer, 16-bit PPG Timer, 16/32-bit Reload Timer, and 16/32-bit PWC Timer. This section explains the timer function with the PWC setting.

10.4.1 Operations of PWC Timer

10.4.2 Timer Control Registers (TMCR, TMCR2), Status Control Register (STC), Status Control Clear Register (STCC), and Status Control Set Register (STCS)

10.4.3 Data Buffer Register (DTBF)

10.4.4 Base Timer Debug Register (BT_DEBUG)

10.4.1. Operations of PWC Timer

The PWC Timer has a pulse width measurement function. The timer can select 12 types of count clocks, and it can measure the time and cycle between any input pulse events by using a counter. This section shows the basic functions/operations of the pulse width measurement function.

10.4.1.1 Pulse Width Measurement Function

After the start, the function does not perform a count operation until the counter is cleared to 0x0000 and the set measurement start edge is input. The function starts counting up from 0x0001 when the measurement start edge is detected. It stops counting when the measurement end edge is detected. The count value at this time is stored as a pulse width in the register.

An interrupt request can be generated at the measurement end time and at the overflow occurrence time.

After measurement ends, the function operates according to the measurement mode as follows.

- In single measurement mode: It stops operating.
- In continuous measurement mode: It first transfers the counter value to the buffer register and then stops counting until the measurement start edge is input again.

Figure 10-28 Pulse Width Measurement Operation (Single Measurement Mode/"H" Width Measurement)

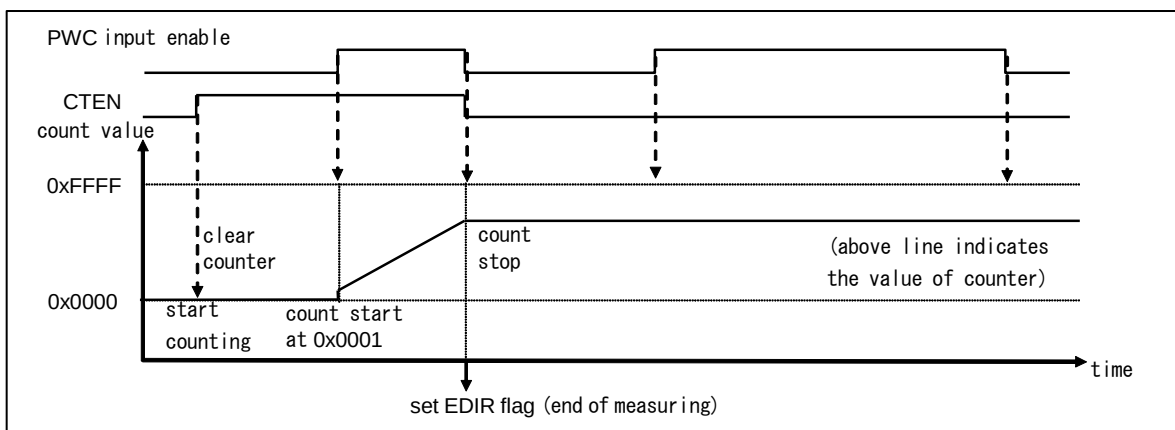
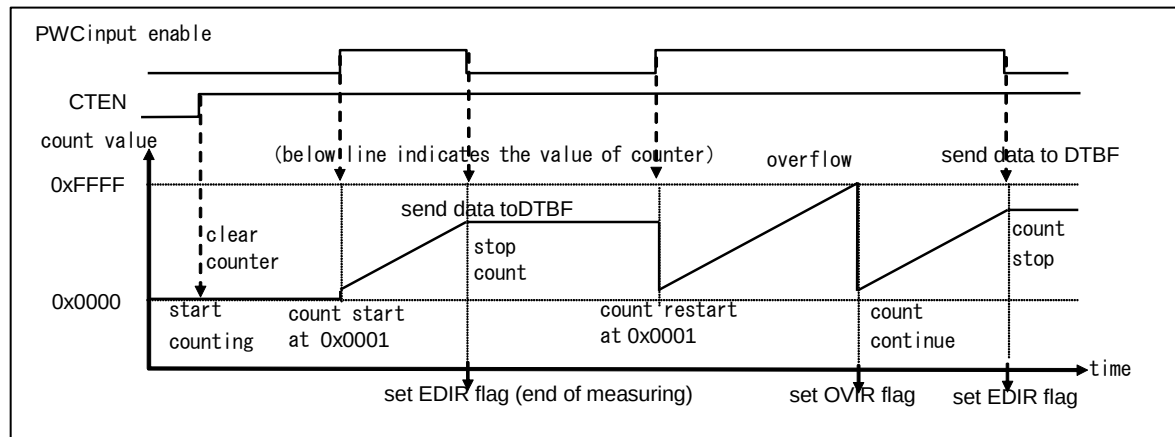


Figure 10-29 Pulse Width Measurement Operation (Continuous Measurement Mode/"H" Width Measurement)



10.4.1.2 Selection of Count Clock

12 types of count clocks can be selected for the counter through the setting of TMC2 register bit0 (CKS3) and TMC2 register bit14 to 12 (CKS2, CKS1, and CKS0).

The following count clocks can be selected.

TMC2 and TMC2 Registers	Internal Count Clock Selected
CKS3, CKS2, CKS1, and CKS0 Bits	
0000	Internal clock [initial value]
0001	Internal clock divided by 4
0010	Internal clock divided by 16
0011	Internal clock divided by 128
0100	Internal clock divided by 256
0101	Setting prohibited
0110	
0111	
1000	Internal clock divided by 512
1001	Internal clock divided by 1024
1010	Internal clock divided by 2048
1011	Internal clock divided by 2
1100	Internal clock divided by 8
1101	Internal clock divided by 32
1110	Internal clock divided by 64
1111	Setting prohibited

The initial value selected after a reset is the internal clock.

Be sure to select a count clock before starting the counter.

10.4.1.3 Selection of Operation Mode

To select each operation mode/measurement mode, set TMCR.

Operation mode setting ... TMCR bit10 to 8: EGS2, EGS1, EGS0 (Select a measurement edge.)

Measurement mode setting ... TMCR bit2: MDSE (Select single measurement/continuous measurement.)

The following table lists a selection of operation modes.

Operation Mode		MDSE	EGS2	EGS1	EGS0
Rising to falling H pulse width measurement	Continuous measurement mode: Buffer enabled	0	0	0	0
	Single measurement mode: Buffer disabled	1	0	0	0
Rising to rising Cycle measurement between rising edges	Continuous measurement mode: Buffer enabled	0	0	0	1
	Single measurement mode: Buffer disabled	1	0	0	1
Falling to falling Cycle measurement between falling edges	Continuous measurement mode: Buffer enabled	0	0	1	0
	Single measurement mode: Buffer disabled	1	0	1	0
Measurement between rising to falling or falling to rising	Continuous measurement mode: Buffer enabled	0	0	1	1
	Single measurement mode: Buffer disabled	1	0	1	1
Falling to rising L pulse width measurement	Continuous measurement mode: Buffer enabled	0	1	0	0
	Single measurement mode: Buffer disabled	1	1	0	0
Setting prohibited		0	1	0	1
		1	1	0	1
		0	1	1	0
		1	1	1	0
		0	1	1	1
		1	1	1	1

The initial values selected after a reset are "H" pulse width measurement and continuous measurement mode.

Be sure to select an operation mode before starting the counter.

10.4.1.4 Starting and Stopping Pulse Width Measurement

To start/restart/forcibly stop each operation, set bit1 (CTEN bit) in TMCR.

Pulse width measurement is started/restarted by the writing of "1" to the CTEN bit and forcibly stopped by the writing of "0" to the CTEN bit.

CTEN	Function
1	Start/Restart pulse width measurement.
0	Stop pulse width measurement.

10.4.1.5 Post-Start Operation

The operations after the start of pulse width measurement mode do not include counting until the measurement start edge is input. After the detection of the measurement start edge, the 16-bit up counter starts counting from 0x0001.

10.4.1.6 Restart

After the start, a repeated start performed during operation (writing "1" again in a state where the CTEN bit is "1") is called a "restart." The operation in any such restart is described below.

- In the measurement start edge wait state:
There is no effect on operation.
- During measurement:
The count is cleared to 0x0000. Then, the measurement start edge wait state begins again. If the measurement end edge is detected at the same time as a restart, the measurement end flag (EDIR) is set to "1". Then, if the mode is continuous measurement mode, the measurement results are transferred to DTBF.

10.4.1.7 About Stopping

In single measurement mode, the count operation is automatically stopped by a counter overflow or the end of measurement, so stopping it does not need to be a concern. In continuous measurement mode, to stop counting before counting is automatically stopped, you need to forcibly stop it.

10.4.1.8 Counter Clearing and Initial Value

The 16-bit up counter is cleared to 0x0000 in the following cases.

- Upon a reset
- When "1" is written to bit1 (CTEN bit) in TMCR (even including restart times)

The 16-bit up counter is initialized to 0x0001 in the following case.

- When the measurement start edge is detected

10.4.1.9 Pulse Width Measurement Operation Details

Single Measurement and Continuous Measurement

The modes for pulse width measurement are a mode where measurement is 1-time only and a mode where measurement is continuous. Each mode is selected with the MDSE bit in TMCR. (See "10.4.1.3 Selection of Operation Mode") The modes differ as described below.

Single measurement mode:

The first input of the measurement end edge stops the counting by the counter and sets the measurement end flag (EDIR) in STC to "1". No subsequent measurements are made. However, if a restart is performed at the same time, the mode enters the measurement start wait state.

Continuous measurement mode:

The input of the measurement end edge stops the counting by the counter and sets the measurement end flag (EDIR) in STC to "1". The counting remains stopped until the measurement start edge is input again. The counter is initialized to 0x0001 and measurement begins when the measurement start edge is input again. The measurement results of the counter are transferred to DTBF at the measurement end time.

Be sure to select/change the measurement mode while the counter is stopped.

Measurement Result Data

The handling of measurement results and counter values and the function of DTBF differ between single measurement mode and continuous measurement mode. The measurement results from each mode differ as described below.

Single measurement mode:

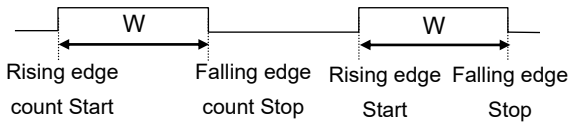
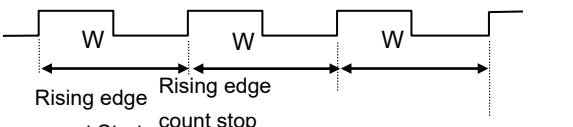
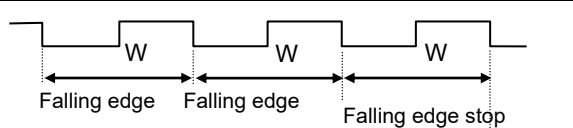
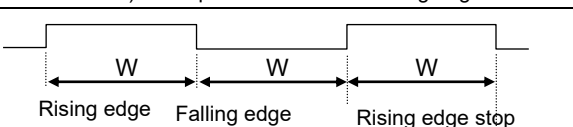
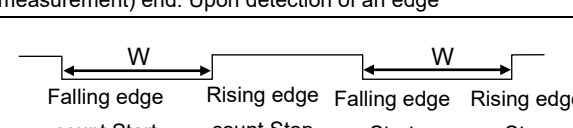
If DTBF is read during operation, the count value being measured is obtained.
 If DTBF is read after measurement ends, the measurement result data is obtained.

Continuous measurement mode:

The measurement results of the counter are transferred to DTBF at the measurement end time. The immediately preceding measurement results are obtained when DTBF is read, and the last measurement results are retained even during a measurement operation. The count value being measured cannot be read.
 In continuous measurement mode, if the next measurement ends before the measurement results are read, the last measurement results are overwritten by the new measurement results. In such cases, the error flag (ERR) is set to "1" in STC. The error flag (ERR) is automatically cleared when DTBF is read.

Measurement Modes and Count Operations

The measurement mode can be selected from the following 5 types, depending on which part of the input pulse is measured. The following table explains them.

Measurement Mode	EGS2, 1, 0	Measurement Description (W: Pulse Width Measured)
"H" pulse width measurement	000	 The width of the "H" period is measured. Count (measurement)start: Upon detection of a rising edge Count (measurement)end: Upon detection of a falling edge
Cycle measurement between rising edges	001	 The cycle between rising edges is measured. Count (measurement)start: Upon detection of a rising edge Count (measurement) end: Upon detection of a rising edge
Cycle measurement between falling edges	010	 The cycle between falling edges is measured. Count (measurement) start: Upon detection of a falling edge Count (measurement)end: Upon detection of a falling edge
Pulse width measurement between all edges	011	 The width between continuously input edges is measured. Count (measurement) start: Upon detection of an edge Count (measurement) end: Upon detection of an edge
"L" pulse width measurement	100	 The width of the "L" period is measured. Count (measurement) start: Upon detection of a falling edge Count (measurement) end: Upon detection of a rising edge

Regardless of the measurement mode, after the counter is cleared to 0x0000 by the start of measurement, the counter does not do any counting until the measurement start edge is input. From the input of the measurement start edge, the counter continues counting up for each count clock until the measurement end edge is input.

For measurements such as pulse width measurement and cycle measurement between all edges in continuous measurement mode, the end edge is the next measurement start edge.

Pulse Width/Cycle Calculation Method

The method of calculating the pulse width/cycle from the obtained measurement result data in DTBF after measurement ends is shown below.

$$Tw = n \times t$$

Tw: Measured pulse width/cycle

n: Measurement result data in DTBF

t: Count clock cycle

Interrupt Request Generation

The following two interrupt requests can be generated.

■ Interrupt request due to a counter overflow

If counting up during measurement causes an overflow, the overflow flag (OVIR) is set to "1".

Furthermore, if overflow interrupt requests are enabled, an interrupt request is generated.

■ Interrupt request due to measurement end

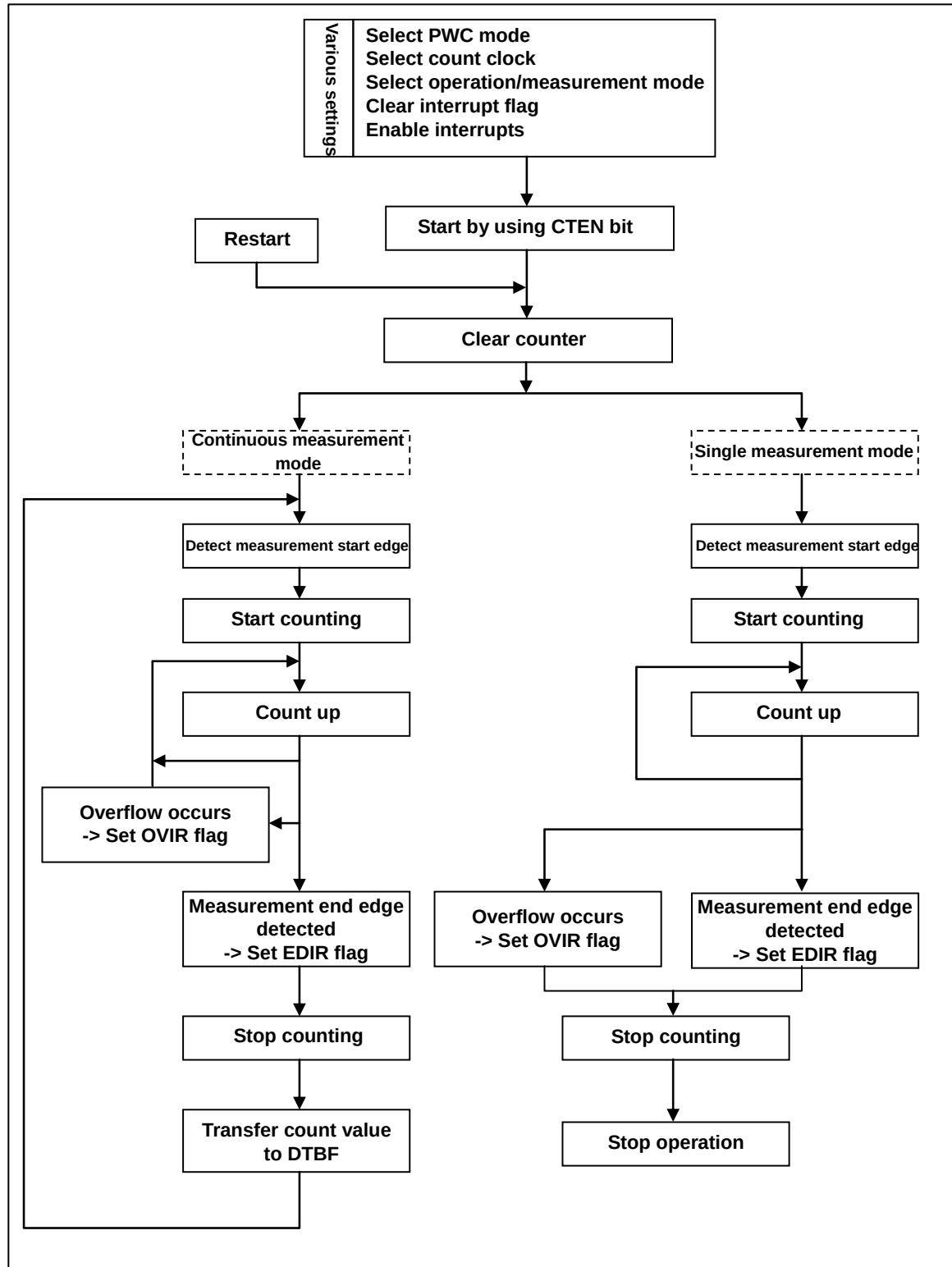
If the measurement end edge is detected, the measurement end flag (EDIR) in STC is set to "1".

Furthermore, if measurement end interrupt requests are enabled, an interrupt request is generated.

The measurement end flag (EDIR) is automatically cleared by the reading of the measurement results, DTBF.

Pulse Width Measurement Operation Flow

Figure 10-30 Pulse Width Measurement Operation Flow



10.4.2. Timer Control Registers (TMCR, TMCR2), Status Control Register (STC), Status Control Clear Register (STCC), and Status Control Set Register (STCS)

The Timer Control Register (TMCR) controls timer operation.

For details on writing to the Status Control Register (STC), see "9. Notes on Using the Base Timer".

10.4.2.1 Timer Control Register (Upper Byte of TMCR)

Bit	15	14	13	12	11	10	9	8
Field	Reserved	CKS2	CKS1	CKS0	Reserved	EGS2	EGS1	EGS0
R/W Attribute	R0,W0	R/W	R/W	R/W	R0,W0	R/W	R/W	R/W
Protection Attribute	-							
Initial Value	0	0	0	0	0	0	0	0

[bit15] Reserved: Reserved Bit

The read value is "0".

If writing to this bit, write "0".

[TMCR2:bit0,bit14:12] CKS3 to CKS0: Count Clock Selection Bits

- These bits select a count clock for the 16-bit down counter.
- Any modification to the count clock is reflected immediately after the setting is changed. Therefore, modify CKS3 to CKS0 while counting is stopped (CTEN="0"). However, note that the bits can be modified at the same time as "1" is written to the CTEN bit.

CKS3	CKS2	CKS1	CKS0	Description
0	0	0	0	Internal clock
0	0	0	1	Internal clock divided by 4
0	0	1	0	Internal clock divided by 16
0	0	1	1	Internal clock divided by 128
0	1	0	0	Internal clock divided by 256
0	1	0	1	Setting prohibited
0	1	1	0	
0	1	1	1	
1	0	0	0	Internal clock divided by 512
1	0	0	1	Internal clock divided by 1024
1	0	1	0	Internal clock divided by 2048
1	0	1	1	Internal clock divided by 2
1	1	0	0	Internal clock divided by 8
1	1	0	1	Internal clock divided by 32
1	1	1	0	Internal clock divided by 64
1	1	1	1	Setting prohibited

[bit11] Reserved: Reserved Bit

The read value is "0".

If writing to this bit, write "0".

[bit10:8] EGS2 to EGS0: Measurement Edge Selection Bits

- These bits set a measurement edge condition.
- Modify EGS2 to EGS0 while counting is stopped (CTEN="0"). However, note that the bits can be modified at the same time as "1" is written to the CTEN bit.

EGS2	EGS1	EGS0	Description
0	0	0	"H" pulse width measurement (rising to falling)
0	0	1	Cycle measurement between rising edges (rising to rising)
0	1	0	Cycle measurement between falling edges (falling to falling)
0	1	1	Pulse width measurement between all edges (rising or falling to falling or rising)
1	0	0	"L" pulse width measurement (falling to rising)
1	0	1	Setting prohibited
1	1	0	
1	1	1	

10.4.2.2 Timer Control Register (Lower Byte of TMCR)

bit	7	6	5	4	3	2	1	0
Field	T32	FMD2	FMD1	FMD0	Reserved	MDSE	CTEN	Reserved
R/W Attribute	R/W	R/W	R/W	R/W	R0,W0	R/W	R,W	R0,W0
Protection Attribute	-							
Initial Value	0	0	0	0	0	0	0	0

[bit7] T32: 32-Bit Timer Selection Bit

- This bit selects the 32-bit timer function.
- If the PWC function is selected with "100" set in the FMD2 to FMD0 bits, setting the T32 bit to "1" results in operation in 32-bit PWC mode.
- Modify these bits while the timer is stopped (CTEN="0"). However, note that the bit can be modified at the same time as "1" is written to the CTEN bit. (See 32-Bit Mode Operation.)

Bit	Description
0	16-bit timer mode
1	32-bit timer mode

[bit6:4] FMD2 to FMD0: Timer Function Selection Bits

- These bits select the timer function.
- If "100" is set in the FMD2 to FMD0 bits, the PWC Timer function is selected.
- Modify these bits while the timer is stopped (CTEN="0"). However, note that the bits can be modified at the same time as "1" is written to the CTEN bit.

FMD2	FMD1	FMD0	Description
0	0	0	Reset mode
0	0	1	16-bit PWM Timer
0	1	0	16-bit PPG Timer
0	1	1	16/32-bit Reload Timer
1	0	0	16/32-bit PWC Timer
1	0	1	Setting prohibited
1	1	0	
1	1	1	

[bit3] Reserved: Reserved Bit

The read value is "0".

If writing to this bit, write "0".

[bit2] MDSE: Mode Selection Bit

- Modify these bits while the timer is stopped (CTEN="0"). However, note that the bits can be modified at the same time as "1" is written to the CTEN bit.

Bit	Description
0	Continuous measurement mode (buffer register enabled)
1	Single measurement mode (stop after 1 measurement)

[bit1] CTEN: Timer Enable Bit

- This bit enables the starting or restarting of the up counter.
- If "1" is written with the counter in the operation enabled state (CTEN bit is "1"), a restart is assumed, the counter is cleared, and operation enters the measurement start edge wait state.
- If "0" is written to this bit when counter operation is enabled (CTEN bit is "1"), the counter stops.
- After measurement ends in single measurement mode, CTEN is cleared.

Bit	Description
0	Stop operation.
1	Enable operation.

Note:

- During timer operation of I/O mode 6 or I/O mode 4, if the falling edge is output from the even-numbered channel, this bit of the odd-numbered channel is cleared to "0".

[bit0] Reserved: Reserved Bit

The read value is "0".

If writing to this bit, write "0".

10.4.2.3 Timer Control Register 2 (TMCR2)

bit	7	6	5	4	3	2	1	0
Field	Reserved							CKS3
R/W Attribute	R0,W0							R/W
Protection Attribute	-							
Initial Value	0000000							0

[bit7:1] Reserved: Reserved Bits

The read value is "0".

If writing to this bit, write "0".

[bit0] CKS3: Count Clock Selection Bit

See "Count clock selection bits" in "10.4.2 Timer Control Registers (TMCR, TMCR2), Status Control Register (STC), Status Control Clear Register (STCC), and Status Control Set Register (STCS)"

10.4.2.4 Status Control Register (STC)

bit	7	6	5	4	3	2	1	0
Field	ERR	EDIE	Reserved	OVIE	Reserved	EDIR	Reserved	OVIR
R/W Attribute	R,WX	R/W	R0,W0	R/W	R0,W0	R,WX	R0,W0	R,WX
Protection Attribute	-							
Initial Value	0	0	0	0	0	0	0	0

[bit7] ERR: Error Flag Bit

- This bit is a flag indicating that, in continuous measurement mode, the next measurement has ended before the measurement results in the DTBF register have been read. In this case, the DTBF register values are updated with the new measurement results, so the immediately preceding measurement results are lost.
- Measurement continues regardless of the ERR bit value.
- The ERR bit is read-only. Writing to the bit has no effect on the bit value.
- Reading the measurement results (DTBF) clears the ERR bit.

Bit	Description
0	Normal state
1	Overwrite any unread measurement results with the next measurement results.

[bit6] EDIE: Measurement End Interrupt Request Enable Bit

- This bit controls interrupt requests of the measurement end interrupt request bit (bit2 EDIR).
- If the EDIE bit is enabled and the EDIR bit is set to "1", an interrupt request is issued to the CPU.
- Writing "1" to the STCC.EDIEC bit clears this bit.
- Writing "1" to the STCS.EDIES bit sets this bit.

Bit	Description
0	Disable interrupt requests.
1	Enable interrupt requests.

[bit5] Reserved: Reserved Bit

The read value is "0".

If writing to this bit, write "0".

[bit4] OVIE: Overflow Interrupt Request Enable Bit

- This bit controls interrupt requests of the overflow interrupt request bit (bit0 OVIR).
- If the OVIE bit is enabled and the OVIR bit is set to "1", an interrupt request is issued to the CPU.
- Writing "1" to the STCC.OVIEC bit clears this bit.
- Writing "1" to the STCS.OVIES bit sets this bit.

Bit	Description
0	Disable interrupt requests.
1	Enable interrupt requests.

[bit3] Reserved: Reserved Bit

The read value is "0".

If writing to this bit, write "0".

[bit2] EDIR: Measurement End Interrupt Request Bit

- This bit indicates that measurement has ended by setting the flag to "1" at the end time.
- Reading the measurement results (DTBF) clears the EDIR bit. The EDIR bit is read-only. Writing to the bit has no effect on the bit value.

Bit	Description
0	Read measurement results (DTBF).
1	Detect the interrupt factor.

[bit1] Reserved: Reserved Bit

The read value is "0".

If writing to this bit, write "0".

[bit0] OVIR: Overflow Interrupt Request Bit

- The flag is set to "1" when the count value overflows from 0xFFFF to 0x0000.
- Writing "1" to the STCC.OVIRC clears this bit.
- This bit is read-only. Writing data to this bit has no effect on operation.

Bit	Description
0	The interrupt factor is cleared.
1	Detect the interrupt factor.

10.4.2.5 Status Control Clear Register (STCC)

bit	7	6	5	4	3	2	1	0
Field	Reserved	EDIEC	Reserved	OVIEC	Reserved			OVIRC
R/W Attribute	R0,W0	R0,W	R0,W0	R0,W	R0,W0			R0,W
Protection Attribute	-							
Initial Value	0	0	0	0	000			0

[bit7] Reserved: Reserved Bit

The read value is "0".

If writing to this bit, write "0".

[bit6] EDIEC: Measurement End Interrupt Request Enable Clear Bit

- If "1" is written to this bit, the STC.EDIE bit is cleared to "0".
- The read value of this bit is always "0".

Bit	Description
0	Invalid
1	Clear the EDIE bit.

[bit5] Reserved: Reserved Bit

The read value is "0".

If writing to this bit, write "0".

[bit4] OVIEC: Overflow Interrupt Request Enable Clear Bit

- If "1" is written to this bit, the STC.OVIE bit is cleared to "0".
- The read value of this bit is always "0".

Bit	Description
0	Invalid
1	Clear the OVIE bit.

[bit3:1] Reserved: Reserved Bits

The read value is "0".

If writing to this bit, write "0".

[bit0] OVIRC: Overflow Interrupt Request Clear Bit

- If "1" is written to this bit, the STC.OVIR bit is cleared to "0".
- The read value of this bit is always "0".

Bit	Description
0	Invalid
1	Clear the OVIR bit.

10.4.2.6 Status Control Set Register (STCS)

bit	7	6	5	4	3	2	1	0
Field	Reserved	EDIES	Reserved	OVIES	Reserved			
R/W Attribute	R0,W0	R0,W	R0,W0	R0,W	R0,W0			
Protection Attribute	-							
Initial Value	0	0	0	0	0000			

[bit7] Reserved: Reserved Bit

The read value is "0".

If writing to this bit, write "0".

[bit6] EDIES: Measurement End Interrupt Request Enable Set Bit

- If "1" is written to this bit, the STC.EDIE bit is set to "1".
- The read value of this bit is always "0".

Bit	Description
0	Invalid
1	Set the EDIE bit.

[bit5] Reserved: Reserved Bit

The read value is "0".

If writing to this bit, write "0".

[bit4] OVIES: Overflow Interrupt Request Enable Set Bit

- If "1" is written to this bit, the STC.OVIE bit is set to "1".
- The read value of this bit is always "0".

Bit	Description
0	Invalid
1	Set the OVIE bit.

[bit3:0] Reserved: Reserved Bits

The read value is "0".

If writing to this bit, write "0".

10.4.3. Data Buffer Register (DTBF)

The Data Buffer Register (DTBF) is a register that can read the measurement value or count value of the PWC Timer. In 32-bit mode, if this is an even-numbered channel the lower 16 bits will be read similarly, for odd number channels, the upper 16 bits will be read.

Be sure to read this register with 16- or 32-bit data transfer instructions.

bit	15	8
Field	DTBF[15:8]	
R/W Attribute	R,WX	
Protection Attribute	-	
Initial Value	00000000	

bit	7	0
Field	DTBF[7:0]	
R/W Attribute	R,WX	
Protection Attribute	-	
Initial Value	00000000	

- These bits compose the DTBF register as a read-only register in either continuous measurement mode or single measurement mode. Writing does not change the register value.
- In continuous measurement mode (TMCR bit2 MDSE = "0"), the register is used as a buffer register to store the last measurement results.
- In single measurement mode (TMCR bit2 MDSE = "1"), the up counter is directly accessed with the DTBF register. Reading is allowed even during counting so that the count value can be read. After measurement ends, the measurement results are stored as is.
- Use 16- or 32-bit data access for the DTBF register.

10.4.4. Base Timer Debug Register (BT_DEBUG)

The Base Timer Debug Register (BT_DEBUG) performs enable/disable setting of debug.

bit	15	8
Field	Reserved	
R/W Attribute	R0,W0	
Protection Attribute	-	
Initial Value	00000000	

bit	7	0
Field	Reserved	DBGEN
R/W Attribute	R0,W0	R/W
Protection Attribute	-	
Initial Value	00000000	0

[bit15:1] Reserved: Reserved Bits

The read value is "0".

If writing to this bit, write "0".

[bit0] DBGEN: Debug Enable Bit

- It is the bit which permits stopping operation of a Base Timer with the debug signal (DEBUG).

Bit	Description
0	Disable
1	Enable

CHAPTER 17: Base Timer I/O Selection Function



This chapter explains the base timer I/O selection function.

1. Overview
2. Configuration
3. Explanation of Operation
4. Registers

CODE:BTSEL-S6J3400-E2

1. Overview

This section provides an overview of the base timer I/O selection function.

The base timer I/O selection function is a function for selecting a signal I/O method for the base timer by setting an I/O mode.

By switching the timer function, the base timer mounted in a channel can be used as any of the timers described below for each channel. The I/O method for the respective functions can be selected.

Timer outputs can be simultaneously read using TOUT Read Register (BT_BTTRR).

The following 7 patterns can be selected for I/O pin connections.

- 16-bit timer standard mode
- 32-bit timer full-function mode
- PPG trigger 2-channel sharing mode
- Timer start/stop mode
- Simultaneous soft start mode
- Timer start/stop and simultaneous soft start mode
- Timer start mode

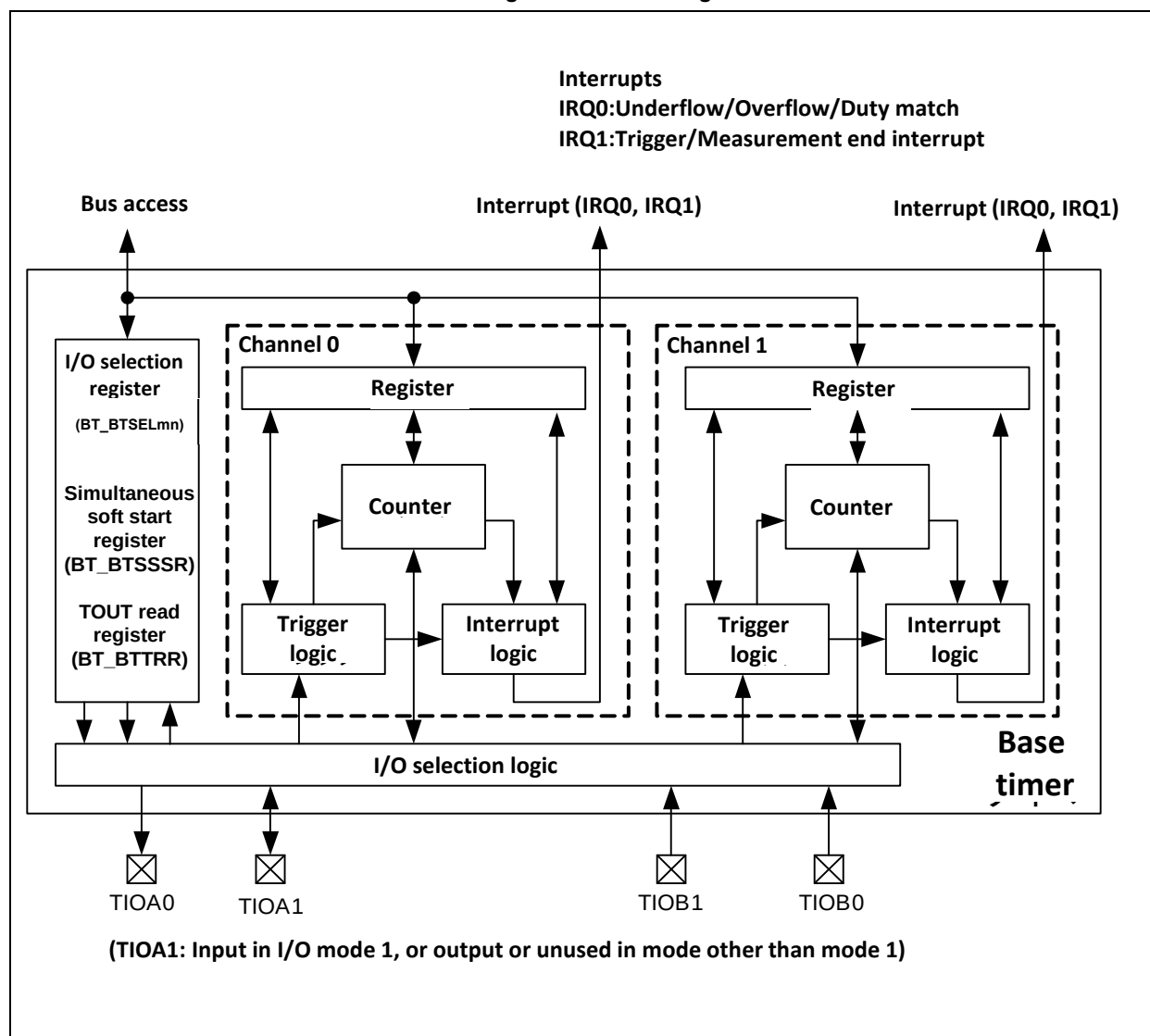
The 32-bit reload timer and 32-bit PWC timer can be implemented by using 2 channels of the mounted base timer. These 2 channels are channel m (m is an even number) and channel n ($n = m + 1$).

2. Configuration

The 32-bit reload timer and 32-bit PWC timer can be implemented by using 2 channels of the mounted base timer. These 2 channels are channel m (m is an even number) and channel n (n = m + 1).

This section explains the configuration of the base timer and I/O selection function.

Figure 2-1 Block Diagram



Configuration for channel 0 and channel 1

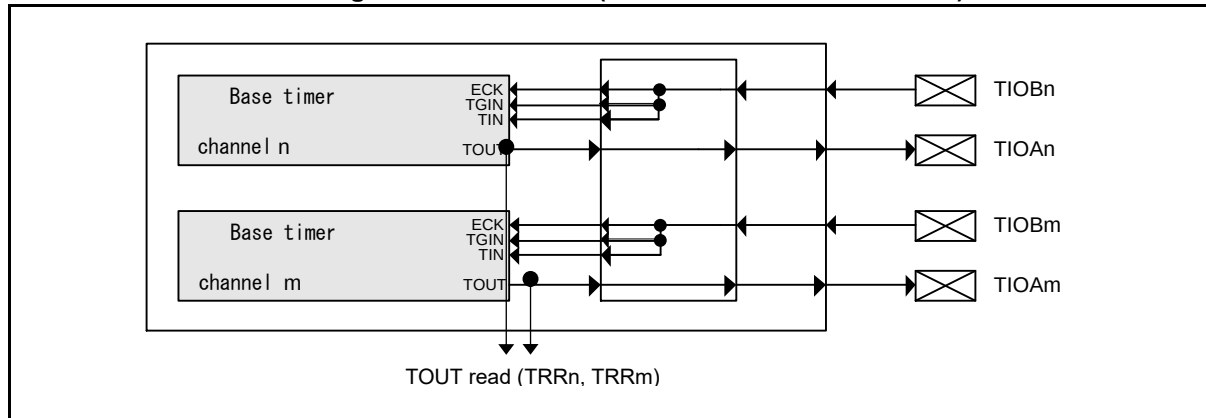
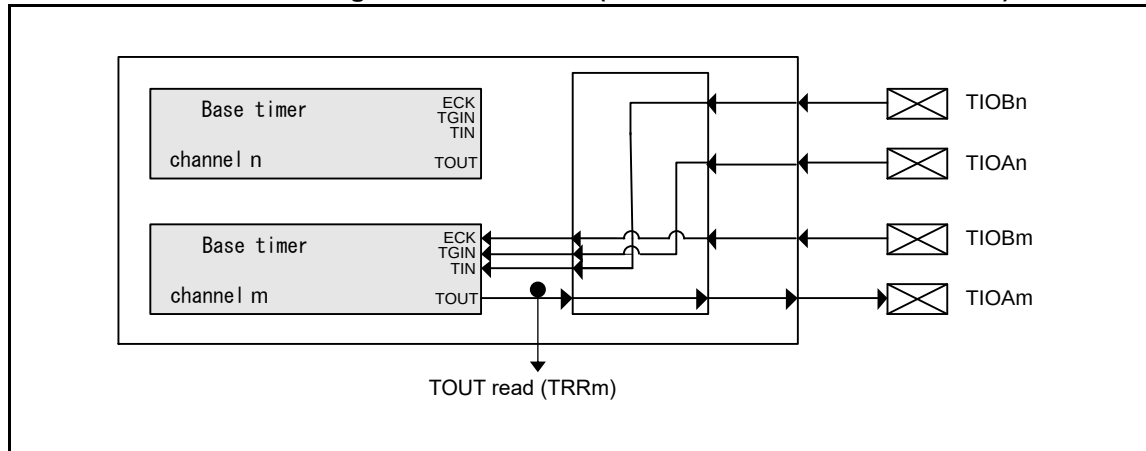
3. Explanation of Operation

This section explains base timer I/O assignment.

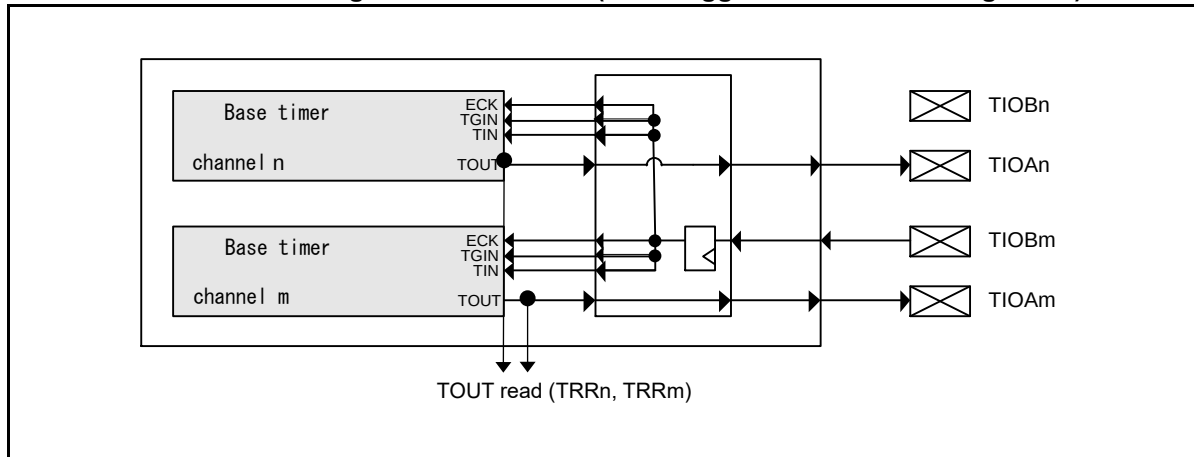
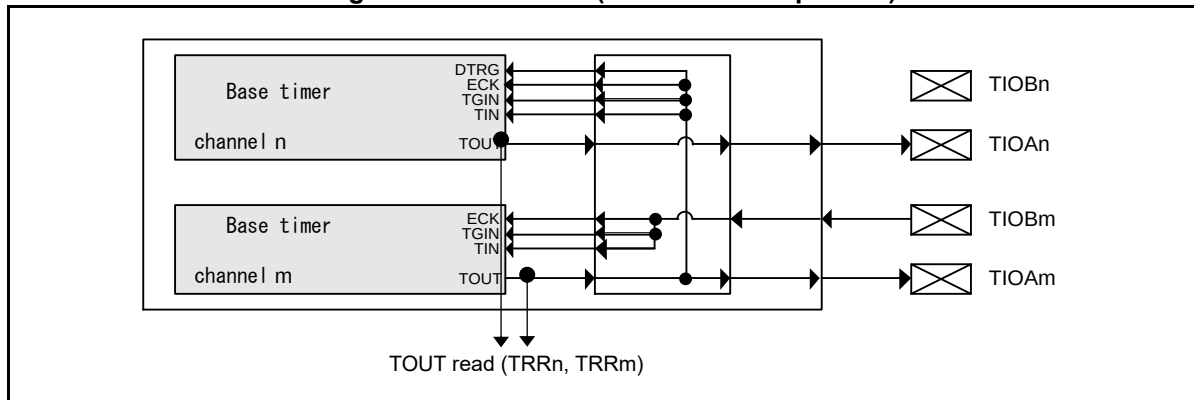
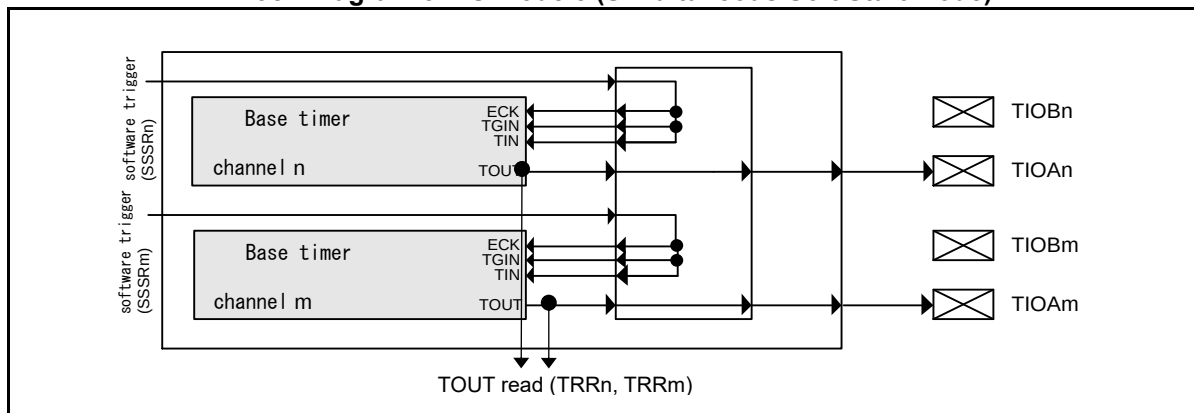
Before using a timer, make an I/O setting for the base timer by using the I/O mode selection bit (BTSEL01). You can select one of the following 7 modes.

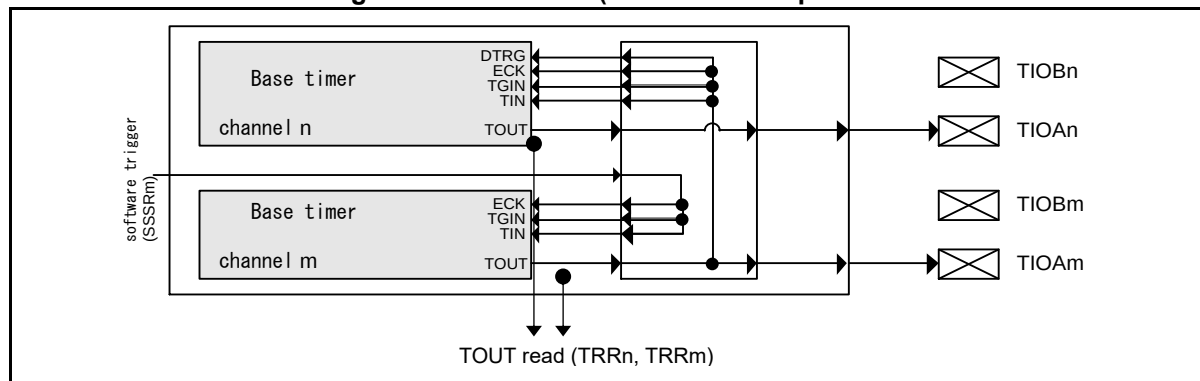
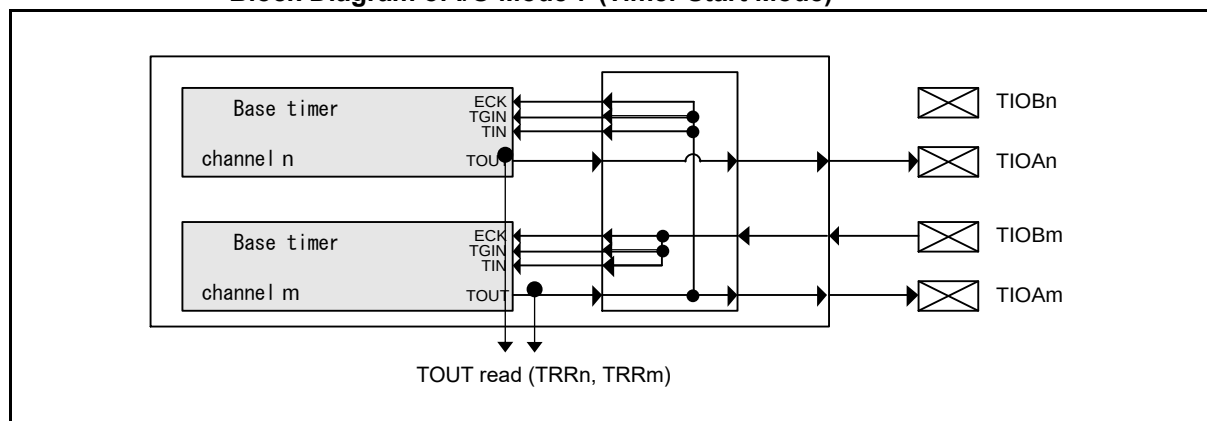
- I/O mode 0: 16-bit timer standard mode
In this mode, the base timer in 1 channel operates individually and separately from the others.
- I/O mode 1: 32-bit timer full-function mode
The signals of the even-numbered channels of the base timer are individually assigned to external pins in operation in this mode.
- I/O mode 2: PPG trigger 2-channel sharing mode
This mode enables simultaneous input of external start triggers to the base timers of 2 channels. The base timers of the 2 channels can be started simultaneously.
- I/O mode 4: Timer start/stop mode
In this mode, an even-numbered channel controls the start/stop of an odd-numbered channel. The odd-numbered channel is started by the rising edge* of an output signal from the even-numbered channel, and stopped by the falling edge*.
- I/O mode 5: Simultaneous soft start mode
In this mode, software starts multiple channels simultaneously.
- I/O mode 6: Soft start timer start/stop mode
In this mode, an even-numbered channel controls the start/stop of an odd-numbered channel. Software starts the even-numbered channel. The odd-numbered channel is started by the rising edge* of an output signal from the even-numbered channel, and stopped by the falling edge*.
- I/O mode 7: Timer start mode
In this mode, an even-numbered channel controls the start of an odd-numbered channel. The odd-numbered channel is started by the rising edge* of an output signal from the even-numbered channel.

*: Use the trigger input selection bit (BTxx_TMCR:EGS) for the setting.

Block Diagram of I/O Mode 0 (16-bit Timer Standard Mode)

Block Diagram of I/O Mode 1 (32-bit Timer Full-function Mode)

Note:

- If I/O mode 1 is set, set read value of TRRn is undefined.

Block Diagram of I/O Mode 2 (PPG Trigger 2-channel Sharing Mode)**Block Diagram of I/O Mode 4 (Timer Start/Stop Mode)****Block Diagram of I/O Mode 5 (Simultaneous Soft Start Mode)**

Block Diagram of I/O Mode 6 (Timer Start/Stop and Simultaneous Soft Start Mode)

Block Diagram of I/O Mode 7 (Timer Start Mode)

Note:

- If I/O mode 1 is set, set TIOAn of the corresponding odd-numbered channel to port input mode by using the GPIO setting.

4. Registers

This section explains the base timer I/O selection function registers.

Table 4-1 List of Base Timer I/O Selection Registers

Abbreviated Register Name	Register Name	Reference
BT_BTSEL01	I/O selection register (channel 0, 1)	4.1
BT_BTSEL23	I/O selection register (channel 2, 3)	4.1
BT_BTSEL45	I/O selection register (channel 4, 5)	4.1
BT_BTSEL67	I/O selection register (channel 6, 7)	4.1
BT_BTSEL89	I/O selection register (channel 8, 9)	4.1
BT_BTSEL1011	I/O selection register (channel 10, 11)	4.1
BT_BTSEL1213	I/O selection register (channel 12, 13)	4.1
BT_BTSEL1415	I/O selection register (channel 14, 15)	4.1
BT_BTSEL1617	I/O selection register (channel 16, 17)	4.1
BT_BTSEL1819	I/O selection register (channel 18, 19)	4.1
BT_BTSEL2021	I/O selection register (channel 20, 21)	4.1
BT_BTSEL2223	I/O selection register (channel 22, 23)	4.1
BT_BTSEL2425	I/O selection register (channel 24, 25)	4.1
BT_BTSEL2627	I/O selection register (channel 26, 27)	4.1
BT_BTSEL2829	I/O selection register (channel 28, 29)	4.1
BT_BTSEL3031	I/O selection register (channel 30, 31)	4.1
BT_BTSEL3233	I/O selection register (channel 32, 33)	4.1
BT_BTSEL3435	I/O selection register (channel 34, 35)	4.1
BT_BTSEL3637	I/O selection register (channel 36, 37)	4.1
BT_BTSEL3839	I/O selection register (channel 38, 39)	4.1
BT_BTSEL4041	I/O selection register (channel 40, 41)	4.1
BT_BTSEL4243	I/O selection register (channel 42, 43)	4.1
BT_BTSEL4445	I/O selection register (channel 44, 45)	4.1
BT_BTSEL4647	I/O selection register (channel 46, 47)	4.1
BT_BTSEL4849	I/O selection register (channel 48, 49)	4.1
BT_BTSEL5051	I/O selection register (channel 50, 51)	4.1
BT_BTSEL5253	I/O selection register (channel 52, 53)	4.1
BT_BTSEL5455	I/O selection register (channel 54, 55)	4.1
BT_BTSEL5657	I/O selection register (channel 56, 57)	4.1
BT_BTSEL5859	I/O selection register (channel 58, 59)	4.1
BT_BTSEL6061	I/O selection register (channel 60, 61)	4.1
BT_BTSEL6263	I/O selection register (channel 62, 63)	4.1
BT_BTSSSR0	Simultaneous soft start register (channel 0)	4.2
BT_BTSSSR12	Simultaneous soft start register (channel 12)	4.2
BT_BTSSSR24	Simultaneous soft start register (channel 24)	4.2
BT_BTSSSR36	Simultaneous soft start register (channel 36)	4.2
BT_BTSSSR48	Simultaneous soft start register (channel 48)	4.2
BT_BTSSSR60	Simultaneous soft start register (channel 60)	4.2
BT_BTTRR0	TOUT read register (channel 0)	4.3
BT_BTTRR12	TOUT read register (channel 12)	4.3
BT_BTTRR24	TOUT read register (channel 24)	4.3

Abbreviated Register Name	Register Name	Reference
BT_BTTRR36	TOUT read register (channel 36)	4.3
BT_BTTRR48	TOUT read register (channel 48)	4.3
BT_BTTRR60	TOUT read register (channel 60)	4.3

Tables 4-2, 4-3, and 4-4 show the register map of each mode.

The "****/****/****/****" expression in each table corresponds to the reload/PWM/PPG/PWC timer, respectively.

Table 4-2 Register Map (Channel No.: 0) (12) (24) (36) (48) (60)

Offset	Register Name/Initial Value			
	+3	+2	+1	+0
0x0000_0000	Reserved 00000000_00000000		BTxx_PCSR/ BTxx_PCSR/ BTxx_PRL / Reserved XXXXXXXX_XXXXXXXX	
0x0000_0004	Reserved 00000000_00000000		Reserved/ BTxx_PDUT/ BTxx_PRLH/ BTxx_DTB XXXXXXXX_XXXXXXXX / 00000000_00000000 (BTxx_DTB)	
0x0000_0008	Reserved/ BTxx_TMR/ Reserved/ Reserved 00000000_00000000		BTxx_TMR/ BTxx_TMR/ BTxx_TMR/ Reserved 00000000_00000000 XXXXXXXX_XXXXXXXX*1	
0x0000_000C	Reserved 00000000_00000000		BTxx_TMCR 00000000_00000000	
0x0000_0010	Reserved 00000000_00000000		BTxx_TMCR2 00000000	BTxx_STC 00000000
0x0000_0014	Reserved 00000000_00000000		Reserved 00000000	BTxx_STCC 00000000
0x0000_0018	Reserved 00000000_00000000		Reserved 00000000	BTxx_STCS 00000000
0x0000_001C	Reserved 00000000_00000000		Reserved/ BTxx_PSDR/ Reserved/ Reserved 00000000_00000000	
0x0000_0020	Reserved 00000000_00000000		Reserved/ BTxx_ADTR/ Reserved/ Reserved 00000000_00000000	
0x0000_0024	Reserved 00000000_00000000		BT_DEBUG 00000000	
0x0000_0028	Reserved 00000000_00000000_00000000_00000000			

Offset	Register Name/Initial Value			
	+3	+2	+1	+0
0x0000_002C	Reserved 00000000_00000000		ETCDR/ ETCDR / ETCDR/ Reserved 01111111_11111111 / 00000000_00000000 (Reserved)	
0x0000_0030	Reserved 11111111_11111111		Reserved 11111111	BT_BTSELmn*2 11110000
0x0000_0034	Reserved 11111111_11111111		BT_BTSSSRn*3 11111111_11111111	
0x0000_0038	Reserved 11111111_11111111		BT_BTTRRn*3 11110000_00000000	

*1 The initial value is XXXXXXXX_XXXXXXX only during reload timer operation.

*2 mn = 01, 1213, 2425, 3637, 4849 and 6061

*3 n = 0, 12, 24, 36, 48 and 60

The "*/**/*/**/" expression in each table corresponds to the reload/PWM/ PPG/PWC timer, respectively.

Table 4-3 Register Map (Channel No.: 1, 3, 5, 7, 9, and 11) (13, 15, 17, 19, 21, and 23) (25, 27, 29, 31, 33, and 35) (37, 39, 41, 43, 45, and 47) (49, 51, 53, 55, 57, and 59) (61 and 63)

Offset	Register Name/Initial Value			
	+3	+2	+1	+0
0x0000_0000	Reserved 00000000_00000000		BTxx_PCSR/ BTxx_PCSR/ BTxx_PRL / Reserved XXXXXXXX_XXXXXXXX	
0x0000_0004	Reserved 00000000_00000000		Reserved/ BTxx_PDUT/ BTxx_PRLH/ BTxx_DTB XXXXXXXX_XXXXXXXX / 00000000_00000000 (BTxx_DTB)	
0x0000_0008	Reserved/ BTxx_TMR/ Reserved/ Reserved 00000000_00000000		BTxx_TMR/ BTxx_TMR/ BTxx_TMR / Reserved 00000000_00000000 / XXXXXXXX_XXXXXXXX*1	
0x0000_000C	Reserved 00000000_00000000		BTxx_TMCR 00000000_00000000	
0x0000_0010	Reserved 00000000_00000000		BTxx_TMCR2 00000000	BTxx_STC 00000000
0x0000_0014	Reserved 00000000_00000000		Reserved 00000000	BTxx_STCC 00000000
0x0000_0018	Reserved 00000000_00000000		Reserved 00000000	BTxx_STCS 00000000

Offset	Register Name/Initial Value			
	+3	+2	+1	+0
0x0000_001C	Reserved 00000000_00000000		Reserved/ BTxx_PSDR/ Reserved/ Reserved 00000000_00000000	
0x0000_0020	Reserved 00000000_00000000		Reserved/ BTxx_ADTR/ Reserved/ Reserved 00000000_00000000	
0x0000_0024	Reserved 00000000_00000000		BT_DEBUG 00000000	
0x0000_0028	Reserved 00000000_00000000_00000000_00000000			
0x0000_002C	Reserved 00000000_00000000		ETCDR/ ETCDR / ETCDR/ Reserved 01111111_11111111 / 00000000_00000000 (Reserved)	

*1 The initial value is XXXXXXXX_XXXXXXX only during reload timer operation.

The "*/*/*/*/" expression in each table corresponds to the reload/PWM/PPG/PWC timer, respectively.

Table 4-4 Register Map (Channel No.: 2, 4, 6, 8, and 10) (14, 16, 18, 20, and 22) (26, 28, 30, 32, and 34) (38, 40, 42, 44, and 46) (50, 52, 54, 56, and 58) (62)

Offset	Register Name/Initial Value			
	+3	+2	+1	+0
0x0000_0000	Reserved 00000000_00000000		BTxx_PCSR/ BTxx_PCSR/ BTxx_PRL / Reserved XXXXXXXX_XXXXXXXX	
0x0000_0004	Reserved 00000000_00000000		Reserved/ BTxx_PDUT/ BTxx_PRLH/ BTxx_DTB XXXXXXXX_XXXXXXXX / 00000000_00000000 (BTxx_DTB)	
0x0000_0008	Reserved/ BTxx_TMR/ Reserved/ Reserved 00000000_00000000		BTxx_TMR/ BTxx_TMR/ BTxx_TMR / Reserved 00000000_00000000 / XXXXXXXX_XXXXXXX*1	
0x0000_000C	Reserved 00000000_00000000		BTxx_TMCR 00000000_00000000	
0x0000_0010	Reserved 00000000_00000000		BTxx_TMCR2 00000000	BTxx_STC 00000000
0x0000_0014	Reserved 00000000_00000000		Reserved 00000000	BTxx_STCC 00000000
0x0000_0018	Reserved 00000000_00000000		Reserved 00000000	BTxx_STCS 00000000

Offset	Register Name/Initial Value			
	+3	+2	+1	+0
0x0000_001C	Reserved 00000000_00000000		Reserved/ BTxx_PSDR/ Reserved/ Reserved 00000000_00000000	
0x0000_0020	Reserved 00000000_00000000		Reserved/ BTxx_ADTR/ Reserved/ Reserved 00000000_00000000	
0x0000_0024	Reserved 00000000_00000000		BT_DEBUG 00000000	
0x0000_0028	Reserved 00000000_00000000_00000000_00000000			
0x0000_002C	Reserved 00000000_00000000		ETCDR/ ETCDR / ETCDR/ Reserved 01111111_11111111 / 00000000_00000000 (Reserved)	
0x0000_0030	Reserved 11111111_11111111		Reserved 11111111	BT_BTSELMn*2 11110000

*1 The initial value is XXXXXXXX_XXXXXXX only during reload timer operation.

*2 mn = 23, 45, 67, 89, 1011, 1415, 1617, 1819, 2021, 2223, 2627, 2829, 3031, 3233, 3435, 3839, 4041, 4243, 4445, 4647, 5051, 5253, 5455, 5657, 5859 and 6263

The "****/****/****/****" expression in each table corresponds to the reload/PWM/PPG/PWC timer, respectively.

4.1. I/O Selection Registers (BT_BTSELmn)

This section shows the bit configuration of the I/O selection registers.

These bits set the I/O modes of the 2 channels of base timer channel m (m is 0 or an even number) and channel n (n = m + 1: odd number) for the following connection.

Bit	31	8
Field	Reserved	
R/W Attribute	R1,WX	
Protection Attribute	-	
Initial Value	11111111 11111111 11111111	

Bit	7	6	5	4	3	2	1	0
Field	Reserved				BTSEL01			
R/W Attribute	R1,WX				R/W			
Protection Attribute	-							
Initial Value	1111				0000			

[bit31:4] Reserved: Reserved bits

[bit3:0] BTSEL01: I/O mode selection bits

These bits set the I/O modes of the 2 channels of base timer channel m and channel n for the following connection.

Bits				Description
0	0	0	0	I/O mode 0: 16-bit timer standard mode
0	0	0	1	I/O mode 1: 32-bit timer full-function mode
0	0	1	0	I/O mode 2: PPG trigger 2-channel sharing mode
0	0	1	1	Setting prohibited
0	1	0	0	I/O mode 4: Timer start/stop mode
0	1	0	1	I/O mode 5: Simultaneous soft start mode
0	1	1	0	I/O mode 6: Timer start/stop and simultaneous soft start mode
0	1	1	1	I/O mode 7: Timer start mode
1	x	x	x	Setting prohibited

Note:

- You cannot initialize this register by setting reset mode (TMCR:FMD2 to 0="0b000"). After setting reset mode, rewrite this register.

4.2. Simultaneous Soft Start Register (BT_BTSSSR)

This section shows the bit configuration of the simultaneous soft start register.

These bits represent input signals in I/O modes 5 and 6. This register can be used to generate triggers for all channels simultaneously.

Bit	31	16
Field	Reserved	
R/W Attribute	R1,WX	
Protection Attribute	-	
Initial Value	11111111_11111111	

Bit	15	14	13	12	11	10	9	8
Field	Reserved				SSSR11	SSSR10	SSSR9	SSSR8
R/W Attribute	R1, WX				R1,W	R1,W	R1,W	R1,W
Protection Attribute	-							
Initial Value	1111				1	1	1	1

Bit	7	6	5	4	3	2	1	0
Field	SSSR7	SSSR6	SSSR5	SSSR4	SSSR3	SSSR2	SSSR1	SSSR0
R/W Attribute	R1,W	R1,W	R1,W	R1,W	R1,W	R1,W	R1,W	R1,W
Protection Attribute	-							
Initial Value	1	1	1	1	1	1	1	1

[bit31:12] Reserved: Reserved bits

[bit11:0] SSSR[11:0]: Simultaneous soft start bits

These bits represent input signals in I/O modes 5 and 6. For details on connections, see the block diagram of each I/O mode in "3. Explanation of Operation."

Writing "1" starts the corresponding channel, and writing "0" has no effect. Up to 12 channels with channel numbers 0 to 11 can be started simultaneously.

Correspondence of the channel number is below.

BT_BTSSSR0 : SSSR0-11 = ch0-11

BT_BTSSSR12 : SSSR0-11 = ch12-23

BT_BTSSSR24 : SSSR0-11 = ch24-35

BT_BTSSSR36 : SSSR0-11 = ch36-47

BT_BTSSSR48 : SSSR0-11 = ch48-59

BT_BTSSSR60 : SSSR0-3 = ch60-63

SSSR [X]	Description
0	No operation
1	Assigns the "1" pulse to input and starts the corresponding channel.

[X] represents the channel number of the base timer. It is a value from 0 to 11.

4.3. TOUT Read Register (BT_BTTRR)

This section shows the bit configuration of the TOUT read register.

By using these bits, software can read TOUT status from the Base Timer channels.

Bit	31	16
Field	Reserved	
R/W Attribute	R1, WX	
Protection Attribute	-	
Initial Value	11111111_11111111	

Bit	15	14	13	12	11	10	9	8
Field	Reserved				TRR11	TRR10	TRR9	TRR8
R/W Attribute	R1, WX				R, WX	R, WX	R, WX	R, WX
Protection Attribute	-				-	-	-	-
Initial Value	1111				0	0	0	0

Bit	7	6	5	4	3	2	1	0
Field	TRR7	TRR6	TRR5	TRR4	TRR3	TRR2	TRR1	TRR0
R/W Attribute	R, WX	R, WX	R, WX	R, WX	R, WX	R, WX	R, WX	R, WX
Protection Attribute	-							
Initial Value	0	0	0	0	0	0	0	0

[bit31:12] Reserved: Reserved bits

[bit11:0] TRR[11:0]: Simultaneous TOUT read bits

These bits represent TOUT status of the Base Timer channels. For details on connections, see the block diagram of each I/O mode in 3. Explanation of Operation.

TRR[X]	Description
0	TOUT status is '0'
1	TOUT status is '1'

[X] represents the channel number of the base timer. It is a value from 0 to 11.

CHAPTER 18: Base Timer Simultaneous Operation



This chapter explains the base timers simultaneous Soft Start .

1. Overview
2. Configuration
3. Explanation of Simultaneous Soft Start Operation
4. Overview of the 16-bit Global Timer
5. Explanation of the 16-bit Global Timer Operation
6. Registers of the 16-bit Global Timer
7. Precautions for Using This Device

CODE: BTSIM-S6J3400-E3

1. Overview

This section provides an overview of the Base Timer simultaneous soft start.

There are the undermentioned two operational modes in the soft start of the Base timer simultaneous.

- The operation by the write to simultaneous soft start registers.
(Refer to the chapter of Base Timer I/O Selection Function on this manual.)
- The operation which uses an external timer
(Refer to the chapter of Base Timer 10.2.4 External Timer Match Starting on this manual.)

This Chapter describes the operation which uses an external timer.

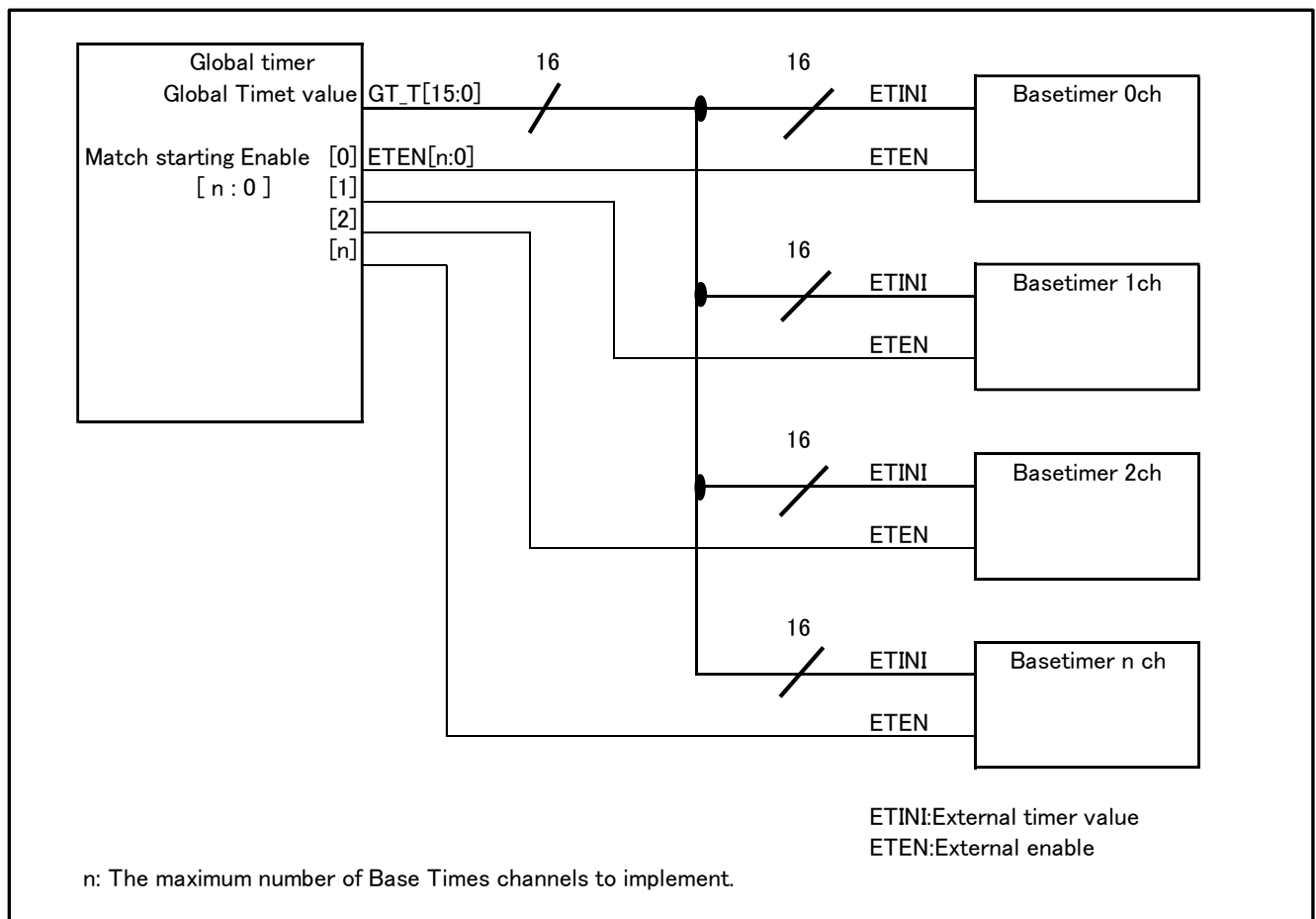
As an external Timer, it uses Global Timer described in this Chapter.

2. Configuration

This section explains the configuration of the Base Timer simultaneous start which uses a Global Timer. From the Global Timer, the undermentioned signals are outputted and it is inputted into each Base Timer.

- Global timer value
It is a 16-bit timer counter value in the Global Timer.
- Match starting Enable
It outputs, the Global Timer match enabling signal to each base timer channel.

Figure 2-1 Block Diagram



3. Explanation of Simultaneous Soft Start Operation

This section explains the operation of Base Timer Simultaneous Soft Start.

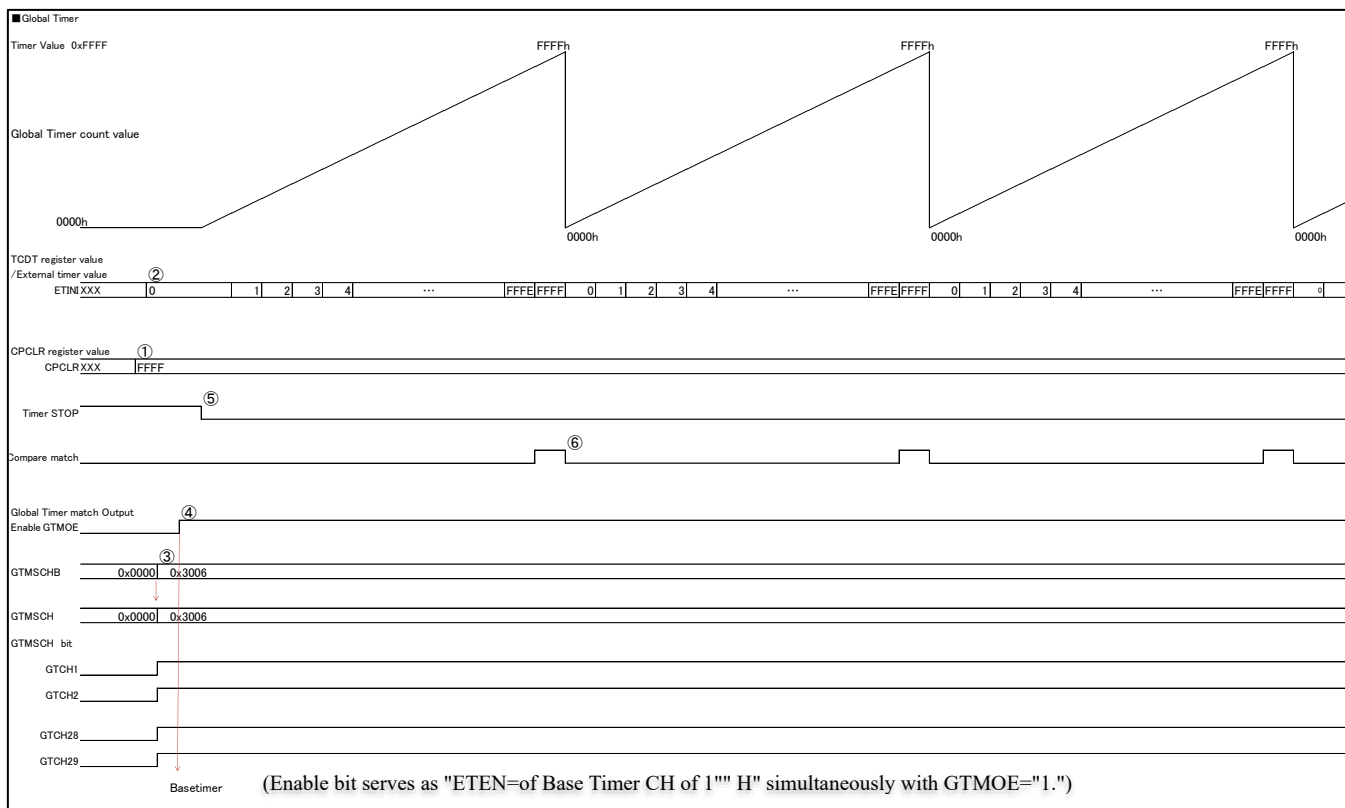
The Procedure in which the simultaneous soft start of the Base Timer was simplified below is shown.

1. It performs an output set of a waveform set of the Base Timer, etc. of operation
2. It performs a set of the Global Timer of operation.
3. Initialization of Global Timer.
4. Set of the Base Timer channel to use an external timer match startup.
5. Global Timer Start.
6. A match of the Global Timer value and the value of external timer compare data in the Base Timer will start the Base Timer.

3.1. Global Time and Base Timers Operation Waveform

The waveform of operation which controls STOP bit in Timer State Control Register (TCCS) starts, and starts Global Timer, and each Base Timers starts is shown below.

Figure 3-1 Global Timer Waveform (It sets a STOP bit as "0" from "1", and starts Global Timer.)



① Global Timer various sets.

It writes an any value in the Global Clear Register (CPCLR), and sets up the Global Timer period.
(ex:0xFFFF)

It writes any value in GT_CLK [3:0], and sets up Global Timer counter clock frequency.

MODE set by GT_MSCTR.MODE bit.

(In the above-mentioned waveform, MODE Bit is "0" and is buffer disable.)

② It writes "0x0000" in the Global Timer Data Register (GT_TCDT), and clears the Global Timer value.

③ It writes an arbitrary value in Global Timer Match Channel Buffer Register (GT_MSCHB0~1).

(It writes "1" in Global Timer Match Starting Channel Buffer Bits (GTCH) of the Base Timer channel to use an external timer match start.)

Since a timer is stopping, the Global Timer Match Channel Buffer Register (GT_MSCHB0~1) set point is immediately transmitted to Global Timer Match Starting Channel register (GT_MSCH0~1).

For output disable (GTMOE="0"), All External Timer Match Enabling Signals (ETEN) are "L."

- ④ After a Global Timer Match Channel Buffer Register (GT_MSCHB0~1) set, it sets it as GTMOE bit ="1" (Enable).

According to the Global Timer Match Starting Channel register (GT_MSCH0~1) set point, the External Timer Match Enable Signal (ETEN) of each Base Timer Channel changes to "H".

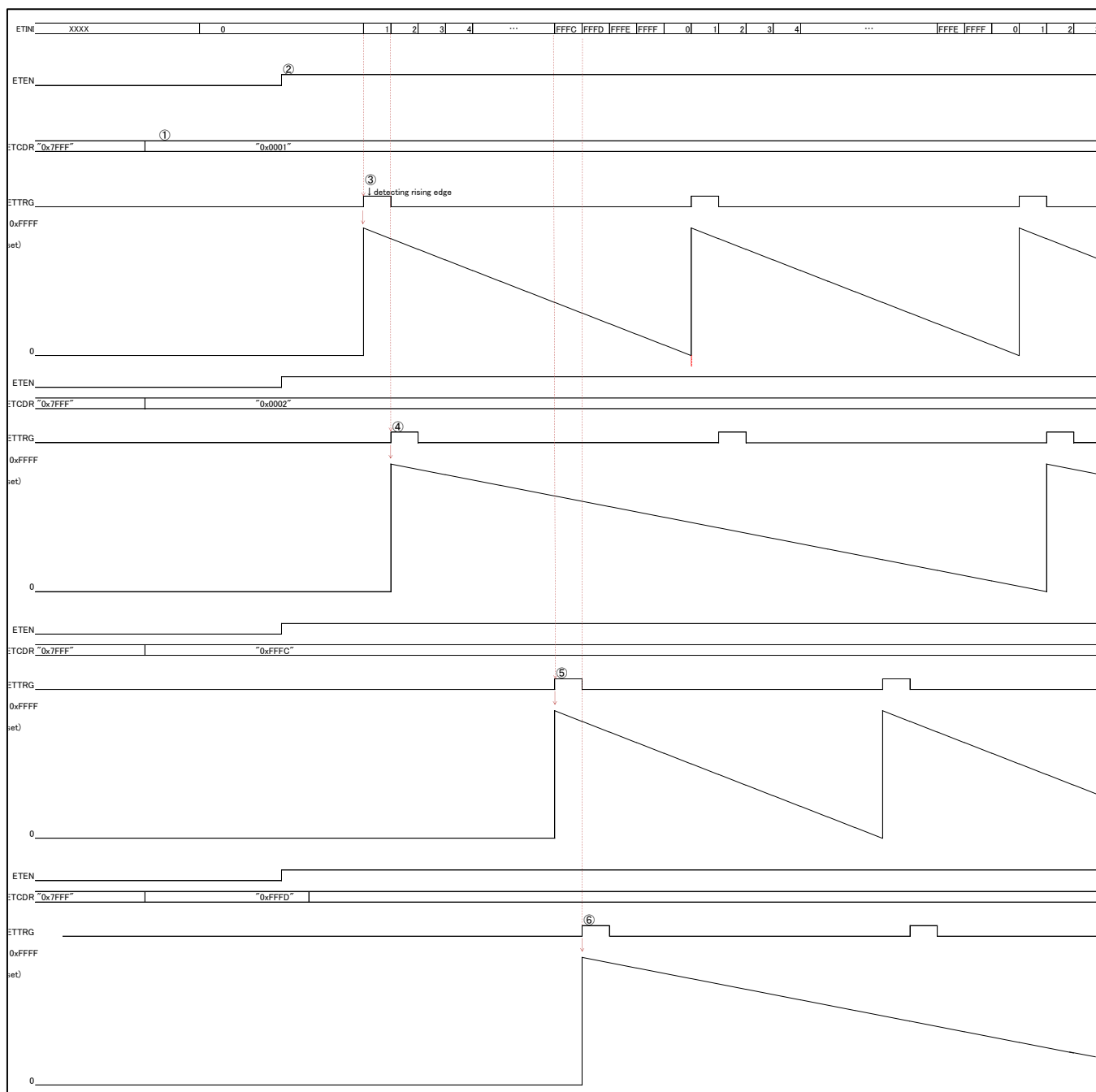
- ⑤ It writes "0" in STOP bit of Global Timer State Control Register(GT_TCCS).

Global Timer start. (It does not stop Global Timer in start once.)

- ⑥ When a match the Global Timer Compare Clear Register (GT_CPCLR) value and Global Timer value, it is a comparison clear flag generate.

In accordance with the setup value, the Base Timer operates after the Global Timer start.

Figure 3-2 Base Timer Waveform



- ① Base timer various sets. (For details, refer to the chapter of Base Timer on this manual)

Note:

- Please set ETCDR of the channel which uses an external timer match start as a larger value than "0x0000".
- ② Simultaneously with GTMOE="1", the ETEN signal of Base Timer CH by which the start set was carried out. "H" It becomes.

- ③ When a match the External Time Comparison Data Register(ETCDR) value and a Global Timer value , ETTRG signal occurs and Base Timer start.(CH1)
- ④ When a match the External Time Comparison Data Register(ETCDR) value and a Global Timer value , ETTRG signal occurs and Base Timer start.(CH2)
- ⑤ When a match the External Time Comparison Data Register(ETCDR) value and a Global Timer value , ETTRG signal occurs and Base Timer start.(CH28)
- ⑥ When a match the External Time Comparison Data Register(ETCDR) value and a Global Timer value , ETTRG signal occurs and Base Timer start.(CH29)

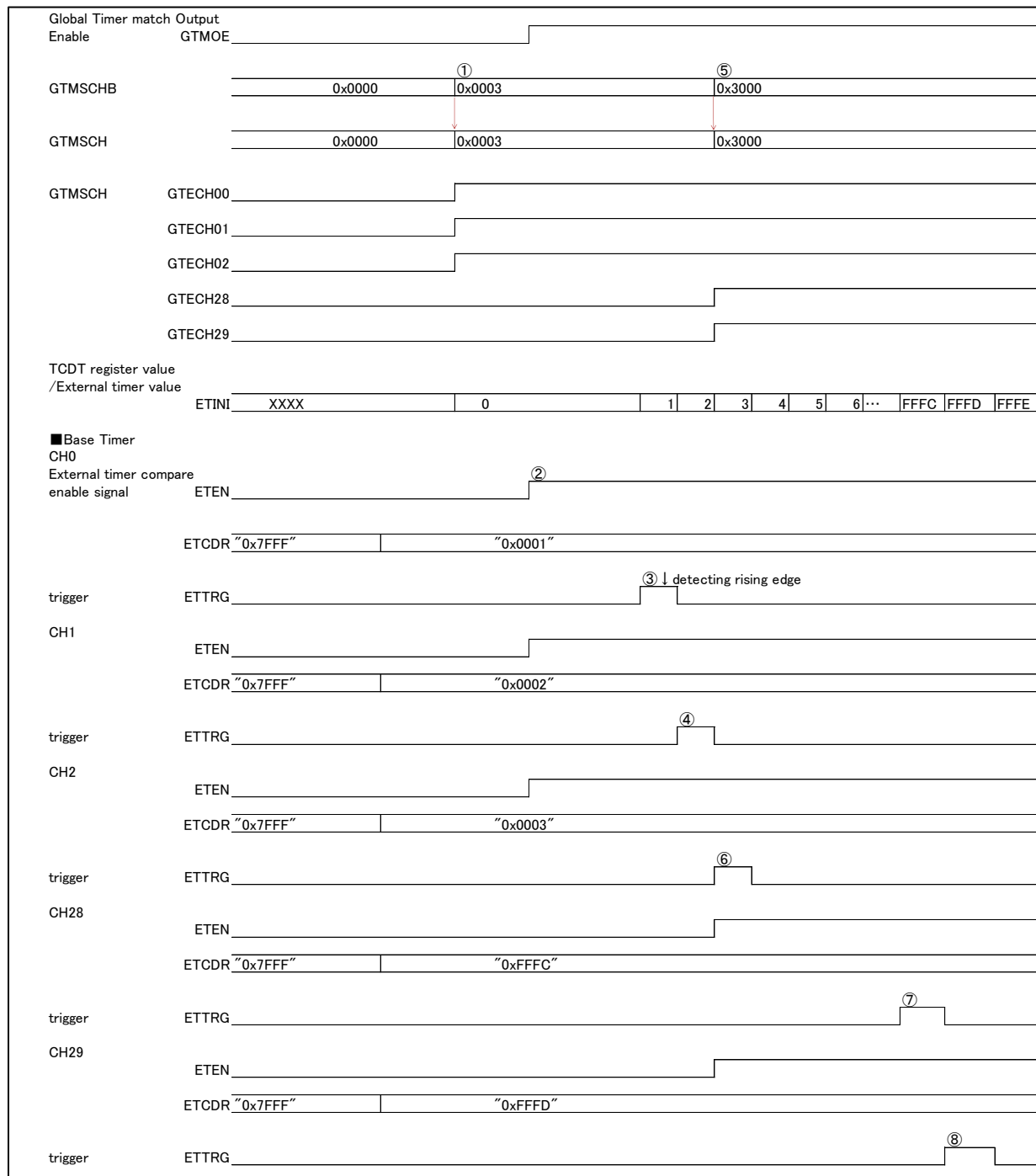
By adding the channel which carries out a Simultaneous Soft Start to GT_MSCHB0~1 Register, and carrying out an enable set, it can carry out the additional operation of Base Timers also after the Global Timer operation.

In that case, Base Timers which want to run an additional simultaneous soft start before needs to be set up.

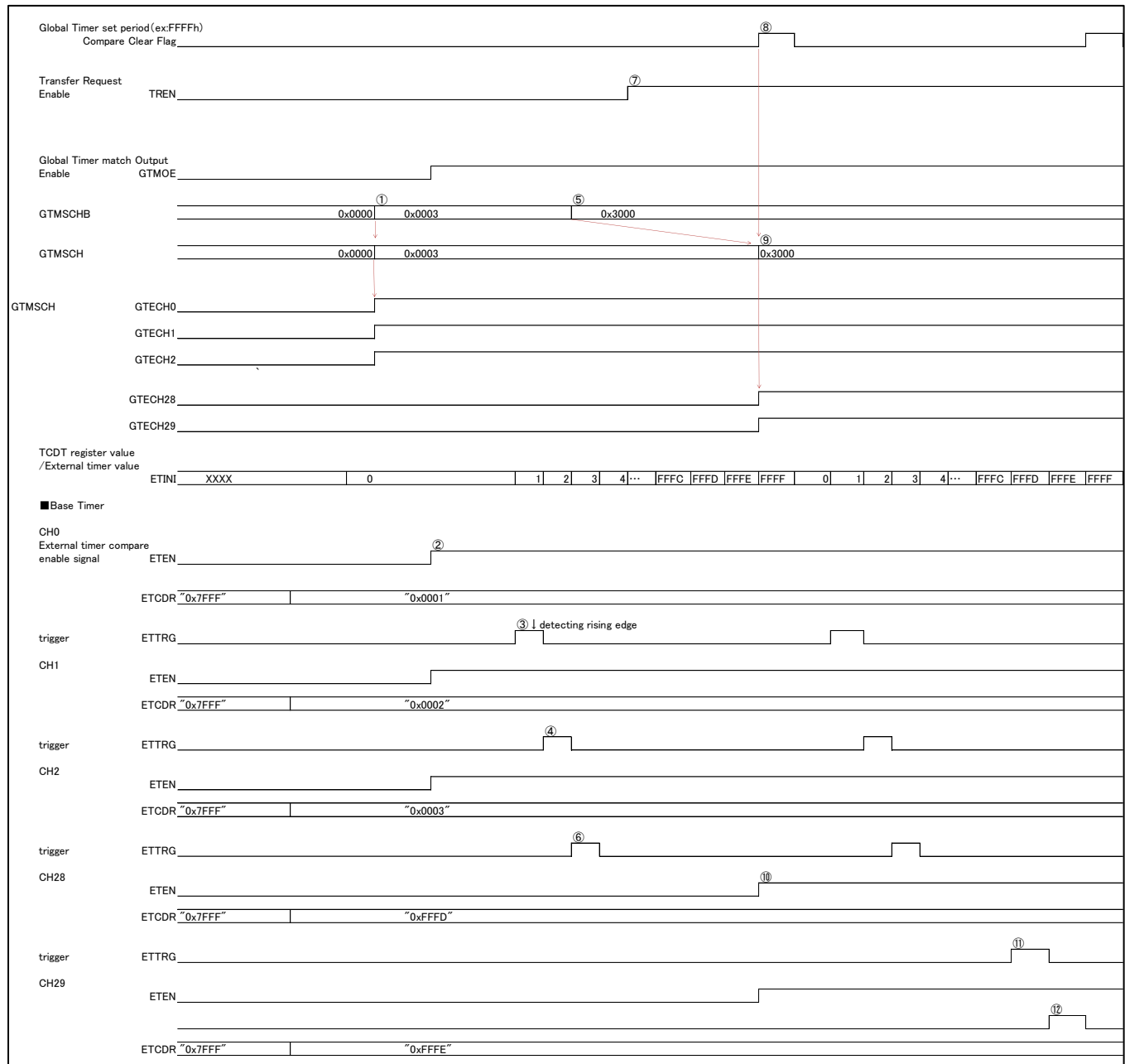
3.2. Global Timer Match Starting Channel Buffer Operation by MODE Set

The MODE value in Global Timer Match Starting Control register, the update time of the Global Timer Match Starting Channel register value has a difference.

Figure 3-3 The Waveform in the Case of Adding Base Timers CH of the Global Timer Match Start Enable. (MODE=0)



- ① It is a start set from Base Timers CH0 to CH3.
A data is immediately updated by GTMSCH for MODE=0, without carrying out a buffer.
- ② Simultaneously with GTMOE="1", the ETEN signal of Base Timer CH by which the start set was carried out. "H" It becomes.
- ③ When a match the External Time Comparison Data Register(ETCDR) value and the Global Timer value , ETTRG signal occurs and Base Timer starts.(CH0)
- ④ When a match the External Time Comparison Data Register(ETCDR) value and the Global Timer value , ETTRG signal occurs and Base Timer starts.(CH1)
- ⑤ It is a start set from Base Timers CH28 to CH29.
- ⑥ When a match the External Time Comparison Data Register(ETCDR) value and the Global Timer value , ETTRG signal occurs and Base Timer starts.(CH2)
- ⑦ When a match the External Time Comparison Data Register(ETCDR) value and the Global Timer value , ETTRG signal occurs and Base Timer starts.(CH28)
- ⑧ When a match the External Time Comparison Data Register(ETCDR) value and the Global Timer value , ETTRG signal occurs and Base Timer starts.(CH29)

Figure 3-4 The Waveform in the Case of Adding Base Timers CH of the Global Timer Match Start Enable. (MODE=1)


- ① It is a start set from Base Timers CH0 to CH3.
A data is immediately updated by GTMSCH for MODE=0, without carrying out a buffer.
- ② Simultaneously with GTMOE="1", the ETEN signal of Base Timer CH by which the start set was carried out. "H" It becomes.
- ③ When a match the External Time Comparison Data Register(ETCDR) value and the Global Timer value , ETTRG signal occurs and Base Timer starts.(CH0)

- ④ When a match the External Time Comparison Data Register(ETCDR) value and the Global Timer value , ETTRG signal occurs and Base Timer starts.(CH1)
- ⑤ It is a start set from Base Timers CH28 to CH29.
It is not updated until the period comparison match flag of Global Timer is outputted for buffer enable mode.
- ⑥ When a match the External Time Comparison Data Register(ETCDR) value and the Global Timer value , ETTRG signal occurs and Base Timer starts.(CH2)
- ⑦ Enable the transfer request of Register data.
- ⑧ By the signal outputted for every period of setup Global Timer.
- ⑨ Global Timer Match Starting Channel register (GT_MSCH0~1) is updated.
- ⑩ Simultaneously with GTMOE="1", the ETEN signal of Base Timer CH by which the start set was carried out. "H" It becomes.
- ⑪ When a match the External Time Comparison Data Register(ETCDR) value and the Global Timer value , ETTRG signal occurs and Base Timer starts.(CH28)
- ⑫ When a match the External Time Comparison Data Register(ETCDR) value and the Global Timer value , ETTRG signal occurs and Base Timer starts.(CH29)

4. Overview of the 16-bit Global Timer

The 16-bit Global Timer supports the 16-bit up count mode.

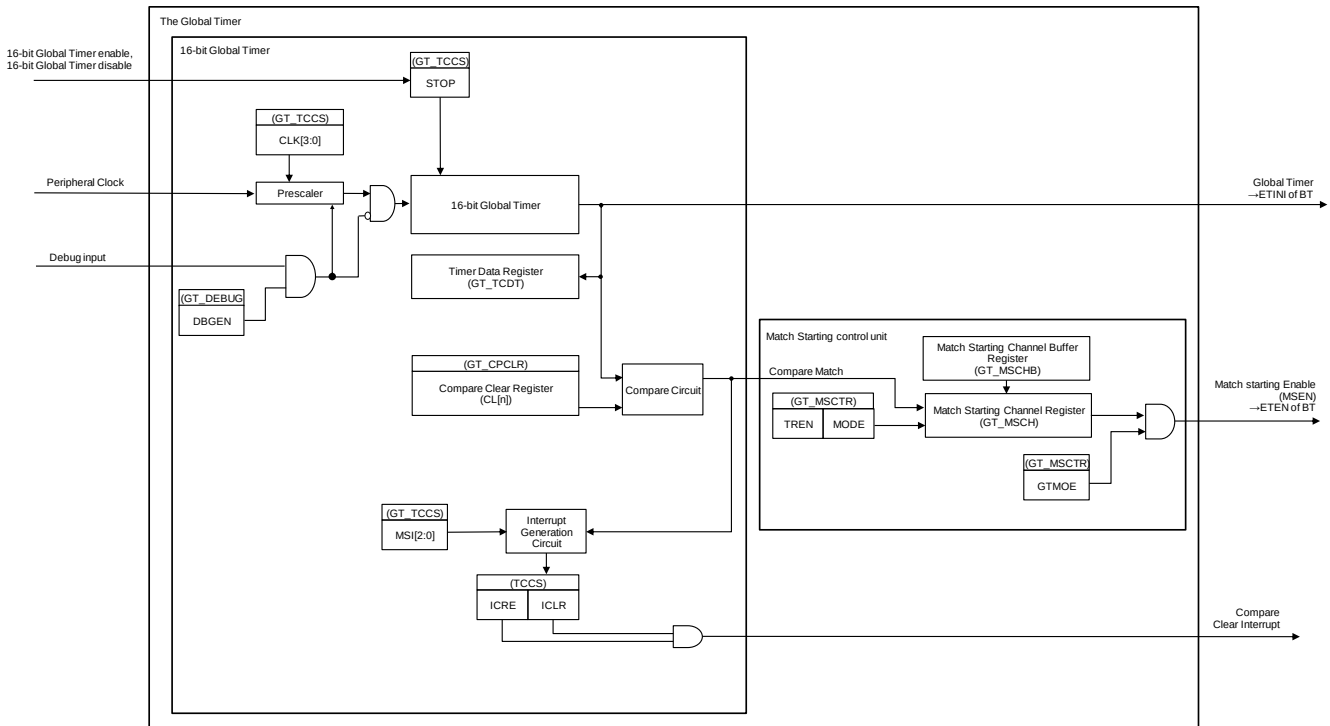
Functions of the 16-bit Global Timer

- The 16-bit Global Timer is composed of the 16-bit up counter, control register, 16-bit compare clear register, and prescaler.
- The 12 types of counter operation clocks (ϕ , $\phi/2$, $\phi/4$, $\phi/8$, $\phi/16$, $\phi/32$, $\phi/64$, $\phi/128$, $\phi/256$, $\phi/512$, $\phi/1024$, and $\phi/2048$) (ϕ : peripheral clock: CLK_LCP1A) can be selected.
- A compare clear interrupt is generated when the values of the compare clear register and the 16-bit counter are compared and their values match.
- The compare clear register has a buffer register (the data written to this buffer register is transferred to the compare clear register). When the 16-bit counter is stopped, the data is transferred as soon as data is written to the buffer. When the 16-bit counter is operating, data is transferred from the buffer upon detecting the count value "0000H".
- The count value is reset to "0000H" when a hardware reset occurs; software clears the timer, or the value of the compare clear register and the count value match.

4.1. Configuration Diagram of the 16-bit Global Timer

Figure 4-1 Figure 4-1 Configuration Diagram of 16-bit Global Timer
 is a configuration diagram of the 16-bit Global Timer.

Figure 4-1 Configuration Diagram of 16-bit Global Timer



5. Explanation of the 16-bit Global Timer Operation

This section provides a summary of the operation of the 16-bit Global Timer.

Operation of the 16-bit Global Timer

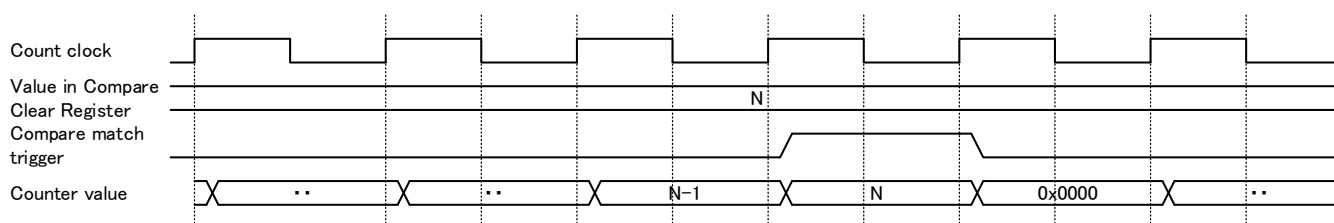
The 16-bit Global Timer starts counting from the value set in the Global Timer Data Register (GT_TCDT) after the timer is set to enabled (GT_TCCS:STOP).

Counter clear

The count value of the Global Timer is cleared to 0 when any of the following conditions is met.

- When the count value matches the value of the Global Timer Compare Clear Register (GT_CPCLR) in the up count.
- When "0000H" is written to the Global Timer Data Register (GT_TCDT) while the Global Timer is stopped (STOP: bit6=1 of the Global Timer State Control Register (GT_TCCS))
- When the hardware is reset. Upon reset, the counter is cleared immediately.

Figure 5-1 Clear Timing of 16-bit Global Timer

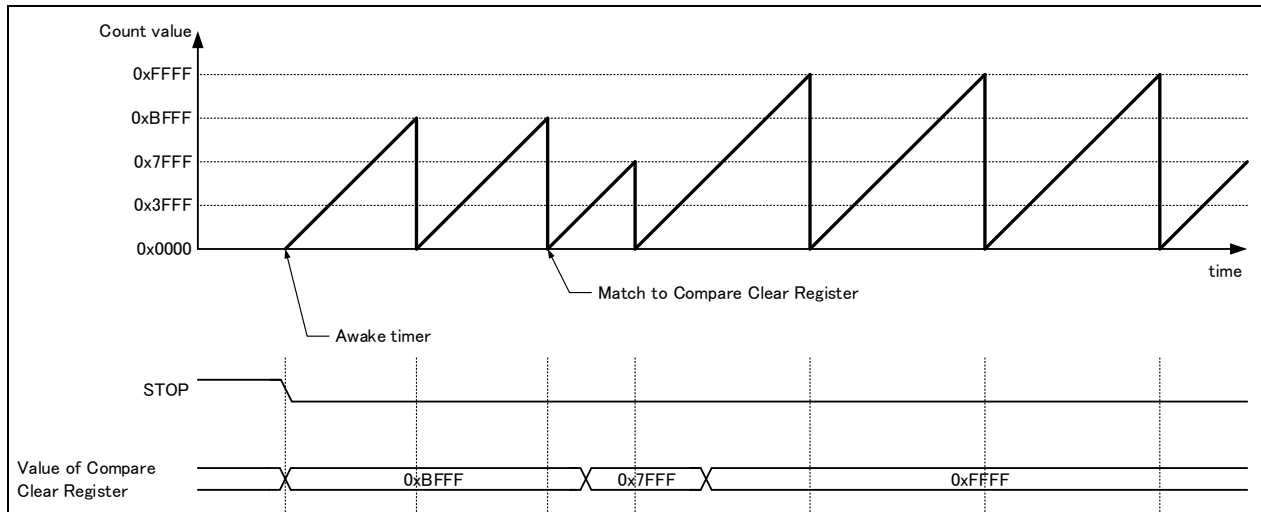


Note:

- Count clock is the count operation clocks.

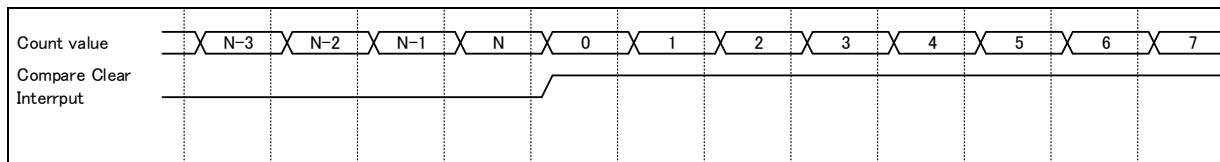
Compare clear

The data can be directly written to the Global Timer Compare Clear Register (GT_CPCLR).

Figure 5-2 Up Count Operation**Timer Interrupt**

The 16-bit Global Timer can generate the following interrupts.

- Compare clear interrupt

Figure 5-3 Interrupt Generated in Up Count**Interrupt Mask Function**

The compare clear interrupt can be masked.

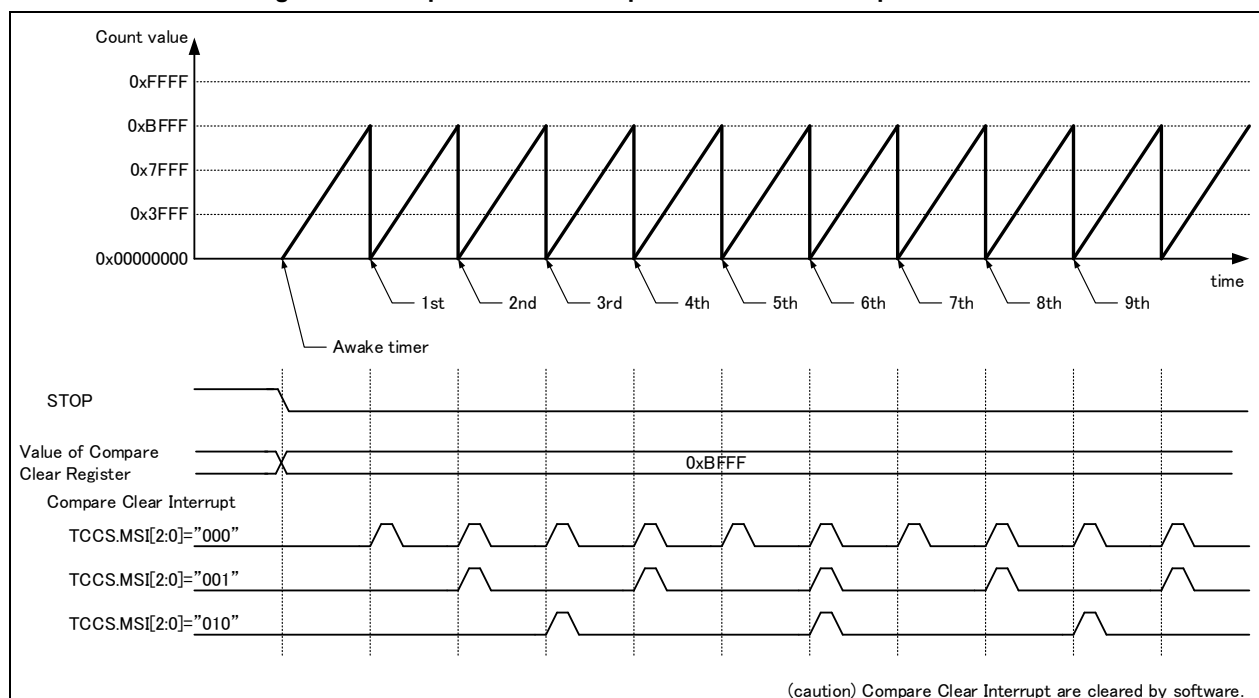
The following describes the case when interrupt is masked.

- The interrupt request flag can be masked by setting the interrupt mask selection bits (MSI2 to GT_MSI0: bit12 to bit10) of the Global Timer State Control Register (GT_TCCS). The interrupt mask selection bits (MSI2 to MSI0: bit12 to bit10) are the 3-bit reload down register that reloads the value when the mask count value reaches "000B". The mask count value can also be loaded by directly writing data to the interrupt mask selection bits (MSI2 to MSI0: bit12 to bit10). The number of mask counts is the value set in the interrupt mask selection bits (MSI2 to MSI0: bit12 to bit10). The interrupt request flag is not masked when the mask count value (MSI2 to MSI0: bit12 to bit10) becomes "000B".

Note:

- If Interrupt mask function "by setting GT_TCCS.MSI[2:0] Register" is used, please write T_TCCS[15:8], GT_TCCSC[15:8] and GT_TCCSS[15:8] after Global Timer stopped.

Figure 5-4 Compare Clear Interrupts to Be Masked in Up Count



5.1. Interrupts of the 16-bit Global Timer

The 16-bit Global Timer has one type of interrupt. : compare interrupt

Global Timer Interrupt

Table 2-1 shows the interrupt control bits and the interrupt factor of the Global Timer.

Table 5-1 Interrupt Control Bits and Interrupt Factor of Global Timer

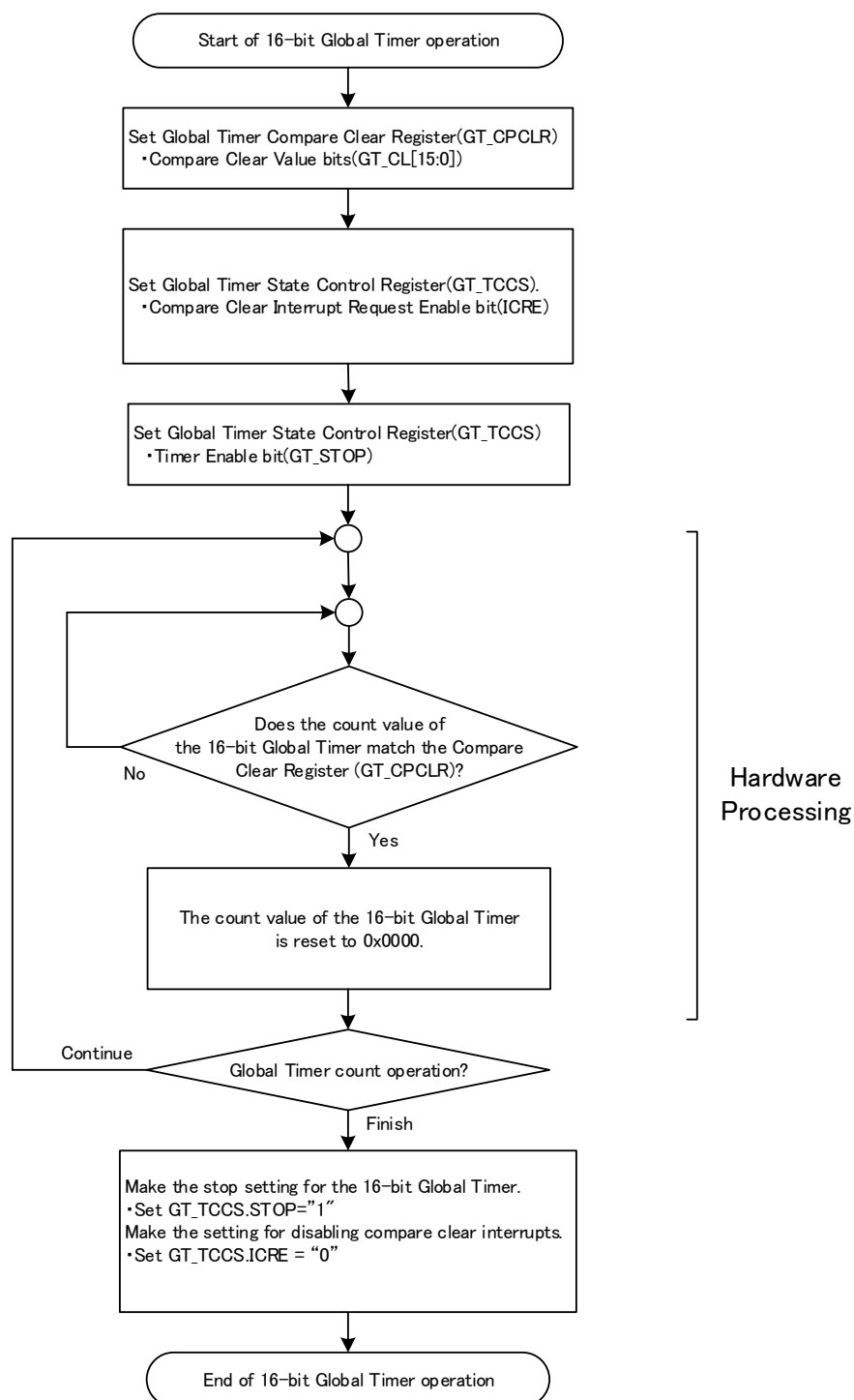
	Global Timer
	Compare Clear
Interrupt request flag bit	Compare clear interrupt flag bit (ICLR:bit9) of the Global Timer State Control Register (GT_TCCS)
Interrupt request enable bit	Compare clear interrupt request enable bit (ICRE:bit8) of the Global Timer State Control Register (GT_TCCS)
Interrupt Factor	The value of the Global Timer matches the value of the Global Timer Compare Clear Register (GT_CPCLR).

"1" is set to the compare clear interrupt flag (ICLR: bit9) of the Global Timer State Control Register (GT_TCCS) when the value of the Global Timer matches the value of the Global Timer Compare Clear Register (GT_CPCLR). When the interrupt request is set to enabled (ICRE: bit8=1 of the Global Timer State Control Register (GT_TCCS)) in this state, then the interrupt request signal (MIRQ) becomes "H".

5.2. Setting Procedure Example of the 16-bit Global Timer

This section provides a setting procedure example of the Global Timer.

Figure 5-5 Setting Procedure Example of Global Timer Operation



5.3. Debug Mode

If it goes into a debug mode, operation of the 16-bit Global Timer can be stopped and debugged.

If all the following conditions are satisfied, it will go into the debug mode.

- The Debug Enable bit (DBGEN) in the Global Timer Debug Register (GT_DEBUG) is "1."
- The debug input (Debug input) is active.

It becomes the following operation when it goes into the debug mode.

- The prescaler stop. The state of prescaler is kept.
- The 16-bit Global Timer stop. Timer value and timer output value are kept.

It becomes the following operation when it restores from the debug mode.

- The prescaler is resumed from the stopped value.
- The 16-bit Global Timer is resumed from the stopped value.

Note:

- *Register access is possible in the debug mode.*

6. Registers of the 16-bit Global Timer

This section provides the register list of the 16-bit Global Timer.

Offset	Address Offset Value / Register Name			
	+3	+2	+1	+0
0000_0000	GT_CPCLR 11111111 11111111 11111111 11111111			
0000_0004	GT_TCDT 11111111 11111111 00000000 00000000			
0000_0008	GT_TCCS 11111111 11111111 00000000 01000000			
0000_000C	-			
0000_0010	GT_TCCSC 11111111 11111111 00000000 00000000			
0000_0014	GT_TCCSS 11111111 11111111 00000000 00000000			
0000_0018	GT_DEBUG 11111111 11111111 00000000 00000000			
0000_001C	-			
0000_0020	GT_MSCTR 11111111 11111111 11111111 00000000			
0000_0024	GT_MSCHB0 00000000 00000000 00000000 00000000			
0000_0028	GT_MSCHB1 00000000 00000000 00000000 00000000			
0000_002C	GT_MSCH0 00000000 00000000 00000000 00000000			
0000_0030	GT_MSCH1 00000000 00000000 00000000 00000000			
0000_0034 0000_03FC	-			

Registers of the 16-bit Global Timer

Table 6-1 Register List of 16-bit Global Timer

Abbreviated Register Name	Register Name	Reference
GT_CPCLR	Global Timer Compare Clear Register	6.1
GT_TCDT	Global Timer Data Register	6.2
GT_TCCS	Global Timer State Control Register	6.3
GT_TCCSC	Global Timer State Control Clear Register	6.4
GT_TCCSS	Global Timer State Control Set Register	6.5
GT_DEBUG	Global Timer Debug Register	6.6
GT_MSCTR	Global Timer Match Starting Control Register	6.7
GT_MSCHB0~1	Global Timer Match Starting Channel Buffer Register	6.8
GT_MSCH0~1	Global Timer Match Starting Channel Register	6.9

Register Bit Locations of the 16-bit Global Timer

Table 6-2 Register Bit Locations of the 16-bit Global Timer

	bit31	bit30	bit29	bit28	bit27	bit26	bit25	bit24
	bit23	bit22	bit21	bit20	bit19	bit18	bit17	bit16
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
GT_CPCLR	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	CL15	CL14	CL13	CL12	CL11	CL10	CL09	CL08
	CL07	CL06	CL05	CL04	CL03	CL02	CL01	CL00
GT_TCDT	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	T15	T14	T13	T12	T11	T10	T09	T08
	T07	T06	T05	T04	T03	T02	T01	T00
GT_TCCS	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	Reserved	Reserved	Reserved	MSI2	MSI1	MSI0	ICLR	ICRE
	Reserved	STOP	Reserved	Reserved	CLK3	CLK2	CLK1	CLK0
GT_TCCSC	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	ICLRC	ICREC
	Reserved	STOPC	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
GT_TCCSS	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	ICRES
	Reserved	STOPS	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
GT_DEBUG	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	DBGEN

GT_MSCTR	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	Reserved	Reserved	Reserved	Reserved	Reserved	TREN	MODE	GTMOE
GT_MSCHB0	GTCH31	GTCH30	GTCH29	GTCH28	GTCH27	GTCH26	GTCH25	GTCH24
	GTCH23	GTCH22	GTCH21	GTCH20	GTCH19	GTCH18	GTCH17	GTCH16
	GTCH15	GTCH14	GTCH13	GTCH12	GTCH11	GTCH10	GTCH9	GTCH8
	GTCH7	GTCH6	GTCH5	GTCH4	GTCH3	GTCH2	GTCH1	GTCH0
GT_MSCHB1	GTCH63	GTCH62	GTCH61	GTCH60	GTCH59	GTCH58	GTCH57	GTCH56
	GTCH55	GTCH54	GTCH53	GTCH52	GTCH51	GTCH50	GTCH49	GTCH48
	GTCH47	GTCH46	GTCH45	GTCH44	GTCH43	GTCH42	GTCH41	GTCH40
	GTCH39	GTCH38	GTCH37	GTCH36	GTCH35	GTCH34	GTCH33	GTCH32
GT_MSCH0	GTCHR31	GTCHR30	GTCHR29	GTCHR28	GTCHR27	GTCHR26	GTCHR25	GTCHR24
	GTCHR23	GTCHR22	GTCHR21	GTCHR20	GTCHR19	GTCHR18	GTCHR17	GTCHR16
	GTCHR15	GTCHR14	GTCHR13	GTCHR12	GTCHR11	GTCHR10	GTCHR9	GTCHR8
	GTCHR7	GTCHR6	GTCHR5	GTCHR4	GTCHR3	GTCHR2	GTCHR1	GTCHR0
GT_MSCH1	GTCHR63	GTCHR62	GTCHR61	GTCHR60	GTCHR59	GTCHR58	GTCHR57	GTCHR56
	GTCHR55	GTCHR54	GTCHR53	GTCHR52	GTCHR51	GTCHR50	GTCHR49	GTCHR48
	GTCHR47	GTCHR46	GTCHR45	GTCHR44	GTCHR43	GTCHR42	GTCHR41	GTCHR40
	GTCHR39	GTCHR38	GTCHR37	GTCHR36	GTCHR35	GTCHR34	GTCHR33	GTCHR32

6.1. Global Timer Compare Clear Register (GT_CPCLR)

Compare Clear Register (GT_CPCLR)

bit	31	30	29	28	27	26	25	24
Field	Reserved							
R/W Attribute	R1,WX							
Protection Attribute	-							
Initial Value	11111111							

bit	23	22	21	20	19	18	17	16
Field	Reserved							
R/W Attribute	R1,WX							
Protection Attribute	-							
Initial Value	11111111							

bit	15	14	13	12	11	10	9	8
Field	CL15	CL14	CL13	CL12	CL11	CL10	CL09	CL08
R/W Attribute	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Protection Attribute	-	-	-	-	-	-	-	-
Initial Value	1	1	1	1	1	1	1	1

bit	7	6	5	4	3	2	1	0
Field	CL07	CL06	CL05	CL04	CL03	CL02	CL01	CL00
R/W Attribute	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Protection Attribute	-	-	-	-	-	-	-	-
Initial Value	1	1	1	1	1	1	1	1

[bit31:16] Reserved bits

"1" is always read from this bit.

Writing data to these bits has no effect on the operation.

[bit15:0] CL15 to CL00: Compare clear value bits

The compare clear register (GT_CPCLR) is used to compare the count value of the Global Timer.

The count value of the Global Timer is reset to "0000H" when the value of this register matches the count value of the Global Timer.

Notes:

- Do not set "0x0000" in the Global Timer Compare Clear Register (GT_CPCLR).
- For access to this register, use half word access instructions.

6.2. Global Timer Data Register (GT_TCDT)

The timer data register (GT_TCDT) reads the count value of the Global Timer. This register can also be used to set the count value of the Global Timer.

bit	31	30	29	28	27	26	25	24
Field	Reserved							
R/W Attribute	R1,WX							
Protection Attribute	-							
Initial Value	11111111							

Bit	23	22	21	20	19	18	17	16
Field	Reserved							
R/W Attribute	R1,WX							
Protection Attribute	-							
Initial Value	11111111							

bit	15	14	13	12	11	10	9	8
Field	T15	T14	T13	T12	T11	T10	T09	T08
R/W Attribute	R,W	R,W	R,W	R,W	R,W	R,W	R,W	R,W
Protection Attribute	-	-	-	-	-	-	-	-
Initial Value	0	0	0	0	0	0	0	0

bit	7	6	5	4	3	2	1	0
Field	T07	T06	T05	T04	T03	T02	T01	T00
R/W Attribute	R,W	R,W	R,W	R,W	R,W	R,W	R,W	R,W
Protection Attribute	-	-	-	-	-	-	-	-
Initial Value	0	0	0	0	0	0	0	0

[bit31:16] Reserved bits

"1" is always read from this bit.

Writing data to these bits has no effect on the operation.

[bit15:0] T15 to T00: Global Timer data value bits

The timer data register (GT_TCDT) is used to read the count value of the Global Timer.

The count value can be set by writing a value to this register. However, a value needs to be written while the Global Timer is stopped (STOP: bit 6=1 of the timer state control register (GT_TCCS)).

The counter is cleared to the count value "0x0000" as soon as any of the following factors occurs.

- Hardware reset
- The value of the compare clear register (GT_CPCLR) matches.

Note:

- For access to this register, use half word access instructions.

6.3. Global Timer State Control Register (GT_TCCS)

The timer state control register (GT_TCCS) is a register that is used to control the operation of the Global Timer.

For details on writing to this register, see "7.Precautions for Using This Device."

bit	31	30	29	28	27	26	25	24
Field	Reserved							
R/W Attribute	R1,WX							
Protection Attribute	-							
Initial Value	11111111							

bit	23	22	21	20	19	18	17	16
Field	Reserved							
R/W Attribute	R1,WX							
Protection Attribute	-							
Initial Value	11111111							

bit	15	14	13	12	11	10	9	8
Field	Reserved			MSI2	MSI1	MSI0	ICLR	ICRE
R/W Attribute	R0/WX			R,W	R,W	R,W	R	R/W
Protection Attribute	-			-	-	-	-	-
Initial Value	000			0	0	0	0	0

bit	7	6	5	4	3	2	1	0
Field	Reserved	STOP	Reserved		CLK3	CLK2	CLK1	CLK0
R/W Attribute	R0/WX	R/W	R0/WX		R/W	R/W	R/W	R/W
Protection Attribute	-	-	-		-	-	-	-
Initial Value	0	1	00		0	0	0	0

[bit31:16] Reserved bits

"1" is always read from this bit.

Writing data to these bits has no effect on the operation.

[bit15:13] Reserved bits

"0" is always read from this bit.

Writing data to these bits has no effect on the operation.

[bit12:10] MSI2 to MSI0: Interrupt mask selection bits

- These bits are used to set the number of times to mask the compare clear interrupt flag.
- When these bits are set to "000B", the interrupt flags are not masked.

Bit			Description
MSI2	MSI1	MSI0	
0	0	0	Generate an interrupt flag at the first match occurrence.
0	0	1	Generate an interrupt flag at the second match occurrence.
0	1	0	Generate an interrupt flag at the third match occurrence.
0	1	1	Generate an interrupt flag at the fourth match occurrence.
1	0	0	Generate an interrupt flag at the fifth match occurrence.
1	0	1	Generate an interrupt flag at the sixth match occurrence.
1	1	0	Generate an interrupt flag at the seventh match occurrence.
1	1	1	Generate an interrupt flag at the eighth match occurrence.

Notes:

The value read is a mask counter value. The mask counter is a decrement counter.

- The written data is written to the mask register.
- If Interrupt mask function "by setting GT_TCCS.MSI[2:0] Register" is used, please write GT_TCCS[15:8], GT_TCCSC[15:8] and GT_TCCSS[15:8] after Global Timer stopped.

[bit9] ICLR: Compare clear interrupt flag bit

This bit is set to "1" when the value of the Global Timer Compare Clear Registers (GT_CPCLR) and the value of the Global Timer match.

This bit is a read-only bit. Writing data to these bits has no effect on the operation.

This bit is cleared by writing "1" to the ICLRC bit of the Global Timer State Control Clear Register (GT_TCCSC).

bit	Description
0	0 No compare clear.
1	1 Compare clear match.

Notes:

- This bit is set to "1" when the interrupt flag set by the interrupt mask selection bits (MSI2 to MSI0) occurs. This bit is not set to "1" when no interrupt occurs.

[bit8] ICRE: Compare clear interrupt request enable bit

When this bit is set to "1" and the compare clear interrupt flag bit (ICLR: bit9) is set to "1", an interrupt request to the CPU is generated.

This bit is cleared to "0" by writing "1" to the ICREC bit of the Global Timer State Control Clear Register (GT_TCCSC).

This bit is set to "1" by writing "1" to the ICRES bit of the Global Timer State Control Set Register (GT_TCCSS).

bit	Description
0	Disable interrupt requests.
1	Enable interrupt requests.

[bit7] Reserved bits

"0" is always read from this bit.

Writing data to these bits has no effect on the operation.

[bit6] STOP: Timer enable bit

This bit is used to stop/start counting of the Global Timer.

When this bit is set to "0".

The Global Timer starts counting.

When this bit is set to "1".

The Global Timer stops counting.

This bit is cleared to "0" by writing "1" to the STOPC bit of the Global Timer State Control Clear Register (GT_TCCSC).

This bit is set to "1" by writing "1" to the STOPS bit of the Global Timer State Control Set Register (GT_TCCSS).

bit	Description
0	Enable counting (start counting).
1	Disable counting (stop counting).

Notes:

- After counting of the Global Timer is stopped , the following initialization setting is necessary.
 1. Initializes of the Global Timer count value.
It writes "0000_0000h" to the Global Timer Data Register(GT_TCDT)[15:0].
 2. Disable of an ETEN(external timer compare enabling signal) signal.
It sets Global Timer Match Output Enable bit(GTMODE) in Global Timer Match Starting Control Register(GT_MSCTR) to "0"

[bit5:4] Reserved bits

"0" is always read from this bit..

Writing data to these bits has no effect on the operation.

[bit3:0] CLK3 to CLK0: Clock frequency selection bits

These bits are used to select the count clock frequency of the Global Timer.

The clock frequency is changed immediately upon setting these bits.

bit				Description					
CLK3	CLK2	CLK1	CLK0	Count Clock	$\phi = 40$ MHz	$\phi = 20$ MHz	$\phi = 10$ MHz	$\phi = 5$ MHz	$\phi = 2.5$ MHz
0	0	0	0	Φ	25 ns	50 ns	100 ns	200 ns	400 ns
0	0	0	1	$\Phi/2$	50 ns	100 ns	200 ns	400 ns	800 ns
0	0	1	0	$\Phi/4$	100 ns	200 ns	400 ns	800 ns	1.6 μ s
0	0	1	1	$\Phi/8$	200 ns	400 ns	800 ns	1.6 μ s	3.2 μ s
0	1	0	0	$\Phi/16$	400 ns	800 ns	1.6 μ s	3.2 μ s	6.4 μ s
0	1	0	1	$\Phi/32$	800 ns	1.6 μ s	3.2 μ s	6.4 μ s	12.8 μ s
0	1	1	0	$\Phi/64$	1.6 μ s	3.2 μ s	6.4 μ s	12.8 μ s	25.6 μ s
0	1	1	1	$\Phi/128$	3.2 μ s	6.4 μ s	12.8 μ s	25.6 μ s	51.2 μ s
1	0	0	0	$\Phi/256$	6.4 μ s	12.8 μ s	25.6 μ s	51.2 μ s	102.4 μ s
1	0	0	1	$\Phi/512$	12.8 μ s	25.6 μ s	51.2 μ s	102.4 μ s	204.8 μ s
1	0	1	0	$\Phi/1024$	25.6 μ s	51.2 μ s	102.4 μ s	204.8 μ s	409.6 μ s
1	0	1	1	$\Phi/2048$	51.2 μ s	102.4 μ s	204.8 μ s	409.6 μ s	819.2 μ s
Other settings are prohibited.				-	-	-	-	-	-

ϕ : Peripheral clock: CLK_LCP1A

6.4. Global Timer State Control Clear register (GT_TCCSC)

The Global Timer State Control Clear Register (GT_TCCSC) is a register that is used to clear bits of the Global Timer State Control Register (GT_TCCS).

For details on writing to this register, see "7.Precautions for Using This Device."

bit	31	30	29	28	27	26	25	24
Field	Reserved							
R/W Attribute	R1,WX							
Protection Attribute	-							
Initial Value	11111111							

bit	23	22	21	20	19	18	17	16
Field	Reserved							
R/W Attribute	R1,WX							
Protection Attribute	-							
Initial Value	11111111							

bit	15	14	13	12	11	10	9	8
Field	Reserved						ICLRC	ICREC
R/W Attribute	R0,WX						R0,W	R0,W
Protection Attribute	-						-	-
Initial Value	000000						0	0

bit	7	6	5	4	3	2	1	0
Field	Reserved	STOPC	Reserved					
R/W Attribute	R0,WX	R0,W	R0,WX					
Protection Attribute	-	-	-					
Initial Value	0	0	00000					

[bit31:16] Reserved bits

"1" is always read from this bit.

Writing data to these bits has no effect on the operation.

[bit15:10] Reserved bits

"0" is always read from this bit.

Writing data to these bits has no effect on the operation.

[bit9] ICLRC: ICLR clear bit

When "1" is written to this bit, the compare clear interrupt flag bit (ICLR) of the Global Timer State Control Register (GT_TCCS) is cleared. "0" is always read from this bit.

bit	Description
0	Affect neither this bit nor the compare clear interrupt flag bit (ICLR) of the Global Timer State Control Register (GT_TCCS).
1	Clear the compare clear interrupt flag bit (ICLR) of the Global Timer State Control Register (GT_TCCS).

[bit8] ICREC: ICRE clear bit

When "1" is written to this bit, the compare clear interrupt request enable bit (ICRE) of the Global Timer State Control Register (GT_TCCS) is cleared. "0" is always read from this bit.

Bit	Description
0	Affect neither this bit nor the compare clear interrupt request enable bit (ICRE) of the Global Timer State Control Register (GT_TCCS).
1	Clear the compare clear interrupt request enable bit (ICRE) of the Global Timer State Control Register (GT_TCCS).

[bit7] Reserved bits

"0" is always read from this bit.

Writing data to these bits has no effect on the operation.

[bit6] STOPC: STOP clear bit

When "1" is written to this bit, the timer enable bit (STOP) of the Global Timer State Control Register (GT_TCCS) is cleared. "0" is always read from this bit.

bit	Description
0	Affect neither this bit nor the timer enable bit (STOP) of the Global Timer State Control Register (GT_TCCS).
1	Clear the timer enable bit (STOP) of the Global Timer State Control Register (GT_TCCS).

[bit5:0] Reserved bits

"0" is always read from this bit. Always write "0" to this bit.

Writing data to these bits has no effect on the operation.

6.5. Global Timer State Control Set register (GT_TCCSS)

The Global Timer State Control Set Register (GT_TCCSS) is a register that is used to set bits of the Global Timer State Control Register (GT_TCCS).

For details on writing to this register, see "7.Precautions for Using This Device."

bit	31	30	29	28	27	26	25	24
Field	Reserved							
R/W Attribute	R1,WX							
Protection Attribute	-							
Initial Value	11111111							

bit	23	22	21	20	19	18	17	16
Field	Reserved							
R/W Attribute	R1,WX							
Protection Attribute	-							
Initial Value	11111111							

bit	15	14	13	12	11	10	9	8
Field	Reserved							ICRES
R/W Attribute	R0,WX							R0,W
Protection Attribute	-							-
Initial Value	0000000							0

bit	7	6	5	4	3	2	1	0
Field	Reserved	STOPS	Reserved					
R/W Attribute	R0,WX	R0,W	R0,WX					
Protection Attribute	-	-	-					
Initial Value	0	0	000000					

[bit31:16] Reserved bits

"1" is always read from this bit.

Writing data to these bits has no effect on the operation.

[bit15:9] Reserved bits

"0" is always read from this bit.

Writing data to these bits has no effect on the operation.

[bit8] ICRES: ICRE set bit

When "1" is written to this bit, the compare clear interrupt request enable bit (ICRE) of the Global Timer State Control Register (GT_TCCS) is set to "1". "0" is always read from this bit.

Bit	Description
0	Affect neither this bit nor the compare clear interrupt request enable bit (ICRE) of the Global Timer State Control Register (GT_TCCS).
1	Set the compare clear interrupt request enable bit (ICRE) of the Global Timer State Control Register (GT_TCCS).

[bit7] Reserved bits

"0" is always read from this bit.

Writing data to these bits has no effect on the operation.

[bit6] STOPS: STOP set bit

When "1" is written to this bit, the timer enable bit (STOP) of the Global Timer State Control Register (GT_TCCS) is set to "1". "0" is always read from this bit.

Bit	Description
0	Affect neither this bit nor the timer enable bit (STOP) of the Global Timer State Control Register (GT_TCCS).
1	Set the timer enable bit (STOP) of the Global Timer State Control Register (GT_TCCS).

[bit5:0] Reserved bits

"0" is always read from this bit.

Writing data to these bits has no effect on the operation.

6.6. Global Timer Debug Register (GT_DEBUG)

The Global Timer Debug Register (GT_DEBUG) performs enable/disable setting of debug.

BIT_OFFSET	31	30	29	28	27	26	25	24
BIT_NAME	Reserved							
ACCESS_TYPE	R1,WX							
PROT_TYPE	-							
INITIAL_VALUE	11111111							

BIT_OFFSET	23	22	21	20	19	18	17	16
BIT_NAME	Reserved							
ACCESS_TYPE	R1,WX							
PROT_TYPE	-							
INITIAL_VALUE	11111111							

BIT_OFFSET	15	14	13	12	11	10	9	8
BIT_NAME	Reserved							
ACCESS_TYPE	R0,W0							
PROT_TYPE	-							
INITIAL_VALUE	00000000							

BIT_OFFSET	7	6	5	4	3	2	1	0
BIT_NAME	Reserved							DBGEN
ACCESS_TYPE	R0,W0							R/W
PROT_TYPE	-							
INITIAL_VALUE	00000000							0

[bit31:16] Reserved bits

The read value is "1".

If writing to this bit, write "1".

[bit15:1] Reserved bits

The read value is "0".

If writing to this bit, write "0".

[bit0] DBGEN: Debug Enable bit

It is the bit which permits stopping operation of a 16-bit Global Timer with the debug input (Debug input).

bit	Description
0	Disable
1	Enable

6.7. Global Timer Match Starting Control Register (GT_MSCTR)

This Global Timer Match Start Control Register controls the Global Timer Match Start Enable Signal which it inputs into the Base Timer.

bit	31	30	29	28	27	26	25	24
Field	Reserved							
R/W Attribute	R1,WX							
Protection Attribute	-							
Initial Value	11111111							

bit	23	22	21	20	19	18	17	16
Field	Reserved							
R/W Attribute	R1,WX							
Protection Attribute	-							
Initial Value	11111111							

bit	15	14	13	12	11	10	9	8
Field	Reserved							
R/W Attribute	R1,WX							
Protection Attribute	-							
Initial Value	11111111							

bit	7	6	5	4	3	2	1	0
Field	Reserved					TREN	MODE	GTMOE
R/W Attribute	R0,WX					R/W	R/W	R/W
Protection Attribute	-							
Initial Value	00000					0	0	0

[bit31:8] Reserved bits

"1" is always read from this bit.

Writing data to these bits has no effect on the operation.

[bit7:3] Reserved bits

"0" is always read from this bit.

Writing data to these bits has no effect on the operation.

[bit2] TREN: Transfer Request Enable bit

It uses this bit in order to enable a transmission request of the Global Timer Match Starting Channel Buffer Register (GT_MSCHB0~1) value.

When this bit is "0", even if the count value of the Global Timer is match with a comparison clear register (GT_CPCLR), the Global Timer Match Starting Channel Buffer Register (GT_MSCHB0~1) value is not transmitted.

When this bit is "1", even if the count value of the Global Timer is match with a comparison clear register (GT_CPCLR), the Global Timer Match Starting Channel Buffer Register (GT_MSCHB0~1) value is transmitted to the Global Timer Match Starting Channel Register (GT_MSCH0~1).

Bit	Description
0	Disable the transfer request of Register data
1	Enable the transfer request of Register data

Notes:

When changing the Global Timer Match Starting Channel Buffer Register (GT_MSCHB0~1) set, it sets this bit to "0."

[bit1] MODE: Mode Select bit

It uses this bit in order to enable the Global Timer Match Starting Channel Buffer Register (GT_MSCHB0~1).

The Global Timer match starting enabling signal of each Base Timer channel is controlled by this bit setup as follows.

- When the is MODE ="0"
 - The Global Timer Match Starting Channel Buffer Register (GT_MSCHB0~1) is invalid.
 - After writing "1" in GTMOE bit, it becomes external timer comparison enabling signal to the Base Timer channel set as 1 (ETEN)" H" by a GT_MSCH0~1 register at once.
- When the is MODE ="1"
 - The Global Timer Match Starting Channel Buffer Register (GT_MSCHB0~1) is valid.
 - The data which was written in the Global Timer Match Start Channel Buffer Register (GT_MSCHB0~1) and was held, After writing "1" in TREN bit, if the Global Timer counting value and the Global Time Compare Clear Register (GT_CPCLR) matches, it is transmitted to the Global Timer Match Starting Channel Register (GT_MSCH0~1), the External Timer Compare Enable Signal (ETEN) to the Base Timer Channel set as "1" in the Global Timer Match Start Channel Register (GT_MSCH0~1) becomes "H".

Bit	Description
0	Buffer Disable
1	Buffer Enable

[bit0] GTMOE: Global Timer Match Output Enable bit

It uses this as an output Enable of the External Timer Compare Enable Signal (ETEN) of Base Timers.

When this bit is "0", the External Timer Compare Enable Signal (ETEN) to the channel of all Base Timers is set to "L".

- It outputs "H" as an external timer compare enabling signal (ETEN) at the time of GTCH="1".
- It outputs "L" as an external timer compare enabling signal (ETEN) at the time of GTCH="0".

Bit	Description
0	Disable the output of all External Timer Compare Enable Signals.
1	Enable the output of all External Timer Compare Enable Signals.

6.8. Global Timer Match Starting Channel Buffer Register (GT_MSCHB0~1)

The Global Timer Match Startup Channel Buffer Register (GT_MSCHB0~1) is a buffer register of the Global Timer Match Startup Channel Register (GT_MSCH0~1)

There is the undermentioned two timing by which this register value is transmitted to the Global Timer Match Startup Channel Register (GT_MSCH0~1).

- The Global Timer is stopping (STOP = "1" of a Global Timer Status Control Register (GT_TCCS)), or it is at the disabled (MODE = "0" of Global Timer Match Starting Control Register (GT_MSCTR)) time about the STOP = "1" buffer function of the Global Timer Status Control Register (GT_TCCS), the value of a Global Timer Match Start Channel Buffer Register (GT_MSCHB0~1) is transmitted to a Global Timer Match Start Channel Register (GT_MSCH0~1) at once.
- The buffer function is at the enable (MODE = "1" of Global Timer Match Starting Control Register (GT_MSCTR)) time, it sets a transmission request of a register value as enable (TREN bit = "1" of Global Timer Match Starting Control Register (GT_MSCTR)), and when the count value of the Global Timer matches the value of the Global Timer Compare Clear Register (GT_CPCLR), the value of a Global Timer Match Start Channel Buffer Register (GT_MSCHB0~1) is transmitted to the Global Timer Match Start Channel Register (GT_MSCH0~1).

Global Timer Match Starting Channel Buffer Registers (GT_MSCHB0)

Bit	31	30	29	28	27	26	25	24
Field	GTCH31	GTCH30	GTCH29	GTCH28	GTCH27	GTCH26	GTCH25	GTCH24
R/W Attribute	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Protection Attribute	-	-	-	-	-	-	-	-
Initial Value	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
Field	GTCH23	GTCH22	GTCH21	GTCH20	GTCH19	GTCH18	GTCH17	GTCH16
R/W Attribute	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Protection Attribute	-	-	-	-	-	-	-	-
Initial Value	0	0	0	0	0	0	0	0

bit	15	14	13	12	11	10	9	8
Field	GTCH15	GTCH14	GTCH13	GTCH12	GTCH11	GTCH10	GTCH9	GTCH8
R/W Attribute	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Protection Attribute	-	-	-	-	-	-	-	-
Initial Value	0	0	0	0	0	0	0	0

bit	7	6	5	4	3	2	1	0
Field	GTCH7	GTCH6	GTCH5	GTCH4	GTCH3	GTCH2	GTCH1	GTCH0
R/W Attribute	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Protection Attribute	-	-	-	-	-	-	-	-
Initial Value	0	0	0	0	0	0	0	0

[bit31:0] GTCH31~0 : Global Timer Match Starting Channel Buffer bits

Bit	Description
0	Global Timer Match Starting Disabled
1	Global Timer Match Starting Enabled

Global Timer Match Starting Channel Buffer Registers (GT_MSCHB1)

bit	31	30	29	28	27	26	25	24
Field	GTCH63	GTCH62	GTCH61	GTCH60	GTCH59	GTCH58	GTCH57	GTCH56
R/W Attribute	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Protection Attribute	-	-	-	-	-	-	-	-
Initial Value	0	0	0	0	0	0	0	0

bit	23	22	21	20	19	18	17	16
Field	GTCH55	GTCH54	GTCH53	GTCH52	GTCH51	GTCH50	GTCH49	GTCH48
R/W Attribute	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Protection Attribute	-	-	-	-	-	-	-	-
Initial Value	0	0	0	0	0	0	0	0

bit	15	14	13	12	11	10	9	8
Field	GTCH47	GTCH46	GTCH45	GTCH44	GTCH43	GTCH42	GTCH41	GTCH40
R/W Attribute	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Protection Attribute	-	-	-	-	-	-	-	-
Initial Value	0	0	0	0	0	0	0	0

bit	7	6	5	4	3	2	1	0
Field	GTCH39	GTCH38	GTCH37	GTCH36	GTCH35	GTCH34	GTCH33	GTCH32
R/W Attribute	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Protection Attribute	-	-	-	-	-	-	-	-
Initial Value	0	0	0	0	0	0	0	0

[bit31:0] GTCH63~32 : Global Timer Match Starting Channel Buffer bits

Bit	Description
0	Global Timer Match Starting Disabled
1	Global Timer Match Starting Enabled

Notes:

- At the time of the Global Timer stop, it is after the Global Timer Match Start Channel Buffer Register (GT_MSCHB0~1) set, please permit the External Timer Compare Enabling-Signal Output (GTMOE = "1" of Global Timer Match Starting Control Register (GT_MSCTR)).
- At the case of TREN = "1" (transmission request Clearance) of Global Timer Match Starting Control register (GT_MSCTR), please do not change the Global Timer Match Start Channel Buffer-Register (GT_MSCHB0~1) set.
- For access to this register, use word access instructions.

6.9. Global Timer Match Starting Channel Register (GT_MSCH0~1)

This register displays the value transmitted from the Global Timer Match Starting Channel Buffer Register (GT_MSCHB0~1) register.

Global Timer Match Starting Channel Registers (GT_MSCH0)

bit	31	30	29	28	27	26	25	24
Field	GTCHR31	GTCHR30	GTCHR29	GTCHR28	GTCHR27	GTCHR26	GTCHR25	GTCHR24
R/W Attribute	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX
Protection Attribute	-	-	-	-	-	-	-	-
Initial Value	0	0	0	0	0	0	0	0

bit	23	22	21	20	19	18	17	16
Field	GTCHR23	GTCHR22	GTCHR21	GTCHR20	GTCHR19	GTCHR18	GTCHR17	GTCHR16
R/W Attribute	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX
Protection Attribute	-	-	-	-	-	-	-	-
Initial Value	0	0	0	0	0	0	0	0

bit	15	14	13	12	11	10	9	8
Field	GTCHR15	GTCHR14	GTCHR13	GTCHR12	GTCHR11	GTCHR10	GTCHR9	GTCHR8
R/W Attribute	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX
Protection Attribute	-	-	-	-	-	-	-	-
Initial Value	0	0	0	0	0	0	0	0

bit	7	6	5	4	3	2	1	0
Field	GTCHR7	GTCHR6	GTCHR5	GTCHR4	GTCHR3	GTCHR2	GTCHR1	GTCHR0
R/W Attribute	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX
Protection Attribute	-	-	-	-	-	-	-	-
Initial Value	0	0	0	0	0	0	0	0

[bit31:0] GTCHR31~0 : Global Timer Match Starting Channel bits

This bit becomes external timer compare enabling-signal to the Base Timer channel which the Global Timer match start is permitted and corresponds when it is 1" (ETEN)" H".

Bit	Description
0	Global Timer Match Starting Disabled
1	Global Timer Match Starting Enabled

Global Timer Match Starting Channel Registers (GT_MSCH1)

bit	31	30	29	28	27	26	25	24
Field	GTCHR63	GTCHR62	GTCHR61	GTCHR60	GTCHR59	GTCHR58	GTCHR57	GTCHR56
R/W Attribute	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX
Protection Attribute	-	-	-	-	-	-	-	-
Initial Value	0	0	0	0	0	0	0	0

bit	23	22	21	20	19	18	17	16
Field	GTCHR55	GTCHR54	GTCHR53	GTCHR52	GTCHR51	GTCHR50	GTCHR49	GTCHR48
R/W Attribute	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX
Protection Attribute	-	-	-	-	-	-	-	-
Initial Value	0	0	0	0	0	0	0	0

bit	15	14	13	12	11	10	9	8
Field	GTCHR47	GTCHR46	GTCHR45	GTCHR44	GTCHR43	GTCHR42	GTCHR41	GTCHR40
R/W Attribute	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX
Protection Attribute	-	-	-	-	-	-	-	-
Initial Value	0	0	0	0	0	0	0	0

bit	7	6	5	4	3	2	1	0
Field	GTCHR39	GTCHR38	GTCHR37	GTCHR36	GTCHR35	GTCHR34	GTCHR33	GTCHR32
R/W Attribute	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX
Protection Attribute	-	-	-	-	-	-	-	-
Initial Value	0	0	0	0	0	0	0	0

[bit31:0] GTCHR63~32 : Global Timer Match Starting Channel bits

This bit becomes external timer compare enabling-signal to the Base Timer channel which the Global Timer match start is permitted and corresponds when it is 1" (ETEN)" H".

Bit	Description
0	Global Timer Match Starting Disabled
1	Global Timer Match Starting Enabled

Notes:

- For access to this register, use word access instructions.

7. Precautions for Using This Device

The following shows the notes when using the 16-bit Global Timer.

Notes to observe when accessing a register

When accessing the compare clear register (GT_CPCLR)

Use half word access instructions to the Global Timer Compare Clear Register (GT_CPCLR)

When accessing the timer state control registers (GT_TCCS)

- This register supports writing from the bit-band alias area. For the bit-band alias area, see the chapter of "Bit-Band Unit" in Traveo™ Platform hardware manual.
- To clear a specified bit of this register, clear the bit by writing "1" to the applicable bit of the Global Timer State Control Clear Register (GT_TCCSC).
- To set a specified bit of this register, set the bit by writing "1" to the applicable bit of the Global Timer State Control Set Register (GT_TCCSS).
- Data can be written directly to this register only when writing to all bits.
- In the normal reading mode, the interrupt mask counter value is read from MSI2 to MSI0.
- If Interrupt mask function "by setting TCCS.MSI[2:0] Register" is used, please write GT_TCCS[15:8], GT_TCCSC[15:8] and GT_TCCSS[15:8] after Global Timer stopped.

When accessing the Global Timer Match Starting Channel Buffer Register (GT_MSCHB0~1)

Use word access instructions to the Global Timer Match Starting Channel Buffer Register (GT_MSCHB0~1)

When accessing the Global Timer Match Starting Channel Register (GT_MSCH0~1)

Use word access instructions to the Global Timer Match Starting Channel Register (GT_MSCH0~1)

Notes when operating the Global Timer

When setting using a program

- The compare clear flag is not set if the timer starts counting when the value of the Global Timer Compare Clear Register (GT_CPCLR) matches the count value.
- Set any values other than 0 to the Global Timer Compare Clear Register (GT_CPCLR). Note that the following operations occur if 0 is set.
 - When the count value is updated to 0 and fixed to 0. Then, the compare clear flag are set at every count clock.

CHAPTER 19: 32-Bit Free-Run Timer



This chapter describes the functions of the 32-bit Free-Run Timer.

1. Overview of the 32-bit Free-run Timer
2. Block Diagram of the 32-bit Free-run Timer
3. Operation of the 32-bit Free-run Timer
4. Registers of the 32-bit Free-run Timer
5. Precautions for Using This Device

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1. Overview of the 32-Bit Free-Run Timer

The 32-bit Free-run Timer supports the 32-bit up count mode or up/down count mode. This timer can be used with the 32-bit Input Capture and the 32-bit Output Compare.

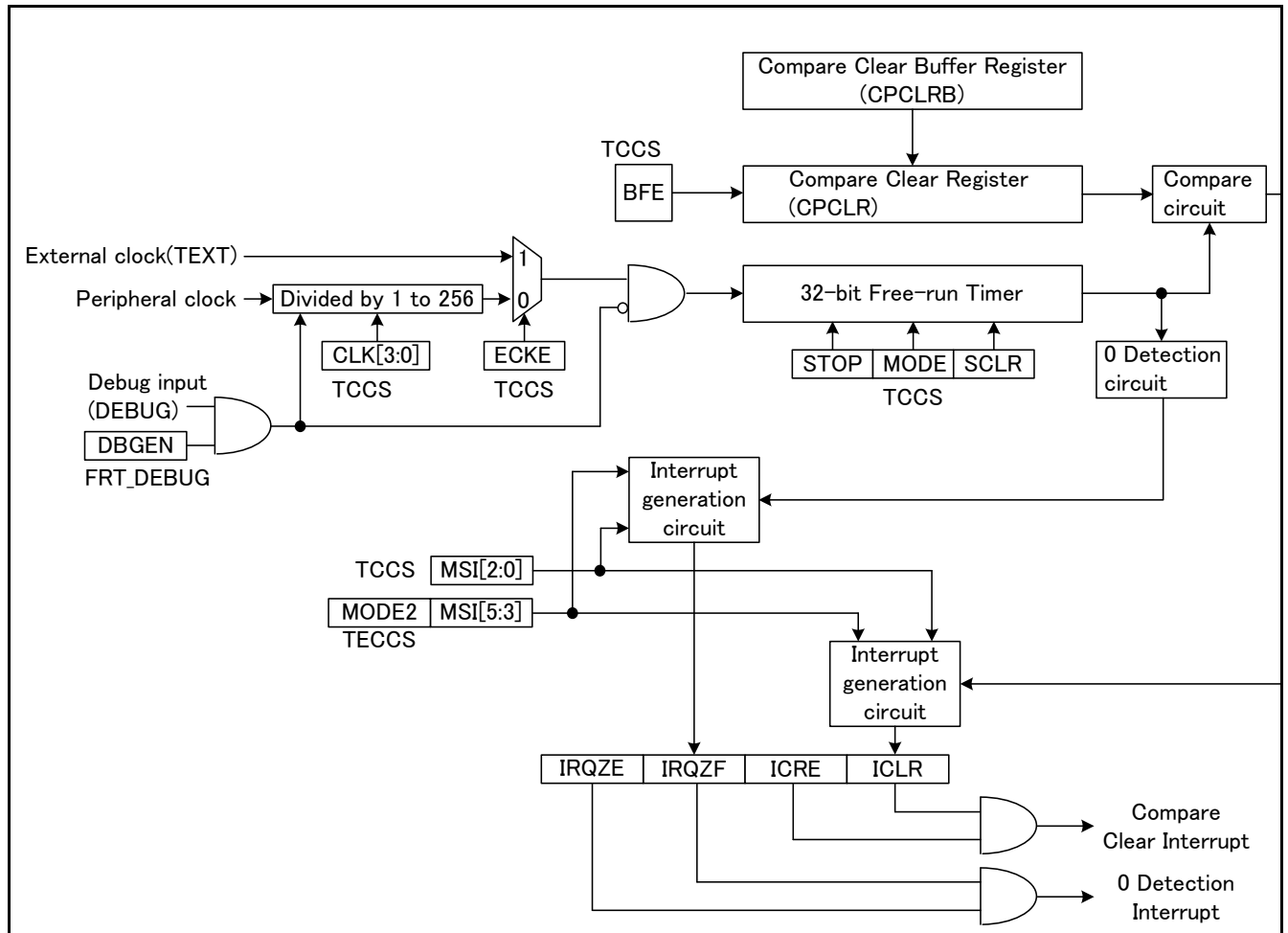
Functions of the 32-Bit Free-Run Timer

- The 32-bit Free-run Timer is composed of the 32-bit up/down counter, Timer State Control Register, 32-bit Compare Clear Register, 32-bit Compare Clear Buffer Register, and Prescaler.
- The 9 types of count clocks (ϕ , $\phi/2$, $\phi/4$, $\phi/8$, $\phi/16$, $\phi/32$, $\phi/64$, $\phi/128$, and $\phi/256$) (ϕ : peripheral clock) can be selected.
- A Compare Clear Interrupt is generated when the values of the Compare Clear Register and the 32-bit counter are compared and their values match. A 0 detection interrupt is generated when the 32-bit counter detects the count value 0x00000000.
- The Compare Clear Register has a buffer register (the data written to this buffer register is transferred to the Compare Clear Register). When the 32-bit counter is stopped, the data is transferred as soon as data is written to the buffer. When the 32-bit counter is operating, data is transferred from the buffer upon detecting the count value 0x00000000.
- The count value is reset to 0x00000000 when a hardware reset occurs, clears the timer, or the value of the Compare Clear Register and the count value match in up count mode.
- The output value of the 32-bit Free-run Timer can be used as a clock count of the 32-bit Output Compare and the 32-bit Input Capture.

2. Block Diagram of the 32-Bit Free-Run Timer

This section shows a block diagram of 32-bit Free-run Timer

Figure 2-1 Block Diagram of 32-Bit Free-Run Timer



3. Operation of the 32-Bit Free-Run Timer

This section describes the operation of the 32-bit Free-run Timer.

Operation of the 32-Bit Free-Run Timer

The 32-bit Free-run Timer starts counting from the value set in the Timer Data Register (TCDT) after the timer is set to enabled (the Timer Enable bit(STOP) in the Timer State Control Register (TCCS)). When the 32-bit Output Compare and the 32-bit Input Capture are connected to the 32-bit Free-run Timer, then the timer count value is used as base time of the 32-bit Output Compare and the 32-bit Input Capture.

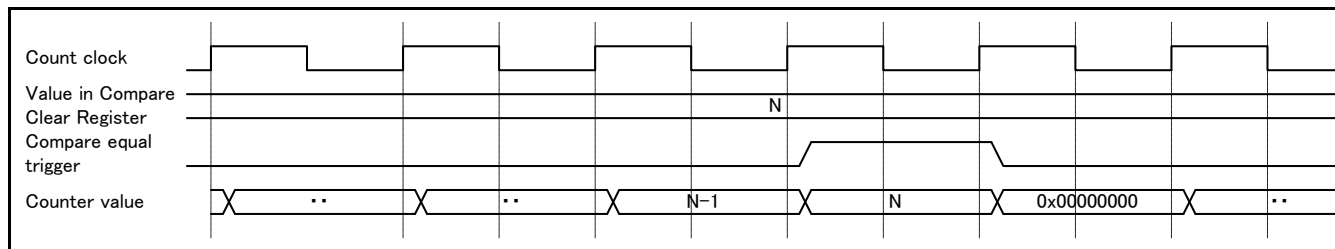
Counter Clear

The count value of the 32-bit Free-run Timer is cleared to 0x00000000 when any of the following conditions is met.

- When the count value matches the value in the Compare Clear Register (CPCLR) in the up count mode (Timer Count Mode bit(MODE) in the Timer State Control Register (TCCS) ="0")
- When "1" is written to the Timer Clear bit (SCLR) in the Timer State Control Register (TCCS) while the 32-bit Free-run Timer is operating (Timer Enable bit(STOP) in the Timer State Control Register (TCCS) ="0")
- When 0x00000000 is written to the Timer Data Register (TCDT) while the 32-bit Free-run Timer is stopped (the Timer Enable bit(STOP) in the Timer State Control Register (TCCS) ="1")
- When the hardware is reset. Upon reset, the counter is cleared immediately.

When "1" is written to the Timer Clear bit (SCLR) in the Timer State Control Register (TCCS) or when the count value matches the value in the Compare Clear Register (CPCLR), the counter is cleared synchronously with the count timing.

Figure 3-1 Clear Timing of 32-Bit Free-Run Timer



Note:

- The count value of the 32-bit Free-run Timer is not cleared if "1" is written to the Timer Clear bit (SCLR) in the Timer State Control Register (TCCS) while the timer is stopped.

Timer Mode

Either of the following modes can be selected for the 32-bit Free-run Timer.

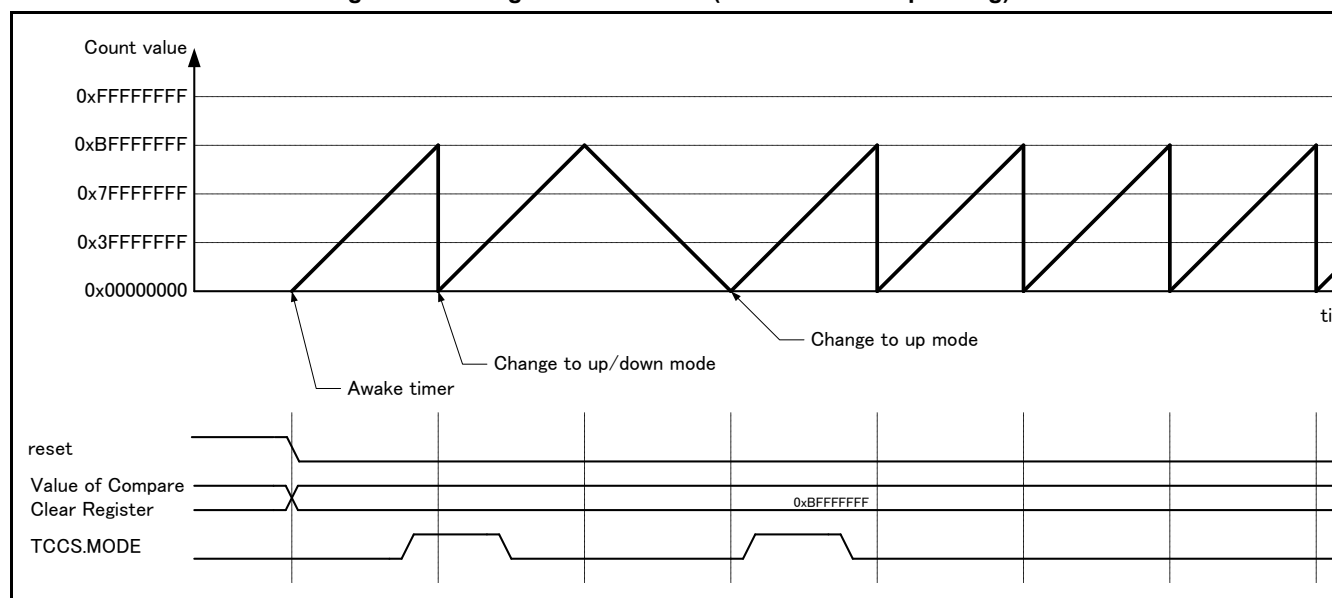
- Up count mode (the Timer Count Mode bit(MODE) in the Timer State Control Register (TCCS) ="0")
- Up/down count mode (the Timer Count Mode bit(MODE) in the Timer State Control Register (TCCS) ="1")

In the up count mode, the counter starts counting from the Timer Data Register (TCDT) that is set in advance. The counter continues to count up until the count value matches the value in the Compare Clear Register (CPCLR). Then, the counter is cleared to 0x00000000 and starts counting up again.

In the up/down count mode, the counter starts counting from the Timer Data Register (TCDT) that is set in advance. The counter continues to count up until the count value matches the value in the Compare Clear Register (CPCLR). Then, the counter changes the counting direction from up count to down count. It continues to count down until the counter value reaches 0x00000000 and starts counting up again.

A value can be written to the Timer Count Mode bit (MODE) in the Timer State Control Register (TCCS) at any time, even when the timer is operating or stopped. The value written to this bit during the timer operation is stored in a buffer. The count mode changes when the count value becomes 0x00000000.

Figure 3-2 Change of Timer Mode (While Timer Is Operating)



Compare Clear Buffer

The Compare Clear Register (CPCLR) has a buffer function that can be enabled or disabled. When the buffer function is enabled (the Compare Clear Buffer Enable bit(BFE) in the Timer State Control Register (TCCS) = "1"), the data written to the Compare Clear Buffer Register (CPCLRB) is transferred to the Compare Clear Register (CPCLR) upon detecting the count value 0x00000000. When the buffer function is disabled (the Compare Clear Buffer Enable bit(BFE) in the Timer State Control Register (TCCS) = "0"), the data can be directly written to the Compare Clear Register (CPCLR).

Figure 3-3 Up Count Mode Operation When Compare Clear Buffer Is Disabled (the Compare Clear Buffer Enable Bit(BFE) of Timer State Control Register (TCCS) ="0")

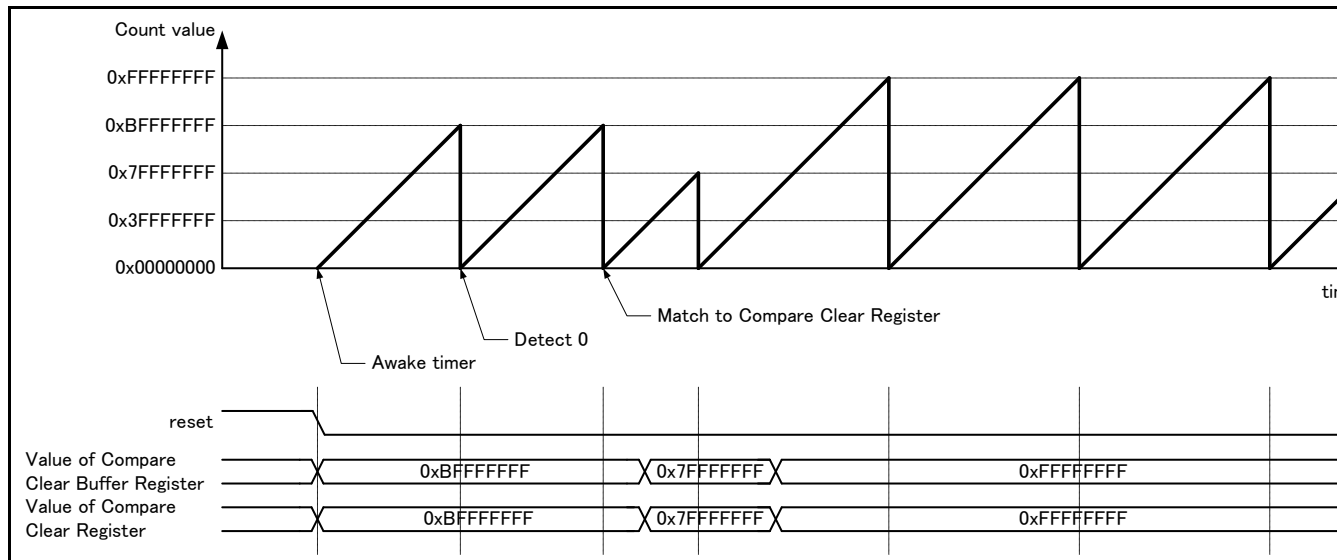


Figure 3-4 Up Count Mode Operation When Compare Clear Buffer Is Enabled (the Compare Clear Buffer Enable Bit(BFE) of Timer State Control Register (TCCS) ="1")

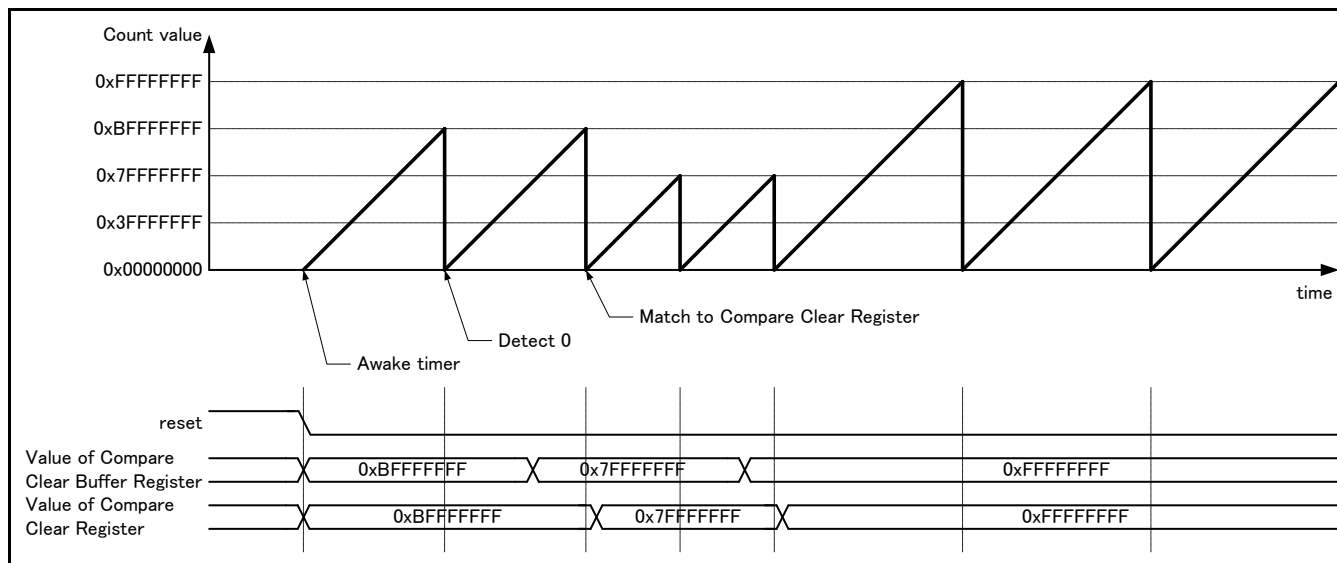
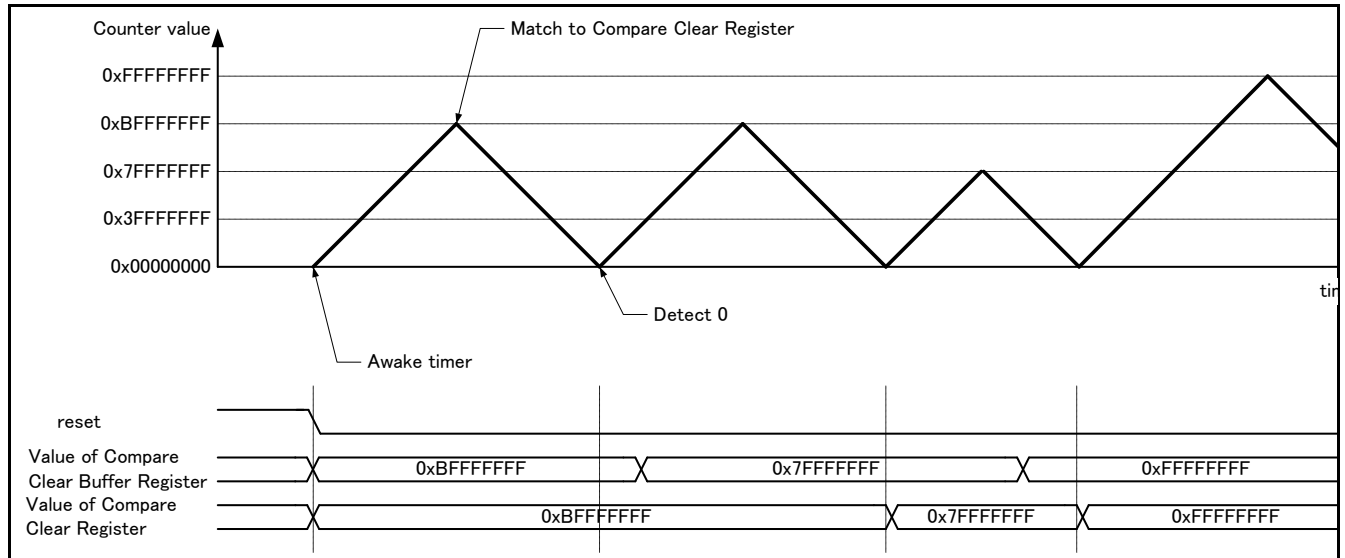


Figure 3-5 Up/Down Count Mode Operation When Compare Clear Buffer Is Enabled (the Compare Clear Buffer Enable Bit(BFE) of Timer State Control Register (TCCS) ="1")



Timer Interrupt

The 32-bit Free-run Timer can generate the following 2 interrupts.

- Compare Clear Interrupt
- 0 Detection Interrupt

The Compare Clear Interrupt is generated when the count value matches the value in the Compare Clear Register (CPCLR). The 0 detection interrupt is generated when the count value reaches 0x00000000.

For Zero Detection and Compare Clear Detection, detection begins when counting is enabled on the 32-bit Free-run Timer and the count value is updated from the current value to the next value.

Note:

- The 0 detection interrupt is not generated when the timer is cleared (the Timer Clear bit(SCLR) in the Timer State Control Register (TCCS) ="1").

Figure 3-6 Interrupt Generated in Up Count Mode (the Timer Count Mode Bit(MODE) in the Timer State Control Register (TCCS) ="0")

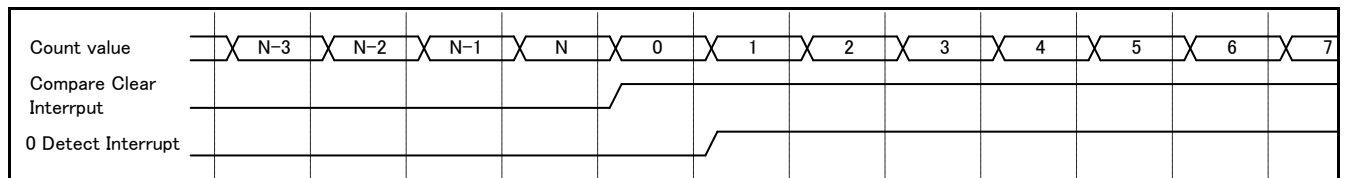
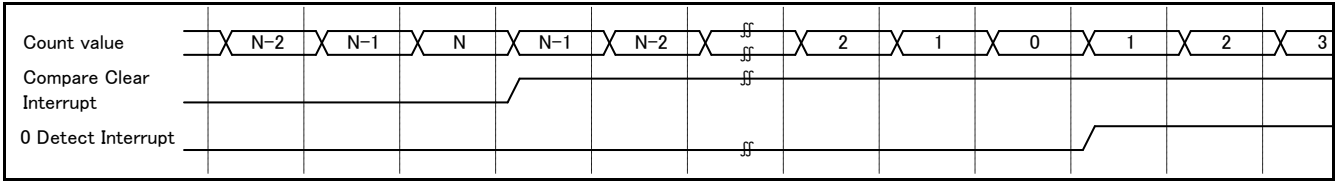


Figure 3-7 Interrupt Generated in Up/Down Count Mode (the Timer Count Mode Bit(MODE) in the Timer State Control Register (TCCS) ="1")



Interrupt Mask Function

Either the 0 detection interrupt or the Compare Clear Interrupt, or both interrupts can be masked.

The following describes the case when either interrupt is masked.

- An interrupt request flag can be masked by setting the Interrupt Mask Selection bits (MSI[2:0]) in the Timer State Control Register (TCCS). The Interrupt Mask Selection bits (MSI[2:0]) in the Timer State Control Register (TCCS) are the 3-bit reload down register that reloads the value when the mask count value reaches "000".
The mask count value can also be loaded by directly writing data to the Interrupt Mask Selection bits (MSI[2:0]) in the Timer State Control Register (TCCS). The number of mask counts is the value set in the Interrupt Mask Selection bits (MSI[2:0]) in the Timer State Control Register (TCCS). An interrupt request flag is not masked when the mask count value (setting in the Interrupt Mask Selection bits (MSI[2:0]) in the Timer State Control Register (TCCS)) becomes "000".
- The mask control of an interrupt request varies depending on the count mode (the Timer Count Mode bit(MODE) in the Timer State Control Register (TCCS)). In the up count mode (Timer Count Mode bit(MODE) in the Timer State Control Register (TCCS) = "0"), only the Compare Clear Interrupt Request Flag can be masked and the 0 detection interrupt is generated every time a timer counter value of 0 is detected. In the up/down count mode (the Timer Count Mode bit(MODE) in the Timer State Control Register (TCCS) = "1"), only the 0 Detection Interrupt Flag (IRQZF) in the Timer State Control Register (TCCS) can be masked.

The following describes the case when both interrupt requests are masked.

- Both interrupts can be masked only when the 32-bit Free-run Timer is in the up/down count mode (the Timer Count Mode bit(MODE) in the Timer State Control Register (TCCS) = "1") and when the Timer Extended State Control Register (TECCS) is set to the Interrupt Mask Mode bit 2(MODE2) in the Timer Extended State Control Register (TECCS) = "1" and the Timer State Control Register (TCCS) is set to the Timer Count Mode bit(MODE) in the Timer State Control Register (TCCS) = "1".
- Interrupt Mask Selection bits (MSI[2:0]) in the Timer State Control Register (TCCS) are used to mask the 0 detection interrupt. Compare Clear Interrupt Mask Selection bits (MSI[5:3]) in the Timer Extended State Control Register (TECCS) are used to mask the Compare Clear Interrupt.

Note:

- *The 0 detection interrupt is not generated when the timer is cleared (the Timer Clear bit(SCLR) in the Timer State Control Register (TCCS) = "1").*
- *If Interrupt mask function "by setting TCCS.MSI[2:0] Register" is used, please write TCCS[15:8], TCCSC[15:8] and TCCSS[15:8] after 32bit free-run timer stopped.*

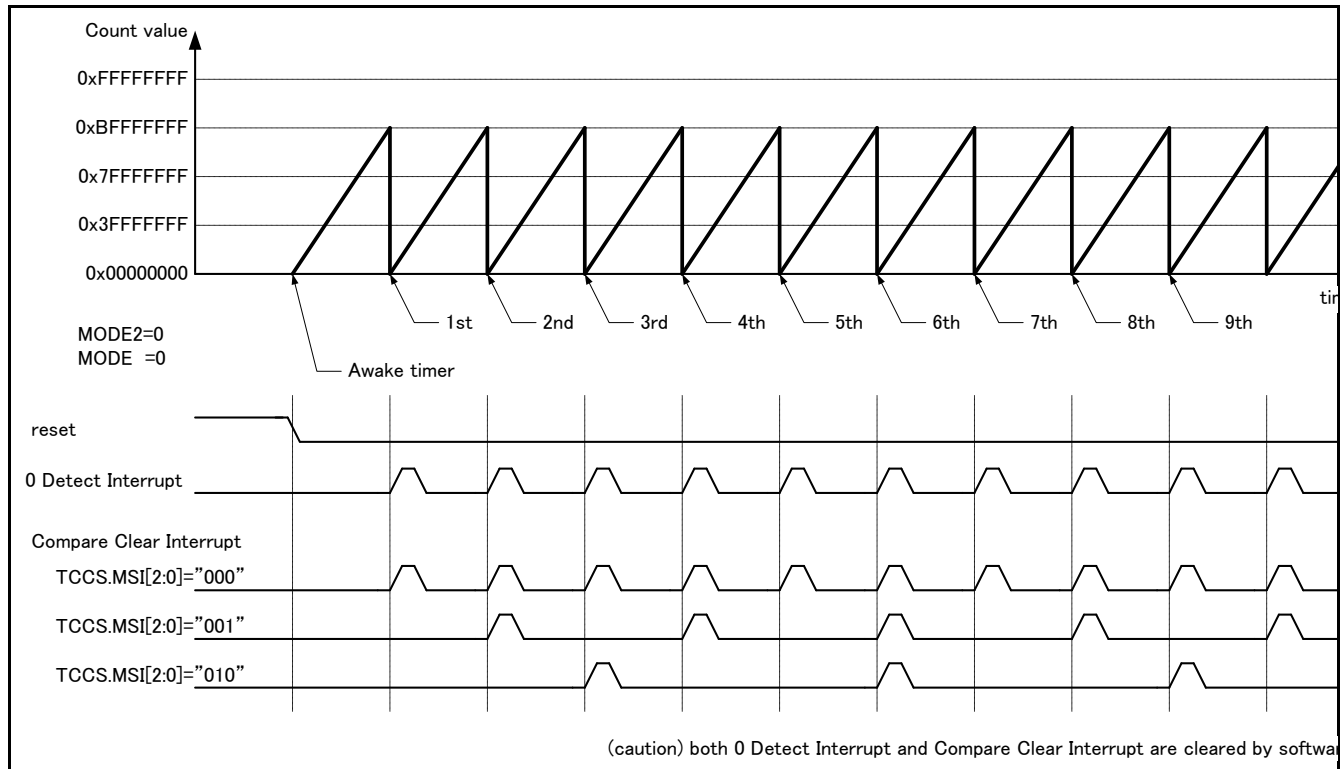
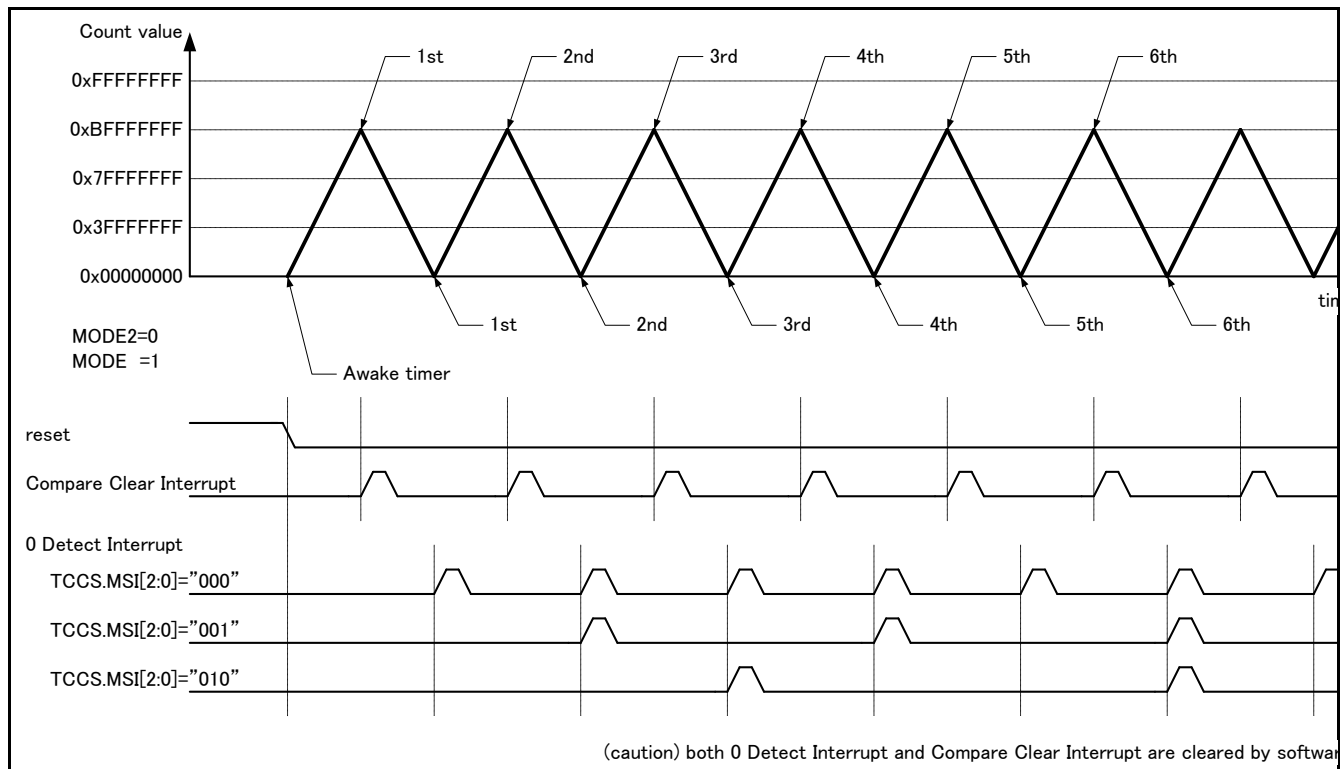
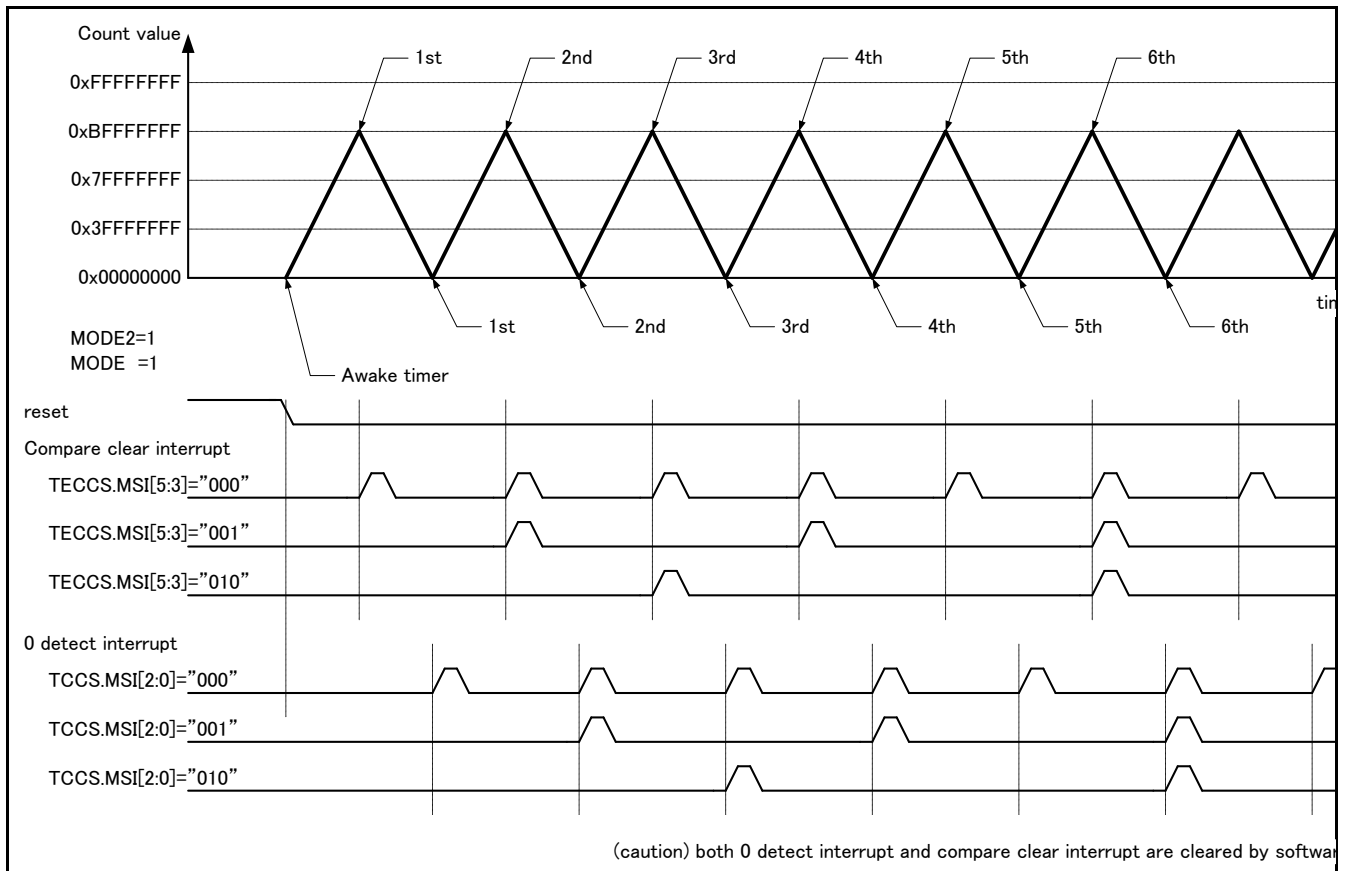
Figure 3-8 Compare Clear Interrupts to Be Masked in Up Count Mode**Figure 3-9 0 Detection Interrupts to Be Masked in Up/Down Count Mode**

Figure 3-10 0 Detection Interrupts and Compare Clear Interrupts to Be Masked in Up/Down Count Mode

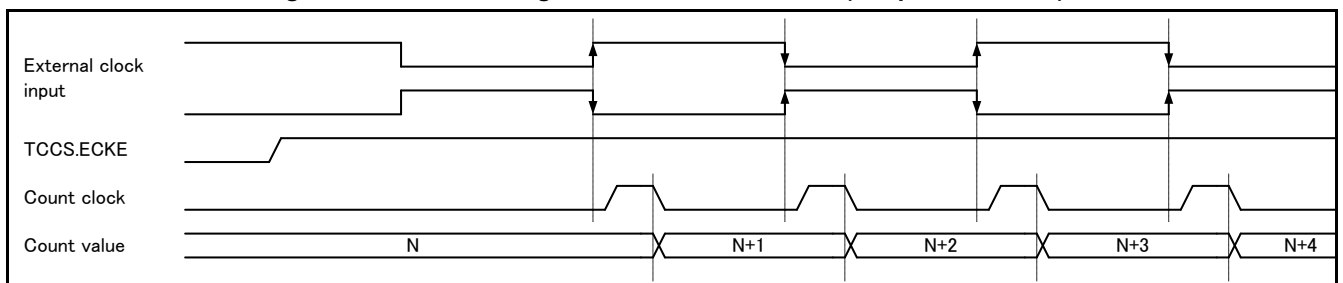


Selected External Count Clock

The 32-bit Free-run Timer counts based on an input clock (peripheral clock or external clock).

If the external clock mode (the Clock Selection bit(ECKE) in the Timer State Control Register (TCCS) ="1") is selected, the 32-bit Free-run Timer starts counting at a rising edge of the external input when the initial value of the external clock input (TEXT) is "H". After that, the 32-bit Free-run Timer counts at both edges. When the initial value of the external input is "L", the 32-bit Free-run Timer starts counting at a falling edge of the external input. After that, the 32-bit Free-run Timer counts up at both edges.

Figure 3-11 Count Timing of 32-Bit Free-Run Timer (in Up Count Mode)



Note:

- When the external clock input is used, the timer counts at both edges of the external clock.

3.1. Interrupts of the 32-Bit Free-Run Timer

There are the 2 types of interrupts as the interrupts of the 32-bit Free-run Timer: Compare Clear Interrupt and 0 Detection Interrupt.

32-Bit Free-Run Timer Interrupt

Table 3-1 shows the interrupt control bits and the interrupt factor of the 32-bit Free-run Timer.

Table 3-1 Interrupt Control Bits and Interrupt Factor of 32-Bit Free-Run Timer

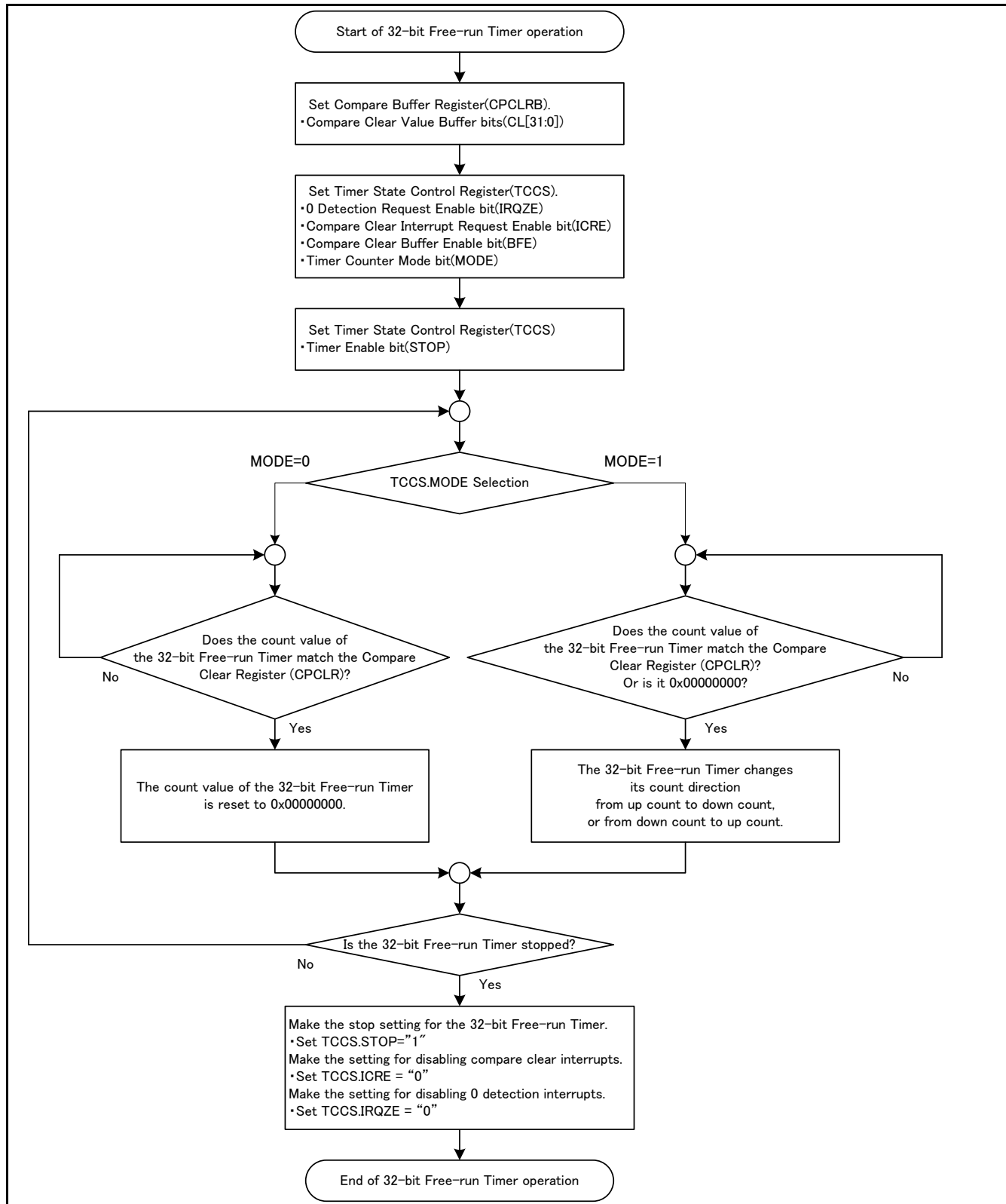
	32-Bit Free-Run Timer	
	Compare Clear	0 Detection
Interrupt request flag	Compare Clear Interrupt Flag (ICLR) in the Timer State Control Register (TCCS)	0 Detection Interrupt Flag (IRQZF) in the Timer State Control Register (TCCS)
Interrupt request enable bit	Compare Clear Interrupt request enable bit (ICRE) in the Timer State Control Register (TCCS)	0 detection interrupt request enable bit (IRQZE) in the Timer State Control Register (TCCS)
Interrupt Factor	The value of the 32-bit Free-run Timer matches the value of the Compare Clear Register (CPCLR).	The 32-bit Free-run Timer value becomes 0x00000000.

"1" is set to the Compare Clear Interrupt Flag (ICLR) in the Timer State Control Register (TCCS) when the value of the 32-bit Free-run Timer matches the value of the Compare Clear Register (CPCLR). When the interrupt request is set to enabled (the Compare Clear Interrupt Request Enable bit(ICRE) in the Timer State Control Register (TCCS) ="1") in this state, then the interrupt request is generated..

"1" is set to the 0 Detection Interrupt Flag (IRQZF) in the Timer State Control Register (TCCS) when the value of the 32-bit Free-run Timer becomes 0x00000000. When the interrupt request is set to enabled (the 0 Detection Request Enable bit(IRQZE) in the Timer State Control Register (TCCS) ="1") in this state, then the interrupt request is generated..

3.2. Setting Procedure Example of the 32-Bit Free-Run Timer

This section provides a setting procedure example of the 32-bit Free-run Timer.

Figure 3-12 Setting Procedure Example of 32-Bit Free-Run Timer Operation

3.3. Debug Mode

If it goes into a debug mode, operation of the 32-bit Free-run Timer can be stopped and debugged.

If all the following conditions are satisfied, it will go into the debug mode.

- The Debug Enable bit (DBGEN) in the Free-run Timer Debug Register (FRT_DEBUG) is "1."
- The debug input (DEBUG) is active.

It becomes the following operation when it goes into the debug mode.

- The prescaler stop. The state of prescaler is kept.
- The 32-bit Free-run Timer stop. Timer value and timer output value are kept.

It becomes the following operation when it restores from the debug mode.

- The prescaler is resumed from the stopped value.
- The 32-bit Free-run Timer is resumed from the stopped value.

Note:

- *Register access is possible in the debug mode.*

4. Registers of the 32-Bit Free-Run Timer

This section provides the register list of the 32-bit Free-run Timer.

Table 4-1 Register Map

Common Peripheral #0 Group (Channel No.:0, 1, 2, 3, 4, 5, 8, 9, 10, 11, 12 and 13)

Offset	Address offset value / Register name				Block name
	+3	+2	+1	+0	
0000_0000	FRTxx_CPCLRB/FRTxx_CPCLR 11111111_11111111_11111111_11111111				Common Peripheral #0
0000_0004	FRTxx_TCDT 00000000_00000000_00000000_00000000				
0000_0008	FRTxx_TCCS 11111111_11111111_00000000_01000000				
0000_000C	FRTxx_TECCS 11111111_11111111_00000000_11111111				
0000_0010	FRTxx_TCCSC 00000000_00000000_00000000_00000000				
0000_0014	FRTxx_TCCSS 00000000_00000000_00000000_00000000				
0000_0018	Reserved 00000000_00000000		FRTxx_DEBUG 00000000_00000000		
0000_001C 0000_03FC	-				

Note:

- xx is the channel number (0 to 5, 8 to 13).

Registers of the 32-Bit Free-Run Timer

Table 4-2 Register List of 32-Bit Free-Run Timer

Abbreviated Register Name	Register Name	Reference
CPCLRB/CPCLR	Compare Clear Buffer Register, Compare Clear Register	4.1
TCDT	Timer Data Register	4.2
TCCS	Timer State Control Register	4.3
TECCS	Timer Extended State Control Register	4.4
TCCSC	Timer State Control Clear Register	4.5
TCCSS	Timer State Control Set Register	4.6
FRT_DEBUG	Free-run Timer Debug Register	4.7

4.1. Compare Clear Buffer Register (CPCLRB)/Compare Clear Register (CPCLR)

The Compare Clear Buffer Register (CPCLRB) is the buffer register of the Compare Clear Register (CPCLR). Both registers are located in the same address.

Compare Clear Buffer Register (CPCLRB)

bit	31	30	29	28	27	26	25	24
Field	CL[31:24]							
R/W Attribute	W							
Protection Attribute	-							
Initial Value	11111111							

bit	23	22	21	20	19	18	17	16
Field	CL[23:16]							
R/W Attribute	W							
Protection Attribute	-							
Initial Value	11111111							

bit	15	14	13	12	11	10	9	8
Field	CL[15:8]							
R/W Attribute	W							
Protection Attribute	-							
Initial Value	11111111							

bit	7	6	5	4	3	2	1	0
Field	CL[7:0]							
R/W Attribute	W							
Protection Attribute	-							
Initial Value	11111111							

[bit31:0] CL[31:0]: Compare Clear Value Buffer Bits

The Compare Clear Buffer Register (CPCLRB) is a buffer register that is located in the same address as the Compare Clear Register (CPCLR).

The value of the Compare Clear Buffer Register (CPCLRB) is immediately transferred to the Compare Clear Register (CPCLR) when the buffer function is set to disabled (the Compare Clear Buffer Enable bit(BFE) in the Timer State Control Register (TCCS) = "0") or the 32-bit Free-run Timer is stopped.

The value of the Compare Clear Buffer Register (CPCLRB) is transferred to the Compare Clear Register (CPCLR) when the buffer function is set to enabled (the Compare Clear Buffer Enable bit(BFE) in the Timer State Control Register (TCCS) = "1") and 0 is detected as the count value of the 32-bit Free-run Timer.

Notes:

- Do not set 0x00000000 in the Compare Clear Buffer Register (CPCLRB).
- For access to this register, use 32-bit access instructions.

Compare Clear Register (CPCLR)

bit	31	30	29	28	27	26	25	24
Field	CL[31:24]							
R/W Attribute	R							
Protection Attribute	-							
Initial Value	11111111							

bit	23	22	21	20	19	18	17	16
Field	CL[23:16]							
R/W Attribute	R							
Protection Attribute	-							
Initial Value	11111111							

bit	15	14	13	12	11	10	9	8
Field	CL[15:8]							
R/W Attribute	R							
Protection Attribute	-							
Initial Value	11111111							

bit	7	6	5	4	3	2	1	0
Field	CL[7:0]							
R/W Attribute	R							
Protection Attribute	-							
Initial Value	11111111							

[bit31:0] CL[31:0]: Compare Clear Value Bits

The Compare Clear Register (CPCLR) is used to compare the count value of the 32-bit Free-run Timer.

In the up count mode (the Timer Count Mode bit(MODE) in the Timer State Control Register (TCCS) ="0"), the count value of the 32-bit Free-run Timer is reset to 0x00000000 when the value of this register matches the count value of the 32-bit Free-run Timer.

In the up/down count mode (the Timer Count Mode bit(MODE) in the Timer State Control Register (TCCS) ="1"), the 32-bit Free-run Timer changes the counting direction from up count to down count when the value of the Compare Clear Register (CPCLR) matches the count value of the 32-bit Free-run Timer. The counting direction is changed from down count to up count when 0 is detected.

Notes:

- For access to this register, use 32-bit access instructions.

4.2. Timer Data Register (TCDT)

The Timer Data Register (TCDT) reads the count value of the 32-bit Free-run Timer. This register can also be used to set the count value of the 32-bit Free-run Timer.

bit	31	30	29	28	27	26	25	24
Field	T[31:24]							
R/W Attribute	R,W							
Protection Attribute	-							
Initial Value	00000000							

bit	23	22	21	20	19	18	17	16
Field	T[23:16]							
R/W Attribute	R,W							
Protection Attribute	-							
Initial Value	00000000							

bit	15	14	13	12	11	10	9	8
Field	T[15:8]							
R/W Attribute	R,W							
Protection Attribute	-							
Initial Value	00000000							

bit	7	6	5	4	3	2	1	0
Field	T[7:0]							
R/W Attribute	R,W							
Protection Attribute	-							
Initial Value	00000000							

[bit31:0] T[31:0]: Timer Data Value Bits

The Timer Data Register (TCDT) is used to read the count value of the 32-bit Free-run Timer.

The count value can be set by writing a value to this register. However, a value needs to be written while the 32-bit Free-run Timer is stopped (the Timer Enable bit(STOP) in the Timer State Control Register (TCCS) ="1").

The counter is cleared to the count value 0x00000000 as soon as any of the following factors occurs.

- Hardware reset. A counter is cleared immediately after being hardware reset.
- The Timer Clear bit (SCLR) in the Timer State Control Register (TCCS) is set to "1" while the 32-bit Free-run Timer is operating (the Timer Enable bit(STOP) in the Timer State Control Register (TCCS) ="0").
- The value of the Compare Clear Register (CPCLR) matches the timer count value in the up count mode (the Timer Count Mode bit(MODE) in the Timer State Control Register (TCCS) ="0").
- The Timer Data Register (TCDT) is set to 0x00000000 while the 32-bit Free-run Timer is stopped (the Timer Enable bit(STOP) in the Timer State Control Register (TCCS) ="1").

If the Timer Clear bit (SCLR) in the Timer State Control Register (TCCS) is set to "1" or the value of the Compare Clear Register (CPCLR) matches the timer count value, the counter is cleared in synchronization with the count timing.

Notes:

- *The 32-bit Free-run Timer is not cleared to 0x00000000 even if the Timer Clear bit (SCLR) in the Timer State Control Register (TCCS) is set to "1" while the 32-bit Free-run Timer is stopped (the Timer Enable bit(STOP) in the Timer State Control Register (TCCS) ="1").*
- *For access to this register, use 32-bit access instructions.*

4.3. Timer State Control Register (TCCS)

The Timer State Control Register (TCCS) is a register that is used to control the operation of the 32-bit Free-run Timer.

For details on writing to this register, see "5.Precautions for Using This Device."

bit	31	30	29	28	27	26	25	24
Field	Reserved							
R/W Attribute	RX,WX							
Protection Attribute	-							
Initial Value	XXXXXXXX							

bit	23	22	21	20	19	18	17	16
Field	Reserved							
R/W Attribute	RX,WX							
Protection Attribute	-							
Initial Value	XXXXXXXX							

bit	15	14	13	12	11	10	9	8
Field	ECKE	IRQZF	IRQZE	MSI[2:0]			ICLR	ICRE
R/W Attribute	R/W	R,WX	R/W	R,W			R,WX	R/W
Protection Attribute	-							
Initial Value	0	0	0	000			0	0

bit	7	6	5	4	3	2	1	0
Field	BFE	STOP	MODE	SCLR	CLK[3:0]			
R/W Attribute	R/W	R/W	R/W	R0,W	R/W			
Protection Attribute	-							
Initial Value	0	1	0	0	0000			

[bit31:16] Reserved Bits

Reading these bits returns an undefined value.

Writing data to these bits has no effect on the operation.

[bit15] ECKE: Clock Selection Bit

This bit is used to select a bus clock or an external clock as the count clock of the 32-bit Free-run Timer.

When this bit is set to "0", a bus clock is selected.

To select the count clock frequency, the Clock Frequency Selection bits (CLK[3:0]) must also be selected.

When this bit is set to "1", an external clock is selected and the clock is input from the external clock input (TEXT).

This bit is cleared to "0" by writing "1" to the Clock Selection Clear bit(ECKEC) in the Timer State Control Clear Register (TCCSC).

This bit is set to "1" by writing "1" to the Clock Selection Set bit(ECKES) in the Timer State Control Set Register (TCCSS).

Bit	Description
0	Bus clock
1	External clock

Note:

- The count clock is changed immediately when this bit is changed. Therefore, change this bit when the 32-bit Output Compare and the 32-bit Input Capture are stopped if the 32-bit Free-run Timer is connected to them.

[bit14] IRQZF: 0 Detection Interrupt Flag

This flag is set to "1" when the count value of the 32-bit Free-run Timer is 0x00000000.

This flag is a read-only bit. Writing data to this flag has no effect on the operation.

This flag is cleared by writing "1" to the 0 Detection Interrupt Flag Clear (IRQZFC) in the Timer State Control Clear Register (TCCSC).

Bit	Description
0	0 is not detected.
1	0 is detected.

Notes:

- This bit is not set to "1" when the timer is cleared ("1" is written to the Timer Clear bit(SCLR)) while the 32-bit Free-run Timer is operating (the Timer Enable bit (STOP)="0").
- In the up/down count mode (the Timer Count Mode bit(MODE) ="1"), this flag is set to "1" when an interrupt that is set by the Interrupt Mask Selection bits (MSI[2:0]) occurs. This flag is not set to "1" when no interrupt occurs.
- In the up count mode (the Timer Count Mode bit(MODE) ="0"), this flag is set to "1" every time 0 is detected regardless of the value of the Interrupt Mask Selection bits (MSI[2:0]).

[bit13] IRQZE: 0 Detection Request Enable Bit

When this bit is set to "1" and the 0 Detection Interrupt Flag (IRQZF) is set to "1", an interrupt request is generated.

This bit is cleared to "0" by writing "1" to the 0 Detection Request Enable Clear bit (IRQZEC) in the Timer State Control Clear Register (TCCSC).

This bit is set to "1" by writing "1" to the 0 Detection Request Enable Set bit (IRQZES) in the Timer State Control Set Register (TCCSS).

Bit	Description
0	Disable interrupt requests.
1	Enable interrupt requests.

[bit12:10] MSI[2:0]: Interrupt Mask Selection Bits

For the Interrupt Mask Mode bit 2(MODE2) in the Timer Extended State Control Register (TECCS) ="0"

- In the up count mode (the Timer Count Mode bit(MODE)="0"), these bits are used to set the number of times to mask the Compare Clear Interrupt flag. In the up/down count mode bit (the Timer Count Mode bit(MODE) ="1"), these bits are used to set the number of times to mask the 0 detection interrupt flag.
- When these bits are set to "000", the interrupt flags are not masked.

For the Interrupt Mask Mode bit 2(MODE2) in the Timer Extended State Control Register (TECCS) ="1"

- In the up/down count mode (the Timer Count Mode bit(MODE) ="1"), these bits are used to set the number of times to mask the 0 detection interrupt flag.
- In the up count mode (the Timer Count Mode bit(MODE) ="0"), it is prohibited to use these bits to make this setting.

Bit	Description
MSI[2:0]	
000	Generate an interrupt flag at the first match occurrence.
001	Generate an interrupt flag at the second match occurrence.
010	Generate an interrupt flag at the third match occurrence.
011	Generate an interrupt flag at the fourth match occurrence.
100	Generate an interrupt flag at the fifth match occurrence.
101	Generate an interrupt flag at the sixth match occurrence.
110	Generate an interrupt flag at the seventh match occurrence.
111	Generate an interrupt flag at the eighth match occurrence.

Notes:

- The value read is a mask counter value. The mask counter is a decrement counter.
- The written data is written to the mask register.
- If Interrupt mask function "by setting TCCS.MSI[2:0] Register" is used, please write TCCS[15:8], TCCSC[15:8] and TCCSS[15:8] after 32bit free-run timer stopped.

[bit9] ICLR: Compare Clear Interrupt Flag

This flag is set to "1" when the value of the Compare Clear Register (CPCLR) and the value of the 32-bit Free-run Timer match.

This flag is a read-only bit. Writing data to these bits has no effect on the operation.

This flag is cleared by writing "1" to the Compare Clear Interrupt Flag Clear(ICLRC) in the Timer State Control Clear Register (TCCSC).

Bit	Description
0	0 No compare clear.
1	1 Compare clear match.

Notes:

- In the up count mode (the Timer Count Mode bit(MODE) = "0"), this flag is set to "1" when the interrupt flag set by the Interrupt Mask Selection bits (MSI[2:0]) occurs. This flag is not set to "1" when no interrupt occurs.
- In the up/down count mode (the Timer Count Mode bit(MODE) = "1"), regardless of the value of the Interrupt Mask Selection bits (MSI[2:0]), this flag is set to "1" every time the compare clear occurs.

[bit8] ICRE: Compare Clear Interrupt Request Enable Bit

When this bit is set to "1" and the Compare Clear Interrupt Flag (ICLR) is set to "1", an interrupt request is generated.

This bit is cleared to "0" by writing "1" to the Compare Clear Interrupt Request Enable Clear bit(ICREC) in the Timer State Control Clear Register (TCCSC).

This bit is set to "1" by writing "1" to the Compare Clear Interrupt Request Enable Set bit(ICRES) in the Timer State Control Set Register (TCCSS).

Bit	Description
0	Disable interrupt requests.
1	Enable interrupt requests.

[bit7] BFE: Compare Clear Buffer Enable Bit

This bit is used to enable the Compare Clear Buffer Register (CPCLRB).

When this bit is set to "0":

The Compare Clear Buffer Register (CPCLRB) becomes invalid. Thus, data can be written directly to the Compare Clear Register (CPCLR).

When this bit is set to "1":

The Compare Clear Buffer Register (CPCLRB) becomes valid. The data written and stored in the Compare Clear Buffer Register (CPCLRB) is transferred to the Compare Clear Register (CPCLR) when "0" is detected as the count value of the 32-bit Free-run Timer.

This bit is cleared to "0" by writing "1" to the Compare Clear Buffer Enable Clear bit(BFEC) in the Timer State Control Clear Register (TCCSC).

This bit is set to "1" by writing "1" to the Compare Clear Buffer Enable Set bit(BFES) in the Timer State Control Set Register (TCCSS).

Bit	Description
0	Disable the Compare Clear Buffer.
1	Enable the Compare Clear Buffer.

[bit6] STOP: Timer Enable Bit

This bit is used to stop/start counting of the 32-bit Free-run Timer.

When this bit is set to "0":

The 32-bit Free-run Timer starts counting.

When this bit is set to "1":

The 32-bit Free-run Timer stops counting.

This bit is cleared to "0" by writing "1" to the Timer Enable Clear bit(STOPC) in the Timer State Control Clear Register (TCCSC).

This bit is set to "1" by writing "1" to the Timer Enable Set bit(STOPS) in the Timer State Control Set Register (TCCSS).

Bit	Description
0	Enable counting (start counting).
1	Disable counting (stop counting).

[bit5] MODE: Timer Count Mode Bit

This bit is used to select a count mode of the 32-bit Free-run Timer.

When this bit is set to "0":

The up count mode is selected. The timer continues to count up until the count value matches the value of the Compare Clear Register (CPCLR) and is reset to 0x00000000. After that, it starts counting up again.

When this bit is set to "1":

The up/down count mode is selected. The timer continues to count up until the count value matches the value of the Compare Clear Register (CPCLR). After that, the count direction changes to down count. When the count value reaches 0x00000000, the count direction changes to up count again.

A value can be written to this bit regardless of whether the timer is operating (the Timer Enable bit (STOP) ="0") or stopped (the Timer Enable bit(STOP) ="1"). When the timer is operating, the value written to this bit is stored in a buffer. After that, when the timer value becomes 0x00000000, the count mode is set based on the value stored in the buffer.

This bit is cleared to "0" by writing "1" to the Timer Count Mode Clear bit(MODEC) in the Timer State Control Clear Register (TCCSC).

This bit is set to "1" by writing "1" to the Timer Count Mode Set bit(MODES) in the Timer State Control Set Register (TCCSS).

Bit	Description
0	Up count mode
1	Up/down count mode

[bit4] SCLR: Timer Clear Bit

This bit is used to initialize the 32-bit Free-run Timer.

Initializing the value of the 32-bit Free-run Timer:

The 32-bit Free-run Timer is initialized to 0x00000000 at the next count clock when "1" is written to this bit while the 32-bit Free-run Timer is operating (the Timer Enable bit (STOP) ="0").

The 32-bit Free-run Timer is not initialized if "1" is written to this bit when the 32-bit Free-run Timer is stopped (the Timer Enable bit (STOP) ="1").

Initializing the count direction of the 32-bit Free-run Timer:

If this bit is set to "1" while the 32-bit Free-run Timer is operating (the Timer Enable bit (STOP) = "0"), the 32-bit Free-run Timer is initialized and then starts counting up.

If this bit is set to "1" while the 32-bit Free-run Timer is stopped (the Timer Enable bit (STOP) = "1") and then the 32-bit Free-run Timer is restarted (the Timer Enable bit (STOP) = "0"), the 32-bit Free-run Timer always counts up when starting operation.

Suppose the 32-bit Free-run Timer stops operating (the Timer Enable bit (STOP) = "1") while counting down and this bit is set to "1". After that, even if the 32-bit Free-run Timer resumes operation (the Timer Enable bit (STOP) = "1"), the 32-bit Free-run Timer counts up when starting operation.

This bit is set to "1" by writing "1" to the Timer Clear Set bit(SCLRS) in the Timer State Control Set Register (TCCSS).

The read value is always "0".

Bit	Description	
	During Read Operation	During Write Operation
0	"0" always read	Do not initialize the counter.
1		Initialize the counter to 0x00000000.

Notes:

- The 0 detection interrupt is not generated even if this bit is set to "1".
- The timer is not cleared when "0" is written to this bit before the next count clock after "1" is written to this bit.
- In the up/down count mode, when "0" is written to the Timer Clear bit(SCLR) before updating the timer count after "1" is written to the Timer Clear bit(SCLR) while the timer is counting down, the count value is not updated and the count direction is changed to up count.

[bit3:0] CLK[3:0]: Clock Frequency Selection Bits

These bits are used to select the count clock frequency of the 32-bit Free-run Timer.

The clock frequency is changed immediately upon setting these bits.

CLK[3:0]	Description					
	Count Clock	ϕ = 40 MHz	ϕ = 20 MHz	ϕ = 10 MHz	ϕ = 5 MHz	ϕ = 2.5 MHz
0000	ϕ	25 ns	50 ns	100 ns	200 ns	400 ns
0001	$\phi/2$	50 ns	100 ns	200 ns	400 ns	800 ns
0010	$\phi/4$	100 ns	200 ns	400 ns	800 ns	1.6 μ s
0011	$\phi/8$	200 ns	400 ns	800 ns	1.6 μ s	3.2 μ s
0100	$\phi/16$	400 ns	800 ns	1.6 μ s	3.2 μ s	6.4 μ s
0101	$\phi/32$	800 ns	1.6 μ s	3.2 μ s	6.4 μ s	12.8 μ s
0110	$\phi/64$	1.6 μ s	3.2 μ s	6.4 μ s	12.8 μ s	25.6 μ s
0111	$\phi/128$	3.2 μ s	6.4 μ s	12.8 μ s	25.6 μ s	51.2 μ s
1000	$\phi/256$	6.4 μ s	12.8 μ s	25.6 μ s	51.2 μ s	102.4 μ s
Other settings are prohibited.	-	-	-	-	-	-

ϕ : Bus clock.

4.4. Timer Extended State Control Register (TECCS)

The Timer Extended State Control Register (TECCS) is an extended control register that controls the operation of the 32-bit Free-run Timer.

bit	31	30	29	28	27	26	25	24
Field	Reserved							
R/W Attribute	RX,WX							
Protection Attribute	-							
Initial Value	XXXXXXXX							

Bit	23	22	21	20	19	18	17	16
Field	Reserved							
R/W Attribute	RX,WX							
Protection Attribute	-							
Initial Value	XXXXXXXX							

bit	15	14	13	12	11	10	9	8
Field	Reserved				MODE2	MSI[5:3]		
R/W Attribute	RX,WX				R/W	R,W		
Protection Attribute	-							
Initial Value	XXXX				0	000		

bit	7	6	5	4	3	2	1	0
Field	Reserved							
R/W Attribute	RX,WX							
Protection Attribute	-							
Initial Value	XXXXXXXX							

[bit31:12] Reserved: Reserved Bits

Reading these bits returns an undefined value.

Writing data to these bits has no effect on the operation.

[bit11] MODE2: Interrupt Mask Mode Bit 2

This bit is used to independently mask the 0 detection interrupt and the Compare Clear Interrupt when the 32-bit Free-run Timer is in the up/down count mode (the Timer Count Mode bit(MODE) in the Timer State Control Register (TCCS) ="1").

If "1" is written to this bit when the 32-bit Free-run Timer is in the up/down count mode (the Timer Count Mode bit(MODE) in the Timer State Control Register (TCCS) ="1"), the value set to the Compare Clear Interrupt Mask Selection bits (MSI[5:3]) of this register is enabled and the Compare Clear Interrupt Flag (ICLR) in the Timer State Control Register (TCCS) is masked the specified number of times. The value set to the Interrupt Mask Selection bits (MSI[2:0]) in the Timer State Control Register (TCCS) becomes valid as the number of times to mask the 0 Detection Interrupt Flag (IRQZF) in the Timer State Control Register (TCCS).

Bit		Description
MODE2	MODE*	
0	0	The setting values of Compare Clear Interrupt Mask Selection bits(MSI[5:3]) are invalid.
0	1	The setting values of Compare Clear Interrupt Mask Selection bits(MSI[5:3]) are invalid.
1	0	The setting is prohibited (the operation is not guaranteed).
1	1	The setting values of Compare Clear Interrupt Mask Selection bits(MSI[5:3]) are valid.

* Timer Count Mode bit (MODE) in the Timer State Control Register (TCCS)

Note:

- The operation when "1" is written to this bit is not guaranteed when the 32-bit Free-run Timer is in the up count mode.

[bit10:8] MSI[5:3]: Compare Clear Interrupt Mask Selection Bits

These bits are valid only when the Interrupt Mask Mode bit 2 (MODE2) is "1" and the 32-bit Free-run Timer is in the up/down count mode (the Timer Count Mode bit(MODE) in the Timer State Control Register (TCCS) ="1"). These bits are used to set the number of times to mask the Compare Clear Interrupt Flag (ICLR) in the Timer State Control Register (TCCS).

The number of times to mask the 0 Detection Interrupt Flag (IRQZF) in the Timer State Control Register (TCCS) is set by Interrupt Mask Selection bits(MSI[2:0]) in the Timer State Control Register (TCCS).

The Compare Clear Interrupt Flag (ICLR) in the Timer State Control Register (TCCS) is not masked when these bits are set to "000".

Bit	Description
MSI[5:3]	
000	Generate an interrupt flag at the first match occurrence.
001	Generate an interrupt flag at the second match occurrence.
010	Generate an interrupt flag at the third match occurrence.
011	Generate an interrupt flag at the fourth match occurrence.
100	Generate an interrupt flag at the fifth match occurrence.
101	Generate an interrupt flag at the sixth match occurrence.
110	Generate an interrupt flag at the seventh match occurrence.
111	Generate an interrupt flag at the eighth match occurrence.

Notes:

- The value read is a mask counter value. The mask counter is a decrement counter.
- The written data is written to the mask register.
- While the 32-bit Free-run Timer is operating (the Timer Enable bit (STOP) in the Timer State Control Register (TCCS) ="0"), the value written to the mask register is reloaded to the counter only when the mask counter becomes "000".
- When the 32-bit Free-run Timer is stopped (the Timer Enable bit (STOP) in the Timer State Control Register (TCCS) ="1"), the value written to the mask register is immediately reloaded to the mask counter.

[bit7:0] Reserved: Reserved Bits

Reading these bits returns an undefined value.

Writing data to these bits has no effect on the operation.

4.5. Timer State Control Clear Register (TCCSC)

The Timer State Control Clear Register (TCCSC) is a register that is used to clear bits of the Timer State Control Register (TCCS).

For details on writing to this register, see "5.Precautions for Using This Device."

bit	31	30	29	28	27	26	25	24
Field	Reserved							
R/W Attribute	R0,W0							
Protection Attribute	-							
Initial Value	00000000							

bit	23	22	21	20	19	18	17	16
Field	Reserved							
R/W Attribute	R0,W0							
Protection Attribute	-							
Initial Value	00000000							

bit	15	14	13	12	11	10	9	8
Field	ECKEC	IRQZFC	IRQZEC	Reserved			ICLRC	ICREC
R/W Attribute	R0,W	R0,W	R0,W	R0,W0			R0,W	R0,W
Protection Attribute	-							
Initial Value	0	0	0	0			0	0

bit	7	6	5	4	3	2	1	0
Field	BFEC	STOPC	MODEC	Reserved				
R/W Attribute	R0,W	R0,W	R0,W	R0,W0				
Protection Attribute	-							
Initial Value	0	0	0	00000				

[bit31:16] Reserved: Reserved Bits

Reading these bits returns "0".

Always write "0" to these bits.

[bit15] ECKEC: Clock Selection Clear Bit

It is the bit which sets the Clock Selection bit (ECKE) in the Timer State Control Register (TCCS) to "0".

Bit	Description	
	Writing	Reading
0	No effect.	Always read "0".
1	Set the Clock Selection bit (ECKE) in the Timer State Control Register (TCCS) to "0".	

[bit14] IRQZFC: 0 Detection Interrupt Flag Clear

It is the bit which sets the 0 Detection Interrupt Flag (IRQZF) in the Timer State Control Register (TCCS) to "0".

Bit	Description	
	Writing	Reading
0	No effect.	Always read "0".
1	Set the 0 Detection Interrupt Flag (IRQZF) in the Timer State Control Register (TCCS) to "0".	

[bit13] IRQZEC: 0 Detection Request Enable Clear Bit

It is the bit which sets the 0 Detection Request Enable bit (IRQZE) in the Timer State Control Register (TCCS) to "0".

Bit	Description	
	Writing	Reading
0	No effect.	Always read "0".
1	Set the 0 Detection Request Enable bit (IRQZE) in the Timer State Control Register (TCCS) to "0".	

[bit12:10] Reserved: Reserved Bits

Reading these bits returns "0".

Always write "0" to these bits.

[bit9] ICLRC: Compare Clear Interrupt Flag Clear

It is the bit which sets the Compare Clear Interrupt Flag (ICLR) in the Timer State Control Register (TCCS) to "0".

Bit	Description	
	Writing	Reading
0	No effect.	Always read "0".
1	Set the Compare Clear Interrupt Flag (ICLR) in the Timer State Control Register (TCCS) to "0".	

[bit8] ICREC: Compare Clear Interrupt Request Enable Clear Bit

It is the bit which sets the Compare Clear Interrupt Request Enable bit (ICRE) in the Timer State Control Register (TCCS) to "0".

Bit	Description	
	Writing	Reading
0	No effect.	Always read "0".
1	Set the Compare Clear Interrupt Request Enable bit (ICRE) in the Timer State Control Register (TCCS) to "0".	

[bit7] BFEC: Compare Clear Buffer Enable Clear Bit

It is the bit which sets the Compare Clear Buffer Enable bit (BFE) in the Timer State Control Register (TCCS) to "0".

Bit	Description	
	Writing	Reading
0	No effect.	Always read "0".
1	Set the Compare Clear Buffer Enable bit (BFE) in the Timer State Control Register (TCCS) to "0".	

[bit6] STOPC: Timer Enable Clear Bit

It is the bit which sets the Timer Enable bit (STOP) in the Timer State Control Register (TCCS) to "0".

Bit	Description	
	Writing	Reading
0	No effect.	Always read "0".
1	Set the Timer Enable bit (STOP) in the Timer State Control Register (TCCS) to "0".	

[bit5] MODEC: Timer Count Mode Clear Bit

It is the bit which sets the Timer Count Mode bit (MODE) in the Timer State Control Register (TCCS) to "0".

Bit	Description	
	Writing	Reading
0	No effect.	Always read "0".
1	Set the Timer Count Mode bit (MODE) in the Timer State Control Register (TCCS) to "0".	

[bit4:0] Reserved: Reserved Bits

Reading these bits returns "0".

Always write "0" to these bits.

4.6. Timer State Control Set Register (TCCSS)

The Timer State Control Set Register (TCCSS) is a register that is used to set bits of the Timer State Control Register (TCCS).

For details on writing to this register, see "5.Precautions for Using This Device."

bit	31	30	29	28	27	26	25	24
Field	Reserved							
R/W Attribute	R0,W0							
Protection Attribute	-							
Initial Value	00000000							

bit	23	22	21	20	19	18	17	16
Field	Reserved							
R/W Attribute	R0,W0							
Protection Attribute	-							
Initial Value	00000000							

bit	15	14	13	12	11	10	9	8
Field	ECKES	Reserved	IRQZES	Reserved				ICRES
R/W Attribute	R0,W	R0,W0	R0,W	R0,W0				R0,W
Protection Attribute	-							
Initial Value	0	0	0	0000				0

bit	7	6	5	4	3	2	1	0
Field	BFES	STOPS	MODES	SCLRS	Reserved			
R/W Attribute	R0,W	R0,W	R0,W	R0,W	R0,W0			
Protection Attribute	-							
Initial Value	0	0	0	0	0000			

[bit31:16] Reserved: Reserved Bits

Reading these bits returns "0".

Always write "0" to these bits.

[bit15] ECKES: Clock Selection Set Bit

It is the bit which sets the Clock Selection bit (ECKE) in the Timer State Control Register (TCCS) to "1".

Bit	Description	
	Writing	Reading
0	No effect.	Always read "0".
1	Set the Clock Selection bit (ECKE) in the Timer State Control Register (TCCS) to "1".	

[bit14] Reserved: Reserved Bit

Reading this bit returns "0".

Always write "0" to this bit.

[bit13] IRQZES: 0 Detection Request Enable Set Bit

It is the bit which sets the 0 Detection Request Enable bit (IRQZE) in the Timer State Control Register (TCCS) to "1".

Bit	Description	
	Writing	Reading
0	No effect.	Always read "0".
1	Set the 0 Detection Request Enable bit (IRQZE) in the Timer State Control Register (TCCS) to "1".	

[bit12:9] Reserved: Reserved Bits

Reading these bits returns "0".

Always write "0" to these bits.

[bit8] ICRES: Compare Clear Interrupt Request Enable Set Bit

It is the bit which sets the Compare Clear Interrupt Request Enable bit (ICRE) in the Timer State Control Register (TCCS) to "1".

Bit	Description	
	Writing	Reading
0	No effect.	Always read "0".
1	Set the Compare Clear Interrupt Request Enable bit (ICRE) in the Timer State Control Register (TCCS) to "1".	

[bit7] BFES: Compare Clear Buffer Enable Set Bit

It is the bit which sets the Compare Clear Buffer Enable bit (BFE) in the Timer State Control Register (TCCS) to "1".

Bit	Description	
	Writing	Reading
0	No effect.	Always read "0".
1	Set the Compare Clear Buffer Enable bit (BFE) in the Timer State Control Register (TCCS) to "1".	

[bit6] STOPS: Timer Enable Set Bit

It is the bit which sets the Timer Enable bit (STOP) in the Timer State Control Register (TCCS) to "1".

Bit	Description	
	Writing	Reading
0	No effect.	Always read "0".
1	Set the Timer Enable bit (STOP) in the Timer State Control Register (TCCS) to "1".	

[bit5] MODES: Timer Count Mode Set Bit

It is the bit which sets the Timer Count Mode bit (MODE) in the Timer State Control Register (TCCS) to "1".

Bit	Description	
	Writing	Reading
0	No effect.	Always read "0".
1	Set the Timer Count Mode bit (MODE) in the Timer State Control Register (TCCS) to "1".	

[bit4] SCLRS: Timer Clear Set Bit

It is the bit which sets the Timer Clear bit (SCLR) in the Timer State Control Register (TCCS) to "1".

Bit	Description	
	Writing	Reading
0	No effect.	Always read "0".
1	Set the Timer Clear bit (SCLR) in the Timer State Control Register (TCCS) to "1".	

[bit3:0] Reserved: Reserved Bits

Reading these bits returns "0".

Always write "0" to these bits.

4.7. Free-Run Timer Debug Register (FRT_DEBUG)

The Free-run Timer Debug Register (FRT_DEBUG) performs enable/disable setting of debug.

bit	15	14	13	12	11	10	9	8
Field	Reserved							
R/W Attribute	R0,W0							
Protection Attribute	-							
Initial Value	00000000							

bit	7	6	5	4	3	2	1	0
Field	Reserved							DBGEN
R/W Attribute	R0,W0							R/W
Protection Attribute	-							
Initial Value	00000000							0

[bit15:1] Reserved: Reserved Bits

The read value is "0".

If writing to this bit, write "0".

[bit0] DBGEN: Debug Enable Bit

It is the bit which permits stopping operation of a 32-bit Free-run Timer with the debug input (DEBUG).

Bit	Description
0	Disable
1	Enable

5. Precautions for Using This Device

The following shows the notes when using the 32-bit Free-run Timer.

Notes to Observe when Accessing a Register

When Accessing the Compare Clear Register (CPCLR) or the Compare Clear Buffer Register (CPCLRB)

Use 32-bit access instructions to the Compare Clear Register (CPCLR) and the Compare Clear Buffer Register (CPCLRB).

When Accessing the Timer State Control Register (TCCS)

- To clear a specified bit of this register, clear the bit by writing "1" to the applicable bit of the Timer State Control Clear Register (TCCSC).
- To set a specified bit of this register, set the bit by writing "1" to the applicable bit of the Timer State Control Set Register (TCCSS).
- Data can be written directly to this register only when writing to all bits.
- In the normal reading mode, the interrupt mask counter value is read from Interrupt Mask Selection bits(MSI[2:0]) in the Timer State Control Register (TCCS).
- If Interrupt mask function "by setting TCCS.MSI[2:0] Register" is used, please write TCCS[15:8], TCCSC[15:8] and TCCSS[15:8] after 32bit free-run timer.

When Accessing the Timer Extended State Control Register (TECCS)

- In the normal reading mode, the interrupt mask counter value is read from Compare Clear Interrupt Mask Selection bits(MSI[5:3]) in the Timer Extended State Control Register (TECCS).

Notes when Operating the 32-Bit Free-Run Timer

When Setting Using a Program

- When the hardware is reset, the count value becomes 0x00000000, but the 0 Detection Interrupt Flag (IRQZF) in the Timer State Control Register (TCCS) is not set.
- Because the timer mode bit (the Timer Count Mode bit(MODE) in the Timer State Control Register (TCCS)) has a buffer, a specified timer mode is enabled after 0 is detected.
- The Timer Clear bit (SCLR) in the Timer State Control Register (TCCS) ="1" initializes the timer. However, this bit does not generate the 0 detection interrupt.
- The Compare Clear Flag is not set if the timer starts counting when the value of the Compare Clear Register (CPCLR) matches the count value.
- Set any values other than 0x00000000 to the Compare Clear Register (CPCLR). Note that the following operations occur if 0x00000000 is set.
 - When the timer mode bit (the Timer Count Mode bit(MODE) in the Timer State Control Register (TCCS)) is in the up count mode (the Timer Count Mode bit(MODE) in the Timer State Control Register (TCCS) ="0"), the count value is updated to 0x00000000 and fixed to 0x00000000. Then, the 0 Detection Interrupt Flag (IRQZF) in the Timer State Control Register (TCCS) and the Compare Clear Interrupt Flag (ICLR) in the Timer State Control Register (TCCS) are set at every count clock.
 - When the Timer Count Mode bit (MODE) in the Timer State Control Register (TCCS) is in the up/down count mode (Timer Count Mode bit(MODE) in the Timer State Control Register (TCCS) ="1"), the count value is counted up from 0x00000000 to 0xFFFFFFFF, and this up count operation is repeated. The 0 Detection Interrupt Flag (IRQZF) in the Timer State Control Register (TCCS) and the Compare Clear Interrupt Flag (ICLR) in the Timer State Control Register (TCCS) are set to "1" when the count value becomes 0x00000000.

CHAPTER 20: 32-Bit Input Capture



This chapter describes the functions of the 32-bit input capture.

1. Overview of the 32-Bit Input Capture
2. Explanation of 32-Bit Input Capture Operation
3. Registers of the 32-Bit Input Capture
4. Precautions for Using This Device

CODE: ICU-S6J3400-E1

1. Overview of the 32-Bit Input Capture

The 32-bit input capture can measure the input pulse width and external clock cycle based on the value of the 32-bit free-run timer.

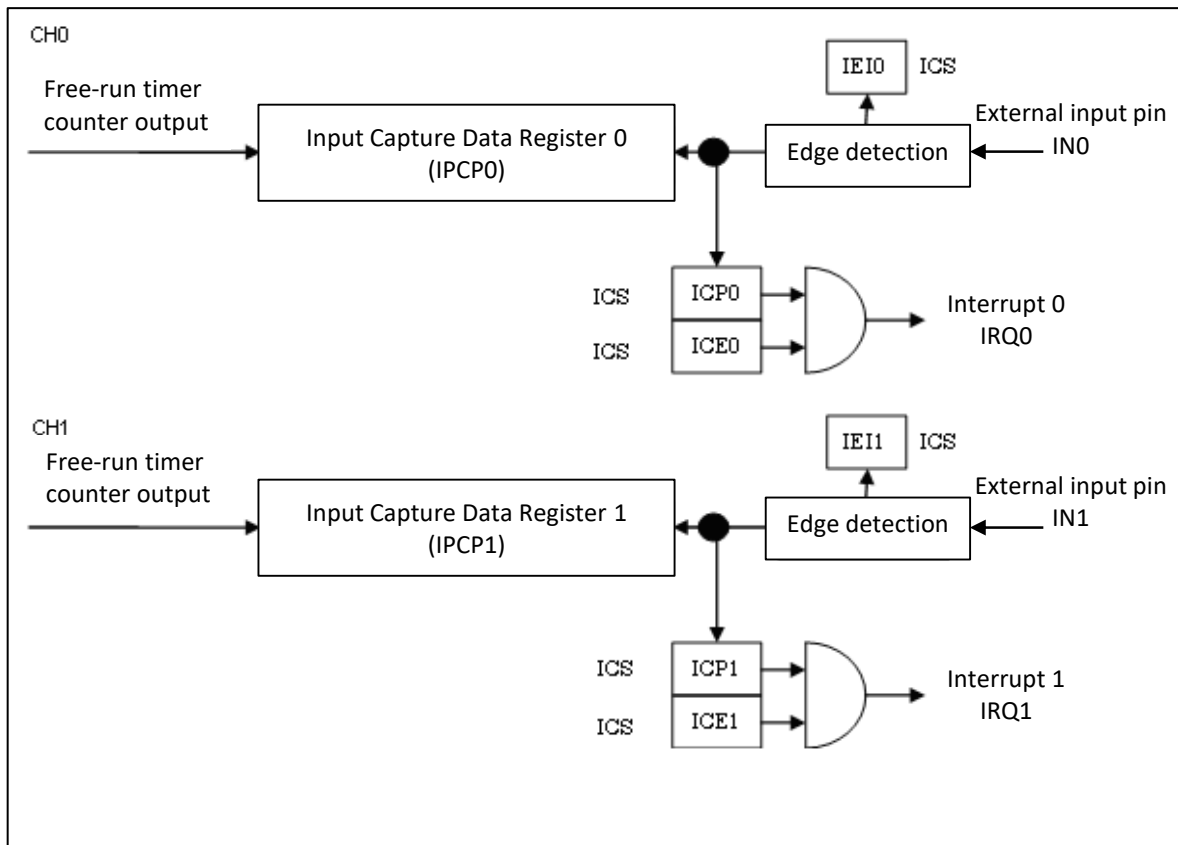
Functions of the 32-Bit Input Capture

- The 32-bit input capture is composed of 2 input captures. Each channel can be operated individually.
- Each input capture is composed of 2 independent external input pins (IN0 and IN1), capture registers that correspond to the pins, and the capture control register. When an edge signal is detected on an external input pin, the value of the free-run timer can be stored in the capture register. At the same time, an interrupt is generated.
- 3 types of trigger edges (rising edge, falling edge, and both edges) of an external input signal can be selected. There is a register that indicates whether a trigger edge is a rising or falling edge.
- An interrupt is generated when a valid edge is detected from an external input signal.

Configuration Diagram of the 32-Bit Input Capture

Figure 1-1 is a configuration diagram of the 32-bit input capture.

Figure 1-1 Configuration Diagram of 32-Bit Input Capture



2. Explanation of 32-Bit Input Capture Operation

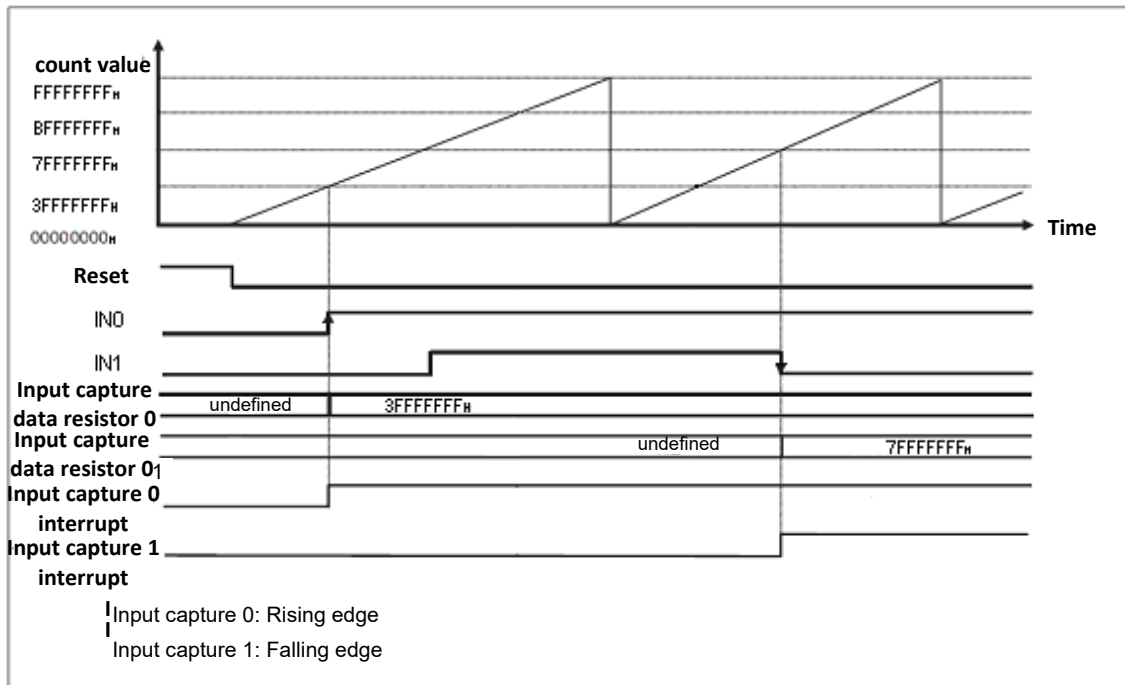
This section provides an overview of 32-bit input capture operation.

Operation of the 32-Bit Input Capture

The 32-bit input capture is used to detect a specified valid edge. When a valid edge is detected, an interrupt flag is set. Then the value of the 32-bit free-run timer is loaded to the input capture register.

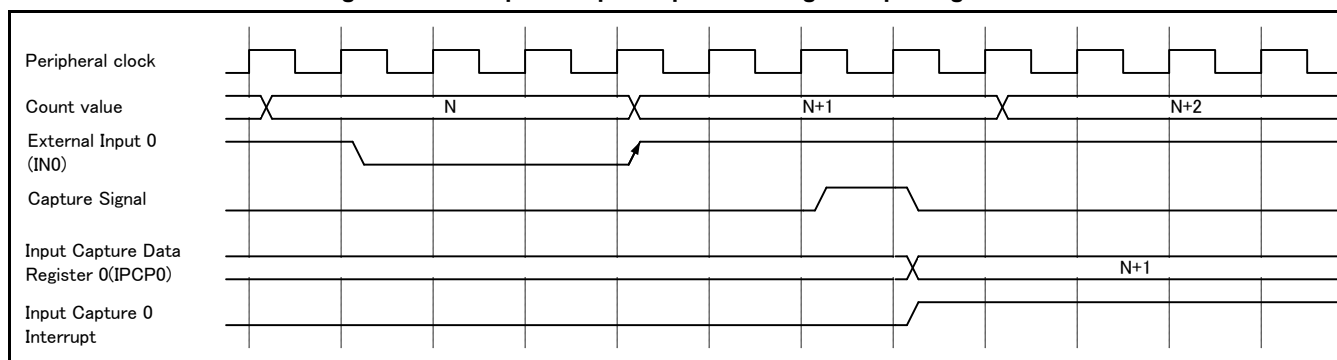
Input Capture Operation

Figure 2-1 Example of Input Capture Timing



Input Capture Input Timing

Figure 2-2 Example of Input Capture Timing for Input Signals



2.1. Interrupt of the 32-Bit Input Capture

As the interrupt of the 32-bit input capture, there is an input capture interrupt triggered by an external input signal.

Input Capture Interrupt

Table 2-1 shows the interrupt control bits and interrupt factor of the input capture.

Table 2-1 Interrupt Control Bits and Interrupt Factor of Input Capture 1, 0

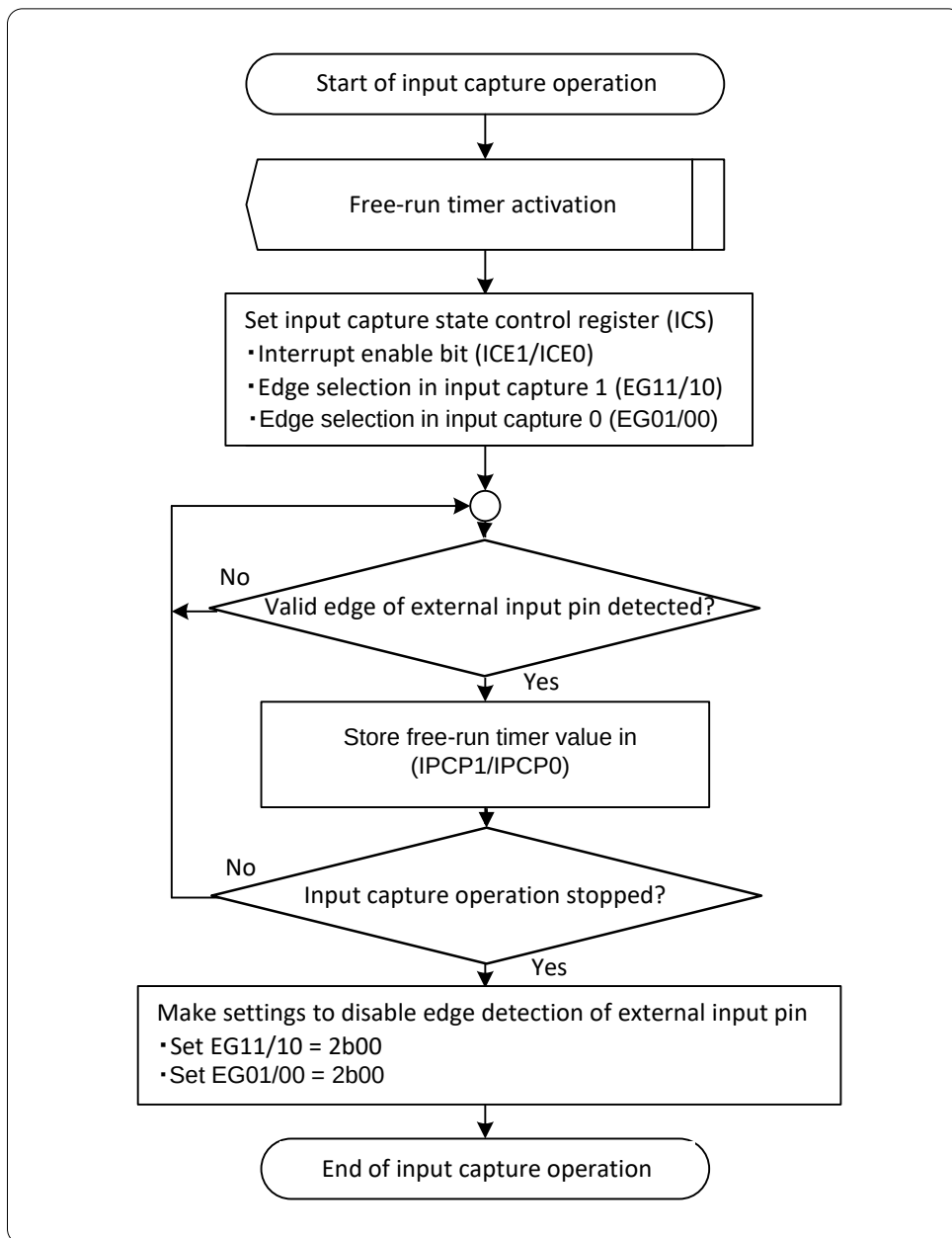
	Input Capture 1, 0
Interrupt Request Flag Bit	The interrupt request flag bits ICP1, 0 (bit7, bit6) in the input capture state control register (ICS)
Interrupt Request Enable Bit	The interrupt request enable bits ICE1, 0 (bit5, bit4) in the input capture state control register (ICS)
Interrupt Factor	A valid edge is detected on the external input pin (IN1, IN0).

For the interrupt capture, when a valid edge is detected on the external input pin (IN1, IN0), the interrupt request flag (ICP1, ICP0: bit7, bit6) in the input capture state control register (ICS) is set to "1". When an interrupt request is set to enabled (ICE1, ICE0: bit5, bit4 = 0b11 in the input capture state control register (ICS)) in this state, then the interrupt request is output to the interrupt controller.

2.2. Setting Procedure Example

This section provides a setting procedure example of the input capture.

Figure 2-3 Procedure Example of Setting Input Capture Operation



3. Registers of the 32-Bit Input Capture

This section provides the register list of the 32-bit input capture.

Table 3-1 Register Map

Common Peripheral Group #0 (Channel No.:0, 1, 2, 8, 9, and 10)

Offset	Address Offset Value / Register Name				Block Name
	+3	+2	+1	+0	
0000_8000	ICUxx_IPCP0 XXXXXXXX_XXXXXXXX_XXXXXXXX_XXXXXXXX				Common Peripheral #0
0000_8004	ICUxx_IPCP1 XXXXXXXX_XXXXXXXX_XXXXXXXX_XXXXXXXX				
0000_8008	ICUxx_ICS 11111111_11111111_11111100_00000000				
0000_800C	ICUxx_ICSC 00000000_00000000_00000000_00000000				
0000_8010	ICUxx_ICSS 00000000_00000000_00000000_00000000				
0000_8014 0000_83FC	-				

Notes:

- “X”: Initial value undefined
- “xx”: Pair channel number (0 to 2, 8 to 10)

Register List of the 32-Bit Input Capture

Table 3-1 Register List of the 32-Bit Input Capture

Abbreviated Register Name	Register Name	Reference
IPCP0/IPCP1	Input capture data registers 0, 1	3.1
ICS	Input capture state control register	3.2
ICSC	Input capture state control clear register	3.3
ICSS	Input capture state control set register	3.4

Register Bit Locations of 32-Bit Input Capture**Table 3-2 Register Bit Locations of 32-Bit Input Capture**

	bit31	bit30	bit29	bit28	bit27	bit26	bit25	bit24
	bit23	bit22	bit21	bit20	bit19	bit18	bit17	bit16
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
IPCP0	CP31	CP30	CP29	CP28	CP27	CP26	CP25	CP24
	CP23	CP22	CP21	CP20	CP19	CP18	CP17	CP16
	CP15	CP14	CP13	CP12	CP11	CP10	CP09	CP08
	CP07	CP06	CP05	CP04	CP03	CP02	CP01	CP00
IPCP1	CP31	CP30	CP29	CP28	CP27	CP26	CP 25	CP24
	CP23	CP22	CP21	CP20	CP19	CP18	CP17	CP16
	CP15	CP14	CP13	CP12	CP11	CP10	CP09	CP08
	CP07	CP06	CP05	CP04	CP03	CP02	CP01	CP00
ICS	Reserved							
	Reserved							
	Reserved						IEI1	IEI0
	ICP1	ICP0	ICE1	ICE0	EG11	EG10	EG01	EG00
ICSC	Reserved							
	Reserved							
	Reserved							
	ICP1C	ICP0C	ICE1C	ICE0C	Reserved			
ICSS	Reserved							
	Reserved							
	Reserved							
	Reserved		ICE1S	ICE0S	Reserved			

3.1. Input Capture Data Registers 0, 1 (IPCP0, IPCP1)

Input capture data registers 0, 1 (IPCP0, IPCP1) are used to store the count value of the free-run timer when a valid edge of an external input signal is detected.

Input Capture Data Register (IPCP0)

bit	31	30	29	28	27	26	25	24
Field	CP31	CP30	CP29	CP28	CP27	CP26	CP25	CP24
R/W Attribute	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX
Protection Attribute	-	-	-	-	-	-	-	-
Initial Value	X	X	X	X	X	X	X	X

bit	23	22	21	20	19	18	17	16
Field	CP23	CP22	CP21	CP20	CP19	CP18	CP17	CP16
R/W Attribute	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX
Protection Attribute	-	-	-	-	-	-	-	-
Initial Value	X	X	X	X	X	X	X	X

bit	15	14	13	12	11	10	9	8
Field	CP15	CP14	CP13	CP12	CP11	CP10	CP09	CP08
R/W Attribute	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX
Protection Attribute	-	-	-	-	-	-	-	-
Initial Value	X	X	X	X	X	X	X	X

bit	7	6	5	4	3	2	1	0
Field	CP07	CP06	CP05	CP04	CP03	CP02	CP01	CP00
R/W Attribute	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX
Protection Attribute	-	-	-	-	-	-	-	-
Initial Value	X	X	X	X	X	X	X	X

[bit31:0] CP[31:00]: Input Capture Data Value Bit

The input capture data register 0 (IPCP0) is used to store the value of the free-run timer when a valid edge of the external input pin IN0 signal is detected.

The free-run timer that is mentioned here indicates the operating state of the free-run timer that is connected to the input capture.

Note:

- For access to this register, use word access instructions.

Input Capture Data Register (IPCP1)

bit	31	30	29	28	27	26	25	24
Field	CP31	CP30	CP29	CP28	CP27	CP26	CP25	CP24
R/W Attribute	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX
Protection Attribute	-	-	-	-	-	-	-	-
Initial Value	X	X	X	X	X	X	X	X

bit	23	22	21	20	19	18	17	16
Field	CP23	CP22	CP21	CP20	CP19	CP18	CP17	CP16
R/W Attribute	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX
Protection Attribute	-	-	-	-	-	-	-	-
Initial Value	X	X	X	X	X	X	X	X

bit	15	14	13	12	11	10	9	8
Field	CP15	CP14	CP13	CP12	CP11	CP10	CP09	CP08
R/W Attribute	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX
Protection Attribute	-	-	-	-	-	-	-	-
Initial Value	X	X	X	X	X	X	X	X

bit	7	6	5	4	3	2	1	0
Field	CP07	CP06	CP05	CP04	CP03	CP02	CP01	CP00
R/W Attribute	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX
Protection Attribute	-	-	-	-	-	-	-	-
Initial Value	X	X	X	X	X	X	X	X

[bit31:0] CP[31:00]: Input Capture Data Value Bit

Input capture data register 1 (IPCP1) is used to store the value of the free-run timer when a valid edge of the external input pin IN1 signal is detected.

The free-run timer that is mentioned here indicates the operating state of the free-run timer that is connected to the input capture.

Note:

- For access to this register, use word access instructions.

3.2. Input Capture State Control Register (ICS)

The input capture state control register (ICS) is used to select an edge, enable an interrupt request, and control an interrupt request flag. This register is also used to indicate a valid edge detected in the input captures 0, 1.

For details on writing to this register, see "4. Precautions for Using This Device."

Flag bits of the input capture state control registers are only read if the APB-IF is valid.

bit	31	30	29	28	27	26	25	24
Field	Reserved							
R/W Attribute	R1,WX							
Protection Attribute	-							
Initial Value	11111111							

bit	23	22	21	20	19	18	17	16
Field	Reserved							
R/W Attribute	R1,WX							
Protection Attribute	-							
Initial Value	11111111							

bit	15	14	13	12	11	10	9	8
Field	Reserved						IEI1	IEI0
R/W Attribute	R1,WX						R,WX	R,WX
Protection Attribute	-						-	-
Initial Value	111111						0	0

bit	7	6	5	4	3	2	1	0
Field	ICP1	ICP0	ICE1	ICE0	EG11	EG10	EG01	EG00
R/W Attribute	R,WX	R,WX	R/W	R/W	R/W	R/W	R/W	R/W
Protection Attribute	-	-	-	-	-	-	-	-
Initial Value	0	0	0	0	0	0	0	0

[bit31:10] Reserved: Reserved Bits

The read value is "1".

Writing data to these bits has no effect on the operation.

[bit9] IEI1: Valid Edge Indication Bit (Input Capture 1)

- This bit is a valid edge indication bit in input capture data register 1. This bit indicates that a rising or falling edge is detected.
- When a falling edge is detected, this bit is set to "0".
- When a rising edge is detected, this bit is set to "1".
- This bit is read-only.

Bit	Description
0	A falling edge is detected.
1	A rising edge is detected.

Notes:

- The value read is meaningless if the edge selection bit (EG11, EG10: bit3, bit2) is set to "00_B".
- If the edge selection bit (EG11, EG10: bit3, bit2) is set to any value other than "00_B", then the value is updated when the interrupt request flag (ICP1) is set.

[bit8] IEI0: Valid Edge Indication Bit (Input Capture 0)

- This bit is a valid edge indication bit in input capture data register 0. This bit indicates that a rising or falling edge is detected.
- When a falling edge is detected, this bit is set to "0".
- When a rising edge is detected, this bit is set to "1".
- This bit is a read-only bit.

Bit	Description
0	A falling edge is detected.
1	A rising edge is detected.

Notes:

- The value read is meaningless if the edge selection bit (EG01, EG00: bit1, bit0) is set to "00_B".
- If the edge selection bit (EG01, EG00: bit1, bit0) is set to any value other than "00_B", then the value is updated when the interrupt request flag (ICP0) is set.

[bit7] ICP1: Interrupt Request Flag Bit (Input Capture 1)

- This bit is used as an interrupt request flag of input capture 1.
- This bit is set to "1" immediately upon detecting a valid edge on the external input pin (IN1).
- An interrupt is generated as soon as this bit is set to "1" when the interrupt request enable bit (ICE1: bit5) is "1".
- This bit is a read-only bit. Writing data to these bits has no effect on the operation.
- This bit is cleared to "0" by writing "1" to the ICP1C bit in the ICSC register.

Bit	Description
0	No valid edge is detected.
1	A valid edge is detected.

[bit6] ICP0: Interrupt Request Flag Bit (Input Capture 0)

- This bit is used as an interrupt request flag of input capture 0.
- This bit is set to "1" immediately upon detecting a valid edge on the external input pin (IN0).
- An interrupt is generated as soon as this bit is set to "1" when the interrupt request enable bit (ICE0: bit4) is "1".
- This bit is a read-only bit. Writing data to these bits has no effect on the operation.
- This bit is cleared to "0" by writing "1" to the ICP0C bit in the ICSC register.

Bit	Description
0	No valid edge is detected.
1	A valid edge is detected.

[bit5] ICE1: Interrupt Request Enable Bit (Input Capture 1)

- This bit is used to enable an interrupt request of input capture 1.
- An interrupt of input capture 1 is generated when the interrupt request flag bit (ICP1: bit7) is set while this bit is "1".
- This bit is cleared to "0" by writing "1" to the ICE1C bit in the ICSC register.
- This bit is set to "1" by writing "1" to the ICE1S bit in the ICSS register.

Bit	Description
0	Disable interrupt requests.
1	Enable interrupt requests.

[bit4] ICE0: Interrupt Request Enable Bit (Input Capture 0)

- This bit is used to enable an interrupt request of input capture 0.
- An interrupt of input capture 0 is generated when the interrupt request flag bit (ICP0: bit6) is set while this bit is "1".
- This bit is cleared to "0" by writing "1" to the ICE0C bit in the ICSC register.
- This bit is set to "1" by writing "1" to the ICE0S bit in the ICSS register.

Bit	Description
0	Disable interrupt requests.
1	Enable interrupt requests.

[bit3:2] EG11, EG10: Edge Selection Bits (Input Capture 1)

- These bits are used to enable the operation of input capture 1. These bits specify a valid edge of the external input (IN1).

Bits		Description
EG11	EG10	
0	0	No edge is detected (stop).
0	1	A rising edge is detected.
1	0	A falling edge is detected.
1	1	Both edges are detected.

[bit1:0] EG01, EG00: Edge Selection Bits (Input Capture 0)

- These bits are used to enable the operation of input capture 0. These bits specify a valid edge of the external input (IN0).

Bits		Description
EG01	EG00	
0	0	No edge is detected (stop).
0	1	A rising edge is detected.
1	0	A falling edge is detected.
1	1	Both edges are detected.

3.3. Input Capture State Control Clear Register (ICSC)

The input capture state control clear register (ICSC) is a register to clear a bit in the input capture state control register (ICS).

bit	31	30	29	28	27	26	25	24
Field	Reserved							
R/W Attribute	R0,W0							
Protection Attribute	-							
Initial Value	00000000							

bit	23	22	21	20	19	18	17	16
Field	Reserved							
R/W Attribute	R0,W0							
Protection Attribute	-							
Initial Value	00000000							

bit	15	14	13	12	11	10	9	8
Field	Reserved							
R/W Attribute	R0,W0							
Protection Attribute	-							
Initial Value	00000000							

bit	7	6	5	4	3	2	1	0
Field	ICP1C	ICP0C	ICE1C	ICE0C	Reserved			
R/W Attribute	R0,W	R0,W	R0,W	R0,W	R0,W0			
Protection Attribute	-	-	-	-	-			
Initial Value	0	0	0	0	0000			

[bit31:8] Reserved: Reserved Bits

The read value is "0".

Always write "0" to this bit.

[bit7] ICP1C: ICP1 Clear Bit

- Writing "1" to this bit clears the ICP1 bit in the ICS register.
- "0" is always read from this bit.

Bit	Description
0	Do not affect this bit and the interrupt request flag bit (input capture1) (ICP1) in the input capture state control register (ICS).
1	Clear the interrupt request flag bit (input capture1) (ICP1) in the input capture state control register (ICS).

[bit6] ICP0C: ICP0 Clear Bit

- Writing "1" to this bit clears the ICP0 bit in the ICS register.
- "0" is always read from this bit.

Bit	Description
0	Do not affect this bit and the interrupt request flag bit (input capture0) (ICP0) in the input capture state control register (ICS).
1	Clear the interrupt request flag bit (input capture0) (ICP0) in the input capture state control register (ICS).

[bit5] ICE1C: ICE1 Clear Bit

- Writing "1" to this bit clears the ICE1 bit in the ICS register.
- "0" is always read from this bit.

Bit	Description
0	Do not affect this bit and the interrupt request enable bit (input capture 1) (ICE1) in the input capture state control register (ICS).
1	Clear the interrupt request enable bit (input capture 1) (ICE1) in the input capture state control register (ICS).

[bit4] ICE0C: ICE0 Clear Bit

- Writing "1" to this bit clears the ICE0 bit in the ICS register.
- "0" is always read from this bit.

Bit	Description
0	Do not affect this bit and the interrupt request enable bit (input capture 0) (ICE0) in the input capture state control register (ICS).
1	Clear the interrupt request enable bit (input capture 0) (ICE0) in the input capture state control register (ICS).

[bit3:0] Reserved: Reserved Bits

The read value is "0".

Always write "0" to this bit.

3.4. Input Capture State Control Set Register (ICSS)

The input capture state control set register (ICSS) is a register that sets the bit in the input capture state control register (ICS).

bit	31	30	29	28	27	26	25	24
Field	Reserved							
R/W Attribute	R0,W0							
Protection Attribute	-							
Initial Value	00000000							

bit	23	22	21	20	19	18	17	16
Field	Reserved							
R/W Attribute	R0,W0							
Protection Attribute	-							
Initial Value	00000000							

bit	15	14	13	12	11	10	9	8
Field	Reserved							
R/W Attribute	R0,W0							
Protection Attribute	-							
Initial Value	00000000							

bit	7	6	5	4	3	2	1	0
Field	Reserved	ICE1S	ICE0S	Reserved				
R/W Attribute	R0,W0	R0,W	R0,W	R0,W0				
Protection Attribute	-	-	-	-				
Initial Value	00	0	0	0000				

[bit31:6] Reserved: Reserved Bits

The read value is "0".

Always write "0" to this bit.

[bit5] ICE1S: ICE1 Set Bit

- Writing "1" to this bit sets the ICE1 bit in the ICS register to "1".
- "0" is always read from this bit.

Bit	Description
0	Do not affect this bit and the interrupt request enable bit (input capture 1) (ICE1) in the input capture state control register (ICS).
1	Set the interrupt request enable bit (input capture 1) (ICE1) in the input capture state control register (ICS).

[bit4] ICE0S: ICE0 Set Bit

- Writing "1" to this bit sets the ICE0 bit in the ICS register to "1".
- "0" is always read from this bit.

Bit	Description
0	Do not affect this bit and the interrupt request enable bit (input capture 0) (ICE0) in the input capture state control register (ICS).
1	Set the interrupt request enable bit (input capture 0) (ICE0) in the input capture state control register (ICS).

[bit3:0] Reserved: Reserved Bit

The read value is "0".

Always write "0" to this bit.

4. Precautions for Using This Device

The following shows the notes when using the 32-bit input capture.

Notes to Observe when Accessing a Register

When Accessing the Input Capture Data Registers 0, 1 (IPCP0, 1)

Use word access instructions for the input capture data registers 0, 1 (IPCP0, 1).

When Accessing the Input Capture State Control Register (ICS)

- This register supports writing from the bit-band alias area. For the bit-band alias area, see the chapter of "Bit-Band Unit" in Traveo™ Platform hardware manual.
- To clear a specified bit in this register, clear the bit by writing "1" to the applicable bit in the input capture state control clear register (ICSC).
- To set a specified bit in this register, set the bit by writing "1" to the applicable bit in the input capture state control set register (ICSS).
- Data can be written directly to this register only when writing to all bits.

Notes on Interrupt Processing

- The valid edge indication bit (IEI1, IEI0: bit9, bit8) in the input capture state control register (ICS) indicates a detected latest edge when the level of the external input pin (IN0, IN1) switches while an interrupt routine is processing after the interrupt request flag (ICP1, ICP0) in the input capture state control register (ICS) is set to "1".

Notes on Input Capture Operation

About Capture Timing

- Capture resolution is 1 peripheral clock because the input capture operates according to the peripheral clock timing. The resolution is 1 timer count because the capture data is the timer counter value of the free-run timer.

CHAPTER 21: 32-bit Reload Timer



This chapter explains 32-bit Reload Timer.

1. Overview
2. Configuration and Block Diagram
3. Operation of the 32-bit Reload Timer
4. Registers

CODE: RLT-S6J3400-E1

1. Overview

This section gives a brief overview of the 32-bit Reload Timer.

Features of 32-bit Reload Timer

The 32-bit Reload Timer consists of a 32-bit down counter, a 32-bit Reload register, one input(TIN), one output (TOT), and control registers. The 32-bit Reload Timer has the following features:

- External and internal clock/event source
- Trigger signal programmable as rising/falling edge or both
- Gated count function
- One-shot or reload counter mode
- Counter state can be made visible at external pin
- Prescaler with six different settings for the internal clock and two different settings for the external clock
- Several Reload Timers can be cascaded to form a longer Reload Timer
- Support for MCU debug mode

DMA and Interrupts

The 32-bit Reload Timer can generate DMA request which can be used to start DMA transfers.

The 32-bit Reload Timer can generate interrupt in case of underflow.

This section shows a block diagram of the 32-bit Reload Timer.

The diagram illustrates the internal architecture of the Real-time Interrupt Controller (RLTn). It features a central BUS interface. Key components include:

- Registers:** RLTn_DMACFG:ENDMAUF, RLTn_TMCSR:UFCLR, RLTn_TMCSR:RELD, RLTn_TMCSR:OUTL, RLTn_TMCSR:INTE, RLTn_TMCSR:CSL0, RLTn_TMCSR:CSL1, RLTn_TMCSR:CSL2, RLTn_TMCSR:UF, RLTn_TMCSR:TRG, RLTn_TMCSR:CNTL, RLTn_TMCSR:MOD[2:0], RLTn_TMCSR:DBGE, and RLTn_TMCSR:NFE.
- Counters and Registers:** 32-bit reload register (RLTn_TMRLR), 32-bit down counter (RLTn_TMR), and a 1/2 divider.
- Control Logic:** CTL, MUX, Clock selector, IN CTL., OUT CTL., Reload, LD CTL., and a Noise filter.
- Inputs/Outputs:** DMA_REQ, DMA_REQ_ACK, IRQn, TOT, TIN, and DEBUG.
- Logic Elements:** AND gates, OR gates, and a multiplexer (MUX).

The diagram shows the flow of data and control signals between these components, including the generation of the DMA_REQ signal and the handling of the TIN input through a noise filter.

3. Operation of the 32-bit Reload Timer

This section describes the operation of the 32-bit Reload Timer.

3.1 Internal Clock and External Event Counter Operations of 32-bit Reload Timer

3.2 Underflow Operation of 32-bit Reload Timer

3.3 Output Functions of 32-bit Reload Timer

3.4 Counter Operation State

3.5 DMA Operation

3.1. Internal Clock and External Event Counter Operations of 32-bit Reload Timer

In internal clock mode, the peripheral clock with different divider settings can be selected as the clock source for operating the Reload Timer. The external input TIN can be selected as either a trigger input, or as a gate input by a register setting.

In event counter mode, the TIN is used as an external event input. Each active edge on this input (rising, falling, or both) decrements the counter.

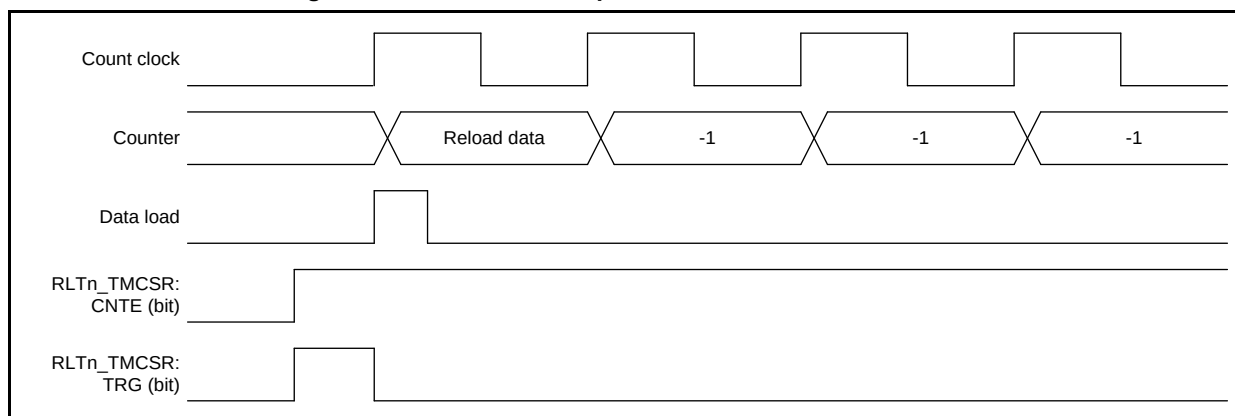
When $RLTn\_TMCSR:CSL0 = 1$, then each second event is counted.

Internal Clock Operation of 32-bit Reload Timer

Writing "1" to both $RLTn\_TMCSR:CNTE$ and $RLTn\_TMCSR:TRG$ bits enables and starts counting at the same time. Using the $RLTn\_TMCSR:TRG$ bit as a trigger input is always available when the timer is enabled ($RLTn\_TMCSR:CNTE = 1$), regardless of the operation mode.

Figure 3-1 shows counter activation and counter operation.

Figure 3-1 Activation and Operation of 32-bit Reload Timer Counter

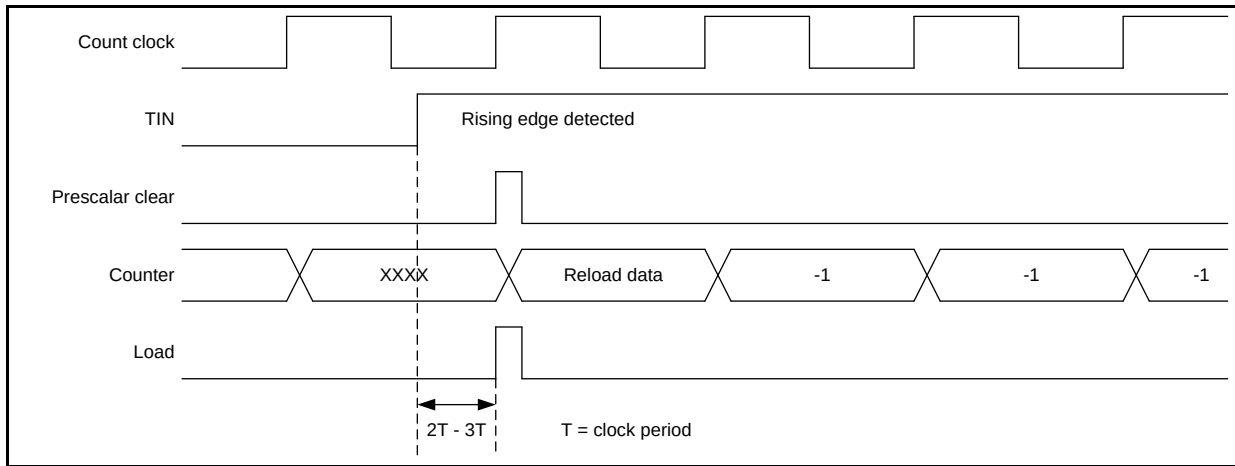


Input Functions of 32-bit Reload Timer (In Internal Clock Mode)

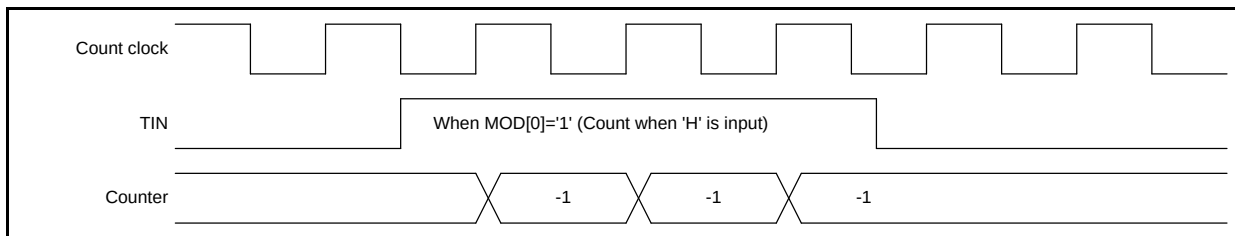
The TIN input can be used as either a trigger input, or as a gate input, when an internal clock is selected as the clock source.

Trigger Input

When used as a trigger input, an active edge causes the timer to load the reload register contents and resets the internal prescaler. Then, count operation starts. For the minimum pulse width length of TIN refer to device specific datasheet.

Figure 3-2 Trigger Input Operation of 32-bit Reload Timer**Gate Input**

When used as a gate input, the counter only counts while the active level specified by the `RLTn_TMCSR:MOD[0]` bit is input to the TIN. In this case, the count clock continues to operate unless stopped. The software trigger can be used in gate mode, regardless of the gate level. For the minimum pulse width length of TIN refer to device specific datasheet.

Figure 3-3 Gate Input Operation of 32-bit Reload Timer**External Event Counter**

When external event count mode is selected, the TIN is used as an external event input. The counter counts on the active edge specified in the `RLTn_TMCSR`. For the minimum pulse width length of TIN refer to device specific datasheet.

3.2. Underflow Operation of 32-bit Reload Timer

An underflow is defined for this timer as the time when the counter value changes from 0x00000000 to 0xFFFFFFFF or reload occurs (RLTn_TMCSR:RELD= 1). Therefore, an underflow occurs after (reload register setting + 1) counts.

Underflow Operation of 32-bit Reload Timer

If the RLTn_TMCSR:RELD bit is "1" and an underflow occurs, the contents of the reload register is loaded into the counter and counting continues.

If the RLTn_TMCSR:RELD bit is "0", counting stops when counter reaches 0xFFFFFFFF.

The RLTn_TMCSR:UF bit is set when the underflow occurs. If the RLTn_TMCSR:INTE bit is "1" at this time, an interrupt request is generated.

Figure 3-4 shows the operation when an underflow occurs with various values of RLTn_TMCSR:RELD. Figure 3-5 shows the clearing operation of underflow flag.

Figure 3-4 Underflow Operation of 32-bit Reload Timer

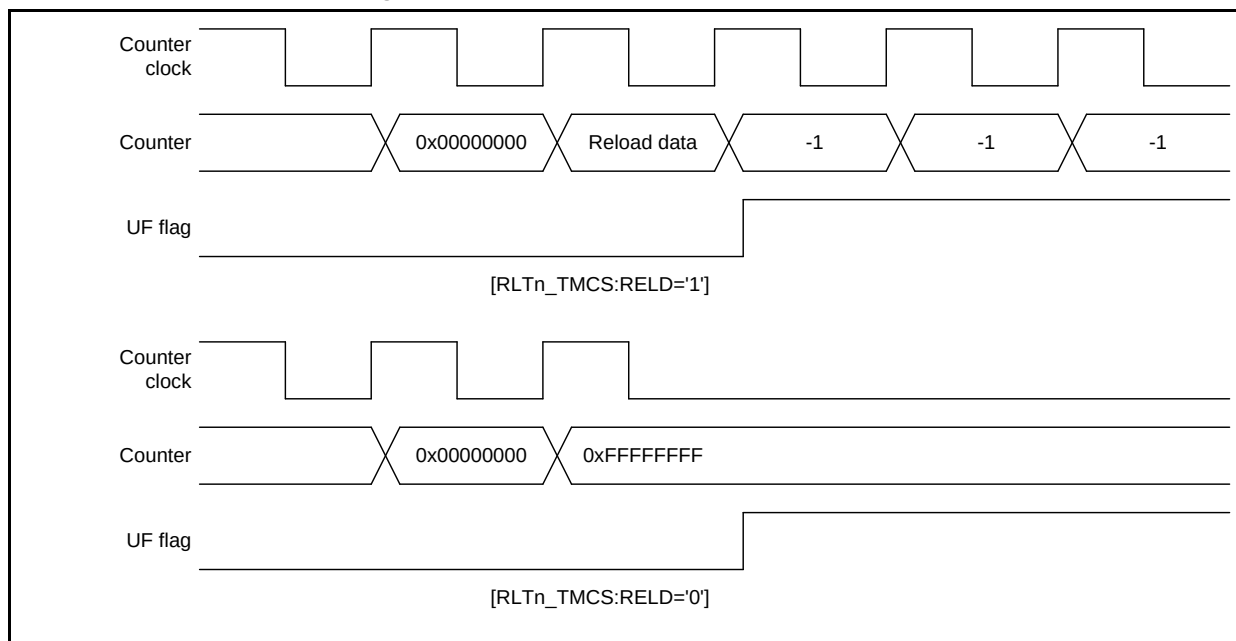
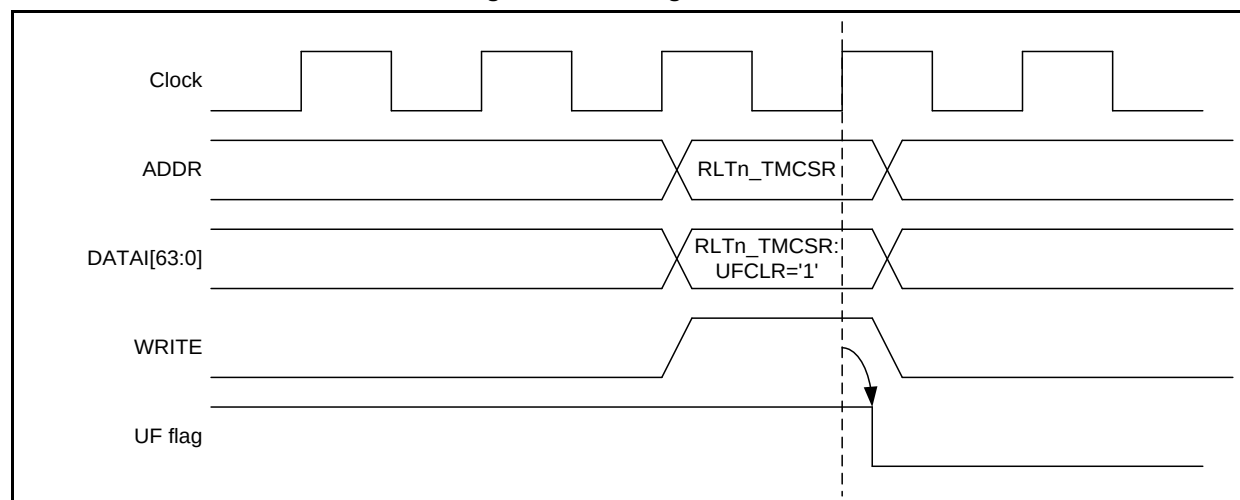


Figure 3-5 Clearing of Underflow Bit

3.3. Output Functions of 32-bit Reload Timer

In reload mode, the TOT output performs toggle output (inverts at each underflow). In one-shot mode, the TOT output is used as a pulse output that shows the configured level while the counting is in progress.

Output Signal Functions of 32-bit Reload Timer

The RL_{Tn}_TMCSR:OUTL bit sets the output polarity.

When RL_{Tn}_TMCSR:OUTL = 0, the initial value for toggle output is "L" and the one-shot pulse output is "H" while the count is in progress.

When RL_{Tn}_TMCSR:OUTL = 1, the output waveforms are opposite.

Figure 3-6 and Figure 3-7 show the output signal functions.

Figure 3-6 Output Signal Function of 32-bit Reload Timer in Reload Mode

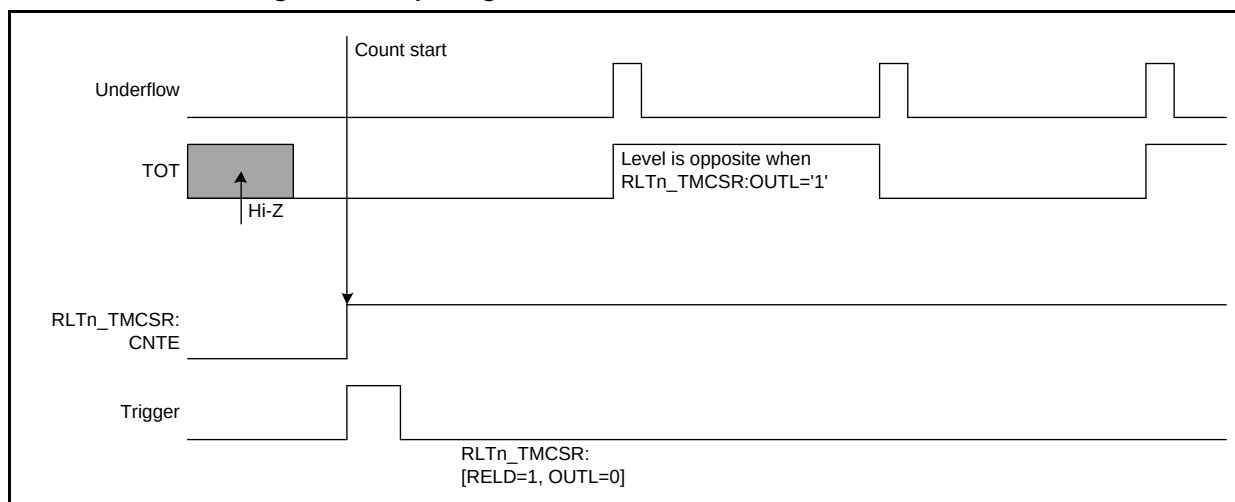
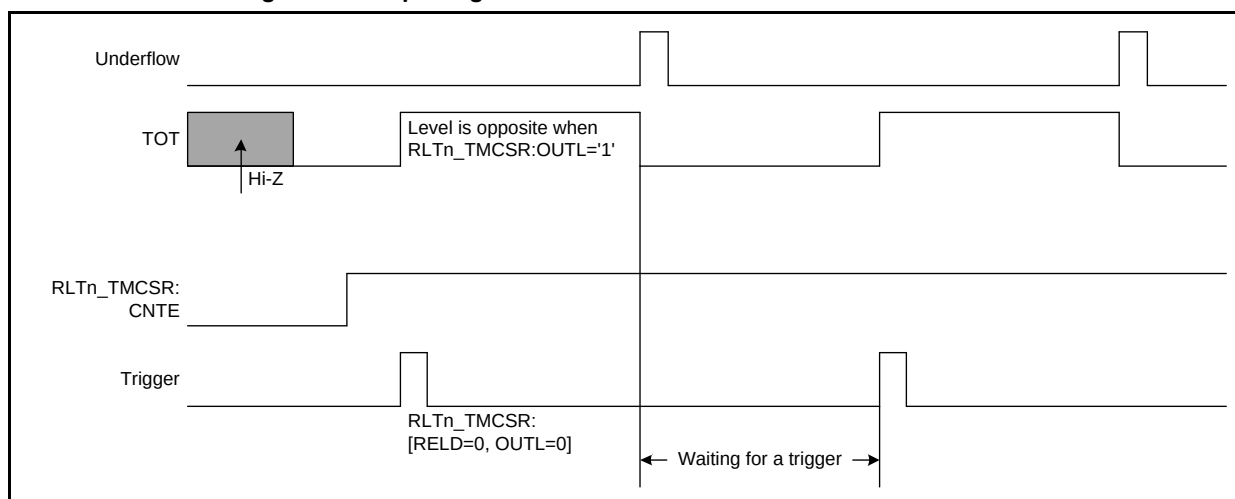


Figure 3-7 Output Signal Function of 32-bit Reload Timer in One-shot Mode



3.4. Counter Operation State

The counter state is determined by RL_{Tn}_TMCSR:CNTE bit in the Timer Control Status Register and the internal WAIT signal.

Available States for Reload Timer Are:

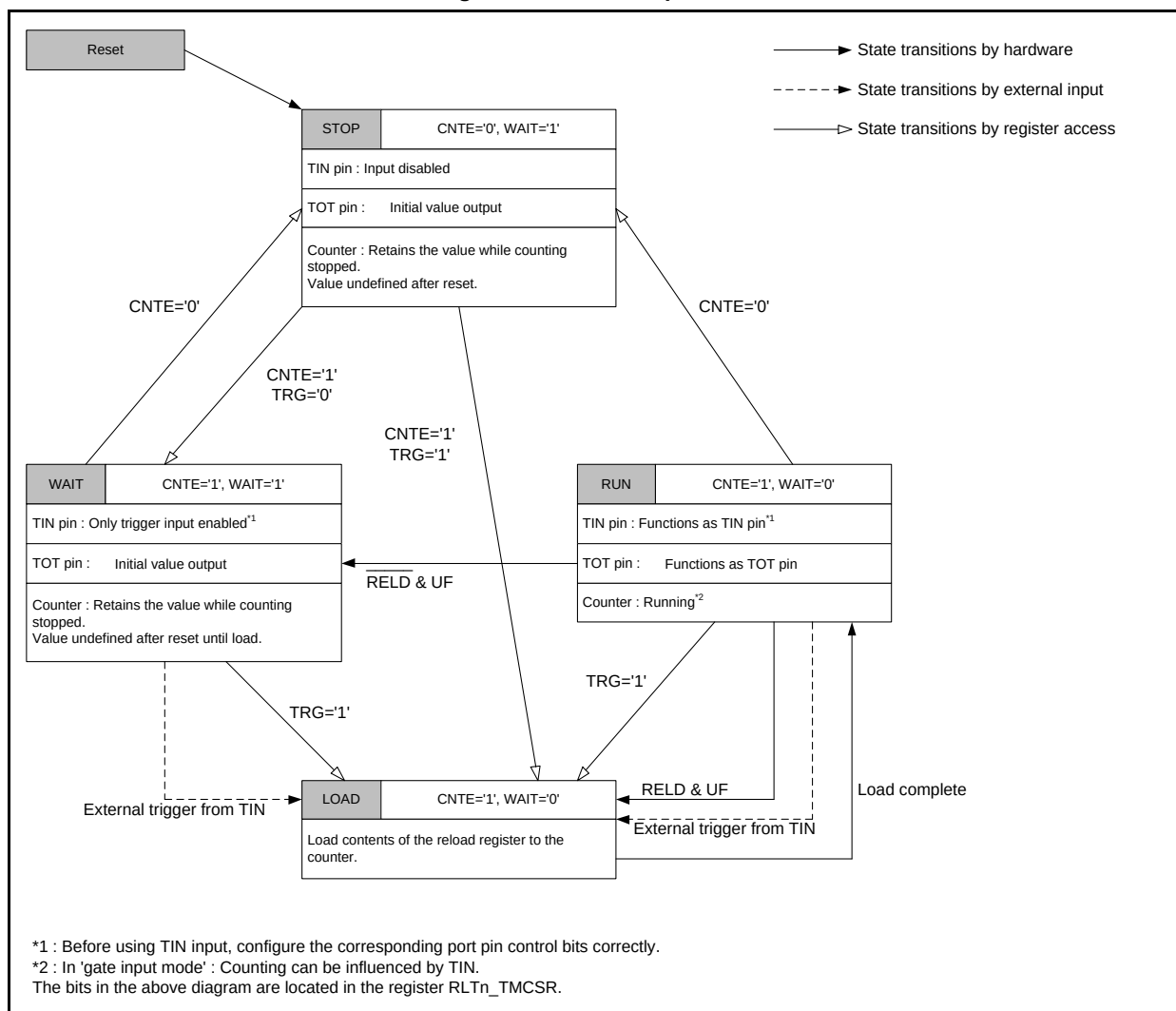
Stop state: RL_{Tn}_TMCSR:CNTE = 0 and WAIT = 1

Wait state: RL_{Tn}_TMCSR:CNTE = 1 and WAIT = 1

Run state: RL_{Tn}_TMCSR:CNTE = 1 and WAIT = 0

Counter Operation States

Figure 3-8 Counter Operation States



3.5. DMA Operation

The DMA support is determined by the RL_{Tn}_DMACFG:ENDMAUF bit. Setting this bit enables DMA request generation for DMA. Assertion of DMA_REQ_ACK signal acknowledges request and hence DMA_REQ signal gets de-asserted.

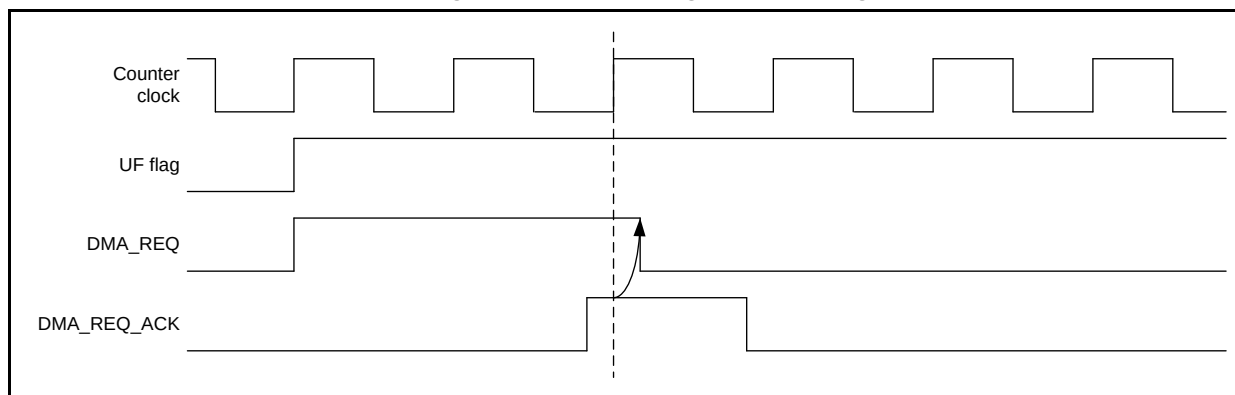
Enabling DMA Support

Writing "1" to RL_{Tn}_DMACFG:ENDMAUF enables DMA request generation for DMA when RL_{Tn}_TMCSR:UF bit sets. However, writing "0" to RL_{Tn}_DMACFG:ENDMAUF disables DMA request generation even if RL_{Tn}_TMCSR:UF bit sets.

When DMA_REQ_ACK is asserted the DMA_REQ signal gets de-asserted by acknowledging the DMA request.

Figure 3-9 shows behavior of DMA_REQ_ACK when asserted.

Figure 3-9 De-Asserting DMA_REQ Signal



4. Registers

This section describes the registers of 32-bit Reload Timer.

Table 4-1 Memory Layout of 32-bit Reload Timer Registers

Offset	+3	+2	+1	+0
0x00000000	RLTn_DMACFG 00000000_00000000_00000000_00000000			
0x00000004	Reserved			
0x00000008	RLTn_TMCSR 00000000_00000000_00000000_00000000			
0x0000000C	Reserved			
0x00000010	RLTn_TMRLR XXXXXXXX_XXXXXXXX_XXXXXXXX_XXXXXXXX			
0x00000014	RLTn_TMR XXXXXXXX_XXXXXXXX_XXXXXXXX_XXXXXXXX			

Note:

- The initial register value after reset indicates as follows:
 - "1": Initial value "1"
 - "0": Initial value "0"
 - "X": Initial value undefined
 - "-": Reserved bit/Undefined bit
 - "*": Initial value "0" or "1" according to the setting

4.1. DMA Configuration Register (RLTn_DMACFG)

The DMA Configuration Register controls the DMA request generation for underflow condition.

BITS_OFFSET	31	30	29	28	27	26	25	24
BITS_NAME	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
ACCESS_TYPE	R0,WX	R0,WX	R0,WX	R0,WX	R0,WX	R0,WX	R0,WX	R0,WX
PROT_TYPE	-							
INITIAL_VALUE	0	0	0	0	0	0	0	0

BITS_OFFSET	23	22	21	20	19	18	17	16
BITS_NAME	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
ACCESS_TYPE	R0,WX	R0,WX	R0,WX	R0,WX	R0,WX	R0,WX	R0,WX	R0,WX
PROT_TYPE	-							
INITIAL_VALUE	0	0	0	0	0	0	0	0

BITS_OFFSET	15	14	13	12	11	10	9	8
BITS_NAME	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
ACCESS_TYPE	R0,WX	R0,WX	R0,WX	R0,WX	R0,WX	R0,WX	R0,WX	R0,WX
PROT_TYPE	-							
INITIAL_VALUE	0	0	0	0	0	0	0	0

BITS_OFFSET	7	6	5	4	3	2	1	0
BITS_NAME	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	ENDMAUF
ACCESS_TYPE	R0,WX	R0,WX	R0,WX	R0,WX	R0,WX	R0,WX	R0,WX	R/W
PROT_TYPE	-							
INITIAL_VALUE	0	0	0	0	0	0	0	0

[bit31:1] Reserved

[bit0] ENDMAUF : DMA enable for underflow (ENDMAUF)

Bit	Description
0	No DMA request is generated
1	A DMA request is generated when the counter, RLTn_TMR, underflows

4.2. Timer Control Status Register (RLTn_TMCSR)

The Timer Control Status Register controls the operation mode and interrupt of the 32-bit Reload Timer.

BIT_OFFSET	31	30	29	28	27	26	25	24
BIT_NAME	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	CNTE
ACCESS_TYPE	R0,WX	R0,WX	R0,WX	R0,WX	R0,WX	R0,WX	R0,WX	R/W
PROT_TYPE	-							
INITIAL_VALUE	0	0	0	0	0	0	0	0

BIT_OFFSET	23	22	21	20	19	18	17	16
BIT_NAME	Reserved	Reserved	Reserved	Reserved	Reserved	TRG	UFCLR	UF
ACCESS_TYPE	R0,WX	R0,WX	R0,WX	R0,WX	R0,WX	R0,W	R0,W	R,WX
PROT_TYPE	-							
INITIAL_VALUE	0	0	0	0	0	0	0	0

BIT_OFFSET	15	14	13	12	11	10	9	8
BIT_NAME	MOD[2]	MOD[1]	MOD[0]	CSL2	CSL1	CSL0	Reserved	NFE
ACCESS_TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R0,WX	R/W
PROT_TYPE	-							
INITIAL_VALUE	0	0	0	0	0	0	0	0

BIT_OFFSET	7	6	5	4	3	2	1	0
BIT_NAME	DBG	Reserved	OUTL	RELD	INTE	Reserved	Reserved	Reserved
ACCESS_TYPE	R/W	R0,W0	R/W	R/W	R/W	R0,WX	R0,WX	R0,WX
PROT_TYPE	-							
INITIAL_VALUE	0	0	0	0	0	0	0	0

[bit31:25] Reserved

[bit24] CNTE: Count enable

The Count Enable (CNTE) bit is a timer count enable bit.

Bit	Description
0	Stops count operation
1	Sets the timer to wait for a trigger

[bit23:19] Reserved

[bit18] TRG: Trigger

Software trigger bit.

Bit	Description
0	No effect
1	Applies a software trigger, causing the timer to load the reload register content to the counter and starts counting

Notes:

- Applying a trigger using this register is only valid when $RLTn\_TMCSR:CNTE = 1$. If $RLTn\_TMCSR:CNTE = 0$, writing "1" to TRG has no effect.
- Set this bit in 'gate input mode' and in 'event count mode' to load the reload register content before counting starts.

[bit17] UFCLR: Underflow interrupt clear

Bit	Description
0	No effect
1	Clears $RLTn\_TMCSR:UF$ bit

[bit16] UF: Underflow

The Underflow (UF) is timer interrupt request flag.

Bit	Description
0	No underflow occurred
1	When an underflow occurred

Note:

- UF bit is cleared by writing "1" to $RLTn\_TMCSR:UFCLR$ bit.

[bit15:13] MOD: Operation mode

The Operation Mode (MOD[2:0]) bits set the operation mode and input (TIN) functions.

Table 4-2 and Table 4-3 list the MOD[2:0] bit settings.

[bit12] CSL2: Clock select 2

The Clock Select 2 (CSL2) bit specifies the clock/event source and the clock division ratio.

Table 4-4 lists the selected clock sources for different CSL0/1/2 settings.

[bit11] CSL1: Clock select 1

The Clock Select 1 (CSL1) bit specifies the clock/event source and the clock division ratio.

Table 4-4 lists the selected clock sources for different CSL0/1/2 settings.

[bit10] CSL0: Clock select 0

The Clock Select 0 (CSL0) bit specifies the count clock division ratio.

Table 4-4 lists the selected clock sources for different CSL0/1/2 settings.

[bit9] Reserved

[bit8] NFE: Noise filter enable

This bit is used to enable/disable the noise filter for the TIN input.

Bit	Description
0	Noise filter for TIN is disabled
1	Noise filter for TIN is enabled

[bit7] DBGE: Debug mode enable

This bit is used to enable/disable debug mode for RLT.

Bit	Description
0	Debug mode disabled
1	Debug mode enabled

Note:

- When DBGE is set to "1" and the processor is in debug state, the timer counter operation is paused, and writing to the RL_{Tn}_TMRLR register directly updates the timer counter (RL_{Tn}_TMR register). When the processor leaves debug state or DBGE is set to "0", the timer counter operation is resumed.

[bit6] Reserved**[bit5] OUTL: Output level**

This Output Level (OUTL) bit sets the output level for the TOT.

Refer to Table 4-5.

[bit4] RELD: Reload

This Reload (RELD) bit enables reload operations.

Refer to Table 4-5.

Bit	Description
0	The timer operates in one-shot mode. In this mode, the count operation stops when an underflow occurs due to the counter value changing from 0x00000000 to 0xFFFFFFFF
1	The timer operates in reload mode. In this mode, the timer loads the reload register contents into the counter and continues counting whenever an underflow occurs

[bit3] INTE: Interrupt enable

Timer interrupt request enable bit.

Bit	Description
0	No interrupt request is generated even when the RL _{Tn} _TMCSR:UF bit changes to "1"
1	An interrupt request is generated when the RL _{Tn} _TMCSR:UF bit changes to "1"

[bit2:0] Reserved

Table 4-2 RL_{Tn}_TMCSR:MOD[2:0] Bit Settings for Internal Clock Mode (RL_{Tn}_TMCSR:CSL1 / RL_{Tn}_TMCSR:CSL2 = 0b00, 0b01, or 0b10)

MOD[2]	MOD[1]	MOD[0]	Input Function	Active Edge or Level
0	0	0	Trigger disabled	-
0	0	1	Trigger input	Rising edge
0	1	0		Falling edge
0	1	1		Both edge
1	x	0	Gate input	"L" level
1	x	1		"H" level

Table 4-3 RL_{Tn}_TMCSR:MOD[2:0] Bit Settings for Event Counter Mode (RL_{Tn}_TMCSR:CSL1 / RL_{Tn}_TMCSR:CSL2 = 0b11)

MOD[2]	MOD[1]	MOD[0]	Input Function	Active Edge or Level
x	0	0	-	-
	0	1	Event input	Rising edge
	1	0		Falling edge
	1	1		Both edge

Table 4-4 Clock Sources for RL_{Tn}_TMCSR:CSL0 / RL_{Tn}_TMCSR:CSL1 / RL_{Tn}_TMCSR:CSL2 Bit Settings

CSL2	CSL1	CSL0	Count Clock (Time for Peripheral Clock)
0	0	0	1/1
0	0	1	1/2
0	1	0	1/4
0	1	1	1/8
1	0	0	1/16
1	0	1	1/32
1	1	0	External event count mode, each event on TIN
1	1	1	External event count mode, each second event on TIN

Table 4-5 RL_{Tn}_TMCSR: OUTL, and RL_{Tn}_TMCSR:RELD Settings

OUTL	RELD	Output Waveform
0	0	Output an "H" level pulse during counting.
1	0	Output an "L" level pulse during counting.
0	1	Toggle output. Starts with "L" level output. Changes level on timer reload.
1	1	Toggle output. Starts with "H" level output. Changes level on timer reload.

Note:

- Bits marked 'x' in the table can be set to any value.

4.3. 32-bit Reload Register (RLTn_TMRLR)

The Timer Reload Register holds the reload value of the 32-bit Reload Timer.

BIT_OFFSET	31	30	29	28	27	26	25	24
BIT_NAME	TMRLR[31:24]							
ACCESS_TYPE	R/W							
PROT_TYPE	-							
INITIAL_VALUE	XXXXXXXX							

BIT_OFFSET	23	22	21	20	19	18	17	16
BIT_NAME	TMRLR[23:16]							
ACCESS_TYPE	R/W							
PROT_TYPE	-							
INITIAL_VALUE	XXXXXXXX							

BIT_OFFSET	15	14	13	12	11	10	9	8
BIT_NAME	TMRLR[15:8]							
ACCESS_TYPE	R/W							
PROT_TYPE	-							
INITIAL_VALUE	XXXXXXXX							

BIT_OFFSET	7	6	5	4	3	2	1	0
BIT_NAME	TMRLR[7:0]							
ACCESS_TYPE	R/W							
PROT_TYPE	-							
INITIAL_VALUE	XXXXXXXX							

[bit31:0] TMRLR: Timer reload register

The Timer Reload Register (RLTn_TMRLR) is a 32-bit reload register holds the reload value. Initial value is undefined.

This register can be accessed only in 32-bit/64-bit mode.

When RLTn_TMCSR:DBGE is set to "1" and the processor is in debug state, writing to this register updates the timer counter immediately.

Note:

- This register is not initialized by Hard Reset (i.e. "X").

4.4. 32-bit Timer Register (RLTn_TMR)

Reading this register returns the count value of the 32-bit Reload Timer. The initial value is undefined.

BIT_OFFSET	31	30	29	28	27	26	25	24
BIT_NAME	TMR[31:24]							
ACCESS_TYPE	R,WX							
PROT_TYPE	-							
INITIAL_VALUE	XXXXXXXX							

BIT_OFFSET	23	22	21	20	19	18	17	16
BIT_NAME	TMR[23:16]							
ACCESS_TYPE	R,WX							
PROT_TYPE	-							
INITIAL_VALUE	XXXXXXXX							

BIT_OFFSET	15	14	13	12	11	10	9	8
BIT_NAME	TMR[15:8]							
ACCESS_TYPE	R,WX							
PROT_TYPE	-							
INITIAL_VALUE	XXXXXXXX							

BIT_OFFSET	7	6	5	4	3	2	1	0
BIT_NAME	TMR[7:0]							
ACCESS_TYPE	R,WX							
PROT_TYPE	-							
INITIAL_VALUE	XXXXXXXX							

[bit31:0] TMR: Timer register

Reading this Timer Register (RLTn_TMR) returns the count value of the 32-bit Reload Timer. Initial value is undefined.

This register can be accessed only in 32-bit/64-bit mode.

Note:

- This register is not initialized by Hard Reset (i.e. "X").

CHAPTER 22: I/O Port



This chapter describes I/O port.

1. Overview
2. Configuration and Block Diagrams
3. Setting Procedure Examples
4. Register List
5. Precautions for Using This Device

CODE: IOPORT-S6J3400-E3

1. Overview

This section provides an overview of I/O port.

I/O port has a general-purpose I/O module. The external pins can be used as I/O ports. Assignment of an external pin and input to an internal resource can be set.

General-Purpose I/O Port Module (GPIO)

General-purpose I/O module enables using external pins as I/O ports. The general-purpose I/O module is composed of 5 GPIO ports. Each GPIO port has 32 channels, which correspond to external pins. For example, the external pin P216 corresponds to the channel 16 setting of the GPIO port 2.

Key code settings are required for writing to registers.

Port Configuration Module (PPC)

The port configuration module sets I/O from/to an external pin. This setting can be set per external pin.

- Output enable display
- I/O status display
- Pull-up setting
- Pull-down setting
- Input level setting
- Output drive capacity setting
- Input disable setting
- Output (GPIO, resource) function selection

Key code settings are required for writing to registers.

Resource Input Configuration Module (RIC)

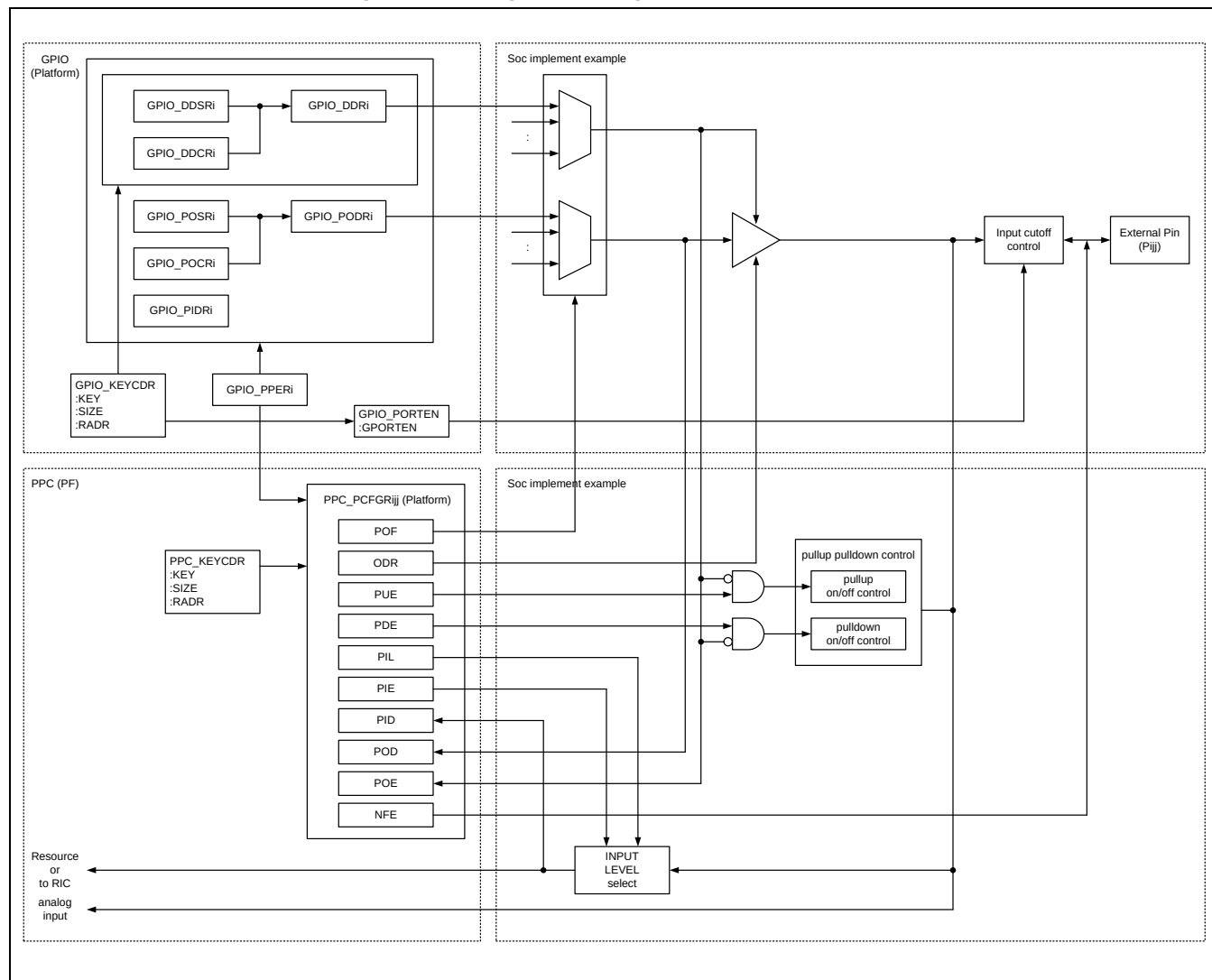
The resource input configuration module selects input from an external pin or output from another internal resource as resource input.

2. Configuration and Block Diagrams

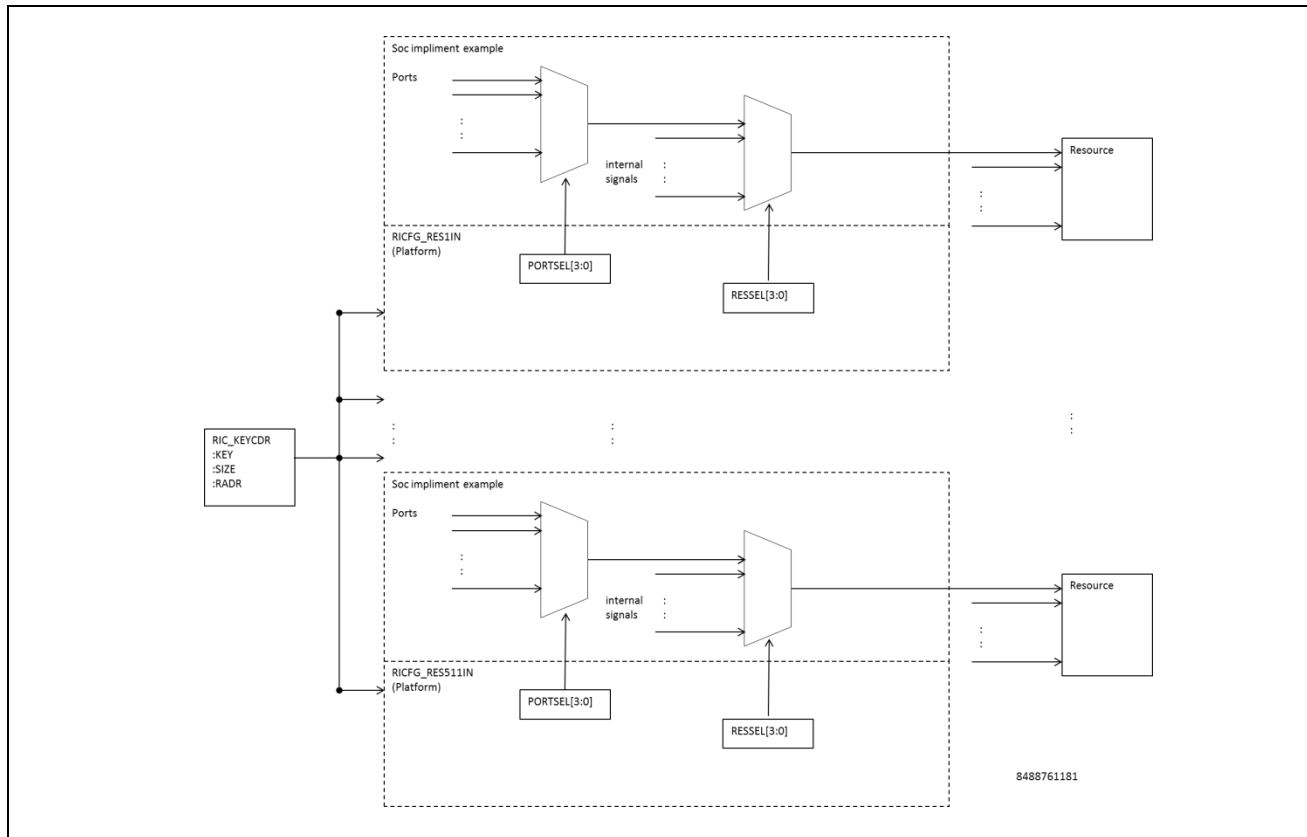
This section describes the block diagram of I/O port.

Figure 2-1 and Figure 2-2 show the I/O port configuration diagrams.

Figure 2-1 Configuration Diagram of GPIO and PPC



Note: GPIO_PPERi is not supported.

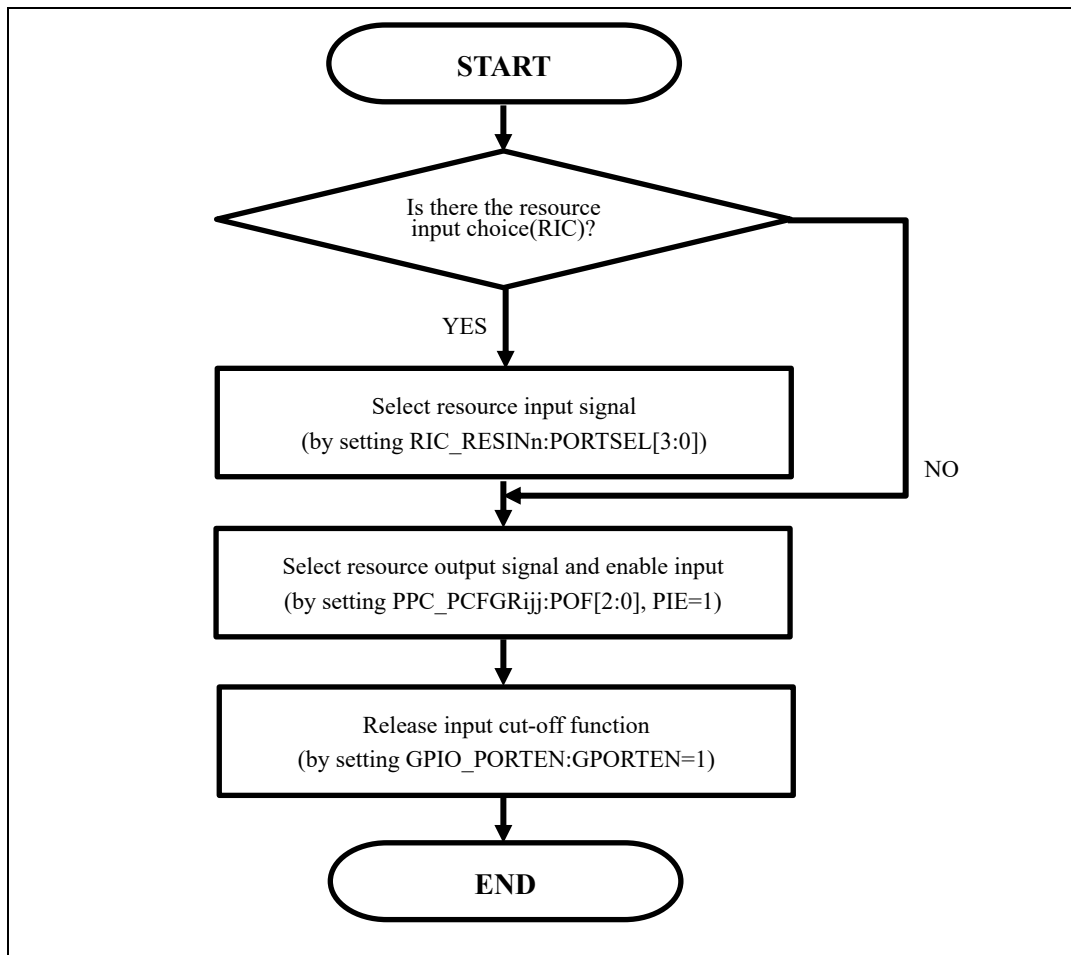
Figure 2-2 Configuration Diagram of RIC

3. Setting Procedure Examples

This section describes the setting procedure examples of I/O port.

Assignment of Resource I/O Pin (Both directions)

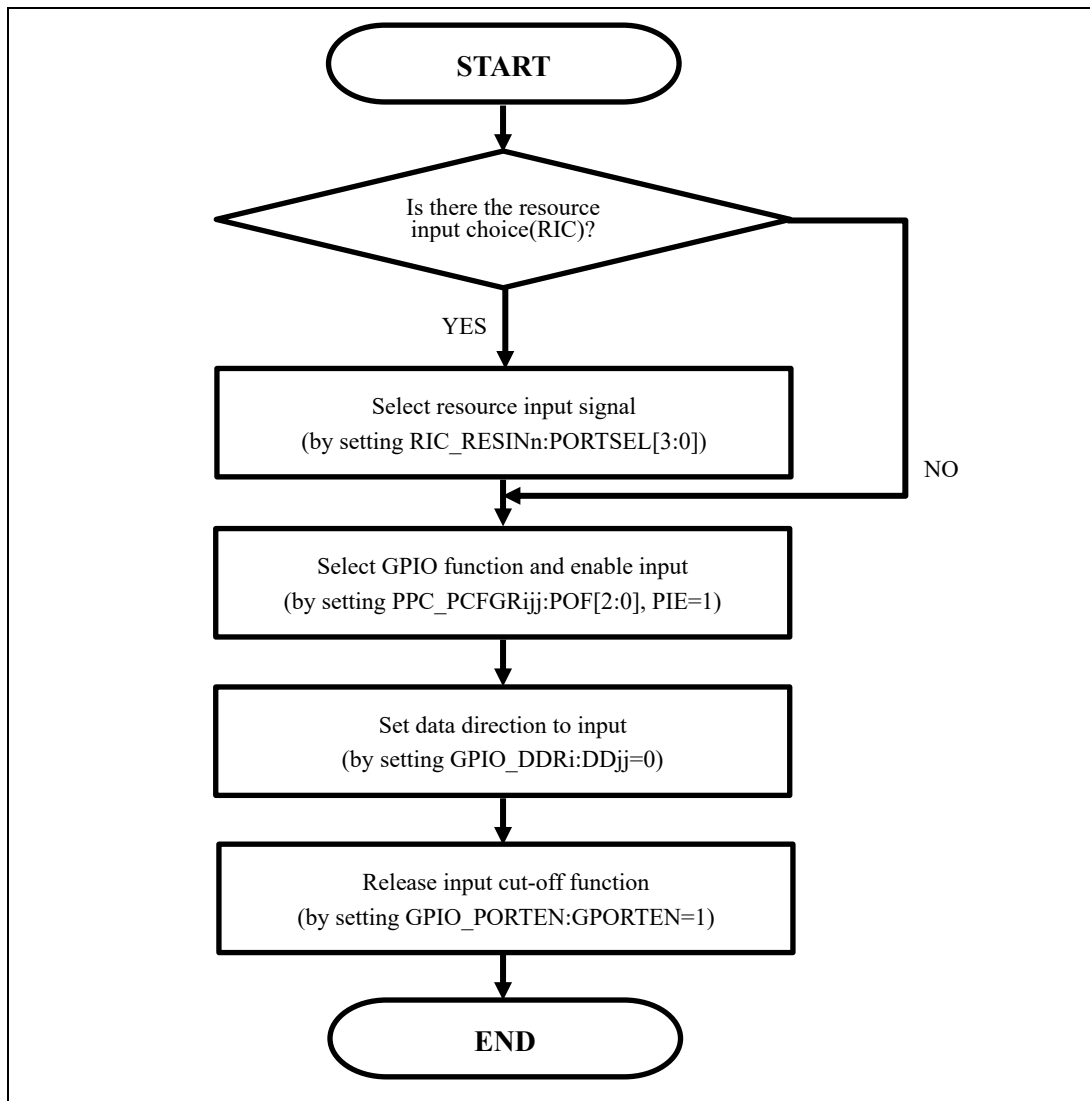
Figure 3-1 Setting Procedure



Notes:

- The following registers are the applicable key code registers.
 - Port enable register (GPIO_PORTEN)
 - Port setting register (PPC_PCFGRIj)
 - Resource Input Setting Register (RIC_RESINn)

Assignment of Resource Input Pin (Selecting the resource input of an external pin)
Figure 3-2 Setting Procedure

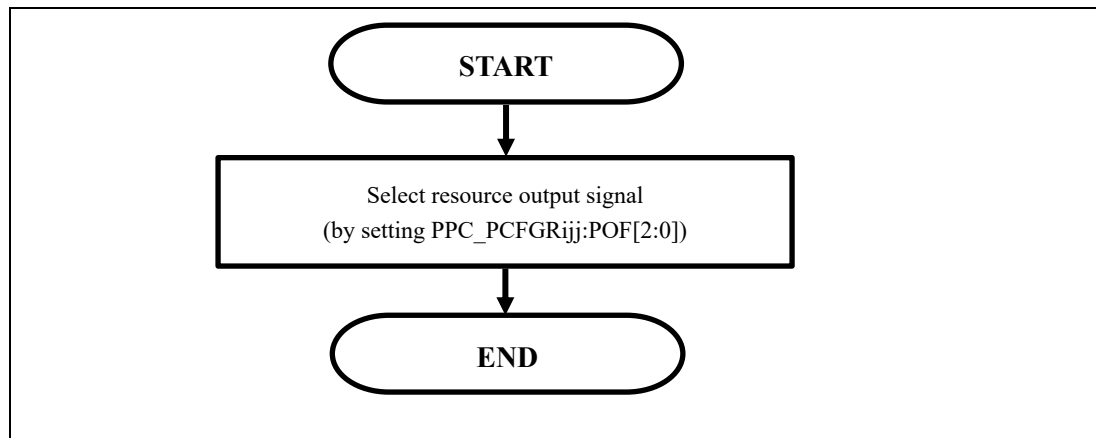


Notes:

- The following registers are the applicable key code registers.
- Data direction register (GPIO_DDRi)
- Port enable register (GPIO_PORTEN)
- Port setting register (PPC_PCFGRijj)
- Resource Input Setting Register (RIC_RESINn)

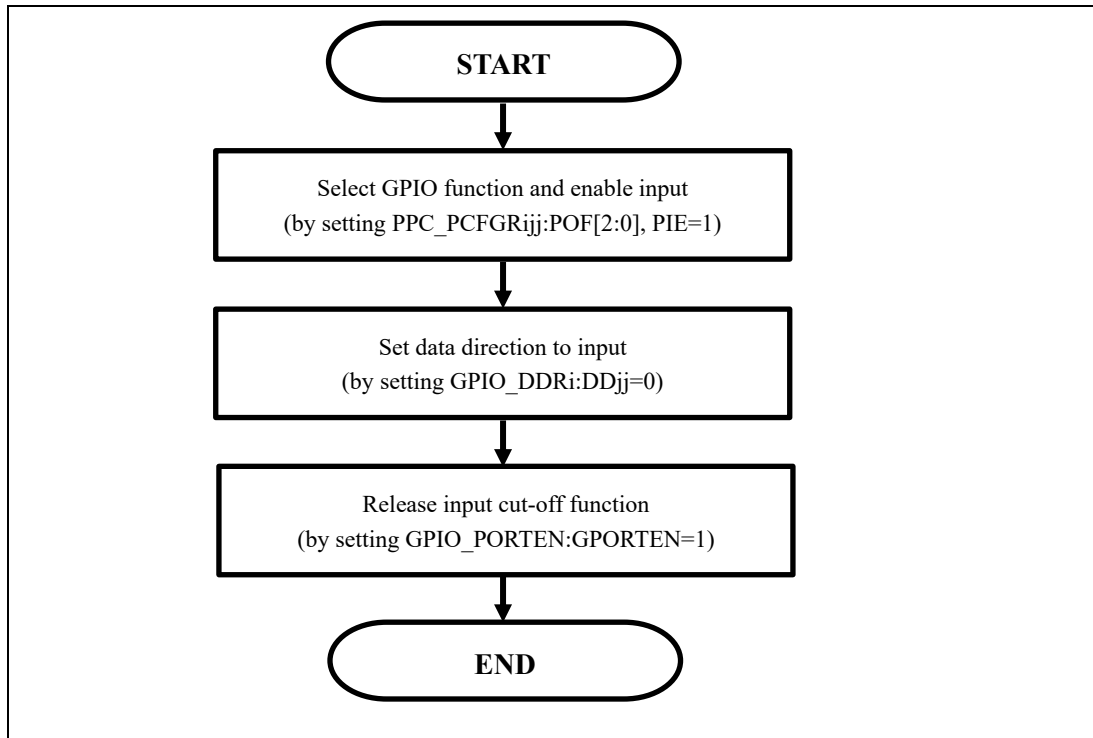
Assignment of Resource Output Pin

Figure 3-3 Setting Procedure



Notes:

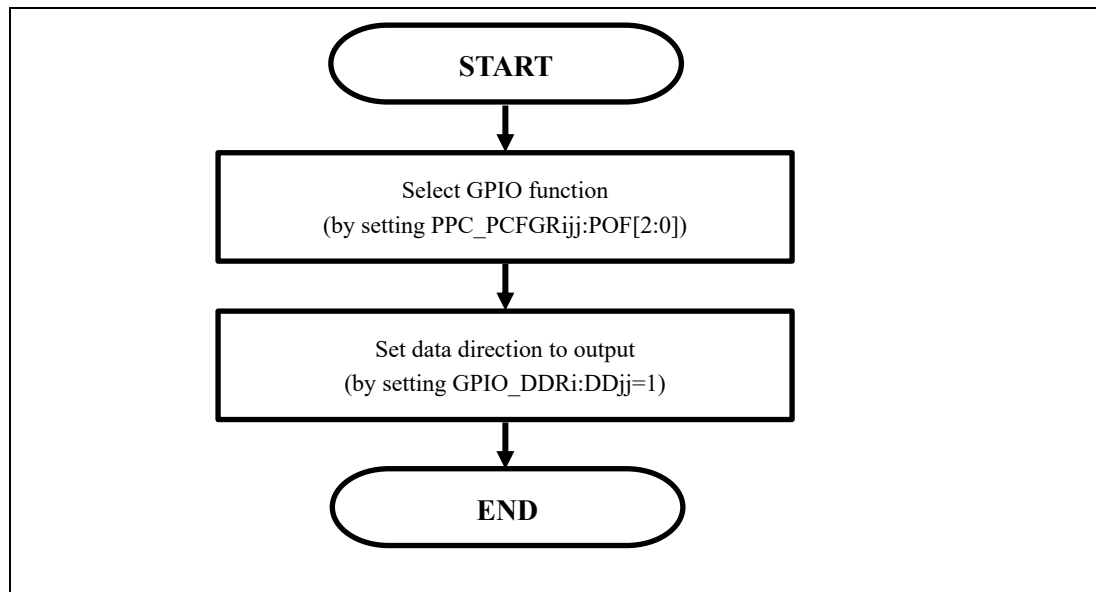
- The following registers are the applicable key code registers.
- Port setting register (PPC_PCFGRijj)

Assignment of Port Function (Input)**Figure 3-4 Setting Procedure****Notes:**

- The following registers are the applicable key code registers.
 - Data direction register (GPIO_DDRI)
 - Port enable register (GPIO_PORTEN)
 - Port setting register (PPC_PCFGRijj)

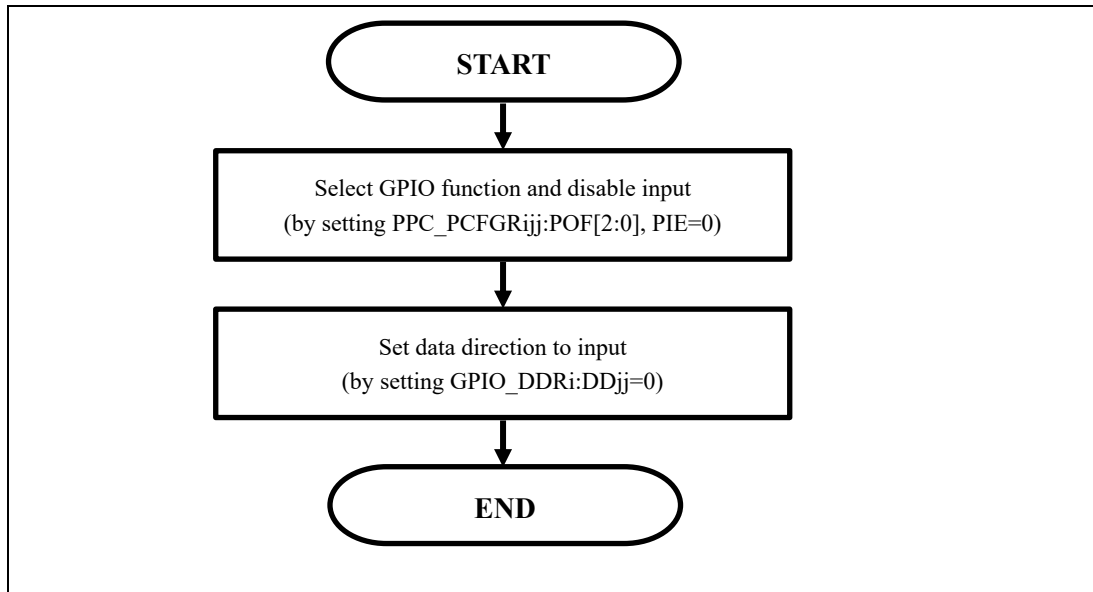
Assignment of Port Function (Output)

Figure 3-5 Setting Procedure



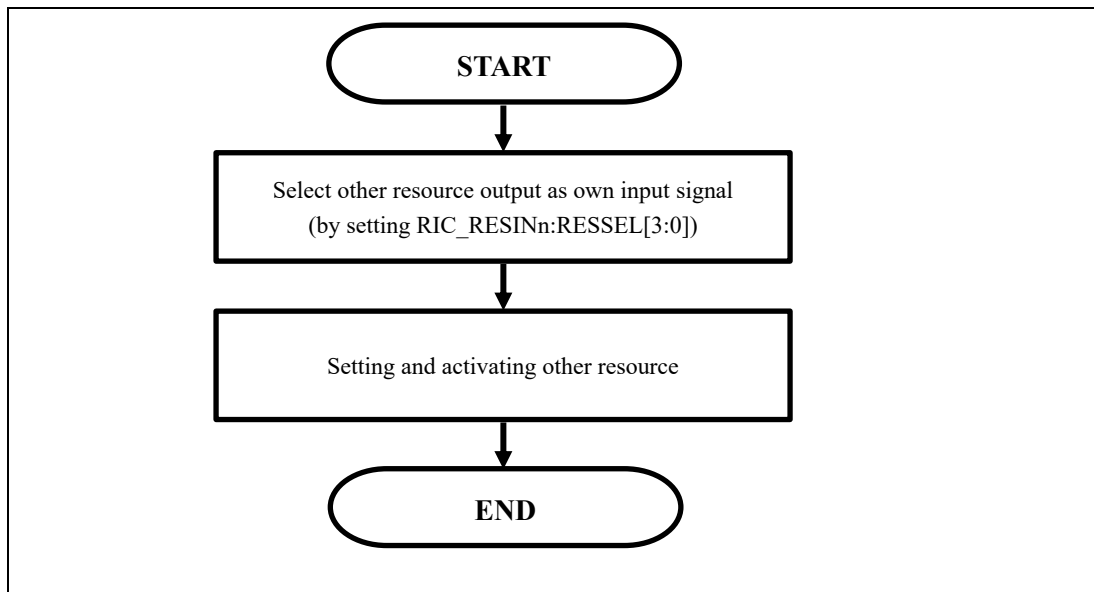
Notes:

- The following registers are the applicable key code registers.
 - Data direction register (GPIO_DDRi)
 - Port setting register (PPC_PCFGRijj)

Assignment of AD Converter Input**Figure 3-6 Setting Procedure****Notes:**

- *The following registers are the applicable key code registers.*
 - Data direction register (GPIO_DDRI)
 - Port setting register (PPC_PCFGRijj)

Resource input selection (selecting other resource output)
Figure 3-7 Setting Procedure



Note:

- For details on resource input selection, see "Resource input configuration of the chapter of "Port Configuration " on this manual.

4. Register List

This section describes the register list of the I/O port.

Table 4-1 I/O Port Register List

Abbreviated Register Name	Register Name	Reference
GPIO_DDRI	Data direction register	4.1
GPIO_DDRI	Data direction set register	4.2
GPIO_DDCRI	Data direction clear register	4.3
GPIO_PODRI	Port output data register	4.4
GPIO_POSRI	Port output set register	4.5
GPIO_POCRI	Port output clear register	4.6
GPIO_PORTEN	Port input enable register	4.7
GPIO_PIDRI	Port input data register	4.8
GPIO_KEYCDR	GPIO key code register	4.9
PPC_PCFGRijj	Port setting register	4.10
PPC_KEYCDR	PPC key code register	4.11
RIC_RESINn	Resource input setting register	4.12
RIC_KEYCDR	RIC key code register	4.13

i: GPIO port number (i = 0 to 4)

jj: GPIO channel number (jj = 00 to 31)

n: Number of selectable resource inputs (n = 0 to 907)

Table 4-2 Register Map of GPIO

Address Offset	Register Name / Initial Value			
	+3	+2	+1	+0
0x00000000	GPIO_POSR0 00000000_00000000_00000000_00000000			
0x00000004	GPIO_POCR0 00000000_00000000_00000000_00000000			
0x00000008	GPIO_DDSR0 00000000_00000000_00000000_00000000			
0x0000000C	GPIO_DDCR0 00000000_00000000_00000000_00000000			
0x00000010	GPIO_POSR1 00000000_00000000_00000000_00000000			
0x00000014	GPIO_POCR1 00000000_00000000_00000000_00000000			
0x00000018	GPIO_DDSR1 00000000_00000000_00000000_00000000			
0x0000001C	GPIO_DDCR1 00000000_00000000_00000000_00000000			
0x00000020	GPIO_POSR2 00000000_00000000_00000000_00000000			
0x00000024	GPIO_POCR2 00000000_00000000_00000000_00000000			
0x00000028	GPIO_DDSR2 00000000_00000000_00000000_00000000			
0x0000002C	GPIO_DDCR2 00000000_00000000_00000000_00000000			
0x00000030	GPIO_POSR3 00000000_00000000_00000000_00000000			
0x00000034	GPIO_POCR3 00000000_00000000_00000000_00000000			
0x00000038	GPIO_DDSR3 00000000_00000000_00000000_00000000			
0x0000003C	GPIO_DDCR3 00000000_00000000_00000000_00000000			
0x00000040	GPIO_POSR4 00000000_00000000_00000000_00000000			
0x00000044	GPIO_POCR4 00000000_00000000_00000000_00000000			
0x00000048	GPIO_DDSR4 00000000_00000000_00000000_00000000			
0x0000004C	GPIO_DDCR4 00000000_00000000_00000000_00000000			
0x00000050 to 000001FC	Reserved			
0x00000200	GPIO_PODR0 00000000_00000000_00000000_00000000			

Address Offset	Register Name / Initial Value			
	+3	+2	+1	+0
0x00000204	GPIO_DDR0 00000000_00000000_00000000_00000000			
0x00000208	GPIO_PODR1 00000000_00000000_00000000_00000000			
0x0000020C	GPIO_DDR1 00000000_00000000_00000000_00000000			
0x00000210	GPIO_PODR2 00000000_00000000_00000000_00000000			
0x00000214	GPIO_DDR2 00000000_00000000_00000000_00000000			
0x00000218	GPIO_PODR3 00000000_00000000_00000000_00000000			
0x0000021C	GPIO_DDR3 00000000_00000000_00000000_00000000			
0x00000220	GPIO_PODR4 00000000_00000000_00000000_00000000			
0x00000224	GPIO_DDR4 00000000_00000000_00000000_00000000			
0x00000228 to 000002FC	Reserved			
0x00000300	GPIO_PIDR0 XXXXXXXX_XXXXXXXX_XXXXXXXX_XXXXXXXX			
0x00000304	GPIO_PIDR1 XXXXXXXX_XXXXXXXX_XXXXXXXX_XXXXXXXX			
0x00000308	GPIO_PIDR2 XXXXXXXX_XXXXXXXX_XXXXXXXX_XXXXXXXX			
0x0000030C	GPIO_PIDR3 XXXXXXXX_XXXXXXXX_XXXXXXXX_XXXXXXXX			
0x00000310	GPIO_PIDR4 XXXXXXXX_XXXXXXXX_XXXXXXXX_XXXXXXXX			
0x00000314 to 37C	Reserved			
0x00000380 to 3FC	Reserved			
0x00000400	GPIO_PORTEN 00000000_00000000_00000000_00000000			
0x00000404	GPIO_KEYCDR 00000000_00000000_00000000_00000000			

Table 4-3 Register Map of PPC

Offset	Register Name / Initial Value			
	+1		+0	
0x00000000 to 0x0000003F	PPC_PCFGR0000 to 0031 00000000_00000000			
0x00000040 to 0x0000007F	PPC_PCFGR0100 to 0131 00000000_00000000			
0x00000080 to 0x000000BF	PPC_PCFGR0200 to 0231 00000000_00000000			
0x000000C0 to 0x000000FF	PPC_PCFGR0300 to 0331 00000000_00000000			
0x00000100 to 0x0000013F	PPC_PCFGR0400 to 0431 00000000_00000000			
0x00000140 to 0x000003FF	Reserved			
Offset	Register Name			
	+3	+2	+1	+0
0x00000400	PPC_KEYCDR 00000000_00000000_00000000_00000000			

Table 4-4 Register Map of RIC

Offset	Register Name			
	+1		+0	
0x00000000 to 0x00000714	RIC_RESINn 00000000_00000000			
0x00000718 to 0x00000FFF	Reserved			
Offset	Register Name			
	+3	+2	+1	+0
0x00001400	RIC_KEYCDR 00000000_00000000_00000000_00000000			

4.1. Data Direction Register (GPIO_DDRI) (i = 0 to 4)

This register sets the I/O direction of a pin. The direction is set when a GPIO is selected by the port output function selection bit (POF[2:0]) of the port setting register (PPC_PCFGRijj). This register can be directly written or can be set/cleared using the data direction set register (GPIO_DDSDi) and the data direction clear register (GPIO_DDCRi).

Bit	31	0
Field	DD	
R/W Attribute	R/W	
Protection Attribute	WS	
Initial Value	00000000_00000000_00000000_00000000	

[bit31:0] DD[n]: Data Direction Selection Bit (n = 0 to 31)

DD[n] n=0 to 31	Description
0	Set data direction to input.
1	Set data direction to output.

Notes:

- This is the applicable key code register. To write to this register, the GPIO key code register (GPIO_KEYCDR) must be set.
- If this register is written before the key code is released, a bus error response is returned.
- After key code release, writing to a different address or using a different access size than specified in the key code sequence will not generate an error response, and it can't write the data correctly.
- Please be sure to read and check a preset value after writing to a GPIO register.

4.2. Data Direction Set Register (GPIO_DDSRi) (i = 0 to 4)

This register is used to set the data direction selection bit (GPIO_DDRi: DD31 to DD0).

Bit	31	0
Field	DDS	
R/W Attribute	R0,W	
Protection Attribute	WS	
Initial Value	00000000_00000000_00000000_00000000	

[bit31:0] DDS[n]: Data Direction Set Bit (n = 0 to 31)

DDS[n] n=0 to 31	Description
0	No effect
1	Set the data direction selection bit (GPIO_DDRi: DD31 to DD0) to "1".

Notes:

- This is the applicable key code register. To write to this register, the GPIO key code register (GPIO_KEYCDR) must be set.
- If this register is written before the key code is released, a bus error response is returned.
- After key code release, writing to a different address or using a different access size than specified in the key code sequence will not generate an error response, and it can't write the data correctly.
- Please be sure to read and check a preset value after writing to a GPIO register.

4.3. Data Direction Clear Register (GPIO_DDCRi) (i = 0 to 4)

The data direction clear (DDC) register is used to clear the corresponding GPIO_DDRi bit.

Bit	31	0
Field	DDC	
R/W Attribute	R0,W	
Protection Attribute	WS	
Initial Value	00000000_00000000_00000000_00000000	

[bit31:0] DDC[n]: Data Direction Clear Register (DDC[n]) (n=0 to 31)

DDC[n] n=0 to31	Description
0	No effect
1	Clear the data direction selection bit (GPIO_DDRi: DD31 to DD0) to "0".

Notes:

- This is the applicable key code register. To write to this register, the GPIO key code register (GPIO_KEYCDR) must be set.
- If this register is written before the key code is released, a bus error response is returned.
- After key code release, writing to a different address or using a different access size than specified in the key code sequence will not generate an error response.
- Please be sure to read and check a preset value after writing to a GPIO register.

4.4. Port Output Data Register (GPIO_PODRi) (i = 0 to 4)

This register is used to set a port output value. The setting value is enabled when a port output is selected (GPIO_DDRi: DD31 to DD0 = 1). This register can be directly written or can be set/cleared using the port output set register (GPIO_POSRi) and the port output clear register (GPIO_POCRi).

Bit	31	0
Field	POD	
R/W Attribute	R/W	
Protection Attribute	-	
Initial Value	00000000_00000000_00000000_00000000	

[bit31:0] POD[n]: Port Output Data Bit (n = 0 to 31)

POD[n] n=0 to 31	Description
0	Output "L".
1	Output "H".

4.5. Port Output Set Register (GPIO_POSRi) (i = 0 to 4)

This register is used to set the port output data bit (GPIO_PODRi: POD31 to POD0).

Bit	31	0
Field	POS	
R/W Attribute	R0,W	
Protection Attribute	-	
Initial Value	00000000_00000000_00000000_00000000	

[bit31:0] POS[n]: Port Output Set Bit (n = 0 to 31)

POS[n] n=0 to 31	Description
0	No effect
1	Set the port output data bit (GPIO_PODRi: POD31 to POD0) to "1".

4.6. Port Output Clear Register (GPIO_POCRI) (i = 0 to 4)

This register is used to clear the port output data bit (GPIO_PODRi: POD31 to POD0).

Bit	31	0
Field	POC	
R/W Attribute	R0,W	
Protection Attribute	-	
Initial Value	00000000_00000000_00000000_00000000	

[bit31:0] POC[n]: Port Output Clear Bit (n = 0 to 31)

POC[n] n=0 to 31	Description
0	No effect
1	Clear the port output data bit (GPIO_PODRi: POD31 to POD0) to "0".

4.7. Port Input Enable Register (GPIO_PORTEN)

This register sets the input rejection of a port.

Bit	31															8														
Field	Reserved																													
R/W Attribute	R0,WX																													
Protection Attribute	WS																													
Initial Value	00000000_00000000_00000000																													

Bit	7				6		5		4		3		2		1		0					
Field	Reserved														Reserved		GPORTEN					
R/W Attribute	R0,WX														R/W0		R/W					
Protection Attribute	WS																					
Initial Value	000000														0		0					

[bit31:1] Reserved: Reserved Bits

[bit0] GPORTEN: Global Input Enable Bit

Bit	Description
0	Disable input to the pin.
1	It is controlled by PIE bit whether the input buffer enabled or not.

Notes:

- This is the applicable key code register. To write to this register, the GPIO key code register (GPIO_KEYCDR) must be set.
- If this register is written before the key code is released, a bus error response is returned.
- After key code release, writing to a different address or using a different access size than specified in the key code sequence will not generate an error response.
- Please be sure to read and check a preset value after writing to a GPIO register.

4.8. Port Input Data Register (GPIO_PIDRi) (i = 0 to 4)

This register indicates an input data value. This register indicates input data according to the setting of the input level selection bit (PPC_PCFGRIj:PIL[1:0]) when the global input enable bit (GPIO_PORTEN:GPORTEN) is "1". An indefinite value is read from the port input data register when the global input enable bit (GPIO_PORTEN:GPORTEN) is "0".

Bit	31	0
Field	PID	
R/W Attribute	R,WX	
Protection Attribute	-	
Initial Value	XXXXXXXX_XXXXXXXX_XXXXXXXX_XXXXXXXX	

[bit31:0] PID[n]: Port Input Data Register (n = 0 to 31)

PID[n] n=0 to31	Description
0	"L" is input.
1	"H" is input.

Note:

- This register is not initialized by Hard Reset (i.e. "X")

4.9. GPIO Key Code Register (GPIO_KEYCDR)

This register sets register writing with a function for protection against erroneous writing. If writing to this register is not done using the prescribed method, writing to the relevant register is invalid. A lock target register can write only once in after unlocking. When writing continuously, please unlock once again.

Bit	31	30	29	28	27	26	25	24
Field	KEY		SIZE		Reserved			
R/W Attribute	R0,W		R0,W		R0,WX			
Protection Attribute	-							
Initial Value	00		00		0000			

Bit	23	22	21	20	19	18	17	16
Field	Reserved							
R/W Attribute	R0,WX							
Protection Attribute	-							
Initial Value	00000000							

Bit	15	14	13	12	11	10	9	8
Field	Reserved	RADR[14:8]						
R/W Attribute	R0,WX	R0,W						
Protection Attribute	-							
Initial Value	0	0000000						

Bit	7	6	5	4	3	2	1	0
Field	RADR[7:0]							
R/W Attribute	R0,W							
Protection Attribute	-							
Initial Value	00000000							

[bit31:30] KEY: Key Code Bits

These are key code setting bits. Write "00", "01", "10", and "11" continuously to these bits in this order. The key code setting becomes invalid immediately upon any writing to these bits in a different order. In such cases, set the key code again from the beginning.

Bits		Description
0	0	1st key code
0	1	2nd key code
1	0	3rd key code
1	1	4th key code

[bit29:28] SIZE: Access Size Bits

These bits set the access size for writing to the applicable key code register. Write the same data to these bits when writing key codes "00", "01", "10", and "11" in this order.

Bits		Description
0	0	Set byte access.
0	1	Set half-word access.
1	0	Set word access.
1	1	Reserved

[bit27:15] Reserved: Reserved Bits

[bit14:0] RADR: Port Address Bits

These bits set the lower 15 bits of the address of the applicable key code register. Write the same data to these bits when writing key codes "00", "01", "10", and "11" in this order.

RADR	Description
-	Set the lower 15 bits of the address of the applicable key code register.

Notes:

- The key code setting becomes invalid upon any writing to the KEY[1:0] in any order than "00", "01", "10", and "11". In such case, set the key code again from the beginning.
- When different data is written to the SIZE[1:0] or the RADR[14:0] while writing the key code "00", "01", "10", and "11", the key code setting will become invalid. In such case, set it again from the beginning.
- The applicable key code registers are the following registers.
 - Data direction register (GPIO_DDRi)
 - Data direction set register (GPIO_DDSDRi)
 - Data direction clear register (GPIO_DDCRi)
 - Port input enable register (GPIO_PORTEN)
- This register is valid only for word access.
- There is no effect on the key code protection release process even if registers other than this register and the applicable key code register that is in the release processing (the register set by the RADR) are accessed while writing the key code "00", "01", "10", and "11".

4.10. Port Setting Register (PPC_PCFGRIjj) (i = 0 to 4, jj = 00 to 31)

This register sets and displays I/O from/to an external pin.

Bit	15	14	13	12	11	10	9	8
Field	POE	POD	PID	PIE	PIL		PUE	PDE
R/W Attribute	R,WX	R,WX	R,WX	R/W	R/W		R/W	R/W
Protection Attribute	WS							
Initial Value	0	0	X	0	00		0	0

Bit	7	6	5	4	3	2	1	0
Field	ODR		NFE	Reserved		POF		
R/W Attribute	R/W		R/W	R0,WX		R/W		
Protection Attribute	WS							
Initial Value	00		0	00		000		

[bit15] POE: Port Output Enable Bit

This bit indicates whether pin output is enabled.

Bit	Description
0	Pin output is high-impedance.
1	Pin output is enabled.

[bit14] POD: Port Output Data Bit

This bit indicates the value outputted to a pin.

Bit	Description
0	Output "L".
1	Output "H".

[bit13] PID: Port Input Data Bit

This bit indicates the value inputted to the pin selected by the input level bit (PIL[1:0]).

This bit is indefinite when the global input enable bit (GPORTEN) is "0".

Bit	Description
0	The pin input is "L".
1	The pin input is "H".

[bit12] PIE: Port Input Enable Bit

This bit sets whether input is enabled or not.

Bit	Description
0	Pin input is disabled or analog input.
1	Pin input is enabled.

[bit11:10] PIL: Input Level Bit

This bit selects a pin input level.

Bits		Description
0	0	Type A
0	1	Type B
1	0	Type C
1	1	Type D

For details, see " Input Level Setting of the chapter of "Port Configuration" on this manual.

[bit9] PUE: Pull Up Enable Bit

This bit sets whether pull-up is performed or not in input status.

Bit	Description
0	No pull up.
1	Pull up.

[bit8] PDE: Pull Down Enable Bit

This bit sets whether pull-down is performed in input status.

Pull up (PUE) has priority over pull down, if pull down and pull up (PUE) are competing.

Bit	Description
0	No pull down.
1	Pull down.

[bit7:6] ODR: Port Output Drive Selection Bit

This bit selects an output drive capacity of a port.

Bits		Description
0	0	Type A
0	1	Type B
1	0	Type C
1	1	Type D

For details, see " Output Drive Capacity Setting of the chapter of "Port Configuration" on this manual.

[bit5] NFE: Port Noise Filter Enable/Disable Select Bit

This bit selects whether to enable or disable the noise filter for the port.

Bit	Description
0	Disable the noise filter.
1	Enable the noise filter.

[bit4:3] Reserved: Reserved Bits**[bit2:0] POF: Port Output Function Selection Bit**

This bit selects a function to output to a port.

Bits			Description
0	0	0	Resource A output
0	0	1	Resource B output
0	1	0	Resource C output
0	1	1	Resource D output
1	0	0	Resource E output
1	0	1	Resource F output
1	1	0	Resource G output
1	1	1	Resource H output

For details, see "Port output function configuration of the chapter of "Port Configuration" on this manual.

Notes:

- This is the applicable key code register. To write to this register, the PPC key code register (PPC_KEYCDR) must be set.
- If this register is written before the key code is released, a bus error response is returned.
- After key code release, writing to a different address or using a different access size than specified in the key code sequence will not generate an error response.
- Please be sure to read and check a preset value after writing to a GPIO register.
- This register is not initialized by Hard Reset (i.e. "X").

4.11. PPC Key Code Register (PPC_KEYCDR)

This register sets register writing with a function for protection against erroneous writing. If writing to this register is not done using the prescribed method, writing to the relevant register is invalid.

Bit	31	30	29	28	27	26	25	24
Field	KEY		SIZE		Reserved			
R/W Attribute	R0,W		R0,W		R0,WX			
Protection Attribute	-							
Initial Value	00		00		0000			

Bit	23	22	21	20	19	18	17	16
Field	Reserved							
R/W Attribute	R0,WX							
Protection Attribute	-							
Initial Value	00000000							

Bit	15	14	13	12	11	10	9	8
Field	Reserved	RADR[14:8]						
R/W Attribute	R0,WX	R0,W						
Protection Attribute	-							
Initial Value	0	0000000						

Bit	7	6	5	4	3	2	1	0
Field	RADR[7:0]							
R/W Attribute	R0,W							
Protection Attribute	-							
Initial Value	00000000							

[bit31:30] KEY: Key Code Bits

These are key code setting bits. Write "00", "01", "10", and "11" continuously to these bits in this order. The key code setting becomes invalid immediately upon any writing to these bits in a different order. In such cases, set the key code again from the beginning.

Bits		Description
0	0	1st key code
0	1	2nd key code
1	0	3rd key code
1	1	4th key code

[bit29:28] SIZE: Access Size Bits

These bits set the access size for writing to the applicable key code register. Write the same data to these bits when writing key codes "00", "01", "10", and "11" in this order.

Bits		Description
0	0	Set byte access.
0	1	Set half-word access.
1	0	Set word access.
1	1	Reserved

[bit27:15] Reserved: Reserved Bits**[bit14:0] RADR: Port Address Bits**

These bits set the lower 15 bits of the address of the applicable key code register. Write the same data to these bits when writing key codes "00", "01", "10", and "11" in this order.

RADR	Description
-	Set the lower 15 bits of the address of the applicable key code register.

Notes:

- The key code setting becomes invalid upon any writing to the KEY[1:0] in any order than "00", "01", "10", and "11". In such case, set the key code again from the beginning.
- When different data is written to the SIZE[1:0] or the RADR[14:0] while writing the key code "00", "01", "10", and "11", the key code setting will become invalid. In such case, set it again from the beginning.
- The applicable key code register is the port setting register (PPC_PCFGRIjj).
- This register is valid only for word access.
- There is no effect on the key code protection release process even if registers other than this register and the applicable key code register that is in the release processing (the register set by the RADR) are accessed while writing the key code "00", "01", "10", and "11".

4.12. Resource Input Setting Register (RIC_RESINn) (n = 0 to 907)

This register selects an external pin input or an output from another internal resource as resource input.

Bit	15	14	13	12	11	10	9	8
Field	Reserved					PORTSEL		
R/W Attribute	R0,WX					R/W		
Protection Attribute	WS							
Initial Value	0000					0000		

Bit	7	6	5	4	3	2	1	0
Field	Reserved				RESSEL			
R/W Attribute	R0,WX				R/W			
Protection Attribute	WS							
Initial Value	0000				0000			

[bit15:12] Reserved: Reserved Bits

[bit11:8] PORTSEL: Resource Selection Bit

This bit selects an input to a corresponding resource.

Bits				Description
0	0	0	0	Source A
0	0	0	1	Source B
0	0	1	0	Source C
0	0	1	1	Source D
0	1	0	0	Source E
0	1	0	1	Source F
0	1	1	0	Source G
0	1	1	1	Source H
1	0	0	0	Source I
1	0	0	1	Source J
1	0	1	0	Source K
1	0	1	1	Source L
1	1	0	0	Source M
1	1	0	1	Source N
1	1	1	0	Source O
1	1	1	1	Source P

For details, see "Resource input configuration of the chapter of "Port Configuration" on this manual.

[bit7:4] Reserved: Reserved Bits**[bit3:0] RESSEL: Resource Selection Bit**

This bit selects an input to a resource.

Bits				Description
0	0	0	0	Source A
0	0	0	1	Source B
0	0	1	0	Source C
0	0	1	1	Source D
0	1	0	0	Source E
0	1	0	1	Source F
0	1	1	0	Source G
0	1	1	1	Source H
1	0	0	0	Source I
1	0	0	1	Source J
1	0	1	0	Source K
1	0	1	1	Source L
1	1	0	0	Source M
1	1	0	1	Source N
1	1	1	0	Source O
1	1	1	1	Source P

For details, see " Resource input configuration of PORT CONFIGURATION ".

Notes:

- The PORTSEL is the applicable key code bit. To write to this bit, the RIC key code register (RIC_KEYCDR) must be set.
- If this bit is written before the key code is released, a bus error response is returned.
- The RESSEL is the applicable key code bit. To write to this bit, the RIC key code register (RIC_KEYCDR) must be set.
- If this bit is written before the key code is released, a bus error response is returned.
- After key code release, writing to a different address or using a different access size than specified in the key code sequence will not generate an error response.
- Please be sure to read and check a preset value after writing to a GPIO register.

4.13. RIC Key Code Register (RIC_KEYCDR)

This register sets register writing with a function for protection against erroneous writing. If writing to this register is not done using the prescribed method, writing to the relevant register is invalid.

Bit	31	30	29	28	27	26	25	24
Field	KEY		SIZE		Reserved			
R/W Attribute	R0,W		R0,W		R0,WX			
Protection Attribute	-							
Initial Value	00		00		0000			

Bit	23	22	21	20	19	18	17	16
Field	Reserved							
R/W Attribute	R0,WX							
Protection Attribute	-							
Initial Value	00000000							

Bit	15	14	13	12	11	10	9	8
Field	Reserved	RADR[14:8]						
R/W Attribute	R0,WX	R0,W						
Protection Attribute	-							
Initial Value	0	0000000						

Bit	7	6	5	4	3	2	1	0
Field	RADR[7:0]							
R/W Attribute	R0,W							
Protection Attribute	-							
Initial Value	00000000							

[bit31:30] KEY: Key Code Bits

These are key code setting bits. Write "00", "01", "10", and "11" continuously to these bits in this order. The key code setting becomes invalid immediately upon any writing to these bits in a different order. In such cases, set the key code again from the beginning.

Bits		Description
0	0	1st key code
0	1	2nd key code
1	0	3rd key code
1	1	4th key code

[bit29:28] SIZE: Access Size Bits

These bits set the access size for writing to the applicable key code register. Write the same data to these bits when writing key codes "00", "01", "10", and "11" in this order.

Bits		Description
0	0	Set byte access.
0	1	Set half-word access.
1	0	Set word access.
1	1	Reserved

[bit27:15] Reserved: Reserved Bits**[bit14:0] RADR: Port Address Bits**

These bits set the lower 15 bits of the address of the applicable key code register. Write the same data to these bits when writing key codes "00", "01", "10", and "11" in this order.

RADR	Description
-	Set the lower 15 bits of the address of the applicable key code register.

Notes:

- The key code setting becomes invalid upon any writing to the KEY[1:0] in any order than "00", "01", "10", and "11". In such case, set the key code again from the beginning.
- When different data is written to the SIZE[1:0] or the RADR[14:0] while writing the key code "00", "01", "10", and "11", the key code setting will become invalid. In such case, set it again from the beginning.
- The applicable key code register is the resource input setting register (RIC_RESINn).
- This register is valid only for word access.
- There is no effect on the key code protection release process even if registers other than this register and the applicable key code register that is in the release processing (the register set by the RADR) are accessed while writing the key code "00", "01", "10", and "11".

5. Precautions for Using This Device

This section describes the precautions necessary when using the I/O port.

A glitch may occur for a brief nanosecond (2 or 3 nanoseconds) when a general-purpose I/O port is switched (from input to output, from output to input, from port function to resource, or from resource to port function).

If this glitch may cause a problem for the system, please write a value to port output data register (GPIO_PODRi) in advance at a level that will not cause a problem.

When a resource input is valid and its assignment is moved to another pin, a trigger which causes resource operation may occur if the pin levels before switching and after switching are different. Therefore, please switch input pins when the resource input function is stopped.

When switching noise filtering on or off, please execute it while resource input function is stopped.

CHAPTER 23: 12/10/8-Bit Analog to Digital Converter



This chapter explains the functions and operations of the 12/10/8-bit A/D Converter.

1. Overview
2. Configuration and Block Diagram
3. Operation of A/D converter
4. Setup procedure examples
5. Registers

CODE: ADC-S6J3400-E2

1. Overview

The A/D Converter converts analog input voltages into digital values. The A/D Converter features eight range comparators, 32 pulse detection units, 32 separate conversion data registers and four multiple conversion channels.

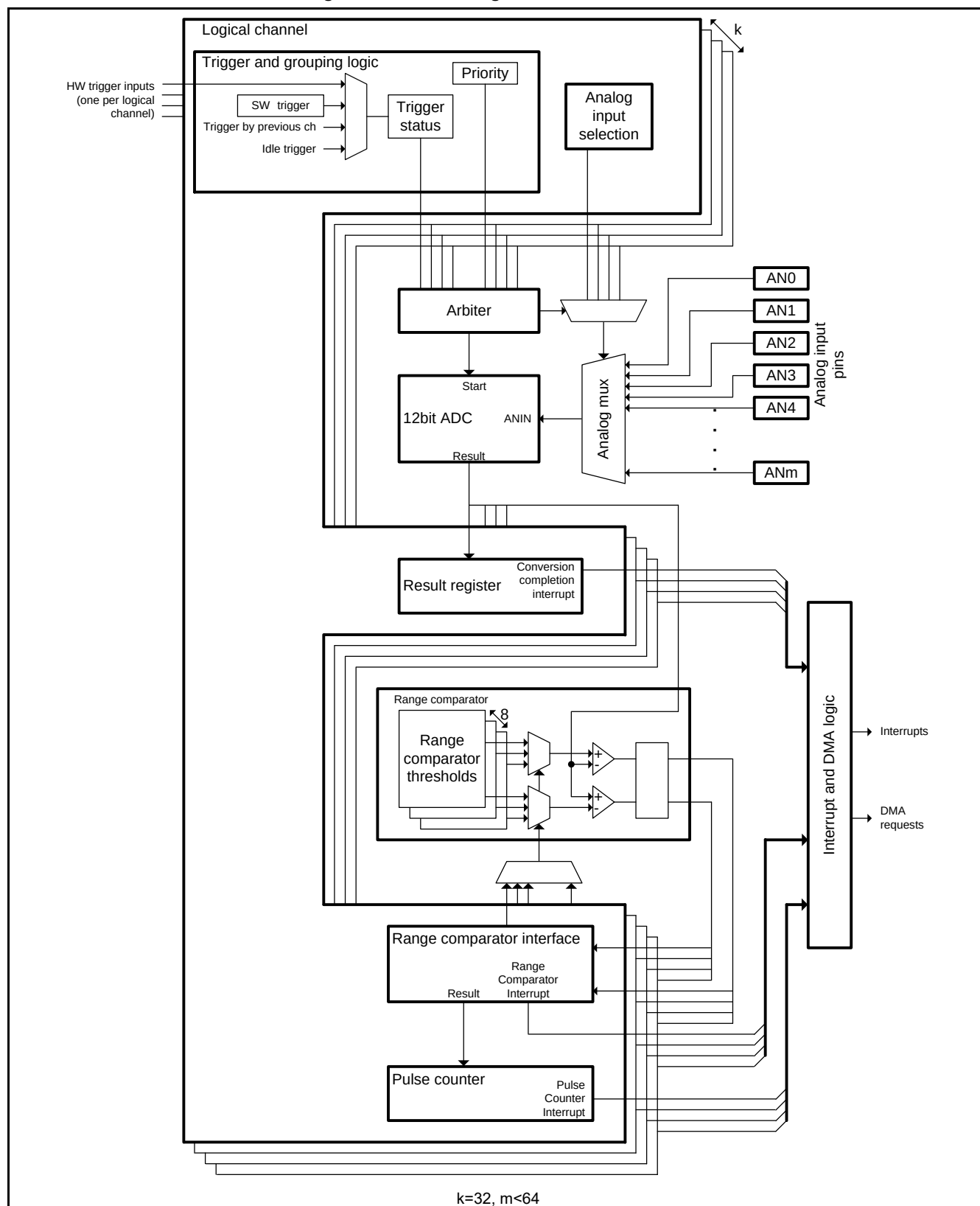
Features of the A/D Converter

- Conversion time: Refer to the datasheet
- 12/10/8-bit resolution
- RC type successive approximation conversion with sample & hold circuit
- Programmable configuration of 32 logical channels by mapping them to analog inputs
 - Each logical channel is mapped to exactly one analog input
 - Several logical channels can be mapped to the same analog input
- 32 dedicated logical channel conversion data registers
- Programmable selection of one of the four global sampling times for each logical channel
- Conversion request for each logical channel i is possible by software trigger only, hardware or software trigger, trigger by conversion completion of the preceding logical channel $i-1$ and idle trigger
- All active conversion requests are compared according to the corresponding logical channel priorities (selectable range is 0-15, 0 is the highest and 15 is the lowest priority) and A/D conversion is started for the logical channel with the highest priority
- When the higher priority conversion requests during an active A/D conversion, it is possible to select the following behavior
 - An active A/D conversion can be interrupted, and the higher priority conversion starts after interrupt operation
 - An active A/D conversion cannot be interrupted, hence the wait time between the higher priority conversion request and its conversion start can be up to the maximum A/D conversion period. In case of multiple conversion channel processing that are configured to be non-interruptible, the wait time can increase to the time needed to the maximum multiple channel conversion period
- The consecutive logical channels can be configured as a group, where the start channel conversion request is set to software trigger only, hardware or software trigger or idle trigger while all other channel conversion requests are set to the preceding logical channel conversion completion
- If a group conversion is interrupted by a higher priority conversion request, after the higher priority request is processed the following group configurations are possible:
 - Resume with the next logical channel in the group
 - Restart with the group start channel or the last converted channel configured as "resume" channel within a group
 - Stop the group processing until next start channel conversion request is issued
- First four logical channels can be configured as:
 - Multiple conversion channels offering the possibility to perform 1 to 16 conversions of the same logical channel and accumulate the result
 - A/D Converter calibration channels providing the configuration for conversion of A/D Converter reference voltages in order to calculate the offset and gain corrections
- Eight range comparators are selectable for every logical channel, comparing the full range (12-bit)/upper 8-bit of the conversion result
- Programmable upper and lower thresholds for each range comparator
- The comparison results will set flags per logical channel, depending on the configuration. Possible configurations are:
 - "Outside range": The flags are set if the A/D result is below the lower OR above the upper threshold

- “Inside range”: The flags are set if the A/D result is above the lower AND below the upper threshold
- The results of the range comparator can be filtered to ignore short spikes
- During an active A/D conversion, it can be forced stop by software
- It is possible to select the operation after A/D conversion finished (and next conversion is not requested)
 - A/D converter goes to idle (power-down) state after A/D conversion finished
 - A/D converter does not go idle (power-down) state, it can start A/D sampling without the resumption time
- Interrupt request generation to CPU is provided for:
 - Conversion done interrupt (end of a logical channel conversion)
 - Group interrupted interrupt (a group processing is interrupted just before the logical channel conversion is to be started or in case of multiple conversion channel before the last conversion is started)
 - Range comparison interrupt
 - Pulse detection interrupt
- Conversion done interrupts of up to four logical channels can trigger DMA requests to transfer the A/D conversion results to memory. The conversion done interrupts of the group last logical channels are good candidates for DMA burst setup, since the group result registers can be read linearly
- Debug mode provides the possibility to freeze further A/D conversion processing at the end of the current conversion

2. Configuration and Block Diagram

This section shows a block diagram of A/D converter.

Figure 2-1 Block Diagram of A/D Converter


3. Operation of A/D Converter

A/D Converter operates using the successive approximation method with 12-bit or 10-bit or 8-bit resolution. There is one A/D Conversion Data Register per logical channel which is updated each time the assigned logical channel is converted. First four logical channels can be configured as multiple conversion channels or used for A/D Converter calibration.

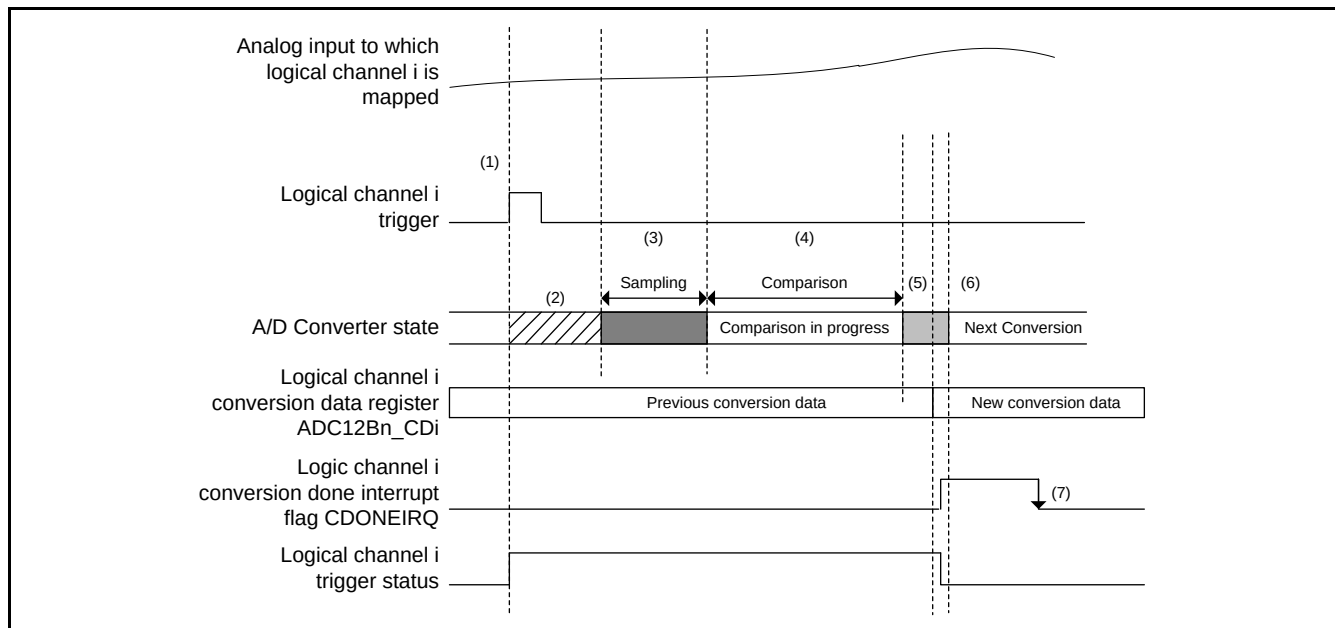
The range comparator compares the converted values with the configured values in the threshold registers and accordingly generates an interrupt for "inside range" or "outside range", depending on the configuration. Any of eight range comparators can be configured for any of 32 logical channels.

A/D Pulse Detection function detects events of desired length and also filters parasitic inverted events. Each logical channel has a dedicated pulse detection function.

3.1. A/D Conversion Flow

The basic A/D conversion flow is shown on Figure 3-1.

Figure 3-1 A/D Conversion Flow



The important steps marked on the figure are:

- (1) A/D conversion request (trigger) is issued for particular logical channel i and the corresponding trigger status is set.
- (2) Period between the trigger and actual conversion start depends on current A/D Converter state condition
 - If A/D Converter is in idle (power-down) state (power-down mode is enabled (ADC12Bn_CTRL.PDDMD = "0")) i.e. there are no trigger status set at the moment the trigger is issued, it is first waited until the resumption time (configured as A/D converter resumption time register (ADC12Bn_RT)) elapses. At the end of resumption time, the priority arbiter compares the priorities of all logical channels with set trigger status and inactive data protection feature. The

conversion of the logical channel *i* start when this channel wins the arbitration, i.e. after all logical channels with higher priority are converted.

- If A/D converter is active at the moment the trigger is issued, the operation is dependent on the setting of forced stop mode (ADC12Bn_CTRL.FSMD).
 - Forced stop is enabled (ADC12Bn_CTRL.FSMD = "1"): Even if the sampling phase is started, an active A/D conversion can be interrupted. So, the logical channel *i* starts after interrupt operations instead of currently performed conversion when this channel wins the priority arbitration.
 - Forced stop is disabled (ADC12Bn_CTRL.FSMD = "0"): The conversion of the logical channel *i* starts when this channel wins the priority arbitration and currently performed conversion is finished, since an A/D conversion cannot be interrupted once its sampling phase is started. Accordingly, even if the logical channel *i* has the highest priority, in worst case it can happen that its conversion is delayed by the maximum configured time needed to convert one logical channel (including the case of multiple conversion channel that cannot be interrupted).

(3) Sampling period. A/D converter internal input signal level goes to the level of the analog input to which the logical channel *i* is mapped.

(4) A/D Comparison.

(5) A/D conversion finalization period. The conversion result is stored in the dedicated conversion data register ADC12Bn_CD*i*, the conversion done interrupt flag is set and the trigger status is cleared.

(6) Started next conversion of the logical channel with the highest priority at the moment. If there is no trigger for any logical channel, the operation is dependent on the setting of power-down disable mode (ADC12Bn_CTRL.PDDMD).

- Power down disable mode (ADC12Bn_CTRL.PDDMD = "1"): Even if the A/D conversion is finished (and next conversion is not requested), A/D converter does not go idle (power-down) state. It can start A/D sampling without A/D converter resumption time.
- Power down enable mode (ADC12Bn_CTRL.PDDMD = "0"): A/D converter goes to idle (power-down) state after A/D conversion finished (and next conversion is not requested).

If the trigger status of any logical channel is already set, next conversion is started without A/D converter resumption time.

(7) After the conversion data register (ADC12Bn_CD*i*) is read or by writing "1" to the corresponding conversion done interrupt clear bit (ADC12Bn_CDONEIRQC0.CDONEIRQC*i*), the conversion done interrupt flag is cleared.

In case A/D Converter reconfiguration takes place during operation (A/D Converter is not in power-down state), the following rules are to be obeyed:

- Do not reconfigure logical channels belonging to the group that is currently converted.
- Set the trigger types (ADC12Bn_CHCTRL0~31.TRGTYP[1:0]) of the logical channels affected by the reconfiguration to software trigger only ("00" setting).
- Clear all the trigger status flags (ADC12Bn_TRGST0.TRGST and ADC12Bn_CHSTAT0~31.TRGST) of the affected logical channels, by writing "1" to the corresponding bits of ADC12Bn_TRGCL0 (or ADC12Bn_CHCTRL0~31.TRGCL) registers.
- Reconfigure the logical channels.

3.2. Logical Channel Mapping to Analog Input Signals

32 logical channels are mapped to analog input signals that need to be converted into the digital values. The mapping is done over ADC12Bn_CHCTRL0~31.ANIN configuration fields in the way that ANIN value controls the number of the analog input signal AN, that is propagated to the A/D Converter input in case the logical channel is converted.

Figure 3-2 illustrates an example of possible logical channel mapping to analog inputs. Each logical channel is mapped to exactly one analog input and it is allowed to map several logical channels to the same analog input (logical channels 4, 5, 6 and 30 are mapped to the analog input AN8).

Figure 3-2 Example of Logical Channel Mapping to Analog Inputs

Example of logical channel mapping to analog inputs															
Logical channel number	0	1	2	3	4	5	6	7	...	26	27	28	29	30	31
ANIN bit field setting	30	14	31	0	8	8	8	16	...	1	2	3	28	8	...
Analog input signal	AN30	AN14	AN31	AN0	AN8	AN8	AN8	AN16	...	AN1	AN2	AN3	AN28	AN8	AN...

The described way of logical channel organization provides following benefits:

- Configurable grouping and consecutive conversion of channels independent on physical pin order.
- Mapping of several logical channels to the same analog input allows repetitive conversion of the same analog input with only one interrupt at the end.

3.3. Logical Channel Data Protection Function

Every logical channel has its own conversion data register ADC12Bn_CD. They are written by hardware at the end of conversion of the dedicated channel. The CPU can read the data registers any time. If a conversion is finished and the data of the previous conversion of the same channel has not been read out, previous data could be overwritten and previous conversion result lost. To avoid this, the data protection function can be enabled so that the next conversion of this logical channel is not started until the previous data has been read out. The data protection function is controlled by the corresponding ADC12Bn_CHCTRL0~31.DP bits:

- If for some logical channel the dedicated ADC12Bn_CHCTRLi.DP bit is equal to "0", then conversion is continued and former conversion data are overwritten.
- In case of a regular logical channel, if the dedicated ADC12Bn_CHCTRLi.DP bit is equal to "1" and conversion done interrupt flag is set to "1", this logical channel cannot be selected for the conversion even though its trigger status may be set. The channel can be selected for conversion again after its conversion done interrupt flag has been cleared, e.g. by reading the conversion data register.
- In case of a multiple conversion logical channel, the channel cannot be selected for conversion until its conversion done interrupt flag or group interrupted interrupt flag have been cleared.
 - if the dedicated DP bit is equal to "1" and conversion done interrupt flag is set to "1".
 - if the dedicated DP bit is equal to "1", group interrupted interrupt flag is set to "1", group interrupted interrupt is enabled and multiple conversions are already started.

Note:

1. *It should set DP to "1" only for the logical channels configured as a group (for details about group configuration please see section "Group processing" in chapter "3. Operation of A/D ") having all its logical channels set to "Resume" (ADC12Bn_CHCTRL0~31.RSMRST = "01"). In case of other group configurations:*
 - *"Restart" setting (ADC12Bn_CHCTRL0~31.RSMRST = "10") - the group may be restarted before the conversion done interrupt of the last channel in the group (meaning the interrupt that indicates that the conversion of the entire group has been completed) is asserted, so the CPU does not know that there is already a result available in this channel.*
 - *"Stop" setting (ADC12Bn_CHCTRL0~31.RSMRST = "00") - with the group interrupted interrupt enabled, it could be possible for the CPU to clear the conversion done interrupt flags of the affected channels, but the use case of both "Stop" and "Restart" is that the results of an interrupted group are not interesting, so they do not need to be protected.*
2. *For groups consisting of only one multiple conversion channel, it should use DP as follows:*
 - *"Resume" setting (ADC12Bn_CHCTRL0~31.RSMRST = "01") - when setting DP to "1", disable the group interrupted interrupt (set the corresponding ADC12Bn_GRP_IRQE0.GRPIRQE0~3 to "0"): The conversion result will be protected only after all conversions of the multiple conversion channel have been performed.*
If the corresponding ADC12Bn_GRP_IRQE0.GRPIRQE0~3 is set to "1", then the conversion result will be protected at the time the channel is interrupted, and the conversions will not be resumed before the group interrupted interrupt flag has been cleared. When the conversion is resumed, the conversion counter is reset and first conversion is started. It means the multiple conversion cannot resume from the interrupted state.
 - *"Restart" setting (ADC12Bn_CHCTRL0~31.RSMRST = "10") - when setting DP to "1", disable the group interrupted interrupt (set the corresponding ADC12Bn_GRP_IRQE0.GRPIRQE0~3 to "0"): The conversion result will be protected only after all conversions of the multiple conversion*

channel have been performed. Even if the corresponding ADC12Bn_GRP_IRQE0_GRP_IRQE0~3 is set to "1", the conversion result will be protected only after all conversions of the multiple conversion channel have been performed.

- *"Stop" setting (ADC12Bn_CHCTRL0~31.RSMRST = "00") - when setting DP to "1", enable the group interrupted interrupt (set the corresponding ADC12Bn_GRP_IRQE0_GRP_IRQE0~3 to "1"): The conversion result will be protected when the channel is interrupted or when all conversions have been completed.*

3.4. Logical Channel Triggering and Priority

Each logical channel has the configuration bit field ADC12Bn_CHCTRL0~31.TRGTYP[1:0], controlling the way a conversion request (trigger) can be issued. The following settings are possible:

- Software trigger only (TRGTYP = "00") - in order to set the dedicated trigger status flags (ADC12Bn_CHSTAT0~31.TRGST and ADC12Bn_TRGST0.TRGST) the corresponding software trigger bit (ADC12Bn_CHCTRL0~31.SWTRG) must be set to "1".
- Hardware or software trigger (TRGTYP = "01") - the corresponding trigger status flags can be set not only through software trigger bit, but also in case of the rising edge event on dedicated hardware trigger input.
- Trigger by completion of the preceding logical channel (TRGTYP = "10") - the trigger status flags are set only at the end of preceding logical channel conversion, i.e. updating of conversion data register ADC12Bn_CD of the preceding channel triggers this channel if the trigger status flags of the preceding channel are still set. This allows combining several consecutive logical channels into a group that will be sequentially converted after the start channel is triggered. To configure a group, the start channel trigger type is set to software trigger only, hardware or software trigger or idle trigger, while all other channel trigger types are set to the preceding logical channel conversion completion. It does not make sense to configure the first logical channel to trigger type 2, since the channels would never be triggered.
- Idle trigger (TRGTYP = "11") - the trigger status flags are set whenever there is no active conversion request, i.e. there is no logical channel having trigger status flag set and inactive data protection function. Accordingly, trigger status flags of all logical channels with idle trigger type are set at the same time. The further processing depends on their priority. The idle trigger type allows to form a regular group (the start channel is set to idle trigger and consecutive channels have preceding channel completion trigger type).

Once the logical channel trigger status is set to "1", the channel priority (bit fields ADC12Bn_CHCTRL0~31.CHPRI) configures the conversion order of logical channels with the inactive data protection function. In case of the same priority, active trigger status and inactive data protection function, the logical channel having lower number wins the priority arbitration. The priority can be set in the range 0 - 15. The setting 0 (CHPRI = "0000") is the highest priority, whereas the lowest possible priority setting is 15 (CHPRI = "1111").

Forced stop mode is enabled (ADC12Bn_CTRL.FSMD = "1"):

When the higher priority conversion was requested during an active A/D conversion, the operation of interrupt is dependent on the setting of the channel priority (ADC12Bn_CHCTRL0~31.CHPRI) only.

- If the priority value (CHPRI) of the requested channel is lower than active channel, it can be interrupted and the conversion of the channel with the higher priority is started.

- If the priority value (CHPRI) is higher or same, it cannot be interrupted.

Figure 3-3 Example of Logical Channel Priority Configuration

Logical channel number	0	1	2	3	4	5	6	7	...	26	27	28	29	30	31
CHPRI bit field setting	0	12	13	5	1	6	3	10	...	1	2	3	14	15	15
Data protection function	1	0	0	0	0	0	0	0	...	0	1	0	0	0	0
Trigger status flag	1	1	1	0	1	0	0	1	...	1	0	1	1	1	1

The example on Figure 3-3 would result in following priority arbitration and corresponding logical channel conversion sequence:

(1) Logical channel 4.

Logical channel 0 has higher priority, but its data protection function is active.

(2) Logical channel 26.

This logical channel has the same priority as logical channel 4, but it is converted as second since its number is higher.

(3) Logical channel 28.

Although the channel 27 has higher priority, its trigger status is not set and even the data protection is active. Moreover, logical channel 6 has the same priority and even lower number, but its trigger status is not set.

(4) Logical channel 7.

Even though the logical channels 3 and 5 have higher priority, their trigger status is not set.

(5) Logical channel 1.

(6) Logical channel 2.

(7) Logical channel 29.

(8) Logical channel 30.

It has lower number than the channel 31.

(9) Logical channel 31.

3.5. Group Processing

A group is defined by the trigger type configuration of consecutive logical channels. The first channel of the group has the trigger type set to software trigger only, hardware or software trigger or idle trigger. If the following channel trigger type is not set to preceding logical channel conversion completion, the group consists of only one channel. Otherwise, the group continues until the last channel in a row having trigger type set to preceding logical channel conversion completion. After the first channel of the group is triggered and converted, automatically the second channel is triggered and so on until the whole group is converted.

Figure 3-4 Group Configuration Examples

a)							b)						
Group	1			2			Group	1			2		
Channel	0	1	2	3	4	5	Channel	0	1	2	3	4	5
Priority	7	8	9	1	2	3	Priority	4	3	3	6	5	5
Trigger type	1	2	2	1	2	2	Trigger type	1	2	2	0	2	2

c)							d)						
Group	1			2	3		Group	x					
Channel	0	1	2	3	4	5	Channel	0	1	2	3	4	5
Priority	0	2	2	0	15	14	Priority	0	2	2	0	14	15
Trigger type	1	2	2	0	3	2	Trigger type	2	2	2	0	2	2

Figure 3-4 shows some possible group configurations:

a) In the example two groups are configured, the group 1 consists of logical channels 0, 1 and 2 and the group 2 includes logical channels 3, 4 and 5. If both groups are triggered (trigger status is set for the starting channels 0 and 3), the group 2 would be converted first due to higher priority setting. Since the first channel in the groups has the highest priority, the groups are "re-triggerable" (if the next starting channel trigger appears before the group conversion is finished, the conversion of the group would be restarted).

b) Here the first channel of the groups has a lower priority then the remaining channels within the groups, hence it is not possible to re-trigger the group processing. The processing of the group 2 can be started only by the software trigger of the logical channel 3. The group 1 allows the triggering by the software or hardware trigger of the channel 0.

c) This example contains three groups, where the group 2 consists of only one logical channel 3. The group 3 shows the configuration of the group starting with the idle trigger type, i.e. the trigger status of the logical channel 4 is set to "1" if there is no logical channel having trigger status flag set and inactive data protection function.

d) In this case first three logical channels are set to trigger type 2 and since there will be no event of preceding channel conversion completion, the logical channels 0, 1 and 2 will never be converted.

Between the different groups (the group 1, the group 2): the priority of all the logical channels should be configured as [the group 1 > the group 2] or [the group 1 < the group 2].

(Example: When the priorities of all the channels included in the group 1 are set as 7-9, all the channels of the group 2 should be set lower (or higher) than 7-9.)

After a group processing is started (at least the conversion of the first channel of the group is started), it can be interrupted.

Forced stop mode is enabled (ADC12Bn_CTRL.FSMD = "1"): If the triggered channel is higher priority than the current channel in the group, current conversion of group processing is interrupted after interrupt operation and the conversion of the channel with the higher priority is started.

Forced stop mode is disabled (ADC12Bn_CTRL.FSMD = "0"): If an A/D conversion is already started, it cannot be stopped. Hence if the triggered channel is higher priority than the next channel in the group, the group processing is interrupted before the conversion start of the next logical channel in the group.

The configuration bit fields ADC12Bn_CHCTRL0~31.RSMRST define how the group processing is to be continued after the higher priority conversion requests are executed. Note that RSMRST setting of the first channel in the group does not matter, since the group cannot be interrupted before the conversion of its first channel started.

If stop group setting (RSMRST[1:0] = "00") is configured for a logical channel and the group is interrupted just before conversion start of that channel, the current processing of the group is stopped. Consequently, the trigger status flag of the logical channel (set by the conversion completion of the preceding channel in the group) is cleared.

Figure 3-5 shows an example of stopping a group processing.

- (1) Logic channel 0 trigger is issued and processing of the group 0 is initiated.
- (2) Processing of the group 0, conversion of logical channels 0 -> 1 -> 2 -> start of channel 3 conversion.
- (3) Logic channel 6 trigger is issued during the conversion of channel 3.
- (4) The operation is dependent on the setting of forced stop mode (ADC12Bn_CTRL.FSMD).

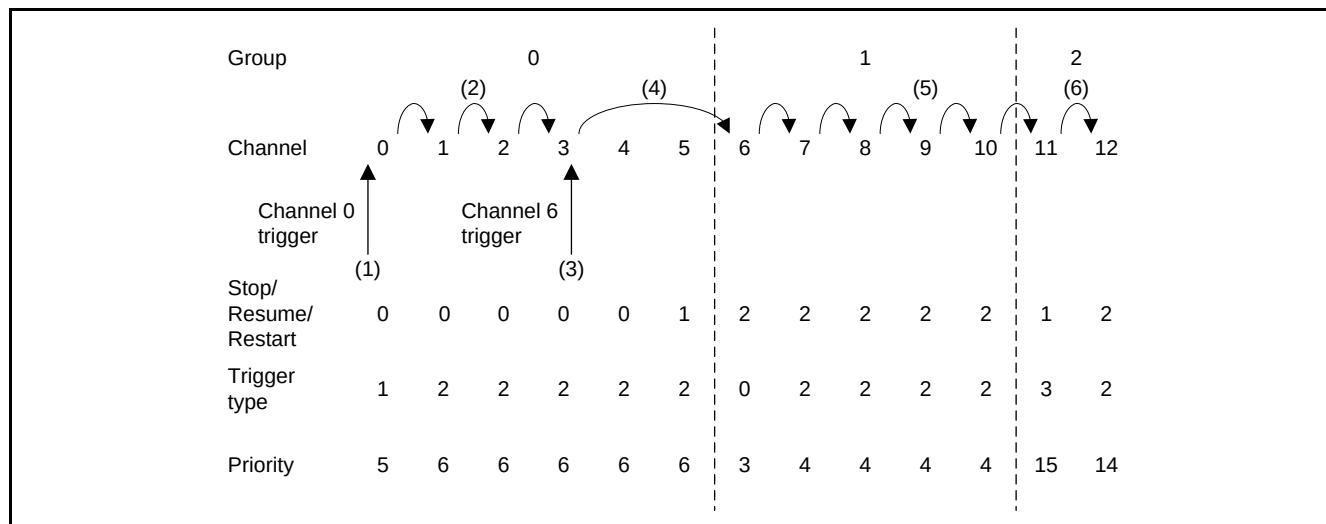
Forced stop mode is enabled (ADC12Bn_CTRL.FSMD = "1"):

Since the priority of the channel 6 is higher than priority of the channel 3, the processing of the group 0 is interrupted during the conversion of channel 3. After interrupted operation, processing continues with the conversion of the channel 6.

Forced stop mode is disabled (ADC12Bn_CTRL.FSMD = "0"):

Since the priority of the channel 6 is higher than priority of the channel 4, the processing of the group 0 is interrupted after the conversion of channel 3 is finished. Moreover, the trigger status flag of the channel 4 is cleared and processing continues with the conversion of the channel 6.

- (5) Group 1 is converted.
- (6) Idle trigger group 2 is converted. Group 0 will not be processed until next channel 0 trigger appears.

Figure 3-5 Stopping of the Group Processing

Resume group setting (RSMRST[1:0] = "01") for a logical channel means that if the group is interrupted, the current processing of the group will be resumed with this channel after higher priority conversions are done.

When the channel which is configured as resume (ADC12Bn_CHCTRL0~31.RSMRST = "01") is in interrupted operation, group interrupted interrupt flag (corresponding bits of ADC12Bn_CHSTAT0~31.GRPIRQ and ADC12Bn_GRPIRQ0.GRPIRQ) is set to "1" whenever converting of other channel occurred.

Figure 3-6 shows an example of resuming a group processing (Forced stop mode is enabled (ADC12Bn_CTRL.FSMD = "1")).

Figure 3-7 shows an example of resuming a group processing (Forced stop mode is disabled (ADC12Bn_CTRL.FSMD = "0")).

- (1) Logic channel 0 trigger is issued and processing of the group 0 is initiated.
- (2) Processing of the group 0, conversion of logical channels 0 -> 1 -> 2 -> start of channel 3 conversion.
- (3) Logic channel 6 trigger is issued during the conversion of channel 3.
- (4) The operation is dependent on the setting of forced stop mode (ADC12Bn_CTRL.FSMD).
 Forced stop mode is enabled (ADC12Bn_CTRL.FSMD = "1", Figure 3-6):
 Since the priority of the channel 6 is higher than priority of the channel 3, the processing of the group 0 is interrupted during the conversion of channel 3.
 Forced stop mode is disabled (ADC12Bn_CTRL.FSMD = "0", Figure 3-7):
 Since the priority of the channel 6 is higher than priority of the channel 4, the processing of the group 0 is interrupted after the conversion of channel 3 is finished.
- (5) Group 1 is converted.
- (6) The operation is dependent on the setting of forced stop mode (ADC12Bn_CTRL.FSMD).
 Forced stop mode is enabled (ADC12Bn_CTRL.FSMD = "1", Figure 3-6):

After group 1 is finished, processing of group 0 is continued with conversion of channel 3 since its trigger status flag is still set.

Forced stop mode is disabled (ADC12Bn_CTRL.FSMD = "0", Figure 3-7):

After group 1 is finished, processing of group 0 is continued with conversion of channel 4 since its trigger status flag is still set.

(7) At the end of group 0 processing, idle trigger group 2 is converted.

Figure 3-6 Resuming of the Group Processing
(Forced stop mode is enabled (ADC12Bn_CTRL.FSMD = "1"))

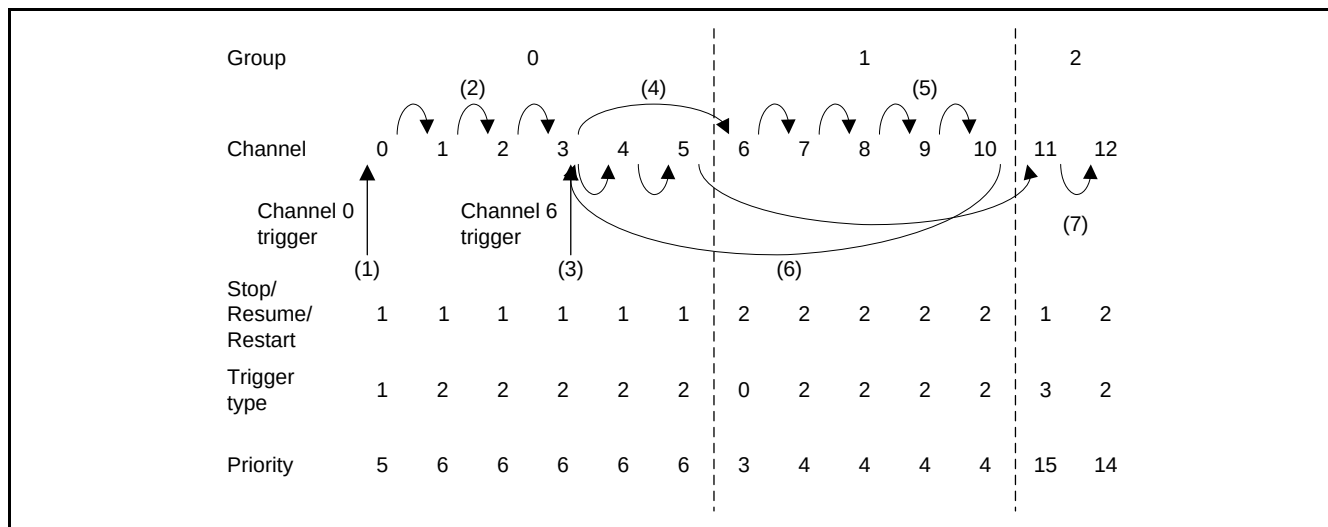
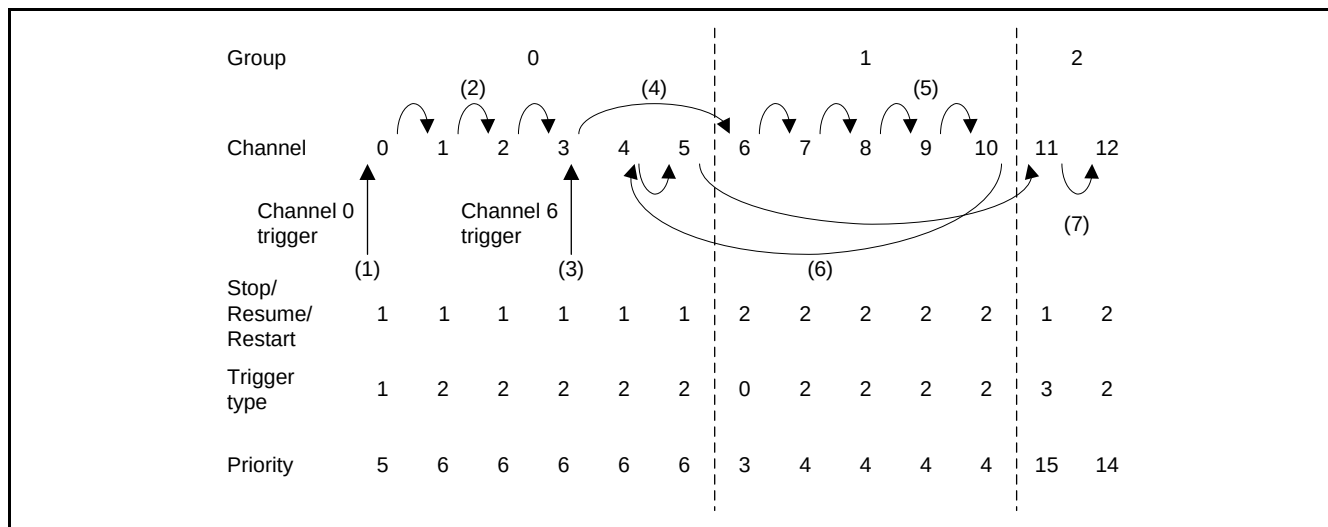


Figure 3-7 Resuming of the Group Processing
(Forced stop mode is disabled (ADC12Bn_CTRL.FSMD = "0"))



Restart group setting (RSMRST[1:0] = "10") for a logical channel configures that if the group is interrupted, its trigger status is cleared and the processing of the group will be restarted after higher priority conversions are done:

- with the closest previous channel of the group set to resume (RSMRST = "1"), accordingly the trigger status flag of that channel is set
- with the first channel of the group (consequently, the trigger status flag of the first channel is set) if there are no previous channels set to resume.

Figure 3-8 shows an example of restarting a group processing with its first channel.

- (1) Logic channel 0 trigger is issued and processing of the group 0 is initiated.
 - (2) Processing of the group 0, conversion of logical channels 0 -> 1 -> 2 -> start of channel 3 conversion.
 - (3) Logic channel 6 trigger is issued during the conversion of channel 3.
 - (4) The operation is dependent on the setting of forced stop mode (ADC12Bn_CTRL.FSMD).
- Forced stop mode is enabled (ADC12Bn_CTRL.FSMD = "1"):
- Since the priority of the channel 6 is higher than priority of the channel 3, the processing of the group 0 is interrupted during the conversion of channel 3 and trigger status of channel 0 is set.
- Forced stop mode is disabled (ADC12Bn_CTRL.FSMD = "0"):
- Since the priority of the channel 6 is higher than priority of the channel 4, the processing of the group 0 is interrupted after the conversion of channel 3 is finished and trigger status of channel 0 is set.
- (5) Group 1 is converted.
 - (6) After group 1 is finished, processing of group 0 is restarted with conversion of channel 0 since its trigger status flag is set to "1".
 - (7) Group 0 is converted.
 - (8) At the end of group 0 processing, idle trigger group 2 is converted.

Figure 3-8 Restarting of the Whole Group Processing

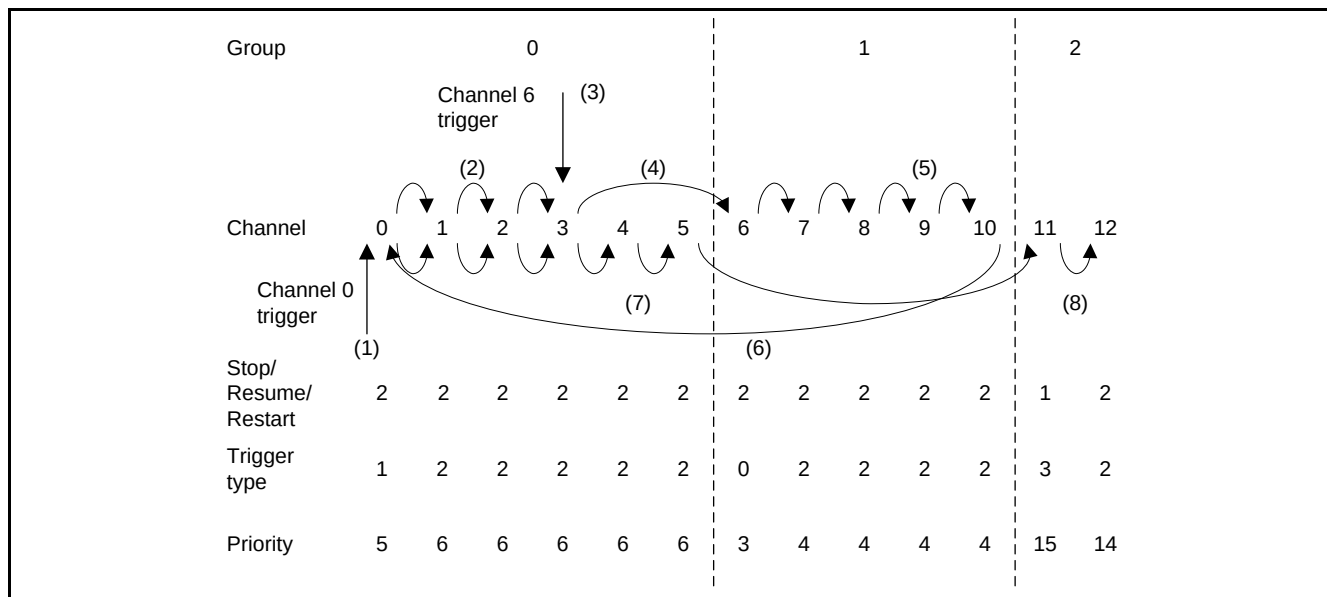


Figure 3-9 shows an example of restarting a group processing with its first channel during the conversion of the last channel of the group processing (Forced stop mode is enabled (ADC12Bn_CTRL.FSMD = "1")).

Figure 3-10 shows an example of restarting a group processing with its first channel during the conversion of the last channel of the group processing (Forced stop mode is disabled (ADC12Bn_CTRL.FSMD = "0")).

- (1) Logic channel 0 trigger is issued and processing of the group 0 is initiated.
- (2) Processing of the group 0, conversion of logical channels 0 -> 1 -> 2 -> 3 -> 4 -> start of channel 5 conversions (last channel of the group 0).
- (3) Logic channel 6 trigger is issued during the conversion of channel 5.

The operations after (3) are dependent on the setting of forced stop mode (ADC12Bn_CTRL.FSMD).

Forced stop mode is enabled (ADC12Bn_CTRL.FSMD = "1", Figure 3-9):

- (4) Since the priority of the channel 6 is higher than priority of the channel 5, the processing of the group 0 is interrupted during the conversion of channel 5 and trigger status of channel 0 is set.
- (5) Group 1 is converted.
- (6) After group 1 is finished, processing of group 0 is restarted with conversion of channel 0 since its trigger status flag is set to "1".
- (7) Group 0 is converted.
- (8) At the end of group 0 processing, idle trigger group 2 is converted.

Forced stop mode is disabled (ADC12Bn_CTRL.FSMD = "0", Figure 3-10):

- (4) After the conversion of channel 5 is finished (group 0 is converted), processing continues with the conversion of the channel 6.
- (5) Group 1 is converted.
- (6) At the end of group 1 processing, idle trigger group 2 is converted (group 0 is not restarted).

Figure 3-9 Restarting a Group Processing with its First Channel during the Conversion of the Last Channel of the Group Processing (Forced stop mode is enabled (ADC12Bn_CTRL.FSMD = "1"))

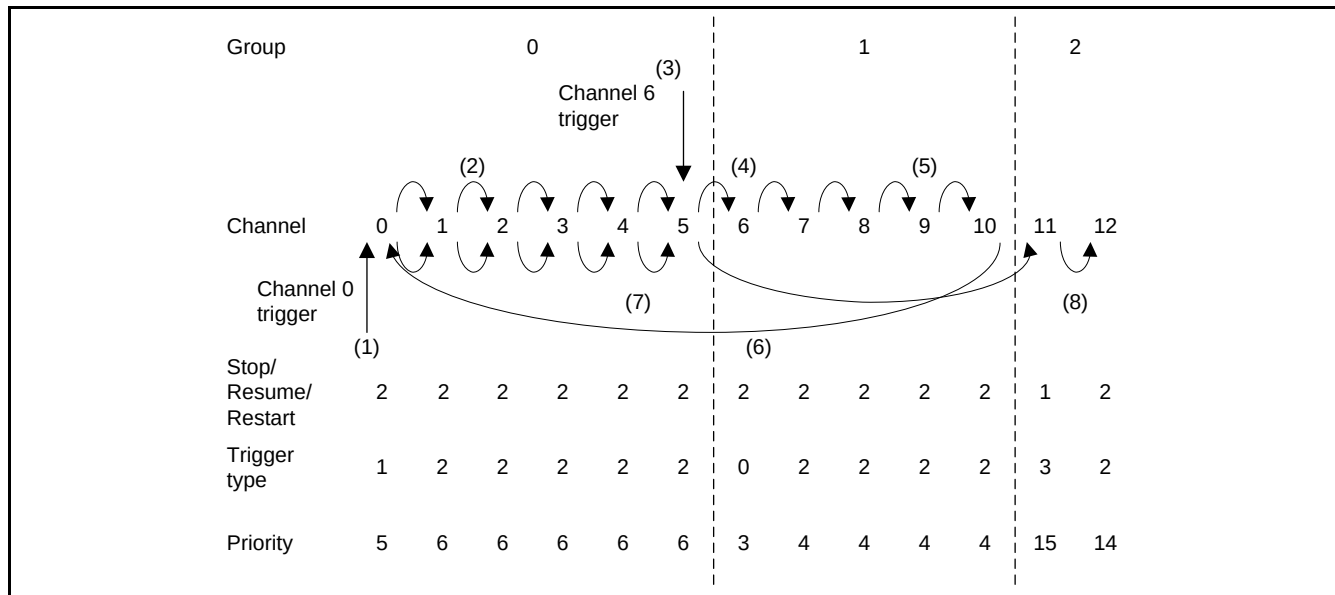


Figure 3-10 Restarting a Group Processing with its First Channel during the Conversion of the Last Channel of the Group Processing (Forced stop mode is disabled (ADC12Bn_CTRL.FSMD = "0"))

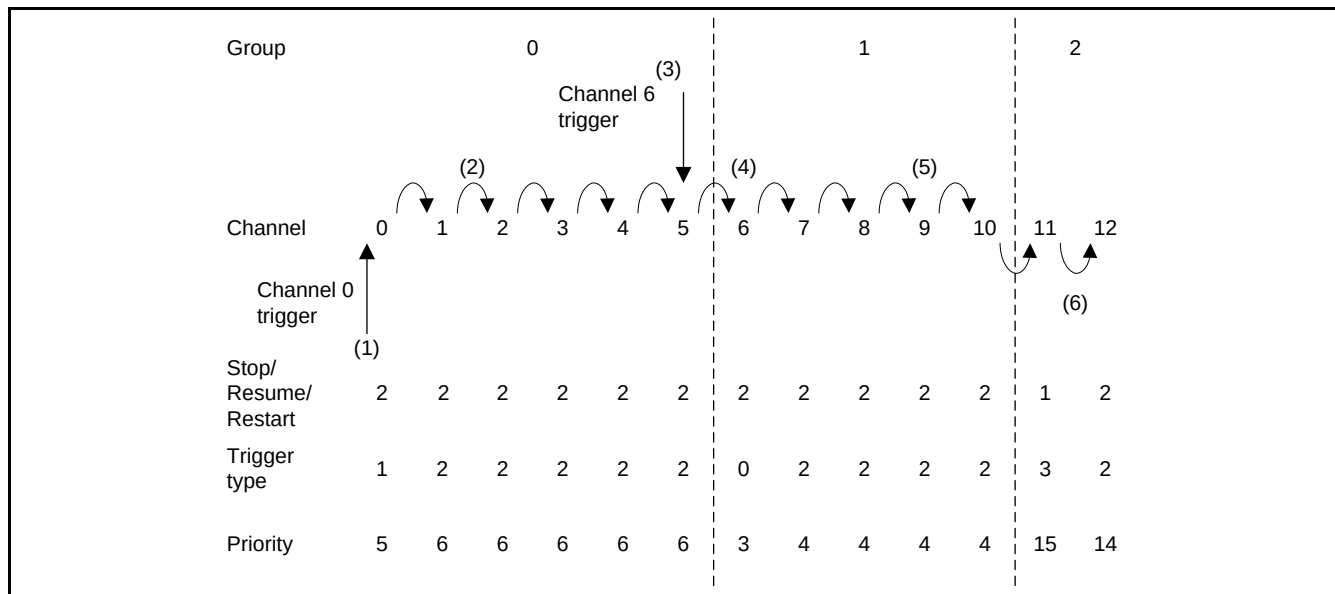


Figure 3-11 shows an example of restarting a group processing with its last converted channel set to resume. These way subgroups can be formed within a group.

- (1) Logic channel 0 trigger is issued and processing of the group 0 is initiated.
- (2) Processing of the group 0, conversion of logical channels 0 -> 1 -> 2 -> start of channel 3 conversion.
- (3) Logic channel 6 trigger is issued during the conversion of channel 3.

(4) The operation is dependent on the setting of forced stop mode (ADC12Bn_CTRL.FSMD).

Forced stop mode is enabled (ADC12Bn_CTRL.FSMD = "1"):

Since the priority of the channel 6 is higher than priority of the channel 3, the processing of the group 0 is interrupted during the conversion of channel 3 and trigger status of channel 1 is set (channel 1 is the last converted channel set to resume).

Forced stop mode is disabled (ADC12Bn_CTRL.FSMD = "0"):

Since the priority of the channel 6 is higher than priority of the channel 4, the processing of the group 0 is interrupted after the conversion of channel 3 is finished and trigger status of channel 1 is set (channel 1 is the last converted channel set to resume).

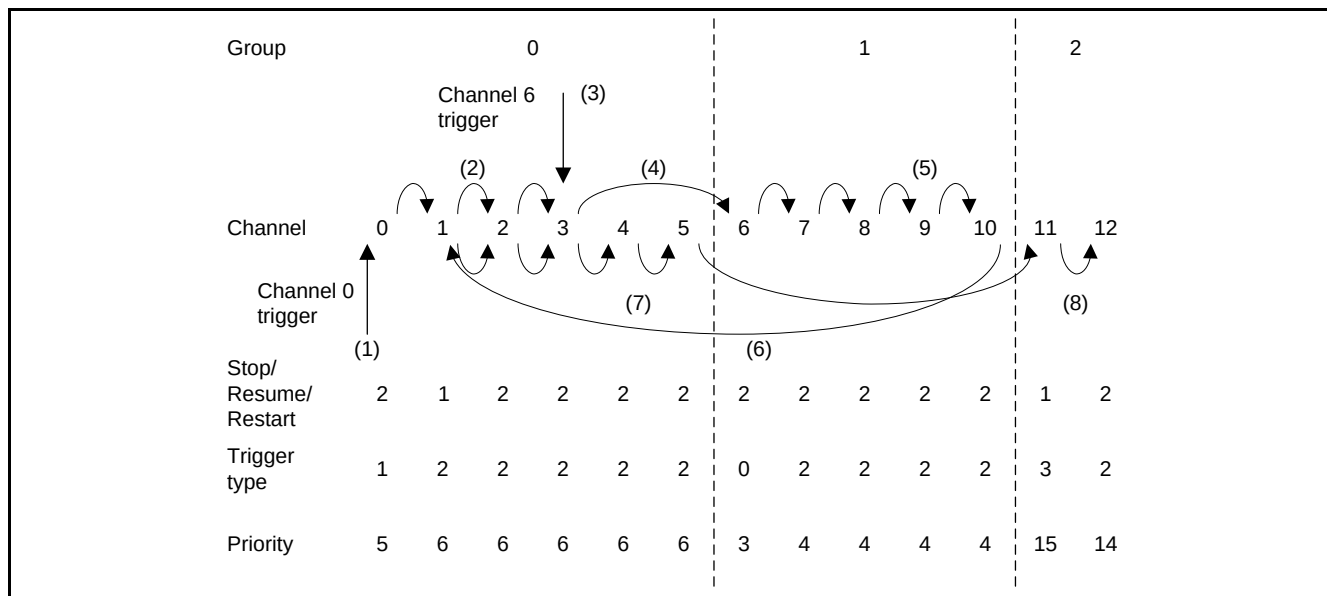
(5) Group 1 is converted.

(6) After group 1 is finished, processing of group 0 is restarted with conversion of channel 1 since its trigger status flag is set to "1".

(7) Subgroup (channels 1 till 5) of the group 0 is converted.

(8) At the end of group 0 processing, idle trigger group 2 is converted.

Figure 3-11 Restarting of the Group Processing with a Subgroup



3.6. Multiple Conversion Logical Channels

First four logical channels can be configured so that after the channel is triggered, several conversions (up to 16) are performed and conversion result is accumulated. These channels are referred to as multiple conversion channels. The following is valid for multiple conversion channels:

- All features and rules provided for regular logical channels (mapping to analog inputs, data protection, triggering rules, priority, channel grouping and behavior within a group) apply also to multiple conversion channels.
- The number of conversions to be performed when the channel is triggered is defined by ADC12Bn_MCCTRL0~3.CNVNUM bit field. If CNVNUM is set to "0", a multiple conversion channel behaves exactly like a regular channel.
- Dedicated A/D conversion data registers ADC12Bn_CD0~3 hold the sum of the single conversion results. Accordingly, ADC12Bn_CD0~3 registers are extended to 16 bits.
- Forced stop mode is enabled (ADC12Bn_CTRL.FSMD = "1"): In case the conversion request with higher priority is issued during multiple conversion, the multiple conversion channel is interrupted after interrupt operation, and the conversion of the channel with the higher priority is started. Forced stop mode is disabled (ADC12Bn_CTRL.FSMD = "0"): Once the first conversion of multiple conversion channel is started, the channel processing cannot be interrupted by higher priority requests until CNVNUM+1 conversions are finished, if the dedicated bit ADC12Bn_MCCTRL0~3.ICIRQY (intra-channel interrupt ability) is set to "1". The setting ADC12Bn_MCCTRL0~3.ICIRQY = "0" allows to interrupt multiple conversion channel processing between single conversions, if a higher priority request appears.
- In the case that a multiple conversion channel is interrupted between/during single conversions, the dedicated group interrupted interrupt flags (ADC12Bn_CHSTAT0~3.GRPIRQ and ADC12Bn_GRPIRQ0.GRPIRQ) are set. The corresponding Resume/Restart/Stop bit field (ADC12Bn_CHCTRL0~3.RSMRST) and intra-channel interrupt ability setting (ADC12Bn_MCCTRL0~3.ICIRQY) determine the further channel processing (after higher priority requests are converted).

Table 3-1 shows the description about multiple conversion after interrupted (ADC12Bn_CTRL.FSMD = "0").

Table 3-2 shows the description about multiple conversion after interrupted (ADC12Bn_CTRL.FSMD = "1").

Table 3-1 Description about Multiple Conversion after Interrupted (ADC12Bn_CTRL.FSMD = "0")

Settings		Description of Trigger Status and Conversion Counter after Interrupted
ADC12Bn_MCCTRL0~3.ICIRQY	ADC12Bn_CHCTRL0~3.RSMRST[1:0]	
"0" (can be interrupted between single conversion)	"00" (Stop)	Imposes the trigger status flag clearing. Keeps current value of the conversion counter. It is cleared by next conversion request.
	"01" (Resume)	Keeps the trigger status flag set and current value of the conversion counter.
	"10" (Restart)	The trigger status flag stays set only if the channel is first channel in the group, otherwise the trigger status of the channel is cleared and instead the trigger status flag of the first channel in the subgroup is set. The conversion counter is cleared immediately. It means that the accumulated conversion result before the interruption is not really usable because it is not known how many conversions are done.

Settings		Description of Trigger Status and Conversion Counter after Interrupted
ADC12Bn_MCCTRL0~3. ICIRQY	ADC12Bn_CHCTRL0~31. RSMRST[1:0]	
"1" (cannot be interrupted between single conversion)	Don't care	Don't care. Multiple conversion is not interrupted.

Table 3-2 Description about Multiple Conversion after Interrupted (ADC12Bn_CTRL.FSMD = "1")

Settings		Description of Trigger Status and Conversion Counter after Interrupted
ADC12Bn_MCCTRL0~3. ICIRQY	ADC12Bn_CHCTRL0~31. RSMRST[1:0]	
"0" (can be interrupted between single conversion)	"00" (Stop)	Imposes the trigger status flag clearing. Keeps current value of the conversion counter. It is cleared by next conversion request.
	"01" (Resume)	Keeps the trigger status flag set. The conversion counter is cleared immediately. It means that the accumulated conversion result before the interruption is not really usable because it is not known how many conversions are done.
	"10" (Restart)	The trigger status flag stays set only if the channel is first channel in the group, otherwise the trigger status of the channel is cleared and instead the trigger status flag of the first channel in the subgroup is set. The conversion counter is cleared immediately. It means that the accumulated conversion result before the interruption is not really usable because it is not known how many conversions are done.
"1" (cannot be interrupted between single conversion)	"00" (Stop)	Imposes the trigger status flag clearing. Keeps current value of the conversion counter. It is cleared by next conversion request.
	"01" (Resume)	Keeps the trigger status flag set and current value of the conversion counter.
	"10" (Restart)	The trigger status flag stays set only if the channel is first channel in the group, otherwise the trigger status of the channel is cleared and instead the trigger status flag of the first channel in the subgroup is set. The conversion counter is cleared immediately. It means that the accumulated conversion result before the interruption is not really usable because it is not known how many conversions are done.

- In the case that range comparison is enabled for a multiple conversion channel, every conversion result is passed to the range comparator.
- For notes of data protection about multiple conversion, refer to section "Logical channel data protection function" in chapter "3. Operation of A/D".

3.7. Forced Stop

■ Forced stop mode (ADC12Bn_CTRL.FSMD = "1"):

During an active A/D conversion, it can be forced stop by the following ways.

- Writing ADC12Bn_CTRL.FSTP = "1":
All channel's trigger status flags are reset.
The current A/D conversion is stopped after interrupt operation.
- Writing "1" to the corresponding bits of ADC12Bn_TRGCL0.TRGCL or ADC12Bn_CHCTRLi.TRGCL:
The corresponding trigger status flag is reset immediately.
The current A/D conversion is stopped after interrupt operation,

■ Not forced stop mode (ADC12Bn_CTRL.FSMD = "0"):

The A/D conversion cannot stop.

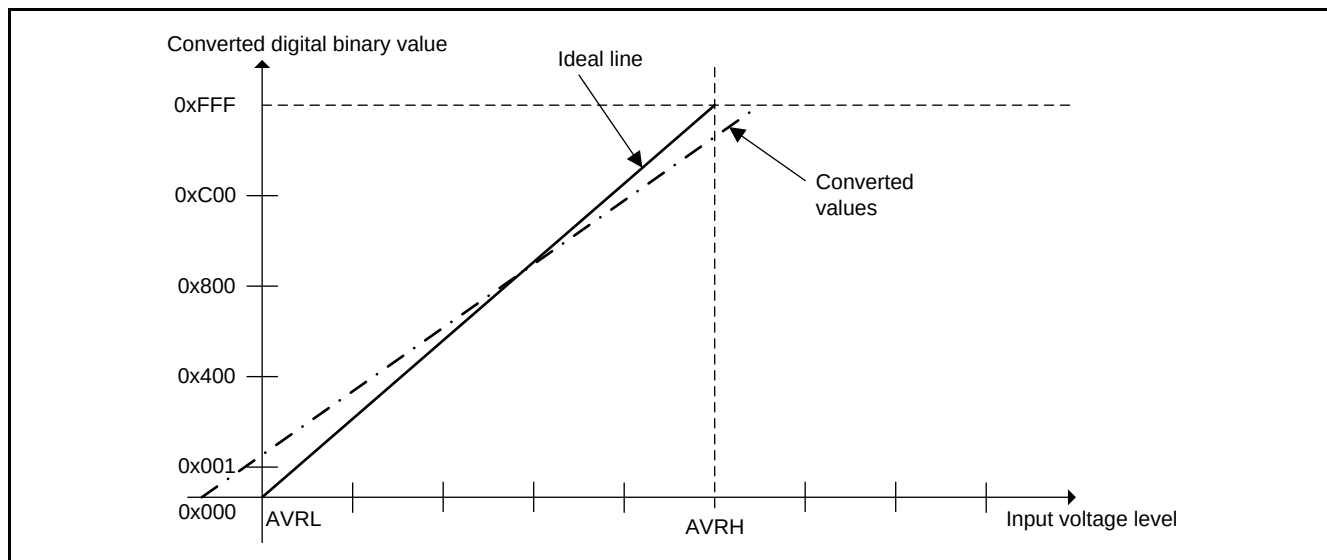
- Writing ADC12Bn_CTRL.FSTP = "1": invalid.
- Writing "1" to the corresponding bits of ADC12Bn_TRGCL0.TRGCL or ADC12Bn_CHCTRLi.TRGCL:
The corresponding trigger status flag is reset immediately.
The current A/D conversion is not stopped, but A/D conversion result (the following) is not update.
 - A/D conversion done interrupt flag (the corresponding bits of ADC12Bn_CDONEIRQ0.CDONEIRQ or ADC12Bn_CHSTATi.CDONEIRQ)
 - A/D conversion data (the corresponding register of ADC12Bn_CD0~31)
 - Converted logical channel number (ADC12Bn_STAT.ACH[5:0] (ADC12Bn_CTRL.ACHMD is set as "1"))

Even if the trigger status flag of the idle trigger channel i (ADC12Bn_CHCTRLi.TRGTYP[1:0] = "11") is cleared (by writing "1" to the corresponding bits of ADC12Bn_TRGCL0 or ADC12Bn_CHCTRLi.TRGCL), it is set "1" again immediately when the trigger status flag of all the channels is "0".

3.8. A/D Converter Calibration

Additional feature of multiple conversion logical channels is selection of A/D Converter reference voltages AVRH or AVRL for conversion instead of dedicated analog input signals. If AVRL conversion is wanted it is enough to set one of ADC12Bn_MCCTRL0~3.AVRLSEL bits to "1" and trigger corresponding channel. For AVRH conversion it is needed to set one of ADC12Bn_MCCTRL0~3.AVRHSEL bits to "1", set corresponding ADC12Bn_MCCTRL0~3.AVRLSEL bit to "0" and trigger the dedicated channel.

If AVRHSEL or ARVRLSEL bits is set to "1", during the conversion of the corresponding channel mapping of the logical channel to an analog inputs is disabled.

Figure 3-12 Example of Converted Digital Value Dependence on Input Voltage Level


This feature can be used to perform A/D Converter calibration. As it is shown on Figure 3-12 ideal characteristics of A/D Converter would have:

- transition between digital values 0x000 and 0x001 at $AVRL + 0.5LSB$ input voltage level and
- transition between digital values 0xFFEh and 0xFFFF at $AVRH - 1.5LSB$ input voltage level.

If this is not the case, A/D Converter can be calibrated by performing following steps:

- Set gain correction setting (ADC12Bn_GCV.GCV) to "0".
- Set a multiple conversion channel to highest priority and its AVRLSEL bit to "1".
- For different ADC12Bn_OCV.OCV settings, trigger the multiple conversion channel, i.e. perform AVRL voltage conversion. It is better to configure multiple conversions of AVRL and calculate average result (accumulated result divided by the number of executed conversions).
- Find ADC12Bn_OCV.OCV setting x for which the transition between digital values 0x000 and 0x001 occurs.
- Set AVRLSEL bit back to "0".
- Set AVRHSEL bit to "1".
- For different ADC12Bn_OCV.OCV settings, trigger the multiple conversion channel, i.e. perform AVRH voltage conversion. It is better to configure multiple conversions of AVRH and calculate average result.
- Find ADC12Bn_OCV.OCV setting y for which the transition between digital values 0xFFE and 0xFFFF occurs.
- Set A/D Converter offset compensation setting register ADC12Bn_OCV to the value calculated as $(x+y)/2 + 2$.
- Set AVRHSEL bit back to "0".
- Set AVRLSEL bit to "1".
- For different ADC12Bn_GCV.GCV settings, trigger the multiple conversion channel, i.e. perform AVRL voltage conversion. It is better to configure multiple conversions of AVRL and calculate average result.
- Find ADC12Bn_GCV.GCV setting z for which the transition between digital values 0x000 and 0x001 occurs.

- Set A/D Converter gain compensation setting register ADC12Bn_GCV to the value calculated as "z + 1".
- Set AVRLSEL and AVRHSEL bits to "0".
- Trigger and perform further logical channel conversions (analog inputs AN to which are logical channels mapped are converted by calibrated A/D Converter).

3.9. DMA Transfer Function

There are four conversion done DMA triggers available. They can be configured through the corresponding ADC12Bn_CDSD0~3 registers:

- The bit field CDCHNUM specifies the logical channel number whose conversion done interrupt flag issues a DMA request,
- CDCHEN bit controls enabling/disabling of the DMA request.

The feature provides an efficient way to transfer A/D conversion results to memory. Selecting of the group last logical channels through the four CDCHNUM bit fields can configure four different groups for DMA transfers. Since the group is always made of consecutive logical channels and the corresponding conversion data registers can be read linearly, the DMA transfer for the whole group is possible after the conversion of the last channel of the group is finished.

3.10. Range Comparator Function

The range comparator offers eight comparison groups with an upper and a lower threshold register each. The 32 logical channels can be enabled for range comparison and assigned to one of the eight comparators individually.

If range comparator is enabled for a logical channel, it provides two result flags:

- Interrupt flags ADC12Bn_RCIRQ0.RCIRQ and ADC12Bn_CHSTAT0~31.RCIRQ, signaling that the A/D conversion result is outside the range or inside the range ("inverted" operation, i.e. ADC12Bn_CHCTRL0~31.RCINVSEL = "1").
- Over threshold flags ADC12Bn_RCOTF0.RCOTF and ADC12Bn_CHSTAT0~31.RCOTF, showing that the A/D conversion value exceeded the upper threshold in the case of outside range detection.

Furthermore, each logical channel can be enabled to send an interrupt request to the CPU, if dedicated flags ADC12Bn_RCIRQ0.RCIRQ31~0 and ADC12Bn_CHSTAT0~31.RCIRQ are set.

The range comparator can choose 12/8-bit mode by the full range comparator mode (ADC12Bn_CTRL.FRCMD).

ADC12Bn_CTRL.FRCMD	Description
"1" : 12-bit range comparator	ADC12Bn_FRCOL0~7/FRCOH0~7 are used for range comparator upper/lower threshold value. Selection of one of eight available range comparator threshold values for the logical channel is configured by corresponding ADC12Bn_CHCTRL0~31.RCSEL[2:0] bit fields. The upper/lower comparator compares the 12 bits, 10 bits or 8 bits of the A/D conversion result. ADC12Bn_CTRL.RES[1:0] define this resolution. – If 12-bit resolution (ADC12Bn_CTRL.RES[1:0] = "x0"): Compares the 12 bits of A/D conversion result. – If 10-bit resolution (ADC12Bn_CTRL.RES[1:0] = "01"): Compares the 10 bits of A/D conversion result. – If 8-bit resolution (ADC12Bn_CTRL.RES[1:0] = "11"): Compares the 8 bits of A/D conversion result.

ADC12Bn_CTRL.FRCMD	Description
"0" : 8-bit range comparator	ADC12Bn_RCOL0~7/RCOH0~7 are used for range comparator upper/lower threshold value. Selection of one of eight available range comparator threshold values for the logical channel is configured by corresponding ADC12Bn_CHCTRL0~31.RCSEL[2:0] bit fields. The upper/lower comparator compares the upper 8 bits of the A/D conversion result.

Figure 3-13 shows the 8-bit range comparator structure.

Figure 3-14 shows the 12-bit range comparator structure.

Figure 3-13 8-bit Range Comparator Structure

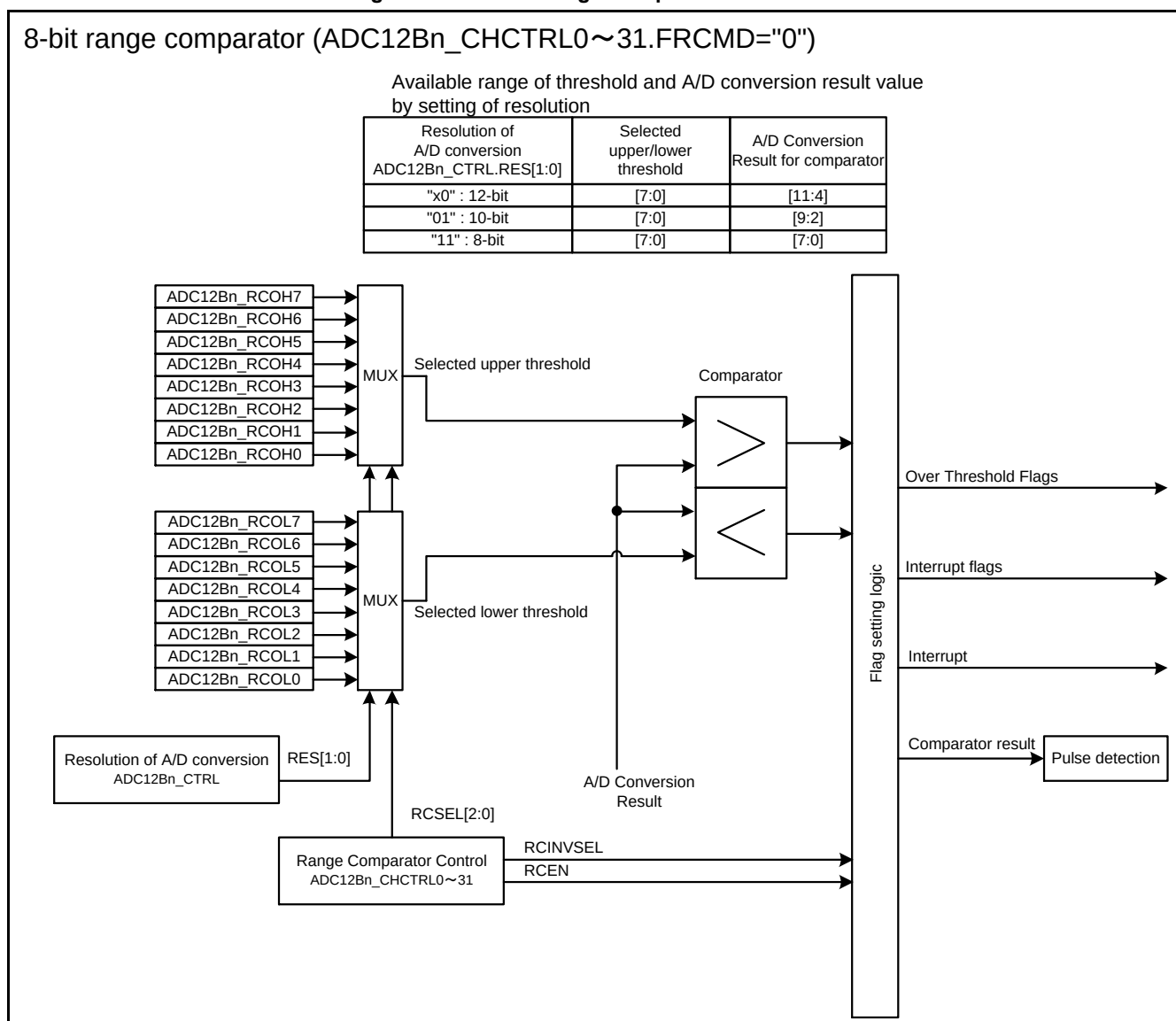
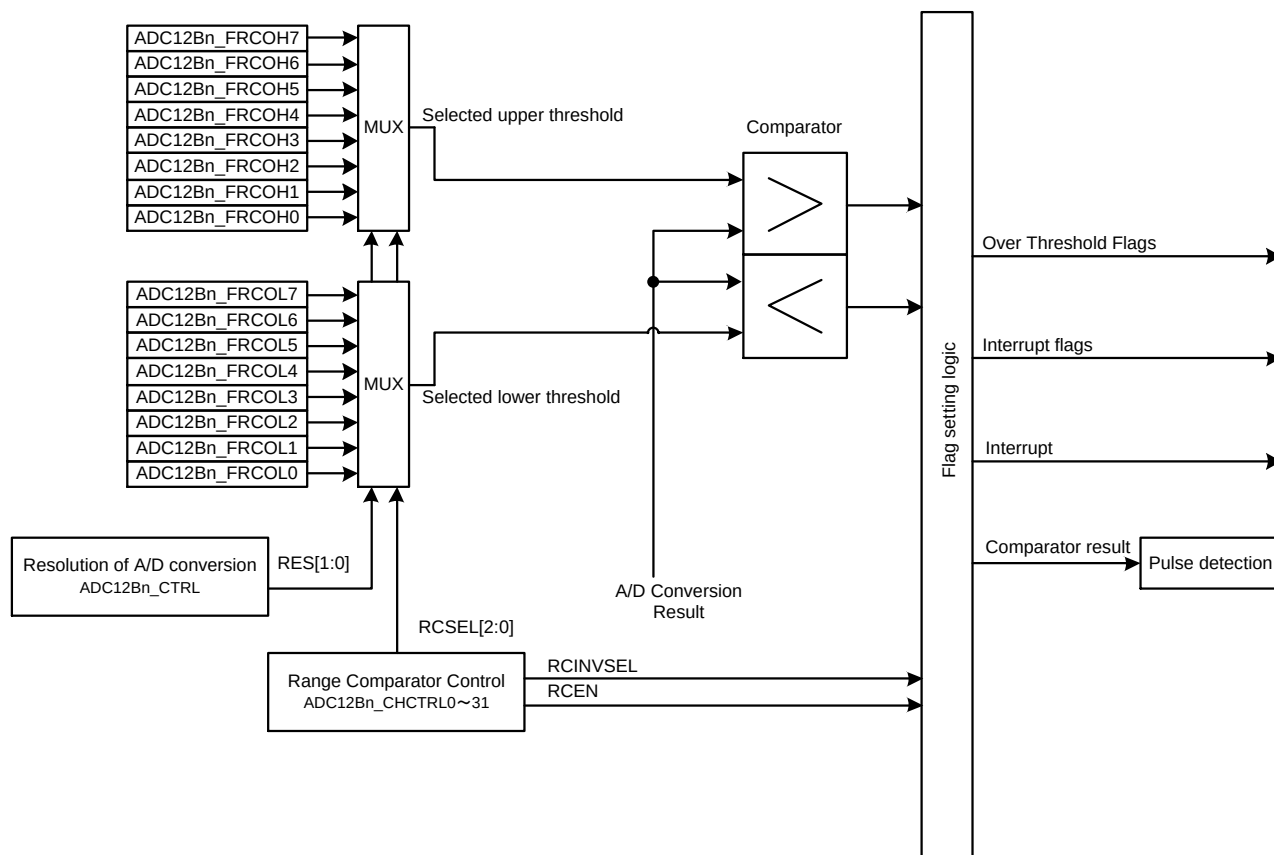


Figure 3-14 12-bit Range Comparator Structure

12-bit range comparator (ADC12Bn_CHCTRL0~31.FRCMD="1")

Available range of threshold and A/D conversion result value
by setting of resolution

Resolution of A/D conversion ADC12Bn_CTRL:RES[1:0]	Selected upper/lower threshold	A/D Conversion Result for comparator
"x0" : 12-bit	[11:0]	[11:0]
"01" : 10-bit	[9:0]	[9:0]
"11" : 8-bit	[7:0]	[7:0]



3.11. Pulse Detection Function

The result of the comparison from the range comparator can be filtered by the pulse detection function. For every logical channel, the pulse detection function has a pair of reload registers to store the initial value for the positive and negative down counters (ADC12Bn_PCCTRL0~31.PCTPRL[7:0] and ADC12Bn_PCCTRL0~31.PCTNRL[4:0]). The positive and the negative counters decrement on positive and negative events obtained from the result of the comparison done by the range comparator.

The features of the pulse detection function are:

- Detect events with desired length
- Filter parasitic inverted events
- Each logical channel has a pulse detection function module associated with it
- Interrupt can be generated on detection of a pulse.

The output of the range comparator for particular logical channel signifies either a positive event or a negative event depending on the configuration of ADC12Bn_CHCTRL0~31.RCINVSEL register in the dedicated channel control register and the converted digital value of the A/D Converter as explained in Table 3-3 "Generation of positive/negative events". Whenever a positive event occurs the corresponding positive counter ADC12Bn_PCCTRL0~31.PCTPCT is decremented. Similarly, the dedicated negative counter ADC12Bn_PCCTRL0~31.PCTNCT decrements with each negative event. The purpose of the positive counter is to detect consecutive range comparator events of desired length. The negative counter can be used to force a restart of the positive counter if a negative events of a certain length are detected due to spikes, noise etc.

Table 3-3 Generation of Positive/Negative Events

Inverted Range Selection RCINVSEL bit	Range Comparator Output	Events
0 (configured for "outside range")	inside range	Negative event
	outside range	Positive event
1 (configured for "inside range")	outside range	Negative event
	inside range	Positive event

The following steps describe the working principle.

- The positive counter is decremented with each positive event of the corresponding logical channel.
- The corresponding pulse counter interrupt flags (ADC12Bn_CHSTAT0~31.PCIRQ and ADC12Bn_PCIRQ0.PCIRQ31~0) are set as the positive counter reaches zero. This flag remains set until it is cleared through writing dedicated ADC12Bn_PCIRQC0.PCIRQC31~0 bit to "1". The positive counter and the negative counter are stopped as long as PCIRQ flag of the channel is "1".
- If PCIRQ is set and the corresponding enable bit ADC12Bn_PCIRQE0.PCIRQE31~0 is equal to "1", an interrupt is generated.
- The negative counter is decremented with each negative event of the corresponding logical channel except while the corresponding PCIRQ flag is set.
- Positive counter is reloaded with the value set in the reload register ADC12Bn_PCCTRL0~31.PCTPRL when:
 - Negative counter reaches zero,
 - "1" is written to dedicated ADC12Bn_PCIRQC0.PCIRQC31~0 bit.
- Negative counter is reloaded with the value set in the reload register ADC12Bn_PCCTRL0~31.PCTNRL when:

3.12. Debug Mode

When the ADC12Bn_CTRL.DBGE bit is set to "1" and the processor is in debug state, the A/D Converter completes the current conversion, but further conversion is stopped. When the processor leaves debug state or ADC12Bn_CTRL.DBGE is set to "0", conversion continues with the next channel from where it had stopped.

The ADC12Bn_STAT.BUSY flag is not affected even while ADC12Bn_CTRL.DBGE bit is set to "1" and the processor is in debug state: If all trigger status bits are cleared, ADC12Bn_STAT.BUSY flag is set to "0", and the A/D Converter goes to idle (power-down) state; if any trigger status bit is set again, the A/D Converter leaves idle state, and the ADC12Bn_STAT.BUSY flag is set to "1" after the resumption time elapses.

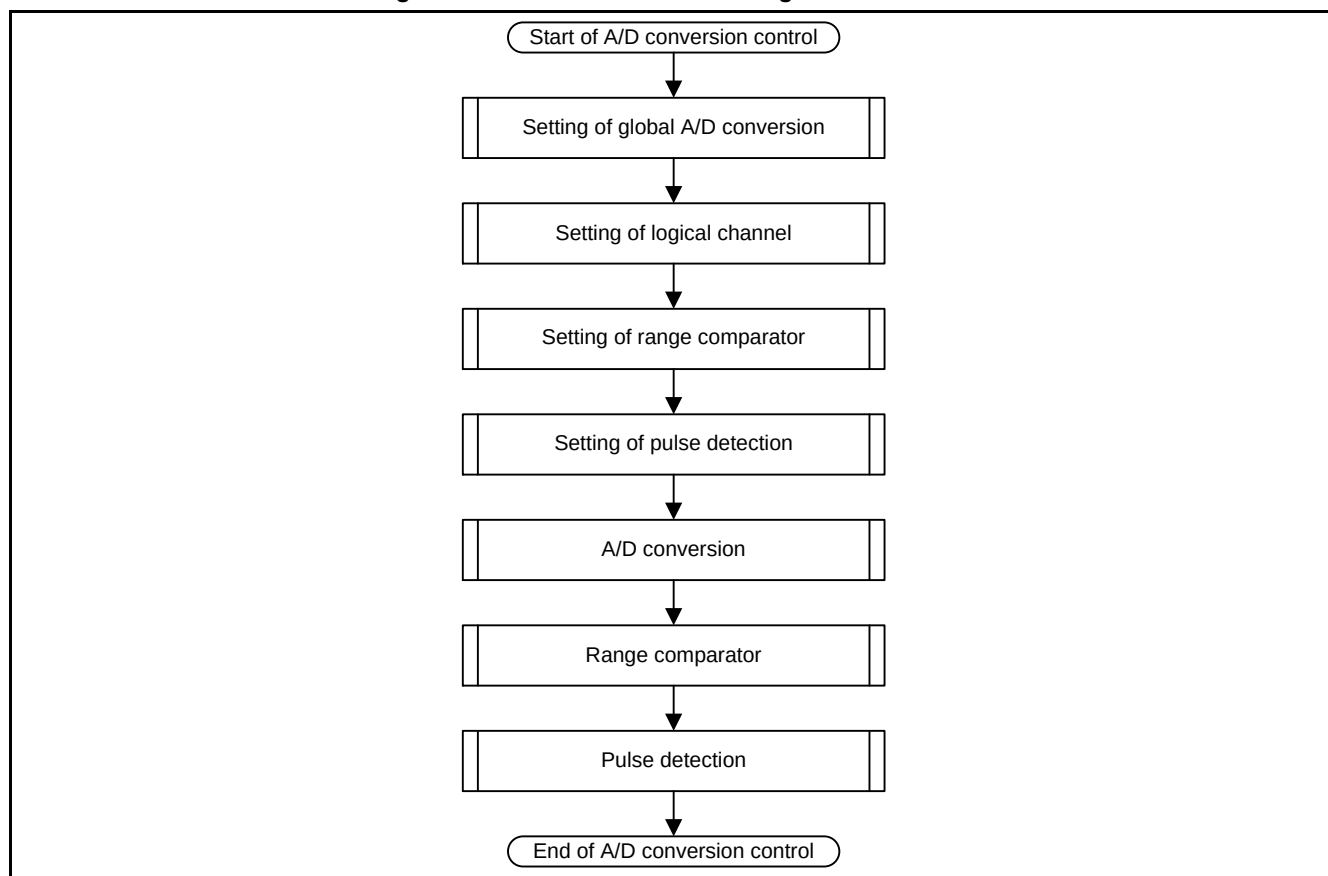
4. Setup Procedure Examples

This section shows examples of setup procedure of A/D converter.

4.1. Control of A/D Conversion

Figure 4-1 shows main flow of controlling A/D converter.

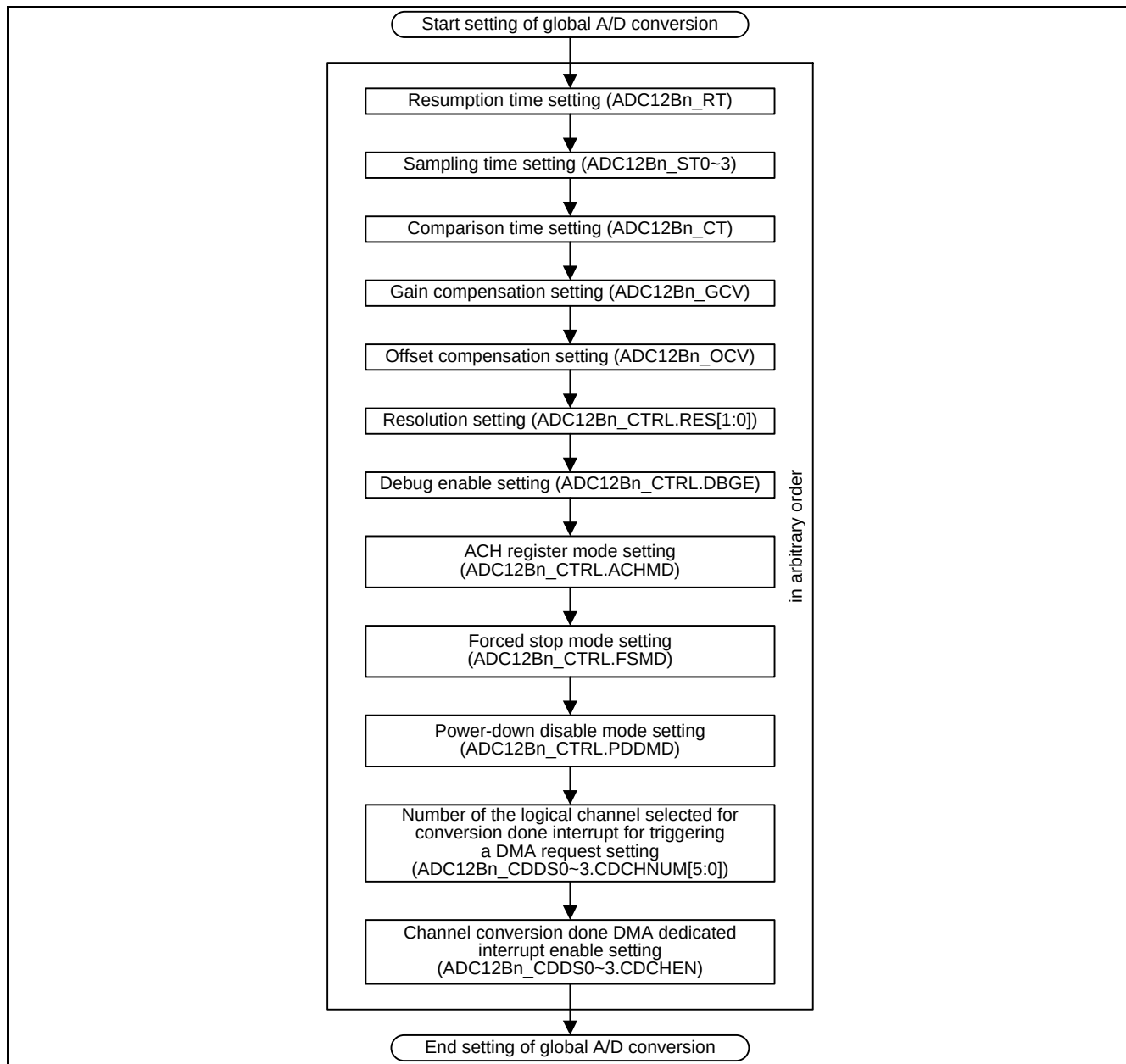
Figure 4-1 Main Flow of Controlling A/D Converter



4.2. Setting of Global A/D Conversion

Figure 4-2 shows the setting procedure of global A/D conversion.

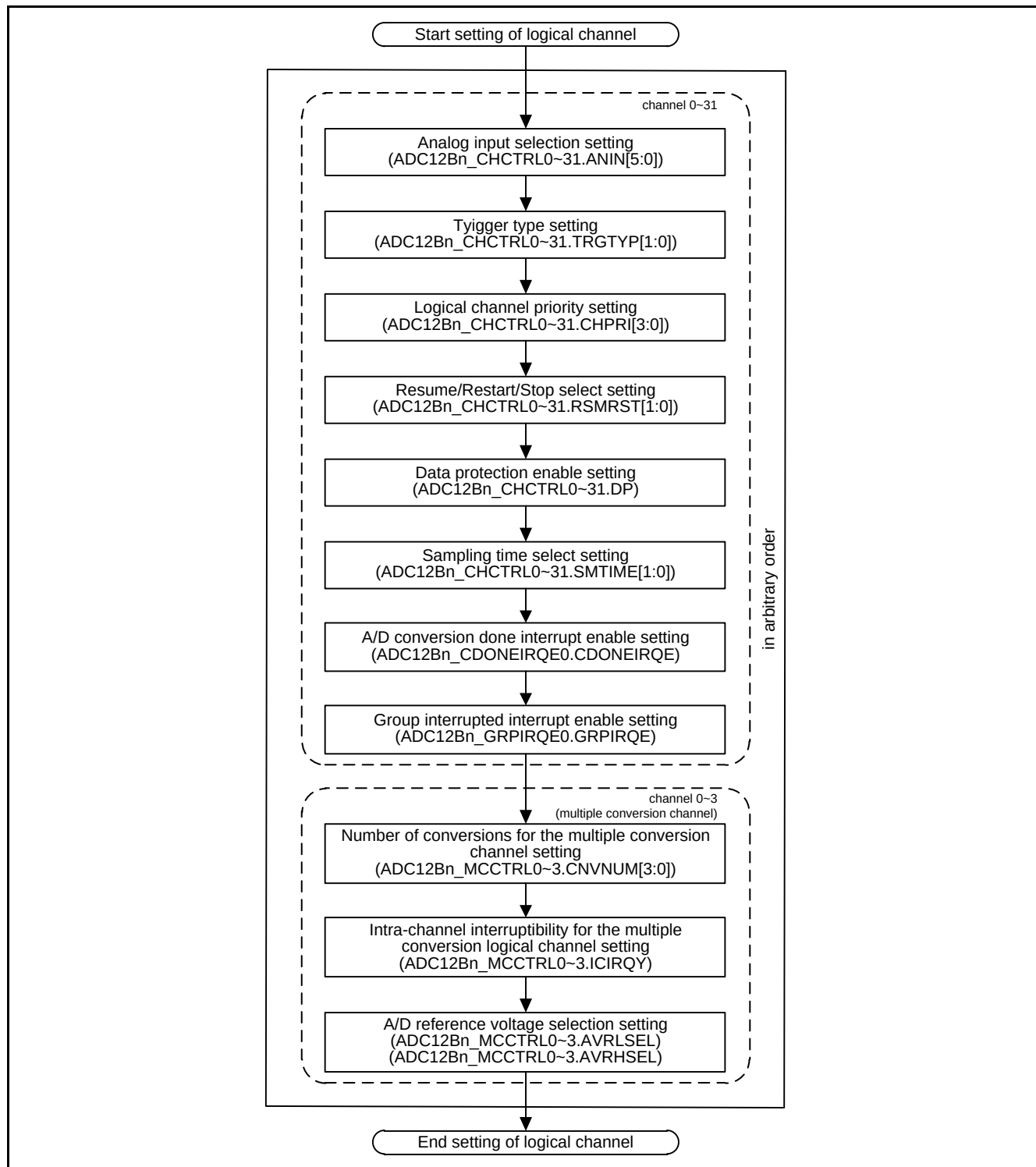
Figure 4-2 Setting of Global A/D Conversion



4.3. Setting of Logical Channel

Figure 4-3 shows the setting procedure of logical channel.

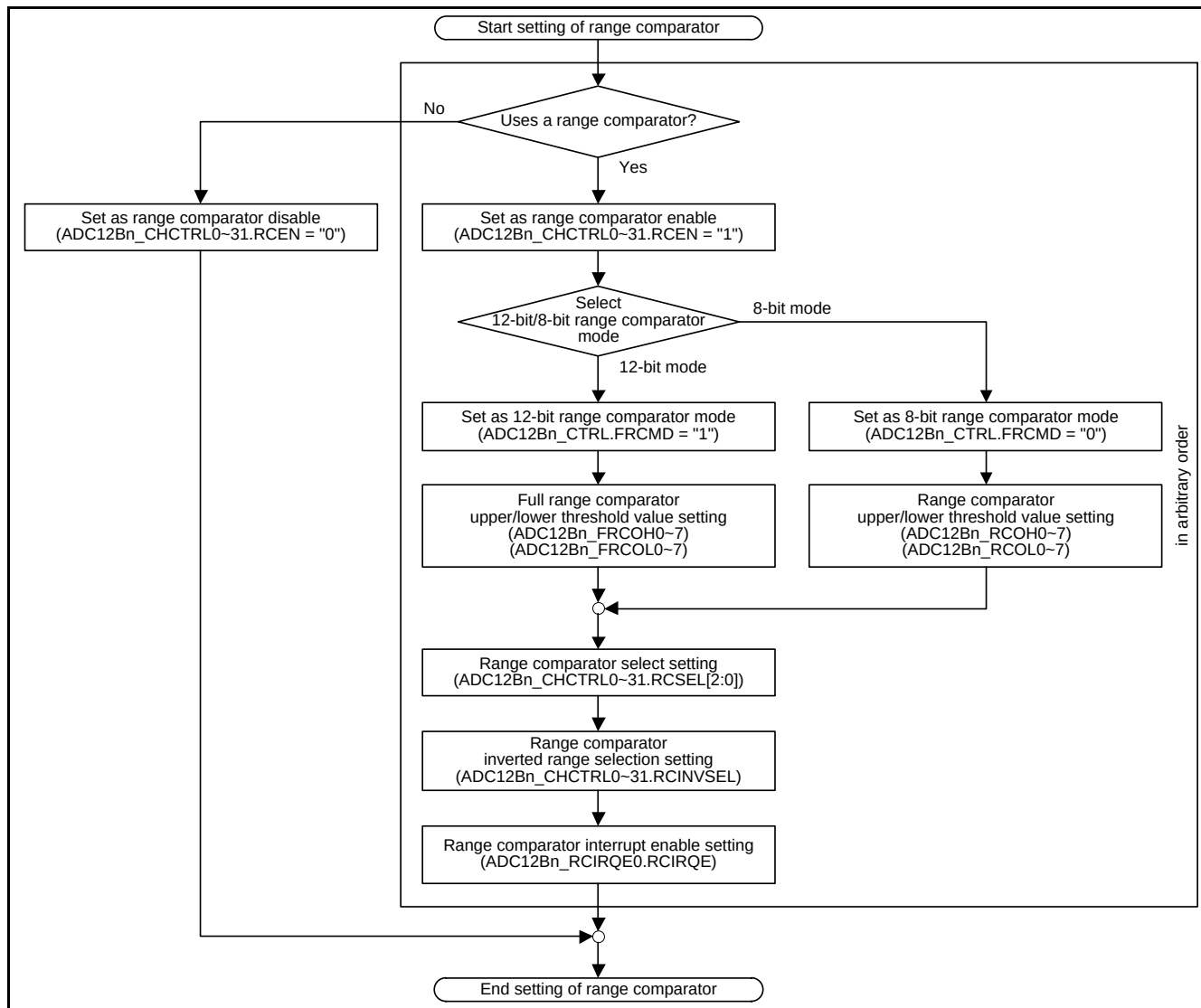
Figure 4-3 Setting of Logical Channel



4.4. Setting of Range Comparator

Figure 4-4 shows the setting procedure of range comparator.

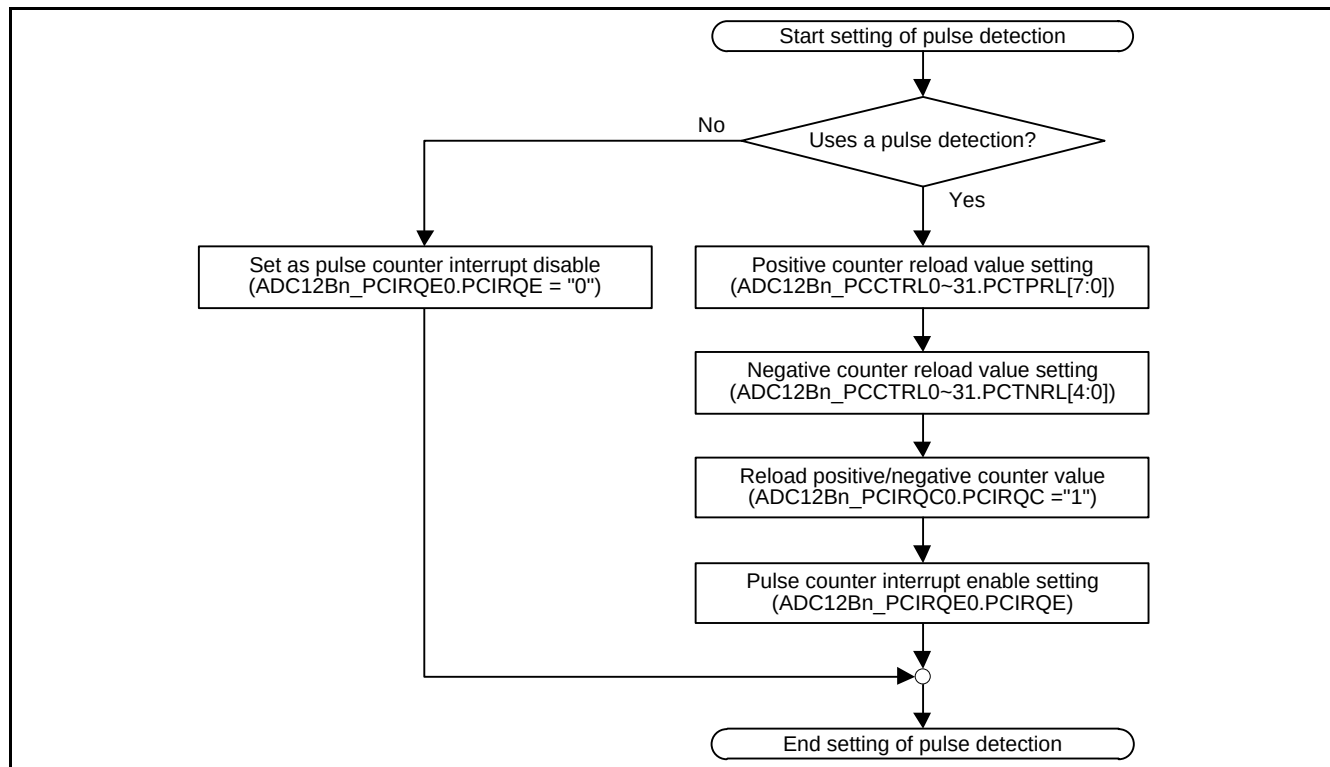
Figure 4-4 Setting of Range Comparator



4.5. Setting of Pulse Detection

Figure 4-5 shows setting procedure of pulse detection.

Figure 4-5 Setting of Pulse Detection

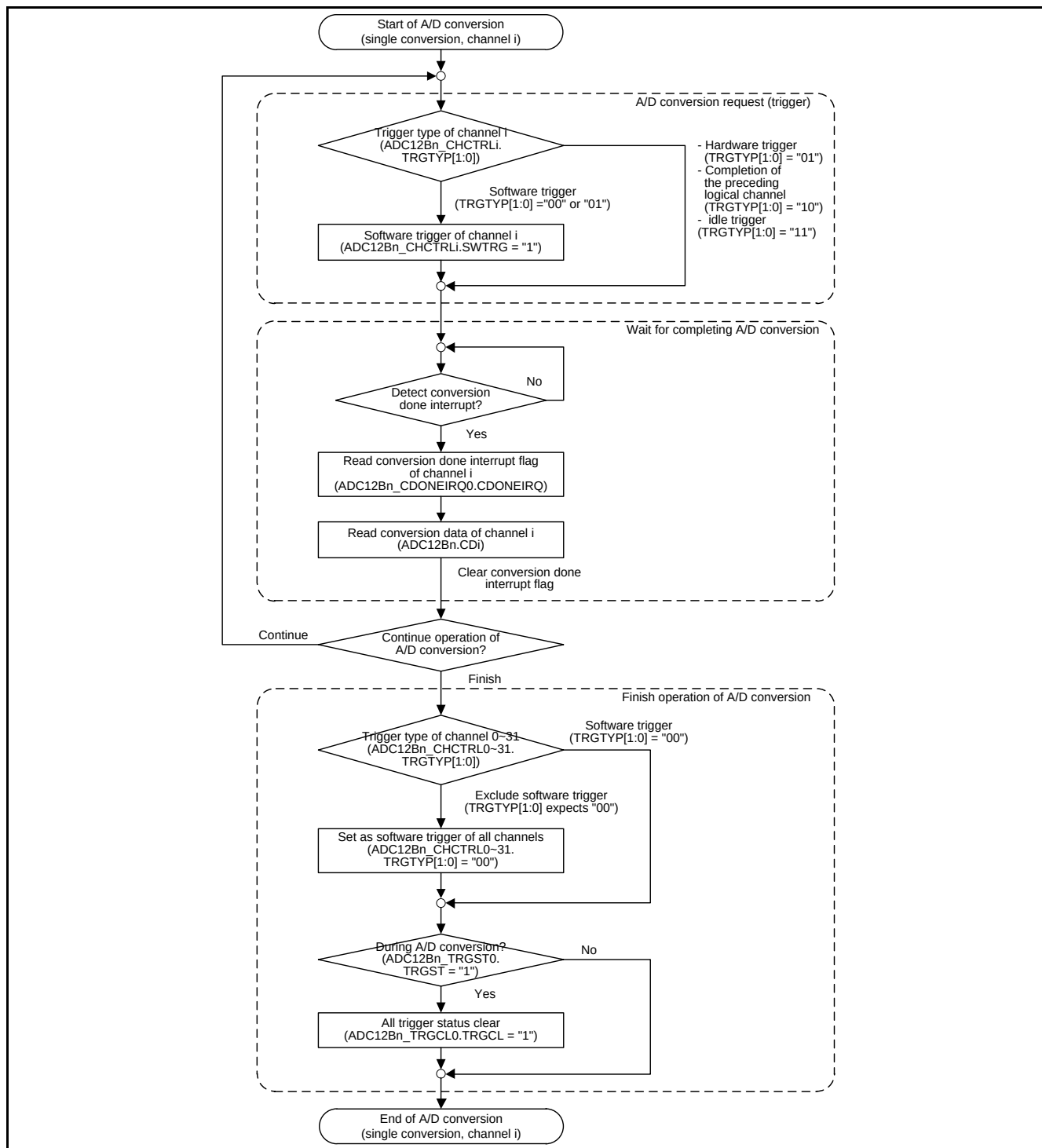


4.6. A/D Conversion

■ Single conversion

Figure 4-6 shows the example of A/D conversion (single conversion) operation.

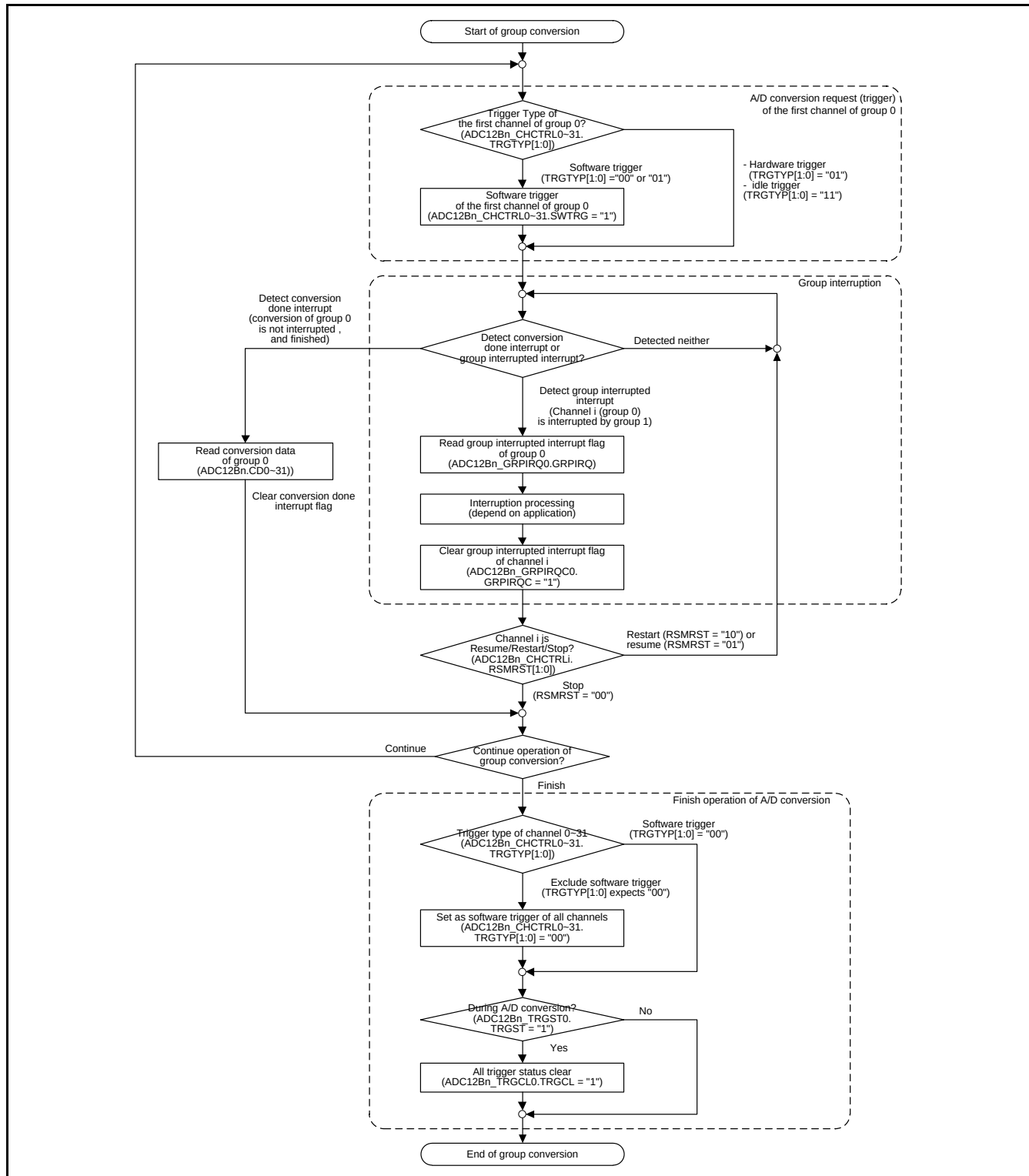
Figure 4-6 A/D Conversion (Single conversion, channel i)



■ Group conversion

Figure 4-7 shows the example of group conversion operation.

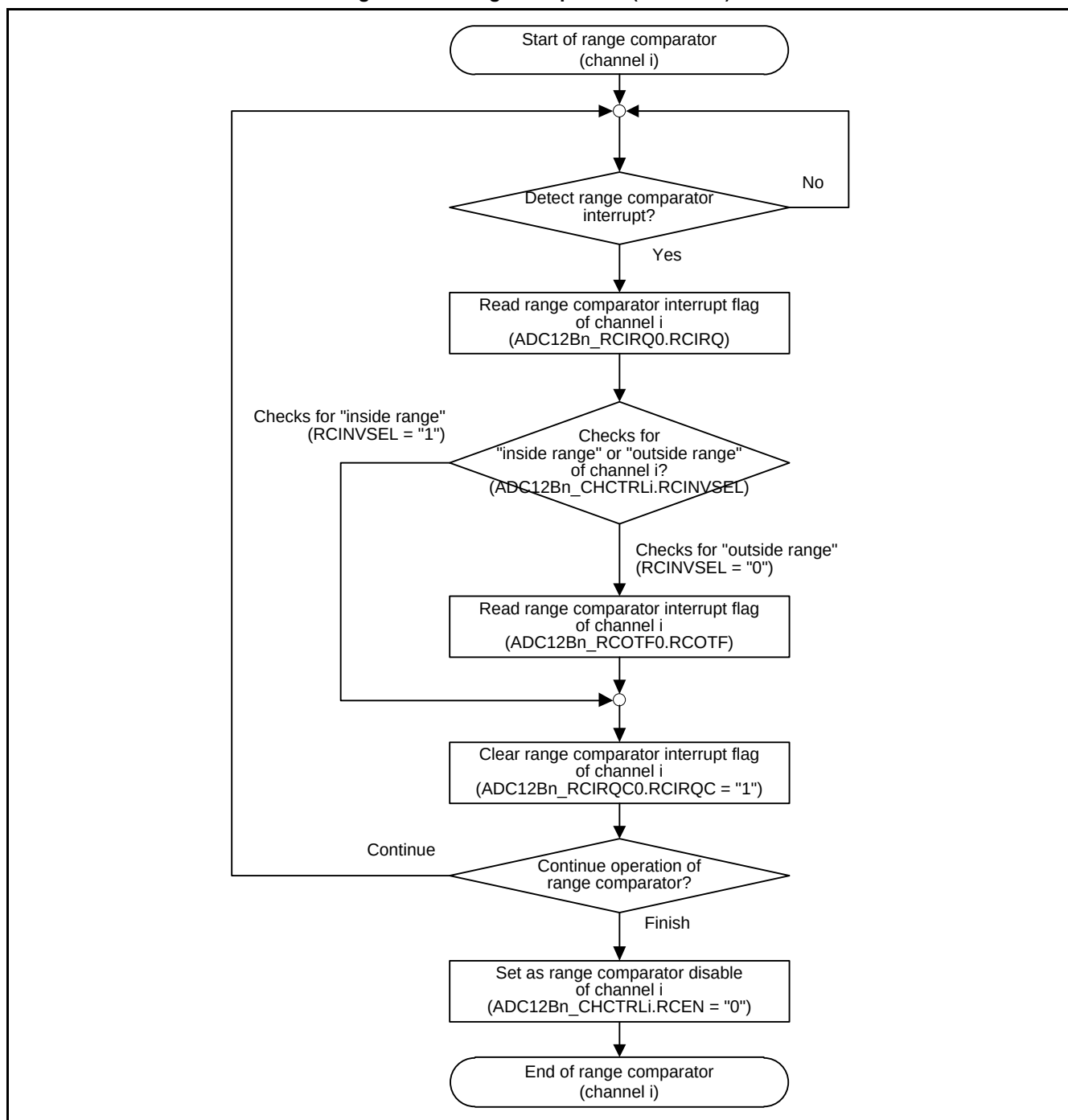
Figure 4-7 Group Conversion



4.7. Range Comparator

Figure 4-8 shows the example of range comparator operation.

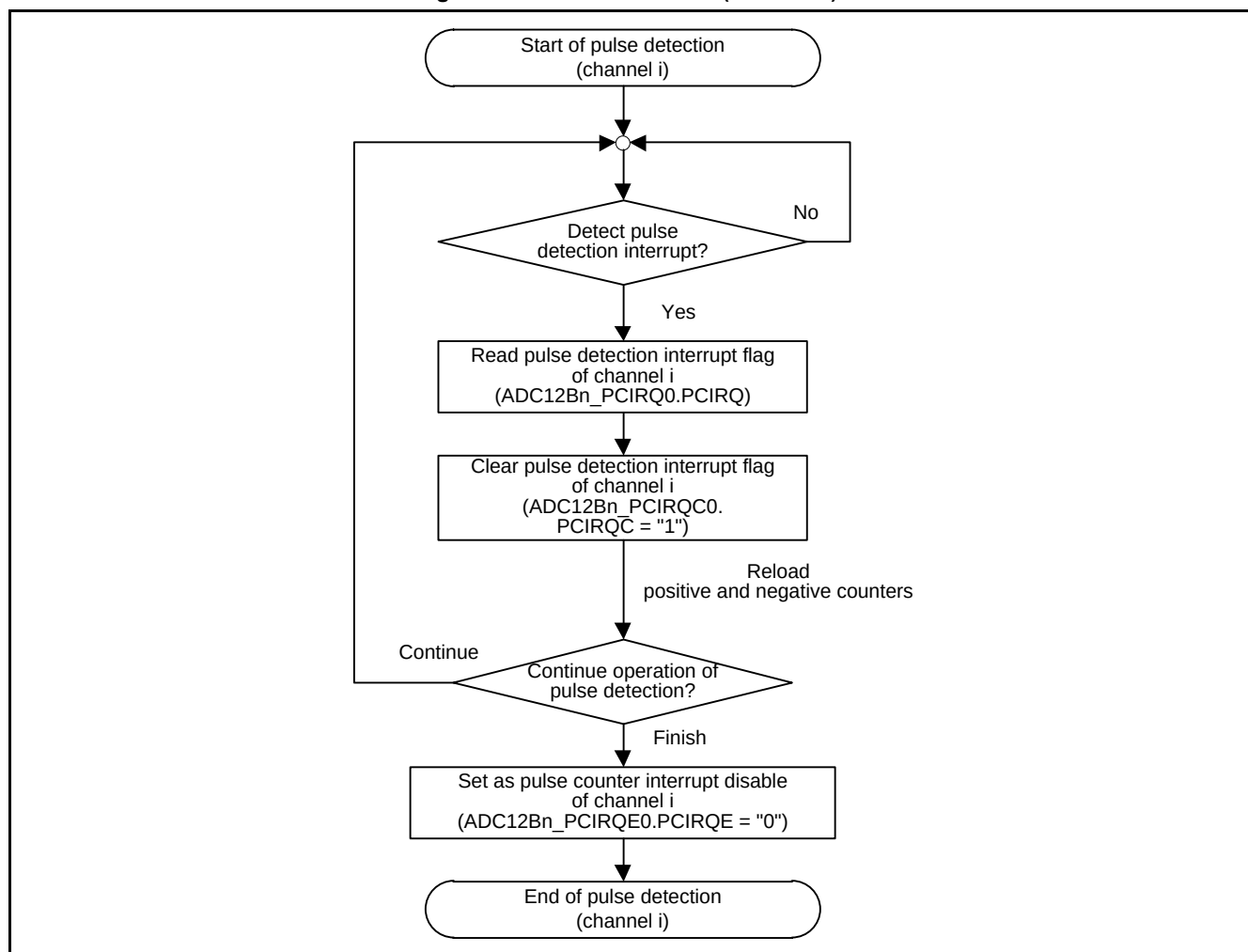
Figure 4-8 Range Comparator (Channel i)



4.8. Pulse Detection

Figure 4-9 shows the example of pulse detection operation.

Figure 4-9 Pulse Detection (Channel i)



5. Registers

The A/D converter contains registers to configure the operation of A/D conversion and to store the converted values. It also contains registers to configure the range comparators and registers to control and store the status of the pulse detection function. This section describes the registers of the A/D Converter in details.

The suffix "n" in the register name indicates that the register is an instance "n" of the module.

Registers of A/D Converter

Logical channel related registers are:

- A/D Channel Control Registers (ADC12Bn_CHCTRL0~31)
- A/D Channel Status Registers (ADC12Bn_CHSTAT0~31)
- A/D Conversion Data Registers (ADC12Bn_CD0~31)
- Pulse Counter Control Registers (ADC12Bn_PCCTRL0~31)
- A/D Conversion Done Interrupt Flags (ADC12Bn_CDONEIRQ0)
- A/D Conversion Done Interrupt Enable Registers (ADC12Bn_CDONEIRQE0)
- A/D Conversion Done Interrupt Clear Registers (ADC12Bn_CDONEIRQC0)
- Group Interrupted Interrupt Flags (ADC12Bn_GRP_IRQ0)
- Group Interrupted Interrupt Enable Registers (ADC12Bn_GRP_IRQE0)
- Group Interrupted Interrupt Clear Registers (ADC12Bn_GRP_IRQC0)
- Range Comparator Interrupt Flags (ADC12Bn_RC_IRQ0)
- Range Comparator Interrupt Enable Registers (ADC12Bn_RC_IRQE0)
- Range Comparator Interrupt Clear Registers (ADC12Bn_RC_IRQC0)
- Pulse Counter Interrupt Flags (ADC12Bn_PC_IRQ0)
- Pulse Counter Interrupt Enable Registers (ADC12Bn_PC_IRQE0)
- Pulse Counter Interrupt Clear Registers (ADC12Bn_PC_IRQC0)
- A/D Channel Trigger Status Flags (ADC12Bn_TRGST0)
- A/D Channel Trigger Status Clear Registers (ADC12Bn_TRGCL0)
- A/D Channel Trigger Overrun Flags (ADC12Bn_TRGOR0)
- A/D Channel Trigger Overrun Clear Registers (ADC12Bn_TRGORC0)
- Range Comparator Over Threshold Flags (ADC12Bn_RCOTF0)

Global A/D Converter registers are:

- Conversion Done DMA Select Registers (ADC12Bn_CDDS0~3)
- A/D Converter Resumption Time Setting Register (ADC12Bn_RT)
- A/D Converter Comparison Time Setting Register (ADC12Bn_CT)
- A/D Converter Sampling Time Setting Registers (ADC12Bn_ST0~3)
- A/D Converter Offset Compensation Setting Register (ADC12Bn_OCV)
- A/D Converter Gain Compensation Setting Register (ADC12Bn_GCV)
- A/D Converter Global Control Register (ADC12Bn_CTRL)
- A/D Converter Global Status Register (ADC12Bn_STAT)
- Range Comparator Upper Threshold Registers (ADC12Bn_RCOH0~7)
- Range Comparator Lower Threshold Registers (ADC12Bn_RCOL0~7)
- Full Range Comparator Upper Threshold Registers (ADC12Bn_FRCOH0~7)
- Full Range Comparator Lower Threshold Registers (ADC12Bn_FRCOL0~7)

Multiple conversion logical channel related registers are:

- A/D Multiple Conversion Channel Control Registers (ADC12Bn_MCCTRL0~3)
- A/D Multiple Conversion Channel Status Registers (ADC12Bn_MCSTAT0~3)

5.1. A/D Channel Control Registers (ADC12Bn_CHCTRL0~31)

The A/D Channel Control Registers configure the logical channel specific settings. ADC12Bn_CHCTRL0 (described here) is dedicated to channel 0, ADC12Bn_CHCTRL31 is dedicated to channel 31. Other registers (ADC12Bn_CHCTRL1,.....ADC12Bn_CHCTRL30) have similar bit fields.

REGISTER_NAME	ADC12Bn_CHCTRLi (i = 0~31)
OFFSET	0x0000 + i*4
ACCESS_SIZE	B H W
MULTIPLE	0: 31
NUMERIC_TYPE	-
OTHER	-

A/D Channel Control Register (ADC12Bn_CHCTRL0)

BIT_OFFSET	31	30	29	28	27	26	25	24
BIT_NAME	Reserved						TRGCL	SWTRG
ACCESS_TYPE	R0,W0						R0,W	R0,W
PROT_TYPE								
INITIAL_VALUE	0x00						0	0

BIT_OFFSET	23	22	21	20	19	18	17	16
BIT_NAME	RCEN	RCINVSEL	Reserved	RCSEL[2]	RCSEL[1]	RCSEL[0]	SMTIME[1]	SMTIME[0]
ACCESS_TYPE	R/W	R/W	R0,W0	R/W	R/W	R/W	R/W	R/W
PROT_TYPE								
INITIAL_VALUE	0	0	0	0	0	0	0	0

BIT_OFFSET	15	14	13	12	11	10	9	8
BIT_NAME	Reserved	DP	RSMRST[1]	RSMRST[0]	CHPRI[3]	CHPRI[2]	CHPRI[1]	CHPRI[0]
ACCESS_TYPE	R0,W0	R/W	R/W	R/W	R/W	R/W	R/W	R/W
PROT_TYPE								
INITIAL_VALUE	0	0	0	0	0	0	0	0

BIT_OFFSET	7	6	5	4	3	2	1	0
BIT_NAME	TRGTYP[1]	TRGTYP[0]	ANIN[5]	ANIN[4]	ANIN[3]	ANIN[2]	ANIN[1]	ANIN[0]
ACCESS_TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
PROT_TYPE								
INITIAL_VALUE	0	0	0	0	0	0	0	0

[bit31:26] Reserved : Reserved bits

When writing, always write "0".

When reading, "0" is always read.

[bit25] TRGCL : Trigger Status Clear bit

bit	Description
0	No effect.
1	Clears corresponding trigger status bits ADC12Bn_CHSTAT0.TRGST and ADC12Bn_TRGST0.TRGST0.

Reading this bit always returns "0".

This bit is identical to the corresponding bit ADC12Bn_TRGCL0.TRGCL0.

[bit24] SWTRG : Software trigger bit

bit	Description
0	No effect.
1	Sets corresponding trigger status bits ADC12Bn_CHSTAT0.TRGST and ADC12Bn_TRGST0.TRGST0. When trigger status bits are cleared and set at the same time, clearing has priority. When TRGTYP bits are set to "10" or "11", writing SWTRG bit to "1" has no effect.

Reading this bit always returns "0".

Note:

- Do not write "1" to this bit and reconfigure TRGTYP with the same access.

[bit23] RCEN : Range Comparator Enable bit

bit	Description
0	Range comparator disabled.
1	Range comparator enabled.

[bit22] RCINVSEL : Range Comparator Inverted Range Selection bit

bit	Description
0	The comparison checks for "outside range", i.e. the over threshold and interrupt flags (ADC12Bn_RCOTF0.RCOTF0, ADC12Bn_CHSTAT0.RCOTF, ADC12Bn_RCIRQ0.RCIRQ0 and ADC12Bn_CHSTAT0.RCIRQ) are set when the ADC result is above the upper threshold OR below the lower threshold. That is called "outside range".
1	The comparison checks for "inside range" i.e., the interrupt flags (ADC12Bn_CHSTAT0.RCIRQ and ADC12Bn_RCIRQ0.RCIRQ0) are set when the ADC result is below or equal the upper threshold AND above or equal the lower threshold. That is called "inside range" mode.

[bit21] Reserved : Reserved bit

When writing, always write "0".

When reading, "0" is always read.

[bit20:18] RCSEL[2:0] : Range Comparator Select bit

RCSEL[2:0]	Description
000	Select range comparator 0, defined by ADC12Bn_RCOH0 and ADC12Bn_RCOL0 registers.
...	...
111	Select range comparator 7, defined by ADC12Bn_RCOH7 and ADC12Bn_RCOL7 registers.

[bit17:16] SMTIME[1:0] : Sampling Time Select bits

SMTIME[1:0]	Description
00	ADC12Bn_ST0 register value is selected as channel sampling time.
01	ADC12Bn_ST1 register value is selected as channel sampling time.
10	ADC12Bn_ST2 register value is selected as channel sampling time.
11	ADC12Bn_ST3 register value is selected as channel sampling time.

[bit15] Reserved : Reserved bit

When writing, always write "0".

When reading, "0" is always read.

[bit14] DP : Data protection Enable bit

bit	Description
0	Data protection function disabled.
1	Data protection function enabled.

[bit13:12] RSMRST[1:0] : Resume/Restart/Stop Select bits

RSMRST[1:0]	Description
00	Stop the group processing until next group start channel conversion request is issued.
01	Resume. If the group is interrupted, resume the group processing with this channel.
10	Restart. After the group is interrupted, restart with the start channel or the last converted channel configured as "resume" channel.
11	Reserved.

RSMRST[1:0] are not allowed to update during A/D conversion operation (ADC12Bn_TRGST0.TRGST and ADC12Bn_CHSTAT0~31.TRGST="1").

[bit11:8] CHPRI[3:0] : Logical channel priority

CHPRI[3:0]	Description
0000	Highest priority.
...	...
1111	Lowest priority.

CHPRI[3:0] are not allowed to update during A/D conversion operation (ADC12Bn_TRGST0.TRGST and ADC12Bn_CHSTAT0~31.TRGST="1").

[bit7:6] TRGTYP[1:0] : Trigger Type bits

TRGTYP[1:0]	Description
00	Software trigger only.
01	Software or hardware trigger.
10	Trigger by conversion completion and updating of conversion data register ADC12Bn_CD of the preceding channel.
11	Idle trigger, the channel trigger status is set if there is no channel having trigger status flag set and inactive data protection function.

TRGTYP[1:0] are not allowed to update during A/D conversion operation (ADC12Bn_TRGST0.TRGST and ADC12Bn_CHSTAT0~31.TRGST="1").

[bit5:0] ANIN[5:0] : Analog Input Selection bits

ANIN[5:0]	Description
000000	Analog input AN0 is selected.
...	...
111111	Analog input AN63 is selected.

The effective bits of ANIN[5:0] change according to the number of analog channels.
For the supported number of analog channels, please refer to the Device Data Sheet.

5.2. A/D Channel Status Registers (ADC12Bn_CHSTAT0~31)

These registers store the status information of the corresponding logical channels related to interrupt flags and trigger status. ADC12Bn_CHSTAT0 (described here) is dedicated to channel 0, ADC12Bn_CHSTAT31 is dedicated to channel 31. Other registers (ADC12Bn_CHSTAT1,.....ADC12Bn_CHSTAT30) have similar bit fields.

REGISTER_NAME	ADC12Bn_CHSTATi (i = 0~31)
OFFSET	0x0100 + i*2
ACCESS_SIZE	B H W
MULTIPLE	0: 31
NUMERIC_TYPE	-
OTHER	-

A/D Channel Status Register (ADC12Bn_CHSTAT0)

BIT_OFFSET	15	14	13	12	11	10	9	8
BIT_NAME	Reserved							
ACCESS_TYPE	RX,WX							
PROT_TYPE								
INITIAL_VALUE	0x00							

BIT_OFFSET	7	6	5	4	3	2	1	0
BIT_NAME	Reserved		RCOTF	PCIRQ	RCIRQ	GRPIRQ	CDONEIRQ	TRGST
ACCESS_TYPE	RX,WX		R,WX	R,WX	R,WX	R,WX	R,WX	R,WX
PROT_TYPE								
INITIAL_VALUE	00		0	0	0	0	0	0

[bit15:6] Reserved : Reserved bits

Reading this bit returns an undefined.

Writing data to these bits has no effect on the operation.

[bit5] RCOTF : Range Comparator Over Threshold flag

bit	Description
0	The conversion result is less than or equal to the upper threshold.
1	The conversion result is above the upper threshold.

This bit is identical to the corresponding bit in the ADC12Bn_RCOTF0 register. For more details, see ADC12Bn_RCOTF0 register description.

[bit4] PCIRQ : Pulse Counter Interrupt flag

bit	Description
0	Not detected.
1	Pulse counter interrupt detected.

This bit is identical to the corresponding bit in the ADC12Bn_PCIRQ0 register. For more details, see ADC12Bn_PCIRQ0 register description.

[bit3] RCIRQ : Range Comparator Interrupt flag

bit	Description
0	Not detected.
1	Range comparator interrupt detected.

This bit is identical to the corresponding bit in the ADC12Bn_RCIRQ0 register. For more details, see ADC12Bn_RCIRQ0 register description

[bit2] GRPIRQ : Group Interrupted Interrupt flag

bit	Description
0	Not detected.
1	Group interrupted interrupt detected.

This bit is identical to the corresponding bit in the ADC12Bn_GRPIRQ0 register. For more details, see ADC12Bn_GRPIRQ0 register description.

[bit1] CDONEIRQ : Conversion done Interrupt flag

bit	Description
0	Not detected
1	Conversion done Interrupt detected.

This bit is identical to the corresponding bit in the ADC12Bn_CDONEIRQ0 register. For more details, see ADC12Bn_CDONEIRQ0 register description.

[bit0] TRGST : Trigger Status flag

bit	Description
0	Conversion request not detected.
1	Conversion request detected.

This bit is identical to the corresponding bit in the ADC12Bn_TRGST0 register. For more details, see ADC12Bn_TRGST0 register description.

5.3. A/D Conversion Data Registers (ADC12Bn_CD0~31)

There are 32 A/D conversion data registers, one per logical channel. The registers are written by hardware at the end of conversion if the trigger status is still set. Registers ADC12Bn_CD0~3 are dedicated to multiple conversion channels so their width is 16 bits. Width of registers ADC12Bn_CD4~31 is 12 bits.

REGISTER_NAME	ADC12Bn_CD <i>i</i> (<i>i</i> = 0~31)
OFFSET	0x0180 + <i>i</i> *2
ACCESS_SIZE	B H W
MULTIPLE	0: 31
NUMERIC_TYPE	-
OTHER	-

A/D Conversion Data Result Registers (ADC12Bn_CD0~3)

Here is the register ADC12Bn_CD0 described, the registers ADC12Bn_CD1~3 have similar bit fields.

BIT_OFFSET	15	14	13	12	11	10	9	8
BIT_NAME	D[15]	D[14]	D[13]	D[12]	D[11]	D[10]	D[9]	D[8]
ACCESS_TYPE	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX
PROT_TYPE								
INITIAL_VALUE	X	X	X	X	X	X	X	X

BIT_OFFSET	7	6	5	4	3	2	1	0
BIT_NAME	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
ACCESS_TYPE	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX
PROT_TYPE								
INITIAL_VALUE	X	X	X	X	X	X	X	X

[bit15:0] D[15:0] : A/D Conversion Data bits

These bits store the conversion data.

The register is updated at the end of the A/D conversion only in the case the corresponding trigger status (ADC12Bn_TRGST0.TRGST0 and ADC12Bn_CHSTAT0.TRGST bits) is still "1".

The logical channel can be configured as multiple conversion channel, if ADC12Bn_MCCTRL0.CNVNUM is greater than 0. In that case the result of conversions is accumulated until the number of conversions reaches ADC12Bn_MCCTRL0.CNVNUM (the result of the first conversion is always directly stored and the following conversion results are added on current register value). Accordingly, if 12-bit conversion resolution is selected the conversion data can become 16-bit wide.

If ADC12Bn_MCCTRL0.CNVNUM is equal 0 (only one consecutive conversion is requested), the conversion data are provided in range of:

- bit[7:0] for 8-bit conversion resolution (bits 15~8 are "0"),
- bit[9:0] for 10-bit conversion resolution (bits 15~10 are "0"),
- bit[11:0] for 12-bit conversion resolution (bits 15~12 are "0").

A/D Conversion Data Registers (ADC12Bn_CD4~31)

Here is the register ADC12Bn_CD4 described, the registers ADC12Bn_CD5~31 have similar bit fields.

BIT_OFFSET	15	14	13	12	11	10	9	8
BIT_NAME	Reserved				D[11]	D[10]	D[9]	D[8]
ACCESS_TYPE	RX,WX				R,WX	R,WX	R,WX	R,WX
PROT_TYPE								
INITIAL_VALUE	0000				X	X	X	X

BIT_OFFSET	7	6	5	4	3	2	1	0
BIT_NAME	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
ACCESS_TYPE	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX
PROT_TYPE								
INITIAL_VALUE	X	X	X	X	X	X	X	X

[bit15:12] Reserved : Reserved bits

Reading this bit returns an undefined.

Writing data to these bits has no effect on the operation.

[bit11:0] D[11:0] : A/D Conversion Data bits

These bits store the conversion data, provided in range of:

- bit[7:0] for 8-bit conversion resolution (bits 11~8 are "0"),
- bit[9:0] for 10-bit conversion resolution (bits 11~10 are "0") and
- bit[11:0] for 12-bit conversion resolution.

The register is updated at the end of the A/D conversion only in the case the corresponding trigger status (ADC12Bn_TRGST0.TRGST4 and ADC12Bn_CHSTAT4.TRGST bits) is still "1".

5.4. Pulse Counter Control Registers (ADC12Bn_PCCTRL0~31)

These registers hold the reload and current values of positive and negative counters of the pulse detection function for the corresponding logical channel. The positive counters count down the positive events of the range comparator and negative counters count down the negative events of the range comparator. ADC12Bn_PCCTRL0 (described here) is dedicated to channel 0, ADC12Bn_PCCTRL31 is dedicated to channel 31. Other registers (ADC12Bn_PCCTRL1,.....ADC12Bn_PCCTRL30) have similar bit fields.

REGISTER_NAME	ADC12Bn_PCCTRLi (i = 0~31)
OFFSET	0x0200 + i*4
ACCESS_SIZE	B H W
MULTIPLE	0: 31
NUMERIC_TYPE	-
OTHER	-

Pulse Counter Control Register (ADC12Bn_PCCTRL0)

BIT_OFFSET	31	30	29	28	27	26	25	24
BIT_NAME	Reserved			PCTNCT[4]	PCTNCT[3]	PCTNCT[2]	PCTNCT[1]	PCTNCT[0]
ACCESS_TYPE	RX,WX			R,WX	R,WX	R,WX	R,WX	R,WX
PROT_TYPE								
INITIAL_VALUE	000			0	0	0	0	0

BIT_OFFSET	23	22	21	20	19	18	17	16
BIT_NAME	Reserved			PCTNRL[4]	PCTNRL[3]	PCTNRL[2]	PCTNRL[1]	PCTNRL[0]
ACCESS_TYPE	R0,W0			R/W	R/W	R/W	R/W	R/W
PROT_TYPE								
INITIAL_VALUE	000			0	0	0	1	0

BIT_OFFSET	15	14	13	12	11	10	9	8
BIT_NAME	PCTPCT[7]	PCTPCT[6]	PCTPCT[5]	PCTPCT[4]	PCTPCT[3]	PCTPCT[2]	PCTPCT[1]	PCTPCT[0]
ACCESS_TYPE	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX
PROT_TYPE								
INITIAL_VALUE	0	0	0	0	0	0	0	0

BIT_OFFSET	7	6	5	4	3	2	1	0
BIT_NAME	PCTPRL[7]	PCTPRL[6]	PCTPRL[5]	PCTPRL[4]	PCTPRL[3]	PCTPRL[2]	PCTPRL[1]	PCTPRL[0]
ACCESS_TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
PROT_TYPE								
INITIAL_VALUE	0	0	0	0	0	0	1	0

[bit31:29] Reserved : Reserved bits

Reading this bit returns an undefined.

Writing data to these bits has no effect on the operation.

[bit28:24] PCTNCT[4:0] : Pulse Negative Counter Register

This register reflects the current counter value of the pulse detection negative counter. Reload value is determined by PCTNRL.

The negative counter is reloaded under one of the following conditions:

- Writing "1" to the corresponding ADC12Bn_PCIRQC0.PCIRQC bit.
- Any positive event from the appropriate range comparator.

Therefore, in order to reload negative counter immediately after set to PCTNRL[4:0], the corresponding ADC12Bn_PCIRQC0.PCIRQC bit should be written "1".

[bit23:21] Reserved : Reserved bits

When writing, always write "0".

When reading, "0" is always read.

[bit20:16] PCTNRL[4:0] : Pulse Negative Counter Reload Register

These register bits hold the reload value of the negative counter PCTNCT used for counting negative events of the range comparator. Do not set this bit field to "00000".

The negative counter is reloaded with the value from this register when "1" is written to the corresponding ADC12Bn_PCIRQC0.PCIRQC bit or on any positive event from the appropriate range comparator.

For further explanation of negative events and operation of pulse detection function refer to section "Pulse Detection Function" in chapter "3 Operation of A/D "

[bit15:8] PCTPCT[7:0] : Pulse Positive Counter Register

This register reflects the current counter value of the pulse detection positive counter. Reload value is determined by PCTPRL.

The positive counter is reloaded under one of the following conditions:

- Writing "1" to the corresponding ADC12Bn_PCIRQC0.PCIRQC bit.
- Expiration of the corresponding negative counter (PCTNCT).

Therefore, in order to reload positive counter immediately after set to PCTPRL[7:0], the corresponding ADC12Bn_PCIRQC0.PCIRQC bit should be written "1".

[bit7:0] PCTPRL[7:0] : Pulse Positive Counter Reload Register

These register bits hold the reload value of the positive counter PCTPCT used for counting positive events of the range comparator. Do not set this bit field to "00000000".

The positive counter is reloaded with the value from this register when "1" is written to the corresponding ADC12Bn_PCIRQC0.PCIRQC bit or on expiration of the corresponding negative counter (PCTNCT).

For further explanation of positive events and operation of pulse detection function refer to section "Pulse Detection Function" in chapter "3 Operation of A/D "

5.5. A/D Conversion Done Interrupt Flag Registers (ADC12Bn_CDONEIRQ0)

A/D Conversion Done Interrupt Flag Registers ADC12Bn_CDONEIRQ0 contain the status of conversion done interrupt flags for all 32 logical channels.

REGISTER_NAME	ADC12Bn_CDONEIRQ0
OFFSET	0x0300
ACCESS_SIZE	B H W
MULTIPLE	0
NUMERIC_TYPE	-
OTHER	-

A/D Conversion Done Interrupt Flag Register (ADC12Bn_CDONEIRQ0)

BIT_OFFSET	31	30	29	28	27	26	25	24
BIT_NAME	CDONEIRQ3 1	CDONEIRQ3 0	CDONEIRQ2 9	CDONEIRQ2 8	CDONEIRQ2 7	CDONEIRQ2 6	CDONEIRQ2 5	CDONEIRQ2 4
ACCESS_TYPE	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX
PROT_TYPE								
INITIAL_VALUE	0	0	0	0	0	0	0	0

BIT_OFFSET	23	22	21	20	19	18	17	16
BIT_NAME	CDONEIRQ2 3	CDONEIRQ2 2	CDONEIRQ2 1	CDONEIRQ2 0	CDONEIRQ1 9	CDONEIRQ1 8	CDONEIRQ1 7	CDONEIRQ1 6
ACCESS_TYPE	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX
PROT_TYPE								
INITIAL_VALUE	0	0	0	0	0	0	0	0

BIT_OFFSET	15	14	13	12	11	10	9	8
BIT_NAME	CDONEIRQ1 5	CDONEIRQ1 4	CDONEIRQ1 3	CDONEIRQ1 2	CDONEIRQ1 1	CDONEIRQ1 0	CDONEIRQ9	CDONEIRQ8
ACCESS_TYPE	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX
PROT_TYPE								
INITIAL_VALUE	0	0	0	0	0	0	0	0

BIT_OFFSET	7	6	5	4	3	2	1	0
BIT_NAME	CDONEIRQ7	CDONEIRQ6	CDONEIRQ5	CDONEIRQ4	CDONEIRQ3	CDONEIRQ2	CDONEIRQ1	CDONEIRQ0
ACCESS_TYPE	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX
PROT_TYPE								
INITIAL_VALUE	0	0	0	0	0	0	0	0

[bit31:0] CDONEIRQ31~0 : Conversion Done Interrupt flags

bit	Description
0	Conversion done interrupt request not detected.
1	Conversion done interrupt request detected.

This bit is set when conversion data is stored in corresponding conversion data register ADC12Bn_CD0~31 and corresponding trigger status (ADC12Bn_TRGST0.TRGST and ADC12Bn_CHSTAT0~31.TRGST bits) is still "1".

In case of multiple conversion channels this bit is set when the last conversion is done, final conversion result is accumulated and corresponding trigger status (ADC12Bn_TRGST0.TRGST and ADC12Bn_CHSTAT0~31.TRGST bits) is still "1".

This bit is cleared by writing "1" to the corresponding ADC12Bn_CDONEIRQC0 bits or by reading the corresponding conversion data register ADC12Bn_CD0~31 (except by the debug master, DAP). All ADC12Bn_CD0~31 read access types (8/16/32-bit) clear the flag.

If this bit is set and cleared at the same time, clearing has higher priority.

This bit is identical to the CDONEIRQ bit in the corresponding ADC12Bn_CHSTAT0~31 registers.

5.6. A/D Conversion Done Interrupt Enable Registers (ADC12Bn_CDONEIRQE0)

These registers contain enable bits for all 32 logical channels, dedicated to the generation of conversion done interrupt.

REGISTER_NAME	ADC12Bn_CDONEIRQE0
OFFSET	0x0308
ACCESS_SIZE	B H W
MULTIPLE	0
NUMERIC_TYPE	-
OTHER	-

A/D Conversion Done Interrupt Enable Register (ADC12Bn_CDONEIRQE0)

BIT_OFFSET	31	30	29	28	27	26	25	24
BIT_NAME	CDONEIRQ E31	CDONEIRQ E30	CDONEIRQ E29	CDONEIRQ E28	CDONEIRQ E27	CDONEIRQ E26	CDONEIRQ E25	CDONEIRQ E24
ACCESS_TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
PROT_TYPE								
INITIAL_VALUE	0	0	0	0	0	0	0	0

BIT_OFFSET	23	22	21	20	19	18	17	16
BIT_NAME	CDONEIRQ E23	CDONEIRQ E22	CDONEIRQ E21	CDONEIRQ E20	CDONEIRQ E19	CDONEIRQ E18	CDONEIRQ E17	CDONEIRQ E16
ACCESS_TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
PROT_TYPE								
INITIAL_VALUE	0	0	0	0	0	0	0	0

BIT_OFFSET	15	14	13	12	11	10	9	8
BIT_NAME	CDONEIRQ E15	CDONEIRQ E14	CDONEIRQ E13	CDONEIRQ E12	CDONEIRQ E11	CDONEIRQ E10	CDONEIRQ E9	CDONEIRQ E8
ACCESS_TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
PROT_TYPE								
INITIAL_VALUE	0	0	0	0	0	0	0	0

BIT_OFFSET	7	6	5	4	3	2	1	0
BIT_NAME	CDONEIRQ E7	CDONEIRQ E6	CDONEIRQ E5	CDONEIRQ E4	CDONEIRQ E3	CDONEIRQ E2	CDONEIRQ E1	CDONEIRQ E0
ACCESS_TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
PROT_TYPE								
INITIAL_VALUE	0	0	0	0	0	0	0	0

[bit31:0] CDONEIRQE31~0 : Conversion Done Interrupt Enable bits

bit	Description
0	Conversion done interrupt disabled
1	Conversion done interrupt enabled.

Conversion done interrupt is issued when the bit is "1" and the corresponding interrupt flags ADC12Bn_CDONEIRQ0.CDONEIRQ31~0 and ADC12Bn_CHSTAT0~31.CDONEIRQ are set to "1".

5.7. A/D Conversion Done Interrupt Clear Registers (ADC12Bn_CDONEIRQC0)

These registers contain bits for clearing corresponding conversion done interrupt flags in the ADC12Bn_CDONEIRQ0 registers. The 32 bits are assigned to 32 logical channels.

REGISTER_NAME	ADC12Bn_CDONEIRQC0
OFFSET	0x0310
ACCESS_SIZE	B H W
MULTIPLE	0
NUMERIC_TYPE	-
OTHER	-

A/D Conversion Done Interrupt Clear Register (ADC12Bn_CDONEIRQC0)

BIT_OFFSET	31	30	29	28	27	26	25	24
BIT_NAME	CDONEIRQ C31	CDONEIRQ C30	CDONEIRQ C29	CDONEIRQ C28	CDONEIRQ C27	CDONEIRQ C26	CDONEIRQ C25	CDONEIRQ C24
ACCESS_TYPE	R0,W	R0,W	R0,W	R0,W	R0,W	R0,W	R0,W	R0,W
PROT_TYPE								
INITIAL_VALUE	0	0	0	0	0	0	0	0

BIT_OFFSET	23	22	21	20	19	18	17	16
BIT_NAME	CDONEIRQ C23	CDONEIRQ C22	CDONEIRQ C21	CDONEIRQ C20	CDONEIRQ C19	CDONEIRQ C18	CDONEIRQ C17	CDONEIRQ C16
ACCESS_TYPE	R0,W	R0,W	R0,W	R0,W	R0,W	R0,W	R0,W	R0,W
PROT_TYPE								
INITIAL_VALUE	0	0	0	0	0	0	0	0

BIT_OFFSET	15	14	13	12	11	10	9	8
BIT_NAME	CDONEIRQ C15	CDONEIRQ C14	CDONEIRQ C13	CDONEIRQ C12	CDONEIRQ C11	CDONEIRQ C10	CDONEIRQ C9	CDONEIRQ C8
ACCESS_TYPE	R0,W	R0,W	R0,W	R0,W	R0,W	R0,W	R0,W	R0,W
PROT_TYPE								
INITIAL_VALUE	0	0	0	0	0	0	0	0

BIT_OFFSET	7	6	5	4	3	2	1	0
BIT_NAME	CDONEIRQ C7	CDONEIRQ C6	CDONEIRQ C5	CDONEIRQ C4	CDONEIRQ C3	CDONEIRQ C2	CDONEIRQ C1	CDONEIRQ C0
ACCESS_TYPE	R0,W	R0,W	R0,W	R0,W	R0,W	R0,W	R0,W	R0,W
PROT_TYPE								
INITIAL_VALUE	0	0	0	0	0	0	0	0

[bit31:0] CDONEIRQC31~0 : Conversion Done Interrupt Clear bits

bit	Description
0	No effect.
1	Conversion Done Interrupt cleared.

When this bit is set to "1", the corresponding bit in the ADC12Bn_CDONEIRQ0 register and CDONEIRQ bit in the corresponding ADC12Bn_CHSTAT0~31 register are cleared.

5.8. Group interrupted Interrupt Flag Registers (ADC12Bn_GRPIRQ0)

These registers contain the status of group interrupted interrupt flags for all 32 logical channels.

REGISTER_NAME	ADC12Bn_GRPIRQ0
OFFSET	0x0318
ACCESS_SIZE	B H W
MULTIPLE	0
NUMERIC_TYPE	-
OTHER	-

Group interrupted Interrupt Flag Register (ADC12Bn_GRPIRQ0)

BIT_OFFSET	31	30	29	28	27	26	25	24
BIT_NAME	GRPIRQ31	GRPIRQ30	GRPIRQ29	GRPIRQ28	GRPIRQ27	GRPIRQ26	GRPIRQ25	GRPIRQ24
ACCESS_TYPE	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX
PROT_TYPE								
INITIAL_VALUE	0	0	0	0	0	0	0	0

BIT_OFFSET	23	22	21	20	19	18	17	16
BIT_NAME	GRPIRQ23	GRPIRQ22	GRPIRQ21	GRPIRQ20	GRPIRQ19	GRPIRQ18	GRPIRQ17	GRPIRQ16
ACCESS_TYPE	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX
PROT_TYPE								
INITIAL_VALUE	0	0	0	0	0	0	0	0

BIT_OFFSET	15	14	13	12	11	10	9	8
BIT_NAME	GRPIRQ15	GRPIRQ14	GRPIRQ13	GRPIRQ12	GRPIRQ11	GRPIRQ10	GRPIRQ9	GRPIRQ8
ACCESS_TYPE	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX
PROT_TYPE								
INITIAL_VALUE	0	0	0	0	0	0	0	0

BIT_OFFSET	7	6	5	4	3	2	1	0
BIT_NAME	GRPIRQ7	GRPIRQ6	GRPIRQ5	GRPIRQ4	GRPIRQ3	GRPIRQ2	GRPIRQ1	GRPIRQ0
ACCESS_TYPE	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX
PROT_TYPE								
INITIAL_VALUE	0	0	0	0	0	0	0	0

[bit31:0] GRPIRQ31~0 : Group Interrupted Interrupt flags

Group Interrupted Interrupt flags for the case the group gets interrupted and stopped before finishing.

bit	Description
0	Group interrupted interrupt not detected.
1	Group interrupted interrupt detected.

The bit is set to "1" if following conditions are fulfilled:

- The corresponding trigger status flags of the channel (ADC12Bn_CHSTAT0~31.TRGST and ADC12Bn_TRGST0.TRGST31~0) are set to "1"
- The channel is not first in the group i.e. the trigger type bits TRGTYP are set to "10" in the corresponding ADC12Bn_CHCTRL0~31 register
- The channel did not win arbitration for the next conversion, i.e. there was a channel with active trigger status and higher priority.

For multiple conversion logical channels, this bit is set to "1" also in the case the multiple conversions are started and they are interrupted before the last conversion is performed.

This bit is cleared by writing "1" to the corresponding ADC12Bn_GRPIRQC0 bits.

This bit is identical to the GRPIRQ bit in the corresponding ADC12Bn_CHSTAT0~31 registers

5.9. Group Interrupted Interrupt Enable Registers (ADC12Bn_GRPIRQE0)

These registers contain enable bits for all 32 logical channels, dedicated to the generation of group interrupted interrupt.

REGISTER_NAME	ADC12Bn_GRPIRQE0
OFFSET	0x0320
ACCESS_SIZE	B H W
MULTIPLE	0
NUMERIC_TYPE	-
OTHER	-

Group interrupted Interrupt Enable Register (ADC12Bn_GRPIRQE0)

BIT_OFFSET	31	30	29	28	27	26	25	24
BIT_NAME	GRPIRQE31	GRPIRQE30	GRPIRQE29	GRPIRQE28	GRPIRQE27	GRPIRQE26	GRPIRQE25	GRPIRQE24
ACCESS_TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
PROT_TYPE								
INITIAL_VALUE	0	0	0	0	0	0	0	0

BIT_OFFSET	23	22	21	20	19	18	17	16
BIT_NAME	GRPIRQE23	GRPIRQE22	GRPIRQE21	GRPIRQE20	GRPIRQE19	GRPIRQE18	GRPIRQE17	GRPIRQE16
ACCESS_TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
PROT_TYPE								
INITIAL_VALUE	0	0	0	0	0	0	0	0

BIT_OFFSET	15	14	13	12	11	10	9	8
BIT_NAME	GRPIRQE15	GRPIRQE14	GRPIRQE13	GRPIRQE12	GRPIRQE11	GRPIRQE10	GRPIRQE9	GRPIRQE8
ACCESS_TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
PROT_TYPE								
INITIAL_VALUE	0	0	0	0	0	0	0	0

BIT_OFFSET	7	6	5	4	3	2	1	0
BIT_NAME	GRPIRQE7	GRPIRQE6	GRPIRQE5	GRPIRQE4	GRPIRQE3	GRPIRQE2	GRPIRQE1	GRPIRQE0
ACCESS_TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
PROT_TYPE								
INITIAL_VALUE	0	0	0	0	0	0	0	0

[bit31:0] GRPIRQE31~0 : Group Interrupted Interrupt Enable bits

bit	Description
0	Group interrupted interrupt disabled.
1	Group interrupted interrupt enabled.

Group interrupted interrupt is issued when this bit is "1" and the corresponding interrupt flags (ADC12Bn_GRPIRQ0.GRPIRQ31~0 and ADC12Bn_CHSTAT0~31.GRPIRQ) are set to "1".

5.10. Group Interrupted Interrupt Clear Registers (ADC12Bn_GRP_IRQC0)

These registers contain bits for clearing corresponding group interrupted interrupt flags in the ADC12Bn_GRP_IRQ0 registers. The 32 bits are assigned to 32 logical channels.

REGISTER_NAME	ADC12Bn_GRP_IRQC0
OFFSET	0x0328
ACCESS_SIZE	B H W
MULTIPLE	0
NUMERIC_TYPE	-
OTHER	-

Group interrupted Interrupt Clear Register (ADC12Bn_GRP_IRQC0)

BITS_OFFSET	31	30	29	28	27	26	25	24
BITS_NAME	GRP_IRQC31	GRP_IRQC30	GRP_IRQC29	GRP_IRQC28	GRP_IRQC27	GRP_IRQC26	GRP_IRQC25	GRP_IRQC24
ACCESS_TYPE	R0,W	R0,W	R0,W	R0,W	R0,W	R0,W	R0,W	R0,W
PROT_TYPE								
INITIAL_VALUE	0	0	0	0	0	0	0	0

BITS_OFFSET	23	22	21	20	19	18	17	16
BITS_NAME	GRP_IRQC23	GRP_IRQC22	GRP_IRQC21	GRP_IRQC20	GRP_IRQC19	GRP_IRQC18	GRP_IRQC17	GRP_IRQC16
ACCESS_TYPE	R0,W	R0,W	R0,W	R0,W	R0,W	R0,W	R0,W	R0,W
PROT_TYPE								
INITIAL_VALUE	0	0	0	0	0	0	0	0

BITS_OFFSET	15	14	13	12	11	10	9	8
BITS_NAME	GRP_IRQC15	GRP_IRQC14	GRP_IRQC13	GRP_IRQC12	GRP_IRQC11	GRP_IRQC10	GRP_IRQC9	GRP_IRQC8
ACCESS_TYPE	R0,W	R0,W	R0,W	R0,W	R0,W	R0,W	R0,W	R0,W
PROT_TYPE								
INITIAL_VALUE	0	0	0	0	0	0	0	0

BITS_OFFSET	7	6	5	4	3	2	1	0
BITS_NAME	GRP_IRQC7	GRP_IRQC6	GRP_IRQC5	GRP_IRQC4	GRP_IRQC3	GRP_IRQC2	GRP_IRQC1	GRP_IRQC0
ACCESS_TYPE	R0,W	R0,W	R0,W	R0,W	R0,W	R0,W	R0,W	R0,W
PROT_TYPE								
INITIAL_VALUE	0	0	0	0	0	0	0	0

[bit31:0] GRPIRQC31~0 : Group Interrupted Clear bits

bit	Description
0	No effect.
1	Group interrupted interrupt cleared.

When this bit is set to "1", the corresponding bit in the ADC12Bn_GRPIRQ0 register and GRPIRQ bit in the corresponding ADC12Bn_CHSTAT0~31 register are cleared.

5.11. Range Comparator Interrupt Flag Registers (ADC12Bn_RCIRQ0)

Range Comparator Interrupt Flag Registers ADC12Bn_RCIRQ0 contain the status of range comparator interrupt flags for all 32 logical channels.

REGISTER_NAME	ADC12Bn_RCIRQ0
OFFSET	0x0330
ACCESS_SIZE	B H W
MULTIPLE	0
NUMERIC_TYPE	-
OTHER	-

Range Comparator Interrupt Flag Register (ADC12Bn_RCIRQ0)

BITS_OFFSET	31	30	29	28	27	26	25	24
BITS_NAME	RCIRQ31	RCIRQ30	RCIRQ29	RCIRQ28	RCIRQ27	RCIRQ26	RCIRQ25	RCIRQ24
ACCESS_TYPE	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX
PROT_TYPE								
INITIAL_VALUE	0	0	0	0	0	0	0	0

BITS_OFFSET	23	22	21	20	19	18	17	16
BITS_NAME	RCIRQ23	RCIRQ22	RCIRQ21	RCIRQ20	RCIRQ19	RCIRQ18	RCIRQ17	RCIRQ16
ACCESS_TYPE	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX
PROT_TYPE								
INITIAL_VALUE	0	0	0	0	0	0	0	0

BITS_OFFSET	15	14	13	12	11	10	9	8
BITS_NAME	RCIRQ15	RCIRQ14	RCIRQ13	RCIRQ12	RCIRQ11	RCIRQ10	RCIRQ9	RCIRQ8
ACCESS_TYPE	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX
PROT_TYPE								
INITIAL_VALUE	0	0	0	0	0	0	0	0

BITS_OFFSET	7	6	5	4	3	2	1	0
BITS_NAME	RCIRQ7	RCIRQ6	RCIRQ5	RCIRQ4	RCIRQ3	RCIRQ2	RCIRQ1	RCIRQ0
ACCESS_TYPE	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX
PROT_TYPE								
INITIAL_VALUE	0	0	0	0	0	0	0	0

[bit31:0] RCIRQ31~0 : Range Comparator Interrupt flags

bit	Description
0	Range comparator interrupt not detected.
1	Range comparator interrupt detected.

This flag shows that an outside range or inside range condition has been found on the corresponding logical channel.

This bit is set under the following conditions:

- The range comparison for this channel is enabled ADC12Bn_CHCTRL0~31.RCEN is set
- The conversion of the logical channel is just finished
- An interrupt condition is met (see Table 5-1)

This bit is cleared by writing "1" to the corresponding ADC12Bn_RCIRQC0.RCIRQC bit.

This bit is identical to the RCIRQ bit in the corresponding ADC12Bn_CHSTAT0~31 register.

Table 5-1 Range Comparator Interrupt Condition

Mode	Inverted Range Selection ADC12Bn_CHCTRL0~31.RCINVSEL	Conversion Result above Upper Threshold	Conversion Result below Lower Threshold	Interrupt Condition
outside range	0	1	x	INT condition: above range, ADC12Bn_RCOTF0.RCOTF and ADC12Bn_CHSTAT0~31.RCOTF are set.
		0	0	-
		0	1	INT condition: below range, ADC12Bn_RCOTF0.RCOTF and ADC12Bn_CHSTAT0~31.RCOTF are cleared.
inside range	1	1	x	-
		0	0	INT condition: inside range
		0	1	-

5.12. Range Comparator Interrupt Enable Registers (ADC12Bn_RCIRQE0)

These registers contain enable bits for all 32 logical channels, dedicated to the generation of range comparator interrupt.

REGISTER_NAME	ADC12Bn_RCIRQE0
OFFSET	0x0338
ACCESS_SIZE	B H W
MULTIPLE	0
NUMERIC_TYPE	-
OTHER	-

Range Comparator Interrupt Enable Register (ADC12Bn_RCIRQE0)

BIT_OFFSET	31	30	29	28	27	26	25	24
BIT_NAME	RCIRQE31	RCIRQE30	RCIRQE29	RCIRQE28	RCIRQE27	RCIRQE26	RCIRQE25	RCIRQE24
ACCESS_TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
PROT_TYPE								
INITIAL_VALUE	0	0	0	0	0	0	0	0

BIT_OFFSET	23	22	21	20	19	18	17	16
BIT_NAME	RCIRQE23	RCIRQE22	RCIRQE21	RCIRQE20	RCIRQE19	RCIRQE18	RCIRQE17	RCIRQE16
ACCESS_TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
PROT_TYPE								
INITIAL_VALUE	0	0	0	0	0	0	0	0

BIT_OFFSET	15	14	13	12	11	10	9	8
BIT_NAME	RCIRQE15	RCIRQE14	RCIRQE13	RCIRQE12	RCIRQE11	RCIRQE10	RCIRQE9	RCIRQE8
ACCESS_TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
PROT_TYPE								
INITIAL_VALUE	0	0	0	0	0	0	0	0

BIT_OFFSET	7	6	5	4	3	2	1	0
BIT_NAME	RCIRQE7	RCIRQE6	RCIRQE5	RCIRQE4	RCIRQE3	RCIRQE2	RCIRQE1	RCIRQE0
ACCESS_TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
PROT_TYPE								
INITIAL_VALUE	0	0	0	0	0	0	0	0

[bit31:0] RCIRQE31~0 : Range Comparator Interrupt Enable bits

bit	Description
0	Range comparator interrupt disabled.
1	Range comparator interrupt enabled

Range comparator interrupt is issued when this bit is "1" and the corresponding interrupt flags ADC12Bn_RCIRQ0.RCIRQ31~0 and ADC12Bn_CHSTAT0~31.RCIRQ are set to "1".

5.13. Range Comparator Interrupt Clear Registers (ADC12Bn_RCIRQC0)

These registers contain bits for clearing corresponding range comparator interrupt flags in the ADC12Bn_RCIRQC0 registers. The 32 bits are assigned to 32 logical channels.

REGISTER_NAME	ADC12Bn_RCIRQC0
OFFSET	0x0340
ACCESS_SIZE	B H W
MULTIPLE	0
NUMERIC_TYPE	-
OTHER	-

Range Comparator Interrupt Clear Register (ADC12Bn_RCIRQC0)

BIT_OFFSET	31	30	29	28	27	26	25	24
BIT_NAME	RCIRQC31	RCIRQC30	RCIRQC29	RCIRQC28	RCIRQC27	RCIRQC26	RCIRQC25	RCIRQC24
ACCESS_TYPE	R0,W	R0,W	R0,W	R0,W	R0,W	R0,W	R0,W	R0,W
PROT_TYPE								
INITIAL_VALUE	0	0	0	0	0	0	0	0

BIT_OFFSET	23	22	21	20	19	18	17	16
BIT_NAME	RCIRQC23	RCIRQC22	RCIRQC21	RCIRQC20	RCIRQC19	RCIRQC18	RCIRQC17	RCIRQC16
ACCESS_TYPE	R0,W	R0,W	R0,W	R0,W	R0,W	R0,W	R0,W	R0,W
PROT_TYPE								
INITIAL_VALUE	0	0	0	0	0	0	0	0

BIT_OFFSET	15	14	13	12	11	10	9	8
BIT_NAME	RCIRQC15	RCIRQC14	RCIRQC13	RCIRQC12	RCIRQC11	RCIRQC10	RCIRQC9	RCIRQC8
ACCESS_TYPE	R0,W	R0,W	R0,W	R0,W	R0,W	R0,W	R0,W	R0,W
PROT_TYPE								
INITIAL_VALUE	0	0	0	0	0	0	0	0

BIT_OFFSET	7	6	5	4	3	2	1	0
BIT_NAME	RCIRQC7	RCIRQC6	RCIRQC5	RCIRQC4	RCIRQC3	RCIRQC2	RCIRQC1	RCIRQC0
ACCESS_TYPE	R0,W	R0,W	R0,W	R0,W	R0,W	R0,W	R0,W	R0,W
PROT_TYPE								
INITIAL_VALUE	0	0	0	0	0	0	0	0

[bit31:0] RCIRQC31~0 : Range Comparator Interrupt Clear bits

bit	Description
0	No effect.
1	Range comparator interrupt cleared.

When this bit is set to "1", the corresponding bit in the ADC12Bn_RCIRQC0 register and RCIRQC bit in the corresponding ADC12Bn_CHSTAT0~31 register are cleared.

5.14. Pulse Counter Interrupt Flag Registers (ADC12Bn_PCIRQ0)

Pulse Comparator Interrupt Flag Registers ADC12Bn_PCIRQ0 contain the status of pulse counter interrupt flags for all 32 logical channels.

REGISTER_NAME	ADC12Bn_PCIRQ0
OFFSET	0x0348
ACCESS_SIZE	B H W
MULTIPLE	0
NUMERIC_TYPE	-
OTHER	-

Pulse Counter Interrupt Flag Register (ADC12Bn_PCIRQ0)

BIT_OFFSET	31	30	29	28	27	26	25	24
BIT_NAME	PCIRQ31	PCIRQ30	PCIRQ29	PCIRQ28	PCIRQ27	PCIRQ26	PCIRQ25	PCIRQ24
ACCESS_TYPE	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX
PROT_TYPE								
INITIAL_VALUE	0	0	0	0	0	0	0	0

BIT_OFFSET	23	22	21	20	19	18	17	16
BIT_NAME	PCIRQ23	PCIRQ22	PCIRQ21	PCIRQ20	PCIRQ19	PCIRQ18	PCIRQ17	PCIRQ16
ACCESS_TYPE	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX
PROT_TYPE								
INITIAL_VALUE	0	0	0	0	0	0	0	0

BIT_OFFSET	15	14	13	12	11	10	9	8
BIT_NAME	PCIRQ15	PCIRQ14	PCIRQ13	PCIRQ12	PCIRQ11	PCIRQ10	PCIRQ9	PCIRQ8
ACCESS_TYPE	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX
PROT_TYPE								
INITIAL_VALUE	0	0	0	0	0	0	0	0

BIT_OFFSET	7	6	5	4	3	2	1	0
BIT_NAME	PCIRQ7	PCIRQ6	PCIRQ5	PCIRQ4	PCIRQ3	PCIRQ2	PCIRQ1	PCIRQ0
ACCESS_TYPE	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX
PROT_TYPE								
INITIAL_VALUE	0	0	0	0	0	0	0	0

[bit31:0] PCIRQ31~0 : Pulse Counter Interrupt flags

bit	Description
0	Pulse counter interrupt not detected.
1	Pulse counter interrupt detected.

This register returns the status of the pulse counter interrupt flag which is set when positive counter ADC12Bn_PCCTRL0~31.PCTPCT of the corresponding logical channel decrements to zero. The positive counter and negative counter are stopped as long as the pulse counter interrupt flag of the appropriate channel is set.

This bit is cleared by writing "1" to the corresponding bit in the ADC12Bn_PCIRQC0 register.

This bit is identical to the PCIRQ bit in the corresponding ADC12Bn_CHSTAT0~31 register.

5.15. Pulse Counter Interrupt Enable Registers (ADC12Bn_PCIRQE0)

These registers contain enable bits for all 32 logical channels, dedicated to the generation of pulse counter interrupt.

REGISTER_NAME	ADC12Bn_PCIRQE0
OFFSET	0x0350
ACCESS_SIZE	B H W
MULTIPLE	0
NUMERIC_TYPE	-
OTHER	-

Pulse Counter Interrupt Enable Register (ADC12Bn_PCIRQE0)

BIT_OFFSET	31	30	29	28	27	26	25	24
BIT_NAME	PCIRQE31	PCIRQE30	PCIRQE29	PCIRQE28	PCIRQE27	PCIRQE26	PCIRQE25	PCIRQE24
ACCESS_TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
PROT_TYPE								
INITIAL_VALUE	0	0	0	0	0	0	0	0

BIT_OFFSET	23	22	21	20	19	18	17	16
BIT_NAME	PCIRQE23	PCIRQE22	PCIRQE21	PCIRQE20	PCIRQE19	PCIRQE18	PCIRQE17	PCIRQE16
ACCESS_TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
PROT_TYPE								
INITIAL_VALUE	0	0	0	0	0	0	0	0

BIT_OFFSET	15	14	13	12	11	10	9	8
BIT_NAME	PCIRQE15	PCIRQE14	PCIRQE13	PCIRQE12	PCIRQE11	PCIRQE10	PCIRQE9	PCIRQE8
ACCESS_TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
PROT_TYPE								
INITIAL_VALUE	0	0	0	0	0	0	0	0

BIT_OFFSET	7	6	5	4	3	2	1	0
BIT_NAME	PCIRQE7	PCIRQE6	PCIRQE5	PCIRQE4	PCIRQE3	PCIRQE2	PCIRQE1	PCIRQE0
ACCESS_TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
PROT_TYPE								
INITIAL_VALUE	0	0	0	0	0	0	0	0

[bit31:0] PCIRQE31~0 : Pulse Counter Interrupt Enable bits

bit	Description
0	Pulse counter interrupt is disabled.
1	Pulse counter interrupt is enabled.

Pulse counter interrupt is issued when this bit is "1" and the corresponding interrupt flags ADC12Bn_PCIRQ0.PCIRQ31~0 and ADC12Bn_CHSTAT0~31.PCIRQ are set to "1".

5.16. Pulse Counter Interrupt Clear Registers (ADC12Bn_PCIRQC0)

These registers contain bits for clearing corresponding pulse counter interrupt flags in the ADC12Bn_PCIRQC0 registers. The 32 bits are assigned to 32 logical channels.

REGISTER_NAME	ADC12Bn_PCIRQC0
OFFSET	0x0358
ACCESS_SIZE	B H W
MULTIPLE	0
NUMERIC_TYPE	-
OTHER	-

Pulse Counter Interrupt Clear Register (ADC12Bn_PCIRQC0)

BIT_OFFSET	31	30	29	28	27	26	25	24
BIT_NAME	PCIRQC31	PCIRQC30	PCIRQC29	PCIRQC28	PCIRQC27	PCIRQC26	PCIRQC25	PCIRQC24
ACCESS_TYPE	R0,W	R0,W	R0,W	R0,W	R0,W	R0,W	R0,W	R0,W
PROT_TYPE								
INITIAL_VALUE	0	0	0	0	0	0	0	0

BIT_OFFSET	23	22	21	20	19	18	17	16
BIT_NAME	PCIRQC23	PCIRQC22	PCIRQC21	PCIRQC20	PCIRQC19	PCIRQC18	PCIRQC17	PCIRQC16
ACCESS_TYPE	R0,W	R0,W	R0,W	R0,W	R0,W	R0,W	R0,W	R0,W
PROT_TYPE								
INITIAL_VALUE	0	0	0	0	0	0	0	0

BIT_OFFSET	15	14	13	12	11	10	9	8
BIT_NAME	PCIRQC15	PCIRQC14	PCIRQC13	PCIRQC12	PCIRQC11	PCIRQC10	PCIRQC9	PCIRQC8
ACCESS_TYPE	R0,W	R0,W	R0,W	R0,W	R0,W	R0,W	R0,W	R0,W
PROT_TYPE								
INITIAL_VALUE	0	0	0	0	0	0	0	0

BIT_OFFSET	7	6	5	4	3	2	1	0
BIT_NAME	PCIRQC7	PCIRQC6	PCIRQC5	PCIRQC4	PCIRQC3	PCIRQC2	PCIRQC1	PCIRQC0
ACCESS_TYPE	R0,W	R0,W	R0,W	R0,W	R0,W	R0,W	R0,W	R0,W
PROT_TYPE								
INITIAL_VALUE	0	0	0	0	0	0	0	0

[bit31:0] PCIRQC31~0 : ADC Pulse Counter Interrupt Clear bits

bit	Description
0	No effect.
1	Pulse counter interrupt cleared.

When this bit is set to "1", the corresponding bit in the ADC12Bn_PCIRQ0 register and PCIRQ bit in the corresponding ADC12Bn_CHSTAT0~31 register are cleared.

Additionally, the corresponding positive and negative counter (ADC12Bn_PCCTRL0~31.PCTPCT and ADC12Bn_PCCTRL0~31.PCTNCT) are reloaded with their reload values defined in the ADC12Bn_PCCTRL0~31.PCTPRL and ADC12Bn_PCCTRL0~31.PCTNRL.

5.17. A/D Channel Trigger Status Flag Registers (ADC12Bn_TRGST0)

A/D Channel Trigger Status Flag Registers ADC12Bn_TRGST0 contain the status of conversion requests for all 32 logical channels.

REGISTER_NAME	ADC12Bn_TRGST0
OFFSET	0x0360
ACCESS_SIZE	B H W
MULTIPLE	0
NUMERIC_TYPE	-
OTHER	-

A/D Channel Trigger Status Flag Register (ADC12Bn_TRGST0)

BIT_OFFSET	31	30	29	28	27	26	25	24
BIT_NAME	TRGST31	TRGST30	TRGST29	TRGST28	TRGST27	TRGST26	TRGST25	TRGST24
ACCESS_TYPE	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX
PROT_TYPE								
INITIAL_VALUE	0	0	0	0	0	0	0	0

BIT_OFFSET	23	22	21	20	19	18	17	16
BIT_NAME	TRGST23	TRGST22	TRGST21	TRGST20	TRGST19	TRGST18	TRGST17	TRGST16
ACCESS_TYPE	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX
PROT_TYPE								
INITIAL_VALUE	0	0	0	0	0	0	0	0

BIT_OFFSET	15	14	13	12	11	10	9	8
BIT_NAME	TRGST15	TRGST14	TRGST13	TRGST12	TRGST11	TRGST10	TRGST9	TRGST8
ACCESS_TYPE	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX
PROT_TYPE								
INITIAL_VALUE	0	0	0	0	0	0	0	0

BIT_OFFSET	7	6	5	4	3	2	1	0
BIT_NAME	TRGST7	TRGST6	TRGST5	TRGST4	TRGST3	TRGST2	TRGST1	TRGST0
ACCESS_TYPE	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX
PROT_TYPE								
INITIAL_VALUE	0	0	0	0	0	0	0	0

[bit31:0] TRGST31~0 : A/D Channel Trigger Status flags

bit	Description
0	No conversion request.
1	Conversion request is issued.

This bit is set if any conversion request, dedicated to the corresponding logical channel, occurs (software, hardware, trigger by completion of preceding channel or idle trigger). Moreover, the bit is set if:

- The group of the corresponding logical channel is interrupted which configured as "restart" channel (ADC12Bn_CHCTRL0~31.RSMRST = "10")
- The channel is the start channel of the group or the last already converted channel configured as "resume" channel (ADC12Bn_CHCTRL0~31.RSMRST = "01").

This bit is cleared under one of the following conditions:

- Completion of the logical channel conversion (the last conversion in the case of multiple conversion channels), at the same time the conversion done interrupt flag is set
- The corresponding group processing is interrupted and the channel is not configured as "resume" channel (ADC12Bn_CHCTRL0~31.RSMRST = "01"). Instead, the group interrupted interrupt flag is set
- Writing "1" to the corresponding bit in the ADC12Bn_TRGCL0 register or writing "1" to the corresponding ADC12Bn_CHCTRL0~31.TRGCL bit.

When setting and clearing of the bit takes place at the same time, clearing has priority.

This bit is identical to the TRGST bit in the corresponding ADC12Bn_CHSTAT0~31 register.

5.18. A/D Channel Trigger Clear Registers (ADC12Bn_TRGCL0)

These registers contain bits for clearing corresponding A/D channel trigger status flags in the ADC12Bn_TRGST0 registers. The 32 bits are assigned to 32 logical channels.

REGISTER_NAME	ADC12Bn_TRGCL0
OFFSET	0x0368
ACCESS_SIZE	B H W
MULTIPLE	0
NUMERIC_TYPE	-
OTHER	-

A/D Channel Trigger Clear Register (ADC12Bn_TRGCL0)

BIT_OFFSET	31	30	29	28	27	26	25	24
BIT_NAME	TRGCL31	TRGCL30	TRGCL29	TRGCL28	TRGCL27	TRGCL26	TRGCL25	TRGCL24
ACCESS_TYPE	R0,W	R0,W	R0,W	R0,W	R0,W	R0,W	R0,W	R0,W
PROT_TYPE								
INITIAL_VALUE	0	0	0	0	0	0	0	0

BIT_OFFSET	23	22	21	20	19	18	17	16
BIT_NAME	TRGCL23	TRGCL22	TRGCL21	TRGCL20	TRGCL19	TRGCL18	TRGCL17	TRGCL16
ACCESS_TYPE	R0,W	R0,W	R0,W	R0,W	R0,W	R0,W	R0,W	R0,W
PROT_TYPE								
INITIAL_VALUE	0	0	0	0	0	0	0	0

BIT_OFFSET	15	14	13	12	11	10	9	8
BIT_NAME	TRGCL15	TRGCL14	TRGCL13	TRGCL12	TRGCL11	TRGCL10	TRGCL9	TRGCL8
ACCESS_TYPE	R0,W	R0,W	R0,W	R0,W	R0,W	R0,W	R0,W	R0,W
PROT_TYPE								
INITIAL_VALUE	0	0	0	0	0	0	0	0

BIT_OFFSET	7	6	5	4	3	2	1	0
BIT_NAME	TRGCL7	TRGCL6	TRGCL5	TRGCL4	TRGCL3	TRGCL2	TRGCL1	TRGCL0
ACCESS_TYPE	R0,W	R0,W	R0,W	R0,W	R0,W	R0,W	R0,W	R0,W
PROT_TYPE								
INITIAL_VALUE	0	0	0	0	0	0	0	0

[bit31:0] TRGCL31~0 : Trigger Status Clear bits

bit	Description
0	No effect.
1	A/D channel trigger status is cleared.

When this bit is set to "1", the corresponding bit in the ADC12Bn_TRGST0 register and TRGST bit in the corresponding ADC12Bn_CHSTAT0~31 register are cleared.

If the corresponding trigger status is cleared during A/D conversion, the operation is dependent on the setting of forced stop mode (ADC12Bn_CTRL.FSMD).

- Forced stop is enabled (ADC12Bn_CTRL.FSMD = "1"): A/D conversion is stopped after interrupt operation.
- Forced stop is disabled (ADC12Bn_CTRL.FSMD = "0"): A/D conversion is not stopped (but A/D conversion result is not updated). Hence, when the next conversion is already requested, the wait time from trigger status flag clear to the start of next conversion can be up to the maximum A/D conversion period.

This bit is identical to the TRGCL bit in the corresponding ADC12Bn_CHCTRL0~31 register.

Note:

- *If forced stop is disabled (ADC12Bn_CTRL.FSMD = "0"), do not set trigger status flag again during the same conversion after the trigger status is cleared.
Please set again after the end timing of the cleared conversion.*

5.19. A/D Channel Trigger Overrun Flag Registers (ADC12Bn_TRGOR0)

A/D Channel Trigger Overrun Flag Registers ADC12Bn_TRGOR0 register the possible trials to set already active (set to "1") trigger status for all 32 logical channels.

REGISTER_NAME	ADC12Bn_TRGOR0
OFFSET	0x0378
ACCESS_SIZE	B H W
MULTIPLE	0
NUMERIC_TYPE	-
OTHER	-

A/D Channel Trigger Overrun Flag Register (ADC12Bn_TRGOR0)

BIT_OFFSET	31	30	29	28	27	26	25	24
BIT_NAME	TRGOR31	TRGOR30	TRGOR29	TRGOR28	TRGOR27	TRGOR26	TRGOR25	TRGOR24
ACCESS_TYPE	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX
PROT_TYPE								
INITIAL_VALUE	0	0	0	0	0	0	0	0

BIT_OFFSET	23	22	21	20	19	18	17	16
BIT_NAME	TRGOR23	TRGOR22	TRGOR21	TRGOR20	TRGOR19	TRGOR18	TRGOR17	TRGOR16
ACCESS_TYPE	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX
PROT_TYPE								
INITIAL_VALUE	0	0	0	0	0	0	0	0

BIT_OFFSET	15	14	13	12	11	10	9	8
BIT_NAME	TRGOR15	TRGOR14	TRGOR13	TRGOR12	TRGOR11	TRGOR10	TRGOR9	TRGOR8
ACCESS_TYPE	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX
PROT_TYPE								
INITIAL_VALUE	0	0	0	0	0	0	0	0

BIT_OFFSET	7	6	5	4	3	2	1	0
BIT_NAME	TRGOR7	TRGOR6	TRGOR5	TRGOR4	TRGOR3	TRGOR2	TRGOR1	TRGOR0
ACCESS_TYPE	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX
PROT_TYPE								
INITIAL_VALUE	0	0	0	0	0	0	0	0

[bit31:0] TRGOR31~0 : A/D Channel Trigger Overrun flags

bit	Description
0	No trigger overrun happened
1	Trigger overrun occurred

This bit is set to "1" under following conditions:

- Conversion request is issued although the corresponding trigger status bits ADC12Bn_TRGST0.TRGST and ADC12Bn_CHSTAT0~31.TRGST are already set to "1"
- Software and hardware trigger are issued at the same cycle and corresponding trigger type ADC12Bn_CHCTRL0~31.TRGTYP[1:0] is set to "01"

Writing "1" to the corresponding bit in the ADC12Bn_TRGORC0 register clears this bit.

5.20. A/D Channel Trigger Overrun Clear Registers (ADC12Bn_TRGORC0)

These registers contain bits for clearing corresponding A/D channel trigger overrun flags in the ADC12Bn_TRGOR0 registers. The 32 bits are assigned to 32 logical channels.

REGISTER_NAME	ADC12Bn_TRGORC0
OFFSET	0x0380
ACCESS_SIZE	B H W
MULTIPLE	0
NUMERIC_TYPE	-
OTHER	-

A/D Channel Trigger Overrun Clear Register (ADC12Bn_TRGORC0)

BIT_OFFSET	31	30	29	28	27	26	25	24
BIT_NAME	TRGORC31	TRGORC30	TRGORC29	TRGORC28	TRGORC27	TRGORC26	TRGORC25	TRGORC24
ACCESS_TYPE	R0,W	R0,W	R0,W	R0,W	R0,W	R0,W	R0,W	R0,W
PROT_TYPE								
INITIAL_VALUE	0	0	0	0	0	0	0	0

BIT_OFFSET	23	22	21	20	19	18	17	16
BIT_NAME	TRGORC23	TRGORC22	TRGORC21	TRGORC20	TRGORC19	TRGORC18	TRGORC17	TRGORC16
ACCESS_TYPE	R0,W	R0,W	R0,W	R0,W	R0,W	R0,W	R0,W	R0,W
PROT_TYPE								
INITIAL_VALUE	0	0	0	0	0	0	0	0

BIT_OFFSET	15	14	13	12	11	10	9	8
BIT_NAME	TRGORC15	TRGORC14	TRGORC13	TRGORC12	TRGORC11	TRGORC10	TRGORC9	TRGORC8
ACCESS_TYPE	R0,W	R0,W	R0,W	R0,W	R0,W	R0,W	R0,W	R0,W
PROT_TYPE								
INITIAL_VALUE	0	0	0	0	0	0	0	0

BIT_OFFSET	7	6	5	4	3	2	1	0
BIT_NAME	TRGORC7	TRGORC6	TRGORC5	TRGORC4	TRGORC3	TRGORC2	TRGORC1	TRGORC0
ACCESS_TYPE	R0,W	R0,W	R0,W	R0,W	R0,W	R0,W	R0,W	R0,W
PROT_TYPE								
INITIAL_VALUE	0	0	0	0	0	0	0	0

[bit31:0] TRGORC31~0 : Trigger Overrun Clear bits

bit	Description
0	No effect.
1	Trigger overrun flag is cleared.

When this bit is set to "1", the corresponding bit in the ADC12Bn_TRGOR0 register is cleared.

5.21. Range Comparator Over Threshold Flag Registers (ADC12Bn_RCOTF0)

The flag bits (ADC12Bn_RCOTF0) are set when the result of the range comparator is "outside range" and the converted value is above the value of the upper threshold register.

REGISTER_NAME	ADC12Bn_RCOTF0
OFFSET	0x0370
ACCESS_SIZE	B H W
MULTIPLE	0
NUMERIC_TYPE	-
OTHER	-

Range Comparator Over Threshold Flag Register (ADC12Bn_RCOTF0)

BIT_OFFSET	31	30	29	28	27	26	25	24
BIT_NAME	RCOTF31	RCOTF30	RCOTF29	RCOTF28	RCOTF27	RCOTF26	RCOTF25	RCOTF24
ACCESS_TYPE	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX
PROT_TYPE								
INITIAL_VALUE	0	0	0	0	0	0	0	0

BIT_OFFSET	23	22	21	20	19	18	17	16
BIT_NAME	RCOTF23	RCOTF22	RCOTF21	RCOTF20	RCOTF19	RCOTF18	RCOTF17	RCOTF16
ACCESS_TYPE	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX
PROT_TYPE								
INITIAL_VALUE	0	0	0	0	0	0	0	0

BIT_OFFSET	15	14	13	12	11	10	9	8
BIT_NAME	RCOTF15	RCOTF14	RCOTF13	RCOTF12	RCOTF11	RCOTF10	RCOTF9	RCOTF8
ACCESS_TYPE	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX
PROT_TYPE								
INITIAL_VALUE	0	0	0	0	0	0	0	0

BIT_OFFSET	7	6	5	4	3	2	1	0
BIT_NAME	RCOTF7	RCOTF6	RCOTF5	RCOTF4	RCOTF3	RCOTF2	RCOTF1	RCOTF0
ACCESS_TYPE	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX
PROT_TYPE								
INITIAL_VALUE	0	0	0	0	0	0	0	0

[bit31:0] RCOTF31~0 : Range Comparator Over Threshold flags

The flag is only applicable in "outside range" mode i.e. while the RCINVSEL bit in the corresponding ADC12Bn_CHCTRL0~31 register is "0". If a range comparator interrupt is signaled (corresponding bits ADC12Bn_RCIRQ0.RCIRQ31~0 = ADC12Bn_CHSTAT0~31.RCIRQ = "1"), this flag has the following meaning:

bit	Description
0	The conversion result is less than or equal to the upper threshold.
1	The conversion result is above the upper threshold.

This bit is updated only in the case the corresponding interrupt flag (ADC12Bn_RCIRQ0.RCIRQ, ADC12Bn_CHSTAT0~31.RCIRQ) has a rising edge.

This bit is identical to the RCOTF bit in the corresponding ADC12Bn_CHSTAT0~31 register.

5.22. Conversion Done DMA Select Registers (ADC12Bn_CDDS0~3)

These four registers specify four logical channels whose conversion done interrupt flags can initiate DMA requests to transfer A/D conversion results to memory. Only ADC12Bn_CDDS0 register is described here. Other registers (ADC12Bn_CDDS1, ADC12Bn_CDDS2 and ADC12Bn_CDDS3) have identical bit fields.

REGISTER_NAME	ADC12Bn_CDDSi (i = 0~3)
OFFSET	0x0388 + i*2
ACCESS_SIZE	B H W
MULTIPLE	0:3
NUMERIC_TYPE	-
OTHER	-

Conversion Done DMA Select Register (ADC12Bn_CDDS0)

BIT_OFFSET	15	14	13	12	11	10	9	8
BIT_NAME	Reserved							
ACCESS_TYPE	R0,W0							
PROT_TYPE								
INITIAL_VALUE	0x00							

BIT_OFFSET	7	6	5	4	3	2	1	0
BIT_NAME	Reserved	CDCHEN	CDCHNUM[5]	CDCHNUM[4]	CDCHNUM[3]	CDCHNUM[2]	CDCHNUM[1]	CDCHNUM[0]
			]	]	]	]	]	]
ACCESS_TYPE	R0,W0	R/W	R/W	R/W	R/W	R/W	R/W	R/W
PROT_TYPE								
INITIAL_VALUE	0	0	0	0	0	0	0	0

[bit15:7] Reserved : Reserved bits

When writing, always write "0".

When reading, "0" is always read.

[bit6] CDCHEN : Channel conversion done DMA dedicated interrupt enable bit

bit	Description
0	Interrupt for triggering DMA request on conversion done interrupt flag (ADC12Bn_CHSTAT0~31.CDONEIRQ = ADC12Bn_CDONEIRQ0.CDONEIRQ = "1") of the logical channel defined by CDCHNUM bits is disabled.
1	Interrupt for triggering DMA request on conversion done interrupt flag (ADC12Bn_CHSTAT0~31.CDONEIRQ = ADC12Bn_CDONEIRQ0.CDONEIRQ = "1") of the logical channel defined by CDCHNUM bits is enabled.

[bit5:0] CDCHNUM[5:0] : Number of the logical channel selected for conversion done interrupt for triggering a DMA request

CDCHNUM[5:0]	Description
000000	Logical channel 0 selected.
000001	Logical channel 1 selected.
...	...
011111	Logical channel 31 selected.
100000~111111	Setting is prohibited.

The conversion done interrupts of the group last logical channels are good candidates for DMA burst setup, since the group result registers can be read linearly.

5.23. A/D Converter Comparison Time Setting Register (ADC12Bn_CT)

ADC12Bn_CT register specifies the comparison time of the A/D converter. It is not allowed to update the value of this register during A/D conversion operation (ADC12Bn_TRGST0.TRGST and ADC12Bn_CHSTAT0~31.TRGST="1").

REGISTER_NAME	ADC12Bn_CT
OFFSET	0x0390
ACCESS_SIZE	B H W
MULTIPLE	1
NUMERIC_TYPE	-
OTHER	-

A/D Converter Comparison Time Setting Register (ADC12Bn_CT)

BIT_OFFSET	15	14	13	12	11	10	9	8
BIT_NAME	CT[15]	CT[14]	CT[13]	CT[12]	CT[11]	CT[10]	CT[9]	CT[8]
ACCESS_TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
PROT_TYPE								
INITIAL_VALUE	0	0	0	0	0	0	0	0

BIT_OFFSET	7	6	5	4	3	2	1	0
BIT_NAME	CT[7]	CT[6]	CT[5]	CT[4]	CT[3]	CT[2]	CT[1]	CT[0]
ACCESS_TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
PROT_TYPE								
INITIAL_VALUE	0	0	0	0	0	1	0	0

[bit15:0] CT[15:0] : A/D Converter Comparison Time Setting bits

These bits specify the comparison phase time.

If [CT value < 4]: Comparison time = (CT value x 12 + 4) x Peripheral clock period

If [CT value ≥ 4]: Comparison time = (CT value x 13) x Peripheral clock period

Do not set CT value to 0.

For specific values of minimum and maximum comparison time, please refer to the Device Data Sheet.

5.24. A/D Converter Resumption Time Setting Register (ADC12Bn_RT)

ADC12Bn_RT register specifies the resumption time of the A/D converter. It is not allowed to update the value of this register during A/D conversion operation (ADC12Bn_TRGST0.TRGST and ADC12Bn_CHSTAT0~31.TRGST="1").

REGISTER_NAME	ADC12Bn_RT
OFFSET	0x0392
ACCESS_SIZE	B H W
MULTIPLE	1
NUMERIC_TYPE	-
OTHER	-

A/D Converter Resumption Time Setting Register (ADC12Bn_RT)

BIT_OFFSET	15	14	13	12	11	10	9	8
BIT_NAME	Reserved							
ACCESS_TYPE	R0,W0							
PROT_TYPE								
INITIAL_VALUE	0x00							

BIT_OFFSET	7	6	5	4	3	2	1	0
BIT_NAME	RT[7]	RT[6]	RT[5]	RT[4]	RT[3]	RT[2]	RT[1]	RT[0]
ACCESS_TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
PROT_TYPE								
INITIAL_VALUE	0	0	1	1	1	1	1	1

[bit15:8] Reserved : Reserved bits

When writing, always write "0".

When reading, "0" is always read.

[bit7:0] RT[7:0] : A/D Converter Resumption Time Setting bits

These bits specify the resumption phase time (power-up wait time).

Please set RT value is longer than the specific values of maximum resumption time.

Do not set RT value to 0.

RT value $\geq$ Maximum resumption time / Peripheral clock period.

For specific values of maximum resumption time, please refer to the Device Data Sheet.

5.25. A/D Converter Sampling Time Setting Registers (ADC12Bn_ST0~3)

ADC12Bn_ST0~3 registers specify four different settings for the selection of the sampling time of the A/D converter. It is not allowed to update the value of these registers during A/D sampling operation (ADC12Bn_TRGST0.TRGST and ADC12Bn_CHSTAT0~31.TRGST="1"). Only ADC12Bn_ST0 register is described here. Other registers (ADC12Bn_ST1, ADC12Bn_ST2 and ADC12Bn_ST3) have similar bit fields.

REGISTER_NAME	ADC12Bn_STi (i = 0~3)
OFFSET	0x0394 + i*2
ACCESS_SIZE	B H W
MULTIPLE	0:3
NUMERIC_TYPE	-
OTHER	-

A/D Converter Sampling Time Setting Register (ADC12Bn_ST0)

BIT_OFFSET	15	14	13	12	11	10	9	8
BIT_NAME	ST[15]	ST[14]	ST[13]	ST[12]	ST[11]	ST[10]	ST[9]	ST[8]
ACCESS_TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
PROT_TYPE								
INITIAL_VALUE	0	0	0	0	0	0	0	0

BIT_OFFSET	7	6	5	4	3	2	1	0
BIT_NAME	ST[7]	ST[6]	ST[5]	ST[4]	ST[3]	ST[2]	ST[1]	ST[0]
ACCESS_TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
PROT_TYPE								
INITIAL_VALUE	0	0	1	0	1	1	0	0

[bit15:0] ST[15:0] : A/D Converter Sampling Time Setting bits

These bits specify one of the four available settings for A/D converter sampling phase time.

This time is selected for a logical channel conversion by configuring the corresponding logical channel register field ADC12Bn_CHCTRL0~31.SMTIME to "00".

Sampling time = ST value x Peripheral clock period

Do not set ST value below 6.

For specific values of minimum sampling time, please refer to the Device Data Sheet.

5.26. A/D Converter Offset Compensation Setting Register (ADC12Bn_OCV)

The global register ADC12Bn_OCV specifies the setting for offset compensation value.

REGISTER_NAME	ADC12Bn_OCV
OFFSET	0x039C
ACCESS_SIZE	B H W
MULTIPLE	1
NUMERIC_TYPE	-
OTHER	-

A/D Converter Offset Compensation Setting Register (ADC12Bn_OCV)

BIT_OFFSET	15	14	13	12	11	10	9	8
BIT_NAME	Reserved							
ACCESS_TYPE	R0,W0							
PROT_TYPE								
INITIAL_VALUE	0x00							

BIT_OFFSET	7	6	5	4	3	2	1	0
BIT_NAME	OCV[7]	OCV[6]	OCV[5]	OCV[4]	OCV[3]	OCV[2]	OCV[1]	OCV[0]
ACCESS_TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
PROT_TYPE								
INITIAL_VALUE	0	0	0	0	0	0	1	0

[bit15:8] Reserved : Reserved bits

When writing, always write "0".

When reading, "0" is always read.

[bit7:0] OCV[7:0] : Offset Compensation Value

The A/D Converter can be configured to convert the values of its reference voltages AVRH and AVRL in order to calculate the offset compensation value.

After A/D Converter calibration, the calculated offset compensation value must be written to this register.

For further explanation of A/D Converter calibration refer to section "A/D Converter Calibration" in chapter "3 Operation of A/D".

Note:

- It is possible to choose the value of this register or the proper trimming value as A/D Converter offset compensation value.
- It is necessary that OCVSEL bit in 4.3.A/D Conversion Offset Compensation value Select Register (PWU_ADOCS) is set to "0" before A/D Converter calibration is performed.

For details on A/D Converter Offset value, see the following section "4.3. A/D Conversion Offset Compensation value Select Register " in the chapter of "Partial Wakeup Control" on this manual.

5.27. A/D Converter Gain Compensation Setting Register (ADC12Bn_GCV)

This register ADC12Bn_GCV specifies the setting for gain compensation value.

REGISTER_NAME	ADC12Bn_GCV
OFFSET	0x039E
ACCESS_SIZE	B H W
MULTIPLE	1
NUMERIC_TYPE	-
OTHER	-

A/D Converter Gain Compensation Setting Register (ADC12Bn_GCV)

BIT_OFFSET	15	14	13	12	11	10	9	8
BIT_NAME	Reserved							
ACCESS_TYPE	R0,W0							
PROT_TYPE								
INITIAL_VALUE	0x00							

BIT_OFFSET	7	6	5	4	3	2	1	0
BIT_NAME	Reserved			GCV[4]	GCV[3]	GCV[2]	GCV[1]	GCV[0]
ACCESS_TYPE	R0,W0			R/W	R/W	R/W	R/W	R/W
PROT_TYPE								
INITIAL_VALUE	000			0	0	0	0	0

[bit15:5] Reserved : Reserved bits

When writing, always write "0".

When reading, "0" is always read.

[bit4:0] GCV[4:0] : Gain Compensation Value

The A/D Converter can be configured to convert the values of its reference voltages AVR_H and AVR_L in order to calculate the gain compensation value.

After A/D Converter calibration, the calculated gain compensation value must be written to this register.

For further explanation of A/D Converter calibration refer to section "A/D Converter Calibration" in chapter "3 Operation of A/D".

5.28. A/D Converter Global Control Register (ADC12Bn_CTRL)

The register configures the global control settings of the A/D Converter: A/D conversion resolution, enabling of the debug feature and the mode of ADC12Bn_STAT.ACH bits, forced stop mode and request, full range comparator mode, and power-down disable mode.

REGISTER_NAME	ADC12Bn_CTRL
OFFSET	0x03A0
ACCESS_SIZE	B H W
MULTIPLE	1
NUMERIC_TYPE	-
OTHER	-

A/D Converter Global Control Register (ADC12Bn_CTRL)

BIT_OFFSET	15	14	13	12	11	10	9	8
BIT_NAME	Reserved							
ACCESS_TYPE	R0,W0							
PROT_TYPE								
INITIAL_VALUE	0x00							

BIT_OFFSET	7	6	5	4	3	2	1	0
BIT_NAME	PDDMD	FSTP	FRCMD	FSMD	ACHMD	DBGE	RES[1]	RES[0]
ACCESS_TYPE	R/W	R0,W	R/W	R/W	R/W	R/W	R/W	R/W
PROT_TYPE								
INITIAL_VALUE	0	0	0	0	0	0	0	0

[bit15:8] Reserved : Reserved bits

When writing, always write "0".

When reading, "0" is always read.

[bit7] PDDMD : Power-down disable mode

bit	Description
0	A/D converter goes to idle (power-down) state after A/D conversion finished (and next conversion is not requested).
1	A/D convertor does not go idle (power-down) state after A/D conversion finished (and next conversion is not requested). It can start A/D sampling without the resumption time.

Note:

- At the following case, even if the power-down mode is disabled (PDDMD="1"), A/D converter is waited until resumption time.
- A/D converter is in idle (power-down) state.
- PDDMD is change "0" to "1".

[bit6] FSTP : Forced stop

When the forced stop mode (FSMD = "1"):

bit	Description	
	Read	Write
0	The value is always "0"	No effect.
1		Request forced stop of A/D conversion.

When the "not" forced stop mode (FSMD = "0"):

"0" is always read from this bit. Writing "0" or "1" to this bit has no effect.

[bit5] FRCMD : Full Range Comparator mode

bit	Description
0	8-bit range comparator mode. ADC12Bn_RCOH and ADC12Bn_RCOL are used for 8-bit range comparator. ADC12Bn_FRCOH0~7 and ADC12Bn_FRCOL0~7 are not used.
1	12-bit range comparator mode. ADC12Bn_RCOH and ADC12Bn_RCOL are not used. ADC12Bn_FRCOH0~7 and ADC12Bn_FRCOL0~7 are used for 12-bit range comparator.

[bit4] FSMD : Forced stop mode

bit	Description
0	The forced stop mode is disabled. - An active A/D conversion cannot be interrupted. - Request forced stop of A/D conversion is disabled.
1	The forced stop mode is enabled. - An active A/D conversion can be interrupted. - Request forced stop of A/D conversion is enabled.

[bit3] ACHMD : ACH register mode

bit	Description
0	Direct ACH register mode. ADC12Bn_STAT.ACH shows the number of currently converted logical channel.
1	Latched ACH register mode. ADC12Bn_STAT.ACH shows the number of the logical channel whose conversion was finished last.

[bit2] DBGE : Debug Enable bit

bit	Description
0	Debug mode disabled
1	Debug mode enabled.

When this bit is set to "1" and the processor is in debug state, the A/D Converter completes the current conversion, but further conversion is stopped. When the processor leaves debug state or DBGE is set to "0", conversion continues with the next channel from where it had stopped.

[bit1:0] RES[1:0] : Resolution of A/D conversion

RES[1:0]	Description
x0	12-bit resolution
01	10-bit resolution
11	8-bit resolution.

Conversion result is stored in lower 10 bits of ADC12Bn_CD0~31 registers in case of 10-bit resolution and in lower 8 bits of ADC12Bn_CD0~31 registers if the 8-bit resolution is configured.

In case of 10-bit or 8-bit resolution, the lower 2 or 4 bits of the 12-bit conversion result are truncated (not rounded).

5.29. A/D Converter Global Status Register (ADC12Bn_STAT)

The register ADC12Bn_STAT is responsible for storing global status information of A/D Converter, such as currently converted channel and activity indication bit.

REGISTER_NAME	ADC12Bn_STAT
OFFSET	0x03A2
ACCESS_SIZE	B H W
MULTIPLE	1
NUMERIC_TYPE	-
OTHER	-

A/D Converter Global Status Register (ADC12Bn_STAT)

BIT_OFFSET	15	14	13	12	11	10	9	8
BIT_NAME	Reserved							
ACCESS_TYPE	RX,WX							
PROT_TYPE								
INITIAL_VALUE	0x00							

BIT_OFFSET	7	6	5	4	3	2	1	0
BIT_NAME	Reserved	BUSY	ACH[5]	ACH[4]	ACH[3]	ACH[2]	ACH[1]	ACH[0]
ACCESS_TYPE	RX,WX	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX
PROT_TYPE								
INITIAL_VALUE	0	0	0	0	0	0	0	0

[bit15:7] Reserved : Reserved bits

Reading this bit returns an undefined.

Writing data to these bits has no effect on the operation.

[bit6] BUSY : A/D Converter Busy flag

bit	Description
0	A/D Converter is not active, i. e. no A/D conversion is ongoing.
1	A/D Converter is active, i. e. A/D conversion is ongoing.

- Power-down disable mode (ADC12Bn_CTRL.PDDMD = "1"):
 - This bit set to "1" when first conversion request (trigger status set to "1") occurs (without A/D converter resumption time).
 - This bit clear to "0" when the all trigger status are cleared.
- Power-down enable mode (ADC12Bn_CTRL.PDDMD = "0"):
 - This bit is set to "1" when first conversion request (trigger status set to "1") occurs and A/D Converter resumption time (power-up wait time configured as A/D converter resumption time register (ADC12Bn_RT)) elapses.
 - This bit clear to "0" when the all trigger status are cleared.

If there is no idle trigger type set for any of logical channels, after all conversion requests are processed A/D Converter goes to idle (power-down) state and BUSY flag becomes "0" until next conversion request appears and resumption time elapses.

In case that idle trigger type is set (ADC12Bn_CHCTRL0~31.TRGTYPE[1:0] = "11"), there will be always at least one conversion request active and after BUSY flag is set first time to "1", it will not change.

[bit5:0] ACH[5:0] : Converted logical channel number

This bit field depends on ADC12Bn_CTRL.ACHMD field setting.

- If ACHMD is equal to "0", ACH represents currently converted logical channel number.
- If ACHMD is equal to "1", ACH represents the last logical channel number whose conversion has finished. ACH is updated at the end of the A/D conversion only in the case the corresponding trigger status (ADC12Bn_TRGST0.TRGST and ADC12Bn_CHSTAT0~31.TRGST bits) is still "1".

5.30. Range Comparator Upper Threshold Registers (ADC12Bn_RCOH0~7)

When the 8-bit range comparator mode (ADC12Bn_CTRL.FRCMD = "0"), these registers are used for 8-bit range comparator.

If the 12-bit range comparator mode (ADC12Bn_CTRL.FRCMD = "1"), these registers are not used.

These registers specify the upper threshold values that can be selected for the 8-bit range comparator to which the output of the A/D Converter is compared. Only ADC12Bn_RCOH0 is described here. Other registers (ADC12Bn_RCOH1,..., ADC12Bn_RCOH6 and ADC12Bn_RCOH7) have similar bit fields.

REGISTER_NAME	ADC12Bn_RCOHi (i = 0~7)
OFFSET	0x03B1 + i*2
ACCESS_SIZE	B H W
MULTIPLE	0:7
NUMERIC_TYPE	-
OTHER	-

Range Comparator Upper Threshold Register 0 (ADC12Bn_RCOH0)

BIT_OFFSET	7	6	5	4	3	2	1	0
BIT_NAME	RCOH[7]	RCOH[6]	RCOH[5]	RCOH[4]	RCOH[3]	RCOH[2]	RCOH[1]	RCOH[0]
ACCESS_TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
PROT_TYPE								
INITIAL_VALUE	1	1	1	1	1	1	1	1

[bit7:0] RCOH[7:0] : Range Comparator Upper Threshold value

The RCOH bits define the upper comparison threshold of the range comparator 0.

The upper comparator compares the upper 8 bits of the A/D conversion result. If the value is higher than RCOH[7:0], then the conversion result is outside range.

Selection of one of eight available range comparator threshold values for the logical channel is configured by corresponding ADC12Bn_CHCTRL0~31.RCSEL[2:0] bit fields.

5.31. Range Comparator Lower Threshold Registers (ADC12Bn_RCOL0~7)

When the 8-bit range comparator mode (ADC12Bn_CTRL.FRCMD = "0"), these registers are used for 8-bit range comparator.

If the 12-bit range comparator mode (ADC12Bn_CTRL.FRCMD = "1"), these registers are not used.

These registers specify the lower threshold values that can be selected for the 8-bit range comparator to which the output of the A/D Converter is compared. Only ADC12Bn_RCOL0 is described here. Other registers (ADC12Bn_RCOL1,...,ADC12Bn_RCOL6, ADC12Bn_RCOL7) have similar bit fields.

REGISTER_NAME	ADC12Bn_RCOLi (i = 0~7)
OFFSET	0x03B0 + i*2
ACCESS_SIZE	B H W
MULTIPLE	0:7
NUMERIC_TYPE	-
OTHER	-

Range Comparator Lower Threshold Register 0 (ADC12Bn_RCOL0)

BIT_OFFSET	7	6	5	4	3	2	1	0
BIT_NAME	RCOL[7]	RCOL[6]	RCOL[5]	RCOL[4]	RCOL[3]	RCOL[2]	RCOL[1]	RCOL[0]
ACCESS_TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
PROT_TYPE								
INITIAL_VALUE	0	0	0	0	0	0	0	0

[bit7:0] RCOL[7:0] : Range Comparator Lower Threshold value

The RCOL bits define the lower comparison threshold of the range comparator 0.

The lower comparator compares the upper 8 bits of the A/D conversion result. If the value is lower than RCOL[7:0], then the conversion result is outside range.

Selection of one of eight available range comparator threshold values for the logical channel is configured by corresponding ADC12Bn_CHCTRL0~31.RCSEL[2:0] bit fields.

5.32. Full Range Comparator Upper Threshold Registers (ADC12Bn_FRCOH0~7)

When the 12-bit range comparator mode (ADC12Bn_CTRL.FRCMD = "1"), these registers are used for 12-bit range comparator.

If the 8-bit range comparator mode (ADC12Bn_CTRL.FRCMD = "0"), these registers are not used.

These registers specify the upper threshold values that can be selected for the 12-bit range comparator to which the output of the A/D Converter is compared. Only ADC12Bn_FRCOH0 is described here. Other registers (ADC12Bn_FRCOH1,..., ADC12Bn_FRCOH6 and ADC12Bn_FRCOH7) have similar bit fields.

REGISTER_NAME	ADC12Bn_FRCOH _i (i = 0~7)
OFFSET	0x03F0 + i*2
ACCESS_SIZE	B H W
MULTIPLE	0:7
NUMERIC_TYPE	-
OTHER	-

Full Range Comparator Upper Threshold Register 0 (ADC12Bn_FRCOH0)

BITS_OFFSET	15	14	13	12	11	10	9	8
BITS_NAME	Reserved				FRCOH[11]	FRCOH[10]	FRCOH[9]	FRCOH[8]
ACCESS_TYPE	R0,W0				R/W	R/W	R/W	R/W
PROT_TYPE								
INITIAL_VALUE	0000				1	1	1	1

BITS_OFFSET	7	6	5	4	3	2	1	0
BITS_NAME	FRCOH[7]	FRCOH[6]	FRCOH[5]	FRCOH[4]	FRCOH[3]	FRCOH[2]	FRCOH[1]	FRCOH[0]
ACCESS_TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
PROT_TYPE								
INITIAL_VALUE	1	1	1	1	1	1	1	1

[bit15:12] Reserved : Reserved bits

When writing, always write "0".

When reading, "0" is always read.

[bit11:0] FRCOH[11:0] : Full Range Comparator Upper Threshold value

The FRCOH bits define the upper comparison threshold of the range comparator 0.

The upper comparator compares the 12 bits, 10 bits or 8 bits of the A/D conversion result.

ADC12Bn_CTRL.RES[1:0] define this resolution.

- If 12-bit resolution (ADC12Bn_CTRL.RES[1:0] = "x0"):

FRCOH[11:0]	Compares the 12 bits of A/D conversion result.

- If 10-bit resolution (ADC12Bn_CTRL.RES[1:0] = "01"):

FRCOH[11:10]	Not used for 10-bit range comparator.
FRCOH[9:0]	Compares the 10 bits of A/D conversion result.

- If 8-bit resolution (ADC12Bn_CTRL.RES[1:0] = "11"):

FRCOH[11:8]	Not used for 8-bit range comparator.
FRCOH[7:0]	Compares the 8 bits of A/D conversion result.

Selection of one of eight available range comparator threshold values for the logical channel is configured by corresponding ADC12Bn_CHCTRL0~31.RCSEL[2:0] bit fields.

5.33. Full Range Comparator Lower Threshold Registers (ADC12Bn_FRCOL0~7)

When the 12-bit range comparator mode (ADC12Bn_CTRL.FRCMD = "1"), these registers are used for 12-bit range comparator.

If the 8-bit range comparator mode (ADC12Bn_CTRL.FRCMD = "0"), these registers are not used.

These registers specify the lower threshold values that can be selected for the 12-bit range comparator to which the output of the A/D Converter is compared. Only ADC12Bn_FRCOL0 is described here. Other registers (ADC12Bn_FRCOL1,..., ADC12Bn_FRCOL6 and ADC12Bn_FRCOL7) have similar bit fields.

REGISTER_NAME	ADC12Bn_FRCOLi (i = 0~7)
OFFSET	0x03D0 + i*2
ACCESS_SIZE	B H W
MULTIPLE	0:7
NUMERIC_TYPE	-
OTHER	-

Full Range Comparator Lower Threshold Register 0 (ADC12Bn_FRCOL0)

BITS_OFFSET	15	14	13	12	11	10	9	8
BITS_NAME	Reserved				FRCOL[11]	FRCOL[10]	FRCOL[9]	FRCOL[8]
ACCESS_TYPE	R0,W0				R/W	R/W	R/W	R/W
PROT_TYPE								
INITIAL_VALUE	0000				0	0	0	0

BITS_OFFSET	7	6	5	4	3	2	1	0
BITS_NAME	FRCOL[7]	FRCOL[6]	FRCOL[5]	FRCOL[4]	FRCOL[3]	FRCOL[2]	FRCOL[1]	FRCOL[0]
ACCESS_TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
PROT_TYPE								
INITIAL_VALUE	0	0	0	0	0	0	0	0

[bit15:12] Reserved : Reserved bits

When writing, always write "0".

When reading, "0" is always read.

[bit11:0] FRCOL[11:0] : Full Range Comparator Lower Threshold value

The FRCOL bits define the lower comparison threshold of the range comparator 0.

The lower comparator compares the 12 bits, 10 bits or 8 bits of the A/D conversion result.

ADC12Bn_CTRL.RES[1:0] define this resolution.

- If 12-bit resolution (ADC12Bn_CTRL.RES[1:0] = "x0"):

FRCOL[11:0]	Compares the 12 bits of A/D conversion result.

- If 10-bit resolution (ADC12Bn_CTRL.RES[1:0] = "01"):

FRCOL[11:10]	Not used for 10-bit range comparator.
FRCOL[9:0]	Compares the 10 bits of A/D conversion result.

- If 8-bit resolution (ADC12Bn_CTRL.RES[1:0] = "11"):

FRCOL[11:8]	Not used for 8-bit range comparator.
FRCOL[7:0]	Compares the 8 bits of A/D conversion result.

Selection of one of eight available range comparator threshold values for the logical channel is configured by corresponding ADC12Bn_CHCTRL0~31.RCSEL[2:0] bit fields.

5.34. A/D Multiple Conversion Channel Control Registers (ADC12Bn_MCCTRL0~3)

These registers ADC12Bn_MCCTRL0~3 contain additional configuration bits for the first four logical channels (multiple conversion logical channels). They control number of conversions, multiple conversion interruption and A/D Converter calibration setup. Only ADC12Bn_MCCTRL0 is described here. Other registers (ADC12Bn_MCCTRL1, ADC12Bn_MCCTRL2 and ADC12Bn_MCCTRL3) have identical bit fields.

REGISTER_NAME	ADC12Bn_MCCTRLi (i = 0~3)
OFFSET	0x03C0 + i
ACCESS_SIZE	B H W
MULTIPLE	0:3
NUMERIC_TYPE	-
OTHER	-

A/D Multiple Conversion Channel Control Register (ADC12Bn_MCCTRL0)

BIT_OFFSET	7	6	5	4	3	2	1	0
BIT_NAME	Reserved	AVRHSEL	AVRLSEL	ICIRQY	CNVNUM[3]	CNVNUM[2]	CNVNUM[1]	CNVNUM[0]
ACCESS_TYPE	R0,W0	R/W	R/W	R/W	R/W	R/W	R/W	R/W
PROT_TYPE								
INITIAL_VALUE	0	0	0	0	0	0	0	0

[bit7] Reserved : Reserved bit

When writing, always write "0".

When reading, "0" is always read.

[bit6] AVRHSEL : A/D reference voltage AVRH selection bit

bit	Description
0	AVRH voltage is not selected for A/D conversion
1	AVRH voltage is selected for A/D conversion.

In case that both bits AVRHSEL and AVRLSEL bits are set to "1", AVRLSEL has higher priority and AVRL voltage is converted.

If any of AVRHSEL/AVRLSEL bits is set to "1", conversion of a regular analog input AN is not possible.

For further explanation of A/D Converter calibration refer to section "A/D Converter Calibration" in chapter "3 Operation of A/D".

[bit5] AVRLSEL : A/D reference voltage AVRL selection bit

bit	Description
0	AVRL voltage is not selected for A/D conversion
1	AVRL voltage is selected for A/D conversion

In case that both bits AVRHSEL and AVRLSEL bits are set to "1", AVRLSEL has higher priority and AVRL voltage is converted.

If any of AVRHSEL/AVRLSEL bits is set to "1", conversion of a regular analog input AN is not possible.
For further explanation of A/D Converter calibration refer to section "A/D Converter Calibration" in chapter "3 Operation of A/D".

[bit4] ICIRQY : Intra-channel interrupt ability for the multiple conversion logical channel

This bit determines if the multiple conversion logical channel can be interrupted between single conversions, in case the conversion request with higher priority is issued.

bit	Description
0	Multiple conversion logical channel can be interrupted between single conversions.
1	Multiple conversion logical channel cannot be interrupted between single conversions.

This bit has no effect if CNVNUM[3:0] is configured to "0000".

[bit3:0] CNVNUM[3:0] : Number of conversions for the multiple conversion channel

This bit field specifies the number of A/D conversions to be performed if the conversion request for the multiple conversion logical channel is issued.

CNVNUM[3:0]	Description
0000	1 conversion. With this setting multiple conversion logical channel behaves like any other logical channel.
0001	2 conversions.
0010	3 conversions.
...	...
1111	16 conversions

CNVNUM[3:0] are not allowed to update during A/D conversion operation (ADC12Bn_TRGST0.TRGST and ADC12Bn_CHSTAT0~31.TRGST="1").

5.35. A/D Multiple Conversion Channel Status Registers (ADC12Bn_MCSTAT0~3)

These registers contain the current status of finished conversion number for first four multiple conversion logical channels. Only ADC12Bn_MCSTAT0 is described here. Other registers (ADC12Bn_MCSTAT1, ADC12Bn_MCSTAT2 and ADC12Bn_MCSTAT3) have identical bit fields.

REGISTER_NAME	ADC12Bn_MCSTATi (i = 0~3)
OFFSET	0x03E0 + i
ACCESS_SIZE	B H W
MULTIPLE	0:3
NUMERIC_TYPE	-
OTHER	-

A/D Multiple Conversion Channel Status Register (ADC12Bn_MCSTAT0)

BIT_OFFSET	7	6	5	4	3	2	1	0
BIT_NAME	Reserved			MCCNT[4]	MCCNT[3]	MCCNT[2]	MCCNT[1]	MCCNT[0]
ACCESS_TYPE	RX,WX			R,WX	R,WX	R,WX	R,WX	R,WX
PROT_TYPE								
INITIAL_VALUE	000			0	0	0	0	0

[bit7:5] Reserved : Reserved bits

Reading this bit returns an undefined.

Writing data to these bits has no effect on the operation.

[bit4:0] MCCNT[4:0] : Counter of the Multiple conversion

Conversion counter counting the number of already finished A/D conversions of the multiple conversion logical channel.

After the set event of the conversion done interrupt flag, the ADC12Bn_MCSTAT.MCCNT[4:0] are meaningless.

MCCNT[4:0]	Description
00000	No conversion is finished.
00001	1 conversion is finished.
...	...
10000	16 conversions are finished.
10001-11111	Reserved

CHAPTER 24: Partial Wakeup Control



This chapter explains the partial wakeup control function and its operations.

1. Overview
2. Configuration
3. Explanation of Operation
4. Registers
5. Precautions for Using this Device

CODE: PWU-S6J3400-E3

1. Overview

This section provides an overview of the partial wakeup control.

Partial wakeup (PWU) mode is implemented in this device.

PWU mode is one of the PSS (Power Saving State) modes. In this mode, only the functions required for voltage monitoring by the A/D converter are operating.

Effective use of this function enables monitoring of voltage, such as in sensor output, with low-power consumption and without starting the CPU.

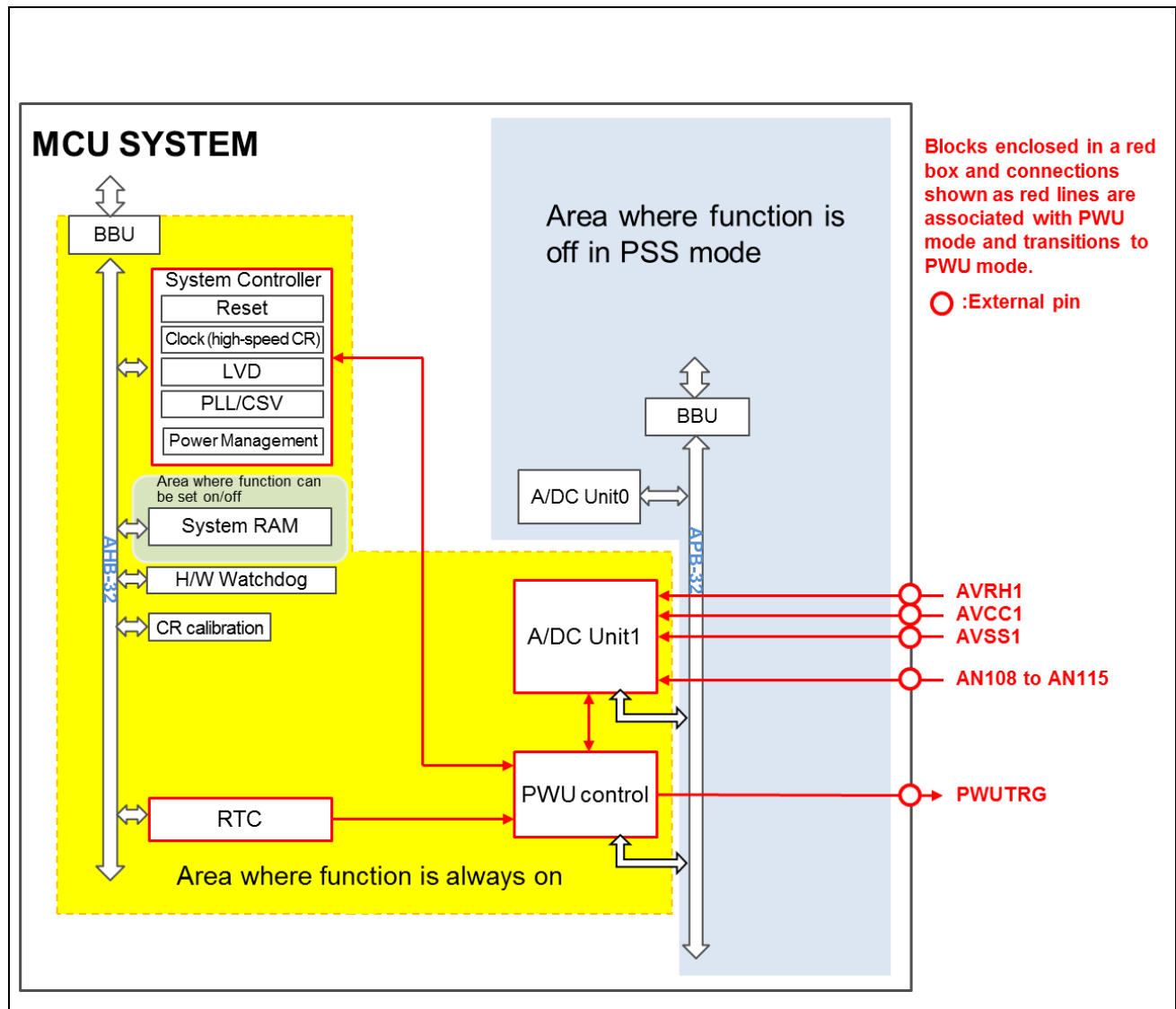
2. Configuration

This section explains the partial wakeup configuration.

Relationship between the Entire System and the Partial Wakeup Function

Figure 2-1 shows the relationship between the entire system and the partial wakeup function.

**Figure 2-1 Relationship between the Entire System and the Partial Wakeup Function
(Describing Only the Relationship with Related Blocks)**



■ RTC

This block counts the cycles for transitioning to PWU mode. The cycles can be set in steps of 8 ms, between 8 and 64 ms. For the setting method, see "3. Explanation of Operation."

Notes:

The term of 8ms is generated from the following calculation in RTC.

$$0.25[s] \div 32 = 7.8125[ms] (\approx 8[ms])$$

Moreover as RTC operates with low-speed CR (typical 100KHz) in PWU mode, the actual cycles for transitioning to PWU mode become as the following.

7.81[ms] (The description in this chapter is "8ms")

15.62[ms] (The description in this chapter is "16ms")

23.43[ms] (The description in this chapter is "24ms")

31.24[ms] (The description in this chapter is "32ms")

39.05[ms] (The description in this chapter is "40ms")

46.86[ms] (The description in this chapter is "48ms")

54.67[ms] (The description in this chapter is "56ms")

62.48[ms] (The description in this chapter is "64ms")

■ System controller

- This block manages the device state (PSS or RUN).
- The block turns on the high-speed CR oscillator when transitioning to PWU mode.

■ PWU control

- This block controls the high-speed CR oscillator, the "PWUTRG" pin output function, and A/DC Unit1.
- In PWU mode, the block outputs "H" from the "PWUTRG" pin.
- The block starts A/D conversion within a certain time after the PWUTRG pin outputs "H". The time until A/D conversion start can be set in steps of 50 us, between 50 and 5100 us.

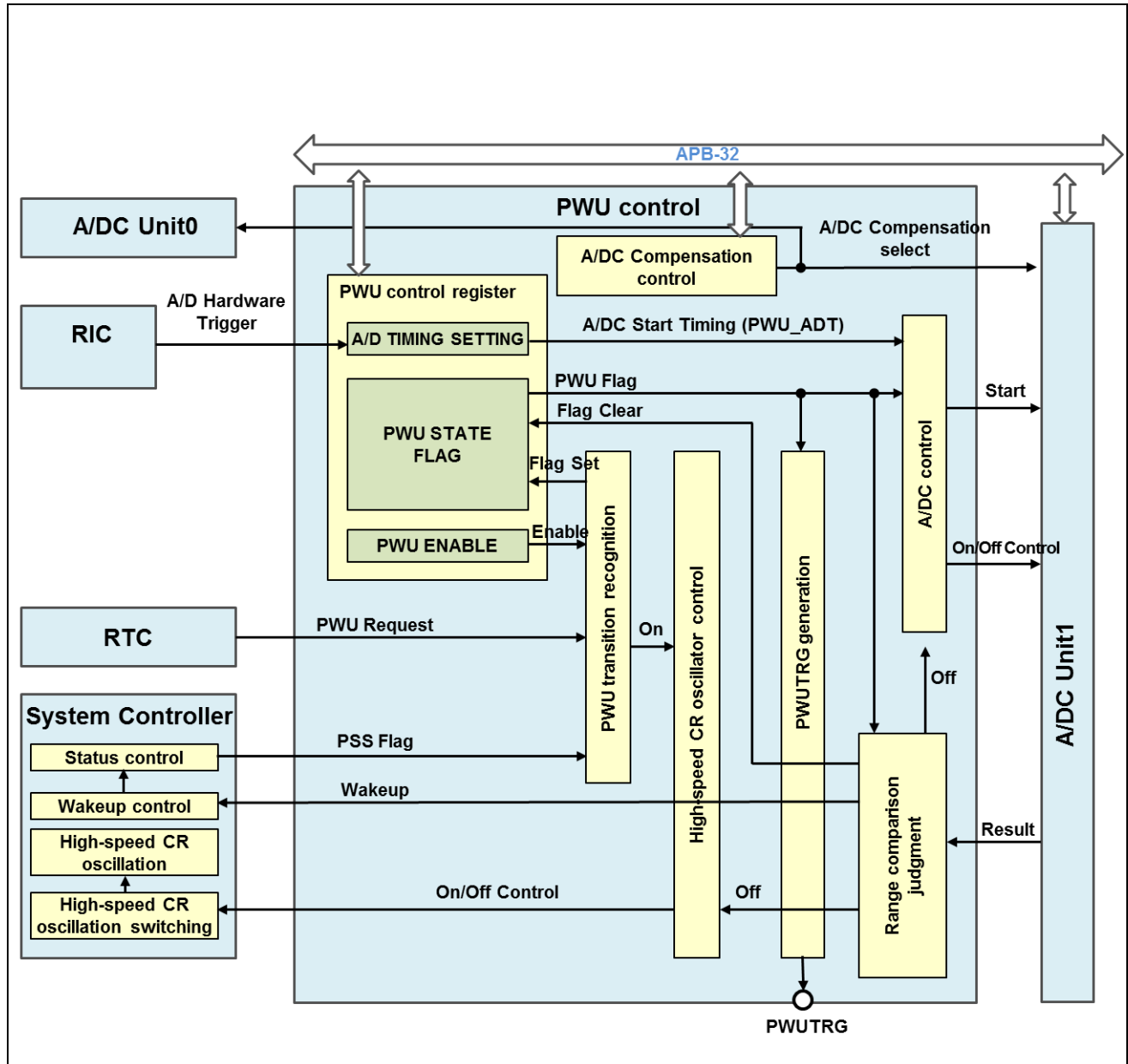
■ A/DC Unit1

- In PWU mode, the A/D converter can be used with the 8 channels from AN108 to AN115 out of all channels.
- In PWU mode, only the range comparison function of the A/D converter can be used. For details, see the chapter of "12/10/8-BIT Analog To Digital Converter" on this manual.

Block Diagram of the Partial Wakeup Function

Figure 2-2 is a block diagram of the partial wakeup function.

Figure 2-2 Block Diagram of the Partial Wakeup Function



■ PWU control register

The configuration includes the "partial wakeup mode enable bit", the "A/D conversion start time setting register", "A/D conversion request trigger control register" and "A/D conversion offset compensation value select register". For details, see the chapter of "Partial Wakeup Control 4. Registers" on this manual.

■ PWU transition recognition

This block judges whether the conditions for transitioning to PWU mode are met. Also, the block turns on the high-speed CR oscillator.

■ High-speed CR oscillator control

This block is used for On/Off control of the high-speed CR oscillator in PWU mode.

■ PWUTRG generation

In PWU mode, this block outputs "H" from the "PWUTRG" pin.

■ A/DC control

This block is used to turn A/DC on or off and to adjust the timing of conversion start in PWU mode.

The block starts A/D conversion within a certain time after the PWUTRG pin outputs "H".

The time until A/D conversion start can be set in steps of 50 us, between 50 and 5100 us.

■ Range comparison judgment

This block determines, from an A/D conversion range comparison, whether to transition to RUN mode or PSS mode.

To transition to RUN mode, it generates a Wakeup signal.

After the completion of A/D conversion, the block generates a signal for turning off the high-speed CR oscillator and A/DC Unit1.

■ A/DC Compensation control

This block switches the A/D conversion Offset Compensation value.

The value which matches use condition can be selected by changing the setting of the corresponding register. For details, see the chapter of "Partial Wakeup Control 4.3. A/D Conversion Offset Compensation value Select Registers" on this manual.

3. Explanation of Operation

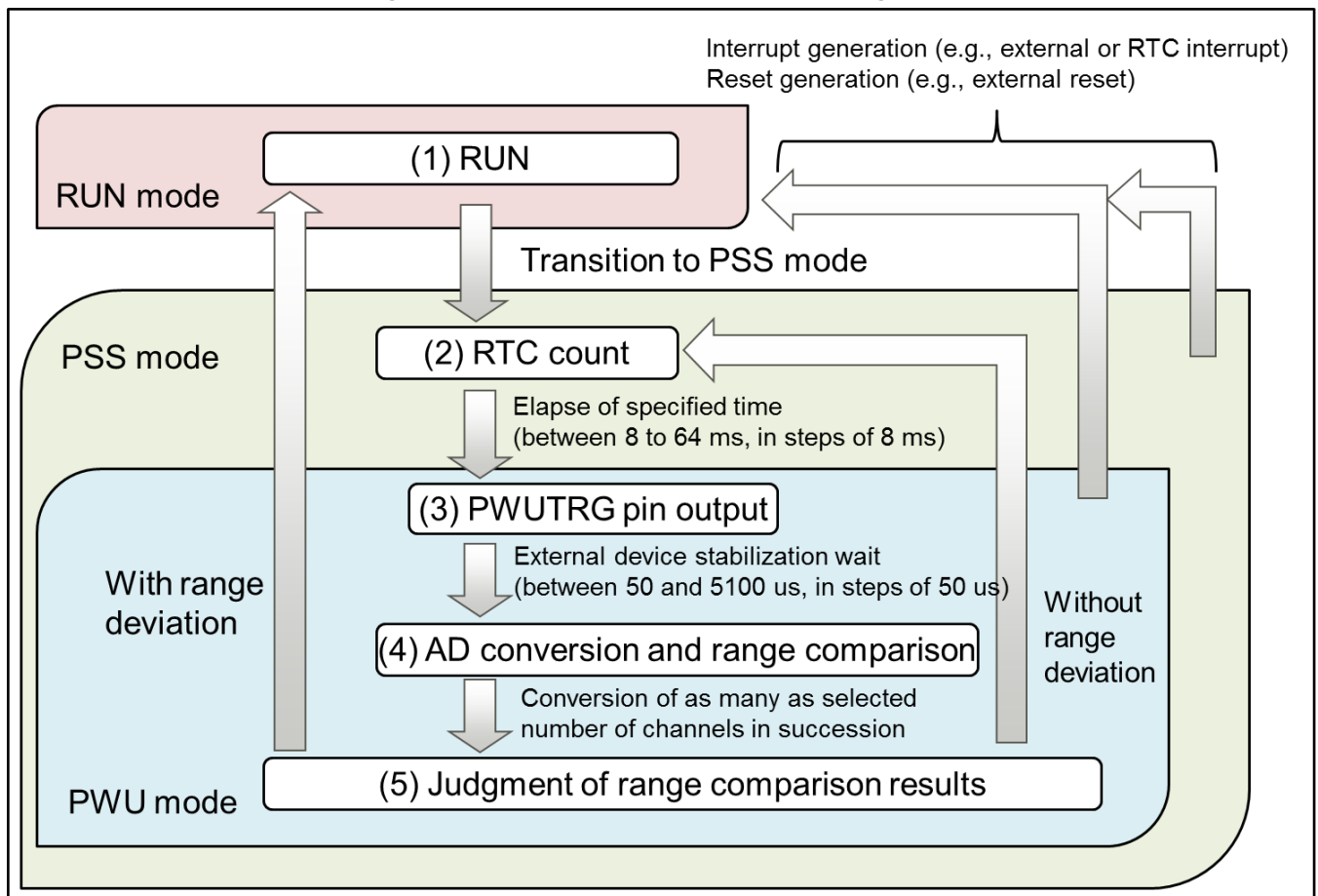
This section explains the operations of partial wakeup control.

3.1. State Transition Diagram

Figure 3-1 shows the relationship between partial wakeup mode and other modes.

The figure outlines the operations. For a more detailed explanation of the operations, see the next section, "Flowchart."

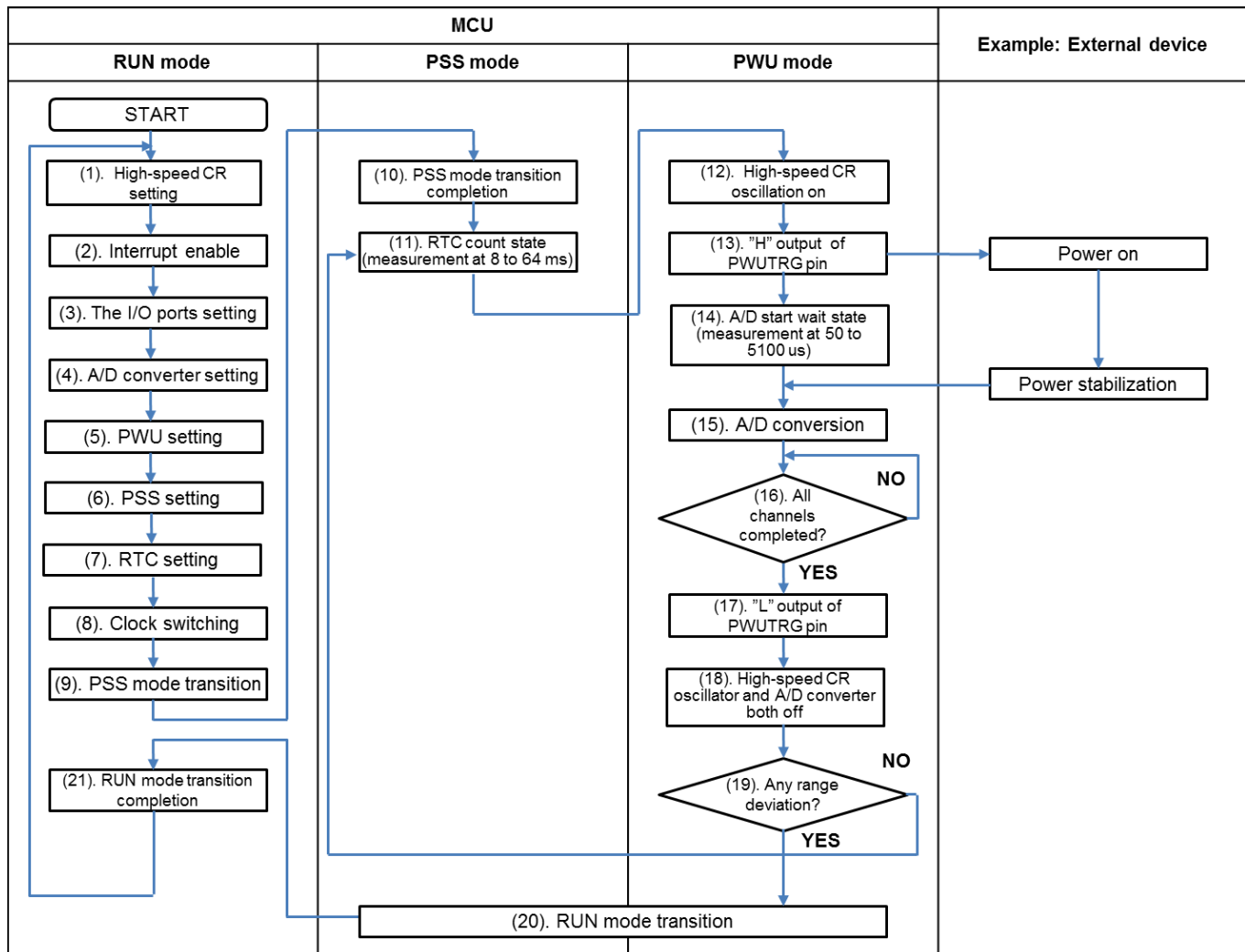
Figure 3-1 Partial Wakeup State Transition Diagram



3.2. Flowchart

This section uses the flowchart in Figure 3-2 to explain the partial wakeup function in detail.

Figure 3-2 Partial Wakeup Function Flowchart



(1) High-speed CR Setting (Processing by software)

(1)-1. Calibration

Software performs high-speed CR oscillation calibration and corrects any deviation in the A/D conversion time and any deviation in the period from PWUTRG pin output to A/D conversion start (external device stabilization wait time). Such deviations are due to process variations and variations depending on the use conditions.

For the setting method for the above, see the chapter of "CR Calibration" in Traveo™ Platform hardware manual.

(1)-2. Stabilization wait time

Set the PSCL bit and CMPR bit in SYSC_FCRCTCPR register to initial (default) value.

These settings are applied to "(13) High-speed CR oscillation on."

If stabilization wait time is set to large value and PWU mode time exceeds PWU transition cycle,

This device becomes illegal state.

In this state, the transition to RUN mode can't occur by A/D converter range deviation.

For the setting method for the above, see the chapter of "Source Clock Timer" in Traveo™ Platform hardware manual.

(2) Interrupt Enable (Processing by software)

You can treat enabled interrupt factors as return factors from PSS mode and PWU mode.

For any return due to an interrupt, there is a transition to the "(20)." processing.

The following can be specified: the interrupt of a resource not in the Power Down state, even in PSS mode.

Examples include external interrupt, RTC, NMI, low-voltage detection*1.

(*1 When used as an interrupt at the abnormal state detection)

For the method of enabling interrupts, see the chapters on the respective resources.

Note that this section does not cover A/DC-related settings because they are handled in the "(4)." processing.

(3) The I/O Ports Setting (Processing by software)

Here, software makes the port output setting for the PWUTRG function and the analog I/O settings of the A/DC.

You can set the PWUTRG by writing appropriate value to the POF bit in the corresponding PPC_PCFGRijj (i=0 to 4, jj=00 to 31) register.

The target port is used as analog input of A/DC by writing appropriate value to the corresponding PPC_PCFGRijj (i=0 to 4, jj=00 to 31) register and GPIO_DDR register.

For a corresponding register and setting, see the chapter of "Port Configuration" on this manual.

Note that this section does not cover settings related to "retaining the pin state in PSS mode" because they are handled in the "(6)." processing.

(4) A/D Converter Setting (Processing by software)

Table 3-1 lists the setting values for writable registers related to A/D converter unit 1, corresponding to PWU mode.

The following values are degrees of limitations.

3: Always set values according to the "setting value."

2: The recommended setting is based on the "setting value." It can be changed to match the use conditions.

1: Set a value appropriate to the use conditions.

Interpret the values as described.

Notes:

'i' represents the logical channel number. $i = 0, 1, 2, \dots, 31$

In PWU mode, the number of activation channel which can be used is maximum 8.

In PWU mode, be sure to select the consecutive logical channel to execute the group processing.

For example

If 8 channels are used and the start channel is 0 ($i=0$), select the following logical channel number.

$i = 0, 1, 2, 3, 4, 5, 6$ and 7

If the start channel is 29 ($i=29$), the available logical channel number is the following.

$i = 29, 30$ and 31 .

For a detailed explanation of the registers and the setting method, see the chapter of "12/10/8-Bit Analog To Digital Converter" on this manual.

Table 3-1 A/D Converter Settings

Register Name	Setting Value	Degree of Limitation
ADC12B1_CHCTRLi ($i = 0 \sim 31$)	TRGCL=1'b0	3
	SWTRG=1'b0	3
	Value of RCEN is set to the following value. RCEN bits corresponding to activation channels are set to 1'b1 (Range comparator enabled), and other bits are set to 1'b0 (Range comparator disabled).	3
	RCINVSEL=Set a value appropriate to use conditions.	1
	RCSEL[2:0]=Set a value appropriate to use conditions. Set the register value "i" (i.e. ADC12B1_FRCOH _i , ADC12B1_FRCOL _i) selected as the upper/lower threshold values.	1
	SMTIME[1:0]=Set a value appropriate to use conditions. Set the register value "i" (i.e. ADC12B1_ST _i) selected as channel sampling time.	2
	DP=1'b0	3
	RSMRST[1:0]=2'b00	1

Register Name	Setting Value	Degree of Limitation
ADC12B1_CHCTRLi (i = 0~31)	Value of CHPRI[3:0] are set to three kinds of priority. CHPRI[3:0]=4'b0000 (Highest priority) Set the first channel (e.g. corresponding to AN108) of the group to the above value. CHPRI[3:0]=4'b0001 Set the following channels (e.g. corresponding to AN109 - AN115) to the above value. CHPRI[3:0]=4'b0010 or more Set the unnecessary channels for PWU mode to the above value. For details and notes on the settings, see the chapter of "12/10/8-Bit Analog To Digital Converter" on this manual.	3
	Value of TRGTYP[1:0] are set to two kinds of the trigger type. TRGTYP[1:0]=2'b01 (Software or hardware trigger.) Set the first channel (e.g. corresponding to AN108) of the group to the above trigger type. TRGTYP[1:0]=2'b10 (Preceding logical channel conversion completion.) Set the following channels (e.g. corresponding to AN109 - AN115) to the above trigger type. No other channel (corresponding no used in PWU mode) must be included in the group which is defined for PWU mode. It is prohibited to set TRGTYP[1:0]=2'b11 (Idle trigger) in PWU mode. For details and notes on the settings, see the chapter of "12/10/8-Bit Analog To Digital Converter" on this manual.	3
	Value of ANIN[5:0]=6'b001000 to 6'b001111 Activation channels and analog input pins are associated. Only analog input pins AN108 to AN115 are enabled with PWU mode.	3
ADC12B1_PCCTRL i (i = 0~31)	Do not use with the PWU function.	1
ADC12B1_CDONEIRQE0	Value of {CDONEIRQE31 to CDONEIRQE0} are set to the following value. Interrupt enable bit (CDONEIRQEx) of the last channel in the group is set to 1'b1 (Conversion done interrupt enabled), and other bits are set to 1'b0 (Conversion done interrupt are disabled). (Do not transition to PWU mode with interrupts left enabled.) The channel set at this register will be the last channel of the group procedure.	3
ADC12B1_CDONEIRQC0	Write "0xFFFF_FFFF" to clear all A/D conversion done interrupt flags.	3
ADC12B1_GRP_IRQE0	Value of {GRPIRQE31 to GRPIRQE0}="0x0000_0000" (Group interrupted interrupt disabled.)	3
ADC12B1_GRP_IRQC0	These bits are not used in PWU mode.	1

Register Name	Setting Value	Degree of Limitation
ADC12B1_RCIRQE0	Value of {RCIRQE31 to RCIRQE0} are set to the following value. Interrupt enable bit (RCIRQEx) of the activation channel for PWU mode is set to 1'b1 (Range comparator interrupt enabled), and other bits are set to 1'b0 (Range comparator interrupt are disabled). (Do not transition to PWU mode with interrupts left enabled.)	3
ADC12B1_RCIRQC0	Write "0xFFFF_FFFF" to clear all Range comparator interrupt flags.	3
ADC12B1_PCIRQE0	Value of {PCIRQE31 to PCIRQE0}="0x0000_0000" (Pulse counter interrupt is disabled.)	3
ADC12B1_PCIRQC0	These bits are not used in PWU mode.	1
ADC12B1_TRGCL0	Write "0xFFFF_FFFF" to clear all A/D channel trigger status flags	3
ADC12B1_TRGORC0	Write "0xFFFF_FFFF" to clear all A/D channel trigger overrun flags	3
ADC12B1_CDDS0~3	CDCHEN=1'b0 (DMA request is disabled.) CDCHNUM[5:0] have no effect with CHCHEN=1'b0.	3
ADC12B1_RT	These bits are not used in PWU mode, when Power down disable mode (ADC12Bn_CTRL.PDDMD = "1"), these bits have no effect.	1
ADC12B1_CT	CT[15:0]="0x0001" ("0x0006" or more is a prohibited setting.) The built-in high-speed CR oscillation clock (4 MHz) is divided according to the setting, and the comparison time is measured using the divided clock. For details and notes on the settings, see the chapter of "12/10/8-Bit Analog To Digital Converter" on this manual.	2
ADC12B1_STi (i = 0~3) * Select only the registers corresponding to the numbers assigned as the settings for the sampling time	STi[15:0]="0x0007" ("0x0019" or more is a prohibited setting.) The built-in high-speed CR oscillation clock (4 MHz) is divided according to the setting, and the sampling time is measured using the divided clock. For details and notes on the settings, see the chapter of "12/10/8-Bit Analog To Digital Converter" on this manual.	2
ADC12B1_OCV	This register specifies the setting for offset compensation value. It is necessary that OCVSEL bit in A/D Converter Offset Compensation value Select register (PWU_ADOCS) is set to "0" before A/D Converter calibration is performed. For details, see "4.Registers" in this chapter.	2
ADC12B1_GCV	This register specifies the setting for gain compensation value. For details, see "4.Registers" in this chapter.	2
ADC12B1_CTRL	RES[1:0]=2'b00 (12 bit resolution)	3
	DBGE=1'b0	3
	ACHMD=1'b0	3
	FSMD=1'b0	3
	FRCMD=1'b1 (12 bit range comparator mode)	3
	FSTP=1'b0 (When the "not" forced stop mode (FSMD = "0"))	1
	PDDMD=1'b1 (A/D convertor does not go idle state after A/D conversion finished.)	3
ADC12B1_RCOH0~7	Do not use with the PWU function.	1

Register Name	Setting Value	Degree of Limitation
ADC12B1_RCOL0~7	Do not use with the PWU function.	1
ADC12B1_FRCOH0~7 * Select only the registers corresponding to the numbers assigned as the upper threshold values	FRCOH[11:0]=Set a value appropriate the use conditions.	1
ADC12B1_FRCOL0~7 * Select only the registers corresponding to the numbers assigned as the lower threshold values	FRCOL[11:0]=Set a value appropriate the use conditions.	1
ADC12B1_MCCTRL0~3	Value of ADC12B1_MCTRL="0x00"	3

(5) PWU Setting (Processing by software)

Here, software makes the following settings.

(5)-1. Enable the PWU function.

(5)-2. Set the external device stabilization wait time, which is the period between PWUTRG pin output and A/D conversion start.

You can select stabilization wait times from 50 to 5100 us, in steps of 50 us.

(5)-3. Select the PWU A/D conversion trigger (PWU_ADT) as A/D conversion trigger.

(5)-4. Set the first logical channel number of the group procedure executing in the PWU mode.

For the method of setting the above, see the chapter of "Partial Wakeup Control 4. Registers" on this manual.

(6) PSS Setting (Processing by software)

Table 3-2 lists the setting values for the writable registers in the PSS profile register group and the writable registers of the system special setting registers. The following values are degrees of limitations.

3: Always set values according to the "setting value."

2: The recommended setting is based on the "setting value." It can be changed to match the use conditions.

1: Set a value appropriate to the use conditions.

Interpret the values as described.

For a detailed explanation of the registers and the setting method, see the chapter "Low-Power Consumption" in Traveo™ Platform hardware manual.

Table 3-2 PSS Profile Register Group Settings

Register Name	Setting Value	Degree of Limitation
SYSC0_PSSPDCFGR	PD4_1EN = Set a value appropriate to Backup area in System SRAM use conditions.	1
	PD4_0EN = Set a value appropriate to Backup area in System SRAM use conditions.	1
	PD2EN=1'b0	3
SYSC0_PSSCKSRER	SSCG0EN=1'b0	3
	PLL0EN=1'b0	3
	MOSCEN=1'b0	3
	SCROSCEN=1'b1	3
	CROSCEN=1'b0	3
	SOSCEN=1'b0	3
SYSC0_PSSCKSELR	CDMCUCCSL=3'b111	3
SYSC0_PSSCKER	ENCLKMCUCP=1'b0	3
	ENCLKMCUCH=1'b0	3
SYSC0_PSSCKDIVR	MCUCHDIV=5'b00000	3
SYSC0_PSSPLLxCNTR	PLLxISEL=1'b0	2
	PLLxDIVN=8'b00001101	2
	PLLxDIVM=4'b0001	2
	PLLxDIVL=2'b00	2
SYSC0_PSSSSCGxCNTR0	SSCGxISEL=1'b0	2
	SSCGxDIVN=8'b00001101	2
	SSCGxDIVM=4'b0001	2
	SSCGxDIVL=2'b00	2
SYSC0_PSSSSCGxCNTR1	SSCGxSEN=1'b0	2
	SSCGxFREQ=2'b00	2
	SSCGxMODE=1'b0	2
	SSCGxRATE=10'b0000101001	2
SYSC0_PSSLVDCFGR	LVDL1S = Set a value appropriate to the use conditions.	1
	LVDL1V = Set a value appropriate to the use conditions.	1
	LVDL1E = Set a value appropriate to the use conditions.	1
	LVDH1S = Set a value appropriate to the use conditions.	1
	LVDH1V = Set a value appropriate to the use conditions.	1
	LVDH1E = Set a value appropriate to the use conditions.	1

Register Name	Setting Value	Degree of Limitation
SYSC0_PSSCSVCFGR	SSCG0CSVE=1'b0	3
	PLL0CSVE=1'b0	3
	SCRCSE=1'b0	3
	CRCSVE=1'b0	3
	SOCSVE=1'b0	3
	MOCSVE=1'b0	3
SYSC0_PSSREGCFGR	RMSEL=1'b1	3
SYSC0_SPECFGR	HOLDIO_PD2=1'b1 The setting by this bit is reflected immediately after writing register, it is not after PSS profile change.	3
	PSSPADCTRL=1'b0	3
	EXVRSTCNT=1'b1 If the setting is EXVRSTCNT=1'b0, the RAM data of Backup area in System SRAM are not guaranteed after LVDH1 reset.	3
SYSC1_PSSCKSELR0	LAPP1ACSL=1'b0	3
	LAPP0ACSL=1'b0	3
	LCP1ACSL=1'b0	3
	LCP0ACSL=1'b0	3
	CD0CSL=3'b111	3
	If this setting is not made, a PSS profile error occurs at a PSS mode transition.	

(7) RTC setting (processing by software)

The following shows examples of RTC settings. For details on the setting method, see the chapter "Real-Time Clock" in Traveo™ Platform hardware manual.

Example of settings

(7)-1. Initialization settings

Sequence	Set Contents *1	Set Timing
1-1.	Write "1" to the ST bit in the RTC_WTCR register.	1st setting only after POR
1-2.	Write "0" to the ST bit in the RTC_WTCR register.	1st setting only after POR
1-3.	Write "2'b10" to the RCKSEL bit in the RTC_WTCR register, write "1" to the CSM bit, and select the low-speed CR clock.	1st setting only after POR (RTC Clock = 100KHz)
1-4.	Set each bit in the RTC_WRT register.	1st setting only after POR

*1 Don't write to the registers by bit level.

In bit-level-write, the no-change-bit have the function which the same value as read data is written to the register. In this case, the bit having difference function between read and write is changed to the other setting.

Therefore the bits no change is intended will be changed.

(7)-2. Calibration setting (for correcting any deviation in the count values due to variations in low-speed oscillation)

Sequence	Set Contents *1	Set Timing
2-1.	Write a value to the DURMW bit in the RTC_DURMW register, and set the calibration period. Normally, set the calibration period to 0.25[s]. To set a time 0.25[s] or shorter, a value of 0.25[s] divided by 1, 2, 4, 8, or 16 can be selected for the period. However, the lower the value set, the lower the accuracy becomes. (Related to the SCAL[2:0] bit) When the main clock is 4 MHz and the calibration period is set to 0.25[s], set DURMW bit value="0xF4240" (1'000'000 as a decimal).	1st setting only after POR
2-2.	Set the related bits in the RTC_WTCR register as described below.	
	– Set the SCAL [2:0] bit according to the RTC_DURMW value. If the calibration period is set to 0.25[s], set "3'b000".	1st setting only after POR
	– Set the CCKSEL bit to 1'b1, and select the low-speed CR.	1st setting only after POR (RTC Clock = 100KHz)
	– Set the ENUP bit according to the use conditions. To update the calibration result automatically as hardware, set "1'b1". To update it with software, set "1'b0".	1st setting only after POR
	– Set the ACAL bit to "1'b0", and disable the auto-calibration.	1st setting only after POR
2-3.	Write "1'b1" to the CALDC bit in the RTC_WINC register, and clear the calibration interrupt.	Clear the interrupt flag after interrupt occurs
2-4.	Write "1'b1" to the MTRG bit in the RTC_WTCR register, and start calibration.	Set in the timing you want to calibrate.(e.g. Post-PWU)
2-5.	Wait until the CALD bit in the RTC_WINS register becomes "1'b1".	The calibration is available on real time count.

*1 Refer to the previous table.

(7)-3. Partial wakeup setting - Case 1: When the ENUP bit in (7)-2-2 is set to "1'b1". -

Sequence	Set contents *1	Set timing
3-1.	Set the related bits in the RTC_PWUTRGCR register as described below.	
	Set the MD bit to "1'b1".	
	For the SEL bit, set the cycles for transitioning to PWU mode in accordance with the purpose. Values ranging from 8 to 64 ms can be selected in units of 8 ms.	The period of PWU can be switched.
3-2.	Wait until the BUSY bit in the RTC_PWUTRGSR register becomes 1'b0.	Set if RTC_PWUTRGCR register is changed.

*1 Refer to the previous table.

(7)-3. Partial wakeup setting - Case 2: When the ENUP bit in (7)-2-2 is set to "1'b0". -

Sequence	Set contents *1	Set timing
3-1.	Read the value of RTC_CNTCAL, execute [-1 processing], and then execute [divide-by-32 processing]. The RTC_CNTCAL includes the counter value of 0.25[s]. By dividing by 32, it generates a count value of approximately 8 ms.	Set if the calibration (the setting of "2-3"- "2-5") is completed.
3-2.	Read the value of RTC_CNTCAL, and execute [-1 processing]. Write the post processing value to the WTBR bit in the RTC_WTBR register.	
3-3.	Set the related bits in the RTC_PWUTRGCR register as described below.	
	- Set the C8MRL bit to the value calculated in "(7)-3-1."	
	- Set the MD bit to "1'b0".	1st setting only after POR
	- For the SEL bit, set the cycles for transitioning to PWU mode in accordance with the purpose. Values ranging from 8 to 64 ms can be selected in units of 8 ms.	The period of PWU can be switched.
3-4.	Wait until the BUSY bit in the RTC_PWUTRGSR register becomes 1'b0.	Set if RTC_PWUTRGCR register is changed.

*1 Refer to the previous table.

(7)-4. RTC count start

Sequence	Set contents *1	Set timing
4-1.	Set the RTC_WINE register, and enable the required interrupts.	1st setting only after POR
4-2.	Write "1" to each bit in the RTC_WINC register, and clear the interrupt flag.	Clear the interrupt flags after interrupts occur
4-3.	Write "1" to the ST bit in the RTC_WTCR register, and start counting.	1st setting only after POR (RTC Clock = 100KHz)

*1 Refer to the previous table.

(8) Clock Switching (Processing by software)

Here, software makes the following settings.

(8)-1. Clock gear down operation

If the PLL clock is being used for operating the internal circuit, use the clock gear down function to set the clock frequency lower in stages to reduce the current fluctuations due to clock switching.

For details on how to use the clock gear down function, see the "Clock Gear" section in the chapter of "Clock System" in Traveo™ Platform hardware manual.

(8)-2. Clock adjustment

To transition to the PSS, establish a 1:1:1:1 relationship between the CPU clock, the memory configuration clock, the SCU clock, and the MCUCH clock.

The absence of this relationship between these clocks may cause a malfunction.

Additionally, PLL and SSCG-PLL must be disabled before PSS mode transition.

Example of settings

Because the SCU clock operates with the high-speed CR oscillation clock, switch the CPU clock (CLK_CPU), memory configuration clock (CLK_MEMC), and MCUCH clock (CLK_SYSC0H) so that they all operate with the high-speed CR oscillation clock.

(8)-2-1. Set the CD0CSL bit in the SYSC1_RUNCKSELR0 register to "All-0".

(8)-2-2. Set the HPMDIV bit and the SYSDIV bit in the SYSC1_RUNCKDIVR0 register to "All-0".

(8)-2-3. Set the CDMCUCCSL bit in the SYSC0_RUNCKSELR register to "All-0".

(8)-2-4. Set the MCHUDIV bit in the SYSC0_RUNCKDIVR register to "All-0".

(8)-2-5. Set the PLL0EN and SSCG0EN bit in the SYSC0_RUNCKSRER register to "All-0".
(PLL and SSCG-PLL are disabled.)

(8)-2-6. Set the SYSC0_RUNPLL0CNTR, SYSC0_RUNSSCG0CNTR0 and SYSC0_RUNSSCG0CNTR1 register to appropriate value to avoid profile error.

For details on the combination of violation settings, see "Profile" in the chapter of "Low-Power Consumption" in Traveo™ Platform hardware manual.

(8)-2-7. Set the SYSC1_RUNENR register to "0xAB".

(8)-2-8. Set the SYSC0_TRGRUNCNTR register to "0xAB". (The RUN profile update starts.)

(8)-2-9. Wait until the RUNDFO bit in the SYSC0_SYSSTSR register becomes "1".

(9) PSS Mode Transition (Processing by software)

See "Operation Procedure" in the chapter of "Low-Power Consumption" in Traveo™ Platform hardware manual and transition to PSS mode.

(10) PSS Mode Transition Completion (Processing by hardware)

There has been a transition to PSS mode according to the PSS profile register settings at "(6)."

(11) RTC Count State (Processing by hardware)

Hardware waits until the RTC count value reaches the cycles set at "(7)."

After the cycles are reached, there is a transition to PWU mode.

For a transition from RUN mode to PSS mode, the RTC is not initialized. For this reason, after the transition from RUN mode to PSS mode, the time until the transition to PWU mode is less than the setting at "(7)."

(The time depends on the RTC count value at the transition to PSS mode.)

(12) High-speed CR Oscillation on (Processing by hardware)

Hardware turns on high-speed CR oscillation.

Stabilization wait time is inserted to turn on high-speed CR oscillation.

This wait time is set at "(1)."

PWU mode operates with the output clock of the high-speed CR oscillation.

(13) "H" Output of the PWUTRG Pin (Processing by hardware)

Hardware changes PWUTRG to "H".

PWUTRG is "L" before this processing.

(14) A/D Start Wait State (Processing by hardware)

Hardware waits until it arrives at the time set at "(5)."

The power supply of external devices is assumed to be stable during this wait period.

When the time comes, A/D conversion request (PWU_ADT) is issued and A/D conversion is started.

(15) A/D Conversion (Processing by hardware)

A/D conversion is executed according to the settings at "(4)."

(16) A/D Conversion Judgment (Processing by hardware)

Hardware waits until the conversion of all selected channels (maximum of 8 channels) completes.

(17) "L" Output of the PWUTRG Pin (Processing by hardware)

Hardware switches PWUTRG output from "H" to "L".

(18) High-speed CR Oscillator and A/D Converter both off (Processing by hardware)

Hardware turns off the high-speed CR oscillator and A/D converter.

(19) Range Comparison Judgment (Processing by hardware)

Hardware judges whether a range deviation has arisen as a result of the A/D conversion at "(15)."

If no deviation has arisen, there is a transition to PSS mode again.

If a deviation has arisen, a WAKEUP signal is issued, followed by a transition to RUN mode to wake up the CPU.

(20) RUN Mode Transition (Processing by hardware)

For details on the operation, see "Operation Procedure" in the chapter of "Low-Power Consumption" in Traveo™ Platform hardware manual .

(21) RUN Mode Transition Completion (Processing by hardware)

The transition to RUN mode has completed.
There are the following notes to design software.

(21)-1. Regarding PSS enable setting

Set PSEN0 bit in SYSC0_PSEN0 register to "0x00".
Otherwise, written data to registers in SYSC0 is invalid. Bus error will occur.
But the set to PSEN1 bit in SYSC1_PSEN0 register is not required
because of initialization with power down.

(21)-2. Regarding the judgment of wakeup factor

If the following "(21)-2-1" and "(21)-2-2" both are "0" before "(9) PSS mode transition (processing by software)" and "1" after RUN mode transition, you are able to judge RUN mode transition occurred by A/D range deviation.

(21)-2-1. RCIRQ0 to RCIRQ31 in ADC12B1_RCIRQ0 register

(21)-2-2. CDONEIRQ0 to CDONEIRQ31 in ADC12B1_CDONEIRQ0 register

Moreover, in case that you set in "(2). Interrupt enable" process,
RUN mode transition might occur by the factor you set.
You need to confirm these interrupt flag.

(21)-3. Regarding A/D Converter use after RUN mode transition

The corresponding A/D Channel Trigger Status flag (ADC12B1_TRGST0.TRGST and ADC12B1_CHSTAT0~31.TRGST) is set if A/D conversion request (PWU_ADT) occurs in PWU mode.
It is not allowed to update the A/D converter setting during A/D conversion operation (ADC12B1_TRGST0.TRGST and ADC12B1_CHSTAT0~31.TRGST="1")
After run mode transition, clear all trigger status flags in case of changing A/D converter setting.

Example of settings

Write "1" to TRGCL0 to TRGCL31 bits in ADC12B1_TRGCL0 register.

For a detailed explanation of the A/D Channel Trigger Status flags, see the chapter of "12/10/8-Bit Analog To Digital Converter" on this manual.

When using hardware trigger as active trigger of A/D Converter Unit1 in RUN mode, write "0" to ADHWTS bit in PWU_ADTC register to make the other activation factor available.

For a detailed description of the A/D conversion hardware trigger select, refer to Section4.

3.3. Timing Charts

Figure 3-3, Figure 3-4, and Figure 3-5 are timing charts related to the transition to partial wakeup mode.

Figure 3-3 With a Range Deviation Arising after a Transition from PSS Mode to PWU Mode

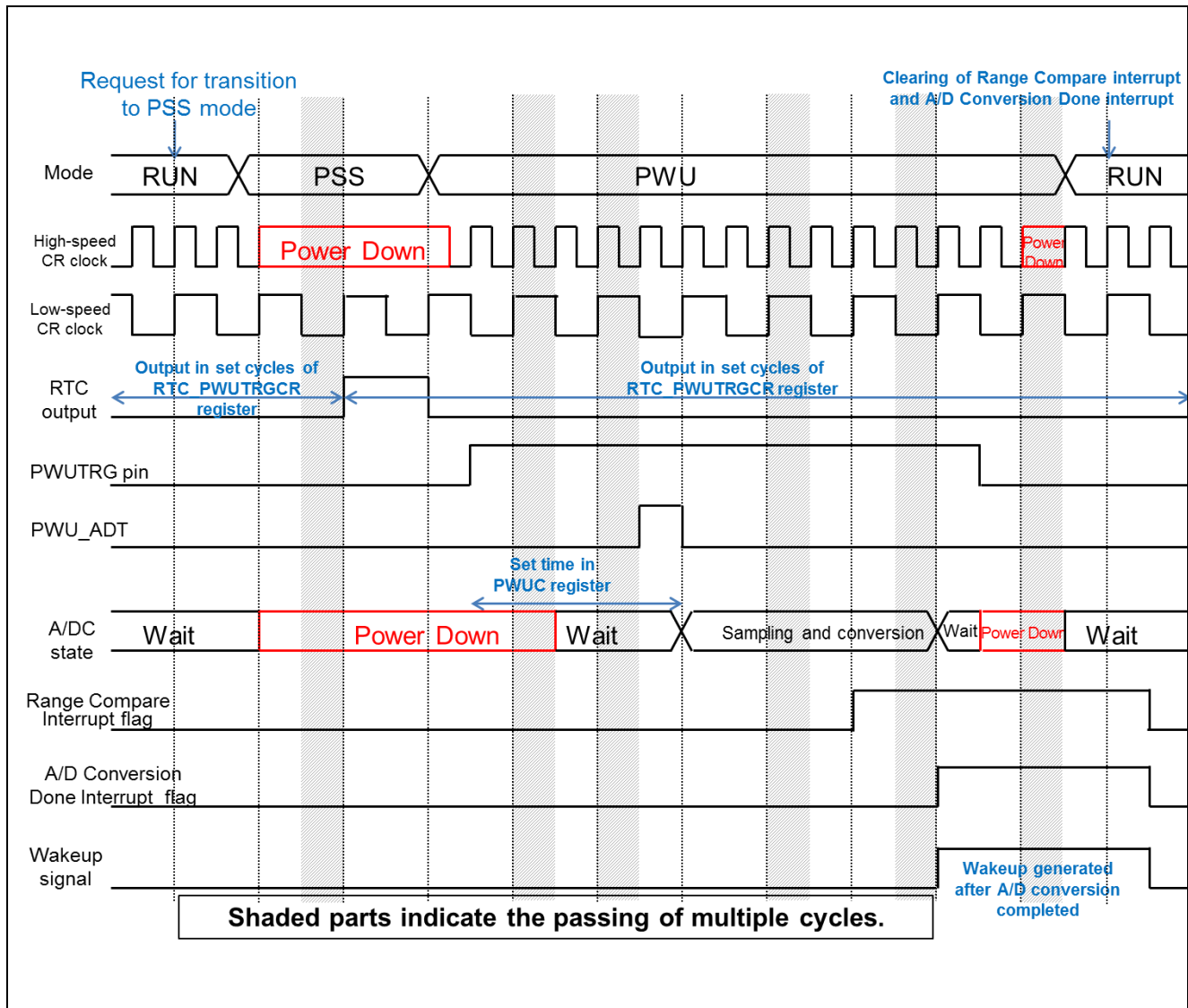


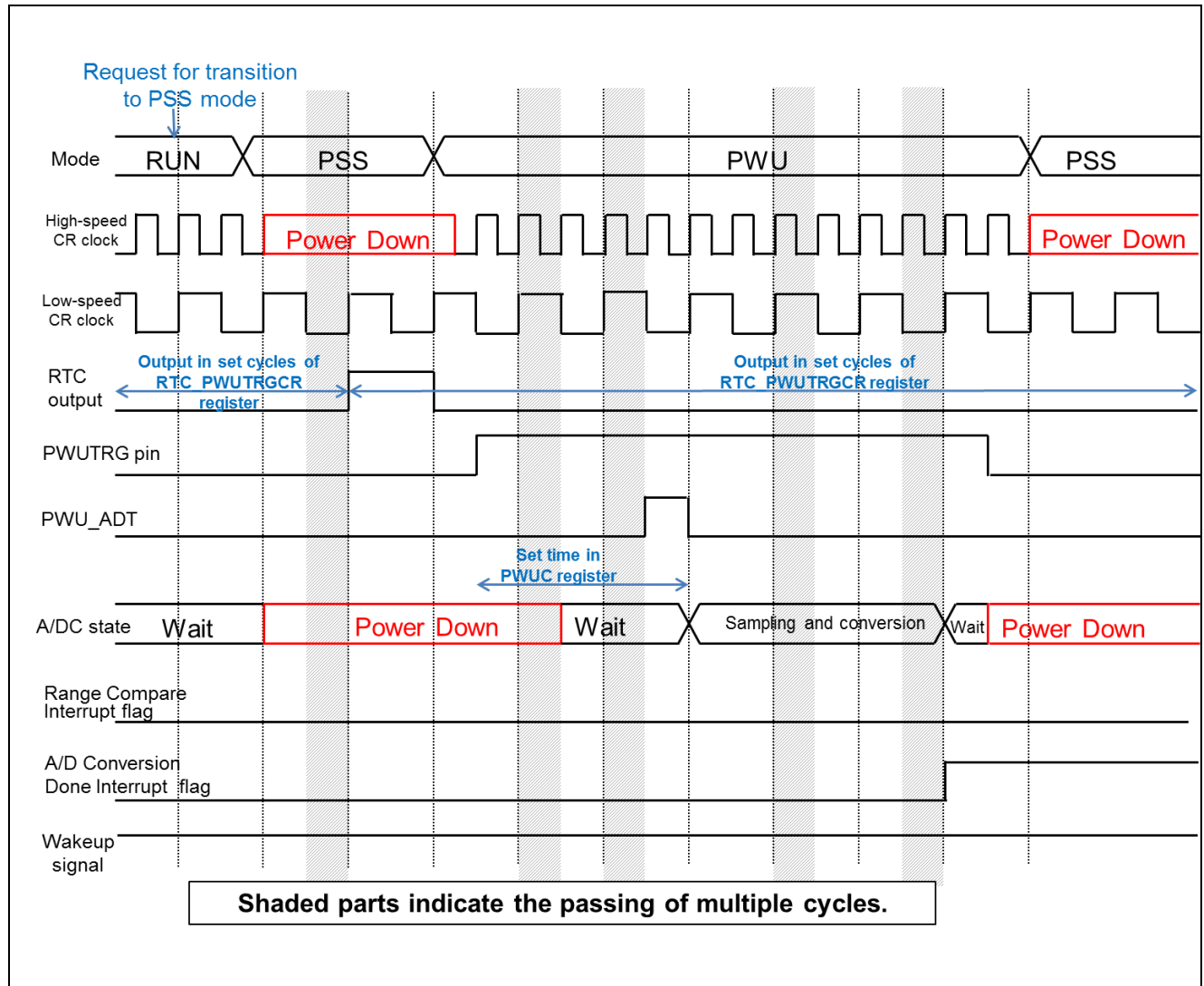
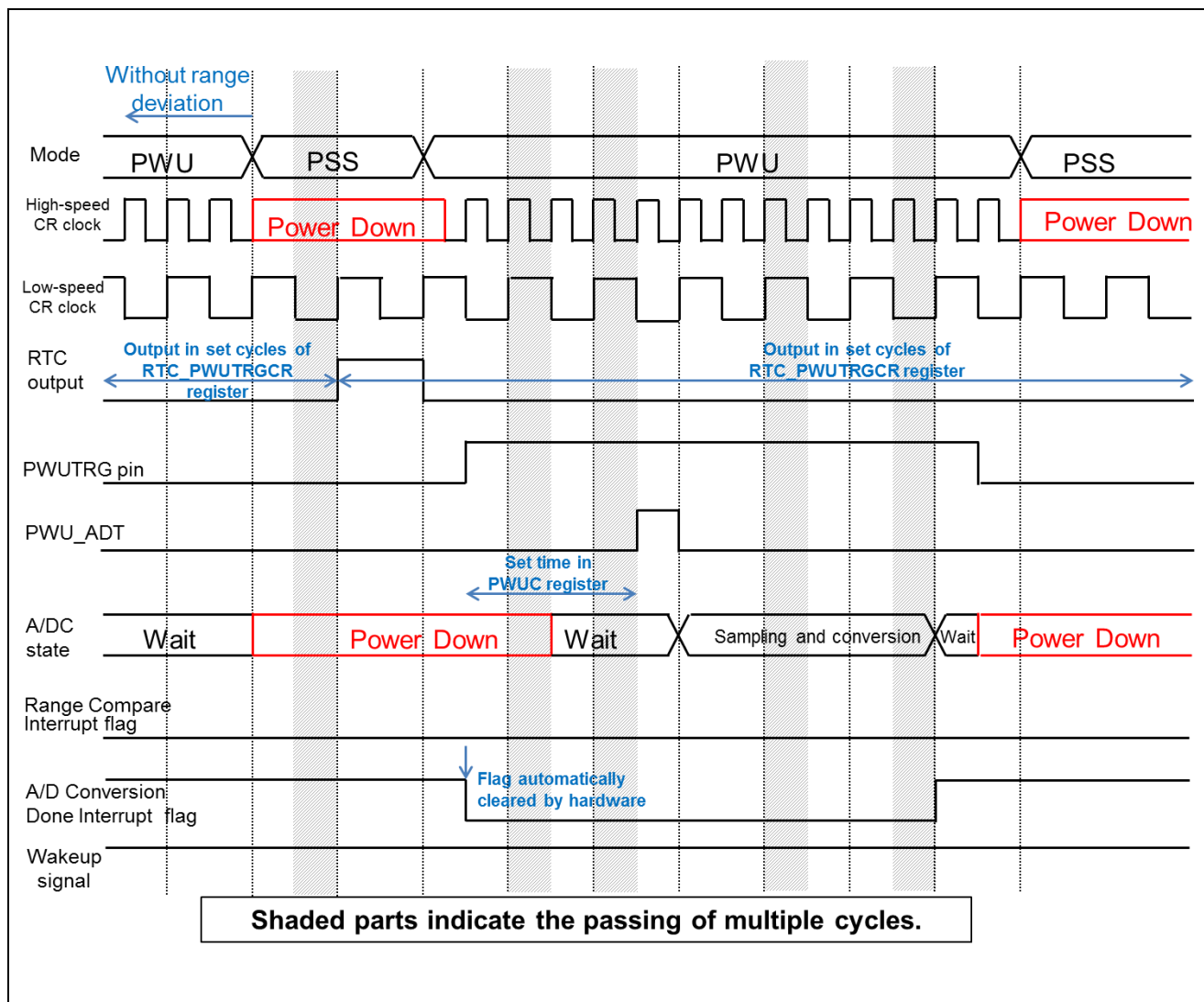
Figure 3-4 Without a Range Deviation Arising after a Transition from PSS Mode to PWU Mode


Figure 3-5 Until a Restart of A/D Conversion after Figure 3-4.

**Note:**

- The clocks in the figures do not match the actual number of cycles.

4. Registers

This section explains the partial wakeup control register.

Table 4-1 List of the Partial Wakeup Control Register

Abbreviated Register Name	Register Name	Reference
PWU_PWUC	PWU control register	4.1
PWU_ADTC	A/D Conversion Request Trigger Control Register	4.2
PWU_ADOCS	A/D Conversion Offset Compensation value Select Register	4.3

Table 4-2 Memory Map and Initial Values of the Partial Wakeup Control Register

Offset	+3	+2	+1	+0
0x00000000	Reserved	Reserved	PWU_ADTC 00000000	PWU_PWUC 00000000
0x00000004	Reserved	Reserved	Reserved	PWU_ADOCS 00000000

The offset value is the value for the "Partial Wake Up" area start address.

The partial wakeup register is deployed after the register of A/D converter unit 1.

4.1. PWU Control Register (PWU_PWUC)

The PWU control register (PWUC) is used to enable PWU mode and to set the period between PWUTRG pin output and A/D conversion start.

Bit	7	6	5	4	3	2	1	0
Field	PWUE	ADSTS6	ADSTS5	ADSTS4	ADSTS3	ADSTS2	ADSTS1	ADSTS0
R/W Attribute	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Protection Attribute	-							
Initial Value	0	0	0	0	0	0	0	0

[bit7] PWUE: PWU mode enable bit

bit	Description
0	Disable transition to PWU mode.
1	Enable transition to PWU mode.

- This bit is used to enable transition to PWU mode.
- When this bit is "1", there is a transition from PSS mode to PWU mode.

[bit6:0] ADSTS [6:0]: A/D conversion start time setting bits

ADSTS [6:0]	Setting	Value for High-speed CR Oscillator, 4 MHz
0000000	200 cycles of high-speed CR oscillation cycle	50 us
0000001	400 cycles of high-speed CR oscillation cycle	100 us
0000010	600 cycles of high-speed CR oscillation cycle	150 us
...	...	...
N	$(n+1) \times 200$ cycles of high-speed CR oscillation cycle	$(n+1) \times 50$ us
...	...	...
1100011	20000 cycles of high-speed CR oscillation cycle	5000 us
1100100	20200 cycles of high-speed CR oscillation cycle	5050 us
1100101	20400 cycles of high-speed CR oscillation cycle	5100 us
110011x	20400 cycles of high-speed CR oscillation cycle	5100 us
1101xxx		
111xxxx		

These bits are used to set the period between PWUTRG pin output and A/D conversion start.

4.2. A/D Conversion Request Trigger Control Register (PWU_ADTC)

The A/D Conversion Request Trigger Control Register configures the logical channel which uses PWU_ADT as A/D Conversion activation trigger.

Bit	15	14	13	12	11	10	9	8
Field	ADHWTS	Reserved	Reserved	ADSTCH[4]	ADSTCH[3]	ADSTCH[2]	ADSTCH[1]	ADSTCH[0]
R/W Attribute	R/W	RX, WX	RX, WX	R/W	R/W	R/W	R/W	R/W
Protection Attribute	-							
Initial Value	0	0	0	0	0	0	0	0

[bit15] ADHWTS: A/D conversion Hardware Trigger Select bit

bit	Description
0	Hardware trigger of A/D conversion request is the other activation factor.
1	Hardware trigger of A/D conversion request is A/D conversion request for PWU (PWU_ADT).

- The other activation factor is configured at RESSEL bit in RIC_RESIN register.
- When this bit is set to “1”, PWU_ADT is selected as hardware trigger of A/D Converter unit 1.
- Before PWU mode transition, set “1” to this bit.
- When using hardware trigger as active trigger of A/D Converter unit1 in RUN mode, write “0” to this bit.

Notes:

- These bits are not allowed to update during A/D conversion operation (ADC12Bn_TRGST0.TRGST and ADC12Bn_CHSTATi.TRGST=“1”).
- When this setting is changed, confirm A/D conversion request isn’t issued (ADC12Bn_TRGST0.TRGST and ADC12Bn_CHSTATi.TRGST=“0”).

[bit14:13] Reserved: Reserved bits

- Reading this bit returns an undefined.
- Writing data to these bits has no effect on the operation.

[bit12:8] ADSTCH [4:0]: A/D conversion start channel setting bits

ADSTCH [4:0]	Description
00000	The logical channel 0 is selected.
00001	The logical channel 1 is selected.
...	...
N	The logical channel N is selected.
...	...
11110	The logical channel 30 is selected.
11111	The logical channel 31 is selected.

These bits are used to set the period between PWUTRG pin output and A/D conversion start.

- Set the first logical channel number of the group procedure executing in the PWU mode.
- PWU_ADT is selected as hardware trigger of the logical channel set at this register.
- When TRGTYP of the logical channel selected at this register is set to Software or Hardware (TRGTYP[1:0] = “01”), A/D conversion request of the corresponding logical channel occurs after PWU mode transition.

4.3. A/D Conversion Offset Compensation Value Select Register (PWU_ADOCS)

The A/D Conversion Offset Compensation value Select Register configures the offset value of each A/DC unit.

Bit	7	6	5	4	3	2	1	0
Field	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	OCVSEL1	OCVSEL0
R/W Attribute	RX, WX	RX, WX	RX, WX	RX, WX	RX, WX	RX, WX	R/W	R/W
Protection Attribute	-							
Initial Value	0	0	0	0	0	0	0	0

[bit7:2] Reserved: Reserved bits

- Reading this bit returns an undefined.
- Writing data to these bits has no effect on the operation.

[bit1:0] OCVSEL1~0: A/DC Offset Compensation Value Select bits

bit	Description
0	The value of A/D Converter Offset Compensation Setting Register (ADC12Bn_OCV) is selected.
1	The proper trimming value is selected.

- After the reset is released, the value of A/D Converter Offset Compensation Setting Register (ADC12Bn_OCV) is selected as A/DC Offset Compensation value.
 - When this bit is set to “1”, the proper trimming value is selected as the offset value.
- For details, see the chapter of “12/10/8-Bit Analog To Digital Converter” on this manual.

Notes:

- *These bits are not allowed to update during A/D conversion operation (ADC12Bn_TRGST0.TRGST and ADC12Bn_CHSTATi.TRGST=“1”).*
- *When this setting is changed, confirm A/D conversion request isn’t issued (ADC12Bn_TRGST0.TRGST and ADC12Bn_CHSTATi.TRGST=“0”).*

5. Precautions for Using This Device

This section provides notes on using the partial wakeup control function.

Time until Transition to PWU Mode

For a transition from RUN mode to PSS mode, the RTC is not initialized.

For this reason, after the transition from RUN mode to PSS mode, the time until the transition to PWU mode is less than the setting at "(7)."

(The time depends on the RTC count value at the transition to PSS mode.)

Restrictions on A/D Conversion Data

If an interrupt factor other than a range comparison interrupt causes a return to RUN mode during A/D conversion, the A/D conversion results (values recorded in the A/D data register) are not guaranteed. Examples of this factor include external interrupts and RTC interrupts.

Restrictions on the Range Comparison Function

The range comparison function sets the upper and lower limit thresholds for voltage and judges A/D conversion results.

8 analog input channels can be used in PWU mode.

However, for pairs of the upper limit thresholds and lower limit thresholds that can be set, select from 4 sets.

Restrictions on Port Settings

- Before transitioning to PSS mode, be sure to use the port function to set for output of the PWUTRG function.
- The state of ports at the generation of various resets is "output Hi-Z" and "input disabled."

Restrictions on Software Watchdog Timer Settings

If the settings of the software watchdog timer in PSS mode contradict the contents of the SYSC0_PSSCKSRER register that have been set in "PSS Setting (Processing by software)" in Section "3.Explanation of Operation", a PSS profile error occurs. It cannot transition to PSS mode.

Be careful when setting the software watchdog timer.

For details on the combination of violation settings, see "Profile" in the chapter of "Low-Power Consumption" in Traveo™ Platform hardware manual.

For details on the setting procedure examples of the software watchdog timer, see " Example of set procedure" in the chapter of "Software Watchdog Timer" in Traveo™ Platform hardware manual.

Restrictions on the Cycles for Transitioning to PWU Mode

The term of 8ms is generated from the following calculation in RTC.

$$0.25[s] \div 32 = 7.8125[ms] (\approx 8[ms])$$

Moreover as RTC operates with low-speed CR (typical 100KHz) in PWU mode, the actual cycles for transitioning to PWU mode become as the following.

- 7.81[ms] (The description in this chapter is "8ms")
- 15.62[ms] (The description in this chapter is "16ms")
- 23.43[ms] (The description in this chapter is "24ms")
- 31.24[ms] (The description in this chapter is "32ms")
- 39.05[ms] (The description in this chapter is "40ms")
- 46.86[ms] (The description in this chapter is "48ms")
- 54.67[ms] (The description in this chapter is "56ms")
- 62.48[ms] (The description in this chapter is "64ms")

Restrictions on the A/D conversion Hardware Trigger Settings

- Before PSS mode transition, be sure to select the PWU A/D conversion trigger (PWU_ADT) as A/D conversion trigger.

Restriction for Fast CR OFF in PSS Mode

It is necessary to enable (PSS Clock Source Enable Register (SYSC0_PSSCKSRER: CROSCEN=1)) Fast CR in PSS mode.

But if the following restrictions are satisfied in user system, it can be used with Fast CR OFF to reduce the current consumption in PSS mode.

- CKTOR flag

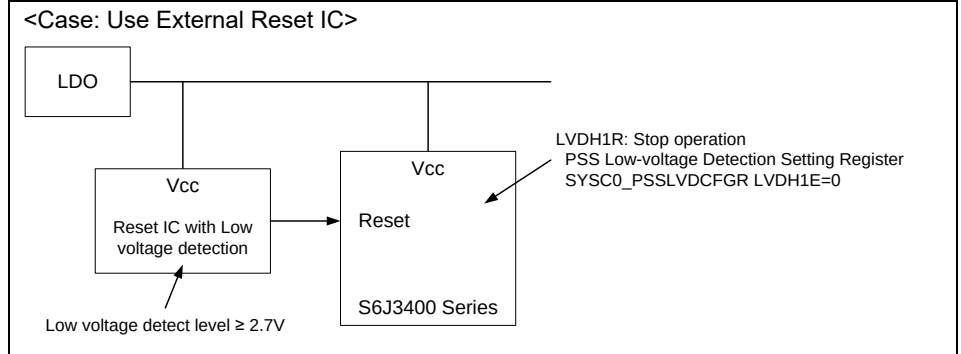
There is a possibility that CKTOR flag of User Reset Factor Register (SYSC_RSTCAUSEUR) is set, when a reset from one of the following reset sources is asserted in PSS mode (PD2: ON/OFF).

 - External Reset (RSTX)
 - External Power Supply Low-Voltage Detection Reset (LVDH1R)
- LVDH1R setting condition

If Fast CR is set to disable in PSS mode, the following conditions are required to avoid malfunction of the device after recovery from PSS mode.

 - RSTX asserting in the MCU operation range ($\geq 2.7V$) as Low voltage detect.
 - Change LVDH1R setting to stop operation (PSS Low-voltage Detection Setting Register SYSC0_PSSLVDCFR: LVDH1E = "0")
 - Workaround

- To reduce power consumption (Fast CR off: PSS Clock Source Enable Register (SYSC0_PSSCKSRER: CROSCEN=0)) in PSS mode, it is necessary for a workaround as following.
- Example of a recommended circuit



CHAPTER 25: Programmable CRC



This chapter explains the function and operation of the Programmable CRC.

1. Overview
2. Configuration and Block Diagram
3. Operation of the Programmable CRC
4. Registers

CODE: PRGCRC-S6J3200-E1

1. Overview

This section describes the features and the block diagram of the Programmable CRC.

Features of Programmable CRC

The Programmable CRC is a software configurable module with serial CRC calculation logic as hardware implementation. The serial CRC logic works on modulo-2 arithmetic for calculation of checksum. The CRC module can detect errors in data blocks by calculating a checksum.

- Programmable 8-, 16-, 24-, or 32-bit input data width
- Programmable polynomial value (polynomial degree from 2 to 32)
- Programmable initial seed value
- Programmable final checksum XOR value
- Interrupt and DMA trigger capability
- Configurable input/output bit reflection and byte swapping. This facilitates the different settings of common CRC standards and the handling of data organized in little or big endian format
- Supports block/multiple data transfers (more than 32-bit)

Areas of Application

- Data security/integrity
- Communication protocols

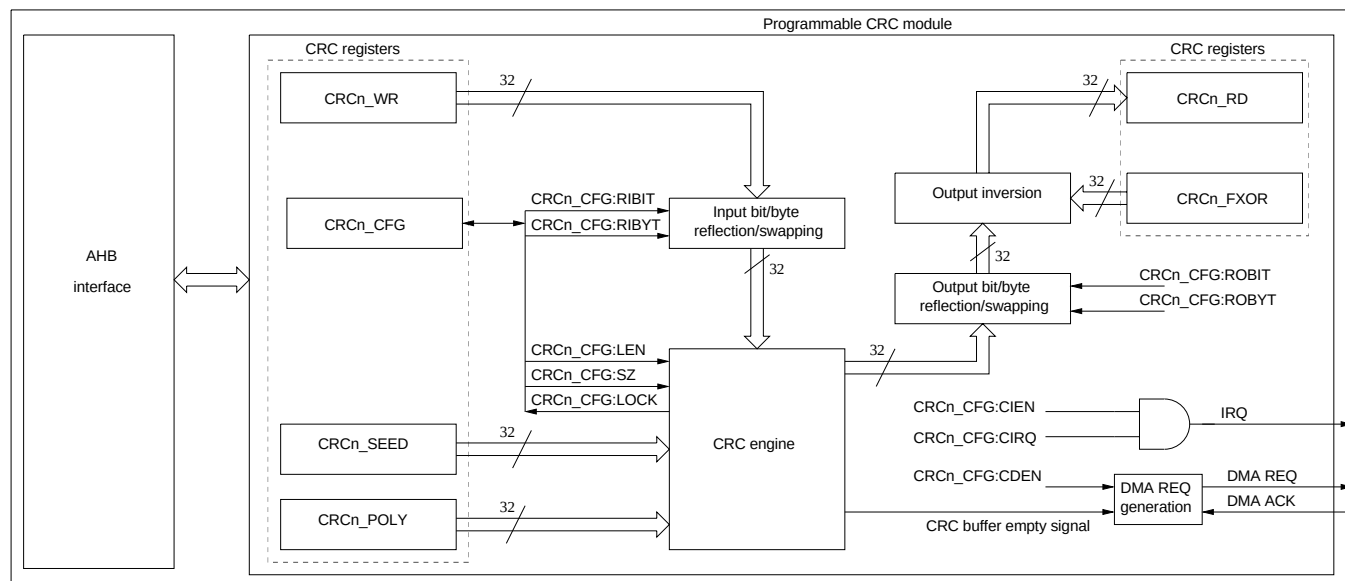
Programmable CRC module can be configured to widely used common CRC standards, some of them are listed below:

- CRC-32-IEEE 802.3
- CRC-16-CCITT
- CRC-8-CCITT
- CRC-5-USB
- CRC-XMODEM
- 12-bit CRC
- 10-bit CRC
- 8-bit CRC

2. Configuration and Block Diagram

This section shows a block diagram of Programmable CRC

Figure 2-1 Block diagram of Programmable CRC



3. Operation of the Programmable CRC

This section describes operation of Programmable CRC in detail.

For more details on flowcharts for CRC operation see Section 3.1, on CRC calculation flow see Section 3.2, and on an example for CRC calculation see Section 3.3

3.1. CRC Operation Flowcharts

The flowcharts Figure 3-1, Figure 3-2 , and Figure 3-3 show the steps to configure CRC registers and to perform a CRC calculation.

Figure 3-1 Polling Based CRC Operation

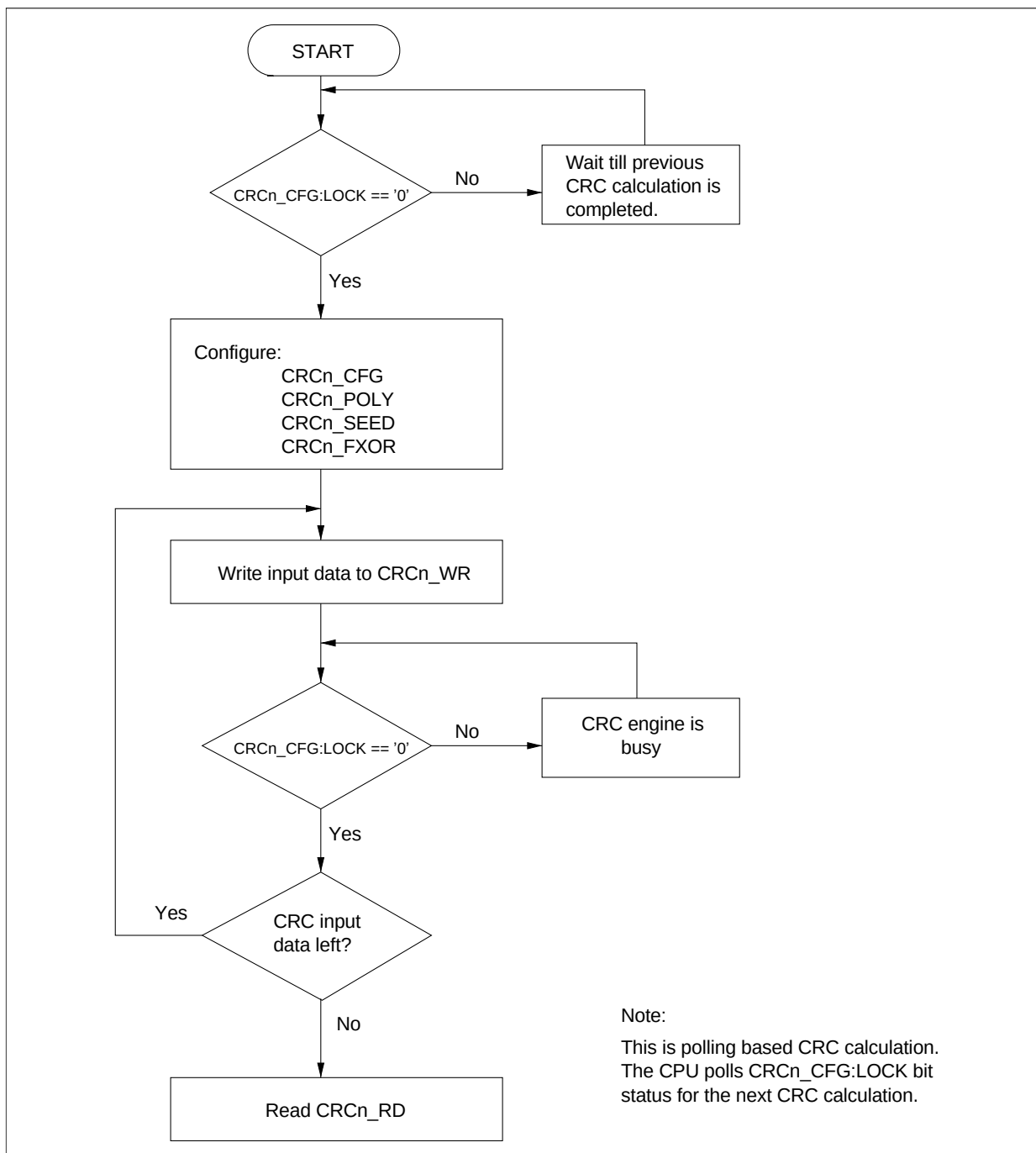


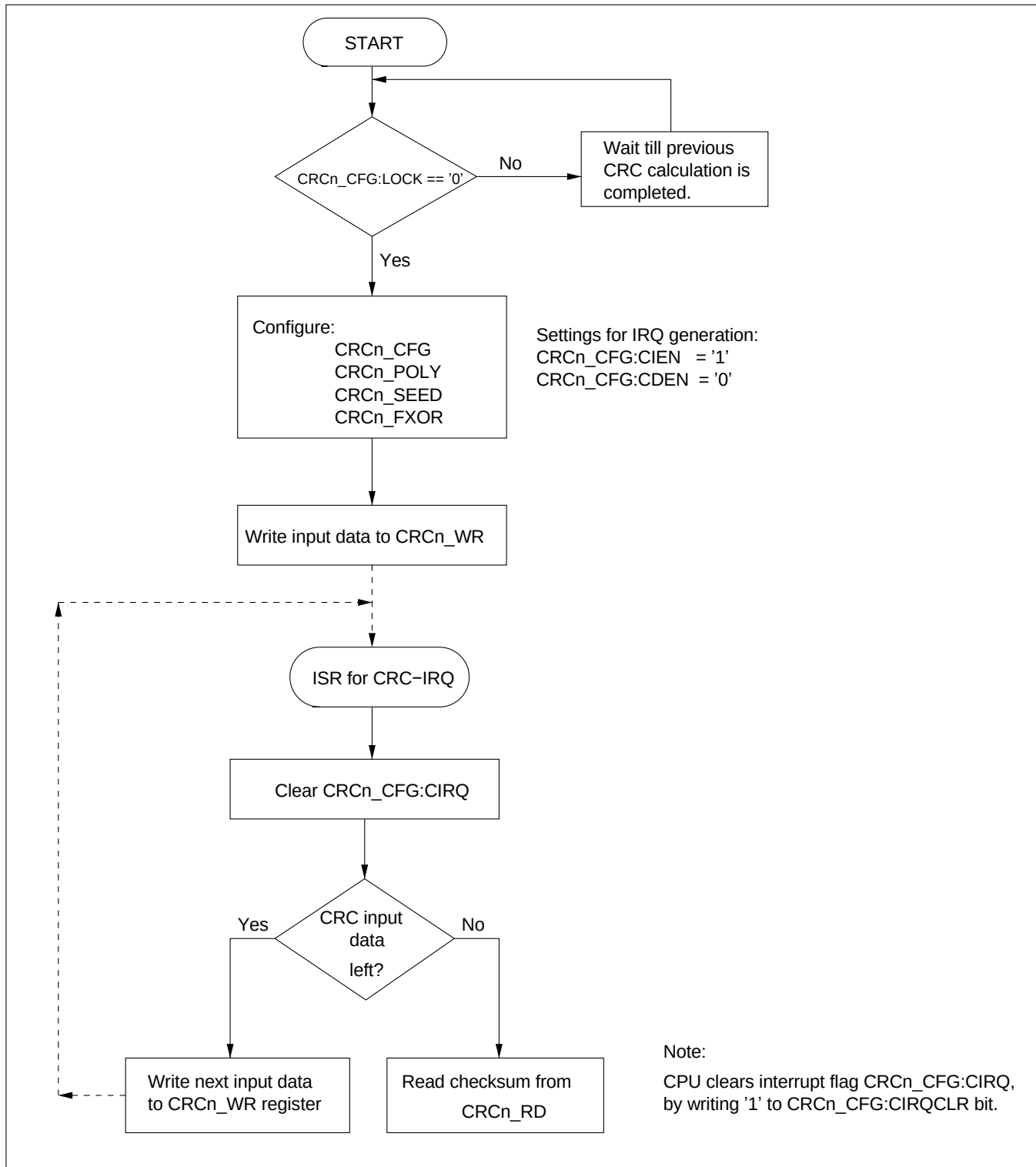
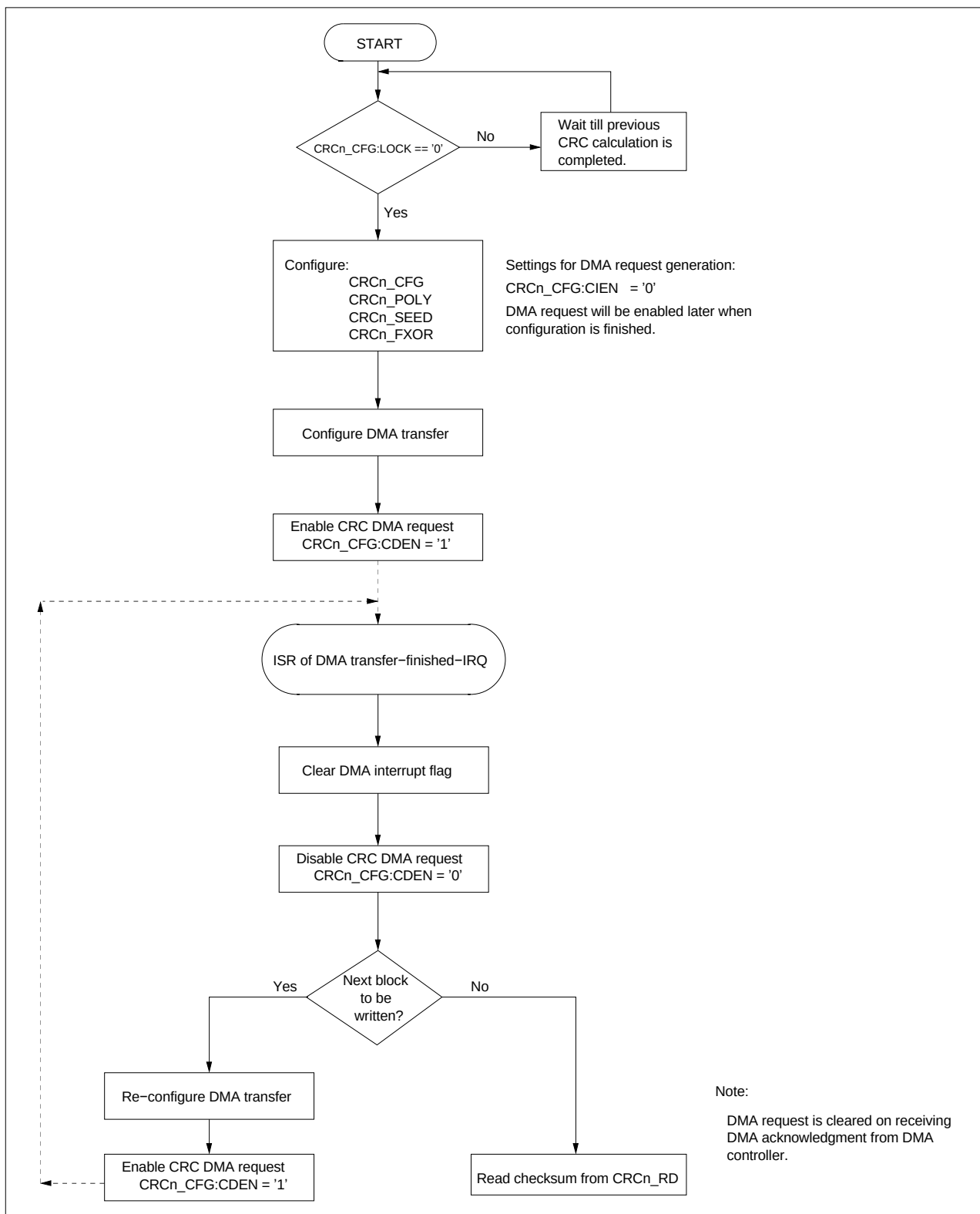
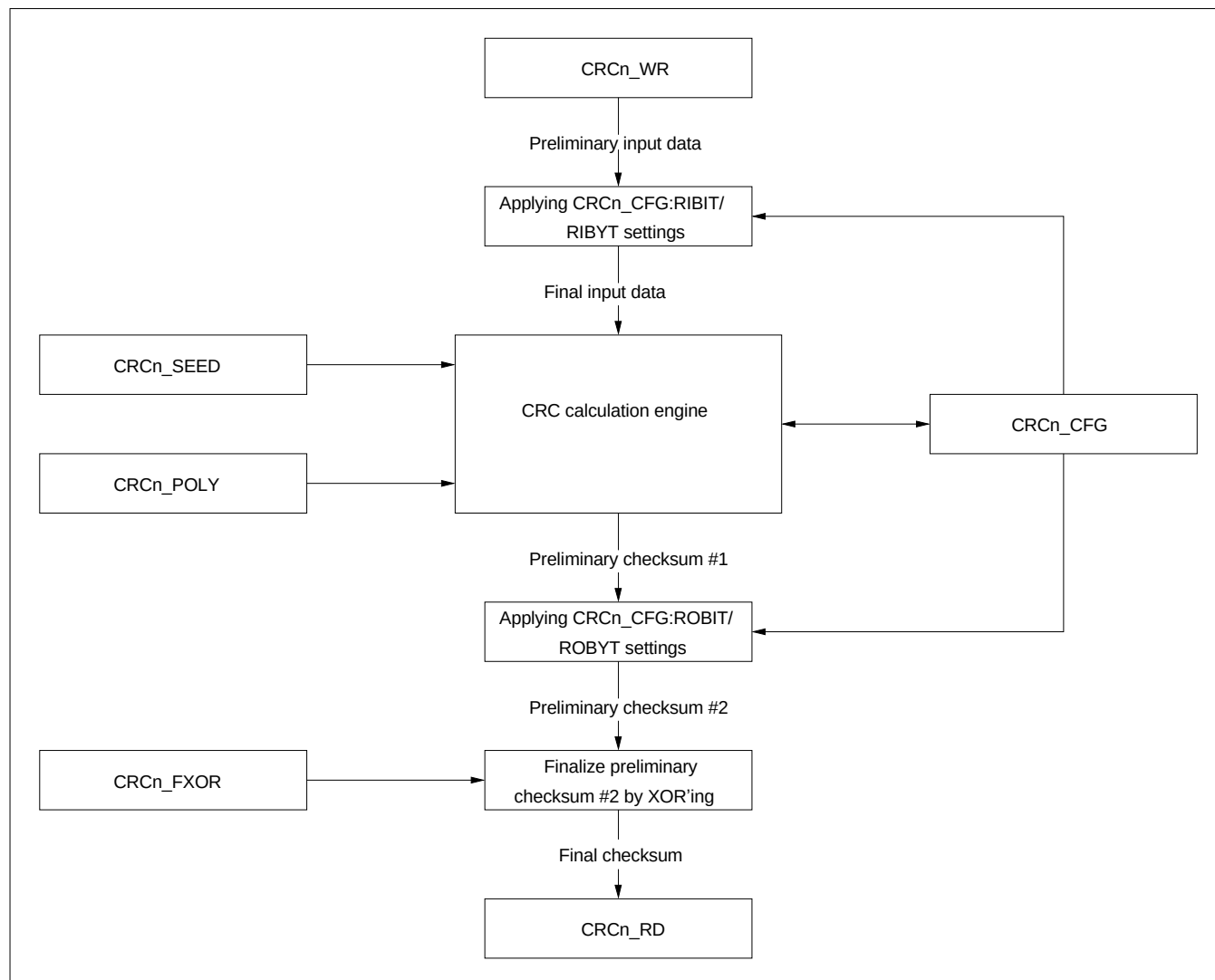
Figure 3-2 CRC Operation with IRQ

Figure 3-3 CRC operation with DMA request


3.2. CRC Input Data and Checksum Calculation Flow

Figure 3-4 Block Diagram of CRC Input Data and Checksum Calculation Flow



1. The input data for which CRC is to be calculated is written to CRCn_WR register. This is the 'preliminary input data'.
2. The 'preliminary input data' bytes can be swapped/reflected bit-wise using CRCn_CFG:RIBIT and/or byte-wise using CRCn_CFG:RIBYT before they enter the CRC engine. The settings are shown below:

'preliminary input data' in CRCn WR register:

A7----A0 B7----B0 C7----C0 D7----D0

If the input data size is less than 32-bit ($SZ < '11'$), then the remaining bits (8-,16-, or 24-bit) of the data are considered as don't care (X) as shown in below table.

Table 3-1 Preliminary Input Data Bit-Wise and/or Byte-Wise Reflection/Swapping

RIBYT	RIBIT	SZ	Final Input Data for CRC Engine			
			+3	+2	+1	+0
'0'	'0'	'00'	XXXX XXXX	XXXX XXXX	XXXX XXXX	D7----- D0
		'01'	XXXX XXXX	XXXX XXXX	C7-----C0	D7-----D0
		'10'	XXXX XXXX	B7-----B0	C7-----C0	D7-----D0
		'11'	A7-----A0	B7-----B0	C7-----C0	D7-----D0
	'1'	'00'	XXXX XXXX	XXXX XXXX	XXXX XXXX	D0-----D7
		'01'	XXXX XXXX	XXXX XXXX	C0-----C7	D0-----D7
		'10'	XXXX XXXX	B0-----B7	C0-----C7	D0-----D7
		'11'	A0-----A7	B0-----B7	C0-----C7	D0-----D7
'1'	'0'	'00'	XXXX XXXX	XXXX XXXX	XXXX XXXX	D7-----D0
		'01'	XXXX XXXX	XXXX XXXX	D7-----D0	C7-----C0
		'10'	XXXX XXXX	D7-----D0	C7-----C0	B7-----B0
		'11'	D7-----D0	C7-----C0	B7-----B0	A7-----A0
	'1'	'00'	XXXX XXXX	XXXX XXXX	XXXX XXXX	D0-----D7
		'01'	XXXX XXXX	XXXX XXXX	D0-----D7	C0-----C7
		'10'	XXXX XXXX	D0-----D7	C0-----C7	B0-----B7
		'11'	D0-----D7	C0-----C7	B0-----B7	A0-----A7

- The 'preliminary input data' after applying the settings of CRCn_CFG:RIBIT/RIBYT results in the 'final input data', which is sent to the CRC engine for checksum calculation.
- The CRCn_SEED register provides the initial value to the CRC engine. The required polynomial is provided by CRCn_POLY register. The CRC engine starts its operation once CRCn_WR register is written with the input data.
- CRC engine performance: The performance of CRC engine for CRC checksum calculation is based on the input data size and number of clock cycles (bus clock) required to complete a calculation. The shows number of clock cycles required to get final checksum at CRCn_RD register with respect to input data size.

Table 3-2 Clock Cycles Requirement for Checksum Calculation

Input Data Size	Number of Clock Cycles Required for Final Checksum at CRCn_RD
8-bit	Input data size (8-bit) + 2 = 10 clock cycles.
16-bit	Input data size (16-bit) + 2 = 18 clock cycles.
24-bit	Input data size (24-bit) + 2 = 26 clock cycles.
32-bit	Input data size (32-bit) + 2 = 34 clock cycles.

- The 'preliminary checksum #1' bytes can be swapped/reflected bit-wise using CRCn_CFG:ROBIT and/or byte-wise using CRCn_CFG:ROBYT. shows at which positions the checksum bits of 'preliminary checksum #1' S[(LEN-1):0] will be located in 'preliminary checksum #2' after CRCn_CFG:ROBIT/ROBYT settings have been applied. Only some examples of different CRCn_CFG:LEN configurations are shown.

Note:

- Only some examples for CRCn_CFG:LEN are shown.

Table 3-3 Preliminary Checksum #1 Bit-Wise and/or Byte-Wise Reflection/Swapping

ROBYT	ROBIT	LEN	Preliminary Checksum #2				Action
			+3	+2	+1	+0	
'0'	'0'	32	S31---S24	S23---S16	S15---S8	S7---S0	No swapping/reflection. The checksum is aligned with the polynomial degree/length.
		21	'0000 0000'	'000 S20---S16'	S15---S8	S7---S0	No swapping/reflection. The checksum is aligned with the polynomial degree/length. The bits S21 to S31 are '0'.
		16	'0000 0000'	'0000 0000'	S15---S8	S7---S0	No swapping/reflection. The checksum is aligned with the polynomial degree/length. The bits S16 to S31 are '0'.
		3	'0000 0000'	'0000 0000'	'0000 0000'	'00000 S2---S0'	No swapping/reflection. The checksum is aligned with the polynomial degree/length. The bits S3 to S31 are '0'.
	'1'	32	S24---S31	S16---S23	S8---S15	S0---S7	Byte aligned checksum reflection.
		21	'0000 0000'	'S16---S20 000'	S8---S15	S0---S7	Bit reflection. The checksum is byte aligned. Bit S21-S23 and S24-S31 are '0'.
		16	'0000 0000'	'0000 0000'	S8---S15	S0---S7	Bit reflection. The checksum is byte aligned. Bit S16-S31 are '0'.
		3	'0000 0000'	'0000 0000'	'0000 0000'	'S0---S2 00000'	Bit reflection. The checksum is byte aligned. Bit S3-S7 and S8-S31 are '0'.

ROBYT	ROBIT	LEN	Preliminary Checksum #2				
			+3	+2	+1	+0	Action
'1'	'0'	32	S7---S0	S15---S8	S23---S16	S31---S24	Byte aligned checksum swapping.
		21	'0000 0000'	S7---S0	S15---S8	'000 S20---S16'	Byte swapping. The checksum is byte aligned. Bit S21-S23 and S24-S31 are '0'.
		16	'0000 0000'	'0000 0000'	S7---S0	S15---S8	Byte aligned checksum swapping. Bit S16-S31 are '0'.
		3	'0000 0000'	'0000 0000'	'0000 0000'	'00000 S2_S0'	No byte swapping. Bit S3-S7 and S8-S31 are '0'.
	'1'	32	S0---S7	S8---S15	S16---S23	S24---S31	Bit reflection and byte swapping aligned with polynomial degree/length.
		21	'0000 0000'	'000 S0---S4'	S5---S12	S13---S20	Bit reflection and byte swapping. The checksum is aligned with polynomial length/degree. Bit S21-S23 and S24-S31 are '0'.
		16	'0000 0000'	'0000 0000'	S0---S7	S8---S15	Bit reflection and byte swapping. The checksum is aligned with polynomial length/degree. Bit S16-S31 are '0'.
		3	'0000 0000'	'0000 0000'	'0000 0000'	'00000 S0---S2'	Bit reflection and byte swapping. The checksum is aligned with polynomial length/degree. Bit S3-S7 and S8-S31 are '0'.

7. The checksum after applying settings of CRCn_CFG:ROBIT/ROBYT is 'preliminary checksum #2'.
8. The 'preliminary checksum #2' is XOR'ed with the contents of CRCn_FXOR register to get the 'final checksum'.
9. The 'final checksum' gets available at CRCn_RD register.

3.3. CRC Calculation Example

Consider the following values for calculating 8-bit CRC checksum value.

Input data = 0x0F (Hex)

Polynomial = $x^8 + x^2 + x + 1$

Seed = 0xFF (Hex)

Final XOR = 0x00 (Hex)

The coefficients of the polynomial are arranged in .

Table 3-4 Coefficients of the Polynomial

x8	x7	x6	x5	x4	x3	x2	x1	x0
1	0	0	0	0	0	1	1	1

The highest order coefficient x8 provides the degree of the CRC polynomial and the checksum length, respectively. It must not be set to '1' while configuring CRCn_POLY register, instead CRCn_CFG:LEN should be configured (here it is CRCn_CFG:LEN = 8). Therefore, the value of the polynomial that is written to CRCn_POLY register in accordance with above coefficients is 0x07 (Hex).

The input/output bit reflection is disabled in this example.

The Programmable CRC registers should be configured as follows for the given values:

The CRC configuration register is configured by considering 8-bit input data size and 8-bit polynomial/checksum length as follows.

CRCn_CFG = 0x00080000 (Hex)

CRCn_POLY = 0x00000007 (Hex)

CRCn_SEED = 0x000000FF (Hex)

CRCn_FXOR = 0x00000000 (Hex)

CRCn_WR = 0x0000000F (Hex)

The final result of CRC checksum calculation is 0xDE (Hex), which gets available after 10 clock cycles (once CRCn_WR is written) in the CRCn_RD register.

If another input data is given to the CRC module, then 'preliminary checksum #1' (0xDE) is used as the initial seed value.

If the new CRC calculation should start from the seed value instead of from the last CRC result, then the CRCn_SEED register needs to be re-written (even if it is the same seed value as before).

4. Registers

All Programmable CRC registers are explained in this section.

The suffix 'n' in the register name indicates that the register is an instance 'n' of the module.

Registers of Programmable CRC

The following registers are available for each instance of Programmable CRC:

- CRC Polynomial Register (CRCn_POLY)
- CRC Seed Register (CRCn_SEED)
- CRC Final XOR Register (CRCn_FXOR)
- CRC Configuration Register (CRCn_CFG)
- CRC Write Register (CRCn_WR)
- CRC Read Register (CRCn_RD)

Memory Layout of Programmable CRC Registers

Figure 4-1 Memory Layout of Programmable CRC Registers

Offset	+3	+2	+1	+0
0x00000000	CRCn_POLY 00000100 11000001 00011101 10110111			
0x00000004	CRCn_SEED 11111111 11111111 11111111 11111111			
0x00000008	CRCn_FXOR 11111111 11111111 11111111 11111111			
0x0000000C	CRCn_CFG 00000000 11100000 00000000 00000000			
0x00000010	CRCn_WR 00000000 00000000 00000000 00000000			
0x00000014	CRCn_RD 00000000 00000000 00000000 00000000			

4.1. CRC Polynomial Register (CRCn_POLY)

The CRC Polynomial Register (CRCn_POLY) defines the polynomial value for the CRC checksum calculation.

CRC Polynomial Register (CRCn_POLY)

BIT_OFFSET	31	30	29	28	27	26	25	24
BIT_NAME	POLY[31]	POLY[30]	POLY[29]	POLY[28]	POLY[27]	POLY[26]	POLY[25]	POLY[24]
ACCESS_TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
PROT_TYPE	Rp/Wp							
INITIAL_VALUE	0	0	0	0	0	1	0	0

BIT_OFFSET	23	22	21	20	19	18	17	16
BIT_NAME	POLY[23]	POLY[22]	POLY[21]	POLY[20]	POLY[19]	POLY[18]	POLY[17]	POLY[16]
ACCESS_TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
PROT_TYPE	Rp/Wp							
INITIAL_VALUE	1	1	0	0	0	0	0	1

BIT_OFFSET	15	14	13	12	11	10	9	8
BIT_NAME	POLY[15]	POLY[14]	POLY[13]	POLY[12]	POLY[11]	POLY[10]	POLY[9]	POLY[8]
ACCESS_TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
PROT_TYPE	Rp/Wp							
INITIAL_VALUE	0	0	0	1	1	1	0	1

BIT_OFFSET	7	6	5	4	3	2	1	0
BIT_NAME	POLY[7]	POLY[6]	POLY[5]	POLY[4]	POLY[3]	POLY[2]	POLY[1]	POLY[0]
ACCESS_TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
PROT_TYPE	Rp/Wp							
INITIAL_VALUE	1	0	1	1	0	1	1	1

[bit31:0] POLY[31:0] : CRC Polynomial

The CRCn_POLY contains the CRC polynomial. The degree of the polynomial must be between 2 to 32. Initial value is the common CRC-32 polynomial 0x04C11DB7 ($x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1$). The highest degree of coefficient should be used to configure polynomial/checksum length (CRCn_CFG:LEN).

Note:

- If the polynomial length as defined by CRCn_CFG:LEN is less than 32-bit, then the upper bits [31:LEN] must be written to '0' by the programmer. The highest order degree must not be set to '1' while configuring CRCn_POLY register, as it is implicitly defined by CRCn_CFG:LEN.

4.2. CRC Seed Register (CRCn_SEED)

The CRC Seed Register (CRCn_SEED) defines the initial value for the CRC checksum calculation.

CRC Seed Register (CRCn_SEED)

BIT_OFFSET	31	30	29	28	27	26	25	24
BIT_NAME	SEED[31]	SEED[30]	SEED[29]	SEED[28]	SEED[27]	SEED[26]	SEED[25]	SEED[24]
ACCESS_TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
PROT_TYPE	Rp/Wp							
INITIAL_VALUE	1	1	1	1	1	1	1	1

BIT_OFFSET	23	22	21	20	19	18	17	16
BIT_NAME	SEED[23]	SEED[22]	SEED[21]	SEED[20]	SEED[19]	SEED[18]	SEED[17]	SEED[16]
ACCESS_TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
PROT_TYPE	Rp/Wp							
INITIAL_VALUE	1	1	1	1	1	1	1	1

BIT_OFFSET	15	14	13	12	11	10	9	8
BIT_NAME	SEED[15]	SEED[14]	SEED[13]	SEED[12]	SEED[11]	SEED[10]	SEED[9]	SEED[8]
ACCESS_TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
PROT_TYPE	Rp/Wp							
INITIAL_VALUE	1	1	1	1	1	1	1	1

BIT_OFFSET	7	6	5	4	3	2	1	0
BIT_NAME	SEED[7]	SEED[6]	SEED[5]	SEED[4]	SEED[3]	SEED[2]	SEED[1]	SEED[0]
ACCESS_TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
PROT_TYPE	Rp/Wp							
INITIAL_VALUE	1	1	1	1	1	1	1	1

[bit31:0] SEED[31:0] : CRC SEED

CRCn_SEED contains the initial value for checksum calculation. If the seed value is not initialized for the next operation (even if the seed value is identical to the previous operation), then calculation is continued from the last state with the current checksum value as initial value. Initial value for seed register is 0xFFFFFFFF.

Note:

- The CRCn_SEED register should be configured with respect to the polynomial length (CRCn_CFG:LEN). If the polynomial length is less than 32-bit, then the upper bits [31:LEN] must be written to '0' by the programmer.

4.3. CRC Final XOR Register (CRCn_FXOR)

The CRC Final XOR register (CRCn_FXOR) contains the values to be XOR'ed with the preliminary checksum to finalize the CRC calculation

CRC Final XOR Register (CRCn_FXOR)

BIT_OFFSET	31	30	29	28	27	26	25	24
BIT_NAME	FXOR[31]	FXOR[30]	FXOR[29]	FXOR[28]	FXOR[27]	FXOR[26]	FXOR[25]	FXOR[24]
ACCESS_TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
PROT_TYPE	Rp/Wp							
INITIAL_VALUE	1	1	1	1	1	1	1	1

BIT_OFFSET	23	22	21	20	19	18	17	16
BIT_NAME	FXOR[23]	FXOR[22]	FXOR[21]	FXOR[20]	FXOR[19]	FXOR[18]	FXOR[17]	FXOR[16]
ACCESS_TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
PROT_TYPE	Rp/Wp							
INITIAL_VALUE	1	1	1	1	1	1	1	1

BIT_OFFSET	15	14	13	12	11	10	9	8
BIT_NAME	FXOR[15]	FXOR[14]	FXOR[13]	FXOR[12]	FXOR[11]	FXOR[10]	FXOR[9]	FXOR[8]
ACCESS_TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
PROT_TYPE	Rp/Wp							
INITIAL_VALUE	1	1	1	1	1	1	1	1

BIT_OFFSET	7	6	5	4	3	2	1	0
BIT_NAME	FXOR[7]	FXOR[6]	FXOR[5]	FXOR[4]	FXOR[3]	FXOR[2]	FXOR[1]	FXOR[0]
ACCESS_TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
PROT_TYPE	Rp/Wp							
INITIAL_VALUE	1	1	1	1	1	1	1	1

[bit31:0] FXOR [31:0] : CRC XOR Data

The contents of CRCn_FXOR register are XOR'ed with the preliminary checksum data (after CRCn_CFG:ROBIT/ROBYT settings have been applied) and then the final checksum is moved to CRCn_RD register. Initial value for final XOR register is 0xFFFFFFFF.

Notes:

- The bits of this register affect the corresponding bits of the CRCn_RD register. Therefore, the bits not belonging to the checksum should be written to '0'. For the position of the checksum bits depending on the used output bit/byte reflection refer to Table 3-3.

4.4. CRC Configuration Register (CRCn_CFG)

The CRC Configuration Register (CRCn_CFG) is used to set the operation mode of the CRC module. CRCn_CFG register describes the polynomial/checksum length, input data size, and input/output bit/byte reflection. It indicates the status of CRC operation. Interrupt and DMA requests are also configured using CRCn_CFG register.

CRC Configuration Register (CRCn_CFG)

BIT_OFFSET	31	30	29	28	27	26	25	24
BIT_NAME	read0	read0	read0	LOCK	read0	CDEN	CIEN	CIRQ
ACCESS_TYPE	R0,WX	R0,WX	R0,WX	R,WX	R0,WX	R/W	R/W	R,WX
PROT_TYPE	Rp/Wp							
INITIAL_VALUE	0	0	0	0	0	0	0	0

BIT_OFFSET	23	22	21	20	19	18	17	16
BIT_NAME	SZ[1]	SZ[0]	LEN[5]	LEN[4]	LEN[3]	LEN[2]	LEN[1]	LEN[0]
ACCESS_TYPE	R/W	R7W	R/W	R/W	R/W	R/W	R/W	R/W
PROT_TYPE	Rp/Wp							
INITIAL_VALUE	1	1	1	0	0	0	0	0

BIT_OFFSET	15	14	13	12	11	10	9	8
BIT_NAME	read0	read0	read0	read0	RIBIT	RIBYT	ROBIT	ROBYT
ACCESS_TYPE	R0,WX	R0,WX	R0,WX	R0,WX	R/W	R/W	R/W	R/W
PROT_TYPE	Rp/Wp							
INITIAL_VALUE	0	0	0	0	0	0	0	0

BIT_OFFSET	7	6	5	4	3	2	1	0
BIT_NAME	read0	read0	read0	read0	read0	read0	read0	CIRQCLR
ACCESS_TYPE	R0,WX	R0,WX	R0,WX	R0,WX	R0,WX	R0,WX	R0,WX	R0,W
PROT_TYPE	Rp/Wp							
INITIAL_VALUE	0	0	0	0	0	0	0	0

[bit31:29] read0 : -

[bit28] LOCK : CRC Engine Status bit

This bit indicates the status of the CRC engine.

bit	Description
0	CRC engine is ready, new data can be written to CRC registers
1	CRC engine is busy and writing to CRC registers is not possible. If the data is written to the CRC registers when LOCK bit is '1', then an error response is generated

[bit27] read0 : -**[bit26] CDEN : DMA Request Enable bit**

This bit enables/disables the DMA request

bit	Description
0	Disable the DMA request
1	Enable the DMA request

DMA request is generated when CRC is in buffer empty state and CRCn_CFG:CDEN is set. DMA ISR should clear this bit after final transfer. Clearing this bit by CPU at any other time might lead to unwanted behavior.

[bit25] CIEN : CRC Interrupt Enable bit to CPU

This bit enables/disables the interrupt request.

bit	Description
0	Disable the interrupt request
1	Enable the interrupt request

The IRQ is triggered when CRCn_CFG:CIEN bit is enabled and CRC interrupt flag (CRCn_CFG:CIRQ) is set.

[bit24] CIRQ : CRC Interrupt Flag

This bit indicates the interrupt status of CRC.

bit	Description
0	No interrupt request Note: CPU clears interrupt flag by writing CRCn_CFG:CIRQCLR bit to '1':
1	Interrupt request

Checksum has been calculated by CRC engine and is available in CRCn_RD register.

[bit23:22] SZ[1:0] : CRC Input Data Size Configuration bits

These bits are used to configure the input data size as follows

bit[1:0]	Description
00	8-bit
01	16-bit
10	24-bit
11	32-bit

[bit21:16] LEN[5:0] : CRC Polynomial/Checksum Length Configuration bits

These bits are used to configure the length (degree) of CRC polynomial/checksum as follows:

bit[5:0]	Description
100000	32
011111	31
.....	
000010	2

Note:

- The following settings are not supported:
- $CRCn\_CFG:LEN > 32$
- $CRCn\_CFG:LEN < 2$

[bit15:12] read0 : -

[bit11] RIBIT : Reflect Input Bits

bit	Description
0	Disable input bit reflection
1	Enable input bit reflection

When the input data in the $CRCn\_WR$ register is passed to the CRC engine, the bit ordering of each byte within input data is reversed. For more details refer to Section 'Operation of the Programmable CRC'.

[bit10] RIBYT : Reflect Input Bytes

bit	Description
0	Disable input byte reflection (swapping)
1	Enable input byte reflection (swapping)

When the input data in the $CRCn\_WR$ register is passed to the CRC engine, the byte ordering of input data is reversed. Only the bytes of the configured input data size $CRCn\_CFG:SZ$ are affected. For more details refer to Section "Operation of the Programmable CRC".

Note:

- For 8-bit input data, this setting has no effect.

[bit9] ROBIT : Reflect Output Bits

bit	Description
0	Disable output bit reflection
1	Enable output bit reflection

The bit ordering of each byte within checksum is reversed, before passing the checksum to final XOR'ing stage. For more details refer to Section "Operation of the Programmable CRC".

[bit8] ROBYT : Reflect Output Bytes

bit	Description
0	Disable output byte reflection (swapping)
1	Enable output byte reflection (swapping)

The byte ordering of checksum data is reversed, before passing the byte aligned polynomial length of checksum data to final XOR'ing stage. For more details refer to Section "Operation of the Programmable CRC".

Note:

- For the checksum data less than or equal to 8 bits, this setting has no effect.

[bit7:1] read0 : -**[bit0] CIRQCLR : Interrupt Clear**

This bit clears the CRC interrupt flag.

bit	Description
0	Write '0' is ignored, reading this bit always returns '0'
1	Clear CRC interrupt flag (CRCn_CFG:CIRQ)

4.5. CRC Write Register (CRCn_WR)

The input data for the CRC checksum calculation must be written to the CRC Write Register (CRCn_WR).

CRC Write Register (CRCn_WR)

BITS_OFFSET	31	30	29	28	27	26	25	24
BITS_NAME	CRCWR[31]	CRCWR[30]	CRCWR[29]	CRCWR[28]	CRCWR[27]	CRCWR[26]	CRCWR[25]	CRCWR[24]
ACCESS_TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
PROT_TYPE	Rp/Wp							
INITIAL_VALUE	0	0	0	0	0	0	0	0

BITS_OFFSET	23	22	21	20	19	18	17	16
BITS_NAME	CRCWR[23]	CRCWR[22]	CRCWR[21]	CRCWR[20]	CRCWR[19]	CRCWR[18]	CRCWR[17]	CRCWR[16]
ACCESS_TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
PROT_TYPE	Rp/Wp							
INITIAL_VALUE	0	0	0	0	0	0	0	0

BITS_OFFSET	15	14	13	12	11	10	9	8
BITS_NAME	CRCWR[15]	CRCWR[14]	CRCWR[13]	CRCWR[12]	CRCWR[11]	CRCWR[10]	CRCWR[9]	CRCWR[8]
ACCESS_TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
PROT_TYPE	Rp/Wp							
INITIAL_VALUE	0	0	0	0	0	0	0	0

BITS_OFFSET	7	6	5	4	3	2	1	0
BITS_NAME	CRCWR[7]	CRCWR[6]	CRCWR[5]	CRCWR[4]	CRCWR[3]	CRCWR[2]	CRCWR[1]	CRCWR[0]
ACCESS_TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
PROT_TYPE	Rp/Wp							
INITIAL_VALUE	0	0	0	0	0	0	0	0

[bit31:0] CRCWR[31:0] : CRC Write Register

The CRCn_WR register contains the input data, for which the CRC checksum is to be calculated. Writing to this register starts the CRC calculation process. After pre-processing (bit/byte reflection/swapping) the contents of the CRCn_WR register are passed to the CRC engine (the contents of CRCn_SEED register are also provided). There it is divided by the content of CRCn_POLY register in modulo-2 arithmetic to get the final checksum after post-processing (bit/byte reflection/swapping and XOR'ing).

Note:

- The size of input data is configured by CRCn_CFG:SZ, where 8, 16, 24, and 32 bits are only supported as data size. If the input data size is less than 32-bit (i.e. 8, 16, or 24 bits), then the invalid/unused bits are considered as don't care (X).

4.6. CRC Read Register (CRCn_RD)

The CRC Read Register (CRCn_RD) contains the final checksum of the data written to the CRCn_WR register.

CRC Read Register (CRCn_RD)

BIT_OFFSET	31	30	29	28	27	26	25	24
BIT_NAME	CRCRD[31]	CRCRD[30]	CRCRD[29]	CRCRD[28]	CRCRD[27]	CRCRD[26]	CRCRD[25]	CRCRD[24]
ACCESS_TYPE	R,W	R,W	R,W	R,W	R,W	R,W	R,W	R,W
PROT_TYPE	Rp/Wp							
INITIAL_VALUE	0	0	0	0	0	0	0	0

BIT_OFFSET	23	22	21	20	19	18	17	16
BIT_NAME	CRCRD[23]	CRCRD[22]	CRCRD[21]	CRCRD[20]	CRCRD[19]	CRCRD[18]	CRCRD[17]	CRCRD[16]
ACCESS_TYPE	R,W	R,W	R,W	R,W	R,W	R,W	R,W	R,W
PROT_TYPE	Rp/Wp							
INITIAL_VALUE	0	0	0	0	0	0	0	0

BIT_OFFSET	15	14	13	12	11	10	9	8
BIT_NAME	CRCRD[15]	CRCRD[14]	CRCRD[13]	CRCRD[12]	CRCRD[11]	CRCRD[10]	CRCRD[9]	CRCRD[8]
ACCESS_TYPE	R,W	R,W	R,W	R,W	R,W	R,W	R,W	R,W
PROT_TYPE	Rp/Wp							
INITIAL_VALUE	0	0	0	0	0	0	0	0

BIT_OFFSET	7	6	5	4	3	2	1	0
BIT_NAME	CRCRD[7]	CRCRD[6]	CRCRD[5]	CRCRD[4]	CRCRD[3]	CRCRD[2]	CRCRD[1]	CRCRD[0]
ACCESS_TYPE	R,W	R,W	R,W	R,W	R,W	R,W	R,W	R,W
PROT_TYPE	Rp/Wp							
INITIAL_VALUE	0	0	0	0	0	0	0	0

[bit31:0] CRCRD[31:0]: CRC Read Data

The CRC Read Register contains the result (final checksum) of the CRC calculation after post-processing (applying CRCn_CFG:ROBIT, CRCn_CFG:ROBYT, and CRCn_FXOR settings). Writing any value on CRCn_RD register changes its content and it does not affect CRC calculation.

Note:

- The polynomial length (CRCn_CFG:LEN) provides the length of the final checksum. If the polynomial length is less than 32-bit, then bits not belonging to the checksum are '0' (in case the invalid bits of the CRCn_FXOR register are not programmed to '0', then these bits in CRCn_RD register might also be '1'). The bit/byte reflection settings (CRCn_CFG:ROBIT/ROBYT) can influence the checksum in CRCn_RD register. For the position of the checksum bits refer to Table 3-3.

CHAPTER 26: Clock Monitor



This chapter explains the clock monitor.

1. Overview
2. Configuration and Block Diagram
3. Operation of clock monitor
4. Registers
5. Precautions

CODE: CLKMON-S6J3400-E1

1. Overview

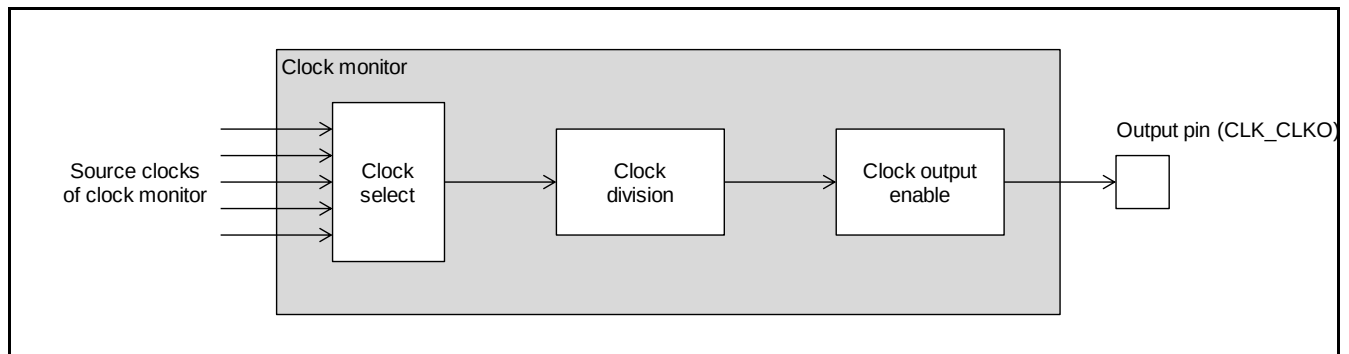
The clock monitor is a macro that outputs internal clock signals to external pin. The clock monitor has a function for dividing the frequency of a clock signal before output to the pin.

Features

- Format: Divide the internal clock signal and output to a pin (CLK_CLKO)
- Channel: 1
- Division ratio: CLK/1 to CLK/128
- Monitoring clock: Fast-CR clock, Slow-CR clock, Main clock, Sub clock, PLL0 clock, SSCG PLL0 clock and other internal clocks (CLK_CAN, CLK_LCP0, CLK_LCP0A, CLK_LCP1, CLK_LCP1A and CLK_SYSC0H)

2. Configuration and Block Diagram

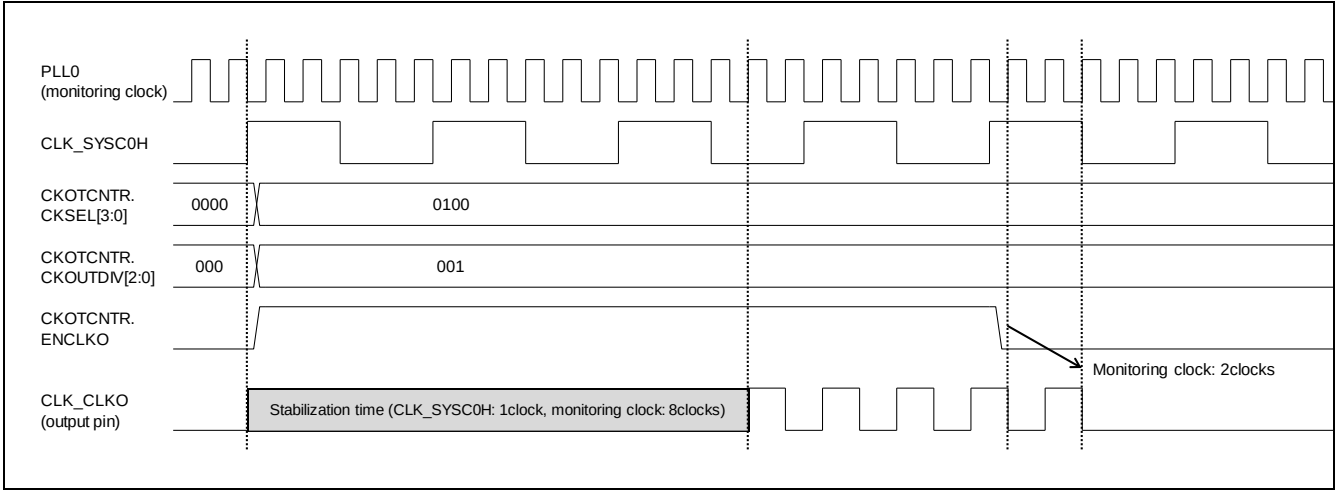
Figure 2 -1 Block Diagram of the Clock Monitor



3. Operation of Clock Monitor

This section explains the operations of the clock monitor.

Figure 3-1: Example of Clock Monitor Timing Chart (Monitoring Clock: PLL0)



4. Registers

Table 4-1: Register List

Abbreviated Register Name	Register Name	Reference
CKOTCNTR	Clock output function control register	4.1

Table 4-2: Clock Monitor Memory Map

Offset Address	Register			
	+3	+2	+1	+0
0x00000000	CKOTCNTR 00000000 00000000 00000000 00000000			

4.1. Clock Output Function Control Register (CKOTCNTR)

Clock output function control register (CKOTCNTR) is used to control clock output function.

BIT_OFFSET	31	30	29	28	27	26	25	24
BIT_NAME	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	ENCLKO
ACCESS_TYPE	R0,WX	R0,WX	R0,WX	R0,WX	R0,WX	R0,WX	R0,WX	R/W
PROT_TYPE	-							
INITIAL_VALUE	0	0	0	0	0	0	0	0

BIT_OFFSET	23	22	21	20	19	18	17	16
BIT_NAME	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
ACCESS_TYPE	R0,WX	R0,WX	R0,WX	R0,WX	R0,WX	R0,WX	R0,WX	R0,WX
PROT_TYPE	-							
INITIAL_VALUE	0	0	0	0	0	0	0	0

BIT_OFFSET	15	14	13	12	11	10	9	8
BIT_NAME	Reserved	Reserved	Reserved	Reserved	Reserved	CKOUTDIV[2]	CKOUTDIV[1]	CKOUTDIV[0]
ACCESS_TYPE	R0,WX	R0,WX	R0,WX	R0,WX	R0,WX	R/W	R/W	R/W
PROT_TYPE	-							
INITIAL_VALUE	0	0	0	0	0	0	0	0

BIT_OFFSET	7	6	5	4	3	2	1	0
BIT_NAME	Reserved	Reserved	Reserved	Reserved	CKSEL[3]	CKSEL[2]	CKSEL[1]	CKSEL[0]
ACCESS_TYPE	R0,WX	R0,WX	R0,WX	R0,WX	R/W	R/W	R/W	R/W
PROT_TYPE	-							
INITIAL_VALUE	0	0	0	0	0	0	0	0

[bit31:25] Reserved

This is a reserved bit. Writing data to these bits has no effect on operation.

[bit24] ENCLKO: Clock output enable bit

This bit controls enable/disable clock output function.

bit	Description
0	Clock output function disable
1	Clock output function enable

[bit23:11] Reserved

This is a reserved bit. Writing data to these bits has no effect on operation.

[bit10:8] CKOUTDIV[2:0]: Clock division bits

These bits configure the clock output divider.

bit10:8	Description
000	Output clock is not divided
001	Output clock is divide by 2
010	Output clock is divide by 4
011	Output clock is divide by 8
100	Output clock is divide by 16
101	Output clock is divide by 32
110	Output clock is divide by 64
111	Output clock is divide by 128

[bit7:4] Reserved

These are reserved bits. Writing data to these bits has no effect on operation.

[bit3:0] CKSEL[3:0]: Clock select bits

These bits select the source clock for clock output function.

bit3:0	Description
0000	Fast-CR clock is selected
0001	Slow-CR clock is selected
0010	Main clock is selected
0011	Sub clock is selected
0100	PLL0 clock is selected
0101	CLK_CAN is selected
0110	CLK_LCP0 is selected
0111	CLK_LCP0A is selected
1000	SSCG PLL0 clock is selected
1001	CLK_LCP1 is selected
1010	CLK_LCP1A is selected
1011	CLK_SYSC0H is selected
1100	Prohibit (Fast-CR clock is selected)
1101	Prohibit (Fast-CR clock is selected)
1110	Prohibit (Fast-CR clock is selected)
1111	Clock is tied to low

5. Precautions

The following shows the precautions when using the clock monitor.

- The frequency which can output as monitor output has a limitation and see S6J3400 datasheet. When monitoring clock is higher than the limitation frequency, always divide clock.
- Monitoring clock cannot change when selected clock or next-selected clock or CLK_SYSC0H stops.

CHAPTER 27: Bus Diagnosis Function



This chapter explains the Bus Diagnosis Function.

1. Overview
2. Configuration and Block Diagram
3. Registers
4. Operation

CODE: BUS_DIAGNOSIS-S6J3400-E1

1. Overview

The bus diagnosis function prevents an LSI malfunction by checking data that was output on a bus during access to each resource.

- Diagnosis target: Addresses and data to be output to the address and data buses, and control signals (read, write, and bus access size signals) for controlling buses
- Diagnosis bus: AHB (Common PERI #0, Common PERI #1, MCU Config Group)
- Diagnosis method: Diagnosis based on parity
 - The output side calculates parity for each 8-bit group and outputs that parity.
 - The input side checks that parity.
- Parity: Odd parity
- Test function: A parity error is generated to support program debug at bus diagnosis.
- Error detection: Control parity error
 - Address parity error
 - Data parity error
 - At error occurrence, the relevant address is displayed in the register.
- Effect: Detection of a bus disconnection
 - Detection of a bus transistor failure
 - Detection of garbled data resulting from a bus short caused by dirt
 - Detection of garbled data caused by a defective contact
- NMI notification: Control parity error, address parity error, data parity error

Features

The bus diagnosis function is realized by adding parity to address, data, and bus control signal of AHB, and by checking the parities. However, if a parity error occurs at write access to the bus diagnosis register, the NMI request signal cannot be cleared. So, the write access to bus diagnosis register is excluded from diagnosis.

When the parity error is detected at write access, write access to peripheral resource is shut off.

NMI output resulting from bus diagnosis is generated by one of the following factors:

- A control parity error (CNER) was detected.
- A data parity error (DER[3:0]) was detected.
- An address parity error (AER[3:0]) was detected.

2. Configuration and Block Diagram

This section explains the configuration of bus diagnosis function.

Figure 2-1 Configuration Diagram

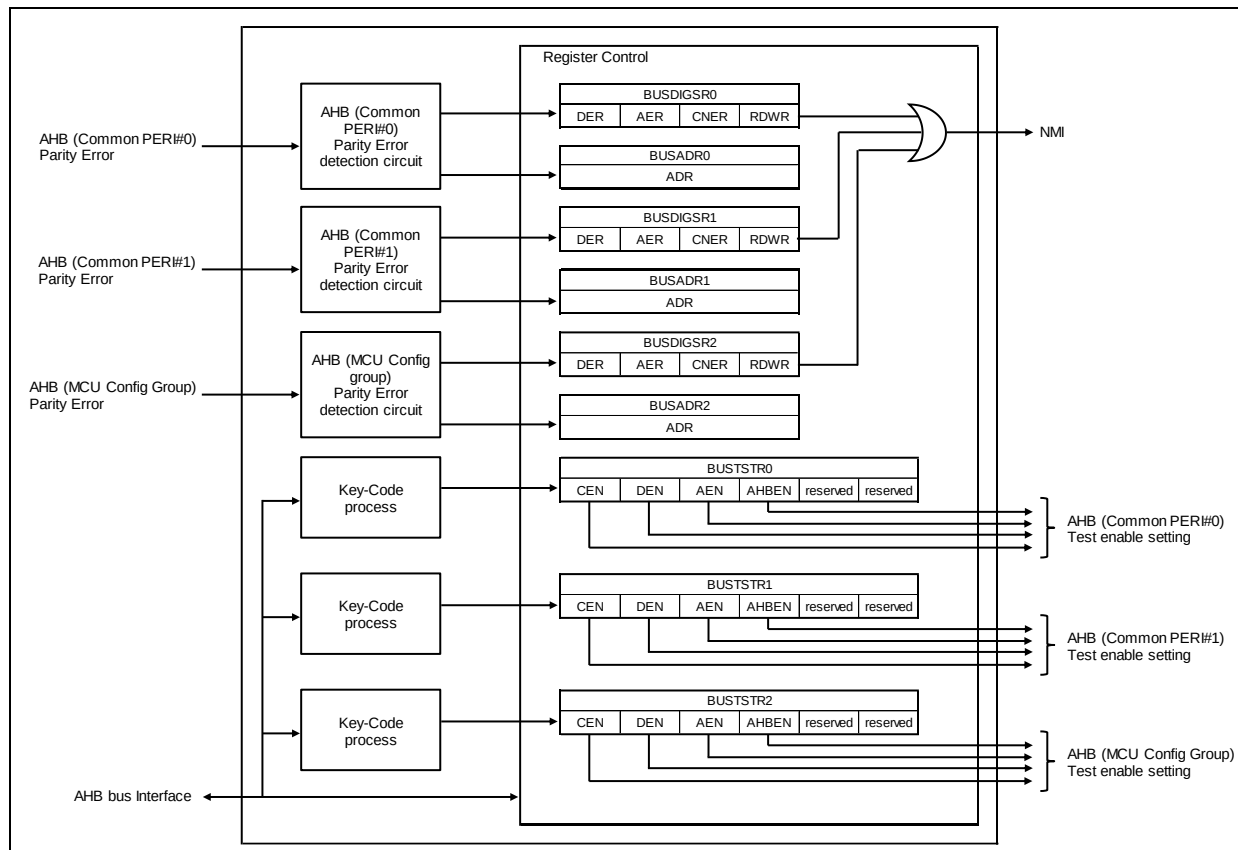
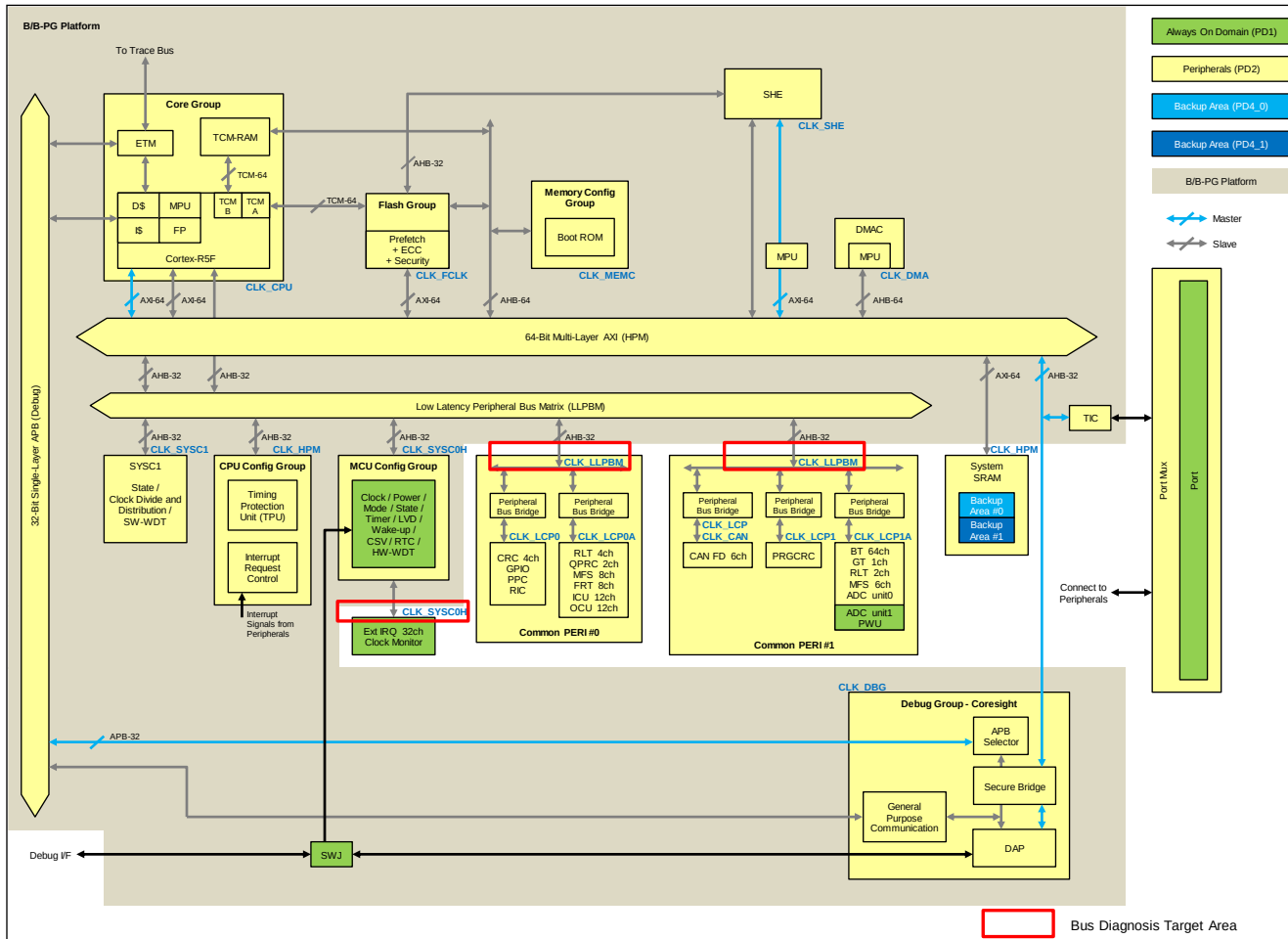


Figure 2-2 Bus Diagnosis Target Area Diagram

**Notes:**

- The address area of bus diagnosis is excluded from bus diagnosis target. (Read data is a diagnosis target.)

3. Registers

Table 3-1: Register List

Abbreviated Register Name	Register Name	Reference
BUSDIGSRn	Bus diagnosis status register	3.1
BUSTSTRn	Bus diagnosis test register	3.2
BUSADRn	Bus diagnosis address register	3.3

Table 3-2: Bus Diagnosis Memory Map

Offset Address	Register			
	+3	+2	+1	+0
0x000	Reserved		BUSDIGSR0 00000000 00000000	
0x004	BUSTSTR0 00000000 00000000		Reserved	
0x008	BUSADR0 00000000 00000000 00000000 00000000			
0x00C	Reserved			
0x010	Reserved			
0x014	Reserved		BUSDIGSR1 00000000 00000000	
0x018	BUSTSTR1 00000000 00000000		Reserved	
0x01C	BUSADR1 00000000 00000000 00000000 00000000			
0x020	Reserved			
0x024	Reserved			
0x028	Reserved		BUSDIGSR2 00000000 00000000	
0x02C	BUSTSTR2 00000000 00000000		Reserved	
0x030	BUSADR2 00000000 00000000 00000000 00000000			
0x034	Reserved			
0x038	Reserved			

Notes:

- When the reserved area is read, the read value is always "1".

3.1. Bus Diagnosis Status Register (BUSDIGSRn) (n=0-2)

The bus diagnosis status register (BUSDIGSRn) consists of a data parity error, address parity error, control parity error, data direction, and error flag clear.

Bus diagnosis status register 0 indicates AHB error status of Common PERI #0. Bus diagnosis status register 1 indicates AHB error status of Common PERI #1. Bus diagnosis status register 2 indicates AHB error status of MCU Config Group.

BIT_OFFSET	15	14	13	12	11	10	9	8
BIT_NAME	DER[3]	DER[2]	DER[1]	DER[0]	AER[3]	AER[2]	AER[1]	AER[0]
ACCESS_TYPE	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX
PROT_TYPE	-							
INITIAL_VALUE	0	0	0	0	0	0	0	0

BIT_OFFSET	7	6	5	4	3	2	1	0
BIT_NAME	PECLR	Reserved					CNER	RDWR
ACCESS_TYPE	R0/W	R0,W0					R,WX	R,WX
PROT_TYPE	-							
INITIAL_VALUE	0	00000					0	0

[bit15:12] DER3 to DER0: Data parity error

Data parity error flag. Parity is calculated for each piece of 8-bit data. If an error occurs, the associated bit is set to "1".

For DER[3]=1, a parity error occurs in bit31 to bit24 of data.

For DER[2]=1, a parity error occurs in bit23 to bit16 of data.

For DER[1]=1, a parity error occurs in bit15 to bit8 of data.

For DER[0]=1, a parity error occurs in bit7 to bit0 of data.

If these bits are "0", this indicates that no error occurs. These bits are not updated while "1" is set in any one of these bits. If these bits are set to "1", NMI occurs.

These bits are read-only. To clear them to "0", write "1" in the PECLR bit.

Notes:

- *These bits are not updated while any one of them is "1", any one of the AER bits is "1", or the CNER bit is "1".*
- *Regarding the data parity error, error detection and notification are made only for data with a valid access size.*
- *Note that it may be led to infinite loop when an error is detected after the status register is read immediately after an error of the bus diagnosis status register is cleared.*

[bit11:8] AER3 to AER0: Address parity error

Address parity error flag. Parity is calculated for each piece of 8-bit address. If an error occurs, the associated bit is set to "1".

For AER[3]=1, a parity error occurs in bit31 to bit24 of address.

For AER[2]=1, a parity error occurs in bit23 to bit16 of address.

For AER[1]=1, a parity error occurs in bit15 to bit8 of address.

For AER[0]=1, a parity error occurs in bit7 to bit0 of address.

If these bits are "0", this indicates that no error occurs. If any one of these bits is set to "1", NMI occurs. These bits are read-only. To clear them to "0", write "1" in the PECLR bit.

Notes:

- *These bits are not updated while any one of them is "1", any one of the DER bits is "1", or the CNER bit is "1".*

[bit7] PECLR: Parity error clear

Parity error clear bit. If "1" is written in this bit, the DER, AER, and CNER bits are set to "0". This bit is always "0" during reading. Writing "0" in this bit is ignored. This bit is write-only.

[bit6:2] Reserved

Always write "0" to these bits.

[bit1] CNER: Control parity error

Control parity error bit. Read/write signals for controlling buses and the data size control signal are handled as data. If a parity error occurs, this bit is set to "1".

If this bit is "0", this indicates that no error occurs. This bit is not updated while "1" is set in this bit. If this bit is set to "1", NMI occurs.

This bit is read-only. To clear it to "0", write "1" in the PECLR bit.

Notes:

- *This bit is not updated while this bit is "1", any of the AER bits is "1", or the DER bit is "1".*

[bit0] RDWR: Data direction

Data direction flag. If a data or address parity error occurs, this bit indicates that the error has occurred during reading or writing.

- The read direction is indicated when this bit is "0".
- The write direction is indicated when this bit is "1".

Notes:

- *Writing "1" in the PECLR bit does not influence this bit.*
- *This bit is not updated while the DER, AER, or CNER bit is "1".*
- *This bit is valid when any one of the DER, AER, and CNER bits is "1".*

Notes:

- *If a diagnosis error occurs during writing to bus diagnosis status register, writing continues and the target error flag is not set to "1".*
- *For access to this register, use word access or half word access instructions.*

3.2. Bus Diagnosis Test Register (BUSTSTRn) (n=0-2)

The bus diagnosis test register (BUSTSTRn) sets the bus diagnosis test function.

Bus diagnosis test register 0 sets at time of AHB bus diagnosis test of common PERI #0. Bus diagnosis test register 1 sets at time of AHB bus diagnosis test of common PERI #1. Bus diagnosis test register 2 sets at time of AHB bus diagnosis test of MCU Config Group.

BIT_OFFSET	15	14	13	12	11	10	9	8
BIT_NAME	KEY1	KEY0	-		CEN	Reserved		AHBEN
ACCESS_TYPE	R0/W	R0/W	R0,WX		R/W	R/W0		R/W
PROT_TYPE	-							
INITIAL_VALUE	0	0	00		0	0	0	0

BIT_OFFSET	7	6	5	4	3	2	1	0
BIT_NAME	DEN[3]	DEN[2]	DEN[1]	DEN[0]	AEN[3]	AEN[2]	AEN[1]	AEN[0]
ACCESS_TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
PROT_TYPE								
INITIAL_VALUE	0	0	0	0	0	0	0	0

[bit15:14] KEY1, KEY0: Key bits

Key bits. If "00", "01", "10", and "11" are continuously written in these bits, the data is updated to the data written in bit11 to bit0. However, during this continuous writing, data in bit11 to bit0 is not updated unless the same value is written in bit11 to bit0 four times. Moreover, data is not updated if the bus diagnosis register is read during writing. In this case, writing to this register continuously four times is required again.

Example:

- Write 01AA_H in BUSTSTRn.
- Next, write 41AA_H in BUSTSTRn.
- Next, write 81AA_H in BUSTSTRn.
- Next, write C1AA_H in BUSTSTRn. → With this writing, BUSTSTRn is set to 01AA_H.

[bit13:12] Undefined

"0" is always read. Writing does not affect operation.

[bit11] CEN: Control error

Control error setting bit

- If this bit is "0", the control parity is properly generated.
- If this bit is "1", a control parity error occurs.

Notes:

- For $AHBEN=0$, this bit is invalid. Under such condition, it will be the same behavior as when "0" is set to this bit.

[bit10:9] Reserved

Always write "0" to these bits.

[bit8] AHBEN: AHB parity error generation enable

This bit enables the generation of an AHB parity error.

- If this bit is "0", the AHB parity is generated as correct one (odd parity).
- If this bit is "1", the AHB parity is generated as even parity so that an error occurs.

Notes:

- For $DEN[3:0]=0000$, $AEN[3:0]=0000$, $CEN=0$, this bit is invalid. Under such condition, it will be the same behavior as when "0" is set to this bit.

[bit7:4] DEN3 to DEN0: Data error

Data error setting bits.

- If $DEN[3]$ is "0", parity in bit31 to bit24 of the data bus is properly generated.
- If $DEN[3]$ is "1", a parity error for bit31 to bit24 of the data bus is generated.
- If $DEN[2]$ is "0", parity in bit23 to bit16 of the data bus is properly generated.
- If $DEN[2]$ is "1", a parity error for bit23 to bit16 of the data bus is generated.
- If $DEN[1]$ is "0", parity in bit15 to bit8 of the data bus is properly generated.
- If $DEN[1]$ is "1", a parity error for bit15 to bit8 of the data bus is generated.
- If $DEN[0]$ is "0", parity in bit7 to bit0 of the data bus is properly generated.
- If $DEN[0]$ is "1", a parity error for bit7 to bit0 of the data bus is generated.

Notes:

- For $AHBEN=0$, these bits are invalid. Under such condition, it will be the same behavior as when "0000" is set to these bits.
- Only value set in valid data range of access size is set as an error.

[bit3:0] AEN3 to AEN0: Address error

Address error setting bits

- If AEN[3] is "0", parity in bit31 to bit24 of the address bus is properly generated.
- If AEN[3] is "1", a parity error for bit31 to bit24 of the address bus is generated.
- If AEN[2] is "0", parity in bit23 to bit16 of the address bus is properly generated.
- If AEN[2] is "1", a parity error for bit23 to bit16 of the address bus is generated.
- If AEN[1] is "0", parity in bit15 to bit8 of the address bus is properly generated.
- If AEN[1] is "1", a parity error for bit15 to bit8 of the address bus is generated.
- If AEN[0] is "0", parity in bit7 to bit0 of the address bus is properly generated.
- If AEN[0] is "1", a parity error for bit7 to bit0 of the address bus is generated.

Notes:

- *For AHBEN=0, these bits are invalid. Under such condition, it will be the same behavior as when "0000" is set to these bits.*

Notes:

- *Any interrupt is disabled during writing to the bus diagnosis test register.*
- *The bus diagnosis test register is used for debugging the bus diagnosis functions.*
- *Writing to the bus diagnosis test register is performed even if diagnosis error occurs, but the error flag of the target status register is not set to "1".*
- *For access to this register, use word access or half word access instructions.*

3.3. Bus Diagnosis Address Register (BUSADR_n) (n=0-2)

If an address parity error, data parity error, or control parity error is detected, the bus diagnosis address register (BUSADR_n) stores the relevant address. This register is valid when the DER, AER, or CNER bit of the bus diagnosis status register (BUSDIGSR_n) is "1".

Bus diagnosis address register 0 indicates an address in which an AHB diagnosis error of Common PERI #0 was detected. Bus diagnosis address register 1 indicates an address in which an AHB diagnosis error of Common PERI #1 was detected. Bus diagnosis address register 2 indicates an address in which an AHB diagnosis error of MCU Config Group was detected.

BIT_OFFSET	31	30	29	28	27	26	25	24
BIT_NAME	ADR[31]	ADR[30]	ADR[29]	ADR[28]	ADR[27]	ADR[26]	ADR[25]	ADR[24]
ACCESS_TYPE	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX
PROT_TYPE	-							
INITIAL_VALUE	0	0	0	0	0	0	0	0

BIT_OFFSET	23	22	21	20	19	18	17	16
BIT_NAME	ADR[23]	ADR[22]	ADR[21]	ADR[20]	ADR[19]	ADR[18]	ADR[17]	ADR[16]
ACCESS_TYPE	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX
PROT_TYPE	-							
INITIAL_VALUE	0	0	0	0	0	0	0	0

BIT_OFFSET	15	14	13	12	11	10	9	8
BIT_NAME	ADR[15]	ADR[14]	ADR[13]	ADR[12]	ADR[11]	ADR[10]	ADR[9]	ADR[8]
ACCESS_TYPE	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX
PROT_TYPE	-							
INITIAL_VALUE	0	0	0	0	0	0	0	0

BIT_OFFSET	7	6	5	4	3	2	1	0
BIT_NAME	ADR[7]	ADR[6]	ADR[5]	ADR[4]	ADR[3]	ADR[2]	ADR[1]	ADR[0]
ACCESS_TYPE	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX	R,WX
PROT_TYPE	-							
INITIAL_VALUE	0	0	0	0	0	0	0	0

[bit31:0] ADR31 to ADR0: Bus address

If an address or data parity error is detected, these bits indicate an address that is accessed at that detection. This register is read-only.

Notes:

- *This register is valid when any one of the DER, AER, or CNER bit of the bus diagnosis status register is "1".*
- *This register is not updated when any one of the DER, AER, or CNER bit of the bus diagnosis status register is "1".*
- *For access to this register, use word access instructions.*

4. Operation

If an access is made from AHB the bus diagnosis performs parity check for the address, data, and control buses to diagnose the address, data, and control bus as being correct.

If a bus is determined as failure by AHB the content of each error is notified to the bus diagnosis status register and address of resource to the bus diagnosis address register, and the content of failure can be determined.

During writing, no writing is made to a peripheral resource if an address parity error, data parity error and control parity error are generated.

4.1. Error Detection

When the error is detected by the bus diagnosis, access address and access direction at the time of error detection are stored in the RDWR bit of the bus diagnosis address register (BUSADR_n) and of the bus diagnosis status register (BUSDISR_n), respectively.

Moreover, when the error by the write access is detected, the write to the resource is not done.

Address Error Detection

When the parity operation result of the bus address is an error, The address error detection sets "1" to AER[3:0] bit in the bus diagnosis status register (BUSDISR_n).

AER[3:0] bit can be cleared by writing "1" to PECLR bit in this register.

Control Error Detection

When the parity operation result of the bus control is an error, the control error detection sets "1" to CNER bit in the bus diagnosis status register (BUSDISR_n).

The CNER bit can be cleared by writing "1" to PECLR bit in this register.

Data Error Detection

When the parity operation result of the bus data is an error, the data error detection sets "1" in the corresponding DER[3:0] bit of the bus diagnosis status register (BUSDIGSR_n) according to the access size of the word, the half-word, and the byte.

DER[3:0] bit can be cleared by writing "1" to PECLR bit in this register.

The error detection part of the bus diagnosis status register (BUSDIGSR_n). DER[3:0] is shown as follows.

(Detect: Error detection is done. , -: Error detection is not done.)

Access size	Address	BUSDIGSR0/1/2 (AHB)			
		DER[0]	DER[1]	DER[2]	DER[3]
		Data bit7-0	Data bit15-8	Data bit23-16	Data bit31-24
Word access	Addr+0	Detect	Detect	Detect	Detect
Half-word access	Addr+0	Detect	Detect	-	-
Half-word access	Addr+2	-	-	Detect	Detect
Byte access	Addr+0	Detect	-	-	-
Byte access	Addr+1	-	Detect	-	-
Byte access	Addr+2	-	-	Detect	-
Byte access	Addr+3	-	-	-	Detect

NMI Request Generation/Stop

NMI request is continued while either error (address error (AER[3:0]), control error (CNER) or data error (DER)) of each bus has been detected.

NMI request is discontinued when all errors (address error (AER[3:0]), control error (CNER) and data error (DER)) of each bus are cleared.

Notes:

- Bus diagnostic function generates NMI interrupt upon detecting of bus error. NMI is an interrupt that cannot be masked (i.e., cannot be suppressed).
- On software side, you must always configure an NMI process routine. If NMI process routine is undefined, and if bus failure occurs, program execution runs out of control after NMI is generated.

4.2. Test Function

This section explains the test function of bus diagnosis function.

In this function, a pseudo error can be generated if bus diagnosis test register (BUSTSTRn) is used.

The key code processing is necessary for being set to this register.

If "00", "01", "10", and "11" are not continuously written in the KEY1 and KEY0 bits, the register is not set. At this time, if the same value is not written four times, the register value is not updated.

However, even if the bus diagnosis test register is set, the pseudo data error is not detected when the reading data is all "1".

Notes:

- ALL "1" read might detect the error according to the register setting and the access requirement.
- Please refer to Notes in "Data error setting" for details.
- Only when the test function is used, the foregoing limitation is applied.

Bus Error Setting

A pseudo error can be caused for the set bus by setting "1" to AHBEN.

However, it is necessary to set "1" to either of AEN[3:0], CEN or DEN[3:0] bit at the same time.

Address Error Setting

The pseudo address error can be caused in the corresponding address bit by setting "1" to AEN[3:0].

However, it is necessary to set "1" to either of AHBEN bit at the same time.

Control Error Setting

The pseudo control error can be caused in the control bit by setting "1" to CEN.

However, it is necessary to set "1" to either of AHBEN bit at the same time.

Data Error Setting

The pseudo data error can be caused in the corresponding data bit by setting "1" to DEN[3:0].

However, it is necessary to set "1" to either of AHBEN bit at the same time.

Notes:

- Set only the bit corresponding to the access size when you set DEN[3:0].
- When DEN[3:0] is set to the bit that doesn't correspond to the access size, the error of the data not accessed might be detected.
- When you set DEN[3:0] to the bit that doesn't correspond to the access size, it might be different from the method of detecting the data error described in "Data error detection".

Bus Diagnosis Pseudo Error Generation Procedure

The procedure that causes a pseudo error is the following.

1. Set the type of the bus error to be diagnosed in the bus diagnosis test register (BUSTSTRn).
 - In the key code, write the same error setting four continuous times, "00" → "01" → "10" → "11".
2. Access the resource in the diagnosis area with the bus that does the pseudo error setting.
 - When you set the address error and the control error (When you do not set the data error).
→ A pseudo error occurs by accessing the resource in the diagnosis area.
 - When you set the data error
→ A pseudo error occurs by accessing the resource in the diagnosis area by the access size corresponding to DEN[3:0]. (See Notes in "Data error setting".

4.3. Example of Operating Bus Diagnosis

The example of operating the bus diagnosis is shown as follows.

- Data error detection operation

The data bus breaks down when the write (read) is accessed to the resource by byte access[31:24].

→ Only DER[3] of the bus diagnosis status register corresponding to the resource is set to "1".

Notes:

- *Even if the bus is out of order at this time by data bus[23:0], neither DER[2], DER[1] nor DER[0] are set to "1".*
- *Only the bit corresponding to the access size is similarly set as for the word and the half-word access.*

- Pseudo data error setting operation

When you want to make the error detected in bus diagnosis status register DER[0] in the test function

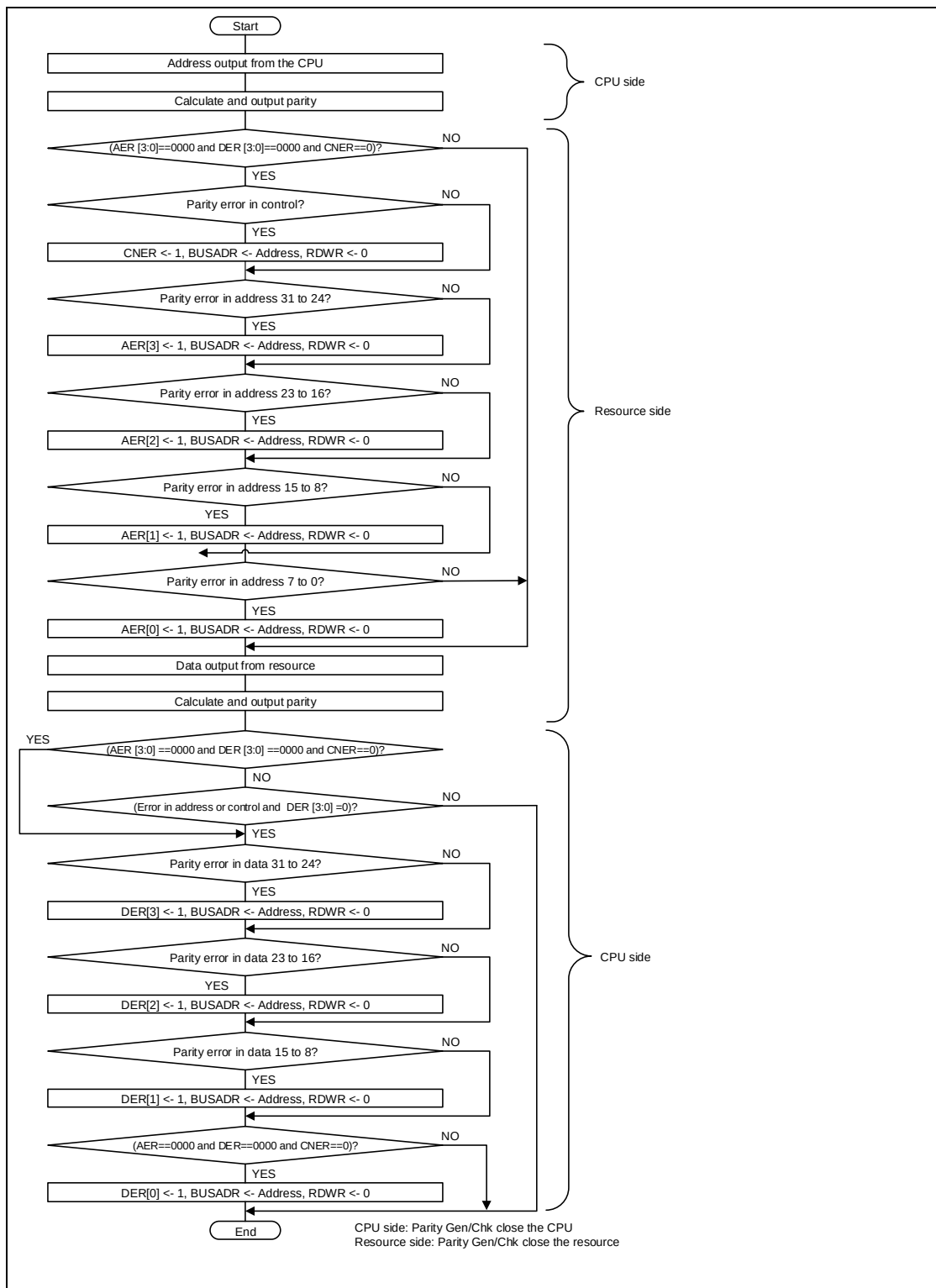
→ Set "1" to bus error setting and data error setting DER[0] by the key code access, and do byte access[7:0].

When DEN[3:1] is set, and byte access [7:0] is done, the error might be detected in bus diagnosis status register DER[3:1].

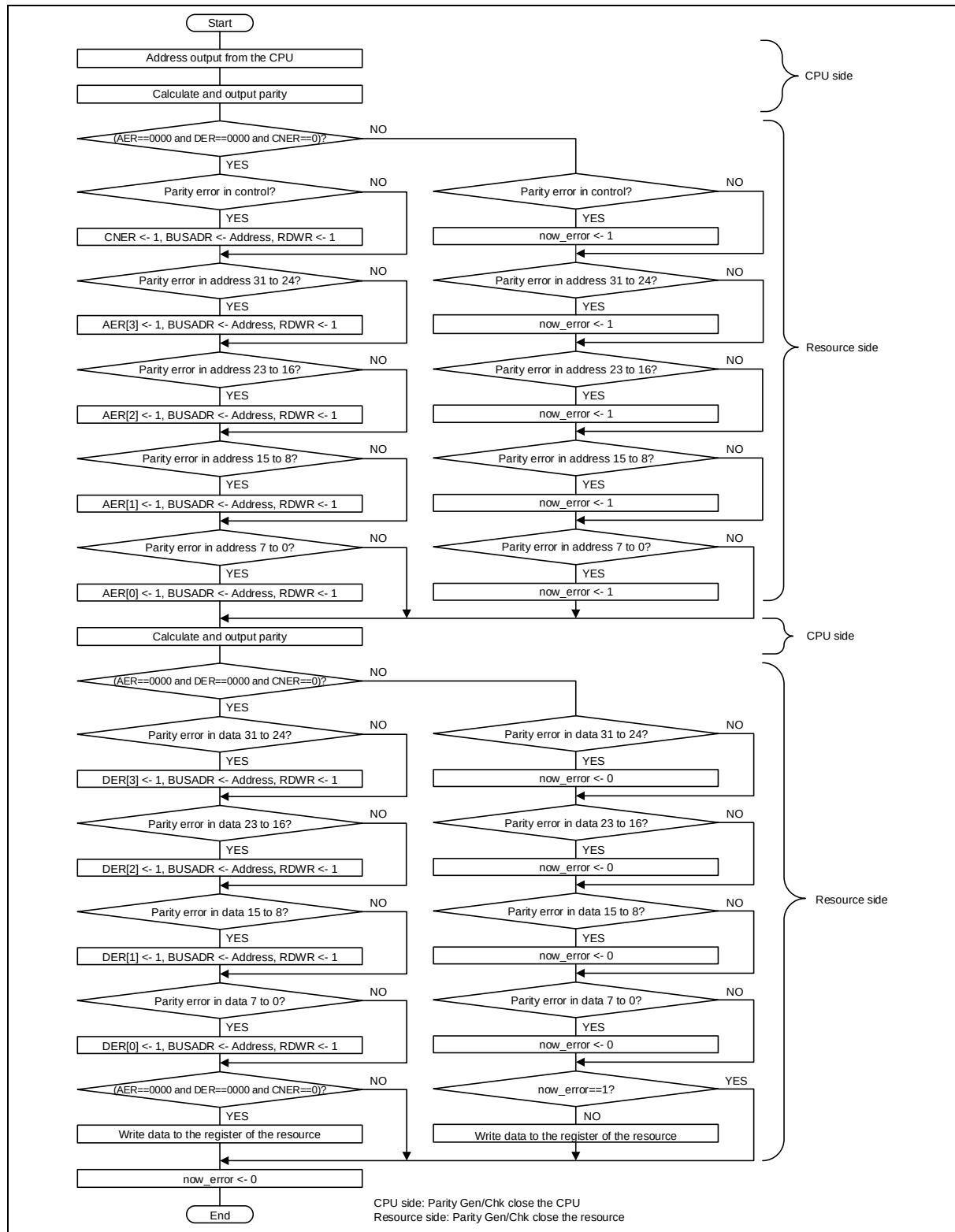
Bus Diagnosis Operation Flow

The operation flow of the bus diagnosis is shown below.

(1) At register reading



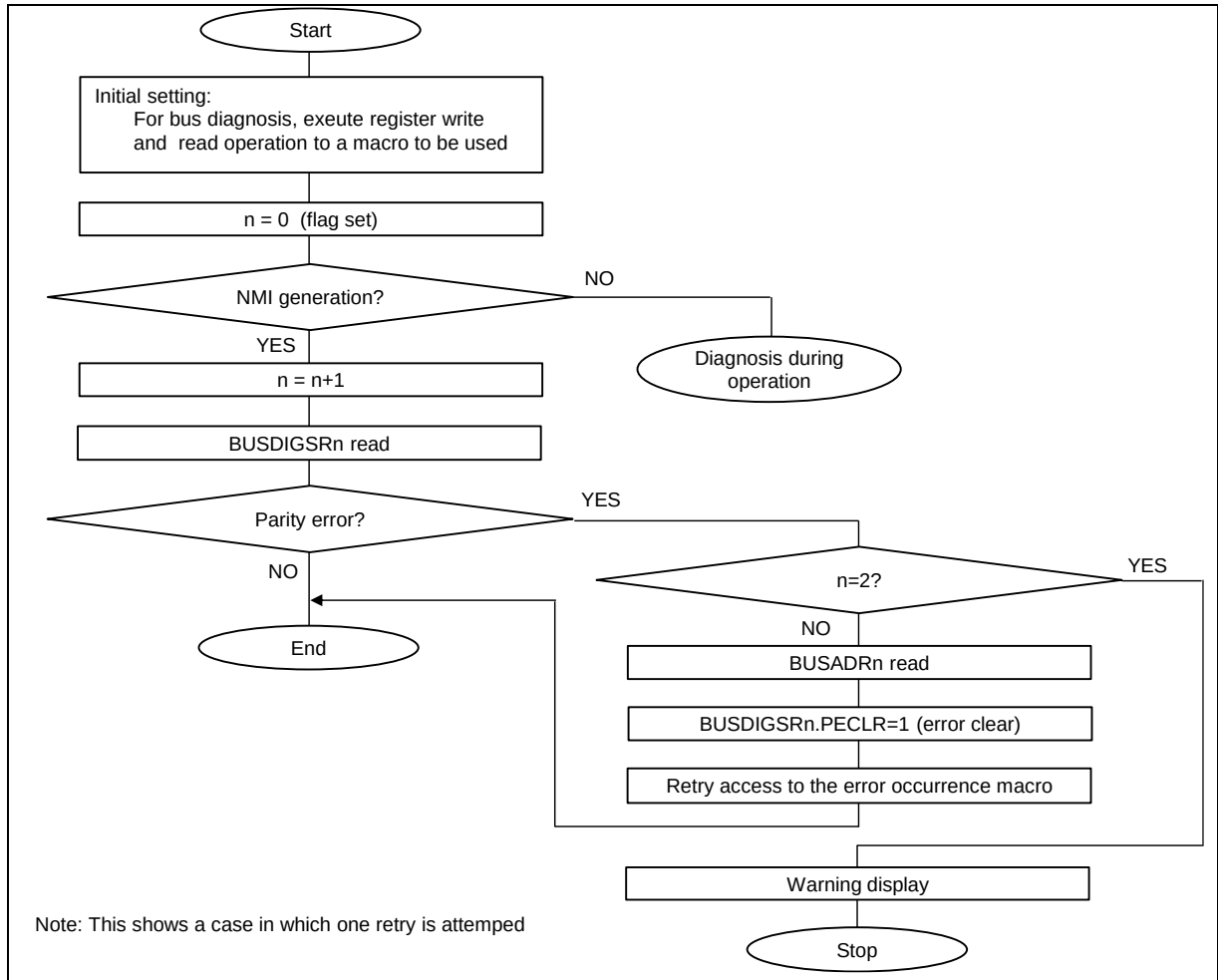
(2) At register writing



(3) Processing at error detection

The following gives an example of processing at error detection.

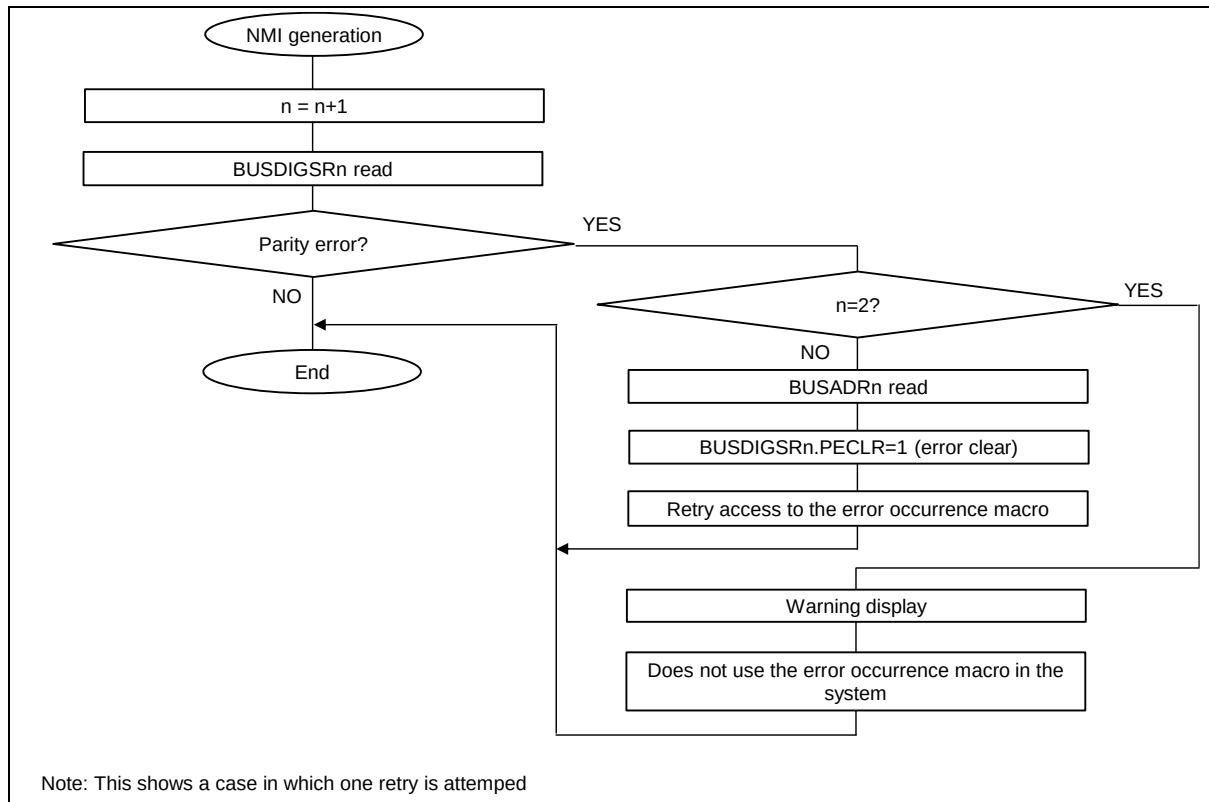
– At Initialization



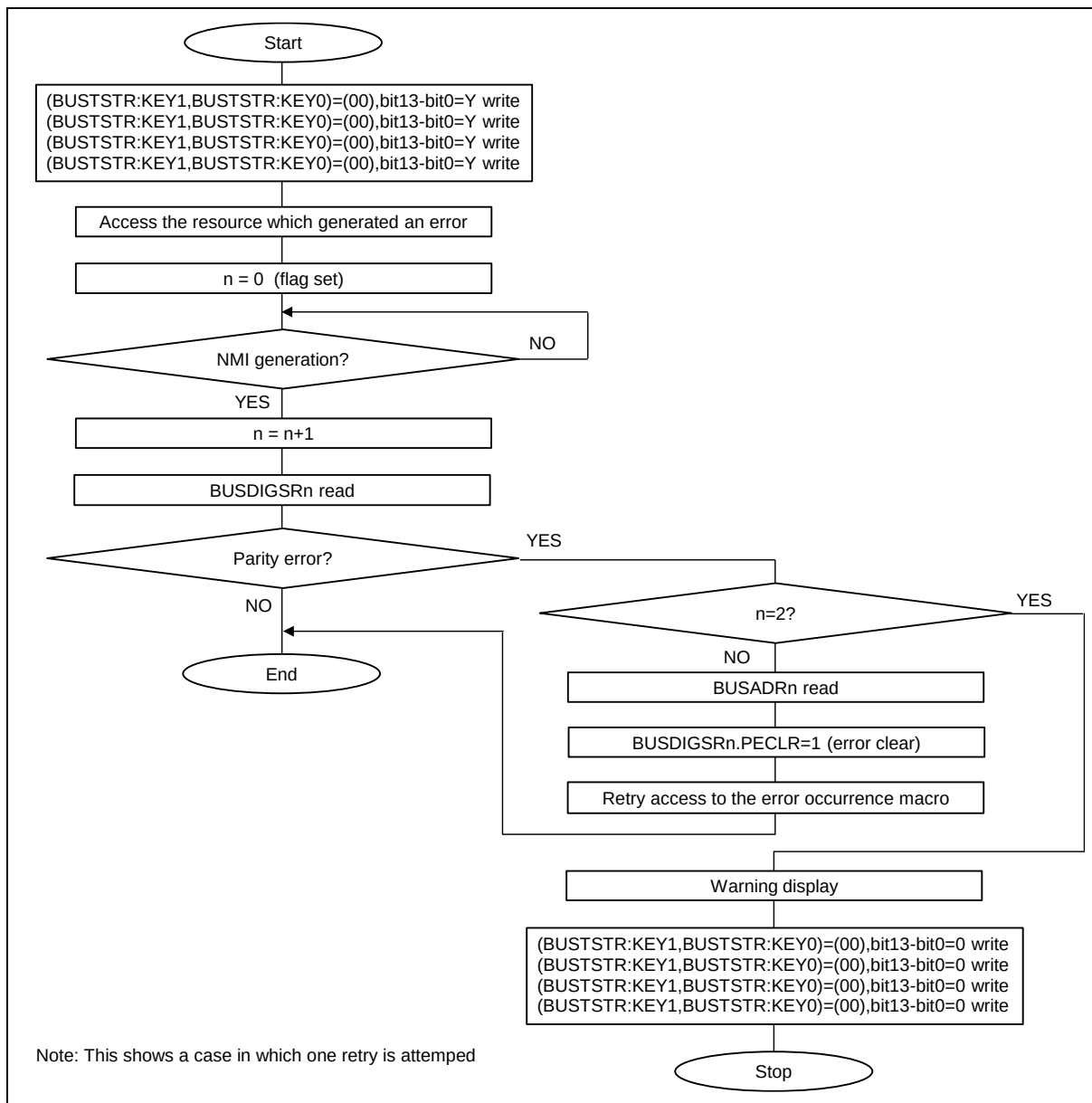
Notes:

- Count the number of retries by a flag.

- During Operation



- In the Test Mode



CHAPTER 28: APPENDIX: Major Changes



Page	Section	Change Results			
Rev.*A					
13	CHAPTER 1: Overview 2.Document Definition	Revised the below:			
		The related documents of S6J3400 are the followings.			
		Table 0-1			
		Error)			
		Document type	Definition	Primary user	Document code
		Datasheet	The function and its characteristics are specified quantitatively.	Investigator and hardware engineer	DS708-00008-Revision
		S6J3400 hardware manual	The function and its operation of S6J3400 series are described.	Software engineer	MN708-00012-Revision
		Traveo™ Platform hardware manual	The function and its operation of CPU core platform are described.	Software engineer	MN708-00010-Revision
		Application note	The reference software, sample application, the reference board design and so on are explained.	Software and hardware engineer	Under consideration
		Correct)			
		Document type	Definition	Primary user	Document code
		Datasheet	The function and its characteristics are specified quantitatively.	Investigator and hardware engineer	001-97829
		S6J3400 hardware manual	The function and its operation of S6J3400 series are described.	Software engineer	002-09919
Traveo™ Platform hardware manual	The function and its operation of CPU core platform are described.	Software engineer	002-07884		
Application note	The reference software, sample application, the reference board design and so on are explained.	Software and hardware engineer	Under consideration		

Page	Section	Change Results																					
22	CHAPTER 2: Function List 2.1.Basic Option	Revised the below: The figure shows the optional function and the part number relations of the series. Figure 0-1 Error) Option <table><tr><td>Digit</td><td>SHE</td></tr><tr><td>S</td><td>ON</td></tr><tr><td>U</td><td>OFF</td></tr></table> Correct) Option <table><tr><td>Digit</td><td>SHE</td><td>MK_CEER*</td></tr><tr><td>S</td><td>ON</td><td>Fixed to Enable</td></tr><tr><td>U</td><td>OFF</td><td>Fixed to Enable</td></tr><tr><td>T</td><td>ON</td><td>Selectable</td></tr><tr><td>V</td><td>OFF</td><td>Selectable</td></tr></table> *:Chip Erase Enable Register	Digit	SHE	S	ON	U	OFF	Digit	SHE	MK_CEER*	S	ON	Fixed to Enable	U	OFF	Fixed to Enable	T	ON	Selectable	V	OFF	Selectable
Digit	SHE																						
S	ON																						
U	OFF																						
Digit	SHE	MK_CEER*																					
S	ON	Fixed to Enable																					
U	OFF	Fixed to Enable																					
T	ON	Selectable																					
V	OFF	Selectable																					
22	CHAPTER 2: Function List 2.1.Basic Option	Revised Memory size as below: Error) Memory size: <table><tr><td rowspan="2">Digit</td><td colspan="2">Flash</td></tr><tr><td>Main</td><td>Work</td></tr></table> Correct) Memory size: <table><tr><td rowspan="2">Digit</td><td colspan="2">Flash</td></tr><tr><td>Program</td><td>Work</td></tr></table>	Digit	Flash		Main	Work	Digit	Flash		Program	Work											
Digit	Flash																						
	Main	Work																					
Digit	Flash																						
	Program	Work																					

Page	Section	Change Results			
25	CHAPTER 2: Function List 2.3. Restriction	Deleted the below::			
		Some functions have restrictions which depend on package pin counts.			
		Table 0-2			
		Error)			
		Function	TEQFP144 LQFP144	TEQFP120 LQFP120	TEQFP100 LQFP100
		Base Timer			TIOB24/26/29/33/35/37/38 _0
		Correct)			
		Function	TEQFP144 LQFP144	TEQFP120 LQFP120	TEQFP100 LQFP100
		Base Timer			TIOB24/29/33/35/37/38_0

Page	Section	Change Results				
31	CHAPTER 3: Product Description 2.Product Description	Added notes as below: Error) <table><tr><td>Embedded Program/Work Flash Memory</td><td> Embedded Program Flash can be accessed with 0wait cycle if CPU frequency is 80MHz or less. 0-wait-cycle: 80MHz or less. 1-wait-cycle: 132MHz or less. The maximum frequency should be referred in datasheet. Erase suspend is supported. Reading and writing to the other sector are possible when Flash Erase is suspended. Serial Flash programing and Parallel Flash programing are supported. Margin mode is not supported. </td></tr></table> Correct) <table><tr><td>Embedded Program/Work Flash Memory</td><td> Embedded Program Flash can be accessed with 0wait cycle if CPU frequency is 80MHz or less. 0-wait-cycle: 80MHz or less. 1-wait-cycle: 132MHz or less. Work Flash can be accessed with 0-wait-cycle if CPU frequency is 12.5MHz or less. 7-wait-cycle: 80MHz or less. 11-wait-cycle: 132MHz or less. The wait-cycle setting see the Traveo™ Platform hardware manual in details. The maximum frequency should be referred in datasheet. Erase suspend is supported. Reading and writing to the other sector are possible when Flash Erase is suspended. Serial Flash programing and Parallel Flash programing are supported. Margin mode is not supported. </td></tr></table>	Embedded Program/Work Flash Memory	Embedded Program Flash can be accessed with 0wait cycle if CPU frequency is 80MHz or less. 0-wait-cycle: 80MHz or less. 1-wait-cycle: 132MHz or less. The maximum frequency should be referred in datasheet. Erase suspend is supported. Reading and writing to the other sector are possible when Flash Erase is suspended. Serial Flash programing and Parallel Flash programing are supported. Margin mode is not supported.	Embedded Program/Work Flash Memory	Embedded Program Flash can be accessed with 0wait cycle if CPU frequency is 80MHz or less. 0-wait-cycle: 80MHz or less. 1-wait-cycle: 132MHz or less. Work Flash can be accessed with 0-wait-cycle if CPU frequency is 12.5MHz or less. 7-wait-cycle: 80MHz or less. 11-wait-cycle: 132MHz or less. The wait-cycle setting see the Traveo™ Platform hardware manual in details. The maximum frequency should be referred in datasheet. Erase suspend is supported. Reading and writing to the other sector are possible when Flash Erase is suspended. Serial Flash programing and Parallel Flash programing are supported. Margin mode is not supported.
Embedded Program/Work Flash Memory	Embedded Program Flash can be accessed with 0wait cycle if CPU frequency is 80MHz or less. 0-wait-cycle: 80MHz or less. 1-wait-cycle: 132MHz or less. The maximum frequency should be referred in datasheet. Erase suspend is supported. Reading and writing to the other sector are possible when Flash Erase is suspended. Serial Flash programing and Parallel Flash programing are supported. Margin mode is not supported.					
Embedded Program/Work Flash Memory	Embedded Program Flash can be accessed with 0wait cycle if CPU frequency is 80MHz or less. 0-wait-cycle: 80MHz or less. 1-wait-cycle: 132MHz or less. Work Flash can be accessed with 0-wait-cycle if CPU frequency is 12.5MHz or less. 7-wait-cycle: 80MHz or less. 11-wait-cycle: 132MHz or less. The wait-cycle setting see the Traveo™ Platform hardware manual in details. The maximum frequency should be referred in datasheet. Erase suspend is supported. Reading and writing to the other sector are possible when Flash Erase is suspended. Serial Flash programing and Parallel Flash programing are supported. Margin mode is not supported.					

Page	Section	Change Results																
36	CHAPTER 3: Product Description 3.4.Restrictio n	Revised the below: Error) <table><tr><td>Main clock division</td><td>SYSC_MOSCCNTR DIV2SEL bit</td><td>Set SYSC_MOSCCNTR.DIV2SEL=1. Main clock pulse that is no division in chip deforms easily by noise. It causes running out of control.</td><td>-</td></tr></table> Correct) <table><tr><td>Main clock division</td><td>SYSC_MOSCCNTR DIV2SEL bit</td><td>Set SYSC_MOSCCNTR.DIV2SEL=1. Main clock pulse that is no division in chip deforms easily by noise. It causes running out of control.</td><td>-</td></tr><tr><td>Main clock fast clock input enable</td><td>SYSC_MOSCCNTR FCIMEN bit</td><td>Set SYSC_MOSCCNTR.FCIMEN=0. Main clock needs setting to 0 to oscillate.</td><td></td></tr></table>	Main clock division	SYSC_MOSCCNTR DIV2SEL bit	Set SYSC_MOSCCNTR.DIV2SEL=1. Main clock pulse that is no division in chip deforms easily by noise. It causes running out of control.	-	Main clock division	SYSC_MOSCCNTR DIV2SEL bit	Set SYSC_MOSCCNTR.DIV2SEL=1. Main clock pulse that is no division in chip deforms easily by noise. It causes running out of control.	-	Main clock fast clock input enable	SYSC_MOSCCNTR FCIMEN bit	Set SYSC_MOSCCNTR.FCIMEN=0. Main clock needs setting to 0 to oscillate.					
Main clock division	SYSC_MOSCCNTR DIV2SEL bit	Set SYSC_MOSCCNTR.DIV2SEL=1. Main clock pulse that is no division in chip deforms easily by noise. It causes running out of control.	-															
Main clock division	SYSC_MOSCCNTR DIV2SEL bit	Set SYSC_MOSCCNTR.DIV2SEL=1. Main clock pulse that is no division in chip deforms easily by noise. It causes running out of control.	-															
Main clock fast clock input enable	SYSC_MOSCCNTR FCIMEN bit	Set SYSC_MOSCCNTR.FCIMEN=0. Main clock needs setting to 0 to oscillate.																
43	CHAPTER5: Clock Configuration 2.Operation	Revised the below: The source clock of each function should be selected as following table. Table 0-3 Error) <table><tr><td rowspan="2">Software watchdog timer</td><td rowspan="2">CLK_SWWDTC</td><td>Internal CR oscillator (High frequency)</td><td>See Traveo™ Platform hardware manual</td></tr><tr><td>Internal CR oscillator (Low frequency)</td><td>See Traveo™ Platform hardware manual</td></tr></table> Correct) <table><tr><td rowspan="4">Software watchdog timer</td><td rowspan="4">CLK_SWWDTC</td><td>Main clock</td><td>See Traveo™ Platform hardware manual</td></tr><tr><td>Sub clock</td><td>See Traveo™ Platform hardware manual</td></tr><tr><td>Internal CR oscillator (High frequency)</td><td>See Traveo™ Platform hardware manual</td></tr><tr><td>Internal CR oscillator (Low frequency)</td><td>See Traveo™ Platform hardware manual</td></tr></table>	Software watchdog timer	CLK_SWWDTC	Internal CR oscillator (High frequency)	See Traveo™ Platform hardware manual	Internal CR oscillator (Low frequency)	See Traveo™ Platform hardware manual	Software watchdog timer	CLK_SWWDTC	Main clock	See Traveo™ Platform hardware manual	Sub clock	See Traveo™ Platform hardware manual	Internal CR oscillator (High frequency)	See Traveo™ Platform hardware manual	Internal CR oscillator (Low frequency)	See Traveo™ Platform hardware manual
Software watchdog timer	CLK_SWWDTC	Internal CR oscillator (High frequency)			See Traveo™ Platform hardware manual													
		Internal CR oscillator (Low frequency)	See Traveo™ Platform hardware manual															
Software watchdog timer	CLK_SWWDTC	Main clock	See Traveo™ Platform hardware manual															
		Sub clock	See Traveo™ Platform hardware manual															
		Internal CR oscillator (High frequency)	See Traveo™ Platform hardware manual															
		Internal CR oscillator (Low frequency)	See Traveo™ Platform hardware manual															
44	CHAPTER5: Clock Configuration 3.remark	Revised the below: See the chapter of clock system before referring this chapter. Note Error) The table shows the divided each clock on n = 1, 2, 3 for CLK_CPU = 132MHz, 80MHz, 40MHz. Correct) The table shows the possible setting for CLK_CPU = 132MHz, 80MHz, 40MHz.																

Page	Section	Change Results																																				
44	CHAPTER5: Clock Configuration 2.remark	Deleted the below: See the chapter of clock system before referring this chapter. Table 2-2 Error) <table><tr><th rowspan="2">CLOCK</th><th colspan="3">CLK_CPU : CLOCK</th></tr><tr><th>≤132MHz</th><th>≤80MHz</th><th>≤40MHz</th></tr><tr><td>CLK_FCLK CLK_LCP</td><td rowspan="2">1:2n</td><td>1:n</td><td rowspan="3">1:n</td></tr><tr><td>CLK_ATB CLK_DBG</td><td rowspan="2"></td></tr><tr><td>CLK_HPM/DMA/MEMC/SHE CLK_SYS1 CLK_LCP0 CLK_LCP0A CLK_LCP1 CLK_LCP1A CLK_SYSC0H/COMH</td><td>1:4n</td><td>1:2n</td></tr><tr><td>CLK_TRC</td><td>1:1</td><td>1:1</td><td>1:1</td></tr></table> n : Same divide number Correct) <table><tr><th rowspan="2">CLOCK</th><th colspan="3">CLK_CPU : CLOCK</th></tr><tr><th>≤132MHz</th><th>≤80MHz</th><th>≤40MHz</th></tr><tr><td>CLK_FCLK CLK_LCP</td><td rowspan="2">1:2n</td><td>1:n</td><td rowspan="3">1:n</td></tr><tr><td>CLK_ATB CLK_DBG</td><td rowspan="2"></td></tr><tr><td>CLK_HPM/DMA/MEMC/SHE CLK_SYS1 CLK_LCP0 CLK_LCP0A CLK_LCP1 CLK_LCP1A CLK_SYSC0H/COMH</td><td>1:4n</td><td>1:2n</td></tr></table> n : Same divide number	CLOCK	CLK_CPU : CLOCK			≤132MHz	≤80MHz	≤40MHz	CLK_FCLK CLK_LCP	1:2n	1:n	1:n	CLK_ATB CLK_DBG		CLK_HPM/DMA/MEMC/SHE CLK_SYS1 CLK_LCP0 CLK_LCP0A CLK_LCP1 CLK_LCP1A CLK_SYSC0H/COMH	1:4n	1:2n	CLK_TRC	1:1	1:1	1:1	CLOCK	CLK_CPU : CLOCK			≤132MHz	≤80MHz	≤40MHz	CLK_FCLK CLK_LCP	1:2n	1:n	1:n	CLK_ATB CLK_DBG		CLK_HPM/DMA/MEMC/SHE CLK_SYS1 CLK_LCP0 CLK_LCP0A CLK_LCP1 CLK_LCP1A CLK_SYSC0H/COMH	1:4n	1:2n
CLOCK	CLK_CPU : CLOCK																																					
	≤132MHz	≤80MHz	≤40MHz																																			
CLK_FCLK CLK_LCP	1:2n	1:n	1:n																																			
CLK_ATB CLK_DBG																																						
CLK_HPM/DMA/MEMC/SHE CLK_SYS1 CLK_LCP0 CLK_LCP0A CLK_LCP1 CLK_LCP1A CLK_SYSC0H/COMH	1:4n			1:2n																																		
CLK_TRC	1:1	1:1	1:1																																			
CLOCK	CLK_CPU : CLOCK																																					
	≤132MHz	≤80MHz	≤40MHz																																			
CLK_FCLK CLK_LCP	1:2n	1:n	1:n																																			
CLK_ATB CLK_DBG																																						
CLK_HPM/DMA/MEMC/SHE CLK_SYS1 CLK_LCP0 CLK_LCP0A CLK_LCP1 CLK_LCP1A CLK_SYSC0H/COMH	1:4n			1:2n																																		

Page	Section	Change Results																																																																																																																																																																																																																																																				
45	CHAPTER5: Clock Configuration 2.remark	Deleted the below: CLK_TRC and n=3 Added notes as below: n=4 See the chapter of clock system before referring this chapter. Table 2-3 Error) <table><thead><tr><th></th><th colspan="3">CLK_CPU = 132MHz</th><th colspan="3">CLK_CPU = 80MHz</th><th colspan="3">CLK_CPU = 40MHz</th></tr><tr><th></th><th>n=1</th><th>n=2</th><th>n=3</th><th>n=1</th><th>n=2</th><th>n=3</th><th>n=1</th><th>n=2</th><th>n=3</th></tr></thead><tbody><tr><td>CLK_TRC</td><td>132MHz</td><td>132MHz</td><td>132MHz</td><td>80MHz</td><td>80MHz</td><td>80MHz</td><td>40MHz</td><td>40MHz</td><td>40MHz</td></tr><tr><td>CLK_FCLK</td><td>66MHz</td><td>33MHz</td><td>22MHz</td><td>80MHz</td><td>40MHz</td><td>26.6MHz</td><td>40MHz</td><td>20MHz</td><td>13.3MHz</td></tr><tr><td>CLK_LCP</td><td>66MHz</td><td>33MHz</td><td>22MHz</td><td>80MHz</td><td>40MHz</td><td>26.6MHz</td><td>40MHz</td><td>20MHz</td><td>13.3MHz</td></tr><tr><td>CLK_ATB</td><td>66MHz</td><td>33MHz</td><td>22MHz</td><td>40MHz</td><td>20MHz</td><td>13.3MHz</td><td>40MHz</td><td>20MHz</td><td>13.3MHz</td></tr><tr><td>CLK_DBG</td><td>66MHz</td><td>33MHz</td><td>22MHz</td><td>40MHz</td><td>20MHz</td><td>13.3MHz</td><td>40MHz</td><td>20MHz</td><td>13.3MHz</td></tr><tr><td>CLK_HPM/DMA/MEMC/SHE</td><td>33MHz</td><td>16.5MHz</td><td>11MHz</td><td>40MHz</td><td>20MHz</td><td>13.3MHz</td><td>40MHz</td><td>20MHz</td><td>13.3MHz</td></tr><tr><td>CLK_SYS1</td><td>33MHz</td><td>16.5MHz</td><td>11MHz</td><td>40MHz</td><td>20MHz</td><td>13.3MHz</td><td>40MHz</td><td>20MHz</td><td>13.3MHz</td></tr><tr><td>CLK_LCP0</td><td>33MHz</td><td>16.5MHz</td><td>11MHz</td><td>40MHz</td><td>20MHz</td><td>13.3MHz</td><td>40MHz</td><td>20MHz</td><td>13.3MHz</td></tr><tr><td>CLK_LCP0A</td><td>33MHz</td><td>16.5MHz</td><td>11MHz</td><td>40MHz</td><td>20MHz</td><td>13.3MHz</td><td>40MHz</td><td>20MHz</td><td>13.3MHz</td></tr><tr><td>CLK_LCP1</td><td>33MHz</td><td>16.5MHz</td><td>11MHz</td><td>40MHz</td><td>20MHz</td><td>13.3MHz</td><td>40MHz</td><td>20MHz</td><td>13.3MHz</td></tr><tr><td>CLK_LCP1A</td><td>33MHz</td><td>16.5MHz</td><td>11MHz</td><td>40MHz</td><td>20MHz</td><td>13.3MHz</td><td>40MHz</td><td>20MHz</td><td>13.3MHz</td></tr><tr><td>CLK_SYSC0H/COMH</td><td>33MHz</td><td>16.5MHz</td><td>11MHz</td><td>40MHz</td><td>20MHz</td><td>13.3MHz</td><td>40MHz</td><td>20MHz</td><td>13.3MHz</td></tr></tbody></table> Correct) <table><thead><tr><th></th><th colspan="2">CLK_CPU = 132MHz</th><th colspan="2">CLK_CPU= 80MHz</th><th colspan="3">CLK_CPU = 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Page	Section	Change Results						
55	CHAPTER7: Memory and Base Address Map 3.Base address map	Revised PPU_No as below: Error)						
		START Address	END Address	Group	Function	PPU_No		
		B060_0000	B060_007F	MCU Config Group	Protection register area	-		
		B060_0080	B060_00FF	MCU Config Group	RUN profile register area	-		
		B060_0100	B060_017F	MCU Config Group	PSS profile register area	-		
		B060_0180	B060_01FF	MCU Config Group	APP profile register area	-		
		B060_0200	B060_027F	MCU Config Group	STS profile register area	-		
		B060_0280	B060_02FF	MCU Config Group	System register area	-		
		B060_0300	B060_037F	MCU Config Group	CSV	-		
		B060_0380	B060_03FF	MCU Config Group	RESET	-		
		Correct)						
		START Address	END Address	Group	Function	PPU_No		
		B060_0000	B060_007F	MCU Config Group	Protection register area	51		
		B060_0080	B060_00FF	MCU Config Group	RUN profile register area	51		
		B060_0100	B060_017F	MCU Config Group	PSS profile register area	51		
		B060_0180	B060_01FF	MCU Config Group	APP profile register area	51		
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		B060_0300	B060_037F	MCU Config Group	CSV	51		
		B060_0380	B060_03FF	MCU Config Group	RESET	51		
56	CHAPTER7: Memory and Base Address Map 3.Base address map	Revised PPU_No as below: Error)						
		START Address	END Address	Group	Function	PPU_No		
		B060_0600	B060_067F	MCU Config Group	Clock System	-		
		B060_0680	B060_06FF	MCU Config Group	Special register area	-		
		B060_0700	B060_07FF	MCU Config Group	Debug register area	-		
		Correct)						
		START Address	END Address	Group	Function	PPU_No		
		B060_0600	B060_067F	MCU Config Group	Clock System	51		
		B060_0680	B060_06FF	MCU Config Group	Special register area	51		
		B060_0700	B060_07FF	MCU Config Group	Debug register area	51		
		57	CHAPTER7: Memory and Base Address Map 3.Base address map	Revised PPU_No. as below: Error)				
				START Address	END Address	Group	Function	PPU_No
				B475_0000	B475_7FFF	CPU Config Group	PPU	-
				Correct)				
START Address	END Address			Group	Function	PPU_No		
B475_0000	B475_7FFF	CPU Config Group	PPU	77				

Page	Section	Change Results			
64	CHAPTER8: IRQ Map/ NMI Map 1.IRQ MAP	Revised PPU_No. as below:			
		This section shows list of interrupt vector.			
		This list shows the assignments of interrupt vectors / interrupt control registers.			
		Error)			
		IQR No.	Detail	IRQ Priority Register	Vector Address Register
		8	TCFLASH Single Bit Error	IRC0_IRQPL2 : IRQPL8	IRC0_IRQVA8
		10	Work FLASH Single Bit Error	IRC0_IRQPL2 : IRQPL10	IRC0_IRQVA10
		20	Work FLASH RDY Interrupt Request / Work FLASH Write Completion	IRC0_IRQPL5 : IRQPL20	IRC0_IRQVA20
		Correct)			
		IQR No.	Detail	IRQ Priority Register	Vector Address Register
		8	TCFLASH RDY, Hang up, Single Bit Error	IRC0_IRQPL2 : IRQPL8	IRC0_IRQVA8
		10	Work FLASH Hang up	IRC0_IRQPL2 : IRQPL10	IRC0_IRQVA10
		20	Work FLASH RDY, Write Enable Release, Single Bit Error	IRC0_IRQPL5 : IRQPL20	IRC0_IRQVA20

Page	Section	Change Results																																																																																																																																																																												
73	CHAPTER9: DMA Channel Activation Factors 1.Factors list	Revised the below: Error) <table><tr><th rowspan="2">Number of channels</th><th colspan="6">Peripheral functions</th><th rowspan="2">Remarks</th></tr><tr><th>Combination. 0</th><th>Combination. 1</th><th>Combination. 2</th><th>Combination. 3</th><th>Combination. 4</th><th>Combination. 5</th></tr><tr><td>45</td><td>MFS ch.13 TX</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td></td></tr><tr><td>46 to 49</td><td colspan="6">Reserved</td><td></td></tr><tr><td>50</td><td>CAN_FD ch.0</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td></td></tr><tr><td>51</td><td>CAN_FD ch.1</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td></td></tr><tr><td>52</td><td>CAN_FD ch.2</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td></td></tr><tr><td>53</td><td>CAN_FD ch.3</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td></td></tr><tr><td>54</td><td>CAN_FD ch.4</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td></td></tr><tr><td>55</td><td>CAN_FD ch.8</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td></td></tr><tr><td>56</td><td>Base Timer ch.0-0</td><td>Base Timer ch.0-1</td><td>Base Timer ch.24-0</td><td>Base Timer ch.24-1</td><td>Base Timer ch.48-0</td><td>Base Timer ch.48-1</td><td>*1</td></tr></table> Correct) <table><tr><th rowspan="2">Number of channels</th><th colspan="6">Peripheral functions</th><th rowspan="2">Remarks</th></tr><tr><th>Combination. 0</th><th>Combination. 1</th><th>Combination. 2</th><th>Combination. 3</th><th>Combination. 4</th><th>Combination. 5</th></tr><tr><td>45</td><td>MFS ch.13 TX</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td></td></tr><tr><td>46 to 49</td><td colspan="6">Reserved</td><td></td></tr><tr><td>50</td><td></td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td></td></tr><tr><td>51</td><td></td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td></td></tr><tr><td>52</td><td></td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td></td></tr><tr><td>53</td><td></td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td></td></tr><tr><td>54</td><td></td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td></td></tr><tr><td>55</td><td></td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td></td></tr><tr><td>56</td><td>Base Timer ch.0-0</td><td>Base Timer ch.0-1</td><td>Base Timer ch.24-0</td><td>Base Timer ch.24-1</td><td>Base Timer ch.48-0</td><td>Base Timer ch.48-1</td><td>*1</td></tr></table>	Number of channels	Peripheral functions						Remarks	Combination. 0	Combination. 1	Combination. 2	Combination. 3	Combination. 4	Combination. 5	45	MFS ch.13 TX	-	-	-	-	-		46 to 49	Reserved							50	CAN_FD ch.0	-	-	-	-	-		51	CAN_FD ch.1	-	-	-	-	-		52	CAN_FD ch.2	-	-	-	-	-		53	CAN_FD ch.3	-	-	-	-	-		54	CAN_FD ch.4	-	-	-	-	-		55	CAN_FD ch.8	-	-	-	-	-		56	Base Timer ch.0-0	Base Timer ch.0-1	Base Timer ch.24-0	Base Timer ch.24-1	Base Timer ch.48-0	Base Timer ch.48-1	*1	Number of channels	Peripheral functions						Remarks	Combination. 0	Combination. 1	Combination. 2	Combination. 3	Combination. 4	Combination. 5	45	MFS ch.13 TX	-	-	-	-	-		46 to 49	Reserved							50		-	-	-	-	-		51		-	-	-	-	-		52		-	-	-	-	-		53		-	-	-	-	-		54		-	-	-	-	-		55		-	-	-	-	-		56	Base Timer ch.0-0	Base Timer ch.0-1	Base Timer ch.24-0	Base Timer ch.24-1	Base Timer ch.48-0	Base Timer ch.48-1	*1
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55		-	-	-	-	-																																																																																																																																																																								
56	Base Timer ch.0-0	Base Timer ch.0-1	Base Timer ch.24-0	Base Timer ch.24-1	Base Timer ch.48-0	Base Timer ch.48-1	*1																																																																																																																																																																							

Page	Section	Change Results										
116	CHAPTER11: Port Configuration 3.1.Resource input configuration	Revised the below:										
		Error)										
		Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL[3:0]	Source for Resource input							
					0	1	2	3	4	5	6	7
					8	9	10	11	12	13	14	15
		RIC_RE SIN210 (0x01A4)	RX0	RESSEL (0-7)	PORT_PIN	CAN0_RX &_TX	-	-	-	-	-	-
				RESSEL (8-15)	-	-	-	-	-	-	-	-
				PORTSEL (0-7)	P307	P229	P225	-	-	-	-	-
				PORTSEL (8-15)	-	-	-	-	-	-	-	-
		Correct)										
		Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL[3:0]	Source for Resource input							
					0	1	2	3	4	5	6	7
					8	9	10	11	12	13	14	15
		RIC_RE SIN210 (0x01A4)	RX0	RESSEL (0-7)	PORT_PIN	CAN0_RX _AND_TX	-	-	-	-	-	-
				RESSEL (8-15)	-	-	-	-	-	-	-	-
				PORTSEL (0-7)	P307	P229	P225	-	-	-	-	-
				PORTSEL (8-15)	-	-	-	-	-	-	-	-

Page	Section	Change Results											
116	CHAPTER11: Port Configuration 3.1.Resource input configuration	Revised the below:											
		Error)											
		Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL L[3:0]	Source for Resource input								
					0	1	2	3	4	5	6	7	
					8	9	10	11	12	13	14	15	
		RIC_RE SIN211 (0x01A6)	RX1	RESSEL (0-7)	PORT_P N	CAN1_RX _&_TX	-	-	-	-	-	-	
				RESSEL (8-15)	-	-	-	-	-	-	-	-	-
				PORTSEL (0-7)	P402	P318	P107	-	-	-	-	-	-
				PORTSEL (8-15)	-	-	-	-	-	-	-	-	-
		Correct)											
		Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL L[3:0]	Source for Resource input								
					0	1	2	3	4	5	6	7	
					8	9	10	11	12	13	14	15	
		RIC_RE SIN211 (0x01A6)	RX1	RESSEL (0-7)	PORT_P N	CAN1_RX _AND_TX	-	-	-	-	-	-	
				RESSEL (8-15)	-	-	-	-	-	-	-	-	-
				PORTSEL (0-7)	P402	P318	P107	-	-	-	-	-	-
				PORTSEL (8-15)	-	-	-	-	-	-	-	-	-

Page	Section	Change Results										
116	CHAPTER11: Port Configuration 3.1.Resource input configuration	Revised the below:										
		Error)										
		Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL[3:0]	Source for Resource input							
					0	1	2	3	4	5	6	7
					8	9	10	11	12	13	14	15
		RIC_RESIN212 (0x01A8)	RX2	RESSEL (0-7)	PORT_PIN	CAN2_RX &_TX	-	-	-	-	-	-
				RESSEL (8-15)	-	-	-	-	-	-	-	-
				PORTSEL (0-7)	P222	P405	-	-	-	-	-	-
				PORTSEL (8-15)	-	-	-	-	-	-	-	-
		Correct)										
		Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL[3:0]	Source for Resource input							
					0	1	2	3	4	5	6	7
					8	9	10	11	12	13	14	15
		RIC_RESIN212 (0x01A8)	RX2	RESSEL (0-7)	PORT_PIN	CAN2_RX _AND_TX	-	-	-	-	-	-
				RESSEL (8-15)	-	-	-	-	-	-	-	-
				PORTSEL (0-7)	P222	P405	-	-	-	-	-	-
				PORTSEL (8-15)	-	-	-	-	-	-	-	-

Page	Section	Change Results										
116	CHAPTER11: Port Configuration 3.1.Resource input configuration	Revised the below:										
		Error)										
		Register (Offset)	Resource	RESSEL[3 :0] /PORTSE L[3:0]	Source for Resource input							
					0	1	2	3	4	5	6	7
					8	9	10	11	12	13	14	15
		RIC_RE SIN213 (0x01AA)	RX3	RESSEL (0-7)	PORT_PI N	CAN3_RX _&_TX	-	-	-	-	-	-
				RESSEL (8-15)	-	-	-	-	-	-	-	-
				PORTSEL (0-7)	-	-	-	-	-	-	-	-
				PORTSEL (8-15)	-	-	-	-	-	-	-	-
		Correct)										
		Register (Offset)	Resource	RESSEL[3 :0] /PORTSE L[3:0]	Source for Resource input							
					0	1	2	3	4	5	6	7
					8	9	10	11	12	13	14	15
		RIC_RE SIN213 (0x01AA)	RX3	RESSEL (0-7)	PORT_PI N	CAN3_RX _AND_TX	-	-	-	-	-	-
				RESSEL (8-15)	-	-	-	-	-	-	-	-
				PORTSEL (0-7)	-	-	-	-	-	-	-	-
				PORTSEL (8-15)	-	-	-	-	-	-	-	-

Page	Section	Change Results										
116	CHAPTER11: Port Configuration 3.1.Resource input configuration	Revised the below:										
		Error)										
		Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL[3:0]	Source for Resource input							
					0	1	2	3	4	5	6	7
					8	9	10	11	12	13	14	15
		RIC_RE SIN214 (0x01AC)	RX4	RESSEL (0-7)	PORT_PIN	CAN4_RX & TX	-	-	-	-	-	-
				RESSEL (8-15)	-	-	-	-	-	-	-	-
				PORTSEL (0-7)	-	-	-	-	-	-	-	-
				PORTSEL (8-15)	-	-	-	-	-	-	-	-
		Correct)										
		Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL[3:0]	Source for Resource input							
					0	1	2	3	4	5	6	7
					8	9	10	11	12	13	14	15
		RIC_RE SIN214 (0x01AC)	RX4	RESSEL (0-7)	PORT_PIN	CAN4_RX AND TX	-	-	-	-	-	-
				RESSEL (8-15)	-	-	-	-	-	-	-	-
				PORTSEL (0-7)	-	-	-	-	-	-	-	-
				PORTSEL (8-15)	-	-	-	-	-	-	-	-

Page	Section	Change Results										
117	CHAPTER11: Port Configuration 3.1.Resource input configuration	Revised the below:										
		Error)										
		Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL L[3:0]	Source for Resource input							
					0	1	2	3	4	5	6	7
		8	9	10	11	12	13	14	15			
		RIC_RE SIN218 (0x01B4)	RX8	RESSEL (0-7)	PORT_P N	CAN8_RX _&_TX	-	-	-	-	-	-
				RESSEL (8-15)	-	-	-	-	-	-	-	-
				PORTSEL (0-7)	-	-	-	-	-	-	-	-
				PORTSEL (8-15)	-	-	-	-	-	-	-	-
		Correct)										
Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL L[3:0]	Source for Resource input									
			0	1	2	3	4	5	6	7		
8	9	10	11	12	13	14	15					
RIC_RE SIN218 (0x01B4)	RX8	RESSEL (0-7)	PORT_P N	CAN8_RX _AND_TX	-	-	-	-	-	-		
		RESSEL (8-15)	-	-	-	-	-	-	-	-		
		PORTSEL (0-7)	-	-	-	-	-	-	-	-		
		PORTSEL (8-15)	-	-	-	-	-	-	-	-		

Page	Section	Change Results																																																																																																																																																																																																														
126	CHAPTER11: Port Configuration 3.1.Resource input configuration	Revised the below: Error) <table><tr><th rowspan="3">Register (Offset)</th><th rowspan="3">Resource</th><th rowspan="3">RESSEL[3 :0] /PORTSEL L[3:0]</th><th colspan="8">Source for Resource input</th></tr><tr><th>0</th><th>1</th><th>2</th><th>3</th><th>4</th><th>5</th><th>6</th><th>7</th></tr><tr><th>8</th><th>9</th><th>10</th><th>11</th><th>12</th><th>13</th><th>14</th><th>15</th></tr><tr><td rowspan="4">RIC_RESI N300 (0x0258)</td><td rowspan="4">OCU0_MOD</td><td>RESSEL (0-7)</td><td>1'b1</td><td>1'b0</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td></tr><tr><td>RESSEL (8-15)</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td></tr><tr><td>PORTSEL (0-7)</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td></tr><tr><td>PORTSEL (8-15)</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td></tr><tr><td rowspan="4">RIC_RESI N301 (0x025A)</td><td rowspan="4">OCU1_MOD</td><td>RESSEL (0-7)</td><td>1'b1</td><td>1'b0</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td></tr><tr><td>RESSEL (8-15)</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td></tr><tr><td>PORTSEL (0-7)</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td></tr><tr><td>PORTSEL (8-15)</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td></tr></table> Correct) <table><tr><th rowspan="3">Register (Offset)</th><th rowspan="3">Resource</th><th rowspan="3">RESSEL[3 :0] /PORTSEL L[3:0]</th><th colspan="8">Source for Resource input</th></tr><tr><th>0</th><th>1</th><th>2</th><th>3</th><th>4</th><th>5</th><th>6</th><th>7</th></tr><tr><th>8</th><th>9</th><th>10</th><th>11</th><th>12</th><th>13</th><th>14</th><th>15</th></tr><tr><td rowspan="4">RIC_RESI N300 (0x0258)</td><td rowspan="4">OCU0_MOD</td><td>RESSEL (0-7)</td><td>set1</td><td>set0</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td></tr><tr><td>RESSEL (8-15)</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td></tr><tr><td>PORTSEL (0-7)</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td></tr><tr><td>PORTSEL (8-15)</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td></tr><tr><td rowspan="4">RIC_RESI N301 (0x025A)</td><td rowspan="4">OCU1_MOD</td><td>RESSEL (0-7)</td><td>set1</td><td>set0</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td></tr><tr><td>RESSEL (8-15)</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td></tr><tr><td>PORTSEL (0-7)</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td></tr><tr><td>PORTSEL (8-15)</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td></tr></table>	Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL L[3:0]	Source for Resource input								0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	RIC_RESI N300 (0x0258)	OCU0_MOD	RESSEL (0-7)	1'b1	1'b0	-	-	-	-	-	-	RESSEL (8-15)	-	-	-	-	-	-	-	-	PORTSEL (0-7)	-	-	-	-	-	-	-	-	PORTSEL (8-15)	-	-	-	-	-	-	-	-	RIC_RESI N301 (0x025A)	OCU1_MOD	RESSEL (0-7)	1'b1	1'b0	-	-	-	-	-	-	RESSEL (8-15)	-	-	-	-	-	-	-	-	PORTSEL (0-7)	-	-	-	-	-	-	-	-	PORTSEL (8-15)	-	-	-	-	-	-	-	-	Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL L[3:0]	Source for Resource input								0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	RIC_RESI N300 (0x0258)	OCU0_MOD	RESSEL (0-7)	set1	set0	-	-	-	-	-	-	RESSEL (8-15)	-	-	-	-	-	-	-	-	PORTSEL (0-7)	-	-	-	-	-	-	-	-	PORTSEL (8-15)	-	-	-	-	-	-	-	-	RIC_RESI N301 (0x025A)	OCU1_MOD	RESSEL (0-7)	set1	set0	-	-	-	-	-	-	RESSEL (8-15)	-	-	-	-	-	-	-	-	PORTSEL (0-7)	-	-	-	-	-	-	-	-	PORTSEL (8-15)	-	-	-	-	-	-	-	-
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131	CHAPTER 11: Port Configuration 3.1.Resource input configuration	Revised the below: Error) <table><tr><th rowspan="3">Register (Offset)</th><th rowspan="3">Resource</th><th rowspan="3">RESSEL[3 :0] /PORTSEL L[3:0]</th><th colspan="8">Source for Resource input</th></tr><tr><th>0</th><th>1</th><th>2</th><th>3</th><th>4</th><th>5</th><th>6</th><th>7</th></tr><tr><th>8</th><th>9</th><th>10</th><th>11</th><th>12</th><th>13</th><th>14</th><th>15</th></tr><tr><td rowspan="4">RIC_RESI N330 (0x0294)</td><td rowspan="4">OCU20_MOD</td><td>RESSEL (0-7)</td><td>1'b1</td><td>1'b0</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td></tr><tr><td>RESSEL (8-15)</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td></tr><tr><td>PORTSEL (0-7)</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td></tr><tr><td>PORTSEL (8-15)</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td></tr><tr><td rowspan="4">RIC_RESI N331 (0x0296)</td><td rowspan="4">OCU21_MOD</td><td>RESSEL (0-7)</td><td>1'b1</td><td>1'b0</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td></tr><tr><td>RESSEL (8-15)</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td></tr><tr><td>PORTSEL (0-7)</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td></tr><tr><td>PORTSEL (8-15)</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td></tr></table> Correct) <table><tr><th rowspan="3">Register (Offset)</th><th rowspan="3">Resource</th><th rowspan="3">RESSEL[3 :0] /PORTSEL L[3:0]</th><th colspan="8">Source for Resource input</th></tr><tr><th>0</th><th>1</th><th>2</th><th>3</th><th>4</th><th>5</th><th>6</th><th>7</th></tr><tr><th>8</th><th>9</th><th>10</th><th>11</th><th>12</th><th>13</th><th>14</th><th>15</th></tr><tr><td rowspan="4">RIC_RESI N330 (0x0294)</td><td rowspan="4">OCU20_MOD</td><td>RESSEL (0-7)</td><td>set1</td><td>set0</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td></tr><tr><td>RESSEL (8-15)</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td></tr><tr><td>PORTSEL (0-7)</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td></tr><tr><td>PORTSEL (8-15)</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td></tr><tr><td rowspan="4">RIC_RESI N331 (0x0296)</td><td rowspan="4">OCU21_MOD</td><td>RESSEL (0-7)</td><td>set1</td><td>set0</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td></tr><tr><td>RESSEL (8-15)</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td></tr><tr><td>PORTSEL (0-7)</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td></tr><tr><td>PORTSEL (8-15)</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td></tr></table>	Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL L[3:0]	Source for Resource input								0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	RIC_RESI N330 (0x0294)	OCU20_MOD	RESSEL (0-7)	1'b1	1'b0	-	-	-	-	-	-	RESSEL (8-15)	-	-	-	-	-	-	-	-	PORTSEL (0-7)	-	-	-	-	-	-	-	-	PORTSEL (8-15)	-	-	-	-	-	-	-	-	RIC_RESI N331 (0x0296)	OCU21_MOD	RESSEL (0-7)	1'b1	1'b0	-	-	-	-	-	-	RESSEL (8-15)	-	-	-	-	-	-	-	-	PORTSEL (0-7)	-	-	-	-	-	-	-	-	PORTSEL (8-15)	-	-	-	-	-	-	-	-	Register (Offset)	Resource	RESSEL[3 :0] /PORTSEL L[3:0]	Source for Resource input								0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	RIC_RESI N330 (0x0294)	OCU20_MOD	RESSEL (0-7)	set1	set0	-	-	-	-	-	-	RESSEL (8-15)	-	-	-	-	-	-	-	-	PORTSEL (0-7)	-	-	-	-	-	-	-	-	PORTSEL (8-15)	-	-	-	-	-	-	-	-	RIC_RESI N331 (0x0296)	OCU21_MOD	RESSEL (0-7)	set1	set0	-	-	-	-	-	-	RESSEL (8-15)	-	-	-	-	-	-	-	-	PORTSEL (0-7)	-	-	-	-	-	-	-	-	PORTSEL (8-15)	-	-	-	-	-	-	-	-
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Page	Section	Change Results
231	CHAPTER11: Port Configuration 3.1.Resource input configuration	Revised the below: Add Note Note: – <i>If BTx_ADTO is used by ADCx_HWTRGx, set by the two RIC_RESIN (Resource Input Setting Register). Select the bt_adto_xxx_x by ADCx_HWTRGx and then, select the BTx_ADTO by bt_adto_xxx_x.</i>

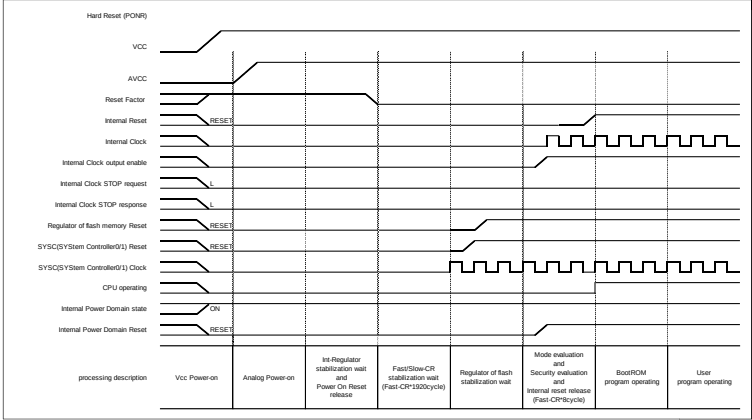
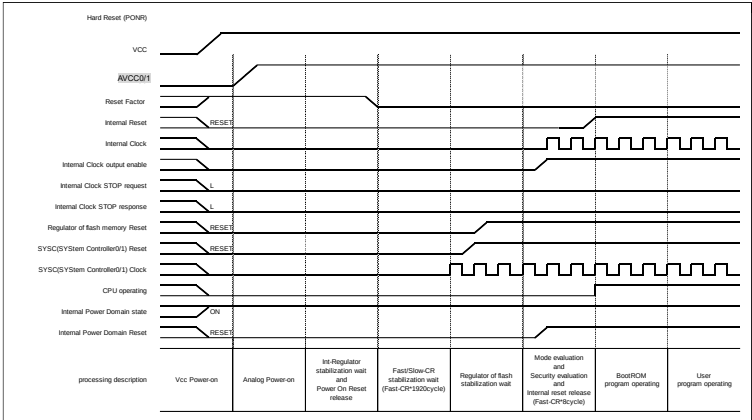
Page	Section	Change Results										
253 to 256	CHAPTER11: Port Configuration 3.6.Function Port Group	Revised the below: Add Function Port Group A port group specifies an I/O port combination for a peripheral function. A peripheral function has some port groups and should be configured and used within a port group of them which is defined in the following table in order to satisfy AC specification. Do not take a port combination which is not described in the following table as a port group. <table><tr><th>Function</th><th>Port Group</th></tr><tr><td>Multi-Function Serial Ch.0</td><td>Group1 - SCK0_0 - SIN0_0 - SOT0_0 - SCS0_0/SCS0_1</td></tr><tr><td>Multi-Function Serial Ch.1</td><td>Group1 - SCK1_0 - SIN1_0 - SOT1_0 - SCS1_0</td></tr><tr><td>Multi-Function Serial Ch.2</td><td>Group1 - SCK2_0 - SIN2_0 - SOT2_0 - SCS20_0 - SCS21_0 - SCS22_0 - SCS23_0 Group2 - SCK2_1 - SIN2_0/SIN2_1/SIN2_2 - SOT2_0/SOT2_1 - SCS20_0/SCS20_1 - SCS21_0/SCS21_1 - SCS22_0/SCS22_1 - SCS23_0/SCS23_1</td></tr><tr><td>Multi-Function Serial Ch.3</td><td>Group1 - SCK3_0 - SIN3_0 - SOT3_0 - SCS30_0/SCS30_1</td></tr></table>	Function	Port Group	Multi-Function Serial Ch.0	Group1 - SCK0_0 - SIN0_0 - SOT0_0 - SCS0_0/SCS0_1	Multi-Function Serial Ch.1	Group1 - SCK1_0 - SIN1_0 - SOT1_0 - SCS1_0	Multi-Function Serial Ch.2	Group1 - SCK2_0 - SIN2_0 - SOT2_0 - SCS20_0 - SCS21_0 - SCS22_0 - SCS23_0 Group2 - SCK2_1 - SIN2_0/SIN2_1/SIN2_2 - SOT2_0/SOT2_1 - SCS20_0/SCS20_1 - SCS21_0/SCS21_1 - SCS22_0/SCS22_1 - SCS23_0/SCS23_1	Multi-Function Serial Ch.3	Group1 - SCK3_0 - SIN3_0 - SOT3_0 - SCS30_0/SCS30_1
Function	Port Group											
Multi-Function Serial Ch.0	Group1 - SCK0_0 - SIN0_0 - SOT0_0 - SCS0_0/SCS0_1											
Multi-Function Serial Ch.1	Group1 - SCK1_0 - SIN1_0 - SOT1_0 - SCS1_0											
Multi-Function Serial Ch.2	Group1 - SCK2_0 - SIN2_0 - SOT2_0 - SCS20_0 - SCS21_0 - SCS22_0 - SCS23_0 Group2 - SCK2_1 - SIN2_0/SIN2_1/SIN2_2 - SOT2_0/SOT2_1 - SCS20_0/SCS20_1 - SCS21_0/SCS21_1 - SCS22_0/SCS22_1 - SCS23_0/SCS23_1											
Multi-Function Serial Ch.3	Group1 - SCK3_0 - SIN3_0 - SOT3_0 - SCS30_0/SCS30_1											

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253 to 256	CHAPTER11: Port Configuration 3.6.Function Port Group	Continuation	
		Multi-Function Serial Ch.4	Group1 - SCK4_0 - SIN4_0/SIN4_2 - SOT4_0 - SCS40_0 - SCS41_0 - SCS42_0 - SCS43_0 Group2 - SCK4_1 - SIN4_1 - SOT4_1 - SCS40_1 - SCS41_1 - SCS42_1 - SCS43_1
		Multi-Function Serial Ch.5	Group1 - SCK5_0/SCK5_1 - SIN5_0/SIN5_1 - SOT5_0/SOT5_1 - SCS50_0 - SCS51_0 - SCS52_0 - SCS53_0

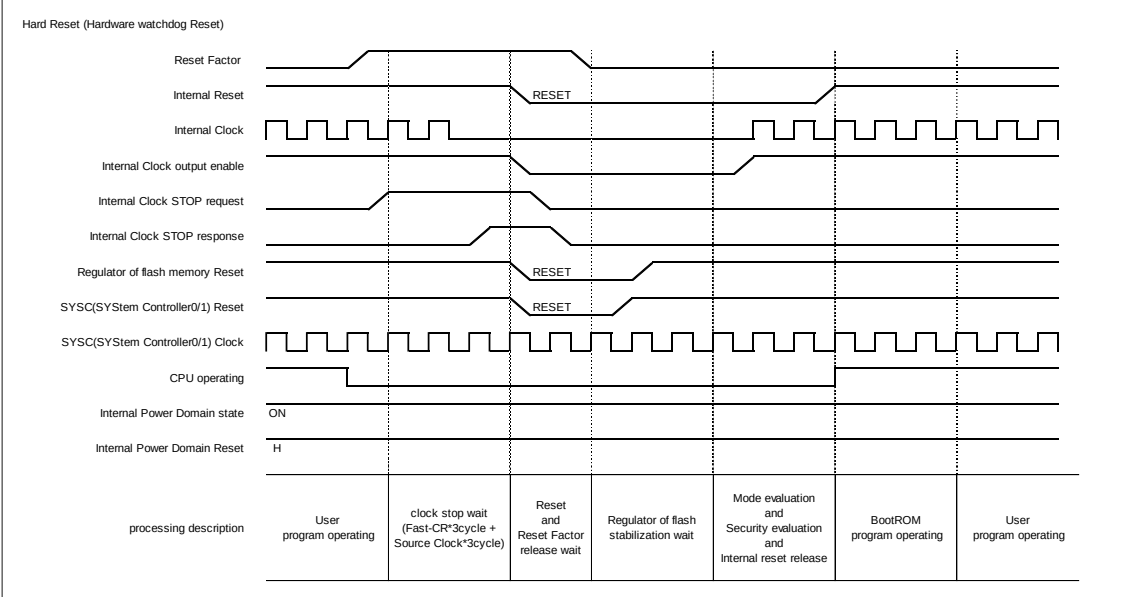
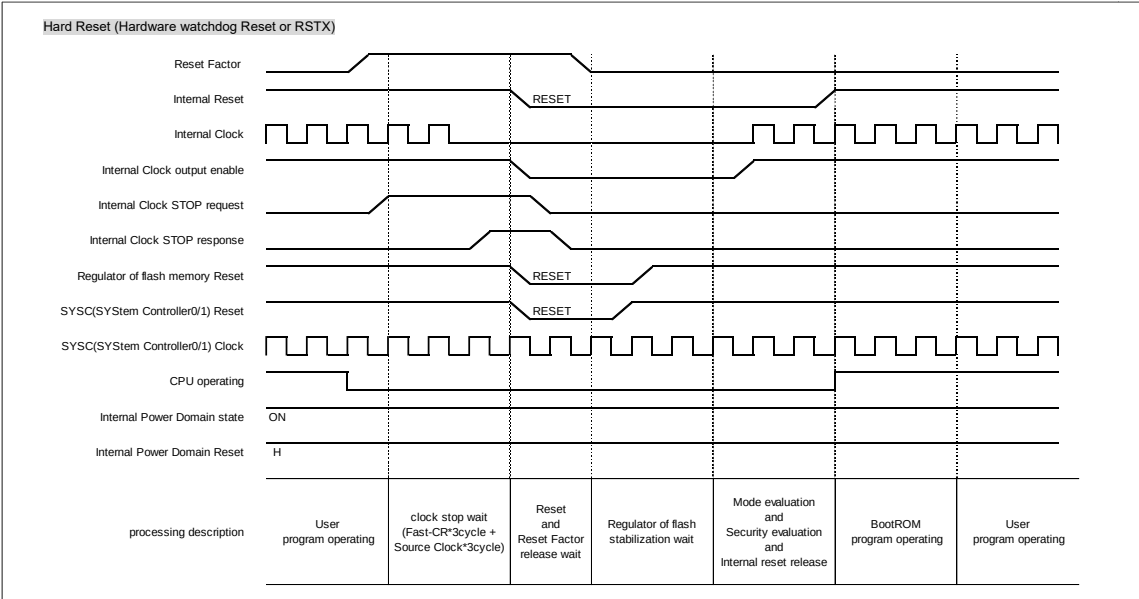
Page	Section	Change Results	
253 to 256	CHAPTER 11: Port Configuration 3.6.Function Port Group	Continuation	
		Multi-Function Serial Ch.6	Group1 - SCK6_0 - SIN6_0 - SOT6_0 - SCS60_0 - SCS61_0 - SCS62_0 - SCS63_0 Group2 - SCK6_1 - SIN6_1 - SOT6_1 - SCS60_1/SCS60_2 - SCS61_1 - SCS62_1 - SCS63_1
		Multi-Function Serial Ch.7	Group1 - SCK7_0 - SIN7_0/SIN7_2/SIN7_3 - SOT7_0 - SCS70_0 - SCS71_0 - SCS72_0 - SCS73_0 Group2 - SCK7_1 - SIN7_1 - SOT7_1 - SCS70_1 - SCS71_1 - SCS72_1 - SCS73_1

Page	Section	Change Results								
253 to 256	CHAPTER11: Port Configuration 3.6.Function Port Group	Continuation <table><tr><td>Multi-Function Serial Ch.8</td><td>Group1 - SCK8_0 - SIN8_0/SIN8_1/SIN8_2 - SOT8_0 - SCS80_0 - SCS81_0 - SCS82_0 - SCS83_0/SCS83_1</td></tr><tr><td>Multi-Function Serial Ch.9</td><td>Group1 - SCK9_0/SCK9_1 - SIN9_0 - SOT9_0/SOT9_1 - SCS90_0/SCS90_1</td></tr><tr><td>Multi-Function Serial Ch.10</td><td>Group1 - SCK10_0 - SIN10_0 - SOT10_0 - SCS100_0/SCS100_1 - SCS101_0/SCS101_1 - SCS102_0/SCS102_1 - SCS103_0</td></tr><tr><td>Multi-Function Serial Ch.11</td><td>Group1 - SCK11_0 - SIN11_0 - SOT11_0/SOT11_1 - SCS110_0/SCS110_1</td></tr></table>	Multi-Function Serial Ch.8	Group1 - SCK8_0 - SIN8_0/SIN8_1/SIN8_2 - SOT8_0 - SCS80_0 - SCS81_0 - SCS82_0 - SCS83_0/SCS83_1	Multi-Function Serial Ch.9	Group1 - SCK9_0/SCK9_1 - SIN9_0 - SOT9_0/SOT9_1 - SCS90_0/SCS90_1	Multi-Function Serial Ch.10	Group1 - SCK10_0 - SIN10_0 - SOT10_0 - SCS100_0/SCS100_1 - SCS101_0/SCS101_1 - SCS102_0/SCS102_1 - SCS103_0	Multi-Function Serial Ch.11	Group1 - SCK11_0 - SIN11_0 - SOT11_0/SOT11_1 - SCS110_0/SCS110_1
Multi-Function Serial Ch.8	Group1 - SCK8_0 - SIN8_0/SIN8_1/SIN8_2 - SOT8_0 - SCS80_0 - SCS81_0 - SCS82_0 - SCS83_0/SCS83_1									
Multi-Function Serial Ch.9	Group1 - SCK9_0/SCK9_1 - SIN9_0 - SOT9_0/SOT9_1 - SCS90_0/SCS90_1									
Multi-Function Serial Ch.10	Group1 - SCK10_0 - SIN10_0 - SOT10_0 - SCS100_0/SCS100_1 - SCS101_0/SCS101_1 - SCS102_0/SCS102_1 - SCS103_0									
Multi-Function Serial Ch.11	Group1 - SCK11_0 - SIN11_0 - SOT11_0/SOT11_1 - SCS110_0/SCS110_1									

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253 to 256	CHAPTER 11: Port Configuration 3.6.Function Port Group	Continuation	
		Multi-Function Serial Ch.12	Group1 - SCK12_0/SCK12_2 - SIN12_0/SIN12_2 - SOT12_0 - SCS120_0 Group2 - SCK12_1 - SIN12_1 - SOT12_1 - SCS120_1
		Multi-Function Serial Ch.13	Group1 - SCK13_0 - SIN13_0 - SOT13_0 - SCS130_0

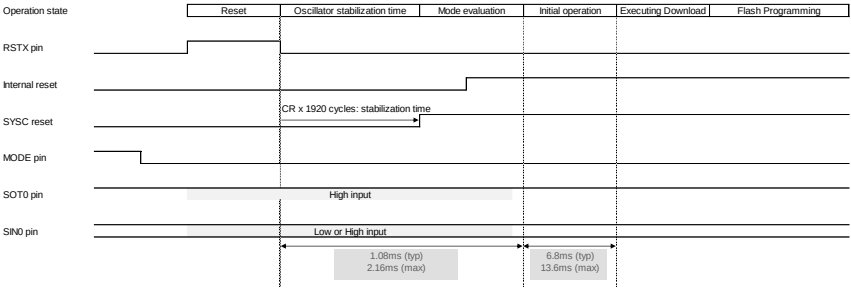
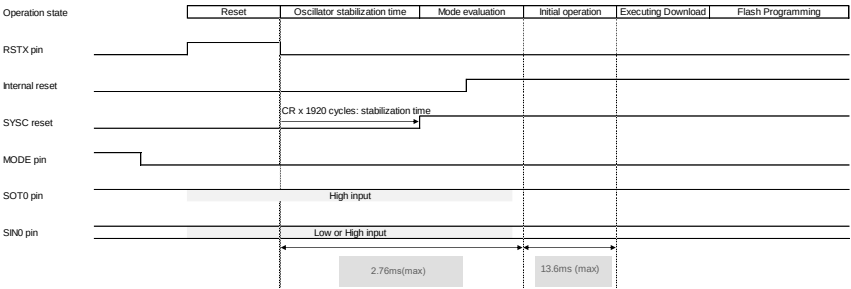
Page	Section	Change Results
263	CHAPTER 12: State Transition 3. Fetching the Operation Mode	Revised the below: This section describes the Fetching the Operation Mode. Figure3-1 Operation Mode Fetch Timing Chart Error)  Correct)  S6J3400 guarantees that 1) Each power supply is stable before reset release for that domain 2) Isolation is valid before each pair of adjacent supplies is stable during power-up sequence Power-up sequence defined in S6J3400 datasheet.

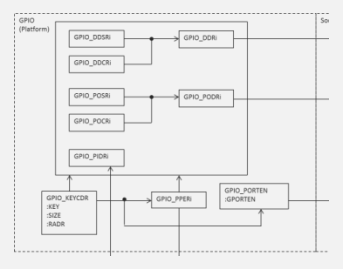
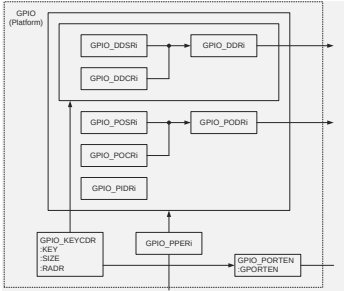
Page	Section	Change Results																																																																																					
263, 264	CHAPTER 12: State Transition 3. Fetching the Operation Mode	Continuation 1) Each power supply is stable before reset release for that domain Below table describes reset asserted until stabilization of each supply: <table><tr><th>#</th><th>Power supply</th><th>Reset</th><th>Responsibility (CY MCU or User?)</th><th>Reset release above Min Safe voltage?</th><th>Corr. phase in POR release diagram (sheet "POR diagram")</th><th>Explanation of Reset</th></tr><tr><td>1</td><td>VCC</td><td>LVDH1 reset</td><td>CY MCU</td><td>Yes</td><td>(1)</td><td>VCC is monitored by LVDH1 which detects & release BOD above Min Safe Voltage</td></tr><tr><td>2</td><td>VDD (internal 1.2V)</td><td>POR</td><td>CY MCU</td><td>Yes</td><td>(3)</td><td>VDD rises above safe voltage during Int-Regulator stabilization wait shown in (3) in sheet POR Diagram</td></tr><tr><td>3</td><td>AVCC0/1</td><td>LVDH1 reset or RSTX</td><td>CY MCU or User (*see note)</td><td>Yes</td><td>(1)</td><td>LVDH1 can monitor AVCC0/1 only if it's shorted with VCC on the customer board. Otherwise, customer needs to take care of the BOD on the board and issue appropriate reset (RSTX, etc.) to inactivate the domain until the supply is stable.</td></tr></table> 2) Isolation is valid before each pair of adjacent supplies is stable during power-up sequence Below table describes isolation available for each adjacent supply pair: <table><tr><th>#</th><th>From</th><th>To</th><th>Isolation method</th><th>Isolator assert timing (sheet "POR diagram")</th><th>Isolator release timing (sheet "POR diagram")</th></tr><tr><td>1</td><td>VCC</td><td>VDD</td><td>POR & LVDH1 initialize both domains until VCC stabilization</td><td>(1) POR assertion</td><td>(2) LVDH1 release</td></tr><tr><td>2</td><td>AVCC0/1</td><td>VDD</td><td>LVDH1 reset (if AVCC0/1 shorted w/ VCC on board) or RSTX, etc. (otherwise) works as isolation until AVCC0/1 powers up and user inverts the bit in software</td><td>(1) POR assertion or RSTX etc. assertion</td><td>(1) LVDH1 or RSTX etc. release</td></tr><tr><td>3</td><td>VDD</td><td>VCC</td><td>POR initialized both domains until VDD stabilization</td><td>(1) POR assertion</td><td>(3) POR release</td></tr><tr><td>4</td><td>VDD</td><td>AVCC0/1</td><td>POR initialized both domains until VDD stabilization</td><td>(1) POR assertion</td><td>(3) POR release</td></tr></table> Existing power supply pairs (# in parenthesis = corresp. entry in above table): <table><tr><th></th><th></th><th colspan="3">To</th><th></th></tr><tr><th rowspan="4">From</th><th></th><th>VCC</th><th>VDD</th><th>AVCC0/1</th><th></th></tr><tr><th>VCC</th><td></td><td>x (1)</td><td></td><td>VCC interacts only with regulated domain</td></tr><tr><th>VDD</th><td>x (3)</td><td></td><td>x (4)</td><td>VDD interacts with Always-ON domain I/Os</td></tr><tr><th>AVCC0/1</th><td></td><td>x (2)</td><td></td><td>AVCC0/1 powers analog SWs & A/D in VDD domain</td></tr></table>	#	Power supply	Reset	Responsibility (CY MCU or User?)	Reset release above Min Safe voltage?	Corr. phase in POR release diagram (sheet "POR diagram")	Explanation of Reset	1	VCC	LVDH1 reset	CY MCU	Yes	(1)	VCC is monitored by LVDH1 which detects & release BOD above Min Safe Voltage	2	VDD (internal 1.2V)	POR	CY MCU	Yes	(3)	VDD rises above safe voltage during Int-Regulator stabilization wait shown in (3) in sheet POR Diagram	3	AVCC0/1	LVDH1 reset or RSTX	CY MCU or User (*see note)	Yes	(1)	LVDH1 can monitor AVCC0/1 only if it's shorted with VCC on the customer board. Otherwise, customer needs to take care of the BOD on the board and issue appropriate reset (RSTX, etc.) to inactivate the domain until the supply is stable.	#	From	To	Isolation method	Isolator assert timing (sheet "POR diagram")	Isolator release timing (sheet "POR diagram")	1	VCC	VDD	POR & LVDH1 initialize both domains until VCC stabilization	(1) POR assertion	(2) LVDH1 release	2	AVCC0/1	VDD	LVDH1 reset (if AVCC0/1 shorted w/ VCC on board) or RSTX, etc. (otherwise) works as isolation until AVCC0/1 powers up and user inverts the bit in software	(1) POR assertion or RSTX etc. assertion	(1) LVDH1 or RSTX etc. release	3	VDD	VCC	POR initialized both domains until VDD stabilization	(1) POR assertion	(3) POR release	4	VDD	AVCC0/1	POR initialized both domains until VDD stabilization	(1) POR assertion	(3) POR release			To				From		VCC	VDD	AVCC0/1		VCC		x (1)		VCC interacts only with regulated domain	VDD	x (3)		x (4)	VDD interacts with Always-ON domain I/Os	AVCC0/1		x (2)		AVCC0/1 powers analog SWs & A/D in VDD domain
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3	AVCC0/1	LVDH1 reset or RSTX	CY MCU or User (*see note)	Yes	(1)	LVDH1 can monitor AVCC0/1 only if it's shorted with VCC on the customer board. Otherwise, customer needs to take care of the BOD on the board and issue appropriate reset (RSTX, etc.) to inactivate the domain until the supply is stable.																																																																																	
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From		VCC	VDD	AVCC0/1																																																																																			
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	VDD	x (3)		x (4)	VDD interacts with Always-ON domain I/Os																																																																																		
	AVCC0/1		x (2)		AVCC0/1 powers analog SWs & A/D in VDD domain																																																																																		

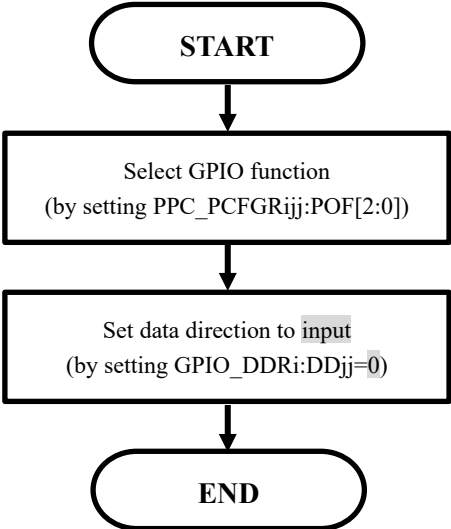
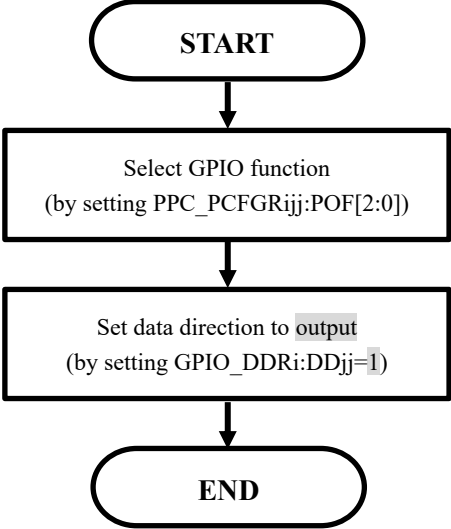
Page	Section	Change Results
265	CHAPTER 12: State Transition 3. Fetching the Operation Mode	Revised the below: This section describes the Fetching the Operation Mode. Figure3-2 Operation Mode Fetch Timing Chart Error)  Correct) 

Page	Section	Change Results																																				
278	CHAPTER14 : Low Voltage Detection 3.Registers	Revised the below: [Bit27:25] LVDL1V Internal low-voltage detection voltage setting bits Error) <table><tr><th>Bit 27:25</th><th>Voltage [V]</th></tr><tr><td>000</td><td>0.875(Initial value)</td></tr><tr><td>001</td><td>0.95</td></tr><tr><td>010</td><td>Reserved</td></tr><tr><td>011</td><td>Reserved</td></tr><tr><td>100</td><td>Reserved</td></tr><tr><td>101</td><td>Reserved</td></tr><tr><td>110</td><td>Reserved</td></tr><tr><td>111</td><td>Reserved</td></tr></table> Correct) <table><tr><th>Bit 27:25</th><th>Voltage [V]</th></tr><tr><td>000 *</td><td>0.875(Initial value)</td></tr><tr><td>001 *</td><td>0.95</td></tr><tr><td>010</td><td>Reserved</td></tr><tr><td>011</td><td>Reserved</td></tr><tr><td>100</td><td>Reserved</td></tr><tr><td>101</td><td>Reserved</td></tr><tr><td>110</td><td>Reserved</td></tr><tr><td>111</td><td>Reserved</td></tr></table> *: These detection voltage level settings are below the minimum operation voltage. Between these detection voltage and the minimum operation voltage, MCU functions are not guaranteed except for the low voltage detector. Note that although the detection level is below the minimum operation guarantee voltage, the LVD reset factor flag is set as the voltage drops below the detection level.	Bit 27:25	Voltage [V]	000	0.875(Initial value)	001	0.95	010	Reserved	011	Reserved	100	Reserved	101	Reserved	110	Reserved	111	Reserved	Bit 27:25	Voltage [V]	000 *	0.875(Initial value)	001 *	0.95	010	Reserved	011	Reserved	100	Reserved	101	Reserved	110	Reserved	111	Reserved
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Page	Section	Change Results																																				
279	CHAPTER14 : Low Voltage Detection 3.Registers	Revised the below: [Bit11:9] LVDH1V External low-voltage detection voltage setting bits Error) <table><thead><tr><th>Bit 11:9</th><th>Voltage [V]</th></tr></thead><tbody><tr><td>000</td><td>2.7</td></tr><tr><td>001</td><td>2.8</td></tr><tr><td>010</td><td>3.6</td></tr><tr><td>011</td><td>3.8</td></tr><tr><td>100</td><td>4.0</td></tr><tr><td>101</td><td>4.2</td></tr><tr><td>110</td><td>2.5</td></tr><tr><td>111</td><td>2.6(Initial value)</td></tr></tbody></table> Correct) <table><thead><tr><th>Bit 11:9</th><th>Voltage [V]</th></tr></thead><tbody><tr><td>000 *</td><td>2.7</td></tr><tr><td>001</td><td>2.8</td></tr><tr><td>010</td><td>3.6</td></tr><tr><td>011</td><td>3.8</td></tr><tr><td>100</td><td>4.0</td></tr><tr><td>101</td><td>4.2</td></tr><tr><td>110 *</td><td>2.5</td></tr><tr><td>111 *</td><td>2.6(Initial value)</td></tr></tbody></table> *: These detection voltage level settings are below the minimum operation assurance voltage (2.7V) . Between these detection voltage and the minimum operation assurance voltage, MCU functions are not guaranteed except for the low voltage detector. Note that although the detection level is below the minimum operation guarantee voltage, the LVD reset factor flag is set as the voltage drops below the detection level.	Bit 11:9	Voltage [V]	000	2.7	001	2.8	010	3.6	011	3.8	100	4.0	101	4.2	110	2.5	111	2.6(Initial value)	Bit 11:9	Voltage [V]	000 *	2.7	001	2.8	010	3.6	011	3.8	100	4.0	101	4.2	110 *	2.5	111 *	2.6(Initial value)
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Page	Section	Change Results
286	CHAPTER15 Serial Programming 5.OPERATIO N	Revised the below: 5.1 Timing chart Figure5-1 Error)  Correct) 

Page	Section	Change Results
549	Error! Use the Home tab to apply 見出し 1 to the text that you want to appear here. Error! Use the Home tab to apply 見出し 1 to the text that you want to appear here. 2.Configuration n and Block Diagram	Revised the below: Figure 0-1 Configuration Diagram of GPIO and PPC Error)  Correct) 

Page	Section	Change Results
555	Error! Use the Home tab to apply 見出し 1 to the text that you want to appear here. Error! Use the Home tab to apply 見出し 1 to the text that you want to appear here. 3.Setting Procedure Examples	Revised the below: Figure 0-5 Setting Procedure Error)  <pre> graph TD START1([START]) --> Select1[Select GPIO function (by setting PPC_PCFGRijj:POF[2:0])] Select1 --> SetDir1[Set data direction to input (by setting GPIO_ODDRi:DDij=0)] SetDir1 --> END1([END]) </pre> Correct)  <pre> graph TD START2([START]) --> Select2[Select GPIO function (by setting PPC_PCFGRijj:POF[2:0])] Select2 --> SetDir2[Set data direction to output (by setting GPIO_ODDRi:DDij=1)] SetDir2 --> END2([END]) </pre>

Page	Section	Change Results						
Rev. *B								
-	-	Modified I ² C from to I ² C.						
20	CHAPTER 2: Function List 1. Function list	Revised as below: Error) <table border="1"> <tr> <td>Core clock frequency</td><td>132MHz</td><td></td></tr> </table> Correct) <table border="1"> <tr> <td>Core clock frequency</td><td>132MHz</td><td>See the AC specification on the datasheet</td></tr> </table>	Core clock frequency	132MHz		Core clock frequency	132MHz	See the AC specification on the datasheet
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20	CHAPTER 2: Function List 1. Function list	Revised as below:																
		Error) <table><tr><td>Embedded CR oscillation</td><td>Slow clock:100kHz, Fast clock: 4MHz (Center frequency)</td><td>See the datasheet</td></tr></table>	Embedded CR oscillation	Slow clock:100kHz, Fast clock: 4MHz (Center frequency)	See the datasheet													
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20	CHAPTER 2: Function List 1. Function list	Revised as below:																
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21	CHAPTER 2: Function List 1. Function list	Revised as below:																
		Error) <table><tr><td rowspan="3">Base timer</td><td>64ch</td><td>60ch</td><td>55ch</td><td>48ch</td><td></td></tr><tr><td>64ch</td><td>55ch</td><td>47ch</td><td>40ch</td><td>with out pin</td></tr><tr><td>64ch</td><td>57ch</td><td>42ch</td><td>30ch</td><td>with in pin</td></tr></table>	Base timer	64ch	60ch	55ch	48ch		64ch	55ch	47ch	40ch	with out pin	64ch	57ch	42ch	30ch	with in pin
		Base timer		64ch	60ch	55ch	48ch											
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Page	Section	Change Results																						
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21	CHAPTER 2: Function List 1. Function list	Revised as below: Error) <table><tr><td rowspan="2">Multi-function serial interface</td><td>14ch</td><td>13ch</td><td>13ch</td><td>13ch</td><td>memory size digit from 8 to A</td></tr><tr><td>14ch</td><td>13ch</td><td>13ch</td><td>12ch</td><td>with CS pin</td></tr></table> Correct) <table><tr><td rowspan="2">Multi-function serial interface</td><td>14ch</td><td>13ch</td><td>13ch</td><td>13ch</td><td>memory size digit from 8 to A See the AC specification on the datasheet</td></tr><tr><td>14ch</td><td>13ch</td><td>13ch</td><td>12ch</td><td>with CS pin See the AC specification on the datasheet</td></tr></table>	Multi-function serial interface	14ch	13ch	13ch	13ch	memory size digit from 8 to A	14ch	13ch	13ch	12ch	with CS pin	Multi-function serial interface	14ch	13ch	13ch	13ch	memory size digit from 8 to A See the AC specification on the datasheet	14ch	13ch	13ch	12ch	with CS pin See the AC specification on the datasheet
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21	CHAPTER 2: Function List 1. Function list	Revised as below: Error) <table><tr><td>CAN-FD RAM (ECC supported)</td><td>16KB/ch It equivalents to 128 message buffer per channel of CCAN module</td><td></td></tr></table> Correct) <table><tr><td>CAN-FD RAM (ECC supported)</td><td>16KB/ch It is equivalent to 192 message buffer per channel of CAN module</td><td></td></tr></table>	CAN-FD RAM (ECC supported)	16KB/ch It equivalents to 128 message buffer per channel of CCAN module		CAN-FD RAM (ECC supported)	16KB/ch It is equivalent to 192 message buffer per channel of CAN module																	
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21	CHAPTER 2: Function List 1. Function list	Deleted as below: Error) <table><tr><td>FlexRay</td><td>No</td><td>See 2.1</td></tr></table>	FlexRay	No	See 2.1																			
FlexRay	No	See 2.1																						

Page	Section	Change Results																																																																												
23	CHAPTER 2: Function List 1. Function list	Revised as below: Error) Figure 2-1 Memory size: <table><thead><tr><th rowspan="2">Digit</th><th colspan="2">Flash</th><th colspan="2">RAM</th></tr><tr><th>Program</th><th>Work</th><th>Main</th><th>Back up</th></tr></thead><tbody><tr><td>E</td><td>4,160 KB</td><td>112 KB</td><td>512 KB</td><td>48+16 KB</td></tr><tr><td>D</td><td>3,136 KB</td><td>112 KB</td><td>320 KB</td><td>48+16 KB</td></tr><tr><td>C</td><td>2,212 KB</td><td>112 KB</td><td>256 KB</td><td>16+8 KB</td></tr><tr><td>B</td><td>1,600 KB</td><td>112 KB</td><td>192 KB</td><td>16+8 KB</td></tr><tr><td>A</td><td>1,088 KB</td><td>112 KB</td><td>128 KB</td><td>8+4 KB</td></tr><tr><td>9</td><td>832 KB</td><td>112 KB</td><td>80 KB</td><td>8+4 KB</td></tr><tr><td>8</td><td>576 KB</td><td>112 KB</td><td>64 KB</td><td>8+4 KB</td></tr></tbody></table> Function: <table><thead><tr><th>Digit</th><th>Flex Ray</th></tr></thead><tbody><tr><td>1</td><td>Yes</td></tr><tr><td>2</td><td>-</td></tr></tbody></table> Correct) Memory size: <table><thead><tr><th rowspan="2">Digit</th><th colspan="2">Flash</th><th colspan="2">RAM</th></tr><tr><th>Program</th><th>Work</th><th>Main</th><th>Back up</th></tr></thead><tbody><tr><td>A</td><td>1,088 KB</td><td>112 KB</td><td>128 KB</td><td>8+4 KB</td></tr><tr><td>9</td><td>832 KB</td><td>112 KB</td><td>80 KB</td><td>8+4 KB</td></tr><tr><td>8</td><td>576 KB</td><td>112 KB</td><td>64 KB</td><td>8+4 KB</td></tr></tbody></table> Function: <table><thead><tr><th>Digit</th></tr></thead><tbody><tr><td>2</td></tr></tbody></table>	Digit	Flash		RAM		Program	Work	Main	Back up	E	4,160 KB	112 KB	512 KB	48+16 KB	D	3,136 KB	112 KB	320 KB	48+16 KB	C	2,212 KB	112 KB	256 KB	16+8 KB	B	1,600 KB	112 KB	192 KB	16+8 KB	A	1,088 KB	112 KB	128 KB	8+4 KB	9	832 KB	112 KB	80 KB	8+4 KB	8	576 KB	112 KB	64 KB	8+4 KB	Digit	Flex Ray	1	Yes	2	-	Digit	Flash		RAM		Program	Work	Main	Back up	A	1,088 KB	112 KB	128 KB	8+4 KB	9	832 KB	112 KB	80 KB	8+4 KB	8	576 KB	112 KB	64 KB	8+4 KB	Digit	2
Digit	Flash			RAM																																																																										
	Program	Work	Main	Back up																																																																										
E	4,160 KB	112 KB	512 KB	48+16 KB																																																																										
D	3,136 KB	112 KB	320 KB	48+16 KB																																																																										
C	2,212 KB	112 KB	256 KB	16+8 KB																																																																										
B	1,600 KB	112 KB	192 KB	16+8 KB																																																																										
A	1,088 KB	112 KB	128 KB	8+4 KB																																																																										
9	832 KB	112 KB	80 KB	8+4 KB																																																																										
8	576 KB	112 KB	64 KB	8+4 KB																																																																										
Digit	Flex Ray																																																																													
1	Yes																																																																													
2	-																																																																													
Digit	Flash		RAM																																																																											
	Program	Work	Main	Back up																																																																										
A	1,088 KB	112 KB	128 KB	8+4 KB																																																																										
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8	576 KB	112 KB	64 KB	8+4 KB																																																																										
Digit																																																																														
2																																																																														
24	CHAPTER 2: Function List 1. Function list	Revised as below: 2.2 ID Error) <table><thead><tr><th>Function digit</th><th>Chip ID</th></tr></thead><tbody><tr><td>8, 9, A</td><td>0x10130000</td></tr></tbody></table> Correct) See the ID specification on the Datasheet in detail.	Function digit	Chip ID	8, 9, A	0x10130000																																																																								
Function digit	Chip ID																																																																													
8, 9, A	0x10130000																																																																													

Page	Section	Change Results			
25	CHAPTER 2: Function List 2. Optional function 2.3. Restriction	Revised as below:			
		Error)			
		Function	TEQFP144 LQFP144	TEQFP120 LQFP120	TEQFP100 LQFP100
		Analog input port (12bit-ADC)	AN001 to 002, AN007, AN012, AN015 to 016, AN023 to 024 (56 ports)	AN001 to 002, AN006 to 007, AN009, AN011 to 012, AN015 to 016, AN020, AN023 to 024, AN031, AN103, AN116, AN122, AN126, AN130 to 131 (45 ports)	AN001 to 002, AN004, AN006 to 007, AN009, AN011 to 012, AN015 to 016, AN018, AN020, AN023 to 024, AN026, AN029, AN031, AN101, AN103 to 105, AN116 to 117, AN122, AN124, AN126, AN130 to 131 (35 ports)
		Correct)			
		Function	TEQFP144 LQFP144	TEQFP120 LQFP120	TEQFP100 LQFP100
		Analog input port (12bit-ADC)	AN001 to 002, AN007, AN012, AN015 to 016, AN023 to 024 (56 ports)	AN001 to 002, AN006 to 007, AN009, AN011 to 012, AN015 to 016, AN020, AN023 to 024, AN031, AN103, AN116, AN122, AN126, AN130 to 131 (45 ports)	AN001 to 002, AN004, AN006 to 007, AN009, AN011 to 012, AN015 to 016, AN018, AN020, AN023 to 024, AN026, AN029, AN031, AN101, AN103 to 105, AN116 to 117, AN122, AN124, AN126, AN130 to 131 (35 ports)

Page	Section	Change Results			
25	CHAPTER 2: Function List 2. Optional function 2.3. Restriction	Revised as below:			
		Error)			
		Function	TEQFP144 LQFP144	TEQFP120 LQFP120	TEQFP100 LQFP100
		General-Purpose I/O	P0_02, P0_04, P0_11, P0_14, P0_25 to 0_26, P1_02, P1_04, P1_10 to 1_11, P1_16, P1_21, P1_24 to 1_25, P2_00 to 2_01, P2_16 to 2_17, P2_21, P3_03, P3_10 to 3_11, P3_16, P3_20, P3_25 to 3_26, P3_28 to 3_29, P4_10, P4_12, P4_15, P4_19	P0_00, P0_02 to P0_04, P0_11, P0_14, P0_18 to 0_19, P0_24 to 0_26, P1_01 to 1_02, P1_04, P1_10 to 1_11, P1_15 to 1_16, P1_18, P1_20 to 1_21, P1_24 to 1_25, P1_29, P2_00 to 2_01, P2_08, P2_12, P2_16 to 2_17, P2_21, P2_31, P3_03, P3_06, P3_10 to 3_12, P3_16 to 3_20, P3_25 to 3_26, P3_28 to 3_30, P4_07 to 4_08, P4_10 to 4_12, P4_14 to 4_15, P4_17, P4_19	P0_00, P0_02 to P0_04, P0_08 to P0_09, P0_11, P0_14, P0_17 to 0_19, P0_23 to 0_26, P0_30, P1_01 to 1_02, P1_04, P1_10 to 1_11, P1_13, P1_15 to 1_16, P1_18, P1_20 to 1_21, P1_24 to 1_25, P1_27, P1_29, P2_00 to 2_01, P2_03, P2_06, P2_08, P2_10, P2_12, P2_16 to 2_19, P2_21, P2_30 to 2_31, P3_00, P3_03, P3_06, P3_08, P3_10 to 3_12, P3_16 to 3_20, P3_25 to 3_26, P3_28 to 3_30, P4_03 to 4_04, P4_06 to 4_08, P4_10 to 4_12, P4_14 to 4_15, P4_17 to 4_19, P4_21
		Correct)			
		Function	TEQFP144 LQFP144	TEQFP120 LQFP120	TEQFP100 LQFP100
		General-Purpose I/O	P002, P004, P011, P014, P025 to 026, P102, P104, P110 to 111, P116, P121, P124 to 125, P200 to 201, P216 to 217, P221, P303, P310 to 311, P316, P320, P325 to 326, P328 to 329, P410, P412, P415, P419	P000, P002 to P004, P011, P014, P018 to 019, P024 to 026, P101 to 102, P104, P110 to 111, P115 to 116, P118, P120 to 121, P124 to 125, P129, P200 to 201, P208, P212, P216 to 217, P221, P231, P303, P306, P310 to 312, P316 to 320, P325 to 326, P328 to 330, P407 to 408, P410 to 412, P414 to 415, P417, P419	P000, P002 to P004, P008 to P009, P011, P014, P017 to 019, P023 to 026, P030, P101 to 102, P104, P110 to 111, P113, P115 to 116, P118, P120 to 121, P124 to 125, P127, P129, P200 to 201, P203, P206, P208, P210, P212, P216 to 219, P221, P230 to 231, P300, P303, P306, P308, P310 to 312, P316 to 320, P325 to 326, P328 to 330, P403 to 404, P406 to 408, P410 to 412, P414 to 415, P417 to 419, P421

Page	Section	Change Results								
25	CHAPTER 2: Function List 2. Optional function 2.3. Restriction	Revised as below:								
		Error)								
		<table><tr><th>Function</th><th>TEQFP144 LQFP144</th><th>TEQFP120 LQFP120</th><th>TEQFP100 LQFP100</th></tr><tr><td>BaseTimer</td><td>TIOA0/1/2/3_1 TIOA14/15/16/17/18_0 TIOA21/25/26/27_1 TIOA51/57/58/59/61_0 TIOB56/57/58/59/60/61/62_0</td><td>TIOA0/1/2/3_1 TIOA9/10/13_1 TIOA8/14/15/16/17/18/19_0 TIOB0/5/10/12_0 TIOA27_0 TIOA21/23/25/26/27_1 TIOA51/53/56/57/58/59/60_0 TIOA61/62/63_0 TIOB24/26/29/33/37/38_0 TIOB43/48/49_0 TIOB51/56/57/58/59/60_0 TIOB61/62/63_0</td><td>TIOA0/1_0 TIOA0/1/2/3/5_1 TIOA9/10/13_1 TIOA7/8/14/15/16/17/18/19_0 TIOB0/4/5/8/10/12_0 TIOB14/15/19/21/22/23_0 TIOA26/27/28_0 TIOA21/23/25/26/27/28_1 TIOA49/51/53/56/57/58/59/60_0 TIOA61/62/63_0 TIOB24/29/33/35/37/38_0 TIOB43/44/46/47/48/49_0 TIOB51/53/56/57/58/59/60_0 TIOB61/62/63_0</td></tr></table>	Function	TEQFP144 LQFP144	TEQFP120 LQFP120	TEQFP100 LQFP100	BaseTimer	TIOA0/1/2/3_1 TIOA14/15/16/17/18_0 TIOA21/25/26/27_1 TIOA51/57/58/59/61_0 TIOB56/57/58/59/60/61/62_0	TIOA0/1/2/3_1 TIOA9/10/13_1 TIOA8/14/15/16/17/18/19_0 TIOB0/5/10/12_0 TIOA27_0 TIOA21/23/25/26/27_1 TIOA51/53/56/57/58/59/60_0 TIOA61/62/63_0 TIOB24/26/29/33/37/38_0 TIOB43/48/49_0 TIOB51/56/57/58/59/60_0 TIOB61/62/63_0	TIOA0/1_0 TIOA0/1/2/3/5_1 TIOA9/10/13_1 TIOA7/8/14/15/16/17/18/19_0 TIOB0/4/5/8/10/12_0 TIOB14/15/19/21/22/23_0 TIOA26/27/28_0 TIOA21/23/25/26/27/28_1 TIOA49/51/53/56/57/58/59/60_0 TIOA61/62/63_0 TIOB24/29/33/35/37/38_0 TIOB43/44/46/47/48/49_0 TIOB51/53/56/57/58/59/60_0 TIOB61/62/63_0
		Function	TEQFP144 LQFP144	TEQFP120 LQFP120	TEQFP100 LQFP100					
BaseTimer	TIOA0/1/2/3_1 TIOA14/15/16/17/18_0 TIOA21/25/26/27_1 TIOA51/57/58/59/61_0 TIOB56/57/58/59/60/61/62_0	TIOA0/1/2/3_1 TIOA9/10/13_1 TIOA8/14/15/16/17/18/19_0 TIOB0/5/10/12_0 TIOA27_0 TIOA21/23/25/26/27_1 TIOA51/53/56/57/58/59/60_0 TIOA61/62/63_0 TIOB24/26/29/33/37/38_0 TIOB43/48/49_0 TIOB51/56/57/58/59/60_0 TIOB61/62/63_0	TIOA0/1_0 TIOA0/1/2/3/5_1 TIOA9/10/13_1 TIOA7/8/14/15/16/17/18/19_0 TIOB0/4/5/8/10/12_0 TIOB14/15/19/21/22/23_0 TIOA26/27/28_0 TIOA21/23/25/26/27/28_1 TIOA49/51/53/56/57/58/59/60_0 TIOA61/62/63_0 TIOB24/29/33/35/37/38_0 TIOB43/44/46/47/48/49_0 TIOB51/53/56/57/58/59/60_0 TIOB61/62/63_0							
Correct)										
<table><tr><th>Function</th><th>TEQFP144 LQFP144</th><th>TEQFP120 LQFP120</th><th>TEQFP100 LQFP100</th></tr><tr><td>BaseTimer</td><td>TIOA0/1/2/3_1 TIOA14/15/16/17/18_0 TIOA21/25/26/27_1 TIOA51/57/58/59/61_0 TIOB56/57/58/59/60/61/62_0 0</td><td>TIOA0/1/2/3_1 TIOA9/10/13_1 TIOA8/14/15/16/17/18/19_0 TIOB0/5/10/12_0 TIOA27_0 TIOA21/23/25/26/27_1 TIOA51/53/56/57/58/59/60_0 TIOA61/62/63_0 TIOB24/25/29/33/37/38_0 TIOB43/48/49_0 TIOB51/56/57/58/59/60_0 TIOB61/62/63_0</td><td>TIOA0/1_0 TIOA0/1/2/3/5_1 TIOA9/10/13_1 TIOA7/8/14/15/16/17/18/19_0 TIOB0/4/5/8/10/12_0 TIOB14/15/19/22/23_0 TIOA21/26/27/28_0 TIOA21/23/25/26/27/28_1 TIOA49/51/53/56/57/58/59/60_0 TIOA61/62/63_0 TIOB24/25/29/33/35/37/38_0 TIOB43/44/46/47/48/49_0 TIOB51/53/56/57/58/59/60_0 TIOB61/62/63_0</td></tr></table>	Function	TEQFP144 LQFP144	TEQFP120 LQFP120	TEQFP100 LQFP100	BaseTimer	TIOA0/1/2/3_1 TIOA14/15/16/17/18_0 TIOA21/25/26/27_1 TIOA51/57/58/59/61_0 TIOB56/57/58/59/60/61/62_0 0	TIOA0/1/2/3_1 TIOA9/10/13_1 TIOA8/14/15/16/17/18/19_0 TIOB0/5/10/12_0 TIOA27_0 TIOA21/23/25/26/27_1 TIOA51/53/56/57/58/59/60_0 TIOA61/62/63_0 TIOB24/25/29/33/37/38_0 TIOB43/48/49_0 TIOB51/56/57/58/59/60_0 TIOB61/62/63_0	TIOA0/1_0 TIOA0/1/2/3/5_1 TIOA9/10/13_1 TIOA7/8/14/15/16/17/18/19_0 TIOB0/4/5/8/10/12_0 TIOB14/15/19/22/23_0 TIOA21/26/27/28_0 TIOA21/23/25/26/27/28_1 TIOA49/51/53/56/57/58/59/60_0 TIOA61/62/63_0 TIOB24/25/29/33/35/37/38_0 TIOB43/44/46/47/48/49_0 TIOB51/53/56/57/58/59/60_0 TIOB61/62/63_0		
Function	TEQFP144 LQFP144	TEQFP120 LQFP120	TEQFP100 LQFP100							
BaseTimer	TIOA0/1/2/3_1 TIOA14/15/16/17/18_0 TIOA21/25/26/27_1 TIOA51/57/58/59/61_0 TIOB56/57/58/59/60/61/62_0 0	TIOA0/1/2/3_1 TIOA9/10/13_1 TIOA8/14/15/16/17/18/19_0 TIOB0/5/10/12_0 TIOA27_0 TIOA21/23/25/26/27_1 TIOA51/53/56/57/58/59/60_0 TIOA61/62/63_0 TIOB24/25/29/33/37/38_0 TIOB43/48/49_0 TIOB51/56/57/58/59/60_0 TIOB61/62/63_0	TIOA0/1_0 TIOA0/1/2/3/5_1 TIOA9/10/13_1 TIOA7/8/14/15/16/17/18/19_0 TIOB0/4/5/8/10/12_0 TIOB14/15/19/22/23_0 TIOA21/26/27/28_0 TIOA21/23/25/26/27/28_1 TIOA49/51/53/56/57/58/59/60_0 TIOA61/62/63_0 TIOB24/25/29/33/35/37/38_0 TIOB43/44/46/47/48/49_0 TIOB51/53/56/57/58/59/60_0 TIOB61/62/63_0							

Page	Section	Change Results			
25	CHAPTER 2: Function List 2. Optional function 2.3. Restriction	Revised as below:			
		Error)			
		Function	TEQFP144 LQFP144	TEQFP120 LQFP120	TEQFP100 LQFP100
		FRT	TEXT6_0	TEXT0/6_0	TEXT0/2/3/6_0
		Correct)			
		Function	TEQFP144 LQFP144	TEQFP120 LQFP120	TEQFP100 LQFP100
		FRT	TEXT10_0	TEXT0/10_0	TEXT0/2/3/10_0, TEXT1/4_1

Page	Section	Change Results			
26	CHAPTER 2: Function List 2. Optional function 2.3. Restriction	Added the Functions below:			
		Correct)			
		Function	TEQFP144 LQFP144	TEQFP120 LQFP120	TEQFP100 LQFP100
		CAN-FD	-	TX0_0, RX1_1, TX1_1	TX0_0, RX1_1, TX1_1 TX2_1
		Multi-function serial	SCS21_1, SCS23_0, SCS23_1, SCS40_1, SCS41_1, SCS52_0, SIN6_1, SOT6_1, SCS70_1, SCS72_1, SCS110_0, SIN12_0, SIN12_1, SOT12_1, SCK13_0, SIN13_0, SOT13_0, SCS130_0	SCK2_0, SIN2_0, SOT2_1, SCS21_0, SCS21_1, SCS22_1, SCS23_0, SCS23_1, SOT4_1, SCS40_1, SCS41_0, SCS41_1, SCS42_0, SCS50_1, SCS52_0, SIN6_1, SOT6_1, SCS60_2, SCS61_0, SCK7_1, SIN7_0, SIN7_2, SOT7_1, SCS70_1, SCS71_0, SCS71_1, SCS72_1, SCS73_0, SCK9_0, SCS102_0, SCS110_0, SIN12_0, SIN12_1, SOT12_1, SCK13_0, SIN13_0, SOT13_0, SCS130_0	SCS0_0, SCK2_0, SIN2_0, SIN2_1, SOT2_1, SCS21_0, SCS21_1, SCS22_0, SCS22_1, SCS23_0, SCS23_1, SCS30_0, SIN4_0, SIN4_1, SOT4_1, SCS40_1, SCS41_0, SCS41_1, SCS42_0, SCS43_0, SCS43_1, SCS50_1, SCS52_0, SIN6_1, SOT6_1, SCS60_2, SCS61_0, SCK7_1, SIN7_0, SIN7_2, SOT7_1, SCS70_1, SCS71_0, SCS71_1, SCS72_1, SCS73_0, SIN8_0, SCS83_0, SCK9_0, SOT9_0, SCS90_1, SCS101_0, SCS102_0, SCS103_0, SOT11_1, SCS110_0, SCK12_0, SIN12_0, SIN12_1, SOT12_1, SCS120_1, SCK13_0, SIN13_0, SOT13_0, SCS130_0

Page	Section	Change Results																												
26, 27	CHAPTER 2: Function List 2. Optional function 2.3. Restriction	Correct) Continuation <table><thead><tr><th>Function</th><th>TEQFP144 LQFP144</th><th>TEQFP120 LQFP120</th><th>TEQFP100 LQFP100</th></tr></thead><tbody><tr><td>I²C</td><td>SCL13_0, SDA13_0</td><td>SCL2_0, SCL9_0, SCL13_0, SDA13_0</td><td>SCL2_0, SCL9_0, SDA9_0, SCL12_0, SCL13_0, SDA13_0</td></tr><tr><td>Input capture</td><td>-</td><td>IN2_1, IN2_2, IN16_1</td><td>IN2/3_0, IN0/2_1, IN0/2_2, IN19/20_0, IN16/20_1</td></tr><tr><td>Output compare</td><td>-</td><td>OUT2_0, OUT5_1, OUT20/21_0</td><td>OUT1/2/3_0, OUT2/5_1, OUT19/20/21_0</td></tr><tr><td>Quad Position & Revolution Counter</td><td>-</td><td>AIN8_0, ZIN8_0</td><td>AIN8_0, AIN8_1, ZIN8_0</td></tr><tr><td>Reload timer</td><td>-</td><td>TOT3_0, TOT16_0, TOT17_0</td><td>TOT2_0, TOT3_0, TOT16_0, TOT17_0</td></tr><tr><td>Trace</td><td>-</td><td>TRACEDATA4/5/7_0</td><td>TRACECTL_0, TRACEDATA0/1/3/4/5/7_0</td></tr></tbody></table>	Function	TEQFP144 LQFP144	TEQFP120 LQFP120	TEQFP100 LQFP100	I ² C	SCL13_0, SDA13_0	SCL2_0, SCL9_0, SCL13_0, SDA13_0	SCL2_0, SCL9_0, SDA9_0, SCL12_0, SCL13_0, SDA13_0	Input capture	-	IN2_1, IN2_2, IN16_1	IN2/3_0, IN0/2_1, IN0/2_2, IN19/20_0, IN16/20_1	Output compare	-	OUT2_0, OUT5_1, OUT20/21_0	OUT1/2/3_0, OUT2/5_1, OUT19/20/21_0	Quad Position & Revolution Counter	-	AIN8_0, ZIN8_0	AIN8_0, AIN8_1, ZIN8_0	Reload timer	-	TOT3_0, TOT16_0, TOT17_0	TOT2_0, TOT3_0, TOT16_0, TOT17_0	Trace	-	TRACEDATA4/5/7_0	TRACECTL_0, TRACEDATA0/1/3/4/5/7_0
Function	TEQFP144 LQFP144	TEQFP120 LQFP120	TEQFP100 LQFP100																											
I ² C	SCL13_0, SDA13_0	SCL2_0, SCL9_0, SCL13_0, SDA13_0	SCL2_0, SCL9_0, SDA9_0, SCL12_0, SCL13_0, SDA13_0																											
Input capture	-	IN2_1, IN2_2, IN16_1	IN2/3_0, IN0/2_1, IN0/2_2, IN19/20_0, IN16/20_1																											
Output compare	-	OUT2_0, OUT5_1, OUT20/21_0	OUT1/2/3_0, OUT2/5_1, OUT19/20/21_0																											
Quad Position & Revolution Counter	-	AIN8_0, ZIN8_0	AIN8_0, AIN8_1, ZIN8_0																											
Reload timer	-	TOT3_0, TOT16_0, TOT17_0	TOT2_0, TOT3_0, TOT16_0, TOT17_0																											
Trace	-	TRACEDATA4/5/7_0	TRACECTL_0, TRACEDATA0/1/3/4/5/7_0																											
30	CHAPTER 3: Product Description 1. Overview	The following sentences modified as below: Error) This chapter explains the product features of S6J3400 series. The description of this chapter should precede the duplicated description on platform manual. Correct) This chapter explains the product features of S6J3400 series. The description of this chapter should precede the duplicated description on Traveo™ Platform hardware manual.																												
31	CHAPTER 3: Product CHAPTER 3: Product 2.Product description	Revised as below: Error) Table 2-1 <table><tr><td>Peripherals</td><td>See function list.</td></tr></table> Correct) <table><tr><td>Peripherals</td><td>See the chapter of “Function List” on this manual.</td></tr></table>	Peripherals	See function list.	Peripherals	See the chapter of “Function List” on this manual.																								
Peripherals	See function list.																													
Peripherals	See the chapter of “Function List” on this manual.																													

Page	Section	Change Results				
31	CHAPTER 3: Product Description 2. Product description	Revised as below: Error) Table 2-1 <table><tr><td>Power Domain (PD)</td><td>See the platform manual and chapter STATE TRANSITION in detail.</td></tr></table> Correct) <table><tr><td>Power Domain (PD)</td><td>See the Traveo™ Platform hardware manual and the chapter of “State Transition” on this manual in detail.</td></tr></table>	Power Domain (PD)	See the platform manual and chapter STATE TRANSITION in detail.	Power Domain (PD)	See the Traveo™ Platform hardware manual and the chapter of “State Transition” on this manual in detail.
Power Domain (PD)	See the platform manual and chapter STATE TRANSITION in detail.					
Power Domain (PD)	See the Traveo™ Platform hardware manual and the chapter of “State Transition” on this manual in detail.					
31	CHAPTER 3: Product Description 2. Product description	Revised as below: Error) Table 2-1 <table><tr><td>Debug and Trace</td><td>See the platform manual in detail. – Standard 5-pin JTAG interface – SWD (Serial Wire Debug) interface – 16kB Embedded Trace Buffer 8-bit trace support.</td></tr></table> Correct) <table><tr><td>Debug and Trace</td><td>See the Traveo™ Platform hardware manual in detail. – Standard 5-pin JTAG interface – SWD (Serial Wire Debug) interface – 16kB Embedded Trace Buffer 8-bit trace support.</td></tr></table>	Debug and Trace	See the platform manual in detail. – Standard 5-pin JTAG interface – SWD (Serial Wire Debug) interface – 16kB Embedded Trace Buffer 8-bit trace support.	Debug and Trace	See the Traveo™ Platform hardware manual in detail. – Standard 5-pin JTAG interface – SWD (Serial Wire Debug) interface – 16kB Embedded Trace Buffer 8-bit trace support.
Debug and Trace	See the platform manual in detail. – Standard 5-pin JTAG interface – SWD (Serial Wire Debug) interface – 16kB Embedded Trace Buffer 8-bit trace support.					
Debug and Trace	See the Traveo™ Platform hardware manual in detail. – Standard 5-pin JTAG interface – SWD (Serial Wire Debug) interface – 16kB Embedded Trace Buffer 8-bit trace support.					
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31	CHAPTER 3: Product Description 2. Product description	Revised as below: Error) Table 2-1 <table><tr><td>Clock</td><td>See the platform manual in detail. CLK_CLKO (Clock Output Function) is supported.</td></tr></table> Correct) <table><tr><td>Clock</td><td>See the Traveo™ Platform hardware manual in detail. CLK_CLKO (Clock Output Function) is supported.</td></tr></table>	Clock	See the platform manual in detail. CLK_CLKO (Clock Output Function) is supported.	Clock	See the Traveo™ Platform hardware manual in detail. CLK_CLKO (Clock Output Function) is supported.
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31	CHAPTER 3: Product Description 2. Product description	Revised as below: Error) Table 2-1 <table><tr><td>Embedded CR oscillation</td><td>See the platform manual in detail. Stabilization time is as followings. – 30us for 4MHz (Fast clock) – 20us for 100kHz (Slow clock)</td></tr></table> Correct) <table><tr><td>Embedded CR oscillation</td><td>See the Traveo™ Platform hardware manual in detail. Stabilization time is as followings. – 30us for 4MHz (Fast clock) – 20us for 100kHz (Slow clock)</td></tr></table>	Embedded CR oscillation	See the platform manual in detail. Stabilization time is as followings. – 30us for 4MHz (Fast clock) – 20us for 100kHz (Slow clock)	Embedded CR oscillation	See the Traveo™ Platform hardware manual in detail. Stabilization time is as followings. – 30us for 4MHz (Fast clock) – 20us for 100kHz (Slow clock)
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31	CHAPTER 3: Product Description 2. Product description	Revised as below: Error) Table 2-1 <table><tr><td>Clock Supervisor</td><td>See the platform manual in detail. This product series doesn't support clock supervisor output port. (Related register and internal circuit is implemented.)</td></tr></table> Correct) <table><tr><td>Clock Supervisor</td><td>See the Traveo™ Platform hardware manual in detail. This product series doesn't support clock supervisor output port. (Related register and internal circuit is implemented.)</td></tr></table>	Clock Supervisor	See the platform manual in detail. This product series doesn't support clock supervisor output port. (Related register and internal circuit is implemented.)	Clock Supervisor	See the Traveo™ Platform hardware manual in detail. This product series doesn't support clock supervisor output port. (Related register and internal circuit is implemented.)
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31	CHAPTER 3: Product Description 2. Product description	Revised as below: Error) Table 2-1 <table><tr><td>Reset</td><td>See the platform manual in detail. Following resets are not mounted on this device. – INITX – SRSTX (and nSRST pin)</td></tr></table> Correct) <table><tr><td>Reset</td><td>RSTX pin + MD pin simultaneous assert INITX (Same as INITX pin input) – Occurrence factor: Simultaneously inputting “L” level to RSTX pin and inputting “L” level to MD pin – Release factor: Inputting “H” level to RSTX pin See the Traveo™ Platform hardware manual in detail. Following resets are not mounted on this device. – SRSTX (and nSRST pin)</td></tr></table>	Reset	See the platform manual in detail. Following resets are not mounted on this device. – INITX – SRSTX (and nSRST pin)	Reset	RSTX pin + MD pin simultaneous assert INITX (Same as INITX pin input) – Occurrence factor: Simultaneously inputting “L” level to RSTX pin and inputting “L” level to MD pin – Release factor: Inputting “H” level to RSTX pin See the Traveo™ Platform hardware manual in detail. Following resets are not mounted on this device. – SRSTX (and nSRST pin)
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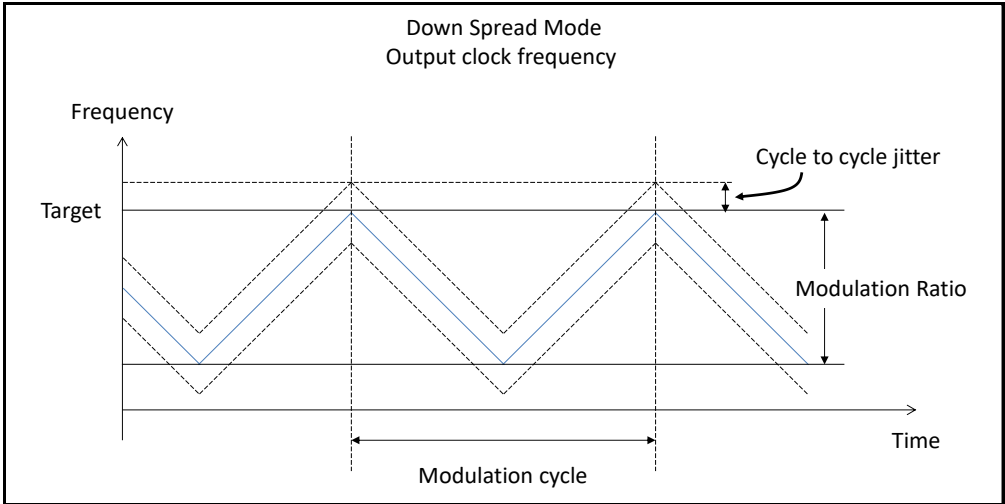
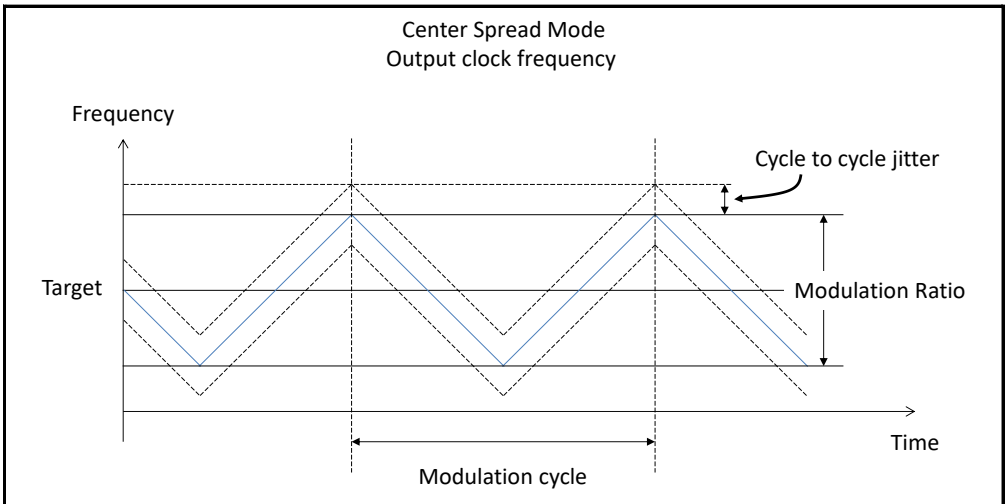
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34	CHAPTER 3: Product Description 2. Product description	Revised as below: Error) <table><tr><td>Real Time Clock (RTC) with auto-calibration</td><td>See the platform manual in detailed.</td></tr></table> Correct) <table><tr><td>Real Time Clock (RTC) with auto-calibration</td><td>See the Traveo™ Platform hardware manual in detailed.</td></tr></table>	Real Time Clock (RTC) with auto-calibration	See the platform manual in detailed.	Real Time Clock (RTC) with auto-calibration	See the Traveo™ Platform hardware manual in detailed.
Real Time Clock (RTC) with auto-calibration	See the platform manual in detailed.					
Real Time Clock (RTC) with auto-calibration	See the Traveo™ Platform hardware manual in detailed.					
34	CHAPTER 3: Product Description 2. Product description	Revised as below: Error) <table><tr><td>SHE</td><td>See the platform manual in detailed.</td></tr></table> Correct) <table><tr><td>SHE</td><td>See the Traveo™ Platform hardware manual in detailed.</td></tr></table>	SHE	See the platform manual in detailed.	SHE	See the Traveo™ Platform hardware manual in detailed.
SHE	See the platform manual in detailed.					
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34	CHAPTER 3: Product Description 2. Product description	Revised as below: Error) <table><tr><td>Source Clock Timer</td><td>See the platform manual in detailed</td></tr></table> Correct) <table><tr><td>Source Clock Timer</td><td>See the Traveo™ Platform hardware manual in detailed</td></tr></table>	Source Clock Timer	See the platform manual in detailed	Source Clock Timer	See the Traveo™ Platform hardware manual in detailed
Source Clock Timer	See the platform manual in detailed					
Source Clock Timer	See the Traveo™ Platform hardware manual in detailed					
34	CHAPTER 3: Product Description 2. Product description	Deleted as below: Error) <table><tr><td>FlexRay controller</td><td>Supports FlexRay protocol specification v2.1 Maximum 128 message buffers 8K Byte message RAM Variable length of message buffers Each message buffer can be allocated as a part of reception buffer, transmission buffer or reception FIFO Host access to the message buffer via input and output buffers Filtering for slot counter, cycle counter and channels Maskable interrupts are supported</td></tr></table>	FlexRay controller	Supports FlexRay protocol specification v2.1 Maximum 128 message buffers 8K Byte message RAM Variable length of message buffers Each message buffer can be allocated as a part of reception buffer, transmission buffer or reception FIFO Host access to the message buffer via input and output buffers Filtering for slot counter, cycle counter and channels Maskable interrupts are supported		
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44	CHAPTER 5: Clock Configuration 1. Overview	The following sentences modified as below: Error) See the chapter of the clock system before referring this chapter. Correct) See the chapter of the “Clock System” in Traveo™ Platform hardware manual before referring this chapter.																				
45	CHAPTER 5: Clock Configuration 2. Operation	Revised as below: Error) Table 2-1 <table><tr><td rowspan="4">Software watchdog timer</td><td rowspan="4">CLK_SWWD</td><td>Main clock</td><td>See Traveo™ Platform hardware manual</td></tr><tr><td>Sub clock</td><td>See Traveo™ Platform hardware manual</td></tr><tr><td>Internal CR oscillator (High frequency)</td><td>See Traveo™ Platform hardware manual</td></tr><tr><td>Internal CR oscillator (Low frequency)</td><td>See Traveo™ Platform hardware manual</td></tr></table> Correct <table><tr><td rowspan="4">Software watchdog timer</td><td rowspan="4">CLK_SWWD</td><td>Main clock</td><td>See Traveo™ Platform hardware manual</td></tr><tr><td>Sub clock</td><td>See Traveo™ Platform hardware manual</td></tr><tr><td>Internal CR oscillator (High frequency)</td><td>See Traveo™ Platform hardware manual</td></tr><tr><td>Internal CR oscillator (Low frequency)</td><td>See Traveo™ Platform hardware manual</td></tr></table>	Software watchdog timer	CLK_SWWD	Main clock	See Traveo™ Platform hardware manual	Sub clock	See Traveo™ Platform hardware manual	Internal CR oscillator (High frequency)	See Traveo™ Platform hardware manual	Internal CR oscillator (Low frequency)	See Traveo™ Platform hardware manual	Software watchdog timer	CLK_SWWD	Main clock	See Traveo™ Platform hardware manual	Sub clock	See Traveo™ Platform hardware manual	Internal CR oscillator (High frequency)	See Traveo™ Platform hardware manual	Internal CR oscillator (Low frequency)	See Traveo™ Platform hardware manual
Software watchdog timer	CLK_SWWD	Main clock			See Traveo™ Platform hardware manual																	
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		Internal CR oscillator (High frequency)	See Traveo™ Platform hardware manual																			
		Internal CR oscillator (Low frequency)	See Traveo™ Platform hardware manual																			

Page	Section	Change Results
46	CHAPTER 5:Clock Configuration 2.Operation 2.1.Spread Spectrum Clock Generator (SSCG)	Added the figures below: Correct) Target frequency of SSCG should be referred in Datasheet. ■ Down Spread Mode Figure 1: Down Spread Mode  ■ Center Spread Mode Figure 2: Center Spread Mode 

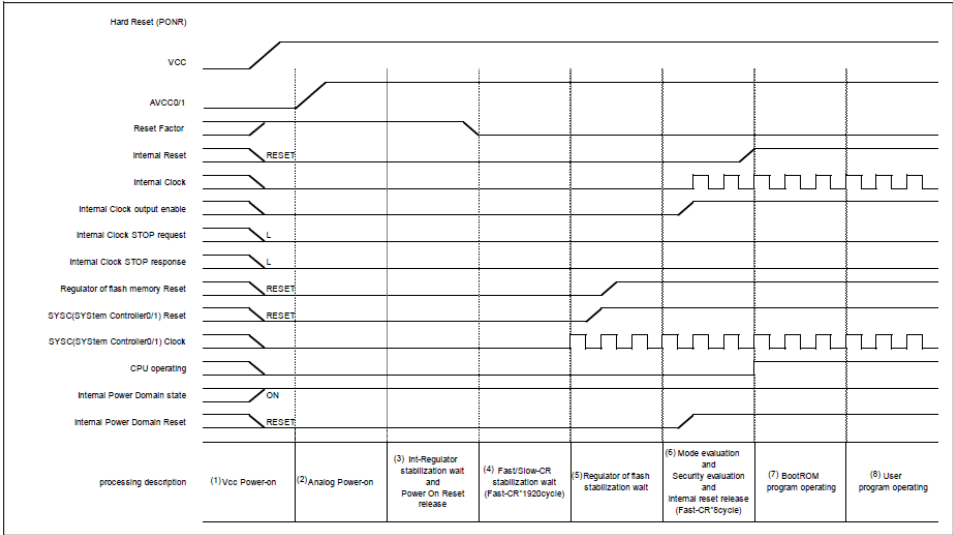
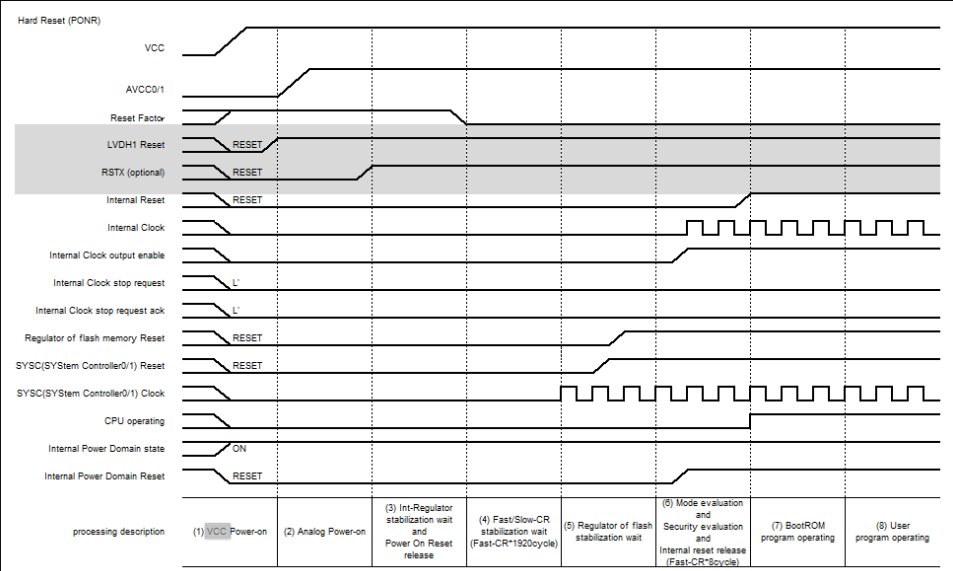
Page	Section	Change Results
47	CHAPTER 5: Clock Configuration 3. Remark	The following sentences modified as below: Error) See the chapter of clock system before referring this chapter. Correct) See the chapter of “Clock System” in Traveo™ Platform hardware manual before referring this chapter.
47	CHAPTER 5: Clock Configuration 3. Remark	The following sentences modified as below: Error) – The group name and its clock source are described in PLATFORM OVERVIEW Configuration and CLOCK SYSTEM. See Traveo™ Platform hardware manual. Correct) – The group name and its clock source are described in the chapter of “Platform Overview” Configuration and “Clock System”. See Traveo™ Platform hardware manual.
51	CHAPTER 6: Operation Mode 2. Configuration	The following sentences modified as below: Error) – <i>As for serial programming, see the chapter of SERIAL PROGRAMMING on this manual.</i> Correct) – <i>As for serial programming, see the chapter of “Serial Programming” on this manual.</i>
57	CHAPTER 7: Memory and Base Address Map 3. Base address map	Added the following sentences: Correct) An address of a certain register can be specified as below. – Base address Look for the base address X of the function from the base address map below. – Offset address Look for the offset address Y of the register from the offset address list which is described in the chapter of the function. Each function chapter has offset address list or its information. – Specify The register address can be specified as X + Y. Note: – <i>Address area of not-implemented function is not supported. See the chapter of function list.</i>

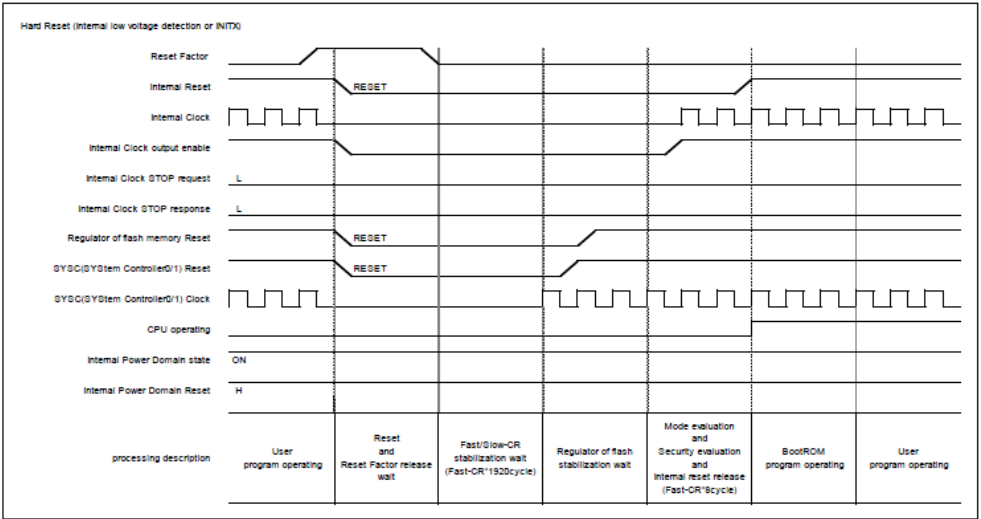
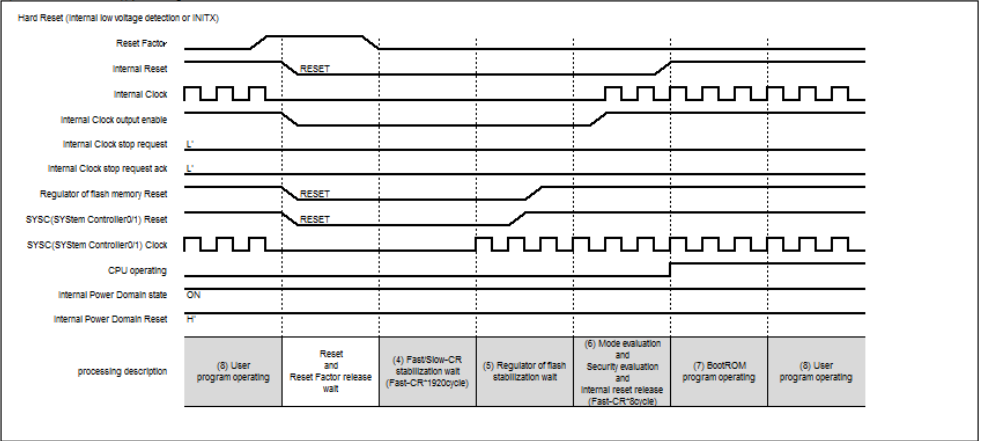
Page	Section	Change Results
65	CHAPTER 8: IRQ Map / NMI Map	The following sentences modified as below: Error) This chapter explains IRQ MAP and NMI MAP. 1.IRQ MAP 2.NMI MAP Correct) This chapter explains IRQ Map and NMI Map. 1.IRQ Map 2.NMI Map
66	CHAPTER 8: IRQ Map / NMI Map	The following title modified as below: Error) 1.IRQ MAP Correct) 1.IRQ Map
72	CHAPTER 8: IRQ Map / NMI Map 2. NMI MAP	The following title modified as below: Error) 2. NMI MAP Correct) 2. NMI Map
77	CHAPTER 9:DMA Channel Activation Factors 1. Factors list	The following sentences modified as below: Error) *1 : For assignment of source, see "RESOURCE INPUT SELECTION". Correct) *1 : For assignment of source, see the chapter of "I/O Port" on this manual.
100	CHAPTER 10: Port Description 2. Remark	The following sentences modified as below: Error) – See the function list of the product as well. Correct) – See the chapter of "Function List" on this manual as well.

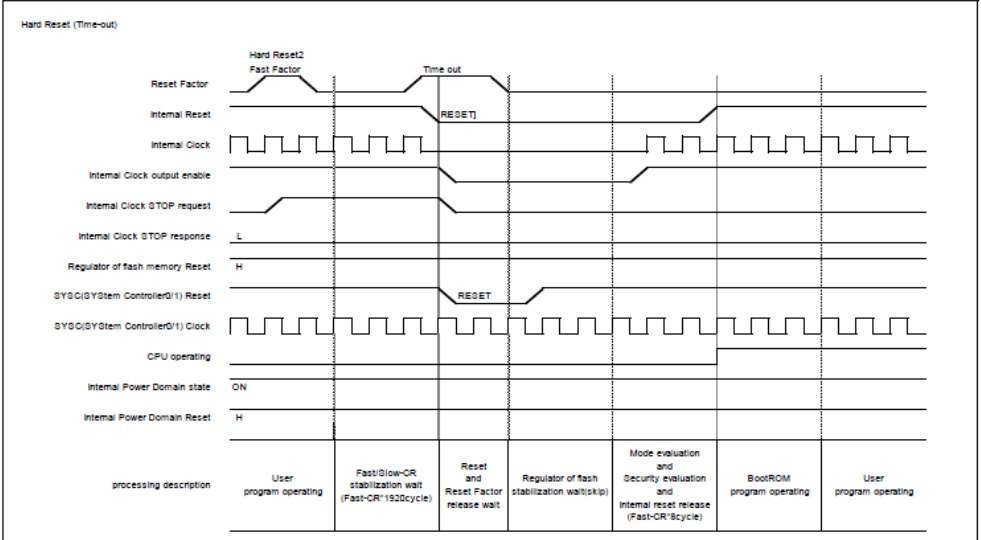
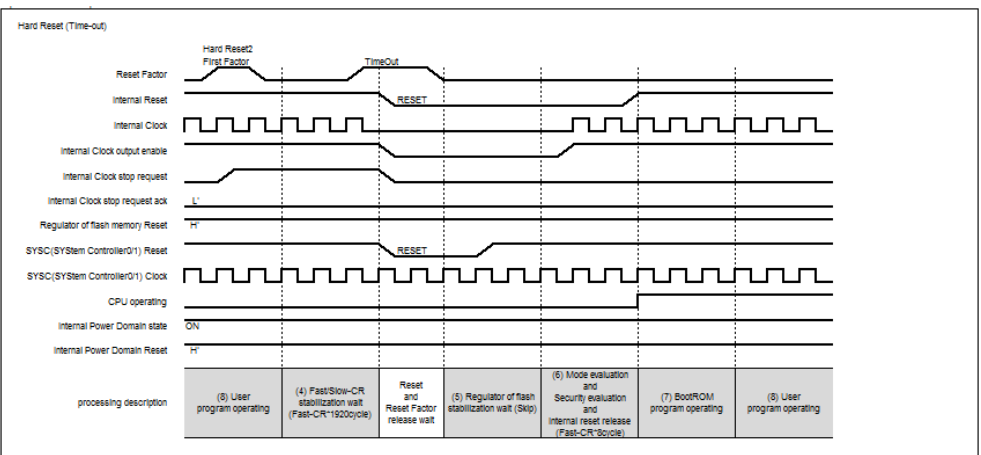
Page	Section	Change Results
102	CHAPTER 11: Port Configuration 1. Overview CHAPTER	The following sentences modified as below: Error) See the common information of the registers on the hardware manual of Traveo™ Platform. Correct) See the common information of the registers on I/O Port.
104	CHAPTER 11: Port Configuration 3. Operation 3.1. Resource input configuration	Added the following sentences: Error) The resource input configuration (RIC) is a function to select input from an external or output from another internal resource as resource input. Correct) The resource input configuration (RIC) is a function to select input from an external or output from another internal resource as resource input. A resource which supports either a port input relocation or a resource inputs.
106, 107, 108, 110, 111, 112, 114, 115, 116, 117	CHAPTER 11: Port Configuration 3.1. Resource input configuration	Revised as below: Error) SCS2 → Correct) SCS20 Error) SCS3 → Correct) SCS30 Error) SCS4 → Correct) SCS40 Error) SCS5 → Correct) SCS50 Error) SCS6 → Correct) SCS60 Error) SCS7 → Correct) SCS70 Error) SCS9 → Correct) SCS90 Error) SCS10 → Correct) SCS100 Error) SCS11 → Correct) SCS110 Error) SCS12 → Correct) SCS120
233	CHAPTER 11: Port Configuration 3. Operation 3.1. Resource input configuration	Added the following sentences: Correct) Notes: - When both GPIO_PORTEN.GPORTEN and PPC_PCFGR.PIE are configured as 0, the input signal is disconnected and external interrupt cannot be detected. During disconnecting, I/O internally outputs "low" to internal logic, and if ELVR is configured as low-level-detection, falling-edge-detection, or both-edge-detection it will be detected as external interrupt with EIRR=1. - OCUx_MODn is described as MODn pin in Traveo™ Platform hardware manual.

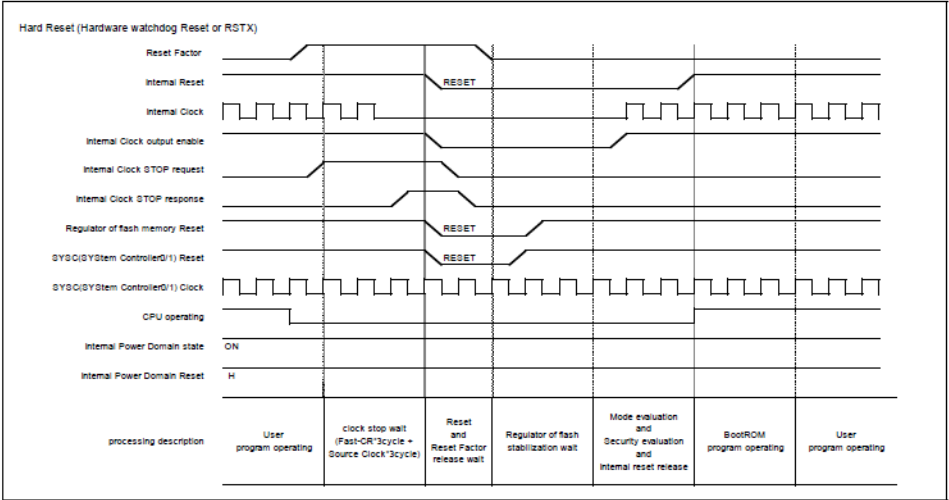
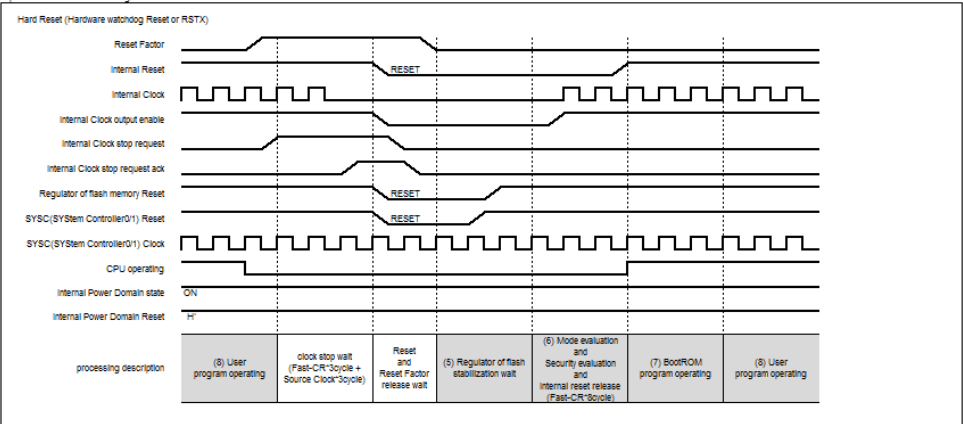
Page	Section	Change Results
234	CHAPTER 11: Port Configuration 3. Operation 3.2. Port output function configuratio	Added the following sentences: Error) The port output function configuration (POF) is a function to select a function to output to a port. Correct) The port output function configuration (POF) is a function to select a function to output to a port. A resource which supports a port output relocation has its PPC_PCFGR.POF to configure resource output.
255	CHAPTER 11: Port Configuration 3. Operation 3.6.Port Status	Added the following sentences: Correct) 3.6.1. Hi-z Control Traveo™ Platform hardware manual has description of System Special Setting Register (SYSC0_SPECIFGR). The [bit23] PSSPADCTRL: PSS-time port configuring bit should be configured as below. – 0: Do not perform Hi-z control. – 1: Perform Hi-z control. Notes: – At RUN mode, if configured as Hi-z control, it doesn't affect the port status immediately, but after executing WFI instruction to update the profile registers, then it turns out Hi-z status during PSS mode. – As opposite control from PSS to RUN, the port status of Hi-z will automatically be released without reconfiguration of SYSC0_SPECIFGR.PSSPADCTRL = 0. 3.6.2. Port Status Hold during PSS Mode All of the GPIO area can be kept the port status during PSS mode by System Special Setting Register (SYSC0_SPECIFGR). The [bit31] to [bit24] HOLDIO_PD_x: HOLD data latch bit should be configured as below. – 0: Do not retain control. – 1: Retain control. Notes: – During MCU RUN mode, I/O port status will be latched immediately after SYSC0_SPECIFGR.HOLDIO_PD_x = 1 (Retain control) configured. – After SYSC0_SPECIFGR.HOLDIO_PD_x = 1, the status of followings will be latched. Please note that PID is not included, that is, input data cannot be latched. – PPC_PCFGR_{ijj} POD, POE, PIL, PUE, PDE, ODR, NFE, and POF. (excluding PID: Input data cannot be latched) – RIC_RESIN_x.PORTSEL and RESSEL – At turning from MCU PSS mode to RUN, the latched status will not be released automatically. Configuration SYSC0_SPECIFGR.HOLDIO_PD_x = 0 should be necessary for releasing the status.

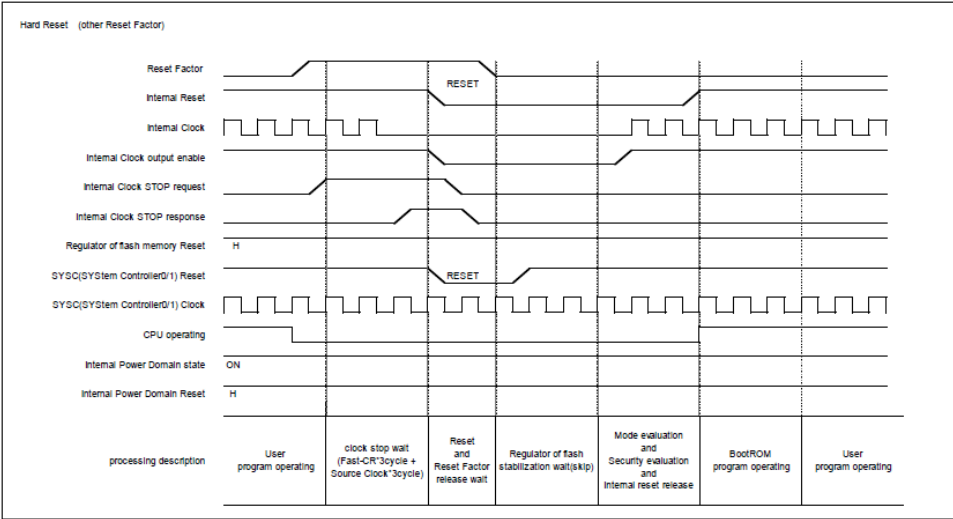
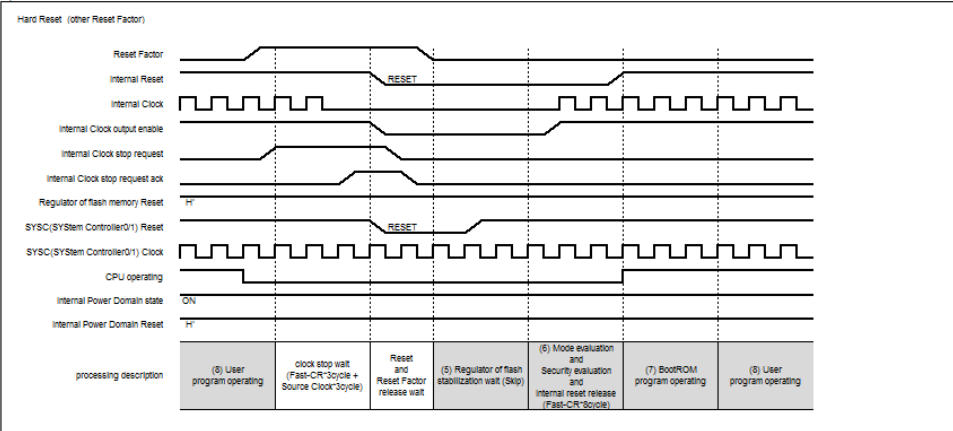
Page	Section	Change Results																																										
260	CHAPTER 11: Port Configuration 3. Operation 3.8. Key Code Register	Added Table 3-1 below: Correct) The write access to I/O Port register is protected by Key Code Register. Table 3-1 Relationship between I/O Port Register and Key Code Register <table border="1"> <thead> <tr> <th>I/O Port Register</th><th>Key Code Register</th><th>Remark</th></tr> </thead> <tbody> <tr> <td>Data Direction Register (GPIO_DDRi)</td><td>GPIO Key Code Register (GPIO_KEYCDR)</td><td>-</td></tr> <tr> <td>Data Direction Set Register (GPIO_DDSRi)</td><td>GPIO Key Code Register (GPIO_KEYCDR)</td><td>-</td></tr> <tr> <td>Data Direction Clear Register (GPIO_DDCRi)</td><td>GPIO Key Code Register (GPIO_KEYCDR)</td><td>-</td></tr> <tr> <td>Port Output Data Register (GPIO_PODRi)</td><td>-</td><td>-</td></tr> <tr> <td>Port Output Set Register (GPIO_POSRi)</td><td>-</td><td>-</td></tr> <tr> <td>Port Output Clear Register (GPIO_POCRi)</td><td>-</td><td>-</td></tr> <tr> <td>Port Input Enable Register (GPIO_PORTEN)</td><td>GPIO Key Code Register (GPIO_KEYCDR)</td><td>-</td></tr> <tr> <td>Port Input Data Register (GPIO_PIDRi)</td><td>-</td><td>-</td></tr> <tr> <td>GPIO Key Code Register (GPIO_KEYCDR)</td><td>-</td><td>-</td></tr> <tr> <td>Port Setting Register (PPC_PCFGRijj)</td><td>PPC Key Code Register (PPC_KEYCDR)</td><td>-</td></tr> <tr> <td>PPC Key Code Register (PPC_KEYCDR)</td><td>-</td><td>-</td></tr> <tr> <td>Resource Input Setting Register (RIC_RESINn)</td><td>RIC Key Code Register (RIC_KEYCDR)</td><td>-</td></tr> <tr> <td>RIC Key Code Register (RIC_KEYCDR)</td><td>-</td><td>-</td></tr> </tbody> </table>	I/O Port Register	Key Code Register	Remark	Data Direction Register (GPIO_DDRi)	GPIO Key Code Register (GPIO_KEYCDR)	-	Data Direction Set Register (GPIO_DDSRi)	GPIO Key Code Register (GPIO_KEYCDR)	-	Data Direction Clear Register (GPIO_DDCRi)	GPIO Key Code Register (GPIO_KEYCDR)	-	Port Output Data Register (GPIO_PODRi)	-	-	Port Output Set Register (GPIO_POSRi)	-	-	Port Output Clear Register (GPIO_POCRi)	-	-	Port Input Enable Register (GPIO_PORTEN)	GPIO Key Code Register (GPIO_KEYCDR)	-	Port Input Data Register (GPIO_PIDRi)	-	-	GPIO Key Code Register (GPIO_KEYCDR)	-	-	Port Setting Register (PPC_PCFGRijj)	PPC Key Code Register (PPC_KEYCDR)	-	PPC Key Code Register (PPC_KEYCDR)	-	-	Resource Input Setting Register (RIC_RESINn)	RIC Key Code Register (RIC_KEYCDR)	-	RIC Key Code Register (RIC_KEYCDR)	-	-
I/O Port Register	Key Code Register	Remark																																										
Data Direction Register (GPIO_DDRi)	GPIO Key Code Register (GPIO_KEYCDR)	-																																										
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Data Direction Clear Register (GPIO_DDCRi)	GPIO Key Code Register (GPIO_KEYCDR)	-																																										
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Port Output Set Register (GPIO_POSRi)	-	-																																										
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RIC Key Code Register (RIC_KEYCDR)	-	-																																										
261	CHAPTER 11: Port Configuration 11: Port Configuration 4. Registers	The following sentences modified as below: Error) See the common information of the registers on the hardware manual of Traveo™ Platform. Correct) See the common information of the registers on I/O Port.																																										

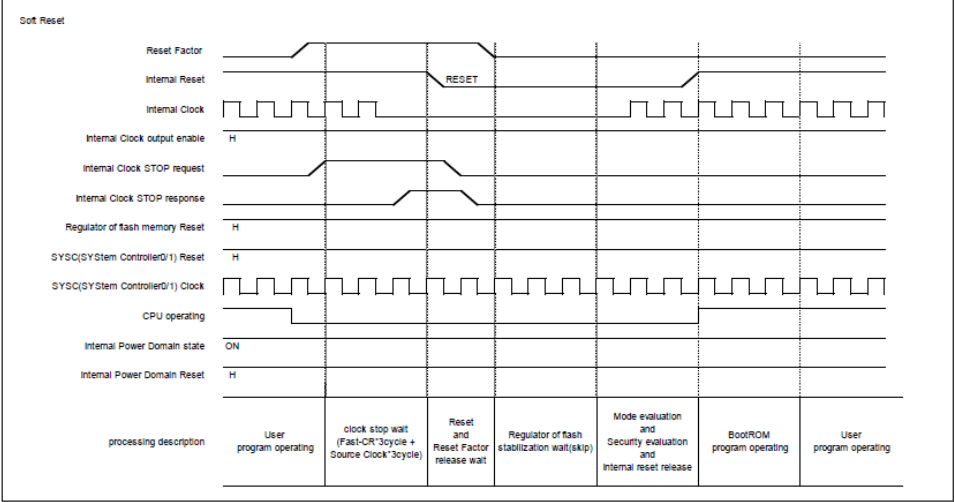
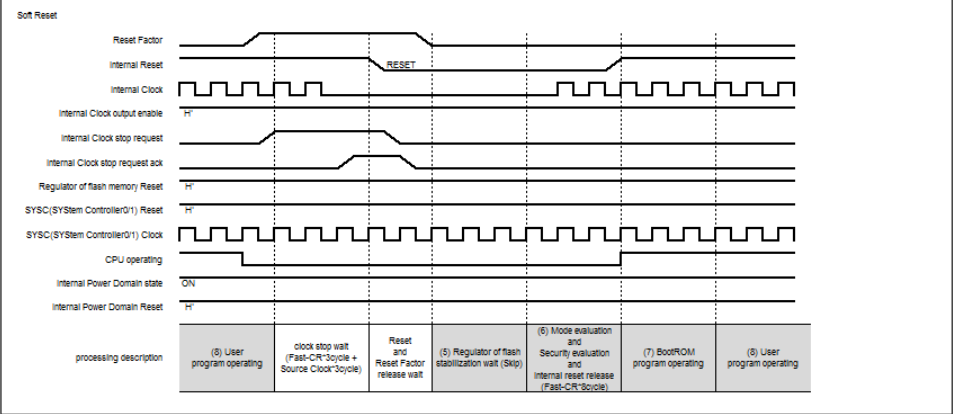
Page	Section	Change Results
264	CHAPTER 12: State Transition 1. Overview	The following sentences modified as below: Error) Refer to the low-power chapter for the detailed information for performing a change state. Correct) Refer to the chapter of "Low-power Consumption" in Traveo™ Platform hardware manual for the detailed information for performing a change state.
267	CHAPTER 12: State Transition 3. Fetching the Operation Mode	The following Figure3-1 modified as below: Error) Figure3-1 Operation Mode Fetch Timing Chart  Correct) Figure3-1 Operation Mode Fetch Timing Chart of PONR 

Page	Section	Change Results
269	CHAPTER 12: State Transition 3. Fetching the Operation Mode	The following Figure3-2 modified as below: Error) Figure3-2 Operation Mode Fetch Timing Chart  Correct) Figure3-2 Operation Mode Fetch Timing Chart of other Reset 

Page	Section	Change Results
269	CHAPTER 12: State Transition 3. Fetching the Operation Mode	The following Figure3-2 modified as below: Error)  Correct) 

Page	Section	Change Results
269	CHAPTER 12: State Transition 3. Fetching the Operation Mode	The following Figure3-2 modified as below: Error)  Correct) 

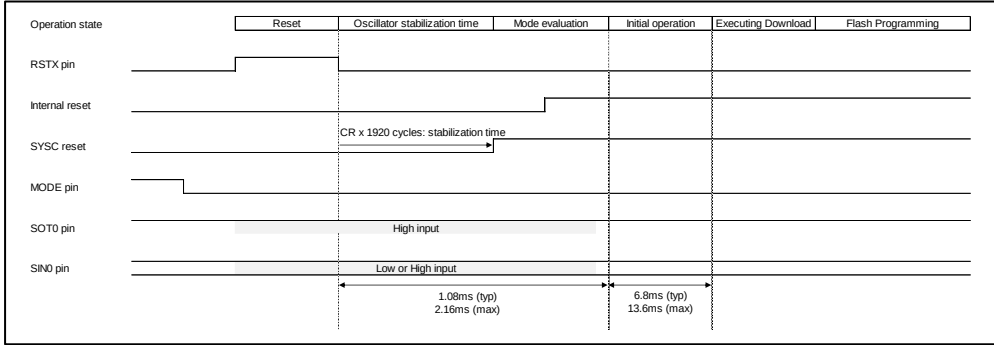
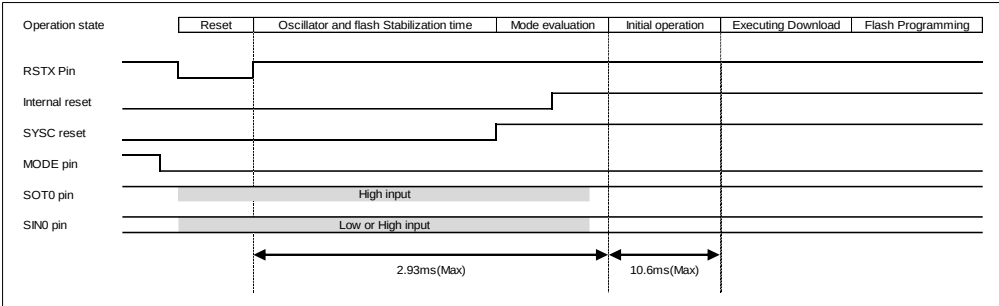
Page	Section	Change Results
270	CHAPTER 12: State Transition 3. Fetching the Operation Mode	The following Figure3-3 modified as below: Error) Figure3-3 Operation Mode Fetch Timing Chart  Correct) Figure3-3 Operation Mode Fetch Timing Chart of other Reset 

Page	Section	Change Results
270	CHAPTER 12: State Transition 3. Fetching the Operation Mode	The following Figure3-3 modified as below: Error)  Correct) 
275	CHAPTER 13: Pin Status in Each CPU State	The following title modified as below: Error) 1. PIN STATUS IN EACH CPU STATE Correct) 1. Pin Status in Each CPU State

Page	Section	Change Results
276	CHAPTER 13: Pin Status in Each CPU State 1. PIN STATUS IN EACH CPU STATE	The following title modified as below: Error) 1. PIN STATUS IN EACH CPU STATE Correct) 1. Pin Status in Each CPU State
276	CHAPTER 13: Pin Status in Each CPU State 1. PIN STATUS IN EACH CPU STATE	The following sentences modified as below: Error) *1 Please refer to "STATE TRANSITION" for the state definition of the PSS mode. Correct) *1 Please refer to the chapter of "State Transition" on this manual for the state definition of the PSS mode.
282	CHAPTER 14: Low Voltage Detection 3. Registers	Added the following sentences: Correct) [Bit30] LVDL1S Internal low-voltage detection voltage operation selection bit [Bit27:25] LVDL1V Internal low-voltage detection voltage setting bits Note: - LVDL1V will be initial value with reset. If LVDL1V is changed from initial value, LVDL1S should be configured as interrupt.
282	CHAPTER 14: Low Voltage Detection 3. Registers	Delete the following sentence: [Bit27:25] LVDL1V Internal low-voltage detection voltage setting bits Error) *: These detection voltage level settings are below the minimum operation voltage. Between these detection voltage and the minimum operation voltage, MCU functions are not guaranteed except for the low voltage detector. Note that although the detection level is below the minimum operation guarantee voltage, the LVD reset factor flag is set as the voltage drops below the detection level. Correct) *: These detection voltage level settings are below the minimum operation voltage. Between these detection voltage and the minimum operation voltage, MCU functions are not guaranteed except for the low voltage detector.

Page	Section	Change Results
283	CHAPTER 14: Low Voltage Detection 3. Registers	Added the following sentences: Correct) [Bit14] LVDH1S Internal low-voltage detection voltage operation selection bit [Bit11:9] LVDH1V External low-voltage detection voltage setting bits Note: – <i>LVDH1V will be initial value with reset. If LVDH1V is changed from initial vale, LVDH1S should be configured as interrupt.</i>
283	CHAPTER 14: Low Voltage Detection 3. Registers	Delete the following sentence: [Bit11:9] LVDH1V External low-voltage detection voltage setting bits Error) *: These detection voltage level settings are below the minimum operation voltage. Between these detection voltage and the minimum operation voltage, MCU functions are not guaranteed except for the low voltage detector. <i>Note that although the detection level is below the minimum operation guarantee voltage, the LVD reset factor flag is set as the voltage drops below the detection level.</i> Correct) *: These detection voltage level settings are below the minimum operation voltage. Between these detection voltage and the minimum operation voltage, MCU functions are not guaranteed except for the low voltage detector.
285	CHAPTER 15: Serial Programming	The following title modified as below: Error) 2. MEMORY MAP 3. FLASH SECTOR CONFIGURATION 4. PORT CONFIGURATION 5. OPERATION Correct) 2. Memory Map 3. Flash Sector Configuration 4. Port Configuration 5. Operation
287	CHAPTER 15: Serial Programming 2. MEMORY MAP	The following title modified as below: Error) 2. MEMORY MAP Correct) 2. Memory Map

Page	Section	Change Results
287	CHAPTER 15: Serial Programming 2. MEMORY MAP	The following sentences modified as below: Error) See the chapter of Memory AND BASE ADDRESS MAP on this hardware manual Correct) See the chapter of “Memory and Base Address Map” on this hardware manual
288	CHAPTER 15: Serial Programming 3. FLASH SECTOR CONFIGURA TION	The following title modified as below: Error) 3. FLASH SECTOR CONFIGURATION Correct) 3. Flash Sector Configuration
288	CHAPTER 15: Serial Programming 3. FLASH SECTOR CONFIGURA TION	The following sentences modified as below: Error) See the chapter of TCFLASH and WORKFLASH of Traveo™ Platform hardware manual Correct) See the chapter of “TCFLASH” and “WorkFLASH” of Traveo™ Platform hardware manual
289	CHAPTER 15: Serial Programming 4. PORT CONFIGURA TION	The following title modified as below: Error) 4. PORT CONFIGURATION Correct) 4. Port Configuration
289	CHAPTER 15: Serial Programming 4. PORT CONFIGURA TION	The following sentences modified as below: Error) – See the chapter of PORT DESCRIPTION for Port name. – See the PIN ASSIGNMENT on Datasheet. Correct) – See the chapter of “Port Description” on this manual for Port name. – See the “Pin Assignment” in Datasheet.

Page	Section	Change Results
290	CHAPTER 15: Serial Programming 5. OPERATION	The following title modified as below: Error) 5. OPERATION Correct) 5. Operation
290	CHAPTER 15: Serial Programming 5. OPERATION 5.1. Timing Chart	The following Figure5-1 modified as below: Error)  Correct) 
311	CHAPTER 16: Base Timer 7. Start of DMA Controller (DMAC)	The following sentences modified as below: Error) For details on DMAC settings, see the following chapters: "DMA Controller" and "INTERRUPTS". Correct) For details on DMAC settings, see the chapter of "DMA Controller" in Traveo™ Platform hardware manual and "6. Interrupts from the Base Timer" on this manual.

Page	Section	Change Results
315, 317	CHAPTER 16: Base Timer 8. Registers of the Base Timer	Revised as below: Table 8-6,8-8 Register Map Error) BT_BTSELM*2 Correct) BT_BTSELMn*2 Error) *2m = Correct) *2mn=
417	CHAPTER 17: Base Timer I/O Selection Function 2. Configuration	The following Figure2-1 modified as below: Error) BT_BTSEL01 Correct) BT_BTSELMn
424, 426	CHAPTER 17: Base Timer I/O Selection Function 4. Registers	The following Table 4-2,4-4 modified as below: Table 4-2,4-4 Register Map Error) BT_BTSELM*2 Correct) BT_BTSELMn*2 Error) *2m = Correct) *2mn=

Page	Section	Change Results
427	CHAPTER 17: Base Timer I/O Selection Function 4.1. I/O Selection Registers (BT_BTSEL)	Title was modified as follows: Error) 4.1. I/O Selection Registers (BT_BTSEL) Correct) 4.1. I/O Selection Registers(BT_BTSEL ~~mn~~)
432	CHAPTER 18: Base Timer Simultaneous Operation 1.Overview	The following sentences modified as below: Error) (Refer to CHAPTER BASE TIMER I/O SELECTION FUNCTION) Correct) (Refer to the chapter of Base Timer I/O Selection Function on this manual.)
432	CHAPTER 18: Base Timer Simultaneous Operation 1.Overview	The following sentences modified as below: Error) (Refer to CHAPTER BASE TIMER 10.1.6 External Timer Match Starting) Correct) (Refer to the chapter of Base Timer 10.2.4 External Timer Match Starting on this manual.)
433	CHAPTER 18: Base Timer Simultaneous Operation 2. Configuration	Delete the following sentence: Error) Figure 2-1 Block Diagram Refer to CHAPTER1 OVERVIEW 3.Models Available for the number of implement channels.
437	CHAPTER 18: Base Timer Simultaneous Operation 3.1. Global Time and Base Timers Operation Waveform	The following sentences modified as below: Error) (For details, refer to CHAPTER BASE TIMER) Correct) (For details, refer to the chapter of Base Timer on this manual)

Page	Section	Change Results
472	CHAPTER 18: Base Timer Simultaneous Operation 7. Precautions for Using This Device	The following sentences modified as below: Error) This register supports writing from the bit-band alias area. For the bit-band alias area, see "CHAPTER: BIT-BAND UNIT." Correct) This register supports writing from the bit-band alias area. For the bit-band alias area, see the chapter of "Bit-Band Unit" in Traveo™ Platform hardware manual.
529	CHAPTER 20: 32-Bit Input Capture 4. Precautions for Using This Device	The following sentences modified as below: Error) This register supports writing from the bit-band alias area. For the bit-band alias area, see "CHAPTER:BIT-BAND UNIT". Correct) This register supports writing from the bit-band alias area. For the bit-band alias area, see the chapter of "Bit-Band Unit" in Traveo™ Platform hardware manual.
534	CHAPTER 21: 32-bit Reload Timer 3. Operation of the 32-bit Reload Timer	The following section describes modified as below: Error) 3.4 Counter Operation 3.5 DMA Correct) 3.4. Counter Operation State 3.5. DMA Operation
553	CHAPTER 22: I/O Port 2. Configuration and Block Diagrams	Added the following sentences: Correct) "GPIO_PPERi" is not supported.
561	CHAPTER 22: I/O Port 3. Setting Procedure Examples	The following sentences modified as below: Error) – For details on resource input selection, see "Resource input configuration of PORT CONFIGURATION " Correct) – For details on resource input selection, see "Resource input configuration" of the chapter of "Port Configuration " on this manual.

Page	Section	Change Results
567	CHAPTER 22: I/O Port 4.2. Data Direction Set Register (GPIO_DDSRi)	Added the following sentences: Correct) Notes: - This is the applicable key code register. To write to this register, the GPIO key code register (GPIO_KEYCDR) must be set. - If this register is written before the key code is released, a bus error response is returned. - After key code release, writing to a different address or using a different access size than specified in the key code sequence will not generate an error response, and it can't write the data correctly. - Please be sure to read and check a preset value after writing to a GPIO register.
575, 580,	CHAPTER 22: I/O Port 4. Register List 4.9. GPIO Key Code Register (GPIO_KEYCDR)	The following sentences modified as below: Error) - <i>There is no effect on the key code protection release process even if registers other than this register and the applicable key code register that is in the release processing (the register set by the RADA) are accessed while writing the key code 0b00, 0b01, 0b10, and 0b11.</i> Correct)
584	CHAPTER 22: I/O Port 4. Register List 4.11. PPC Key Code Register (PPC_KEYCDR) CHAPTER 22: I/O Port 4. Register List 4.13. RIC Key Code Register (RIC_KEYCDR)	- <i>There is no effect on the key code protection release process even if registers other than this register and the applicable key code register that is in the release processing (the register set by the RADR) are accessed while writing the key code 0b00, 0b01, 0b10, and 0b11.</i>

Page	Section	Change Results
576	CHAPTER 22: I/O Port 4. Register List 4.10. Port Setting Register (PPC_PCFG Rijj) (i = 0 to (product specification) , jj = 00 to 31)	The following sentences modified as below: Error) [bit14] POD: Port Output Data Bit This bit indicates the value outputted to a pin. This bit is enabled only when the port output enable bit (POE) is "1". [bit13] PID: Port Input Data Bit This bit indicates the value inputted to the pin selected by the input level bit (PIL[1:0]). This bit is indefinite when the global input enable bit (GPIO_GPORTEN) is "0". Correct) [bit14] POD: Port Output Data Bit This bit indicates the value outputted to a pin. [bit13] PID: Port Input Data Bit This bit indicates the value inputted to the pin selected by the input level bit (PIL[1:0]). This bit is indefinite when the global input enable bit (GPORTEN) is "0".
577	CHAPTER 22: I/O Port 4.10 Port Setting Register (PPC_PCFG Rijj)	The following sentences modified as below: Error) For details, see " Input Level Setting of PORT CONFIGURATION ". Correct) For details, see " Input Level Setting" of the chapter of "Port Configuration" on this manual.
577	CHAPTER 22: I/O Port 4.10 Port Setting Register (PPC_PCFG Rijj)	The following sentences modified as below: Error) For details, see " Output Drive Capacity Setting of PORT CONFIGURATION ". Correct) For details, see " Output Drive Capacity Setting of the chapter of "Port Configuration" on this manual.
578	CHAPTER 22: I/O Port 4.10 Port Setting Register (PPC_PCFG Rijj)	The following sentences modified as below: Error) For details, see " Port output function configuration of PORT CONFIGURATION ". Correct) For details, see " Port output function configuration of the chapter of "Port Configuration" on this manual.

Page	Section	Change Results
581	CHAPTER 22: I/O Port 4.12. Resource Input Setting Resister (RIC_RESIN n)	The following sentences modified as below: Error) For details, see " Resource input configuration of PORT CONFIGURATION ". Correct) For details, see " Resource input configuration of the chapter of "Port Configuration" on this manual.
683	CHAPTER 23: 12/10/8-Bit Analog to Digital Converter	The following sentences modified as below: Error) For details on A/D Converter Offset value, see the following section "4.3. A/D Conversion Offset Compensation value Select Register " in "CHAPTER: 37 PARTIAL WAKEUP CONTROL". Correct) For details on A/D Converter Offset value, see the following section "4.3. A/D Conversion Offset Compensation value Select Register" in the chapter of "Partial Wakeup Control" on this manual.
702	CHAPTER 24: Partial Wakeup Control	The following sentences modified as below: Error) – In PWU mode, only the range comparison function of the A/D converter can be used. For details, see "CHAPTER 36: 12/10/8-BIT ANALOG TO DIGITAL CONVERTER." Correct) – In PWU mode, only the range comparison function of the A/D converter can be used. For details, see the chapter of "12/10/8-BIT Analog To Digital Converter" on this manual.
703	CHAPTER 24: Partial Wakeup Control	The following sentences modified as below: Error) For details, see "CHAPTER 24:4. Registers." Correct) For details, see the chapter of "Partial Wakeup Control 4. Registers" on this manual.
704	CHAPTER 24: Partial Wakeup Control	The following sentences modified as below: Error) For details, see "CHAPTER 24:4.3. A/D Conversion Offset Compensation value Select Registers". Correct) For details, see the chapter of "Partial Wakeup Control 4.3. A/D Conversion Offset Compensation value Select Registers" on this manual.

Page	Section	Change Results
707	CHAPTER 24: Partial Wakeup Control	The following sentences modified as below: Error) For the setting method for the above, see "CHAPTER 10: CR CALIBRATION." Correct) For the setting method for the above, see the chapter of "CR Calibration" in Traveo™ Platform hardware manual.
707	CHAPTER 24: Partial Wakeup Control	The following sentences modified as below: Error) For the setting method for the above, see "CHAPTER 8: SOURCE CLOCK TIMER." Correct) For the setting method for the above, see the chapter of "Source Clock Timer" in Traveo™ Platform hardware manual.
707	CHAPTER 24: Partial Wakeup Control	The following sentences modified as below: Error) For a corresponding register and setting, see " CHAPTER 11: PORT CONFIGURATION." Correct) For a corresponding register and setting, see the chapter of "Port Configuration" on this manual.
708	CHAPTER 24: Partial Wakeup Control	The following sentences modified as below: Error) For a detailed explanation of the registers and the setting method, see "CHAPTER 36: 12/10/8-BIT ANALOG TO DIGITAL CONVERTER." Correct) For a detailed explanation of the registers and the setting method, see the chapter of "12/10/8-Biy Analog To Digital Converter" on this manual.
709	CHAPTER 24: Partial Wakeup Control	The following sentences modified as below: Error) For details and notes on the settings, see "CHAPTER 36: 12/10/8-BIT ANALOG TO DIGITAL CONVERTER." Correct) For details and notes on the settings, see the chapter of "12/10/8-Bit Analog To Digital Converter" on this manual.

Page	Section	Change Results
709	CHAPTER 24: Partial Wakeup Control	The following sentences modified as below: Error) For details and notes on the settings, see "CHAPTER 36: 12/10/8-BIT ANALOG TO DIGITAL CONVERTER." Correct) For details and notes on the settings, see the chapter of "12/10/8-Bit Analog To Digital Converter" on this manual.
710	CHAPTER 24: Partial Wakeup Control	The following sentences modified as below: Error) For details and notes on the settings, see "CHAPTER 36: 12/10/8-BIT ANALOG TO DIGITAL CONVERTER." Correct) For details and notes on the settings, see the chapter of "12/10/8-Bit Analog To Digital Converter" on this manual.
710	CHAPTER 24: Partial Wakeup Control	The following sentences modified as below: Error) For details and notes on the settings, see "CHAPTER 36: 12/10/8-BIT ANALOG TO DIGITAL CONVERTER." Correct) For details and notes on the settings, see the chapter of "12/10/8-Bit Analog To Digital Converter" on this manual.
712	CHAPTER 24: Partial Wakeup Control	The following sentences modified as below: Error) For the method of setting the above, see "CHAPTER 24.4. Registers" in this chapter. Correct) For the method of setting the above, see the chapter of "Partial Wakeup Control 4. Registers" on this manual.

Page	Section	Change Results
712	CHAPTER 24: Partial Wakeup Control	The following sentences modified as below: Error) For a detailed explanation of the registers and the setting method, see "CHAPTER 14: LOW-POWER CONSUMPTION." Correct) For a detailed explanation of the registers and the setting method, see the chapter Low-Power Consumption" in Traveo™ Platform hardware manual.
715	CHAPTER 24: Partial Wakeup Control	The following sentences modified as below: Error) For details on the setting method, see "CHAPTER 9:REAL-TIME CLOCK." Correct) For details on the setting method, see the chapter "Real-Time Clock" in Traveo™ Platform hardware manual.
717	CHAPTER 24: Partial Wakeup Control	The following sentences modified as below: Error) For details on how to use the clock gear down function, see the "Clock Gear" section in "CHAPTER 4:CLOCK SYSTEM." Correct) For details on how to use the clock gear down function, see the "Clock Gear" section in the chapter of "Clock System" in Traveo™ Platform hardware manual.
718	CHAPTER 24: Partial Wakeup Control	The following sentences modified as below: Error) see "Profile" in "CHAPTER 5: LOW-POWER CONSUMPTION". Correct) see "Profile" in the chapter of "Low-Power Consumption" in Traveo™ Platform hardware manual.
718	CHAPTER 24: Partial Wakeup Control	The following sentences modified as below: Error) See "Operation Procedure" in "CHAPTER 5: LOW-POWER CONSUMPTION," and transition to PSS mode. Correct) See "Operation Procedure" in the chapter of "Low-Power Consumption" in Traveo™ Platform hardware manual and transition to PSS mode.

Page	Section	Change Results
720	CHAPTER 24: Partial Wakeup Control	The following sentences modified as below: Error) See "Operation Procedure" in "CHAPTER 5: LOW-POWER CONSUMPTION," Correct) See "Operation Procedure" in the chapter of "Low-Power Consumption" in Traveo™ Platform hardware manual
721	CHAPTER 24: Partial Wakeup Control	The following sentences modified as below: Error) For a detailed explanation of the A/D Channel Trigger Status flags, see "CHAPTER 36: 12/10/8-BIT ANALOG TO DIGITAL CONVERTER". Correct) For a detailed explanation of the A/D Channel Trigger Status flags, see the chapter of "12/10/8-Bit Analog To Digital Converter" on this manual.
728	CHAPTER 24: Partial Wakeup Control	The following sentences modified as below: Error) For details, see "CHAPTER 36: 12/10/8-BIT ANALOG TO DIGITAL CONVERTER Correct) For details, see the chapter of "12/10/8-Bit Analog To Digital Converter" on this manual.
729	CHAPTER 24: Partial Wakeup Control	The following sentences modified as below: Error) For details on the combination of violation settings, see "Profile" in "CHAPTER 5: LOW-POWER CONSUMPTION". Correct) For details on the combination of violation settings, see "Profile" in the chapter of "Low-Power Consumption" in Traveo™ Platform hardware manual.
729	CHAPTER 24: Partial Wakeup Control	The following sentences modified as below: Error) For details on the setting procedure examples of the software watchdog timer, see " Example of set procedure" in "CHAPTER 14: SOFTWARE WATCHDOG TIMER." Correct) For details on the setting procedure examples of the software watchdog timer, see " Example of set procedure" in the chapter of "Software Watchdog Timer" in Traveo™ Platform hardware manual.

Page	Section	Change Results
747	CHAPTER 25: Programmable CRC 4. Registers 4.4. CRC Configuration Register (CRCn_CFG)	Revised as below: (Error) LEN[4] R/W (Correct) LEN[4] R/W

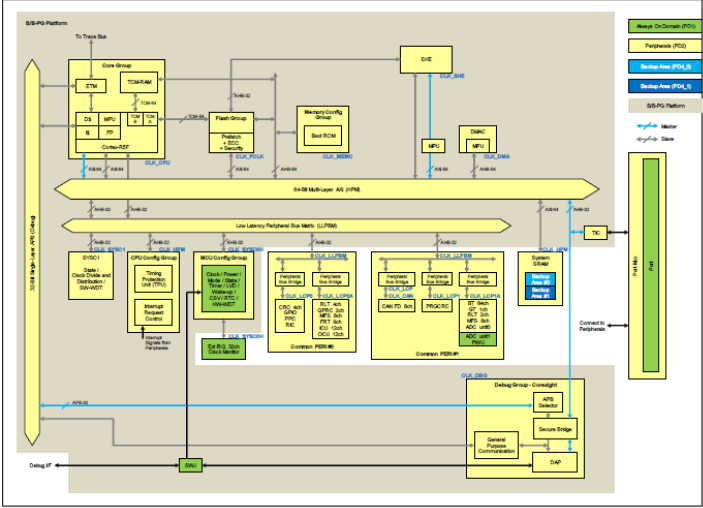
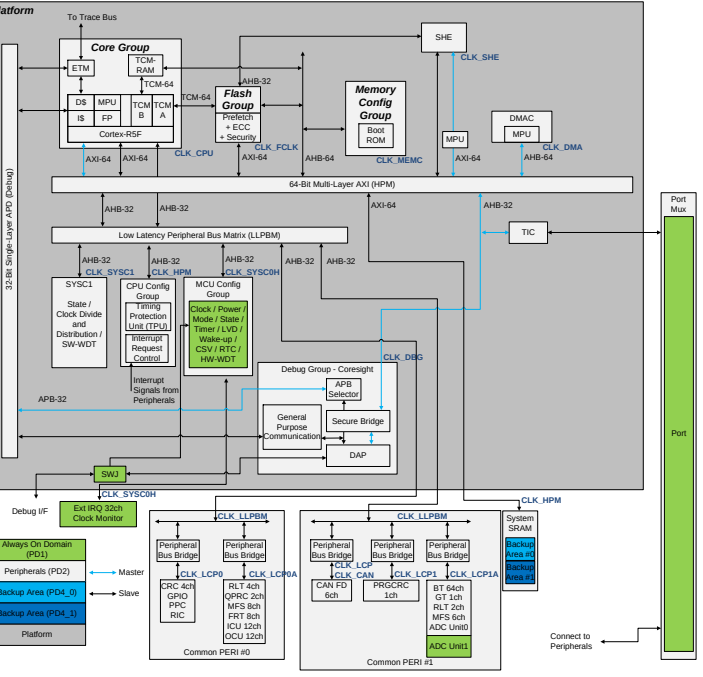
Page	Section	Change Results																																																					
Rev. *C																																																							
-	CHAPTER 24: Partial Wakeup Control	Deleted the CHAPTER 24																																																					
21	CHAPTER 2: Function List 1. Function list	Deleted the below of Table 1-1 <table><tr><td>Function</td><td colspan="4"></td><td>Remark</td></tr><tr><td></td><td>S6J34xxJxx</td><td>S6J34xxHxx</td><td>S6J34xxGxx</td><td>S6J34xxFxx</td><td></td></tr><tr><td>Partial Wake Up</td><td>analog input 8ch</td><td>analog input 8ch</td><td>analog input 8ch</td><td>analog input 7ch</td><td>Trigger 1ch</td></tr></table>	Function					Remark		S6J34xxJxx	S6J34xxHxx	S6J34xxGxx	S6J34xxFxx		Partial Wake Up	analog input 8ch	analog input 8ch	analog input 8ch	analog input 7ch	Trigger 1ch																																			
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Partial Wake Up	analog input 8ch	analog input 8ch	analog input 8ch	analog input 7ch	Trigger 1ch																																																		
22	CHAPTER 2: Function List 2.1. Basic option	Revised the Figure 2-1: Error) <table><tr><td rowspan="2">Digit</td><td colspan="2">Flash</td><td colspan="2">RAM</td></tr><tr><td>Program</td><td>Work</td><td>Main</td><td>Buck up</td></tr><tr><td>A</td><td>1,088 KB</td><td>112 KB</td><td>128 KB</td><td>8+4 KB</td></tr><tr><td>9</td><td>832 KB</td><td>112 KB</td><td>80 KB</td><td>8+4 KB</td></tr><tr><td>8</td><td>576 KB</td><td>112 KB</td><td>64 KB</td><td>8+4 KB</td></tr></table> Correct) <table><tr><td rowspan="2">Digit</td><td colspan="2">Flash</td><td colspan="3">RAM</td></tr><tr><td>Program</td><td>Work</td><td>TCRAM</td><td>SysRAM</td><td>Buck up</td></tr><tr><td>A</td><td>1,088 KB</td><td>112 KB</td><td>64 KB</td><td>64 KB</td><td>8+4 KB</td></tr><tr><td>9</td><td>832 KB</td><td>112 KB</td><td>32 KB</td><td>48 KB</td><td>8+4 KB</td></tr><tr><td>8</td><td>576 KB</td><td>112 KB</td><td>32 KB</td><td>32 KB</td><td>8+4 KB</td></tr></table>	Digit	Flash		RAM		Program	Work	Main	Buck up	A	1,088 KB	112 KB	128 KB	8+4 KB	9	832 KB	112 KB	80 KB	8+4 KB	8	576 KB	112 KB	64 KB	8+4 KB	Digit	Flash		RAM			Program	Work	TCRAM	SysRAM	Buck up	A	1,088 KB	112 KB	64 KB	64 KB	8+4 KB	9	832 KB	112 KB	32 KB	48 KB	8+4 KB	8	576 KB	112 KB	32 KB	32 KB	8+4 KB
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8	576 KB	112 KB	32 KB	32 KB	8+4 KB																																																		
25	CHAPTER 2: Function List 2.3. Restriction	Deleted PartialWakeUp of Table 2-1 Error) <table><tr><td>Function</td><td>TEQFP144 LQFP144</td><td>TEQFP120 LQFP120</td><td>TEQFP100 LQFP100</td></tr><tr><td>PartialWakeUp</td><td>PWUTRG_0</td><td>PWUTRG_0</td><td>PWU_AN7 PWUTRG_0</td></tr></table>	Function	TEQFP144 LQFP144	TEQFP120 LQFP120	TEQFP100 LQFP100	PartialWakeUp	PWUTRG_0	PWUTRG_0	PWU_AN7 PWUTRG_0																																													
Function	TEQFP144 LQFP144	TEQFP120 LQFP120	TEQFP100 LQFP100																																																				
PartialWakeUp	PWUTRG_0	PWUTRG_0	PWU_AN7 PWUTRG_0																																																				

Page	Section	Change Results																
30	CHAPTER 3: Product Description 2. Product description	Revised the Table 2-1 below: Error) <table><tr><th>Feature</th><th>Description</th></tr><tr><td>Partial wakeup</td><td>Partial wakeup function is mounted. This mode is one of the PSS modes.</td></tr></table> Correct) <table><tr><th>Feature</th><th>Description</th></tr><tr><td>Partial wakeup</td><td>This product series doesn't support Partial wakeup function.</td></tr></table>	Feature	Description	Partial wakeup	Partial wakeup function is mounted. This mode is one of the PSS modes.	Feature	Description	Partial wakeup	This product series doesn't support Partial wakeup function.								
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34	CHAPTER 3: Product Description 3. Note	Revised as below: 3.3. Register Initial Value Error) <table><tr><th>Register</th><th>Bit</th><th>Initial Value</th><th>Description</th></tr><tr><td>SYSC0_APPLVDCFGR</td><td>LVDH1S</td><td>0</td><td>-</td></tr></table> Correct) <table><tr><th>Register</th><th>Bit</th><th>Initial Value</th><th>Description</th></tr><tr><td>SYSC0_APPLVDCFGR</td><td>LVDH1S</td><td>0</td><td>LVDH1 need to be used as Reset function. LVDH1S must not be changed by Initial value.</td></tr></table>	Register	Bit	Initial Value	Description	SYSC0_APPLVDCFGR	LVDH1S	0	-	Register	Bit	Initial Value	Description	SYSC0_APPLVDCFGR	LVDH1S	0	LVDH1 need to be used as Reset function. LVDH1S must not be changed by Initial value.
Register	Bit	Initial Value	Description															
SYSC0_APPLVDCFGR	LVDH1S	0	-															
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34	CHAPTER 3: Product Description 3. Note	Revised as below: 3.3. Register Initial Value Error) <table><tr><th>Register</th><th>Bit</th><th>Initial Value</th><th>Description</th></tr><tr><td>SYSC0_STSLVDCFGR</td><td>LVDH1S</td><td>0</td><td>-</td></tr></table> Correct) <table><tr><th>Register</th><th>Bit</th><th>Initial Value</th><th>Description</th></tr><tr><td>SYSC0_STSLVDCFGR</td><td>LVDH1S</td><td>0</td><td>LVDH1 need to be used as Reset function. LVDH1S must not be changed by Initial value.</td></tr></table>	Register	Bit	Initial Value	Description	SYSC0_STSLVDCFGR	LVDH1S	0	-	Register	Bit	Initial Value	Description	SYSC0_STSLVDCFGR	LVDH1S	0	LVDH1 need to be used as Reset function. LVDH1S must not be changed by Initial value.
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Register	Bit	Initial Value	Description															
SYSC0_STSLVDCFGR	LVDH1S	0	LVDH1 need to be used as Reset function. LVDH1S must not be changed by Initial value.															

Page	Section	Change Results			
34	CHAPTER 3: Product Description 3. Note	Revised as below:			
		3.3. Register Initial Value Error)			
		Register	Bit	Initial Value	Description
		SYSC0_PSSLVDCFGR	LVDH1S	0	1 should be written only if LVDH1V is changed from initial value
		Correct)			
		Register	Bit	Initial Value	Description
SYSC0_PSSLVDCFGR	LVDH1S	0	LVDH1 need to be used as Reset function. LVDH1S must not be changed by Initial value.		
35	CHAPTER 3: Product Description 3. Note	Revised as below:			
		3.3. Register Initial Value Error)			
		Register	Bit	Initial Value	Description
		SYSC0_RUNLVDCFGR	LVDH1S	0	1 should be written only if LVDH1V is changed from initial value
		Correct)			
		Register	Bit	Initial Value	Description
SYSC0_RUNLVDCFGR	LVDH1S	0	LVDH1 need to be used as Reset function. LVDH1S must not be changed by Initial value.		
35	CHAPTER 3: Product Description 3. Note	Added following Restriction:			
		3.4. Restriction			
		Function	Related Register and Configuration	Restriction	Remark
		Low-power Consumption	SYSC0_STSLVDCFGR LVDH1S bit	Set SYSC0_STSLVDCFGR.LVDH1S = 0. LVDH1 need to be used as Reset function.	-
			SYSC0_SPECFGR EXVRSTCNT bit	Set SYSC0_SPECFGR.EXVRSTCNT = 0. External power supply control need to be reset by LVDH1.	-
			SYSC0_PSSCKSRER	Do not disable FastCR (4MHz) in PSS mode (PD2: ON/OFF).	-

Page	Section	Change Results			
36	CHAPTER 3: Product Description 3. Note	Added following Restriction:			
		3.4. Restriction			
		Function	Related Register and Configuration	Restriction	Remark
		Reset	-	All RAM data (include TCRAM, System RAM, Backup RAM) are not guaranteed after release of RSTX pin input reset.	-
			SYSC_RSTCAUSEUR SWDR bit	SWDR (Software Watchdog Reset Detection) flag of SYSC_RSTCAUSEUR (User Reset Factor Register) is set when a reset from one of the following reset is asserted in PSS mode (PD2:OFF).. In this case please ignore SWDR = 1. - RAM retention low-voltage detection reset (RVD) - INITX (INITX) - Illegal mode detection reset (IMR) - Internal power supply low-voltage detection reset (LVDL1R) - External power supply low-voltage detection reset (LVDH1R) - Hardware watchdog reset (HWDR)	-
		Clock system	SYSC_CKOTCNTR CKSEL bit	Do not set SYSC_CKOTCNTR.CKSEL[3:0] = 0011. Sub clock do not use to the source clocks.	-
		Partial Wakeup Control	-	This product series doesn't support Partial wakeup function.	-
		Real Time Clock	-	All RTC registers are not initialized by RSTX(external reset), and there are possibilities that the RTC registers are overwritten. The RTC registers need setting after release of RSTX again.	-

Page	Section	Change Results			
36	CHAPTER 3: Product Description 3. Note	Added following Restriction:			
		3.4. Restriction			
		Function	Related Register and Configuration	Restriction	Remark
		Security	TCFCFG0_CSWP0.SWP0 to SWP31 bit TCFCFG0_CSWP1to8.SWP0 to SWP31 bit	In order to write successfully any sector of Code Flash, all Sectors must have their SWP (TCFCFG0_CSWP0.SWP0 to SWP31 , TCFCFG0_CSWP1.SWP0 to SWP31) set to 1.	-

Page	Section	Change Results
38	CHAPTER 4: Block Diagram 1. Block diagram	The following Figure1-1 modified as below: Error)  Correct) 

Page	Section	Change Results																																																																						
59	CHAPTER 7: Memory and Base Address Map 3. Base address map	Revised the START Address as below: Error) <table><tr><th>START Address</th><th>END Address</th><th>Group</th><th>Function</th><th>PPU_No</th></tr><tr><td>B485_0400</td><td>B485_07FF</td><td>Reserved</td><td>Reserved</td><td>-</td></tr><tr><td>B486_0800</td><td>B487_FFFF</td><td>Reserved</td><td>Reserved</td><td>-</td></tr><tr><td>B488_0000</td><td>B488_03FF</td><td>Common PERI #1</td><td>M.F.Serial ch.8</td><td>184</td></tr></table> Correct) <table><tr><th>START Address</th><th>END Address</th><th>Group</th><th>Function</th><th>PPU_No</th></tr><tr><td>B485_0400</td><td>B485_07FF</td><td>Reserved</td><td>Reserved</td><td>-</td></tr><tr><td>B485_0800</td><td>B487_FFFF</td><td>Reserved</td><td>Reserved</td><td>-</td></tr><tr><td>B488_0000</td><td>B488_03FF</td><td>Common PERI #1</td><td>M.F.Serial ch.8</td><td>184</td></tr></table>	START Address	END Address	Group	Function	PPU_No	B485_0400	B485_07FF	Reserved	Reserved	-	B486_0800	B487_FFFF	Reserved	Reserved	-	B488_0000	B488_03FF	Common PERI #1	M.F.Serial ch.8	184	START Address	END Address	Group	Function	PPU_No	B485_0400	B485_07FF	Reserved	Reserved	-	B485_0800	B487_FFFF	Reserved	Reserved	-	B488_0000	B488_03FF	Common PERI #1	M.F.Serial ch.8	184																														
START Address	END Address	Group	Function	PPU_No																																																																				
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72 to 75	CHAPTER 9: DMA Channel Activation Factors 1. Factors list	Revised the Factors list as below: Error) <table><tr><th rowspan="2">Number of channels</th><th colspan="6">Peripheral functions</th><th rowspan="2">Remarks</th></tr><tr><th>Combination 0</th><th>Combination 1</th><th>Combination 2</th><th>Combination 3</th><th>Combination 4</th><th>Combination 5</th></tr><tr><td>0 to 8</td><td colspan="6">Reserved</td><td></td></tr><tr><td>9</td><td>WORK FLASH</td><td></td><td></td><td></td><td></td><td></td><td></td></tr></table> Correct) <table><tr><th rowspan="2">client number</th><th colspan="6">Peripheral functions</th><th rowspan="2">Remarks</th></tr><tr><th>Combination 0</th><th>Combination 1</th><th>Combination 2</th><th>Combination 3</th><th>Combination 4</th><th>Combination 5</th></tr><tr><td>0 to 8</td><td colspan="6">Reserved</td><td></td></tr><tr><td>9</td><td>WORK FLASH</td><td></td><td></td><td></td><td></td><td></td><td>*2</td></tr></table> *2 : DSTP_ACK function is set by DMAi_CMCICm:BEHSTPACK.	Number of channels	Peripheral functions						Remarks	Combination 0	Combination 1	Combination 2	Combination 3	Combination 4	Combination 5	0 to 8	Reserved							9	WORK FLASH							client number	Peripheral functions						Remarks	Combination 0	Combination 1	Combination 2	Combination 3	Combination 4	Combination 5	0 to 8	Reserved							9	WORK FLASH						*2										
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9	WORK FLASH						*2																																																																	
81	CHAPTER 10:Port Description 1. Port description list	Deleted the below of Port description list <table><tr><th rowspan="2">Port name</th><th rowspan="2">Description</th><th colspan="4">Pin No. of Package</th></tr><tr><th>TEQFP 100</th><th>TEQFP 120</th><th>TEQFP 144</th><th>TEQFP 176</th></tr><tr><td>PWU_AN0</td><td>Partial wakeup ADC analog 0 input pin</td><td>54</td><td>66</td><td>78</td><td>97</td></tr><tr><td>PWU_AN1</td><td>Partial wakeup ADC analog 1 input pin</td><td>55</td><td>67</td><td>79</td><td>98</td></tr><tr><td>PWU_AN2</td><td>Partial wakeup ADC analog 2 input pin</td><td>56</td><td>68</td><td>80</td><td>99</td></tr><tr><td>PWU_AN3</td><td>Partial wakeup ADC analog 3 input pin</td><td>57</td><td>69</td><td>81</td><td>100</td></tr><tr><td>PWU_AN4</td><td>Partial wakeup ADC analog 4 input pin</td><td>61</td><td>73</td><td>85</td><td>104</td></tr><tr><td>PWU_AN5</td><td>Partial wakeup ADC analog 5 input pin</td><td>62</td><td>74</td><td>86</td><td>105</td></tr><tr><td>PWU_AN6</td><td>Partial wakeup ADC analog 6 input pin</td><td>63</td><td>75</td><td>87</td><td>106</td></tr><tr><td>PWU_AN7</td><td>Partial wakeup ADC analog 7 input pin</td><td>-</td><td>76</td><td>88</td><td>107</td></tr><tr><td>PWUTRG_0</td><td>Partial wakeup trigger output pin (0)</td><td>-</td><td>-</td><td>-</td><td>130</td></tr><tr><td>PWUTRG_1</td><td>Partial wakeup trigger output pin (1)</td><td>74</td><td>89</td><td>107</td><td>131</td></tr></table>	Port name	Description	Pin No. of Package				TEQFP 100	TEQFP 120	TEQFP 144	TEQFP 176	PWU_AN0	Partial wakeup ADC analog 0 input pin	54	66	78	97	PWU_AN1	Partial wakeup ADC analog 1 input pin	55	67	79	98	PWU_AN2	Partial wakeup ADC analog 2 input pin	56	68	80	99	PWU_AN3	Partial wakeup ADC analog 3 input pin	57	69	81	100	PWU_AN4	Partial wakeup ADC analog 4 input pin	61	73	85	104	PWU_AN5	Partial wakeup ADC analog 5 input pin	62	74	86	105	PWU_AN6	Partial wakeup ADC analog 6 input pin	63	75	87	106	PWU_AN7	Partial wakeup ADC analog 7 input pin	-	76	88	107	PWUTRG_0	Partial wakeup trigger output pin (0)	-	-	-	130	PWUTRG_1	Partial wakeup trigger output pin (1)	74	89	107	131
Port name	Description	Pin No. of Package																																																																						
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PWU_AN7	Partial wakeup ADC analog 7 input pin	-	76	88	107																																																																			
PWUTRG_0	Partial wakeup trigger output pin (0)	-	-	-	130																																																																			
PWUTRG_1	Partial wakeup trigger output pin (1)	74	89	107	131																																																																			

Page	Section	Change Results																																																																												
232 to 242	CHAPTER 11: Port Configuration 3. Operation 3.2. Port output function configuration	Added a hyphen to the blanks of the table Error) <table><tr><th rowspan="2">Register (Offset)₁</th><th rowspan="2">Port₁</th><th colspan="8">Resource Functional Outputs₁</th></tr><tr><th>POF=0₁</th><th>POF=1₁</th><th>POF=2₁</th><th>POF=3₁</th><th>POF=4₁</th><th>POF=5₁</th><th>POF=6₁</th><th>POF=7₁</th></tr><tr><td>PPC_PCFG R000 (0x0000)₁</td><td>P000₁</td><td>GPIO_POD R0:POD00₁</td><td> </td><td> </td><td>SOUT2₁</td><td> </td><td> </td><td> </td><td>TIOA63₁</td></tr><tr><td>PPC_PCFG R001 (0x0002)₁</td><td>P001₁</td><td>GPIO_POD R0:POD01₁</td><td> </td><td>SCS30₁</td><td>SCS20₁</td><td> </td><td> </td><td> </td><td>TIOA54₁</td></tr></table> Correct) <table><tr><th rowspan="2">Register (Offset)₁</th><th rowspan="2">Port₁</th><th colspan="8">Resource Functional Outputs₁</th></tr><tr><th>POF=0₁</th><th>POF=1₁</th><th>POF=2₁</th><th>POF=3₁</th><th>POF=4₁</th><th>POF=5₁</th><th>POF=6₁</th><th>POF=7₁</th></tr><tr><td>PPC_PCFG R000 (0x0000)₁</td><td>P000₁</td><td>GPIO_POD R0:POD00₁</td><td> </td><td> </td><td>SOUT2₁</td><td> </td><td> </td><td> </td><td>TIOA63₁</td></tr><tr><td>PPC_PCFG R001 (0x0002)₁</td><td>P001₁</td><td>GPIO_POD R0:POD01₁</td><td> </td><td>SCS30₁</td><td>SCS20₁</td><td> </td><td> </td><td> </td><td>TIOA54₁</td></tr></table>	Register (Offset) ₁	Port ₁	Resource Functional Outputs ₁								POF=0 ₁	POF=1 ₁	POF=2 ₁	POF=3 ₁	POF=4 ₁	POF=5 ₁	POF=6 ₁	POF=7 ₁	PPC_PCFG R000 (0x0000) ₁	P000 ₁	GPIO_POD R0:POD00 ₁			SOUT2 ₁				TIOA63 ₁	PPC_PCFG R001 (0x0002) ₁	P001 ₁	GPIO_POD R0:POD01 ₁		SCS30 ₁	SCS20 ₁				TIOA54 ₁	Register (Offset) ₁	Port ₁	Resource Functional Outputs ₁								POF=0 ₁	POF=1 ₁	POF=2 ₁	POF=3 ₁	POF=4 ₁	POF=5 ₁	POF=6 ₁	POF=7 ₁	PPC_PCFG R000 (0x0000) ₁	P000 ₁	GPIO_POD R0:POD00 ₁			SOUT2 ₁				TIOA63 ₁	PPC_PCFG R001 (0x0002) ₁	P001 ₁	GPIO_POD R0:POD01 ₁		SCS30 ₁	SCS20 ₁				TIOA54 ₁
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239	CHAPTER 11: Port Configuration 3. Operation 3.2. Port output function configuration	Revised the Pin name as below: Error) <table><tr><th rowspan="2">Register (Offset)</th><th rowspan="2">Port</th><th colspan="8">Resource Functional Outputs</th></tr><tr><th>POF=0</th><th>POF=1</th><th>POF=2</th><th>POF=2</th><th>POF=4</th><th>POF=5</th><th>POF=6</th><th>POF=7</th></tr><tr><td>PPC_PCFG R320 (0x00E8)</td><td>P320</td><td>GPIO_POD R3:POD20</td><td></td><td></td><td></td><td>PWUTRG</td><td></td><td></td><td></td></tr><tr><td>PPC_PCFG R321 (0x00EA)</td><td>P321</td><td>GPIO_POD R3:POD21</td><td></td><td></td><td></td><td>PWUTRG</td><td>TRACECL K</td><td></td><td>TIOA45</td></tr></table> Correct) <table><tr><th rowspan="2">Register (Offset)</th><th rowspan="2">Port</th><th colspan="8">Resource Functional Outputs</th></tr><tr><th>POF=0</th><th>POF=1</th><th>POF=2</th><th>POF=2</th><th>POF=4</th><th>POF=5</th><th>POF=6</th><th>POF=7</th></tr><tr><td>PPC_PCFG R320 (0x00E8)</td><td>P320</td><td>GPIO_POD R3:POD20</td><td> </td><td> </td><td> </td><td> </td><td> </td><td> </td><td> </td></tr><tr><td>PPC_PCFG R321 (0x00EA)</td><td>P321</td><td>GPIO_POD R3:POD21</td><td> </td><td> </td><td> </td><td> </td><td>TRACECL K</td><td> </td><td>TIOA45</td></tr></table>	Register (Offset)	Port	Resource Functional Outputs								POF=0	POF=1	POF=2	POF=2	POF=4	POF=5	POF=6	POF=7	PPC_PCFG R320 (0x00E8)	P320	GPIO_POD R3:POD20				PWUTRG				PPC_PCFG R321 (0x00EA)	P321	GPIO_POD R3:POD21				PWUTRG	TRACECL K		TIOA45	Register (Offset)	Port	Resource Functional Outputs								POF=0	POF=1	POF=2	POF=2	POF=4	POF=5	POF=6	POF=7	PPC_PCFG R320 (0x00E8)	P320	GPIO_POD R3:POD20								PPC_PCFG R321 (0x00EA)	P321	GPIO_POD R3:POD21					TRACECL K		TIOA45
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Page	Section	Change Results
263	CHAPTER 12: State Transition 2. Diagram of State transition	Revised Figure 2-1 Diagram of Device State Transitions Error) The diagram shows the following states and transitions: Power Domain Shutdown to Int-Regulator stabilization wait for Standby mode Power Domain Power-on to Change in the main mode of a Int-Regulator Int-Regulator stabilization wait for Standby mode to PSS STOP mode Shutdown (Transition: <u>Setting in PSS Profile</u> - All oscillation circuit disable.) Change in the main mode of a Int-Regulator to PSS STOP mode Shutdown (Transition: <u>Interrupt request</u>) PSS STOP mode Shutdown to PSS Timer mode shutdown (Transition: <u>Setting in PSS Profile</u> - Slow-CR or Main and Slow-CR or Fast-CR is oscillation enable.) PSS Timer mode shutdown to PSS Partial Wake Up mode shutdown (Transition: <u>Partial Wake Up start processing</u> - RTC Timer count progress) PSS Partial Wake Up mode shutdown to Power Domain Power-on (Transition: <u>Interrupt request</u> - Range over of A/D/C - Other interrupt occur) PSS Partial Wake Up mode shutdown to Fast-CR oscillation Start (Transition: <u>Fast-CR oscillation Start</u>) Fast-CR oscillation Start to Fast-CR oscillation Stopping (Transition: <u>Fast-CR oscillation Stopping</u>) Fast-CR oscillation Stopping to PSS Partial Wake Up mode shutdown (Transition: <u>Partial Wake Up end processing</u> - No range over of A/D/C) Correct) The diagram shows the following states and transitions: Power Domain Shutdown to Int-Regulator stabilization wait for Standby mode Power Domain Power-on to Change in the main mode of a Int-Regulator Int-Regulator stabilization wait for Standby mode to PSS STOP mode Shutdown (Transition: <u>Setting in PSS Profile</u> - All oscillation circuit disable.) Change in the main mode of a Int-Regulator to PSS STOP mode Shutdown (Transition: <u>Interrupt request</u>) PSS STOP mode Shutdown to PSS Timer mode shutdown (Transition: <u>Setting in PSS Profile</u> - Slow-CR or Main or Sub is oscillation enable.) PSS Timer mode shutdown to Change in the main mode of a Int-Regulator (Transition: <u>Interrupt request</u>)

Page	Section	Change Results																																
264	CHAPTER 12: State Transition 2. Diagram of State transition	Deleted PSS PWU mode Shutdown column of Figure 2-2																																
264	CHAPTER 12: State Transition 2. Diagram of State transition	Revised as below: Error) oscillation state of a source clock <table><tr><td></td><td>RUN Normal Operation</td><td>RUN CPU Sleep</td><td>PSS Timer mode</td><td>PSS STOP mode</td><td>PSS PWU mode Shutdown</td><td>PSS Timer mode shutdown</td><td>PSS STOP mode Shutdown</td></tr><tr><td>Fast-CR</td><td>4Hz</td><td>←</td><td>4MHz/disable</td><td>Prohibition of an oscillation</td><td>4MHz/disable (Fast-CR is unrelated to the PSS profile to oscillate</td><td>4MHz/disable</td><td>Prohibition of an oscillation</td></tr></table> Correct) <table><tr><td></td><td>RUN Normal Operation</td><td>RUN CPU Sleep</td><td>PSS Timer mode</td><td>PSS STOP mode</td><td>PSS PWU mode Shutdown</td><td>PSS Timer mode shutdown</td><td>PSS STOP mode Shutdown</td></tr><tr><td>Fast-CR</td><td>4Hz</td><td>←</td><td>←</td><td>←</td><td>←</td><td>←</td><td>←</td></tr></table>		RUN Normal Operation	RUN CPU Sleep	PSS Timer mode	PSS STOP mode	PSS PWU mode Shutdown	PSS Timer mode shutdown	PSS STOP mode Shutdown	Fast-CR	4Hz	←	4MHz/disable	Prohibition of an oscillation	4MHz/disable (Fast-CR is unrelated to the PSS profile to oscillate	4MHz/disable	Prohibition of an oscillation		RUN Normal Operation	RUN CPU Sleep	PSS Timer mode	PSS STOP mode	PSS PWU mode Shutdown	PSS Timer mode shutdown	PSS STOP mode Shutdown	Fast-CR	4Hz	←	←	←	←	←	←
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Fast-CR	4Hz	←	←	←	←	←	←																											
264	CHAPTER 12: State Transition 2. Diagram of State transition	Added the Note as below: Note: - Do not disable FastCR (4MHz) in PSS mode (PD2: ON/OFF).																																

Page	Section	Change Results																																																				
265	CHAPTER 12: State Transition 3. Fetching the Operation Mode	Revised as below: 1) Each power supply is stable before reset release for that domain Error) <table><tr><th>#</th><th>Power supply</th><th>Reset</th><th>Responsibility (CY MCU or User?)</th><th>Reset release above Min Safe voltage?</th><th>Corr. phase in POR release diagram (sheet "POR diagram")</th><th>Explanation of Reset</th></tr><tr><td>1</td><td>VCC</td><td>LVDH1 reset</td><td>CY MCU</td><td>Yes</td><td>(1)</td><td>VCC is monitored by LVDH1 which detects & release BOD above Min Safe Voltage</td></tr><tr><td>2</td><td>VDD (internal 1.2V)</td><td>POR</td><td>CY MCU</td><td>Yes</td><td>(3)</td><td>VDD rises above safe voltage during Int-Regulator stabilization wait shown in (3) in sheet POR Diagram</td></tr><tr><td>3</td><td>AVCC0/1</td><td>LVDH1 reset or RSTX</td><td>CY MCU or User (*see note)</td><td>Yes</td><td>(1)</td><td>LVDH1 can monitor AVCC0/1 only if it's shorted with VCC on the customer board. Otherwise, customer needs to take care of the BOD on the board and issue appropriate reset (RSTX, etc.) to inactivate the domain until the supply is stable.</td></tr></table> Correct) <table><tr><th>#</th><th>Power supply</th><th>Reset</th><th>Who must monitor the supply?</th><th>Corr. phase in POR release diagram (sheet "POR diagram")</th><th>Explanation of Reset</th></tr><tr><td>1</td><td>VCC</td><td>LVDH1 reset</td><td>CY MCU</td><td>(1)</td><td>VCC is monitored by LVDH1 which issues & releases reset above minimum operation voltage</td></tr><tr><td>2</td><td>VDD (internal 1.2V)</td><td>POR</td><td>CY MCU</td><td>(3)</td><td>VDD rises above minimum operation voltage during Int-Regulator stabilization wait shown in (3) in sheet POR Diagram</td></tr><tr><td>3</td><td>AVCC0/1</td><td>LVDH1 reset or RSTX</td><td>CY MCU or User</td><td>(1)</td><td>LVDH1 can monitor AVCC0/1 only if it's shorted with VCC on the board. Otherwise, this supply has to be monitored on the board and RSTX has to be issued to inactivate the domain until the supply is stable.</td></tr></table>	#	Power supply	Reset	Responsibility (CY MCU or User?)	Reset release above Min Safe voltage?	Corr. phase in POR release diagram (sheet "POR diagram")	Explanation of Reset	1	VCC	LVDH1 reset	CY MCU	Yes	(1)	VCC is monitored by LVDH1 which detects & release BOD above Min Safe Voltage	2	VDD (internal 1.2V)	POR	CY MCU	Yes	(3)	VDD rises above safe voltage during Int-Regulator stabilization wait shown in (3) in sheet POR Diagram	3	AVCC0/1	LVDH1 reset or RSTX	CY MCU or User (*see note)	Yes	(1)	LVDH1 can monitor AVCC0/1 only if it's shorted with VCC on the customer board. Otherwise, customer needs to take care of the BOD on the board and issue appropriate reset (RSTX, etc.) to inactivate the domain until the supply is stable.	#	Power supply	Reset	Who must monitor the supply?	Corr. phase in POR release diagram (sheet "POR diagram")	Explanation of Reset	1	VCC	LVDH1 reset	CY MCU	(1)	VCC is monitored by LVDH1 which issues & releases reset above minimum operation voltage	2	VDD (internal 1.2V)	POR	CY MCU	(3)	VDD rises above minimum operation voltage during Int-Regulator stabilization wait shown in (3) in sheet POR Diagram	3	AVCC0/1	LVDH1 reset or RSTX	CY MCU or User	(1)	LVDH1 can monitor AVCC0/1 only if it's shorted with VCC on the board. Otherwise, this supply has to be monitored on the board and RSTX has to be issued to inactivate the domain until the supply is stable.
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274	CHAPTER 13: Pin Status in Each CPU State 1. Pin Status in Each CPU State	Revised the description of *1 as below: Error) To power off power domains 2 and 3, be sure to set HOLDIO_PD2 (SYSC_SSPECFGR.HOLDIO_PD2=1). Correct) To power off power domains 2, be sure to set HOLDIO_PD2 (SYSC_SSPECFGR.HOLDIO_PD2=1).																																																				
280	CHAPTER 14: Low Voltage Detection 3. Registers	Added the Note as below: Note: - LVDH1 reset does not clear the LVDH1S, LVDH1V, LVDH1E configured value. The following factors clear the value to initial value - Power-on reset - LVDL0(RAM maintenance low voltage detection reset) - LVDL1(Internal low voltage detection reset) - Illegal mode detection reset - INITX (RSTX pin + MD pin simultaneous assert reset)																																																				

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280	CHAPTER 14: Low Voltage Detection 3. Registers	Revised as below [Bit27:25] LVDL1V Internal low-voltage detection voltage setting bits Error) <table><thead><tr><th>Bit 27:25</th><th>Voltage [V]</th></tr></thead><tbody><tr><td>000 *</td><td>0.875(Initial value)</td></tr><tr><td>001 *</td><td>0.95</td></tr><tr><td>010</td><td>Reserved</td></tr><tr><td>011</td><td>Reserved</td></tr><tr><td>100</td><td>Reserved</td></tr><tr><td>101</td><td>Reserved</td></tr><tr><td>110</td><td>Reserved</td></tr><tr><td>111</td><td>Reserved</td></tr></tbody></table> *: These detection voltage level settings are below the minimum operation voltage. Between these detection voltage and the minimum operation voltage, MCU functions are not guaranteed except for the low voltage detector. Correct) <table><thead><tr><th>Bit 27:25</th><th>Voltage [V]</th><th>Guaranteed MCU operation range</th></tr></thead><tbody><tr><td>000 *</td><td>0.875(Initial value)</td><td rowspan="8">No</td></tr><tr><td>001 *</td><td>0.95</td></tr><tr><td>010</td><td>Reserved</td></tr><tr><td>011</td><td>Reserved</td></tr><tr><td>100</td><td>Reserved</td></tr><tr><td>101</td><td>Reserved</td></tr><tr><td>110</td><td>Reserved</td></tr><tr><td>111</td><td>Reserved</td></tr></tbody></table> *: This LVD cannot be used to reliably generate a reset before voltage dips below minimum guaranteed MCU operation voltage, as these detection levels are below the minimum guaranteed MCU operation voltage.	Bit 27:25	Voltage [V]	000 *	0.875(Initial value)	001 *	0.95	010	Reserved	011	Reserved	100	Reserved	101	Reserved	110	Reserved	111	Reserved	Bit 27:25	Voltage [V]	Guaranteed MCU operation range	000 *	0.875(Initial value)	No	001 *	0.95	010	Reserved	011	Reserved	100	Reserved	101	Reserved	110	Reserved	111	Reserved
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281	CHAPTER 14: Low Voltage Detection 3. Registers	Revised the Note below: [Bit14] LVDH1S Internal low-voltage detection voltage operation selection bit Error) Note: - LVDH1V will be initial value with reset. If LVDH1V is changed from initial vale, LVDH1S should be configured as interrupt. Correct) Note: - Set SYSC0_STSLVDCFGR.LVDH1S = 0. LVDH1 need to be used as Reset function.																																						

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281	CHAPTER 14: Low Voltage Detection 3. Registers	Revised as below [Bit11:9] LVDH1V External low-voltage detection voltage setting bits Error) <table><thead><tr><th>Bit 11:9</th><th>Voltage [V]</th></tr></thead><tbody><tr><td>000 *</td><td>2.7</td></tr><tr><td>001</td><td>2.8</td></tr><tr><td>010</td><td>3.6</td></tr><tr><td>011</td><td>3.8</td></tr><tr><td>100</td><td>4.0</td></tr><tr><td>101</td><td>4.2</td></tr><tr><td>110 *</td><td>2.5</td></tr><tr><td>111 *</td><td>2.6(Initial value)</td></tr></tbody></table> *: These detection voltage level settings are below the minimum operation voltage. Between these detection voltage and the minimum operation voltage, MCU functions are not guaranteed except for the low voltage detector. Correct) <table><thead><tr><th>Bit 11:9</th><th>Voltage [V]</th><th>Guaranteed MCU operation voltage range</th></tr></thead><tbody><tr><td>000 *</td><td>2.7</td><td>No</td></tr><tr><td>001</td><td>2.8</td><td rowspan="5">Yes</td></tr><tr><td>010</td><td>3.6</td></tr><tr><td>011</td><td>3.8</td></tr><tr><td>100</td><td>4.0</td></tr><tr><td>101</td><td>4.2</td></tr><tr><td>110 *</td><td>2.5</td><td rowspan="2">No</td></tr><tr><td>111 *</td><td>2.6(Initial value)</td></tr></tbody></table> *: These LVD settings cannot be used to reliably generate a reset before voltage dips below minimum guaranteed MCU operation voltage, as these detection levels are below the minimum guaranteed MCU operation voltage (2.7V).	Bit 11:9	Voltage [V]	000 *	2.7	001	2.8	010	3.6	011	3.8	100	4.0	101	4.2	110 *	2.5	111 *	2.6(Initial value)	Bit 11:9	Voltage [V]	Guaranteed MCU operation voltage range	000 *	2.7	No	001	2.8	Yes	010	3.6	011	3.8	100	4.0	101	4.2	110 *	2.5	No	111 *	2.6(Initial value)
Bit 11:9	Voltage [V]																																									
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281	CHAPTER 14: Low Voltage Detection 3. Registers	Deleted the Note below: [Bit11:9] LVDH1V External low-voltage detection voltage setting bits Note: – LVDH1V will be initial value with reset. If LVDH1V is changed from initial vale, LVDH1S should be configured as interrupt.																																								

Page	Section	Change Results
420	CHAPTER 17: Base Timer I/O Selection Function 4. Registers	Revised Register Name as below: Table 4 1 List of Base Timer I/O Selection Registers BT_BTSEL3031 Error) I/O selection register (channel 10, 31) Correct) I/O selection register (channel 30, 31)
426	CHAPTER 17: Base Timer I/O Selection Function 4. Registers 4.2. Simultaneous Soft Start Register (BT_BTSSSR)	Revised as below: [bit11:0] SSSR[11:0]: Simultaneous soft start bits Error) BT_BTSSSR0 : SSSR0-11 = ch0-11 (cperi0) BT_BTSSSR12 : SSSR0-11 = ch12-23 (cperi1) BT_BTSSSR24 : SSSR0-11 = ch24-35 (cperi2) Correct) BT_BTSSSR0 : SSSR0-11 = ch0-11 BT_BTSSSR12 : SSSR0-11 = ch12-23 BT_BTSSSR24 : SSSR0-11 = ch24-35 BT_BTSSSR36 : SSSR0-11 = ch36-47 BT_BTSSSR48 : SSSR0-11 = ch48-59 BT_BTSSSR60 : SSSR0-3 = ch60-63
444	CHAPTER 18: Base Timer Simultaneous Operation 5. Explanation of the 16-bit Global Timer Operation	Added the Note as below: Interrupt mask function Note: - If Interrupt mask function "by setting GT_TCCS.MSI[2:0] Register" is used, please write T_TCCS[15:8], GT_TCCSC[15:8] and GT_TCCSS[15:8] after Global Timer stopped.

Page	Section	Change Results												
455	CHAPTER 18: Base Timer Simultaneous Operation 6. Registers of the 16-bit Global Timer	Revised the Note as below: [bit12:10] MSI2 to MSI0: Interrupt mask selection bits (Error) - The written data is written to the mask register. - While the Global Timer is operating (STOP: bit6=0 of the timer enable bit), the value written to the mask register is reloaded to the counter only when the mask counter becomes 0. - When the Global Timer is stopped (STOP: bit6=1 of the timer enable bit), the value written to the mask register is immediately reloaded to the mask counter. Correct) - The written data is written to the mask register. - If Interrupt mask function "by setting GT_TCCS.MSI[2:0] Register" is used, please write GT_TCCS[15:8], GT_TCCSC[15:8] and GT_TCCSS[15:8] after Global Timer stopped.												
455	CHAPTER 18: Base Timer Simultaneous Operation 6. Registers of the 16-bit Global Timer	Revised as below: [bit9] ICLR: Compare clear interrupt flag bit (Error) <table><tr><th>bit</th><th>Description</th></tr><tr><td>0</td><td>0 is not detected</td></tr><tr><td>1</td><td>0 is detected.</td></tr></table> Correct) <table><tr><th>bit</th><th>Description</th></tr><tr><td>0</td><td>0 No compare clear</td></tr><tr><td>1</td><td>1 Compare clear match.</td></tr></table>	bit	Description	0	0 is not detected	1	0 is detected.	bit	Description	0	0 No compare clear	1	1 Compare clear match.
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458	CHAPTER 18: Base Timer Simultaneous Operation 6. Registers of the 16-bit Global Timer	Added the following sentences: 6.4. Global Timer State Control Clear register (GT_TCCSC) For details on writing to this register, see "7.Precautions for Using This Device."												

Page	Section	Change Results
460	CHAPTER 18: Base Timer Simultaneous Operation 6. Registers of the 16-bit Global Timer	Revised the description of Register below: 6.5. Global Timer State Control Set register (GT_TCCSS) Error) The Global Timer State Control Set Register (GT_TCCSC) is a register that is used to set bits of the Global Timer State Control Register (GT_TCCS). Correct) The Global Timer State Control Set Register (GT_TCCSS) is a register that is used to set bits of the Global Timer State Control Register (GT_TCCS).
460	CHAPTER 18: Base Timer Simultaneous Operation 6. Registers of the 16-bit Global Timer	Added the following sentences to description of Register: 6.5. Global Timer State Control Set register (GT_TCCSS) For details on writing to this register, see "7.Precautions for Using This Device."
470	CHAPTER 18: Base Timer Simultaneous Operation 7. Precautions for Using This Device	Added the following sentences: When accessing the timer state control registers (GT_TCCS) ■ If Interrupt mask function "by setting TCCS.MSI[2:0] Register" is used, please write GT_TCCS[15:8], GT_TCCSC[15:8] and GT_TCCSS[15:8] after Global Timer stopped.
479	CHAPTER 19: 32-Bit Free-Run Timer 3. Operation of the 32-Bit Free-Run Timer	Added the following to the Note: The following describes the case when both interrupt requests are masked. – If Interrupt mask function "by setting TCCS.MSI[2:0] Register" is used, please write TCCS[15:8], TCCSC[15:8] and TCCSS[15:8] after 32bit free-run timer stopped.

Page	Section	Change Results												
493	CHAPTER 19: 32-Bit Free-Run Timer 4. Registers of the 32-Bit Free-Run Timer	Revised the Note below: [bit12:10] MSI[2:0]: Interrupt Mask Selection Bits (Error) - The value read is a mask counter value. The mask counter is a decrement counter. - The written data is written to the mask register. - While the 32-bit Free-run Timer is operating (the Timer Enable bit (STOP) ="0"), the value written to the mask register is reloaded to the counter only when the mask counter becomes 0. - When the 32-bit Free-run Timer is stopped (the Timer Enable bit (STOP) ="1"), the value written to the mask register is immediately reloaded to the mask counter. Correct) - The value read is a mask counter value. The mask counter is a decrement counter. - The written data is written to the mask register. - If Interrupt mask function "by setting TCCS.MSI[2:0] Register" is used, please write TCCS[15:8], TCCSC[15:8] and TCCSS[15:8] after 32bit free-run timer stopped.												
493	CHAPTER 19: 32-Bit Free-Run Timer 4. Registers of the 32-Bit Free-Run Timer	Revised as below: [bit9] ICLR: Compare Clear Interrupt Flag Error) <table><tr><th>Bit</th><th>Description</th></tr><tr><td>0</td><td>0 is not detected</td></tr><tr><td>1</td><td>0 is detected.</td></tr></table> Correct) <table><tr><th>Bit</th><th>Description</th></tr><tr><td>0</td><td>0 No compare clear</td></tr><tr><td>1</td><td>1 Compare clear match.</td></tr></table>	Bit	Description	0	0 is not detected	1	0 is detected.	Bit	Description	0	0 No compare clear	1	1 Compare clear match.
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500	CHAPTER 19: 32-Bit Free-Run Timer 4. Registers of the 32-Bit Free-Run Timer	Added the following sentences to description of Register: 4.5. Timer State Control Clear Register (TCCSC) For details on writing to this register, see "5.Precautions for Using This Device."												
504	CHAPTER 19: 32-Bit Free-Run Timer 4. Registers of the 32-Bit Free-Run Timer	Added the following sentences to description of Register: 4.6. Timer State Control Set Register (TCCSS) For details on writing to this register, see "5.Precautions for Using This Device."												

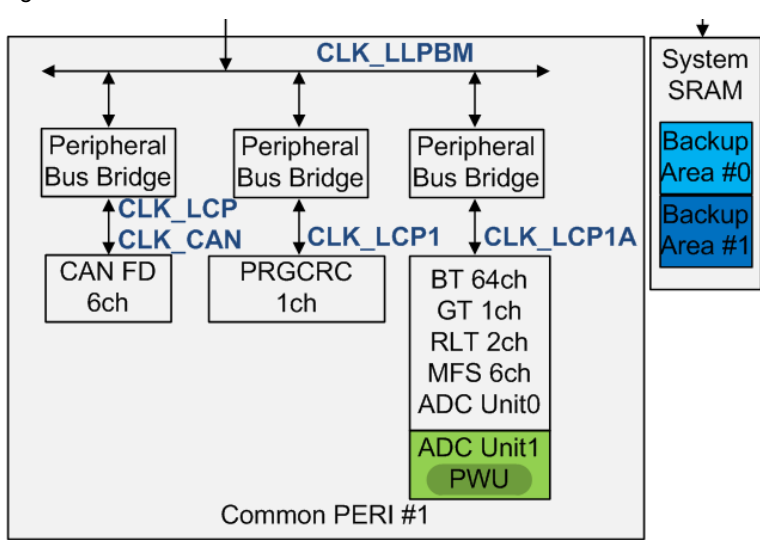
Page	Section	Change Results						
508	CHAPTER 19: 32-Bit Free-Run Timer 5. Precautions for Using This Device	Added the following sentences: When Accessing the Timer State Control Register (TCCS) - If Interrupt mask function "by setting TCCS.MSI[2:0] Register" is used, please write TCCS[15:8], TCCSC[15:8] and TCCSS[15:8] after 32bit free-run timer.						
560	CHAPTER 22: I/O Port 4. Register List	Revised Reference of Port output data register as below: Error) <table border="1"> <tr> <td>GPIO_PODRi</td><td>Port output data register</td><td>0</td></tr> </table> Correct) <table border="1"> <tr> <td>GPIO_PODRi</td><td>Port output data register</td><td>4.4</td></tr> </table>	GPIO_PODRi	Port output data register	0	GPIO_PODRi	Port output data register	4.4
GPIO_PODRi	Port output data register	0						
GPIO_PODRi	Port output data register	4.4						
734	CHAPTER 26: Bus Diagnosis Function 3. Registers 3.1. Bus diagnosis status register (BUSDIGSRn) (n=0-2)	Added the following to the Note: Reference of Port output data register [bit0] RDWR: Data direction Error) Notes: - If a diagnosis error occurs during writing to bus diagnosis status register, writing continues and the target error flag is not set to "1". Correct) Notes: - If a diagnosis error occurs during writing to bus diagnosis status register, writing continues and the target error flag is not set to "1". - For access to this register, use word access or half word access instructions.						

Page	Section	Change Results
737	CHAPTER 26: Bus Diagnosis Function 3. Registers 3.2. Bus diagnosis test register (BUSTSTRn) (n=0-2)	Added the following to the Note: Reference of Port output data register [bit3:0] AEN3 to AEN0: Address error Error) Notes: – Any interrupt is disabled during writing to the bus diagnosis test register. – The bus diagnosis test register is used for debugging the bus diagnosis functions. – Writing to the bus diagnosis test register is performed even if diagnosis error occurs, but the error flag of the target status register is not set to "1". Correct) Notes: – Any interrupt is disabled during writing to the bus diagnosis test register. – The bus diagnosis test register is used for debugging the bus diagnosis functions. – Writing to the bus diagnosis test register is performed even if diagnosis error occurs, but the error flag of the target status register is not set to "1". – For access to this register, use word access or half word access instructions.
739	CHAPTER 26: Bus Diagnosis Function 3. Registers 3.3. Bus diagnosis address register (BUSADRn) (n=0-2)	Added the following to the Note: Reference of Port output data register [bit31:0] ADR31 to ADR0: Bus address Error) Notes: – This register is valid when any one of the DER, AER, or CNER bit of the bus diagnosis status register is "1". – This register is not updated when any one of the DER, AER, or CNER bit of the bus diagnosis status register is "1". Correct) Notes: – This register is valid when any one of the DER, AER, or CNER bit of the bus diagnosis status register is "1". – This register is not updated when any one of the DER, AER, or CNER bit of the bus diagnosis status register is "1". – For access to this register, use word access instructions.

Page	Section	Change Results													
Rev. *D															
-	CHAPTER 2: Function List CHAPTER 3: Product Description CHAPTER 10: Port Description CHAPTER 11: Port Configuration CHAPTER 13: Pin Status in Each CPU State	Removed LQFP176, TEQFP144, LQFP120, TEQFP120 and TEQFP100 of the Package.													
21	CHAPTER 2: Function List 1. Function List	The shading parts added as below. <table><tr><th rowspan="2">Function</th><th colspan="3">Description</th><th rowspan="2">Remark</th></tr><tr><th>S6J34xxJxx</th><th>S6J34xxHxx</th><th>S6J34xxFxx</th></tr><tr><td>Partial Wake Up</td><td>analog input 8ch</td><td>analog input 8ch</td><td>analog input 7ch</td><td>Trigger 1ch</td></tr></table>	Function	Description			Remark	S6J34xxJxx	S6J34xxHxx	S6J34xxFxx	Partial Wake Up	analog input 8ch	analog input 8ch	analog input 7ch	Trigger 1ch
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Partial Wake Up	analog input 8ch	analog input 8ch	analog input 7ch	Trigger 1ch											
26	CHAPTER 2: Function List 2.3. Restriction	The shading parts added as below. <table><tr><th>Function</th><th>LQFP144</th><th>LQFP100</th></tr><tr><td>PartialWakeUp</td><td>PWUTRG_0</td><td>PWU_AN7 PWUTRG_0</td></tr></table>	Function	LQFP144	LQFP100	PartialWakeUp	PWUTRG_0	PWU_AN7 PWUTRG_0							
Function	LQFP144	LQFP100													
PartialWakeUp	PWUTRG_0	PWU_AN7 PWUTRG_0													
32	CHAPTER 3: Product Description 2. Product Description	The shading parts revised as below. Error) <table><tr><th>Feature</th><th>Description</th></tr><tr><td>Partial wakeup</td><td>This product series doesn't support Partial wakeup function.</td></tr></table> Correct) <table><tr><th>Feature</th><th>Description</th></tr><tr><td>Partial wakeup</td><td>Partial wakeup function is mounted. This mode is one of the PSS modes.</td></tr></table>	Feature	Description	Partial wakeup	This product series doesn't support Partial wakeup function.	Feature	Description	Partial wakeup	Partial wakeup function is mounted. This mode is one of the PSS modes.					
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Page	Section	Change Results								
33	CHAPTER 3: Product Description 2. Product Description	The shading parts revised as below. Error) Work Flash can be accessed with 0-wait-cycle if CPU frequency is 12.5MHz or less. 7-wait-cycle: 80MHz or less. 11-wait-cycle: 132MHz or less. Correct) Work Flash can be accessed with 0-wait-cycle if CPU frequency is 12.5MHz or less. 6-wait-cycle: 80MHz or less. 10-wait-cycle: 132MHz or less.								
34	CHAPTER 3: Product Description 2. Product Description	The shading parts added as below. Error) <table><tr><th>Feature</th><th>Description</th></tr><tr><td>Multi-Functional Serial (MFS)</td><td>UART mode CSIO (SPI) mode LIN mode I²C mode Only 2 ports of MFS have the dedicated I/O for I²C. See the datasheet in detailed. CTS/RTS is not mounted (hardware flow control is not supported for this series.) This model does not support Wake Up Function.</td></tr></table> Correct) <table><tr><th>Feature</th><th>Description</th></tr><tr><td>Multi-Functional Serial (MFS)</td><td>UART mode CSIO (SPI) mode LIN mode I²C mode Only 2 ports of MFS have the dedicated I/O for I²C. See the datasheet in detailed. The I²C is not designed to be hot swappable. CTS/RTS is not mounted (hardware flow control is not supported for this series.) This model does not support Wake Up Function.</td></tr></table>	Feature	Description	Multi-Functional Serial (MFS)	UART mode CSIO (SPI) mode LIN mode I ² C mode Only 2 ports of MFS have the dedicated I/O for I ² C. See the datasheet in detailed. CTS/RTS is not mounted (hardware flow control is not supported for this series.) This model does not support Wake Up Function.	Feature	Description	Multi-Functional Serial (MFS)	UART mode CSIO (SPI) mode LIN mode I ² C mode Only 2 ports of MFS have the dedicated I/O for I ² C. See the datasheet in detailed. The I ² C is not designed to be hot swappable. CTS/RTS is not mounted (hardware flow control is not supported for this series.) This model does not support Wake Up Function.
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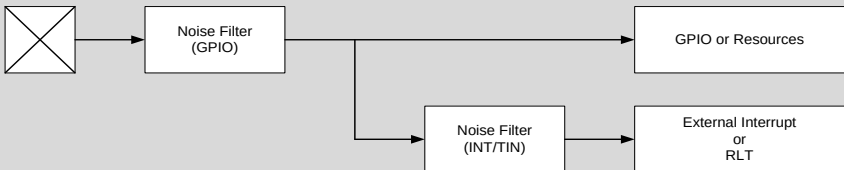
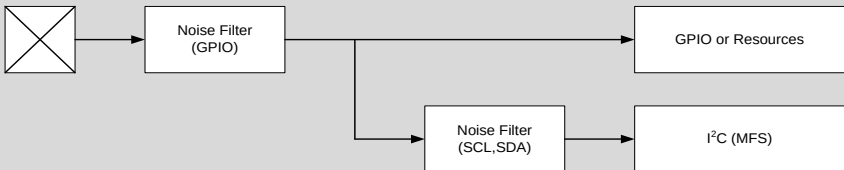
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34	CHAPTER 3: Product Description 2. Product Description	Deleted the below Note: – The description of the preliminary documentation will be changed without any notification.																																																																								
35	CHAPTER 3: Product Description 2. Product Description	Added the 2.1 Reset signal. The shading parts added as below. 2.1 Reset signal The following table shows the reset signal of each function. See the chapter of "Reset" in Traveo™ Platform hardware manual for details of reset signal "RSTX_**". Table 2-2. The Reset signal of each function. <table><tr><th>Functions</th><th>CHAPTER</th><th>Reset signal</th><th>Remark</th></tr><tr><td>Base Timer</td><td>CHAPTER 16</td><td>RSTX_PD2</td><td></td></tr><tr><td>Base Timer I/O Selection Function</td><td>CHAPTER 17</td><td>RSTX_PD2</td><td></td></tr><tr><td>Base Timer Simultaneous Operation</td><td>CHAPTER 18</td><td>RSTX_PD2</td><td></td></tr><tr><td>32-Bit Free-Run Timer</td><td>CHAPTER 19</td><td>RSTX_PD2</td><td></td></tr><tr><td>32-Bit Input Capture</td><td>CHAPTER 20</td><td>RSTX_PD2</td><td></td></tr><tr><td>32-bit Reload Timer</td><td>CHAPTER 21</td><td>RSTX_PD2</td><td></td></tr><tr><td rowspan="2">I/O Port</td><td rowspan="2">CHAPTER 22</td><td>RSTX_PD2</td><td>for I/O Controller</td></tr><tr><td>RSTX_IO_5V</td><td>for I/O</td></tr><tr><td rowspan="2">12/10/8-Bit Analog to Digital Converter</td><td rowspan="2">CHAPTER 23</td><td>RSTX_PD2</td><td>for Unit0</td></tr><tr><td>RSTX_PD1</td><td>for Unit1</td></tr><tr><td>Partial Wakeup Control</td><td>CHAPTER 24</td><td>RSTX_PD1</td><td></td></tr><tr><td>Programmable CRC</td><td>CHAPTER 25</td><td>RSTX_PD2</td><td></td></tr><tr><td>Clock Monitor</td><td>CHAPTER 26</td><td>RSTX_PD1</td><td></td></tr><tr><td>Bus Diagnosis Function</td><td>CHAPTER 27</td><td>RSTX_PD2</td><td></td></tr><tr><td>CAN FD Controller</td><td>Traveo™ Platform hardware manual</td><td>RSTX_PD2</td><td></td></tr><tr><td>Multi-function Serial Interface</td><td>Traveo™ Platform hardware manual</td><td>RSTX_PD2</td><td></td></tr><tr><td>32-bit Output Compare</td><td>Traveo™ Platform hardware manual</td><td>RSTX_PD2</td><td></td></tr><tr><td>QPRC (Quadrature Position/Revolution Counter)</td><td>Traveo™ Platform hardware manual</td><td>RSTX_PD2</td><td></td></tr></table>	Functions	CHAPTER	Reset signal	Remark	Base Timer	CHAPTER 16	RSTX_PD2		Base Timer I/O Selection Function	CHAPTER 17	RSTX_PD2		Base Timer Simultaneous Operation	CHAPTER 18	RSTX_PD2		32-Bit Free-Run Timer	CHAPTER 19	RSTX_PD2		32-Bit Input Capture	CHAPTER 20	RSTX_PD2		32-bit Reload Timer	CHAPTER 21	RSTX_PD2		I/O Port	CHAPTER 22	RSTX_PD2	for I/O Controller	RSTX_IO_5V	for I/O	12/10/8-Bit Analog to Digital Converter	CHAPTER 23	RSTX_PD2	for Unit0	RSTX_PD1	for Unit1	Partial Wakeup Control	CHAPTER 24	RSTX_PD1		Programmable CRC	CHAPTER 25	RSTX_PD2		Clock Monitor	CHAPTER 26	RSTX_PD1		Bus Diagnosis Function	CHAPTER 27	RSTX_PD2		CAN FD Controller	Traveo™ Platform hardware manual	RSTX_PD2		Multi-function Serial Interface	Traveo™ Platform hardware manual	RSTX_PD2		32-bit Output Compare	Traveo™ Platform hardware manual	RSTX_PD2		QPRC (Quadrature Position/Revolution Counter)	Traveo™ Platform hardware manual	RSTX_PD2	
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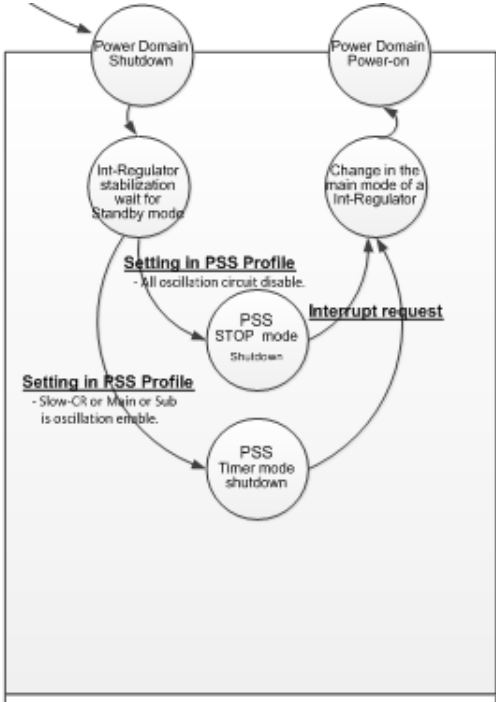
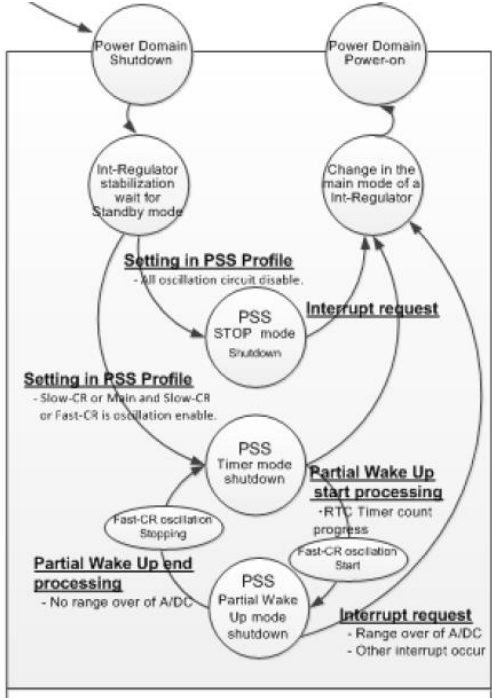
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39	CHAPTER 3: Product Description 3. Note	The shading parts added as below. <table><thead><tr><th>Function</th><th>Related Register and Configuration</th><th>Restriction</th><th>Remark</th></tr></thead><tbody><tr><td>Low-power Consumption</td><td>SYSC0_PSSCKSRER</td><td>Do not disable FastCR (4MHz) in PSS mode (PD2: ON/OFF). If FastCR disable, please see Note in the "5. Precautions for Using this Device" of chapter 24.</td><td>-</td></tr></tbody></table>	Function	Related Register and Configuration	Restriction	Remark	Low-power Consumption	SYSC0_PSSCKSRER	Do not disable FastCR (4MHz) in PSS mode (PD2: ON/OFF). If FastCR disable, please see Note in the "5. Precautions for Using this Device" of chapter 24.	-								
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39	CHAPTER 3: Product Description 3. Note	The shading parts revised as below. Error) <table><thead><tr><th>Function</th><th>Related Register and Configuration</th><th>Restriction</th><th>Remark</th></tr></thead><tbody><tr><td>Partial Wakeup Control</td><td>-</td><td>This product series doesn't support Partial wakeup function.</td><td>-</td></tr></tbody></table> Correct) <table><thead><tr><th>Function</th><th>Related Register and Configuration</th><th>Restriction</th><th>Remark</th></tr></thead><tbody><tr><td>Partial Wakeup Control</td><td>-</td><td>This function has restriction. Please see the "5. Precautions for Using this Device" of chapter 24.</td><td>-</td></tr></tbody></table>	Function	Related Register and Configuration	Restriction	Remark	Partial Wakeup Control	-	This product series doesn't support Partial wakeup function.	-	Function	Related Register and Configuration	Restriction	Remark	Partial Wakeup Control	-	This function has restriction. Please see the "5. Precautions for Using this Device" of chapter 24.	-
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42	CHAPTER 4: Block Diagram 1. Block Diagram	The shading parts added as below. Figure1-1 																

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61	CHAPTER 7: Memory and Base Address Map 3. Base Address Map	The shading parts revised as below. Error) <table><tr><th>START Address</th><th>END Address</th><th>Group</th><th>Function</th><th>PPU_No</th></tr><tr><td>B475_0000</td><td>B475_7FFF</td><td>CPU Config Group</td><td>PPU</td><td>77</td></tr></table> Correct) <table><tr><th>START Address</th><th>END Address</th><th>Group</th><th>Function</th><th>PPU_No</th></tr><tr><td>B475_0000</td><td>B475_7FFF</td><td>CPU Config Group</td><td>PPU</td><td>-</td></tr></table>	START Address	END Address	Group	Function	PPU_No	B475_0000	B475_7FFF	CPU Config Group	PPU	77	START Address	END Address	Group	Function	PPU_No	B475_0000	B475_7FFF	CPU Config Group	PPU	-																																																																																														
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76 to 80	CHAPTER 9: DMA Channel Activation Factors 1. Factors List	The shading parts added as below. Error) <table><tr><th rowspan="2">client number</th><th colspan="6">Peripheral functions</th><th rowspan="2">Remarks</th></tr><tr><th>Combinatio n.0</th><th>Combinatio n.1</th><th>Combinatio n.2</th><th>Combinatio n.3</th><th>Combinatio n.4</th><th>Combinatio n.5</th></tr><tr><td>0 to 8</td><td colspan="6">Reserved</td><td></td></tr><tr><td>9</td><td>WORK FLASH</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>*2</td></tr><tr><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td><td></td></tr><tr><td>103</td><td>PRGCRC</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td></td></tr><tr><td>104 to 127</td><td colspan="6">Reserved</td><td></td></tr></table> *1: For assignment of source, see the chapter of "I/O Port" on this manual. *2: DSTP_ACK function is set by DMAi_CMCICm:BEHSTPACK. Correct) <table><tr><th rowspan="2">Client Number</th><th colspan="6">Peripheral functions</th><th rowspan="2">Enable Setting of IRQ Request</th><th rowspan="2">Remarks</th></tr><tr><th>Combinati on.0</th><th>Combinati on.1</th><th>Combinati on.2</th><th>Combinati on.3</th><th>Combinati on.4</th><th>Combinati on.5</th></tr><tr><td>0 to 8</td><td colspan="6">Reserved</td><td></td><td></td></tr><tr><td>9</td><td>WORK FLASH</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>Unnecessary</td><td>*2</td></tr><tr><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td><td></td></tr><tr><td>103</td><td>PRGCRC</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>Unnecessary</td><td></td></tr><tr><td>104 to 127</td><td colspan="6">Reserved</td><td></td><td></td></tr></table> *1: For assignment of source, see the chapter of "I/O Port" on this manual. *2: DSTP_ACK function is set by DMAi_CMCICm:BEHSTPACK. *3: The interrupt factor flags of peripheral function are cleared automatically by acceptance of DMA transfer request. *4: The interrupt factor flags of peripheral function are cleared automatically after DMA transfer is started.	client number	Peripheral functions						Remarks	Combinatio n.0	Combinatio n.1	Combinatio n.2	Combinatio n.3	Combinatio n.4	Combinatio n.5	0 to 8	Reserved							9	WORK FLASH	-	-	-	-	-	*2	:	:	:	:	:	:	:		103	PRGCRC	-	-	-	-	-		104 to 127	Reserved							Client Number	Peripheral functions						Enable Setting of IRQ Request	Remarks	Combinati on.0	Combinati on.1	Combinati on.2	Combinati on.3	Combinati on.4	Combinati on.5	0 to 8	Reserved								9	WORK FLASH	-	-	-	-	-	Unnecessary	*2	:	:	:	:	:	:	:	:		103	PRGCRC	-	-	-	-	-	Unnecessary		104 to 127	Reserved							
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85	CHAPTER 10: Port Description 1. Port Description List	The shading parts added as below. <table><thead><tr><th rowspan="2">Port name</th><th rowspan="2">Description</th><th colspan="3">Pin No. of Package</th></tr><tr><th>LQFP 100</th><th>LQFP 144</th><th>TEQFP 176</th></tr></thead><tbody><tr><td>PWU_AN0</td><td>Partial wakeup ADC analog 0 input pin</td><td>54</td><td>78</td><td>97</td></tr><tr><td>PWU_AN1</td><td>Partial wakeup ADC analog 1 input pin</td><td>55</td><td>79</td><td>98</td></tr><tr><td>PWU_AN2</td><td>Partial wakeup ADC analog 2 input pin</td><td>56</td><td>80</td><td>99</td></tr><tr><td>PWU_AN3</td><td>Partial wakeup ADC analog 3 input pin</td><td>57</td><td>81</td><td>100</td></tr><tr><td>PWU_AN4</td><td>Partial wakeup ADC analog 4 input pin</td><td>61</td><td>85</td><td>104</td></tr><tr><td>PWU_AN5</td><td>Partial wakeup ADC analog 5 input pin</td><td>62</td><td>86</td><td>105</td></tr><tr><td>PWU_AN6</td><td>Partial wakeup ADC analog 6 input pin</td><td>63</td><td>87</td><td>106</td></tr><tr><td>PWU_AN7</td><td>Partial wakeup ADC analog 7 input pin</td><td>-</td><td>88</td><td>107</td></tr><tr><td>PWUTRG_0</td><td>Partial wakeup trigger output pin (0)</td><td>-</td><td>-</td><td>130</td></tr><tr><td>PWUTRG_1</td><td>Partial wakeup trigger output pin (1)</td><td>74</td><td>107</td><td>131</td></tr></tbody></table>	Port name	Description	Pin No. of Package			LQFP 100	LQFP 144	TEQFP 176	PWU_AN0	Partial wakeup ADC analog 0 input pin	54	78	97	PWU_AN1	Partial wakeup ADC analog 1 input pin	55	79	98	PWU_AN2	Partial wakeup ADC analog 2 input pin	56	80	99	PWU_AN3	Partial wakeup ADC analog 3 input pin	57	81	100	PWU_AN4	Partial wakeup ADC analog 4 input pin	61	85	104	PWU_AN5	Partial wakeup ADC analog 5 input pin	62	86	105	PWU_AN6	Partial wakeup ADC analog 6 input pin	63	87	106	PWU_AN7	Partial wakeup ADC analog 7 input pin	-	88	107	PWUTRG_0	Partial wakeup trigger output pin (0)	-	-	130	PWUTRG_1	Partial wakeup trigger output pin (1)	74	107	131
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102	CHAPTER 10: Port Description 2. Remark	The shading parts added as below. Error) Note: - The port description list shows the port function of description which is mounted and supported on the product. The function which is not described in this table is not supported and assured. - See the chapter of “Function List” on this manual as well. Correct) Note: - The port description list shows the port function of description which is mounted and supported on the product. The function which is not described in this table is not supported and assured. - See the chapter of “Function List” on this manual as well. - PWU function have restriction. Please see Note in the “5. Precautions for Using this Device” of chapter 24.																																																										
105	CHAPTER 11:Port Configuration 2. Configuration and Block Diagram	The shading parts revised as below. Error) This chapter doesn't have a block diagram. Correct) See the “2. Configuration and Block Diagrams” of Chapter 22.																																																										

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243	CHAPTER 11: Port Configuration 3. Operation 3.2. Port Output Function Configuration	The shading parts added as below. Error) <table><tr><th rowspan="2">Register (Offset)</th><th rowspan="2">Port</th><th colspan="8">Resource Functional Outputs</th></tr><tr><th>POF=0</th><th>POF=1</th><th>POF=2</th><th>POF=2</th><th>POF=4</th><th>POF=5</th><th>POF=6</th><th>POF=7</th></tr><tr><td>PPC_PCFG R320 (0x00E8)</td><td>P320</td><td>GPIO_POD R3:POD20</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td></tr><tr><td>PPC_PCFG R321 (0x00EA)</td><td>P321</td><td>GPIO_POD R3:POD21</td><td>-</td><td>-</td><td>-</td><td>-</td><td>TRACECL K</td><td>-</td><td>TIOA45</td></tr></table> Correct) <table><tr><th rowspan="2">Register (Offset)</th><th rowspan="2">Port</th><th colspan="8">Resource Functional Outputs</th></tr><tr><th>POF=0</th><th>POF=1</th><th>POF=2</th><th>POF=2</th><th>POF=4</th><th>POF=5</th><th>POF=6</th><th>POF=7</th></tr><tr><td>PPC_PCFG R320 (0x00E8)</td><td>P320</td><td>GPIO_POD R3:POD20</td><td>-</td><td>-</td><td>-</td><td>PWUTRG 0</td><td>-</td><td>-</td><td>-</td></tr><tr><td>PPC_PCFG R321 (0x00EA)</td><td>P321</td><td>GPIO_POD R3:POD21</td><td>-</td><td>-</td><td>-</td><td>PWUTRG 1</td><td>TRACECL K</td><td>-</td><td>TIOA45</td></tr></table>	Register (Offset)	Port	Resource Functional Outputs								POF=0	POF=1	POF=2	POF=2	POF=4	POF=5	POF=6	POF=7	PPC_PCFG R320 (0x00E8)	P320	GPIO_POD R3:POD20	-	-	-	-	-	-	-	PPC_PCFG R321 (0x00EA)	P321	GPIO_POD R3:POD21	-	-	-	-	TRACECL K	-	TIOA45	Register (Offset)	Port	Resource Functional Outputs								POF=0	POF=1	POF=2	POF=2	POF=4	POF=5	POF=6	POF=7	PPC_PCFG R320 (0x00E8)	P320	GPIO_POD R3:POD20	-	-	-	PWUTRG 0	-	-	-	PPC_PCFG R321 (0x00EA)	P321	GPIO_POD R3:POD21	-	-	-	PWUTRG 1	TRACECL K	-	TIOA45
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264	CHAPTER 11: Port Configuration	Added the 5. Precautions 5.1. Noise Filter. The shading parts added as below. 5. Precautions 5.1. Noise Filter Each GPIO has the noise filter for noise removal from external input. Also, some resources have additional dedicated noise filter for resource input. See the following Configuration and Diagram Table 5-1: Configuration for Noise Filter <table><tr><th>Noise filter for resource</th><th>PPC_PCFGRIij: NFE</th><th>EICxx_NFER: NFE_n</th><th>RLTn_TMCSR: NFE</th><th>RIC_RESINn: RESSEL</th></tr><tr><td>GPIO</td><td>Enable/Disable</td><td>- *1</td><td>- *1</td><td>- *1</td></tr><tr><td>External interrupt (INT)</td><td>Disable *2</td><td>Enable/Disable</td><td>- *1</td><td>- *1</td></tr><tr><td>Reload Timer input (TIN)</td><td>Disable *2</td><td>- *1</td><td>Enable/Disable</td><td>- *1</td></tr><tr><td>I²C interface (SCL, SDA)</td><td>Disable *2</td><td>- *1</td><td>- *1</td><td>Enable/Disable</td></tr></table> *1: It is unrelated to register's setting. *2: When selecting a Noise Filter other than for GPIO, set the Port Setting Register (PPC_PCFGRIij: NFE) to Disable. Figure 5-1: Diagram of Noise Filter - External pins GPIO for using some resources except INTx_y, TINx_y, SCLx_y, SDAX_y  - External pins GPIO for using INTx_y or TINx_y  - External pins GPIO for using SCLx_y, SDAX_y of I²C 	Noise filter for resource	PPC_PCFGRIij: NFE	EICxx_NFER: NFE _n	RLTn_TMCSR: NFE	RIC_RESINn: RESSEL	GPIO	Enable/Disable	- *1	- *1	- *1	External interrupt (INT)	Disable *2	Enable/Disable	- *1	- *1	Reload Timer input (TIN)	Disable *2	- *1	Enable/Disable	- *1	I ² C interface (SCL, SDA)	Disable *2	- *1	- *1	Enable/Disable
Noise filter for resource	PPC_PCFGRIij: NFE	EICxx_NFER: NFE _n	RLTn_TMCSR: NFE	RIC_RESINn: RESSEL																							
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Page	Section	Change Results
267	CHAPTER 12: State Transition 2. Diagram of State Transition	Revised Figure 2-1 Diagram of Device State Transitions Error)  Correct) 

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268	CHAPTER 12: State Transition 2. Diagram of State Transition	The shading parts added as below. S6J3400 supports only the below defined operating state. Internal state and a frequency definition <table><tr><th></th><th></th><th>RUN Normal Operation</th><th>RUN CPU Sleep</th><th>PSS Timer mode</th><th>PSS STOP mode</th><th>PSS PWU mode Shutdown</th><th>PSS Timer mode shutdown</th><th>PSS STOP mode Shutdown</th></tr><tr><td rowspan="14">Clocks</td><td>CLK_CPU</td><td rowspan="14">Customer any Frequency</td><td rowspan="14">←</td><td rowspan="3">Prohibition of an oscillation</td><td rowspan="3">Prohibition of an oscillation</td><td rowspan="3">Prohibition of an oscillation</td><td rowspan="3">Prohibition of an oscillation</td><td rowspan="3">Prohibition of an oscillation</td></tr><tr><td>CLK_FCLK</td></tr><tr><td>CLK_ATB</td></tr><tr><td>CLK_DBG</td><td rowspan="3">Customer any Frequency</td><td rowspan="3">Prohibition of an oscillation</td><td rowspan="3">Customer any Frequency</td><td rowspan="3">Prohibition of an oscillation</td><td rowspan="3">Prohibition of an oscillation</td></tr><tr><td>CLK_HPM</td></tr><tr><td>CLK_DMA</td></tr><tr><td>CLK_MEMC</td><td rowspan="3">Prohibition of an oscillation</td><td rowspan="3">Prohibition of an oscillation</td><td rowspan="3">Prohibition of an oscillation</td><td rowspan="3">Prohibition of an oscillation</td></tr><tr><td>CLK_SYSC1</td></tr><tr><td>CLK_TRC</td></tr><tr><td>CLK_SYSC0H</td><td rowspan="7">Prohibition of an oscillation</td><td rowspan="7">Prohibition of an oscillation</td><td rowspan="7">Prohibition of an oscillation</td><td rowspan="7">Prohibition of an oscillation</td></tr><tr><td>CLK_COMH</td></tr><tr><td>CLK_LLPM</td></tr><tr><td>CLK_LCP</td></tr><tr><td>CLK_LCP0</td></tr><tr><td>CLK_LCP0A</td></tr><tr><td>CLK_LCP1</td></tr><tr><td>CLK_LCP1A</td></tr><tr><td rowspan="6">oscillation state of a source clock</td><td>Slow-CR</td><td>100KHz</td><td>←</td><td>100KHz / disable</td><td>Prohibition of an oscillation</td><td>100KHz</td><td>100KHz / disable</td><td>Prohibition of an oscillation</td></tr><tr><td>Fast-CR</td><td>4MHz</td><td>←</td><td>4MHz / disable</td><td>Prohibition of an oscillation</td><td>4MHz / disable (Fast-CR is unrelated to the PSS profile to oscillate.)</td><td>4MHz / disable</td><td>Prohibition of an oscillation</td></tr><tr><td>Main oscillator</td><td>4MHz~16MHz</td><td>←</td><td>4~16MHz / disable</td><td>Prohibition of an oscillation</td><td>Prohibition of an oscillation</td><td>4~16MHz / disable</td><td>Prohibition of an oscillation</td></tr><tr><td>Sub oscillator</td><td>32KHz</td><td>←</td><td>32KHz / disable</td><td>Prohibition of an oscillation</td><td>Prohibition of an oscillation</td><td>32KHz / disable</td><td>Prohibition of an oscillation</td></tr><tr><td>PLL</td><td>Customer any Frequency</td><td>←</td><td colspan="5">Prohibition of an oscillation</td></tr><tr><td>SSCG_PLL</td><td>Customer any Frequency</td><td>←</td><td colspan="5"></td></tr></table> The macro operating state in each mode, and the state of the power domain. <table><tr><th></th><th></th><th>RUN Normal Operation</th><th>RUN CPU Sleep</th><th>PSS Timer mode</th><th>PSS STOP mode</th><th>PSS PWU mode Shutdown</th><th>PSS Timer mode shutdown</th><th>PSS STOP mode Shutdown</th></tr><tr><td>CPU(PD2)</td><td>-</td><td>enable</td><td>disable</td><td>disable</td><td>disable</td><td>Power down</td><td>Power down</td><td>Power down</td></tr><tr><td>FLASH(PD2)</td><td>-</td><td>Operation</td><td>NOP</td><td>Deep Sleep</td><td>Deep Sleep</td><td>Power down</td><td>Power down</td><td>Power down</td></tr><tr><td>Backup RAM(PD4)</td><td>-</td><td>Operation</td><td>NOP</td><td>NOP</td><td>NOP</td><td>NOP</td><td>NOP</td><td>NOP</td></tr><tr><td>Int-Regulator</td><td>-</td><td>Main mode</td><td>Main mode</td><td>Main mode</td><td>Main mode</td><td>Standby mode</td><td>Standby mode</td><td>Standby mode</td></tr><tr><td rowspan="2">Power Domain</td><td>PD2</td><td>ON</td><td>ON</td><td>ON</td><td>ON</td><td>OFF</td><td>OFF</td><td>OFF</td></tr><tr><td>PD4</td><td>ON</td><td>ON</td><td>ON</td><td>ON</td><td>ON</td><td>ON</td><td>ON</td></tr></table> The conditions for changing in each state. <table><tr><th></th><th></th><th>RUN Normal Operation</th><th>RUN CPU Sleep</th><th>PSS Timer mode</th><th>PSS STOP mode</th><th>PSS PWU mode Shutdown</th><th>PSS Timer mode shutdown</th><th>PSS STOP mode Shutdown</th></tr><tr><td rowspan="2">Setup for changes</td><td>PSSEN0</td><td>-</td><td>disable</td><td>enable</td><td>enable</td><td>enable</td><td>enable</td><td>enable</td></tr><tr><td>PSSEN1</td><td>-</td><td>enable</td><td>enable</td><td>enable</td><td>enable</td><td>enable</td><td>enable</td></tr><tr><td colspan="2">Changes start command</td><td>-</td><td colspan="6">Execution of a WFI command</td></tr></table>			RUN Normal Operation	RUN CPU Sleep	PSS Timer mode	PSS STOP mode	PSS PWU mode Shutdown	PSS Timer mode shutdown	PSS STOP mode Shutdown	Clocks	CLK_CPU	Customer any Frequency	←	Prohibition of an oscillation	Prohibition of an oscillation	Prohibition of an oscillation	Prohibition of an oscillation	Prohibition of an oscillation	CLK_FCLK	CLK_ATB	CLK_DBG	Customer any Frequency	Prohibition of an oscillation	Customer any Frequency	Prohibition of an oscillation	Prohibition of an oscillation	CLK_HPM	CLK_DMA	CLK_MEMC	Prohibition of an oscillation	Prohibition of an oscillation	Prohibition of an oscillation	Prohibition of an oscillation	CLK_SYSC1	CLK_TRC	CLK_SYSC0H	Prohibition of an oscillation	Prohibition of an oscillation	Prohibition of an oscillation	Prohibition of an oscillation	CLK_COMH	CLK_LLPM	CLK_LCP	CLK_LCP0	CLK_LCP0A	CLK_LCP1	CLK_LCP1A	oscillation state of a source clock	Slow-CR	100KHz	←	100KHz / disable	Prohibition of an oscillation	100KHz	100KHz / disable	Prohibition of an oscillation	Fast-CR	4MHz	←	4MHz / disable	Prohibition of an oscillation	4MHz / disable (Fast-CR is unrelated to the PSS profile to oscillate.)	4MHz / disable	Prohibition of an oscillation	Main oscillator	4MHz~16MHz	←	4~16MHz / disable	Prohibition of an oscillation	Prohibition of an oscillation	4~16MHz / disable	Prohibition of an oscillation	Sub oscillator	32KHz	←	32KHz / disable	Prohibition of an oscillation	Prohibition of an oscillation	32KHz / disable	Prohibition of an oscillation	PLL	Customer any Frequency	←	Prohibition of an oscillation					SSCG_PLL	Customer any Frequency	←								RUN Normal Operation	RUN CPU Sleep	PSS Timer mode	PSS STOP mode	PSS PWU mode Shutdown	PSS Timer mode shutdown	PSS STOP mode Shutdown	CPU(PD2)	-	enable	disable	disable	disable	Power down	Power down	Power down	FLASH(PD2)	-	Operation	NOP	Deep Sleep	Deep Sleep	Power down	Power down	Power down	Backup RAM(PD4)	-	Operation	NOP	NOP	NOP	NOP	NOP	NOP	Int-Regulator	-	Main mode	Main mode	Main mode	Main mode	Standby mode	Standby mode	Standby mode	Power Domain	PD2	ON	ON	ON	ON	OFF	OFF	OFF	PD4	ON	ON	ON	ON	ON	ON	ON			RUN Normal Operation	RUN CPU Sleep	PSS Timer mode	PSS STOP mode	PSS PWU mode Shutdown	PSS Timer mode shutdown	PSS STOP mode Shutdown	Setup for changes	PSSEN0	-	disable	enable	enable	enable	enable	enable	PSSEN1	-	enable	enable	enable	enable	enable	enable	Changes start command		-	Execution of a WFI command					
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	CLK_SYSC0H			Prohibition of an oscillation	Prohibition of an oscillation	Prohibition of an oscillation	Prohibition of an oscillation																																																																																																																																																																																												
	CLK_COMH																																																																																																																																																																																																		
	CLK_LLPM																																																																																																																																																																																																		
	CLK_LCP																																																																																																																																																																																																		
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CLK_LCP1A																																																																																																																																																																																																			
oscillation state of a source clock	Slow-CR	100KHz	←	100KHz / disable	Prohibition of an oscillation	100KHz	100KHz / disable	Prohibition of an oscillation																																																																																																																																																																																											
	Fast-CR	4MHz	←	4MHz / disable	Prohibition of an oscillation	4MHz / disable (Fast-CR is unrelated to the PSS profile to oscillate.)	4MHz / disable	Prohibition of an oscillation																																																																																																																																																																																											
	Main oscillator	4MHz~16MHz	←	4~16MHz / disable	Prohibition of an oscillation	Prohibition of an oscillation	4~16MHz / disable	Prohibition of an oscillation																																																																																																																																																																																											
	Sub oscillator	32KHz	←	32KHz / disable	Prohibition of an oscillation	Prohibition of an oscillation	32KHz / disable	Prohibition of an oscillation																																																																																																																																																																																											
	PLL	Customer any Frequency	←	Prohibition of an oscillation																																																																																																																																																																																															
	SSCG_PLL	Customer any Frequency	←																																																																																																																																																																																																
		RUN Normal Operation	RUN CPU Sleep	PSS Timer mode	PSS STOP mode	PSS PWU mode Shutdown	PSS Timer mode shutdown	PSS STOP mode Shutdown																																																																																																																																																																																											
CPU(PD2)	-	enable	disable	disable	disable	Power down	Power down	Power down																																																																																																																																																																																											
FLASH(PD2)	-	Operation	NOP	Deep Sleep	Deep Sleep	Power down	Power down	Power down																																																																																																																																																																																											
Backup RAM(PD4)	-	Operation	NOP	NOP	NOP	NOP	NOP	NOP																																																																																																																																																																																											
Int-Regulator	-	Main mode	Main mode	Main mode	Main mode	Standby mode	Standby mode	Standby mode																																																																																																																																																																																											
Power Domain	PD2	ON	ON	ON	ON	OFF	OFF	OFF																																																																																																																																																																																											
	PD4	ON	ON	ON	ON	ON	ON	ON																																																																																																																																																																																											
		RUN Normal Operation	RUN CPU Sleep	PSS Timer mode	PSS STOP mode	PSS PWU mode Shutdown	PSS Timer mode shutdown	PSS STOP mode Shutdown																																																																																																																																																																																											
Setup for changes	PSSEN0	-	disable	enable	enable	enable	enable	enable																																																																																																																																																																																											
	PSSEN1	-	enable	enable	enable	enable	enable	enable																																																																																																																																																																																											
Changes start command		-	Execution of a WFI command																																																																																																																																																																																																
268	CHAPTER 12: State Transition 2. Diagram of State Transition	The shading parts added as below. Note: - Do not disable FastCR (4MHz) in PSS mode (PD2: ON/OFF). If FastCR disable, Please see Note in the "5. Precautions for Using this Device" of chapter 24.																																																																																																																																																																																																	

Page	Section	Change Results						
278	CHAPTER 13: Pin Status in Each CPU State 1. Pin Status in Each CPU State	The shading sentences added as below. Correct) Legend Hi-Z - Output is Hi-Z. Input blocked - Input is actually disconnected.						
284	CHAPTER 14: Low Voltage Detection 3. Registers	The shading part added as below. Error) <table border="1"> <thead> <tr> <th>Bit 27:25</th><th>Voltage [V]</th><th>Guaranteed MCU operation Range</th></tr> </thead> </table> Correct) <table border="1"> <thead> <tr> <th>Bit 27:25</th><th>Voltage [V]</th><th>Guaranteed MCU Operation Voltage Range</th></tr> </thead> </table>	Bit 27:25	Voltage [V]	Guaranteed MCU operation Range	Bit 27:25	Voltage [V]	Guaranteed MCU Operation Voltage Range
Bit 27:25	Voltage [V]	Guaranteed MCU operation Range						
Bit 27:25	Voltage [V]	Guaranteed MCU Operation Voltage Range						
285	CHAPTER 14: Low Voltage Detection 3. Registers	The shading sentences revised as below. Error) [Bit14] LVDH1S Internal low-voltage detection voltage operation selection bit Correct) [Bit14] LVDH1S External low-voltage detection voltage operation selection bit						
285	CHAPTER 14: Low Voltage Detection 3. Registers	The shading sentences revised as below. Error) [Bit8] LVDH1E Internal low-voltage detection operation enable bit Correct) [Bit8] LVDH1E External low-voltage detection operation enable bit						
598	CHAPTER 23: 12/10/8-Bit Analog to Digital Converter 3.5. Group Processing	The shading part added as below. Error) Figure 3- shows some possible group configurations: Correct) Figure 3-4 shows some possible group configurations:						

Page	Section	Change Results
599	CHAPTER 23: 12/10/8-Bit Analog to Digital Converter 3.5. Group Processing	The shading part added as below. Error) Figure 3- shows an example of stopping a group processing. Correct) Figure 3-5 shows an example of stopping a group processing.
600	CHAPTER 23: 12/10/8-Bit Analog to Digital Converter 3.5. Group Processing	The shading parts added as below. Error) Figure 3- shows an example of resuming a group processing (Forced stop mode is enabled (ADC12Bn_CTRL.FSMD = "1")). Figure 3- shows an example of resuming a group processing (Forced stop mode is disabled (ADC12Bn_CTRL.FSMD = "0")). Correct) Figure 3-6 shows an example of resuming a group processing (Forced stop mode is enabled (ADC12Bn_CTRL.FSMD = "1")). Figure 3-7 shows an example of resuming a group processing (Forced stop mode is disabled (ADC12Bn_CTRL.FSMD = "0")).
600	CHAPTER 23: 12/10/8-Bit Analog to Digital Converter 3.5. Group Processing	The shading parts added as below. Error) (4) The operation is dependent on the setting of forced stop mode (ADC12Bn_CTRL.FSMD). Forced stop mode is enabled (ADC12Bn_CTRL.FSMD = "1", Figure 3-): : Forced stop mode is disabled (ADC12Bn_CTRL.FSMD = "0", Figure 3-): Correct) (4) The operation is dependent on the setting of forced stop mode (ADC12Bn_CTRL.FSMD). Forced stop mode is enabled (ADC12Bn_CTRL.FSMD = "1", Figure 3-6): : Forced stop mode is disabled (ADC12Bn_CTRL.FSMD = "0", Figure 3-7):

Page	Section	Change Results
600,601	CHAPTER 23: 12/10/8-Bit Analog to Digital Converter 3.5. Group Processing	The shading parts added as below. Error) (6) The operation is dependent on the setting of forced stop mode (ADC12Bn_CTRL.FSMD). Forced stop mode is enabled (ADC12Bn_CTRL.FSMD = "1", Figure 3-): : Forced stop mode is disabled (ADC12Bn_CTRL.FSMD = "0", Figure 3-): Correct) (6) The operation is dependent on the setting of forced stop mode (ADC12Bn_CTRL.FSMD). Forced stop mode is enabled (ADC12Bn_CTRL.FSMD = "1", Figure 3-6): : Forced stop mode is disabled (ADC12Bn_CTRL.FSMD = "0", Figure 3-7):
602	CHAPTER 23: 12/10/8-Bit Analog to Digital Converter 3.5. Group Processing	The shading part added as below. Error) Figure 3- shows an example of restarting a group processing with its first channel. Correct) Figure 3-8 shows an example of restarting a group processing with its first channel.
603	CHAPTER 23: 12/10/8-Bit Analog to Digital Converter 3.5. Group Processing	The shading parts added as below. Error) Figure 3- shows an example of restarting a group processing with its first channel during the conversion of the last channel of the group processing (Forced stop mode is enabled (ADC12Bn_CTRL.FSMD = "1")). Figure 3- shows an example of restarting a group processing with its first channel during the conversion of the last channel of the group processing (Forced stop mode is disabled (ADC12Bn_CTRL.FSMD = "0")). Correct) Figure 3-9 shows an example of restarting a group processing with its first channel during the conversion of the last channel of the group processing (Forced stop mode is enabled (ADC12Bn_CTRL.FSMD = "1")). Figure 3-10 shows an example of restarting a group processing with its first channel during the conversion of the last channel of the group processing (Forced stop mode is disabled (ADC12Bn_CTRL.FSMD = "0")).

Page	Section	Change Results
603	CHAPTER 23: 12/10/8-Bit Analog to Digital Converter 3.5. Group Processing	The shading parts added as below. Error) The operations after (3) are dependent on the setting of forced stop mode (ADC12Bn_CTRL.FSMD). Forced stop mode is enabled (ADC12Bn_CTRL.FSMD = "1", Figure 3-): : Forced stop mode is disabled (ADC12Bn_CTRL.FSMD = "0", Figure 3-): Correct) The operations after (3) are dependent on the setting of forced stop mode (ADC12Bn_CTRL.FSMD). Forced stop mode is enabled (ADC12Bn_CTRL.FSMD = "1", Figure 3-9): : Forced stop mode is disabled (ADC12Bn_CTRL.FSMD = "0", Figure 3-10):
604	CHAPTER 23: 12/10/8-Bit Analog to Digital Converter 3.5. Group Processing	The shading part added as below. Error) Figure 3- shows an example of restarting a group processing with its last converted channel set to resume. These way subgroups can be formed within a group. Correct) Figure 3-11 shows an example of restarting a group processing with its last converted channel set to resume. These way subgroups can be formed within a group.
605	CHAPTER 23: 12/10/8-Bit Analog to Digital Converter 3.5. Group Processing	The shading parts revised as below. Error) Figure 3-4 Restarting of the group processing with a subgroup Correct) Figure 3-11 Restarting of the group processing with a subgroup
609	CHAPTER 23: 12/10/8-Bit Analog to Digital Converter 3.8. A/D Converter Calibration	The shading parts revised as below. Error) Figure 3-5 Example of converted digital value dependence on input voltage level Correct) Figure 3-12 Example of converted digital value dependence on input voltage level

Page	Section	Change Results
609	CHAPTER 23: 12/10/8-Bit Analog to Digital Converter 3.8. A/D Converter Calibration	The shading part added as below. Error) This feature can be used to perform A/D Converter calibration. As it is shown on Figure 3- ideal characteristics of A/D Converter would have: Correct) This feature can be used to perform A/D Converter calibration. As it is shown on Figure 3-12 ideal characteristics of A/D Converter would have:
611	CHAPTER 23: 12/10/8-Bit Analog to Digital Converter 3.10. Range Comparator Function	The shading parts added as below. Error) Figure 3- shows the 8-bit range comparator structure. Figure 3- shows the 12-bit range comparator structure. Correct) Figure 3-13 shows the 8-bit range comparator structure. Figure 3-14 shows the 12-bit range comparator structure.
611	CHAPTER 23: 12/10/8-Bit Analog to Digital Converter 3.10. Range Comparator Function	The shading parts revised as below. Error) Figure 3-6 8-bit Range Comparator Structure Correct) Figure 3-13 8-bit Range Comparator Structure
612	CHAPTER 23: 12/10/8-Bit Analog to Digital Converter 3.10. Range Comparator Function	The shading parts revised as below. Error) Figure 3-7 12-bit Range Comparator Structure Correct) Figure 3-14 12-bit Range Comparator Structure

Page	Section	Change Results										
614	CHAPTER 23: 12/10/8-Bit Analog to Digital Converter 3.11. Pulse Detection Function	The shading part added as below. Error) The Figure 3- shows the operation of the pulse detection function for channel 0 with Correct) The Figure 3-15 shows the operation of the pulse detection function for channel 0 with										
614	CHAPTER 23: 12/10/8-Bit Analog to Digital Converter 3.11. Pulse Detection Function	The shading parts revised as below. Error) Figure 3-8 Example of Pulse Detection operation Correct) Figure 3-15 Example of Pulse Detection operation										
695	CHAPTER 24: Partial Wakeup Control	Added the CHAPTER 24										
742	CHAPTER 25: Programmable CRC 4.3. CRC Final XOR Register	The shading part added as below. Error) <table border="1"><tr><td>30</td></tr><tr><td>[30]</td></tr><tr><td>R/W</td></tr><tr><td>Rp/Wp</td></tr><tr><td>1</td></tr></table> Correct) <table border="1"><tr><td>30</td></tr><tr><td>FXOR[30]</td></tr><tr><td>R/W</td></tr><tr><td>Rp/Wp</td></tr><tr><td>1</td></tr></table>	30	[30]	R/W	Rp/Wp	1	30	FXOR[30]	R/W	Rp/Wp	1
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Rp/Wp												
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Page	Section	Change Results
Rev. *E		
45	CHAPTER 5: Clock Configuration	The shading part revised as below. Error) - Overview - Configuration and Block Diagram - Operation of the Your_Peripheral - Registers Correct) - Overview - Operation - Remark
103	CHAPTER 11: Port Configuration	The shading part added as below. Error) - Overview - Configuration and Block Diagram - Operation - Registers Correct) - Overview - Configuration and Block Diagram - Operation - Registers - Precautions
265	CHAPTER 11: Port Configuration 5. Precautions	The shading parts added as below. 5.2 I²C setting For I²C fast-mode output pins “P006 (SDA3_0), P007 (SCL3_0), P225 (SDA5_0), P226 (SCL5_0)” to output Hi-Z after reset, the registers must be set in the following order. (1) Set the MD (Operation Mode Setting Bits) of the SMR (Serial Mode Register) to I²C mode. (2) Set the POF (Port Output Function Selection Bit) of the PPC_PCFGRIj (Port Setting Register) to I²C. If not set in the above order, the MCU will output "H" level before outputting Hi-Z to each port.
589	CHAPTER 23: 12/10/8-Bit Analog to Digital Converter	The shading part deleted as below. 6. History

Page	Section	Change Results																																																																																
743	CHAPTER 26: Clock Monitor	The shading part revised as below. Error) 5. Precautions for Using This Device Correct) 5. Precautions																																																																																
Rev. *F																																																																																		
236	CHAPTER 11: Port Configuration 3.2. Port output function configuration	The shading part revised as below. Error) <table><tr><th rowspan="2">Register (Offset)</th><th rowspan="2">Port</th><th colspan="4">Resource Functional Outputs</th></tr><tr><th>POF=0</th><th>POF=1</th><th>POF=2</th><th>POF=3</th></tr><tr><td>PPC_PCFG R000 (0x0000)</td><td>P000</td><td>GPIO_POD R0:POD00</td><td>-</td><td>-</td><td>SOUT2</td></tr><tr><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td></tr><tr><td>PPC_PCFG R006 (0x000C)</td><td>P006</td><td>GPIO_POD R0:POD06</td><td>-</td><td>SOUT3</td><td>-</td></tr><tr><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td></tr><tr><td>PPC_PCFG R010 (0x0014)</td><td>P010</td><td>GPIO_POD R0:POD10</td><td>TIOA2</td><td>SOUT8</td><td>-</td></tr></table> Correct) <table><tr><th rowspan="2">Register (Offset)</th><th rowspan="2">Port</th><th colspan="4">Resource Functional Outputs</th></tr><tr><th>POF=0</th><th>POF=1</th><th>POF=2</th><th>POF=3</th></tr><tr><td>PPC_PCFG R000 (0x0000)</td><td>P000</td><td>GPIO_POD R0:POD00</td><td>-</td><td>-</td><td>SOT2</td></tr><tr><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td></tr><tr><td>PPC_PCFG R006 (0x000C)</td><td>P006</td><td>GPIO_POD R0:POD06</td><td>-</td><td>SOT3</td><td>-</td></tr><tr><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td></tr><tr><td>PPC_PCFG R010 (0x0014)</td><td>P010</td><td>GPIO_POD R0:POD10</td><td>TIOA2</td><td>SOT8</td><td>-</td></tr></table>	Register (Offset)	Port	Resource Functional Outputs				POF=0	POF=1	POF=2	POF=3	PPC_PCFG R000 (0x0000)	P000	GPIO_POD R0:POD00	-	-	SOUT2	:	:	:	:	:	:	PPC_PCFG R006 (0x000C)	P006	GPIO_POD R0:POD06	-	SOUT3	-	:	:	:	:	:	:	PPC_PCFG R010 (0x0014)	P010	GPIO_POD R0:POD10	TIOA2	SOUT8	-	Register (Offset)	Port	Resource Functional Outputs				POF=0	POF=1	POF=2	POF=3	PPC_PCFG R000 (0x0000)	P000	GPIO_POD R0:POD00	-	-	SOT2	:	:	:	:	:	:	PPC_PCFG R006 (0x000C)	P006	GPIO_POD R0:POD06	-	SOT3	-	:	:	:	:	:	:	PPC_PCFG R010 (0x0014)	P010	GPIO_POD R0:POD10	TIOA2	SOT8	-
Register (Offset)	Port	Resource Functional Outputs																																																																																
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PPC_PCFG R000 (0x0000)	P000	GPIO_POD R0:POD00	-	-	SOUT2																																																																													
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PPC_PCFG R006 (0x000C)	P006	GPIO_POD R0:POD06	-	SOUT3	-																																																																													
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237	CHAPTER 11: Port Configuration 3.2. Port output function configuration	The shading part revised as below. Error) <table><thead><tr><th rowspan="2">Register (Offset)</th><th rowspan="2">Port</th><th colspan="4">Resource Functional Outputs</th></tr><tr><th>POF=0</th><th>POF=1</th><th>POF=2</th><th>POF=3</th></tr></thead><tbody><tr><td>PPC_PCFG R014 (0x001C)</td><td>P014</td><td>GPIO_POD R0:POD14</td><td>TIOA3</td><td>-</td><td>SOUT12</td></tr><tr><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td></tr><tr><td>PPC_PCFG R020 (0x0028)</td><td>P020</td><td>GPIO_POD R0:POD20</td><td>-</td><td>SOUT0</td><td>-</td></tr><tr><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td></tr><tr><td>PPC_PCFG R023 (0x002E)</td><td>P023</td><td>GPIO_POD R0:POD23</td><td>-</td><td>SCS00</td><td>-</td></tr><tr><td>PPC_PCFG R024 (0x0030)</td><td>P024</td><td>GPIO_POD R0:POD24</td><td>-</td><td>-</td><td>SOUT4</td></tr><tr><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td></tr><tr><td>PPC_PCFG R027 (0x0036)</td><td>P027</td><td>GPIO_POD R0:POD27</td><td>TIOA4</td><td>SCS00</td><td>SCS42</td></tr></tbody></table>	Register (Offset)	Port	Resource Functional Outputs				POF=0	POF=1	POF=2	POF=3	PPC_PCFG R014 (0x001C)	P014	GPIO_POD R0:POD14	TIOA3	-	SOUT12	:	:	:	:	:	:	PPC_PCFG R020 (0x0028)	P020	GPIO_POD R0:POD20	-	SOUT0	-	:	:	:	:	:	:	PPC_PCFG R023 (0x002E)	P023	GPIO_POD R0:POD23	-	SCS00	-	PPC_PCFG R024 (0x0030)	P024	GPIO_POD R0:POD24	-	-	SOUT4	:	:	:	:	:	:	PPC_PCFG R027 (0x0036)	P027	GPIO_POD R0:POD27	TIOA4	SCS00	SCS42
Register (Offset)	Port	Resource Functional Outputs																																																										
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PPC_PCFG R014 (0x001C)	P014	GPIO_POD R0:POD14	TIOA3	-	SOUT12																																																							
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PPC_PCFG R020 (0x0028)	P020	GPIO_POD R0:POD20	-	SOUT0	-																																																							
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PPC_PCFG R023 (0x002E)	P023	GPIO_POD R0:POD23	-	SCS00	-																																																							
PPC_PCFG R024 (0x0030)	P024	GPIO_POD R0:POD24	-	-	SOUT4																																																							
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PPC_PCFG R027 (0x0036)	P027	GPIO_POD R0:POD27	TIOA4	SCS00	SCS42																																																							

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		Correct) <table><tr><th rowspan="2">Register (Offset)</th><th rowspan="2">Port</th><th colspan="4">Resource Functional Outputs</th></tr><tr><th>POF=0</th><th>POF=1</th><th>POF=2</th><th>POF=3</th></tr><tr><td>PPC_PCFG R014 (0x001C)</td><td>P014</td><td>GPIO_POD R0:POD14</td><td>TIOA3</td><td>-</td><td>SOT12</td></tr><tr><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td></tr><tr><td>PPC_PCFG R020 (0x0028)</td><td>P020</td><td>GPIO_POD R0:POD20</td><td>-</td><td>SOT0</td><td>-</td></tr><tr><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td></tr><tr><td>PPC_PCFG R023 (0x002E)</td><td>P023</td><td>GPIO_POD R0:POD23</td><td>-</td><td>SCS0</td><td>-</td></tr><tr><td>PPC_PCFG R024 (0x0030)</td><td>P024</td><td>GPIO_POD R0:POD24</td><td>-</td><td>-</td><td>SOT4</td></tr><tr><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td></tr><tr><td>PPC_PCFG R027 (0x0036)</td><td>P027</td><td>GPIO_POD R0:POD27</td><td>TIOA4</td><td>SCS0</td><td>SCS42</td></tr></table>	Register (Offset)	Port	Resource Functional Outputs				POF=0	POF=1	POF=2	POF=3	PPC_PCFG R014 (0x001C)	P014	GPIO_POD R0:POD14	TIOA3	-	SOT12	:	:	:	:	:	:	PPC_PCFG R020 (0x0028)	P020	GPIO_POD R0:POD20	-	SOT0	-	:	:	:	:	:	:	PPC_PCFG R023 (0x002E)	P023	GPIO_POD R0:POD23	-	SCS0	-	PPC_PCFG R024 (0x0030)	P024	GPIO_POD R0:POD24	-	-	SOT4	:	:	:	:	:	:	PPC_PCFG R027 (0x0036)	P027	GPIO_POD R0:POD27	TIOA4	SCS0	SCS42
Register (Offset)	Port	Resource Functional Outputs																																																										
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PPC_PCFG R014 (0x001C)	P014	GPIO_POD R0:POD14	TIOA3	-	SOT12																																																							
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PPC_PCFG R020 (0x0028)	P020	GPIO_POD R0:POD20	-	SOT0	-																																																							
:	:	:	:	:	:																																																							
PPC_PCFG R023 (0x002E)	P023	GPIO_POD R0:POD23	-	SCS0	-																																																							
PPC_PCFG R024 (0x0030)	P024	GPIO_POD R0:POD24	-	-	SOT4																																																							
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PPC_PCFG R027 (0x0036)	P027	GPIO_POD R0:POD27	TIOA4	SCS0	SCS42																																																							

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		PPC_PCFG R406 (0x010C)	P406	GPIO_POD R4:POD06	-	SOUT9	SDA9	DBG_TR ACEDAT A[3]	TX2
		PPC_PCFG R407 (0x010E)	P407	GPIO_POD R4:POD07	-	SCK9	SCK7	DBG_TR ACEDAT A[4]	-
		PPC_PCFG R408 (0x0110)	P408	GPIO_POD R4:POD08	-	-	-	DBG_TR ACEDAT A[5]	-
		PPC_PCFG R409 (0x0112)	P409	GPIO_POD R4:POD09	TIOA24	SOUT2	SDA2	DBG_TR ACEDAT A[6]	-
		:	:	:	:	:	:	:	:
		PPC_PCFG R411 (0x0116)	P411	GPIO_POD R4:POD11	-	SCK2	SCS71	DBG_TR ACEDAT A[7]	-
		:	:	:	:	:	:	:	:
PPC_PCFG R417 (0x0122)	P417	GPIO_POD R4:POD17	TIOA23	-	SOUT7	-	-		

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Revision History



Document Revision History

Document Title: S6J34x8/9/A 32-bit Microcontroller S6J3400 Series Hardware Manual Traveo™ Family		
Document Number: 002-09919		
Revision	ECN No.	Description of Change
**	5037429	New Specification
*A	5281295	Modified some sentences. For details, please see the chapter 28. Major Changes.
*B	5397944	For details, please see the chapter 28. Major Changes.
*C	5610276	For details, please see the chapter 27. Major Changes.
*D	5803557	Modified some sentences. For details, please see the chapter 28. Major Changes.
*E	5936417	Modified some sentences. For details, please see the chapter 28. Major Changes.
*F	6962248	Modified some sentences. For details, please see the chapter 28. Major Changes.