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S6J3400 Series

32-bit Arm® Cortex®-R5F TRAVEO™ T1G Microcontroller

S6J3400 is a series of microcontrollers targeted at automotive systems such as body control units. This embedded device enables next-generation functions such as Controller Area Network with Flexible Data rate (CAN FD) and Secure Hardware Extension (SHE). Automotive body control applications require a flexible product line-up to meet various specifications. The S6J3400 product portfolio meets these requirements.

Features

Key Features

- 132-MHz operation frequency for S6J3428/9/A
- 80-MHz internal program flash memory access speed
- 2.7-V to 5.5-V power supply voltage range
- 64-channel 12-bit A/D converter with 1 Msps conversion rate
- Embedded 6-channel CAN FD controller
- 14-channel Multi-Function Serial (MFS) communication block for S6J3428/9/A
- Embedded SHE
- Low standby current in Partial Wake Up mode
- 125 °C operating temperature
- Low power consumption
- Flash memory retention time up to 20 years
- ASIL-B support on ISO26262 specification
- 176-pin, 144-pin, and 100-pin packages
- Power domain control

Applications

- Overall automotive body application
- Heating, Ventilation, and Air Conditioning (HVAC)
- Body Control Module (BCM)
- Gateway
- Collision Warning
- Lighting

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1. Features

1.1 Function List

The following table shows the functions that are implemented in the S6J3400 series.

Function	S6J34xxJxx	S6J34xxHxx	S6J34xxFxx	Remark
CPU core	Arm Cortex R5F			
FPU	Available			
PPU	Available			
MPU	Available			
TPU	Available			
Endian	Little endian			
Core clock frequency	132 MHz			See the AC specifications in this datasheet
HPM bus frequency	33 MHz			See the AC specifications in this datasheet
LLPM bus frequency	33 MHz			See the AC specifications in this datasheet
Resource clock frequency	40 MHz (Max)			
Embedded CR oscillation	Slow clock: 100 kHz Fast clock: 4 MHz (Center frequency)			See the AC specifications in this datasheet
PLL	PLL0			
SSCG PLL	SSCG0			
Clock supervisor	Available			
DMA	16 ch			
Boot-ROM	16 KB			
JTAG	Available			
Data cache	16 KB			
Instruction cache	16 KB			
Program Flash	Option			See Section 1.2.1
Work Flash	112 KB			
TC-RAM	Option			See Section 1.2.1
System-RAM	Option			See Section 1.2.1
Backup area in System-RAM	Option			See Section 1.2.1
Security (SHE)	Option			See Section 1.2.1
Low latency interrupt	Available			
Power domain	3 domains			
Power supply	5.0 V $\pm$ 0.5 V or 3.3 V $\pm$ 0.3 V			See the AC specifications in this datasheet

Function	S6J34xxJxx	S6J34xxHxx	S6J34xxFxx	Remark
Embedded LDO power supply for 5.0 V	Available			
Low-voltage detection of external power supply	Available			
Low-voltage detection of internal LDO output	Available			
Hardware watchdog timer	Available			
Software watchdog timer	Available			
Package	Option			See Section 1.2.1
General-purpose I/O	Option			See Section 1.2.3
Up/down counter	2 ch			
I/O timer	FRT 8 ch, ICU 12 ch, OCU 12 ch			S6J3428/9/A
32-bit reload timer	6 ch			
Real-time clock	Available			Automatic calibration
Base timer	64 ch	60 ch	48 ch	With output pin or input pin
	64 ch	55 ch	40 ch	With output pin
	64 ch	57 ch	30 ch	With input pin
12-bit-A/D converter	64 ch 32 ch+32 ch	56 ch 24 ch+32 ch	35 ch 15 ch+20 ch	See Section 1.2.3
Partial Wake Up	Analog input 8 ch	Analog input 8 ch	Analog input 7 ch	Trigger 1 ch
CRC	4 ch			
Programmable CRC	1 ch			
Source clock timer	4 ch			
NMI	Available			
External interrupt	32 ch			See the AC specifications in this datasheet
Internal interrupt	256 vectors			
Multi-function serial interface	14 ch	13 ch	13 ch	S6J3428/9/A
	14 ch	13 ch	12 ch	with CS pin
CAN FD	6 ch			
CAN FD RAM (ECC supported)	16 KB/ch It is equivalent to 192 message buffer per channel of CAN module			

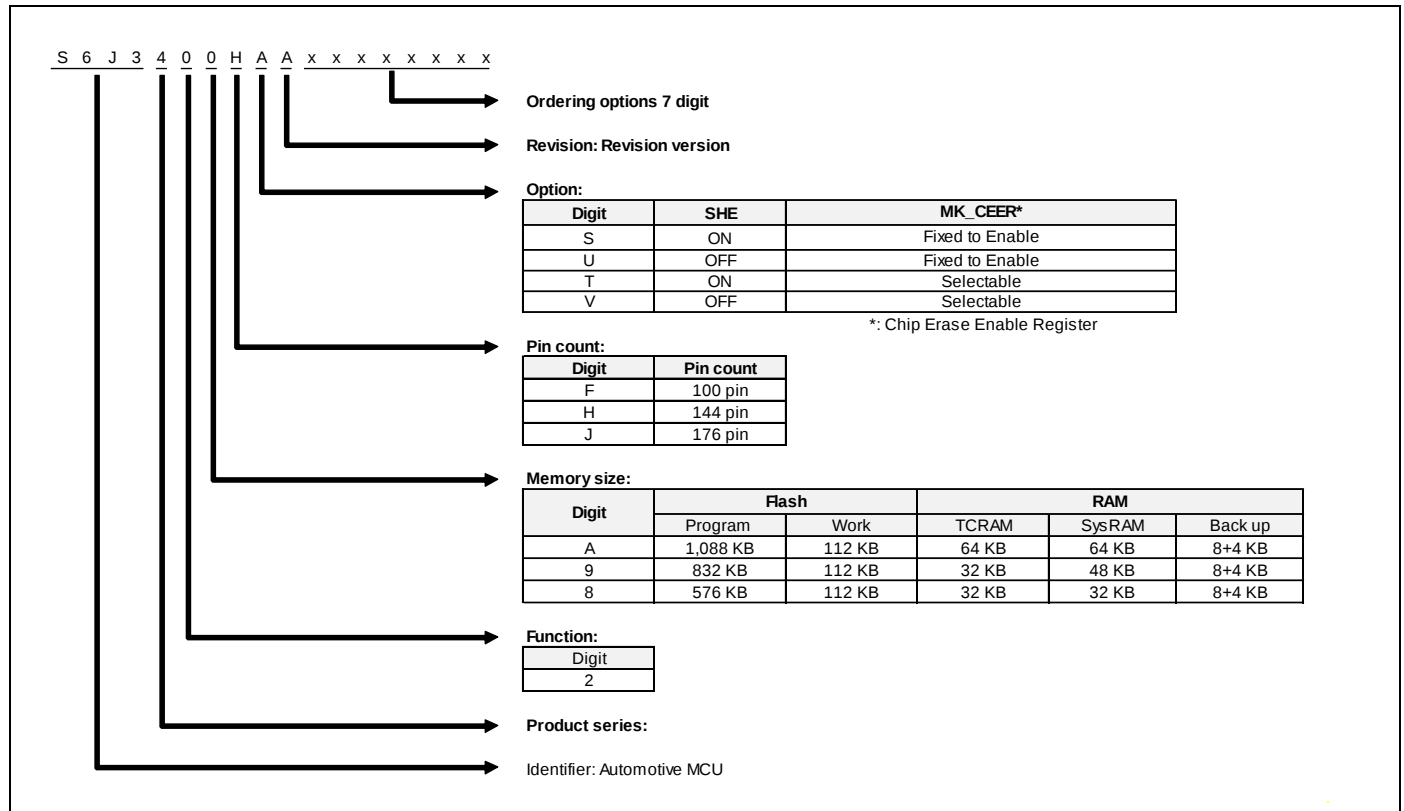
Notes:

- The options are described in Section 1.2.
- The specifications in the table that are related to electrical characteristics only show the typical values. They do not necessarily include the width of characteristics, errors, and so on. The details are described in "Recommended Operating Conditions".
- Some functions have restrictions. For details, see the "Restriction" section in the "Product Description" chapter in the S6J3400 Series hardware manual.

1.2 Optional Function

1.2.1 Basic Option

The following figure shows the optional functions and the part number relations of the series.



Note:

- This table only shows the relation between the optional function and the part numbers; that is, all products are not necessarily available for orders. See the "Ordering Information" in this datasheet and confirm product availability.

1.2.2 ID

ID is specified for each memory size digit, option digit, and revision.

Memory size	Option	Revision	Chip ID	JTAG ID	SHE Module ID (SHE_MID) *
A	S	A	0x10130100	0x002005CF	0x000F_0300
A	U	A		0x002015CF	
A	T	A		0x002065CF	
A	V	A		0x002075CF	
9	S	A		0x002025CF	
9	U	A		0x002035CF	
9	T	A		0x002085CF	
9	V	A		0x002095CF	
8	S	A		0x002045CF	
8	U	A		0x002055CF	
8	T	A		0x0020A5CF	
8	V	A		0x0020B5CF	
A	S	B		0x102005CF	
A	U	B		0x102015CF	
A	T	B		0x102065CF	
A	V	B		0x102075CF	
9	S	B		0x102025CF	
9	U	B		0x102035CF	
9	T	B		0x102085CF	
9	V	B		0x102095CF	
8	S	B		0x102045CF	
8	U	B		0x102055CF	
8	T	B		0x1020A5CF	
8	V	B		0x1020B5CF	

* See "SHE Module ID Register" in the "Secure Hardware Extension (SHE)" chapter in the TRAVEO™ T1G Platform hardware manual for details.

1.2.3 Function Table

Specification	176-Pin	144-Pin	100-Pin
FRT	8 ch	7 ch - internal 8 ch	
ADC	64 ch - 32+32 ch	56 ch - 24+32 ch	35 ch - 15+20 ch
Base Timer	64 ch ch. with - both in/out : 64 ch	60 ch ch. with - output : 55 ch - input : 57 ch - both : 52 ch	48 ch ch. with - output : 40 ch - input : 30 ch - both : 22 ch
MFS	14 ch w/ 14 ch CS	13 ch w/ 13 ch CS	13 ch w/ 12 ch CS
I ² C	14 ch - 400 kbps 2 ch	13 ch - 400 kbps 2 ch	
GPIO	151 149 : w/ subclk	119 117 : w/ subclk	75 73 : w/subclk

1.2.4 Restriction

Some functions have restrictions depending on package pin counts.

Function	LQFP-144	LQFP-100
Analog input port (12-bit ADC)	AN001 to 002, AN007, AN012, AN015 to 016, AN023 to 024 (56 ports)	AN001 to 002, AN004, AN006 to 007, AN009, AN011 to 012, AN015 to 016, AN018, AN020, AN023 to 024, AN026, AN029, AN031, AN101, AN103 to 105, AN115 to 117, AN122, AN124, AN126, AN130 to 131 (35 ports)
General-Purpose I/O	P002, P004, P011, P014, P025 to 026, P102, P104, P110 to 111, P116, P121, P124 to 125, P200 to 201, P216 to 217, P221, P303, P310 to 311, P316, P320, P325 to 326, P328 to 329, P410, P412, P415, P419	P000, P002 to P004, P008 to P009, P011, P014, P017 to 019, P023 to 026, P030, P101 to 102, P104, P110 to 111, P113, P115 to 116, P118, P120 to 121, P124 to 125, P127, P129, P200 to 201, P203, P206, P208, P210, P212, P216 to 219, P221, P230 to 231, P300, P303, P306, P308, P310 to 312, P316 to 320, P325 to 326, P328 to 330, P403 to 404, P406 to 408, P410 to 412, P414 to 415, P417 to 419, P421
BaseTimer	TIOA0/1/2/3_1 TIOA14/15/16/17/18_0 TIOA21/25/26/27_1 TIOA51/57/58/59/61_0 TIOB56/57/58/59/60/61/62_0	TIOA0/1_0 TIOA0/1/2/3/5_1 TIOA9/10/13_1 TIOA7/8/14/15/16/17/18/19_0 TIOB0/4/5/8/10/12_0 TIOB14/15/19/22/23_0 TIOA21/26/27/28_0 TIOA21/23/25/26/27/28_1 TIOA49/51/53/56/57/58/59/60_0 TIOA61/62/63_0 TIOB24/25/29/33/35/37/38_0 TIOB43/44/46/47/48/49_0 TIOB51/53/56/57/58/59/60_0 TIOB61/62/63_0
FRT	TEXT10_0	TEXT0/2/3/10_0, TEXT1/4_1
External interrupt	INT10/13/15_0, INT23/25/26_1, INT1_2	INT6/9/10_0, INT12/13/14/15_0, INT0/5_1, INT11/12/13/15/16/19_1, INT20/22/23/25/26/27_1, INT31_1, INT1/4/5_2, INT11/12_2
Partial Wake Up	PWUTRG_0	PWU_AN7 PWUTRG_0
CAN-FD	-	TX0_0, RX1_1, TX1_1 TX2_1

Function	LQFP-144	LQFP-100
Multi-function serial	SCS21_1, SCS23_0, SCS23_1, SCS40_1, SCS41_1, SCS52_0, SIN6_1, SOT6_1, SCS70_1, SCS72_1, SCS110_0, SIN12_0, SIN12_1, SOT12_1, SCK13_0, SIN13_0, SOT13_0, SCS130_0	SCS0_0, SCK2_0, SIN2_0, SIN2_1, SOT2_1, SCS21_0, SCS21_1, SCS22_0, SCS22_1, SCS23_0, SCS23_1, SCS30_0, SIN4_0, SIN4_1, SOT4_1, SCS40_1, SCS41_0, SCS41_1, SCS42_0, SCS43_0, SCS43_1, SCS50_1, SCS52_0, SIN6_1, SOT6_1, SCS60_2, SCS61_0, SCK7_1, SIN7_0, SIN7_2, SOT7_1, SCS70_1, SCS71_0, SCS71_1, SCS72_1, SCS73_0, SIN8_0, SCS83_0, SCK9_0, SOT9_0, SCS90_1, SCS101_0, SCS102_0, SCS103_0, SOT11_1, SCS110_0, SCK12_0, SIN12_0, SIN12_1, SOT12_1, SCS120_1, SCK13_0, SIN13_0, SOT13_0, SCS130_0
I ² C	SCL13_0, SDA13_0	SCL2_0, SCL9_0, SDA9_0, SCL12_0, SCL13_0, SDA13_0
Input capture	-	1N2/3_0, 1N0/2_1, IN0/2_2, IN19/20_0, IN16/20_1
Output compare	-	OUT1/2/3_0, OUT2/5_1, OUT19/20/21_0
Quad Position & Revolution Counter	-	AIN8_0, AIN8_1, ZIN8_0
Reload timer	-	TOT2_0, TOT3_0, TOT16_0, TOT17_0
Trace	-	TRACECTL_0, TRACEDATA0/1/3/4/5/7_0

Notes:

- See multiplexed functions on the pin assignment sheet.
- The restrictions of functions, other than those above, are described in the S6J3400 Series hardware manual. For details, see the "Restriction" section in the "Product Description" chapter in the S6J3400 Series hardware manual.
- The optional restriction will be added without notification.

2. Precautions and Handling Devices

2.1 Handling Precautions

All semiconductor devices have inherently a certain rate of failure. The possibility of failure is affected by the conditions in which they are used (circuit conditions, environmental conditions, and so on). This section describes precautions that you must take to minimize the chance of failure and to obtain higher reliability from your semiconductor devices.

2.1.1 Precautions for Product Design

This section describes precautions to take when you design electronic equipment using semiconductor devices.

Absolute Maximum Ratings

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, and so on) in excess of certain established limits, called absolute maximum ratings. Do not exceed these ratings.

Recommended Operating Conditions

Always use semiconductor devices within the recommended operating conditions, which are the normal operating ranges for semiconductor devices. All the device's electrical characteristics are warranted when operated within these ranges.

Operation outside these ranges may adversely affect reliability and can result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the datasheet. Users considering application outside the listed conditions are advised to contact their sales representative.

Processing and Protection of Pins

Follow these precautions when handling the pins, which connect semiconductor devices to power supply and input/output functions.

1. Preventing Overvoltage and Overcurrent Conditions

Exposure to voltage or current levels in excess of maximum ratings at any pin may cause deterioration within the device, and in extreme cases lead to permanent damage of the device. Try to prevent such overvoltage or overcurrent conditions at the design stage.

2. Protection of Output Pins

Shorting of output pins to supply pins or other output pins, or connection to large capacitance can cause large current flows. Such conditions, if present for extended periods of time, can damage the device. Therefore, avoid this type of connection.

3. Handling of Unused Input Pins

Unconnected input pins, with very high impedance levels, can adversely affect stability of operation. Such pins should be connected through an appropriate resistance to a power supply pin or ground pin.

2.1.2 Precautions for Package Mounting

Package mounting may be either lead-insertion type or surface-mount type. In either case, for heat resistance during soldering, mount only under the recommended conditions. For detailed information about mount conditions, contact your sales representative.

Lead-Insertion Type

You can mount lead-insertion type packages on printed circuit boards using two methods: direct soldering on the board or mounting by using a socket.

1. Direct mounting on boards normally involves processes for inserting leads into through-holes on the board and using the flow soldering (wave soldering) method of applying liquid solder. In this case, the soldering process usually causes leads to be subjected to thermal stress in excess of the absolute ratings for storage temperature. Mounting processes should conform to recommended mounting conditions.
2. If socket mounting is used, differences in surface treatment of the socket contacts and IC lead surfaces can lead to contact deterioration after long periods. For this reason, it is recommended that you verify the surface treatment of socket contacts and IC leads before mounting.

Surface-Mount Type

Surface-mount packaging has longer and thinner leads than the lead-insertion packaging, and therefore, leads are more easily deformed or bent. The use of packages with higher pin counts and narrower pin pitch results in increased susceptibility to open connections caused by deformed pins, or shorting due to solder bridges.

Use appropriate mounting techniques. Cypress recommends the solder reflow method, and has established a ranking of mounting conditions for each product. Users are advised to mount packages in accordance with the Cypress ranking of recommended conditions.

Storage of Semiconductor Devices

Because plastic chip packages are formed from plastic resins, exposure to natural environmental conditions causes absorption of moisture. During mounting, the application of heat to a package that has absorbed moisture can cause surfaces to peel, reducing moisture resistance and causing packages to crack. To prevent, do the following:

1. Avoid exposure to rapid temperature changes, which cause moisture to condense inside the product. Store products in locations where temperature changes are slight.
2. Use dry boxes for product storage. Products should be stored below 70 percent relative humidity, and at temperatures between 5 °C and 30 °C. The recommended humidity for dry packages are from 40 percent to 70 percent.
3. When necessary, Cypress packages semiconductor devices in highly moisture-resistant aluminum laminate bags, with a silica gel desiccant. Devices should be sealed in their aluminum laminate bags for storage.
4. Avoid storing packages where they are exposed to corrosive gases or high levels of dust.

Baking

Packages that have absorbed moisture may be de-moisturized by baking (heat drying). Follow the recommended conditions for baking.

Condition: 125 °C/24 h

Static Electricity

Because semiconductor devices are particularly susceptible to damage by static electricity, follow these precautions:

1. Maintain relative humidity in the working environment between 40 percent and 70 percent.
You may need an apparatus for ion generation to remove electricity.
2. Electrically ground all conveyors, solder vessels, soldering irons, and peripheral equipment.
3. Eliminate static body electricity by the use of rings or bracelets connected to ground through high resistance (on the level of 1 MΩ). Wearing of conductive clothing and shoes, use of conductive floor mats, and other measures to minimize shock loads is recommended.
4. Ground all fixtures and instruments or protect with anti-static measures.
5. Avoid the use of Styrofoam or other highly static-prone materials for storage of completed board assemblies.

2.1.3 Precautions for Use Environment

Reliability of semiconductor devices depends on ambient temperature and other conditions as described above.

For reliable performance, do the following:

1. Humidity
Prolonged use in high humidity can lead to leakage in devices as well as printed circuit boards. If high humidity levels are anticipated, consider anti-humidity processing.
2. Discharge of Static Electricity
When high-voltage charges exist close to semiconductor devices, discharges can cause abnormal operation. In such cases, use anti-static measures or processing to prevent discharges.
3. Corrosive Gases, Dust, or Oil
Exposure to corrosive gases or contact with dust or oil may lead to chemical reactions that will adversely affect the device. If you use devices in such conditions, consider ways to prevent such exposure or to protect the devices.

4. Radiation, Including Cosmic Radiation

Most devices are not designed for environments involving exposure to radiation or cosmic radiation. Provide shielding as appropriate.

5. Smoke and Flame

CAUTION: Plastic molded devices are flammable, and therefore should not be used near combustible substances. If devices begin to smoke or burn, there is a danger of the release of toxic gases.

Customers considering the use of Cypress products in other special environmental conditions should consult with our sales representatives.

3. Handling Devices

Latch-Up Prevention

The latch-up phenomenon may occur on a CMOS IC in the following cases: the voltage applied to an input or output pin is higher than VCC or lower than VSS; or the voltage applied between a VCC pin and a VSS pin exceeds the rating. A latch-up causes a rapid increase in the power supply current, possibly resulting in thermal damage to an element. When using the device, take sufficient care not to exceed the maximum rating.

Also be careful that analog power supplies (AVCC0, AVCC1, AVRHO, and AVRH1) and analog inputs do not exceed the digital power supply (VCC) at the analog system power-on and power-off times. The power-on sequence is as follows. Simultaneously turn on the digital supply voltage (VCC) and analog supply voltages (AVCC0, AVCC1, AVRHO, AVRH1), or turn on the digital supply voltage (VCC) and then the analog supply voltages (AVCC0, AVCC1, AVRHO, AVRH1).

Handling Unused Pins

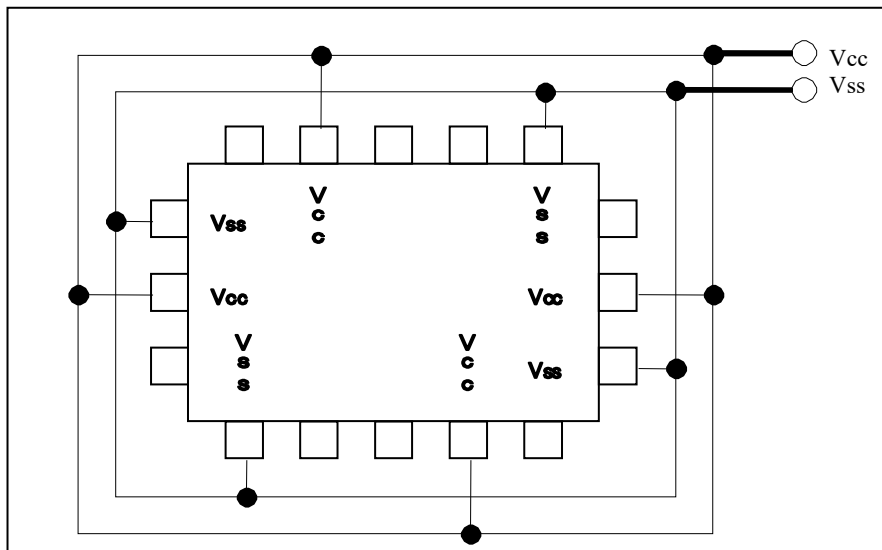
Leaving unused input pins open may cause permanent damage from a malfunction or latch-up. Take measures, such as pulling up or pulling down the voltage with resistors of 2 kΩ or higher, for unused pins.

If there are any unused input/output pins, set them to the output state and then open them, or set them to the input state and handle them in the same way as input pins.

Power Supply Pins

If the device has multiple VCC and VSS pins, the device is designed in such a way that the pins of the same potential are connected to each other inside the device to prevent malfunctions such as latch-up. However, to reduce unwanted emissions, prevent malfunctions of strobe signals caused by an increase of the ground level, and observe standards on total output current, be sure to connect all the VCC and VSS pins to the power source and ground externally. Also, handle all the VSS power supply pins as shown in the following diagram. If there are multiple VCC or VSS systems, the device does not operate normally even within the guaranteed operating range.

Figure 3-1 Pin Assignment



In addition, consider connecting with low impedance from the power supply source to the VCC and VSS of this device.

We recommend connecting a ceramic capacitor as a bypass capacitor between VCC and VSS, near this device.

Crystal Oscillation Circuit

Noise entering the X0 or X1 pin may cause a malfunction. Design the printed circuit board in such a way that the X0 and X1 pins, the crystal oscillator (or ceramic resonator), and a bypass capacitor to ground are located very close to the device.

We recommend that the printed circuit board artwork have the X0 and X1 pins enclosed by ground.

Mode Pin (MD)

Use mode pin MD by directly connecting it to a VCC or VSS pin. To prevent noise from causing the device to accidentally enter test mode, reduce the pattern length between each mode pin and a VCC or VSS pin on the printed circuit board, and connect them with low impedance.

PLL Clock Operation

While a PLL clock is selected, if the oscillator breaks off or input stops, the PLL clock may continue operating with the free running frequency of the internal self-oscillator circuit. This operation is outside of the guaranteed range.

Power Supply Pin Processing of an A/D Converter

Even when no A/D converter is used, establish a connection such that $AVCC0=AVCC1=AVRH0=AVRH1=VCC$ and $AVSS0=AVSS1=VSS$.

Points to Note about Using External Clocks

External clocks are not supported.

External direct clock input cannot be used.

Power-on Sequence of the Power Supply Analog Inputs of an A/D Converter

Be sure to turn on the digital power supply (VCC) before the application of the power supplies ($AVCC0$, $AVCC1$, $AVRH0$, and $AVRH1$) and analog inputs ($AN000$ to $AN031$ and $AN100$ to $AN131$) of an A/D converter. At the power-off time, turn off the power supplies and analog inputs of the A/D converter, and then turn off the digital power supply (VCC). Perform these power-on and power-off operations without $AVRH0/1$ exceeding $AVCC0/1$. Even when using a pin shared with an analog input as an input port, do not allow the input voltage to exceed $AVCC0/1$. (Turning on or off the analog supply voltage and digital supply voltage simultaneously is not a problem.)

C-Pin Processing

This device has a built-in voltage step-down circuit. Be sure to connect a capacitor to the C pin (see pin assignment) for internal stabilization of the device. For the standard values, see "Recommended operating conditions" in the latest datasheet.

Writing to a Register Containing a Status Flag

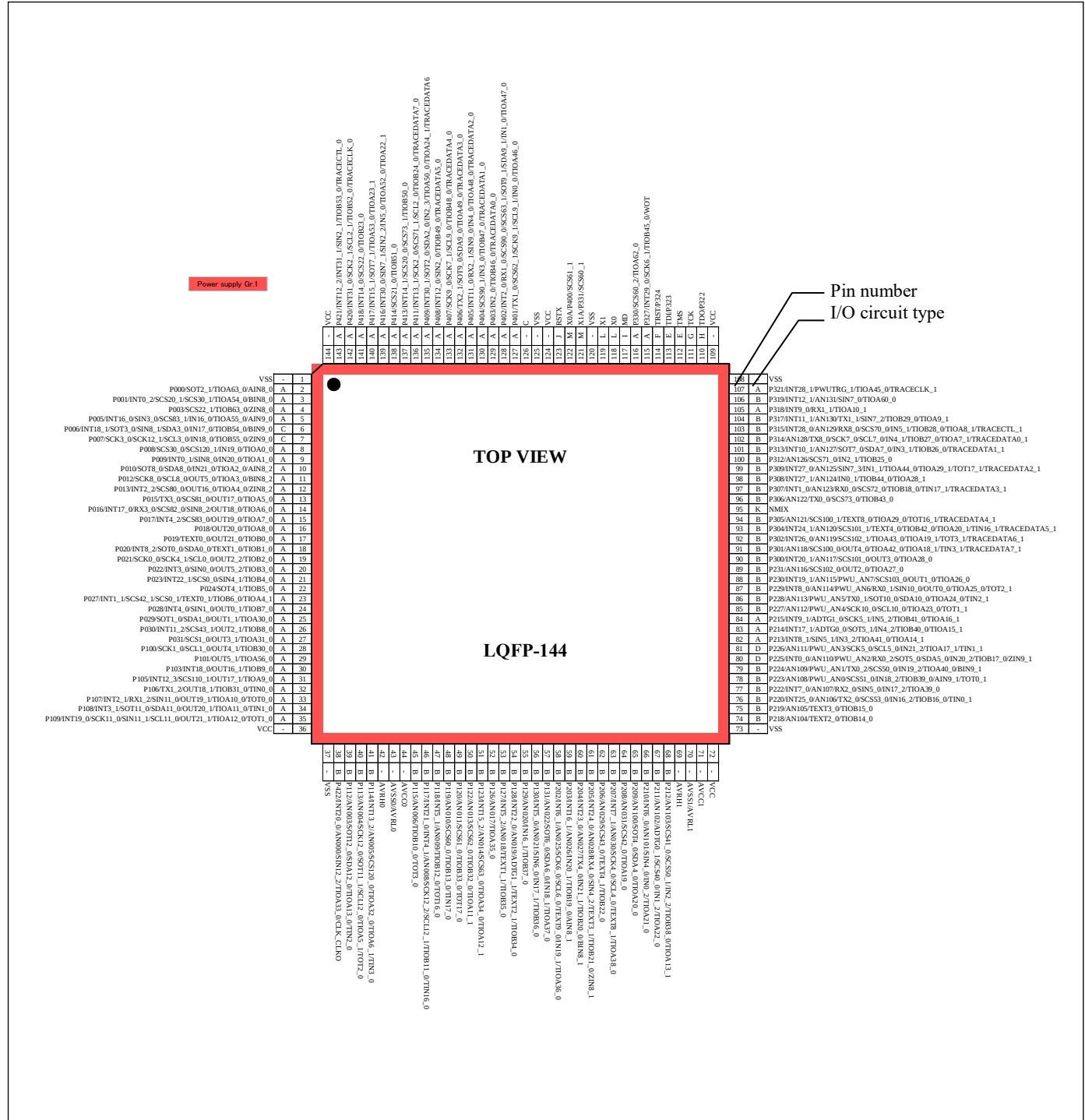
In writing to a register containing a status flag (such as an interrupt request flag) to control a function, take care not to accidentally clear the status flag. Therefore, before the write operation, configure the status bit such that the flag is not cleared, and then set the control bit to the desired value. Especially for control bits configured as a set of multiple bits, bit instructions cannot be used (bit instructions have only 1-bit access). In such cases, byte, half-word, or word access is used to write to the control bits and a status flag simultaneously. However, at this time, be careful not to accidentally clear bits other than the intended ones (the status flag bit in this case).

Note: Bit instructions take this point into consideration for registers that support bit-band units, so it is not a concern. You need to take care when using bit instructions for registers that do not support bit-band units.

Figure 4-1 TEQFP-176

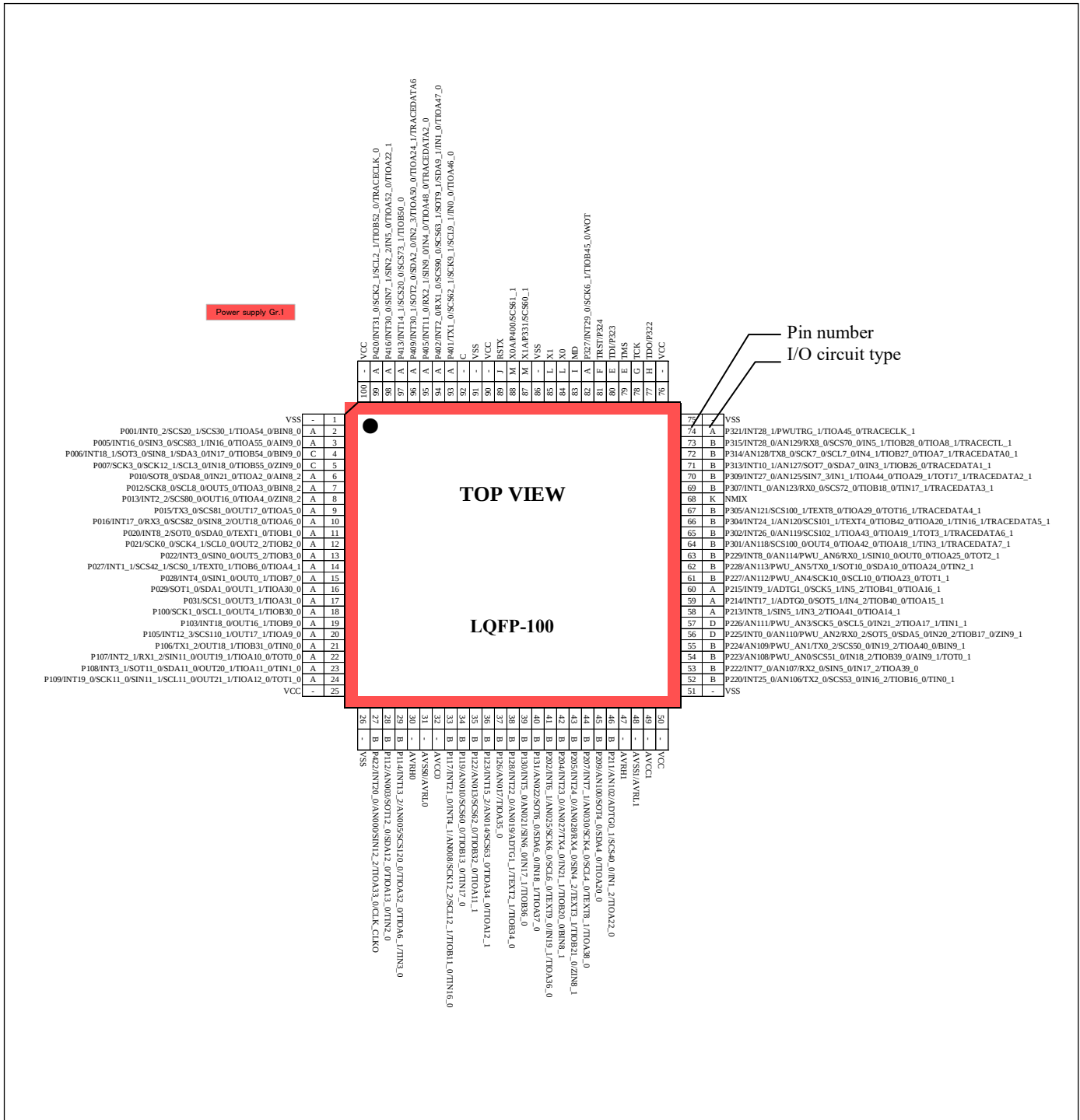
4.2 LQFP-144 Pin Assignment

Figure 4-2 LQFP-144



4.3 LQFP-100 Pin Assignment

Figure 4-3 LQFP-100



5. Pin Descriptions

5.1 Pin Descriptions

Table 5-1 Pin Descriptions

Port Name	Description	Pin No. of Package			Remark
		LQFP 100	LQFP 144	TEQFP 176	
MD	Mode pin	83	117	145	
RSTX	External reset input pin	89	123	151	
NMIX	Non-maskable interrupt input pin	68	95	115	
X0	Main clock oscillation input pin	84	118	146	
X1	Main clock oscillation output pin	85	119	147	
X0A	Sub clock oscillation input pin	88	122	150	
X1A	Sub clock oscillation output pin	87	121	149	
INT0_0	External interrupt ch.0 input pin (0)	56	80	99	
INT0_1	External interrupt ch.0 input pin (1)	-	9	11	
INT0_2	External interrupt ch.0 input pin (2)	2	3	3	
INT1_0	External interrupt ch.1 input pin (0)	69	97	117	
INT1_1	External interrupt ch.1 input pin (1)	14	23	29	
INT1_2	External interrupt ch.1 input pin (2)	-	-	13	
INT2_0	External interrupt ch.2 input pin (0)	94	128	156	
INT2_1	External interrupt ch.2 input pin (1)	22	33	41	
INT2_2	External interrupt ch.2 input pin (2)	8	12	15	
INT3_0	External interrupt ch.3 input pin (0)	13	20	24	
INT3_1	External interrupt ch.3 input pin (1)	23	34	42	
INT4_0	External interrupt ch.4 input pin (0)	15	24	30	
INT4_1	External interrupt ch.4 input pin (1)	33	46	57	
INT4_2	External interrupt ch.4 input pin (2)	-	15	19	
INT5_0	External interrupt ch.5 input pin (0)	39	56	70	
INT5_1	External interrupt ch.5 input pin (1)	-	47	58	
INT5_2	External interrupt ch.5 input pin (2)	-	53	67	
INT6_0	External interrupt ch.6 input pin (0)	-	66	82	
INT6_1	External interrupt ch.6 input pin (1)	41	58	74	
INT7_0	External interrupt ch.7 input pin (0)	53	77	96	
INT7_1	External interrupt ch.7 input pin (1)	44	63	79	
INT8_0	External interrupt ch.8 input pin (0)	63	87	106	
INT8_1	External interrupt ch.8 input pin (1)	58	82	101	
INT8_2	External interrupt ch.8 input pin (2)	11	18	22	
INT9_0	External interrupt ch.9 input pin (0)	-	105	128	
INT9_1	External interrupt ch.9 input pin (1)	60	84	103	

Port Name	Description	Pin No. of Package			Remark
		LQFP 100	LQFP 144	TEQFP 176	
INT10_0	External interrupt ch.10 input pin (0)	-	-	139	
INT10_1	External interrupt ch.10 input pin (1)	71	101	123	
INT11_0	External interrupt ch.11 input pin (0)	95	131	159	
INT11_1	External interrupt ch.11 input pin (1)	-	104	127	
INT11_2	External interrupt ch.11 input pin (2)	-	26	32	
INT12_0	External interrupt ch.12 input pin (0)	-	134	162	
INT12_1	External interrupt ch.12 input pin (1)	-	106	129	
INT12_2	External interrupt ch.12 input pin (2)	-	143	175	
INT12_3	External interrupt ch.12 input pin (3)	20	31	39	
INT13_0	External interrupt ch.13 input pin (0)	-	-	169	
INT13_1	External interrupt ch.13 input pin (1)	-	136	165	
INT13_2	External interrupt ch.13 input pin (2)	29	41	51	
INT14_0	External interrupt ch.14 input pin (0)	-	141	172	
INT14_1	External interrupt ch.14 input pin (1)	97	137	167	
INT15_0	External interrupt ch.15 input pin (0)	-	-	120	
INT15_1	External interrupt ch.15 input pin (1)	-	140	171	
INT15_2	External interrupt ch.15 input pin (2)	36	51	63	
INT16_0	External interrupt ch.16 input pin (0)	3	5	7	
INT16_1	External interrupt ch.16 input pin (1)	-	59	75	
INT17_0	External interrupt ch.17 input pin (0)	10	14	18	
INT17_1	External interrupt ch.17 input pin (1)	59	83	102	
INT18_0	External interrupt ch.18 input pin (0)	19	30	37	
INT18_1	External interrupt ch.18 input pin (1)	4	6	8	
INT19_0	External interrupt ch.19 input pin (0)	24	35	43	
INT19_1	External interrupt ch.19 input pin (1)	-	88	107	
INT20_0	External interrupt ch.20 input pin (0)	27	38	46	
INT20_1	External interrupt ch.20 input pin (1)	-	90	109	
INT21_0	External interrupt ch.21 input pin (0)	33	46	57	
INT22_0	External interrupt ch.22 input pin (0)	38	54	68	
INT22_1	External interrupt ch.22 input pin (1)	-	21	25	
INT23_0	External interrupt ch.23 input pin (0)	42	60	76	
INT23_1	External interrupt ch.23 input pin (1)	-	-	48	
INT24_0	External interrupt ch.24 input pin (0)	43	61	77	
INT24_1	External interrupt ch.24 input pin (1)	66	93	113	
INT25_0	External interrupt ch.25 input pin (0)	52	76	94	
INT25_1	External interrupt ch.25 input pin (1)	-	-	64	

Port Name	Description	Pin No. of Package			Remark
		LQFP 100	LQFP 144	TEQFP 176	
INT26_0	External interrupt ch.26 input pin (0)	65	92	111	
INT26_1	External interrupt ch.26 input pin (1)	-	-	143	
INT27_0	External interrupt ch.27 input pin (0)	70	99	119	
INT27_1	External interrupt ch.27 input pin (1)	-	98	118	
INT28_0	External interrupt ch.28 input pin (0)	73	103	125	
INT28_1	External interrupt ch.28 input pin (1)	74	107	131	
INT29_0	External interrupt ch.29 input pin (0)	82	115	141	
INT30_0	External interrupt ch.30 input pin (0)	98	139	170	
INT30_1	External interrupt ch.30 input pin (1)	96	135	163	
INT31_0	External interrupt ch.31 input pin (0)	99	142	174	
INT31_1	External interrupt ch.31 input pin (1)	-	143	175	
ADTG0_0	ADC unit0 external trigger input pin (0)	59	83	102	
ADTG0_1	ADC unit0 external trigger input pin (1)	46	67	83	
ADTG1_0	ADC unit1 external trigger input pin (0)	60	84	103	
ADTG1_1	ADC unit1 external trigger input pin (1)	38	54	68	
AN000	ADC unit0 ch.0 analog input pin	27	38	46	
AN001	ADC unit0 ch.1 analog input pin	-	-	47	
AN002	ADC unit0 ch.2 analog input pin	-	-	48	
AN003	ADC unit0 ch.3 analog input pin	28	39	49	
AN004	ADC unit0 ch.4 analog input pin	-	40	50	
AN005	ADC unit0 ch.5 analog input pin	29	41	51	
AN006	ADC unit0 ch.6 analog input pin	-	45	55	
AN007	ADC unit0 ch.7 analog input pin	-	-	56	
AN008	ADC unit0 ch.8 analog input pin	33	46	57	
AN009	ADC unit0 ch.9 analog input pin	-	47	58	
AN010	ADC unit0 ch.10 analog input pin	34	48	59	
AN011	ADC unit0 ch.11 analog input pin	-	49	60	
AN012	ADC unit0 ch.12 analog input pin	-	-	61	
AN013	ADC unit0 ch.13 analog input pin	35	50	62	
AN014	ADC unit0 ch.14 analog input pin	36	51	63	
AN015	ADC unit0 ch.15 analog input pin	-	-	64	
AN016	ADC unit0 ch.16 analog input pin	-	-	65	
AN017	ADC unit0 ch.17 analog input pin	37	52	66	
AN018	ADC unit0 ch.18 analog input pin	-	53	67	
AN019	ADC unit0 ch.19 analog input pin	38	54	68	
AN020	ADC unit0 ch.20 analog input pin	-	55	69	

Port Name	Description	Pin No. of Package			Remark
		LQFP 100	LQFP 144	TEQFP 176	
AN021	ADC unit0 ch.21 analog input pin	39	56	70	
AN022	ADC unit0 ch.22 analog input pin	40	57	71	
AN023	ADC unit0 ch.23 analog input pin	-	-	72	
AN024	ADC unit0 ch.24 analog input pin	-	-	73	
AN025	ADC unit0 ch.25 analog input pin	41	58	74	
AN026	ADC unit0 ch.26 analog input pin	-	59	75	
AN027	ADC unit0 ch.27 analog input pin	42	60	76	
AN028	ADC unit0 ch.28 analog input pin	43	61	77	
AN029	ADC unit0 ch.29 analog input pin	-	62	78	
AN030	ADC unit0 ch.30 analog input pin	44	63	79	
AN031	ADC unit0 ch.31 analog input pin	-	64	80	
AN100	ADC unit1 ch.0 analog input pin	45	65	81	
AN101	ADC unit1 ch.1 analog input pin	-	66	82	
AN102	ADC unit1 ch.2 analog input pin	46	67	83	
AN103	ADC unit1 ch.3 analog input pin	-	68	84	
AN104	ADC unit1 ch.4 analog input pin	-	74	92	
AN105	ADC unit1 ch.5 analog input pin	-	75	93	
AN106	ADC unit1 ch.6 analog input pin	52	76	94	
AN107	ADC unit1 ch.7 analog input pin	53	77	96	
AN108	ADC unit1 ch.8 analog input pin	54	78	97	
AN109	ADC unit1 ch.9 analog input pin	55	79	98	
AN110	ADC unit1 ch.10 analog input pin	56	80	99	
AN111	ADC unit1 ch.11 analog input pin	57	81	100	
AN112	ADC unit1 ch.12 analog input pin	61	85	104	
AN113	ADC unit1 ch.13 analog input pin	62	86	105	
AN114	ADC unit1 ch.14 analog input pin	63	87	106	
AN115	ADC unit1 ch.15 analog input pin	-	88	107	
AN116	ADC unit1 ch.16 analog input pin	-	89	108	
AN117	ADC unit1 ch.17 analog input pin	-	90	109	
AN118	ADC unit1 ch.18 analog input pin	64	91	110	
AN119	ADC unit1 ch.19 analog input pin	65	92	111	
AN120	ADC unit1 ch.20 analog input pin	66	93	113	
AN121	ADC unit1 ch.21 analog input pin	67	94	114	
AN122	ADC unit1 ch.22 analog input pin	-	96	116	
AN123	ADC unit1 ch.23 analog input pin	69	97	117	
AN124	ADC unit1 ch.24 analog input pin	-	98	118	

Port Name	Description	Pin No. of Package			Remark
		LQFP 100	LQFP 144	TEQFP 176	
AN125	ADC unit1 ch.25 analog input pin	70	99	119	
AN126	ADC unit1 ch.26 analog input pin	-	100	122	
AN127	ADC unit1 ch.27 analog input pin	71	101	123	
AN128	ADC unit1 ch.28 analog input pin	72	102	124	
AN129	ADC unit1 ch.29 analog input pin	73	103	125	
AN130	ADC unit1 ch.30 analog input pin	-	104	127	
AN131	ADC unit1 ch.31 analog input pin	-	106	129	
PWU_AN0	Partial wakeup ADC analog 0 input pin	54	78	97	
PWU_AN1	Partial wakeup ADC analog 1 input pin	55	79	98	
PWU_AN2	Partial wakeup ADC analog 2 input pin	56	80	99	
PWU_AN3	Partial wakeup ADC analog 3 input pin	57	81	100	
PWU_AN4	Partial wakeup ADC analog 4 input pin	61	85	104	
PWU_AN5	Partial wakeup ADC analog 5 input pin	62	86	105	
PWU_AN6	Partial wakeup ADC analog 6 input pin	63	87	106	
PWU_AN7	Partial wakeup ADC analog 7 input pin	-	88	107	
PWUTRG_0	Partial wakeup trigger output pin (0)	-	-	130	
PWUTRG_1	Partial wakeup trigger output pin (1)	74	107	131	
RX0_0	CAN ch.0 reception data input pin (0)	69	97	117	
RX0_1	CAN ch.0 reception data input pin (1)	63	87	106	
RX0_2	CAN ch.0 reception data input pin (2)	56	80	99	
TX0_0	CAN ch.0 transmission data output pin (0)	-	96	116	
TX0_1	CAN ch.0 transmission data output pin (1)	62	86	105	
TX0_2	CAN ch.0 transmission data output pin (2)	55	79	98	
RX1_0	CAN ch.1 reception data input pin (0)	94	128	156	
RX1_1	CAN ch.1 reception data input pin (1)	-	105	128	
RX1_2	CAN ch.1 reception data input pin (2)	22	33	41	
TX1_0	CAN ch.1 transmission data output pin (0)	93	127	155	
TX1_1	CAN ch.1 transmission data output pin (1)	-	104	127	
TX1_2	CAN ch.1 transmission data output pin (2)	21	32	40	
RX2_0	CAN ch.2 reception data input pin (0)	53	77	96	
RX2_1	CAN ch.2 reception data input pin (1)	95	131	159	
TX2_0	CAN ch.2 transmission data output pin (0)	52	76	94	
TX2_1	CAN ch.2 transmission data output pin (1)	-	132	160	
RX3_0	CAN ch.3 reception data input pin (0)	10	14	18	
TX3_0	CAN ch.3 transmission data output pin (0)	9	13	17	
RX4_0	CAN ch.4 reception data input pin (0)	43	61	77	

Port Name	Description	Pin No. of Package			Remark
		LQFP 100	LQFP 144	TEQFP 176	
TX4_0	CAN ch.4 transmission data output pin (0)	42	60	76	
RX8_0	CAN ch.8 reception data input pin (0)	73	103	125	
TX8_0	CAN ch.8 transmission data output pin (0)	72	102	124	
SCK0_0	Multi-function serial ch.0 clock I/O pin (0)	12	19	23	
SIN0_0	Multi-function serial ch.0 serial data input pin (0)	13	20	24	
SOT0_0	Multi-function serial ch.0 serial data output pin (0)	11	18	22	
SCS0_0	Multi-function serial ch.0 serial chip select 0 I/O pin (0)	-	21	25	
SCS0_1	Multi-function serial ch.0 serial chip select 0 I/O pin (1)	14	23	29	
SCK1_0	Multi-function serial ch.1 clock I/O pin (0)	18	28	34	
SIN1_0	Multi-function serial ch.1 serial data input pin (0)	15	24	30	
SOT1_0	Multi-function serial ch.1 serial data output pin (0)	16	25	31	
SCS1_0	Multi-function serial ch.1 serial chip select 0 I/O pin (0)	17	27	33	
SCK2_0	Multi-function serial ch.2 clock I/O pin (0)	-	136	165	
SCK2_1	Multi-function serial ch.2 clock I/O pin (1)	99	142	174	
SIN2_0	Multi-function serial ch.2 serial data input pin (0)	-	134	162	
SIN2_1	Multi-function serial ch.2 serial data input pin (1)	-	143	175	
SIN2_2	Multi-function serial ch.2 serial data input pin (2)	98	139	170	
SOT2_0	Multi-function serial ch.2 serial data output pin (0)	96	135	163	
SOT2_1	Multi-function serial ch.2 serial data output pin (1)	-	2	2	
SCS20_0	Multi-function serial ch.2 serial chip select 0 I/O pin (0)	97	137	167	
SCS20_1	Multi-function serial ch.2 serial chip select 0 I/O pin (1)	2	3	3	
SCS21_0	Multi-function serial ch.2 serial chip select 1 output pin (0)	-	138	168	
SCS21_1	Multi-function serial ch.2 serial chip select 1 output pin (1)	-	-	4	
SCS22_0	Multi-function serial ch.2 serial chip select 2 output pin (0)	-	141	172	
SCS22_1	Multi-function serial ch.2 serial chip select 2 output pin (1)	-	4	5	
SCS23_0	Multi-function serial ch.2 serial chip select 3 output pin (0)	-	-	173	
SCS23_1	Multi-function serial ch.2 serial chip select 3 output pin (1)	-	-	6	
SCK3_0	Multi-function serial ch.3 clock I/O pin (0)	5	7	9	
SIN3_0	Multi-function serial ch.3 serial data input pin (0)	3	5	7	
SOT3_0	Multi-function serial ch.3 serial data output pin (0)	4	6	8	
SCS30_0	Multi-function serial ch.3 serial chip select 0 I/O pin (0)	-	8	10	
SCS30_1	Multi-function serial ch.3 serial chip select 0 I/O pin (1)	2	3	3	
SCK4_0	Multi-function serial ch.4 clock I/O pin (0)	44	63	79	
SCK4_1	Multi-function serial ch.4 clock I/O pin (1)	12	19	23	
SIN4_0	Multi-function serial ch.4 serial data input pin (0)	-	66	82	
SIN4_1	Multi-function serial ch.4 serial data input pin (1)	-	21	25	

Port Name	Description	Pin No. of Package			Remark
		LQFP 100	LQFP 144	TEQFP 176	
SIN4_2	Multi-function serial ch.4 serial data input pin (2)	43	61	77	
SOT4_0	Multi-function serial ch.4 serial data output pin (0)	45	65	81	
SOT4_1	Multi-function serial ch.4 serial data output pin (1)	-	22	26	
SCS40_0	Multi-function serial ch.4 serial chip select 0 I/O pin (0)	46	67	83	
SCS40_1	Multi-function serial ch.4 serial chip select 0 I/O pin (1)	-	-	27	
SCS41_0	Multi-function serial ch.4 serial chip select 1 output pin (0)	-	68	84	
SCS41_1	Multi-function serial ch.4 serial chip select 1 output pin (1)	-	-	28	
SCS42_0	Multi-function serial ch.4 serial chip select 2 output pin (0)	-	64	80	
SCS42_1	Multi-function serial ch.4 serial chip select 2 output pin (1)	14	23	29	
SCS43_0	Multi-function serial ch.4 serial chip select 3 output pin (0)	-	62	78	
SCS43_1	Multi-function serial ch.4 serial chip select 3 output pin (1)	-	26	32	
SCK5_0	Multi-function serial ch.5 clock I/O pin (0)	57	81	100	
SCK5_1	Multi-function serial ch.5 clock I/O pin (1)	60	84	103	
SIN5_0	Multi-function serial ch.5 serial data input pin (0)	53	77	96	
SIN5_1	Multi-function serial ch.5 serial data input pin (1)	58	82	101	
SOT5_0	Multi-function serial ch.5 serial data output pin (0)	56	80	99	
SOT5_1	Multi-function serial ch.5 serial data output pin (1)	59	83	102	
SCS50_0	Multi-function serial ch.5 serial chip select 0 I/O pin (0)	55	79	98	
SCS50_1	Multi-function serial ch.5 serial chip select 0 I/O pin (1)	-	68	84	
SCS51_0	Multi-function serial ch.5 serial chip select 1 output pin (0)	54	78	97	
SCS52_0	Multi-function serial ch.5 serial chip select 2 output pin (0)	-	-	95	
SCS53_0	Multi-function serial ch.5 serial chip select 3 output pin (0)	52	76	94	
SCK6_0	Multi-function serial ch.6 clock I/O pin (0)	41	58	74	
SCK6_1	Multi-function serial ch.6 clock I/O pin (1)	82	115	141	
SIN6_0	Multi-function serial ch.6 serial data input pin (0)	39	56	70	
SIN6_1	Multi-function serial ch.6 serial data input pin (1)	-	-	143	
SOT6_0	Multi-function serial ch.6 serial data output pin (0)	40	57	71	
SOT6_1	Multi-function serial ch.6 serial data output pin (1)	-	-	142	
SCS60_0	Multi-function serial ch.6 serial chip select 0 I/O pin (0)	34	48	59	
SCS60_1	Multi-function serial ch.6 serial chip select 0 I/O pin (1)	87	121	149	
SCS60_2	Multi-function serial ch.6 serial chip select 0 I/O pin (2)	-	116	144	
SCS61_0	Multi-function serial ch.6 serial chip select 1 output pin (0)	-	49	60	
SCS61_1	Multi-function serial ch.6 serial chip select 1 output pin (1)	88	122	150	
SCS62_0	Multi-function serial ch.6 serial chip select 2 output pin (0)	35	50	62	
SCS62_1	Multi-function serial ch.6 serial chip select 2 output pin (1)	93	127	155	
SCS63_0	Multi-function serial ch.6 serial chip select 3 output pin (0)	36	51	63	

Port Name	Description	Pin No. of Package			Remark
		LQFP 100	LQFP 144	TEQFP 176	
SCS63_1	Multi-function serial ch.6 serial chip select 3 output pin (1)	94	128	156	
SCK7_0	Multi-function serial ch.7 clock I/O pin (0)	72	102	124	
SCK7_1	Multi-function serial ch.7 clock I/O pin (1)	-	133	161	
SIN7_0	Multi-function serial ch.7 serial data input pin (0)	-	106	129	
SIN7_1	Multi-function serial ch.7 serial data input pin (1)	98	139	170	
SIN7_2	Multi-function serial ch.7 serial data input pin (2)	-	104	127	
SIN7_3	Multi-function serial ch.7 serial data input pin (3)	70	99	119	
SOT7_0	Multi-function serial ch.7 serial data output pin (0)	71	101	123	
SOT7_1	Multi-function serial ch.7 serial data output pin (1)	-	140	171	
SCS70_0	Multi-function serial ch.7 serial chip select 0 I/O pin (0)	73	103	125	
SCS70_1	Multi-function serial ch.7 serial chip select 0 I/O pin (1)	-	-	164	
SCS71_0	Multi-function serial ch.7 serial chip select 1 output pin (0)	-	100	122	
SCS71_1	Multi-function serial ch.7 serial chip select 1 output pin (1)	-	136	165	
SCS72_0	Multi-function serial ch.7 serial chip select 2 output pin (0)	69	97	117	
SCS72_1	Multi-function serial ch.7 serial chip select 2 output pin (1)	-	-	166	
SCS73_0	Multi-function serial ch.7 serial chip select 3 output pin (0)	-	96	116	
SCS73_1	Multi-function serial ch.7 serial chip select 3 output pin (1)	97	137	167	
SCK8_0	Multi-function serial ch.8 clock I/O pin (0)	7	11	14	
SIN8_0	Multi-function serial ch.8 serial data input pin (0)	-	9	11	
SIN8_1	Multi-function serial ch.8 serial data input pin (1)	4	6	8	
SIN8_2	Multi-function serial ch.8 serial data input pin (2)	10	14	18	
SOT8_0	Multi-function serial ch.8 serial data output pin (0)	6	10	12	
SCS80_0	Multi-function serial ch.8 serial chip select 0 I/O pin (0)	8	12	15	
SCS81_0	Multi-function serial ch.8 serial chip select 1 output pin (0)	9	13	17	
SCS82_0	Multi-function serial ch.8 serial chip select 2 output pin (0)	10	14	18	
SCS83_0	Multi-function serial ch.8 serial chip select 3 output pin (0)	-	15	19	
SCS83_1	Multi-function serial ch.8 serial chip select 3 output pin (1)	3	5	7	
SCK9_0	Multi-function serial ch.9 clock I/O pin (0)	-	133	161	
SCK9_1	Multi-function serial ch.9 clock I/O pin (1)	93	127	155	
SIN9_0	Multi-function serial ch.9 serial data input pin (0)	95	131	159	
SOT9_0	Multi-function serial ch.9 serial data output pin (0)	-	132	160	
SOT9_1	Multi-function serial ch.9 serial data output pin (1)	94	128	156	
SCS90_0	Multi-function serial ch.9 serial chip select 0 I/O pin (0)	94	128	156	
SCS90_1	Multi-function serial ch.9 serial chip select 0 I/O pin (1)	-	130	158	
SCK10_0	Multi-function serial ch.10 clock I/O pin (0)	61	85	104	
SIN10_0	Multi-function serial ch.10 serial data input pin (0)	63	87	106	

Port Name	Description	Pin No. of Package			Remark
		LQFP 100	LQFP 144	TEQFP 176	
SOT10_0	Multi-function serial ch.10 serial data output pin (0)	62	86	105	
SCS100_0	Multi-function serial ch.10 serial chip select 0 I/O pin (0)	64	91	110	
SCS100_1	Multi-function serial ch.10 serial chip select 0 I/O pin (1)	67	94	114	
SCS101_0	Multi-function serial ch.10 serial chip select 1 output pin (0)	-	90	109	
SCS101_1	Multi-function serial ch.10 serial chip select 1 output pin (1)	66	93	113	
SCS102_0	Multi-function serial ch.10 serial chip select 2 output pin (0)	-	89	108	
SCS102_1	Multi-function serial ch.10 serial chip select 2 output pin (1)	65	92	111	
SCS103_0	Multi-function serial ch.10 serial chip select 3 output pin (0)	-	88	107	
SCK11_0	Multi-function serial ch.11 clock I/O pin (0)	24	35	43	
SIN11_0	Multi-function serial ch.11 serial data input pin (0)	22	33	41	
SIN11_1	Multi-function serial ch.11 serial data input pin (1)	24	35	43	
SOT11_0	Multi-function serial ch.11 serial data output pin (0)	23	34	42	
SOT11_1	Multi-function serial ch.11 serial data output pin (1)	-	40	50	
SCS110_0	Multi-function serial ch.11 serial chip select 0 I/O pin (0)	-	-	47	
SCS110_1	Multi-function serial ch.11 serial chip select 0 I/O pin (1)	20	31	39	
SCK12_0	Multi-function serial ch.12 clock I/O pin (0)	-	40	50	
SCK12_1	Multi-function serial ch.12 clock I/O pin (1)	5	7	9	
SCK12_2	Multi-function serial ch.12 clock I/O pin (2)	33	46	57	
SIN12_0	Multi-function serial ch.12 serial data input pin (0)	-	-	48	
SIN12_1	Multi-function serial ch.12 serial data input pin (1)	-	-	13	
SIN12_2	Multi-function serial ch.12 serial data input pin (2)	27	38	46	
SOT12_0	Multi-function serial ch.12 serial data output pin (0)	28	39	49	
SOT12_1	Multi-function serial ch.12 serial data output pin (1)	-	-	16	
SCS120_0	Multi-function serial ch.12 serial chip select 0 I/O pin (0)	29	41	51	
SCS120_1	Multi-function serial ch.12 serial chip select 0 I/O pin (1)	-	8	10	
SCK13_0	Multi-function serial ch.13 clock I/O pin (0)	-	-	66	
SIN13_0	Multi-function serial ch.13 serial data input pin (0)	-	-	64	
SOT13_0	Multi-function serial ch.13 serial data output pin (0)	-	-	65	
SCS130_0	Multi-function serial ch.13 serial chip select 0 I/O pin (0)	-	-	61	
SCL0_0	I ² C ch.0 clock I/O pin (0)	12	19	23	
SDA0_0	I ² C ch.0 serial data I/O pin (0)	11	18	22	
SCL1_0	I ² C ch.1 clock I/O pin (0)	18	28	34	
SDA1_0	I ² C ch.1 serial data I/O pin (0)	16	25	31	
SCL2_0	I ² C ch.2 clock I/O pin (0)	-	136	165	
SCL2_1	I ² C ch.2 clock I/O pin (1)	99	142	174	
SDA2_0	I ² C ch.2 serial data I/O pin (0)	96	135	163	

Port Name	Description	Pin No. of Package			Remark
		LQFP 100	LQFP 144	TEQFP 176	
SCL3_0	I ² C ch.3 clock I/O pin (0)	5	7	9	
SDA3_0	I ² C ch.3 serial data I/O pin (0)	4	6	8	
SCL4_0	I ² C ch.4 clock I/O pin (0)	44	63	79	
SDA4_0	I ² C ch.4 serial data I/O pin (0)	45	65	81	
SCL5_0	I ² C ch.5 clock I/O pin (0)	57	81	100	
SDA5_0	I ² C ch.5 serial data I/O pin (0)	56	80	99	
SCL6_0	I ² C ch.6 clock I/O pin (0)	41	58	74	
SDA6_0	I ² C ch.6 serial data I/O pin (0)	40	57	71	
SCL7_0	I ² C ch.7 clock I/O pin (0)	72	102	124	
SDA7_0	I ² C ch.7 serial data I/O pin (0)	71	101	123	
SCL8_0	I ² C ch.8 clock I/O pin (0)	7	11	14	
SDA8_0	I ² C ch.8 serial data I/O pin (0)	6	10	12	
SCL9_0	I ² C ch.9 clock I/O pin (0)	-	133	161	
SCL9_1	I ² C ch.9 clock I/O pin (1)	93	127	155	
SDA9_0	I ² C ch.9 serial data I/O pin (0)	-	132	160	
SDA9_1	I ² C ch.9 serial data I/O pin (1)	94	128	156	
SCL10_0	I ² C ch.10 clock I/O pin (0)	61	85	104	
SDA10_0	I ² C ch.10 serial data I/O pin (0)	62	86	105	
SCL11_0	I ² C ch.11 clock I/O pin (0)	24	35	43	
SDA11_0	I ² C ch.11 serial data I/O pin (0)	23	34	42	
SCL12_0	I ² C ch.12 clock I/O pin (0)	-	40	50	
SCL12_1	I ² C ch.12 clock I/O pin (1)	33	46	57	
SDA12_0	I ² C ch.12 serial data I/O pin (0)	28	39	49	
SCL13_0	I ² C ch.13 clock I/O pin (0)	-	-	66	
SDA13_0	I ² C ch.13 serial data I/O pin (0)	-	-	65	
TEXT0_0	Free-run timer ch.0 clock input pin (0)	-	17	21	
TEXT0_1	Free-run timer ch.0 clock input pin (1)	14	23	29	
TEXT1_0	Free-run timer ch.1 clock input pin (0)	11	18	22	
TEXT1_1	Free-run timer ch.1 clock input pin (1)	-	53	67	
TEXT2_0	Free-run timer ch.2 clock input pin (0)	-	74	92	
TEXT2_1	Free-run timer ch.2 clock input pin (1)	38	54	68	
TEXT3_0	Free-run timer ch.3 clock input pin (0)	-	75	93	
TEXT3_1	Free-run timer ch.3 clock input pin (1)	43	61	77	
TEXT4_0	Free-run timer ch.4 clock input pin (0)	66	93	113	
TEXT4_1	Free-run timer ch.4 clock input pin (1)	-	62	78	
TEXT8_0	Free-run timer ch.8 clock input pin (0)	67	94	114	

Port Name	Description	Pin No. of Package			Remark
		LQFP 100	LQFP 144	TEQFP 176	
TEXT8_1	Free-run timer ch.8 clock input pin (1)	44	63	79	
TEXT9_0	Free-run timer ch.9 clock input pin (0)	41	58	74	
TEXT10_0	Free-run timer ch.10 clock input pin (0)	-	-	73	
IN0_0	Input capture ch.0 input pin (0)	93	127	155	
IN0_1	Input capture ch.0 input pin (1)	-	98	118	
IN0_2	Input capture ch.0 input pin (2)	-	66	82	
IN1_0	Input capture ch.1 input pin (0)	94	128	156	
IN1_1	Input capture ch.1 input pin (1)	70	99	119	
IN1_2	Input capture ch.1 input pin (2)	46	67	83	
IN2_0	Input capture ch.2 input pin (0)	-	129	157	
IN2_1	Input capture ch.2 input pin (1)	-	100	122	
IN2_2	Input capture ch.2 input pin (2)	-	68	84	
IN2_3	Input capture ch.2 input pin (3)	96	135	163	
IN3_0	Input capture ch.3 input pin (0)	-	130	158	
IN3_1	Input capture ch.3 input pin (1)	71	101	123	
IN3_2	Input capture ch.3 input pin (2)	58	82	101	
IN4_0	Input capture ch.4 input pin (0)	95	131	159	
IN4_1	Input capture ch.4 input pin (1)	72	102	124	
IN4_2	Input capture ch.4 input pin (2)	59	83	102	
IN5_0	Input capture ch.5 input pin (0)	98	139	170	
IN5_1	Input capture ch.5 input pin (1)	73	103	125	
IN5_2	Input capture ch.5 input pin (2)	60	84	103	
IN16_0	Input capture ch.16 input pin (0)	3	5	7	
IN16_1	Input capture ch.16 input pin (1)	-	55	69	
IN16_2	Input capture ch.16 input pin (2)	52	76	94	
IN17_0	Input capture ch.17 input pin (0)	4	6	8	
IN17_1	Input capture ch.17 input pin (1)	39	56	70	
IN17_2	Input capture ch.17 input pin (2)	53	77	96	
IN18_0	Input capture ch.18 input pin (0)	5	7	9	
IN18_1	Input capture ch.18 input pin (1)	40	57	71	
IN18_2	Input capture ch.18 input pin (2)	54	78	97	
IN19_0	Input capture ch.19 input pin (0)	-	8	10	
IN19_1	Input capture ch.19 input pin (1)	41	58	74	
IN19_2	Input capture ch.19 input pin (2)	55	79	98	
IN20_0	Input capture ch.20 input pin (0)	-	9	11	
IN20_1	Input capture ch.20 input pin (1)	-	59	75	

Port Name	Description	Pin No. of Package			Remark
		LQFP 100	LQFP 144	TEQFP 176	
IN20_2	Input capture ch.20 input pin (2)	56	80	99	
IN21_0	Input capture ch.21 input pin (0)	6	10	12	
IN21_1	Input capture ch.21 input pin (1)	42	60	76	
IN21_2	Input capture ch.21 input pin (2)	57	81	100	
OUT0_0	Output compare ch.0 output pin (0)	63	87	106	
OUT0_1	Output compare ch.0 output pin (1)	15	24	30	
OUT1_0	Output compare ch.1 output pin (0)	-	88	107	
OUT1_1	Output compare ch.1 output pin (1)	16	25	31	
OUT2_0	Output compare ch.2 output pin (0)	-	89	108	
OUT2_1	Output compare ch.2 output pin (1)	-	26	32	
OUT2_2	Output compare ch.2 output pin (2)	12	19	23	
OUT3_0	Output compare ch.3 output pin (0)	-	90	109	
OUT3_1	Output compare ch.3 output pin (1)	17	27	33	
OUT4_0	Output compare ch.4 output pin (0)	64	91	110	
OUT4_1	Output compare ch.4 output pin (1)	18	28	34	
OUT5_0	Output compare ch.5 output pin (0)	7	11	14	
OUT5_1	Output compare ch.5 output pin (1)	-	29	35	
OUT5_2	Output compare ch.5 output pin (2)	13	20	24	
OUT16_0	Output compare ch.16 output pin (0)	8	12	15	
OUT16_1	Output compare ch.16 output pin (1)	19	30	37	
OUT17_0	Output compare ch.17 output pin (0)	9	13	17	
OUT17_1	Output compare ch.17 output pin (1)	20	31	39	
OUT18_0	Output compare ch.18 output pin (0)	10	14	18	
OUT18_1	Output compare ch.18 output pin (1)	21	32	40	
OUT19_0	Output compare ch.19 output pin (0)	-	15	19	
OUT19_1	Output compare ch.19 output pin (1)	22	33	41	
OUT20_0	Output compare ch.20 output pin (0)	-	16	20	
OUT20_1	Output compare ch.20 output pin (1)	23	34	42	
OUT21_0	Output compare ch.21 output pin (0)	-	17	21	
OUT21_1	Output compare ch.21 output pin (1)	24	35	43	
TIOA0_0	Base timer ch.0 TIOA output pin (0)	-	8	10	
TIOA0_1	Base timer ch.0 TIOA output pin (1)	-	-	4	
TIOA1_0	Base timer ch.1 TIOA I/O pin (0)	-	9	11	
TIOA1_1	Base timer ch.1 TIOA I/O pin (1)	-	-	6	
TIOB0_0	Base timer ch.0 TIOB input pin (0)	-	17	21	
TIOB1_0	Base timer ch.1 TIOB input pin (0)	11	18	22	

Port Name	Description	Pin No. of Package			Remark
		LQFP 100	LQFP 144	TEQFP 176	
TIOA2_0	Base timer ch.2 TIOA output pin (0)	6	10	12	
TIOA2_1	Base timer ch.2 TIOA output pin (1)	-	-	13	
TIOA3_0	Base timer ch.3 TIOA I/O pin (0)	7	11	14	
TIOA3_1	Base timer ch.3 TIOA I/O pin (1)	-	-	16	
TIOB2_0	Base timer ch.2 TIOB input pin (0)	12	19	23	
TIOB3_0	Base timer ch.3 TIOB input pin (0)	13	20	24	
TIOA4_0	Base timer ch.4 TIOA output pin (0)	8	12	15	
TIOA4_1	Base timer ch.4 TIOA output pin (1)	14	23	29	
TIOA5_0	Base timer ch.5 TIOA I/O pin (0)	9	13	17	
TIOA5_1	Base timer ch.5 TIOA I/O pin (1)	-	40	50	
TIOB4_0	Base timer ch.4 TIOB input pin (0)	-	21	25	
TIOB5_0	Base timer ch.5 TIOB input pin (0)	-	22	26	
TIOA6_0	Base timer ch.6 TIOA output pin (0)	10	14	18	
TIOA6_1	Base timer ch.6 TIOA output pin (1)	29	41	51	
TIOA7_0	Base timer ch.7 TIOA I/O pin (0)	-	15	19	
TIOA7_1	Base timer ch.7 TIOA I/O pin (1)	72	102	124	
TIOB6_0	Base timer ch.6 TIOB input pin (0)	14	23	29	
TIOB7_0	Base timer ch.7 TIOB input pin (0)	15	24	30	
TIOA8_0	Base timer ch.8 TIOA output pin (0)	-	16	20	
TIOA8_1	Base timer ch.8 TIOA output pin (1)	73	103	125	
TIOA9_0	Base timer ch.9 TIOA I/O pin (0)	20	31	39	
TIOA9_1	Base timer ch.9 TIOA I/O pin (1)	-	104	127	
TIOB8_0	Base timer ch.8 TIOB input pin (0)	-	26	32	
TIOB9_0	Base timer ch.9 TIOB input pin (0)	19	30	37	
TIOA10_0	Base timer ch.10 TIOA output pin (0)	22	33	41	
TIOA10_1	Base timer ch.10 TIOA output pin (1)	-	105	128	
TIOA11_0	Base timer ch.11 TIOA I/O pin (0)	23	34	42	
TIOA11_1	Base timer ch.11 TIOA I/O pin (1)	35	50	62	
TIOB10_0	Base timer ch.10 TIOB input pin (0)	-	45	55	
TIOB11_0	Base timer ch.11 TIOB input pin (0)	33	46	57	
TIOA12_0	Base timer ch.12 TIOA output pin (0)	24	35	43	
TIOA12_1	Base timer ch.12 TIOA output pin (1)	36	51	63	
TIOA13_0	Base timer ch.13 TIOA I/O pin (0)	28	39	49	
TIOA13_1	Base timer ch.13 TIOA I/O pin (1)	-	68	84	
TIOB12_0	Base timer ch.12 TIOB input pin (0)	-	47	58	
TIOB13_0	Base timer ch.13 TIOB input pin (0)	34	48	59	

Port Name	Description	Pin No. of Package			Remark
		LQFP 100	LQFP 144	TEQFP 176	
TIOA14_0	Base timer ch.14 TIOA output pin (0)	-	-	61	
TIOA14_1	Base timer ch.14 TIOA output pin (1)	58	82	101	
TIOA15_0	Base timer ch.15 TIOA I/O pin (0)	-	-	64	
TIOA15_1	Base timer ch.15 TIOA I/O pin (1)	59	83	102	
TIOB14_0	Base timer ch.14 TIOB input pin (0)	-	74	92	
TIOB15_0	Base timer ch.15 TIOB input pin (0)	-	75	93	
TIOA16_0	Base timer ch.16 TIOA output pin (0)	-	-	65	
TIOA16_1	Base timer ch.16 TIOA output pin (1)	60	84	103	
TIOA17_0	Base timer ch.17 TIOA I/O pin (0)	-	-	72	
TIOA17_1	Base timer ch.17 TIOA I/O pin (1)	57	81	100	
TIOB16_0	Base timer ch.16 TIOB input pin (0)	52	76	94	
TIOB17_0	Base timer ch.17 TIOB input pin (0)	56	80	99	
TIOA18_0	Base timer ch.18 TIOA output pin (0)	-	-	73	
TIOA18_1	Base timer ch.18 TIOA output pin (1)	64	91	110	
TIOA19_0	Base timer ch.19 TIOA I/O pin (0)	-	64	80	
TIOA19_1	Base timer ch.19 TIOA I/O pin (1)	65	92	111	
TIOB18_0	Base timer ch.18 TIOB input pin (0)	69	97	117	
TIOB19_0	Base timer ch.19 TIOB input pin (0)	-	59	75	
TIOA20_0	Base timer ch.20 TIOA output pin (0)	45	65	81	
TIOA20_1	Base timer ch.20 TIOA output pin (1)	66	93	113	
TIOA21_0	Base timer ch.21 TIOA I/O pin (0)	-	66	82	
TIOA21_1	Base timer ch.21 TIOA I/O pin (1)	-	-	126	
TIOB20_0	Base timer ch.20 TIOB input pin (0)	42	60	76	
TIOB21_0	Base timer ch.21 TIOB input pin (0)	43	61	77	
TIOA22_0	Base timer ch.22 TIOA output pin (0)	46	67	83	
TIOA22_1	Base timer ch.22 TIOA output pin (1)	98	139	170	
TIOA23_0	Base timer ch.23 TIOA I/O pin (0)	61	85	104	
TIOA23_1	Base timer ch.23 TIOA I/O pin (1)	-	140	171	
TIOB22_0	Base timer ch.22 TIOB input pin (0)	-	62	78	
TIOB23_0	Base timer ch.23 TIOB input pin (0)	-	141	172	
TIOA24_0	Base timer ch.24 TIOA output pin (0)	62	86	105	
TIOA24_1	Base timer ch.24 TIOA output pin (1)	96	135	163	
TIOA25_0	Base timer ch.25 TIOA I/O pin (0)	63	87	106	
TIOA25_1	Base timer ch.25 TIOA I/O pin (1)	-	-	166	
TIOB24_0	Base timer ch.24 TIOB input pin (0)	-	136	165	
TIOB25_0	Base timer ch.25 TIOB input pin (0)	-	100	122	

Port Name	Description	Pin No. of Package			Remark
		LQFP 100	LQFP 144	TEQFP 176	
TIOA26_0	Base timer ch.26 TIOA output pin (0)	-	88	107	
TIOA26_1	Base timer ch.26 TIOA output pin (1)	-	-	169	
TIOA27_0	Base timer ch.27 TIOA I/O pin (0)	-	89	108	
TIOA27_1	Base timer ch.27 TIOA I/O pin (1)	-	-	173	
TIOB26_0	Base timer ch.26 TIOB input pin (0)	71	101	123	
TIOB27_0	Base timer ch.27 TIOB input pin (0)	72	102	124	
TIOA28_0	Base timer ch.28 TIOA output pin (0)	-	90	109	
TIOA28_1	Base timer ch.28 TIOA output pin (1)	-	98	118	
TIOA29_0	Base timer ch.29 TIOA I/O pin (0)	67	94	114	
TIOA29_1	Base timer ch.29 TIOA I/O pin (1)	70	99	119	
TIOB28_0	Base timer ch.28 TIOB input pin (0)	73	103	125	
TIOB29_0	Base timer ch.29 TIOB input pin (0)	-	104	127	
TIOA30_0	Base timer ch.30 TIOA output pin (0)	16	25	31	
TIOA31_0	Base timer ch.31 TIOA I/O pin (0)	17	27	33	
TIOB30_0	Base timer ch.30 TIOB input pin (0)	18	28	34	
TIOB31_0	Base timer ch.31 TIOB input pin (0)	21	32	40	
TIOA32_0	Base timer ch.32 TIOA output pin (0)	29	41	51	
TIOA33_0	Base timer ch.33 TIOA I/O pin (0)	27	38	46	
TIOB32_0	Base timer ch.32 TIOB input pin (0)	35	50	62	
TIOB33_0	Base timer ch.33 TIOB input pin (0)	-	49	60	
TIOA34_0	Base timer ch.34 TIOA output pin (0)	36	51	63	
TIOA35_0	Base timer ch.35 TIOA I/O pin (0)	37	52	66	
TIOB34_0	Base timer ch.34 TIOB input pin (0)	38	54	68	
TIOB35_0	Base timer ch.35 TIOB input pin (0)	-	53	67	
TIOA36_0	Base timer ch.36 TIOA output pin (0)	41	58	74	
TIOA37_0	Base timer ch.37 TIOA I/O pin (0)	40	57	71	
TIOB36_0	Base timer ch.36 TIOB input pin (0)	39	56	70	
TIOB37_0	Base timer ch.37 TIOB input pin (0)	-	55	69	
TIOA38_0	Base timer ch.38 TIOA output pin (0)	44	63	79	
TIOA39_0	Base timer ch.39 TIOA I/O pin (0)	53	77	96	
TIOB38_0	Base timer ch.38 TIOB input pin (0)	-	68	84	
TIOB39_0	Base timer ch.39 TIOB input pin (0)	54	78	97	
TIOA40_0	Base timer ch.40 TIOA output pin (0)	55	79	98	
TIOA41_0	Base timer ch.41 TIOA I/O pin (0)	58	82	101	
TIOB40_0	Base timer ch.40 TIOB input pin (0)	59	83	102	
TIOB41_0	Base timer ch.41 TIOB input pin (0)	60	84	103	

Port Name	Description	Pin No. of Package			Remark
		LQFP 100	LQFP 144	TEQFP 176	
TIOA42_0	Base timer ch.42 TIOA output pin (0)	64	91	110	
TIOA43_0	Base timer ch.43 TIOA I/O pin (0)	65	92	111	
TIOB42_0	Base timer ch.42 TIOB input pin (0)	66	93	113	
TIOB43_0	Base timer ch.43 TIOB input pin (0)	-	96	116	
TIOA44_0	Base timer ch.44 TIOA output pin (0)	70	99	119	
TIOA45_0	Base timer ch.45 TIOA I/O pin (0)	74	107	131	
TIOB44_0	Base timer ch.44 TIOB input pin (0)	-	98	118	
TIOB45_0	Base timer ch.45 TIOB input pin (0)	82	115	141	
TIOA46_0	Base timer ch.46 TIOA output pin (0)	93	127	155	
TIOA47_0	Base timer ch.47 TIOA I/O pin (0)	94	128	156	
TIOB46_0	Base timer ch.46 TIOB input pin (0)	-	129	157	
TIOB47_0	Base timer ch.47 TIOB input pin (0)	-	130	158	
TIOA48_0	Base timer ch.48 TIOA output pin (0)	95	131	159	
TIOA49_0	Base timer ch.49 TIOA I/O pin (0)	-	132	160	
TIOB48_0	Base timer ch.48 TIOB input pin (0)	-	133	161	
TIOB49_0	Base timer ch.49 TIOB input pin (0)	-	134	162	
TIOA50_0	Base timer ch.50 TIOA output pin (0)	96	135	163	
TIOA51_0	Base timer ch.51 TIOA I/O pin (0)	-	-	164	
TIOB50_0	Base timer ch.50 TIOB input pin (0)	97	137	167	
TIOB51_0	Base timer ch.51 TIOB input pin (0)	-	138	168	
TIOA52_0	Base timer ch.52 TIOA output pin (0)	98	139	170	
TIOA53_0	Base timer ch.53 TIOA I/O pin (0)	-	140	171	
TIOB52_0	Base timer ch.52 TIOB input pin (0)	99	142	174	
TIOB53_0	Base timer ch.53 TIOB input pin (0)	-	143	175	
TIOA54_0	Base timer ch.54 TIOA output pin (0)	2	3	3	
TIOA55_0	Base timer ch.55 TIOA I/O pin (0)	3	5	7	
TIOB54_0	Base timer ch.54 TIOB input pin (0)	4	6	8	
TIOB55_0	Base timer ch.55 TIOB input pin (0)	5	7	9	
TIOA56_0	Base timer ch.56 TIOA output pin (0)	-	29	35	
TIOA57_0	Base timer ch.57 TIOA I/O pin (0)	-	-	36	
TIOB56_0	Base timer ch.56 TIOB input pin (0)	-	-	47	
TIOB57_0	Base timer ch.57 TIOB input pin (0)	-	-	48	
TIOA58_0	Base timer ch.58 TIOA output pin (0)	-	-	90	
TIOA59_0	Base timer ch.59 TIOA I/O pin (0)	-	-	120	
TIOB58_0	Base timer ch.58 TIOB input pin (0)	-	-	91	
TIOB59_0	Base timer ch.59 TIOB input pin (0)	-	-	121	

Port Name	Description	Pin No. of Package			Remark
		LQFP 100	LQFP 144	TEQFP 176	
TIOA60_0	Base timer ch.60 TIOA output pin (0)	-	106	129	
TIOA61_0	Base timer ch.61 TIOA I/O pin (0)	-	-	139	
TIOB60_0	Base timer ch.60 TIOB input pin (0)	-	-	130	
TIOB61_0	Base timer ch.61 TIOB input pin (0)	-	-	140	
TIOA62_0	Base timer ch.62 TIOA output pin (0)	-	116	144	
TIOA63_0	Base timer ch.63 TIOA I/O pin (0)	-	2	2	
TIOB62_0	Base timer ch.62 TIOB input pin (0)	-	-	143	
TIOB63_0	Base timer ch.63 TIOB input pin (0)	-	4	5	
AIN8_0	Quad Position and Revolution Counter ch.8 AIN input pin (0)	-	2	2	
AIN8_1	Quad Position and Revolution Counter ch.8 AIN input pin (1)	-	59	75	
AIN8_2	Quad Position and Revolution Counter ch.8 AIN input pin (2)	6	10	12	
BIN8_0	Quad Position and Revolution Counter ch.8 BIN input pin (0)	2	3	3	
BIN8_1	Quad Position and Revolution Counter ch.8 BIN input pin (1)	42	60	76	
BIN8_2	Quad Position and Revolution Counter ch.8 BIN input pin (2)	7	11	14	
ZIN8_0	Quad Position and Revolution Counter ch.8 ZIN input pin (0)	-	4	5	
ZIN8_1	Quad Position and Revolution Counter ch.8 ZIN input pin (1)	43	61	77	
ZIN8_2	Quad Position and Revolution Counter ch.8 ZIN input pin (2)	8	12	15	
AIN9_0	Quad Position and Revolution Counter ch.9 AIN input pin (0)	3	5	7	
AIN9_1	Quad Position and Revolution Counter ch.9 AIN input pin (1)	54	78	97	
BIN9_0	Quad Position and Revolution Counter ch.9 BIN input pin (0)	4	6	8	
BIN9_1	Quad Position and Revolution Counter ch.9 BIN input pin (1)	55	79	98	
ZIN9_0	Quad Position and Revolution Counter ch.9 ZIN input pin (0)	5	7	9	
ZIN9_1	Quad Position and Revolution Counter ch.9 ZIN input pin (1)	56	80	99	
TIN0_0	Reload timer ch.0 event input pin (0)	21	32	40	
TIN0_1	Reload timer ch.0 event input pin (1)	52	76	94	
TOT0_0	Reload timer ch.0 output pin (0)	22	33	41	
TOT0_1	Reload timer ch.0 output pin (1)	54	78	97	
TIN1_0	Reload timer ch.1 event input pin (0)	23	34	42	
TIN1_1	Reload timer ch.1 event input pin (1)	57	81	100	
TOT1_0	Reload timer ch.1 output pin (0)	24	35	43	
TOT1_1	Reload timer ch.1 output pin (1)	61	85	104	
TIN2_0	Reload timer ch.2 event input pin (0)	28	39	49	
TIN2_1	Reload timer ch.2 event input pin (1)	62	86	105	
TOT2_0	Reload timer ch.2 output pin (0)	-	40	50	
TOT2_1	Reload timer ch.2 output pin (1)	63	87	106	
TIN3_0	Reload timer ch.3 event input pin (0)	29	41	51	

Port Name	Description	Pin No. of Package			Remark
		LQFP 100	LQFP 144	TEQFP 176	
TIN3_1	Reload timer ch.3 event input pin (1)	64	91	110	
TOT3_0	Reload timer ch.3 output pin (0)	-	45	55	
TOT3_1	Reload timer ch.3 output pin (1)	65	92	111	
TIN16_0	Reload timer ch.16 event input pin (0)	33	46	57	
TIN16_1	Reload timer ch.16 event input pin (1)	66	93	113	
TOT16_0	Reload timer ch.16 output pin (0)	-	47	58	
TOT16_1	Reload timer ch.16 output pin (1)	67	94	114	
TIN17_0	Reload timer ch.17 event input pin (0)	34	48	59	
TIN17_1	Reload timer ch.17 event input pin (1)	69	97	117	
TOT17_0	Reload timer ch.17 output pin (0)	-	49	60	
TOT17_1	Reload timer ch.17 output pin (1)	70	99	119	
WOT	RTC overflow output pin	82	115	141	
CLK_CLKO	Clock monitor output pin	27	38	46	
TRACECLK_0	Trace clock output pin (0)	99	142	174	
TRACECLK_1	Trace clock output pin (1)	74	107	131	
TRACECTL_0	Trace control output pin (0)	-	143	175	
TRACECTL_1	Trace control output pin (1)	73	103	125	
TRACEDATA0_0	Trace data 0 output pin (0)	-	129	157	
TRACEDATA0_1	Trace data 0 output pin (1)	72	102	124	
TRACEDATA1_0	Trace data 1 output pin (0)	-	130	158	
TRACEDATA1_1	Trace data 1 output pin (1)	71	101	123	
TRACEDATA2_0	Trace data 2 output pin (0)	95	131	159	
TRACEDATA2_1	Trace data 2 output pin (1)	70	99	119	
TRACEDATA3_0	Trace data 3 output pin (0)	-	132	160	
TRACEDATA3_1	Trace data 3 output pin (1)	69	97	117	
TRACEDATA4_0	Trace data 4 output pin (0)	-	133	161	
TRACEDATA4_1	Trace data 4 output pin (1)	67	94	114	
TRACEDATA5_0	Trace data 5 output pin (0)	-	134	162	
TRACEDATA5_1	Trace data 5 output pin (1)	66	93	113	
TRACEDATA6_0	Trace data 6 output pin (0)	96	135	163	
TRACEDATA6_1	Trace data 6 output pin (1)	65	92	111	
TRACEDATA7_0	Trace data 7 output pin (0)	-	136	165	
TRACEDATA7_1	Trace data 7 output pin (1)	64	91	110	
TRST	JTAG test reset input pin	81	114	138	
TCK	JTAG test clock input pin	78	111	135	
TDI	JTAG test data input pin	80	113	137	

Port Name	Description	Pin No. of Package			Remark
		LQFP 100	LQFP 144	TEQFP 176	
TDO	JTAG test data output pin	77	110	134	
TMS	JTAG test mode state input pin	79	112	136	
P000	General-purpose I/O port	-	2	2	
P001	General-purpose I/O port	2	3	3	
P002	General-purpose I/O port	-	-	4	
P003	General-purpose I/O port	-	4	5	
P004	General-purpose I/O port	-	-	6	
P005	General-purpose I/O port	3	5	7	
P006	General-purpose I/O port	4	6	8	
P007	General-purpose I/O port	5	7	9	
P008	General-purpose I/O port	-	8	10	
P009	General-purpose I/O port	-	9	11	
P010	General-purpose I/O port	6	10	12	
P011	General-purpose I/O port	-	-	13	
P012	General-purpose I/O port	7	11	14	
P013	General-purpose I/O port	8	12	15	
P014	General-purpose I/O port	-	-	16	
P015	General-purpose I/O port	9	13	17	
P016	General-purpose I/O port	10	14	18	
P017	General-purpose I/O port	-	15	19	
P018	General-purpose I/O port	-	16	20	
P019	General-purpose I/O port	-	17	21	
P020	General-purpose I/O port	11	18	22	
P021	General-purpose I/O port	12	19	23	
P022	General-purpose I/O port	13	20	24	
P023	General-purpose I/O port	-	21	25	
P024	General-purpose I/O port	-	22	26	
P025	General-purpose I/O port	-	-	27	
P026	General-purpose I/O port	-	-	28	
P027	General-purpose I/O port	14	23	29	
P028	General-purpose I/O port	15	24	30	
P029	General-purpose I/O port	16	25	31	
P030	General-purpose I/O port	-	26	32	
P031	General-purpose I/O port	17	27	33	
P100	General-purpose I/O port	18	28	34	
P101	General-purpose I/O port	-	29	35	

Port Name	Description	Pin No. of Package			Remark
		LQFP 100	LQFP 144	TEQFP 176	
P102	General-purpose I/O port	-	-	36	
P103	General-purpose I/O port	19	30	37	
P104	General-purpose I/O port	-	-	38	
P105	General-purpose I/O port	20	31	39	
P106	General-purpose I/O port	21	32	40	
P107	General-purpose I/O port	22	33	41	
P108	General-purpose I/O port	23	34	42	
P109	General-purpose I/O port	24	35	43	
P110	General-purpose I/O port	-	-	47	
P111	General-purpose I/O port	-	-	48	
P112	General-purpose I/O port	28	39	49	
P113	General-purpose I/O port	-	40	50	
P114	General-purpose I/O port	29	41	51	
P115	General-purpose I/O port	-	45	55	
P116	General-purpose I/O port	-	-	56	
P117	General-purpose I/O port	33	46	57	
P118	General-purpose I/O port	-	47	58	
P119	General-purpose I/O port	34	48	59	
P120	General-purpose I/O port	-	49	60	
P121	General-purpose I/O port	-	-	61	
P122	General-purpose I/O port	35	50	62	
P123	General-purpose I/O port	36	51	63	
P124	General-purpose I/O port	-	-	64	
P125	General-purpose I/O port	-	-	65	
P126	General-purpose I/O port	37	52	66	
P127	General-purpose I/O port	-	53	67	
P128	General-purpose I/O port	38	54	68	
P129	General-purpose I/O port	-	55	69	
P130	General-purpose I/O port	39	56	70	
P131	General-purpose I/O port	40	57	71	
P200	General-purpose I/O port	-	-	72	
P201	General-purpose I/O port	-	-	73	
P202	General-purpose I/O port	41	58	74	
P203	General-purpose I/O port	-	59	75	
P204	General-purpose I/O port	42	60	76	
P205	General-purpose I/O port	43	61	77	

Port Name	Description	Pin No. of Package			Remark
		LQFP 100	LQFP 144	TEQFP 176	
P206	General-purpose I/O port	-	62	78	
P207	General-purpose I/O port	44	63	79	
P208	General-purpose I/O port	-	64	80	
P209	General-purpose I/O port	45	65	81	
P210	General-purpose I/O port	-	66	82	
P211	General-purpose I/O port	46	67	83	
P212	General-purpose I/O port	-	68	84	
P213	General-purpose I/O port	58	82	101	
P214	General-purpose I/O port	59	83	102	
P215	General-purpose I/O port	60	84	103	
P216	General-purpose I/O port	-	-	90	
P217	General-purpose I/O port	-	-	91	
P218	General-purpose I/O port	-	74	92	
P219	General-purpose I/O port	-	75	93	
P220	General-purpose I/O port	52	76	94	
P221	General-purpose I/O port	-	-	95	
P222	General-purpose I/O port	53	77	96	
P223	General-purpose I/O port	54	78	97	
P224	General-purpose I/O port	55	79	98	
P225	General-purpose I/O port	56	80	99	
P226	General-purpose I/O port	57	81	100	
P227	General-purpose I/O port	61	85	104	
P228	General-purpose I/O port	62	86	105	
P229	General-purpose I/O port	63	87	106	
P230	General-purpose I/O port	-	88	107	
P231	General-purpose I/O port	-	89	108	
P300	General-purpose I/O port	-	90	109	
P301	General-purpose I/O port	64	91	110	
P302	General-purpose I/O port	65	92	111	
P303	General-purpose I/O port	-	-	112	
P304	General-purpose I/O port	66	93	113	
P305	General-purpose I/O port	67	94	114	
P306	General-purpose I/O port	-	96	116	
P307	General-purpose I/O port	69	97	117	
P308	General-purpose I/O port	-	98	118	
P309	General-purpose I/O port	70	99	119	

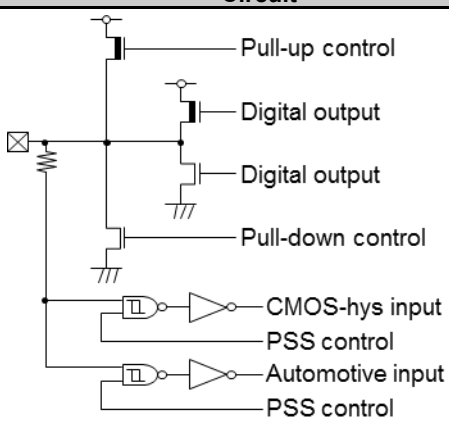
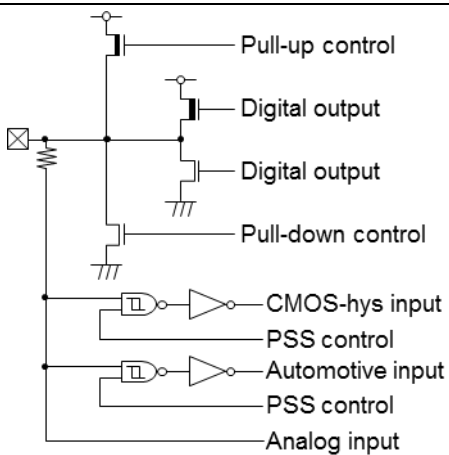
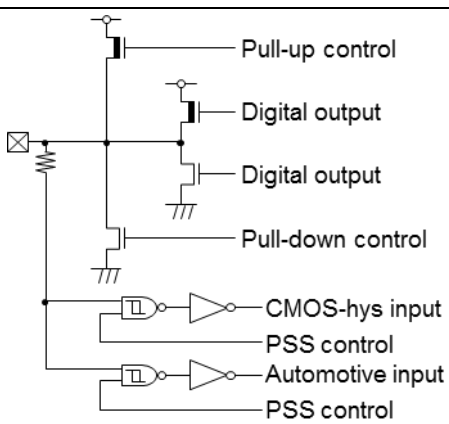
Port Name	Description	Pin No. of Package			Remark
		LQFP 100	LQFP 144	TEQFP 176	
P310	General-purpose I/O port	-	-	120	
P311	General-purpose I/O port	-	-	121	
P312	General-purpose I/O port	-	100	122	
P313	General-purpose I/O port	71	101	123	
P314	General-purpose I/O port	72	102	124	
P315	General-purpose I/O port	73	103	125	
P316	General-purpose I/O port	-	-	126	
P317	General-purpose I/O port	-	104	127	
P318	General-purpose I/O port	-	105	128	
P319	General-purpose I/O port	-	106	129	
P320	General-purpose I/O port	-	-	130	
P321	General-purpose I/O port	74	107	131	
P322	General-purpose output port	77	110	134	
P323	General-purpose output port	80	113	137	
P324	General-purpose output port	81	114	138	
P325	General-purpose I/O port	-	-	139	
P326	General-purpose I/O port	-	-	140	
P327	General-purpose I/O port	82	115	141	
P328	General-purpose I/O port	-	-	142	
P329	General-purpose I/O port	-	-	143	
P330	General-purpose I/O port	-	116	144	
P331	General-purpose I/O port	87	121	149	
P400	General-purpose I/O port	88	122	150	
P401	General-purpose I/O port	93	127	155	
P402	General-purpose I/O port	94	128	156	
P403	General-purpose I/O port	-	129	157	
P404	General-purpose I/O port	-	130	158	
P405	General-purpose I/O port	95	131	159	
P406	General-purpose I/O port	-	132	160	
P407	General-purpose I/O port	-	133	161	
P408	General-purpose I/O port	-	134	162	
P409	General-purpose I/O port	96	135	163	
P410	General-purpose I/O port	-	-	164	
P411	General-purpose I/O port	-	136	165	
P412	General-purpose I/O port	-	-	166	
P413	General-purpose I/O port	97	137	167	

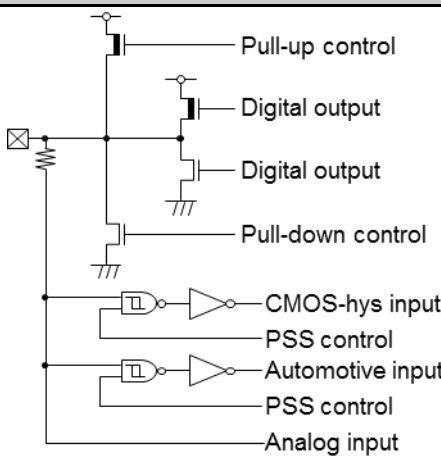
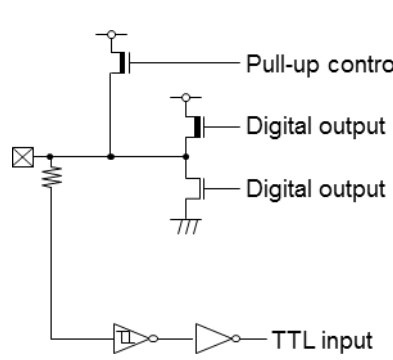
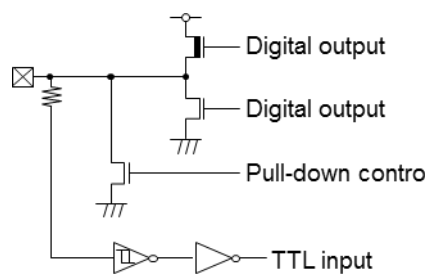
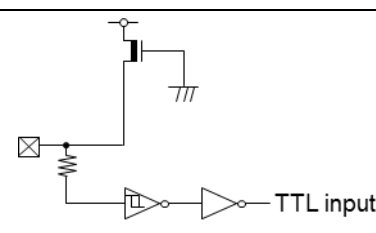
Port Name	Description	Pin No. of Package			Remark
		LQFP 100	LQFP 144	TEQFP 176	
P414	General-purpose I/O port	-	138	168	
P415	General-purpose I/O port	-	-	169	
P416	General-purpose I/O port	98	139	170	
P417	General-purpose I/O port	-	140	171	
P418	General-purpose I/O port	-	141	172	
P419	General-purpose I/O port	-	-	173	
P420	General-purpose I/O port	99	142	174	
P421	General-purpose I/O port	-	143	175	
P422	General-purpose I/O port	27	38	46	
AVCC0	Analog power supply pin for A/D converter unit 0	32	44	54	
AVCC1	Analog power supply pin for A/D converter unit 1	49	71	87	
AVSS0	GND pin for A/D converter unit 0	31	43	53	
AVSS1	GND pin for A/D converter unit 1	48	70	86	
AVRH0	Upper-limit reference voltage pin for A/D converter unit 0	30	42	52	
AVRH1	Upper-limit reference voltage pin for A/D converter unit 1	47	69	85	
AVRL0	Lower-limit reference voltage pin for A/D converter unit 0	31	43	53	
AVRL1	Lower-limit reference voltage pin for A/D converter unit 1	48	70	86	
C	External capacity connection output pin	92	126	154	
VCC	Power supply pin	25	36	44	
		50	72	88	
		76	109	133	
		90	124	152	
		100	144	176	
VSS	GND pin	1	1	1	
		26	37	45	
		51	73	89	
		75	108	132	
		86	120	148	
		91	125	153	

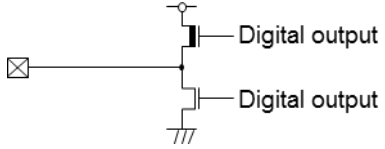
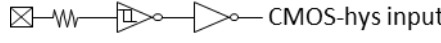
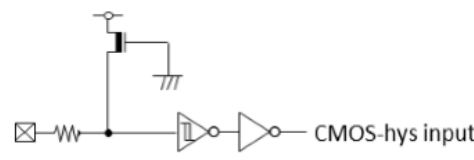
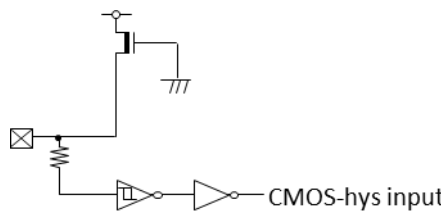
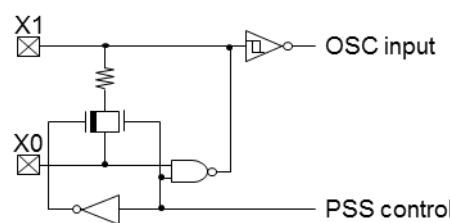
5.2 I/O Circuit Type

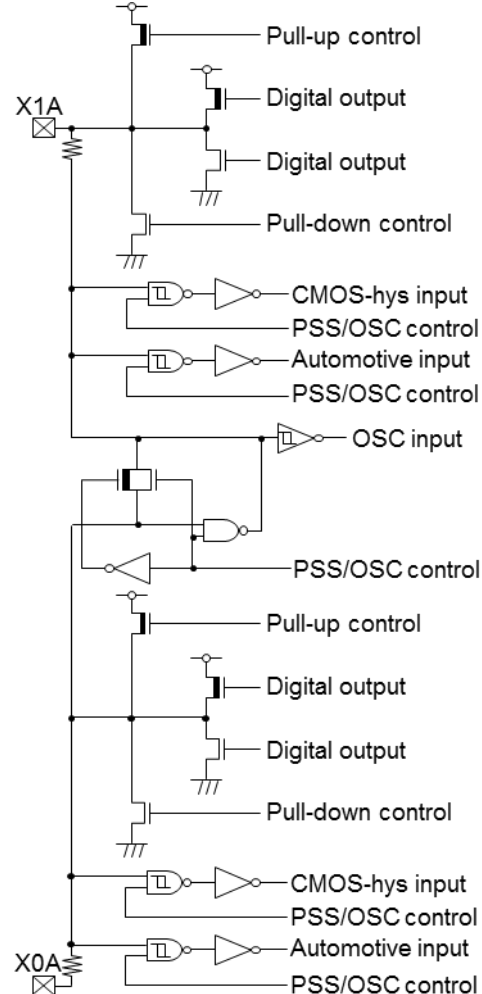
This section explains I/O circuit types.

Table 5-2 I/O Circuit Type

Type	Circuit	Remark
A	 Pull-up control Digital output Digital output Pull-down control CMOS-hys input PSS control Automotive input PSS control	- General-purpose I/O port - Output 1 mA, 2 mA, or 5 mA selectable - 50 kΩ with pull-up resistor control - 50 kΩ with pull-down resistor control - CMOS hysteresis or Automotive hysteresis input selectable
B	 Pull-up control Digital output Digital output Pull-down control CMOS-hys input PSS control Automotive input PSS control Analog input	- General-purpose I/O port with analog input - Output 1 mA, 2 mA, or 5 mA selectable - 50 kΩ with pull-up resistor control - 50 kΩ with pull-down resistor control - CMOS hysteresis or Automotive hysteresis input selectable
C	 Pull-up control Digital output Digital output Pull-down control CMOS-hys input PSS control Automotive input PSS control	- General-purpose I/O port - Output 1 mA, 2 mA, 3 mA(I²C), or 5 mA selectable - 50 kΩ with pull-up resistor control - 50 kΩ with pull-down resistor control - CMOS hysteresis or Automotive hysteresis input selectable

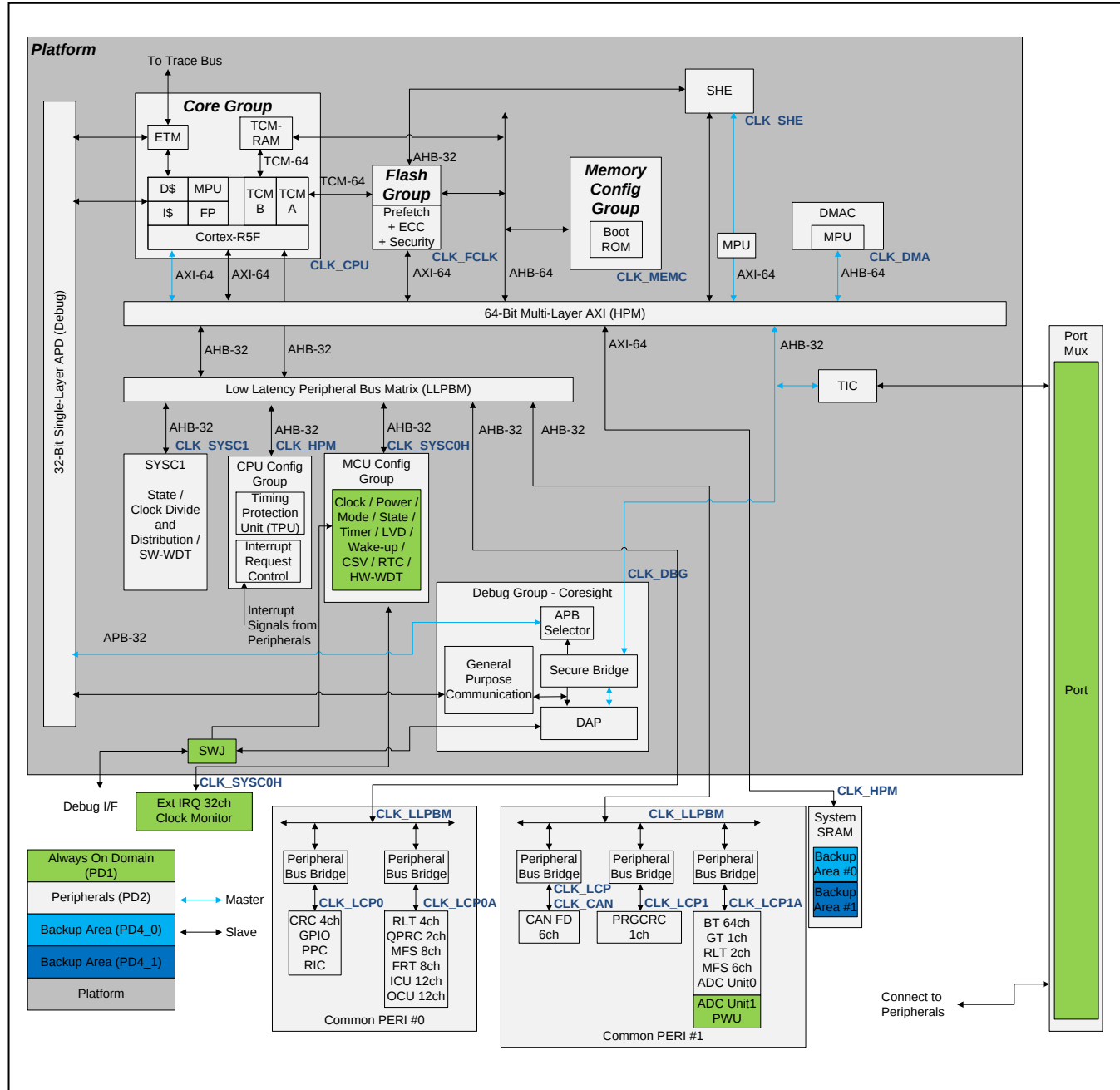
Type	Circuit	Remark
D		- General-purpose I/O port with analog input - Output 1 mA, 2 mA, 3 mA(I²C), or 5 mA selectable - 50 kΩ with pull-up resistor control - 50 kΩ with pull-down resistor control - CMOS hysteresis or Automotive hysteresis input selectable
E		- JTAG_TDI/JTAG_TMS - General-purpose output port - Output 1 mA, 2 mA, or 5 mA selectable (in the case of GPIO) - Output 5 mA (In the case of Serial Wire Debugger) - 50 kΩ with pull-up resistor control - TTL hysteresis input
F		- JTAG_TRST - General-purpose output port - Output 1 mA, 2 mA, or 5 mA selectable (In the case of GPIO) - 50 kΩ with pull-down resistor control - TTL hysteresis input
G		- JTAG_TCK - 50 kΩ with pull-up resistor - TTL hysteresis input

Type	Circuit	Remark
H		- JTAG_TDO - General-purpose output port - Output 5 mA (In the case of JTAG) - Output 1 mA, 2 mA, or 5 mA selectable (in the case of GPIO)
I		- Mode input - CMOS hysteresis input
J		- Reset input - 50 kΩ with pull-up resistor - CMOS hysteresis input
K		- NMIX input - 50 kΩ with pull-up resistor - CMOS hysteresis input
L		- Main oscillation I/O - Feedback resistor = approx.2.1 MΩ

Type	Circuit	Remark
M	 The circuit diagram for Type M shows two identical I/O blocks. Each block consists of a pull-up control, a digital output, a pull-down control, a CMOS-hys input, a PSS/OSC control, an Automotive input, and an OSC input. The top block is connected to X1A and the bottom block to X0A. The circuit includes various transistors, resistors, and logic gates to implement these functions.	- Sub oscillation I/O shared General-purpose I/O port - Feedback resistor = approx. 13 MΩ - Output 1 mA, 2 mA, or 5 mA selectable - 50 kΩ with pull-up resistor control - 50 kΩ with pull-down resistor control - CMOS hysteresis or Automotive hysteresis input selectable

6. Block Diagram

Figure 6-1 Block Diagram



7. Electrical Characteristics

7.1 Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage ^{*1, *2}	V _{CC}	V _{SS} -0.3	V _{SS} +6.0	V	
Analog supply voltage ^{*1, *2}	AV _{CC}	V _{SS} -0.3	V _{SS} +6.0	V	AV _{CC} ≤ V _{CC}
Analog reference voltage ^{*1}	AV _{RH}	V _{SS} -0.3	V _{SS} +6.0	V	AV _{RH} ≤ AV _{CC}
Input voltage ^{*1}	V _{I1}	V _{SS} -0.3	V _{CC} +0.3	V	
Analog pin input voltage ^{*1}	V _{IA}	V _{SS} -0.3	V _{CC} +0.3	V	
Output voltage ^{*1}	V _{O1}	V _{SS} -0.3	V _{CC} +0.3	V	
Maximum clamp current ^{*9}	I _{CLAMP}	-	4	mA	*10
Total maximum clamp current ^{*9}	Σ I _{CLAMP}	-	20	mA	*10
"L"-level maximum output current ^{*3}	I _{OL1}	-	3.5	mA	When setting is 1 mA
	I _{OL2}	-	7	mA	When setting is 2 mA
	I _{OL3}	-	10	mA	When setting is 5 mA
	I _{OL4}	-	8	mA	When setting is 3 mA ^{*8}
"L"-level average output current ^{*4}	I _{OLAV1}	-	1	mA	When setting is 1 mA
	I _{OLAV2}	-	2	mA	When setting is 2 mA
	I _{OLAV3}	-	5	mA	When setting is 5 mA
	I _{OLAV4}	-	3	mA	When setting is 3 mA ^{*8}
"L"-level total output current ^{*5}	ΣI _{OL1}	-	50	mA	
"H"-level maximum output current ^{*3}	I _{OH1}	-	-3.5	mA	When setting is 1 mA
	I _{OH2}	-	-7	mA	When setting is 2 mA
	I _{OH3}	-	-10	mA	When setting is 5 mA
"H"-level average output current ^{*4}	I _{OHAV1}	-	-1	mA	When setting is 1 mA
	I _{OHAV2}	-	-2	mA	When setting is 2 mA
	I _{OHAV3}	-	-5	mA	When setting is 5 mA
"H"-level total output current ^{*5}	ΣI _{OH1}	-	-50	mA	
Power consumption	P _D	-	1530	mW	
Operating temperature	T _A	-40	+105	°C	P _D ≤ 1530 mW ^{*6}
		-40	+105	°C	P _D ≤ 930 mW ^{*7}
		-40	+125	°C	P _D ≤ 965 mW ^{*6}
Storage temperature	T _{stg}	-55	+150	°C	

*1: These parameters are based on the condition that V_{SS}=AV_{SS}=0.0 V.

*2: Take care that AV_{CC} does not exceed V_{CC} at, for example, the power-on time.

*3: The maximum output current is defined as the value of the peak current flowing through any one of the corresponding pins.

*4: The average output current is defined as the value of the average current flowing through any one of the corresponding pins for a 10-ms period. The average value is the operation current × the operation ratio.

*5: The total output current is defined as the maximum current value flowing through all of corresponding pins.

*6: It is a condition that can be used by limiting the product type of TEQFP.

*7: It is a condition that can be used by limiting the product type of LQFP.

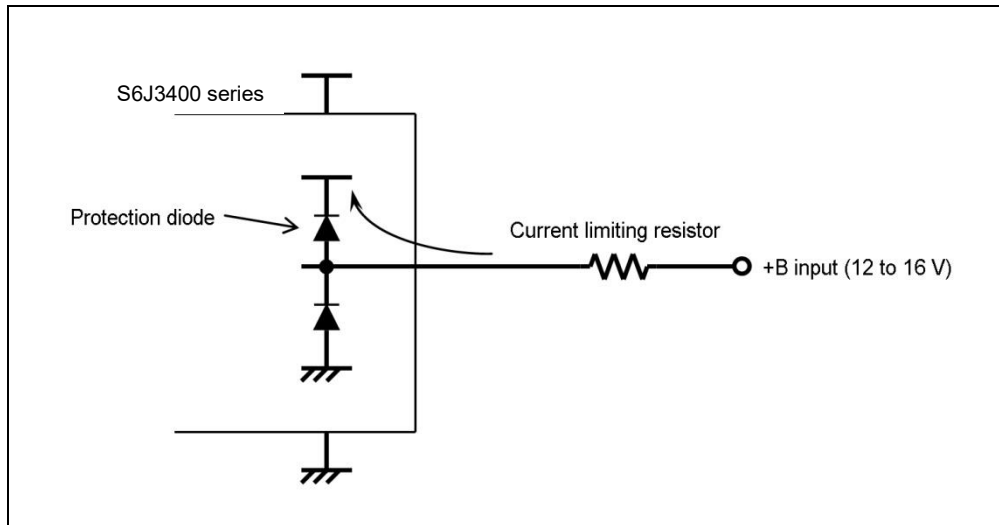
*8: Output of I²C

*9: Relevant pins: All general-purpose ports and analog input pins

- Corresponding pins : all general-purpose ports
- Use within recommended operating conditions.
- Use at DC voltage (current).
- The +B signal should always be applied by connecting a limiting resistor between the +B signal and the microcontroller.
- The value of the limiting resistor should be set so that the current input to the microcontroller pin does not exceed rated values at any time regardless of instantaneous or constant +B signal input.
- When the microcontroller drive current is low, such as in the low power consumption modes, the + B input potential can increase the potential at the VCC pin via a protective diode, possibly affecting other devices.
- If the + B signal is input when the microcontroller is off (not fixed at 0 V), since the power is supplied through the pin, the microcontroller may not operate completely.
- If the +B signal is input at power-on, since the power is supplied through the pin, the power-on reset may not function in the power supply voltage.
- Do not leave + B input pins open.

*10: VI or VO should never exceed the specified ratings. However, if the maximum current to/from an input is limited by a suitable external resistor, the ICLAMP rating supersedes the VI rating.

Example of a recommended circuit



WARNING:

- Semiconductor devices may be permanently damaged by application of stress (including, without limitation, voltage, current or temperature) in excess of absolute maximum ratings. Do not exceed any of these ratings.

7.2 Recommended Operating Conditions

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Supply voltage	V_{CC}/AV_{CC}	4.5	5.5	V	Recommended operation assurance range (when 5.0 V is used)
		3.0	3.6	V	Recommended operation assurance Range (when 3.3 V is used)
		2.7	5.5	V	Operation assurance range* ¹
Smoothing capacitor* ²	C_S	4.7		μF	Tolerance of up to ±40%
Operating temperature	T_A	-40	+105	°C	$P_D \leq 1530 \text{ mW}^{*3}$
		-40	+105	°C	$P_D \leq 930 \text{ mW}^{*4}$
		-40	+125	°C	$P_D \leq 965 \text{ mW}^{*3}$

*1: When it is used outside recommended range (this is the range of guaranteed operation), contact your sales representative.

The initial detection voltage of the external low voltage detection is 2.6 V±3.5%.

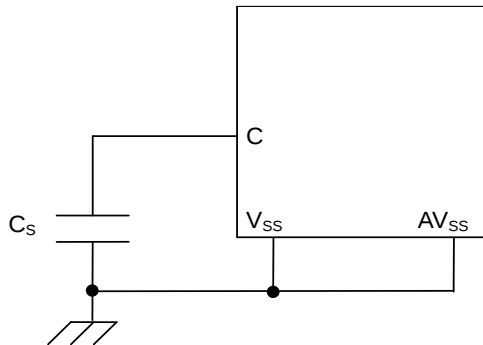
This LVD setting and internal LVD (LVDL0/LVDL1) cannot be used to reliably generate a reset before voltage dips below minimum guaranteed MCU operation voltage, as these detection levels are below the minimum guaranteed MCU operation voltage.

*2: For the connections of smoothing capacitor C_S , see the following diagram.

*3: It is a condition that can be used by limiting the package type to TEQFP.

*4: It is a condition that can be used by limiting the product type of LQFP.

C Pin Connection Diagram



WARNING:

- The recommended operating conditions are required to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are guaranteed when the device is operated under these conditions.
- Any use of semiconductor devices will be under their recommended operating condition.
- Operation under any conditions other than these conditions may adversely affect reliability of device and can result in device failure.
- No guarantee is made with respect to any use, operating conditions, or combinations not represented on this datasheet. If you want to operate the application under any condition other than listed herein, contact the sales representatives.

Note:

The power-on sequence is as follows. Simultaneously turn on the digital supply voltage (V_{CC}) and analog supply voltages (AV_{CC0} , AV_{CC1} , AV_{RH0} , AV_{RH1}), or turn on the digital supply voltage (V_{CC}) and then the analog supply voltages (AV_{CC0} , AV_{CC1} , AV_{RH0} , AV_{RH1}). Be careful that analog power supplies (AV_{CC0} , AV_{CC1} , AV_{RH0} , and AV_{RH1}) and analog inputs do not exceed the digital power supply (V_{CC}) at the analog system power-on and power-off times.

7.3 DC Characteristics

(Condition: See Recommended Operating Conditions)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"H" level Input voltage	V _{IH4}	P000 to P029, P030, P031, P100 to P129, P130, P131, P200 to P229, P230, P231, P300 to P319, P320, P321, P325 to P329, P330, P331, P400 to P419, P420 to P422	CMOS hysteresis input level is selected	0.7×V _{CC}	-	V _{CC} +0.3	V	
	V _{IH5}	P000 to P029, P030, P031, P100 to P129, P130, P131, P200 to P229, P230, P231, P300 to P319, P320, P321, P325 to P329, P330, P331, P400 to P419, P420 to P422	Automotive input level is selected	0.8×V _{CC}	-	V _{CC} +0.3	V	
"H" level Input voltage	V _{IH9}	RSTX, NMIX	CMOS hysteresis input level	0.7×V _{CC}	-	V _{CC} +0.3	V	
	V _{IH10}	MD	CMOS hysteresis input level	0.7×V _{CC}	-	V _{CC} +0.3	V	
	V _{IH11}	TRST, TCK, TDI, TMS	TTL input level	2.7	-	V _{CC} +0.3	V	
"L" level Input Voltage	V _{IL4}	P000 to P029, P030, P031, P100 to P129, P130, P131, P200 to P229, P230, P231, P300 to P319, P320, P321, P325 to P329, P330, P331, P400 to P419, P420 to P422	CMOS hysteresis input level is selected	V _{SS} -0.3	-	0.3×V _{CC}	V	
	V _{IL5}	P000 to P029, P030, P031, P100 to P129, P130, P131, P200 to P229, P230, P231, P300 to P319, P320, P321, P325 to P329, P330, P331, P400 to P419, P420 to P422	Automotive input level is selected	V _{SS} -0.3	-	0.5×V _{CC}	V	
"L" level Input Voltage	V _{IL9}	RSTX, NMIX	CMOS hysteresis input level	V _{SS} -0.3	-	0.3×V _{CC}	V	
	V _{IL10}	MD	CMOS hysteresis input level	V _{SS} -0.3	-	0.3×V _{CC}	V	
	V _{IL11}	TRST, TCK, TDI, TMS	TTL input level	V _{SS} -0.3	-	0.8	V	
Hysteresis voltage	V _{HYS4}	P000 to P031, P100 to P131, P200 to P231, P300 to P321, P325 to P331, P400 to P422	CMOS hysteresis input level is selected	-	0.05×V _{CC}	-	V	
	V _{HYS5}	P000 to P031, P100 to P131, P200 to P231, P300 to P321, P325 to P331, P400 to P422	Automotive input level is selected	-	0.03×V _{CC}	-	V	
	V _{HYS9}	RSTX, NMIX	-	-	0.05×V _{CC}	-	V	
	V _{HYS10}	MD	-	-	0.05×V _{CC}	-	V	
	V _{HYS11}	TRST, TCK, TDI, TMS	-	-	0.035	-	V	

(Condition: See Recommended Operating Conditions)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"H" level output voltage	V _{OH4}	P000 to P031, P100 to P131, P200 to P231, P300 to P331, P400 to P422	V _{CC} =4.5 V I _{OH} =-1.0 mA	V _{CC} - 0.5	-	V _{CC}	V	ODR[1:0]=2b00
			V _{CC} =3.0 V I _{OH} =-0.5 mA	V _{CC} - 0.5	-	V _{CC}	V	
	V _{OH5}		V _{CC} =4.5 V I _{OH} =-2.0 mA	V _{CC} - 0.5	-	V _{CC}	V	ODR[1:0]=2b01
			V _{CC} =3.0 V I _{OH} =-1.0 mA	V _{CC} - 0.5	-	V _{CC}	V	
	V _{OH6}		V _{CC} =4.5 V I _{OH} =-5.0 mA	V _{CC} - 0.5	-	V _{CC}	V	ODR[1:0]=2b11
			V _{CC} =3.0 V I _{OH} =-2.0 mA	V _{CC} - 0.5	-	V _{CC}	V	
	V _{OH8}	TDO	V _{CC} =4.5 V I _{OH} =-5.0 mA	V _{CC} - 0.5	-	V _{CC}	V	
			V _{CC} =3.0 V I _{OH} =-2.0 mA	V _{CC} - 0.5	-	V _{CC}	V	
"L" level output voltage	V _{OL4}	P000 to P031, P100 to P131, P200 to P231, P300 to P331, P400 to P422	V _{CC} =4.5 V I _{OL} =1.0 mA	0	-	0.4	V	ODR[1:0]=2b00
			V _{CC} =3.0 V I _{OL} =0.5 mA	0	-	0.4	V	
	V _{OL5}		V _{CC} =4.5 V I _{OL} =2.0 mA	0	-	0.4	V	ODR[1:0]=2b01
			V _{CC} =3.0 V I _{OL} =1.0 mA	0	-	0.4	V	
	V _{OL6}		V _{CC} =4.5 V I _{OL} =5.0 mA	0	-	0.4	V	ODR[1:0]=2b11
			V _{CC} =3.0 V I _{OL} =2.0 mA	0	-	0.4	V	
	V _{OL8}	TDO	V _{CC} =4.5 V I _{OL} =5.0 mA	0	-	0.4	V	
			V _{CC} =3.0 V I _{OL} =2.0 mA	0	-	0.4	V	
	V _{OL9}	P006, P007, P225, P226	V _{CC} =4.5 V I _{OL} =3.0 mA	0	-	0.4	V	I ² C

(Condition: See Recommended Operating Conditions)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input leakage current	I _{IL}	P000 to P029, P030, P031, P100 to P129, P130, P131, P200 to P229, P230, P231, P300 to P319, P320, P321, P325 to P329, P330, P331, P400 to P419, P420 to P422	V _{CC} =AV _{CC} =5.5 V V _{SS} < V _I < V _{CC}	-5	-	+5	μA	
Pull-up resistor	R _{UP1}	RSTX, NMIX	-	25	50	100	kΩ	
	R _{UP2}	P000 to P029, P030, P031, P100 to P129, P130, P131, P200 to P229, P230, P231, P300 to P319, P320, P321, P325 to P329, P330, P331, P400 to P419, P420 to P422	Pull-up resistor selected	25	50	100	kΩ	
	R _{UP4}	TDI, TMS, TCK	-	25	50	100	kΩ	
Pull-down resistor	R _{down1}	P000 to P029, P030, P031, P100 to P129, P130, P131, P200 to P229, P230, P231, P300 to P319, P320, P321, P325 to P329, P330, P331, P400 to P419, P420 to P422	Pull-down resistor selected	25	50	100	kΩ	
	R _{down3}	TRST	-	25	50	100	kΩ	
Input capacitance	C _{IN1}	P000 to P029, P030, P031, P100 to P129, P130, P131, P200 to P229, P230, P231, P300 to P319, P320, P321, P325 to P329, P330, P331, P400 to P419, P420 to P422	-	-	5	15	pF	

(T_A: -40 °C to +105 °C, V_{CC} = AV_{CC} = 5.0 V ± 0.5 V / V_{CC} = AV_{CC} = 3.3 V ± 0.3 V, V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin Name	Conditions *3		Value			Unit	Remarks		
					Min	Typ	Max				
Power supply current	I _{CC5}	V _{CC}	Normal operation		-	50	110	mA	Operating at 132 MHz, HPM 33 MHz, Peripheral 33 MHz* ¹		
			Work Flash write/erase		-	70	130	mA	Operating at 132 MHz, HPM 33 MHz, Peripheral 33 MHz* ¹		
			TC Flash write/erase		-	70	130	mA	Operating at 132 MHz, HPM 33 MHz, Peripheral 33 MHz* ¹		
			Normal operation		-	45	105	mA	Operating at 80 MHz, HPM 40 MHz, Peripheral 40 MHz		
			Work Flash write/erase		-	65	125	mA	Operating at 80 MHz, HPM 40 MHz, Peripheral 40 MHz		
			TC Flash write/erase		-	65	125	mA	Operating at 80 MHz, HPM 40 MHz, Peripheral 40 MHz		
	I _{CCS5}		CPU sleep		-	35	85	mA	Operating at 132 MHz, HPM 33 MHz, Peripheral 33 MHz* ¹		
					-	35	85	mA	Operating at 80 MHz, HPM 40 MHz, Peripheral 40 MHz		
	I _{CC75}		Timer mode		Fast CR ON	-	1190	2715	μA	T _A =25 °C, When using 4 MHz crystal for main oscillator.	
						-	915	2305	μA	T _A =25 °C, When using Slow-CR source oscillation.	
						-	925	2320	μA	T _A =25 °C, When using 32 kHz sub source oscillation.	
					Fast CR OFF * ⁴	-	990	2415	μA	T _A =25 °C, When using 4 MHz crystal for main oscillator.	
						-	715	2005	μA	T _A =25 °C, When using Slow-CR source oscillation.	
						-	725	2020	μA	T _A =25 °C, When using 32 kHz sub source oscillation.	
	I _{CC75}		Stop mode		Fast CR ON	-	915	2300	μA	T _A =25 °C	
					Fast CR OFF * ⁴	-	715	2000	μA	T _A =25 °C	
	I _{CCP}		PWU mode * ⁴ (Shutdown)			-	45	120	μA	T _A =25 °C (PWU operation cycle 16 ms)	
						-	40	105	μA	T _A =25 °C (PWU operation cycle 32 ms)	
	I _{CC752}		Timer mode (Shutdown)		Fast CR ON	-	515	790	μA	T _A =25 °C, When using 4 MHz crystal for main oscillator.	RTC operation, BackupRAM 12 KB retention.
						-	235	390	μA	T _A =25 °C, When using Slow-CR source oscillation.	
						-	245	405	μA	T _A =25 °C, When using 32 kHz sub source oscillation.	
					Fast CR OFF * ⁴	-	315	490	μA	T _A =25 °C, When using 4 MHz crystal for main oscillator.	
						-	35	90	μA	T _A =25 °C, When using Slow-CR source oscillation.	
						-	45	105	μA	T _A =25 °C, When using 32 kHz sub source oscillation.	
	I _{CC752}		Stop mode (Shutdown)		Fast CR ON	-	235	385	μA	T _A =25 °C	BackupRAM 12 KB retention.
					Fast CR OFF * ⁴	-	35	85	μA	T _A =25 °C	

*1: LQFP PKG is 80 MHz or less; TEQFP PKG is 132 MHz or less.

*3: Corresponding mode sets for state definitions are described in the chapter of "State Transition" in S6J3400 Series hardware manual.

*4: PSS mode has some restrictions. For details, see the "Restriction" of chapter "Product Description" in S6J3400 Series hardware manual.

(T_A: -40 °C to +125 °C, V_{CC} = AV_{CC} = 5.0 V ± 0.5 V / V_{CC} = AV_{CC} = 3.3 V ± 0.3 V, V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin Name	*3 Conditions		Value			Unit	Remarks		
					Min	Typ	Max				
Power supply current	I _{CC5}	V _{CC}	Normal operation		-	50	130	mA	Operating at 132 MHz, HPM 33 MHz, Peripheral 33 MHz* ²		
			Work Flash write/erase		-	70	150	mA	Operating at 132 MHz, HPM 33 MHz, Peripheral 33 MHz* ²		
			TC Flash write/erase		-	70	150	mA	Operating at 132 MHz, HPM 33 MHz, Peripheral 33 MHz* ²		
			Normal operation		-	45	125	mA	Operating at 80 MHz, HPM 40 MHz, Peripheral 40 MHz		
			Work Flash write/erase		-	65	150	mA	Operating at 80 MHz, HPM 40 MHz, Peripheral 40 MHz		
			TC Flash write/erase		-	65	150	mA	Operating at 80 MHz, HPM 40 MHz, Peripheral 40 MHz		
	I _{CCS5}		CPU sleep		-	35	110	mA	Operating at 132 MHz, HPM 33 MHz, Peripheral 33 MHz* ²		
					-	35	110	mA	Operating at 80 MHz, HPM 40 MHz, Peripheral 40 MHz		
	I _{CC75}		Timer mode		Fast CR ON	-	1190	2715	μA	T _A =25 °C, When using 4 MHz crystal for main oscillator.	
						-	915	2305	μA	T _A =25 °C, When using Slow-CR source oscillation.	
						-	925	2320	μA	T _A =25 °C, When using 32 kHz sub source oscillation.	
					Fast CR OFF ^{*4}	-	990	2415	μA	T _A =25 °C, When using 4 MHz crystal for main oscillator.	
						-	715	2005	μA	T _A =25 °C, When using Slow-CR source oscillation.	
						-	725	2020	μA	T _A =25 °C, When using 32 kHz sub source oscillation.	
	I _{CCH5}		Stop mode		Fast CR ON	-	915	2300	μA	T _A =25 °C	
					Fast CR OFF ^{*4}	-	715	2000	μA	T _A =25 °C	
	I _{CCP}		PWU mode ^{*4} (Shutdown)			-	45	120	μA	T _A =25 °C (PWU operation cycle 16 ms)	
						-	40	105	μA	T _A =25 °C (PWU operation cycle 32 ms)	
	I _{CC752}		Timer mode (Shutdown)		Fast CR ON	-	515	790	μA	T _A =25 °C, When using 4 MHz crystal for main oscillator.	RTC operation, BackupRAM 12 KB retention.
						-	235	390	μA	T _A =25 °C, When using Slow-CR source oscillation.	
						-	245	405	μA	T _A =25 °C, When using 32 kHz sub source oscillation.	
					Fast CR OFF ^{*4}	-	315	490	μA	T _A =25 °C, When using 4 MHz crystal for main oscillator.	
						-	35	90	μA	T _A =25 °C, When using Slow-CR source oscillation.	
						-	45	105	μA	T _A =25 °C, When using 32 kHz sub source oscillation.	
	I _{CCH52}		Stop mode (Shutdown)		Fast CR ON	-	235	385	μA	T _A =25 °C	BackupRAM 12 KB retention.
					Fast CR OFF ^{*4}	-	35	85	μA	T _A =25 °C	

*2. It is a condition that can be used by limiting the product type of TEQFP.

*3: Corresponding mode sets for state definitions are described in the chapter of "State Transition" in S6J3400 Series hardware manual.

*4: PSS mode has some restrictions. For details, see the "Restriction" of chapter "Product Description" in S6J3400 Series hardware manual.

7.4 AC Characteristics

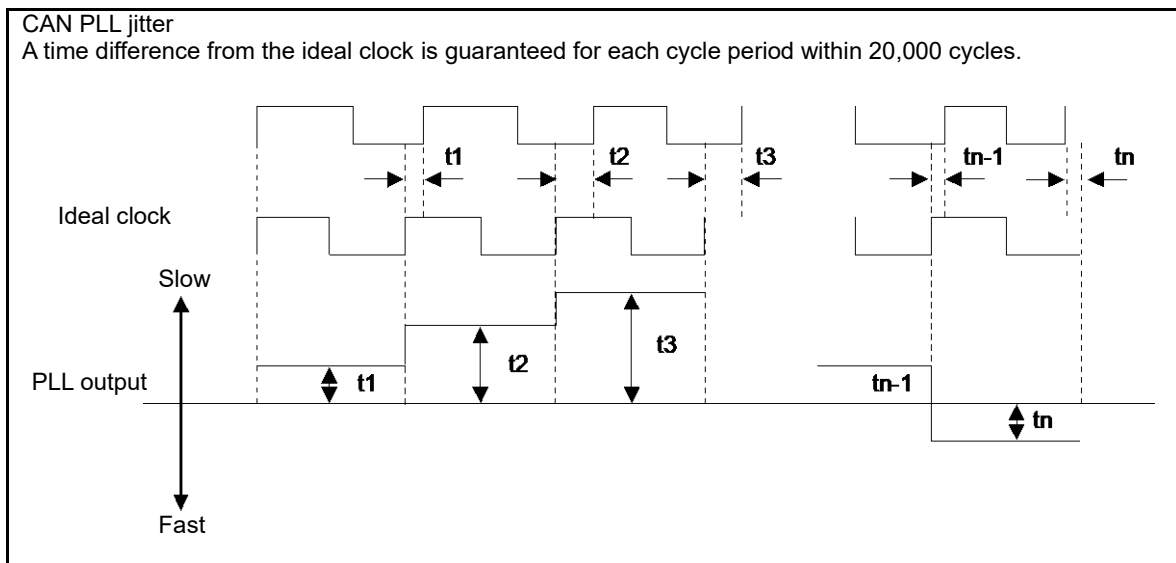
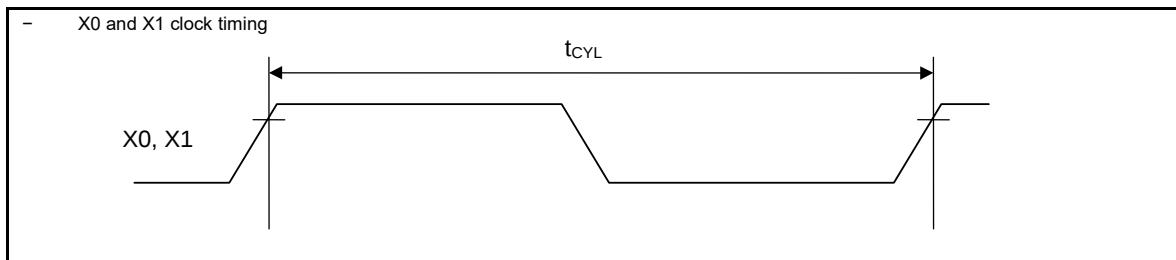
7.4.1 Source Clock Timing

(Condition: See Recommended Operating Conditions)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Source oscillation clock frequency	f_C	X0, X1	-	3.6	-	16	MHz	
Source oscillation clock cycle time	t_{CYL}	X0, X1	-	62.5	-	277.8	ns	
CAN PLL jitter (when locked)	t_{PJ}	-	-	-10	-	10	ns	
Internal Slow CR oscillation frequency	f_{CRS}	-	-	50	100	150	kHz	
Internal Fast CR oscillation frequency	f_{CRF}	-	-	2.40	4.00	5.61	MHz	

Notes:

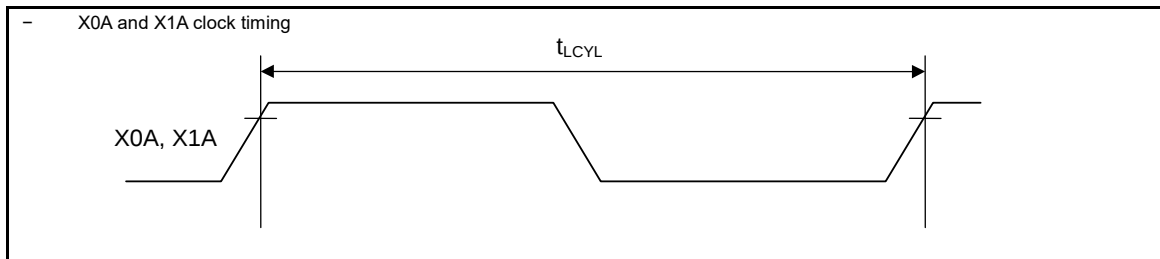
- The maximum/minimum values have been standardized with the main clock and PLL clock in use.
- Jitter of source oscillator must be smaller than 300 ppm.



7.4.2 Sub Clock Timing

(Condition: See Recommended Operating Conditions)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Source oscillation clock frequency	f_{CL}	X0A, X1A	-	-	32.768	-	kHz	
Source oscillation clock cycle time	t_{LCYL}	X0A, X1A	-	-	30.52	-	μs	



7.4.3 Internal Clock Timing

- This section shows the target characteristics for internal clock timing at the current stage.
- In the Symbol column, same clock names as described in the chapter of “Clock System” in TRAVEO™ T1G Platform hardware manual are used.
- Corresponding functions for these clocks are described in the chapter of “Clock Configuration” in S6J3400 series hardware manual.

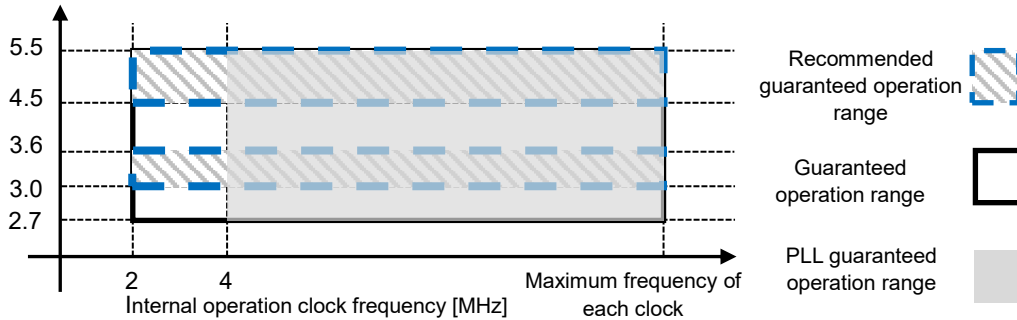
(Condition: See Recommended Operating Conditions)

Parameter	Symbol	Pin Name	Conditions	Value				Unit	Remarks
				Min	Typ	Max ^{*1}	Max ^{*2}		
Internal clock frequency	fSSCG0out	-	-	200	-	320	320	MHz	
	fPLL0out	-	-	200	-	320	320	MHz	
	fCLK_CPU	-	-	-	-	132	80	MHz	
	fCLK_SHE	-	-	-	-	33	40	MHz	
	fCLK_FCLK	-	-	-	-	66	80	MHz	
	fCLK_ATB	-	-	-	-	66	40	MHz	
	fCLK_DBG	-	-	-	-	66	40	MHz	
	fCLK_HPM	-	-	-	-	33	40	MHz	
	fCLK_DMA	-	-	-	-	33	40	MHz	
	fCLK_MEMC	-	-	-	-	33	40	MHz	
	fCLK_SYSC1	-	-	-	-	33	40	MHz	
	fCLK_LLPM	-	-	-	-	132	80	MHz	
	fCLK_LCP	-	-	-	-	66	80	MHz	
	fCLK_LCP0	-	-	-	-	33	40	MHz	
	fCLK_LCP0A	-	-	-	-	40	40	MHz	
	fCLK_LCP1	-	-	-	-	33	40	MHz	
	fCLK_LCP1A	-	-	-	-	40	40	MHz	
	fCLK_TRC	-	-	-	-	66	40	MHz	
	fCLK_SYSC0H	-	-	-	-	33	40	MHz	
	fCLK_COMH	-	-	-	-	33	40	MHz	
	fCLK_CAN	-	-	-	-	48	48	MHz	
	fCLK_JTAG	-	-	-	-	20	20	MHz	
	fCLK_CLKO	-	-	-	-	10	10	MHz	

*1: Target maximum clock frequencies when CPU clock is 132 MHz with the TEQFP package

*2: Target maximum clock frequencies when CPU clock is 80 MHz with the LQFP package

- Operation assurance range; Relationship between the internal clock frequency and supply voltage
Power supply [V]

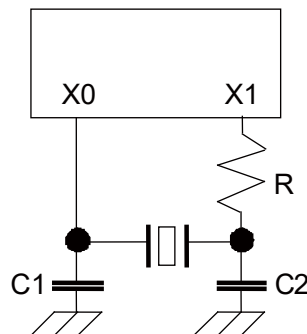


Note: CPU will be reset, when the power supply voltage is equal to or less than LVD setting voltage.

- Relationship between the oscillation clock frequency and internal clock frequency

		Internal Operation Clock Frequency							
		Main Clock	PLL Clock						
			Multiplied by 1	Multiplied by 2	Multiplied by 3	Multiplied by 4	...	Multiplied by 20	Multiplied by 33
Oscillation clock frequency [MHz]	4	2	4	8	12	16	...	80	132

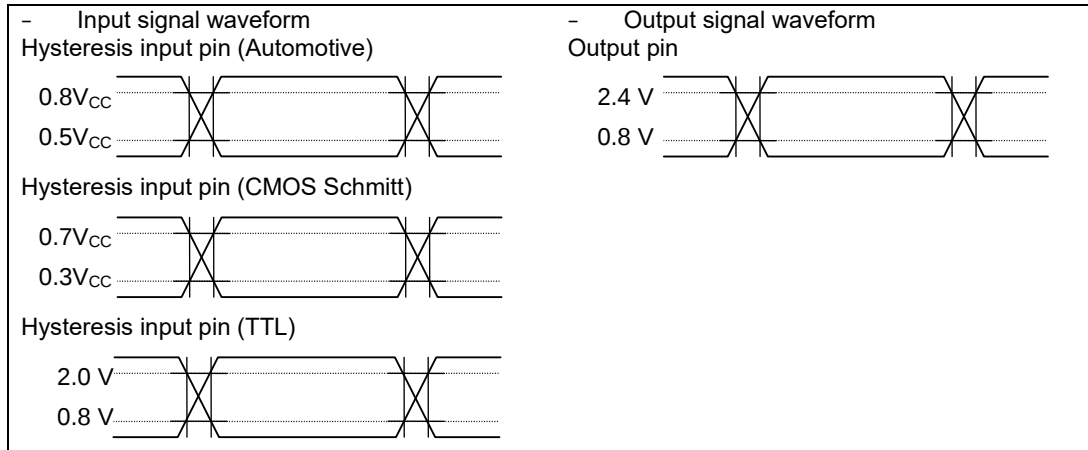
- Oscillation circuit example



Note:

For the configuration of an oscillation circuit, request the oscillator manufacturer to perform a circuit matching evaluation before starting design.

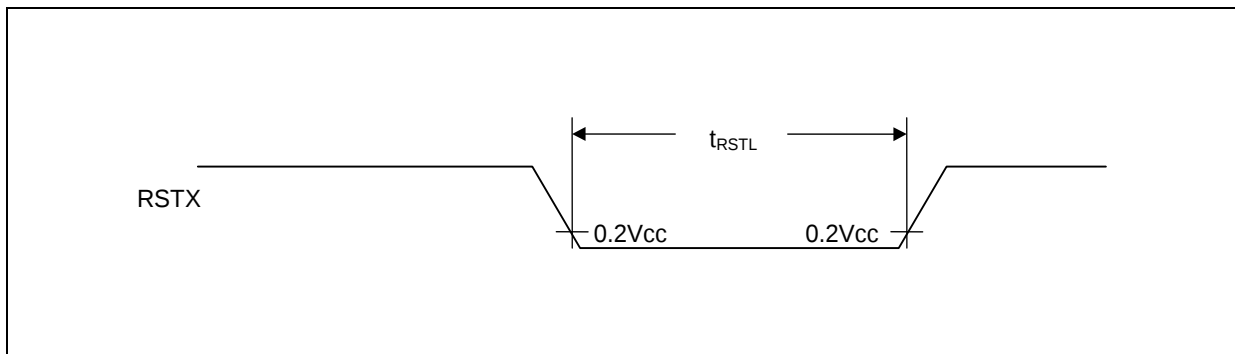
AC characteristics are specified by the following measurement reference voltage values.



7.4.4 Reset Input

(Condition: See Recommended Operating Conditions)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Reset input time	t _{RSTL}	RSTX	-	10	-	μs	
Reset input pulse filtered				-	1	μs	



7.4.5 Power-on Conditions

(Condition: See Recommended Operating Conditions)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Level detection voltage	-	VCC	-	2.2	2.4	2.6	V	
Level detection hysteresis width	-	VCC	-	-	100	-	mV	
Level detection time	-	-	-	-	-	40	μs	*1
Power off time	-	VCC	-	100	-	-	μs	*2
Power ramp rate	dV/dt	VCC	VCC: 1.5 V to 2.6 V	-	-	1	V/μs	*3
Maximum ramp rate guaranteed to not generate power-on reset	dV/dt	VCC	VCC: Between 2.7 V and 4.5 V	-	-	50	mV/μs	*4

*1: This specification is at 1 V/μs of power ramp rate.

*2: VCC must be held below 1.5 V for a minimum period of t_{OFF} .

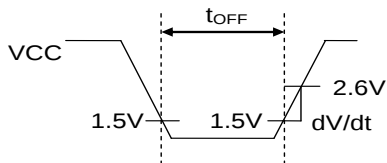
*3: Power ramp rate must be 1 V/μs or less from 1.5 V to 2.6 V.
Power-on can detect by satisfying power ramp rate and power off time.

*4: This specification is specified the power supply fluctuation after power on detection. When VCC voltage is between 2.7 V and 4.5 V, the power supply fluctuation is below 50 mV/μs, the detection of power-on is suppressed. The power-on does not detect in any power fluctuation between 4.5 V and 5.5 V.

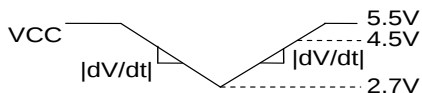
Note:

When using the S6J3400 Series,*2 and *3 must be satisfied. When neither *2 nor *3 can be satisfied, assert external reset (RSTX) at power up and any brownout event.

• Power off time, Power ramp rate



• Maximum ramp rate guaranteed to not generate power-on reset



7.4.6 Multi-Function Serial

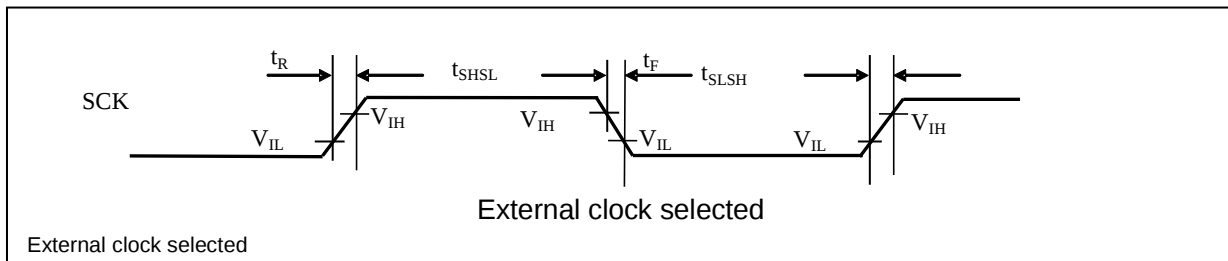
7.4.6.1 Asynchronous serial interface (UART) Timing (SMR:MD2-0=0b000, 0b001)

External Clock Selected (BGR:EXT=1)

(Condition: See Recommended Operating Conditions)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock "L" pulse width	t _{SLSH}	SCK0 to SCK13	-	t _{CLK_LCPnA} ^{*1} +10	-	ns	
Serial clock "H" pulse width	t _{SHSL}	SCK0 to SCK13		t _{CLK_LCPnA} ^{*1} +10	-	ns	
SCK falling time	t _F	SCK0 to SCK13		-	5	ns	
SCK rising time	t _R			-	5	ns	

*1: n=0:ch.0 to ch.7, n=1:ch.8 to ch.13



7.4.6.2 CSIO Timing (SMR:MD2-0=0b010)

(1) Normal Synchronous Transfer (SCR:SPI=0) and Mark Level "H" of Serial Clock Output (SMR:SCINV=0)

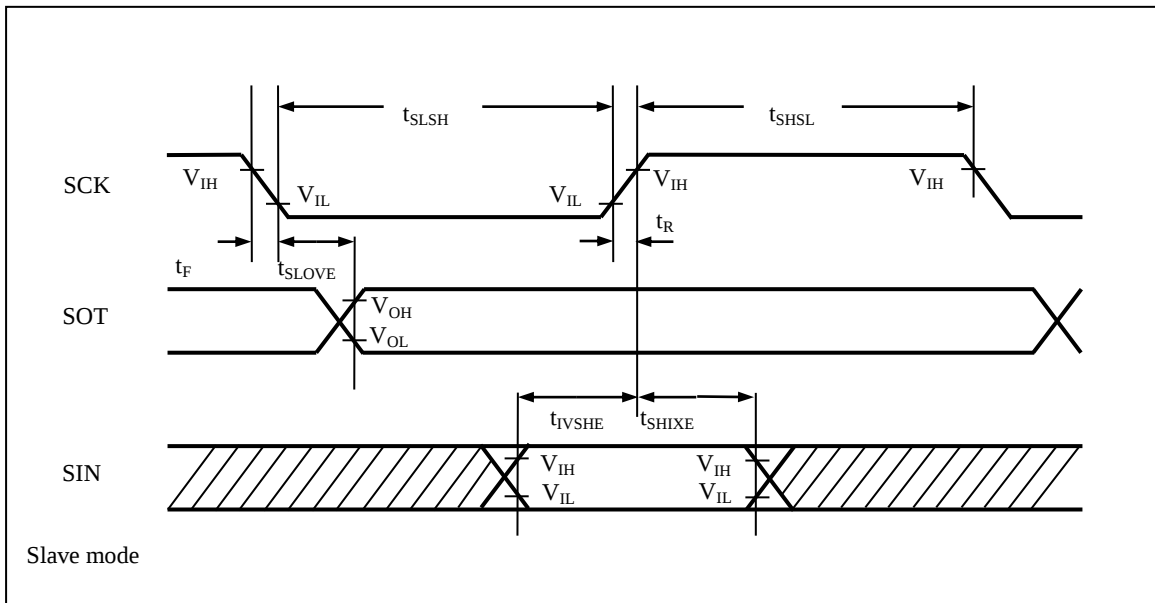
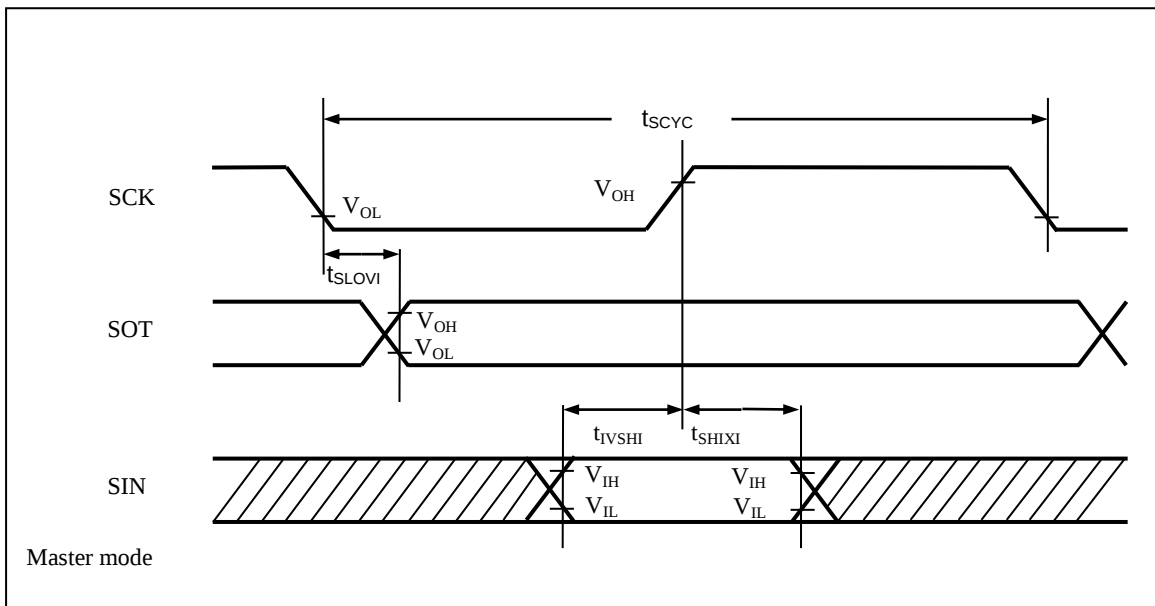
(Condition: See Recommended Operating Conditions)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t _{SCYC}	SCK0 to SCK13	Master Mode (C _L = 20 pF, I _{OL} =-2 mA, I _{OH} =2 mA)	4t _{CLK_LCPnA} ^{*1}	-	ns	
SCK ↓ → SOT delay time	t _{SLOVI}	SCK0 to SCK13 SOT0 to SOT13		-30	+30	ns	
Valid SIN → SCK ↑ setup time	t _{IVSHI}	SCK0 to SCK13 SIN0 to SIN13		30	-	ns	
SCK ↑→ Valid SIN hold time	t _{SHIXI}			0	-	ns	
Serial clock "H" pulse width	t _{SHSL}	SCK0 to SCK13	Slave Mode (C _L =20 pF, I _{OL} =-2 mA, I _{OH} =2 mA)	2t _{CLK_LCPnA} ^{*1}	-	ns	
Serial clock "L" pulse width	t _{SLSH}	SCK0 to SCK13		2t _{CLK_LCPnA} ^{*1}	-	ns	
SCK ↓→ SOT delay time	t _{SLOVE}	SCK0 to SCK13, SOT0 to SOT13		-	30	ns	
Valid SIN → SCK ↑ setup time	t _{IVSHE}	SCK0 to SCK13, SIN0 to SIN13		10	-	ns	
SCK ↑ → Valid SIN hold time	t _{SHIXE}			20	-	ns	
SCK falling time	t _F	SCK0 to SCK13		-	5	ns	
SCK rising time	t _R	SCK0 to SCK13		-	5	ns	

*1: n=0:ch.0 to ch.7, n=1:ch.8 to ch.13

Notes:

- This table provides the alternate current standard for CLK synchronous mode.
- C_L is the load capability value connected to the pin during testing.
- The maximum baud rate is limited by the internal operating clock used and other parameters. For details, see the hardware manual.



(2) Normal Synchronous Transfer (SCR:SPI=0) and Mark Level "L" of Serial Clock Output (SMR:SCINV=1)

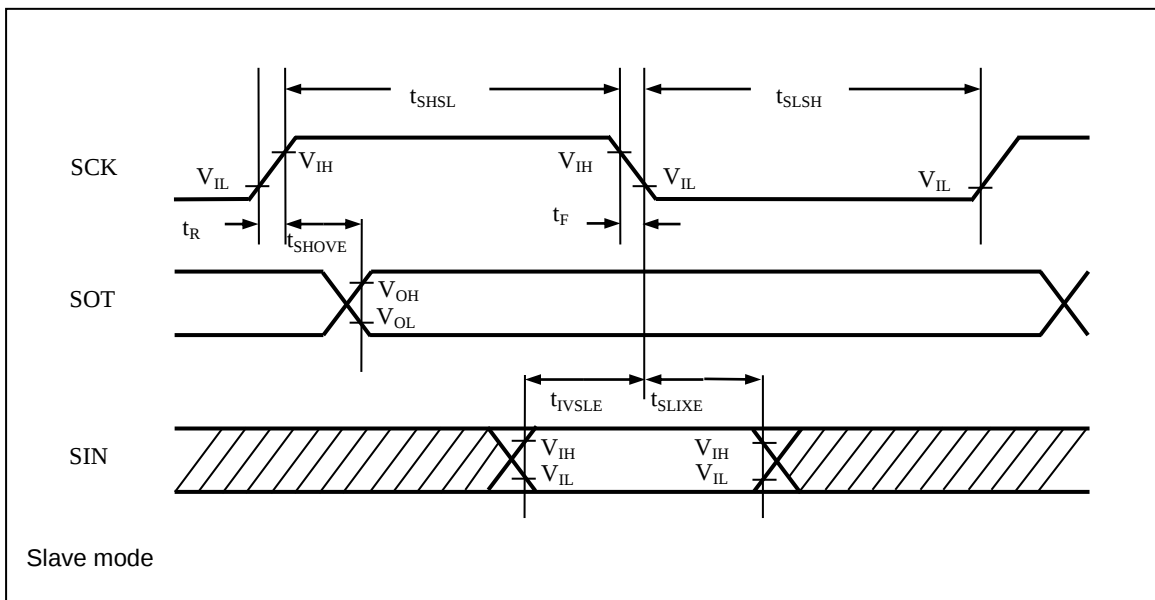
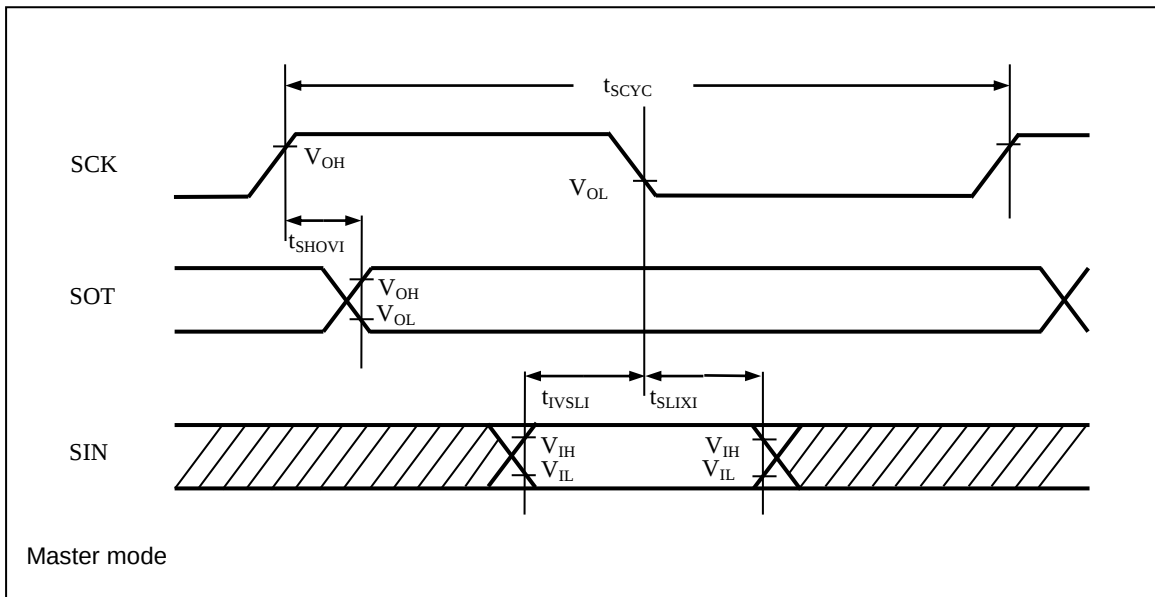
(Condition: See Recommended Operating Conditions)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	tSCYC	SCK0 to SCK13	Master Mode (CL = 20 pF, IOL=-2 mA, IOH=2 mA)	4tCLK_LCPnA*1	-	ns	
SCK ↑ → SOT delay time	tSHOVI	SCK0 to SCK13 SOT0 to SOT13		-30	+30	ns	
Valid SIN → SCK ↓ setup time	tIVSLI	SCK0 to SCK13 SIN0 to SIN13		30	-	ns	
SCK ↓ → Valid SIN hold time	tSLIXI			0	-	ns	
Serial clock "H" pulse width	tSHSL	SCK0 to SCK13	Slave Mode (CL=20 pF, IOL=-2 mA, IOH=2 mA)	2tCLK_LCPnA*1	-	ns	
Serial clock "L" pulse width	tSLSH	SCK0 to SCK13		2tCLK_LCPnA*1	-	ns	
SCK ↑ → SOT delay time	tSHOVE	SCK0 to SCK13 SOT0 to SOT13		-	30	ns	
Valid SIN → SCK ↓ setup time	tIVSLE	SCK0 to SCK13 SIN0 to SIN13		10	-	ns	
SCK ↓ → Valid SIN hold time	tSLIXE			20	-	ns	
SCK falling time	tF	SCK0 to SCK13		-	5	ns	
SCK rising time	tR	SCK0 to SCK13		-	5	ns	

*1: n=0:ch.0 to ch.7, n=1:ch.8 to ch.13

Notes:

- This table provides the alternate current standard for CLK synchronous mode.
- C_L is the load capability value connected to the pin during testing.
- The maximum baud rate is limited by the internal operating clock used and other parameters. For details, see the hardware manual.



(3) SPI Supported (SCR:SPI=1), and Mark Level "H" of Serial Clock Output (SMR:SCINV=0)

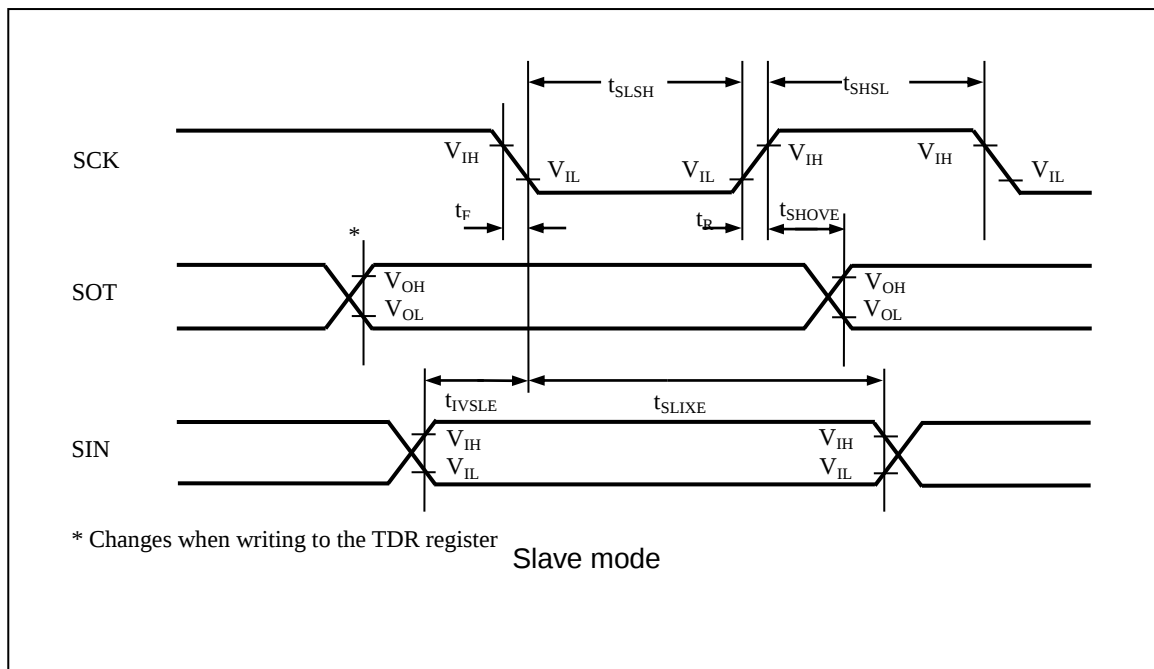
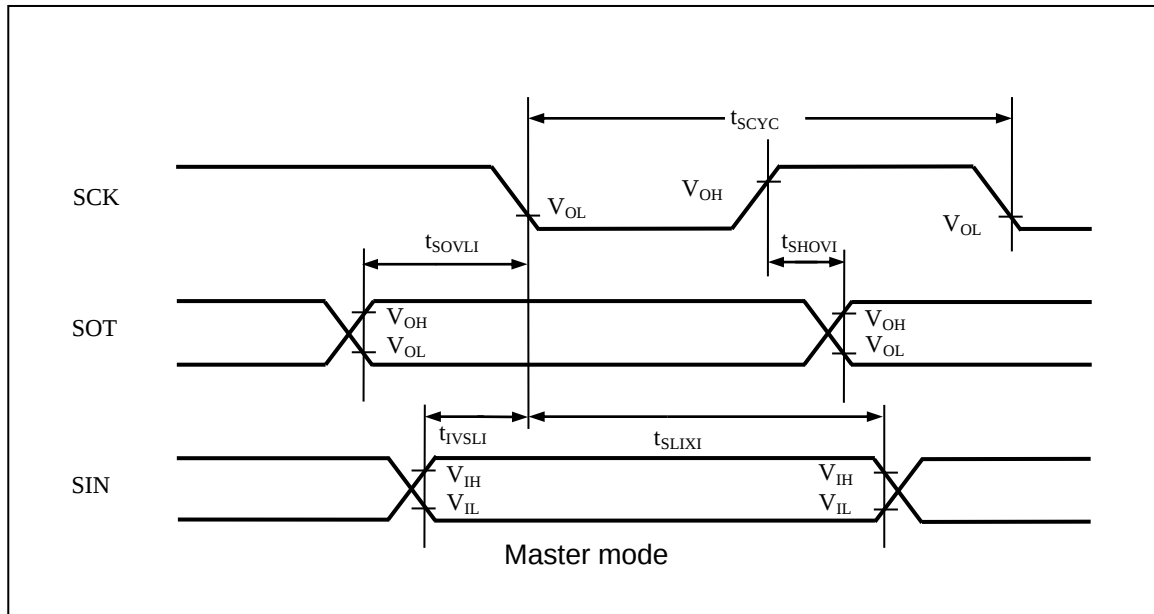
(Condition: See Recommended Operating Conditions)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	tSCYC	SCK0 to SCK13	Master Mode (CL = 20 pF, IOL=-2 mA, IOH=2 mA)	4tCLK_LCPnA*1	-	ns	
SCK ↑ → SOT delay time	tSHOVI	SCK0 to SCK13 SOT0 to SOT13		-30	+30	ns	
Valid SIN → SCK ↓ setup time	tIVSLI	SCK0 to SCK13 SIN0 to SIN13		30	-	ns	
SCK ↓ → Valid SIN hold time	tSLIXI			0	-	ns	
SOT → SCK ↓ delay time	tSOVLI	SCK0 to SCK13 SOT0 to SOT13		2tCLK_LCPnA*1 - 30	-	ns	
Serial clock "H" pulse width	tSHSL	SCK0 to SCK13	Slave Mode (CL=20 pF, IOL=-2 mA, IOH=2 mA)	2tCLK_LCPnA*1	-	ns	
Serial clock "L" pulse width	tSLSH	SCK0 to SCK13		2tCLK_LCPnA*1	-	ns	
SCK ↑ → SOT delay time	tSHOVE	SCK0 to SCK13 SOT0 to SOT13		-	30	ns	
Valid SIN → SCK ↓ setup time	tIVSLE	SCK0 to SCK13 SIN0 to SIN13		10	-	ns	
SCK ↓ → Valid SIN hold time	tSLIXE			20	-	ns	
SCK falling time	tF	SCK0 to SCK13		-	5	ns	
SCK rising time	tR	SCK0 to SCK13		-	5	ns	

*1: n=0:ch.0 to ch.7, n=1:ch.8 to ch.13

Notes:

- This table provides the alternate current standard for CLK synchronous mode.
- C_L is the load capability value connected to the pin during testing.
- The maximum baud rate is limited by the internal operating clock used and other parameters. For details, see the hardware manual.



(4) SPI Supported (SCR:SPI=1), and Mark Level "L" of Serial Clock Output (SMR:SCINV=1)

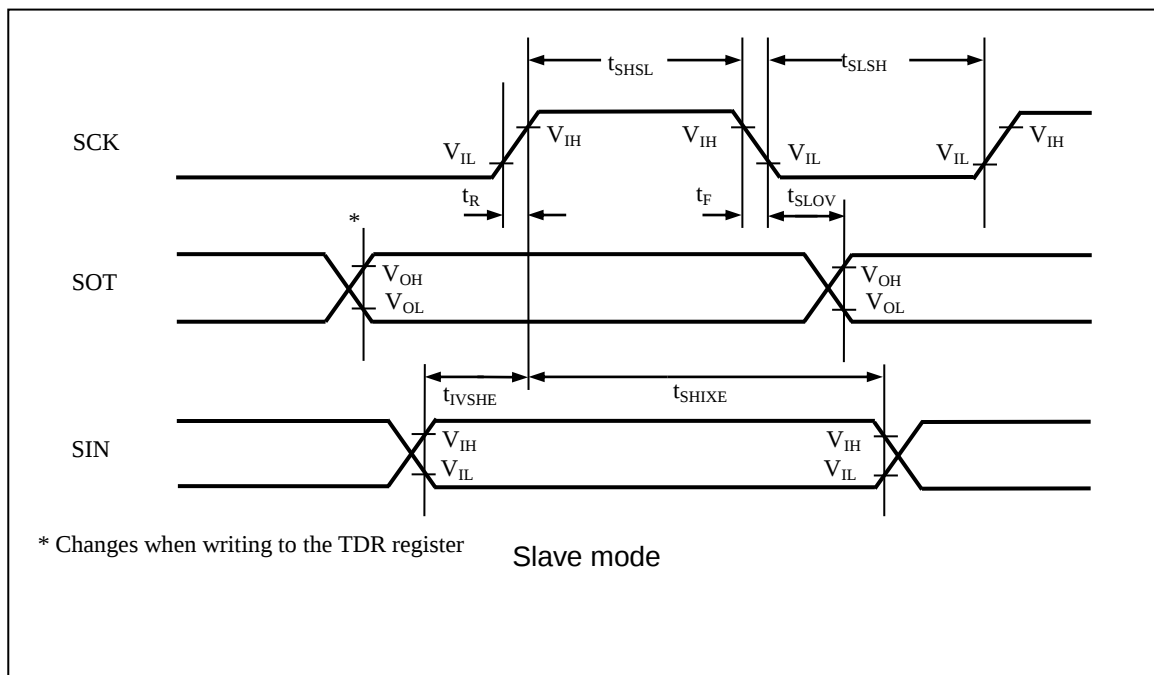
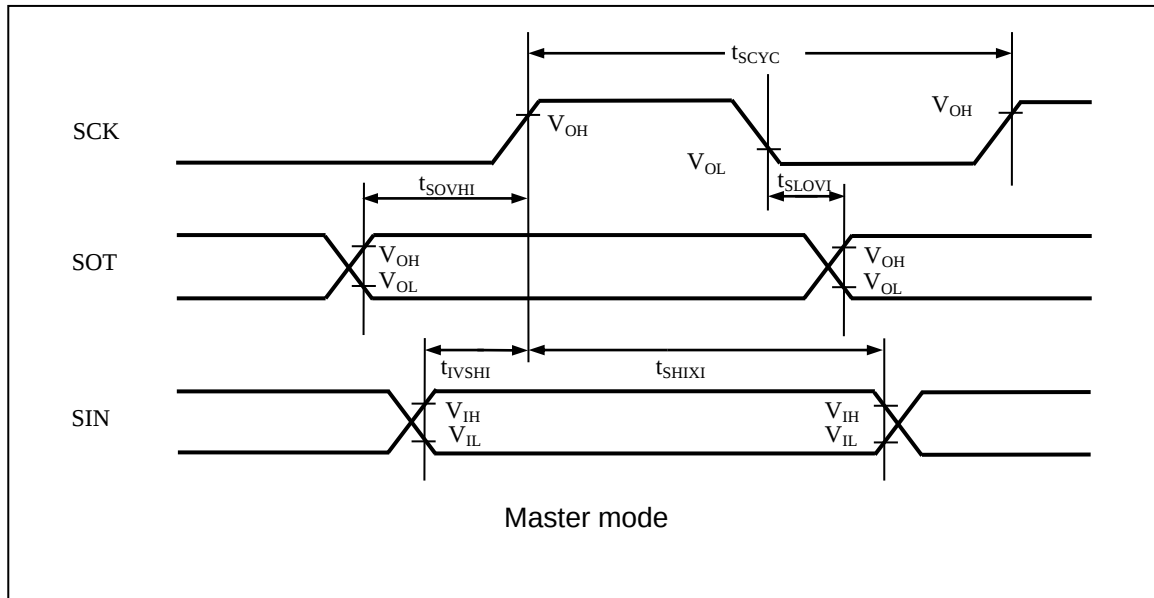
(Condition: See Recommended Operating Conditions)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	tSCYC	SCK0 to SCK13	Master Mode (CL = 20 pF, IOL=-2 mA, IOH=2 mA)	4tCLK_LCPnA*1	-	ns	
SCK ↓ → SOT delay time	tSLOVI	SCK0 to SCK13 SOT0 to SOT13		-30	+30	ns	
Valid SIN → SCK ↑ setup time	tIVSHI	SCK0 to SCK13 SIN0 to SIN13		30	-	ns	
SCK ↑ → Valid SIN hold time	tSHIXI			0	-	ns	
SOT → SCK ↑ delay time	tSOVHI	SCK0 to SCK13 SOT0 to SOT13		2tCLK_LCPnA*1 - 30	-	ns	
Serial clock "H" pulse width	tSHSL	SCK0 to SCK13	Slave Mode (CL=20 pF, IOL=-2 mA, IOH=2 mA)	2tCLK_LCPnA*1	-	ns	
Serial clock "L" pulse width	tSLSH	SCK0 to SCK13		2tCLK_LCPnA*1	-	ns	
SCK ↓ → SOT delay time	tSLOVE	SCK0 to SCK13 SOT0 to SOT13		-	30	ns	
Valid SIN → SCK ↑ setup time	tIVSHE	SCK0 to SCK13 SIN0 to SIN13		10	-	ns	
SCK ↑ → Valid SIN hold time	tSHIXE			20	-	ns	
SCK falling time	tF	SCK0 to SCK13		-	5	ns	
SCK rising time	tR	SCK0 to SCK13		-	5	ns	

*1: n=0:ch.0 to ch.7, n=1:ch.8 to ch.13

Notes:

- This table provides the alternate current standard for CLK synchronous mode.
- C_L is the load capability value connected to the pin during testing.
- The maximum baud rate is limited by the internal operating clock used and other parameters. For details, see the hardware manual.



(5) Serial Chip Select Used (SCSCR:CSEN=1)

- Mark level "H" of serial clock output (SMR, SCSFR:SCINV=0)
- Inactive level "H" of serial chip select (SCSCR, SCSFR:CSLVL=1)

(Condition: See Recommended Operating Conditions)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
SCS ↑ → SCK ↓ setup time	t _{CSSI}	SCK0 to SCK13 SCS0x to SCS13x	Master Mode (C _L = 20 pF, I _{OL} =-2 mA, I _{OH} =2 mA)	t _{CSSU} ^{*1} -50	-	ns	
SCK ↑ → SCS ↑ hold time	t _{CSHI}			t _{CSHD} ^{*2} +0	-	ns	
SCS deselect time	t _{CSDI}	SCS0x to SCS13x		t _{CSDS} ^{*3} -50 +5t _{CLK_LCPnA} ^{*4}	-	ns	
SCS ↓ → SCK ↓ setup time	t _{CSSE}	SCK0 to SCK13 SCS0x to SCS13x	Slave Mode (C _L =20 pF, I _{OL} =-2 mA, I _{OH} =2 mA)	3t _{CLK_LCPnA} ^{*4} +30	-	ns	
SCK ↑ → SCS ↑ hold time	t _{CSHE}	SCK0 to SCK13 SCS0x to SCS13x		0	-	ns	
SCS deselect time	t _{CSDE}	SCS0x to SCS13x		3t _{CLK_LCPnA} ^{*4} +30	-	ns	
SCS ↓ → SOT delay time	t _{DSE}	SCS0x to SCS13x SOT0 to SOT13		-	40	ns	
SCS ↑ → SOT delay time	t _{DDE}			0	-	ns	
SCK ↓ → SCS ↓ clock switching time	t _{SCC}	SCK0 to SCK13 SCS0x to SCS13x	Master mode round operation (C _L =20 pF, I _{OL} =-2 mA, I _{OH} =2 mA)	3t _{CLK_LCPnA} ^{*4} +0	3t _{CLK_LCPnA} ^{*4} +50	ns	

*1: t_{CSSU}=SCSTR:CSSU[7:0] x serial chip select timing operating clock

*2: t_{CSHD}=SCSTR:CSHD[7:0] x serial chip select timing operating clock

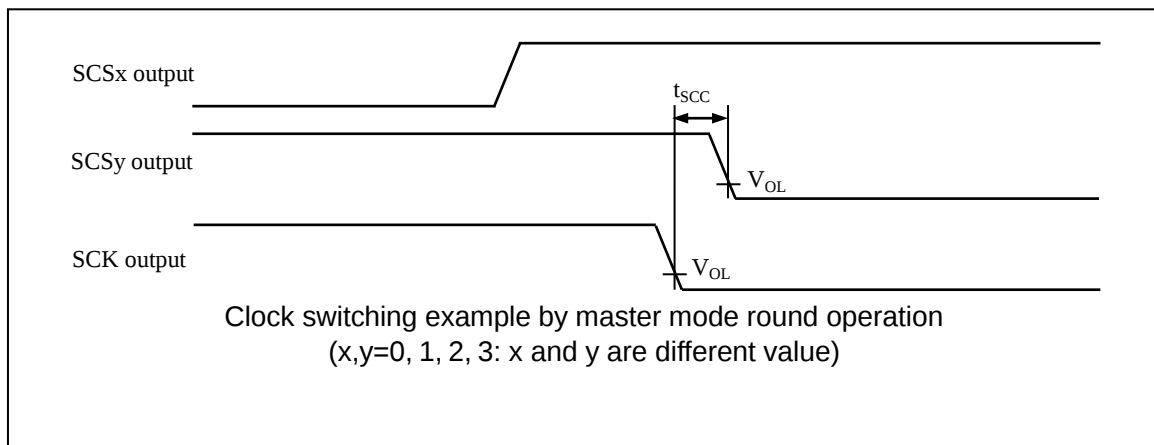
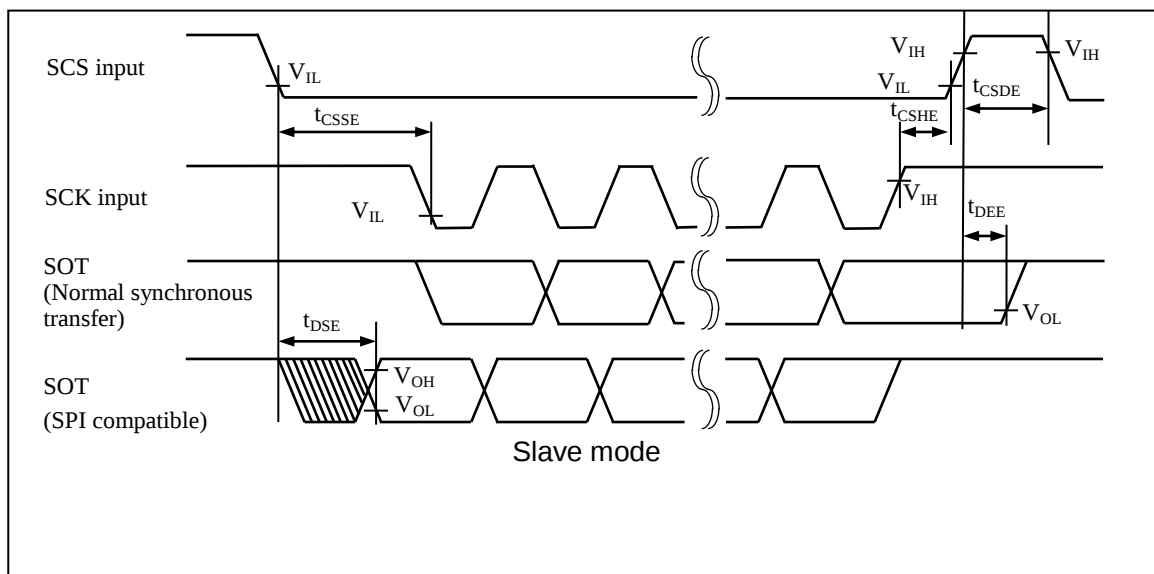
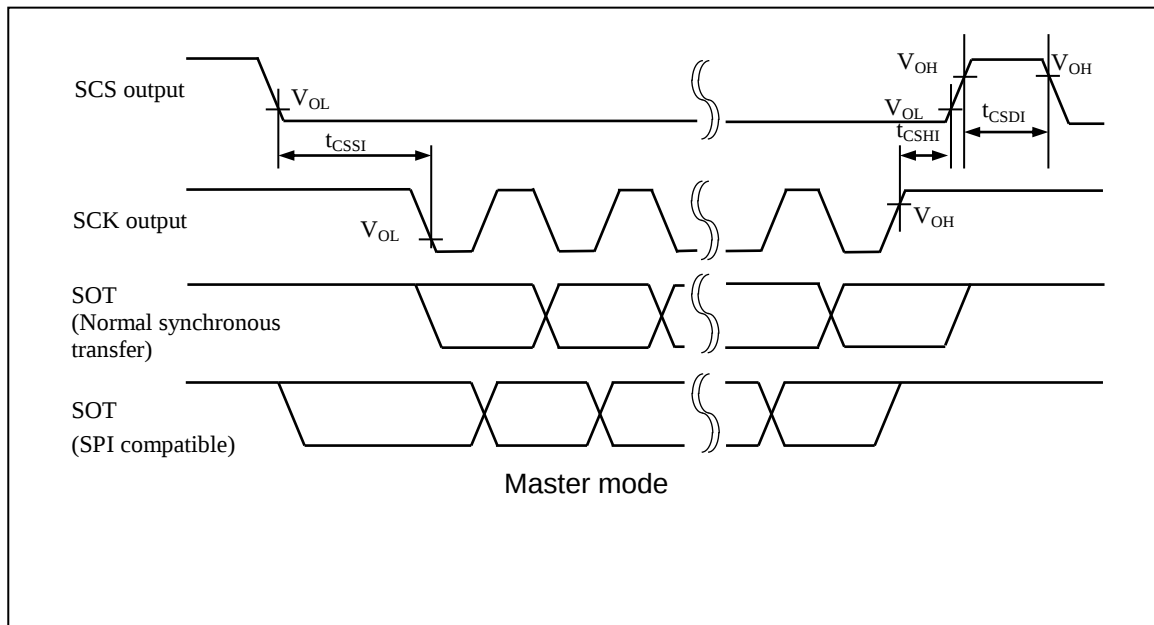
*3: t_{CSDS}=SCSTR:CSDS[15:0] x serial chip select timing operating clock

For details on *1, *2, and *3 above, see the hardware manual.

*4: t_{CLK_LCPnA} n=0:ch.0 to ch.7, n=1:ch.8 to ch.13

Notes:

- This is the AC characteristic in CLK synchronized mode.
- C_L is the load capacitance applied to pins during testing.
- The maximum baud rate is limited by the internal operating clock used and other parameters.
For details, see the hardware manual.



(6) Serial Chip Select Used (SCSCR:CSSEN=1)

■ Serial clock output signal detect level "L" (SMR, SCSTR:SCINV=1)

■ Serial chip select inactive level "H" (SCSCR, SCSTR:CSLVL=1)

(Condition: See Recommended Operating Conditions)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
SCS ↓→ SCK ↑ setup time	t _{CSSI}	SCK0 to SCK13 SCS0x to SCS13x	Master mode (C _L =20 pF, I _{OL} =-2 mA, I _{OH} =2 mA)	t _{CSSU} ^{*1} -50	-	ns	
SCK ↓→ SCS ↑ hold time	t _{CSHI}			t _{CSHD} ^{*2} +0	-	ns	
SCS deselect time	t _{CSDI}	SCS0x to SCS13x		t _{CSDS} ^{*3} -50 +5 t _{CLK_LCPnA} ^{*4}	-	ns	
SCS ↓ → SCK ↑ setup time	t _{CSSE}	SCK0 to SCK13 SCS0x to SCS13x	Slave mode (C _L =20 pF, I _{OL} =-2 mA, I _{OH} =2 mA)	3t _{CLK_LCPnA} ^{*4} +30	-	ns	
SCK ↓ → SCS ↑ hold time	t _{CSHE}	SCK0 to SCK13 SCS0x to SCS13x		0	-	ns	
SCS deselect time	t _{CSDE}	SCS0x to SCS13x		3t _{CLK_LCPnA} ^{*4} +30	-	ns	
SCS ↓ → SOT delay time	t _{DSE}	SCS0x to SCS13x SOT0 to SOT13		-	40	ns	
SCS ↑ → SOT delay time	t _{DDE}			0	-	ns	
SCK ↑ → SCS ↓ clock switching time	t _{SCC}	SCK0 to SCK13 SCS0x to SCS13x	Master mode round operation (CL=20 pF, I _{OL} =-2 mA, I _{OH} =2 mA)	3t _{CLK_LCPnA} ^{*4} +0	3t _{CLK_LCPnA} ^{*4} +50	ns	

*1: $t_{CSSU}=SCSTR:CSSU[7:0]$ x serial chip select timing operating clock

*2: $t_{CSHD}=SCSTR:CSHD[7:0]$ x serial chip select timing operating clock

*3: $t_{CSDS}=SCSTR:CSDS[15:0]$ x serial chip select timing operating clock

For details on *1, *2, and *3 above, see the hardware manual.

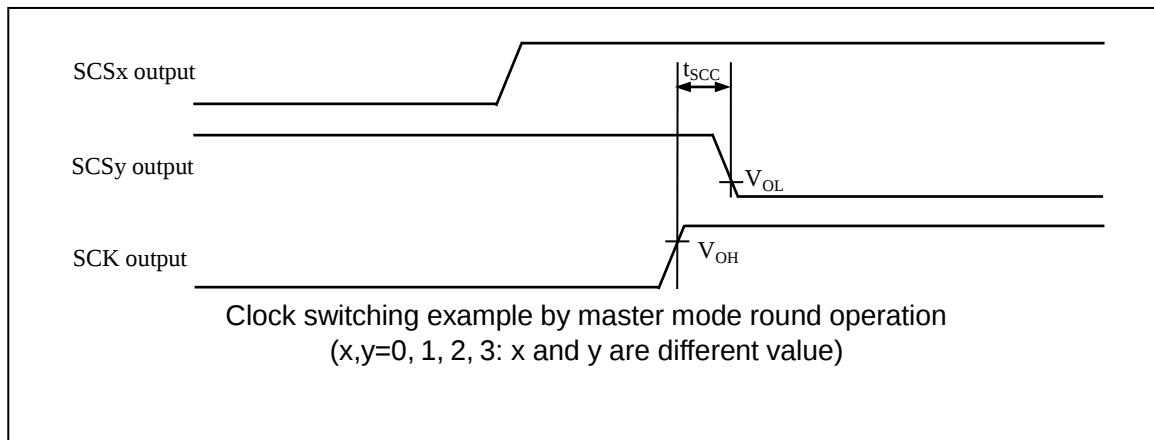
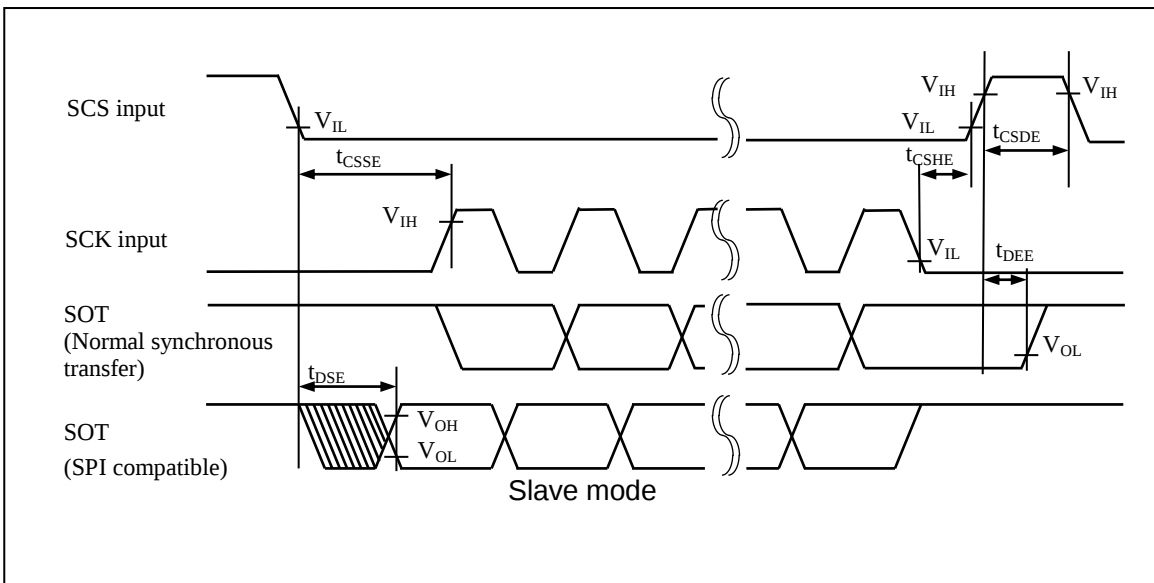
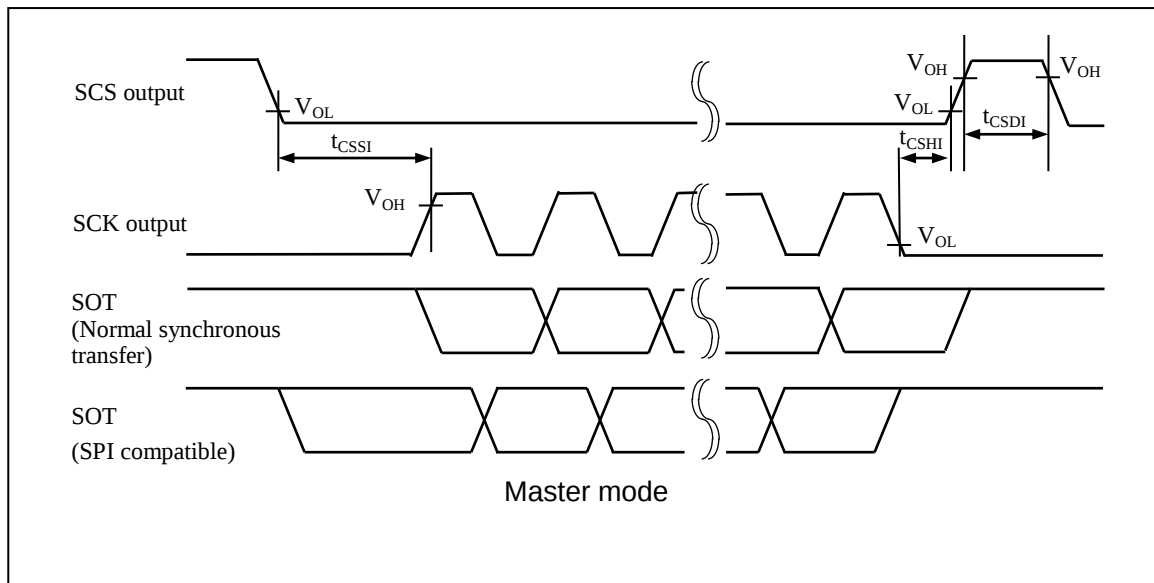
*4: t_{CLK_LCPnA} n=0:ch.0 to ch.7, n=1:ch.8 to ch.13

Notes:

■ This is the AC characteristic in CLK synchronized mode.

■ C_L is the load capacitance applied to pins during testing.

■ The maximum baud rate is limited by the internal operating clock used and other parameters.
For details, see the hardware manual.



(7) Serial Chip Select Used (SCSCR:CSEN=1)

■ Serial clock output signal detect level "H" (SMR, SCSFR:SCINV=0)

■ Serial chip select inactive level "L" (SCSCR, SCSFR:CSLVL=0)

(Condition: See Recommended Operating Conditions)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
SCS ↑ → SCK ↓ setup time	t _{CSSU}	SCK0 to SCK13 SCS0x to SCS13x	Master mode (C _L =20 pF, I _{OL} =-2 mA, I _{OH} =2 mA)	t _{CSSU} ^{*1} -50	-	ns	
SCK ↑ → SCS ↓ hold time	t _{CSDH}			t _{CSDH} ^{*2} +0	-	ns	
SCS deselect time	t _{CSDI}	SCS0x to SCS13x		t _{CSDS} ^{*3} -50 +5 t _{CLK_LCPnA} ^{*4}	-	ns	
SCS ↑ → SCK ↓ setup time	t _{CSSE}	SCK0 to SCK13 SCS0x to SCS13x	Slave mode (C _L =20 pF, I _{OL} =-2 mA, I _{OH} =2 mA)	3t _{CLK_LCPnA} ^{*4} +30	-	ns	
SCK ↑ → SCS ↓ hold time	t _{CSHE}	SCK0 to SCK13 SCS0x to SCS13x		0	-	ns	
SCS deselect time	t _{CSDE}	SCS0x to SCS13x		3t _{CLK_LCPnA} ^{*4} +30	-	ns	
SCS ↑ → SOT delay time	t _{DSE}	SCS0x to SCS13x SOT0 to SOT13		-	40	ns	
SCS ↓ → SOT delay time	t _{DEE}			0	-	ns	
SCK ↓ → SCS ↑ clock switching time	t _{SCC}	SCK0 to SCK13 SCS0x to SCS13x	Master mode round operation (C _L =20 pF, I _{OL} =-2 mA, I _{OH} =2 mA)	3t _{CLK_LCPnA} ^{*4} +0	3t _{CLK_LCPnA} ^{*4} +50	ns	

*1: t_{CSSU}=SCSTR:CSSU[7:0] x serial chip select timing operating clock

*2: t_{CSDH}=SCSTR:CSDH[7:0] x serial chip select timing operating clock

*3: t_{CSDS}=SCSTR:CSDS[15:0] x serial chip select timing operating clock

For details on *1, *2, and *3 above, see the hardware manual.

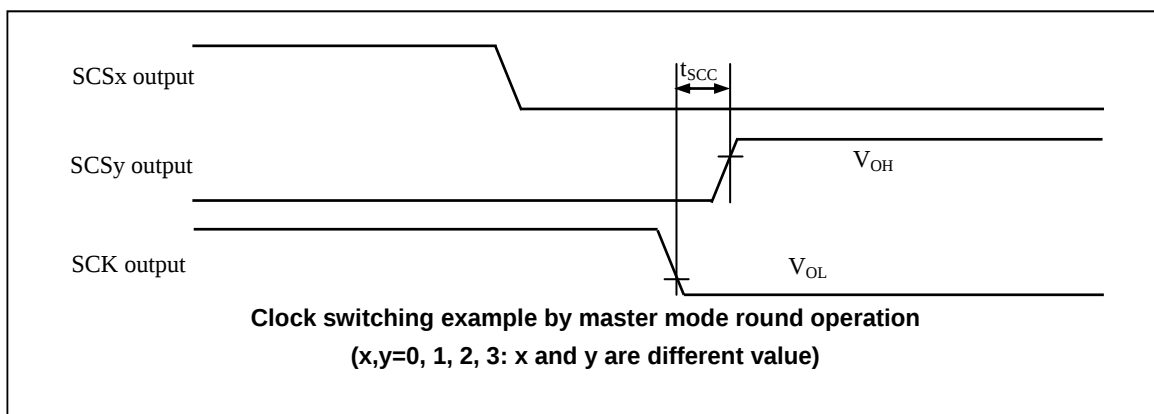
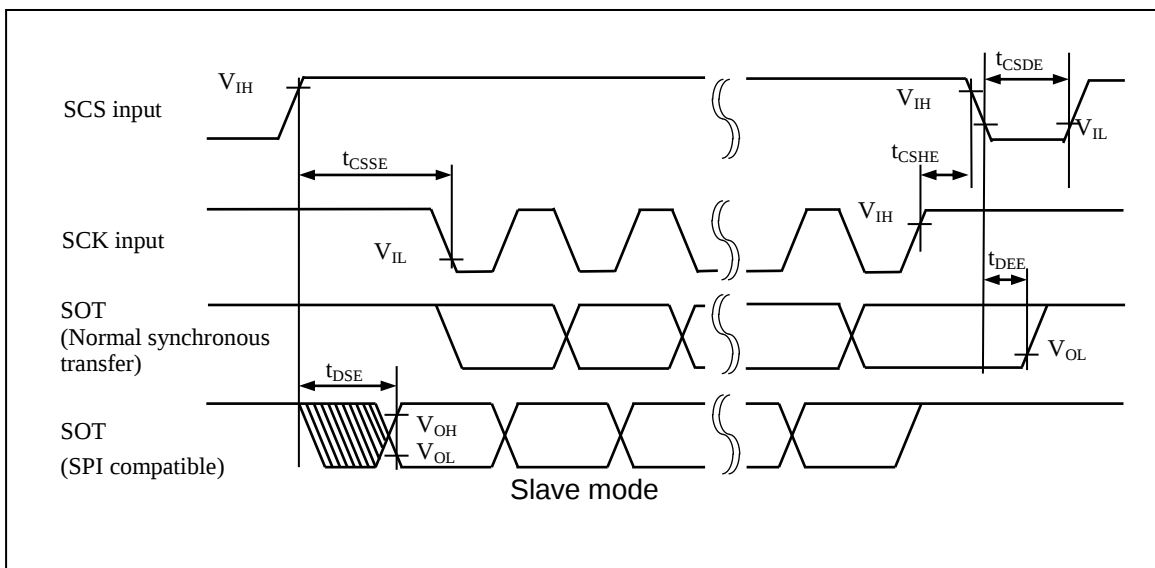
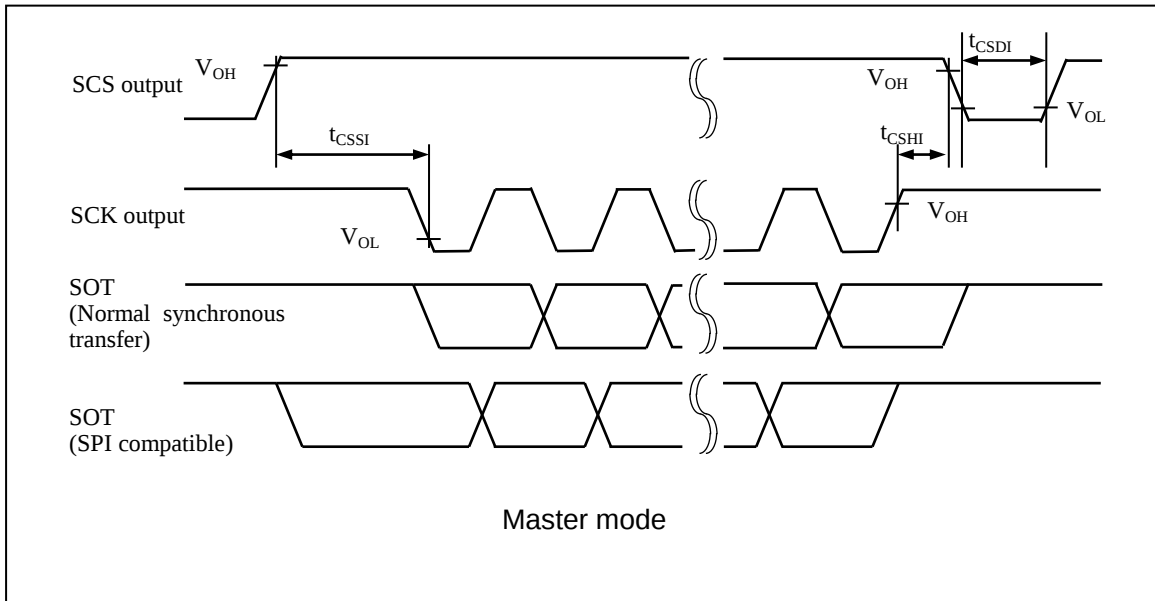
*4: t_{CLK_LCPnA} n=0:ch.0 to ch.7, n=1:ch.8 to ch.13

Notes:

■ This is the AC characteristic in CLK synchronized mode.

■ C_L is the load capacitance applied to pins during testing.

■ The maximum baud rate is limited by the internal operating clock used and other parameters.
For details, see the hardware manual



(8) Serial Chip Select Used (SCSCR:CSEN=1)

■ Serial clock output signal detect level "L" (SMR, SCSTR:SCINV=1)

■ Serial chip select inactive level "L" (SCSCR, SCSTR:CSLVL=0)

(Condition: See Recommended Operating Conditions)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
SCS ↑ → SCK ↑ setup time	t _{CSSI}	SCK0 to SCK13 SCS0x to SCS13x	Master mode (C _L =20 pF, I _{OL} =-2 mA, I _{OH} =2 mA)	t _{CSSU} ^{*1} -50	-	ns	
SCK ↓ → SCS ↓ hold time	t _{CSHI}			t _{CSHD} ^{*2} +0	-	ns	
SCS deselect time	t _{CSDI}	SCS0x to SCS13x		t _{CSDS} ^{*3} -50 +5 t _{CLK_LCPnA} ^{*4}	-	ns	
SCS ↑ → SCK ↑ setup time	t _{CSSE}	SCK0 to SCK13 SCS0x to SCS13x	Slave mode (C _L =20 pF, I _{OL} =-2 mA, I _{OH} =2 mA)	3t _{CLK_LCPnA} ^{*4} +3 0	-	ns	
SCK ↓ → SCS ↓ hold time	t _{CSHE}	SCK0 to SCK13 SCS0x to SCS13x		0	-	ns	
SCS deselect time	t _{CSDE}	SCS0x to SCS13x		3t _{CLK_LCPnA} ^{*4} +3 0	-	ns	
SCS ↑ → SOT delay time	t _{DSE}	SCS0x to SCS13x SOT0 to SOT13		-	40	ns	
SCS ↓ → SOT delay time	t _{DEE}			0	-	ns	
SCK ↑ → SCS ↑ clock switching time	t _{SCC}	SCK0 to SCK13 SCS0x to SCS13x	Master mode round operation (C _L =20 pF, I _{OL} =-2 mA, I _{OH} =2 mA)	3t _{CLK_LCPnA} ^{*4} +0	3t _{CLK_LCPnA} ^{*4} +50	ns	

*1: $t_{CSSU}=SCSTR:CSSU[7:0]$ x serial chip select timing operating clock

*2: $t_{CSHD}=SCSTR:CSHD[7:0]$ x serial chip select timing operating clock

*3: $t_{CSDS}=SCSTR:CSDS[15:0]$ x serial chip select timing operating clock. For details on *1, *2, and *3 above, see the hardware manual.

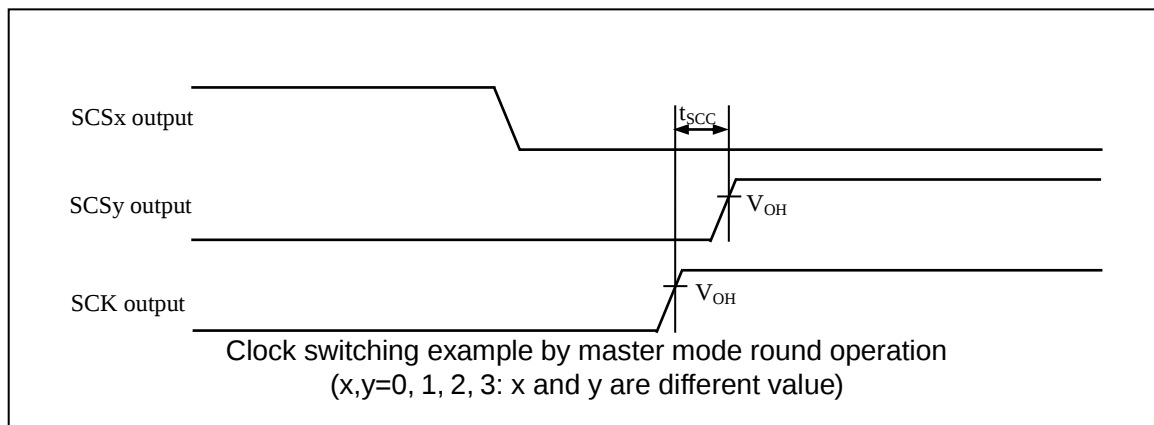
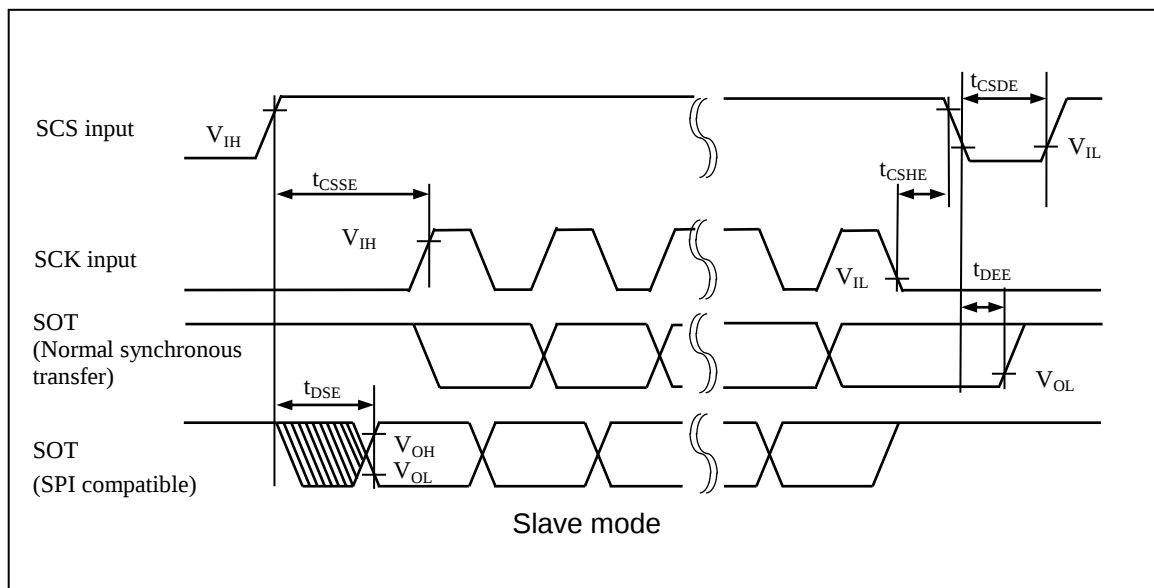
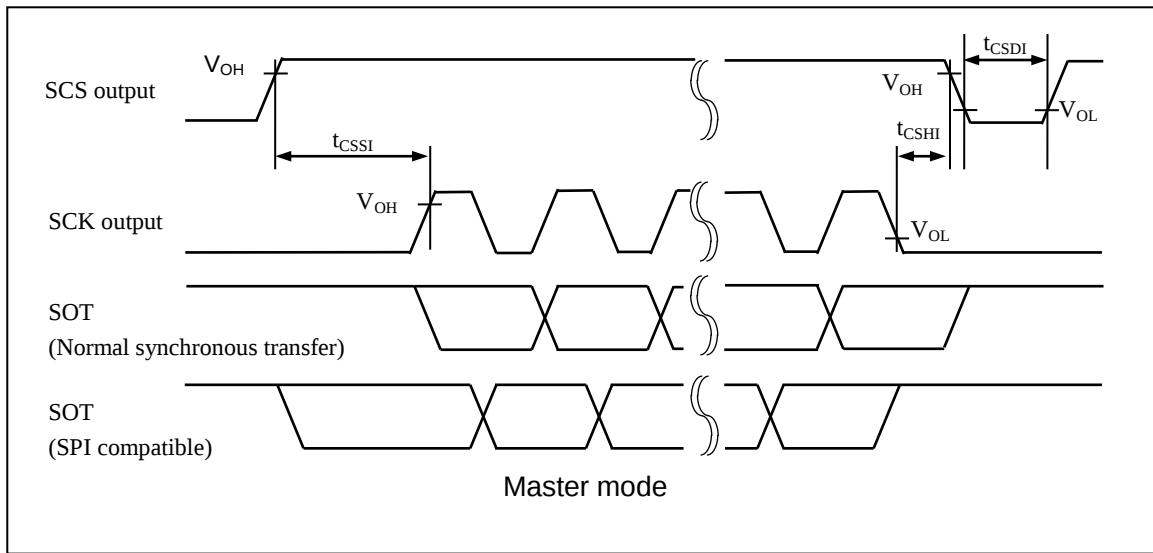
*4: t_{CLK_LCPnA} n=0:ch.0 to ch.7, n=1:ch.8 to ch.13

Notes:

■ This is the AC characteristic in CLK synchronized mode.

■ C_L is the load capacitance applied to pins during testing.

■ The maximum baud rate is limited by the internal operating clock used and other parameters. For details, see the hardware manual.



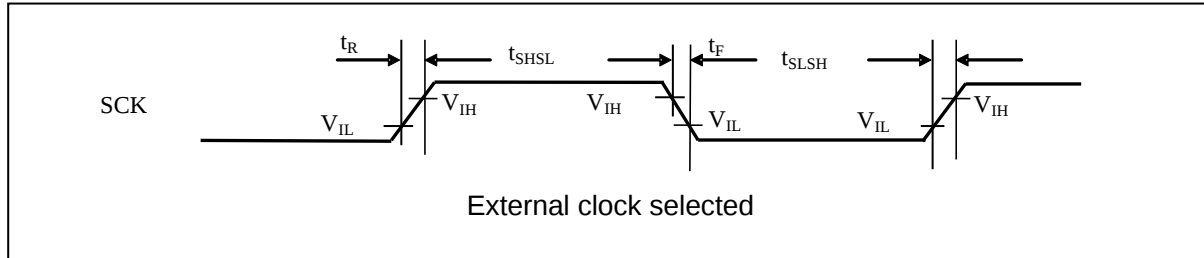
7.4.6.3 LIN Interface (v2.1) (LIN communication control interface (v2.1)) Timing (SMR:MD2-0=0b011)

External Clock Selected (BGR:EXT=1)

(Condition: See Recommended Operating Conditions)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock "L" pulse width	t _{SLSH}	SCK0 to SCK13	-	t _{CLK_LCPnA} ^{*1} +10	-	ns	
Serial clock "H" pulse width	t _{SHSL}	SCK0 to SCK13		t _{CLK_LCPnA} ^{*1} +10	-	ns	
SCK falling time	t _F	SCK0 to SCK13		-	5	ns	
SCK rising time	t _R			-	5	ns	

*1: n=0:ch.0 to ch.7, n=1:ch.8 to ch.13



7.4.6.4 I²C Timing (SMR:MD2-0=0b100)

(Condition: See Recommended Operating Conditions)

Parameter	Symbol	Pin Name	Conditions	Standard Mode		Fast Mode		Unit	Remarks
				Min	Max	Min	Max		
SCL clock frequency	f _{SCL}	SCL0 to SCL13	C _L =50 pF, R=(V _p /I _{OL}) ^{*1}	0	100	0	400	kHz	
Repeat "start" condition hold time SDA ↓ → SCL ↓	t _{HDSTA}	SDA0 to SDA13 SCL0 to SCL13		4.0	-	0.6	-	μs	
Period of "L" for SCL clock	t _{LOW}	SCL0 to SCL13		4.7	-	1.3	-	μs	
Period of "H" for SCL clock	t _{HIGH}			4.0	-	0.6	-	μs	
Repeat "start" condition setup time SCL ↑ → SDA ↓	t _{SUSTA}	SDA0 to SDA13 SCL0 to SCL13		4.7	-	0.6	-	μs	
Data hold time SCL ↓ → SDA ↓ ↑	t _{HDDAT}			0	3.45 ^{*2}	0	0.9 ^{*3}	μs	
Data setup time SDA ↓ ↑ → SCL ↑	t _{SUDAT}			250	-	100	-	ns	
"Stop" condition setup time SCL ↑ → SDA ↑	t _{SUSTO}			4.0	-	0.6	-	μs	
Bus-free time between "stop" condition and "start" condition	t _{BUF}	-		4.7	-	1.3	-	μs	
Noise filter	t _{SP}	-		t _{NFT} ^{*4}	-	t _{NFT} ^{*4}	-	ns	

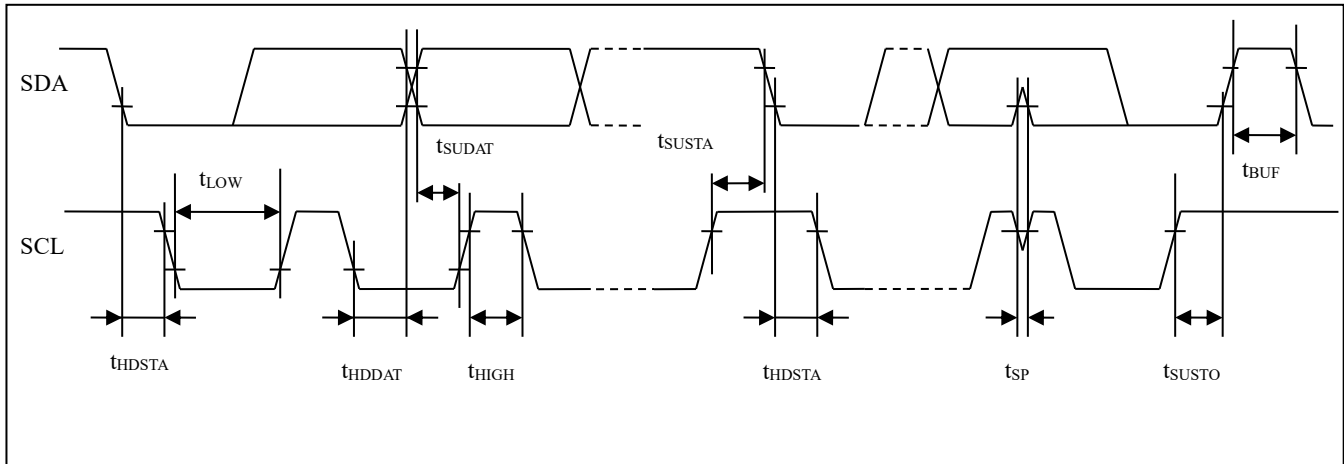
Note: There is standard mode/fast mode correspondence only ch.3 and ch.5. In ch.0 to ch.2, ch.4, and ch.6 to ch.13, the only correspondence is standard mode.

*1: R and C_L represent the pull-up resistance and load capacitance of the SCL and SDA output lines, respectively.
V_p shows the power-supply voltage of the pull-up resistor and I_{OL} shows the V_{OL} guarantee current.

*2: The maximum t_{HDDAT} must only be met if the device does not extend the "L" width (t_{LOW}) of the SCL signal.

*3: A fast mode I²C bus device can be used on a standard mode I²C bus system as long as the device satisfies the requirement of "t_{SUDAT} ≥ 250 ns".

*4: t_{NFT} = (NFCR:NFT[4:0] + 1) × 2 × t_{CLK_LCP0A} (ch.0 to ch.7)
t_{NFT} = (NFCR:NFT[4:0] + 1) × 2 × t_{CLK_LCP1A} (ch.8 to ch.13)

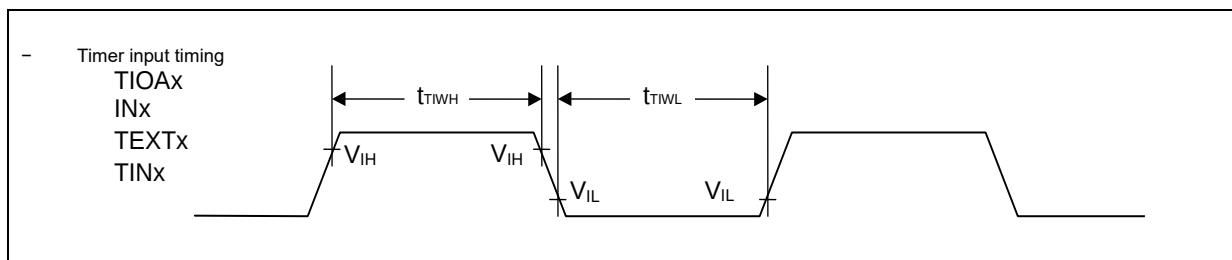


7.4.7 Timer Input

(Condition: See Recommended Operating Conditions)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TWH} , t_{TWL}	TIOA0 to TIOA63	-	$4t_{CLK_LCP1A}$	-	ns	$4t_{CLK_LCP1A} \geq 100$ ns
				100			$4t_{CLK_LCP1A} < 100$ ns
		ICU0_IN0 to ICU5_IN0 , ICU0_IN1 to ICU5_IN1 , ICU16_IN0 to ICU21_IN0 , ICU16_IN1 to ICU21_IN1	-	$4t_{CLK_LCP0A}$	-	ns	$4t_{CLK_LCP0A} \geq 100$ ns
				100			$4t_{CLK_LCP0A} < 100$ ns
		TEXT0 to TEXT7	-	$4t_{CLK_LCP0A}$	-	ns	$4t_{CLK_LCP0A} \geq 100$ ns
				100			$4t_{CLK_LCP0A} < 100$ ns
		TIN0 to TIN3 , TIN16 to TIN17	-	$4t_{CLK_LCPnA}^{*1}$	-	ns	$4t_{CLK_LCPnA}^{*1} \geq 100$ ns
				100			$4t_{CLK_LCPnA}^{*1} < 100$ ns

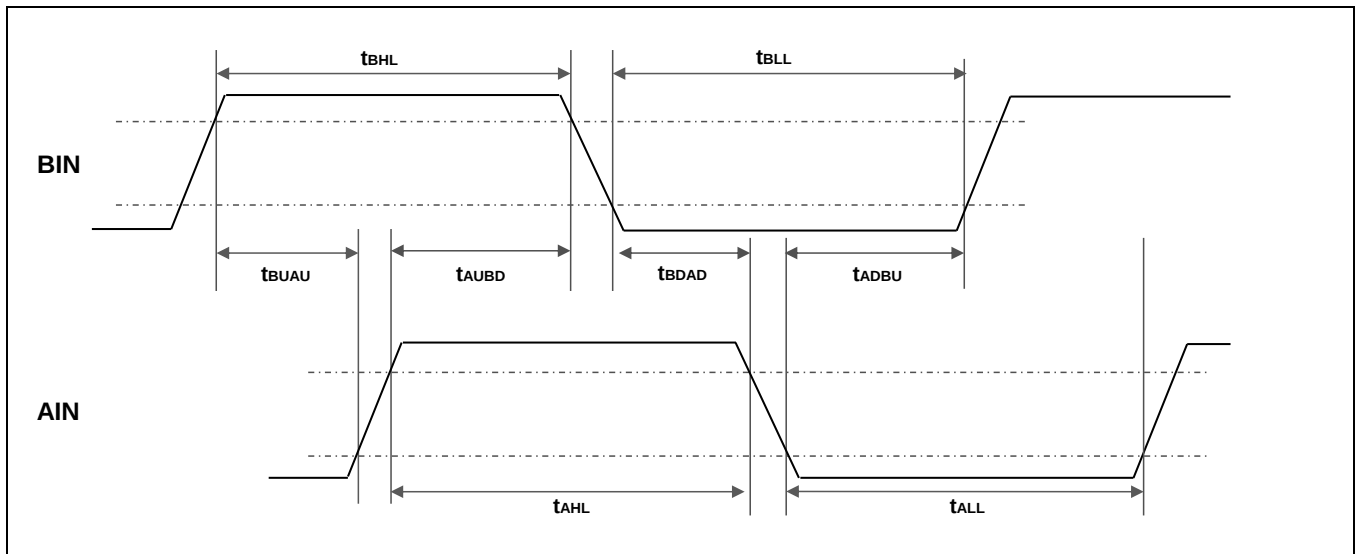
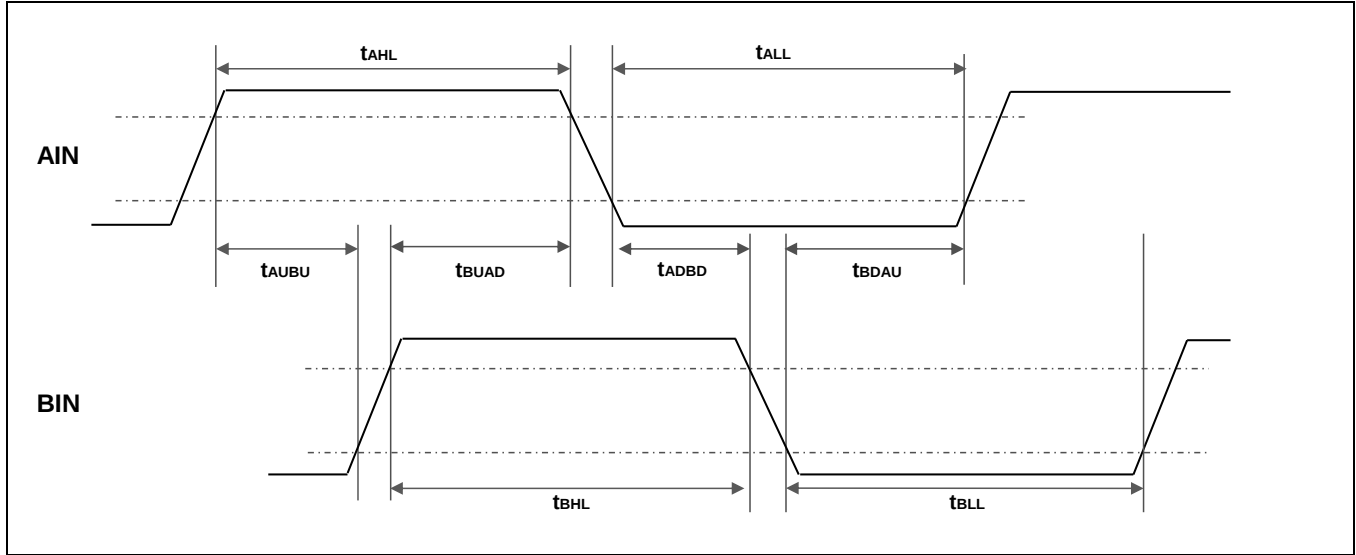
*1: n=0:ch.0 to ch.3, n=1:ch.16 to ch.17

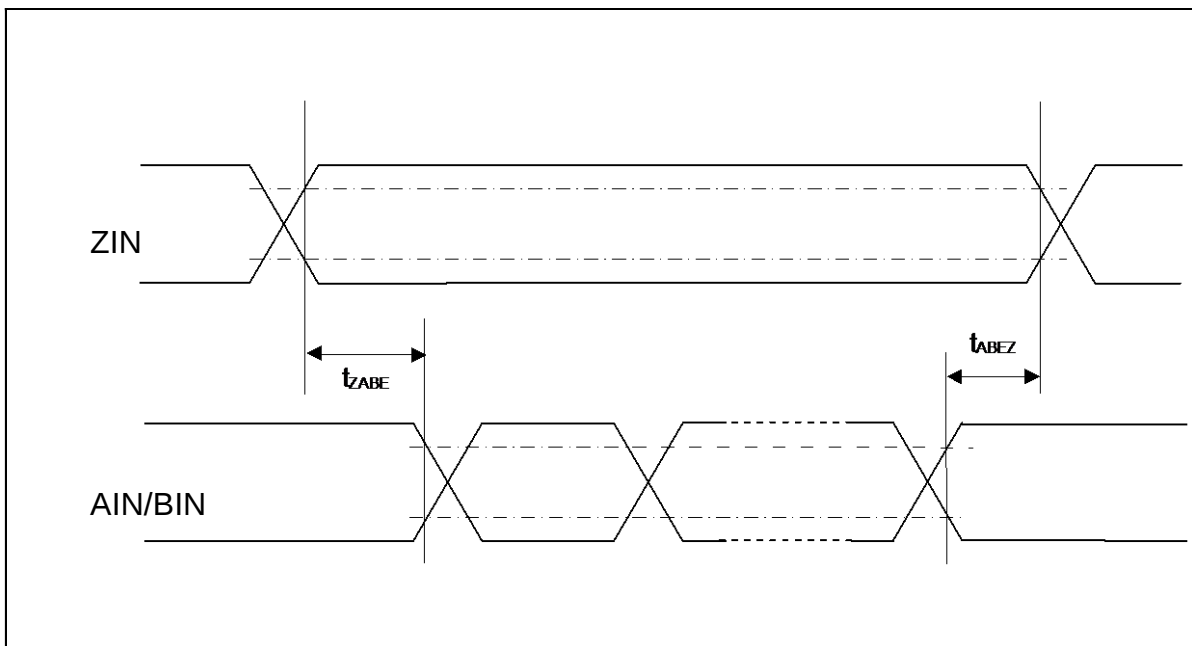
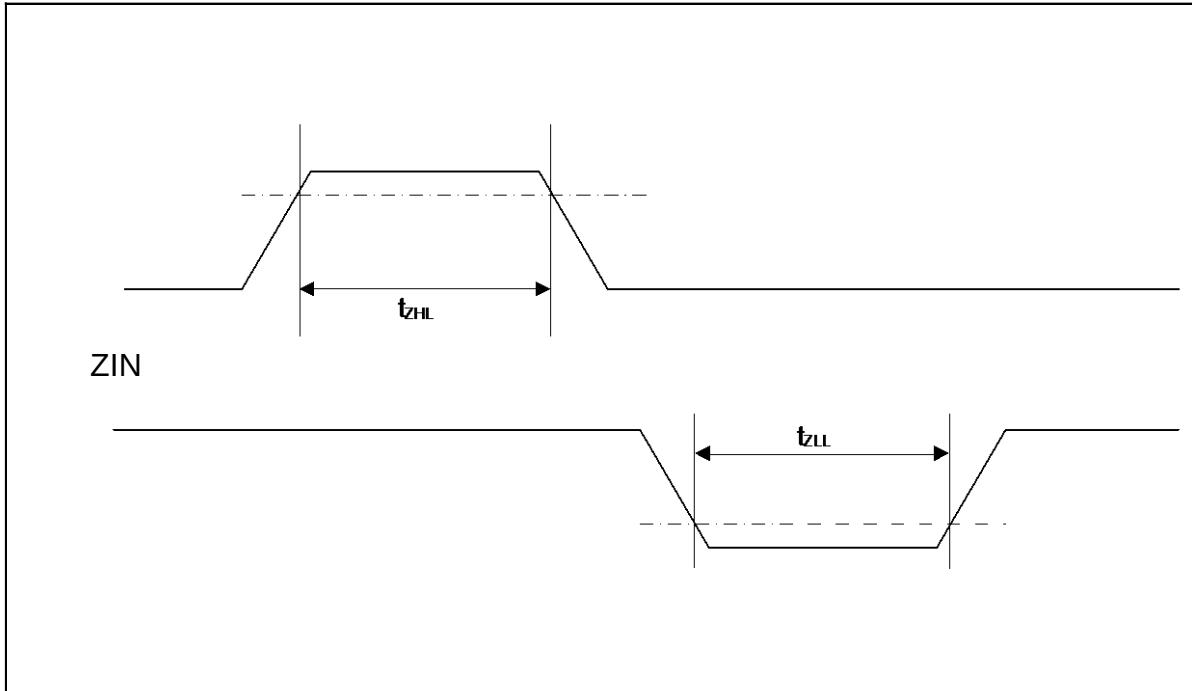


7.4.8 QPRC Timing

(Condition: See Recommended Operating Conditions)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
AIN pin "H" width	t_{AHL}	AIN8 to AIN9	-	4t _{CLK_LCP0A}	-	ns	4t _{CLK_LCP0A} ≥ 100 ns
AIN pin "L" width	t_{ALL}	AIN8 to AIN9	-				
BIN pin "H" width	t_{BHL}	BIN8 to BIN9	-				
BIN pin "L" width	t_{BLL}	BIN8 to BIN9	-				
Time from AIN pin "H" level to BIN rise	t_{AUBU}	AIN8 to AIN9, BIN8 to BIN9	PC_Mode2 or PC_Mode3				
Time from BIN pin "H" level to AIN fall	t_{BUAD}	AIN8 to AIN9, BIN8 to BIN9	PC_Mode2 or PC_Mode3				
Time from AIN pin "L" level to BIN fall	t_{ADBD}	AIN8 to AIN9, BIN8 to BIN9	PC_Mode2 or PC_Mode3				
Time from BIN pin "L" level to AIN rise	t_{BDAU}	AIN8 to AIN9, BIN8 to BIN9	PC_Mode2 or PC_Mode3				
Time from BIN pin "H" level to AIN rise	t_{BUAU}	AIN8 to AIN9, BIN8 to BIN9	PC_Mode2 or PC_Mode3				
Time from AIN pin "H" level to BIN fall	t_{AUBD}	AIN8 to AIN9, BIN8 to BIN9	PC_Mode2 or PC_Mode3				
Time from BIN pin "L" level to AIN fall	t_{BDAD}	AIN8 to AIN9, BIN8 to BIN9	PC_Mode2 or PC_Mode3				
Time from AIN pin "L" level to BIN rise	t_{ADBU}	AIN8 to AIN9, BIN8 to BIN9	PC_Mode2 or PC_Mode3				
ZIN pin "H" width	t_{ZHL}	ZIN8 to ZIN9	QCR:CGSC="0"				
ZIN pin "L" width	t_{ZLL}	ZIN8 to ZIN9	QCR:CGSC="0"				
Time from determined ZIN level to AIN/BIN rise and fall	t_{ZABE}	AIN8 to AIN9, BIN8 to BIN9, ZIN8 to ZIN9	QCR:CGSC="1"				
Time from AIN/BIN rise and fall time to determined ZIN level	t_{ABEZ}	AIN8 to AIN9, BIN8 to BIN9, ZIN8 to ZIN9	QCR:CGSC="1"				

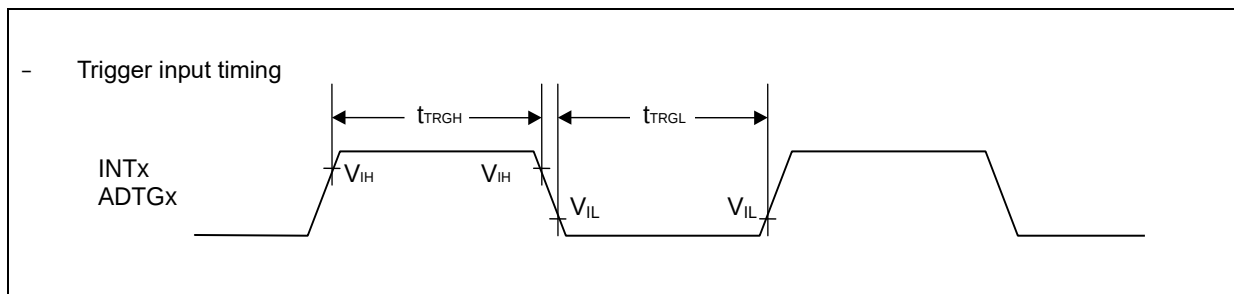




7.4.9 Trigger Input

(Condition: See Recommended Operating Conditions)

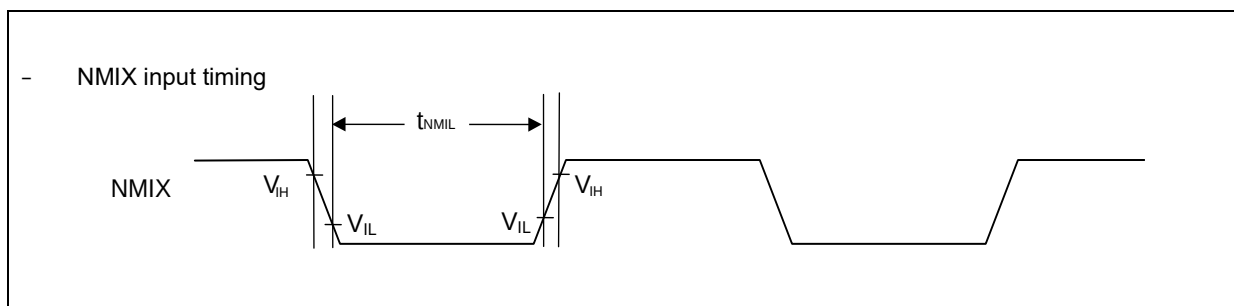
Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TRGH} , t_{TRGL}	INT0 to INT31	-	100	-	ns	
		ADTG0 to ADTG1	-	$5t_{CLK_LCP1A}$	-	ns	$5t_{CLK_LCP1A} \geq 100$ ns
				100			$5t_{CLK_LCP1A} < 100$ ns
		INT0 to INT31	-	1	-	μs	Stop mode



7.4.10 NMI Input

(Condition: See Recommended Operating Conditions)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{NMIL}	NMIX	-	300	-	ns	



7.4.11 Low Voltage Detection (External Voltage)

(Condition: See Recommended Operating Conditions)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Supply voltage range	V _{DP5}	VCC	-	2.4	-	5.5	V	
Detection voltage	V _{DLAT}	VCC	*1	2.5	2.6	2.7	V	When power-supply voltage falls and detection level is set initially *3 Typ ± 3.5%
Hysteresis width	V _{HYS}	VCC	-	-	100	-	mV	When power-supply voltage rises
Low-voltage detection time	t _d	-	-	-	-	40	μs	
Power supply voltage regulation	-	VCC	-	-2	-	2	V/ms	*2

*1: If the power supply fluctuation is faster than the low-voltage detection time, it is possible to generate or release after the power supply voltage has exceeded the detection voltage range.

*2: For low-voltage detection by VDL, suppress the power supply to be within the range of the power-supply voltage regulation.

*3: This LVD setting cannot be used to reliably generate a reset before voltage dips below minimum guaranteed MCU operation voltage, as these detection levels are below the minimum guaranteed MCU operation voltage (2.7 V).

7.4.12 Low-Voltage Detection (Internal Voltage)

7.4.12.1 Low-voltage Detection (RAM retention low-voltage detection for LVDL0)

(Condition: See Recommended Operating Conditions)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Supply voltage range	V _{RDP5}	-	-	0.6	-	1.21	V	
Detection voltage	V _{RDL}	-	*1	0.75	0.85	0.95	V	When power-supply voltage falls*2
Hysteresis width	V _{RHYS}	-	-	-	75	-	mV	When power-supply voltage rises
Low-voltage detection time	t _{Rd}	-	-	-	-	30	μs	

*1: If the power fluctuation time is less than the low-voltage detection time (TRd) and has passed the detection voltage range, the detection may occur or be cancelled after the supply voltage passes the detection voltage range.

*2: This LVD setting cannot be used to reliably generate a reset before voltage dips below minimum guaranteed MCU operation voltage, as this detection level is below the minimum guaranteed MCU operation voltage.

7.4.12.2 Low-voltage Detection (internal low-voltage detection for LVDL1)

(Condition: See Recommended Operating Conditions)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Supply voltage range	V _{RDP5}	-	-	0.6	-	1.21	V	
Detection voltage	V _{RDLAT}	-	*1	0.844	0.875	0.906	V	When power-supply voltage falls and detection level is set initially *2 Typ±3.5%
Hysteresis width	V _{RHYS}	-	-	-	75	-	mV	When power-supply voltage rises
Low-voltage detection time	t _{Rd}	-	-	-	-	30	μs	

*1: If the power fluctuation time is less than the low-voltage detection time (TRd) and has passed the detection voltage range, the detection may occur or be cancelled after the supply voltage passes the detection voltage range.

*2: This LVD setting cannot be used to reliably generate a reset before voltage dips below minimum guaranteed MCU operation voltage, as this detection level is below the minimum guaranteed MCU operation voltage.

7.4.13 Port Noise Filter

(Condition: See Recommended Operating Conditions)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Width for input removal	-	ALL GPIO	-	-	100	ns	*1

*1: Input pulse width less than at least Typ 25 ns to Max 100 ns is removed when the port noise filter is enabled.

7.4.14 Clock Monitor

(Condition: See Recommended Operating Conditions)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Clock Monitor frequency	-	CLK_CLKO	-	-	10	MHz	

7.5 A/D Converter

7.5.1 Electrical Characteristics

(T_A: Recommended operating conditions, V_{CC} = AV_{CC} = 5.0 V ± 0.5 V, V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin Name	Conditions			Unit	Remarks
			Min	Typ	Max		
Resolution	-	-	-	-	12	bit	
Total error	-	-	-	-	±6	LSB	*3
	-	-	-	-	±12	LSB	*4
Integral nonlinearity	-	-	-	-	±4.0	LSB	*5
Differential nonlinearity	-	-	-	-	±1.9	LSB	*5
Zero transition voltage	V _{ZT}	AN000 to AN031, AN100 to AN131	AVRL -11.5LSB	-	AVRL +12.5LSB	V	*4
Full-scale transition voltage	V _{FST}	AN000 to AN031, AN100 to AN131	AVRH -13.5LSB	-	AVRH +10.5LSB	V	
Sampling time	t _{SMP}	-	0.3	-	-	μs	*1
Compare time	t _{CMP}	-	0.7	-	26	μs	*1
A/D conversion time	t _{CNV}	-	1.0	-	-	μs	*1
Resumption time	-	-	-	-	1	μs	
Analog port input current	I _{AIN}	AN000 to AN031, AN100 to AN131	-1.0	-	1.0	μA	AV _{SS} ≤ V _{AIN} ≤ AV _{CC}
Analog input voltage	V _{AIN}	AN000 to AN031, AN100 to AN131	AVRL	-	AVRH	V	
Reference voltage	AVRH	AVRH0, AVRH1	4.5	-	5.5	V	AV _{CC} ≥ AVRH
	AVRL	AVRL0/AVSS0, AVRL1/AVSS1	-	0.0	-	V	
Power supply current	I _A	AVCC0, AVCC1	-	600	700	μA	Per unit
	I _{AH}		-	1.0	100	μA	Per unit *2
	I _R	AVRH0, AVRH1	-	0.7	1.95	mA	Per unit
	I _{RH}		-	-	5.0	μA	Per unit *2
Variation between channels	-	AN000 to AN031, AN100 to AN131	-	-	4.0	LSB	Per unit

(TA: Recommended operating conditions, $V_{CC} = AV_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$, $V_{SS} = AV_{SS} = 0.0 \text{ V}$)

Parameter	Symbol	Pin Name	Conditions			Unit	Remarks
			Min	Typ	Max		
Resolution	-	-	-	-	12	bit	
Total error	-	-	-	-	± 6	LSB	*3
Integral nonlinearity	-	-	-	-	± 4.0	LSB	*5
Differential nonlinearity	-	-	-	-	± 1.9	LSB	*5
Zero transition voltage	V_{ZT}	AN000 to AN031, AN100 to AN131	AVRL -14.5LSB	-	AVRL +15.5LSB	V	*4
Full-scale transition voltage	V_{FST}	AN000 to AN031, AN100 to AN131	AVRH -16.5LSB	-	AVRH +13.5LSB	V	
Sampling time	t_{SMP}	-	0.5	-	-	μs	*1
Compare time	t_{CMP}	-	1.4	-	26	μs	*1
A/D conversion time	t_{CNV}	-	1.9	-	-	μs	*1
Resumption time	-	-	-	-	1	μs	
Analog port input current	I_{AIN}	AN000 to AN031, AN100 to AN131	-1.0	-	1.0	μA	$AV_{SS} \leq V_{AIN} \leq AV_{CC}$
Analog input voltage	V_{AIN}	AN000 to AN031, AN100 to AN131	AVRL	-	AVRH	V	
Reference voltage	AVRH	AVRH0, AVRH1	3.0	-	3.6	V	$AV_{CC} \geq AVRH$
	AVRL	AVRL0/AVSS0, AVRL1/AVSS1	-	0.0	-	V	
Power supply current	I_A	AVCC0, AVCC1	-	600	700	μA	Per unit
	I_{AH}		-	1.0	100	μA	Per unit *2
	I_R	AVRH0, AVRH1	-	0.5	1.3	mA	Per unit
	I_{RH}		-	-	7.0	μA	Per unit *2
Variation between channels	-	AN000 to AN031, AN100 to AN131	-	-	4.0	LSB	Per unit

*1: Time per channel

 *2: Definition of the power supply current (when $V_{CC} = AV_{CC} = 5.0 \text{ V}$) while the A/D converter is not operating and in stop mode

 *3: Total error is a comprehensive static error that includes the linearity after trimming by software. $1 \text{ LSB} = (AVRH - AVRL) / 4096$

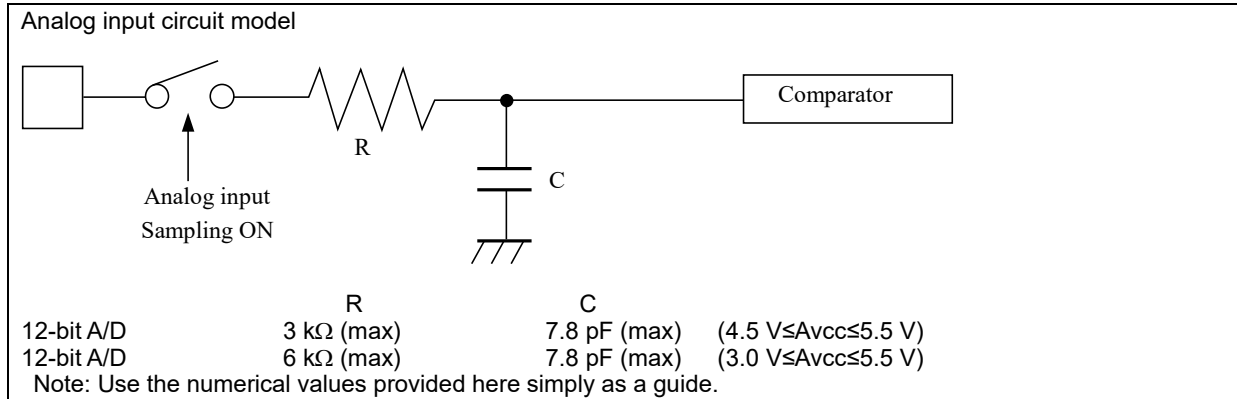
 *4: $1 \text{ LSB} = (AVRH - AVRL) / 4096$

 *5: $1 \text{ LSB} = (VFST - VZT) / 4094$

7.5.2 Notes on A/D Converters

Output Impedance of an External Circuit for Analog Input

When the external impedance is too high, the analog voltage sampling time may become insufficient. In this case, we recommend attaching a capacitor (about 0.1 μF) to an analog input pin.



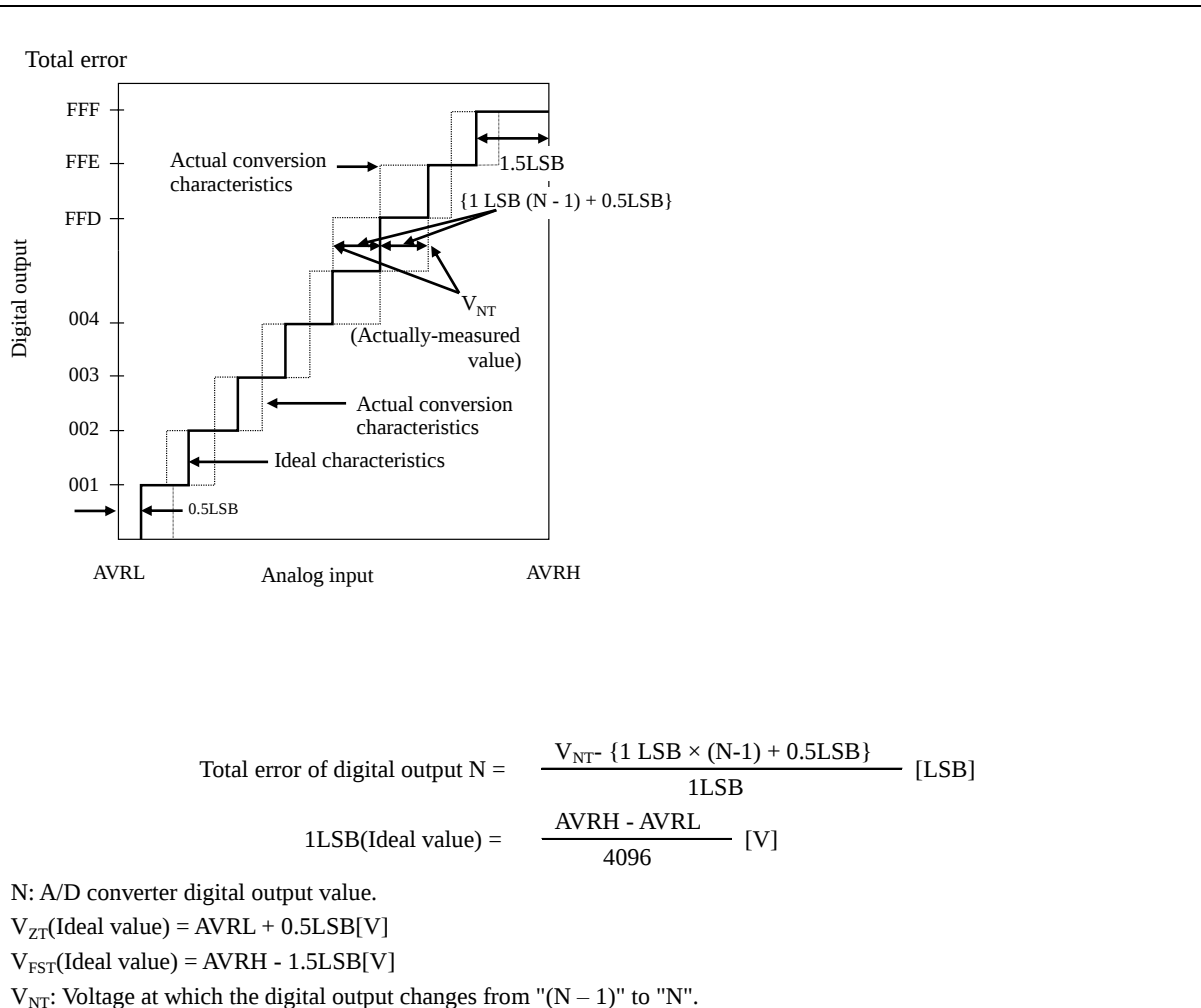
7.5.3 Glossary

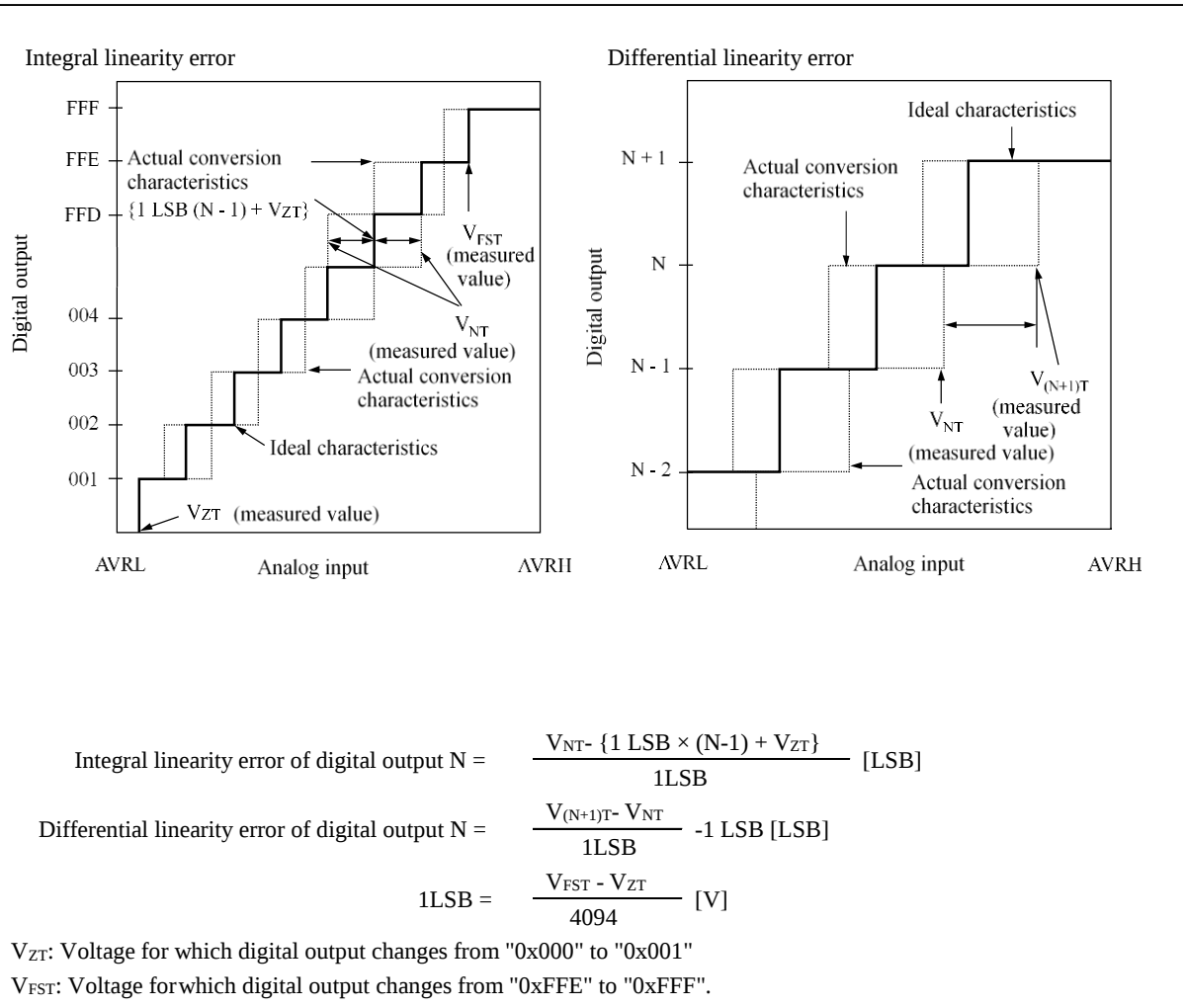
Resolution: Analog change that can be identified by an A/D converter.

Integral linearity error: Deviation of the straight line connecting the zero transition point ("0000 0000 0000" ↔ "0000 0000 0001") and full-scale transition point ("1111 1111 1110" ↔ "1111 1111 1111") from actual conversion characteristics includes zero transition error, full-scale transition error, and nonlinearity error.

Differential linearity error: Deviation from the ideal value of the input voltage required for changing the output code by 1 LSB.

Total error: Difference between the actual value and the theoretical value.





7.6 Flash Memory

7.6.1 Electrical Characteristics

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Sector erase time	-	120	180	ms	Large sector* ¹ Internal preprogramming time included
	-	120	180	ms	8-kB sector* ¹ Internal preprogramming time included
	-	120	180	ms	4-kB sector* ² Internal preprogramming time included
32-bit write time(Program)	-	30	60	μs	System-level overhead time excluded* ¹
64-bit write time(Program)	-	30	60	μs	System-level overhead time excluded* ¹
256-bit write time(Program)	-	40	70	μs	System-level overhead time excluded* ¹
32-bit write time(Work)	-	30	60	μs	System-level overhead time excluded* ²
Erase count / Data retention time (Program)	1,000/20 years	-	-	-	Temperature at write/erase time Average temperature T _A = +85 degrees Celsius
Erase count / Data retention time (Work)	1,000/20 years 10,000/10 years 100,000/5 years	-	-	-	Temperature at write/erase time Average temperature T _A = +85 degrees Celsius

*1: Guaranteed value for up to 1,000 erases

*2: Guaranteed value for up to 100,000 erases

7.6.2 Notes

While the Flash memory is written or erased, shutdown of the external power (V_{CC}) is prohibited.

In application systems where V_{CC} may be shut down while writing or erasing, be sure to turn the power off by using an external voltage detection function.

In other words, after the external power supply voltage falls below the detection voltage (V_{DL}), hold V_{CC} at 2.7 V or more within the duration calculated by the following expression:

$$T_d^{*1} [\mu s] + (1 / F_{CRF}^{*2} [MHz]) \times 1029 + 25 [\mu s]$$

*1: See Low Voltage Detection (External Voltage)

*2: See Source Clock Timing

8. Ordering Information

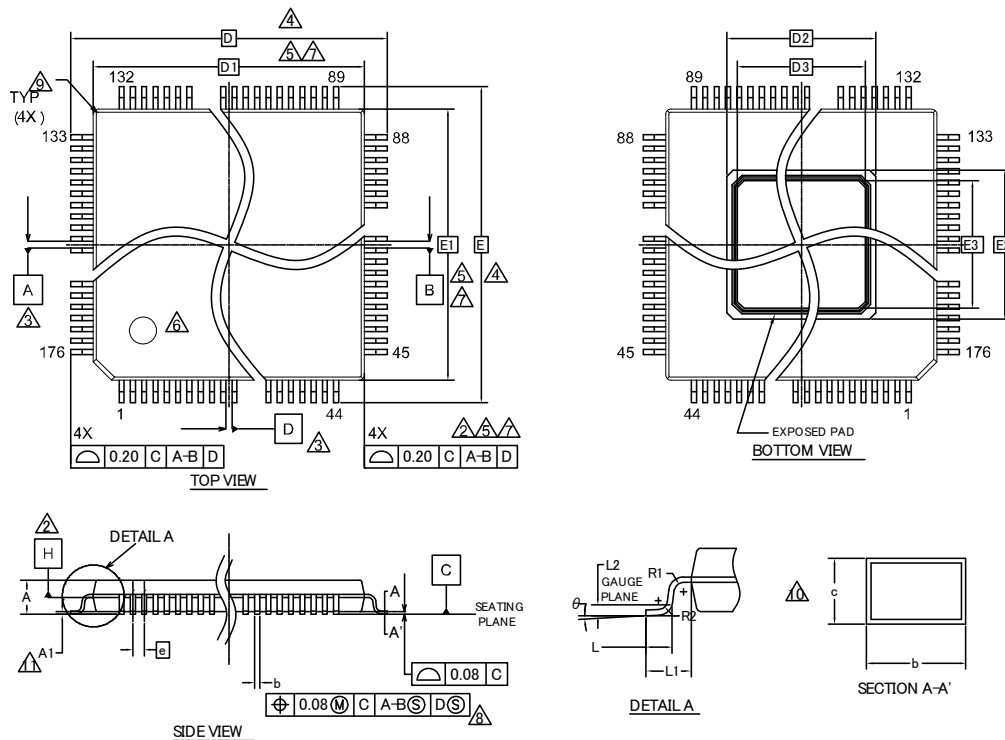
Part Number	Package
S6J342AFSBSV20000	LQI100 (100-pin 0.5-mm pitch Plastic LQFP)
S6J342AFTBSV20000	
S6J342AFUBSV20000	
S6J3428FVBSV20000	
S6J342AHSBSV20000	LQS144 (144-pin 0.5-mm pitch Plastic LQFP)
S6J342AHTBSV20000	
S6J342AHUBSV20000	
S6J342AHVBSV20000	
S6J3429HUBSV20000	
S6J3429HVBSV20000	
S6J342AJSBSE20000	LEH176 (176-pin 0.5-mm pitch Plastic TEQFP)
S6J342AJTBSE20000	

9. Package Dimensions

9.1 TEQFP-176

LEH176, 176 Lead Plastic Low Profile Quad Flat Package

Package Type	Package Code
TEQFP 176pin	LEH176



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.05	—	0.15
D	26.00 BSC		
D1	24.00 BSC		
D2	5.00 REF		
D3	3.80 REF		
E	26.00 BSC		
E1	24.00 BSC		
E2	5.00 REF		
E3	3.80 REF		
R1	0.08	—	—
R2	0.08	—	0.20
θ	0°	4°	8°
c	0.09	—	0.20
b	0.17	0.22	0.27
L	0.45	0.60	0.75
L1	1.00 REF		
L2	0.25		
e	0.50 BSC		

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.

△ DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.

△ DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.

△ TO BE DETERMINED AT SEATING PLANE C.

△ DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION.

ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.

△ DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.

△ REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS, DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS, BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.

△ DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBER PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBER CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.

△ EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.

△ THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.

△ A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

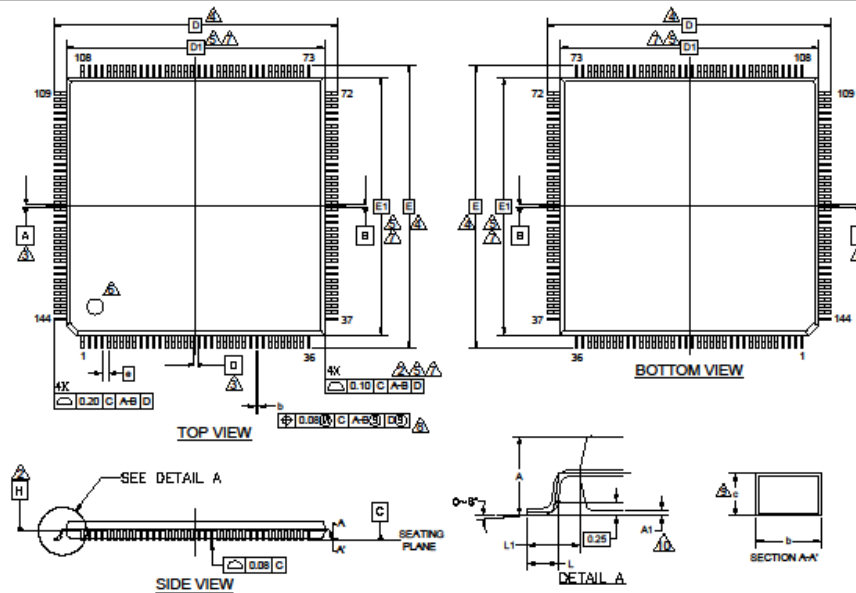
002-13037 **

PACKAGE OUTLINE, 176 LEAD TEQFP
24.0X24.0X1.7 MM LEH176 Rev**

9.2 LQFP-144

LQS144, 144 Lead Plastic Low Profile Quad Flat Package

Package Type	Package Code
LQFP 144pin	LQS144



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.05	—	0.15
b	0.17	0.22	0.27
c	0.09	—	0.20
D	22.00 BSC		
D1	20.00 BSC		
e	0.50 BSC		
E	22.00 BSC		
E1	20.00 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		

NOTES

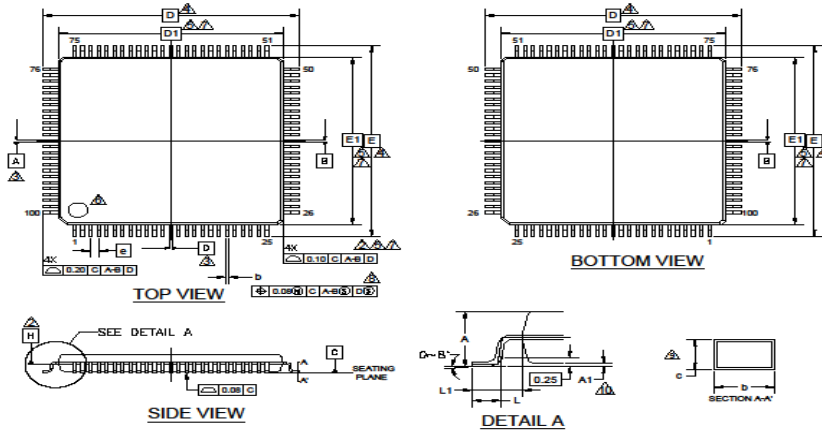
- ALL DIMENSIONS ARE IN MILLIMETERS
- DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
- DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
- TO BE DETERMINED AT SEATING PLANE C.
- DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE.
- DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
- DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
- REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS, DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS, BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
- DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
- THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
- A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-13015 *B

9.3 LQFP-100

LQI100, 100 Lead Plastic Low Profile Quad Flat Package

Package Type	Package Code
LQFP 100pin	LQI100



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.05	—	0.15
b	0.15	—	0.27
c	0.09	—	0.20
D	16.00	BSC	—
D1	14.00	BSC	—
e	0.50	BSC	—
E	16.00	BSC	—
E1	14.00	BSC	—
L	0.45	0.60	0.75
L1	—	1.00	REF

- NOTES :
- ALL DIMENSIONS ARE IN MILLIMETERS.
 - DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
 - DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
 - TO BE DETERMINED AT SEATING PLANE C.
 - DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALL ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
 - DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
 - REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS, DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS, BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
 - DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.05mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
 - THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
 - A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-11500 *B

10. Acronyms

Acronym	Definition
A/D converter	Analog digital converter
ADC	Analog-to-digital converter
AHB	Advanced high-performance bus
AMBATM	Advanced microcontroller bus architecture
APB	Advanced peripheral bus
ATCM	TCM-A port
AXI	Advanced extensible interface
B0TCM	TCM B0 port
B1TCM	TCM B1 port
BBU	Bit banding unit
BDR	Boot description record
CAN	Controller area network
CD	Clock domain
CPU	Central processing unit
CR	CR oscillator
CRC	Cyclic redundancy check
CSV	Clock supervisor
DAP	Debug access port
DED	Dual error detection
DMA	Direct memory access
DMAC	DMA controller
ECC	Error correction code
ETM	Embedded trace macro
EXT-IRC	External interrupt controller
FIQ	Fast interrupt request
FPU	Floating point unit
FRT	Free-run timer
GPIO	General-purpose I/O
HPM	High-performance matrix
HW-WDT	Hardware watchdog timer
I/O	Input or output
ICU	Input capture unit
IPCU	Inter-processor communication unit
IRC	Interrupt controller
IRQ	Interrupt request
ISR	Interrupt service routine
JTAG	Joint Test Action Group

Acronym	Definition
LLPP	Low-latency peripheral port
LVD	Low-voltage detector
MCU	Microcontroller unit
MFS	Multi-function serial interface
NF	Noise filter
NMI	Non-maskable interrupt
OCU	Output compare unit
OSC	Oscillator
PLL	Phase-locked loop
PONR	Power-on reset
PPC	Port pin configuration
PSS	Power saving state
PWM	Pulse width modulation
RAM	Random access memory
RIC	Resource input configuration
ROM	Read-only memory
RTC	Real-time clock
RVD	Low-voltage detection and reset for RAM retention
RMW	Read modify write
SCT	Source clock timer
SEC	Single error correction
SECDED	Single error correction and dual error detection
SHE	Secure Hardware Extension
SRAM	Static RAM
SW-WDT	Software watchdog timer
SYSC	System controller
TCFLASH	Flash connected to TCM
TCM	Tightly coupled memory
TCRAM	RAM connected to TCM
TPU	Timing protection unit
UDC	Up-down counter
VIC	Vectored interrupt controller
WDR	Watchdog description record
WDT	Watchdog timer
WorkFLASH	Work Flash memory

11. Errata

This section describes the errata for the S6J3400 Series. Details include errata trigger conditions, scope of impact, available workarounds, and silicon revision applicability. Contact your local Cypress Sales Representative if you have questions.

Part Numbers Affected

Part Number
S6J3428xxx
S6J3429xxx
S6J342Axxx

S6J3428/9/A Qualification Status

Product Status: Production

Errata Summary

The following table defines the errata applicability to available S6J3400 Series devices.

Items	Part Number	Fix Status
1. MCAN wrong message transmission	S6J3428xxx S6J3429xxx S6J342Axxx	No silicon fix planned.
2. CAN FD controller message order inversion when transmitting from dedicated Tx Buffers configured with same Message ID		
3. CAN FD incomplete description of Dedicated Tx Buffers and Tx Queue related to transmission from multiple buffers configured with the same Message ID		

1. MCAN wrong message transmission

■ Problem Definition

There is a possibility a message with an ID (arbitration field) and a format and DLC (control field) is transmitted which was not configured by the application. The message itself is syntactically correct and can be received by other nodes.

The occurrence of the limitation requires a certain relationship in time between a transmission request for sending a message and the coincidence of noise in the 3rd bit of intermission field which is treated as the start of new message transmission (SoF).

■ Trigger Condition

Under the following conditions a message with wrong ID, format and DLC is transmitted:

- M_CAN is in state "Receiver" (PSR.ACT = "10"), no pending transmission.
- A new transmission is requested after sample point of 2nd bit of intermission but before the 3rd bit of Intermission is reached.
- The CAN bus is sampled dominant at the third bit of Intermission which is treated as SoF (see ISO11898-1:2015 Section 10.4.2.2).

■ Scope of Impact

Under the conditions listed above it may happen, that:

- The shift register is not loaded with ID, format, and DLC of the requested message.
- The M_CAN will start arbitration with wrong ID, format, and DLC.
- In case the ID won arbitration, a CAN message with valid CRC is transmitted.
- In case this message is acknowledged, the ID stored in the Tx Event FIFO is the ID of the requested Tx message and not the ID of the message transmitted on the CAN bus
- Neither an error is detected by the transmitting node nor at the receiving node.

■ Workaround

Workaround 1:

This workaround avoids submitting a transmission request in the critical time window of about one bit time before the sample point of the 3rd bit of intermission field when on other pending transmission request exists:

- Request a new transmission if another transmission is already pending or when the M_CAN / M_TTCAN is not in state "Receiver" (when PSR.ACT ≠ "10").
- If no pending transmission request exists, the application software needs to evaluate the Rx Interrupt flags IR.DRX, IR.RF0N, IR.RF1N which are set at the last bit of EoF when a received and accepted message gets valid.
- A new transmission may be requested by writing to TXBAR once the Rx interrupt occurred and the application waited another 3 bit times before submitting its Tx request. Note the Rx interrupt is generated at the last bit of EoF which is followed by three bits of Intermission.
- The application has to take care that the transmission request for the CAN Protocol Controller is activated before the critical window of the following reception is reached.

A supplemental action can be applied in order to detect messages which contain wrong ID and control filed information:

- A checksum covering arbitration and control fields can be added to the data field of the message to be transmitted, to detect frames transmitted with wrong arbitration and control fields.

Workaround 2:

This workaround ensures that always at least one pending Tx request exists. If that is the case, the application may launch its Tx requests at any time without suffering from the limitation.

- Define a low priority message with DLC = 0 that can be sent without harm. E.g. loses arbitration against all other application messages, does not pass any acceptance filter of nodes in the same network. DLC = 0 shall reduce latency for other application messages.
- Configure sufficient Tx buffers – at least two - for this message type thus that there is always another one waiting to be sent. E.g. an application that cannot react quickly enough with the time a single message of this type is sent, more than 2 Tx buffer may become necessary.
- The application uses the standard interfaces of the CAN / CAN FD stack to feed these messages.
- Whenever Tx confirmation is indicated for the second but last message of this type with pending Tx request, the application needs to submit at least one new Tx request. Note Tx confirmation is a standard feature in the AUTOSAR SW architecture.
- Before initially leaving INIT state of the M_CAN IP by clearing CCCR.INIT bit, make sure to activate a Tx request after having cleared CCCR.CCE. This will ensure that the conditions for the occurrence of the limitation when synchronizing to the CAN bus the first time after RESET are prevented.

■ Fix Status

No silicon fix planned.

2. CAN FD controller message order inversion when transmitting from dedicated Tx Buffers configured with same Message ID

■ Problem Definition

CAN FD controller message order inversion when multiple Tx Buffers that are configured with the same Message ID have pending Tx requests.

■ Configuration

Several Tx Buffers are configured with the same Message ID. Transmission of these Tx Buffers is requested sequentially with a delay between the individual Tx requests.

■ Expected behavior

When multiple Tx Buffers that are configured with the same Message ID have pending Tx requests, they shall be transmitted in ascending order of their Tx Buffer numbers. The Tx Buffer with lowest buffer number and pending Tx request is transmitted first.

■ Observed behavior

It may happen, depending on the delay between the individual Tx requests, that where multiple Tx Buffers are configured with the same Message ID the Tx Buffers are not transmitted in order of the Tx Buffer number (lowest number first).

■ Workaround

First, write the group of Tx messages with the same Message ID to the Message RAM and then request transmission of all these messages concurrently by a single write access to TXBAR. Before requesting a group of Tx messages with this Message ID, ensure that no message with this Message ID has a pending Tx request.

Applications not able to use the above workaround can implement a counter within the data section of their messages sent with same ID in order to allow the recipients to determine the correct sending sequence.

■ Fix Status

No silicon fix planned

3. CAN FD incomplete description of Dedicated Tx Buffers and Tx Queue related to transmission from multiple buffers configured with the same Message ID**■ Problem Definition**

There was an incomplete description related to transmission from multiple buffers configured with the same Message ID in Section 3.5.2 Dedicated Tx Buffers and Section 3.5.4 Tx Queue of the Hardware Manual.

■ Detailed explanation

The following is the updated description in Section 3.5.2 Dedicated Tx Buffers and Section 3.5.4 Tx Queue of the Hardware Manual.

Section 3.5.2 Dedicated Tx Buffers:

- Original content in the Hardware Manual:

In case that multiple Tx Buffers are configured with the same Message ID, the Tx Buffer with the lowest buffer number is transmitted first.

- Enhancement:

These Tx buffers shall be requested in ascending order with the lowest buffer number first. Alternatively, all Tx buffers configured with the same Message ID can be requested simultaneously by a single write access to TXBAR.

Section 3.5.4 Tx Queue:

- Original content in the Hardware Manual:

In case that multiple Queue Buffers are configured with the same Message ID, the Queue Buffer with the lowest buffer number is transmitted first.

- Replacement:

In case that multiple Tx Queue buffers are configured with the same Message ID, the transmission order depends on numbers of the buffers where the messages were stored for transmission. As these buffer numbers depend on the then current states of the PUT index, a prediction of the transmission order is not possible.

- Original content in the Hardware Manual:

An Add Request cyclically increments the Put Index to the next free Tx Buffer.

- Replacement:

The Put Index always points to that free buffer of the Tx Queue with the lowest buffer number.

■ Workaround

In case a defined order of transmission is required, the Tx FIFO shall be used for transmission of messages with the same Message ID. Alternatively, dedicated Tx buffers with the same Message ID shall be requested in ascending order with the lowest buffer number first or by a single write access to TXBAR. Alternatively, a single Tx Buffer can be used to transmit those messages one after the other.

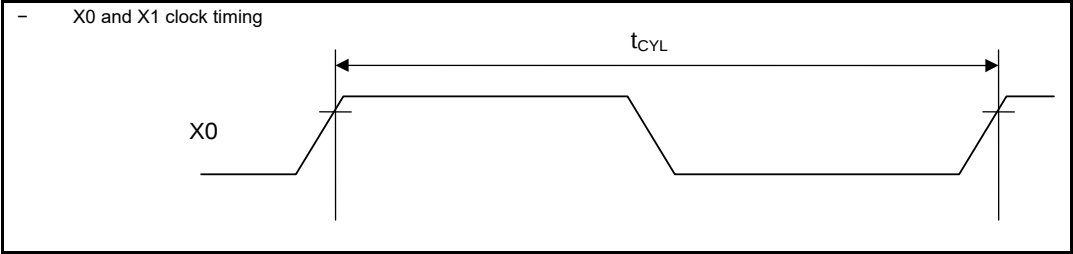
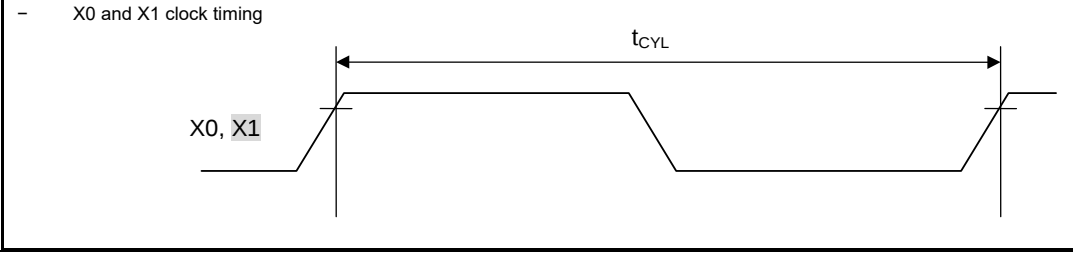
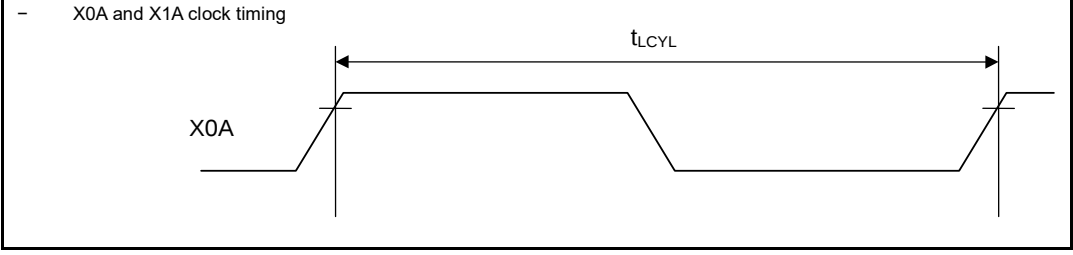
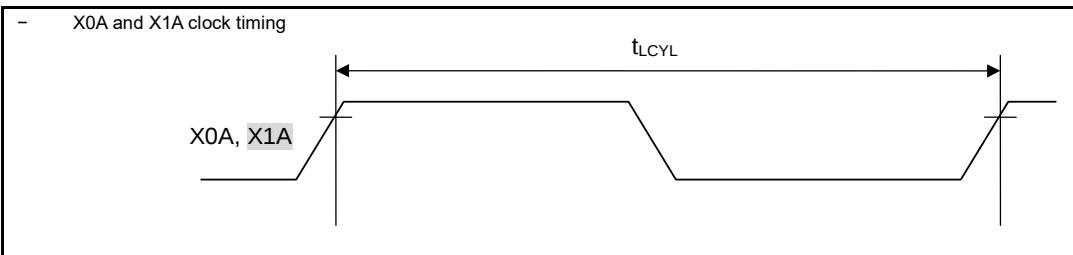
■ Fix Status

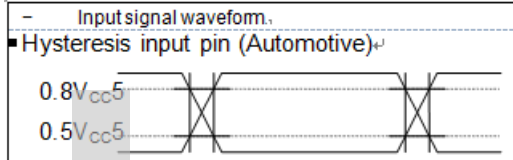
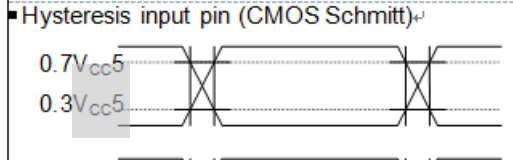
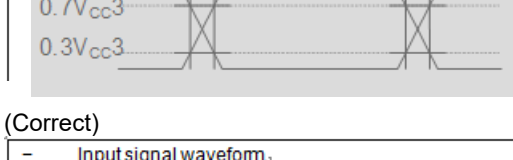
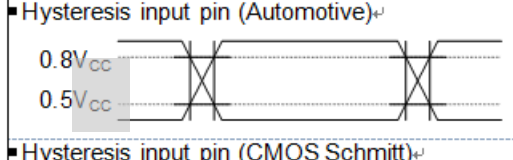
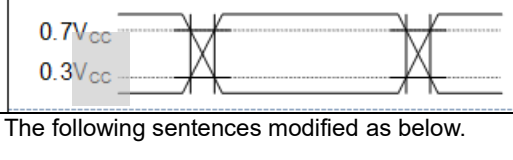
No silicon fix planned. Use workaround.

Hardware Manual will be updated accordingly.

12. Major Changes

Page	Section	Change Results																																																												
Rev.*A																																																														
1 to 109	Datasheet title	Modified the datasheet to be Advance instead of Preliminary.																																																												
1 to 109	Datasheet title	Modified title to include the part series instead of individual part numbers. (Error) S6J34xxJxx, S6J34xxHxx S6J34xxGxx, S6J34xxFxx (Correct) S6J3400 Series																																																												
8	1.2 Optional Function	Modified the Basic Option as following. (Error) *Function : <table><tr><td>Digit</td><td>FlexRay</td></tr><tr><td>2</td><td>Yes</td></tr><tr><td>4</td><td>-</td></tr></table> (Correct) *Function : <table><tr><td>Digit</td><td>FlexRay</td></tr><tr><td>1</td><td>Yes</td></tr><tr><td>2</td><td>-</td></tr></table>	Digit	FlexRay	2	Yes	4	-	Digit	FlexRay	1	Yes	2	-																																																
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2	-																																																													
9 to 12	1.3 Precautions and Handling Devices	Added the section of Precautions and Handling Devices.																																																												
43	4. Block Diagram	Updated the Figure 4-1 Block Diagram.																																																												
52	6.3 AC Characteristics	Modified the Source Clock Timing as following. (Error) <table><tr><th rowspan="2">Parameter</th><th rowspan="2">Symbol</th><th rowspan="2">Pin Name</th><th rowspan="2">Conditions</th><th colspan="3">Value</th><th rowspan="2">Unit</th><th rowspan="2">Remarks</th></tr><tr><th>Min</th><th>Typ</th><th>Max</th></tr><tr><td>Source oscillation clock frequency</td><td>f_c</td><td>X0, X1</td><td>-</td><td>3.6</td><td>-</td><td>16</td><td>MHz</td><td></td></tr><tr><td>Source oscillation clock cycle time</td><td>t_{cYL}</td><td>X0, X1</td><td>-</td><td>62.5</td><td>250.0</td><td>-</td><td>ns</td><td></td></tr></table> (Correct) <table><tr><th rowspan="2">Parameter</th><th rowspan="2">Symbol</th><th rowspan="2">Pin Name</th><th rowspan="2">Conditions</th><th colspan="3">Value</th><th rowspan="2">Unit</th><th rowspan="2">Remarks</th></tr><tr><th>Min</th><th>Typ</th><th>Max</th></tr><tr><td>Source oscillation clock frequency</td><td>f_c</td><td>X0, X1</td><td>-</td><td>3.6</td><td>-</td><td>16</td><td>MHz</td><td></td></tr><tr><td>Source oscillation clock cycle time</td><td>t_{cYL}</td><td>X0, X1</td><td>-</td><td>62.5</td><td>-</td><td>277.8</td><td>ns</td><td></td></tr></table>	Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks	Min	Typ	Max	Source oscillation clock frequency	f _c	X0, X1	-	3.6	-	16	MHz		Source oscillation clock cycle time	t _{cYL}	X0, X1	-	62.5	250.0	-	ns		Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks	Min	Typ	Max	Source oscillation clock frequency	f _c	X0, X1	-	3.6	-	16	MHz		Source oscillation clock cycle time	t _{cYL}	X0, X1	-	62.5	-	277.8	ns	
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Page	Section	Change Results
52	6.3 AC Characteristics	Modified the X0 and X1 clock timing as below. (Error)  (Correct) 
53	6.3 AC Characteristics	Modified the X0A and X1A clock timing as below. (Error)  (Correct) 
54	6.3 AC Characteristics	The following sentences modified as below. (Error) Corresponding functions for these clocks are described in Chapter 5: Clock Configuration of the S6J3300 series hardware manual. (Correct) Corresponding functions for these clocks are described in Chapter 5: Clock Configuration of the S6J3400 series hardware manual.

Page	Section	Change Results								
56	6.3 AC Characteristics	The following sentences modified as below. (Error) Input signal waveform. ■ Hysteresis input pin (Automotive)[↵]  0.8V_{cc5} 0.5V_{cc5} ■ Hysteresis input pin (CMOS Schmitt)[↵]  0.7V_{cc5} 0.3V_{cc5}  0.7V_{cc3} 0.3V_{cc3} (Correct) Input signal waveform. ■ Hysteresis input pin (Automotive)[↵]  0.8V_{cc} 0.5V_{cc} ■ Hysteresis input pin (CMOS Schmitt)[↵]  0.7V_{cc} 0.3V_{cc}								
64	6.3 AC Characteristics	The following sentences modified as below. (Error) <table><tr><td>SOT → SCK ↓[↵] delay time[↵]</td><td>t_{SOVLI}[↵]</td><td>SCK0 to SCK13[↵] SOT0 to SOT13[↵]</td><td>t_{CLK_LCPnA}*1 -30[↵]</td></tr></table> (Correct) <table><tr><td>SOT → SCK ↓[↵] delay time[↵]</td><td>t_{SOVLI}[↵]</td><td>SCK0 to SCK13[↵] SOT0 to SOT13[↵]</td><td>2t_{CLK_LCPnA}*1 -30[↵]</td></tr></table>	SOT → SCK ↓ [↵] delay time [↵]	t _{SOVLI} [↵]	SCK0 to SCK13 [↵] SOT0 to SOT13 [↵]	t _{CLK_LCPnA} *1 -30 [↵]	SOT → SCK ↓ [↵] delay time [↵]	t _{SOVLI} [↵]	SCK0 to SCK13 [↵] SOT0 to SOT13 [↵]	2t _{CLK_LCPnA} *1 -30 [↵]
SOT → SCK ↓ [↵] delay time [↵]	t _{SOVLI} [↵]	SCK0 to SCK13 [↵] SOT0 to SOT13 [↵]	t _{CLK_LCPnA} *1 -30 [↵]							
SOT → SCK ↓ [↵] delay time [↵]	t _{SOVLI} [↵]	SCK0 to SCK13 [↵] SOT0 to SOT13 [↵]	2t _{CLK_LCPnA} *1 -30 [↵]							
66	6.3 AC Characteristics	The following sentences modified as below. (Error) <table><tr><td>SOT → SCK ↑[↵] delay time[↵]</td><td>t_{SOVHI}[↵]</td><td>SCK0 to SCK13[↵] SOT0 to SOT13[↵]</td><td>t_{CLK_LCPnA}*1 -30[↵]</td></tr></table> (Correct) <table><tr><td>SOT → SCK ↑[↵] delay time[↵]</td><td>t_{SOVHI}[↵]</td><td>SCK0 to SCK13[↵] SOT0 to SOT13[↵]</td><td>2t_{CLK_LCPnA}*1 -30[↵]</td></tr></table>	SOT → SCK ↑ [↵] delay time [↵]	t _{SOVHI} [↵]	SCK0 to SCK13 [↵] SOT0 to SOT13 [↵]	t _{CLK_LCPnA} *1 -30 [↵]	SOT → SCK ↑ [↵] delay time [↵]	t _{SOVHI} [↵]	SCK0 to SCK13 [↵] SOT0 to SOT13 [↵]	2t _{CLK_LCPnA} *1 -30 [↵]
SOT → SCK ↑ [↵] delay time [↵]	t _{SOVHI} [↵]	SCK0 to SCK13 [↵] SOT0 to SOT13 [↵]	t _{CLK_LCPnA} *1 -30 [↵]							
SOT → SCK ↑ [↵] delay time [↵]	t _{SOVHI} [↵]	SCK0 to SCK13 [↵] SOT0 to SOT13 [↵]	2t _{CLK_LCPnA} *1 -30 [↵]							

Page	Section	Change Results																
86, 87	6.4 A/D Converter	The following sentences modified as below. (Error) <table><tr><td>Analog port input current^o</td><td>I_{AIN}^o</td><td>AN000 to AN031, ^o AN100 to AN131</td><td>-1.0^o</td><td>-^o</td><td>1.0^o</td><td>μA^o</td><td>V_{AVSS}≤^o V_{AIN}≤V_{AVCC}^o</td></tr></table> (Correct) <table><tr><td>Analog port input current^o</td><td>I_{AIN}^o</td><td>AN000 to AN031, ^o AN100 to AN131</td><td>-1.0^o</td><td>-^o</td><td>1.0^o</td><td>μA^o</td><td>V_{SS}≤^o V_{AIN}≤V_{CC}^o</td></tr></table>	Analog port input current ^o	I _{AIN} ^o	AN000 to AN031, ^o AN100 to AN131	-1.0 ^o	- ^o	1.0 ^o	μA ^o	V _{AVSS} ≤ ^o V _{AIN} ≤V _{AVCC} ^o	Analog port input current ^o	I _{AIN} ^o	AN000 to AN031, ^o AN100 to AN131	-1.0 ^o	- ^o	1.0 ^o	μA ^o	V _{SS} ≤ ^o V _{AIN} ≤V _{CC} ^o
Analog port input current ^o	I _{AIN} ^o	AN000 to AN031, ^o AN100 to AN131	-1.0 ^o	- ^o	1.0 ^o	μA ^o	V _{AVSS} ≤ ^o V _{AIN} ≤V _{AVCC} ^o											
Analog port input current ^o	I _{AIN} ^o	AN000 to AN031, ^o AN100 to AN131	-1.0 ^o	- ^o	1.0 ^o	μA ^o	V _{SS} ≤ ^o V _{AIN} ≤V _{CC} ^o											
87	6.4 A/D Converter	The following *6 sentences deleted. (Error) *6: 1LSB=(AVRH-AVRL)/4096																
92 to 96	7. Ordering Information	Modified the section 7.Ordering Information.																
107, 108	9. Acronyms	Moved the Acronyms table to the end of the document																
Rev.*B																		
-	-	Removed Spansion from the content. Modified content for better clarity.																
Rev.*C																		
6	1.Features 1.2Optional Function	Revised Option as below (Correct) Option: <table><tr><th>Digit</th><th>SHE</th><th>MK_CEER*</th></tr><tr><td>S</td><td>ON</td><td>Fixed to Enable</td></tr><tr><td>T</td><td>OFF</td><td>Fixed to Enable</td></tr><tr><td>U</td><td>ON</td><td>Selectable</td></tr><tr><td>V</td><td>OFF</td><td>Selectable</td></tr></table> *: Chip Erase Enable Register	Digit	SHE	MK_CEER*	S	ON	Fixed to Enable	T	OFF	Fixed to Enable	U	ON	Selectable	V	OFF	Selectable	
Digit	SHE	MK_CEER*																
S	ON	Fixed to Enable																
T	OFF	Fixed to Enable																
U	ON	Selectable																
V	OFF	Selectable																
6	1.Features 1.2Optional Function	Revised Memory size as below: (Error) Memory size: <table><tr><td rowspan="2">Digit</td><td colspan="2">Flash</td></tr><tr><td>Main</td><td>Work</td></tr></table> (Correct) Memory size: <table><tr><td rowspan="2">Digit</td><td colspan="2">Flash</td></tr><tr><td>Program</td><td>Work</td></tr></table>	Digit	Flash		Main	Work	Digit	Flash		Program	Work						
Digit	Flash																	
	Main	Work																
Digit	Flash																	
	Program	Work																

Page	Section	Change Results			
7	1.Features 1.2.4 Restriction	Revised Port Name as below:			
		(Error)			
		Function	TEQFP144 LQFP144	TEQFP120 LQFP120	TEQFP100 LQFP100
		General-Purpose I/O	P0_02, P0_04, P0_11, P0_14, P0_25 to 0_26, P1_02, P1_04, P1_10 to 1_11, P1_16, P1_21, P1_24 to 1_25, P2_00 to 2_01, P2_16 to 2_17, P2_21, P3_03, P3_10 to 3_11, P3_16, P3_20, P3_25 to 3_26, P3_28 to 3_29, P4_10, P4_12, P4_15, P4_19	P0_00, P0_02 to P0_04, P0_11, P0_14, P0_18 to 0_19, P0_24 to 0_26, P1_01 to 1_02, P1_04, P1_10 to 1_11, P1_15 to 1_16, P1_18, P1_20 to 1_21, P1_24 to 1_25, P1_29, P2_00 to 2_01, P2_08, P2_12, P2_16 to 2_17, P2_21, P2_31, P3_03, P3_06, P3_10 to 3_12, P3_16 to 3_20, P3_25 to 3_26, P3_28 to 3_30, P4_07 to 4_08, P4_10 to 4_12, P4_14 to 4_15, P4_17, P4_19	P0_00, P0_02 to P0_04, P0_08 to P0_09, P0_11, P0_14, P0_17 to 0_19, P0_23 to 0_26, P0_30, P1_01 to 1_02, P1_04, P1_10 to 1_11, P1_13, P1_15 to 1_16, P1_18, P1_20 to 1_21, P1_24 to 1_25, P1_27, P1_29, P2_00 to 2_01, P2_03, P2_06, P2_08, P2_10, P2_12, P2_16 to 2_19, P2_21, P2_30 to 2_31, P3_00, P3_03, P3_06, P3_08, P3_10 to 3_12, P3_16 to 3_20, P3_25 to 3_26, P3_28 to 3_30, P4_03 to 4_04, P4_06 to 4_08, P4_10 to 4_12, P4_14 to 4_15, P4_17 to 4_19, P4_21
		(Correct)			
		Function	TEQFP144 LQFP144	TEQFP120 LQFP120	TEQFP100 LQFP100
		General-Purpose I/O	P002, P004, P011, P014, P025 to 026, P102, P104, P110 to 111, P116, P121, P124 to 125, P200 to 201, P216 to 217, P221, P303, P310 to 311, P316, P320, P325 to 326, P328 to 329, P410, P412, P415, P419	P000, P002 to P004, P011, P014, P018 to 019, P024 to 026, P101 to 102, P104, P110 to 111, P115 to 116, P118, P120 to 121, P124 to 125, P129, P200 to 201, P208, P212, P216 to 217, P221, P231, P303, P306, P310 to 312, P316 to 320, P325 to 326, P328 to 330, P407 to 408, P410 to 412, P414 to 415, P417, P419	P000, P002 to P004, P008 to P009, P011, P014, P017 to 019, P023 to 026, P030, P101 to 102, P104, P110 to 111, P113, P115 to 116, P118, P120 to 121, P124 to 125, P127, P129, P200 to 201, P203, P206, P208, P210, P212, P216 to 219, P221, P230 to 231, P300, P303, P306, P308, P310 to 312, P316 to 320, P325 to 326, P328 to 330, P403 to 404, P406 to 408, P410 to 412, P414 to 415, P417 to 419, P421

Page	Section	Change Results																																										
47	7.Electric Characteristics 7.1 Absolute Maximum Rating	Added Remarks of a comment as below: (Correct) <table><tr><th rowspan="2">Parameter</th><th rowspan="2">Symbol</th><th colspan="2">Rating</th><th rowspan="2">Unit</th><th rowspan="2">Remarks</th></tr><tr><th>Min</th><th>Max</th></tr><tr><td>Maximum clamp current *9</td><td> I_{CLAMP} </td><td>-</td><td>4</td><td>mA</td><td>*10</td></tr><tr><td>Total maximum clamp current *9</td><td>Σ I_{CLAMP} </td><td>-</td><td>20</td><td>mA</td><td>*10</td></tr></table>	Parameter	Symbol	Rating		Unit	Remarks	Min	Max	Maximum clamp current *9	I _{CLAMP}	-	4	mA	*10	Total maximum clamp current *9	Σ I _{CLAMP}	-	20	mA	*10																						
Parameter	Symbol	Rating			Unit	Remarks																																						
		Min	Max																																									
Maximum clamp current *9	I _{CLAMP}	-	4	mA	*10																																							
Total maximum clamp current *9	Σ I _{CLAMP}	-	20	mA	*10																																							
48	7.Electric Characteristics 7.1 Absolute Maximum Rating	Added Note of a comment as below: Maximum clamp current, Total maximum clamp current (Correct) *10 VI or VO should never exceed the specified ratings. However, if the maximum current to/from an input is limited by a suitable external resistor, the ICLAMP rating supersedes the VI rating.																																										
49	7.Electric Characteristics 7.2 Recommended Operating Conditions	Revised as below (Error) *1: When it is used outside recommended range (this is the range of guaranteed operation), contact your sales representative. Moreover, the minimum supply voltage value with an external low-voltage detection reset must meet this range requirement because it will be the chip operating value until reset occurs. (Correct) *1: When it is used outside recommended range (this is the range of guaranteed operation), contact your sales representative. Detection voltage of the external low voltage detection reset (initial) is 2.6V±3.5%. This detection voltage level setting is below the minimum operation assurance voltage (2.7V) . Between this detection voltage and the minimum operation assurance voltage, MCU functions are not guaranteed except for the low voltage detector. Note that although the detection level is below the minimum operation guarantee voltage, the LVD reset factor flag is set as the voltage drops below the detection level.																																										
50	7.Electrical Characteristics 7.3DC Characteristics	Revised "H" level Input voltage as below: (Error) <table><tr><th rowspan="2">Parameter</th><th rowspan="2">Symbol</th><th rowspan="2">Pin Name</th><th rowspan="2">Condit ions</th><th colspan="3">Value</th><th rowspan="2">Unit</th><th rowspan="2">Remarks</th></tr><tr><th>Min</th><th>Typ</th><th>Max</th></tr><tr><td>"H" level Input voltage</td><td>V_{IH11}</td><td>TRST, TCK, TDI, TMS</td><td>TTL input level</td><td>2.0</td><td>-</td><td>V_{CC}+0.3</td><td>V</td><td>-</td></tr></table> (Correct) <table><tr><th rowspan="2">Parameter</th><th rowspan="2">Symbol</th><th rowspan="2">Pin Name</th><th rowspan="2">Condit ions</th><th colspan="3">Value</th><th rowspan="2">Unit</th><th rowspan="2">Remarks</th></tr><tr><th>Min</th><th>Typ</th><th>Max</th></tr><tr><td>"H" level Input voltage</td><td>V_{IH11}</td><td>TRST, TCK, TDI, TMS</td><td>TTL input level</td><td>2.7</td><td>-</td><td>V_{CC}+0.3</td><td>V</td><td>-</td></tr></table>	Parameter	Symbol	Pin Name	Condit ions	Value			Unit	Remarks	Min	Typ	Max	"H" level Input voltage	V _{IH11}	TRST, TCK, TDI, TMS	TTL input level	2.0	-	V _{CC} +0.3	V	-	Parameter	Symbol	Pin Name	Condit ions	Value			Unit	Remarks	Min	Typ	Max	"H" level Input voltage	V _{IH11}	TRST, TCK, TDI, TMS	TTL input level	2.7	-	V _{CC} +0.3	V	-
Parameter	Symbol	Pin Name					Condit ions	Value				Unit	Remarks																															
			Min	Typ	Max																																							
"H" level Input voltage	V _{IH11}	TRST, TCK, TDI, TMS	TTL input level	2.0	-	V _{CC} +0.3	V	-																																				
Parameter	Symbol	Pin Name	Condit ions	Value			Unit	Remarks																																				
				Min	Typ	Max																																						
"H" level Input voltage	V _{IH11}	TRST, TCK, TDI, TMS	TTL input level	2.7	-	V _{CC} +0.3	V	-																																				

Page	Section	Change Results																												
53	7.Electrical Characteristics 7.3 DC Characteristics	Added Conditions *3 and *3 sentences as below: (Error) <table><tr><th>Parameter</th><th>Symbol</th><th>Pin Name</th><th>Conditions</th></tr><tr><td></td><td></td><td></td><td></td></tr></table> (Correct) <table><tr><th>Parameter</th><th>Symbol</th><th>Pin Name</th><th>Conditions</th></tr><tr><td></td><td></td><td></td><td>*3</td></tr></table> *3: Corresponding mode sets for state definitions are described in Chapter 12: State Transition of the S6J3400 Series hardware manual	Parameter	Symbol	Pin Name	Conditions					Parameter	Symbol	Pin Name	Conditions				*3												
Parameter	Symbol	Pin Name	Conditions																											
Parameter	Symbol	Pin Name	Conditions																											
			*3																											
54	7.Electrical Characteristics 7.3 DC Characteristics	Added Conditions *3 and *3 sentences as below: (Error) <table><tr><th>Parameter</th><th>Symbol</th><th>Pin Name</th><th>Conditions</th></tr><tr><td></td><td></td><td></td><td></td></tr></table> (Correct) <table><tr><th>Parameter</th><th>Symbol</th><th>Pin Name</th><th>Conditions</th></tr><tr><td></td><td></td><td></td><td>*3</td></tr></table> *3: Corresponding mode sets for state definitions are described in Chapter 12: State Transition of the S6J3400 Series hardware manual	Parameter	Symbol	Pin Name	Conditions					Parameter	Symbol	Pin Name	Conditions				*3												
Parameter	Symbol	Pin Name	Conditions																											
Parameter	Symbol	Pin Name	Conditions																											
			*3																											
57	7.Electrical Characteristics 7.4.3 Internal Clock Timing	Added Symbol as below: (Correct) <table><tr><th rowspan="2">Parameter</th><th rowspan="2">Symbol</th><th colspan="2">Value</th><th rowspan="2">Unit</th><th rowspan="2">Remarks</th></tr><tr><th>Max *1</th><th>Max *2</th></tr><tr><td rowspan="2">Internal clock frequency</td><td>f_{SSCG0}</td><td>264</td><td>320</td><td>MHz</td><td>-</td></tr><tr><td>f_{PLL0}</td><td>288</td><td>288</td><td>MHz</td><td>-</td></tr></table>	Parameter	Symbol	Value		Unit	Remarks	Max *1	Max *2	Internal clock frequency	f _{SSCG0}	264	320	MHz	-	f _{PLL0}	288	288	MHz	-									
Parameter	Symbol	Value			Unit	Remarks																								
		Max *1	Max *2																											
Internal clock frequency	f _{SSCG0}	264	320	MHz	-																									
	f _{PLL0}	288	288	MHz	-																									
57	7.Electrical Characteristics 7.4.3 Internal Clock Timing	Revised " F_{CLK_TRC}" as below: (Error) <table><tr><th rowspan="2">Parameter</th><th rowspan="2">Symbol</th><th colspan="2">Value</th><th rowspan="2">Unit</th><th rowspan="2">Remarks</th></tr><tr><th>Max *1</th><th>Max *2</th></tr><tr><td>Internal clock frequency</td><td>f_{CLK_TRC}</td><td>132</td><td>80</td><td>MHz</td><td>-</td></tr></table> (Correct) <table><tr><th rowspan="2">Parameter</th><th rowspan="2">Symbol</th><th colspan="2">Value</th><th rowspan="2">Unit</th><th rowspan="2">Remarks</th></tr><tr><th>Max *1</th><th>Max *2</th></tr><tr><td>Internal clock frequency</td><td>f_{CLK_TRC}</td><td>66</td><td>40</td><td>MHz</td><td>-</td></tr></table>	Parameter	Symbol	Value		Unit	Remarks	Max *1	Max *2	Internal clock frequency	f _{CLK_TRC}	132	80	MHz	-	Parameter	Symbol	Value		Unit	Remarks	Max *1	Max *2	Internal clock frequency	f _{CLK_TRC}	66	40	MHz	-
Parameter	Symbol	Value			Unit	Remarks																								
		Max *1	Max *2																											
Internal clock frequency	f _{CLK_TRC}	132	80	MHz	-																									
Parameter	Symbol	Value		Unit	Remarks																									
		Max *1	Max *2																											
Internal clock frequency	f _{CLK_TRC}	66	40	MHz	-																									

Page	Section	Change Results
58	7.Electrical Characteristics 7.4.3 Internal Clock Timing	Revised Operation assurance range; Relationship between the internal clock frequency and supply voltage as below: (Error) (Correct) Legend: - Recommended guaranteed operation range: Dashed black/blue rectangle - Guaranteed operation range: Solid black rectangle - PLL guaranteed operation range: Shaded gray rectangle

Page

Section

607.Electrical Characteristi

cs

7.4.5 Power-on Conditions

Revised as below:

(Error)

6.3.5

Power-on Conditions

(Condition: See 6.1. Operation assurance condition)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Level detection voltage	-	VCC	-	2.2	2.4	2.6	V	
Level detection hysteresis width	-	VCC	-	-	100	-	mV	
Level detection time	-	-	-	-	-	40	μs	*1
Slope detection undetected standard	-	VCC	VCC = at level detection release level time	-	-	4	mV/μs	*2
Power off time	-	VCC	-	50	-	-	ms	*3

*1: If a power fluctuation precedes the low-voltage detection time, the detection may occur or be canceled after the supply voltage passes the detection voltage range.

*2: This is the period from when the power supply is turned off to when an internal charge is released and tilt detection becomes possible for the next power-on.

*3: This time is to start the slope detection at the next power on after power down and internal charge loss.

(Correct)

7.4.5

Power-on Conditions

(Condition: See Recommended Operating Conditions)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Level detection voltage	-	VCC	-	2.2	2.4	2.6	V	
Level detection hysteresis width	-	VCC	-	-	100	-	mV	
Level detection time	-	-	-	-	-	40	μs	*1
Power off time	-	VCC	-	100	-	-	μs	*2
Power ramp rate	dV/dt	VCC	VCC: 1.5V to 2.6V	-	-	1	V/μs	*3
Maximum ramp rate guaranteed to not generate power-on reset	dV/dt	VCC	VCC: Between 2.7V and 4.5V	-	-	50	mV/μs	*4

*1: This specification is at 1V/μs of power ramp rate.

*2: VCC must be held below 1.5V for a minimum period of t_{off}.

*3: Power ramp rate must be 1V/μs or less from 1.5V to 2.6V. Power-on can detect by satisfying power ramp rate and power off time.

*4: This specification is specified the power supply fluctuation after power on detection. When VCC voltage is between 2.7V and 4.5V, the power supply fluctuation is below 50mV/μs, the detection of power-on is suppressed. The power-on does not detect in any power fluctuation between 4.5V and 5.5V.

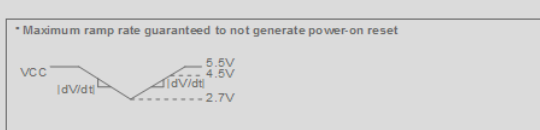
Notes:

When using S6J3400 Series,*2 and *3 must be satisfied. When neither*2 nor*3 can be satisfied, assert external reset (RSTX) at power up and any brownout event.

Power off time, Power ramp rate



Maximum ramp rate guaranteed to not generate power-on reset



Page	Section	Change Results																																				
79	7.Electrical Characteristics 7.4.6.4 I ² C Timing	Revised as below: (Error) <table><tr><th colspan="2">High-Speed Mode</th></tr><tr><th>Min</th><th>Max</th></tr><tr><td></td><td></td></tr></table> Notes: There is standard mode/high-speed mode correspondence only ch.3 and ch.5. In ch.0 to ch2, ch.4, and ch.6 to ch.13, the only correspondence is standard mode. *3: A high-speed mode I²C bus device can be used on a standard mode I²C bus system as long as the device satisfies the requirement of "t_{SUDAT} ≥ 250 ns". (Correct) <table><tr><th colspan="2">Fast Mode</th></tr><tr><th>Min</th><th>Max</th></tr><tr><td></td><td></td></tr></table> Notes: There is standard mode/fast mode correspondence only ch.3 and ch.5. In ch.0 to ch2, ch.4, and ch.6 to ch.13, the only correspondence is standard mode. *3: A fast mode I²C bus device can be used on a standard mode I²C bus system as long as the device satisfies the requirement of "t_{SUDAT} ≥ 250 ns".	High-Speed Mode		Min	Max			Fast Mode		Min	Max																										
High-Speed Mode																																						
Min	Max																																					
Fast Mode																																						
Min	Max																																					
85	7.Electrical Characteristics 7.4.11 Low Voltage Detection (External Voltage)	Added *3 and *3 sentences as below: (Error) <table><tr><td>Detection voltage⁺</td><td>V_{DLAT}⁺</td><td>VCC⁺</td><td>*1⁺</td><td>2.5⁺</td><td>2.6⁺</td><td>2.7⁺</td><td>V⁺</td><td>When power-supply voltage falls⁺ and detection level is set initially⁺ Typ ± 3.5%⁺</td></tr><tr><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr></table> (Correct) <table><tr><td>Detection voltage⁺</td><td>V_{DLAT}⁺</td><td>VCC⁺</td><td>*1⁺</td><td>2.5⁺</td><td>2.6⁺</td><td>2.7⁺</td><td>V⁺</td><td>When power-supply voltage falls⁺ and detection level is set initially⁺ *3⁺ Typ ± 3.5%⁺</td></tr><tr><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr></table> *3: This detection voltage level setting is below the minimum operation assurance voltage (2.7V) . Between this detection voltage and the minimum operation assurance voltage, MCU functions are not guaranteed except for the low voltage detector. Note that although the detection level is below the minimum operation guarantee voltage, the LVD reset factor flag is set as the voltage drops below the detection level.	Detection voltage ⁺	V _{DLAT} ⁺	VCC ⁺	*1 ⁺	2.5 ⁺	2.6 ⁺	2.7 ⁺	V ⁺	When power-supply voltage falls ⁺ and detection level is set initially ⁺ Typ ± 3.5% ⁺										Detection voltage ⁺	V _{DLAT} ⁺	VCC ⁺	*1 ⁺	2.5 ⁺	2.6 ⁺	2.7 ⁺	V ⁺	When power-supply voltage falls ⁺ and detection level is set initially ⁺ *3 ⁺ Typ ± 3.5% ⁺									
Detection voltage ⁺	V _{DLAT} ⁺	VCC ⁺	*1 ⁺	2.5 ⁺	2.6 ⁺	2.7 ⁺	V ⁺	When power-supply voltage falls ⁺ and detection level is set initially ⁺ Typ ± 3.5% ⁺																														
Detection voltage ⁺	V _{DLAT} ⁺	VCC ⁺	*1 ⁺	2.5 ⁺	2.6 ⁺	2.7 ⁺	V ⁺	When power-supply voltage falls ⁺ and detection level is set initially ⁺ *3 ⁺ Typ ± 3.5% ⁺																														

Page	Section	Change Results																																						
85	7.Electrical Characteristics 7.4.12 Low-Voltage Detection (Internal Voltage) 7.4.12.1 Low-voltage Detection (RAM retention low-voltage detection for LVDL0)	Revised as below: (Error) 7.4.12.1 Low-voltage Detection (internal low-voltage detection for LVDL0) (Correct) 7.4.12.1 Low-voltage Detection (RAM retention low-voltage detection for LVDL0)																																						
86	7.Electrical Characteristics 7.4.12 Low-Voltage Detection (Internal Voltage) 7.4.12.2 Low-voltage Detection (internal low-voltage detection for LVDL1)	Revised and added *2 sentences as below: (Error) <table><tr><td>Detection voltage↗</td><td>V_{RDLAT}↗</td><td>→↗</td><td>*1↗</td><td>0.844↗</td><td>0.875↗</td><td>0.906↗</td><td>V↗</td><td>When power-supply voltage falls↗ Typ±3.5%↗</td></tr></table> (Correct) <table><tr><td>Detection voltage↗</td><td>V_{RDLAT}↗</td><td>→↗</td><td>*1↗</td><td>0.844↗</td><td>0.875↗</td><td>0.906↗</td><td>V↗</td><td>When power-supply voltage falls and detection level is set initially *2↗ Typ±3.5%↗</td></tr></table> *2: This detection voltage level setting is below the minimum operation voltage. Between this detection voltage and the minimum operation voltage, MCU functions are not guaranteed except for the low voltage detector. Note that although the detection level is below the minimum operation guarantee voltage, the LVD reset factor flag is set as the voltage drops below the detection level.	Detection voltage↗	V _{RDLAT} ↗	→↗	*1↗	0.844↗	0.875↗	0.906↗	V↗	When power-supply voltage falls↗ Typ±3.5%↗	Detection voltage↗	V _{RDLAT} ↗	→↗	*1↗	0.844↗	0.875↗	0.906↗	V↗	When power-supply voltage falls and detection level is set initially *2↗ Typ±3.5%↗																				
Detection voltage↗	V _{RDLAT} ↗	→↗	*1↗	0.844↗	0.875↗	0.906↗	V↗	When power-supply voltage falls↗ Typ±3.5%↗																																
Detection voltage↗	V _{RDLAT} ↗	→↗	*1↗	0.844↗	0.875↗	0.906↗	V↗	When power-supply voltage falls and detection level is set initially *2↗ Typ±3.5%↗																																
87	7.Electrical Characteristics 7.5 A/D Converter 7.5.1 Electrical Characteristics	Revised as below: (TA: Recommended operating conditions, VCC=5.0 V ± 0.5 V, VSS=AVSS=0.0 V) (Error) <table><tr><th rowspan="2">Parameter</th><th rowspan="2">Symbol</th><th rowspan="2">Pin Name</th><th colspan="3">Conditions</th><th rowspan="2">Unit</th><th rowspan="2">Remarks</th></tr><tr><th>Min</th><th>Typ</th><th>Max</th></tr><tr><td>Analog input voltage</td><td>V_{AIN}</td><td>AN000 to AN031, AN100 to AN131</td><td>AVSS</td><td>-</td><td>AVRH</td><td>V</td><td></td></tr></table> (Correct) <table><tr><th rowspan="2">Parameter</th><th rowspan="2">Symbol</th><th rowspan="2">Pin Name</th><th colspan="3">Conditions</th><th rowspan="2">Unit</th><th rowspan="2">Remarks</th></tr><tr><th>Min</th><th>Typ</th><th>Max</th></tr><tr><td>Analog input voltage</td><td>V_{AIN}</td><td>AN000 to AN031, AN100 to AN131</td><td>AVRL</td><td>-</td><td>AVRH</td><td>V</td><td></td></tr></table>	Parameter	Symbol	Pin Name	Conditions			Unit	Remarks	Min	Typ	Max	Analog input voltage	V _{AIN}	AN000 to AN031, AN100 to AN131	AVSS	-	AVRH	V		Parameter	Symbol	Pin Name	Conditions			Unit	Remarks	Min	Typ	Max	Analog input voltage	V _{AIN}	AN000 to AN031, AN100 to AN131	AVRL	-	AVRH	V	
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Page	Section	Change Results																																																																																						
88	7.Electrical Characteristics 7.5 A/D Converter 7.5.1 Electrical Characteristics	Revised as below: (TA: Recommended operating conditions, VCC=3.3 V ± 0.3 V, VSS=AVSS=0.0 V) (Error) <table><tr><th rowspan="2">Parameter</th><th rowspan="2">Symbol</th><th rowspan="2">Pin Name</th><th colspan="3">Conditions</th><th rowspan="2">Unit</th><th rowspan="2">Remarks</th></tr><tr><th>Min</th><th>Typ</th><th>Max</th></tr><tr><td>Analog input voltage</td><td>V_{AIN}</td><td>AN000 to AN031, AN100 to AN131</td><td>AVSS</td><td>-</td><td>AVRH</td><td>V</td><td></td></tr></table> (Correct) <table><tr><th rowspan="2">Parameter</th><th rowspan="2">Symbol</th><th rowspan="2">Pin Name</th><th colspan="3">Conditions</th><th rowspan="2">Unit</th><th rowspan="2">Remarks</th></tr><tr><th>Min</th><th>Typ</th><th>Max</th></tr><tr><td>Analog input voltage</td><td>V_{AIN}</td><td>AN000 to AN031, AN100 to AN131</td><td>AVRL</td><td>-</td><td>AVRH</td><td>V</td><td></td></tr></table>	Parameter	Symbol	Pin Name	Conditions			Unit	Remarks	Min	Typ	Max	Analog input voltage	V _{AIN}	AN000 to AN031, AN100 to AN131	AVSS	-	AVRH	V		Parameter	Symbol	Pin Name	Conditions			Unit	Remarks	Min	Typ	Max	Analog input voltage	V _{AIN}	AN000 to AN031, AN100 to AN131	AVRL	-	AVRH	V																																																	
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92	7.Electrical Characteristics 7.6 Flash Memory 7.6.1 Electrical Characteristics	Added write time as below: (Error) <table><tr><th rowspan="2">Parameter</th><th colspan="3">Value</th><th rowspan="2">Unit</th><th rowspan="2">Remarks</th></tr><tr><th>Min</th><th>Typ</th><th>Max^{*3}</th></tr><tr><td rowspan="3">Sector erase time</td><td>-</td><td>120</td><td>480</td><td>ms</td><td>Large sector^{*1} Internal preprogramming time included</td></tr><tr><td>-</td><td>120</td><td>480</td><td>ms</td><td>8-kB sector^{*1} Internal preprogramming time included</td></tr><tr><td>-</td><td>120</td><td>480</td><td>ms</td><td>4-kB sector^{*2} Internal preprogramming time included</td></tr><tr><td>32-bit write time</td><td>-</td><td>30</td><td>384</td><td>μs</td><td>System-level overhead time excluded^{*1}</td></tr><tr><td>64-bit write time</td><td>-</td><td>30</td><td>384</td><td>μs</td><td>System-level overhead time excluded^{*1}</td></tr><tr><td>256-bit write time</td><td>-</td><td>40</td><td>512</td><td>μs</td><td>System-level overhead time excluded^{*1}</td></tr></table> (Correct) <table><tr><th rowspan="2">Parameter</th><th colspan="3">Value</th><th rowspan="2">Unit</th><th rowspan="2">Remarks</th></tr><tr><th>Min</th><th>Typ</th><th>Max^{*3}</th></tr><tr><td rowspan="3">Sector erase time</td><td>-</td><td>120</td><td>480</td><td>ms</td><td>Large sector^{*1} Internal preprogramming time included</td></tr><tr><td>-</td><td>120</td><td>480</td><td>ms</td><td>8-kB sector^{*1} Internal preprogramming time included</td></tr><tr><td>-</td><td>120</td><td>480</td><td>ms</td><td>4-kB sector^{*2} Internal preprogramming time included</td></tr><tr><td>32-bit write time(Program)</td><td>-</td><td>30</td><td>384</td><td>μs</td><td>System-level overhead time excluded^{*1}</td></tr><tr><td>64-bit write time(Program)</td><td>-</td><td>30</td><td>384</td><td>μs</td><td>System-level overhead time excluded^{*1}</td></tr><tr><td>256-bit write time(Program)</td><td>-</td><td>40</td><td>512</td><td>μs</td><td>System-level overhead time excluded^{*1}</td></tr></table>	Parameter	Value			Unit	Remarks	Min	Typ	Max ^{*3}	Sector erase time	-	120	480	ms	Large sector ^{*1} Internal preprogramming time included	-	120	480	ms	8-kB sector ^{*1} Internal preprogramming time included	-	120	480	ms	4-kB sector ^{*2} Internal preprogramming time included	32-bit write time	-	30	384	μs	System-level overhead time excluded ^{*1}	64-bit write time	-	30	384	μs	System-level overhead time excluded ^{*1}	256-bit write time	-	40	512	μs	System-level overhead time excluded ^{*1}	Parameter	Value			Unit	Remarks	Min	Typ	Max ^{*3}	Sector erase time	-	120	480	ms	Large sector ^{*1} Internal preprogramming time included	-	120	480	ms	8-kB sector ^{*1} Internal preprogramming time included	-	120	480	ms	4-kB sector ^{*2} Internal preprogramming time included	32-bit write time(Program)	-	30	384	μs	System-level overhead time excluded ^{*1}	64-bit write time(Program)	-	30	384	μs	System-level overhead time excluded ^{*1}	256-bit write time(Program)	-	40	512	μs	System-level overhead time excluded ^{*1}
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Page	Section	Change Results																					
92	7.Electrical Characteristics	Revised Erase count*2 /Data retention time*3 as below:																					
	7.6 Flash Memory	(Error)																					
	7.6.1 Electrical Characteristics	<table><tr><th rowspan="2">Parameter</th><th colspan="3">Value</th><th rowspan="2">Unit</th><th rowspan="2">Remarks</th></tr><tr><th>Min</th><th>Typ</th><th>Max*3</th></tr><tr><td>Erase count*2 / Data retention time*3 (code)</td><td>1,000/20 years</td><td>-</td><td>-</td><td>-</td><td>Temperature at write/erase time Average temperature T_A =+85 °C</td></tr><tr><td>Erase count*2 / Data retention time*3 (Work)</td><td>1,000/20 years 10,000/10 years 100,000/5 years</td><td>-</td><td>-</td><td>-</td><td>Temperature at write/erase time Average temperature T_A =+85 °C</td></tr></table>	Parameter	Value			Unit	Remarks	Min	Typ	Max*3	Erase count*2 / Data retention time*3 (code)	1,000/20 years	-	-	-	Temperature at write/erase time Average temperature T _A =+85 °C	Erase count*2 / Data retention time*3 (Work)	1,000/20 years 10,000/10 years 100,000/5 years	-	-	-	Temperature at write/erase time Average temperature T _A =+85 °C
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Page	Section	Change Results																						
93 to 97	8. Ordering Information	Revised the package type as below: (Error) <table><tr><th>Package</th></tr><tr><td>Plastic • LQFP 100-pin (0.5-mm pitch), (FPT-100P-MXX)</td></tr><tr><td>Plastic • TEQFP 100-pin (0.5-mm pitch), (XXX-100P-MXX)</td></tr><tr><td>Plastic • LQFP 120-pin (0.5-mm pitch), (FPT-120P-MXX)</td></tr><tr><td>Plastic • TEQFP 120-pin (0.5-mm pitch), (XXX-120P-MXX)</td></tr><tr><td>Plastic • LQFP 144-pin (0.4-mm pitch), (FPT-144P-MXX)</td></tr><tr><td>Plastic • TEQFP 144-pin (0.4-mm pitch), (XXX-144P-MXX)</td></tr><tr><td>Plastic • LQFP 144-pin (0.5-mm pitch), (FPT-144P-MXX)</td></tr><tr><td>Plastic • TEQFP 144-pin (0.5-mm pitch), (XXX-144P-MXX)</td></tr><tr><td>Plastic • LQFP 176-pin (0.5-mm pitch), (FPT-144P-MXX)</td></tr><tr><td>Plastic • TEQFP 176-pin (0.5-mm pitch), (XXX-144P-MXX)</td></tr></table> (Correct) <table><tr><th>Package</th></tr><tr><td>LQI100 (100-pin 0.5-mm pitch Plastic LQFP)</td></tr><tr><td>LEI100 (100-pin 0.5-mm pitch Plastic TEQFP)</td></tr><tr><td>Lxx120 (120-pin 0.5-mm pitch Plastic LQFP)</td></tr><tr><td>Lxx120 (120-pin 0.5-mm pitch Plastic TEQFP)</td></tr><tr><td>Lxx144 (144-pin 0.4-mm pitch Plastic LQFP)</td></tr><tr><td>Lxx144 (144-pin 0.4-mm pitch Plastic TEQFP)</td></tr><tr><td>LQS144 (144-pin 0.5-mm pitch Plastic LQFP)</td></tr><tr><td>LEJ144 (144-pin 0.5-mm pitch Plastic TEQFP)</td></tr><tr><td>Lxx176 (176-pin 0.5-mm pitch Plastic LQFP)</td></tr><tr><td>LEH176 (176-pin 0.5-mm pitch Plastic TEQFP)</td></tr></table> For LQFP120/TEQFP120/LQFP144(0.4mm pitch)/LQFP176 package product, contact your sales representative.	Package	Plastic • LQFP 100-pin (0.5-mm pitch), (FPT-100P-MXX)	Plastic • TEQFP 100-pin (0.5-mm pitch), (XXX-100P-MXX)	Plastic • LQFP 120-pin (0.5-mm pitch), (FPT-120P-MXX)	Plastic • TEQFP 120-pin (0.5-mm pitch), (XXX-120P-MXX)	Plastic • LQFP 144-pin (0.4-mm pitch), (FPT-144P-MXX)	Plastic • TEQFP 144-pin (0.4-mm pitch), (XXX-144P-MXX)	Plastic • LQFP 144-pin (0.5-mm pitch), (FPT-144P-MXX)	Plastic • TEQFP 144-pin (0.5-mm pitch), (XXX-144P-MXX)	Plastic • LQFP 176-pin (0.5-mm pitch), (FPT-144P-MXX)	Plastic • TEQFP 176-pin (0.5-mm pitch), (XXX-144P-MXX)	Package	LQI100 (100-pin 0.5-mm pitch Plastic LQFP)	LEI100 (100-pin 0.5-mm pitch Plastic TEQFP)	Lxx120 (120-pin 0.5-mm pitch Plastic LQFP)	Lxx120 (120-pin 0.5-mm pitch Plastic TEQFP)	Lxx144 (144-pin 0.4-mm pitch Plastic LQFP)	Lxx144 (144-pin 0.4-mm pitch Plastic TEQFP)	LQS144 (144-pin 0.5-mm pitch Plastic LQFP)	LEJ144 (144-pin 0.5-mm pitch Plastic TEQFP)	Lxx176 (176-pin 0.5-mm pitch Plastic LQFP)	LEH176 (176-pin 0.5-mm pitch Plastic TEQFP)
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98, 99	9. Package Dimensions	Added the 9.Package Dimensions as below: 9.1 LQFP144 (LQS144) 9.2 LQFP (LQI100)																						

Page	Section	Change Results						
Rev.*D								
-	-	Modified from I2C to I ² C.						
1	Features Key Features	Revised as below: Error) ■ 132-MHz operation frequency for S6J3428/9/A/B/C and 144-MHz operation frequency for S6J34xD/E Correct) ■ 132-MHz operation frequency for S6J3428/9/A						
1	Features Key Features	Revised as below: Error) ■ 14-channel Multi-Function Serial (MFS) communication block for S6J3428/9/A and S6J342B/C, 22-channel MFS block for S6J34xD/E Correct) ■ 14-channel Multi-Function Serial (MFS) communication block for S6J3428/9/A						
4	1. Features 1.1 Function List	Added as below: Error) <table border="1"> <tr> <td>Core clock frequency</td><td>132MHz</td><td></td></tr> </table> Correct) <table border="1"> <tr> <td>Core clock frequency</td><td>132MHz</td><td>See the AC specification on this datasheet</td></tr> </table>	Core clock frequency	132MHz		Core clock frequency	132MHz	See the AC specification on this datasheet
Core clock frequency	132MHz							
Core clock frequency	132MHz	See the AC specification on this datasheet						
4	1. Features 1.1 Function List	Added as below: Error) <table border="1"> <tr> <td>HPM bus frequency</td><td>33MHz</td><td></td></tr> </table> Correct) <table border="1"> <tr> <td>HPM bus frequency</td><td>33MHz</td><td>See the AC specification on this datasheet</td></tr> </table>	HPM bus frequency	33MHz		HPM bus frequency	33MHz	See the AC specification on this datasheet
HPM bus frequency	33MHz							
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Page	Section	Change Results										
4	1. Features 1.1 Function List	Added as below: Error) <table border="1"> <tr> <td>Embedded CR oscillation</td><td>Slow clock:100kHz, Fast clock: 4MHz (Center frequency)</td><td></td></tr> </table> Correct) <table border="1"> <tr> <td>Embedded CR oscillation</td><td>Slow clock:100kHz, Fast clock: 4MHz (Center frequency)</td><td>See the AC specification on this datasheet</td></tr> </table>	Embedded CR oscillation	Slow clock:100kHz, Fast clock: 4MHz (Center frequency)		Embedded CR oscillation	Slow clock:100kHz, Fast clock: 4MHz (Center frequency)	See the AC specification on this datasheet				
Embedded CR oscillation	Slow clock:100kHz, Fast clock: 4MHz (Center frequency)											
Embedded CR oscillation	Slow clock:100kHz, Fast clock: 4MHz (Center frequency)	See the AC specification on this datasheet										
4	1. Features 1.1 Function List	Added as below: Error) <table border="1"> <tr> <td>Power supply</td><td>5.0V ± 0.5V or 3.3V ± 0.3V</td><td></td></tr> </table> Correct) <table border="1"> <tr> <td>Power supply</td><td>5.0V ± 0.5V or 3.3V ± 0.3V</td><td>See the AC specification on this datasheet</td></tr> </table>	Power supply	5.0V ± 0.5V or 3.3V ± 0.3V		Power supply	5.0V ± 0.5V or 3.3V ± 0.3V	See the AC specification on this datasheet				
Power supply	5.0V ± 0.5V or 3.3V ± 0.3V											
Power supply	5.0V ± 0.5V or 3.3V ± 0.3V	See the AC specification on this datasheet										
5	1. Features 1.1 Function List	Added as below: Error) <table border="1"> <tr> <td>Package</td><td>Option</td><td>See 1.2.1</td></tr> </table> Correct) <table border="1"> <tr> <td>Package</td><td>Option</td><td>See Section 1.2.1</td></tr> </table>	Package	Option	See 1.2.1	Package	Option	See Section 1.2.1				
Package	Option	See 1.2.1										
Package	Option	See Section 1.2.1										
5	1. Features 1.1 Function List	Added as below: Error) <table border="1"> <tr> <td>General-purpose I/O</td><td>Option</td><td>See 1.2.3</td></tr> </table> Correct) <table border="1"> <tr> <td>General-purpose I/O</td><td>Option</td><td>See Section 1.2.3</td></tr> </table>	General-purpose I/O	Option	See 1.2.3	General-purpose I/O	Option	See Section 1.2.3				
General-purpose I/O	Option	See 1.2.3										
General-purpose I/O	Option	See Section 1.2.3										
5	1. Features 1.1 Function List	Revised as below: Error) <table border="1"> <tr> <td rowspan="3">I/O timer</td><td>FRT 12 ch, ICU 12 ch, OCU 14 ch</td><td>S6J34xD/E</td></tr> <tr> <td>FRT 12 ch, ICU 12 ch, OCU 14 ch</td><td>S6J342B/C</td></tr> <tr> <td>FRT 8 ch, ICU 12 ch, OCU 12 ch</td><td>S6J3428/9/A</td></tr> </table> Correct) <table border="1"> <tr> <td>I/O timer</td><td>FRT 8 ch, ICU 12 ch, OCU 12 ch</td><td>S6J3428/9/A</td></tr> </table>	I/O timer	FRT 12 ch, ICU 12 ch, OCU 14 ch	S6J34xD/E	FRT 12 ch, ICU 12 ch, OCU 14 ch	S6J342B/C	FRT 8 ch, ICU 12 ch, OCU 12 ch	S6J3428/9/A	I/O timer	FRT 8 ch, ICU 12 ch, OCU 12 ch	S6J3428/9/A
I/O timer	FRT 12 ch, ICU 12 ch, OCU 14 ch	S6J34xD/E										
	FRT 12 ch, ICU 12 ch, OCU 14 ch	S6J342B/C										
	FRT 8 ch, ICU 12 ch, OCU 12 ch	S6J3428/9/A										
I/O timer	FRT 8 ch, ICU 12 ch, OCU 12 ch	S6J3428/9/A										

Page	Section	Change Results																																
5	1. Features 1.1 Function List	Revised as below: Error) <table><tr><td rowspan="3">Base timer</td><td>64ch</td><td>60ch</td><td>55ch</td><td>48ch</td><td></td></tr><tr><td>64ch</td><td>55ch</td><td>47ch</td><td>40ch</td><td>with out pin</td></tr><tr><td>64ch</td><td>57ch</td><td>42ch</td><td>30ch</td><td>with in pin</td></tr></table> Correct) <table><tr><td rowspan="3">Base timer</td><td>64ch</td><td>60ch</td><td>55ch</td><td>48ch</td><td>with output pin or input pin</td></tr><tr><td>64ch</td><td>55ch</td><td>47ch</td><td>40ch</td><td>with output pin</td></tr><tr><td>64ch</td><td>57ch</td><td>42ch</td><td>30ch</td><td>with input pin</td></tr></table>	Base timer	64ch	60ch	55ch	48ch		64ch	55ch	47ch	40ch	with out pin	64ch	57ch	42ch	30ch	with in pin	Base timer	64ch	60ch	55ch	48ch	with output pin or input pin	64ch	55ch	47ch	40ch	with output pin	64ch	57ch	42ch	30ch	with input pin
Base timer	64ch	60ch		55ch	48ch																													
	64ch	55ch		47ch	40ch	with out pin																												
	64ch	57ch	42ch	30ch	with in pin																													
Base timer	64ch	60ch	55ch	48ch	with output pin or input pin																													
	64ch	55ch	47ch	40ch	with output pin																													
	64ch	57ch	42ch	30ch	with input pin																													
5	1. Features 1.1 Function List	Added as below: Error) <table><tr><td>External interrupt</td><td>32 ch</td><td></td></tr></table> Correct) <table><tr><td>External interrupt</td><td>32 ch</td><td>See the AC specification on this datasheet</td></tr></table>	External interrupt	32 ch		External interrupt	32 ch	See the AC specification on this datasheet																										
External interrupt	32 ch																																	
External interrupt	32 ch	See the AC specification on this datasheet																																
5	1. Features 1.1 Function List	Revised as below: Error) <table><tr><td rowspan="4">Multi-function serial interface</td><td>22 ch</td><td>13 ch</td><td>13 ch</td><td>13 ch</td><td>S6J34xD/E</td></tr><tr><td>14 ch</td><td>13 ch</td><td>13 ch</td><td>13 ch</td><td>S6J342B/C</td></tr><tr><td>14 ch</td><td>13 ch</td><td>13 ch</td><td>13 ch</td><td>S6J3428/9/A</td></tr><tr><td>14 ch</td><td>13 ch</td><td>13 ch</td><td>12 ch</td><td>with CS pin</td></tr></table> Correct) <table><tr><td rowspan="2">Multi-function serial interface</td><td>14 ch</td><td>13 ch</td><td>13 ch</td><td>13 ch</td><td>S6J3428/9/A</td></tr><tr><td>14 ch</td><td>13 ch</td><td>13 ch</td><td>12 ch</td><td>with CS pin</td></tr></table>	Multi-function serial interface	22 ch	13 ch	13 ch	13 ch	S6J34xD/E	14 ch	13 ch	13 ch	13 ch	S6J342B/C	14 ch	13 ch	13 ch	13 ch	S6J3428/9/A	14 ch	13 ch	13 ch	12 ch	with CS pin	Multi-function serial interface	14 ch	13 ch	13 ch	13 ch	S6J3428/9/A	14 ch	13 ch	13 ch	12 ch	with CS pin
Multi-function serial interface	22 ch	13 ch		13 ch	13 ch	S6J34xD/E																												
	14 ch	13 ch		13 ch	13 ch	S6J342B/C																												
	14 ch	13 ch		13 ch	13 ch	S6J3428/9/A																												
	14 ch	13 ch	13 ch	12 ch	with CS pin																													
Multi-function serial interface	14 ch	13 ch	13 ch	13 ch	S6J3428/9/A																													
	14 ch	13 ch	13 ch	12 ch	with CS pin																													
5	1. Features 1.1 Function List	Revised as below: Error) <table><tr><td>CAN-FD RAM (ECC supported)</td><td>16 KB/ch It is equivalent to 128 message buffer per channel of CAN module</td><td></td></tr></table> Correct) <table><tr><td>CAN-FD RAM (ECC supported)</td><td>16 KB/ch It is equivalent to 192 message buffer per channel of CAN module</td><td></td></tr></table>	CAN-FD RAM (ECC supported)	16 KB/ch It is equivalent to 128 message buffer per channel of CAN module		CAN-FD RAM (ECC supported)	16 KB/ch It is equivalent to 192 message buffer per channel of CAN module																											
CAN-FD RAM (ECC supported)	16 KB/ch It is equivalent to 128 message buffer per channel of CAN module																																	
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5	1. Features 1.1 Function List	Deleted as below: Error) <table><tr><td>FlexRay</td><td>Option</td><td>See Section 1.2.1</td></tr></table>	FlexRay	Option	See Section 1.2.1																													
FlexRay	Option	See Section 1.2.1																																

Page	Section	Change Results
5	1. Features 1.1 Function List	Deleted as below: Error) The details are described in 6 "Recommended Operating Conditions". Correct) The details are described in "Recommended Operating Conditions".

Page	Section	Change Results																																																																																						
6	1.2 Optional Function 1.2.1 Basic Option	Revised as below: Error) Option: <table><tr><td>Digit</td></tr><tr><td>S</td></tr><tr><td>T</td></tr><tr><td>U</td></tr><tr><td>V</td></tr></table> Memory size: <table><tr><th rowspan="2">Digit</th><th colspan="2">Flash</th><th colspan="2">RAM</th></tr><tr><th>Program</th><th>Work</th><th>Main</th><th>Back up</th></tr><tr><td>E</td><td>4,160 KB</td><td>112 KB</td><td>512 KB</td><td>48+16 KB</td></tr><tr><td>D</td><td>3,136 KB</td><td>112 KB</td><td>320 KB</td><td>48+16 KB</td></tr><tr><td>C</td><td>2,212 KB</td><td>112 KB</td><td>256 KB</td><td>16+8 KB</td></tr><tr><td>B</td><td>1,600 KB</td><td>112 KB</td><td>192 KB</td><td>16+8 KB</td></tr><tr><td>A</td><td>1,088 KB</td><td>112 KB</td><td>128 KB</td><td>8+4 KB</td></tr><tr><td>9</td><td>832 KB</td><td>112 KB</td><td>80 KB</td><td>8+4 KB</td></tr><tr><td>8</td><td>576 KB</td><td>112 KB</td><td>64 KB</td><td>8+4 KB</td></tr></table> Function: <table><tr><th>Digit</th><th>Flex Ray</th></tr><tr><td>1</td><td>Yes</td></tr><tr><td>2</td><td>-</td></tr></table> Correct) Option: <table><tr><td>Digit</td></tr><tr><td>S</td></tr><tr><td>U</td></tr><tr><td>T</td></tr><tr><td>V</td></tr></table> Memory size: <table><tr><th rowspan="2">Digit</th><th colspan="2">Flash</th><th colspan="2">RAM</th></tr><tr><th>Program</th><th>Work</th><th>Main</th><th>Back up</th></tr><tr><td>A</td><td>1,088 KB</td><td>112 KB</td><td>128 KB</td><td>8+4 KB</td></tr><tr><td>9</td><td>832 KB</td><td>112 KB</td><td>80 KB</td><td>8+4 KB</td></tr><tr><td>8</td><td>576 KB</td><td>112 KB</td><td>64 KB</td><td>8+4 KB</td></tr></table> Function: <table><tr><th>Digit</th></tr><tr><td>2</td></tr></table> Note: This table only shows the relation between the optional function and the part numbers; that is, all products are not necessarily available for orders. See the “Ordering Information” on this datasheet and confirm product availability.	Digit	S	T	U	V	Digit	Flash		RAM		Program	Work	Main	Back up	E	4,160 KB	112 KB	512 KB	48+16 KB	D	3,136 KB	112 KB	320 KB	48+16 KB	C	2,212 KB	112 KB	256 KB	16+8 KB	B	1,600 KB	112 KB	192 KB	16+8 KB	A	1,088 KB	112 KB	128 KB	8+4 KB	9	832 KB	112 KB	80 KB	8+4 KB	8	576 KB	112 KB	64 KB	8+4 KB	Digit	Flex Ray	1	Yes	2	-	Digit	S	U	T	V	Digit	Flash		RAM		Program	Work	Main	Back up	A	1,088 KB	112 KB	128 KB	8+4 KB	9	832 KB	112 KB	80 KB	8+4 KB	8	576 KB	112 KB	64 KB	8+4 KB	Digit	2
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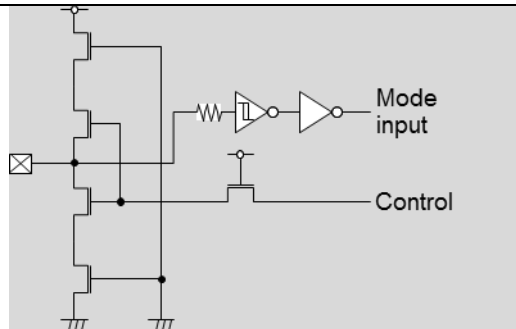
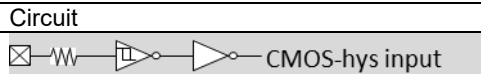
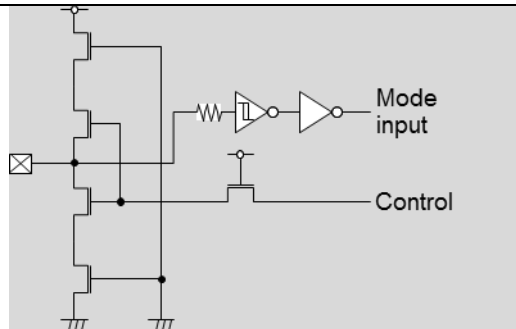
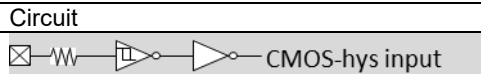
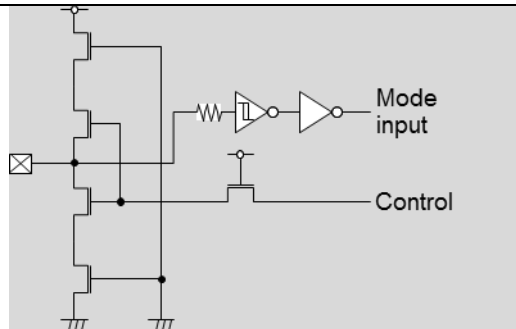
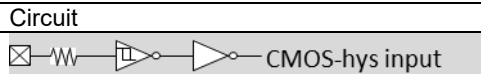
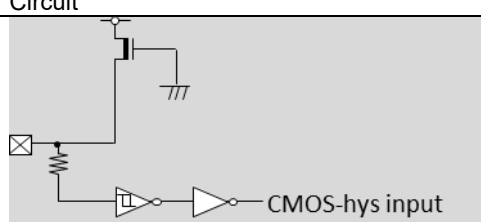
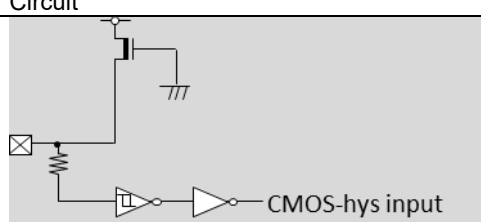
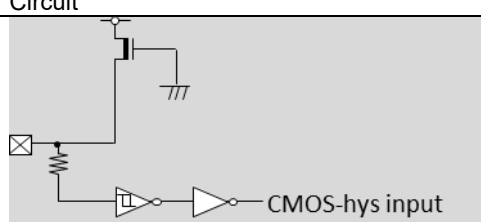
Page	Section	Change Results																																																								
6	1. Features 1.2.1 Basic Option	Revised as below: Error) See the order number on the datasheet and confirm product availability. Correct) See the “Ordering Information” on this datasheet and confirm product availability.																																																								
7	1. Features 1.2.2 ID	Added as below: Correct) ID is specified for each Memory size digit, Option digit and revision. <table><tr><th>Memory size</th><th>Option</th><th>Revision</th><th>Chip ID</th><th>JTAG ID</th><th>SHE Module ID (SHE_MID) *</th></tr><tr><td>A</td><td>S</td><td>A</td><td rowspan="12">0x10130100</td><td>0x002005CF</td><td rowspan="12">0x000F_0300</td></tr><tr><td>A</td><td>U</td><td>A</td><td>0x002015CF</td></tr><tr><td>A</td><td>T</td><td>A</td><td>0x002065CF</td></tr><tr><td>A</td><td>V</td><td>A</td><td>0x002075CF</td></tr><tr><td>9</td><td>S</td><td>A</td><td>0x002025CF</td></tr><tr><td>9</td><td>U</td><td>A</td><td>0x002035CF</td></tr><tr><td>9</td><td>T</td><td>A</td><td>0x002085CF</td></tr><tr><td>9</td><td>V</td><td>A</td><td>0x002095CF</td></tr><tr><td>8</td><td>S</td><td>A</td><td>0x002045CF</td></tr><tr><td>8</td><td>U</td><td>A</td><td>0x002055CF</td></tr><tr><td>8</td><td>T</td><td>A</td><td>0x0020A5CF</td></tr><tr><td>8</td><td>V</td><td>A</td><td>0x0020B5CF</td></tr></table> * Refer to "SHE Module ID Register" of the chapter of "Secure Hardware Extension (SHE)" in TRAVEO™ T1G Platform hardware manual for details.	Memory size	Option	Revision	Chip ID	JTAG ID	SHE Module ID (SHE_MID) *	A	S	A	0x10130100	0x002005CF	0x000F_0300	A	U	A	0x002015CF	A	T	A	0x002065CF	A	V	A	0x002075CF	9	S	A	0x002025CF	9	U	A	0x002035CF	9	T	A	0x002085CF	9	V	A	0x002095CF	8	S	A	0x002045CF	8	U	A	0x002055CF	8	T	A	0x0020A5CF	8	V	A	0x0020B5CF
Memory size	Option	Revision	Chip ID	JTAG ID	SHE Module ID (SHE_MID) *																																																					
A	S	A	0x10130100	0x002005CF	0x000F_0300																																																					
A	U	A		0x002015CF																																																						
A	T	A		0x002065CF																																																						
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8	S	A		0x002045CF																																																						
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8	T	A		0x0020A5CF																																																						
8	V	A		0x0020B5CF																																																						

Page	Section	Change Results			
8	1. Features 1.2.4 Restriction	Revised as below:			
		Error)			
		Function	TEQFP144 LQFP144	TEQFP120 LQFP120	TEQFP100 LQFP100
		Analog input port (12bit-ADC)	AN001 to 002, AN007, AN012, AN015 to 016, AN023 to 024 (56 ports)	AN001 to 002, AN006 to 007, AN009, AN011 to 012, AN015 to 016, AN020, AN023 to 024, AN031, AN103, AN116, AN122, AN126, AN130 to 131 (45 ports)	AN001 to 002, AN004, AN006 to 007, AN009, AN011 to 012, AN015 to 016, AN018, AN020, AN023 to 024, AN026, AN029, AN031, AN101, AN103 to 105, AN116 to 117, AN122, AN124, AN126, AN130 to 131 (35 ports)
		Correct)			
		Function	TEQFP144 LQFP144	TEQFP120 LQFP120	TEQFP100 LQFP100
		Analog input port (12bit-ADC)	AN001 to 002, AN007, AN012, AN015 to 016, AN023 to 024 (56 ports)	AN001 to 002, AN006 to 007, AN009, AN011 to 012, AN015 to 016, AN020, AN023 to 024, AN031, AN103, AN116, AN122, AN126, AN130 to 131 (45 ports)	AN001 to 002, AN004, AN006 to 007, AN009, AN011 to 012, AN015 to 016, AN018, AN020, AN023 to 024, AN026, AN029, AN031, AN101, AN103 to 105, AN115 to 117, AN122, AN124, AN126, AN130 to 131 (35 ports)

Page	Section	Change Results			
9	1. Features 1.2.4 Restriction	Revised as below:			
		Error)			
		Function	TEQFP144 LQFP144	TEQFP120 LQFP120	TEQFP100 LQFP100
		BaseTimer	TIOA0/1/2/3_1 TIOA14/15/16/17/18_0 TIOA21/25/26/27_1 TIOA51/57/58/59/61_0 TIOB56/57/58/59/60/61/62_0	TIOA0/1/2/3_1 TIOA9/10/13_1 TIOA8/14/15/16/17/18/19_0 TIOB0/5/10/12_0 TIOA27_0 TIOA21/23/25/26/27_1 TIOA51/53/56/57/58/59/60_0 TIOA61/62/63_0 TIOB24/26/29/33/37/38_0 TIOB43/48/49_0 TIOB51/56/57/58/59/60_0 TIOB61/62/63_0	TIOA0/1_0 TIOA0/1/2/3/5_1 TIOA9/10/13_1 TIOA7/8/14/15/16/17/18/19_0 TIOB0/4/5/8/10/12_0 TIOB14/15/19/21/22/23_0 TIOA26/27/28_0 TIOA21/23/25/26/27/28_1 TIOA49/51/53/56/57/58/59/60_0 TIOA61/62/63_0 TIOB24/29/33/35/37/38_0 TIOB43/44/46/47/48/49_0 TIOB51/53/56/57/58/59/60_0 TIOB61/62/63_0
		Correct)			
Function	TEQFP144 LQFP144	TEQFP120 LQFP120	TEQFP100 LQFP100		
BaseTimer	TIOA0/1/2/3_1 TIOA14/15/16/17/18_0 TIOA21/25/26/27_1 TIOA51/57/58/59/61_0 TIOB56/57/58/59/60/61/62_0	TIOA0/1/2/3_1 TIOA9/10/13_1 TIOA8/14/15/16/17/18/19_0 TIOB0/5/10/12_0 TIOA27_0 TIOA21/23/25/26/27_1 TIOA51/53/56/57/58/59/60_0 TIOA61/62/63_0 TIOB24/25/29/33/37/38_0 TIOB43/48/49_0 TIOB51/56/57/58/59/60_0 TIOB61/62/63_0	TIOA0/1_0 TIOA0/1/2/3/5_1 TIOA9/10/13_1 TIOA7/8/14/15/16/17/18/19_0 TIOB0/4/5/8/10/12_0 TIOB14/15/19/22/23_0 TIOA21/26/27/28_0 TIOA21/23/25/26/27/28_1 TIOA49/51/53/56/57/58/59/60_0 TIOA61/62/63_0 TIOB24/25/29/33/35/37/38_0 TIOB43/44/46/47/48/49_0 TIOB51/53/56/57/58/59/60_0 TIOB61/62/63_0		

Page	Section	Change Results																
9	1. Features 1.2.4 Restriction	Revised as below: Error) <table><tr><th>Function</th><th>TEQFP144 LQFP144</th><th>TEQFP120 LQFP120</th><th>TEQFP100 LQFP100</th></tr><tr><td>FRT</td><td>TEXT6_0</td><td>TEXT0/6_0</td><td>TEXT0/2/3/6_0</td></tr></table> Correct) <table><tr><th>Function</th><th>TEQFP144 LQFP144</th><th>TEQFP120 LQFP120</th><th>TEQFP100 LQFP100</th></tr><tr><td>FRT</td><td>TEXT10_0</td><td>TEXT0/10_0</td><td>TEXT0/2/3/10_0, TEXT1/4_1</td></tr></table>	Function	TEQFP144 LQFP144	TEQFP120 LQFP120	TEQFP100 LQFP100	FRT	TEXT6_0	TEXT0/6_0	TEXT0/2/3/6_0	Function	TEQFP144 LQFP144	TEQFP120 LQFP120	TEQFP100 LQFP100	FRT	TEXT10_0	TEXT0/10_0	TEXT0/2/3/10_0, TEXT1/4_1
Function	TEQFP144 LQFP144	TEQFP120 LQFP120	TEQFP100 LQFP100															
FRT	TEXT6_0	TEXT0/6_0	TEXT0/2/3/6_0															
Function	TEQFP144 LQFP144	TEQFP120 LQFP120	TEQFP100 LQFP100															
FRT	TEXT10_0	TEXT0/10_0	TEXT0/2/3/10_0, TEXT1/4_1															
9	1. Features 1.2.4 Restriction	Added as below: Correct) <table><tr><th>Function</th><th>TEQFP144 LQFP144</th><th>TEQFP120 LQFP120</th><th>TEQFP100 LQFP100</th></tr><tr><td>CAN-FD</td><td>-</td><td>TX0_0, RX1_1, TX1_1</td><td>TX0_0, RX1_1, TX1_1 TX2_1</td></tr><tr><td>Multi-function serial</td><td>SCS21_1, SCS23_0, SCS23_1, SCS40_1, SCS41_1, SCS52_0, SIN6_1, SOT6_1, SCS70_1, SCS72_1, SCS110_0, SIN12_0, SIN12_1, SOT12_1, SCK13_0, SIN13_0, SOT13_0, SCS130_0</td><td>SCK2_0, SIN2_0, SOT2_1, SCS21_0, SCS21_1, SCS22_1, SCS23_0, SCS23_1, SOT4_1, SCS40_1, SCS41_0, SCS41_1, SCS42_0, SCS50_1, SCS52_0, SIN6_1, SOT6_1, SCS60_2, SCS61_0, SCK7_1, SIN7_0, SIN7_2, SOT7_1, SCS70_1, SCS71_0, SCS71_1, SCS72_1, SCS73_0, SCK9_0, SCS102_0, SCS110_0, SIN12_0, SIN12_1, SOT12_1, SCK13_0, SIN13_0, SOT13_0, SCS130_0</td><td>SCS0_0, SCK2_0, SIN2_0, SIN2_1, SOT2_1, SCS21_0, SCS21_1, SCS22_0, SCS22_1, SCS23_0, SCS23_1, SCS30_0, SIN4_0, SIN4_1, SOT4_1, SCS40_1, SCS41_0, SCS41_1, SCS42_0, SCS43_0, SCS43_1, SCS50_1, SCS52_0, SIN6_1, SOT6_1, SCS60_2, SCS61_0, SCK7_1, SIN7_0, SIN7_2, SOT7_1, SCS70_1, SCS71_0, SCS71_1, SCS72_1, SCS73_0, SIN8_0, SCS83_0, SCK9_0, SOT9_0, SCS90_1, SCS101_0, SCS102_0, SCS103_0, SOT11_1, SCS110_0, SCK12_0, SIN12_0, SIN12_1, SOT12_1, SCS120_1, SCK13_0, SIN13_0, SOT13_0, SCS130_0</td></tr></table>	Function	TEQFP144 LQFP144	TEQFP120 LQFP120	TEQFP100 LQFP100	CAN-FD	-	TX0_0, RX1_1, TX1_1	TX0_0, RX1_1, TX1_1 TX2_1	Multi-function serial	SCS21_1, SCS23_0, SCS23_1, SCS40_1, SCS41_1, SCS52_0, SIN6_1, SOT6_1, SCS70_1, SCS72_1, SCS110_0, SIN12_0, SIN12_1, SOT12_1, SCK13_0, SIN13_0, SOT13_0, SCS130_0	SCK2_0, SIN2_0, SOT2_1, SCS21_0, SCS21_1, SCS22_1, SCS23_0, SCS23_1, SOT4_1, SCS40_1, SCS41_0, SCS41_1, SCS42_0, SCS50_1, SCS52_0, SIN6_1, SOT6_1, SCS60_2, SCS61_0, SCK7_1, SIN7_0, SIN7_2, SOT7_1, SCS70_1, SCS71_0, SCS71_1, SCS72_1, SCS73_0, SCK9_0, SCS102_0, SCS110_0, SIN12_0, SIN12_1, SOT12_1, SCK13_0, SIN13_0, SOT13_0, SCS130_0	SCS0_0, SCK2_0, SIN2_0, SIN2_1, SOT2_1, SCS21_0, SCS21_1, SCS22_0, SCS22_1, SCS23_0, SCS23_1, SCS30_0, SIN4_0, SIN4_1, SOT4_1, SCS40_1, SCS41_0, SCS41_1, SCS42_0, SCS43_0, SCS43_1, SCS50_1, SCS52_0, SIN6_1, SOT6_1, SCS60_2, SCS61_0, SCK7_1, SIN7_0, SIN7_2, SOT7_1, SCS70_1, SCS71_0, SCS71_1, SCS72_1, SCS73_0, SIN8_0, SCS83_0, SCK9_0, SOT9_0, SCS90_1, SCS101_0, SCS102_0, SCS103_0, SOT11_1, SCS110_0, SCK12_0, SIN12_0, SIN12_1, SOT12_1, SCS120_1, SCK13_0, SIN13_0, SOT13_0, SCS130_0				
Function	TEQFP144 LQFP144	TEQFP120 LQFP120	TEQFP100 LQFP100															
CAN-FD	-	TX0_0, RX1_1, TX1_1	TX0_0, RX1_1, TX1_1 TX2_1															
Multi-function serial	SCS21_1, SCS23_0, SCS23_1, SCS40_1, SCS41_1, SCS52_0, SIN6_1, SOT6_1, SCS70_1, SCS72_1, SCS110_0, SIN12_0, SIN12_1, SOT12_1, SCK13_0, SIN13_0, SOT13_0, SCS130_0	SCK2_0, SIN2_0, SOT2_1, SCS21_0, SCS21_1, SCS22_1, SCS23_0, SCS23_1, SOT4_1, SCS40_1, SCS41_0, SCS41_1, SCS42_0, SCS50_1, SCS52_0, SIN6_1, SOT6_1, SCS60_2, SCS61_0, SCK7_1, SIN7_0, SIN7_2, SOT7_1, SCS70_1, SCS71_0, SCS71_1, SCS72_1, SCS73_0, SCK9_0, SCS102_0, SCS110_0, SIN12_0, SIN12_1, SOT12_1, SCK13_0, SIN13_0, SOT13_0, SCS130_0	SCS0_0, SCK2_0, SIN2_0, SIN2_1, SOT2_1, SCS21_0, SCS21_1, SCS22_0, SCS22_1, SCS23_0, SCS23_1, SCS30_0, SIN4_0, SIN4_1, SOT4_1, SCS40_1, SCS41_0, SCS41_1, SCS42_0, SCS43_0, SCS43_1, SCS50_1, SCS52_0, SIN6_1, SOT6_1, SCS60_2, SCS61_0, SCK7_1, SIN7_0, SIN7_2, SOT7_1, SCS70_1, SCS71_0, SCS71_1, SCS72_1, SCS73_0, SIN8_0, SCS83_0, SCK9_0, SOT9_0, SCS90_1, SCS101_0, SCS102_0, SCS103_0, SOT11_1, SCS110_0, SCK12_0, SIN12_0, SIN12_1, SOT12_1, SCS120_1, SCK13_0, SIN13_0, SOT13_0, SCS130_0															

Page	Section	Change Results																												
10	1. Features 1.2.4 Restriction	Added as below: Correct) <table><thead><tr><th>Function</th><th>TEQFP144 LQFP144</th><th>TEQFP120 LQFP120</th><th>TEQFP100 LQFP100</th></tr></thead><tbody><tr><td>I²C</td><td>SCL13_0, SDA13_0</td><td>SCL2_0, SCL9_0, SCL13_0, SDA13_0</td><td>SCL2_0, SCL9_0, SDA9_0, SCL12_0, SCL13_0, SDA13_0</td></tr><tr><td>Input capture</td><td>-</td><td>IN2_1, IN2_2, IN16_1</td><td>IN2/3_0, IN0/2_1, IN0/2_2, IN19/20_0, IN16/20_1</td></tr><tr><td>Output compare</td><td>-</td><td>OUT2_0, OUT5_1, OUT20/21_0</td><td>OUT1/2/3_0, OUT2/5_1, OUT19/20/21_0</td></tr><tr><td>Quad Position & Revolution Counter</td><td>-</td><td>AIN8_0, ZIN8_0</td><td>AIN8_0, AIN8_1, ZIN8_0</td></tr><tr><td>Reload timer</td><td>-</td><td>TOT3_0, TOT16_0, TOT17_0</td><td>TOT2_0, TOT3_0, TOT16_0, TOT17_0</td></tr><tr><td>Trace</td><td>-</td><td>TRACEDATA4/5/7_0</td><td>TRACECTL_0, TRACEDATA0/1/3/4/5/7_0</td></tr></tbody></table>	Function	TEQFP144 LQFP144	TEQFP120 LQFP120	TEQFP100 LQFP100	I ² C	SCL13_0, SDA13_0	SCL2_0, SCL9_0, SCL13_0, SDA13_0	SCL2_0, SCL9_0, SDA9_0, SCL12_0, SCL13_0, SDA13_0	Input capture	-	IN2_1, IN2_2, IN16_1	IN2/3_0, IN0/2_1, IN0/2_2, IN19/20_0, IN16/20_1	Output compare	-	OUT2_0, OUT5_1, OUT20/21_0	OUT1/2/3_0, OUT2/5_1, OUT19/20/21_0	Quad Position & Revolution Counter	-	AIN8_0, ZIN8_0	AIN8_0, AIN8_1, ZIN8_0	Reload timer	-	TOT3_0, TOT16_0, TOT17_0	TOT2_0, TOT3_0, TOT16_0, TOT17_0	Trace	-	TRACEDATA4/5/7_0	TRACECTL_0, TRACEDATA0/1/3/4/5/7_0
Function	TEQFP144 LQFP144	TEQFP120 LQFP120	TEQFP100 LQFP100																											
I ² C	SCL13_0, SDA13_0	SCL2_0, SCL9_0, SCL13_0, SDA13_0	SCL2_0, SCL9_0, SDA9_0, SCL12_0, SCL13_0, SDA13_0																											
Input capture	-	IN2_1, IN2_2, IN16_1	IN2/3_0, IN0/2_1, IN0/2_2, IN19/20_0, IN16/20_1																											
Output compare	-	OUT2_0, OUT5_1, OUT20/21_0	OUT1/2/3_0, OUT2/5_1, OUT19/20/21_0																											
Quad Position & Revolution Counter	-	AIN8_0, ZIN8_0	AIN8_0, AIN8_1, ZIN8_0																											
Reload timer	-	TOT3_0, TOT16_0, TOT17_0	TOT2_0, TOT3_0, TOT16_0, TOT17_0																											
Trace	-	TRACEDATA4/5/7_0	TRACECTL_0, TRACEDATA0/1/3/4/5/7_0																											
45	5.2 I/O Circuit Type	Revised as below for Type E: Error) <table><thead><tr><th>Remark</th></tr></thead><tbody><tr><td> - JTAG_TDI - General-purpose output port - Output 1 mA, 2 mA, or 5 mA selectable (in the case of GPIO) - 50 kΩ with pull-up resistor control - TTL hysteresis input </td></tr></tbody></table> Correct) <table><thead><tr><th>Remark</th></tr></thead><tbody><tr><td> - JTAG_TDI / JTAG_TMS - General-purpose output port - Output 1mA, 2mA or 5mA selectable (In the case of GPIO) - Output 5mA (In the case of Serial Wire Debugger) - 50kΩ with pull-up resistor control - TTL hvsteresis input </td></tr></tbody></table>	Remark	- JTAG_TDI - General-purpose output port - Output 1 mA, 2 mA, or 5 mA selectable (in the case of GPIO) - 50 kΩ with pull-up resistor control - TTL hysteresis input	Remark	- JTAG_TDI / JTAG_TMS - General-purpose output port - Output 1mA, 2mA or 5mA selectable (In the case of GPIO) - Output 5mA (In the case of Serial Wire Debugger) - 50kΩ with pull-up resistor control - TTL hvsteresis input																								
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Remark																														
- JTAG_TDI / JTAG_TMS - General-purpose output port - Output 1mA, 2mA or 5mA selectable (In the case of GPIO) - Output 5mA (In the case of Serial Wire Debugger) - 50kΩ with pull-up resistor control - TTL hvsteresis input																														

Page	Section	Change Results												
45	5.2 I/O Circuit Type	Revised as below for Type G: Error) <table><tr><th>Remark</th></tr><tr><td> - JTAG_TCK/TMS - 50 kΩ with pull-up resistor - TTL hysteresis input </td></tr></table> Correct) <table><tr><th>Remark</th></tr><tr><td> - JTAG_TCK - 50kΩ with pull-up resistor - TTL hysteresis input </td></tr></table>	Remark	- JTAG_TCK/TMS - 50 kΩ with pull-up resistor - TTL hysteresis input	Remark	- JTAG_TCK - 50kΩ with pull-up resistor - TTL hysteresis input								
Remark														
- JTAG_TCK/TMS - 50 kΩ with pull-up resistor - TTL hysteresis input														
Remark														
- JTAG_TCK - 50kΩ with pull-up resistor - TTL hysteresis input														
46	5.2 I/O Circuit Type	Revised as below for Type I: Error) <table><tr><th>Type</th><th>Circuit</th><th>Remark</th></tr><tr><td>I</td><td></td><td> - MD input - CMOS hysteresis input </td></tr></table> Correct) <table><tr><th>Type</th><th>Circuit</th><th>Remark</th></tr><tr><td>I</td><td></td><td> - MD input - CMOS hysteresis input </td></tr></table>	Type	Circuit	Remark	I		- MD input - CMOS hysteresis input	Type	Circuit	Remark	I		- MD input - CMOS hysteresis input
Type	Circuit	Remark												
I		- MD input - CMOS hysteresis input												
Type	Circuit	Remark												
I		- MD input - CMOS hysteresis input												
46	5.2 I/O Circuit Type	Revised as below for Type K: Correct) <table><tr><th>Type</th><th>Circuit</th><th>Remark</th></tr><tr><td>K</td><td></td><td> - NIMIX input - 50kΩ with pull-up resistor - CMOS hysteresis input </td></tr></table>	Type	Circuit	Remark	K		- NIMIX input - 50kΩ with pull-up resistor - CMOS hysteresis input						
Type	Circuit	Remark												
K		- NIMIX input - 50kΩ with pull-up resistor - CMOS hysteresis input												
46	5.2 I/O Circuit Type	Revised as below: Error) <table><tr><th>Type</th></tr><tr><td>K</td></tr></table> Correct) <table><tr><th>Type</th></tr><tr><td>L</td></tr></table>	Type	K	Type	L								
Type														
K														
Type														
L														

Page	Section	Change Results				
47	5.2 I/O Circuit Type	Revised as below: Error)<table><tr><td>Type</td></tr><tr><td>L</td></tr></table> Correct)<table><tr><td>Type</td></tr><tr><td>M</td></tr></table>	Type	L	Type	M
Type						
L						
Type						
M						
51	7.2 Recommended Operating Conditions	Delete the following sentence: Error) *1: When it is used outside recommended range (this is the range of guaranteed operation), contact your sales representative. Detection voltage of the external low voltage detection reset (initial) is 2.6V±3.5%.This detection voltage level setting is below the minimum operation assurance voltage (2.7V). Between this detection voltage and the minimum operation assurance voltage, MCU functions are not guaranteed except for the low voltage detector. Note that although the detection level is below the minimum operation guarantee voltage, the LVD reset factor flag is set as the voltage drops below the detection level. Correct) *1: When it is used outside recommended range (this is the range of guaranteed operation), contact your sales representative. Detection voltage of the external low voltage detection reset (initial) is 2.6V±3.5%.This detection voltage level setting is below the minimum operation assurance voltage (2.7V). Between this detection voltage and the minimum operation assurance voltage, MCU functions are not guaranteed except for the low voltage detector.				
55, 56	7. Electrical Characteristics 7.3 DC Characteristics	Revised as below: Error) *3: Corresponding mode sets for state definitions are described in Chapter 12: State Transition of the S6J3400 Series hardware manual Correct) *3: Corresponding mode sets for state definitions are described in the chapter of “State Transition” in S6J3400 Series hardware manual				
59	7. Electrical Characteristics 7.4.3 Internal Clock Timing	Revised as below: Error) ■ In the Symbol column, same clock names as described in Chapter 5: Clock System of the platform hardware manual are used. Correct) ■ In the Symbol column, same clock names as described in the chapter of “Clock System” in Traveo™ Platform hardware manual are used.				

Page	Section	Change Results																																																
59	7. Electrical Characteristics 7.4.3 Internal Clock Timing	Revised as below: Error) ■ Corresponding functions for these clocks are described in Chapter 5: Clock Configuration of the S6J3400 series hardware manual. Correct) ■ Corresponding functions for these clocks are described in the chapter of “Clock Configuration” in S6J3400 series hardware manual.																																																
59	7. Electrical Characteristics 7.4.3 Internal Clock Timing	Revised as below: Error) <table><tr><th>Symbol</th><th>Pin Name</th><th>Conditions</th><th>Min</th><th>Typ</th><th>Max *1</th><th>Max *2</th><th>Unit</th></tr><tr><td>fSSCG0</td><td>-</td><td>-</td><td>-</td><td>-</td><td>264</td><td>320</td><td>MHz</td></tr><tr><td>fPLL0</td><td>-</td><td>-</td><td>-</td><td>-</td><td>288</td><td>288</td><td>MHz</td></tr></table> Correct) <table><tr><th>Symbol</th><th>Pin Name</th><th>Conditions</th><th>Min</th><th>Typ</th><th>Max *1</th><th>Max *2</th><th>Unit</th></tr><tr><td>fSSCG0out</td><td>-</td><td>-</td><td>200</td><td>-</td><td>320</td><td>320</td><td>MHz</td></tr><tr><td>fPLL0out</td><td>-</td><td>-</td><td>200</td><td>-</td><td>320</td><td>320</td><td>MHz</td></tr></table>	Symbol	Pin Name	Conditions	Min	Typ	Max *1	Max *2	Unit	fSSCG0	-	-	-	-	264	320	MHz	fPLL0	-	-	-	-	288	288	MHz	Symbol	Pin Name	Conditions	Min	Typ	Max *1	Max *2	Unit	fSSCG0out	-	-	200	-	320	320	MHz	fPLL0out	-	-	200	-	320	320	MHz
Symbol	Pin Name	Conditions	Min	Typ	Max *1	Max *2	Unit																																											
fSSCG0	-	-	-	-	264	320	MHz																																											
fPLL0	-	-	-	-	288	288	MHz																																											
Symbol	Pin Name	Conditions	Min	Typ	Max *1	Max *2	Unit																																											
fSSCG0out	-	-	200	-	320	320	MHz																																											
fPLL0out	-	-	200	-	320	320	MHz																																											
64, 66, 68, 70	7. Electrical Characteristics 7.4.6 Multi-Function Serial	Revised as below: Error) <table><tr><th>Conditions</th></tr><tr><td>Master Mode (CL = 50pF, IOL = -2mA, IOH = 2mA), (CL = 20pF, IOL = -1mA, IOH = 1mA)</td></tr><tr><td>Slave Mode (CL = 50pF, IOL = -2mA, IOH = 2mA), (CL = 20pF, IOL = -1mA, IOH = 1mA)</td></tr></table> Correct) <table><tr><th>Conditions</th></tr><tr><td>Master Mode (CL = 20pF, IOL = -2mA, IOH = 2mA)</td></tr><tr><td>Slave Mode (CL = 20pF, IOL = -2mA, IOH = 2mA)</td></tr></table>	Conditions	Master Mode (CL = 50pF, IOL = -2mA, IOH = 2mA), (CL = 20pF, IOL = -1mA, IOH = 1mA)	Slave Mode (CL = 50pF, IOL = -2mA, IOH = 2mA), (CL = 20pF, IOL = -1mA, IOH = 1mA)	Conditions	Master Mode (CL = 20pF, IOL = -2mA, IOH = 2mA)	Slave Mode (CL = 20pF, IOL = -2mA, IOH = 2mA)																																										
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72, 74, 76, 78	7. Electrical Characteristics 7.4.6 Multi-Function Serial	Revised as below: Error) <table><tr><th>Conditions</th></tr><tr><td>Master Mode (CL = 50pF, IOL = -2mA, IOH = 2mA), (CL = 20pF, IOL = -1mA, IOH = 1mA)</td></tr><tr><td>Slave Mode (CL = 50pF, IOL = -2mA, IOH = 2mA), (CL = 20pF, IOL = -1mA, IOH = 1mA)</td></tr><tr><td>Master Mode round operation (CL = 50pF, IOL = -2mA, IOH = 2mA), (CL = 20pF, IOL = -1mA, IOH = 1mA)</td></tr></table> Correct) <table><tr><th>Conditions</th></tr><tr><td>Master Mode (CL = 20pF, IOL = -2mA, IOH = 2mA)</td></tr><tr><td>Slave Mode (CL = 20pF, IOL = -2mA, IOH = 2mA)</td></tr><tr><td>Master Mode round operation (CL = 20pF, IOL = -2mA, IOH = 2mA)</td></tr></table>	Conditions	Master Mode (CL = 50pF, IOL = -2mA, IOH = 2mA), (CL = 20pF, IOL = -1mA, IOH = 1mA)	Slave Mode (CL = 50pF, IOL = -2mA, IOH = 2mA), (CL = 20pF, IOL = -1mA, IOH = 1mA)	Master Mode round operation (CL = 50pF, IOL = -2mA, IOH = 2mA), (CL = 20pF, IOL = -1mA, IOH = 1mA)	Conditions	Master Mode (CL = 20pF, IOL = -2mA, IOH = 2mA)	Slave Mode (CL = 20pF, IOL = -2mA, IOH = 2mA)	Master Mode round operation (CL = 20pF, IOL = -2mA, IOH = 2mA)																																								
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Page	Section	Change Results												
87	7.4.11 Low Voltage Detection (External Voltage)	Delete the following sentence: Error) *3: This detection voltage level setting is below the minimum operation assurance voltage (2.7V). Between this detection voltage and the minimum operation assurance voltage, MCU functions are not guaranteed except for the low voltage detector. Note that although the detection level is below the minimum operation guarantee voltage, the LVD reset factor flag is set as the voltage drops below the detection level. Correct) *3: This detection voltage level setting is below the minimum operation assurance voltage (2.7V). Between this detection voltage and the minimum operation assurance voltage, MCU functions are not guaranteed except for the low voltage detector.												
88	7.4.12.2 Low-voltage Detection (internal low-voltage detection for LVDL1)	Delete the following sentence: Error) *2: This detection voltage level setting is below the minimum operation voltage. Between this detection voltage and the minimum operation voltage, MCU functions are not guaranteed except for the low voltage detector. Note that although the detection level is below the minimum operation guarantee voltage, the LVD reset factor flag is set as the voltage drops below the detection level. Correct) *2: This detection voltage level setting is below the minimum operation voltage. Between this detection voltage and the minimum operation voltage, MCU functions are not guaranteed except for the low voltage detector.												
89, 90	7. Electrical Characteristics 7.5.1 Electrical Characteristics	Revised as below: Error) <table><tr><td>Pin Name</td></tr><tr><td>AVRH0/AVRH1</td></tr></table> Correct) <table><tr><td>Pin Name</td></tr><tr><td>AVRH0, AVRH1</td></tr></table> Revised as below: Error) <table><tr><td>Pin Name</td></tr><tr><td>AVCC</td></tr></table> Correct) <table><tr><td>Pin Name</td></tr><tr><td>AVCC0, AVCC1</td></tr></table> Revised as below: Error) <table><tr><td>Pin Name</td></tr><tr><td>AVRH</td></tr></table> Correct) <table><tr><td>Pin Name</td></tr><tr><td>AVRH0, AVRH1</td></tr></table>	Pin Name	AVRH0/AVRH1	Pin Name	AVRH0, AVRH1	Pin Name	AVCC	Pin Name	AVCC0, AVCC1	Pin Name	AVRH	Pin Name	AVRH0, AVRH1
Pin Name														
AVRH0/AVRH1														
Pin Name														
AVRH0, AVRH1														
Pin Name														
AVCC														
Pin Name														
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94	7. Electrical Characteristics 7.6.2 Notes	The following sentences modified as below. Error) While the Flash memory is written or erased, shutdown of the external power (Vcc5) is prohibited. In application systems where Vcc5 may be shut down while writing or erasing, be sure to turn the power off by using an external voltage detection function. In other words, after the external power supply voltage falls below the detection voltage (VDL), hold Vcc5 at 2.7 V or more within the duration calculated by the following expression: Correct) While the Flash memory is written or erased, shutdown of the external power (Vcc) is prohibited. In application systems where Vcc may be shut down while writing or erasing, be sure to turn the power off by using an external voltage detection function. In other words, after the external power supply voltage falls below the detection voltage (VDL), hold Vcc at 2.7 V or more within the duration calculated by the following expression:																								
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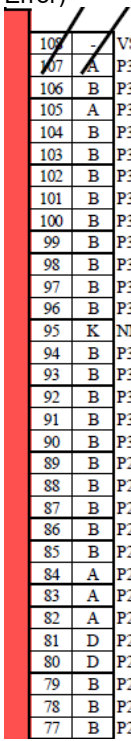
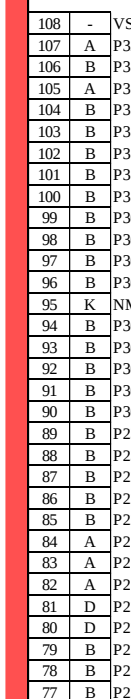
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1	Features Key Features	Revised as below Error) ■ 132-MHz operation frequency for S6J3428/9/A ■ 80-MHz internal flash memory access speed Correct) ■ 132 MHz operation frequency for S6J3428/9/A ■ 80 MHz internal Program flash memory access speed																																	
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51	7. Electrical Characteristics 7.2 Recommended Operating Conditions	Added Warning comment as below: Error) WARNING: ■ No guarantee is made with respect to any use, operating conditions, or combinations not represented on this datasheet. If you want to operate the application under any condition other than listed herein, contact the sales representatives. Correct) WARNING: ■ No guarantee is made with respect to any use, operating conditions, or combinations not represented on this datasheet. If you want to operate the application under any condition other than listed herein, contact the sales representatives. ■ The power-on sequence is as follows. Simultaneously turn on the digital supply voltage (VCC) and analog supply voltages (AVCC0, AVCC1, AVRH0, AVRH1), or turn on the digital supply voltage (VCC) and then the analog supply voltages (AVCC0, AVCC1, AVRH0, AVRH1). Be careful that analog power supplies (AVCC0, AVCC1, AVRH0, and AVRH1) and analog inputs do not exceed the digital power supply (VCC) at the analog system power-on and power-off times.																		
87	7. Electrical Characteristics 7.4.12.1 Low-voltage Detection (RAM retention low-voltage detection for LVDL0)	Revised as below Error) <table><tr><td>Hysteresis width</td><td>V_{RHYS}</td><td>-</td><td>-</td><td>-</td><td>100</td><td>-</td><td>mV</td><td>When power-supply voltage rises</td></tr></table> Correct) <table><tr><td>Hysteresis width</td><td>V_{RHYS}</td><td>-</td><td>-</td><td>-</td><td>75</td><td>-</td><td>mV</td><td>When power-supply voltage rises</td></tr></table>	Hysteresis width	V _{RHYS}	-	-	-	100	-	mV	When power-supply voltage rises	Hysteresis width	V _{RHYS}	-	-	-	75	-	mV	When power-supply voltage rises
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89	7. Electrical Characteristics 7.5.1 Electrical Characteristics	Revised as below Error) (T_A: Recommended operating conditions, V_{CC}=5.0 V ± 0.5 V, V_{SS}=AV_{SS}=0.0 V) Correct) (T_A: Recommended operating conditions, V_{CC}=AV_{CC}=5.0 V ± 0.5 V, V_{SS}=AV_{SS}=0.0 V)																		
90	7. Electrical Characteristics 7.5.1 Electrical Characteristics	Revised as below Error) (T_A: Recommended operating conditions, V_{CC}=3.3 V ± 0.3 V, V_{SS}=AV_{SS}=0.0 V) Correct) (T_A: Recommended operating conditions, V_{CC}=AV_{CC}=3.3 V ± 0.3 V, V_{SS}=AV_{SS}=0.0 V)																		
98	8. Ordering Information	Revised as below Error) For LQFP120/TEQFP120/LQFP144(0.4mm pitch)/LQFP176 package product, contact your sales representative. Correct) For LQFP120/TEQFP120/LQFP144(0.4mm pitch)/TEQFP144(0.4mm pitch)/LQFP176 package product, contact your sales representative.																		

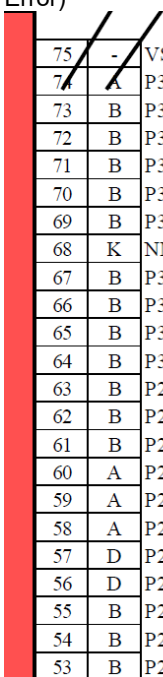
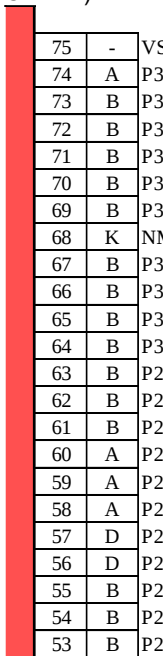
Page	Section	Change Results																																																								
Rev. *G																																																										
-	10.Errata	Deleted the Errata section. Regarding the contents of Errata, it moved as a Note for Interrupt Mask Function restriction of 32-bit Free-Run Timer to TRM 002-09919_Rev.C.																																																								
1	Features Key Features	The following sentences deleted. Error) ■ Low standby current in Partial Wake Up mode																																																								
5	1.Features 1.1 Function List	Deleted as below. Error) <table><tr><td>Function</td><td>S6J34xxJxx</td><td>S6J34xxHxx</td><td>S6J34xxGxx</td><td>S6J34xxFxx</td><td>Remark</td></tr><tr><td>Partial Wake Up</td><td>Analog input 8ch</td><td>Analog input 8ch</td><td>Analog input 8ch</td><td>Analog input 7ch</td><td>Trigger 1ch</td></tr></table>	Function	S6J34xxJxx	S6J34xxHxx	S6J34xxGxx	S6J34xxFxx	Remark	Partial Wake Up	Analog input 8ch	Analog input 8ch	Analog input 8ch	Analog input 7ch	Trigger 1ch																																												
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6	1. Features 1.2 Optional Function 1.2.1 Basic Option	Revised as below: Memory size Error) <table><tr><td rowspan="2">Dight</td><td colspan="2">Flash</td><td colspan="2">RAM</td></tr><tr><td>Program</td><td>Work</td><td>Main</td><td>Buck up</td></tr><tr><td>A</td><td>1,088 KB</td><td>112 KB</td><td>128 KB</td><td>8+4 KB</td></tr><tr><td>9</td><td>832 KB</td><td>112 KB</td><td>80 KB</td><td>8+4 KB</td></tr><tr><td>8</td><td>576 KB</td><td>112 KB</td><td>64 KB</td><td>8+4 KB</td></tr></table> Correct) <table><tr><td rowspan="2">Dight</td><td colspan="2">Flash</td><td colspan="3">RAM</td></tr><tr><td>Program</td><td>Work</td><td>TCRAM</td><td>SysRAM</td><td>Buck up</td></tr><tr><td>A</td><td>1,088 KB</td><td>112 KB</td><td>64 KB</td><td>64 KB</td><td>8+4 KB</td></tr><tr><td>9</td><td>832 KB</td><td>112 KB</td><td>32 KB</td><td>48 KB</td><td>8+4 KB</td></tr><tr><td>8</td><td>576 KB</td><td>112 KB</td><td>32 KB</td><td>32 KB</td><td>8+4 KB</td></tr></table>	Dight	Flash		RAM		Program	Work	Main	Buck up	A	1,088 KB	112 KB	128 KB	8+4 KB	9	832 KB	112 KB	80 KB	8+4 KB	8	576 KB	112 KB	64 KB	8+4 KB	Dight	Flash		RAM			Program	Work	TCRAM	SysRAM	Buck up	A	1,088 KB	112 KB	64 KB	64 KB	8+4 KB	9	832 KB	112 KB	32 KB	48 KB	8+4 KB	8	576 KB	112 KB	32 KB	32 KB	8+4 KB			
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7	1. Features 1.2 Optional Function 1.2.2 ID	Added the table as below: <table><tr><td>Memory size</td><td>Option</td><td>Revision</td><td>Chip ID</td><td>JTAG ID</td><td>SHE Module ID (SHE_MID) *</td></tr><tr><td>A</td><td>S</td><td>B</td><td rowspan="12">0x10130100</td><td>0x102005CF</td><td rowspan="12">0x000F_0300</td></tr><tr><td>A</td><td>U</td><td>B</td><td>0x102015CF</td></tr><tr><td>A</td><td>T</td><td>B</td><td>0x102065CF</td></tr><tr><td>A</td><td>V</td><td>B</td><td>0x102075CF</td></tr><tr><td>9</td><td>S</td><td>B</td><td>0x102025CF</td></tr><tr><td>9</td><td>U</td><td>B</td><td>0x102035CF</td></tr><tr><td>9</td><td>T</td><td>B</td><td>0x102085CF</td></tr><tr><td>9</td><td>V</td><td>B</td><td>0x102095CF</td></tr><tr><td>8</td><td>S</td><td>B</td><td>0x102045CF</td></tr><tr><td>8</td><td>U</td><td>B</td><td>0x102055CF</td></tr><tr><td>8</td><td>T</td><td>B</td><td>0x1020A5CF</td></tr><tr><td>8</td><td>V</td><td>B</td><td>0x1020B5CF</td></tr></table>	Memory size	Option	Revision	Chip ID	JTAG ID	SHE Module ID (SHE_MID) *	A	S	B	0x10130100	0x102005CF	0x000F_0300	A	U	B	0x102015CF	A	T	B	0x102065CF	A	V	B	0x102075CF	9	S	B	0x102025CF	9	U	B	0x102035CF	9	T	B	0x102085CF	9	V	B	0x102095CF	8	S	B	0x102045CF	8	U	B	0x102055CF	8	T	B	0x1020A5CF	8	V	B	0x1020B5CF
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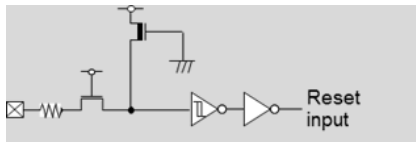
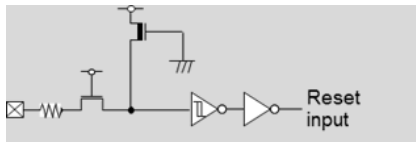
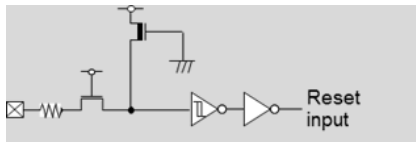
Page	Section	Change Results																			
8	1. Features 1.2 Optional Function 1.2.3 Function Table	Revised as below: 176-Pin of GPIO Error) <table><tr><td>Specification</td><td colspan="3">176-Pin</td></tr><tr><td>GPIO</td><td>151</td><td colspan="2">141:w/ subclk</td></tr></table> Correct) <table><tr><td>Specification</td><td colspan="3">176-Pin</td></tr><tr><td>GPIO</td><td>151</td><td colspan="2">149:w/ subclk</td></tr></table>				Specification	176-Pin			GPIO	151	141:w/ subclk		Specification	176-Pin			GPIO	151	149:w/ subclk	
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10	1. Features 1.2 Optional Function 1.2.4 Restriction	Deleted as below. Error) <table><tr><td>Function</td><td>TEQFP144 LQF144</td><td>TEQFP120 LQFP120</td><td colspan="2">TEQFP100 LQFP100</td></tr><tr><td>Partial Wake Up</td><td>PWUTRG_0</td><td>PWUTRG_0</td><td colspan="2">PWU_AN7 PWUTRG_0</td></tr></table>				Function	TEQFP144 LQF144	TEQFP120 LQFP120	TEQFP100 LQFP100		Partial Wake Up	PWUTRG_0	PWUTRG_0	PWU_AN7 PWUTRG_0							
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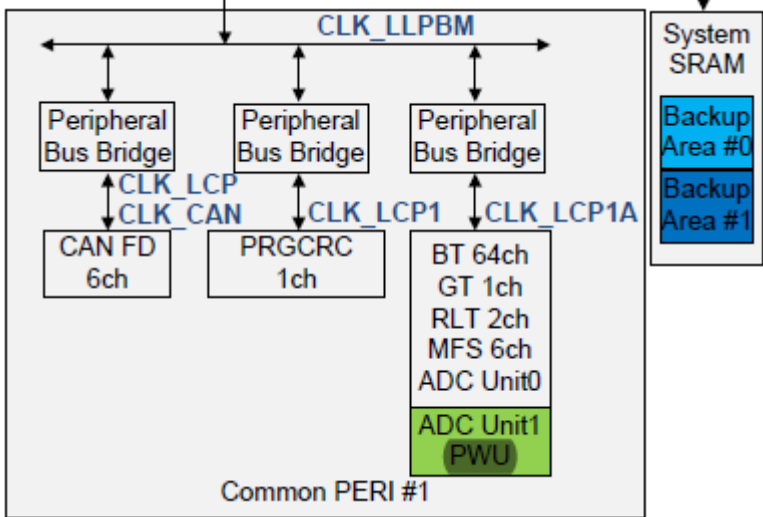
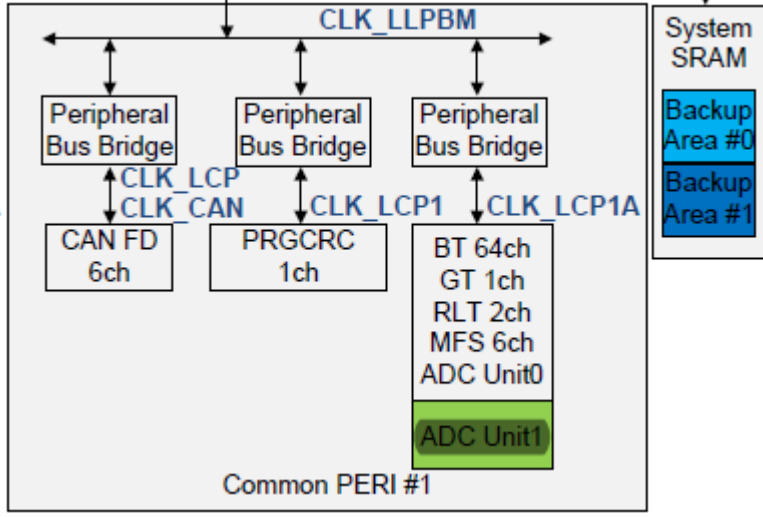
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16	4.Pin Assignment	Signals Indicated by the shading below deleted in Figure. Figure 4-1 LQFP/TEQFP-176 -Right side Error)  <table> <tr><td>137</td><td>-</td><td>VSS</td></tr> <tr><td>136</td><td>A</td><td>P321/INT28_1/PWUTRG_1/TIOA45_0/TRACECLK_1</td></tr> <tr><td>130</td><td>A</td><td>P320/PWUTRG_0/TIOB60_0</td></tr> <tr><td>129</td><td>B</td><td>P319/INT12_1/AN131/SIN7_0/TIOA60_0</td></tr> <tr><td>128</td><td>A</td><td>P318/INT9_0/RX1_1/TIOA10_1</td></tr> <tr><td>127</td><td>B</td><td>P317/INT11_1/AN130/TX1_1/SIN7_2/TIOB29_0/TIOA9_1</td></tr> <tr><td>126</td><td>A</td><td>P316/TIOA21_1</td></tr> <tr><td>125</td><td>B</td><td>P315/INT28_0/AN129/RX8_0/SCS70_0/IN5_1/TIOB28_0/TIOA8_1/TRACECTL_1</td></tr> <tr><td>124</td><td>B</td><td>P314/AN128/TX8_0/SCK7_0/SCL7_0/IN4_1/TIOB27_0/TIOA7_1/TRACEDATA0_1</td></tr> <tr><td>123</td><td>B</td><td>P313/INT10_1/AN127/SOT7_0/SDA7_0/IN3_1/TIOB26_0/TRACEDATA1_1</td></tr> <tr><td>122</td><td>B</td><td>P312/AN126/SCS71_0/IN2_1/TIOB25_0</td></tr> <tr><td>121</td><td>A</td><td>P311/TIOB59_0</td></tr> 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<tr><td>99</td><td>D</td><td>P225/INT0_0/AN110/PWU_AN2/RX0_2/SOT5_0/SDA5_0/IN20_2/TIOB17_0/ZIN9_1</td></tr> <tr><td>98</td><td>B</td><td>P224/AN109/PWU_AN1/TX0_2/SCS50_0/IN19_2/TIOA40_0/BIN9_1</td></tr> <tr><td>97</td><td>B</td><td>P223/AN108/PWU_AN0/SCS51_0/IN18_2/TIOB39_0/AIN9_1/TOT0_1</td></tr> <tr><td>96</td><td>B</td><td>P222/INT7_0/AN107/RX2_0/SIN5_0/IN17_2/TIOA39_0</td></tr> </table> Correct)  <table> <tr><td>132</td><td>-</td><td>VSS</td></tr> <tr><td>131</td><td>A</td><td>P321/INT28_1/TIOA45_0/TRACECLK_1</td></tr> <tr><td>130</td><td>A</td><td>P320/TIOB60_0</td></tr> <tr><td>129</td><td>B</td><td>P319/INT12_1/AN131/SIN7_0/TIOA60_0</td></tr> <tr><td>128</td><td>A</td><td>P318/INT9_0/RX1_1/TIOA10_1</td></tr> <tr><td>127</td><td>B</td><td>P317/INT11_1/AN130/TX1_1/SIN7_2/TIOB29_0/TIOA9_1</td></tr> <tr><td>126</td><td>A</td><td>P316/TIOA21_1</td></tr> <tr><td>125</td><td>B</td><td>P315/INT28_0/AN129/RX8_0/SCS70_0/IN5_1/TIOB28_0/TIOA8_1/TRACECTL_1</td></tr> <tr><td>124</td><td>B</td><td>P314/AN128/TX8_0/SCK7_0/SCL7_0/IN4_1/TIOB27_0/TIOA7_1/TRACEDATA0_1</td></tr> <tr><td>123</td><td>B</td><td>P313/INT10_1/AN127/SOT7_0/SDA7_0/IN3_1/TIOB26_0/TRACEDATA1_1</td></tr> <tr><td>122</td><td>B</td><td>P312/AN126/SCS71_0/IN2_1/TIOB25_0</td></tr> <tr><td>121</td><td>A</td><td>P311/TIOB59_0</td></tr> <tr><td>120</td><td>A</td><td>P310/INT15_0/TIOA59_0</td></tr> <tr><td>119</td><td>B</td><td>P309/INT27_0/AN125/SIN7_3/IN1_1/TIOA44_0/TIOA29_1/TOT17_1/TRACEDATA2_1</td></tr> <tr><td>118</td><td>B</td><td>P308/INT27_1/AN124/IN0_1/TIOB44_0/TIOA28_1</td></tr> <tr><td>117</td><td>B</td><td>P307/INT1_0/AN123/RX0_0/SCS72_0/TIOB18_0/TIN17_1/TRACEDATA3_1</td></tr> <tr><td>116</td><td>B</td><td>P306/AN122/TX0_0/SCS73_0/TIOB43_0</td></tr> <tr><td>115</td><td>K</td><td>NMIX</td></tr> <tr><td>114</td><td>B</td><td>P305/AN121/SCS100_1/TEXT8_0/TIOA29_0/TOT16_1/TRACEDATA4_1</td></tr> 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<tr><td>102</td><td>A</td><td>P214/INT17_1/ADTG0_0/SOT5_1/IN4_2/TIOB40_0/TIOA15_1</td></tr> <tr><td>101</td><td>A</td><td>P213/INT8_1/SIN5_1/IN3_2/TIOA41_0/TIOA14_1</td></tr> <tr><td>100</td><td>D</td><td>P226/AN111/SCK5_0/SCL5_0/IN21_2/TIOA17_1/TIN1_1</td></tr> <tr><td>99</td><td>D</td><td>P225/INT0_0/AN110/RX0_2/SOT5_0/SDA5_0/IN20_2/TIOB17_0/ZIN9_1</td></tr> <tr><td>98</td><td>B</td><td>P224/AN109/TX0_2/SCS50_0/IN19_2/TIOA40_0/BIN9_1</td></tr> <tr><td>97</td><td>B</td><td>P223/AN108/SCS51_0/IN18_2/TIOB39_0/AIN9_1/TOT0_1</td></tr> <tr><td>96</td><td>B</td><td>P222/INT7_0/AN107/RX2_0/SIN5_0/IN17_2/TIOA39_0</td></tr> </table>	137	-	VSS	136	A	P321/INT28_1/PWUTRG_1/TIOA45_0/TRACECLK_1	130	A	P320/PWUTRG_0/TIOB60_0	129	B	P319/INT12_1/AN131/SIN7_0/TIOA60_0	128	A	P318/INT9_0/RX1_1/TIOA10_1	127	B	P317/INT11_1/AN130/TX1_1/SIN7_2/TIOB29_0/TIOA9_1	126	A	P316/TIOA21_1	125	B	P315/INT28_0/AN129/RX8_0/SCS70_0/IN5_1/TIOB28_0/TIOA8_1/TRACECTL_1	124	B	P314/AN128/TX8_0/SCK7_0/SCL7_0/IN4_1/TIOB27_0/TIOA7_1/TRACEDATA0_1	123	B	P313/INT10_1/AN127/SOT7_0/SDA7_0/IN3_1/TIOB26_0/TRACEDATA1_1	122	B	P312/AN126/SCS71_0/IN2_1/TIOB25_0	121	A	P311/TIOB59_0	120	A	P310/INT15_0/TIOA59_0	119	B	P309/INT27_0/AN125/SIN7_3/IN1_1/TIOA44_0/TIOA29_1/TOT17_1/TRACEDATA2_1	118	B	P308/INT27_1/AN124/IN0_1/TIOB44_0/TIOA28_1	117	B	P307/INT1_0/AN123/RX0_0/SCS72_0/TIOB18_0/TIN17_1/TRACEDATA3_1	116	B	P306/AN122/TX0_0/SCS73_0/TIOB43_0	115	K	NMIX	114	B	P305/AN121/SCS100_1/TEXT8_0/TIOA29_0/TOT16_1/TRACEDATA4_1	113	B	P304/INT24_1/AN120/SCS101_1/TEXT4_0/TIOB42_0/TIOA20_1/TIN16_1/TRACEDATA5_1	112	A	P303	111	B	P302/INT26_0/AN119/SCS102_1/TIOA43_0/TIOA19_1/TOT3_1/TRACEDATA6_1	110	B	P301/AN118/SCS100_0/OUT4_0/TIOA42_0/TIOA18_1/TIN3_1/TRACEDATA7_1	109	B	P300/INT20_1/AN117/SCS101_0/OUT3_0/TIOA28_0	108	B	P231/AN116/SCS102_0/OUT2_0/TIOA27_0	107	B	P230/INT19_1/AN115/PWU_AN7/SCS103_0/OUT1_0/TIOA26_0	106	B	P229/INT8_0/AN114/PWU_AN6/RX0_1/SIN10_0/OUT0_0/TIOA25_0/TOT2_1	105	B	P228/AN113/PWU_AN5/TX0_1/SOT10_0/SDA10_0/TIOA24_0/TIN2_1	104	B	P227/AN112/PWU_AN4/SCK10_0/SCL10_0/TIOA23_0/TOT1_1	103	A	P215/INT9_1/ADTG1_0/SCK5_1/IN5_2/TIOB41_0/TIOA16_1	102	A	P214/INT17_1/ADTG0_0/SOT5_1/IN4_2/TIOB40_0/TIOA15_1	101	A	P213/INT8_1/SIN5_1/IN3_2/TIOA41_0/TIOA14_1	100	D	P226/AN111/PWU_AN3/SCK5_0/SCL5_0/IN21_2/TIOA17_1/TIN1_1	99	D	P225/INT0_0/AN110/PWU_AN2/RX0_2/SOT5_0/SDA5_0/IN20_2/TIOB17_0/ZIN9_1	98	B	P224/AN109/PWU_AN1/TX0_2/SCS50_0/IN19_2/TIOA40_0/BIN9_1	97	B	P223/AN108/PWU_AN0/SCS51_0/IN18_2/TIOB39_0/AIN9_1/TOT0_1	96	B	P222/INT7_0/AN107/RX2_0/SIN5_0/IN17_2/TIOA39_0	132	-	VSS	131	A	P321/INT28_1/TIOA45_0/TRACECLK_1	130	A	P320/TIOB60_0	129	B	P319/INT12_1/AN131/SIN7_0/TIOA60_0	128	A	P318/INT9_0/RX1_1/TIOA10_1	127	B	P317/INT11_1/AN130/TX1_1/SIN7_2/TIOB29_0/TIOA9_1	126	A	P316/TIOA21_1	125	B	P315/INT28_0/AN129/RX8_0/SCS70_0/IN5_1/TIOB28_0/TIOA8_1/TRACECTL_1	124	B	P314/AN128/TX8_0/SCK7_0/SCL7_0/IN4_1/TIOB27_0/TIOA7_1/TRACEDATA0_1	123	B	P313/INT10_1/AN127/SOT7_0/SDA7_0/IN3_1/TIOB26_0/TRACEDATA1_1	122	B	P312/AN126/SCS71_0/IN2_1/TIOB25_0	121	A	P311/TIOB59_0	120	A	P310/INT15_0/TIOA59_0	119	B	P309/INT27_0/AN125/SIN7_3/IN1_1/TIOA44_0/TIOA29_1/TOT17_1/TRACEDATA2_1	118	B	P308/INT27_1/AN124/IN0_1/TIOB44_0/TIOA28_1	117	B	P307/INT1_0/AN123/RX0_0/SCS72_0/TIOB18_0/TIN17_1/TRACEDATA3_1	116	B	P306/AN122/TX0_0/SCS73_0/TIOB43_0	115	K	NMIX	114	B	P305/AN121/SCS100_1/TEXT8_0/TIOA29_0/TOT16_1/TRACEDATA4_1	113	B	P304/INT24_1/AN120/SCS101_1/TEXT4_0/TIOB42_0/TIOA20_1/TIN16_1/TRACEDATA5_1	112	A	P303	111	B	P302/INT26_0/AN119/SCS102_1/TIOA43_0/TIOA19_1/TOT3_1/TRACEDATA6_1	110	B	P301/AN118/SCS100_0/OUT4_0/TIOA42_0/TIOA18_1/TIN3_1/TRACEDATA7_1	109	B	P300/INT20_1/AN117/SCS101_0/OUT3_0/TIOA28_0	108	B	P231/AN116/SCS102_0/OUT2_0/TIOA27_0	107	B	P230/INT19_1/AN115/SCS103_0/OUT1_0/TIOA26_0	106	B	P229/INT8_0/AN114/RX0_1/SIN10_0/OUT0_0/TIOA25_0/TOT2_1	105	B	P228/AN113/TX0_1/SOT10_0/SDA10_0/TIOA24_0/TIN2_1	104	B	P227/AN112/SCK10_0/SCL10_0/TIOA23_0/TOT1_1	103	A	P215/INT9_1/ADTG1_0/SCK5_1/IN5_2/TIOB41_0/TIOA16_1	102	A	P214/INT17_1/ADTG0_0/SOT5_1/IN4_2/TIOB40_0/TIOA15_1	101	A	P213/INT8_1/SIN5_1/IN3_2/TIOA41_0/TIOA14_1	100	D	P226/AN111/SCK5_0/SCL5_0/IN21_2/TIOA17_1/TIN1_1	99	D	P225/INT0_0/AN110/RX0_2/SOT5_0/SDA5_0/IN20_2/TIOB17_0/ZIN9_1	98	B	P224/AN109/TX0_2/SCS50_0/IN19_2/TIOA40_0/BIN9_1	97	B	P223/AN108/SCS51_0/IN18_2/TIOB39_0/AIN9_1/TOT0_1	96	B	P222/INT7_0/AN107/RX2_0/SIN5_0/IN17_2/TIOA39_0
137	-	VSS																																																																																																																																																																																																																														
136	A	P321/INT28_1/PWUTRG_1/TIOA45_0/TRACECLK_1																																																																																																																																																																																																																														
130	A	P320/PWUTRG_0/TIOB60_0																																																																																																																																																																																																																														
129	B	P319/INT12_1/AN131/SIN7_0/TIOA60_0																																																																																																																																																																																																																														
128	A	P318/INT9_0/RX1_1/TIOA10_1																																																																																																																																																																																																																														
127	B	P317/INT11_1/AN130/TX1_1/SIN7_2/TIOB29_0/TIOA9_1																																																																																																																																																																																																																														
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124	B	P314/AN128/TX8_0/SCK7_0/SCL7_0/IN4_1/TIOB27_0/TIOA7_1/TRACEDATA0_1																																																																																																																																																																																																																														
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122	B	P312/AN126/SCS71_0/IN2_1/TIOB25_0																																																																																																																																																																																																																														
121	A	P311/TIOB59_0																																																																																																																																																																																																																														
120	A	P310/INT15_0/TIOA59_0																																																																																																																																																																																																																														
119	B	P309/INT27_0/AN125/SIN7_3/IN1_1/TIOA44_0/TIOA29_1/TOT17_1/TRACEDATA2_1																																																																																																																																																																																																																														
118	B	P308/INT27_1/AN124/IN0_1/TIOB44_0/TIOA28_1																																																																																																																																																																																																																														
117	B	P307/INT1_0/AN123/RX0_0/SCS72_0/TIOB18_0/TIN17_1/TRACEDATA3_1																																																																																																																																																																																																																														
116	B	P306/AN122/TX0_0/SCS73_0/TIOB43_0																																																																																																																																																																																																																														
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108	B	P231/AN116/SCS102_0/OUT2_0/TIOA27_0																																																																																																																																																																																																																														
107	B	P230/INT19_1/AN115/PWU_AN7/SCS103_0/OUT1_0/TIOA26_0																																																																																																																																																																																																																														
106	B	P229/INT8_0/AN114/PWU_AN6/RX0_1/SIN10_0/OUT0_0/TIOA25_0/TOT2_1																																																																																																																																																																																																																														
105	B	P228/AN113/PWU_AN5/TX0_1/SOT10_0/SDA10_0/TIOA24_0/TIN2_1																																																																																																																																																																																																																														
104	B	P227/AN112/PWU_AN4/SCK10_0/SCL10_0/TIOA23_0/TOT1_1																																																																																																																																																																																																																														
103	A	P215/INT9_1/ADTG1_0/SCK5_1/IN5_2/TIOB41_0/TIOA16_1																																																																																																																																																																																																																														
102	A	P214/INT17_1/ADTG0_0/SOT5_1/IN4_2/TIOB40_0/TIOA15_1																																																																																																																																																																																																																														
101	A	P213/INT8_1/SIN5_1/IN3_2/TIOA41_0/TIOA14_1																																																																																																																																																																																																																														
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97	B	P223/AN108/PWU_AN0/SCS51_0/IN18_2/TIOB39_0/AIN9_1/TOT0_1																																																																																																																																																																																																																														
96	B	P222/INT7_0/AN107/RX2_0/SIN5_0/IN17_2/TIOA39_0																																																																																																																																																																																																																														
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131	A	P321/INT28_1/TIOA45_0/TRACECLK_1																																																																																																																																																																																																																														
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106	B	P229/INT8_0/AN114/RX0_1/SIN10_0/OUT0_0/TIOA25_0/TOT2_1																																																																																																																																																																																																																														
105	B	P228/AN113/TX0_1/SOT10_0/SDA10_0/TIOA24_0/TIN2_1																																																																																																																																																																																																																														
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102	A	P214/INT17_1/ADTG0_0/SOT5_1/IN4_2/TIOB40_0/TIOA15_1																																																																																																																																																																																																																														
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Page	Section	Change Results
17	4.Pin Assignment	Signals Indicated by the shading below deleted in Figure. Figure 4-2 LQFP/TEQFP-144 -Right side Error)  Correct) 

Page	Section	Change Results																																																																																																																																																												
18	4.Pin Assignment	Signals Indicated by the shading below deleted in Figure. Figure 4-3 LQFP/TEQFP-120 -Right side Error) <table> <tr><td>90</td><td>-</td><td>VSS</td></tr> <tr><td>89</td><td>A</td><td>P321/INT28_1/PWUTRG_1/TIOA45_0/TRACECLK_1</td></tr> <tr><td>88</td><td>B</td><td>P315/INT28_0/AN129/RX8_0/SCS70_0/IN5_1/TIOB28_0/TIOA8_1/TRACECTL_1</td></tr> <tr><td>87</td><td>B</td><td>P314/AN128/TX8_0/SCK7_0/SCL7_0/IN4_1/TIOB27_0/TIOA7_1/TRACEDATA0_1</td></tr> <tr><td>86</td><td>B</td><td>P313/INT10_1/AN127/SOT7_0/SDA7_0/IN3_1/TIOB26_0/TRACEDATA1_1</td></tr> <tr><td>85</td><td>B</td><td>P309/INT27_0/AN125/SIN7_3/IN1_1/TIOA44_0/TIOA29_1/TOT17_1/TRACEDATA2_1</td></tr> <tr><td>84</td><td>B</td><td>P308/INT27_1/AN124/IN0_1/TIOB44_0/TIOA28_1</td></tr> <tr><td>83</td><td>B</td><td>P307/INT1_0/AN123/RX0_0/SCS72_0/TIOB18_0/TIN17_1/TRACEDATA3_1</td></tr> <tr><td>82</td><td>K</td><td>NMIX</td></tr> <tr><td>81</td><td>B</td><td>P305/AN121/SCS100_1/TEXT8_0/TIOA29_0/TOT16_1/TRACEDATA4_1</td></tr> <tr><td>80</td><td>B</td><td>P304/INT24_1/AN120/SCS101_1/TEXT4_0/TIOB42_0/TIOA20_1/TIN16_1/TRACEDATA5_1</td></tr> <tr><td>79</td><td>B</td><td>P302/INT26_0/AN119/SCS102_1/TIOA43_0/TIOA19_1/TOT3_1/TRACEDATA6_1</td></tr> <tr><td>78</td><td>B</td><td>P301/AN118/SCS100_0/OUT4_0/TIOA42_0/TIOA18_1/TIN3_1/TRACEDATA7_1</td></tr> <tr><td>77</td><td>B</td><td>P300/INT20_1/AN117/SCS101_0/OUT3_0/TIOA28_0</td></tr> <tr><td>76</td><td>B</td><td>P230/INT19_1/AN115/PWU_AN7/SCS103_0/OUT1_0/TIOA26_0</td></tr> <tr><td>75</td><td>B</td><td>P229/INT8_0/AN114/PWU_AN6/RX0_1/SIN10_0/OUT0_0/TIOA25_0/TOT2_1</td></tr> <tr><td>74</td><td>B</td><td>P228/AN113/PWU_AN5/TX0_1/SOT10_0/SDA10_0/TIOA24_0/TIN2_1</td></tr> <tr><td>73</td><td>B</td><td>P227/AN112/PWU_AN4/SCK10_0/SCL10_0/TIOA23_0/TOT1_1</td></tr> <tr><td>72</td><td>A</td><td>P215/INT9_1/ADTG1_0/SCK5_1/IN5_2/TIOB41_0/TIOA16_1</td></tr> <tr><td>71</td><td>A</td><td>P214/INT17_1/ADTG0_0/SOT5_1/IN4_2/TIOB40_0/TIOA15_1</td></tr> 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84	B	P308/INT27_1/AN124/IN0_1/TIOB44_0/TIOA28_1																																																																																																																																																												
83	B	P307/INT1_0/AN123/RX0_0/SCS72_0/TIOB18_0/TIN17_1/TRACEDATA3_1																																																																																																																																																												
82	K	NMIX																																																																																																																																																												
81	B	P305/AN121/SCS100_1/TEXT8_0/TIOA29_0/TOT16_1/TRACEDATA4_1																																																																																																																																																												
80	B	P304/INT24_1/AN120/SCS101_1/TEXT4_0/TIOB42_0/TIOA20_1/TIN16_1/TRACEDATA5_1																																																																																																																																																												
79	B	P302/INT26_0/AN119/SCS102_1/TIOA43_0/TIOA19_1/TOT3_1/TRACEDATA6_1																																																																																																																																																												
78	B	P301/AN118/SCS100_0/OUT4_0/TIOA42_0/TIOA18_1/TIN3_1/TRACEDATA7_1																																																																																																																																																												
77	B	P300/INT20_1/AN117/SCS101_0/OUT3_0/TIOA28_0																																																																																																																																																												
76	B	P230/INT19_1/AN115/SCS103_0/OUT1_0/TIOA26_0																																																																																																																																																												
75	B	P229/INT8_0/AN114/RX0_1/SIN10_0/OUT0_0/TIOA25_0/TOT2_1																																																																																																																																																												
74	B	P228/AN113/TX0_1/SOT10_0/SDA10_0/TIOA24_0/TIN2_1																																																																																																																																																												
73	B	P227/AN112/SCK10_0/SCL10_0/TIOA23_0/TOT1_1																																																																																																																																																												
72	A	P215/INT9_1/ADTG1_0/SCK5_1/IN5_2/TIOB41_0/TIOA16_1																																																																																																																																																												
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Page	Section	Change Results																																																																																																																																										
19	4.Pin Assignment	Signals Indicated by the shading below deleted in Figure. Figure 4- 4 LQFP/TEQFP-100 -Right side Error)  <table> <tr><td>75</td><td>-</td><td>VSS</td></tr> <tr><td>74</td><td>A</td><td>P321/INT28_1/PWUTRG_1/TIOA45_0/TRACECLK_1</td></tr> <tr><td>73</td><td>B</td><td>P315/INT28_0/AN129/RX8_0/SCS70_0/IN5_1/TIOB28_0/TIOA8_1/TRACECTL_1</td></tr> <tr><td>72</td><td>B</td><td>P314/AN128/TX8_0/SCK7_0/SCL7_0/IN4_1/TIOB27_0/TIOA7_1/TRACEDATA0_1</td></tr> <tr><td>71</td><td>B</td><td>P313/INT10_1/AN127/SOT7_0/SDA7_0/IN3_1/TIOB26_0/TRACEDATA1_1</td></tr> <tr><td>70</td><td>B</td><td>P309/INT27_0/AN125/SIN7_3/IN1_1/TIOA44_0/TIOA29_1/TOT17_1/TRACEDATA2_1</td></tr> <tr><td>69</td><td>B</td><td>P307/INT1_0/AN123/RX0_0/SCS72_0/TIOB18_0/TIN17_1/TRACEDATA3_1</td></tr> <tr><td>68</td><td>K</td><td>NMIX</td></tr> <tr><td>67</td><td>B</td><td>P305/AN121/SCS100_1/TEXT8_0/TIOA29_0/TOT16_1/TRACEDATA4_1</td></tr> <tr><td>66</td><td>B</td><td>P304/INT24_1/AN120/SCS101_1/TEXT4_0/TIOB42_0/TIOA20_1/TIN16_1/TRACEDATA5_1</td></tr> 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</table>	75	-	VSS	74	A	P321/INT28_1/PWUTRG_1/TIOA45_0/TRACECLK_1	73	B	P315/INT28_0/AN129/RX8_0/SCS70_0/IN5_1/TIOB28_0/TIOA8_1/TRACECTL_1	72	B	P314/AN128/TX8_0/SCK7_0/SCL7_0/IN4_1/TIOB27_0/TIOA7_1/TRACEDATA0_1	71	B	P313/INT10_1/AN127/SOT7_0/SDA7_0/IN3_1/TIOB26_0/TRACEDATA1_1	70	B	P309/INT27_0/AN125/SIN7_3/IN1_1/TIOA44_0/TIOA29_1/TOT17_1/TRACEDATA2_1	69	B	P307/INT1_0/AN123/RX0_0/SCS72_0/TIOB18_0/TIN17_1/TRACEDATA3_1	68	K	NMIX	67	B	P305/AN121/SCS100_1/TEXT8_0/TIOA29_0/TOT16_1/TRACEDATA4_1	66	B	P304/INT24_1/AN120/SCS101_1/TEXT4_0/TIOB42_0/TIOA20_1/TIN16_1/TRACEDATA5_1	65	B	P302/INT26_0/AN119/SCS102_1/TIOA43_0/TIOA19_1/TOT3_1/TRACEDATA6_1	64	B	P301/AN118/SCS100_0/OUT4_0/TIOA42_0/TIOA18_1/TIN3_1/TRACEDATA7_1	63	B	P229/INT8_0/AN114/PWU_AN6/RX0_1/SIN10_0/OUT0_0/TIOA25_0/TOT2_1	62	B	P228/AN113/PWU_AN5/TX0_1/SOT10_0/SDA10_0/TIOA24_0/TIN2_1	61	B	P227/AN112/PWU_AN4/SCK10_0/SCL10_0/TIOA23_0/TOT1_1	60	A	P215/INT9_1/ADTG1_0/SCK5_1/IN5_2/TIOB41_0/TIOA16_1	59	A	P214/INT17_1/ADTG0_0/SOT5_1/IN4_2/TIOB40_0/TIOA15_1	58	A	P213/INT8_1/SIN5_1/IN3_2/TIOA41_0/TIOA14_1	57	D	P226/AN111/PWU_AN3/SCK5_0/SCL5_0/IN21_2/TIOA17_1/TIN1_1	56	D	P225/INT0_0/AN110/PWU_AN2/RX0_2/SOT5_0/SDA5_0/IN20_2/TIOB17_0/ZIN9_1	55	B	P224/AN109/PWU_AN1/TX0_2/SCS50_0/IN19_2/TIOA40_0/BIN9_1	54	B	P223/AN108/PWU_AN0/SCS51_0/IN18_2/TIOB39_0/AIN9_1/TOT0_1	53	B	P222/INT7_0/AN107/RX2_0/SIN5_0/IN17_2/TIOA39_0	75	-	VSS	74	A	P321/INT28_1/TIOA45_0/TRACECLK_1	73	B	P315/INT28_0/AN129/RX8_0/SCS70_0/IN5_1/TIOB28_0/TIOA8_1/TRACECTL_1	72	B	P314/AN128/TX8_0/SCK7_0/SCL7_0/IN4_1/TIOB27_0/TIOA7_1/TRACEDATA0_1	71	B	P313/INT10_1/AN127/SOT7_0/SDA7_0/IN3_1/TIOB26_0/TRACEDATA1_1	70	B	P309/INT27_0/AN125/SIN7_3/IN1_1/TIOA44_0/TIOA29_1/TOT17_1/TRACEDATA2_1	69	B	P307/INT1_0/AN123/RX0_0/SCS72_0/TIOB18_0/TIN17_1/TRACEDATA3_1	68	K	NMIX	67	B	P305/AN121/SCS100_1/TEXT8_0/TIOA29_0/TOT16_1/TRACEDATA4_1	66	B	P304/INT24_1/AN120/SCS101_1/TEXT4_0/TIOB42_0/TIOA20_1/TIN16_1/TRACEDATA5_1	65	B	P302/INT26_0/AN119/SCS102_1/TIOA43_0/TIOA19_1/TOT3_1/TRACEDATA6_1	64	B	P301/AN118/SCS100_0/OUT4_0/TIOA42_0/TIOA18_1/TIN3_1/TRACEDATA7_1	63	B	P229/INT8_0/AN114/RX0_1/SIN10_0/OUT0_0/TIOA25_0/TOT2_1	62	B	P228/AN113/TX0_1/SOT10_0/SDA10_0/TIOA24_0/TIN2_1	61	B	P227/AN112/SCK10_0/SCL10_0/TIOA23_0/TOT1_1	60	A	P215/INT9_1/ADTG1_0/SCK5_1/IN5_2/TIOB41_0/TIOA16_1	59	A	P214/INT17_1/ADTG0_0/SOT5_1/IN4_2/TIOB40_0/TIOA15_1	58	A	P213/INT8_1/SIN5_1/IN3_2/TIOA41_0/TIOA14_1	57	D	P226/AN111/SCK5_0/SCL5_0/IN21_2/TIOA17_1/TIN1_1	56	D	P225/INT0_0/AN110/RX0_2/SOT5_0/SDA5_0/IN20_2/TIOB17_0/ZIN9_1	55	B	P224/AN109/TX0_2/SCS50_0/IN19_2/TIOA40_0/BIN9_1	54	B	P223/AN108/SCS51_0/IN18_2/TIOB39_0/AIN9_1/TOT0_1	53	B	P222/INT7_0/AN107/RX2_0/SIN5_0/IN17_2/TIOA39_0
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65	B	P302/INT26_0/AN119/SCS102_1/TIOA43_0/TIOA19_1/TOT3_1/TRACEDATA6_1																																																																																																																																										
64	B	P301/AN118/SCS100_0/OUT4_0/TIOA42_0/TIOA18_1/TIN3_1/TRACEDATA7_1																																																																																																																																										
63	B	P229/INT8_0/AN114/RX0_1/SIN10_0/OUT0_0/TIOA25_0/TOT2_1																																																																																																																																										
62	B	P228/AN113/TX0_1/SOT10_0/SDA10_0/TIOA24_0/TIN2_1																																																																																																																																										
61	B	P227/AN112/SCK10_0/SCL10_0/TIOA23_0/TOT1_1																																																																																																																																										
60	A	P215/INT9_1/ADTG1_0/SCK5_1/IN5_2/TIOB41_0/TIOA16_1																																																																																																																																										
59	A	P214/INT17_1/ADTG0_0/SOT5_1/IN4_2/TIOB40_0/TIOA15_1																																																																																																																																										
58	A	P213/INT8_1/SIN5_1/IN3_2/TIOA41_0/TIOA14_1																																																																																																																																										
57	D	P226/AN111/SCK5_0/SCL5_0/IN21_2/TIOA17_1/TIN1_1																																																																																																																																										
56	D	P225/INT0_0/AN110/RX0_2/SOT5_0/SDA5_0/IN20_2/TIOB17_0/ZIN9_1																																																																																																																																										
55	B	P224/AN109/TX0_2/SCS50_0/IN19_2/TIOA40_0/BIN9_1																																																																																																																																										
54	B	P223/AN108/SCS51_0/IN18_2/TIOB39_0/AIN9_1/TOT0_1																																																																																																																																										
53	B	P222/INT7_0/AN107/RX2_0/SIN5_0/IN17_2/TIOA39_0																																																																																																																																										

Page	Section	Change Results																																																																																	
24	5.Pin Descriptions 5.1 Pin Descriptions	The following Partial wakeup function deleted. ■ Table 12-1 Pin Descriptions Error) <table><tr><th rowspan="2">Port Name</th><th rowspan="2">Description</th><th colspan="4">Pin No. of Package</th><th rowspan="2">Remark</th></tr><tr><th>LQFP/TEQFP 100</th><th>LQFP/TEQFP 120</th><th>LQFP/TEQFP 144</th><th>LQFP/TEQFP 176</th></tr><tr><td>PWU_AN0</td><td>Partial wakeup ADC analog 0 input pin</td><td>54</td><td>66</td><td>78</td><td>97</td><td></td></tr><tr><td>PWU_AN1</td><td>Partial wakeup ADC analog 1 input pin</td><td>55</td><td>67</td><td>79</td><td>98</td><td></td></tr><tr><td>PWU_AN2</td><td>Partial wakeup ADC analog 2 input pin</td><td>56</td><td>68</td><td>80</td><td>99</td><td></td></tr><tr><td>PWU_AN3</td><td>Partial wakeup ADC analog 3 input pin</td><td>57</td><td>69</td><td>81</td><td>100</td><td></td></tr><tr><td>PWU_AN4</td><td>Partial wakeup ADC analog 4 input pin</td><td>61</td><td>73</td><td>85</td><td>104</td><td></td></tr><tr><td>PWU_AN5</td><td>Partial wakeup ADC analog 5 input pin</td><td>62</td><td>74</td><td>86</td><td>105</td><td></td></tr><tr><td>PWU_AN6</td><td>Partial wakeup ADC analog 6 input pin</td><td>63</td><td>75</td><td>87</td><td>106</td><td></td></tr><tr><td>PWU_AN7</td><td>Partial wakeup ADC analog 7 input pin</td><td>-</td><td>76</td><td>88</td><td>107</td><td></td></tr><tr><td>PWUTRG_0</td><td>Partial wakeup trigger output pin (0)</td><td>-</td><td>-</td><td>-</td><td>130</td><td></td></tr><tr><td>PWUTRG_1</td><td>Partial wakeup trigger output pin (1)</td><td>74</td><td>89</td><td>107</td><td>131</td><td></td></tr></table>	Port Name	Description	Pin No. of Package				Remark	LQFP/TEQFP 100	LQFP/TEQFP 120	LQFP/TEQFP 144	LQFP/TEQFP 176	PWU_AN0	Partial wakeup ADC analog 0 input pin	54	66	78	97		PWU_AN1	Partial wakeup ADC analog 1 input pin	55	67	79	98		PWU_AN2	Partial wakeup ADC analog 2 input pin	56	68	80	99		PWU_AN3	Partial wakeup ADC analog 3 input pin	57	69	81	100		PWU_AN4	Partial wakeup ADC analog 4 input pin	61	73	85	104		PWU_AN5	Partial wakeup ADC analog 5 input pin	62	74	86	105		PWU_AN6	Partial wakeup ADC analog 6 input pin	63	75	87	106		PWU_AN7	Partial wakeup ADC analog 7 input pin	-	76	88	107		PWUTRG_0	Partial wakeup trigger output pin (0)	-	-	-	130		PWUTRG_1	Partial wakeup trigger output pin (1)	74	89	107	131	
Port Name	Description	Pin No. of Package				Remark																																																																													
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PWU_AN2	Partial wakeup ADC analog 2 input pin	56	68	80	99																																																																														
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PWU_AN5	Partial wakeup ADC analog 5 input pin	62	74	86	105																																																																														
PWU_AN6	Partial wakeup ADC analog 6 input pin	63	75	87	106																																																																														
PWU_AN7	Partial wakeup ADC analog 7 input pin	-	76	88	107																																																																														
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46	5. Pin Descriptions 5.2 I/O Circuit Type	Revised as below: Circuit of Type J Error) <table><tr><th>Type</th><th>Circuit</th><th>Remark</th></tr><tr><td>J</td><td></td><td> - Reset input - 50 kΩ with pull-up resistor - CMOS hysteresis input </td></tr></table> Correct) <table><tr><th>Type</th><th>Circuit</th><th>Remark</th></tr><tr><td>J</td><td></td><td> - Reset input - 50 kΩ with pull-up resistor - CMOS hysteresis input </td></tr></table>	Type	Circuit	Remark	J		- Reset input - 50 kΩ with pull-up resistor - CMOS hysteresis input	Type	Circuit	Remark	J		- Reset input - 50 kΩ with pull-up resistor - CMOS hysteresis input																																																																					
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Page	Section	Change Results
48	6.Block Diagram	Modified the Partial wakeup(PWU) of Block Diagram as following. Figure6-1 Block Diagram Error)  Correct) 

Page	Section	Change Results
51	7. Electrical Characteristics 7.2 Recommended Operating Conditions	Revised as below. Error) *1: When it is used outside recommended range (this is the range of guaranteed operation), contact your sales representative. Detection voltage of the external low voltage detection reset (initial) is 2.6V±3.5%. This detection voltage level setting is below the minimum operation assurance voltage (2.7V) . Between this detection voltage and the minimum operation assurance voltage, MCU functions are not guaranteed except for the low voltage detector. Correct) *1: When it is used outside recommended range (this is the range of guaranteed operation), contact your sales representative. The initial detection voltage of the external low voltage detection is 2.6V±3.5%. This LVD setting and internal LVD (LVDL0/LVDL1) cannot be used to reliably generate a reset before voltage dips below minimum guaranteed MCU operation voltage, as these detection levels are below the minimum guaranteed MCU operation voltage.
51		Revised as below. Error) ■ <i>The power-on sequence is as follows. Simultaneously turn on the digital supply voltage (VCC) and analog supply voltages (AVCC0, AVCC1, AVRH0, AVRH1), or turn on the digital supply voltage (VCC) and then the analog supply voltages (AVCC0, AVCC1, AVRH0, AVRH1). Be careful that analog power supplies (AVCC0, AVCC1, AVRH0, and AVRH1) and analog inputs do not exceed the digital power supply (VCC) at the analog system power-on and power-off times.</i> Correct) Note: <i>The power-on sequence is as follows. Simultaneously turn on the digital supply voltage (VCC) and analog supply voltages (AVCC0, AVCC1, AVRH0, AVRH1), or turn on the digital supply voltage (VCC) and then the analog supply voltages (AVCC0, AVCC1, AVRH0, AVRH1). Be careful that analog power supplies (AVCC0, AVCC1, AVRH0, and AVRH1) and analog inputs do not exceed the digital power supply (VCC) at the analog system power-on and power-off times.</i>

Page	Section	Change Results						
55	7. Electrical Characteristics 7.3 DC Characteristics	Modified the Power supply current (Symbol: I _{CCT5} , I _{CCH5} , I _{CCT52} , I _{CCH52}) as following. Symbol I _{CCP} is deleted All.						
		Power supply current Error)						
		(T _A : -40 °C to +105 °C, V _{CC} =AV _{CC} =5.0 V±0.5 V/ V _{CC} =AV _{CC} =3.3 V±0.3 V, V _{SS} =AV _{SS} =0.0 V)						
		Symbol	Conditions*3	Value			Remarks	
				Min	Typ	Max		
		I _{CCT5}	Timer mode	-	1295	2605	T _A =25 °C When using 4 MHz crystal for main oscillator.	
				-	1100	2220	T _A =25 °C When using Slow-CR source oscillation.	
				-	1100	2240	T _A =25 °C When using 32 kHz sub source oscillation.	
		I _{CCH5}	Stop mode	-	1100	2220	T _A =25 °C	
		I _{CCP}	PWU mode (Shutdown)	-	65	130	T _A =25 °C (PWU operation cycle 16 ms)	
				-	55	115	T _A =25 °C (PWU operation cycle 32 ms)	
		I _{CCT52}	Timer mode (Shutdown)	-	320	530	T _A =25 °C When using 4 MHz crystal for main oscillator.	RTC operation, BackupRAM 12 KB retention.
-	45			100	T _A =25 °C When using Slow-CR source oscillation.			
-	55			120	T _A =25 °C When using 32 kHz sub source oscillation.			
I _{CCH52}	Stop mode (Shutdown)	-	45	95	T _A =25 °C	BackupRAM 12 KB retention.		

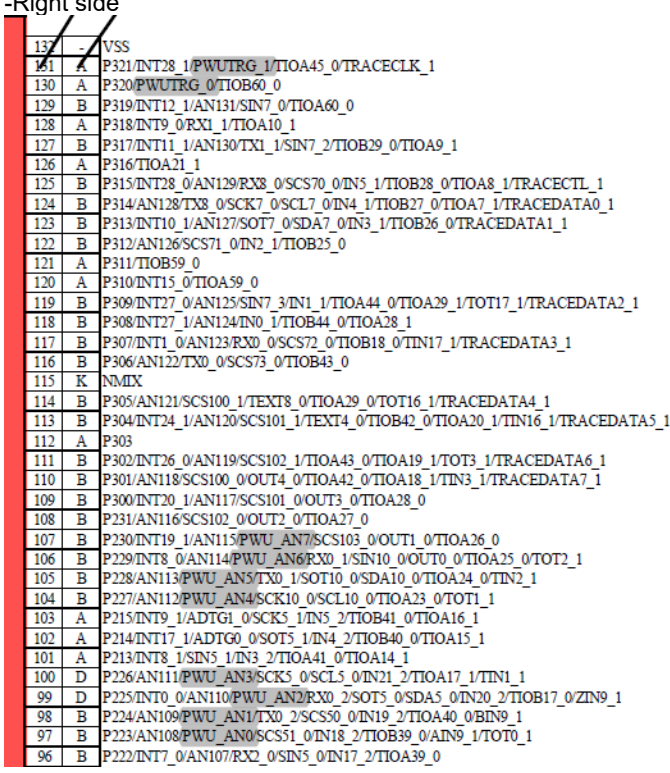
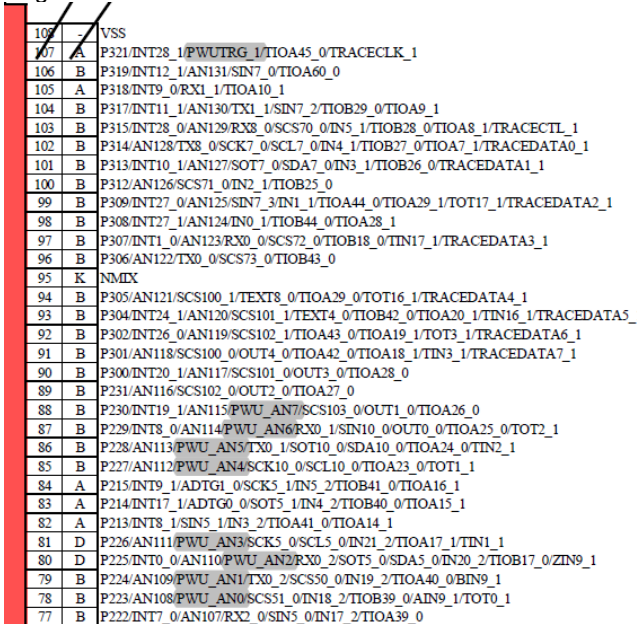
Page	Section	Change Results						
55	7. Electrical Characteristics 7.3 DC Characteristics	Correct)						
		(T _A : -40 °C to +105 °C, VCC=AVCC=5.0 V±0.5 V/ VCC=AVCC=3.3 V±0.3 V, VSS=AVSS=0.0 V)						
		Symbol	Conditions*3	Value			Remarks	
				Min	Typ	Max		
		I _{CCT5}	Timer mode	-	1495	2905	T _A =25 °C When using 4 MHz crystal for main oscillator.	
				-	1300	2520	T _A =25 °C When using Slow-CR source oscillation.	
				-	1300	2540	T _A =25 °C When using 32 kHz sub source oscillation.	
		I _{CCH5}	Stop mode	-	1300	2520	T _A =25 °C	
		I _{CCT52}	Timer mode (Shutdown)	-	520	830	T _A =25 °C When using 4 MHz crystal for main oscillator.	RTC operation, BackupRAM 12 KB retention.
				-	245	400	T _A =25 °C When using Slow-CR source oscillation.	
-	255			420	T _A =25 °C When using 32 kHz sub source oscillation.			
I _{CCH52}	Stop mode (Shutdown)	-	245	395	T _A =25 °C	BackupRAM 12 KB retention.		

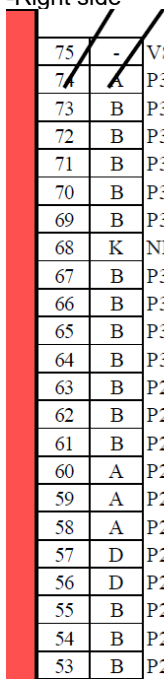
Page	Section	Change Results																																																																				
56	7. Electrical Characteristics 7.3 DC Characteristics	Modified the Power supply current (Symbol: I_{CCT5}, I_{CCH5}, I_{CCT52}, I_{CCH52}) as following. Symbol I_{CCP} is deleted All. Power supply current Error) (T_A: -40 °C to +125 °C, VCC=AVCC=5.0 V±0.5 V/ VCC=AVCC=3.3 V±0.3 V, VSS=AVSS=0.0 V) <table><tr><th rowspan="2">Symbol</th><th rowspan="2">Conditions*3</th><th colspan="3">Value</th><th colspan="2" rowspan="2">Remarks</th></tr><tr><th>Min</th><th>Typ</th><th>Max</th></tr><tr><td rowspan="3">I_{CCT5}</td><td rowspan="3">Timer mode</td><td>-</td><td>1295</td><td>2605</td><td colspan="2">T_A=25 °C When using 4 MHz crystal for main oscillator.</td></tr><tr><td>-</td><td>1100</td><td>2220</td><td colspan="2">T_A=25 °C When using Slow-CR source oscillation.</td></tr><tr><td>-</td><td>1100</td><td>2240</td><td colspan="2">T_A=25 °C When using 32 kHz sub source oscillation.</td></tr><tr><td>I_{CCH5}</td><td>Stop mode</td><td>-</td><td>1100</td><td>2220</td><td colspan="2">T_A=25 °C</td></tr><tr><td rowspan="2">I_{CCP}</td><td rowspan="2">PWU mode (Shutdown)</td><td>-</td><td>65</td><td>130</td><td colspan="2">T_A=25 °C (PWU operation cycle 16 ms)</td></tr><tr><td>-</td><td>55</td><td>115</td><td colspan="2">T_A=25 °C (PWU operation cycle 32 ms)</td></tr><tr><td rowspan="3">I_{CCT52}</td><td rowspan="3">Timer mode (Shutdown)</td><td>-</td><td>320</td><td>530</td><td>T_A=25 °C When using 4 MHz crystal for main oscillator.</td><td rowspan="3">RTC operation, BackupRAM 12 KB retention.</td></tr><tr><td>-</td><td>45</td><td>100</td><td>T_A=25 °C When using Slow-CR source oscillation.</td></tr><tr><td>-</td><td>55</td><td>120</td><td>T_A=25 °C When using 32 kHz sub source oscillation.</td></tr><tr><td>I_{CCH52}</td><td>Stop mode (Shutdown)</td><td>-</td><td>45</td><td>95</td><td>T_A=25 °C</td><td>BackupRAM 12 KB retention.</td></tr></table>	Symbol	Conditions*3	Value			Remarks		Min	Typ	Max	I _{CCT5}	Timer mode	-	1295	2605	T _A =25 °C When using 4 MHz crystal for main oscillator.		-	1100	2220	T _A =25 °C When using Slow-CR source oscillation.		-	1100	2240	T _A =25 °C When using 32 kHz sub source oscillation.		I _{CCH5}	Stop mode	-	1100	2220	T _A =25 °C		I _{CCP}	PWU mode (Shutdown)	-	65	130	T _A =25 °C (PWU operation cycle 16 ms)		-	55	115	T _A =25 °C (PWU operation cycle 32 ms)		I _{CCT52}	Timer mode (Shutdown)	-	320	530	T _A =25 °C When using 4 MHz crystal for main oscillator.	RTC operation, BackupRAM 12 KB retention.	-	45	100	T _A =25 °C When using Slow-CR source oscillation.	-	55	120	T _A =25 °C When using 32 kHz sub source oscillation.	I _{CCH52}	Stop mode (Shutdown)	-	45	95	T _A =25 °C	BackupRAM 12 KB retention.
Symbol	Conditions*3	Value			Remarks																																																																	
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I _{CCT5}	Timer mode	-	1295	2605	T _A =25 °C When using 4 MHz crystal for main oscillator.																																																																	
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Page	Section	Change Results																																																								
56	7. Electrical Characteristics 7.3 DC Characteristics	Correct) (T_A: -40 °C to +125 °C, VCC=AVCC=5.0 V±0.5 V/ VCC=AVCC=3.3 V±0.3 V, VSS=AVSS=0.0 V) <table><tr><th rowspan="2">Symbol</th><th rowspan="2">Conditions*3</th><th colspan="3">Value</th><th colspan="2" rowspan="2">Remarks</th></tr><tr><th>Min</th><th>Typ</th><th>Max</th></tr><tr><td rowspan="3">I_{CC}T5</td><td rowspan="3">Timer mode</td><td>-</td><td>1495</td><td>2905</td><td colspan="2">T_A=25 °C When using 4 MHz crystal for main oscillator.</td></tr><tr><td>-</td><td>1300</td><td>2520</td><td colspan="2">T_A=25 °C When using Slow-CR source oscillation.</td></tr><tr><td>-</td><td>1300</td><td>2540</td><td colspan="2">T_A=25 °C When using 32 kHz sub source oscillation.</td></tr><tr><td>I_{CC}H5</td><td>Stop mode</td><td>-</td><td>1300</td><td>2520</td><td colspan="2">T_A=25 °C</td></tr><tr><td rowspan="3">I_{CC}T52</td><td rowspan="3">Timer mode (Shutdown)</td><td>-</td><td>520</td><td>830</td><td>T_A=25 °C When using 4 MHz crystal for main oscillator.</td><td rowspan="3">RTC operation, BackupRAM 12 KB retention.</td></tr><tr><td>-</td><td>245</td><td>400</td><td>T_A=25 °C When using Slow-CR source oscillation.</td></tr><tr><td>-</td><td>255</td><td>420</td><td>T_A=25 °C When using 32 kHz sub source oscillation.</td></tr><tr><td>I_{CC}H52</td><td>Stop mode (Shutdown)</td><td>-</td><td>245</td><td>395</td><td>T_A=25 °C</td><td>BackupRAM 12 KB retention.</td></tr></table>	Symbol	Conditions*3	Value			Remarks		Min	Typ	Max	I _{CC} T5	Timer mode	-	1495	2905	T _A =25 °C When using 4 MHz crystal for main oscillator.		-	1300	2520	T _A =25 °C When using Slow-CR source oscillation.		-	1300	2540	T _A =25 °C When using 32 kHz sub source oscillation.		I _{CC} H5	Stop mode	-	1300	2520	T _A =25 °C		I _{CC} T52	Timer mode (Shutdown)	-	520	830	T _A =25 °C When using 4 MHz crystal for main oscillator.	RTC operation, BackupRAM 12 KB retention.	-	245	400	T _A =25 °C When using Slow-CR source oscillation.	-	255	420	T _A =25 °C When using 32 kHz sub source oscillation.	I _{CC} H52	Stop mode (Shutdown)	-	245	395	T _A =25 °C	BackupRAM 12 KB retention.
Symbol	Conditions*3	Value			Remarks																																																					
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I _{CC} H52	Stop mode (Shutdown)	-	245	395	T _A =25 °C	BackupRAM 12 KB retention.																																																				
87	7. Electrical Characteristics 7.4.11 Low Voltage Detection (External Voltage)	Revised as below Error) *3: This detection voltage level setting is below the minimum operation assurance voltage (2.7V) . Between this detection voltage and the minimum operation assurance voltage, MCU functions are not guaranteed except for the low voltage detector. Correct) *3: This LVD settings cannot be used to reliably generate a reset before voltage dips below minimum guaranteed MCU operation voltage, as these detection levels are below the minimum guaranteed MCU operation voltage (2.7V).																																																								
87	7. Electrical Characteristics 7.4.12 Low-Voltage Detection (Internal Voltage)	Added as below. Correct) <table><tr><td>Detection voltage</td><td>V_{RDL}</td><td>-</td><td>*1</td><td>0.75</td><td>0.85</td><td>0.95</td><td>V</td><td>When Power-supply Voltage falls^{*2}</td></tr></table> *2: This LVD setting cannot be used to reliably generate a reset before voltage dips below minimum guaranteed MCU operation voltage, as this detection level is below the minimum guaranteed MCU operation voltage.	Detection voltage	V _{RDL}	-	*1	0.75	0.85	0.95	V	When Power-supply Voltage falls ^{*2}																																															
Detection voltage	V _{RDL}	-	*1	0.75	0.85	0.95	V	When Power-supply Voltage falls ^{*2}																																																		

Page	Section	Change Results				
88	7. Electrical Characteristics 7.4.12.2 Low-voltage Detection (internal low-voltage detection for LVDL1)	Revised as below. Error) *2: This detection voltage level setting is below the minimum operation voltage. Between this detection voltage and the minimum operation voltage, MCU functions are not guaranteed except for the low voltage detector. Correct) *2: This LVD setting cannot be used to reliably generate a reset before voltage dips below minimum guaranteed MCU operation voltage, as this detection level is below the minimum guaranteed MCU operation voltage.				
92	7. Electrical Characteristics 7.5 A/D Converter 7.5.3 Glossary	Revised as below. Error) Integral linearity error: Deviation of the straight line connecting the zero transition point ("0000 0000 0000" ←→ "0000 0000 0001") and full-scale transition point ("1111 1111 1110" ←→ "1111 1111 1111") from actual conversion characteristics includes zero transition error, full-scale transition error, and nonlinearity error. Correct) Integral linearity error: Deviation of the straight line connecting the zero transition point ("0000 0000 0000" ↔ "0000 0000 0001") and full-scale transition point ("1111 1111 1110" ↔ "1111 1111 1111") from actual conversion characteristics includes zero transition error, full-scale transition error, and non linearity error.				
99	9. Package Dimensions	Added as below. <table><tr><th>Package Type</th><th>Package Code</th></tr><tr><td>TEQFP 176pin</td><td>LEH176</td></tr></table> 002-13037 **	Package Type	Package Code	TEQFP 176pin	LEH176
Package Type		Package Code				
TEQFP 176pin		LEH176				
100		Added as below. <table><tr><th>Package Type</th><th>Package Code</th></tr><tr><td>TEQFP 144pin</td><td>LEJ144</td></tr></table> Revised as below 002-13036 *A	Package Type	Package Code	TEQFP 144pin	LEJ144
Package Type	Package Code					
TEQFP 144pin	LEJ144					
101	Added as below. <table><tr><th>Package Type</th><th>Package Code</th></tr><tr><td>TEQFP 100pin</td><td>LEI100</td></tr></table> Revised as below 002-13035 *A	Package Type	Package Code	TEQFP 100pin	LEI100	
Package Type	Package Code					
TEQFP 100pin	LEI100					
102	Added as below. <table><tr><th>Package Type</th><th>Package Code</th></tr><tr><td>LQFP 144pin</td><td>LQS144</td></tr></table> 002-13015 **	Package Type	Package Code	LQFP 144pin	LQS144	
Package Type	Package Code					
LQFP 144pin	LQS144					

Page	Section	Change Results										
103	9. Package Dimensions	Added as below. <table><tr><td>Package Type</td><td>Package Code</td></tr><tr><td>LQFP 100pin</td><td>LQI100</td></tr></table> 002-11500 **	Package Type	Package Code	LQFP 100pin	LQI100						
Package Type	Package Code											
LQFP 100pin	LQI100											
Rev.*H												
-	Datasheet title	Removed Preliminary status.										
-	1.Features, 4.Pin Assignment, 5.Pin Descriptions, 8.Ordering Information, 9.Package Dimensions	Removed LQFP176, TEQFP144, LQFP120, TEQFP120 and TEQFP100 of the Package.										
1	Features Key Features	The shading sentences added as below. ■ Low standby current in Partial Wake Up mode										
5	1.Features 1.1 Function List	The shading parts added as below. <table><tr><td>Function</td><td>S6J34xxJxx</td><td>S6J34xxHxx</td><td>S6J34xxFxx</td><td>Remark</td></tr><tr><td>Partial Wake Up</td><td>Analog input 8ch</td><td>Analog input 8ch</td><td>Analog input 7ch</td><td>Trigger 1ch</td></tr></table>	Function	S6J34xxJxx	S6J34xxHxx	S6J34xxFxx	Remark	Partial Wake Up	Analog input 8ch	Analog input 8ch	Analog input 7ch	Trigger 1ch
Function	S6J34xxJxx	S6J34xxHxx	S6J34xxFxx	Remark								
Partial Wake Up	Analog input 8ch	Analog input 8ch	Analog input 7ch	Trigger 1ch								
5	1.Features 1.1 Function List	The shading sentences added as below. Notes: ■ Some Functions have the restrictions. For details, see the "Restriction" of chapter "Product Description" in S6J3400 Series hardware manual.										
10	1. Features 1.2 Optional Function 1.2.4 Restriction	The shading parts added as below. <table><tr><td>Function</td><td>LQFP144</td><td>LQFP100</td></tr><tr><td>Partial Wake Up</td><td>PWUTRG_0</td><td>PWU_AN7 PWUTRG_0</td></tr></table>	Function	LQFP144	LQFP100	Partial Wake Up	PWUTRG_0	PWU_AN7 PWUTRG_0				
Function	LQFP144	LQFP100										
Partial Wake Up	PWUTRG_0	PWU_AN7 PWUTRG_0										
11	1. Features 1.2 Optional Function 1.2.4 Restriction	The shading sentences added as below. Notes: ■ The restrictions of other than those above are described in S6J3400 Series hardware manual. For details, see the "Restriction" of chapter "Product Description" in S6J3400 Series hardware manual.										

Page	Section	Change Results
16	4.Pin Assignment	Signals Indicated by the shading below added in Figure. Figure 4-1 TEQFP-176 -Right side  137 - VSS 131 A P321/INT28_1/PWUTRG_1/TIOA45_0/TRACECLK_1 130 A P320/PWUTRG_0/TIOB60_0 129 B P319/INT12_1/AN131/SIN7_0/TIOA60_0 128 A P318/INT9_0/RXI_1/TIOA10_1 127 B P317/INT11_1/AN130/TXI_1/SIN7_2/TIOB29_0/TIOA9_1 126 A P316/TIOA21_1 125 B P315/INT28_0/AN129/RX8_0/SCS70_0/TN5_1/TIOB28_0/TIOA8_1/TRACECTL_1 124 B P314/AN128/TX8_0/SCK7_0/SCL7_0/TN4_1/TIOB27_0/TIOA7_1/TRACEDATA0_1 123 B P313/INT10_1/AN127/SOT7_0/SDA7_0/TN3_1/TIOB26_0/TRACEDATA1_1 122 B P312/AN126/SCS71_0/TN2_1/TIOB25_0 121 A P311/TIOB59_0 120 A P310/INT15_0/TIOA59_0 119 B P309/INT27_0/AN125/SIN7_3/TN1_1/TIOA44_0/TIOA29_1/TOT17_1/TRACEDATA2_1 118 B P308/INT27_1/AN124/TN0_1/TIOB44_0/TIOA28_1 117 B P307/INT1_0/AN123/RX0_0/SCS72_0/TIOB18_0/TN17_1/TRACEDATA3_1 116 B P306/AN122/TX0_0/SCS73_0/TIOB43_0 115 K NMIX 114 B P305/AN121/SCS100_1/TEXT8_0/TIOA29_0/TOT16_1/TRACEDATA4_1 113 B P304/INT24_1/AN120/SCS101_1/TEXT4_0/TIOB42_0/TIOA20_1/TN16_1/TRACEDATA5_1 112 A P303 111 B P302/INT26_0/AN119/SCS102_1/TIOA43_0/TIOA19_1/TOT3_1/TRACEDATA6_1 110 B P301/AN118/SCS100_0/OUT4_0/TIOA42_0/TIOA18_1/TN3_1/TRACEDATA7_1 109 B P300/INT20_1/AN117/SCS101_0/OUT3_0/TIOA28_0 108 B P231/AN116/SCS102_0/OUT2_0/TIOA27_0 107 B P230/INT19_1/AN115/PWU_AN7/SCS103_0/OUT1_0/TIOA26_0 106 B P229/INT8_0/AN114/PWU_AN6/RX0_1/SIN10_0/OUT0_0/TIOA25_0/TOT2_1 105 B P228/AN113/PWU_AN5/TX0_1/SOT10_0/SDA10_0/TIOA24_0/TN2_1 104 B P227/AN112/PWU_AN4/SCK10_0/SCL10_0/TIOA23_0/TOT1_1 103 A P215/INT9_1/ADTG1_0/SCK5_1/TN5_2/TIOB41_0/TIOA16_1 102 A P214/INT17_1/ADTG0_0/SOT5_1/TN4_2/TIOB40_0/TIOA15_1 101 A P213/INT8_1/SIN5_1/TN3_2/TIOA41_0/TIOA14_1 100 D P226/AN111/PWU_AN3/SCK5_0/SCL5_0/TN21_2/TIOA17_1/TN1_1 99 D P225/INT0_0/AN110/PWU_AN2/RX0_2/SOT5_0/SDA5_0/TN20_2/TIOB17_0/ZIN9_1 98 B P224/AN109/PWU_AN1/TX0_2/SCS50_0/TN19_2/TIOA40_0/BIN9_1 97 B P223/AN108/PWU_AN0/SCS51_0/TN18_2/TIOB39_0/AIN9_1/TOT0_1 96 B P222/INT7_0/AN107/RX2_0/SIN5_0/TN17_2/TIOA39_0
17	4.Pin Assignment	Signals Indicated by the shading below added in Figure. Figure 4-2 LQFP-144 -Right side  107 - VSS 107 A P321/INT28_1/PWUTRG_1/TIOA45_0/TRACECLK_1 106 B P319/INT12_1/AN131/SIN7_0/TIOA60_0 105 A P318/INT9_0/RXI_1/TIOA10_1 104 B P317/INT11_1/AN130/TXI_1/SIN7_2/TIOB29_0/TIOA9_1 103 B P315/INT28_0/AN129/RX8_0/SCS70_0/TN5_1/TIOB28_0/TIOA8_1/TRACECTL_1 102 B P314/AN128/TX8_0/SCK7_0/SCL7_0/TN4_1/TIOB27_0/TIOA7_1/TRACEDATA0_1 101 B P313/INT10_1/AN127/SOT7_0/SDA7_0/TN3_1/TIOB26_0/TRACEDATA1_1 100 B P312/AN126/SCS71_0/TN2_1/TIOB25_0 99 B P309/INT27_0/AN125/SIN7_3/TN1_1/TIOA44_0/TIOA29_1/TOT17_1/TRACEDATA2_1 98 B P308/INT27_1/AN124/TN0_1/TIOB44_0/TIOA28_1 97 B P307/INT1_0/AN123/RX0_0/SCS72_0/TIOB18_0/TN17_1/TRACEDATA3_1 96 B P306/AN122/TX0_0/SCS73_0/TIOB43_0 95 K NMIX 94 B P305/AN121/SCS100_1/TEXT8_0/TIOA29_0/TOT16_1/TRACEDATA4_1 93 B P304/INT24_1/AN120/SCS101_1/TEXT4_0/TIOB42_0/TIOA20_1/TN16_1/TRACEDATA5_1 92 B P302/INT26_0/AN119/SCS102_1/TIOA43_0/TIOA19_1/TOT3_1/TRACEDATA6_1 91 B P301/AN118/SCS100_0/OUT4_0/TIOA42_0/TIOA18_1/TN3_1/TRACEDATA7_1 90 B P300/INT20_1/AN117/SCS101_0/OUT3_0/TIOA28_0 89 B P231/AN116/SCS102_0/OUT2_0/TIOA27_0 88 B P230/INT19_1/AN115/PWU_AN7/SCS103_0/OUT1_0/TIOA26_0 87 B P229/INT8_0/AN114/PWU_AN6/RX0_1/SIN10_0/OUT0_0/TIOA25_0/TOT2_1 86 B P228/AN113/PWU_AN5/TX0_1/SOT10_0/SDA10_0/TIOA24_0/TN2_1 85 B P227/AN112/PWU_AN4/SCK10_0/SCL10_0/TIOA23_0/TOT1_1 84 A P215/INT9_1/ADTG1_0/SCK5_1/TN5_2/TIOB41_0/TIOA16_1 83 A P214/INT17_1/ADTG0_0/SOT5_1/TN4_2/TIOB40_0/TIOA15_1 82 A P213/INT8_1/SIN5_1/TN3_2/TIOA41_0/TIOA14_1 81 D P226/AN111/PWU_AN3/SCK5_0/SCL5_0/TN21_2/TIOA17_1/TN1_1 80 D P225/INT0_0/AN110/PWU_AN2/RX0_2/SOT5_0/SDA5_0/TN20_2/TIOB17_0/ZIN9_1 79 B P224/AN109/PWU_AN1/TX0_2/SCS50_0/TN19_2/TIOA40_0/BIN9_1 78 B P223/AN108/PWU_AN0/SCS51_0/TN18_2/TIOB39_0/AIN9_1/TOT0_1 77 B P222/INT7_0/AN107/RX2_0/SIN5_0/TN17_2/TIOA39_0

Page	Section	Change Results																																																																					
18	4.Pin Assignment	Signals Indicated by the shading below added in Figure. Figure 4-3 LQFP-100 -Right side  <table><tr><td>75</td><td>-</td><td>VSS</td></tr><tr><td>74</td><td>A</td><td>P321/INT28_1/PWUTRG_1/TIOA45_0/TRACECLK_1</td></tr><tr><td>73</td><td>B</td><td>P315/INT28_0/AN129/RX8_0/SCS70_0/TN5_1/TIOB28_0/TIOA8_1/TRACECTL_1</td></tr><tr><td>72</td><td>B</td><td>P314/AN128/TX8_0/SCK7_0/SCL7_0/TN4_1/TIOB27_0/TIOA7_1/TRACEDATA0_1</td></tr><tr><td>71</td><td>B</td><td>P313/INT10_1/AN127/SOT7_0/SDA7_0/TN3_1/TIOB26_0/TRACEDATA1_1</td></tr><tr><td>70</td><td>B</td><td>P309/INT27_0/AN125/SIN7_3/TN1_1/TIOA44_0/TIOA29_1/TOT17_1/TRACEDATA2_1</td></tr><tr><td>69</td><td>B</td><td>P307/INT1_0/AN123/RX0_0/SCS72_0/TIOB18_0/TIN17_1/TRACEDATA3_1</td></tr><tr><td>68</td><td>K</td><td>NMIX</td></tr><tr><td>67</td><td>B</td><td>P305/AN121/SCS100_1/TEXT8_0/TIOA29_0/TOT16_1/TRACEDATA4_1</td></tr><tr><td>66</td><td>B</td><td>P304/INT24_1/AN120/SCS101_1/TEXT4_0/TIOB42_0/TIOA20_1/TIN16_1/TRACEDATA5_1</td></tr><tr><td>65</td><td>B</td><td>P302/INT26_0/AN119/SCS102_1/TIOA43_0/TIOA19_1/TOT3_1/TRACEDATA6_1</td></tr><tr><td>64</td><td>B</td><td>P301/AN118/SCS100_0/OUT4_0/TIOA42_0/TIOA18_1/TN3_1/TRACEDATA7_1</td></tr><tr><td>63</td><td>B</td><td>P229/INT8_0/AN114/PWU_AN6/RX0_1/SIN10_0/OUT0_0/TIOA25_0/TOT2_1</td></tr><tr><td>62</td><td>B</td><td>P228/AN113/PWU_AN5/TX0_1/SOT10_0/SDA10_0/TIOA24_0/TIN2_1</td></tr><tr><td>61</td><td>B</td><td>P227/AN112/PWU_AN4/SCK10_0/SCL10_0/TIOA23_0/TOT1_1</td></tr><tr><td>60</td><td>A</td><td>P215/INT9_1/ADTG1_0/SCK5_1/TN5_2/TIOB41_0/TIOA16_1</td></tr><tr><td>59</td><td>A</td><td>P214/INT17_1/ADTG0_0/SOT5_1/TN4_2/TIOB40_0/TIOA15_1</td></tr><tr><td>58</td><td>A</td><td>P213/INT8_1/SIN5_1/TN3_2/TIOA41_0/TIOA14_1</td></tr><tr><td>57</td><td>D</td><td>P226/AN111/PWU_AN3/SCK5_0/SCL5_0/TN21_2/TIOA17_1/TIN1_1</td></tr><tr><td>56</td><td>D</td><td>P225/INT0_0/AN110/PWU_AN2/RX0_2/SOT5_0/SDA5_0/TN20_2/TIOB17_0/ZIN9_1</td></tr><tr><td>55</td><td>B</td><td>P224/AN109/PWU_AN1/TX0_2/SCS50_0/TN19_2/TIOA40_0/BIN9_1</td></tr><tr><td>54</td><td>B</td><td>P223/AN108/PWU_AN0/SCS51_0/TN18_2/TIOB39_0/AIN9_1/TOT0_1</td></tr><tr><td>53</td><td>B</td><td>P222/INT7_0/AN107/RX2_0/SIN5_0/TN17_2/TIOA39_0</td></tr></table>	75	-	VSS	74	A	P321/INT28_1/PWUTRG_1/TIOA45_0/TRACECLK_1	73	B	P315/INT28_0/AN129/RX8_0/SCS70_0/TN5_1/TIOB28_0/TIOA8_1/TRACECTL_1	72	B	P314/AN128/TX8_0/SCK7_0/SCL7_0/TN4_1/TIOB27_0/TIOA7_1/TRACEDATA0_1	71	B	P313/INT10_1/AN127/SOT7_0/SDA7_0/TN3_1/TIOB26_0/TRACEDATA1_1	70	B	P309/INT27_0/AN125/SIN7_3/TN1_1/TIOA44_0/TIOA29_1/TOT17_1/TRACEDATA2_1	69	B	P307/INT1_0/AN123/RX0_0/SCS72_0/TIOB18_0/TIN17_1/TRACEDATA3_1	68	K	NMIX	67	B	P305/AN121/SCS100_1/TEXT8_0/TIOA29_0/TOT16_1/TRACEDATA4_1	66	B	P304/INT24_1/AN120/SCS101_1/TEXT4_0/TIOB42_0/TIOA20_1/TIN16_1/TRACEDATA5_1	65	B	P302/INT26_0/AN119/SCS102_1/TIOA43_0/TIOA19_1/TOT3_1/TRACEDATA6_1	64	B	P301/AN118/SCS100_0/OUT4_0/TIOA42_0/TIOA18_1/TN3_1/TRACEDATA7_1	63	B	P229/INT8_0/AN114/PWU_AN6/RX0_1/SIN10_0/OUT0_0/TIOA25_0/TOT2_1	62	B	P228/AN113/PWU_AN5/TX0_1/SOT10_0/SDA10_0/TIOA24_0/TIN2_1	61	B	P227/AN112/PWU_AN4/SCK10_0/SCL10_0/TIOA23_0/TOT1_1	60	A	P215/INT9_1/ADTG1_0/SCK5_1/TN5_2/TIOB41_0/TIOA16_1	59	A	P214/INT17_1/ADTG0_0/SOT5_1/TN4_2/TIOB40_0/TIOA15_1	58	A	P213/INT8_1/SIN5_1/TN3_2/TIOA41_0/TIOA14_1	57	D	P226/AN111/PWU_AN3/SCK5_0/SCL5_0/TN21_2/TIOA17_1/TIN1_1	56	D	P225/INT0_0/AN110/PWU_AN2/RX0_2/SOT5_0/SDA5_0/TN20_2/TIOB17_0/ZIN9_1	55	B	P224/AN109/PWU_AN1/TX0_2/SCS50_0/TN19_2/TIOA40_0/BIN9_1	54	B	P223/AN108/PWU_AN0/SCS51_0/TN18_2/TIOB39_0/AIN9_1/TOT0_1	53	B	P222/INT7_0/AN107/RX2_0/SIN5_0/TN17_2/TIOA39_0
75	-	VSS																																																																					
74	A	P321/INT28_1/PWUTRG_1/TIOA45_0/TRACECLK_1																																																																					
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72	B	P314/AN128/TX8_0/SCK7_0/SCL7_0/TN4_1/TIOB27_0/TIOA7_1/TRACEDATA0_1																																																																					
71	B	P313/INT10_1/AN127/SOT7_0/SDA7_0/TN3_1/TIOB26_0/TRACEDATA1_1																																																																					
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69	B	P307/INT1_0/AN123/RX0_0/SCS72_0/TIOB18_0/TIN17_1/TRACEDATA3_1																																																																					
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63	B	P229/INT8_0/AN114/PWU_AN6/RX0_1/SIN10_0/OUT0_0/TIOA25_0/TOT2_1																																																																					
62	B	P228/AN113/PWU_AN5/TX0_1/SOT10_0/SDA10_0/TIOA24_0/TIN2_1																																																																					
61	B	P227/AN112/PWU_AN4/SCK10_0/SCL10_0/TIOA23_0/TOT1_1																																																																					
60	A	P215/INT9_1/ADTG1_0/SCK5_1/TN5_2/TIOB41_0/TIOA16_1																																																																					
59	A	P214/INT17_1/ADTG0_0/SOT5_1/TN4_2/TIOB40_0/TIOA15_1																																																																					
58	A	P213/INT8_1/SIN5_1/TN3_2/TIOA41_0/TIOA14_1																																																																					
57	D	P226/AN111/PWU_AN3/SCK5_0/SCL5_0/TN21_2/TIOA17_1/TIN1_1																																																																					
56	D	P225/INT0_0/AN110/PWU_AN2/RX0_2/SOT5_0/SDA5_0/TN20_2/TIOB17_0/ZIN9_1																																																																					
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53	B	P222/INT7_0/AN107/RX2_0/SIN5_0/TN17_2/TIOA39_0																																																																					
23	5.Pin Discriptions 5.1 Pin Descriptions	The shading parts added as below. ■ Table 5-1 Pin Descriptions <table><tr><th rowspan="2">Port Name</th><th rowspan="2">Description</th><th colspan="3">Pin No. of Package</th><th rowspan="2">Remark</th></tr><tr><th>LQFP 100</th><th>LQFP/ 144</th><th>TEQFP 176</th></tr><tr><td>PWU_AN0</td><td>Partial wakeup ADC analog 0 input pin</td><td>54</td><td>78</td><td>97</td><td></td></tr><tr><td>PWU_AN1</td><td>Partial wakeup ADC analog 1 input pin</td><td>55</td><td>79</td><td>98</td><td></td></tr><tr><td>PWU_AN2</td><td>Partial wakeup ADC analog 2 input pin</td><td>56</td><td>80</td><td>99</td><td></td></tr><tr><td>PWU_AN3</td><td>Partial wakeup ADC analog 3 input pin</td><td>57</td><td>81</td><td>100</td><td></td></tr><tr><td>PWU_AN4</td><td>Partial wakeup ADC analog 4 input pin</td><td>61</td><td>85</td><td>104</td><td></td></tr><tr><td>PWU_AN5</td><td>Partial wakeup ADC analog 5 input pin</td><td>62</td><td>86</td><td>105</td><td></td></tr><tr><td>PWU_AN6</td><td>Partial wakeup ADC analog 6 input pin</td><td>63</td><td>87</td><td>106</td><td></td></tr><tr><td>PWU_AN7</td><td>Partial wakeup ADC analog 7 input pin</td><td>-</td><td>88</td><td>107</td><td></td></tr><tr><td>PWUTRG_0</td><td>Partial wakeup trigger output pin (0)</td><td>-</td><td>-</td><td>130</td><td></td></tr><tr><td>PWUTRG_1</td><td>Partial wakeup trigger output pin (1)</td><td>74</td><td>107</td><td>131</td><td></td></tr></table>	Port Name	Description	Pin No. of Package			Remark	LQFP 100	LQFP/ 144	TEQFP 176	PWU_AN0	Partial wakeup ADC analog 0 input pin	54	78	97		PWU_AN1	Partial wakeup ADC analog 1 input pin	55	79	98		PWU_AN2	Partial wakeup ADC analog 2 input pin	56	80	99		PWU_AN3	Partial wakeup ADC analog 3 input pin	57	81	100		PWU_AN4	Partial wakeup ADC analog 4 input pin	61	85	104		PWU_AN5	Partial wakeup ADC analog 5 input pin	62	86	105		PWU_AN6	Partial wakeup ADC analog 6 input pin	63	87	106		PWU_AN7	Partial wakeup ADC analog 7 input pin	-	88	107		PWUTRG_0	Partial wakeup trigger output pin (0)	-	-	130		PWUTRG_1	Partial wakeup trigger output pin (1)	74	107	131	
Port Name	Description	Pin No. of Package			Remark																																																																		
		LQFP 100	LQFP/ 144	TEQFP 176																																																																			
PWU_AN0	Partial wakeup ADC analog 0 input pin	54	78	97																																																																			
PWU_AN1	Partial wakeup ADC analog 1 input pin	55	79	98																																																																			
PWU_AN2	Partial wakeup ADC analog 2 input pin	56	80	99																																																																			
PWU_AN3	Partial wakeup ADC analog 3 input pin	57	81	100																																																																			
PWU_AN4	Partial wakeup ADC analog 4 input pin	61	85	104																																																																			
PWU_AN5	Partial wakeup ADC analog 5 input pin	62	86	105																																																																			
PWU_AN6	Partial wakeup ADC analog 6 input pin	63	87	106																																																																			
PWU_AN7	Partial wakeup ADC analog 7 input pin	-	88	107																																																																			
PWUTRG_0	Partial wakeup trigger output pin (0)	-	-	130																																																																			
PWUTRG_1	Partial wakeup trigger output pin (1)	74	107	131																																																																			

Page	Section	Change Results
47	6.Block Diagram	The shading parts added as below. Figure 6-1 Block Diagram Common PERI #1

Page	Section	Change Results																																																																																																																																																																																															
54	7. Electrical Characteristics 7.3 DC Characteristics	The shading parts added as below. (T_A: -40 °C to +105 °C, VCC=AVCC=5.0 V±0.5 V/ VCC=AVCC=3.3 V±0.3 V, VSS=AVSS=0.0 V) <table><tr><th>Parameter</th><th>Symbol</th><th>Pin Name</th><th colspan="2">*3</th><th colspan="3">Value</th><th>Unit</th><th>Remarks</th></tr><tr><th></th><th></th><th></th><th colspan="2">Conditions</th><th>Min</th><th>Typ</th><th>Max</th><th></th><th></th></tr><tr><td rowspan="30">Power supply current</td><td rowspan="6">I_{CCS}</td><td rowspan="27">V_{CC}</td><td colspan="2">Normal operation</td><td>-</td><td>85</td><td>120</td><td>mA</td><td>Operating at 132 MHz, HPM 33 MHz, Peripheral 33 MHz^{*1}</td></tr><tr><td colspan="2">Work Flash write/erase</td><td>-</td><td>105</td><td>140</td><td>mA</td><td>Operating at 132 MHz, HPM 33 MHz, Peripheral 33 MHz^{*1}</td></tr><tr><td colspan="2">TC Flash write/erase</td><td>-</td><td>105</td><td>140</td><td>mA</td><td>Operating at 132 MHz, HPM 33 MHz, Peripheral 33 MHz^{*1}</td></tr><tr><td colspan="2">Normal operation</td><td>-</td><td>70</td><td>105</td><td>mA</td><td>Operating at 80 MHz, HPM 40 MHz, Peripheral 40 MHz</td></tr><tr><td colspan="2">Work Flash write/erase</td><td>-</td><td>90</td><td>125</td><td>mA</td><td>Operating at 80 MHz, HPM 40 MHz, Peripheral 40 MHz</td></tr><tr><td colspan="2">TC Flash write/erase</td><td>-</td><td>90</td><td>125</td><td>mA</td><td>Operating at 80 MHz, HPM 40 MHz, Peripheral 40 MHz</td></tr><tr><td rowspan="2">I_{CCS5}</td><td colspan="2" rowspan="2">CPU sleep</td><td>-</td><td>55</td><td>95</td><td>mA</td><td>Operating at 132 MHz, HPM 33 MHz, Peripheral 33 MHz^{*1}</td></tr><tr><td>-</td><td>45</td><td>85</td><td>mA</td><td>Operating at 80 MHz, HPM 40 MHz, Peripheral 40 MHz</td></tr><tr><td rowspan="6">I_{CC75}</td><td colspan="2" rowspan="6">Timer mode</td><td rowspan="3">Fast CR ON</td><td>-</td><td>1495</td><td>2905</td><td>μA</td><td>T_A=25 °C, When using 4 MHz crystal for main oscillator.</td></tr><tr><td>-</td><td>1300</td><td>2520</td><td>μA</td><td>T_A=25 °C, When using Slow-CR source oscillation.</td></tr><tr><td>-</td><td>1300</td><td>2540</td><td>μA</td><td>T_A=25 °C, When using 32 kHz sub source oscillation.</td></tr><tr><td rowspan="3">Fast CR OFF ^{*4}</td><td>-</td><td>1295</td><td>2605</td><td>μA</td><td>T_A=25 °C, When using 4 MHz crystal for main oscillator.</td></tr><tr><td>-</td><td>1100</td><td>2220</td><td>μA</td><td>T_A=25 °C, When using Slow-CR source oscillation.</td></tr><tr><td>-</td><td>1100</td><td>2240</td><td>μA</td><td>T_A=25 °C, When using 32 kHz sub source oscillation.</td></tr><tr><td rowspan="2">I_{CC85}</td><td colspan="2" rowspan="2">Stop mode</td><td>Fast CR ON</td><td>-</td><td>1300</td><td>2520</td><td>μA</td><td>T_A=25 °C</td></tr><tr><td>Fast CR OFF ^{*4}</td><td>-</td><td>1100</td><td>2220</td><td>μA</td><td>T_A=25 °C</td></tr><tr><td rowspan="2">I_{CCP}</td><td colspan="2" rowspan="2">PWU mode ^{*4} (Shutdown)</td><td>-</td><td>65</td><td>130</td><td>μA</td><td>T_A=25 °C (PWU operation cycle 16 ms)</td></tr><tr><td>-</td><td>55</td><td>115</td><td>μA</td><td>T_A=25 °C (PWU operation cycle 32 ms)</td></tr><tr><td rowspan="6">I_{CC752}</td><td colspan="2" rowspan="6">Timer mode (Shutdown)</td><td rowspan="3">Fast CR ON</td><td>-</td><td>520</td><td>830</td><td>μA</td><td>T_A=25 °C, When using 4 MHz crystal for main oscillator.</td></tr><tr><td>-</td><td>245</td><td>400</td><td>μA</td><td>T_A=25 °C, When using Slow-CR source oscillation.</td></tr><tr><td>-</td><td>255</td><td>420</td><td>μA</td><td>T_A=25 °C, When using 32 kHz sub source oscillation.</td></tr><tr><td rowspan="3">Fast CR OFF ^{*4}</td><td>-</td><td>320</td><td>530</td><td>μA</td><td>T_A=25 °C, When using 4 MHz crystal for main oscillator.</td></tr><tr><td>-</td><td>45</td><td>100</td><td>μA</td><td>T_A=25 °C, When using Slow-CR source oscillation.</td></tr><tr><td>-</td><td>55</td><td>120</td><td>μA</td><td>T_A=25 °C, When using 32 kHz sub source oscillation.</td></tr><tr><td rowspan="2">I_{CC852}</td><td colspan="2" rowspan="2">Stop mode (Shutdown)</td><td>Fast CR ON</td><td>-</td><td>245</td><td>395</td><td>μA</td><td>T_A=25 °C</td></tr><tr><td>Fast CR OFF ^{*4}</td><td>-</td><td>45</td><td>95</td><td>μA</td><td>T_A=25 °C</td></tr></table>	Parameter	Symbol	Pin Name	*3		Value			Unit	Remarks				Conditions		Min	Typ	Max			Power supply current	I _{CCS}	V _{CC}	Normal operation		-	85	120	mA	Operating at 132 MHz, HPM 33 MHz, Peripheral 33 MHz ^{*1}	Work Flash write/erase		-	105	140	mA	Operating at 132 MHz, HPM 33 MHz, Peripheral 33 MHz ^{*1}	TC Flash write/erase		-	105	140	mA	Operating at 132 MHz, HPM 33 MHz, Peripheral 33 MHz ^{*1}	Normal operation		-	70	105	mA	Operating at 80 MHz, HPM 40 MHz, Peripheral 40 MHz	Work Flash write/erase		-	90	125	mA	Operating at 80 MHz, HPM 40 MHz, Peripheral 40 MHz	TC Flash write/erase		-	90	125	mA	Operating at 80 MHz, HPM 40 MHz, Peripheral 40 MHz	I _{CCS5}	CPU sleep		-	55	95	mA	Operating at 132 MHz, HPM 33 MHz, Peripheral 33 MHz ^{*1}	-	45	85	mA	Operating at 80 MHz, HPM 40 MHz, Peripheral 40 MHz	I _{CC75}	Timer mode		Fast CR ON	-	1495	2905	μA	T _A =25 °C, When using 4 MHz crystal for main oscillator.	-	1300	2520	μA	T _A =25 °C, When using Slow-CR source oscillation.	-	1300	2540	μA	T _A =25 °C, When using 32 kHz sub source oscillation.	Fast CR OFF ^{*4}	-	1295	2605	μA	T _A =25 °C, When using 4 MHz crystal for main oscillator.	-	1100	2220	μA	T _A =25 °C, When using Slow-CR source oscillation.	-	1100	2240	μA	T _A =25 °C, When using 32 kHz sub source oscillation.	I _{CC85}	Stop mode		Fast CR ON	-	1300	2520	μA	T _A =25 °C	Fast CR OFF ^{*4}	-	1100	2220	μA	T _A =25 °C	I _{CCP}	PWU mode ^{*4} (Shutdown)		-	65	130	μA	T _A =25 °C (PWU operation cycle 16 ms)	-	55	115	μA	T _A =25 °C (PWU operation cycle 32 ms)	I _{CC752}	Timer mode (Shutdown)		Fast CR ON	-	520	830	μA	T _A =25 °C, When using 4 MHz crystal for main oscillator.	-	245	400	μA	T _A =25 °C, When using Slow-CR source oscillation.	-	255	420	μA	T _A =25 °C, When using 32 kHz sub source oscillation.	Fast CR OFF ^{*4}	-	320	530	μA	T _A =25 °C, When using 4 MHz crystal for main oscillator.	-	45	100	μA	T _A =25 °C, When using Slow-CR source oscillation.	-	55	120	μA	T _A =25 °C, When using 32 kHz sub source oscillation.	I _{CC852}	Stop mode (Shutdown)		Fast CR ON	-	245	395	μA	T _A =25 °C	Fast CR OFF ^{*4}	-	45	95	μA	T _A =25 °C
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40 MHz, Peripheral 40 MHz		Work Flash write/erase	-	90	175	mA	Operating at 80 MHz, HPM 40 MHz, Peripheral 40 MHz		TC Flash write/erase	-	90	175	mA	Operating at 80 MHz, HPM 40 MHz, Peripheral 40 MHz		I _{CCS5}	CPU sleep	-	55	155	mA	Operating at 132 MHz, HPM 33 MHz, Peripheral 33 MHz ^{*2}		-	45	135	mA	Operating at 80 MHz, HPM 40 MHz, Peripheral 40 MHz		I _{CC75}	Timer mode	Fast CR ON	-	1495	2905	μA	T _A =25 °C, When using 4 MHz crystal for main oscillator.		-	1300	2520	μA	T _A =25 °C, When using Slow-CR source oscillation.		-	1300	2540	μA	T _A =25 °C, When using 32 kHz sub source oscillation.		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I _{CC752}	Stop mode (Shutdown)	Fast CR ON	-	245	395	μA	T _A =25 °C	BackupRAM 12 KB retention.	Fast CR OFF ^{*4}	-	45	95	μA	T _A =25 °C
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					-	1100	2240	μA	T _A =25 °C, When using 32 kHz sub source oscillation.																																																																																																																																																																																									
	I _{CC75}		Stop mode	Fast CR ON	-	1300	2520	μA	T _A =25 °C																																																																																																																																																																																									
				Fast CR OFF ^{*4}	-	1100	2220	μA	T _A =25 °C																																																																																																																																																																																									
	I _{CCP}		PWU mode ^{*4} (Shutdown)	-	65	130	μA	T _A =25 °C (PWU operation cycle 16 ms)																																																																																																																																																																																										
				-	55	115	μA	T _A =25 °C (PWU operation cycle 32 ms)																																																																																																																																																																																										
	I _{CC752}		Timer mode (Shutdown)	Fast CR ON	-	520	830	μA	T _A =25 °C, When using 4 MHz crystal for main oscillator.	RTC operation, BackupRAM 12 KB retention.																																																																																																																																																																																								
					-	245	400	μA	T _A =25 °C, When using Slow-CR source oscillation.																																																																																																																																																																																									
					-	255	420	μA	T _A =25 °C, When using 32 kHz sub source oscillation.																																																																																																																																																																																									
				Fast CR OFF ^{*4}	-	320	530	μA	T _A =25 °C, When using 4 MHz crystal for main oscillator.																																																																																																																																																																																									
					-	45	100	μA	T _A =25 °C, When using Slow-CR source oscillation.																																																																																																																																																																																									
					-	55	120	μA	T _A =25 °C, When using 32 kHz sub source oscillation.																																																																																																																																																																																									
	I _{CC752}		Stop mode (Shutdown)	Fast CR ON	-	245	395	μA	T _A =25 °C	BackupRAM 12 KB retention.																																																																																																																																																																																								
				Fast CR OFF ^{*4}	-	45	95	μA	T _A =25 °C																																																																																																																																																																																									
	*2. It is a condition that can be used by limiting the product type of TEQFP.																																																																																																																																																																																																	
	*3: Corresponding mode sets for state definitions are described in the chapter of "State Transition" in S6J3400 Series hardware manual.																																																																																																																																																																																																	
	*4: PSS mode has some restrictions. For details, see the "Restriction" of chapter "Product Description" in S6J3400 Series hardware manual.																																																																																																																																																																																																	

Page	Section	Change Results																
Rev. *I																		
51	7. Electrical Characteristics 7.3 DC Characteristics	- Added the P322, P323, P324 and P331. - Arranged Pin Name. Error) <table border="1"> <thead> <tr> <th>Parameter</th><th>Symbol</th><th>Pin Name</th></tr> </thead> <tbody> <tr> <td rowspan="3">H" level output voltage</td><td>V_{OH4}</td><td rowspan="3"> P000 to P009, P010 to P029, P030, P031, P100 to P129, P130, P131, P200 to P219, P220 to P229, P230, P231, P300 to P319, P320, P321, P325 to P329, P330, P400 to P419, P420 to P422 </td></tr> <tr> <td>V_{OH5}</td></tr> <tr> <td>V_{OH6}</td></tr> </tbody> </table> Correct) <table border="1"> <thead> <tr> <th>Parameter</th><th>Symbol</th><th>Pin Name</th></tr> </thead> <tbody> <tr> <td rowspan="3">H" level output voltage</td><td>V_{OH4}</td><td rowspan="3"> P000 to P031, P100 to P131, P200 to P231, P300 to P331, P400 to P422 </td></tr> <tr> <td>V_{OH5}</td></tr> <tr> <td>V_{OH6}</td></tr> </tbody> </table>	Parameter	Symbol	Pin Name	H" level output voltage	V _{OH4}	P000 to P009, P010 to P029, P030, P031, P100 to P129, P130, P131, P200 to P219, P220 to P229, P230, P231, P300 to P319, P320, P321, P325 to P329, P330, P400 to P419, P420 to P422	V _{OH5}	V _{OH6}	Parameter	Symbol	Pin Name	H" level output voltage	V _{OH4}	P000 to P031, P100 to P131, P200 to P231, P300 to P331, P400 to P422	V _{OH5}	V _{OH6}
Parameter	Symbol	Pin Name																
H" level output voltage	V _{OH4}	P000 to P009, P010 to P029, P030, P031, P100 to P129, P130, P131, P200 to P219, P220 to P229, P230, P231, P300 to P319, P320, P321, P325 to P329, P330, P400 to P419, P420 to P422																
	V _{OH5}																	
	V _{OH6}																	
Parameter	Symbol	Pin Name																
H" level output voltage	V _{OH4}	P000 to P031, P100 to P131, P200 to P231, P300 to P331, P400 to P422																
	V _{OH5}																	
	V _{OH6}																	

Page	Section	Change Results																
51	7. Electrical Characteristics 7.3 DC Characteristics	- Added the P322, P323, P324 and P331. - Arranged Pin Name. Error) <table border="1"> <thead> <tr> <th>Parameter</th><th>Symbol</th><th>Pin Name</th></tr> </thead> <tbody> <tr> <td rowspan="3">"L" level output voltage</td><td>V_{OL4}</td><td rowspan="3"> P000 to P009, P010 to P029, P030, P031, P100 to P129, P130, P131, P200 to P219, P220 to P229, P230, P231, P300 to P319, P320, P321, P325 to P329, P330, P400 to P419, P420 to P422 </td></tr> <tr> <td>V_{OL5}</td></tr> <tr> <td>V_{OL6}</td></tr> </tbody> </table> Correct) <table border="1"> <thead> <tr> <th>Parameter</th><th>Symbol</th><th>Pin Name</th></tr> </thead> <tbody> <tr> <td rowspan="3">"L" level output voltage</td><td>V_{OL4}</td><td rowspan="3"> P000 to P031, P100 to P131, P200 to P231, P300 to P331, P400 to P422 </td></tr> <tr> <td>V_{OL5}</td></tr> <tr> <td>V_{OL6}</td></tr> </tbody> </table>	Parameter	Symbol	Pin Name	"L" level output voltage	V _{OL4}	P000 to P009, P010 to P029, P030, P031, P100 to P129, P130, P131, P200 to P219, P220 to P229, P230, P231, P300 to P319, P320, P321, P325 to P329, P330, P400 to P419, P420 to P422	V _{OL5}	V _{OL6}	Parameter	Symbol	Pin Name	"L" level output voltage	V _{OL4}	P000 to P031, P100 to P131, P200 to P231, P300 to P331, P400 to P422	V _{OL5}	V _{OL6}
Parameter	Symbol	Pin Name																
"L" level output voltage	V _{OL4}	P000 to P009, P010 to P029, P030, P031, P100 to P129, P130, P131, P200 to P219, P220 to P229, P230, P231, P300 to P319, P320, P321, P325 to P329, P330, P400 to P419, P420 to P422																
	V _{OL5}																	
	V _{OL6}																	
Parameter	Symbol	Pin Name																
"L" level output voltage	V _{OL4}	P000 to P031, P100 to P131, P200 to P231, P300 to P331, P400 to P422																
	V _{OL5}																	
	V _{OL6}																	

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537. Electrical Characteristics7.3 DC Characteristics

Modified the shading parts as below.
Error)

(T_A: -40 °C to +105 °C, VCC=AVCC=5.0 V±0.5 V/ VCC=AVCC=3.3 V±0.3 V, VSS=AVSS=0.0 V)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks	
				Min	Typ	Max			
Power supply current	I _{CCS}	V _{CC}	Normal operation	-	85	120	mA	Operating at 132 MHz, HPM 33 MHz, Peripheral 33 MHz ^{*1}	
			Work Flash write/erase	-	105	140	mA	Operating at 132 MHz, HPM 33 MHz, Peripheral 33 MHz ^{*1}	
			TC Flash write/erase	-	105	140	mA	Operating at 132 MHz, HPM 33 MHz, Peripheral 33 MHz ^{*1}	
			Normal operation	-	70	105	mA	Operating at 80 MHz, HPM 40 MHz, Peripheral 40 MHz	
			Work Flash write/erase	-	90	125	mA	Operating at 80 MHz, HPM 40 MHz, Peripheral 40 MHz	
			TC Flash write/erase	-	90	125	mA	Operating at 80 MHz, HPM 40 MHz, Peripheral 40 MHz	
	I _{CCSS}	V _{CC}	CPU sleep	-	55	95	mA	Operating at 132 MHz, HPM 33 MHz, Peripheral 33 MHz ^{*1}	
				-	45	85	mA	Operating at 80 MHz, HPM 40 MHz, Peripheral 40 MHz	
	I _{CCT5}	V _{CC}	Timer mode	Fast CR ON	-	1495	2905	μA	T _A =25 °C, When using 4 MHz crystal for main oscillator.
					-	1300	2520	μA	T _A =25 °C, When using Slow-CR source oscillation.
					-	1300	2540	μA	T _A =25 °C, When using 32 kHz sub source oscillation.
				Fast CR OFF ^{*4}	-	1295	2605	μA	T _A =25 °C, When using 4 MHz crystal for main oscillator.
					-	1100	2220	μA	T _A =25 °C, When using Slow-CR source oscillation.
					-	1100	2240	μA	T _A =25 °C, When using 32 kHz sub source oscillation.

Correct)

(T_A: -40 °C to +105 °C, VCC=AVCC=5.0 V±0.5 V/ VCC=AVCC=3.3 V±0.3 V, VSS=AVSS=0.0 V)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks	
				Min	Typ	Max			
Power supply current	I _{CCS}	V _{CC}	Normal operation	-	50	110	mA	Operating at 132 MHz, HPM 33 MHz, Peripheral 33 MHz ^{*1}	
			Work Flash write/erase	-	70	130	mA	Operating at 132 MHz, HPM 33 MHz, Peripheral 33 MHz ^{*1}	
			TC Flash write/erase	-	70	130	mA	Operating at 132 MHz, HPM 33 MHz, Peripheral 33 MHz ^{*1}	
			Normal operation	-	45	105	mA	Operating at 80 MHz, HPM 40 MHz, Peripheral 40 MHz	
			Work Flash write/erase	-	65	125	mA	Operating at 80 MHz, HPM 40 MHz, Peripheral 40 MHz	
			TC Flash write/erase	-	65	125	mA	Operating at 80 MHz, HPM 40 MHz, Peripheral 40 MHz	
	I _{CCSS}	V _{CC}	CPU sleep	-	35	85	mA	Operating at 132 MHz, HPM 33 MHz, Peripheral 33 MHz ^{*1}	
				-	35	85	mA	Operating at 80 MHz, HPM 40 MHz, Peripheral 40 MHz	
	I _{CCT5}	V _{CC}	Timer mode	Fast CR ON	-	1190	2715	μA	T _A =25 °C, When using 4 MHz crystal for main oscillator.
					-	915	2305	μA	T _A =25 °C, When using Slow-CR source oscillation.
					-	925	2320	μA	T _A =25 °C, When using 32 kHz sub source oscillation.
				Fast CR OFF ^{*4}	-	990	2415	μA	T _A =25 °C, When using 4 MHz crystal for main oscillator.
					-	715	2005	μA	T _A =25 °C, When using Slow-CR source oscillation.
					-	725	2020	μA	T _A =25 °C, When using 32 kHz sub source oscillation.

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537. Electrical Characteristics
7.3 DC Characteristics

Modified the shading parts as below.

Error)

(T_A: -40 °C to +105 °C, VCC=AVCC=5.0 V±0.5 V/ VCC=AVCC=3.3 V±0.3 V, VSS=AVSS=0.0 V)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks	
				Min	Typ	Max			
Power supply current	I _{CCH5}	V _{CC}	Stop mode	Fast CR ON	-	1300	2520	μA	T _A =25 °C
				Fast CR OFF *4	-	1100	2220	μA	T _A =25 °C
	I _{CCP}		PWU mode *4 (Shutdown)		-	65	130	μA	T _A =25 °C (PWU operation cycle 16 ms)
					-	55	115	μA	T _A =25 °C (PWU operation cycle 32 ms)
	I _{CC52}		Timer mode (Shutdown)	Fast CR ON	-	520	830	μA	T _A =25 °C, When using 4 MHz crystal for main oscillator.
					-	245	400	μA	T _A =25 °C, When using Slow-CR source oscillation.
					-	255	420	μA	T _A =25 °C, When using 32 kHz sub source oscillation.
				Fast CR OFF *4	-	320	530	μA	T _A =25 °C, When using 4 MHz crystal for main oscillator.
					-	45	100	μA	T _A =25 °C, When using Slow-CR source oscillation.
					-	55	120	μA	T _A =25 °C, When using 32 kHz sub source oscillation.
	I _{CCH52}		Stop mode (Shutdown)	Fast CR ON	-	245	395	μA	T _A =25 °C
				Fast CR OFF *4	-	45	95	μA	T _A =25 °C

Correct)

(T_A: -40 °C to +105 °C, VCC=AVCC=5.0 V±0.5 V/ VCC=AVCC=3.3 V±0.3 V, VSS=AVSS=0.0 V)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks	
				Min	Typ	Max			
Power supply current	I _{CCH5}	V _{CC}	Stop mode	Fast CR ON	-	915	2300	μA	T _A =25 °C
				Fast CR OFF *4	-	715	2000	μA	T _A =25 °C
	I _{CCP}		PWU mode *4 (Shutdown)		-	45	120	μA	T _A =25 °C (PWU operation cycle 16 ms)
					-	40	105	μA	T _A =25 °C (PWU operation cycle 32 ms)
	I _{CC52}		Timer mode (Shutdown)	Fast CR ON	-	515	790	μA	T _A =25 °C, When using 4 MHz crystal for main oscillator.
					-	235	390	μA	T _A =25 °C, When using Slow-CR source oscillation.
					-	245	405	μA	T _A =25 °C, When using 32 kHz sub source oscillation.
				Fast CR OFF *4	-	315	490	μA	T _A =25 °C, When using 4 MHz crystal for main oscillator.
					-	35	90	μA	T _A =25 °C, When using Slow-CR source oscillation.
					-	45	105	μA	T _A =25 °C, When using 32 kHz sub source oscillation.
	I _{CCH52}		Stop mode (Shutdown)	Fast CR ON	-	235	385	μA	T _A =25 °C
				Fast CR OFF *4	-	35	85	μA	T _A =25 °C

Page	Section	Change Results										
54	7. Electrical Characteristics 7.3 DC Characteristics	Modified the shading parts as below. Error) (T _A : -40 °C to +125 °C, VCC=AVCC=5.0 V±0.5 V/ VCC=AVCC=3.3 V±0.3 V, VSS=AVSS=0.0 V)										
Parameter		Symbol	Pin Name	Conditions		Value			Unit	Remarks		
						Min	Typ	Max				
Power supply current	I _{CCS}			Normal operation		-	85	175	mA	Operating at 132 MHz, HPM 33 MHz, Peripheral 33 MHz ^{*2}		
				Work Flash write/erase		-	105	195	mA	Operating at 132 MHz, HPM 33 MHz, Peripheral 33 MHz ^{*2}		
				TC Flash write/erase		-	105	195	mA	Operating at 132 MHz, HPM 33 MHz, Peripheral 33 MHz ^{*2}		
				Normal operation		-	70	155	mA	Operating at 80 MHz, HPM 40 MHz, Peripheral 40 MHz		
				Work Flash write/erase		-	90	175	mA	Operating at 80 MHz, HPM 40 MHz, Peripheral 40 MHz		
				TC Flash write/erase		-	90	175	mA	Operating at 80 MHz, HPM 40 MHz, Peripheral 40 MHz		
	I _{CCSS}		V _{CC}	CPU sleep		-	55	155	mA	Operating at 132 MHz, HPM 33 MHz, Peripheral 33 MHz ^{*2}		
						-	45	135	mA	Operating at 80 MHz, HPM 40 MHz, Peripheral 40 MHz		
	I _{CCTS}			Timer mode	Fast CR ON	-	1495	2905	μA	T _A =25 °C, When using 4 MHz crystal for main oscillator.		
						-	1300	2520	μA	T _A =25 °C, When using Slow-CR source oscillation.		
						-	1300	2540	μA	T _A =25 °C, When using 32 kHz sub source oscillation.		
					Fast CR OFF ^{*4}	-	1295	2605	μA	T _A =25 °C, When using 4 MHz crystal for main oscillator.		
						-	1100	2220	μA	T _A =25 °C, When using Slow-CR source oscillation.		
						-	1100	2240	μA	T _A =25 °C, When using 32 kHz sub source oscillation.		
	Correct)											
	(T _A : -40 °C to +125 °C, VCC=AVCC=5.0 V±0.5 V/ VCC=AVCC=3.3 V±0.3 V, VSS=AVSS=0.0 V)											
	Parameter		Symbol	Pin Name	Conditions		Value			Unit	Remarks	
						Min	Typ	Max				
Power supply current	I _{CCS}			Normal operation		-	50	130	mA	Operating at 132 MHz, HPM 33 MHz, Peripheral 33 MHz ^{*2}		
				Work Flash write/erase		-	70	150	mA	Operating at 132 MHz, HPM 33 MHz, Peripheral 33 MHz ^{*2}		
				TC Flash write/erase		-	70	150	mA	Operating at 132 MHz, HPM 33 MHz, Peripheral 33 MHz ^{*2}		
				Normal operation		-	45	125	mA	Operating at 80 MHz, HPM 40 MHz, Peripheral 40 MHz		
				Work Flash write/erase		-	65	150	mA	Operating at 80 MHz, HPM 40 MHz, Peripheral 40 MHz		
				TC Flash write/erase		-	65	150	mA	Operating at 80 MHz, HPM 40 MHz, Peripheral 40 MHz		
	I _{CCSS}		V _{CC}	CPU sleep		-	35	110	mA	Operating at 132 MHz, HPM 33 MHz, Peripheral 33 MHz ^{*2}		
						-	35	110	mA	Operating at 80 MHz, HPM 40 MHz, Peripheral 40 MHz		
	I _{CCTS}			Timer mode	Fast CR ON	-	1190	2715	μA	T _A =25 °C, When using 4 MHz crystal for main oscillator.		
						-	915	2305	μA	T _A =25 °C, When using Slow-CR source oscillation.		
						-	925	2320	μA	T _A =25 °C, When using 32 kHz sub source oscillation.		
					Fast CR OFF ^{*4}	-	990	2415	μA	T _A =25 °C, When using 4 MHz crystal for main oscillator.		
						-	715	2005	μA	T _A =25 °C, When using Slow-CR source oscillation.		
						-	725	2020	μA	T _A =25 °C, When using 32 kHz sub source oscillation.		

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7. Electrical Characteristics

7.3 DC Characteristics

Modified the shading parts as below.
Error)

(T_A: -40 °C to +125 °C, VCC=AVCC=5.0 V±0.5 V/ VCC=AVCC=3.3 V±0.3 V, VSS=AVSS=0.0 V)

Parameter	Symbol	Pin Name	*3 Conditions		Value			Unit	Remarks	
					Min	Typ	Max			
Power supply current	I _{CH5}	V _{CC}	Stop mode	Fast CR ON	-	1300	2520	μA	T _A =25 °C	
				Fast CR OFF *4	-	1100	2220	μA	T _A =25 °C	
	I _{CCP}		PWU mode *4 (Shutdown)		-	65	130	μA	T _A =25 °C (PWU operation cycle 16 ms)	
					-	55	115	μA	T _A =25 °C (PWU operation cycle 32 ms)	
	I _{CH52}		Timer mode (Shutdown)	Fast CR ON	-	520	830	μA	T _A =25 °C, When using 4 MHz crystal for main oscillator.	
					-	245	400	μA	T _A =25 °C, When using Slow-CR source oscillation.	
					-	255	420	μA	T _A =25 °C, When using 32 kHz sub source oscillation.	
				Fast CR OFF *4	-	320	530	μA	T _A =25 °C, When using 4 MHz crystal for main oscillator.	
					-	45	100	μA	T _A =25 °C, When using Slow-CR source oscillation.	
					-	55	120	μA	T _A =25 °C, When using 32 kHz sub source oscillation.	
	I _{CH52}		Stop mode (Shutdown)	Fast CR ON	-	245	395	μA	T _A =25 °C	
				Fast CR OFF *4	-	45	95	μA	T _A =25 °C	

Correct)

(T_A: -40 °C to +125 °C, VCC=AVCC=5.0 V±0.5 V/ VCC=AVCC=3.3 V±0.3 V, VSS=AVSS=0.0 V)

Parameter	Symbol	Pin Name	*3 Conditions		Value			Unit	Remarks	
					Min	Typ	Max			
Power supply current	I _{CH5}	V _{CC}	Stop mode	Fast CR ON	-	915	2300	μA	T _A =25 °C	
				Fast CR OFF *4	-	715	2000	μA	T _A =25 °C	
	I _{CCP}		PWU mode *4 (Shutdown)		-	45	120	μA	T _A =25 °C (PWU operation cycle 16 ms)	
					-	40	105	μA	T _A =25 °C (PWU operation cycle 32 ms)	
	I _{CH52}		Timer mode (Shutdown)	Fast CR ON	-	515	790	μA	T _A =25 °C, When using 4 MHz crystal for main oscillator.	
					-	235	390	μA	T _A =25 °C, When using Slow-CR source oscillation.	
					-	245	405	μA	T _A =25 °C, When using 32 kHz sub source oscillation.	
				Fast CR OFF *4	-	315	490	μA	T _A =25 °C, When using 4 MHz crystal for main oscillator.	
					-	35	90	μA	T _A =25 °C, When using Slow-CR source oscillation.	
					-	45	105	μA	T _A =25 °C, When using 32 kHz sub source oscillation.	
	I _{CH52}		Stop mode (Shutdown)	Fast CR ON	-	235	385	μA	T _A =25 °C	
				Fast CR OFF *4	-	35	85	μA	T _A =25 °C	

Page	Section	Change Results																																														
59	7. Electrical Characteristics 7.4.4 Reset Input	Modified the shading parts as below. Error) <table><tr><th rowspan="2">Parameter</th><th rowspan="2">Symbol</th><th rowspan="2">Pin Name</th><th rowspan="2">Conditions</th><th colspan="2">Value</th><th rowspan="2">Unit</th><th rowspan="2">Remarks</th></tr><tr><th>Min</th><th>Max</th></tr><tr><td>Reset input time</td><td rowspan="2">t_{RSTL}</td><td rowspan="2">RSTX</td><td rowspan="2">-</td><td>10</td><td>-</td><td>μs</td><td></td></tr><tr><td>Width for reset input removal</td><td>1</td><td>-</td><td>μs</td><td></td></tr></table> Correct) <table><tr><th rowspan="2">Parameter</th><th rowspan="2">Symbol</th><th rowspan="2">Pin Name</th><th rowspan="2">Conditions</th><th colspan="2">Value</th><th rowspan="2">Unit</th><th rowspan="2">Remarks</th></tr><tr><th>Min</th><th>Max</th></tr><tr><td>Reset input time</td><td rowspan="2">t_{RSTL}</td><td rowspan="2">RSTX</td><td rowspan="2">-</td><td>10</td><td>-</td><td>μs</td><td></td></tr><tr><td>Reset input pulse filtered</td><td>-</td><td>1</td><td>μs</td><td></td></tr></table>	Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks	Min	Max	Reset input time	t _{RSTL}	RSTX	-	10	-	μs		Width for reset input removal	1	-	μs		Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks	Min	Max	Reset input time	t _{RSTL}	RSTX	-	10	-	μs		Reset input pulse filtered	-	1	μs	
Parameter	Symbol	Pin Name					Conditions	Value			Unit	Remarks																																				
			Min	Max																																												
Reset input time	t _{RSTL}	RSTX	-	10	-	μs																																										
Width for reset input removal				1	-	μs																																										
Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks																																									
				Min	Max																																											
Reset input time	t _{RSTL}	RSTX	-	10	-	μs																																										
Reset input pulse filtered				-	1	μs																																										

Page	Section	Change Results																																																																																																																										
92	7.6 Flash Memory 7.6.1 Electrical Characteristics	Modified the shading parts as below. Error) <table><thead><tr><th rowspan="2">Parameter</th><th colspan="3">Value</th><th rowspan="2">Unit</th><th rowspan="2">Remarks</th></tr><tr><th>Min</th><th>Typ</th><th>Max^{*3}</th></tr></thead><tbody><tr><td rowspan="3">Sector erase time</td><td>-</td><td>120</td><td>480</td><td>ms</td><td>Large sector^{*1} Internal preprogramming time included</td></tr><tr><td>-</td><td>120</td><td>480</td><td>ms</td><td>8-kB sector^{*1} Internal preprogramming time included</td></tr><tr><td>-</td><td>120</td><td>480</td><td>ms</td><td>4-kB sector^{*2} Internal preprogramming time included</td></tr><tr><td>32-bit write time(Program)</td><td>-</td><td>30</td><td>384</td><td>μs</td><td>System-level overhead time excluded^{*1}</td></tr><tr><td>64-bit write time(Program)</td><td>-</td><td>30</td><td>384</td><td>μs</td><td>System-level overhead time excluded^{*1}</td></tr><tr><td>256-bit write time(Program)</td><td>-</td><td>40</td><td>512</td><td>μs</td><td>System-level overhead time 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44	5.2 I/O Circuit Type	Modified the shading parts as below. Error) <table><tr><th>Type</th><th>Remark</th></tr><tr><td>L</td><td> - Main oscillation I/O - Feedback resistor = approx.1.0 MΩ </td></tr></table> Correct) <table><tr><th>Type</th><th>Remark</th></tr><tr><td>L</td><td> - Main oscillation I/O - Feedback resistor = approx.2.1 MΩ </td></tr></table>	Type	Remark	L	- Main oscillation I/O - Feedback resistor = approx.1.0 MΩ	Type	Remark	L	- Main oscillation I/O - Feedback resistor = approx.2.1 MΩ																																													
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51	7.3 DC Characteristics	Added the shading parts as below. <table><tr><th rowspan="2">Parameter</th><th rowspan="2">Symbol</th><th rowspan="2">Pin Name</th><th rowspan="2">Conditions</th><th colspan="3">Value</th><th rowspan="2">Unit</th><th rowspan="2">Remarks</th></tr><tr><th>Min</th><th>Typ</th><th>Max</th></tr><tr><td rowspan="5">Hysteresis voltage</td><td>V_{HYS4}</td><td>P000 to P031, P100 to P131, P200 to P231, P300 to P321, P325 to P331, P400 to P422</td><td>CMOS hysteresis input level is selected</td><td>-</td><td>0.05×V_{CC}</td><td>-</td><td>V</td><td></td></tr><tr><td>V_{HYS5}</td><td></td><td>Automotive input level is selected</td><td>-</td><td>0.03×V_{CC}</td><td>-</td><td>V</td><td></td></tr><tr><td>V_{HYS9}</td><td>RSTX, NMIX</td><td>-</td><td>-</td><td>0.05×V_{CC}</td><td>-</td><td>V</td><td></td></tr><tr><td>V_{HYS10}</td><td>MD</td><td>-</td><td>-</td><td>0.05×V_{CC}</td><td>-</td><td>V</td><td></td></tr><tr><td>V_{HYS11}</td><td>TRST, TCK, TDI, TMS</td><td>-</td><td>-</td><td>0.035</td><td>-</td><td>V</td><td></td></tr></table>	Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks	Min	Typ	Max	Hysteresis voltage	V _{HYS4}	P000 to P031, P100 to P131, P200 to P231, P300 to P321, P325 to P331, P400 to P422	CMOS hysteresis input level is selected	-	0.05×V _{CC}	-	V		V _{HYS5}		Automotive input level is selected	-	0.03×V _{CC}	-	V		V _{HYS9}	RSTX, NMIX	-	-	0.05×V _{CC}	-	V		V _{HYS10}	MD	-	-	0.05×V _{CC}	-	V		V _{HYS11}	TRST, TCK, TDI, TMS	-	-	0.035	-	V	
Parameter	Symbol	Pin Name					Conditions	Value				Unit	Remarks																																										
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	V _{HYS11}	TRST, TCK, TDI, TMS	-	-	0.035	-	V																																																

Page

Section

93

7.6.1 Electrical Characteristics

Change Results

Deleted the shading parts as below.

Error)

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Sector erase time	-	120	180	ms	Large sector ^{*1} Internal preprogramming time included
	-	120	180	ms	8-kB sector ^{*1} Internal preprogramming time included
	-	120	180	ms	4-kB sector ^{*2} Internal preprogramming time included
32-bit write time(Program)	-	30	60	μs	System-level overhead time excluded ^{*1}
64-bit write time(Program)	-	30	60	μs	System-level overhead time excluded ^{*1}
256-bit write time(Program)	-	40	70	μs	System-level overhead time excluded ^{*1}
32-bit write time(Work)	-	30	60	μs	System-level overhead time excluded ^{*2}
Erase count ^{*2} / Data retention time ^{*3} (Program)	1,000/20 years	-	-	-	Temperature at write/erase time Average temperature T _A =+85 degrees Celsius
Erase count ^{*2} / Data retention time ^{*3} (Work)	1,000/20 years 10,000/10 years 100,000/5 years	-	-	-	Temperature at write/erase time Average temperature T _A =+85 degrees Celsius

*1: Guaranteed value for up to 1,000 erases

*2: Guaranteed value for up to 100,000 erases

*3: Target value

Correct)

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Sector erase time	-	120	180	ms	Large sector ^{*1} Internal preprogramming time included
	-	120	180	ms	8-kB sector ^{*1} Internal preprogramming time included
	-	120	180	ms	4-kB sector ^{*2} Internal preprogramming time included
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64-bit write time(Program)	-	30	60	μs	System-level overhead time excluded ^{*1}
256-bit write time(Program)	-	40	70	μs	System-level overhead time excluded ^{*1}
32-bit write time(Work)	-	30	60	μs	System-level overhead time excluded ^{*2}
Erase count / Data retention time (Program)	1,000/20 years	-	-	-	Temperature at write/erase time Average temperature T _A =+85 degrees Celsius
Erase count / Data retention time (Work)	1,000/20 years 10,000/10 years 100,000/5 years	-	-	-	Temperature at write/erase time Average temperature T _A =+85 degrees Celsius

*1: Guaranteed value for up to 1,000 erases

*2: Guaranteed value for up to 100,000 erases

Page	Section	Change Results														
94	8. Ordering Information	Updated the shading parts as below. [LQI100] Error) <table><tr><th>Part Number</th><th>Package</th></tr><tr><td>S6J342AFSXxxxxxx</td><td rowspan="4">LQI100 (100-pin 0.5-mm pitch Plastic LQFP)</td></tr><tr><td>S6J342AFUXxxxxxx</td></tr><tr><td></td></tr><tr><td>S6J3428FVXxxxxxx</td></tr></table> Correct) <table><tr><th>Part Number</th><th>Package</th></tr><tr><td>S6J342AFSBSV20000</td><td rowspan="4">LQI100 (100-pin 0.5-mm pitch Plastic LQFP)</td></tr><tr><td>S6J342AFTBSV20000</td></tr><tr><td>S6J342AFUBSV20000</td></tr><tr><td>S6J3428FVBSV20000</td></tr></table>	Part Number	Package	S6J342AFSXxxxxxx	LQI100 (100-pin 0.5-mm pitch Plastic LQFP)	S6J342AFUXxxxxxx		S6J3428FVXxxxxxx	Part Number	Package	S6J342AFSBSV20000	LQI100 (100-pin 0.5-mm pitch Plastic LQFP)	S6J342AFTBSV20000	S6J342AFUBSV20000	S6J3428FVBSV20000
Part Number	Package															
S6J342AFSXxxxxxx	LQI100 (100-pin 0.5-mm pitch Plastic LQFP)															
S6J342AFUXxxxxxx																
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S6J342AFSBSV20000	LQI100 (100-pin 0.5-mm pitch Plastic LQFP)															
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S6J3428FVBSV20000																
94	8. Ordering Information	Deleted the shading parts as below. [Lxx144] <table><tr><th>Part Number</th><th>Package</th></tr><tr><td>S6J342AHSXxxxxxx</td><td rowspan="4">Lxx144 (144-pin 0.4-mm pitch Plastic LQFP)</td></tr><tr><td>S6J342AHUXxxxxxx</td></tr><tr><td></td></tr><tr><td>S6J3428HVXxxxxxx</td></tr></table> For LQFP144 (0.4-mm pitch) package product, contact your sales representative.	Part Number	Package	S6J342AHSXxxxxxx	Lxx144 (144-pin 0.4-mm pitch Plastic LQFP)	S6J342AHUXxxxxxx		S6J3428HVXxxxxxx							
Part Number	Package															
S6J342AHSXxxxxxx	Lxx144 (144-pin 0.4-mm pitch Plastic LQFP)															
S6J342AHUXxxxxxx																
S6J3428HVXxxxxxx																

Page	Section	Change Results																
94	8. Ordering Information	Updated the shading parts as below. [LQS144] Error) <table><tr><th>Part Number</th><th>Package</th></tr><tr><td>S6J342AHSXxxxxxx</td><td rowspan="4">LQS144 (144-pin 0.5-mm pitch Plastic LQFP)</td></tr><tr><td>S6J342AHUXxxxxxx</td></tr><tr><td> </td></tr><tr><td>S6J3428HVXxxxxxx</td></tr></table> Correct) <table><tr><th>Part Number</th><th>Package</th></tr><tr><td>S6J342AHSBSV20000</td><td rowspan="6">LQS144 (144-pin 0.5-mm pitch Plastic LQFP)</td></tr><tr><td>S6J342AHTBSV20000</td></tr><tr><td>S6J342AHUBSV20000</td></tr><tr><td>S6J342AHVBSV20000</td></tr><tr><td>S6J3429HUBSV20000</td></tr><tr><td>S6J3429HVBSV20000</td></tr></table>	Part Number	Package	S6J342AHSXxxxxxx	LQS144 (144-pin 0.5-mm pitch Plastic LQFP)	S6J342AHUXxxxxxx		S6J3428HVXxxxxxx	Part Number	Package	S6J342AHSBSV20000	LQS144 (144-pin 0.5-mm pitch Plastic LQFP)	S6J342AHTBSV20000	S6J342AHUBSV20000	S6J342AHVBSV20000	S6J3429HUBSV20000	S6J3429HVBSV20000
Part Number	Package																	
S6J342AHSXxxxxxx	LQS144 (144-pin 0.5-mm pitch Plastic LQFP)																	
S6J342AHUXxxxxxx																		
S6J3428HVXxxxxxx																		
Part Number	Package																	
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S6J342AHVBSV20000																		
S6J3429HUBSV20000																		
S6J3429HVBSV20000																		
94	8. Ordering Information	Updated the shading parts as below. [LEH176] Error) <table><tr><th>Part Number</th><th>Package</th></tr><tr><td>S6J342AJSXxxxxxx</td><td rowspan="4">LEH176 (176-pin 0.5-mm pitch Plastic TEQFP)</td></tr><tr><td>S6J342AJUXxxxxxx</td></tr><tr><td> </td></tr><tr><td>S6J3428JVXxxxxxx</td></tr></table> Correct) <table><tr><th>Part Number</th><th>Package</th></tr><tr><td>S6J342AJSBSE20000</td><td rowspan="2">LEH176 (176-pin 0.5-mm pitch Plastic TEQFP)</td></tr><tr><td>S6J342AJTBSE20000</td></tr></table>	Part Number	Package	S6J342AJSXxxxxxx	LEH176 (176-pin 0.5-mm pitch Plastic TEQFP)	S6J342AJUXxxxxxx		S6J3428JVXxxxxxx	Part Number	Package	S6J342AJSBSE20000	LEH176 (176-pin 0.5-mm pitch Plastic TEQFP)	S6J342AJTBSE20000				
Part Number	Package																	
S6J342AJSXxxxxxx	LEH176 (176-pin 0.5-mm pitch Plastic TEQFP)																	
S6J342AJUXxxxxxx																		
S6J3428JVXxxxxxx																		
Part Number	Package																	
S6J342AJSBSE20000	LEH176 (176-pin 0.5-mm pitch Plastic TEQFP)																	
S6J342AJTBSE20000																		

Page	Section	Change Results
Rev. *K		
96 to 97	11. Errata	Added the "11.Errata" section.
Rev. *L		
13	3. Handling Devices	Added the shading parts as below. Correct) Points to Note about Using External Clocks External clocks are not supported. External direct clock input cannot be used.
55	7.4.3 Internal Clock Timing	Added the shading parts as below. Error) *1: Target maximum clock frequencies when CPU clock is 132 MHz *2: Target maximum clock frequencies when CPU clock is 80 MHz Correct) *1: Target maximum clock frequencies when CPU clock is 132 MHz with the TEQFP package *2: Target maximum clock frequencies when CPU clock is 80 MHz with the LQFP package
Rev. *M		
96, 97, 98	11. Errata	Added about CAN FD controller message order inversion when transmitting from dedicated Tx Buffers configured with same Message ID
Rev. *N		
96, 98, 99	11. Errata	Added CAN FD incomplete description of Dedicated Tx Buffers and Tx Queue related to transmission from multiple buffers configured with the same Message ID

NOTE: Please see "Document History" for later revised information.

Document History

Document Title: S6J3400 Series 32-bit Arm® Cortex®-R5F TRAVEO™ T1G Microcontroller

Document Number: 001-97829

Revision	ECN	Submission Date	Description of Change
**	4790224	08/05/2015	New datasheet.
*A	4976602	11/03/2015	Modified the datasheet to be Advance instead of Preliminary Modified title to include the part series instead of individual part numbers Moved the Acronyms table to the end of the document Added section 1.3. Precautions and Handling Devices Modified 6.3 AC Characteristics and 6.4 A/D Converter Modified 4-1 Block Diagram Modified 1.2.1 Basic Option Modified 7.Ordering Information
*B	5257213	05/05/2016	Removed Spansion from the content. Modified content for better clarity.
*C	5278808	05/20/2016	Modified some sentences. For details, please see "Major Changes".
*D	5390104	08/04/2016	Modified some sentences. For details, please see "Major Changes".
*E	5404891	08/16/2016	Added Errata.
*F	5436370	09/14/2016	Modified some sentences. For details, please see "Major Changes".
*G	5611948	01/31/2017	Modified some sentences. For details, please see "Major Changes".
*H	5710830	05/09/2017	Removed Preliminary status. Modified some sentences. For details, please see "Major Changes".
*I	5962312	11/09/2017	Modified some sentences. For details, please see "Major Changes".
*J	6205388	06/13/2018	Modified some sentences. For details, please see "Major Changes".
*K	6295504	08/30/2018	Added the "11.Errata" section.
*L	6676299	09/18/2019	Modified some sentences. For details, please see "Major Changes".
*M	7101746	03/18/2021	Updated 11. Errata For details, see 12. Major Changes.
*N	7388124	10/25/2021	Updated 11. Errata For details, see 12. Major Changes.

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