SUPPLEMENT

S29GL-S (S Models)

3V Flash with Page Mode featuring 65 nm MirrorBit® Process Technology Permanent Sector Lock Security Device Documentation

General Description

This supplementary document provides information on a device designed for limited distribution. It describes how the features, operation, and ordering options of this device have been enhanced or changed from the standard device on which it is based. The information contained in this document modifies any information on the same topics established by the data sheets listed in the Affected Documents/Related Documents table and should be used in conjunction with those documents. This document may also contain information that was not previously covered by the S29GL-S data sheet. It is intended for hardware system designers and software developers of applications, operating systems, or tools.

Affected Documents/Related Documents

Title	Publication Number
S29GL-S MirrorBit® Flash Family Data Sheet	S29GL_128S_01GS_00

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1. Device Description

1.1 Permanent Sector Lock Algorithm Feature Description

The device offers a unique Permanent Sector Lock Algorithm that allows the host system to permanently secure the data in any desired sectors of the memory array via a software command at V_{CC} supply levels. Initiating this software command sequence permanently disables both program and erase operations in any desired sectors. In Read Password Protection Mode, reads are also disabled to non-boot sectors. This feature protects the data in these areas from being programmed or erased (or read) in any way after this command has been activated. Sectors can be incrementally locked at any time and in any sequence.

2. Device Bus Operation Changed

None.

2.1 Device ID Changed

Permanent Sector Lock devices have three byte Device IDs. The Device ID (SA) + 000Eh is different from those found in standard S29GL-S devices. Customers can distinguish Standard and Permanent Sector Lock devices by reading the status of a Lock Register (See Section 4. for more details).

Table 1. ID (Autoselect) Address Map

Description	Address	Read Data
Device ID	(SA) + 0001h	227Eh
Device ID	(SA) + 000Eh	2240h = 1 Gb 2239h = 512 Mb 2238h = 256 Mb 2237h = 128 Mb
Device ID	(SA) + 000Fh	2201h

3. Advance Sector Protection Clarification

The Advance Sector Protection feature can disable programming or erase operations in any or all sectors, and can be implemented via software and/or hardware methods. Figure 1, Figure 2, and Figure 3 illustrate a high level logic diagram between the Persistent Protection Mode and Read Password Protection Mode.

Figure 1. Persistent Protection Mode

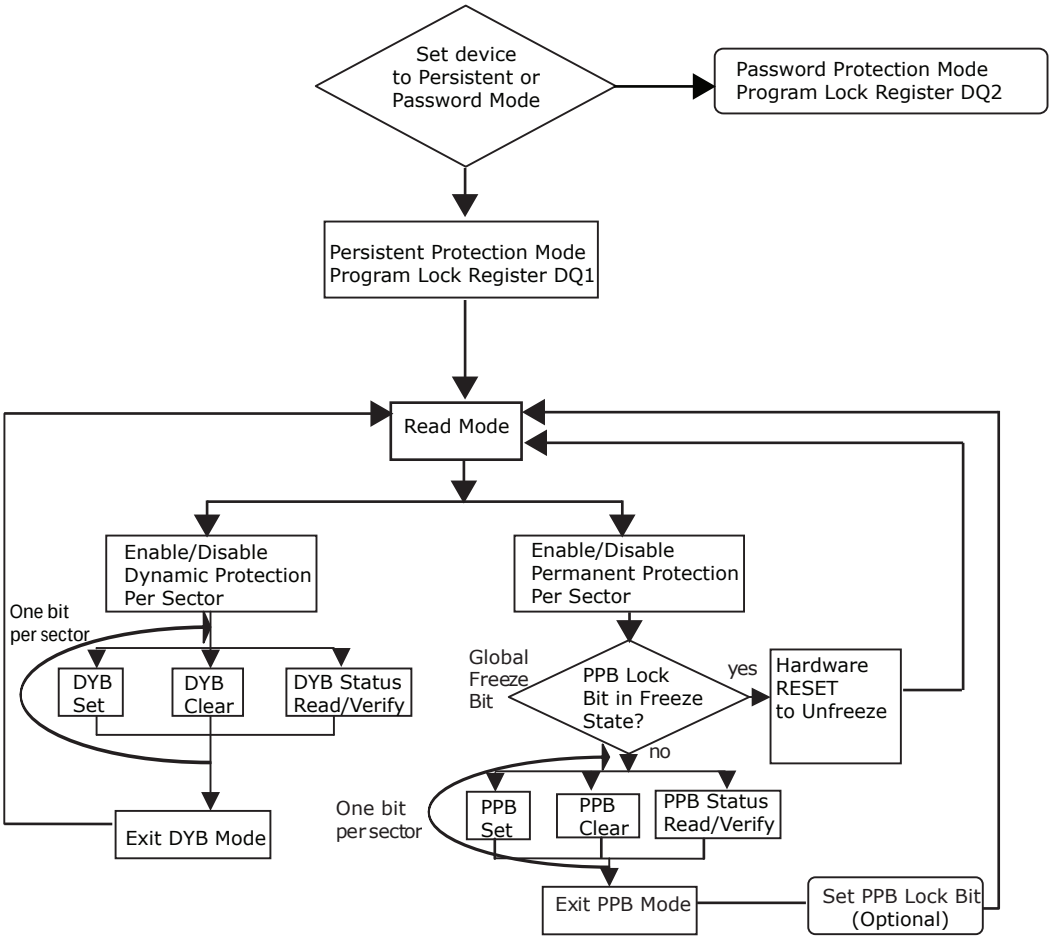


Figure 2. Read Password Protection Mode

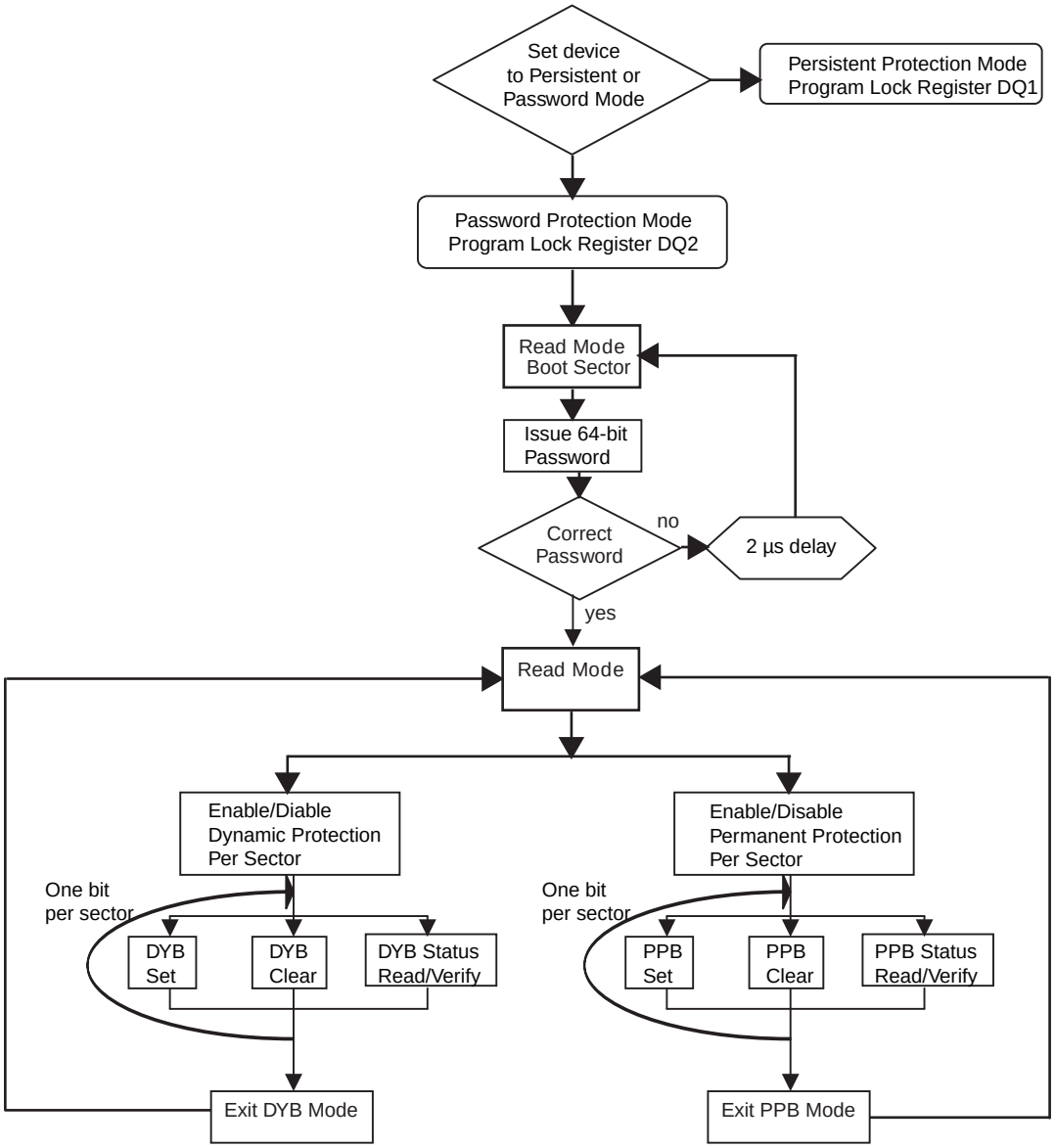
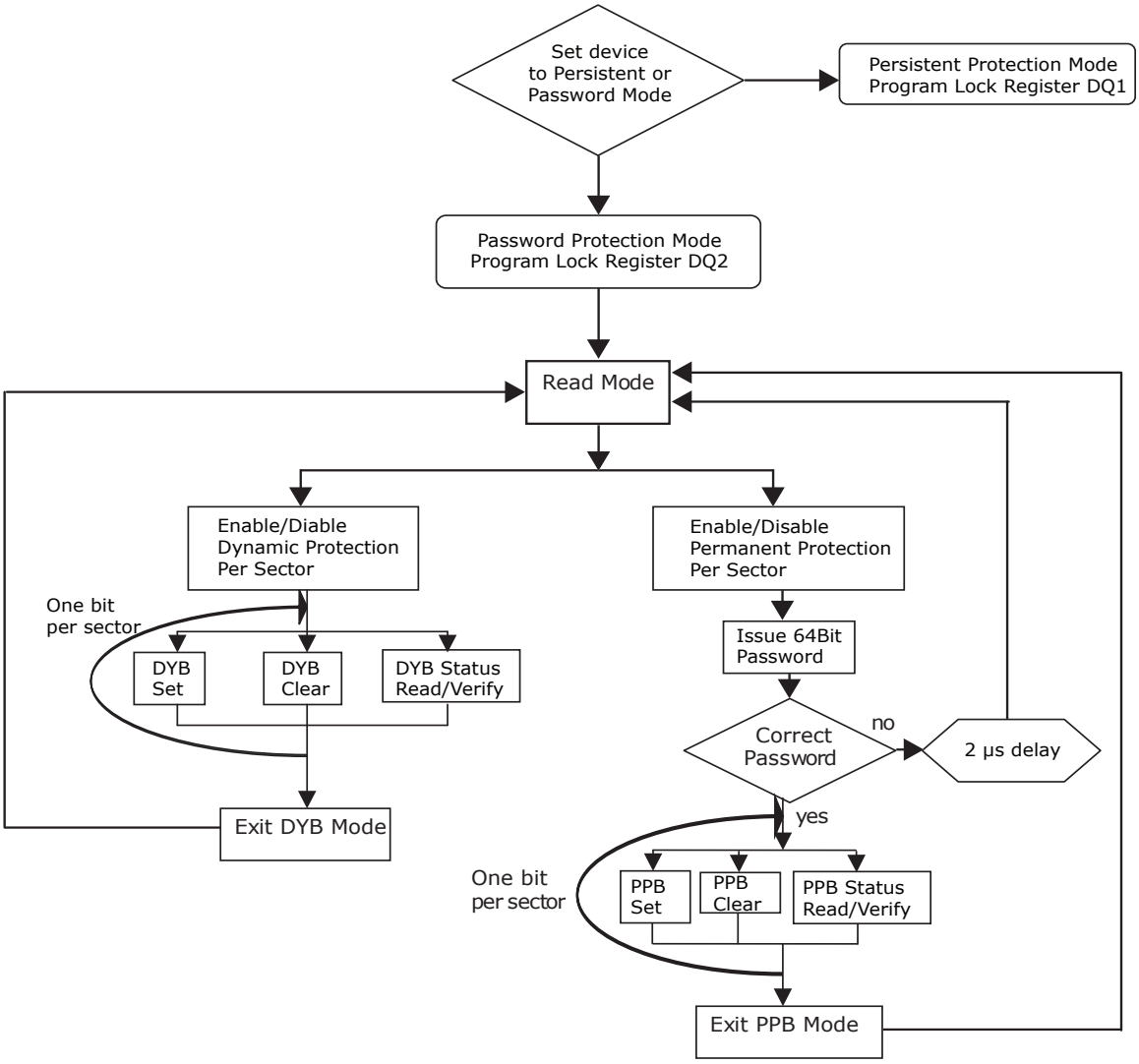


Figure 3. PPB Password Protection Mode



4. Distinguishing Permanent Sector Protection from Standard (Non-Permanent Sector Protection) Devices

4.1 Lock Register

The Lock Register holds the non-volatile OTP bits for controlling protection of the SSR and determining the PPB Lock bit management method (protection mode). The Lock Register consists of 16 bits. The DQ6, DQ2, and DQ1 bits of the Lock Register are programmable by the user. The programming time of the Lock Register is the same as the typical word programming time without utilizing the Write Buffer of the device. During a Lock Register programming sequence execution, the DQ6 Toggle Bit I toggles until the programming of the Lock Register has completed to indicate programming status. All Lock Register bits are readable to allow users to verify Lock Register statuses. Initial access time is required to read the Lock Register.

Table 2. Lock Register

Bit	Default Value	Name
15-9	1	Reserved
8	0	PPB Enable Bit
7	X	Reserved
6	1	SSR Region 1 (Customer) Lock Bit
5	0 or 1	Read Password Mode Enable Bit
4	0 or 1	DYB Boot Bit
3	0	Persistent Sector Protection PPB (Erase)
2	1	Password Protection Mode Lock Bit
1	1	Persistent Protection Mode Lock Bit
0	0	SSR Region 0 (Factory) Lock Bit

- DQ0 Secure Silicon Region (SSR) 0 (Factory) Lock Bit – is set at factory through Factory Set option to lock the SSR 0.
- DQ1 Persistent Protection Mode Lock Bit – allows the user to set the device permanently to operate in the Persistent Protection Mode.
- DQ2 Password Protection Mode Lock Bit – allows the user to set the device permanently to operate in the Password Protection Mode.
- DQ3 Persistent Sector Protection – is set at factory through Factory Set option to disable the “All PPB Erase” command, and allows for incremental lock down.
- DQ4 DYB Boot Bit – when set at factory through Factory Set option it will enable all DYB to be powered up in the “Unprotected State” or “Protected State” depending on the value.
- DQ5 Read Password Mode Enable Bit – is set at factory through Factory Set option to enable the protection of the array from read, program, and erase or just program and erase.
- DQ6 Secure Silicon Region (SSR) 1 (Customer) Lock Bit – allows the user to lock the SSR 1.
- DQ7 Reserved – is set at factory and can be either 0 or 1.
- DQ8 PPB Enable Bit – is set at the factory through Factory Set option to enable the use of the sector PPB protection bits.
- DQ15-DQ9 Reserved – are set at the factory and are 1's.

The Secure Silicon Region (SSR) protection bits must be used with caution, as once locked, there is no procedure available for unlocking the protected portion of the Secure Silicon Region and none of the bits in the protected Secure Silicon Region memory space can be modified in any way. Once the Secure Silicon Region area is protected, any further attempts to program in the area will fail with status indicating the area being programmed is protected. The Region 0 Indicator Bit is located in the Lock Register at bit location 0 and Region 1 in bit location 6.

As shipped from the factory, all devices default to the Persistent Protection method, with all sectors unprotected (or protected depending on the DYB power-up option) when power is applied. The device programmer or host system can then choose which sector protection method to use. Programming the one-time programmable, non-volatile bit, locks the part permanently in the Password Mode.

■ Password Protection Mode Lock Bit (DQ2) vs. Persistent Protection Mode Lock Bit (DQ1)

Once the Password Mode Lock Bit is programmed, the Persistent Mode Lock Bit is permanently disabled and no changes to the protection scheme are allowed.

If the password mode is chosen, the password must be programmed prior to setting the corresponding lock register bit. After the Password Protection Mode Lock Bit is programmed, a power cycle, hardware reset, or PPB Lock Bit Set command is required to set the PPB Lock bit to 0 to protect the PPB array.

The programming time of the Lock Register is the same as the typical word programming time. During a Lock Register programming EA, Data polling Status DQ6 Toggle Bit I will toggle until the programming has completed. The system can also determine the status of the lock register programming by reading the Status Register.

The user is not required to program DQ6 and DQ2 or DQ1bits at the same time. This allows the user to lock the SSR before or after choosing the device protection scheme. When programming the Lock Bits, all Factory Set Option bits (see below) MUST be programmed to 1 (even if the value of the bit is 0). A read-modify-program implementation will not work, because the Factor Set Option bits may read back as 0 and attempts to set Factor Set Options to 0 (even if they are already set to 0) will cause the entire Lock Register programming operation to fail without indication.

Lock Register - Factory Set Options

There are thirteen factory set options defined in the Lock register:

■ SSR 0 (Factory) Lock Bit (DQ0)

■ Persistent Sector Protection OTP Bit (DQ3)

■ DYB Boot Bit (DQ4)

■ Read Password Mode Enable Bit (DQ5)

■ Reserved (DQ7)

■ PPB Enable Bit (DQ8)

■ Reserved (DQ15 - DQ9)

Lock Register Command Set sequence is needed to program and read Lock Register Bits.

Table 3. Lock Register Bit Read-Out Sequence (Read Password)

		DQ15 – DQ9	DQ8	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
		(Factory Default)	PPB Enable Bit	(Factory Default)	SSR 1 (Customer Lock) Bit	Read Password Mode Enable Bit	DYB Boot Bit (1)	Persistent Sector Protection OTP Bit	Password Protection Mode Lock Bit	Persistent Protection Mode Lock Bit	SSR 0 (Factory Lock) Bit
New Device		1's	0	X	1	0	1	0	1	1	0
Permanent Sector Protection Device	Read Password Mode	1's	0	X	X	0	1	0	0	1	0

Note:

1. *DYB bits powers up in unprotected state. The DYB Boot Bit in the Lock Register can be factory programmed to 0, so all the DYB bits will be cleared to 0 (protected state) during POR or hardware reset. This is an order option.*

Table 4. Lock Register Bit Read-Out Sequence (PPB Password)

		DQ15 – DQ9	DQ8	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
		(Factory Default)	PPB Enable Bit	(Factory Default)	SSR 1 (Customer Lock) Bit	Read Password Mode Enable Bit	DYB Boot Bit (1)	Persistent Sector Protection OTP Bit	Password Protection Mode Lock Bit	Persistent Protection Mode Lock Bit	SSR 0 (Factory Lock) Bit
New Device		1's	0	X	1	1	1	0	1	1	0
Permanent Sector Protection Device	Persistent Mode	1's	0	X	X	1	1	0	1	0	0
	PPB Password Mode	1's	0	X	X	1	1	0	0	1	0

Note:

1. *DYB bits powers up in unprotected state. The DYB Boot Bit in the Lock Register can be factory programmed to 0, so all the DYB bits will be cleared to 0 (protected state) during POR or hardware reset. This is an order option.*

4.2 Password Protection Mode

4.2.1 Read Password Protection Mode

The Read Password Protection Mode enables protecting the main Flash array from read, program and erase. Only the lowest or highest Sector, selected for WP# protection, ID, CFI, and Status Register, remains readable until a successful Password Unlock command is completed. All other commands are ignored.

In this mode the PPB Lock bit is used to control the high order bits of address and disable embedded algorithm commands. When the PPB Lock bit is 1, the address and commands operate normally. When the PPB Lock is 0, the address bits that select a sector are forced either to 0's or to 1's to select the lowest or highest address sector. Also, all embedded algorithm commands that could change data are disabled to protect all sectors.

The PPB bits are protected from program and erase when PPB Lock is 0 and may be programmed or erased when PPB Lock is 1.

The PPB Lock bit is cleared to 0 when the user clears a PPB Lock bit to 0, generates a POR or hardware reset.

Read Password Protection Mode Notes:

- The command sequence for programming, reading, and locking of the Password is the same as the PPB Password Protection Mode.
- When the Password Protection Mode Lock Bit is enabled (i.e. DQ2 is set to 0), then all addresses are redirected to the WP# protected sector until the password unlocking sequence is properly entered, with the correct password. At which time, the Read Password Protection Mode is disabled and all addressing will direct to the proper location.
- Persistent Protection Mode Lock Bit (DQ1) can not be set to 0. Read Password Protection Mode does not support Persistent Protection Mode.
- If a system hardware reset or POR occurs, then the Read Password Protection Mode is re-enabled.
- If the part is unlocked from Read Password Protection Mode and the users does a PPB Lock bit clear to 0, the part will return to Read Password Protection Mode.
- If DQ5=0 then the device is ready for Read Password Protection Mode. However, Read Password Protection Mode is not enabled until DQ2=0. At which point, the addresses decode only to top/bottom sectors, until the device is unlocked with the proper unlocking sequence and Password. When DQ2=1 the addresses decode normally. This allows the user to program in their code, test it, provide a password, and then lock it by programming DQ2=0.
- Data Polling Status or Status Register can be read when the device is in Read Password Protection Mode. If the user issues a status register read during Program or Erase, when the PPB Lock is 0, the status will reflect a fail with the reason being because the sector is locked (the chip is in read password mode with PPB Lock =0). Similarly, Data Polling would show DQ5=1 to indicate the failed program or erase, just as it would normally.
- Programming in the Lock Register ASO is not allowed when Password Protection Mode Lock Bit and PPB Lock bit are 0.
- The ID/CFI ASO Entry is supported when in Read Password Protection Mode.
- The ID/CFI ASO will show all sectors locked when reading location 2h.

4.2.2 PPB Password Protection Mode

The PPB Password Protection Mode enables protecting the main Flash array from program and erase.

In this mode the PPB Lock bit is used to control the high order bits of address and disable embedded algorithm commands. When the PPB Lock bit is 1, the address and commands operate normally. When the PPB Lock is 0, all embedded algorithm commands that could change data are disabled to protect sectors which have their PPB bit set.

The PPB bits are protected from program and erase when PPB Lock is 0 and may be programmed or erased when PPB Lock is 1.

The PPB Lock bit is set to 1 when the PPB Password Protection Mode is unlocked. The PPB Lock is cleared to 0 when the users clears a PPB Lock bit to 0, generates a POR or hardware reset.

PPB Password Protection Notes:

- The command sequence for programming, reading, and locking of the Password is described in the S29GL-S data sheet (S29GL_128S_01GS_00).
- When the Password Protection Mode Lock Bit is enabled (i.e. DQ2 is set to 0), then sectors which have their PPB bit set can't be programmed or erased until the password unlocking sequence is properly entered and then the associated PPB bit cleared.
- If a system hardware reset or POR occurs, then the PPB Password Protection Mode is re-enabled.
- If the part is unlocked from PPB Password Protection Mode and the users does a PPB Lock bit clear to 0, the part will return to PPB Password Protection Mode.
- If DQ5=1 then the device is ready for PPB Password Protection Mode. However, PPB Password Protection Mode is not enabled until DQ2=0. At which point, sectors which have their PPB bit set can't be programmed or erased, until the device is unlocked with the proper unlocking sequence and Password. When DQ2=1 the addresses decode normally. This allows the user to program in their code, test it, provide a password, and then lock it by programming DQ2=0.
- Data Polling Status or Status Register can be read when the device is in PPB Password Protection Mode. If the user issues a status register read during Program or Erase, when the PPB Lock is 0, the status will reflect a fail with the reason being because the sector is locked (the chip is in PPB password mode with PPB Lock =0). Similarly, Data Polling would show DQ5=1 to indicate the failed program or erase, just as it would normally.

4.2.3 Dynamic Protection Bits (DYB)

The DYB Boot Bit in the Lock Register can be factory programmed to 0, so all the DYB will be cleared to 0 (protected state) during POR or hardware reset. If the DYB Boot Bit is 1, the DYB will be set to 1 (unprotect state) during POR or hardware reset. This is an order option.

5. Ordering Information

Valid Combinations:

The Recommended Combinations table lists configurations planned to be available in volume. The table below will be updated as new combinations are released. Consult your local sales representative to confirm availability of specific combinations and to check on newly released combinations.

S29GL-S Valid Combinations					
Base OPN	**Speed (ns)**	**Package and Temperature**	**Model Number**	**Packing Type**	**Ordering Part Number (yy = Model Number, x = Packing Type)**
S29GL01GS	100	DHS, FHS (Note 1)	S1, S2, S3, S4, S5, S6, S7, S8	0, 3 (Note 2)	S29GL01GS10DHSyyx S29GL01GS10FHSyyx
S29GL512S	100				S29GL512S10DHSyyx S29GL512S10FHSyyx
S29GL256S	90				S29GL256S90DHSyyx S29GL256S90FHSyyx
S29GL128S	90				S29GL128S90DHSyyx S29GL128S90FHSyyx

Notes:

1. *Additional speed, package, and temperature options maybe offered in the future. Check with your local sales representative for availability.*
2. *Package Type 0 is standard option.*

The ordering part number for the General Market device is formed by a valid combination of the following:

S29GL01GS **10** **D** **H** **S** **S1** **0**

Packing Type
0 = Tray
3 = 13” Tape and Reel

Model Number (V_{IO} and V_{CC} Range)
S1 = V_{IO} = V_{CC} = 2.7 to 3.6V, highest address sector protected, DYB's power up in unprotected state, Read Password Mode
S2 = V_{IO} = V_{CC} = 2.7 to 3.6V, lowest address sector protected, DYB's power up in unprotected state, Read Password Mode
S3 = V_{IO} = V_{CC} = 2.7 to 3.6V, highest address sector protected, DYB's power up in protected state, Read Password Mode
S4 = V_{IO} = V_{CC} = 2.7 to 3.6V, lowest address sector protected, DYB's power up in protected state, Read Password Mode
S5 = V_{IO} = V_{CC} = 2.7 to 3.6V, highest address sector protected, DYB's power up in unprotected state, PPB Password Mode
S6 = V_{IO} = V_{CC} = 2.7 to 3.6V, lowest address sector protected, DYB's power up in unprotected state, PPB Password Mode
S7 = V_{IO} = V_{CC} = 2.7 to 3.6V, highest address sector protected, DYB's power up in protected state, PPB Password Mode
S8 = V_{IO} = V_{CC} = 2.7 to 3.6V, lowest address sector protected, DYB's power up in protected state, PPB Password Mode

Temperature Range
S = Extended Commercial (0°C to +85°C)

Package Materials Set
H = Low Halogen, Pb-Free

Package Type
D = Fortified Ball-Grid Array Package (LAE064) 9 mm x 9 mm
F = Fortified Ball-Grid Array Package (LAA064) 13 mm x 11 mm

Speed Option
90 = 90 ns random access time
10 = 100 ns random access time
11 = 110 ns random access time

Device Number/Description
S29GL01GS, S29GL512S, S29GL256S, S29GL128S
3.0 Volt Core, with V_{IO} Option, 1024, 512, 256, 128 Megabit Page-Mode Flash Memory, Manufactured on 65 nm MirrorBit Eclipse Process Technology

6. Revision History

Spansion Publication Number: S29GL_128S_01GS_SP

Section	Description
Revision 01 (March 4, 2011)	
	Initial release
Revision 02 (March 30, 2011)	
Advance Sector Protection Clarification	All PPB Clear was removed from Protection Mode figures
Lock Register	Lock Register 8 default value was corrected to be 0 and text corrected to state that this bit is set at factory through factory Set option Lock Register Bit Read-out Sequence table was updated
Revision 03 (July 8, 2011)	
Lock Register	Clarification when programming the Lock Register
Ordering Information	Addition of LAA064 13 mm x 11 mm package
Revision 04 (September 26, 2011)	
Lock Register	Persistent Protection Mode Lock Bit (DQ1) not a customer programmable bit
Order Information	Updated
Revision 05 (October 21, 2011)	
Lock Register	Clarification of bits and differences between Read Password and PPB Password
Read Password	Clarification
PPB Password	Section added
Ordering Information	Updated
Revision 06 (December 14, 2011)	
Advance Sector Protection Clarification	Added link to Figure 3.2 - Read Password Protection Mode
Lock Register	Clarification of Programming Factory Set Options
Ordering Information	Added additional OPN's Clarification to S8 option
Revision 07 (March 21, 2012)	
Lock Register	Clarified the programming of the Lock Register
Ordering Information	Updated Valid Combinations

Document History Page

Document Title: S29GL-S (S Models) 3V Flash with Page Mode featuring 65 nm MirrorBit® Process Technology Permanent Sector Lock Security Device Documentation Document Number: 002-00783				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	-	RYSU	08/19/2015	-
*A	-	RYSU	08/19/2015	-
*B	-	RYSU	08/19/2015	-
*C	-	RYSU	08/19/2015	-
*D	-	RYSU	08/19/2015	-
*E	-	RYSU	08/19/2015	-
*F	-	SZZX	03/21/2012	-
*G	5730088	SZZX	05/08/2017	Updated to Cypress format and Datasheet reactivated.

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