Please note that Cypress is an Infineon Technologies Company.
The document following this cover page is marked as “Cypress” document as this is the company that originally developed the product. Please note that Infineon will continue to offer the product to new and existing customers as part of the Infineon product portfolio.

Continuity of document content
The fact that Infineon offers the following product as part of the Infineon product portfolio does not lead to any changes to this document. Future revisions will occur when appropriate, and any changes will be set out on the document history page.

Continuity of ordering part numbers
Infineon continues to support existing part numbers. Please continue to use the ordering part numbers listed in the datasheet for ordering.

S29AL032D

32 Mbit, 3 V, Flash 4 M x 8-Bit Uniform Sector 4 M x 8-Bit/2 M x 16-Bit Boot Sector

This product has been retired and is not recommended for designs. For new and current designs, the S29GL064S supersedes the S29AL032D. This is the factory-recommended migration path. Please refer to the S29GL064S data sheet for specifications and ordering information. Availability of this document is retained for reference and historical purposes only.

Distinctive Characteristics

Architectural Advantages

- Single power supply operation
  - Full voltage range: 2.7 to 3.6 volt read and write operations for battery-powered applications
- Manufactured on 200-nm process technology
  - Fully compatible with 0.23 µm Am29LV320D, 0.32 µm Am29LV033C, and 0.33 µm MBM29LV320E devices
- Flexible sector architecture
  - Boot sector models: Eight 8-Kbyte sectors; sixty-three 64-Kbyte sectors; top or bottom boot block configurations available
  - Uniform sector models: Sixty-four 64-Kbyte sectors
- Sector Protection features
  - A hardware method of locking a sector to prevent any program or erase operations within that sector
  - Sectors can be locked in-system or via programming equipment
  - Temporary Sector Unprotect feature allows code changes in previously locked sectors
- Unlock Bypass Program Command
  - Reduces overall programming time when issuing multiple program command sequences
- Secured Silicon Sector
  - 128-word sector for permanent, secure identification through an 8-word random Electronic Serial Number
  - May be programmed and locked at the factory or by the customer
  - Accessible through a command sequence
- Compatibility with JEDEC standards
  - Pinout and software compatible with single-power supply Flash
  - Superior inadvertent write protection

Package Options

- 48-ball FBGA
- 48-pin TSOP
- 40-pin TSOP

Performance Characteristics

- High performance
  - Access times as fast as 70 ns
- Ultra low power consumption (typical values at 5 MHz)
  - 200 nA Automatic Sleep mode current
  - 200 nA standby mode current
  - 9 mA read current
  - 20 mA program/erase current
- Cycling endurance: 1,000,000 cycles per sector typical
- Data retention: 20 years typical

Software Features

- CFI (Common Flash Interface) compliant
  - Provides device-specific information to the system, allowing host software to easily reconfigure for different Flash devices
- Erase Suspend/Erase Resume
  - Suspends an erase operation to read data from, or program data to, a sector that is not being erased, then resumes the erase operation
- Data# Polling and toggle bits
  - Provides a software method of detecting program or erase operation completion
  - Unlock Bypass Program Command
    Reduces overall programming time when issuing multiple program command sequences

Hardware Features

- Ready/Busy# pin (RY/BY#)
  - Provides a hardware method of detecting program or erase cycle completion
- Hardware reset pin (RESET#)
  - Hardware method to reset the device to reading array data
- WP#/ACC input pin
  - Write protect (WP#) function allows protection of two outermost boot sectors (boot sector models only), regardless of sector protect status
  - Acceleration (ACC) function provides accelerated program times

Not Recommended for New Design

General Description

The S29AL032D is a 32-megabit, 3.0 volt-only flash memory device, organized as 2,097,152 words of 16 bits each or 4,194,304 bytes of 8 bits each. Word mode data appears on DQ0-DQ15; byte mode data appears on DQ0-DQ7. The device is designed to be programmed in-system with the standard 3.0 volt VCC supply, and can also be programmed in standard EPROM programmers.

The device is available with access times as fast as 70 ns. The devices are offered in 40-pin TSOP, 48-pin TSOP and 48-ball FBGA packages. Standard control pins- chip enable (CE#), write enable (WE#), and output enable (OE#)-control normal read and write operations, and avoid bus contention issues.

The device requires only a **single 3.0 volt power supply** for both read and write functions. Internally generated and regulated voltages are provided for the pro-gram and erase operations.

S29AL032D Features

The **Secured Silicon Sector** is an extra sector capable of being permanently locked by Spansion or customers. The **Secured Silicon Indicator Bit** (DQ7) is permanently set to a 1 if the part is **factory locked**, and set to a 0 if customer lockable. This way, customer lockable parts can never be used to replace a factory locked part. **Note that the S29AL032D has a Secured Silicon Sector size of 128 words (256 bytes)**.

Factory locked parts provide several options. The Secured Silicon Sector may store a secure, random 16 byte ESN (Electronic Serial Number), customer code (programmed through the Spansion programming service), or both.

The S29AL032D is entirely command set compatible with the **JEDEC single-power-supply Flash standard**. Commands are written to the command register using standard microprocessor write timings. Register contents serve as input to an internal state-machine that controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from other Flash or EPROM devices.

Device programming occurs by executing the program command sequence. This initiates the **Embedded Program** algorithm—an internal algorithm that automatically times the program pulse widths and verifies proper cell margin. The **Unlock Bypass** mode facilitates faster programming times by requiring only two write cycles to program data instead of four.

Device erasure occurs by executing the erase command sequence. This initiates the **Embedded Erase** algorithm—an internal algorithm that automatically preprograms the array (if it is not already programmed) before executing the erase operation. During erase, the device automatically times the erase pulse widths and verifies proper cell margin.

The host system can detect whether a program or erase operation is complete by observing the RY/BY# pin, or by reading the DQ7 (Data# Polling) and DQ6 (toggle) **status bits**. After a program or erase cycle has been completed, the device is ready to read array data or accept another command.

The **sector erase architecture** allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. The device is fully erased when shipped from the factory.

Hardware data protection measures include a low V_{CC} detector that automatically inhibits write operations during power transitions. The **hardware sector protection** feature disables both program and erase operations in any combination of the sectors of memory. This can be achieved in-system or via programming equipment.

The **Erase Suspend/Erase Resume** feature enables the user to put erase on hold for any period of time to read data from, or program data to, any sector that is not selected for erasure. True background erase can thus be achieved.

The **hardware RESET# pin** terminates any operation in progress and resets the internal state machine to reading array data. The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the device, enabling the system microprocessor to read the boot-up firmware from the Flash memory.

The device offers two power-saving features. When addresses are stable for a specified amount of time, the device enters the **automatic sleep mode**. The system can also place the device into the **standby mode**. Power consumption is greatly reduced in both these modes.

The Spansion Flash technology combines years of Flash memory manufacturing experience to produce the highest levels of quality, reliability and cost effectiveness. The device electrically erases all bits within a sector simultaneously via Fowler-Nordheim tunneling. The data is programmed using hot-electron injection.

Not Recommended for New Design

Contents

1. Product Selector Guide 4

2. Block Diagram 4

3. Connection Diagrams 5
3.1 FBGA Package for Model 00 Only 6
3.2 FBGA Package for Models 03, 04 Only 7
3.3 Special Handling Instructions 7

4. Pin Configuration 7

5. Logic Symbols 8

6. Ordering Information 9
6.1 S29AL032D Standard Products 9
6.2 Valid Combinations 10

7. Device Bus Operations 10
7.1 Word/Byte Configuration (Models 03, 04 Only) 10
7.2 Requirements for Reading Array Data 11
7.3 Writing Commands/Command Sequences 11
7.4 Program and Erase Operation Status 11
7.5 Accelerated Program Operation 11
7.6 Standby Mode 11
7.7 Automatic Sleep Mode 12
7.8 RESET#: Hardware Reset Pin 12
7.9 Output Disable Mode 13
7.10 Sector Addresss Tables 13
7.11 Autoselect Mode 19
7.12 Sector Protection/Unprotection 20
7.13 Write Protect (WP#) — Models 03, 04 Only 24
7.14 Temporary Sector Unprotect 24

8. Secured Silicon Sector Flash Memory Region 24
8.1 Factory Locked: Secured Silicon Sector Programmed and Protected at the Factory 25
8.2 Customer Lockable: Secured Silicon Sector NOT Programmed or Protected at the Factory 25

9. Hardware Data Protection 26
9.1 Low V_{CC} Write Inhibit 26
9.2 Write Pulse “Glitch” Protection 26
9.3 Logical Inhibit 26
9.4 Power-Up Write Inhibit 26

10. Common Flash Memory Interface (CFI) 27

11. Command Definitions 29
11.1 Reading Array Data 29
11.2 Reset Command 29
11.3 Autoselect Command Sequence 30
11.4 Enter Secured Silicon Sector/Exit Secured Silicon Sector Command Sequence 30
11.5 Word/Byte Program Command Sequence 30
11.6 Unlock Bypass Command Sequence 30
11.7 Chip Erase Command Sequence 31
11.8 Sector Erase Command Sequence 32
11.9 Erase Suspend/Erase Resume Commands 32
11.10 Command Definitions Table 34

12. Write Operation Status 37
12.1 DQ7: Data# Polling 37
12.2 RY/BY#: Ready/Busy# 38
12.3 DQ6: Toggle Bit I 39
12.4 DQ2: Toggle Bit II 39
12.5 Reading Toggle Bits DQ6/DQ2 39
12.6 DQ5: Exceeded Timing Limits 40
12.7 DQ3: Sector Erase Timer 41

13. Absolute Maximum Ratings 42

14. Operating Ranges 43

15. DC Characteristics 44
15.1 Zero Power Flash 45

16. Test Conditions 46
16.1 Key to Switching Waveforms 46

17. AC Characteristics 47
17.1 Read Operations 47
17.2 Hardware Reset (RESET#) 48
17.3 Word/Byte Configuration (BYTE#) (Models 03, 04 Only) 49
17.4 Erase/Program Operations 50
17.5 Temporary Sector Unprotect 53
17.6 Alternate CE# Controlled Erase/Program Operations 55

18. Erase and Programming Performance 57

19. TSOP and BGA Pin Capacitance 57
19.1 TS040—40-Pin Standard TSOP 58
19.2 TS 048—48-Pin Standard TSOP 60
19.3 VBN048—48-Ball Fine-Pitch Ball Grid Array (FBGA) 10.0 x 6.0 mm 61

20. Document History Page 62

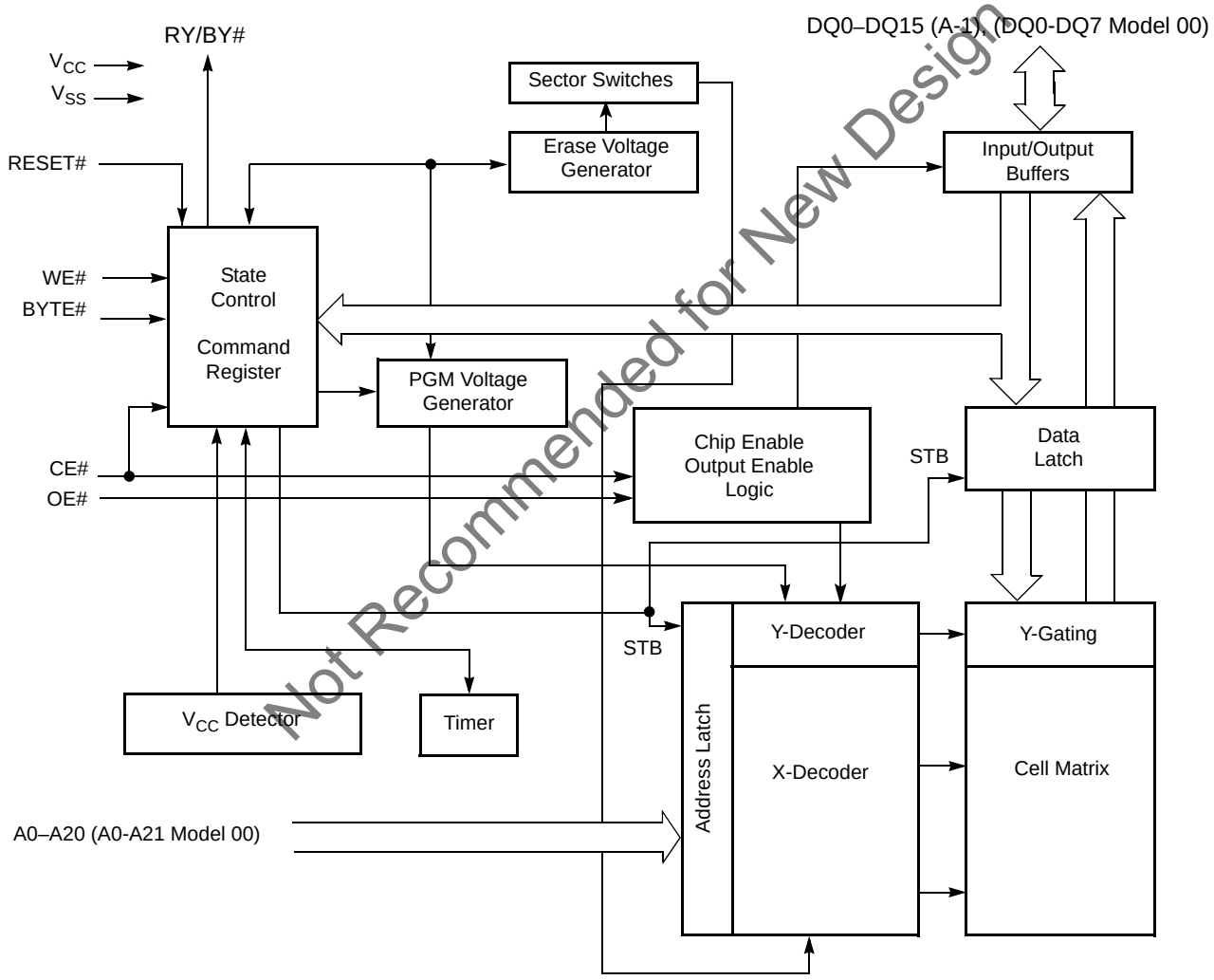
Not Recommended for New Design

1. Product Selector Guide

Family Part Number		S29AL032D	
Speed Option	**Voltage Range: V_{CC} = 2.7–3.6 V**	**70**	**90**
Max access time, ns (t_{ACC})		70	90
Max CE# access time, ns (t_{CE})		70	90
Max OE# access time, ns (t_{OE})		30	35

Note
See AC Characteristics on page 47 for full specifications.

2. Block Diagram

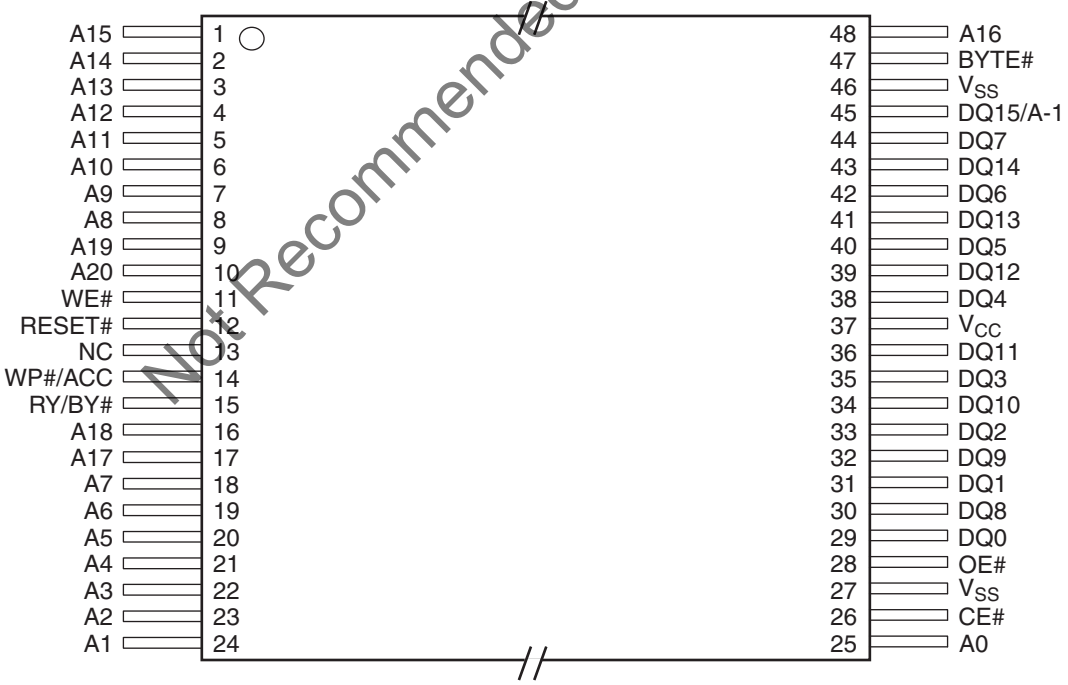


3. Connection Diagrams

Figure 3.1 40-pin Standard TSOP



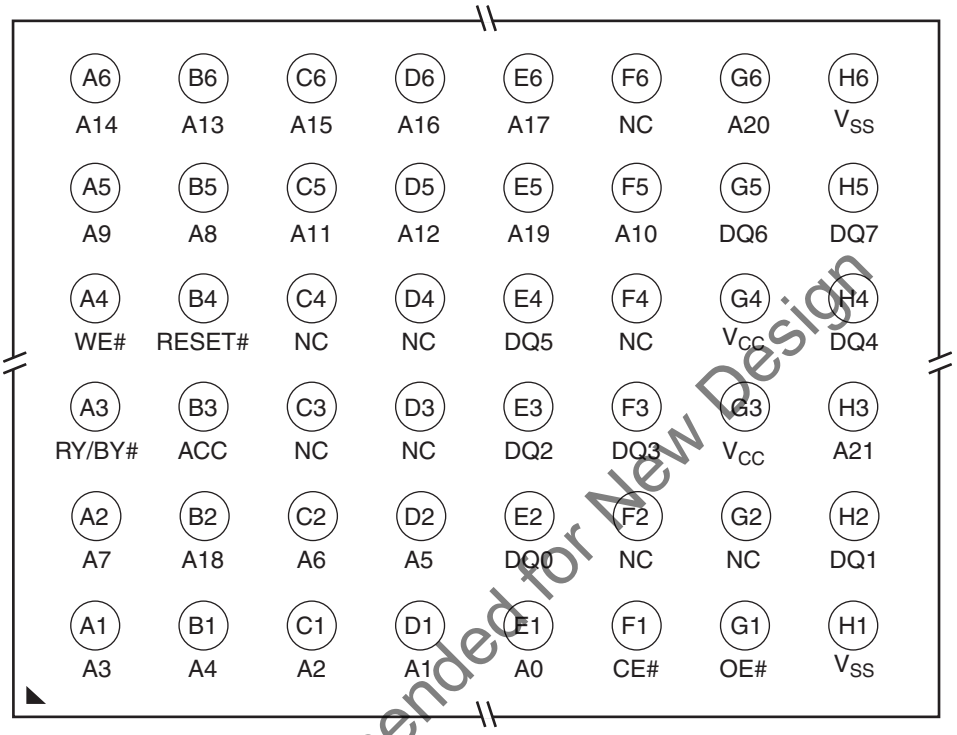
Figure 3.2 48-pin Standard TSOP



Not Recommended for New Design

3.1 FBGA Package for Model 00 Only

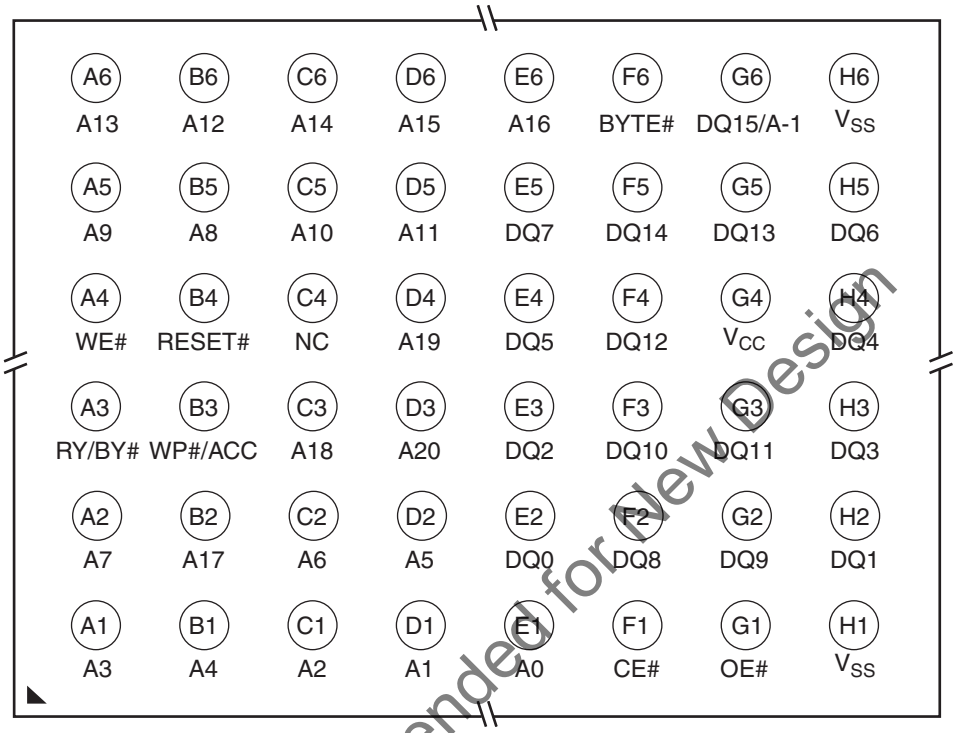
Figure 3.3 Model 00 48-ball FBGA (Top View, Balls Facing Down)



Not Recommended for New Design

3.2 FBGA Package for Models 03, 04 Only

Figure 3.4 Models 03, 04 48-ball FBGA (Top View, Balls Facing Down)



Not Recommended for New Design

3.3 Special Handling Instructions

Special handling is required for Flash Memory products in FBGA packages.

Flash memory devices in FBGA packages may be damaged if exposed to ultrasonic cleaning methods. The package and/or data integrity may be compromised if the package body is exposed to temperatures above 150°C for prolonged periods of time.

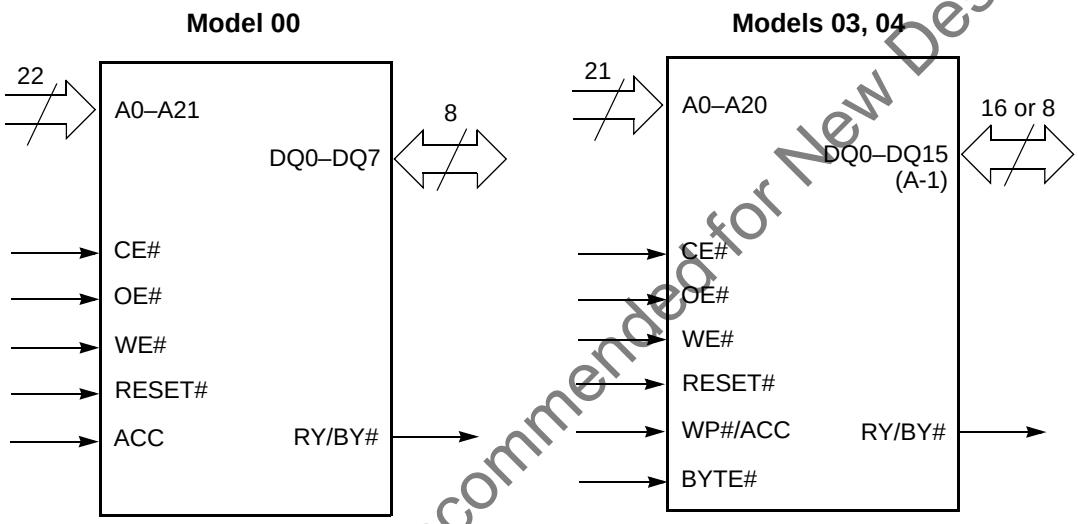
4. Pin Configuration

Pin	Description
A0–A21	22 address inputs
A0-A20	21 address inputs
DQ0–DQ7	8 data inputs/outputs
DQ0-DQ14	15 data inputs/outputs
DQ15/A-1	DQ15 (data input/output, word mode), A-1 (LSB address input, byte mode)
BYTE#	Selects 8-bit or 16-bit mode
CE#	Chip enable
OE#	Output enable
WE#	Write enable
RESET#	Hardware reset pin
WP#/ACC	Hardware Write Protect input/Programming Acceleration input.

Pin	Description
ACC	Hardware Write Protect input
RY/BY#	Ready/Busy output
V_{CC}	3.0 volt-only single power supply (see Product Selector Guide on page 4 for speed options and voltage supply tolerances)
V_{SS}	Device ground
NC	Pin not connected internally

5. Logic Symbols

Figure 5.1 Logic Symbols



Not Recommended for New Design

6. Ordering Information

6.1 S29AL032D Standard Products

Spansion standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.

S29AL032D 70 T A I 00 0

PACKING TYPE

0 = Tray
2 = 7” Tape and Reel
3 = 13” Tape and Reel

MODEL NUMBER

00 = x8, V_{CC} = 2.7 V to 3.6 V, Uniform sector device
03 = x8/x16, V_{CC} = 2.7 V to 3.6 V, Top boot sector device, top two address sectors protected when WP#/ACC = V_{IL}
04 = x8/x16, V_{CC} = 2.7 V to 3.6 V, Bottom boot sector device, bottom two address sectors protected when WP#/ACC = V_{IL}

TEMPERATURE RANGE

I = Industrial (–40°C to +85°C)
N = Extended (-40°C to +125°C)

PACKAGE MATERIAL SET

A = Standard
F = Pb-Free

PACKAGE TYPE

T = Thin Small Outline Package (TSOP) Standard Pinout
B = Fine-pitch Ball-Grid Array Package

SPEED OPTION

See Product Selector Guide and Valid Combinations

DEVICE NUMBER/DESCRIPTION

S29AL032D
3.0 Volt-only, 32 Megabit Standard Flash Memory, manufactured using 200 nm process technology

Not Recommended for New Design

S29AL032D Valid Combinations					Package Description	
Device Number	**Speed Option**	**Package Type, Material, and Temperature Range**	**Model Number**	**Packing Type**		
S29AL032D	70	TAI, TFI	00	0, 3 (Note 1)	TS040 (Note 2)	TSOP
			03, 04		TS048 (Note 2)	
		BAI, BFI	00, 03, 04	0, 2, 3 (Note 1)	VBN048 (Note 3)	Fine-Pitch BGA
	90	TAI, TFI, TAN, TFN	00	0, 3 (Note 1)	TS040 (Note 2)	TSOP
			03, 04		TS048 (Note 2)	
		BAI, BFI, BAN, BFN	00, 03, 04	0, 2, 3 (Note 1)	VBN048 (Note 3)	Fine-Pitch BGA

Notes

1. *Type 0 is standard. Specify other options as required.*
2. *TSOP package marking omits packing type designator from ordering part number.*
3. *BGA package marking omits leading S29 and packing type designator from ordering part number.*

Not Recommended for New Design

6.2 Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

7. Device Bus Operations

This section describes the requirements and use of the device bus operations, which are initiated through the internal command register. The command register itself does not occupy any addressable memory location. The register is composed of latches that store the commands, along with the address and data information needed to execute the command. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device. Table 8 lists the device bus operations, the inputs and control levels they require, and the resulting output. The following subsections describe each of these operations in further detail.

Table 8. S29AL032D Device Bus Operations

Operation	CE#	OE#	WE#	RESET#	WP#(Note 6)/ACC	Addresses (Note 3)	DQ0–DQ7	DQ8–DQ15 (Note 6)	
								BYTE# = V_{IH}	BYTE# = V_{IL}
Read	L	L	H	H	L/H	A_{IN}	D_{OUT}	D_{OUT}	DQ8–DQ14 = High-Z, DQ15 = A-1
Write (Note 1)	L	H	L	H	(Note 4)	A_{IN}	(Note 5)	(Note 5)	
Accelerated Program (Note 6)	L	H	L	H	V_{HH}	A_{IN}	(Note 5)	(Note 5)	
Standby	$V_{CC} \pm 0.3$ V	X	X	$V_{CC} \pm 0.3$ V	H	X	High-Z	High-Z	High-Z
Output Disable	L	H	H	H	L/H	X	High-Z	High-Z	High-Z
Reset	X	X	X	L	L/H	X	High-Z	High-Z	High-Z
Sector Protect (Note 3)	L	H	L	V_{ID}	L/H	SA, A6 = L, A1 = H, A0 = L	(Note 5)	X	X
Sector Unprotect (Note 3)	L	H	L	V_{ID}	(Note 4)	SA, A6 = H, A1 = H, A0 = L	(Note 5)	X	X
Temporary Sector Unprotect	X	X	X	V_{ID}	(Note 4)	A_{IN}	(Note 5)	(Note 5)	High-Z

Legend

L = Logic Low = V_{IL}, H = Logic High = V_{IH}, V_{ID} = 12.0 ± 0.5 V, X = Don't Care, A_{IN} = Address In, D_{IN} = Data In, D_{OUT} = Data Out

Notes

1. *When the ACC pin is at V_{HH}, the device enters the accelerated program mode. See*
2. *Addresses are A20:A0 in word mode (BYTE# = V_{IH}), A20:A-1 in byte mode (BYTE# = V_{IL}).*
3. *The sector protect and sector unprotect functions may also be implemented via programming equipment.*
4. *If WP#/ACC = V_{IL}, the two outermost boot sectors remain protected. If WP#/ACC = V_{IH}, the two outermost boot sector protection depends on whether they were last protected or unprotected. If WP#/ACC = V_{HH}, all sectors are unprotected.*
5. *D_{IN} or D_{OUT} as required by command sequence, data polling, or sector protection algorithm.*
6. *Models 03, 04 only*

7.1 Word/Byte Configuration (Models 03, 04 Only)

The BYTE# pin controls whether the device data I/O pins DQ15–DQ0 operate in the byte or word configuration. If the BYTE# pin is set at logic *1*, the device is in word configuration, DQ15–DQ0 are active and controlled by CE# and OE#.

If the BYTE# pin is set at logic *0*, the device is in byte configuration, and only data I/O pins DQ0–DQ7 are active and controlled by CE# and OE#. The data I/O pins DQ8–DQ14 are tri-stated, and the DQ15 pin is used as an input for the LSB (A-1) address function.

7.2 Requirements for Reading Array Data

To read array data from the outputs, the system must drive the CE# and OE# pins to V_{IL}. CE# is the power control and selects the device. OE# is the output control and gates array data to the output pins. WE# should remain at V_{IH}. The BYTE# pin determines whether the device outputs array data in words or bytes.

The internal state machine is set for reading array data upon device power-up, or after a hardware reset. This ensures that no spurious alteration of the memory content occurs during the power transition. No command is necessary in this mode to obtain array data. Standard microprocessor read cycles that assert valid addresses on the device-address inputs produce valid data on the device-data outputs. The device remains enabled for read access until the command register contents are altered.

See Reading Array Data on page 29 for more information. Refer to the AC Read Operations on page 47 table for timing specifications and to Figure 17.1 on page 47 for the timing diagram. I_{CC1} in the DC Characteristics table represents the active current specification for reading array data.

Not Recommended for New Design

7.3 Writing Commands/Command Sequences

To write a command or command sequence (which includes programming data to the device and erasing sectors of memory), the system must drive WE# and CE# to V_{IL}, and OE# to V_{IH}.

For program operations, the BYTE# pin determines whether the device accepts program data in bytes or words. Refer to Word/Byte Configuration (Models 03, 04 Only) on page 11 for more information.

The device features an **Unlock Bypass** mode to facilitate faster programming. Once the device enters the Unlock Bypass mode, only two write cycles are required to program a word or byte, instead of four. Word/Byte Program Command Sequence on page 30 has details on programming data to the device using both standard and Unlock Bypass command sequences.

An erase operation can erase one sector, multiple sectors, or the entire device. Table 8 on page 13 and Table 10 on page 15 indicate the address space that each sector occupies. A *sector address* consists of the address bits required to uniquely select a sector. The Command Definitions on page 29 contains details on erasing a sector or the entire chip, or suspending/resuming the erase operation.

After the system writes the autoselect command sequence, the device enters the autoselect mode. The system can then read autoselect codes from the internal register (which is separate from the memory array) on DQ7–DQ0. Standard read cycle timings apply in this mode. Refer to Autoselect Mode on page 19 and Autoselect Command Sequence on page 30 for more information.

I_{CC2} in the DC Characteristics table represents the active current specification for the write mode. AC Characteristics on page 47 contains timing specification tables and timing diagrams for write operations.

7.4 Program and Erase Operation Status

During an erase or program operation, the system may check the status of the operation by reading the status bits on DQ7–DQ0. Standard read cycle timings and I_{CC} read specifications apply. Refer to Write Operation Status on page 37 for more information, and to AC Characteristics on page 47 for timing diagrams.

7.5 Accelerated Program Operation

The device offers accelerated program operations through the ACC function. This is one of two functions provided by the WP#/ACC (ACC on Model 00) pin. This function is primarily intended to allow faster manufacturing throughput at the factory.

If the system asserts V_{HH} on this pin, the device automatically enters the previously mentioned Unlock Bypass mode, temporarily unprotects any protected sectors, and uses the higher voltage on the pin to reduce the time required for program operations. The system would use a two-cycle program command sequence as required by the Unlock Bypass mode. Removing V_{HH} from the WP#/ACC pin returns the device to normal operation. Note that the WP#/ACC pin must not be at V_{HH} for operations other than accelerated programming, or device damage may result. In addition, the WP#/ACC pin must not be left floating or unconnected; inconsistent behavior of the device may result.

7.6 Standby Mode

When the system is not reading or writing to the device, it can place the device in the standby mode. In this mode, current consumption is greatly reduced, and the outputs are placed in the high impedance state, independent of the OE# input.

The device enters the CMOS standby mode when the CE# and RESET# pins are both held at $V_{CC} \pm 0.3$ V. (Note that this is a more restricted voltage range than V_{IH}.) If CE# and RESET# are held at V_{IH}, but not within $V_{CC} \pm 0.3$ V, the device will be in the standby mode, but the standby current will be greater. The device requires standard access time (t_{CE}) for read access when the device is in either of these standby modes, before it is ready to read data.

If the device is deselected during erasure or programming, the device draws active current until the operation is completed.

In the DC Characteristics table, I_{CC3} and I_{CC4} represents the standby current specification.

7.7 Automatic Sleep Mode

The automatic sleep mode minimizes Flash device energy consumption. The device automatically enables this mode when addresses remain stable for t_{ASM}. The automatic sleep mode is independent of the CE#, WE#, and OE# control signals. Standard address access timings provide new data when addresses are changed. While in sleep mode, output data is latched and always available to the system. I_{CC4} in DC Characteristics on page 44 represents the automatic sleep mode current specification.

Table 8. Automatic Sleep Mode Timing

Parameter	Description	Max.	Unit
t_{ASM}	Automatic Sleep Mode	t_{ACC}+30	ns

7.8 RESET#: Hardware Reset Pin

The RESET# pin provides a hardware method of resetting the device to reading array data. When the system drives the RESET# pin to V_{IL} for at least a period of t_{RP}, the device **immediately terminates** any operation in progress, tristates all data output pins, and ignores all read/write attempts for the duration of the RESET# pulse. The device also resets the internal state machine to reading array data. The operation that was interrupted should be reinitiated once the device is ready to accept another command sequence, to ensure data integrity.

Current is reduced for the duration of the RESET# pulse. When RESET# is held at $V_{SS} \pm 0.3$ V, the device draws CMOS standby current (I_{CC4}). If RESET# is held at V_{IL} but not within $V_{SS} \pm 0.3$ V, the standby current will be greater.

The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the Flash memory, enabling the system to read the boot-up firmware from the Flash memory.

If RESET# is asserted during a program or erase operation, the RY/BY# pin remains a *0* (busy) until the internal reset operation is complete, which requires a time of t_{READY} (during Embedded Algorithms). The system can thus monitor RY/BY# to determine whether the reset operation is complete. If RESET# is asserted when a program or erase operation is not executing (RY/BY# pin is *1*), the reset operation is completed within a time of t_{READY} (not during Embedded Algorithms). The system can read data t_{RH} after the RESET# pin returns to V_{IH}.

Refer to AC Characteristics on page 47 for RESET# parameters and to Figure 17.2 on page 48 for the timing diagram.

Not Recommended for New Design

7.9 Output Disable Mode

When the OE# input is at V_{IH}, output from the device is disabled. The output pins are placed in the high impedance state.

7.10 Sector Addresss Tables

Table 8. Model 00 Sector Addresses (Sheet 1 of 2)

Sector	A21	A20	A19	A18	A17	A16	Address Range (in hexadecimal)
SA0	0	0	0	0	0	0	000000–00FFFF
SA1	0	0	0	0	0	1	010000–01FFFF
SA2	0	0	0	0	1	0	020000–02FFFF
SA3	0	0	0	0	1	1	030000–03FFFF
SA4	0	0	0	1	0	0	040000–04FFFF
SA5	0	0	0	1	0	1	050000–05FFFF
SA6	0	0	0	1	1	0	060000–06FFFF
SA7	0	0	0	1	1	1	070000–07FFFF
SA8	0	0	1	0	0	0	080000–08FFFF
SA9	0	0	1	0	0	1	090000–09FFFF
SA10	0	0	1	0	1	0	0A0000–0AFFFF
SA11	0	0	1	0	1	1	0B0000–0BFFFF
SA12	0	0	1	1	0	0	0C0000–0CFFFF
SA13	0	0	1	1	0	1	0D0000–0DFFFF
SA14	0	0	1	1	1	0	0E0000–0EFFFF
SA15	0	0	1	1	1	1	0F0000–0FFFFF
SA16	0	1	0	0	0	0	100000–10FFFF
SA17	0	1	0	0	0	1	110000–11FFFF
SA18	0	1	0	0	1	0	120000–12FFFF
SA19	0	1	0	0	1	1	130000–13FFFF
SA20	0	1	0	1	0	0	140000–14FFFF
SA21	0	1	0	1	0	1	150000–15FFFF
SA22	0	1	0	1	1	0	160000–16FFFF
SA23	0	1	0	1	1	1	170000–17FFFF
SA24	0	1	1	0	0	0	180000–18FFFF
SA25	0	1	1	0	0	1	190000–19FFFF
SA26	0	1	1	0	1	0	1A0000–1AFFFF
SA27	0	1	1	0	1	1	1B0000–1BFFFF
SA28	0	1	1	1	0	0	1C0000–1CFFFF
SA29	0	1	1	1	0	1	1D0000–1DFFFF
SA30	0	1	1	1	1	0	1E0000–1EFFFF
SA31	0	1	1	1	1	1	1F0000–1FFFFF
SA32	1	0	0	0	0	0	200000–20FFFF
SA33	1	0	0	0	0	1	210000–21FFFF
SA34	1	0	0	0	1	0	220000–22FFFF
SA35	1	0	0	0	1	1	230000–23FFFF

Not Recommended for New Design

Table 8. Model 00 Sector Addresses (Sheet 2 of 2)

Sector	A21	A20	A19	A18	A17	A16	Address Range (in hexadecimal)
SA36	1	0	0	1	0	0	240000–24FFFF
SA37	1	0	0	1	0	1	250000–25FFFF
SA38	1	0	0	1	1	0	260000–26FFFF
SA39	1	0	0	1	1	1	270000–27FFFF
SA40	1	0	1	0	0	0	280000–28FFFF
SA41	1	0	1	0	0	1	290000–29FFFF
SA42	1	0	1	0	1	0	2A0000–2AFFFF
SA43	1	0	1	0	1	1	2B0000–2BFFFF
SA44	1	0	1	1	0	0	2C0000–2CFFFF
SA45	1	0	1	1	0	1	2D0000–2DFFFF
SA46	1	0	1	1	1	0	2E0000–2EFFFF
SA47	1	0	1	1	1	1	2F0000–2FFFFF
SA48	1	1	0	0	0	0	300000–30FFFF
SA49	1	1	0	0	0	1	310000–31FFFF
SA50	1	1	0	0	1	0	320000–32FFFF
SA51	1	1	0	0	1	1	330000–33FFFF
SA52	1	1	0	1	0	0	340000–34FFFF
SA53	1	1	0	1	0	1	350000–35FFFF
SA54	1	1	0	1	1	0	360000–36FFFF
SA55	1	1	0	1	1	1	370000–37FFFF
SA56	1	1	1	0	0	0	380000–38FFFF
SA57	1	1	1	0	0	1	390000–39FFFF
SA58	1	1	1	0	1	0	3A0000–3AFFFF
SA59	1	1	1	0	1	1	3B0000–3BFFFF
SA60	1	1	1	1	0	0	3C0000–3CFFFF
SA61	1	1	1	1	0	1	3D0000–3DFFFF
SA62	1	1	1	1	1	0	3E0000–3EFFFF
SA63	1	1	1	1	1	1	3F0000–3FFFFF

Note
All sectors are 64 Kbytes in size.

Not Recommended for New Design

Table 9. Model 00 Secured Silicon Sector Addresses

Sector Address A21–A7	Sector Size (bytes)	(x8) Address Range
000000000000000	128	000000h–00007fh
000000000001000	128	000400h-00047Fh

Table 10. Model 03 Sector Addresses (Sheet 1 of 2)

Sector	Sector Address A20–A12	Sector Size (Kbytes/ Kwords)	(x8) Address Range	(x16) Address Range
SA0	000000xxx	64/32	000000h–00FFFFh	000000h–07FFFh
SA1	000001xxx	64/32	010000h–01FFFFh	008000h–0FFFFh
SA2	000010xxx	64/32	020000h–02FFFFh	010000h–17FFFh
SA3	000011xxx	64/32	030000h–03FFFFh	018000h–01FFFFh
SA4	000100xxx	64/32	040000h–04FFFFh	020000h–027FFFh
SA5	000101xxx	64/32	050000h–05FFFFh	028000h–02FFFFh
SA6	000110xxx	64/32	060000h–06FFFFh	030000h–037FFFh
SA7	000111xxx	64/32	070000h–07FFFFh	038000h–03FFFFh
SA8	001000xxx	64/32	080000h–08FFFFh	040000h–047FFFh
SA9	001001xxx	64/32	090000h–09FFFFh	048000h–04FFFFh
SA10	001010xxx	64/32	0A0000h–0AFFFFh	050000h–057FFFh
SA11	001011xxx	64/32	0B0000h–0BFFFFh	058000h–05FFFFh
SA12	001100xxx	64/32	0C0000h–0CFFFFh	060000h–067FFFh
SA13	001101xxx	64/32	0D0000h–0DFFFFh	068000h–06FFFFh
SA14	001110xxx	64/32	0E0000h–0EFFFFh	070000h–077FFFh
SA15	001111xxx	64/32	0F0000h–0FFFFFh	078000h–07FFFFh
SA16	010000xxx	64/32	100000h–10FFFFh	080000h–087FFFh
SA17	010001xxx	64/32	110000h–11FFFFh	088000h–08FFFFh
SA18	010010xxx	64/32	120000h–12FFFFh	090000h–097FFFh
SA19	010011xxx	64/32	130000h–13FFFFh	098000h–09FFFFh
SA20	010100xxx	64/32	140000h–14FFFFh	0A0000h–0A7FFFh
SA21	010101xxx	64/32	150000h–15FFFFh	0A8000h–0AFFFFh
SA22	010110xxx	64/32	160000h–16FFFFh	0B0000h–0B7FFFh
SA23	010111xxx	64/32	170000h–17FFFFh	0B8000h–0BFFFFh
SA24	011000xxx	64/32	180000h–18FFFFh	0C0000h–0C7FFFh
SA25	011001xxx	64/32	190000h–19FFFFh	0C8000h–0CFFFFh
SA26	011010xxx	64/32	1A0000h–1AFFFFh	0D0000h–0D7FFFh
SA27	011011xxx	64/32	1B0000h–1BFFFFh	0D8000h–0DFFFFh
SA28	011100xxx	64/32	1C0000h–1CFFFFh	0E0000h–0E7FFFh
SA29	011101xxx	64/32	1D0000h–1DFFFFh	0E8000h–0EFFFFh
SA30	011110xxx	64/32	1E0000h–1EFFFFh	0F0000h–0F7FFFh
SA31	011111xxx	64/32	1F0000h–1FFFFFh	0F8000h–0FFFFFh
SA32	100000xxx	64/32	200000h–20FFFFh	100000h–107FFFh
SA33	100001xxx	64/32	210000h–21FFFFh	108000h–10FFFFh
SA34	100010xxx	64/32	220000h–22FFFFh	110000h–117FFFh
SA35	100011xxx	64/32	230000h–23FFFFh	118000h–11FFFFh
SA36	100100xxx	64/32	240000h–24FFFFh	120000h–127FFFh
SA37	100101xxx	64/32	250000h–25FFFFh	128000h–12FFFFh
SA38	100110xxx	64/32	260000h–26FFFFh	130000h–137FFFh
SA39	100111xxx	64/32	270000h–27FFFFh	138000h–13FFFFh
SA40	101000xxx	64/32	280000h–28FFFFh	140000h–147FFFh

Not Recommended for New Design

Table 10. Model 03 Sector Addresses (Sheet 2 of 2)

Sector	Sector Address A20–A12	Sector Size (Kbytes/ Kwords)	(x8) Address Range	(x16) Address Range
SA41	101001xxx	64/32	290000h–29FFFFh	148000h–14FFFFh
SA42	101010xxx	64/32	2A0000h–2AFFFFh	150000h–157FFFh
SA43	101011xxx	64/32	2B0000h–2BFFFFh	158000h–15FFFFh
SA44	101100xxx	64/32	2C0000h–2CFFFFh	160000h–167FFFh
SA45	101101xxx	64/32	2D0000h–2DFFFFh	168000h–16FFFFh
SA46	101110xxx	64/32	2E0000h–2EFFFFh	170000h–177FFFh
SA47	101111xxx	64/32	2F0000h–2FFFFFh	178000h–17FFFFh
SA48	110000xxx	64/32	300000h–30FFFFh	180000h–187FFFh
SA49	110001xxx	64/32	310000h–31FFFFh	188000h–18FFFFh
SA50	110010xxx	64/32	320000h–32FFFFh	190000h–197FFFh
SA51	110011xxx	64/32	330000h–33FFFFh	198000h–19FFFFh
SA52	110100xxx	64/32	340000h–34FFFFh	1A0000h–1A7FFFh
SA53	110101xxx	64/32	350000h–35FFFFh	1A8000h–1AFFFFh
SA54	110110xxx	64/32	360000h–36FFFFh	1B0000h–1B7FFFh
SA55	110111xxx	64/32	370000h–37FFFFh	1B8000h–1BFFFFh
SA56	111000xxx	64/32	380000h–38FFFFh	1C0000h–1C7FFFh
SA57	111001xxx	64/32	390000h–39FFFFh	1C8000h–1CFFFFh
SA58	111010xxx	64/32	3A0000h–3AFFFFh	1D0000h–1D7FFFh
SA59	111011xxx	64/32	3B0000h–3BFFFFh	1D8000h–1DFFFFh
SA60	111100xxx	64/32	3C0000h–3CFFFFh	1E0000h–1E7FFFh
SA61	111101xxx	64/32	3D0000h–3DFFFFh	1E8000h–1EFFFFh
SA62	111110xxx	64/32	3E0000h–3EFFFFh	1F0000h–1F7FFFh
SA63	111111000	8/4	3F0000h–3F1FFFh	1F8000h–1F8FFFh
SA64	111111001	8/4	3F2000h–3F3FFFh	1F9000h–1F9FFFh
SA65	111111010	8/4	3F4000h–3F5FFFh	1FA000h–1FAFFFh
SA66	111111011	8/4	3F6000h–3F7FFFh	1FB000h–1FBFFFh
SA67	111111100	8/4	3F8000h–3F9FFFh	1FC000h–1FCFFFh
SA68	111111101	8/4	3FA000h–3FBFFFh	1FD000h–1FDFFFh
SA69	111111110	8/4	3FC000h–3FDFFFh	1FE000h–1FEFFFh
SA70	111111111	8/4	3FE000h–3FFFFFh	1FF000h–1FFFFFh

Note
The address range is A20:A-1 in byte mode (BYTE#=V_{IL}) or A20:A0 in word mode (BYTE#=V_{IH}).

Table 11. Model 03 Secured Silicon Sector Addresses

Sector Address A20–A12	Sector Size (bytes/words)	(x8) Address Range	(x16) Address Range
111111111	256/128	3FFF00h–3FFFFFh	1FFF80h–1FFFFFh

Not Recommended for New Design

Table 12. Model 04 Sector Addresses (Sheet 1 of 2)

Sector	Sector Address A20–A12	Sector Size (Kbytes/ Kwords)	(x8) Address Range	(x16) Address Range
SA0	000000000	8/4	000000h-001FFFh	000000h–000FFFh
SA1	000000001	8/4	002000h-003FFFh	001000h–001FFFh
SA2	000000010	8/4	004000h-005FFFh	002000h–002FFFh
SA3	000000011	8/4	006000h-007FFFh	003000h–003FFFh
SA4	000000100	8/4	008000h-009FFFh	004000h–004FFFh
SA5	000000101	8/4	00A000h-00BFFFh	005000h–005FFFh
SA6	000000110	8/4	00C000h-00DFFFh	006000h–006FFFh
SA7	000000111	8/4	00E000h-00FFFFh	007000h–007FFFh
SA8	000001xxx	64/32	010000h-01FFFFh	008000h–00FFFFh
SA9	000010xxx	64/32	020000h-02FFFFh	010000h–017FFFh
SA10	000011xxx	64/32	030000h-03FFFFh	018000h–01FFFFh
SA11	000100xxx	64/32	040000h-04FFFFh	020000h–027FFFh
SA12	000101xxx	64/32	050000h-05FFFFh	028000h–02FFFFh
SA13	000110xxx	64/32	060000h-06FFFFh	030000h–037FFFh
SA14	000111xxx	64/32	070000h-07FFFFh	038000h–03FFFFh
SA15	001000xxx	64/32	080000h-08FFFFh	040000h–047FFFh
SA16	001001xxx	64/32	090000h-09FFFFh	048000h–04FFFFh
SA17	001010xxx	64/32	0A0000h-0AFFFFh	050000h–057FFFh
SA18	001011xxx	64/32	0B0000h-0BFFFFh	058000h–05FFFFh
SA19	001100xxx	64/32	0C0000h-0CFFFFh	060000h–067FFFh
SA20	001101xxx	64/32	0D0000h-0DFFFFh	068000h–06FFFFh
SA21	001110xxx	64/32	0E0000h-0EFFFFh	070000h–077FFFh
SA22	001111xxx	64/32	0F0000h-0FFFFFh	078000h–07FFFFh
SA23	010000xxx	64/32	100000h-10FFFFh	080000h–087FFFh
SA24	010001xxx	64/32	110000h-11FFFFh	088000h–08FFFFh
SA25	010010xxx	64/32	120000h-12FFFFh	090000h–097FFFh
SA26	010011xxx	64/32	130000h-13FFFFh	098000h–09FFFFh
SA27	010100xxx	64/32	140000h-14FFFFh	0A0000h–0A7FFFh
SA28	010101xxx	64/32	150000h-15FFFFh	0A8000h–0AFFFFh
SA29	010110xxx	64/32	160000h-16FFFFh	0B0000h–0B7FFFh
SA30	010111xxx	64/32	170000h-17FFFFh	0B8000h–0BFFFFh
SA31	011000xxx	64/32	180000h-18FFFFh	0C0000h–0C7FFFh
SA32	011001xxx	64/32	190000h-19FFFFh	0C8000h–0CFFFFh
SA33	011010xxx	64/32	1A0000h-1AFFFFh	0D0000h–0D7FFFh
SA34	011011xxx	64/32	1B0000h-1BFFFFh	0D8000h–0DFFFFh
SA35	011100xxx	64/32	1C0000h-1CFFFFh	0E0000h–0E7FFFh
SA36	011101xxx	64/32	1D0000h-1DFFFFh	0E8000h–0EFFFFh
SA37	011110xxx	64/32	1E0000h-1EFFFFh	0F0000h–0F7FFFh
SA38	011111xxx	64/32	1F0000h-1FFFFFh	0F8000h–0FFFFFh
SA39	100000xxx	64/32	200000h-20FFFFh	100000h–107FFFh

Not Recommended for New Design

Table 12. Model 04 Sector Addresses (Sheet 2 of 2)

Sector	Sector Address A20–A12	Sector Size (Kbytes/ Kwords)	(x8) Address Range	(x16) Address Range
SA40	100001xxx	64/32	210000h-21FFFFh	108000h–10FFFFh
SA41	100010xxx	64/32	220000h-22FFFFh	110000h–117FFFh
SA42	100011xxx	64/32	230000h-23FFFFh	118000h–11FFFFh
SA43	100100xxx	64/32	240000h-24FFFFh	120000h–127FFFh
SA44	100101xxx	64/32	250000h-25FFFFh	128000h–12FFFFh
SA45	100110xxx	64/32	260000h-26FFFFh	130000h–137FFFh
SA46	100111xxx	64/32	270000h-27FFFFh	138000h–13FFFFh
SA47	101000xxx	64/32	280000h-28FFFFh	140000h–147FFFh
SA48	101001xxx	64/32	290000h-29FFFFh	148000h–14FFFFh
SA49	101010xxx	64/32	2A0000h-2AFFFFh	150000h–157FFFh
SA50	101011xxx	64/32	2B0000h-2BFFFFh	158000h–15FFFFh
SA51	101100xxx	64/32	2C0000h-2CFFFFh	160000h–167FFFh
SA52	101101xxx	64/32	2D0000h-2DFFFFh	168000h–16FFFFh
SA53	101110xxx	64/32	2E0000h-2EFFFFh	170000h–177FFFh
SA54	101111xxx	64/32	2F0000h-2FFFFFh	178000h–17FFFFh
SA55	111000xxx	64/32	300000h-30FFFFh	180000h–187FFFh
SA56	110001xxx	64/32	310000h-31FFFFh	188000h–18FFFFh
SA57	110010xxx	64/32	320000h-32FFFFh	190000h–197FFFh
SA58	110011xxx	64/32	330000h-33FFFFh	198000h–19FFFFh
SA59	110100xxx	64/32	340000h-34FFFFh	1A0000h–1A7FFFh
SA60	110101xxx	64/32	350000h-35FFFFh	1A8000h–1AFFFFh
SA61	110110xxx	64/32	360000h-36FFFFh	1B0000h–1B7FFFh
SA62	110111xxx	64/32	370000h-37FFFFh	1B8000h–1BFFFFh
SA63	111000xxx	64/32	380000h-38FFFFh	1C0000h–1C7FFFh
SA64	111001xxx	64/32	390000h-39FFFFh	1C8000h–1CFFFFh
SA65	111010xxx	64/32	3A0000h-3AFFFFh	1D0000h–1D7FFFh
SA66	111011xxx	64/32	3B0000h-3BFFFFh	1D8000h–1DFFFFh
SA67	111100xxx	64/32	3C0000h-3CFFFFh	1E0000h–1E7FFFh
SA68	111101xxx	64/32	3D0000h-3DFFFFh	1E8000h–1EFFFFh
SA69	111110xxx	64/32	3E0000h-3EFFFFh	1F0000h–1F7FFFh
SA70	111111xxx	64/32	3F0000h-3FFFFFh	1F8000h–1FFFFFh

Not Recommended for New Design

Note
The address range is A20:A-1 in byte mode (BYTE#=V_{IL}) or A20:A0 in word mode (BYTE#=V_{IH}).

Table 13. Model 04 Secured Silicon Sector Addresses

Sector Address A20–A12	Sector Size (bytes/words)	(x8) Address Range	(x16) Address Range
000000000	256/128	000000h-0000FFh	00000h-0007Fh

7.11 Autoselect Mode

The autoselect mode provides manufacturer and device identification, and sector protection verification, through identifier codes output on DQ7–DQ0. This mode is primarily intended for programming equipment to automatically match a device to be programmed with its corresponding programming algorithm. However, the autoselect codes can also be accessed in-system through the command register.

When using programming equipment, the autoselect mode requires V_{ID} (11.5 V to 12.5 V) on address pin A9. Address pins A6, A1, and A0 must be as shown in Table 8. In addition, when verifying sector protection, the sector address must appear on the appropriate highest order address bits (see Table 8 on page 13 and Table 10 on page 15). Table 8 shows the remaining address bits that are don't care. When all necessary bits have been set as required, the programming equipment may then read the corresponding identifier code on DQ7-DQ0.

To access the autoselect codes in-system, the host system can issue the autoselect command via the command register, as shown in Table 13 on page 35. This method does not require V_{ID}. See Command Definitions for details on using the autoselect mode.

Table 8. S29AL032D Autoselect Codes (High Voltage Method)

Description	Mode	CE#	OE#	WE#	A21 to A12	A11 to A10	A9	A8 to A7	A6	A5 to A4	A3 to A2	A1	A0	DQ8 to DQ15	DQ7 to DQ0
Manufacturer ID: Spansion		L	L	H	X	X	V_{ID}	X	L	X	L	L	L	X	01h
Device ID: S29AL032D (Model 00)	Byte	L	L	H	X	X	V_{ID}	X	L	X	L	L	H	N/A	A3h
Device ID: S29AL032D (Model 03)	Word	L	L	H	X	X	V_{ID}	X	L	X	L	L	H	22h	F6h
	Byte	L	L	H										X	F6h
Device ID: S29AL032D (Model 04)	Word	L	L	H	X	X	V_{ID}	X	L	X	L	L	H	22h	F9h
	Byte	L	L	H										X	F9h
Sector Protection Verification		L	L	H	SA	X	V_{ID}	X	L	X	L	H	L	X	01h (protected)
														X	00h (unprotected)
Secured Silicon Sector Indicator Bit (DQ7) (Model 00)		L	L	H	X	X	V_{ID}	X	L	X	L	H	H	X	85 (factory locked)
														X	05 (not factory locked)
Secured Silicon Sector Indicator Bit (DQ7) (Model 03)		L	L	H	X	X	V_{ID}	X	L	X	L	H	H	X	8D (factory locked)
														X	1D (not factory locked)
Secured Silicon Sector Indicator Bit (DQ7) (Model 04)		L	L	H	X	X	V_{ID}	X	L	X	L	H	H	X	9D (factory locked)
														X	0D (not factory locked)

Not Recommended for New Design

Legend

L = Logic Low = V_{IL}, H = Logic High = V_{IH}, SA = Sector Address, X = Don't care.

Note

The autoselect codes may also be accessed in-system via command sequences. See Table 13 on page 35.

7.12 Sector Protection/Unprotection

The hardware sector protection feature disables both program and erase operations in any sector. The hardware sector unprotection feature re-enables both program and erase operations in previously protected sectors.

The device is shipped with all sectors unprotected. Spansion offers the option of programming and protecting sectors at its factory prior to shipping the device through the Spansion ExpressFlash™ Service. Contact a Spansion representative for further details.

It is possible to determine whether a sector is protected or unprotected. See Autoselect Mode for details.

Sector protection/unprotection can be implemented via two methods.

The primary method requires V_{ID} on the RESET# pin only, and can be implemented either in-system or via programming equipment. Figure 10.1 on page 23 shows the algorithms and Figure 18.3 on page 55 shows the timing diagram. This method uses standard microprocessor bus cycle timing. For sector unprotect, all unprotected sectors must first be protected prior to the first sector unprotect write cycle.

The alternate method intended only for programming equipment requires V_{ID} on address pin A9 and OE#. This method is compatible with programmer routines written for earlier 3.0-volt-only Spansion flash devices. Details on this method are provided in a supplement, publication number 21468. Contact a Spansion representative to request a copy.

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Table 8. Sector Block Addresses for Protection/Unprotection — Model 00

Sector/Sector Block	A21–A16	Sector/Sector Block Size
SA0	000000	64 Kbytes
SA1-SA3	000001, 000010, 000011	192 (3x64) Kbytes
SA4-SA7	000100, 000101, 000110, 000111	256 (4x64) Kbytes
SA8-SA11	001000, 001001, 001010, 001011	256 (4x64) Kbytes
SA12-SA15	001100, 001101, 001110, 001111	256 (4x64) Kbytes
SA16-SA19	010000, 010001, 010010, 010011	256 (4x64) Kbytes
SA20-SA23	010100, 010101, 010110, 010111	256 (4x64) Kbytes
SA24-SA27	011000, 011001, 011010, 011011	256 (4x64) Kbytes
SA28-SA31	011100, 011101, 011110, 011111	256 (4x64) Kbytes
SA32-SA35	100000, 100001, 100010, 100011	256 (4x64) Kbytes
SA36-SA39	100100, 100101, 100110, 100111	256 (4x64) Kbytes
SA40-SA43	101000, 101001, 101010, 101011	256 (4x64) Kbytes
SA44-SA47	101100, 101101, 101110, 101111	256 (4x64) Kbytes
SA48-SA51	110000, 110001, 110010, 110011	256 (4x64) Kbytes
SA52-SA55	110100, 110101, 110110, 110111	256 (4x64) Kbytes
SA56-SA59	111000, 111001, 111010, 111011	256 (4x64) Kbytes
SA60-SA62	111100, 111101, 111110	192 (4x64) Kbytes
SA63	111111	64 Kbytes

Table 9. Sector Block Addresses for Protection/Unprotection — Model 03 (Sheet 1 of 2)

Sector / Sector Block	A20–A12	Sector/Sector Block Size
SA0-SA3	000000XXX, 000001XXX, 000010XXX, 000011XXX	256 (4x64) Kbytes
SA4-SA7	0001XXXXX	256 (4x64) Kbytes
SA8-SA11	0010XXXXX	256 (4x64) Kbytes
SA12-SA15	0011XXXXX	256 (4x64) Kbytes
SA16-SA19	0100XXXXX	256 (4x64) Kbytes

Table 9. Sector Block Addresses for Protection/Unprotection — Model 03 (Sheet 2 of 2)

Sector / Sector Block	A20–A12	Sector/Sector Block Size
SA20-SA23	0101XXXXX	256 (4x64) Kbytes
SA24-SA27	0110XXXXX	256 (4x64) Kbytes
SA28-SA31	0111XXXXX	256 (4x64) Kbytes
SA32-SA35	1000XXXXX	256 (4x64) Kbytes
SA36-SA39	1001XXXXX	256 (4x64) Kbytes
SA40-SA43	1010XXXXX	256 (4x64) Kbytes
SA44-SA47	1011XXXXX	256 (4x64) Kbytes
SA48-SA51	1100XXXXX	256 (4x64) Kbytes
SA52-SA55	1101XXXXX	256 (4x64) Kbytes
SA56-SA59	1110XXXXX	256 (4x64) Kbytes
SA60-SA62	111100XXX, 111101XXX, 111110XXX	192 (3x64) Kbytes
SA63	111111000	8 Kbytes
SA64	111111001	8 Kbytes
SA65	111111010	8 Kbytes
SA66	111111011	8 Kbytes
SA67	111111100	8 Kbytes
SA68	111111101	8 Kbytes
SA69	111111110	8 Kbytes
SA70	111111111	8 Kbytes

Table 10. Sector Block Addresses for Protection/Unprotection — Model 04

Sector / Sector Block	A20–A12	Sector/Sector Block Size
SA70-SA67	111111XXX, 111110XXX, 111101XXX, 111100XXX	256 (4x64) Kbytes
SA66-SA63	1110XXXXX	256 (4x64) Kbytes
SA62-SA59	1101XXXXX	256 (4x64) Kbytes
SA58-SA55	1100XXXXX	256 (4x64) Kbytes
SA54-SA51	1011XXXXX	256 (4x64) Kbytes
SA50-SA47	1010XXXXX	256 (4x64) Kbytes
SA46-SA43	1001XXXXX	256 (4x64) Kbytes
SA42-SA39	1000XXXXX	256 (4x64) Kbytes
SA38-SA35	0111XXXXX	256 (4x64) Kbytes
SA34-SA31	0110XXXXX	256 (4x64) Kbytes
SA30-SA27	0101XXXXX	256 (4x64) Kbytes
SA26-SA23	0100XXXXX	256 (4x64) Kbytes
SA22–SA19	0011XXXXX	256 (4x64) Kbytes
SA18-SA15	0010XXXXX	256 (4x64) Kbytes
SA14-SA11	0001XXXXX	256 (4x64) Kbytes
SA10-SA8	000011XXX, 000010XXX, 000001XXX	192 (3x64) Kbytes
SA7	000000111	8 Kbytes
SA6	000000110	8 Kbytes
SA5	000000101	8 Kbytes

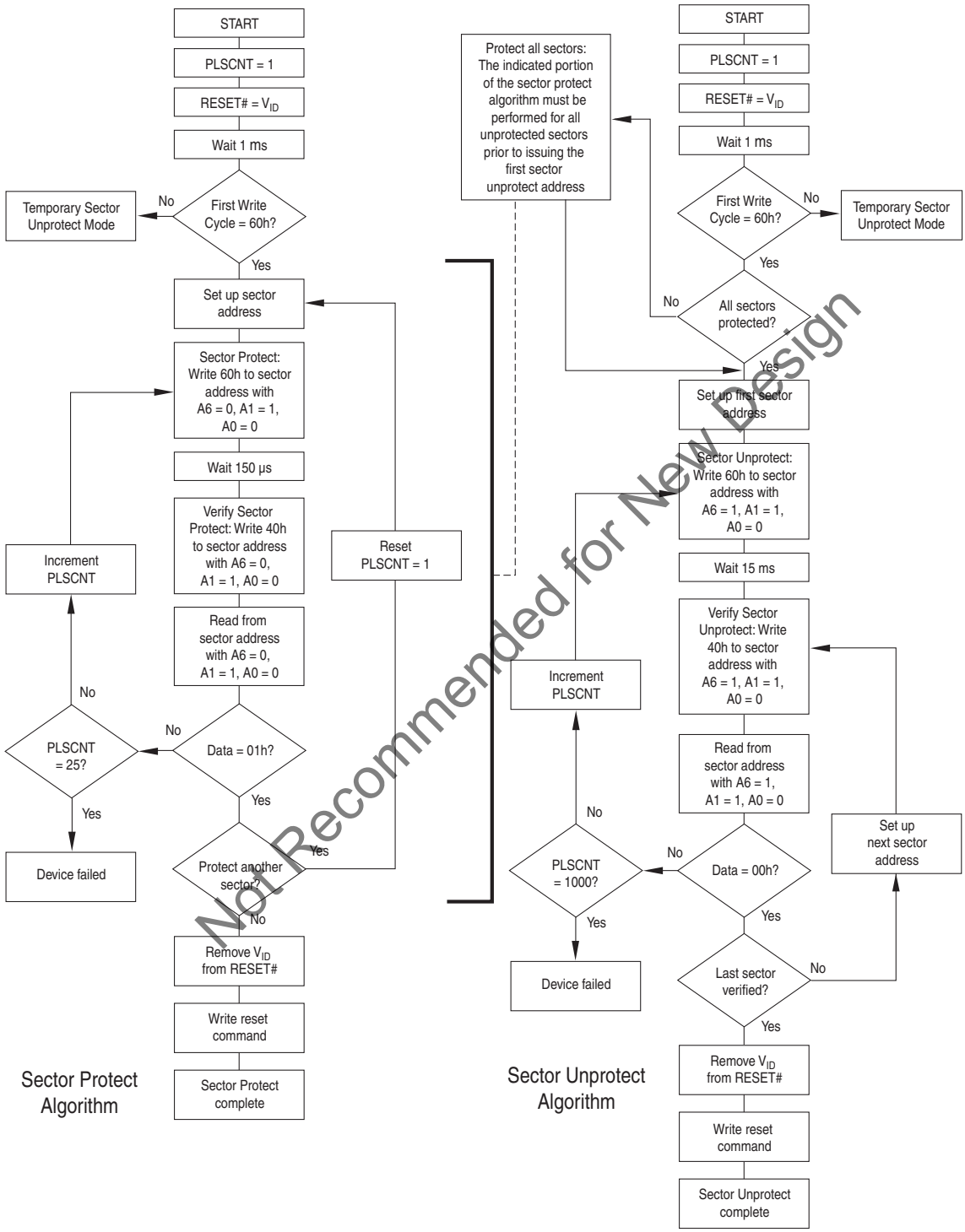
Not Recommended for New Design

Table 10. Sector Block Addresses for Protection/Unprotection — Model 04

Sector / Sector Block	A20–A12	Sector/Sector Block Size
SA4	000000100	8 Kbytes
SA3	000000011	8 Kbytes
SA2	000000010	8 Kbytes
SA1	000000001	8 Kbytes
SA0	000000000	8 Kbytes

Not Recommended for New Design

Figure 10.1 In-System Sector Protect/Unprotect Algorithms



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7.13 Write Protect (WP#) — Models 03, 04 Only

The Write Protect function provides a hardware method of protecting certain boot sectors without using V_{ID}. This function is one of two provided by the WP#/ACC pin.

If the system asserts V_{IL} on the WP#/ACC pin, the device disables program and erase functions in the two *outermost* 8-Kbyte boot sectors independently of whether those sectors were protected or unprotected using the method described in Sector Protection/ Unprotection on page 20. The two outermost 8-Kbyte boot sectors are the two sectors containing the lowest addresses in a bottom-boot-configured device, or the two sectors containing the highest addresses in a top-boot-configured device.

If the system asserts V_{IH} on the WP#/ACC pin, the device reverts to whether the two outermost 8-KByte boot sectors were last set to be protected or unprotected. That is, sector protection or unprotection for these two sectors depends on whether they were last protected or unprotected using the method described in Sector Protection/Unprotection on page 20.

Note that the WP#/ACC pin must not be left floating or unconnected; inconsistent behavior of the device may result.

7.14 Temporary Sector Unprotect

This feature allows temporary unprotection of previously protected sectors to change data in-system. The Sector Unprotect mode is activated by setting the RESET# pin to V_{ID}. During this mode, formerly protected sectors can be programmed or erased by selecting the sector addresses. Once V_{ID} is removed from the RESET# pin, all the previously protected sectors are protected again. Figure , shows the algorithm, and Figure 18.1 on page 53 shows the timing diagrams, for this feature.

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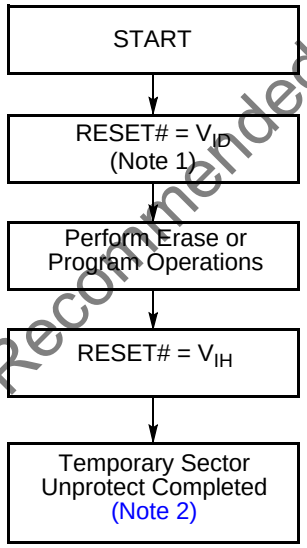
Figure 7.2 Temporary Sector Unprotect Operation



Notes

1. *All protected sectors unprotected.*
2. *All previously protected sectors are protected once again.*

8. Secured Silicon Sector Flash Memory Region

The Secured Silicon Sector feature provides a 256-byte Flash memory region that enables permanent part identification through an Electronic Serial Number (ESN). The Secured Silicon Sector uses a Secured Silicon Sector Indicator Bit (DQ7) to indicate whether or not the Secured Silicon Sector is locked when shipped from the factory. This bit is permanently set at the factory and cannot be changed, which prevents cloning of a factory-locked part. This ensures the security of the ESN once the product is shipped to the field.

Spansion offers the device with the Secured Silicon Sector either factory-locked or customer-lockable. The factory-locked version is always protected when shipped from the factory, and has the Secured Silicon Sector Indicator Bit permanently set to a *1.* The customer-lockable version is shipped with the Secured Silicon Sector unprotected, allowing customers to utilize the that sector in any manner they choose. The customer-lockable version has the Secured Silicon Sector Indicator Bit permanently set to a *0.* Thus, the Secured Silicon Sector Indicator Bit prevents customer-lockable devices from being used to replace devices that are factory locked.

The system accesses the Secured Silicon Sector through a command sequence (see Enter Secured Silicon Sector/Exit Secured Silicon Sector Command Sequence on page 30). After the system writes the Enter Secured Silicon Sector command sequence, it may read the Secured Silicon Sector by using the addresses normally occupied by the boot sectors. This mode of operation continues until the system issues the Exit Secured Silicon Sector command sequence, or until power is removed from the device. On power-up, or following a hardware reset, the device reverts to sending commands to the boot sectors.

8.1 Factory Locked: Secured Silicon Sector Programmed and Protected at the Factory

In a factory locked device, the Secured Silicon Sector is protected when the device is shipped from the factory. The Secured Silicon Sector cannot be modified in any way. The device is available pre-programmed with one of the following:

- A random, secure ESN only.
- Customer code through the ExpressFlash service.
- Both a random, secure ESN and customer code through the ExpressFlash service.

In devices that have an ESN, a Bottom Boot device has the 16-byte (8-word) ESN in sector 0 at addresses 00000h–0000Fh in byte mode (or 00000h–00007h in word mode). In the Top Boot device, the ESN is in sector 70 at addresses 3FFF00h–3FFF0Fh in byte mode (or 1FFF80h–1FFF87h in word mode). In the Uniform device, the ESN is in sector 63 at addresses 3FFF00h-3FFF0Fh in byte mode (or 1FFF80h-1FFF87h in word mode).

Customers may opt to have their code programmed by Spansion through the Spansion ExpressFlash service. Spansion programs the customer's code, with or without the random ESN. The devices are then shipped from the Spansion factory with the Secured Silicon Sector permanently locked. Contact a Spansion representative for details on using the Spansion ExpressFlash service.

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8.2 Customer Lockable: Secured Silicon Sector NOT Programmed or Protected at the Factory

The customer lockable version allows the Secured Silicon Sector to be programmed once, and then permanently locked after it ships from Spansion. Note that the accelerated programming (ACC) and unlock bypass functions are not available when programming the Secured Silicon Sector.

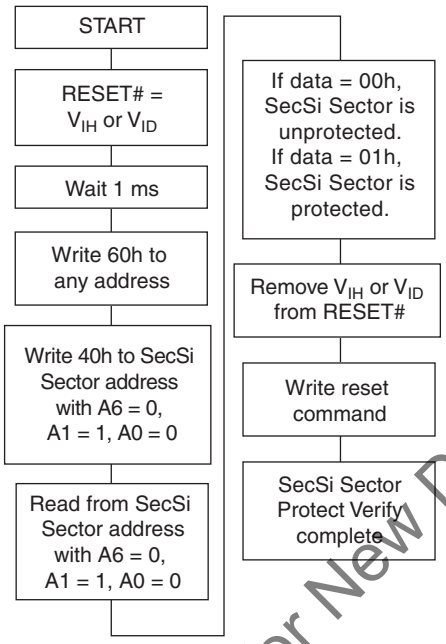
The Secured Silicon Sector area can be protected using the following procedures:

- Write the three-cycle Enter Secured Silicon Region command sequence, and then follow the in-system sector protect algorithm as shown in Figure 10.1 on page 23, except that *RESET# may be at either V_{IH} or V_{ID}*. This allows in-system protection of the Secured Silicon Sector without raising any device pin to a high voltage. Note that this method is only applicable to the Secured Silicon Sector.
- To verify the protect/unprotect status of the Secured Silicon Sector, follow the algorithm shown in Figure 8.1 on page 26.

Once the Secured Silicon Sector is locked and verified, the system must write the Exit Secured Silicon Sector Region command sequence to return to reading and writing the remainder of the array.

The Secured Silicon Sector protection must be used with caution since, once protected, there is no procedure available for unprotecting the Secured Silicon Sector area, and none of the bits in the Secured Silicon Sector memory space can be modified in any way.

Figure 8.1 Secured Silicon Sector Protect Verify



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9. Hardware Data Protection

The command sequence requirement of unlock cycles for programming or erasing provides data protection against inadvertent writes (refer to Table 13 on page 35 for command definitions). In addition, the following hardware data protection measures prevent accidental erasure or programming, which might otherwise be caused by spurious system level signals during V_{CC} power-up and power-down transitions, or from system noise.

9.1 Low V_{CC} Write Inhibit

When V_{CC} is less than V_{LKO}, the device does not accept any write cycles. This protects data during V_{CC} power-up and power-down. The command register and all internal program/erase circuits are disabled, and the device resets. Subsequent writes are ignored until V_{CC} is greater than V_{LKO}. The system must provide the proper signals to the control pins to prevent unintentional writes when V_{CC} is greater than V_{LKO}.

9.2 Write Pulse “Glitch” Protection

Noise pulses of less than 5 ns (typical) on OE#, CE# or WE# do not initiate a write cycle.

9.3 Logical Inhibit

Write cycles are inhibited by holding any one of OE# = V_{IL}, CE# = V_{IH} or WE# = V_{IH}. To initiate a write cycle, CE# and WE# must be a logical zero while OE# is a logical one.

9.4 Power-Up Write Inhibit

If WE# = CE# = V_{IL} and OE# = V_{IH} during power up, the device does not accept commands on the rising edge of WE#. The internal state machine is automatically reset to reading array data on power-up.

10. Common Flash Memory Interface (CFI)

The Common Flash Interface (CFI) specification outlines device and host system software interrogation handshake, which allows specific vendor-specified software algorithms to be used for entire families of devices. Software support can then be device-independent, JEDEC ID-independent, and forward- and backward-compatible for the specified flash device families. Flash vendors can standardize their existing interfaces for long-term compatibility.

This device enters the CFI Query mode when the system writes the CFI Query command, 98h, to address 55h in word mode (or address AAh in byte mode), any time the device is ready to read array data. The system can read CFI information at the addresses given in Tables 11–14. In word mode, the upper address bits (A7–MSB) must be all zeros. To terminate reading CFI data, the system must write the reset command.

The system can also write the CFI query command when the device is in the autoselect mode. The device enters the CFI query mode, and the system can read CFI data at the addresses given in Tables 11–14. The system must write the reset command to return the device to the autoselect mode.

For further information, please contact a Spansion representative for a copy of this document.

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Table 11. CFI Query Identification String

Addresses	Addresses (Models 03, 04 Byte Mode Only)	Data	Description
10h 11h 12h	20h 22h 24h	0051h 0052h 0059h	Query Unique ASCII string QRY
13h 14h	26h 28h	0002h 0000h	Primary OEM Command Set
15h 16h	2Ah 2Ch	0040h 0000h	Address for Primary Extended Table
17h 18h	2Eh 30h	0000h 0000h	Alternate OEM Command Set (00h = none exists)
19h 1Ah	32h 34h	0000h 0000h	Address for Alternate OEM Extended Table (00h = none exists)

Table 12. System Interface String

Addresses	Addresses (Models 03, 04 Byte Mode Only)	Data	Description
1Bh	36h	0027h	V_{CC} Min. (write/erase) D7–D4: volt, D3–D0: 100 millivolt
1Ch	38h	0036h	V_{CC} Max. (write/erase) D7–D4: volt, D3–D0: 100 millivolt
1Dh	3Ah	0000h	V_{PP} Min. voltage (00h = no V_{PP} pin present)
1Eh	3Ch	0000h	V_{PP} Max. voltage (00h = no V_{PP} pin present)
1Fh	3Eh	0004h	Typical timeout per single byte/word write 2^N µs
20h	40h	0000h	Typical timeout for Min. size buffer write 2^N µs (00h = not supported)
21h	42h	000Ah	Typical timeout per individual block erase 2^N ms
22h	44h	0000h	Typical timeout for full chip erase 2^N ms (00h = not supported)
23h	46h	0005h	Max. timeout for byte/word write 2^N times typical
24h	48h	0000h	Max. timeout for buffer write 2^N times typical
25h	4Ah	0004h	Max. timeout per individual block erase 2^N times typical
26h	4Ch	0000h	Max. timeout for full chip erase 2^N times typical (00h = not supported)

Table 13. Device Geometry Definition

Addresses	Addresses (Models 03, 04 Byte Mode Only)	Data	Description
27h	4Eh	0016h	Device Size = 2^N byte
28h 29h	50h 52h	000xh 0000h	Flash Device Interface description (refer to CFI publication 100) (0 = Model 00, 2 = Models 03, 04)
2Ah 2Bh	54h 56h	0000h 0000h	Max. number of byte in multi-byte write = 2^N (00h = not supported)
2Ch	58h	000xh	Number of Erase Block Regions within device (1 = Model 00, 2 = Models 03, 04)
2Dh 2Eh 2Fh 30h	5Ah 5Ch 5Eh 60h	00xxh 0000h 00x0h 000xh	Erase Block Region 1 Information (refer to the CFI specification or CFI publication 100) (003F, 0000, 0000, 0001) = Model 00 (0007, 0000, 0020, 0000) = Models 03, 04
31h 32h 33h 34h	62h 64h 66h 68h	00xxh 0000h 0020h 000xh	Erase Block Region 2 Information (0000, 0000, 0000, 0000) = Model 00 (003E, 0000, 0000, 0001) = Models 03, 04
35h 36h 37h 38h	6Ah 6Ch 6Eh 70h	0000h 0000h 0000h 0000h	Erase Block Region 3 Information
39h 3Ah 3Bh 3Ch	72h 74h 76h 78h	0000h 0000h 0000h 0000h	Erase Block Region 4 Information

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Table 14. Primary Vendor-Specific Extended Query (Sheet 1 of 2)

Addresses	Addresses (Models 03, 04 Byte Mode Only)	Data	Description
40h 41h 42h	80h 82h 84h	0050h 0052h 0049h	Query-unique ASCII string “PRI”
43h	86h	0031h	Major version number, ASCII
44h	88h	0031h	Minor version number, ASCII
45h	8Ah	000xh	Address Sensitive Unlock 0 = Required (Models 03, 04), 1 = Not Required (Model 00)
46h	8Ch	0002h	Erase Suspend 0 = Not Supported, 1 = To Read Only, 2 = To Read & Write
47h	8Eh	0001h	Sector Protect 0 = Not Supported, X = Number of sectors in per group
48h	90h	0001h	Sector Temporary Unprotect 00 = Not Supported, 01 = Supported
49h	92h	0004h	Sector Protect/Unprotect scheme 01 = 29F040 mode, 02 = 29F016 mode, 03 = 29F400 mode, 04 = 29LV800A mode
4Ah	94h	0000h	Simultaneous Operation 00 = Not Supported, 01 = Supported

Table 14. Primary Vendor-Specific Extended Query (Sheet 2 of 2)

Addresses	Addresses (Models 03, 04 Byte Mode Only)	Data	Description
4Bh	96h	0000h	Burst Mode Type 00 = Not Supported, 01 = Supported
4Ch	98h	0000h	Page Mode Type 00 = Not Supported, 01 = 4 Word Page, 02 = 8 Word Page
4Dh	9Ah	00B5h	ACC (Acceleration) Supply Minimum 00h = Not Supported, D7-D4: Volt, D3-D0: 100 mV
4Eh	9Ch	00C5h	ACC (Acceleration) Supply Maximum 00h = Not Supported, D7-D4: Volt, D3-D0: 100 mV
4Fh	9Eh	000xh	Top/Bottom Boot Sector Flag (0 = Model 00, 3 = Model 03, 2 = Model 04)

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11. Command Definitions

Writing specific address and data commands or sequences into the command register initiates device operations. Table 13 on page 35 defines the valid register command sequences. Writing **incorrect address and data values** or writing them in the **improper sequence** resets the device to reading array data.

All addresses are latched on the falling edge of WE# or CE#, whichever happens later. All data is latched on the rising edge of WE# or CE#, whichever happens first. Refer to the appropriate timing diagrams under AC Characteristics.

11.1 Reading Array Data

The device is automatically set to reading array data after device power-up. No commands are required to retrieve data. The device is also ready to read array data after completing an Embedded Program or Embedded Erase algorithm.

After the device accepts an Erase Suspend command, the device enters the Erase Suspend mode. The system can read array data using the standard read timings, except that if it reads at an address within erase-suspended sectors, the device outputs status data. After completing a programming operation in the Erase Suspend mode, the system may once again read array data with the same exception. See Erase Suspend/Erase Resume Commands on page 32 for more information on this mode.

The system *must* issue the reset command in order to re-enable the device for reading array data if DQ5 goes high, or while in the autoselect mode. See Reset Command on page 29.

See also Requirements for Reading Array Data on page 11 for more information. The Read Operations on page 47 provides the read parameters, and Figure 17.1 on page 47 shows the timing diagram.

11.2 Reset Command

Writing the reset command to the device resets the device to reading array data. Address bits are don't care for this command.

The reset command may be written between the sequence cycles in an erase command sequence before erasing begins. This resets the device to reading array data. Once erasure begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in a program command sequence before programming begins. This resets the device to reading array data (also applies to programming in Erase Suspend mode). Once programming begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in an autoselect command sequence. Once in the autoselect mode, the reset command *must* be written to return to reading array data (also applies to autoselect during Erase Suspend).

If DQ5 goes high during a program or erase operation, writing the reset command returns the device to reading array data (also applies during Erase Suspend).

11.3 Autoselect Command Sequence

The autoselect command sequence allows the host system to access the manufacturer and devices codes, and determine whether a sector is protected. Table 13 on page 35 shows the address and data requirements. This method is an alternative to that shown in Table on page 19, which is intended for PROM programmers and requires V_{ID} on address bit A9.

The autoselect command sequence is initiated by writing two unlock cycles, followed by the autoselect command. The device then enters the autoselect mode, and the system may read at any address any number of times, without initiating another command sequence.

A read cycle at address 0XXX00h retrieves the manufacturer code. A read cycle at address 0XXX01h returns the device code. A read cycle containing a sector address (SA) and the address 02h in word mode (or 04h in byte mode) returns 01h if that sector is protected, or 00h if it is unprotected. Refer to Table 8 on page 13 and Table 10 on page 15 for valid sector addresses.

The system must write the reset command to exit the autoselect mode and return to reading array data.

11.4 Enter Secured Silicon Sector/Exit Secured Silicon Sector Command Sequence

The Secured Silicon Sector region provides a secured data area containing a random, sixteen-byte electronic serial number (ESN). The system can access the Secured Silicon Sector region by issuing the three-cycle Enter Secured Silicon Sector command sequence. The device continues to access the Secured Silicon Sector region until the system issues the four-cycle Exit Secured Silicon Sector command sequence. The Exit Secured Silicon Sector command sequence returns the device to normal operation. Table 12 on page 34 and Table 13 on page 35 show the addresses and data requirements for both command sequences. Note that the ACC function and unlock bypass modes are not available when the device enters the Secured Silicon Sector. See also Secured Silicon Sector Flash Memory Region on page 24 for further information.

Not Recommended for New Design

11.5 Word/Byte Program Command Sequence

Models 03, 04 may program the device by word or byte, depending on the state of the BYTE# pin. Model 00 may program the device by byte only. Programming is a four-bus-cycle operation. The program command sequence is initiated by writing two unlock write cycles, followed by the program set-up command. The program address and data are written next, which in turn initiate the Embedded Program algorithm. The system is *not* required to provide further controls or timings. The device automatically generates the program pulses and verifies the programmed cell margin. Table 13 on page 35 shows the address and data requirements for the byte program command sequence.

When the Embedded Program algorithm is complete, the device then returns to reading array data and addresses are no longer latched. The system can determine the status of the program operation by using DQ7, DQ6, or RY/BY#. See Write Operation Status on page 37 for information on these status bits.

Any commands written to the device during the Embedded Program Algorithm are ignored. Note that a **hardware reset** immediately terminates the programming operation. The Byte Program command sequence should be reinitiated once the device has reset to reading array data, to ensure data integrity.

Programming is allowed in any sequence and across sector boundaries. **A bit cannot be programmed from a *0* back to a *1*.** Attempting to do so may halt the operation and set DQ5 to *1,* or cause the Data# Polling algorithm to indicate the operation was successful. However, a succeeding read will show that the data is still *0*. Only erase operations can convert a *0* to a *1*.

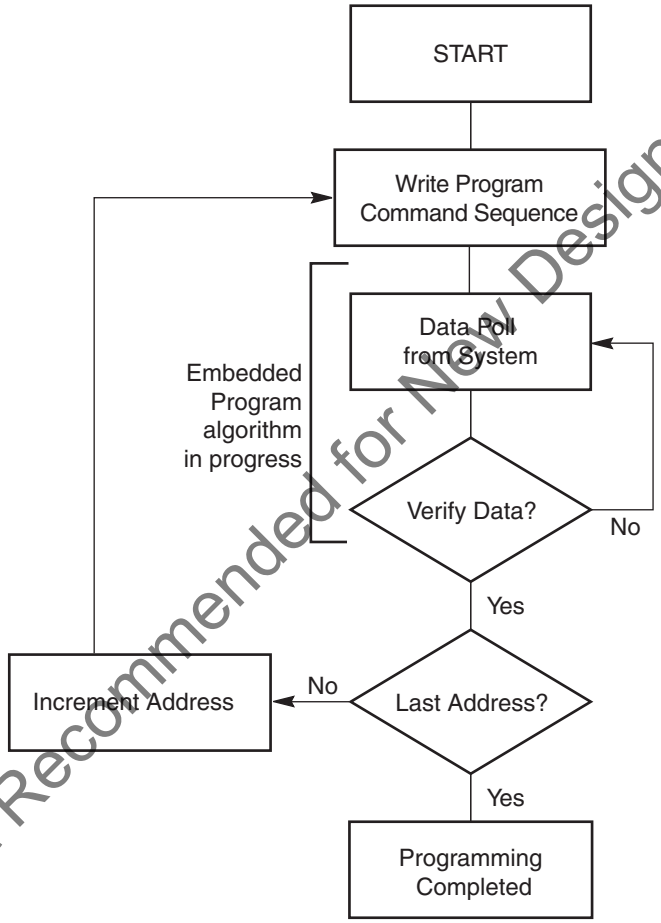
11.6 Unlock Bypass Command Sequence

The unlock bypass feature allows the system to program bytes or words to the device faster than using the standard program command sequence. The unlock bypass command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle containing the unlock bypass command, 20h. The device then enters the unlock bypass mode. A two-cycle unlock bypass program command sequence is all that is required to program in this mode. The first cycle in this sequence contains the unlock bypass program command, A0h; the second cycle contains the program address and data. Additional data is programmed in the same manner. This mode dispenses with the initial two unlock cycles required in the standard program command sequence, resulting in faster total programming time. Table 13 on page 35 shows the requirements for the command sequence.

During the unlock bypass mode, only the Unlock Bypass Program and Unlock Bypass Reset commands are valid. To exit the unlock bypass mode, the system must issue the two-cycle unlock bypass reset command sequence. The first cycle must contain the data 90h; the second cycle the data 00h. Addresses are don't care for both cycles. The device then returns to reading array data.

Figure 11.1 on page 31 illustrates the algorithm for the program operation. See the Erase/Program Operations on page 50 for parameters, and to Figure 18.1 on page 50 for timing diagrams.

Figure 11.1 Program Operation



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Note
See Table 13 for program command sequence.

11.7 Chip Erase Command Sequence

Chip erase is a six bus-cycle operation. The chip erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the chip erase command, which in turn invokes the Embedded Erase algorithm. The device does *not* require the system to preprogram prior to erase. The Embedded Erase algorithm automatically preprograms and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations. Table 13 on page 35 shows the address and data requirements for the chip erase command sequence.

Any commands written to the chip during the Embedded Erase algorithm are ignored. Note that a **hardware reset** during the chip erase operation immediately terminates the operation. The Chip Erase command sequence should be reinitiated once the device has returned to reading array data, to ensure data integrity.

The system can determine the status of the erase operation by using DQ7, DQ6, DQ2, or RY/BY#. See Write Operation Status on page 37 for information on these status bits. When the Embedded Erase algorithm is complete, the device returns to reading array data and addresses are no longer latched.

Figure 11.2 on page 33 illustrates the algorithm for the erase operation. See Erase/Program Operations on page 50 for parameters, and to Figure 18.2 on page 51 for timing diagrams.

11.8 Sector Erase Command Sequence

Sector erase is a six bus cycle operation. The sector erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the address of the sector to be erased, and the sector erase command. Table 13 on page 35 shows the address and data requirements for the sector erase command sequence.

The device does *not* require the system to preprogram the memory prior to erase. The Embedded Erase algorithm automatically programs and verifies the sector for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations.

After the command sequence is written, a sector erase time-out of 50 µs begins. During the time-out period, additional sector addresses and sector erase commands may be written. Loading the sector erase buffer may be done in any sequence, and the number of sectors may be from one sector to all sectors. The time between these additional cycles must be less than 50 µs, otherwise the last address and command might not be accepted, and erasure may begin. It is recommended that processor interrupts be disabled during this time to ensure all commands are accepted. The interrupts can be re-enabled after the last Sector Erase command is written. If the time between additional sector erase commands can be assumed to be less than 50 µs, the system need not monitor DQ3. **Any command other than Sector Erase or Erase Suspend during the time-out period resets the device to reading array data.** The system must rewrite the command sequence and any additional sector addresses and commands.

The system can monitor DQ3 to determine if the sector erase timer has timed out. (See the DQ3: Sector Erase Timer section.) The time-out begins from the rising edge of the final WE# pulse in the command sequence.

Once the sector erase operation has begun, only the Erase Suspend command is valid. All other commands are ignored. Note that a **hardware reset** during the sector erase operation immediately terminates the operation. The Sector Erase command sequence should be reinitiated once the device has returned to reading array data, to ensure data integrity.

When the Embedded Erase algorithm is complete, the device returns to reading array data and addresses are no longer latched. The system can determine the status of the erase operation by using DQ7, DQ6, DQ2, or RY/BY#. (Refer to Write Operation Status for information on these status bits.)

Figure 11.2 on page 33 illustrates the algorithm for the erase operation. Refer to Erase/Program Operations on page 50 for parameters, and to Figure 18.2 on page 51 for timing diagrams.

Not Recommended for New Design

11.9 Erase Suspend/Erase Resume Commands

The Erase Suspend command allows the system to interrupt a sector erase operation and then read data from, or program data to, any sector not selected for erasure. This command is valid only during the sector erase operation, including the 50-µs time-out period during the sector erase command sequence. The Erase Suspend command is ignored if it is written during the chip erase operation or Embedded Program algorithm. Writing the Erase Suspend command during the Sector Erase time-out immediately terminates the time-out period and suspends the erase operation. Addresses are don't cares when writing the Erase Suspend command.

When the Erase Suspend command is written during a sector erase operation, the device requires a maximum of 20 µs to suspend the erase operation. However, when the Erase Suspend command is written during the sector erase time-out, the device immediately terminates the time-out period and suspends the erase operation.

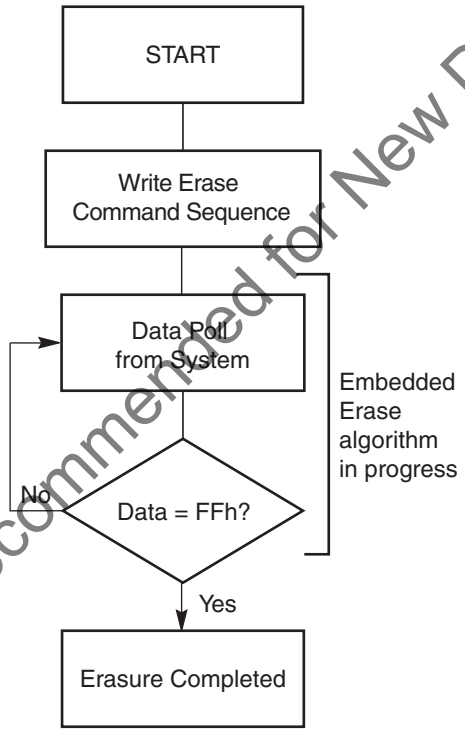
After the erase operation has been suspended, the system can read array data from or program data to any sector not selected for erasure. (The device *erase suspends* all sectors selected for erasure.) Normal read and write timings and command definitions apply. Reading at any address within erase-suspended sectors produces status data on DQ7–DQ0. The system can use DQ7, or DQ6 and DQ2 together, to determine if a sector is actively erasing or is erase-suspended. See Write Operation Status on page 37 for information on these status bits.

After an erase-suspended program operation is complete, the system can once again read array data within non-suspended sectors. The system can determine the status of the program operation using the DQ7 or DQ6 status bits, just as in the standard program operation. See Write Operation Status on page 37 for more information.

The system may also write the autoselect command sequence when the device is in the Erase Suspend mode. The device allows reading autoselect codes even at addresses within erasing sectors, since the codes are not stored in the memory array. When the device exits the autoselect mode, the device reverts to the Erase Suspend mode, and is ready for another valid operation. See Autoselect Command Sequence on page 30 for more information.

The system must write the Erase Resume command (address bits are *don't care*) to exit the erase suspend mode and continue the sector erase operation. Further writes of the Resume command are ignored. Another Erase Suspend command can be written after the device has resumed erasing.

Figure 11.2 Erase Operation



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Notes

1. *See Table 13 for erase command sequence.*
2. *See DQ3: Sector Erase Timer on page 41 for more information.*

11.10 Command Definitions Table

Table 12. S29AL032D Command Definitions — Model 00

Command Sequence (Note 1)		Cycles	Bus Cycles (Notes 2–3)											
			First		Second		Third		Fourth		Fifth		Sixth	
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read (Note 4)		1	RA	RD										
Reset (Note 7)		1	XXX	F0										
Autoselect (Note 6)	Manufacturer ID (Note 7)	4	XXX	AA	XXX	55	0XXXXX	90	0XXX00	01				
	Device ID (Note 7)	4	XXX	AA	XXX	55	0XXXXX	90	0XXX01	A3				
	Secured Silicon Sector Factory Protect (Note 14)	4	AAA	AA	555	55	AAA	90	X06	85/05				
	Sector Protect Verify (Note 8)	4	XXX	AA	XXX	55	0XXXXX or 2XXXXX	90	SA X02	00				
			XXX		XXX					01				
Enter Secured Silicon Sector Region		3	XXX	AA	XXX	55	XXX	88	XXX					
Exit Secured Silicon Sector Region		4	XXX	AA	XXX	55	XXX	90	XXX	00				
Byte Program		4	XXX	AA	XXX	55	XXX	A0	PA	PD				
Unlock Bypass		3	XXX	AA	XXX	55	XXX	20						
Unlock Bypass Program (Note 9)		2	XXX	A0	PA	PD								
Unlock Bypass Reset (Note 10)		2	XXX	90	XXX	00								
Chip Erase		6	XXX	AA	XXX	55	XXX	80	XXX	AA	XXX	55	XXX	10
Sector Erase		6	XXX	AA	XXX	55	XXX	80	XXX	AA	XXX	55	SA	30
Erase Suspend (Note 11)		1	XXX	B0										
Erase Resume (Note 12)		1	XXX	30										
CFI Query (Note 13)		1	XXX	98										

Legend

X = Don't care

RA = Address of the memory location to be read

RD = Data read from location RA during read operation

PA = Address of the memory location to be programmed. Addresses are latched on the falling edge of the WE# or CE# pulse, whichever happens later.

PD = Data to be programmed at location PA. Data is latched on the rising edge of WE# or CE# pulse, whichever happens first.

SA = Address of the sector to be erased or verified. Address bits A21–A16 uniquely select any sector.

Notes

1. *See Table 8 on page 10 for descriptions of bus operations.*
2. *All values are in hexadecimal. Except when reading array or autoselect data, all bus cycles are write operations.*
3. *Address bits are don't care for unlock and command cycles, except when PA or SA is required.*
4. *No unlock or command cycles required when device is in read mode.*
5. *The Reset command is required to return to the read mode when the device is in the autoselect mode or if DQ5 goes high.*
6. *The fourth cycle of the autoselect command sequence is a read cycle.*
7. *In the third and fourth cycles of the command sequence, set A21 to 0.*
8. *In the third cycle of the command sequence, address bit A21 must be set to 0 if verifying sectors 0–31, or to 1 if verifying sectors 32–64. The data in the fourth cycle is 00h for an unprotected sector/sector block and 01h for a protected sector/sector block.*
9. *The Unlock Bypass command is required prior to the Unlock Bypass Program command.*
10. *The Unlock Bypass Reset command is required to return to reading array data when the device is in the Unlock Bypass mode.*
11. *The system may read and program functions in non-erasing sectors, or enter the autoselect mode, when in the Erase Suspend mode. The Erase Suspend command is valid only during a sector erase operation.*
12. *The Erase Resume command is valid only during the Erase Suspend mode.*
13. *Command is valid when device is ready to read array data or when device is in autoselect mode.*
14. *The data is 85h for factory locked and 05h for not factory locked.*

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Table 13. S29AL032D Command Definitions, x8 Mode — Models 03, 04

Command Sequence (Note 1)		Cycles	Bus Cycles (Notes 2–5)											
			First		Second		Third		Fourth		Fifth		Sixth	
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read (Note 6)		1	RA	RD										
Reset (Note 7)		1	XXX	F0										
Autoselect (Note 8)	Manufacturer ID	4	AAA	AA	555	55	AAA	90	X00	01				
	Device ID, Model 03	4	AAA	AA	555	55	AAA	90	X02	22F6				
	Device ID, Model 04	4	AAA	AA	555	55	AAA	90	X02	F9				
	Secured Silicon Sector Factory Protect, Model 03 (Note 9)	4	AAA	AA	555	55	AAA	90	X06	8D/1D				
	Secured Silicon Sector Factory Protect, Model 04 (Note 9)	4	AAA	AA	555	55	AAA	90	X06	9D/0D				
	Sector Protect Verify (Note 10)	4	AAA	AA	555	55	AAA	90	(SA)X04	(Note 10)				
Enter Secured Silicon Sector Region		3	AAA	AA	555	55	AAA	88						
Exit Secured Silicon Sector Region		4	AAA	AA	555	55	AAA	90	XXX	00				
CFI Query (Note 11)		1	AA	98										
Program		4	AAA	AA	555	55	AAA	A0	PA	PD				
Unlock Bypass		3	AAA	AA	555	55	AAA	20						
Unlock Bypass Program (Note 12)		2	XXX	A0	PA	PD								
Unlock Bypass Reset (Note 13)		2	XXX	90	XXX	00								
Chip Erase		6	AAA	AA	555	55	AAA	80	AAA	AA	555	55	AAA	10
Sector Erase		6	AAA	AA	555	55	AAA	80	AAA	AA	555	55	SA	30
Erase Suspend (Note 14)		1	XXX	B0										
Erase Resume (Note 15)		1	XXX	30										

Legend

X = Don't care

RA = Address of the memory location to be read

RD = Data read from location RA during read operation

PA = Address of the memory location to be programmed. Addresses are latched on the falling edge of the WE# or CE# pulse, whichever happens later.

PD = Data to be programmed at location PA. Data is latched on the rising edge of WE# or CE# pulse, whichever happens first.

SA = Address of the sector to be erased or verified. Address bits A19–A12 uniquely select any sector.

Notes

1. *See Table 8 on page 10 for description of bus operations.*
2. *All values are in hexadecimal.*
3. *Except for the read cycle and the fourth cycle of the autoselect command sequence, all bus cycles are write cycles.*
4. *Data bits DQ15–DQ8 are don't cares for unlock and command cycles.*
5. *Address bits A19–A11 are don't cares for unlock and command cycles, unless SA or PA required.*
6. *No unlock or command cycles required when reading array data.*
7. *The Reset command is required to return to reading array data when device is in the autoselect mode, or if DQ5 goes high (while the device is providing status data).*
8. *The fourth cycle of the autoselect command sequence is a read cycle.*
9. *For Model 03, the data is 8Dh for factory locked and 0Dh for not factory locked. For Model 04, the data is 9Dh for factory locked and 1Dh for not factory locked.*
10. *The data is 00h for an unprotected sector and 01h for a protected sector. See "Autoselect Command Sequence"for more information.*
11. *Command is valid when device is ready to read array data or when device is in autoselect mode.*
12. *The Unlock Bypass command is required prior to the Unlock Bypass Program command.*
13. *The Unlock Bypass Reset command is required to return to reading array data when the device is in the unlock bypass mode. F0h is also acceptable.*
14. *The system may read and program in non-erasing sectors, or enter the autoselect mode, when in the Erase Suspend mode. The Erase Suspend command is valid only during a sector erase operation.*
15. *The Erase Resume command is valid only during the Erase Suspend mode.*

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Table 14. S29AL032D Command Definitions, x16 Mode — Models 03, 04

Command Sequence (Note 1)		Cycles	Bus Cycles (Notes 2–5)											
			First		Second		Third		Fourth		Fifth		Sixth	
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read (Note 6)		1	RA	RD										
Reset (Note 7)		1	XXX	F0										
Autoselect (Note 8)	Manufacturer ID	4	555	AA	2AA	55	555	90	X00	01				
	Device ID, Model 03	4	555	AA	2AA	55	555	90	X01	22F6				
	Device ID, Model 04	4	555	AA	2AA	55	555	90	X01	22F9				
	Secured Silicon Sector Factory Protect, Model 03 (Note 9)	4	555	AA	2AA	55	555	90	X03	8D/0D				
	Secured Silicon Sector Factory Protect, Model 04 (Note 9)	4	555	AA	2AA	55	555	90	X03	9D/1D				
	Sector Protect Verify (Note 10)	4	555	AA	2AA	55	555	90	(SA)X02	(Note 10)				
Enter Secured Silicon Sector Region		3	555	AA	2AA	55	555	88						
Exit Secured Silicon Sector Region		4	555	AA	2AA	55	555	90	XXX	00				
CFI Query (Note 11)		1	55	98										
Program		4	555	AA	2AA	55	555	A0	PA	PD				
Unlock Bypass		3	555	AA	2AA	55	555	20						
Unlock Bypass Program (Note 12)		2	XXX	A0	PA	PD								
Unlock Bypass Reset (Note 13)		2	XXX	90	XXX	00								
Chip Erase		6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10
Sector Erase		6	555	AA	2AA	55	555	80	555	AA	2AA	55	SA	30
Erase Suspend (Note 14)		1	XXX	B0										
Erase Resume (Note 15)		1	XXX	30										

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Legend

X = Don't care

RA = Address of the memory location to be read

RD = Data read from location RA during read operation

PA = Address of the memory location to be programmed. Addresses are latched on the falling edge of the WE# or CE# pulse, whichever happens later.

PD = Data to be programmed at location PA. Data is latched on the rising edge of WE# or CE# pulse, whichever happens first.

SA = Address of the sector to be erased or verified. Address bits A19–A12 uniquely select any sector.

Notes

1. *See Table 8 on page 10 for description of bus operations.*
2. *All values are in hexadecimal.*
3. *Except for the read cycle and the fourth cycle of the autoselect command sequence, all bus cycles are write cycles.*
4. *Data bits DQ15–DQ8 are don't cares for unlock and command cycles.*
5. *Address bits A19–A11 are don't cares for unlock and command cycles, unless SA or PA required.*
6. *No unlock or command cycles required when reading array data.*
7. *The Reset command is required to return to reading array data when device is in the autoselect mode, or if DQ5 goes high (while the device is providing status data).*
8. *The fourth cycle of the autoselect command sequence is a read cycle.*
9. *For Model 03, the data is 8Dh for factory locked and 0Dh for not factory locked. For Model 04, the data is 9Dh for factory locked and 1Dh for not factory locked.*
10. *The data is 00h for an unprotected sector and 01h for a protected sector. See "Autoselect Command Sequence"for more information.*
11. *Command is valid when device is ready to read array data or when device is in autoselect mode.*
12. *The Unlock Bypass command is required prior to the Unlock Bypass Program command.*
13. *The Unlock Bypass Reset command is required to return to reading array data when the device is in the unlock bypass mode. F0 is also acceptable.*
14. *The system may read and program in non-erasing sectors, or enter the autoselect mode, when in the Erase Suspend mode. The Erase Suspend command is valid only during a sector erase operation.*
15. *The Erase Resume command is valid only during the Erase Suspend mode.*

12. Write Operation Status

The device provides several bits to determine the status of a write operation: DQ2, DQ3, DQ5, DQ6, DQ7, and RY/BY#. Table 13 on page 41 and the following subsections describe the functions of these bits. DQ7, RY/BY#, and DQ6 each offer a method for determining whether a program or erase operation is complete or in progress. These three bits are discussed first.

12.1 DQ7: Data# Polling

The Data# Polling bit, DQ7, indicates to the host system whether an Embedded Algorithm is in progress or completed, or whether the device is in Erase Suspend. Data# Polling is valid after the rising edge of the final WE# pulse in the program or erase command sequence.

During the Embedded Program algorithm, the device outputs on DQ7 the complement of the datum programmed to DQ7. This DQ7 status also applies to programming during Erase Suspend. When the Embedded Program algorithm is complete, the device outputs the datum programmed to DQ7. The system must provide the program address to read valid status information on DQ7. If a program address falls within a protected sector, Data# Polling on DQ7 is active for approximately 1 µs, then the device returns to reading array data.

During the Embedded Erase algorithm, Data# Polling produces a *0* on DQ7. When the Embedded Erase algorithm is complete, or if the device enters the Erase Suspend mode, Data# Polling produces a *1* on DQ7. This is analogous to the complement/true datum output described for the Embedded Program algorithm: the erase function changes all the bits in a sector to *1*; prior to this, the device outputs the *complement*, or *0.* The system must provide an address within any of the sectors selected for erasure to read valid status information on DQ7.

After an erase command sequence is written, if all sectors selected for erasing are protected, Data# Polling on DQ7 is active for approximately 100 µs, then the device returns to reading array data. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

When the system detects DQ7 has changed from the complement to true data, it can read valid data at DQ7–DQ0 on the *following* read cycles. This is because DQ7 may change asynchronously with DQ0–DQ6 while Output Enable (OE#) is asserted low. Figure 18.4 on page 52, Data# Polling Timings (During Embedded Algorithms), under AC Characteristics on page 47 illustrates this.

Figure 13 on page 41 shows the outputs for Data# Polling on DQ7. Figure 12.2 on page 40 shows the Data# Polling algorithm.

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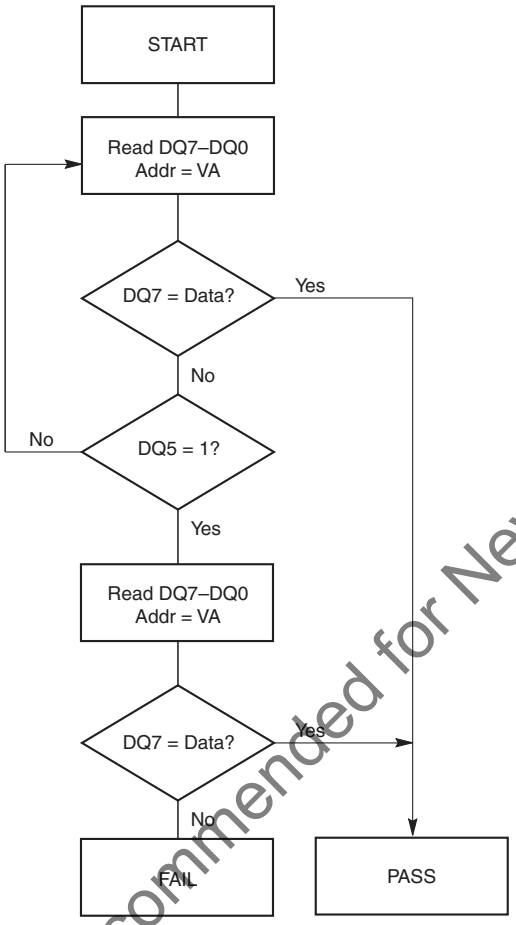
Figure 12.1 Data# Polling Algorithm



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Notes

1. *VA = Valid address for programming. During a sector erase operation, a valid address is an address within any sector selected for erasure. During chip erase, a valid address is any non-protected sector address.*
2. *DQ7 should be rechecked even if DQ5 = 1 because DQ7 may change simultaneously with DQ5.*

12.2 RY/BY#: Ready/Busy#

The RY/BY# is a dedicated, open-drain output pin that indicates whether an Embedded Algorithm is in progress or complete. The RY/BY# status is valid after the rising edge of the final WE# pulse in the command sequence. Since RY/BY# is an open-drain output, several RY/BY# pins can be tied together in parallel with a pull-up resistor to V_{CC}.

If the output is low (Busy), the device is actively erasing or programming. (This includes programming in the Erase Suspend mode.) If the output is high (Ready), the device is ready to read array data (including during the Erase Suspend mode), or is in the standby mode.

Table 13 on page 41 shows the outputs for RY/BY#. Figures Figure 17.1 on page 47, Figure 17.2 on page 48, Figure 18.1 on page 50 and Figure 18.2 on page 51 shows RY/BY# for read, reset, program, and erase operations, respectively.

12.3 DQ6: Toggle Bit I

Toggle Bit I on DQ6 indicates whether an Embedded Program or Erase algorithm is in progress or complete, or whether the device has entered the Erase Suspend mode. Toggle Bit I may be read at any address, and is valid after the rising edge of the final WE# pulse in the command sequence (prior to the program or erase operation), and during the sector erase time-out.

During an Embedded Program or Erase algorithm operation, successive read cycles to any address cause DQ6 to toggle. (The system may use either OE# or CE# to control the read cycles.) When the operation is complete, DQ6 stops toggling.

After an erase command sequence is written, if all sectors selected for erasing are protected, DQ6 toggles for approximately 100 µs, then returns to reading array data. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

The system can use DQ6 and DQ2 together to determine whether a sector is actively erasing or is erase-suspended. When the device is actively erasing (that is, the Embedded Erase algorithm is in progress), DQ6 toggles. When the device enters the Erase Suspend mode, DQ6 stops toggling. However, the system must also use DQ2 to determine which sectors are erasing or erase-suspended. Alternatively, the system can use DQ7 (see the subsection on DQ7: Data# Polling on page 37).

If a program address falls within a protected sector, DQ6 toggles for approximately 1 µs after the program command sequence is written, then returns to reading array data.

DQ6 also toggles during the erase-suspend-program mode, and stops toggling once the Embedded Program algorithm is complete.

Table 13 on page 41 shows the outputs for Toggle Bit I on DQ6. Figure 12.2 on page 40 shows the toggle bit algorithm in flowchart form, and the section Reading Toggle Bits DQ6/DQ2 on page 39 explains the algorithm. Figure 18.5 on page 53 shows the toggle bit timing diagrams. Figure 18.6 on page 53 shows the differences between DQ2 and DQ6 in graphical form. See also the subsection on DQ2: Toggle Bit II.

12.4 DQ2: Toggle Bit II

The *Toggle Bit II* on DQ2, when used with DQ6, indicates whether a particular sector is actively erasing (that is, the Embedded Erase algorithm is in progress), or whether that sector is erase-suspended. Toggle Bit II is valid after the rising edge of the final WE# pulse in the command sequence.

DQ2 toggles when the system reads at addresses within those sectors that have been selected for erasure. (The system may use either OE# or CE# to control the read cycles.) But DQ2 cannot distinguish whether the sector is actively erasing or is erase-suspended. DQ6, by comparison, indicates whether the device is actively erasing, or is in Erase Suspend, but cannot distinguish which sectors are selected for erasure. Thus, both status bits are required for sector and mode information. Refer to Table 13 on page 41 to compare outputs for DQ2 and DQ6.

Figure 12.2 on page 40 shows the toggle bit algorithm in flowchart form, and the section Reading Toggle Bits DQ6/DQ2 on page 39 explains the algorithm. See also the DQ6: Toggle Bit I subsection. Figure 18.5 on page 53 shows the toggle bit timing diagram. Figure 18.6 on page 53 shows the differences between DQ2 and DQ6 in graphical form.

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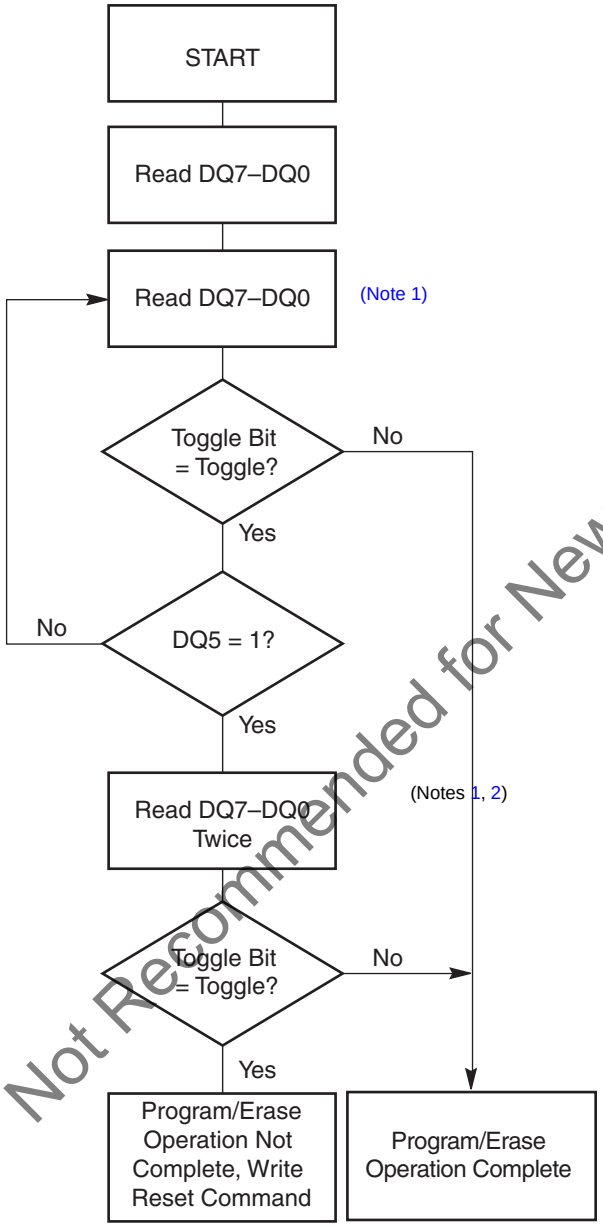
12.5 Reading Toggle Bits DQ6/DQ2

Refer to Figure 12.2 on page 40 for the following discussion. Whenever the system initially begins reading toggle bit status, it must read DQ7–DQ0 at least twice in a row to determine whether a toggle bit is toggling. Typically, the system would note and store the value of the toggle bit after the first read. After the second read, the system would compare the new value of the toggle bit with the first. If the toggle bit is not toggling, the device has completed the program or erase operation. The system can read array data on DQ7–DQ0 on the following read cycle.

However, if after the initial two read cycles, the system determines that the toggle bit is still toggling, the system also should note whether the value of DQ5 is high (see the section on DQ5). If it is, the system should then determine again whether the toggle bit is toggling, since the toggle bit may have stopped toggling just as DQ5 went high. If the toggle bit is no longer toggling, then the device has successfully completed the program or erase operation. If it is still toggling, then the device had not complete the operation successfully, and the system must write the reset command in order to return to reading array data.

The remaining scenario is that the system initially determines that the toggle bit is toggling and DQ5 has not gone high. The system may continue to monitor the toggle bit and DQ5 through successive read cycles, determining the status as described in the previous paragraph. Alternatively, it may choose to perform other system tasks. In this case, the system must start at the beginning of the algorithm when it returns to determine the status of the operation (top of Figure 12.2 on page 40).

Figure 12.2 Toggle Bit Algorithm



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Notes

1. *Read toggle bit twice to determine whether or not it is toggling. See text.*
2. *Recheck toggle bit because it may stop toggling as DQ5 changes to* 1*. See text.*

12.6 DQ5: Exceeded Timing Limits

DQ5 indicates whether the program or erase time has exceeded a specified internal pulse count limit. Under these conditions DQ5 produces a *1*. This is a failure condition that indicates the program or erase cycle was not successfully completed.

The DQ5 failure condition may appear if the system tries to program a *1* to a location that is previously programmed to *0.* **Only an erase operation can change a *0* back to a *1*.** Under this condition, the device halts the operation, and when the operation has exceeded the timing limits, DQ5 produces a *1*.

Under both these conditions, the system must issue the reset command to return the device to reading array data.

12.7 DQ3: Sector Erase Timer

After writing a sector erase command sequence, the system may read DQ3 to determine whether or not an erase operation has begun. (The sector erase timer does not apply to the chip erase command.) If additional sectors are selected for erasure, the entire time-out also applies after each additional sector erase command. When the time-out is complete, DQ3 switches from *0* to *1.* The system may ignore DQ3 if the system can guarantee that the time between additional sector erase commands will always be less than 50 μs. See also Sector Erase Command Sequence on page 32.

After the sector erase command sequence is written, the system should read the status on DQ7 (Data# Polling) or DQ6 (Toggle Bit I) to ensure that the device accepts the command sequence, and then read DQ3. If DQ3 is *1*, the internally controlled erase cycle has begun; all further commands (other than Erase Suspend) are ignored until the erase operation is complete. If DQ3 is *0*, the device accepts additional sector erase commands. To ensure that the command has been accepted, the system software should check the status of DQ3 prior to and following each subsequent sector erase command. If DQ3 is high on the second status check, the last command might not have been accepted. Table 13 shows the outputs for DQ3.

Table 13. Write Operation Status

Operation		DQ7 (Note 2)	DQ6	DQ5 (Note 1)	DQ3	DQ2 (Note 2)	RY/BY#
Standard Mode	Embedded Program Algorithm	DQ7#	Toggle	0	N/A	No toggle	0
	Embedded Erase Algorithm	0	Toggle	0	1	Toggle	0
Erase Suspend Mode	Reading within Erase Suspended Sector	1	No toggle	0	N/A	Toggle	1
	Reading within Non-Erase Suspended Sector	Data	Data	Data	Data	Data	1
	Erase-Suspend-Program	DQ7#	Toggle	0	N/A	N/A	0

Notes

1. *DQ5 switches to '1' when an Embedded Program or Embedded Erase operation exceeds the maximum timing limits. See DQ5: Exceeded Timing Limits on page 40 for more information.*
2. *DQ7 and DQ2 require a valid address when reading status information. Refer to the appropriate subsection for further details.*

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13. Absolute Maximum Ratings

Table 14. Absolute Maximum Ratings

Parameter		Rating
Storage Temperature, Plastic Packages		–65°C to +150°C
Ambient Temperature with Power Applied		–65°C to +125°C
Voltage with Respect to Ground	V_{CC} (Note 1)	–0.5 V to +4.0 V
	A9, OE#, and RESET# (Note 2)	–0.5 V to +12.5 V
	All other pins (Note 1)	–0.5 V to V_{CC}+0.5 V
Output Short Circuit Current (Note 3)		200 mA

Notes

1. *Minimum DC voltage on input or I/O pins is –0.5 V. During voltage transitions, input or I/O pins may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. See Figure 14.1 on page 42. Maximum DC voltage on input or I/O pins is V_{CC} +0.5 V. During voltage transitions, input or I/O pins may overshoot to V_{CC} +2.0 V for periods up to 20 ns. See Figure 14.2 on page 42.*
2. *Minimum DC input voltage on pins A9, OE#, and RESET# is -0.5 V. During voltage transitions, A9, OE#, and RESET# may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. See Figure 14.1 on page 42. Maximum DC input voltage on pin A9 is +12.5 V which may overshoot to 14.0 V for periods up to 20 ns.*
3. *No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.*
4. *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.*

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Figure 14.1 Maximum Negative Overshoot Waveform

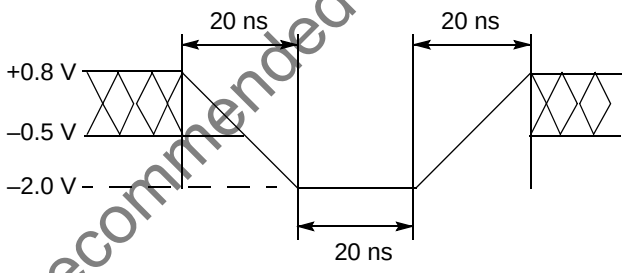
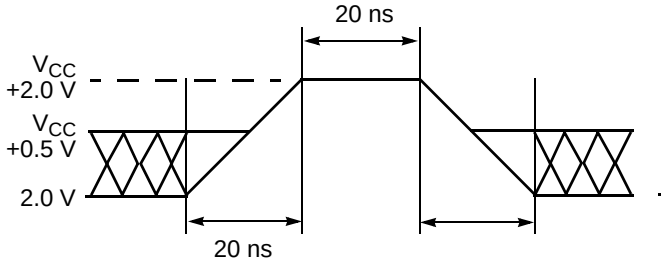


Figure 14.2 Maximum Positive Overshoot Waveform



14. Operating Ranges

Table 15. Operating Ranges

Parameter		Range
Ambient Temperature (T_A)	Industrial (I) Devices	–40°C to +85°C
	Extended (N) Devices	–40°C to +125°C
V_{CC} Supply Voltages	V_{CC} for standard voltage range	2.7 V to 3.6 V

Note
Operating ranges define those limits between which the functionality of the device is guaranteed.

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15. DC Characteristics

Table 16. DC Characteristics, CMOS Compatible

Parameter	Description	Test Conditions		Min	Typ	Max	Unit
I_{LI}	Input Load Current (Note 1)	$V_{IN} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC\ max}$				±1.0	µA
I_{LIT}	A9 Input Load Current	$V_{CC} = V_{CC\ max}$; A9 = 12.5 V				35	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC\ max}$				±1.0	µA
I_{CC1}	V_{CC} Active Read Current (Notes 2, 3)	CE# = V_{IL}, OE# = V_{IH}, Byte Mode	10 MHz		15	30	mA
			5 MHz		9	16	
			1 MHz		2	4	
		CE# = V_{IL}, OE# = V_{IH}, Word Mode	10 MHz		18	35	
			5 MHz		9	16	
			1 MHz		2	4	
I_{CC2}	V_{CC} Active Write Current (Notes 3, 4, 6)	CE# = V_{IL}, OE# = V_{IH}			15	35	mA
I_{CC3}	V_{CC} Standby Current (Notes 3, 5)	CE#, RESET# = V_{CC}±0.3 V			0.2	5	µA
I_{CC4}	V_{CC} Standby Current During Reset (Notes 3, 5)	RESET# = V_{SS} ± 0.3 V			0.2	5	µA
I_{CC5}	Automatic Sleep Mode (Notes 3, 5, 7)	$V_{IH} = V_{CC}$ ± 0.3 V; $V_{IL} = V_{SS}$ ± 0.3 V			0.2	5	µA
I_{ACC}	ACC Accelerated Program Current, Word or Byte	CE# = V_{IL}, OE# = V_{IH}	ACC pin		5	10	mA
			V_{CC} pin		15	30	mA
V_{IL}	Input Low Voltage			–0.5		0.8	V
V_{IH}	Input High Voltage			0.7 x V_{CC}		V_{CC} + 0.3	V
V_{HH}	Voltage for WP#/ACC Sector Protect/ Unprotect and Program Acceleration	V_{CC} = 3.0 V ± 10%		11.5		12.5	V
V_{ID}	Voltage for Autoselect and Temporary Sector Unprotect	V_{CC} = 3.3 V		11.5		12.5	V
V_{OL}	Output Low Voltage	I_{OL} = 4.0 mA, $V_{CC} = V_{CC\ min}$				0.45	V
V_{OH1}	Output High Voltage	I_{OH} = -2.0 mA, $V_{CC} = V_{CC\ min}$		2.4			V
V_{OH2}		I_{OH} = -100 µA, $V_{CC} = V_{CC\ min}$		V_{CC}–0.4			V
V_{LKO}	Low V_{CC} Lock-Out Voltage (Note 4)			2.3		2.5	V

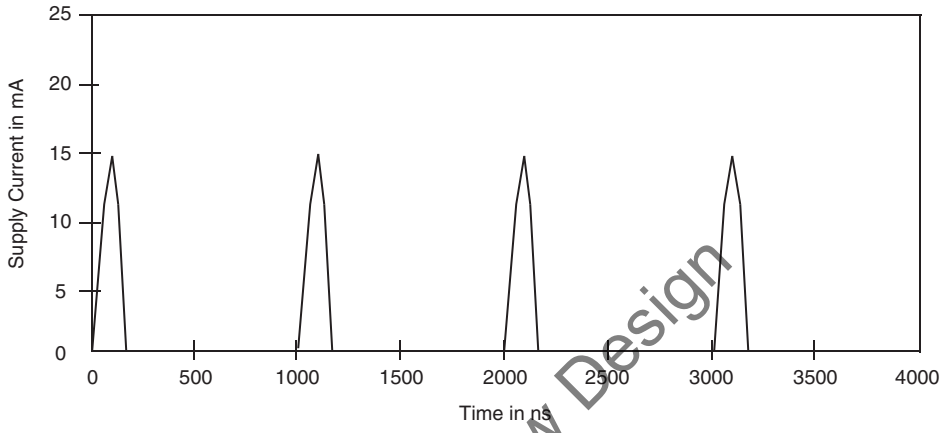
Not Recommended for New Design

Notes

1. *On the ACC pin only, the maximum input load current when ACC = V_{IL} is ±5.0 µA.*
2. *The I_{CC} current listed is typically less than 2 mA/MHz, with OE# at V_{IH}. Typical V_{CC} is 3.0 V.*
3. *Maximum I_{CC} specifications are tested with $V_{CC} = V_{CC}$max.*
4. *I_{CC} active while Embedded Erase or Embedded Program is in progress.*
5. *At extended temperature range (>+85°C), maximum current is 15 µA.*
6. *Automatic sleep mode enables the low power mode when addresses remain stable for t_{ACC} + 30 ns. Typical sleep mode current is 200 nA.*
7. *Not 100% tested.*

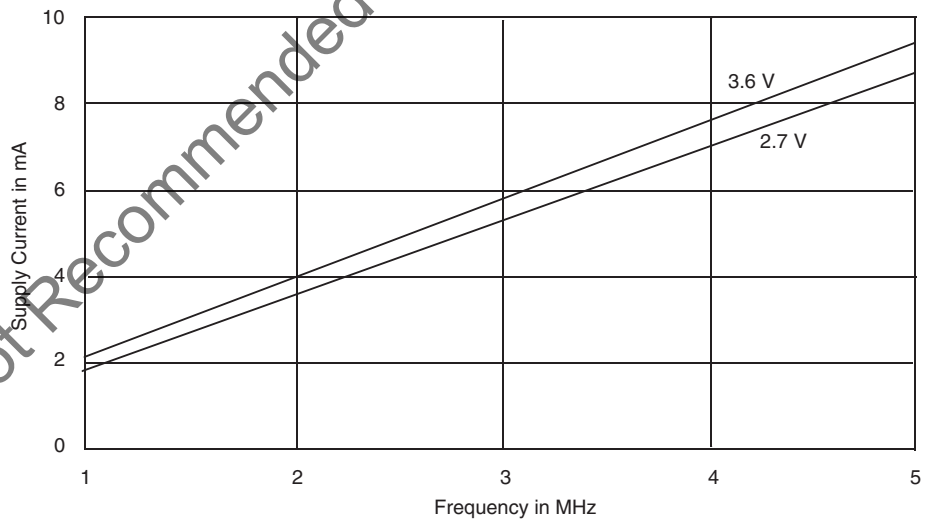
15.1 Zero Power Flash

Figure 15.1 I_{CC1} Current vs. Time (Showing Active and Automatic Sleep Currents)



Note
Addresses are switching at 1 MHz.

Figure 15.2 Typical I_{CC1} vs. Frequency

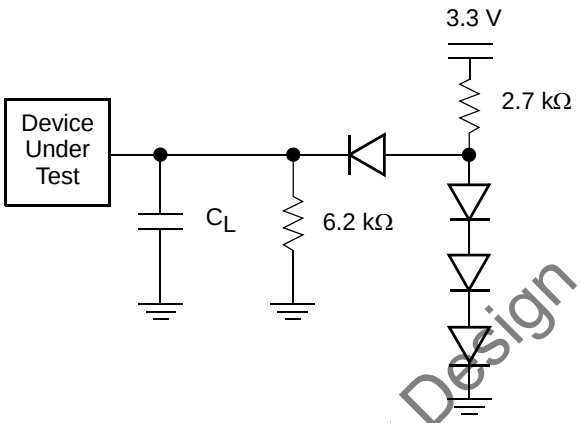


Note
T = 25°C

Not Recommended for New Design

16. Test Conditions

Figure 16.1 Test Setup

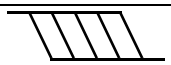
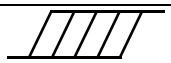
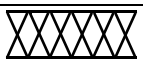
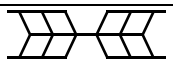


Note
Diodes are IN3064 or equivalent.

Table 17. Test Specifications

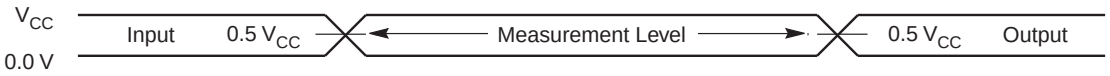
Speed Option	70	90	Unit
Output Load	1 TTL gate		
Output Load Capacitance, C_L (including jig capacitance)	30	100	pF
Input Rise and Fall Times	5		ns
Input Pulse Levels	0.0 or V_{CC}		V
Input timing measurement reference levels	0.5 V_{CC}		V
Output timing measurement reference levels	0.5 V_{CC}		V

16.1 Key to Switching Waveforms

Waveform	Inputs	Outputs
	Steady	
	Changing from H to L	
	Changing from L to H	
	Don’t Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High Impedance State (High Z)

Not Recommended for New Design

Figure 16.1 Input Waveforms and Measurement Levels



17. AC Characteristics

17.1 Read Operations

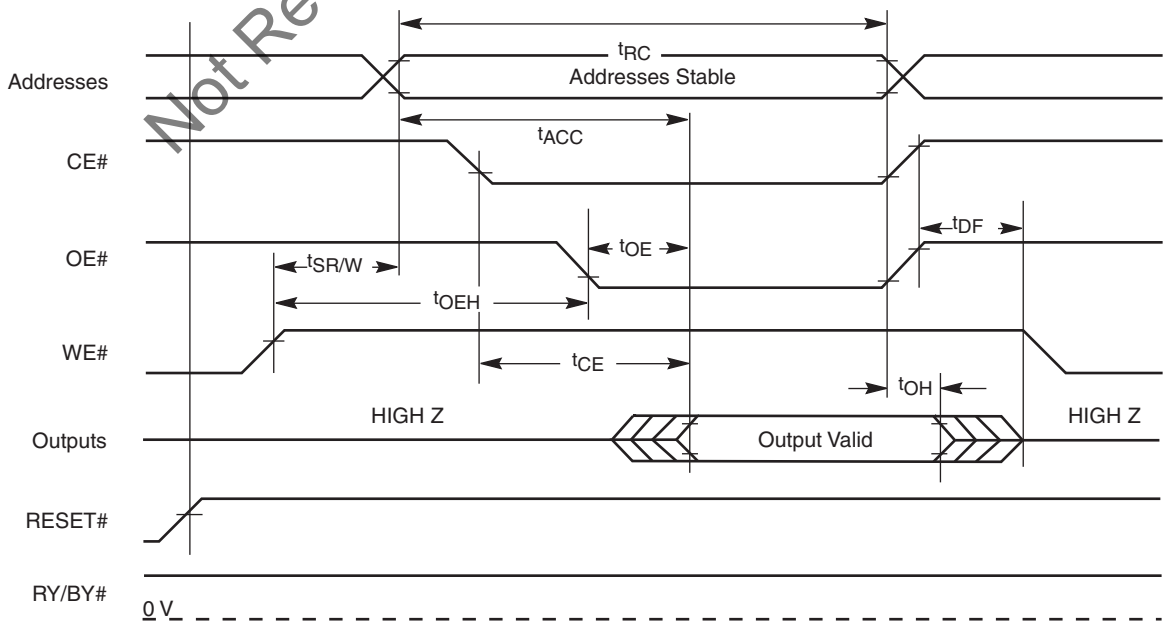
Parameter		Description		Test Setup		Speed Options		Unit
JEDEC	Std					70	90	
t_{AVAV}	t_{RC}	Read Cycle Time (Note 1)			Min	70	90	ns
t_{AVQV}	t_{ACC}	Address to Output Delay		CE# = V_{IL} OE# = V_{IL}	Max	70	90	ns
t_{ELQV}	t_{CE}	Chip Enable to Output Delay		OE# = V_{IL}	Max	70	90	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay			Max	30	35	ns
t_{EHQZ}	t_{DF}	Chip Enable to Output High Z (Note 1)			Max	16		ns
t_{GHQZ}	t_{DF}	Output Enable to Output High Z (Note 1)			Max	16		ns
	$t_{SR/W}$	Latency Between Read and Write Operations			Min	20		ns
	t_{OEH}	Output Enable Hold Time (Note 1)	Read		Min	0		ns
			Toggle and Data# Polling		Min	10		ns
t_{AXQX}	t_{OH}	Output Hold Time From Addresses, CE# or OE#, Whichever Occurs First (Note 1)			Min	0		ns

Notes

1. *Not 100% tested.*
2. *See Figure 16.1 on page 46 and Table 17 on page 46 for test specifications.*

Not Recommended for New Design

Figure 17.1 Read Operations Timings

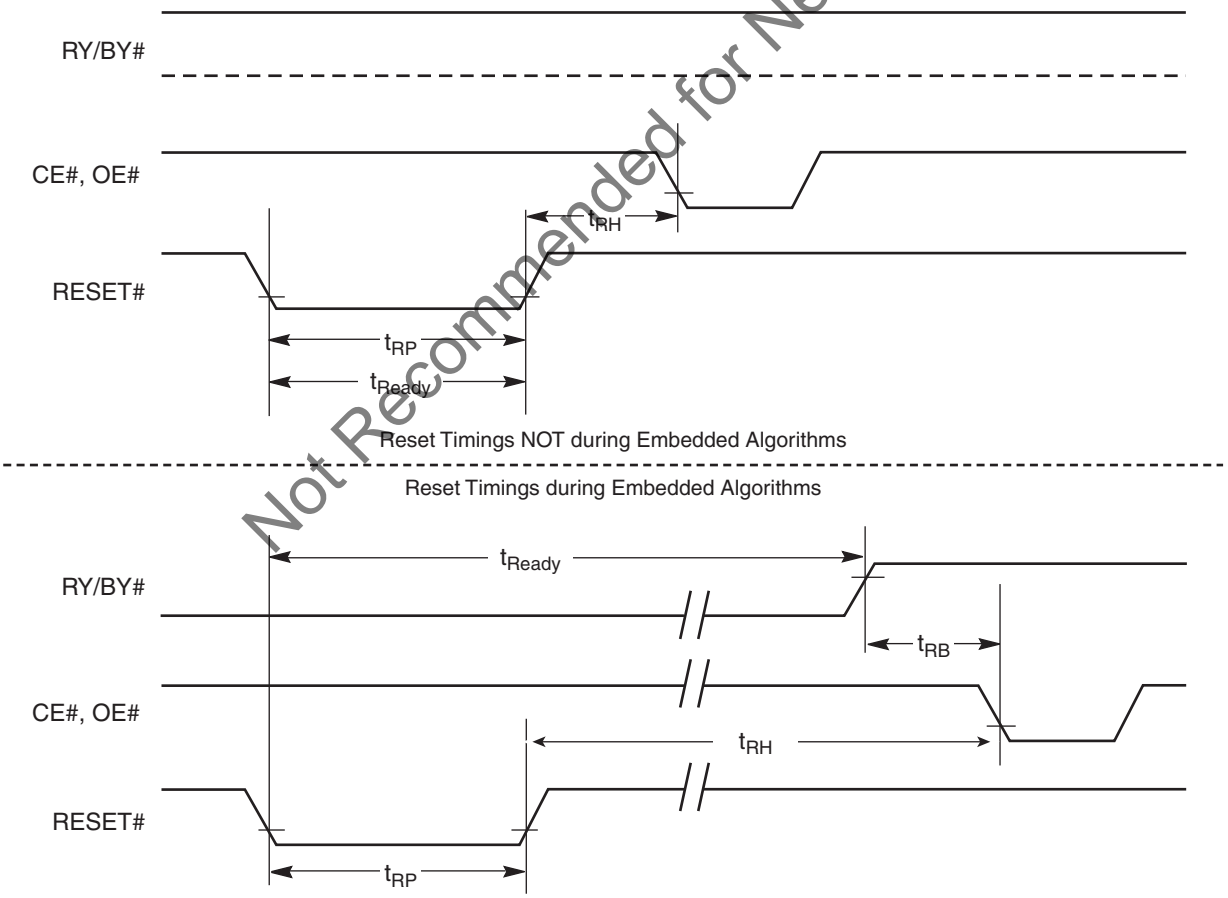


17.2 Hardware Reset (RESET#)

Parameter		Description	Test Setup		All Speed Options	Unit
JEDEC	Std.					
	t_{READY}	RESET# Pin Low (During Embedded Algorithms) to Read or Write (See Note)		Max	20	µs
	t_{READY}	RESET# Pin Low (NOT During Embedded Algorithms) to Read or Write (See Note)		Max	500	ns
	t_{RP}	RESET# Pulse Width		Min	500	ns
	t_{RH}	RESET# High Time Before Read (See Note)		Min	50	ns
	t_{RPD}	RESET# Low to Standby Mode		Min	20	µs
	t_{RB}	RY/BY# Recovery Time		Min	0	ns

Note
Not 100% tested.

Figure 17.2 RESET# Timings

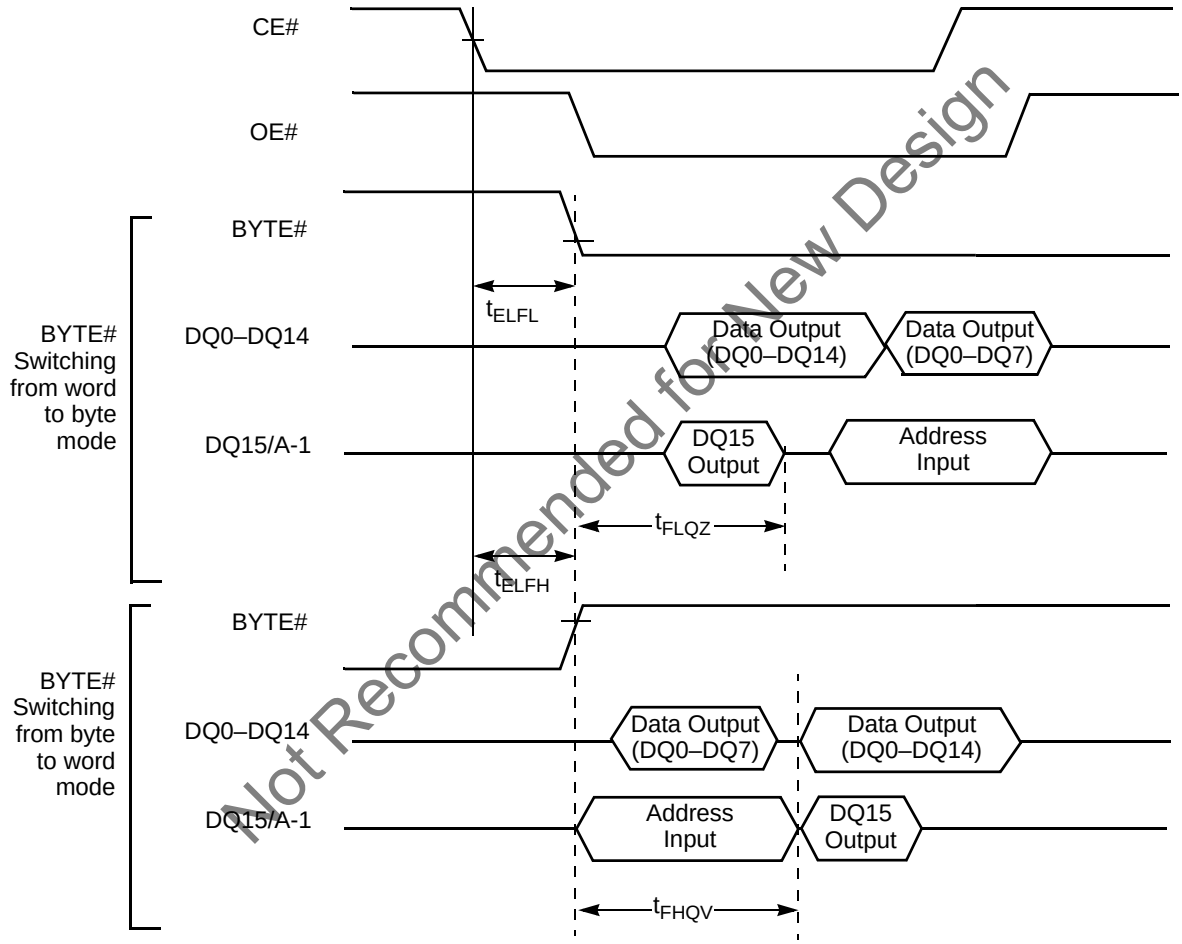


Not Recommended for New Design

17.3 Word/Byte Configuration (BYTE#) (Models 03, 04 Only)

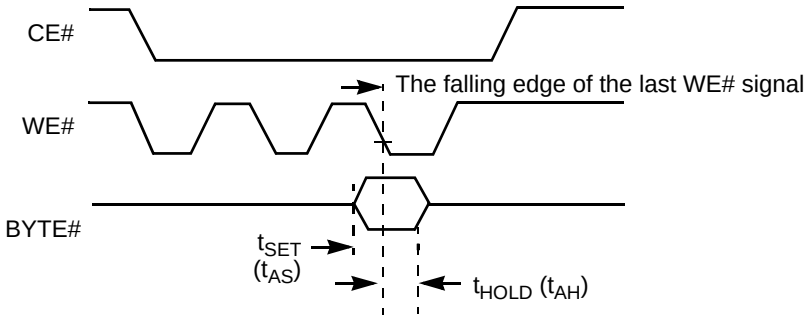
Parameter		Description		Speed Options		Unit
JEDEC	Std.			70	90	
	t_{ELFL}/t_{ELFH}	CE# to BYTE# Switching Low or High	Max	5		ns
	t_{FLQZ}	BYTE# Switching Low to Output HIGH Z	Max	16		ns
	t_{FHQV}	BYTE# Switching High to Output Active	Min	70	90	ns

Figure 17.3 BYTE# Timings for Read Operations



Not Recommended for New Design

Figure 17.4 BYTE# Timings for Write Operations



Note
Refer to the Erase/Program Operations table for t_{AS} and t_{AH} specifications.

17.4 Erase/Program Operations

Table 18. Erase/Program Operations

Parameter		Description			Speed Options		Unit
JEDEC	Std.				70	90	
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)		Min	70	90	ns
t_{AVWL}	t_{AS}	Address Setup Time		Min	0		ns
t_{WLAX}	t_{AH}	Address Hold Time		Min	45	45	ns
t_{DVWH}	t_{DS}	Data Setup Time		Min	35	45	ns
t_{WHDX}	t_{DH}	Data Hold Time		Min	0		ns
	t_{OES}	Output Enable Setup Time		Min	0		ns
t_{GHWL}	t_{GHWL}	Read Recovery Time Before Write (OE# High to WE# Low)		Min	0		ns
t_{ELWL}	t_{CS}	CE# Setup Time		Min	0		ns
t_{WHEH}	t_{CH}	CE# Hold Time		Min	0		ns
t_{WLWH}	t_{WP}	Write Pulse Width		Min	35	35	ns
t_{WHWL}	t_{WPH}	Write Pulse Width High		Min	30		ns
	$t_{SR/W}$	Latency Between Read and Write Operations		Min	20		ns
t_{WHWH1}	t_{WHWH1}	Programming Operation (Note 2)	Byte	Typ	9		µs
			Word	Typ	11		
t_{WHWH1}	t_{WHWH1}	Accelerated Programming Operation, Word or Byte (Note 2)		Typ	7		µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 2)		Typ	0.7		sec
	t_{VCS}	V_{CC} Setup Time (Note 1)		Min	50		µs
	t_{RB}	Recovery Time from RY/BY#		Min	0		ns
	t_{BUSY}	Program/Erase Valid to RY/BY# Delay		Max	90		ns

Notes
1. *Not 100% tested.*
2. *See Erase and Programming Performance on page 57 for more information.*

Not Recommended for New Design

Figure 18.1 Program Operation Timings

Notes
1. *PA = program address, PD = program data, D_{OUT} is the true data at the program address.*
2. *Illustration shows device in word mode.*

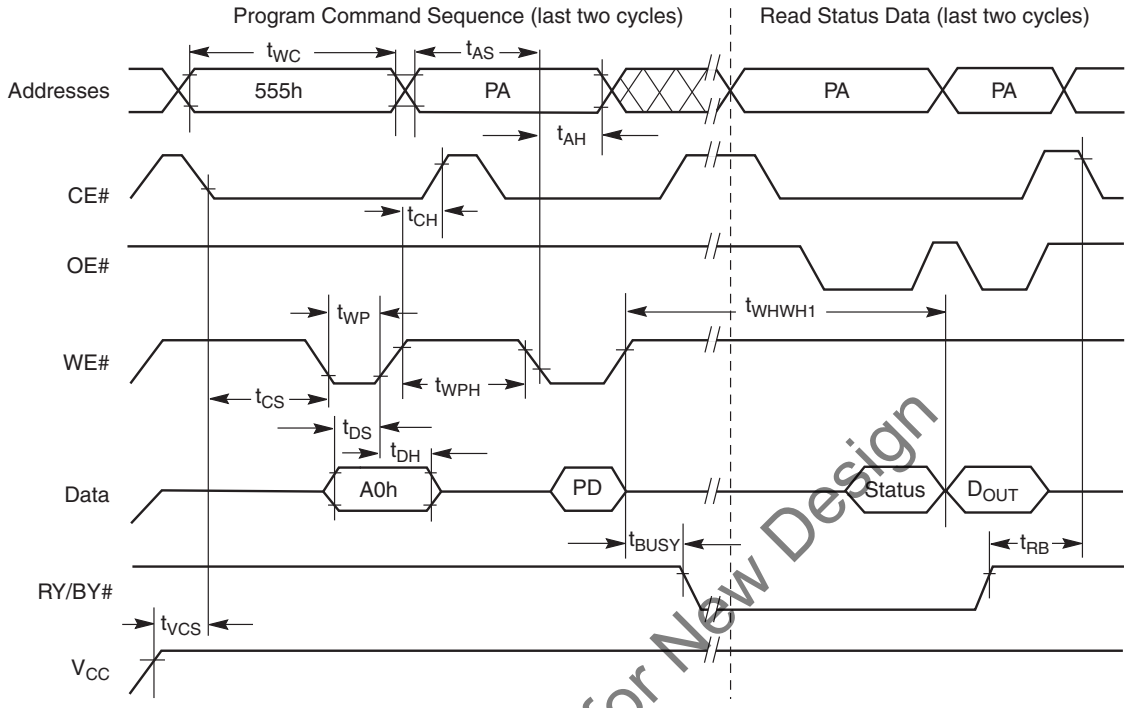
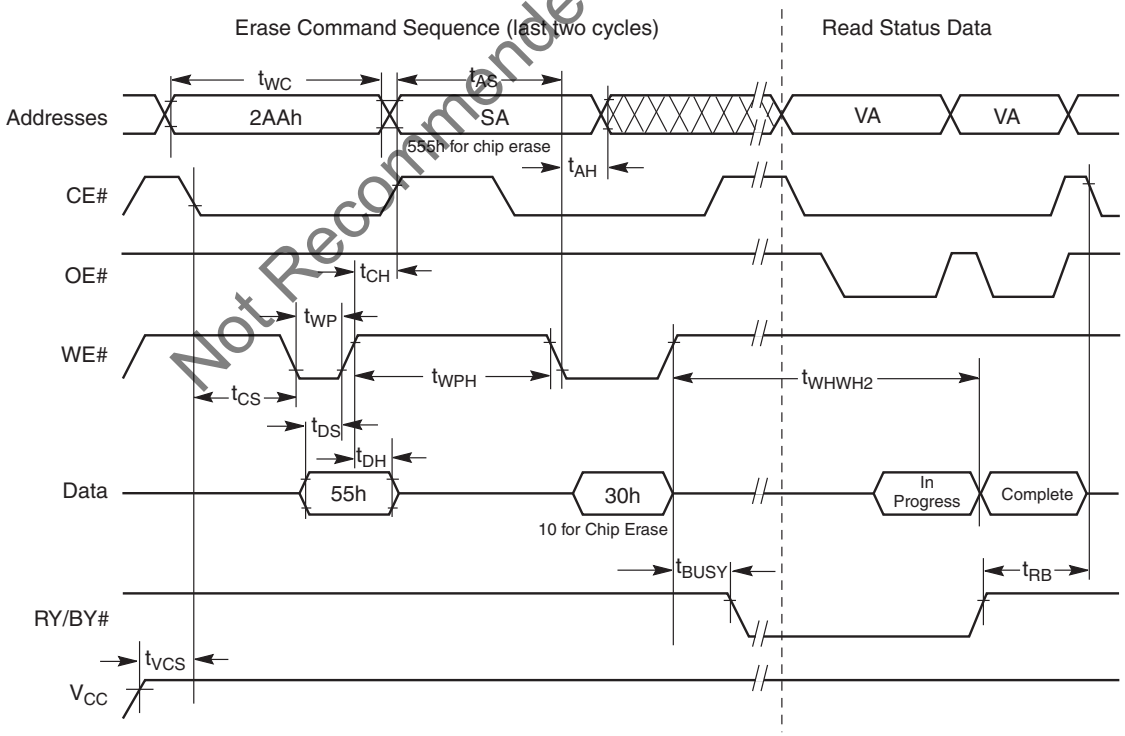


Figure 18.2 Chip/Sector Erase Operation Timings



Not Recommended for New Design

Notes

1. *SA = sector address (for Sector Erase), VA = Valid Address for reading status data (see Write Operation Status on page 37).*
2. *Illustration shows device in word mode.*

Figure 18.3 Back to Back Read/Write Cycle Timing

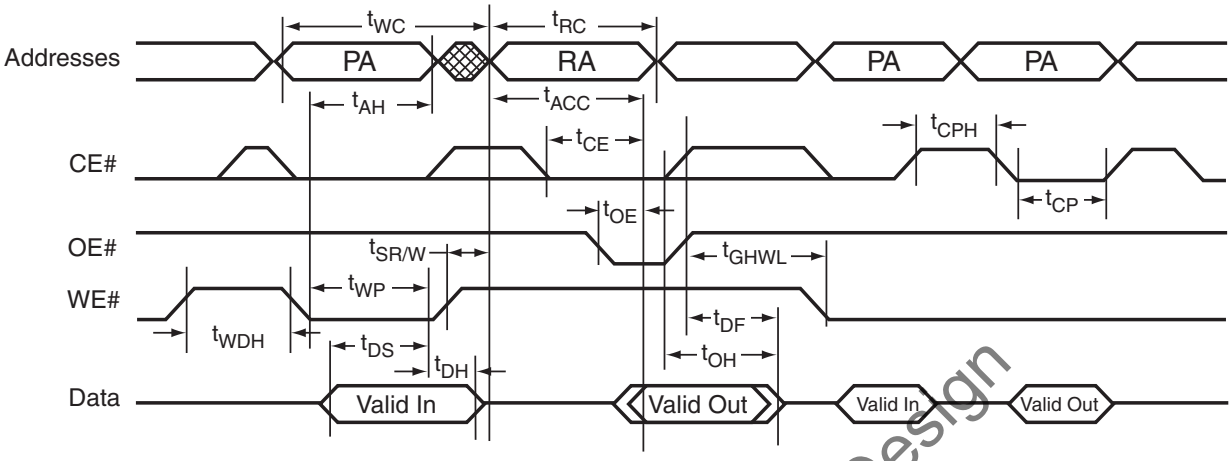
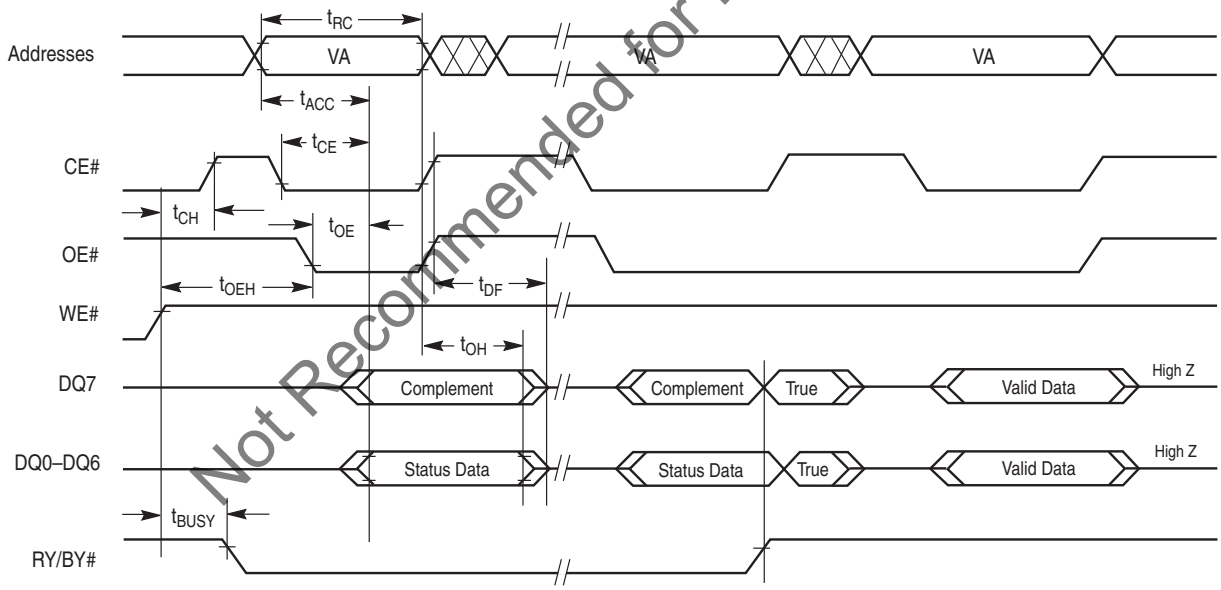


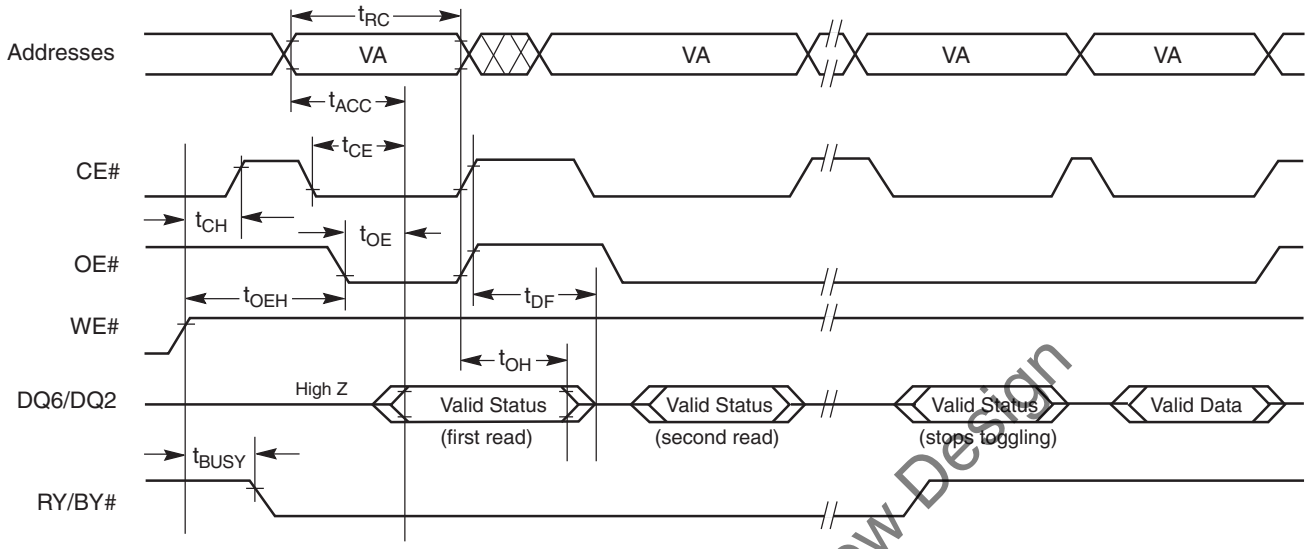
Figure 18.4 Data# Polling Timings (During Embedded Algorithms)



Not Recommended for New Design

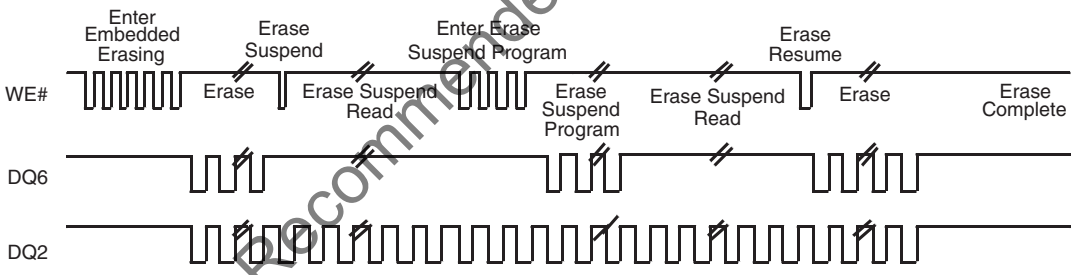
Note
VA = Valid address. Illustration shows first status cycle after command sequence, last status read cycle, and array data read cycle.

Figure 18.5 Toggle Bit Timings (During Embedded Algorithms)



Note
VA = Valid address; not required for DQ6. Illustration shows first two status cycle after command sequence, last status read cycle, and array data read cycle.

Figure 18.6 DQ2 vs. DQ6 for Erase and Erase Suspend Operations



Note
The system may use CE# or OE# to toggle DQ2 and DQ6. DQ2 toggles only when read at an address within an erase-suspended sector.

Not Recommended for New Design

17.5 Temporary Sector Unprotect

Table 18. Temporary Sector Unprotect

Parameter		Description		All Speed Options	Unit
JEDEC	Std.				
	t_{VIDR}	V_{ID} Rise and Fall Time (See Note)	Min	500	ns
	t_{RSP}	RESET# Setup Time for Temporary Sector Unprotect	Min	4	µs

Note
Not 100% tested.

Figure 18.1 Temporary Sector Unprotect Timing Diagram

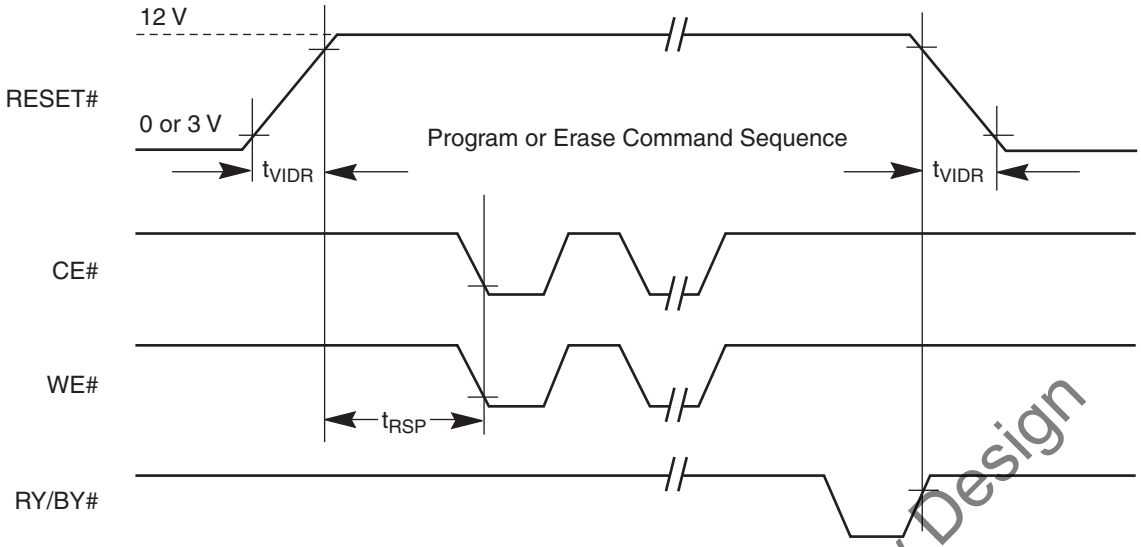
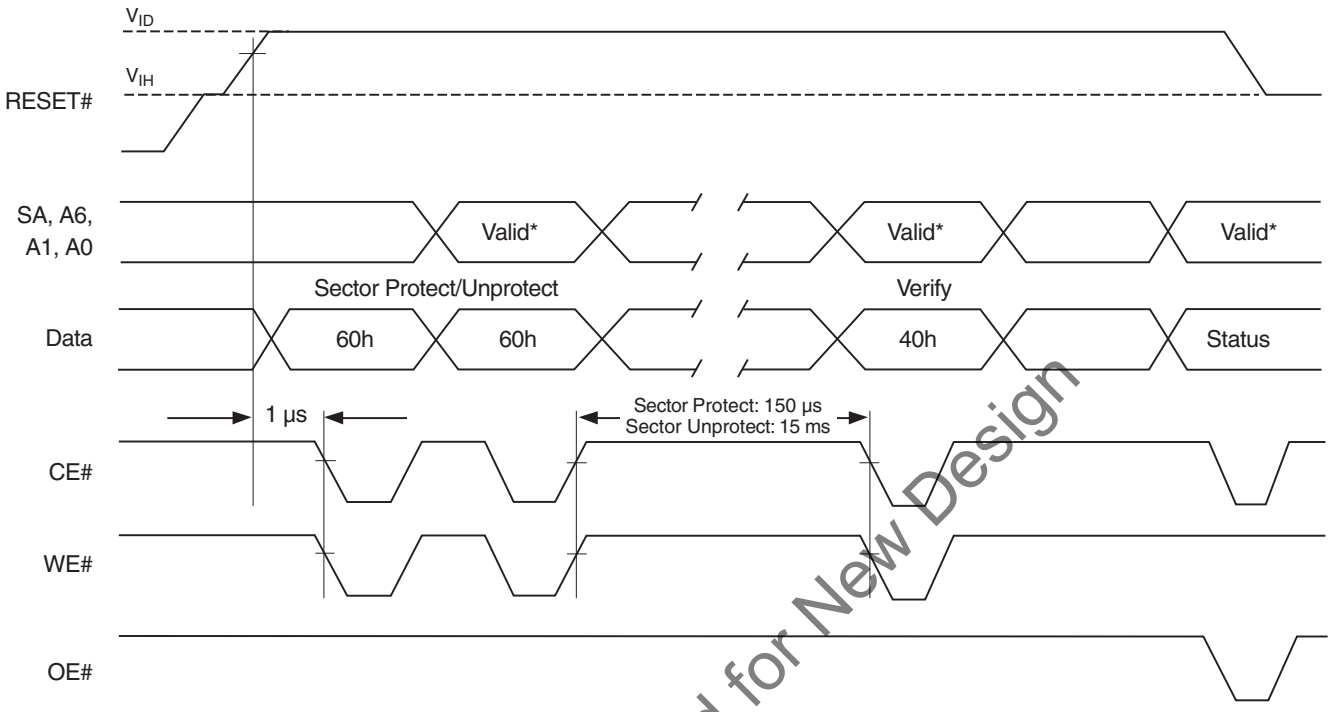


Figure 18.2 Accelerated Program Timing Diagram



Not Recommended for New Design

Figure 18.3 Sector Protect/Unprotect Timing Diagram



Note
For sector protect, A6 = 0, A1 = 1, A0 = 0. For sector unprotect, A6 = 1, A1 = 1, A0 = 0.

Not Recommended for New Design

17.6 Alternate CE# Controlled Erase/Program Operations

Table 18. Alternate CE# Controlled Erase/Program Operations

Parameter		Description			Speed Options		Unit
JEDEC	Std.				70	90	
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)		Min	70	90	ns
t_{AVEL}	t_{AS}	Address Setup Time		Min	0		ns
t_{ELAX}	t_{AH}	Address Hold Time		Min	45	45	ns
t_{DVEH}	t_{DS}	Data Setup Time		Min	35	45	ns
t_{EHDX}	t_{DH}	Data Hold Time		Min	0		ns
	t_{OES}	Output Enable Setup Time		Min	0		ns
t_{GHEL}	t_{GHEL}	Read Recovery Time Before Write (OE# High to WE# Low)		Min	0		ns
t_{WLEL}	t_{WS}	WE# Setup Time		Min	0		ns
t_{EHWH}	t_{WH}	WE# Hold Time		Min	0		ns
t_{ELEH}	t_{CP}	CE# Pulse Width		Min	35	35	ns
t_{EHEL}	t_{CPH}	CE# Pulse Width High		Min	30		ns
	$t_{SR/W}$	Latency Between Read and Write Operations		Min	20		ns
t_{WHWH1}	t_{WHWH1}	Programming Operation (Note 2)	Byte	Typ	9		µs
			Word	Typ	11		

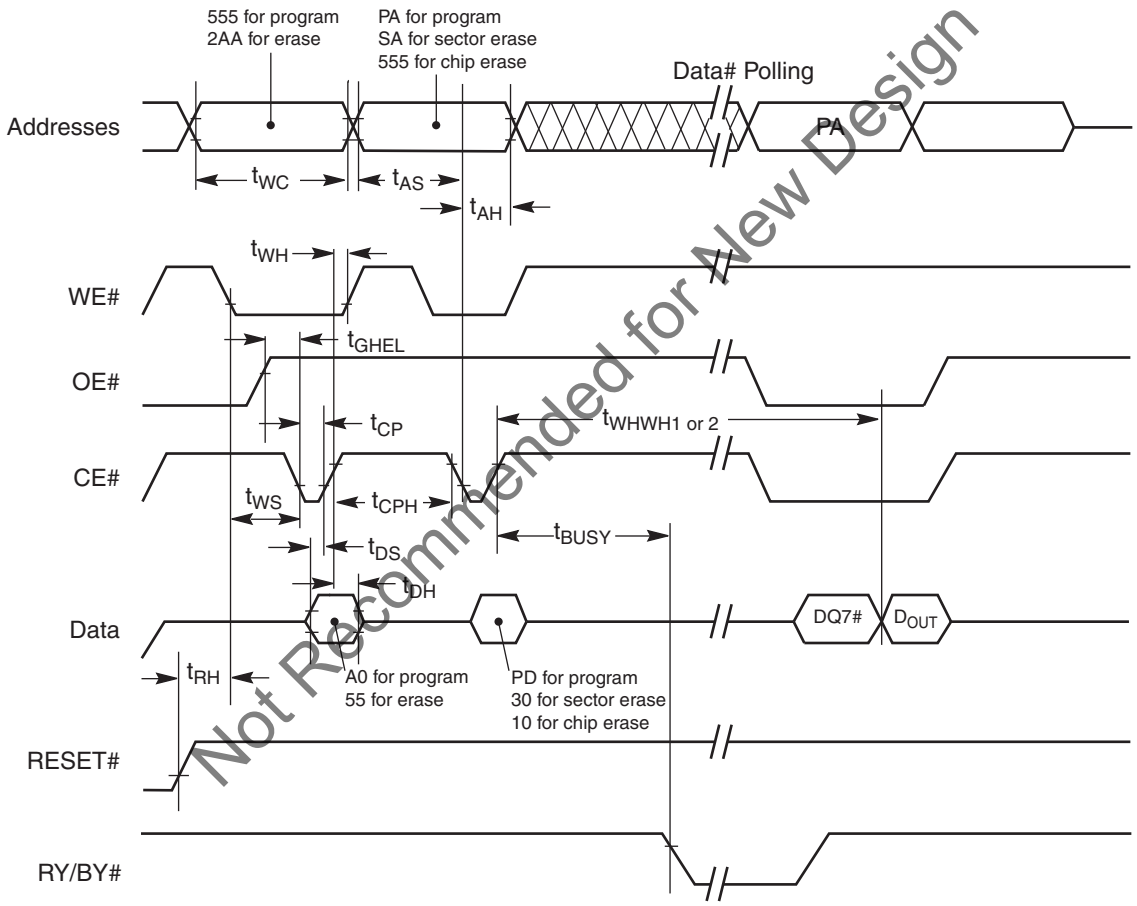
Table 18. Alternate CE# Controlled Erase/Program Operations

Parameter		Description		Speed Options		Unit
JEDEC	Std.			70	90	
t_{WHWH1}	t_{WHWH1}	Accelerated Programming Operation, Word or Byte (Note 2)	Typ	7		µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 2)	Typ	0.7		sec

Notes

1. *Not 100% tested.*
2. *See the Erase and Programming Performance on page 57 section for more information.*

Figure 18.1 Alternate CE# Controlled Write Operation Timings



Not Recommended for New Design

Notes

1. *PA = program address, PD = program data, DQ7# = complement of the data written to the device, D_{OUT} = data written to the device.*
2. *Figure indicates the last two bus cycles of the command sequence.*
3. *Word mode address used as an example.*

18. Erase and Programming Performance

Parameter		Typ (Note 1)	Max (Note 2)	Unit	Comments
Sector Erase Time (Note 7)		0.7	10	s	Excludes 00h programming prior to erasure (Note 4)
Chip Erase Time (Note 8)		45		s	
Byte Programming Time		9	300	µs	Excludes system level overhead (Note 5)
Word Programming Time		11	360	µs	
Accelerated Byte/Word Programming Time		7	210	µs	
Chip Programming Time (Note 3)	Byte Mode	36	108	s	
	Word Mode	24	72	s	

Notes

1. *Typical program and erase times assume the following conditions: 25°C, V_{CC} = 3.0 V, 100,000 cycles, checkerboard data pattern.*
2. *Under worst case conditions of 90°C, V_{CC} = 2.7 V, 1,000,000 cycles.*
3. *The typical chip programming time is considerably less than the maximum chip programming time listed, since most bytes program faster than the maximum program times listed.*
4. *In the pre-programming step of the Embedded Erase algorithm, all bytes are programmed to 00h before erasure.*
5. *System-level overhead is the time required to execute the two- or four-bus-cycle sequence for the program command. See Table 13 for further information on command definitions.*
6. *The device has a minimum erase and program cycle endurance of 100,000 cycles per sector.*
7. *At extended temperature range (>+85°C), typical erase time is 1.75 s and maximum erase time is 25 s.*
8. *At extended temperature range (>+85°C), typical erase time is 112 s.*

19. TSOP and BGA Pin Capacitance

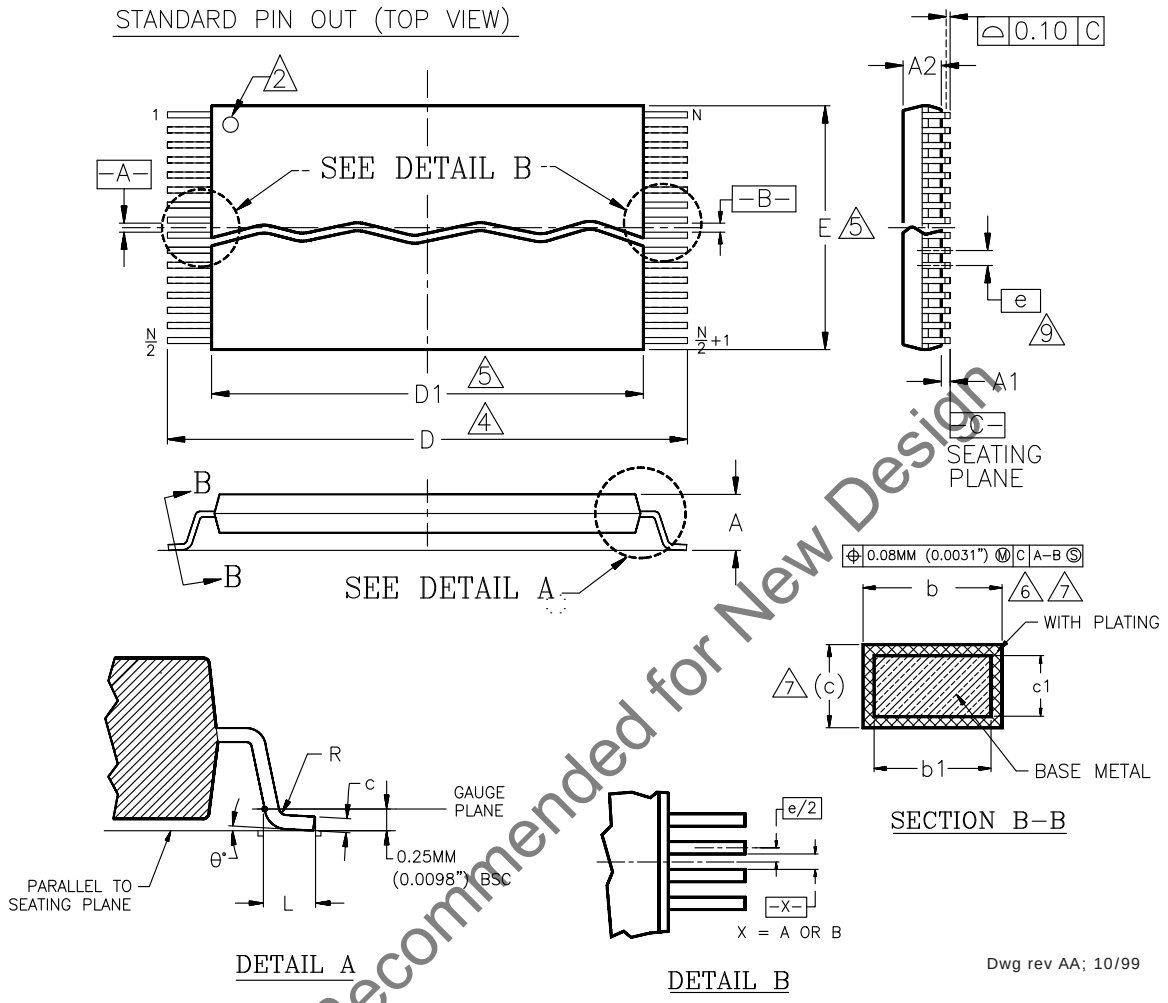
Parameter Symbol	Parameter Description	Test Setup	Package	Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	TSOP	6	7.5	pF
			BGA	4.2	5.0	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	TSOP	8.5	12	pF
			BGA	5.4	6.5	pF
C_{IN2}	Control Pin Capacitance	V_{IN} = 0	TSOP	7.5	9	pF
			BGA	3.9	4.7	pF

Notes

1. *Sampled, not 100% tested.*
2. *Test conditions T_A = 25°C, f = 1.0 MHz.Physical Dimensions*

Not Recommended for New Design

19.1 TS040—40-Pin Standard TSOP

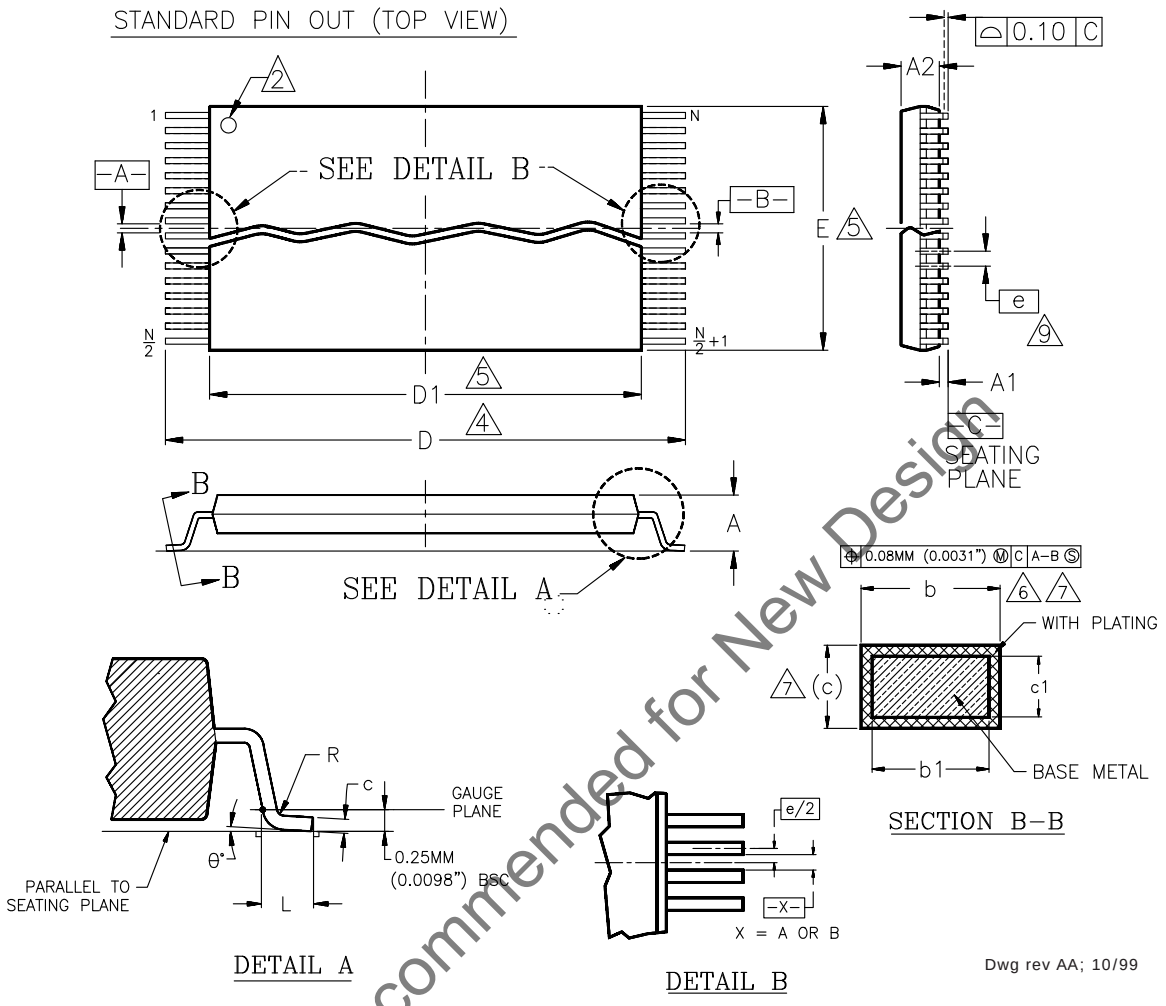


Package	TS 40		
Jedec	MO-142 (B) CD		
Symbol	MIN	NOM	MAX
A	—	—	1.20
A1	0.05	—	0.15
A2	0.95	1.00	1.05
b1	0.17	0.20	0.23
b	0.17	0.22	0.27
c1	0.10	—	0.16
c	0.10	—	0.21
D	19.80	20.00	20.20
D1	18.30	18.40	18.50
E	9.90	10.00	10.10
e	0.50 BASIC		
L	0.50	0.60	0.70
θ	0°	3°	5°
R	0.08	—	0.20
N	40		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (mm). (DIMENSIONING AND TOLERANCING CONFORMS TO ANSI Y14.5M-1982)
2. PIN 1 IDENTIFIER FOR STANDARD PIN OUT (DIE UP).
3. PIN 1 IDENTIFIER FOR REVERSE PIN OUT (DIE DOWN): INK OR LASER MARK.
4. TO BE DETERMINED AT THE SEATING PLANE -C-. THE SEATING PLANE IS DEFINED AS THE PLANE OF CONTACT THAT IS MADE WHEN THE PACKAGE LEADS ARE ALLOWED TO REST FREELY ON A FLAT HORIZONTAL SURFACE.
5. DIMENSIONS D1 AND E DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTUSION IS 0.15mm (.0059") PER SIDE.
6. DIMENSION b DOES NOT INCLUDE DAMBAR PROTUSION. ALLOWABLE DAMBAR PROTUSION SHALL BE 0.08mm (0.0031") TOTAL IN EXCESS OF b DIMENSION AT MAX. MATERIAL CONDITION. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD TO BE 0.07mm (0.0028").
7. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm (.0039") AND 0.25mm (0.0098") FROM THE LEAD TIP.
8. LEAD COPLANARITY SHALL BE WITHIN 0.10mm (0.004") AS MEASURED FROM THE SEATING PLANE.
9. DIMENSION "e" IS MEASURED AT THE CENTERLINE OF THE LEADS.

Not Recommended for New Design



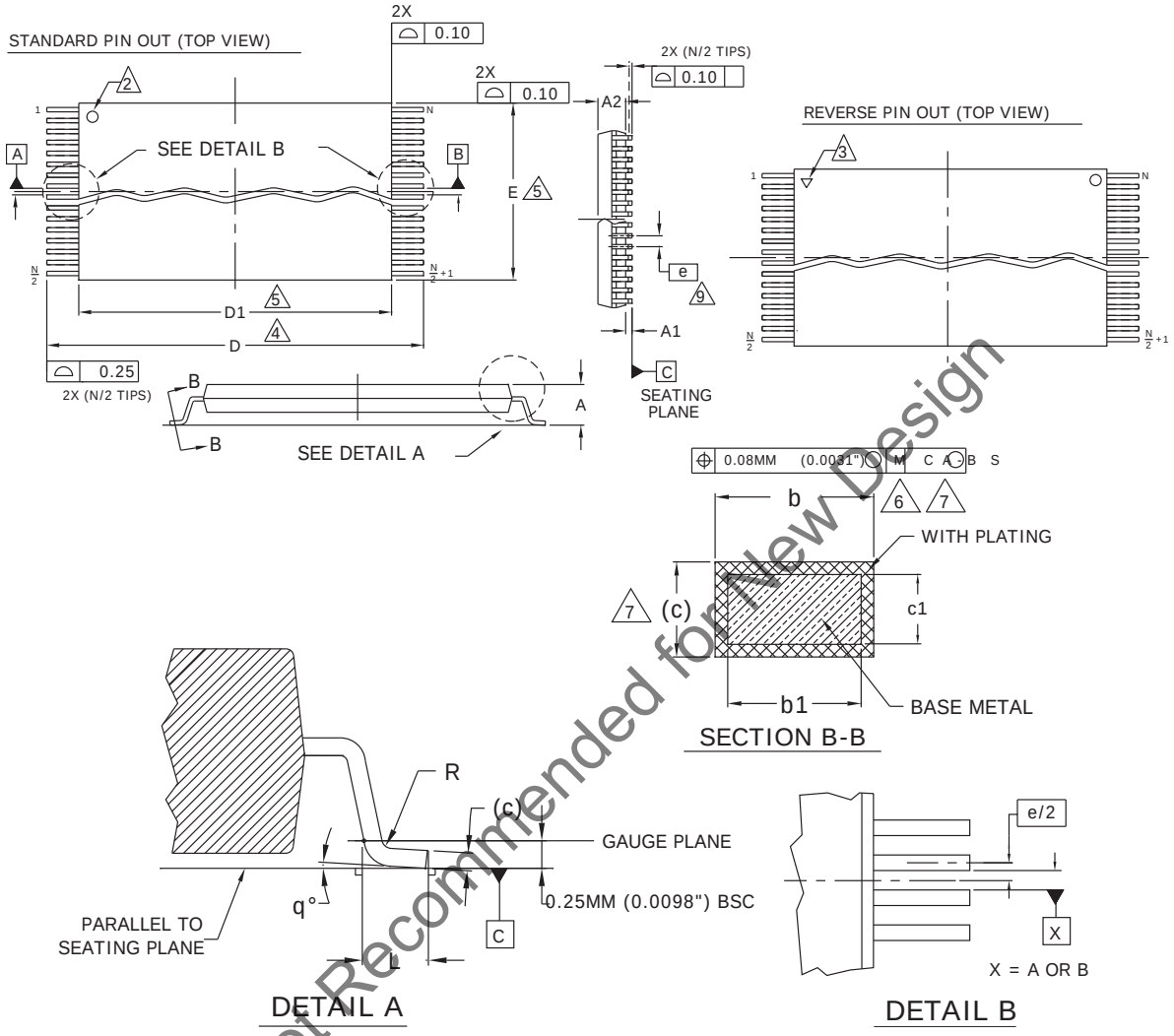
Not Recommended for New Design

Package	TS 40		
Jedec	MO-142 (B) CD		
Symbol	MIN	NOM	MAX
A	—	—	1.20
A1	0.05	—	0.15
A2	0.95	1.00	1.05
b1	0.17	0.20	0.23
b	0.17	0.22	0.27
c1	0.10	—	0.16
c	0.10	—	0.21
D	19.80	20.00	20.20
D1	18.30	18.40	18.50
E	9.90	10.00	10.10
e	0.50 BASIC		
L	0.50	0.60	0.70
θ	0°	3°	5°
R	0.08	—	0.20
N	40		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (mm). (DIMENSIONING AND TOLERANCING CONFORMS TO ANSI Y14.5M-1982)
2. PIN 1 IDENTIFIER FOR STANDARD PIN OUT (DIE UP).
3. PIN 1 IDENTIFIER FOR REVERSE PIN OUT (DIE DOWN): INK OR LASER MARK.
4. TO BE DETERMINED AT THE SEATING PLANE -C-. THE SEATING PLANE IS DEFINED AS THE PLANE OF CONTACT THAT IS MADE WHEN THE PACKAGE LEADS ARE ALLOWED TO REST FREELY ON A FLAT HORIZONTAL SURFACE.
5. DIMENSIONS D1 AND E DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTUSION IS 0.15mm (.0059") PER SIDE.
6. DIMENSION b DOES NOT INCLUDE DAMBAR PROTUSION. ALLOWABLE DAMBAR PROTUSION SHALL BE 0.08mm (0.0031") TOTAL IN EXCESS OF b DIMENSION AT MAX. MATERIAL CONDITION. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD TO BE 0.07mm (0.0028").
7. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm (.0039") AND 0.25mm (0.0098") FROM THE LEAD TIP.
8. LEAD COPLANARITY SHALL BE WITHIN 0.10mm (0.004") AS MEASURED FROM THE SEATING PLANE.
9. DIMENSION "e" IS MEASURED AT THE CENTERLINE OF THE LEADS.

19.2 TS 048—48-Pin Standard TSOP



Not Recommended for New Design

Jedec	MO-142 (D) DD		
Symbol	MIN	NOM	MAX
A	—	—	1.20
A1	0.05	—	0.15
A2	0.95	1.00	1.05
b1	0.17	0.20	0.23
b	0.17	0.22	0.27
c1	0.10	—	0.16
c	0.10	—	0.21
D	19.80	20.00	20.20
D1	18.30	18.40	18.50
E	11.90	12.00	12.10
e	0.50 BASIC		
L	0.50	0.60	0.70
θ	0°	—	8°
R	0.08	—	0.20
N	48		

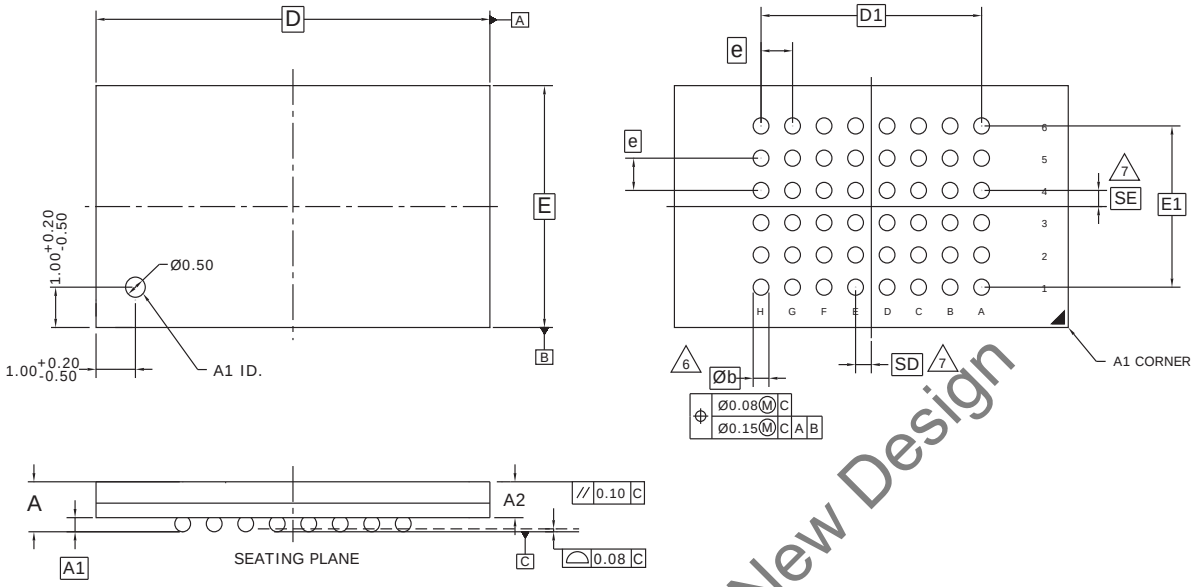
NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (mm). (DIMENSIONING AND TOLERANCING CONFORMS TO ANSI Y14.5M-1982)
2. PIN 1 IDENTIFIER FOR REVERSE PIN OUT (DIE UP).
3. PIN 1 IDENTIFIER FOR REVERSE PIN OUT (DIE DOWN), INK OR LASER MARK.
4. TO BE DETERMINED AT THE SEATING PLANE -C- . THE SEATING PLANE IS DEFINED AS THE PLANE OF CONTACT THAT IS MADE WHEN THE PACKAGE LEADS ARE ALLOWED TO REST FREELY ON A FLAT HORIZONTAL SURFACE.
5. DIMENSIONS D1 AND E DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTUSION IS 0.15mm (.0059") PER SIDE.
6. DIMENSION b DOES NOT INCLUDE DAMBAR PROTUSION. ALLOWABLE DAMBAR PROTUSION SHALL BE 0.08 (0.0031") TOTAL IN EXCESS OF b DIMENSION AT MAX. MATERIAL CONDITION. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD TO BE 0.07 (0.0028").
7. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10MM (.0039") AND 0.25MM (0.0098") FROM THE LEAD TIP.
8. LEAD COPLANARITY SHALL BE WITHIN 0.10mm (0.004") AS MEASURED FROM THE SEATING PLANE.
9. DIMENSION "e" IS MEASURED AT THE CENTERLINE OF THE LEADS.

3355 \ 16-038.10c

** For reference only. BSC is an ANSI standard for Basic Space Centering.*

19.3 VBN048—48-Ball Fine-Pitch Ball Grid Array (FBGA) 10.0 x 6.0 mm



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PACKAGE	VBN 048			
JEDEC	N/A			
	10.00 mm x 6.00 mm NOM PACKAGE			
SYMBOL	MIN	NOM	MAX	NOTE
A	---	---	1.00	OVERALL THICKNESS
A1	0.17	---	---	BALL HEIGHT
A2	0.62	---	0.73	BODY THICKNESS
D	10.00 BSC.			BODY SIZE
E	6.00 BSC.			BODY SIZE
D1	5.60 BSC.			BALL FOOTPRINT
E1	4.00 BSC.			BALL FOOTPRINT
MD	8			ROW MATRIX SIZE D DIRECTION
ME	6			ROW MATRIX SIZE E DIRECTION
N	48			TOTAL BALL COUNT
fb	0.35	---	0.45	BALL DIAMETER
e	0.80 BSC.			BALL PITCH
SD / SE	0.40 BSC.			SOLDER BALL PLACEMENT
	NONE			DEPOPULATED SOLDER BALLS

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JESD 95-1, SPP-010 (EXCEPT AS NOTED).
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL ROW MATRIX SIZE IN THE "D" DIRECTION.

   SYMBOL "ME" IS THE BALL COLUMN MATRIX SIZE IN THE "E" DIRECTION.

   N IS THE TOTAL NUMBER OF SOLDER BALLS.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW PARALLEL TO THE D OR E DIMENSION, RESPECTIVELY, SD OR SE = 0.000.

   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2
8. NOT USED.
9. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
10. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

3425\ 16-038.25

20. Document History Page

Document Title:S29AL032D 32 Mbit, 3 V, Flash 4 M x 8-Bit Uniform Sector 4 M x 8-Bit/2 M x 16-Bit Boot Sector Document Number: 002-02003				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	-	RYSU	01/31/2005	Initial release **Spansion Publication Number:** S29AL032D_00
			03/16/2005	**Distinctive Characteristics** Revised Secured Silicon Sector with 128-word information. **Common Flash Memory Interface — (CFI)** Modified Primary Vendor-Specific Extended Query table information for 45h address..
			04/19/2005	**Valid Combinations Table** Clarified available packing types for TSOP and FBGA package. Modified Note 1. **Device Bus Operations** Added Secured Silicon Sector Addresses—Model 00 table Modified Top Boot Secured Silicon Sector Addresses—Model 03 and Bottom Boot Secured Silicon Sector Addresses—Model 04 tables **S29AL032D Command Definitions Model 00 table** Added Secured Silicon Sector Factory Protect information. **Accelerated Program Operation Added section.** Secured Silicon Sector Added section. **AC Characteristics** Added ACC programming timing diagram
**	-	RYSU	06/13/2005	**Autoselect Mode** Updated Table 8 to include models 00, 03, and 04. **Common Flash Memory Interface** Updated table headings in table 12, 13, 14, and 15. **Absolute Maximum Rating** Updated figure 8. **DC Characteristics** Updated CMOS Compatible table. **AC Characteristics** Updated Erase/Program Operations table. Added new figure: Back-to-Back Read/Write Cycle Timing. Updated Alternate CE# Controlled Erase/Program Operations table.
			07/29/2005	**DS Status** Change of DS status to “Preliminary” from “Advance Information”. **Output Disable Mode** Updated Model 00 Secured Silicon Sector Analysis table. **Autoselect Mode** Updated S29AL032D Autoselect Codes (High Voltage Method) table.

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Document Title:S29AL032D 32 Mbit, 3 V, Flash 4 M x 8-Bit Uniform Sector 4 M x 8-Bit/2 M x 16-Bit Boot Sector Document Number: 002-02003				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	-	RYSU	09/21/2005	**DS Status** Change of DS status to “Preliminary” from “Advance Information”. **Sector Protection/Unprotection** Corrected “In-System Sector Protect/Unprotect Algorithms” figure.
			05/22/2006	**AC Characteristics** Added $t_{SR/W}$ parameter to read and erase/program operations tables. Added back-to-back read/write cycle timing diagram. Changed maximum value for t_{DF} and t_{FLQZ}.
			06/19/2006	**Ordering Information** Added extended temperature range options to valid combinations. **Common Flash Memory Interface (CFI)** *Primary Vendor-Specific Extended Query table:* Change description for data at address 4Fh (address 9Eh on Models 03, 04). **DC Characteristics** Changed Note 4. **Read Operations Timings figure** Connected end of t_{RC} period to start of t_{OH} period. **Erase and Programming Performance** Added Notes 7 and 8 to table.
**	-	RYSU	11/02/2006	**Valid Combinations** Updated table.
			01/19/2007	**Autoselect Code (High Voltage Method)table; Command Definitions, x8 Mode—Models 03, 04 table** Corrected data for Secured Silicon Sector Sector Indicator Bit.
*A	5038714	RYSU	12/07/2015	Updated to cypress template
*B	5075821	RYSU	01/08/2016	Added a note in blue font in page 1 showing the suggested replacement parts. Removed Spansion Revision History.

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