PSOC™ 4 high voltage (HV) mixed signal (MS) MCU: PSOC™ 4 HVMS-64K registers

Reference manual

About this document

Scope and purpose

The PSOC™ 4 HVMS-64K registers reference manual provides reference information for registers and contains respective programming details.

Intended audience

This reference manual is intended for the system designers, programmers who are designing, or programming using PSOC™ 4 HVMS-64K parts.

Definitions

Register Permission

The following table lists the register permission based on protection context and priviledges.

Permission	Description
READ	User mode = Read access, privilege mode = read, Non-secure = yes
PRIVILEGE - WRITE	User mode = Read access, privilege mode = Read and Write access, Non-secure = yes
NO-ACCESS	User mode = No access, Privilege mode = No access, Non-secure = yes
SECURE - READ	User mode = Read access, Privilege mode = Read access, Non-secure = No
FULL	Read and Write access in all modes, Non-secure = yes

Software Access

The following table lists the behavior of registers, on various Software Read/Write Accesses.

SW Access	HW Access	Software Reads Register	Software Writes Register	Software Description
R	any	Register contents	Ignored	Software read-only
RW	any	Register contents	Register takes data written	Software read and write
RW1S	any	Register contents	Every bit is set upon writing 1	Software read and write 1 to set
RW0S	any	Register contents	Every bit is set upon writing 0	Software read and write 0 to set
RW1C	any	Register contents	Every bit is cleared upon writing 1	Software read and write 1 to clear
RW0C	any	Register contents	Every bit is cleared upon writing 0	Software read and write 0 to clear
RW1SC	any	NA	NA	Illegal
RW0SC	any	NA	NA	Illegal
W	any	Zero	Register takes data written	Software write only
W1S	any	Zero	Every bit is set upon writing 1	Software write 1 to set (no read)
W0S	any	Zero	Every bit is set upon writing 0	Software write 0 to set (no read)
W1C	any	Zero	Every bit is cleared upon writing 1	Software write 1 to clear (no read)
W0C	any	Zero	Every bit is cleared upon writing 0	Software write 0 to clear (no read)
W1SC	any	NA	NA	Illegal
W0SC	any	NA	NA	Illegal
A	any	NA	NA	Illegal

Hardware Access

The following table lists the behavior of registers, on various Hardware Read/Write Accesses.

HW Access	SW Access	Hardware Description
any	R	Hardware read only
any	RW	Hardware read and write
any	RW1S	Hardware read and set
any	RW0S	Hardware read and set
any	RW1C	Hardware read and clear
any	RW0C	Hardware read and clear
any	RW1SC	Hardware read and set/clear
any	RW0SC	Hardware read and set/clear
any	W	Write access only
any	W1S	Hardware set
any	W0S	Hardware set
any	W1C	Hardware clear
any	W0C	Hardware clear
any	W1SC	Hardware set/clear
any	W0SC	Hardware set/clear
R	A	Not supported
RW	A	Hardware read and write
RW1S	A	Hardware read and set
RW0S	A	Hardware read and set
RW1C	A	Hardware read and clear
RW0C	A	Hardware read and clear
RW1SC	A	Not supported
RW0SC	A	Not supported
W	A	Not supported
W1S	A	Not supported
W0S	A	Not supported
W1C	A	Not supported
W0C	A	Not supported
W1SC	A	Not supported
W0SC	A	Not supported

Core, Bus and Memory Access

The Cortex-M0+ CPUSS uses AHB-Lite also for the system interconnect. Most of the IPs are compliant to the AHB-Lite protocol.

The AHB-Lite protocol is little endian; the least significant byte of a word is mapped onto the word's lowest byte address IPs use a bus data width of 32 bit.

This allows for byte (8-bit), halfword (16-bit) and word (32-bit) transfers. We distinguish two types of transfer types:
- MMIO registers: These registers are typically used for IP control and status information. Unless otherwise noted, transfers to these registers must be 32-bit transfers; any other transfer size generates an AHB-Lite bus error. An IP's MMIO registers do not necessarily fully occupy a consecutive memory region; i.e. holes may be present in the region
- Memory structures: This includes generic memory structures, such as system FLASH, system RAM and system ROM, but also IP specific memory structures. Transfer to these memory structures may be 8-bit, 16-bit or 32-bit transfers; any other transfer size generates an AHB-Lite bus error. A memory structure fully occupies a consecutive memory region; i.e. no holes are present in the memory structure region

A bus slave memory region may contain both MMIO registers and zero or more memory structures. Gaps might exist in the bus slave's memory region, either due to gaps in the MMIO memory region or gaps between the MMIO and memory structure region(s)

Gaps in the address space are reserved. Do not access these gaps, if accessed can result in Hard faults or BUS ERROR depending on which bus segment or a peripheral an address space is allocated to.

List of Partnumber

This TRM is valid for the following part numbers.

MPN	Package	Code Flash(KB)	Work Flash(KB)	SRAM(KB)
CY8C4125LCE-HVS003	32-QFN	32	0	4
CY8C4125LCE-HVS013	32-QFN	32	0	4
CY8C4126LCE-HVS003	32-QFN	64	0	8
CY8C4126LCE-HVS013	32-QFN	64	0	8
CY8C4146LCE-HVS003	32-QFN	64	0	8
CY8C4146LCE-HVS013	32-QFN	64	0	8
CY8C4125LCE-HVS103	32-QFN	32	0	4
CY8C4125LCE-HVS113	32-QFN	32	0	4
CY8C4126LCE-HVS103	32-QFN	64	0	8
CY8C4126LCE-HVS113	32-QFN	64	0	8
CY8C4146LCE-HVS103	32-QFN	64	0	8
CY8C4146LCE-HVS113	32-QFN	64	0	8
CY8C4125LDE-HVS004	48-QFN	32	0	4
CY8C4125LDE-HVS014	48-QFN	32	0	4
CY8C4126LDE-HVS004	48-QFN	64	0	8
CY8C4126LDE-HVS014	48-QFN	64	0	8
CY8C4146LDE-HVS004	48-QFN	64	0	8
CY8C4146LDE-HVS014	48-QFN	64	0	8
CY8C4125LDE-HVS104	48-QFN	32	0	4
CY8C4125LDE-HVS114	48-QFN	32	0	4
CY8C4126LDE-HVS104	48-QFN	64	0	8
CY8C4126LDE-HVS114	48-QFN	64	0	8
CY8C4146LDE-HVS104	48-QFN	64	0	8
CY8C4146LDE-HVS114	48-QFN	64	0	8
CY8C4125LWE-HVS005	56-QFN	32	0	4
CY8C4125LWE-HVS015	56-QFN	32	0	4
CY8C4126LWE-HVS005	56-QFN	64	0	8
CY8C4126LWE-HVS015	56-QFN	64	0	8
CY8C4146LWE-HVS005	56-QFN	64	0	8
CY8C4146LWE-HVS015	56-QFN	64	0	8
CY8C4125LWE-HVS105	56-QFN	32	0	4
CY8C4125LWE-HVS115	56-QFN	32	0	4
CY8C4126LWE-HVS104	56-QFN	64	0	8
CY8C4126LWE-HVS115	56-QFN	64	0	8
CY8C4146LWE-HVS105	56-QFN	64	0	8
CY8C4146LWE-HVS115	56-QFN	64	0	8

Memory mapping

MMIO	IP	Address	Description
CM0P	CM0P	0xe0000000	Cortex-M0+ System Bus (ARM PPB Peripherals)
CPUMEMSSV3_VER3	CPUSS	0x40100000	CPU Subsystem
	DMAC	0x40101000	DataWire/DMA Controller
	SPCIF	0x40110000	Flash Control Interface
FAULT	FAULT	0x40130000	Fault structures
MMIO0	PERI	0x40010000	Peripheral Interconnect
	HSIOM	0x40020000	High Speed IO Matrix (HSIOM)
	SRSSHV	0x40030000	System Resources High Voltage Subsystem
	GPIO	0x40040000	GPIO port control/configuration
	PRGIO	0x40050000	Programmable IO configuration
	HVSS	0x40060000	High Voltage Subsystem
MMIO1	TCPWM	0x40200000	Timer/Counter/PWM
	SCB 0	0x40240000	Serial Communications Block (SPI/UART/I2C)
	SCB 1	0x40250000	Serial Communications Block (SPI/UART/I2C)
	MSC	0x40290000	MultiSense Controller
	LPCOMP 0	0x402b0000	Low Power Comparators
	LPCOMP 1	0x402c0000	Low Power Comparators
	LIN	0x402d0000	LIN
	CXPI	0x402e0000	CXPI
MMIO2	SAR	0x403a0000	SAR ADC with Sequencer
	PASS	0x403f0000	PASS top-level MMIO (DSABv2, INTR)
ROMTABLE	ROMTABLE	0xf0000000	CoreSight ROM-Table with Cypress Vendor/Silicon ID
SFLASH	SFLASH	0xfffe000	Supervisory Flash Area (Cypress Trim & Wounding Info)

1 CM0P

Description Cortex-M0+ System Bus (ARM PPB Peripherals)
Base Address 0xE0000000
Size 0x100000
Slave Num MEMORYMAP

Register Name	Address	Permission	Description
CM0P_DWT_CTRL	0xE0001000	FULL	Watchpoint Comparator Configuration
CM0P_DWT_PCSR	0xE000101C	FULL	Watchpoint Comparator PC Sample
CM0P_DWT_COMP0	0xE0001020	FULL	Watchpoint Comparator Compare Value
CM0P_DWT_MASK0	0xE0001024	FULL	Watchpoint Comparator Mask
CM0P_DWT_FUNCTION0	0xE0001028	FULL	Watchpoint Comparator Function
CM0P_DWT_COMP1	0xE0001030	FULL	Watchpoint Comparator Compare Value
CM0P_DWT_MASK1	0xE0001034	FULL	Watchpoint Comparator Mask
CM0P_DWT_FUNCTION1	0xE0001038	FULL	Watchpoint Comparator Function
CM0P_DWT_PID4	0xE0001FD0	FULL	Watchpoint Unit CoreSight ROM Table Peripheral ID #4
CM0P_DWT_PID0	0xE0001FE0	FULL	Watchpoint Unit CoreSight ROM Table Peripheral ID #0
CM0P_DWT_PID1	0xE0001FE4	FULL	Watchpoint Unit CoreSight ROM Table Peripheral ID #1
CM0P_DWT_PID2	0xE0001FE8	FULL	Watchpoint Unit CoreSight ROM Table Peripheral ID #2
CM0P_DWT_PID3	0xE0001FEC	FULL	Watchpoint Unit CoreSight ROM Table Peripheral ID #3
CM0P_DWT_CID0	0xE0001FF0	FULL	Watchpoint Unit CoreSight ROM Table Component ID #0
CM0P_DWT_CID1	0xE0001FF4	FULL	Watchpoint Unit CoreSight ROM Table Component ID #1
CM0P_DWT_CID2	0xE0001FF8	FULL	Watchpoint Unit CoreSight ROM Table Component ID #2
CM0P_DWT_CID3	0xE0001FFC	FULL	Watchpoint Unit CoreSight ROM Table Component ID #3
CM0P_BP_CTRL	0xE0002000	FULL	Breakpoint Unit Control
CM0P_BP_COMP0	0xE0002008	FULL	Breakpoint Compare Register
CM0P_BP_COMP1	0xE000200C	FULL	Breakpoint Compare Register
CM0P_BP_COMP2	0xE0002010	FULL	Breakpoint Compare Register
CM0P_BP_COMP3	0xE0002014	FULL	Breakpoint Compare Register
CM0P_BP_PID4	0xE0002FD0	FULL	Breakpoint Unit CoreSight ROM Table Peripheral ID #4
CM0P_BP_PID0	0xE0002FE0	FULL	Breakpoint Unit CoreSight ROM Table Peripheral ID #0
CM0P_BP_PID1	0xE0002FE4	FULL	Breakpoint Unit CoreSight ROM Table Peripheral ID #1
CM0P_BP_PID2	0xE0002FE8	FULL	Breakpoint Unit CoreSight ROM Table Peripheral ID #2
CM0P_BP_PID3	0xE0002FEC	FULL	Breakpoint Unit CoreSight ROM Table Peripheral ID #3
CM0P_BP_CID0	0xE0002FF0	FULL	Breakpoint Unit CoreSight ROM Table Component ID #0
CM0P_BP_CID1	0xE0002FF4	FULL	Breakpoint Unit CoreSight ROM Table Component ID #1
CM0P_BP_CID2	0xE0002FF8	FULL	Breakpoint Unit CoreSight ROM Table Component ID #2
CM0P_BP_CID3	0xE0002FFC	FULL	Breakpoint Unit CoreSight ROM Table Component ID #3
CM0P_ACTLR	0xE000E008	FULL	Auxiliary Control Register
CM0P_SYST_CSR	0xE000E010	FULL	SysTick Control & Status
CM0P_SYST_RVR	0xE000E014	FULL	SysTick Reload Value
CM0P_SYST_CVR	0xE000E018	FULL	SysTick Current Value
CM0P_SYST_CALIB	0xE000E01C	FULL	SysTick Calibration Value
CM0P_ISER	0xE000E100	FULL	Interrupt Set-Enable Register

Register Name	Address	Permission	Description
CM0P_ICER	0xE000E180	FULL	Interrupt Clear Enable Register
CM0P_ISPR	0xE000E200	FULL	Interrupt Set-Pending Register
CM0P_ICPR	0xE000E280	FULL	Interrupt Clear-Pending Register
CM0P_IPR0	0xE000E400	FULL	Interrupt Priority Registers
CM0P_IPR1	0xE000E404	FULL	Interrupt Priority Registers
CM0P_IPR2	0xE000E408	FULL	Interrupt Priority Registers
CM0P_IPR3	0xE000E40C	FULL	Interrupt Priority Registers
CM0P_IPR4	0xE000E410	FULL	Interrupt Priority Registers
CM0P_IPR5	0xE000E414	FULL	Interrupt Priority Registers
CM0P_IPR6	0xE000E418	FULL	Interrupt Priority Registers
CM0P_IPR7	0xE000E41C	FULL	Interrupt Priority Registers
CM0P_CPUID	0xE000ED00	FULL	CPUID Register
CM0P_ICSR	0xE000ED04	FULL	Interrupt Control State Register
CM0P_VTOR	0xE000ED08	FULL	Vector Table Offset Register
CM0P_AIRCR	0xE000ED0C	FULL	Application Interrupt and Reset Control Register
CM0P_SCR	0xE000ED10	FULL	System Control Register
CM0P_CCR	0xE000ED14	FULL	Configuration and Control Register
CM0P_SHPR2	0xE000ED1C	FULL	System Handler Priority Register 2
CM0P_SHPR3	0xE000ED20	FULL	System Handler Priority Register 3
CM0P_SHCSR	0xE000ED24	FULL	System Handler Control and State Register
CM0P_DFSR	0xE000ED30	FULL	Debug Fault Status Register
CM0P_DHCSR	0xE000EDF0	FULL	Debug Halting Control and Status Register
CM0P_DCRSR	0xE000EDF4	FULL	Debug Core Register Selector Register
CM0P_DCRDR	0xE000EDF8	FULL	Debug Core Register Data Register
CM0P_DEMCR	0xE000EDFC	FULL	Debug Exception and Monitor Control Register
CM0P_SCS_PID4	0xE000EFD0	FULL	System Control Space ROM Table Peripheral ID #4
CM0P_SCS_PID0	0xE000EFE0	FULL	System Control Space ROM Table Peripheral ID #0
CM0P_SCS_PID1	0xE000EFE4	FULL	System Control Space ROM Table Peripheral ID #1
CM0P_SCS_PID2	0xE000EFE8	FULL	System Control Space ROM Table Peripheral ID #2
CM0P_SCS_PID3	0xE000EFEC	FULL	System Control Space ROM Table Peripheral ID #3
CM0P_SCS_CID0	0xE000EFF0	FULL	System Control Space ROM Table Component ID #0
CM0P_SCS_CID1	0xE000EFF4	FULL	System Control Space ROM Table Component ID #1
CM0P_SCS_CID2	0xE000EFF8	FULL	System Control Space ROM Table Component ID #2
CM0P_SCS_CID3	0xE000EFFC	FULL	System Control Space ROM Table Component ID #3
CM0P_ROM_SCS	0xE00FF000	FULL	CM0+ CoreSight ROM Table Peripheral #0
CM0P_ROM_DWT	0xE00FF004	FULL	CM0+ CoreSight ROM Table Peripheral #1
CM0P_ROM_BPU	0xE00FF008	FULL	CM0+ CoreSight ROM Table Peripheral #2
CM0P_ROM_END	0xE00FF00C	FULL	CM0+ CoreSight ROM Table End Marker
CM0P_ROM_CSMT	0xE00FFFCC	FULL	CM0+ CoreSight ROM Table Memory Type
CM0P_ROM_PID4	0xE00FFFD0	FULL	CM0+ CoreSight ROM Table Peripheral ID #4
CM0P_ROM_PID0	0xE00FFFE0	FULL	CM0+ CoreSight ROM Table Peripheral ID #0
CM0P_ROM_PID1	0xE00FFFE4	FULL	CM0+ CoreSight ROM Table Peripheral ID #1
CM0P_ROM_PID2	0xE00FFFE8	FULL	CM0+ CoreSight ROM Table Peripheral ID #2
CM0P_ROM_PID3	0xE00FFFEC	FULL	CM0+ CoreSight ROM Table Peripheral ID #3
CM0P_ROM_CID0	0xE00FFFF0	FULL	CM0+ CoreSight ROM Table Component ID #0
CM0P_ROM_CID1	0xE00FFFF4	FULL	CM0+ CoreSight ROM Table Component ID #1
CM0P_ROM_CID2	0xE00FFFF8	FULL	CM0+ CoreSight ROM Table Component ID #2
CM0P_ROM_CID3	0xE00FFFFC	FULL	CM0+ CoreSight ROM Table Component ID #3

1.1 Register Details

1.1.1 CM0P_DWT_CTRL

Description: Watchpoint Comparator Configuration
Address: 0xE0001000
Offset: 0x1000
Retention: Retained
IsDeepSleep: No
Comment: Defines the number of comparators implemented
Default: 0x20000000

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	NUMCOMP [31:28]				None [27:24]			

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
28:31	NUMCOMP	R		2	Number of comparators available

1.1.2 CM0P_DWT_PCSR

Description: Watchpoint Comparator PC Sample
Address: 0xE000101C
Offset: 0x101C
Retention: Retained
IsDeepSleep: No
Comment: Samples the current value of the program counter. Unless DWT_PCSR reads as 0xFFFFFFFF, under the conditions described in Program counter sampling support on page C1-344, bit [0] is RAZ. When RAZ, bit [0] does not reflect instruction set state as is the case with similar functionality in other ARM architecture profiles.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	EIASAMPLE [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	EIASAMPLE [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	EIASAMPLE [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	EIASAMPLE [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	EIASAMPLE	R	W	X	Executed Instruction Address sample value

1.1.3 CM0P_DWT_COMP0

Description: Watchpoint Comparator Compare Value
Address: 0xE0001020
Offset: 0x1020
Retention: Retained
IsDeepSleep: No
Comment: Provides a reference value for use by comparator
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	COMP [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	COMP [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	COMP [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	COMP [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	COMP	RW	R	X	Reference value for comparison.

1.1.4 CM0P_DWT_MASK0

Description: Watchpoint Comparator Mask
Address: 0xE0001024
Offset: 0x1024
Retention: Retained
IsDeepSleep: No
Comment: Provides the size of the ignore mask applied to the access address range matching
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	MASK [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	MASK [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	MASK [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	MASK [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	MASK	RW	R	X	The size of the ignore mask applied to address range matching. The mask range is IMPLEMENTATION DEFINED. Writing all ones to this field and reading it back can be used to determine the maximum mask size supported.

1.1.5 CM0P_DWT_FUNCTION0

Description: Watchpoint Comparator Function
Address: 0xE0001028
Offset: 0x1028
Retention: Retained
IsDeepSleep: No
Comment: Controls the operation of the comparator
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:4]				FUNCTION [3:0]			

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:25]							MATCHED [24:24]

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:3	FUNCTION	RW	R	0	Select action on comparator match.
	DISABLE			0	Disabled
	IADDR			4	PC watchpoint event
	DADDR_RO			5	Watchpoint event
	DADDR_WO			6	Watchpoint event
	DADDR_RW			7	Watchpoint event
24	MATCHED	R	RW	0	Comparator match. It indicates that the operation defined by FUNCTION has occurred since the bit was last read: 0 the associated comparator has matched. 1 the associated comparator has not matched. Reading the register clears this bit to 0.

1.1.6 CM0P_DWT_COMP1

Description: Watchpoint Comparator Compare Value
Address: 0xE0001030
Offset: 0x1030
Retention: Retained
IsDeepSleep: No
Comment: Provides a reference value for use by comparator
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	COMP [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	COMP [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	COMP [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	COMP [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	COMP	RW	R	X	Reference value for comparison.

1.1.7 CM0P_DWT_MASK1

Description: Watchpoint Comparator Mask
Address: 0xE0001034
Offset: 0x1034
Retention: Retained
IsDeepSleep: No
Comment: Provides the size of the ignore mask applied to the access address range matching
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	MASK [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	MASK [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	MASK [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	MASK [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	MASK	RW	R	X	The size of the ignore mask applied to address range matching. The mask range is IMPLEMENTATION DEFINED. Writing all ones to this field and reading it back can be used to determine the maximum mask size supported.

1.1.8 CM0P_DWT_FUNCTION1

Description: Watchpoint Comparator Function
Address: 0xE0001038
Offset: 0x1038
Retention: Retained
IsDeepSleep: No
Comment: Controls the operation of the comparator
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:4]				FUNCTION [3:0]			

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:25]							MATCHED [24:24]

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:3	FUNCTION	RW	R	0	Select action on comparator match.
	DISABLE			0	Disabled
	IADDR			4	PC watchpoint event
	DADDR_RO			5	Watchpoint event
	DADDR_WO			6	Watchpoint event
	DADDR_RW			7	Watchpoint event
24	MATCHED	R	RW	0	Comparator match. It indicates that the operation defined by FUNCTION has occurred since the bit was last read: 0 the associated comparator has matched. 1 the associated comparator has not matched. Reading the register clears this bit to 0.

1.1.9 CM0P_DWT_PID4

Description: Watchpoint Unit CoreSight ROM Table Peripheral ID #4
Address: 0xE0001FD0
Offset: 0x1FD0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x4

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	VALUE [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	VALUE	R		4	Peripheral ID #4

1.1.10 CM0P_DWT_PID0

Description: Watchpoint Unit CoreSight ROM Table Peripheral ID #0
Address: 0xE0001FE0
Offset: 0x1FE0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xA

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	VALUE [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	VALUE	R		10	Peripheral ID #0

1.1.11 CM0P_DWT_PID1

Description: Watchpoint Unit CoreSight ROM Table Peripheral ID #1
Address: 0xE0001FE4
Offset: 0x1FE4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xB0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	VALUE [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	VALUE	R		176	Peripheral ID #1

1.1.12 CM0P_DWT_PID2

Description: Watchpoint Unit CoreSight ROM Table Peripheral ID #2
Address: 0xE0001FE8
Offset: 0x1FE8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xB

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	VALUE [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	VALUE	R		11	Peripheral ID #2

1.1.13 CM0P_DWT_PID3

Description: Watchpoint Unit CoreSight ROM Table Peripheral ID #3
Address: 0xE0001FEC
Offset: 0x1FEC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	VALUE [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	VALUE	R		0	Peripheral ID #3

1.1.14 CM0P_DWT_CID0

Description: Watchpoint Unit CoreSight ROM Table Component ID #0
Address: 0xE0001FF0
Offset: 0x1FF0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xD

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	VALUE [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	VALUE	R		13	Component ID #0

1.1.15 CM0P_DWT_CID1

Description: Watchpoint Unit CoreSight ROM Table Component ID #1
Address: 0xE0001FF4
Offset: 0x1FF4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xE0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	VALUE [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	VALUE	R		224	Component ID #1

1.1.16 CM0P_DWT_CID2

Description: Watchpoint Unit CoreSight ROM Table Component ID #2
Address: 0xE0001FF8
Offset: 0x1FF8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x5

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	VALUE [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	VALUE	R		5	Component ID #2

1.1.17 CM0P_DWT_CID3

Description: Watchpoint Unit CoreSight ROM Table Component ID #3
Address: 0xE0001FFC
Offset: 0x1FFC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xB1

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	VALUE [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	VALUE	R		177	Component ID #3

1.1.18 CM0P_BP_CTRL

Description: Breakpoint Unit Control
Address: 0xE0002000
Offset: 0x2000
Retention: Retained
IsDeepSleep: No
Comment: Provides BPU implementation information, and the global enable for the BPU.
Default: 0x40

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	NUM_CODE [7:4]				None [3:2]		KEY [1:1]	ENABLE [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	ENABLE	RW	R	0	Enables the BPU: 0 BPU is disabled. 1 BPU is enabled.
1	KEY	RW	R	0	RAZ on reads, SBO for writes. If written as zero, the write to the register is ignored.
4:7	NUM_CODE	R		4	The number of breakpoint comparators. If NUM_CODE is zero, the implementation does not support any comparators.

1.1.19 CM0P_BP_COMP0

Description: Breakpoint Compare Register
Address: 0xE0002008
Offset: 0x2008
Retention: Retained
IsDeepSleep: No
Comment: Holds a breakpoint address for comparison with instruction addresses in the Code memory region, see The system address map on page B3-258 for more information.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name							None [1:1]	ENABLE [0:0]

Bits	15	14	13	12	11	10	9	8
Name	COMP_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	COMP_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	MATCH [31:30]		None [29:29]	COMP_ADDR [28:24]				

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	ENABLE	RW	R	0	Enables the comparator: Note BP_CTRL.ENABLE must also be set to 1 to enable a comparator.
2:28	COMP_ADDR	RW	R	X	Stores bits [28:2] of the comparison address. The comparison address is compared with the address from the Code memory region. Bits [31:29] and [1:0] of the comparison address are zero.
30:31	MATCH	RW	R	X	BP_MATCH defines the behavior when the COMP address is matched.
	NONE			0	No breakpoint matching
	LOWER			1	Breakpoint on lower halfword, upper is unaffected.
	UPPER			2	Breakpoint on upper halfword, lower is unaffected.
	BOTH			3	Breakpoint on both lower and upper halfwords.

1.1.20 CM0P_BP_COMP1

Description: Breakpoint Compare Register
Address: 0xE000200C
Offset: 0x200C
Retention: Retained
IsDeepSleep: No
Comment: Holds a breakpoint address for comparison with instruction addresses in the Code memory region, see The system address map on page B3-258 for more information.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name							None [1:1]	ENABLE [0:0]

Bits	15	14	13	12	11	10	9	8
Name	COMP_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	COMP_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	MATCH [31:30]		None [29:29]	COMP_ADDR [28:24]				

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	ENABLE	RW	R	0	Enables the comparator: Note BP_CTRL.ENABLE must also be set to 1 to enable a comparator.
2:28	COMP_ADDR	RW	R	X	Stores bits [28:2] of the comparison address. The comparison address is compared with the address from the Code memory region. Bits [31:29] and [1:0] of the comparison address are zero.
30:31	MATCH	RW	R	X	BP_MATCH defines the behavior when the COMP address is matched.
	NONE			0	No breakpoint matching
	LOWER			1	Breakpoint on lower halfword, upper is unaffected.
	UPPER			2	Breakpoint on upper halfword, lower is unaffected.
	BOTH			3	Breakpoint on both lower and upper halfwords.

1.1.21 CM0P_BP_COMP2

Description: Breakpoint Compare Register
Address: 0xE0002010
Offset: 0x2010
Retention: Retained
IsDeepSleep: No
Comment: Holds a breakpoint address for comparison with instruction addresses in the Code memory region, see The system address map on page B3-258 for more information.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name							None [1:1]	ENABLE [0:0]

Bits	15	14	13	12	11	10	9	8
Name	COMP_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	COMP_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	MATCH [31:30]		None [29:29]	COMP_ADDR [28:24]				

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	ENABLE	RW	R	0	Enables the comparator: Note BP_CTRL.ENABLE must also be set to 1 to enable a comparator.
2:28	COMP_ADDR	RW	R	X	Stores bits [28:2] of the comparison address. The comparison address is compared with the address from the Code memory region. Bits [31:29] and [1:0] of the comparison address are zero.
30:31	MATCH	RW	R	X	BP_MATCH defines the behavior when the COMP address is matched.
	NONE			0	No breakpoint matching
	LOWER			1	Breakpoint on lower halfword, upper is unaffected.
	UPPER			2	Breakpoint on upper halfword, lower is unaffected.
	BOTH			3	Breakpoint on both lower and upper halfwords.

1.1.22 CM0P_BP_COMP3

Description: Breakpoint Compare Register
Address: 0xE0002014
Offset: 0x2014
Retention: Retained
IsDeepSleep: No
Comment: Holds a breakpoint address for comparison with instruction addresses in the Code memory region, see The system address map on page B3-258 for more information.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name							None [1:1]	ENABLE [0:0]

Bits	15	14	13	12	11	10	9	8
Name	COMP_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	COMP_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	MATCH [31:30]		None [29:29]	COMP_ADDR [28:24]				

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	ENABLE	RW	R	0	Enables the comparator. Note BP_CTRL.ENABLE must also be set to 1 to enable a comparator.
2:28	COMP_ADDR	RW	R	X	Stores bits [28:2] of the comparison address. The comparison address is compared with the address from the Code memory region. Bits [31:29] and [1:0] of the comparison address are zero.
30:31	MATCH	RW	R	X	BP_MATCH defines the behavior when the COMP address is matched.
	NONE			0	No breakpoint matching
	LOWER			1	Breakpoint on lower halfword, upper is unaffected.
	UPPER			2	Breakpoint on upper halfword, lower is unaffected.
	BOTH			3	Breakpoint on both lower and upper halfwords.

1.1.23 CM0P_BP_PID4

Description: Breakpoint Unit CoreSight ROM Table Peripheral ID #4
Address: 0xE0002FD0
Offset: 0x2FD0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x4

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	VALUE [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	VALUE	R		4	Peripheral ID #4

1.1.24 CM0P_BP_PID0

Description: Breakpoint Unit CoreSight ROM Table Peripheral ID #0
Address: 0xE0002FE0
Offset: 0x2FE0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xB

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	VALUE [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	VALUE	R		11	Peripheral ID #0

1.1.25 CM0P_BP_PID1

Description: Breakpoint Unit CoreSight ROM Table Peripheral ID #1
Address: 0xE0002FE4
Offset: 0x2FE4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xB0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	VALUE [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	VALUE	R		176	Peripheral ID #1

1.1.26 CM0P_BP_PID2

Description: Breakpoint Unit CoreSight ROM Table Peripheral ID #2
Address: 0xE0002FE8
Offset: 0x2FE8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xB

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	VALUE [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	VALUE	R		11	Peripheral ID #2

1.1.27 CM0P_BP_PID3

Description: Breakpoint Unit CoreSight ROM Table Peripheral ID #3
Address: 0xE0002FEC
Offset: 0x2FEC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	VALUE [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	VALUE	R		0	Peripheral ID #3

1.1.28 CM0P_BP_CID0

Description: Breakpoint Unit CoreSight ROM Table Component ID #0
Address: 0xE0002FF0
Offset: 0x2FF0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xD

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	VALUE [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	VALUE	R		13	Component ID #0

1.1.29 CM0P_BP_CID1

Description: Breakpoint Unit CoreSight ROM Table Component ID #1
Address: 0xE0002FF4
Offset: 0x2FF4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xE0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	VALUE [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	VALUE	R		224	Component ID #1

1.1.30 CM0P_BP_CID2

Description: Breakpoint Unit CoreSight ROM Table Component ID #2
Address: 0xE0002FF8
Offset: 0x2FF8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x5

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	VALUE [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	VALUE	R		5	Component ID #2

1.1.31 CM0P_BP_CID3

Description: Breakpoint Unit CoreSight ROM Table Component ID #3
Address: 0xE0002FFC
Offset: 0x2FFC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xB1

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	VALUE [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	VALUE	R		177	Component ID #3

1.1.32 CM0P_ACTLR

Description: Auxiliary Control Register
Address: 0xE000E008
Offset: 0xE008
Retention: Retained
IsDeepSleep: No
Comment: Provides configuration and control options.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	ACTRL [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	ACTRL [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	ACTRL [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	ACTRL [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	ACTRL	R		0	Always 0 for CM0+ r0p1

1.1.33 CM0P_SYST_CSR

Description: SysTick Control & Status
Address: 0xE000E010
Offset: 0xE010
Retention: Retained
IsDeepSleep: No
Comment: Controls the SysTick counter and provides status data. The SysTick counter is functional in the Active and Sleep power modes (and not functional in the DeepSleep, Hibernate and Stop power modes).
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:3]					CLKSOURCE [2:2]	TICKINT [1:1]	ENABLE [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:17]							COUNTFLAG [16:16]

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	ENABLE	RW	R	0	Indicates the enabled status of the SysTick counter: '0': counter is disabled. '1': counter is operating.
1	TICKINT	RW	R	0	Indicates whether counting to '0' causes the status of the SysTick exception to change to pending: '0': count to '0' does not affect the SysTick exception status. '1': count to '0' changes the SysTick exception status to pending. Changing the value of the counter to '0' by writing zero to the SYST_CVR register to '0' never changes the status of the SysTick exception.
2	CLKSOURCE	RW	R	0	Indicates the SysTick counter clock source: '0': SysTick uses the low frequency clock 'clk_lf'. For this mode to function, 'clk_lf' should be less than half the frequency of 'clk_sys'. Note that 'clk_lf' is generated by a low accuracy ILO (Internal Low power Oscillator), with a target frequency of 32.768 kHz (frequency can be as low as 15 kHz and as high as 60 kHz). '1': SysTick uses the system/processor clock 'clk_sys'. If SysTick counter functionality is not present in the device. This field should be set to '1', such that SysTick uses the system clock 'clk_sys'.

Bits	Name	SW	HW	Default or Enum	Description
16	COUNTFLAG	R	RW	0	Indicates whether the counter has counted to '0' since the last read of this register: '0': counter has not counted to '0'. '1': counter has counted to '0'. COUNTFLAG is set to '1' by a count transition from '1' to '0'. COUNTFLAG is cleared to '0' by a read of this register, and by any write to the SYST_CVR register.

1.1.34 CM0P_SYST_RVR

Description: SysTick Reload Value
Address: 0xE000E014
Offset: 0xE014
Retention: Retained
IsDeepSleep: No
Comment: Sets or reads the reload value of the SYST_CVR register.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	RELOAD [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	RELOAD [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	RELOAD [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:23	RELOAD	RW	R	X	The value to load into the SYST_CVR register when the counter reaches 0.

1.1.35 CM0P_SYST_CVR

Description: SysTick Current Value
Address: 0xE000E018
Offset: 0xE018
Retention: Retained
IsDeepSleep: No
Comment: Reads or clears the current counter value. Any write to the register clears the register to 0.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	CURRENT [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	CURRENT [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	CURRENT [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:23	CURRENT	RW	R	X	Current counter value. This is the value of the counter at the time it is sampled.

1.1.36 CM0P_SYST_CALIB

Description: SysTick Calibration Value
Address: 0xE000E01C
Offset: 0xE01C
Retention: Retained
IsDeepSleep: No
Comment: Reads the calibration value and parameters for SysTick.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	TENMS [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	TENMS [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	TENMS [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	NOREF [31:31]	SKEW [30:30]	None [29:24]					

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:23	TENMS	R	RW	X	Optionally, holds a reload value to be used for 10ms (100Hz) timing, subject to system clock skew errors. If this field is '0', the calibration value is not known. In PSoC4A-BLE (and later products), SysTick counter functionality on the low frequency clock is provided and this field is 0x00:00147. In earlier products, SysTick counter functionality on the low frequency clock is NOT provided and this field is 0x00:0000.
30	SKEW	R	RW	X	Indicates whether the 10ms calibration value is exact: '0': 10ms calibration value is exact. '1': 10ms calibration value is inexact, because of the clock frequency. In PSoC4A-BLE (and later products), SysTick counter functionality on the low frequency clock is provided and this field is '1' (due to the low accuracy ILO). In earlier products, SysTick counter functionality on the low frequency clock is NOT provided and this field is '0'.
31	NOREF	R		0	Indicates whether a implementation defined reference clock is provided: '0': the reference clock is provided. '1': the reference clock is not provided. When this bit is '1', the SYST_CSR.CLKSOURCEis forced to '1' and cannot be cleared to '0'. In PSoC4A-BLE (and later products), SysTick counter functionality on the low frequency clock is provided and this field is '0'. In earlier products, SysTick counter functionality on the low frequency clock is NOT provided and this field is '1'.

1.1.37 CM0P_ISER

Description: Interrupt Set-Enable Register
Address: 0xE000E100
Offset: 0xE100
Retention: Retained
IsDeepSleep: No
Comment: Enables, or reads the enabled state of one or more interrupts.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	SETENA [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	SETENA [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	SETENA [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	SETENA [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	SETENA	RW1S	R	0	Enables, or reads the enabled state of one or more interrupts. Each bit corresponds to the same numbered interrupt.

1.1.38 CM0P_ICER

Description: Interrupt Clear Enable Register
Address: 0xE000E180
Offset: 0xE180
Retention: Retained
IsDeepSleep: No
Comment: Disables, or reads the enabled state of one or more interrupts
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	CLRENA [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	CLRENA [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	CLRENA [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	CLRENA [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	CLRENA	RW1C	R	0	Disables, or reads the enabled state of one or more interrupts. Each bit corresponds to the same numbered interrupt.

1.1.39 CM0P_ISPR

Description: Interrupt Set-Pending Register
Address: 0xE000E200
Offset: 0xE200
Retention: Retained
IsDeepSleep: No
Comment: On writes, sets the status of one or more interrupts to pending. On reads, shows the pending status of the interrupts.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	SETPEND [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	SETPEND [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	SETPEND [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	SETPEND [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	SETPEND	RW1S	R	0	Changes the state of one or more interrupts to pending. Each bit corresponds to the same numbered interrupt.

1.1.40 CM0P_ICPR

Description: Interrupt Clear-Pending Register
Address: 0xE000E280
Offset: 0xE280
Retention: Retained
IsDeepSleep: No
Comment: On writes, clears the status of one or more interrupts to pending. On reads, shows the pending status of the interrupts.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	CLRPEND [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	CLRPEND [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	CLRPEND [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	CLRPEND [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	CLRPEND	RW1C	R	0	Changes the state of one or more interrupts to not pending. Each bit corresponds to the same numbered interrupt.

1.1.41 CM0P_IPR

Description: Interrupt Priority Registers
Address: 0xE000E400
Offset: 0xE400
Retention: Retained
IsDeepSleep: No
Comment: Sets or reads interrupt priorities. Register n contains priorities for interrupts N=4n .. 4n+3
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	PRI_N0 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
Name	PRI_N1 [15:14]		None [13:8]					

Bits	23	22	21	20	19	18	17	16
Name	PRI_N2 [23:22]		None [21:16]					

Bits	31	30	29	28	27	26	25	24
Name	PRI_N3 [31:30]		None [29:24]					

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
6:7	PRI_N0	RW	R	0	Priority of interrupt number N.
14:15	PRI_N1	RW	R	0	Priority of interrupt number N+1.
22:23	PRI_N2	RW	R	0	Priority of interrupt number N+2.
30:31	PRI_N3	RW	R	0	Priority of interrupt number N+3.

1.1.42 CM0P_CPUID

Description: CPUID Register
Address: 0xE000ED00
Offset: 0xED00
Retention: Retained
IsDeepSleep: No
Comment: Contains the part number, version, and implementation information that is specific to this processor.
Default: 0x410CC601

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name					REVISION [3:0]			

Bits	15	14	13	12	11	10	9	8
Name	PARTNO [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	VARIANT [23:20]				CONSTANT [19:16]			

Bits	31	30	29	28	27	26	25	24
Name	IMPLEMENTER [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:3	REVISION	R		1	Indicates revision. In ARM implementations this is the minor revision number n in the pn part of the rnpn revision status, see Product revision status on page xii. For release r0p1.
4:15	PARTNO	R		3168	Indicates part number, Cortex-M0+
16:19	CONSTANT	R		12	Indicates the architecture, ARMv6-M
20:23	VARIANT	R		0	Implementation defined. In ARM implementations this is the major revision number n in the rn part of the rnpn revision status, Product revision status on page xii.
24:31	IMPLEMENTER	R		65	Implementer code for ARM.

1.1.43 CM0P_ICSR

Description: Interrupt Control State Register
Address: 0xE000ED04
Offset: 0xED04
Retention: Retained
IsDeepSleep: No
Comment: Controls and provides status information for the ARMv6-M.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	VECTACTIVE [7:0]							

Bits	15	14	13	12	11	10	9	8
Name					None [11:9]			VECTACTIVE [8:8]

Bits	23	22	21	20	19	18	17	16
Name	ISRPREEMPT [23:23]	ISRPENDING [22:22]	None [21:21]	VECTPENDING [20:16]				

Bits	31	30	29	28	27	26	25	24
Name	NMIPENDSET [31:31]	None [30:29]		PENDSVSET [28:28]	PENDSVCLR [27:27]	PENDSTSETB [26:26]	PENDSTCLR [25:25]	None [24:24]

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:8	VECTACTIVE	R	RW	0	The exception number for the current executing exception. 0= Thread mode. This is the same value as IPSR[8:0]
12:20	VECTPENDING	R	RW	0	The exception number for the highest priority pending exception. 0= No pending exceptions. The pending state includes the effect of memory-mapped enable and mask registers. It does not include the PRIMASK special-purpose register qualifier.
22	ISRPENDING	R	RW	0	Indicates if an external configurable, NVIC generated, interrupt is pending.
23	ISRPREEMPT	R	RW	0	Indicates whether a pending exception will be serviced on exit from debug halt state.
25	PENDSTCLR	RW1C	R	0	Clears a pending SysTick, whether set here or by the timer hardware.
26	PENDSTSETB	RW1S	RW	0	Sets a pending SysTick or reads back the current state. Writing PENDSTSET and PENDSTCLR to '1' concurrently is UNPREDICTABLE.
27	PENDSVCLR	RW1C	R	0	Clears a pending PendSV interrupt.
28	PENDSVSET	RW1S	RW	0	Sets a pending PendSV interrupt or reads back the current state. Use this normally to request a context switch. Writing PENDSVSET and PENDSVCLR to '1' concurrently is UNPREDICTABLE.
31	NMIPENDSET	RW1S	RW	0	Activates an NMI exception or reads back the current state. Because NMI is the highest priority exception, it activates as soon as it is registered.

1.1.44 CM0P_VTOR

Description: Vector Table Offset Register
Address: 0xE000ED08
Offset: 0xED08
Retention: Retained
IsDeepSleep: No
Comment: Holds the vector table offset address
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	TBLOFF [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	TBLOFF [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	TBLOFF [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
8:31	TBLOFF	RW	R	0	Table offset address. All bits of the Vector table address that are not defined by the VTOR are zero.

1.1.45 CM0P_AIRCR

Description: Application Interrupt and Reset Control Register
Address: 0xE000ED0C
Offset: 0xED0C
Retention: Retained
IsDeepSleep: No
Comment: Sets or returns interrupt control data.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:3]					SYSRESETREQ [2:2]	VECTCLRACTIVE [1:1]	None [0:0]

Bits	15	14	13	12	11	10	9	8
Name	ENDIANNESS [15:15]	None [14:8]						

Bits	23	22	21	20	19	18	17	16
Name	VECTKEY [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	VECTKEY [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
1	VECTCLRACTIVE	RW1C	R	0	Clears all active state information for fixed and configurable exceptions. The effect of writing a 1 to this bit if the processor is not halted in Debug state is UNPREDICTABLE.
2	SYSRESETREQ	RW1S	R	0	System Reset Request. Writing 1 to this bit asserts a signal to request a reset by the external system. This will cause a full system reset of the CPU and all other components in the device. See Reset management on page B1-240 for more information.
15	ENDIANNESS	R		0	Indicates the memory system data endianness: 0 little endian 1 big endian. See Endian support on page A3-44 for more information.
16:31	VECTKEY	RW	R	X	Vector Key. The value 0x05FA must be written to this register, otherwise the register write is UNPREDICTABLE. Readback value is UNKNOWN.

1.1.46 CM0P_SCR

Description: System Control Register
Address: 0xE000ED10
Offset: 0xED10
Retention: Retained
IsDeepSleep: No
Comment: Sets or returns system control data.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:5]			SEVONPEND [4:4]	None [3:3]	SLEEPDEEP [2:2]	SLEEPONEXIT [1:1]	None [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
1	SLEEPONEXIT	RW	R	0	Determines whether, on an exit from an ISR that returns to the base level of execution priority, the processor enters a sleep state: 0 do not enter sleep state. 1 enter sleep state. See Power management on page B1-240 for more information.
2	SLEEPDEEP	RW	R	0	An implementation can use this bit to select DeepSleep/Hibernate power modes upon execution of WFI/WFE: 0: Select Sleep mode 1: Select DeepSleep/Hibernate (depends on PWR_CONTROL.HIBERNATE)
4	SEVONPEND	RW	R	0	Determines whether an interrupt transition from inactive state to pending state is a wakeup event: 0: transitions from inactive to pending are not wakeup events. 1: transitions from inactive to pending are wakeup events. See WFE on page A6-197 for more information.

1.1.47 CM0P_CCR

Description: Configuration and Control Register
Address: 0xE000ED14
Offset: 0xED14
Retention: Retained
IsDeepSleep: No
Comment: Returns configuration and control data.
Default: 0x208

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:4]				UNALIGN_TRP [3:3]	None [2:0]		

Bits	15	14	13	12	11	10	9	8
Name	None [15:10]						STKALIGN [9:9]	None [8:8]

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
3	UNALIGN_TRP	R		1	1: unaligned word and halfword accesses generate a HardFault exception.
9	STKALIGN	R		1	1: On exception entry, the SP used prior to the exception is adjusted to be 8-byte aligned and the context to restore it is saved. The SP is restored on the associated exception return.

1.1.48 CM0P_SHPR2

Description: System Handler Priority Register 2
Address: 0xE000ED1C
Offset: 0xED1C
Retention: Retained
IsDeepSleep: No
Comment: Sets or returns priority for system handler 11
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	PRI_11 [31:30]		None [29:24]					

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
30:31	PRI_11	RW	R	0	Priority of system handler 11, SVCall

1.1.49 CM0P_SHPR3

Description: System Handler Priority Register 3
Address: 0xE000ED20
Offset: 0xED20
Retention: Retained
IsDeepSleep: No
Comment: Sets or returns priority for system handlers 14-15.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	PRI_14 [23:22]		None [21:16]					

Bits	31	30	29	28	27	26	25	24
Name	PRI_15 [31:30]		None [29:24]					

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
22:23	PRI_14	RW	R	0	Priority of system handler 14, PendSV
30:31	PRI_15	RW	R	0	Priority of system handler 15, SysTick

1.1.50 CM0P_SHCSR

Description: System Handler Control and State Register
Address: 0xE000ED24
Offset: 0xED24
Retention: Retained
IsDeepSleep: No
Comment: Controls and provides the status of system handlers.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	SVCALLPENDED [15:15]	None [14:8]						

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
15	SVCALLPENDED	RW	RW	0	0 SVCall is not pending. 1 SVCall is pending. This bit reflects the pending state on a read, and updates the pending state, to the value written, on a write. (Pending state bits are set to 1 when an exception occurs, and are cleared to 0 when an exception becomes active.)

1.1.51 CM0P_DFSR

Description: Debug Fault Status Register
Address: 0xE000ED30
Offset: 0xED30
Retention: Retained
IsDeepSleep: No
Comment: Provides the top level reason why a debug event has occurred. Writing 1 to a register bit clears that bit to 0. A read of the HALTED bit by an instruction executed by stepping returns an UNKNOWN value, For more information see Debug stepping on page C1-325.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:5]			EXTERNAL [4:4]	VCATCH [3:3]	DWTTRAP [2:2]	BKPT [1:1]	HALTED [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	HALTED	RW1C	RW1S	0	Indicates a debug event generated by a C_HALT or C_STEP request, triggered by a write to the DHCSR: 0 no active halt request debug event. 1 halt request debug event active. See Debug Halting Control and Status Register, DHCSR for more information.
1	BKPT	RW1C	RW1S	0	Indicates a debug event generated by BKPT instruction execution or a breakpoint match in the BPU: 0 no breakpoint debug event. 1 at least one breakpoint debug event.
2	DWTTRAP	RW1C	RW1S	0	Indicates a debug event generated by the DWT: 0 no debug events generated by the DWT. 1 at least one debug event generated by the DWT.
3	VCATCH	RW1C	RW1S	0	Indicates whether a vector catch debug event was generated: 0 no vector catch debug event generated. 1 vector catch debug event generated. The corresponding FSR shows the primary cause of the exception.
4	EXTERNAL	RW1C	RW1S	0	Indicates an asynchronous debug event generated because of EDBGRQ being asserted: 0 no EDBGRQ debug event. 1 EDBGRQ debug event.

1.1.52 CM0P_DHCSR

Description: Debug Halting Control and Status Register
Address: 0xE000EDF0
Offset: 0xEDF0
Retention: Retained
IsDeepSleep: No
Comment: Controls halting debug. When C_DEBUGEN is set to 1, C_STEP and C_MASKINTS must not be
modified when the processor is running. Note: S_HALT is 0 when the processor is running. When C_DEBUGEN is set to 0, the processor ignores the values of all other bits in this register. For more information on the use of DHCSR, see Debug stepping on page C1-325. Note: any write to this register must have [31:16]=0xA05F - if not, the write is ignored.
Default: 0x2000000

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:4]				C_MASKINTS [3:3]	C_STEP [2:2]	C_HALT [1:1]	C_DEBUGEN [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	DBG_KEY_P1 [23:20]				S_LOCKUP [19:19]	S_SLEEP [18:18]	S_HALT [17:17]	S_REGRDY [16:16]

Bits	31	30	29	28	27	26	25	24
Name	DBG_KEY_P2 [31:26]						S_RESET_ST [25:25]	S_RETIRE_ST [24:24]

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	C_DEBUGEN	RW	R	0	Halting debug enable bit. If a debugger writes to DHCSR to change the value of this bit from 0 to 1, it must also write 0 to the C_MASKINTS bit, otherwise behavior is UNPREDICTABLE. This bit can only be written from the DAP. Access to the DHCSR from software running on the processor is IMPLEMENTATION DEFINED. However, writes to this bit from software running on the processor are ignored.
1	C_HALT	RW	R	X	Processor halt bit. The effects of writes to this bit are: 0 Request a halted processor to run. 1 Request a running processor to halt. Table C1-7 on page C1-326 shows the effect of writes to this bit when the processor is in Debug state.
2	C_STEP	RW	R	X	Processor step bit. The effects of writes to this bit are: 0 Single-stepping disabled. 1 Single-stepping enabled. For more information about the use of this bit see Table C1-7 on page C1-326.

Bits	Name	SW	HW	Default or Enum	Description
3	C_MASKINTS	RW	R	X	When debug is enabled, the debugger can write to this bit to mask PendSV, SysTick and external configurable interrupts. The effect of any attempt to change the value of this bit is UNPREDICTABLE unless both: - before the write to DHCSR, the value of the C_HALT bit is 1 - the write to the DHCSR that changes the C_MASKINTS bit also writes 1 to the C_HALT bit This means that a single write to DHCSR cannot set the C_HALT to 0 and change the value of the C_MASKINTS bit. The bit does not affect NMI. When DHCSR.C_DEBUGEN is set to 0, the value of this bit is UNKNOWN. For more information about the use of this bit see Table C1-7 on page C1-326.
16	S_REGRDY	R	RW	X	A handshake flag for transfers through the DCRDR: - Writing to DCRSR clears the bit to 0. - Completion of the DCRDR transfer then sets the bit to 1. For more information about DCRDR transfers see Debug Core Register Data Register, DCRDR on page C1-337. 0: There has been a write to the DCRDR, but the transfer is not complete. 1: The transfer to or from the DCRDR is complete. This bit is only valid when the processor is in Debug state, otherwise the bit is UNKNOWN.
17	S_HALT	R	RW	0	Indicates whether the processor is in Debug state.
18	S_SLEEP	R	RW	0	Indicates whether the processor is sleeping. The debugger must set the DHCSR.C_HALT bit to 1 to gain control, or wait for an interrupt or other wakeup event to wakeup the system.
19	S_LOCKUP	R	RW	0	Indicates whether the processor is locked up because of an unrecoverable exception. See Unrecoverable exception cases on page B1-238 for more information. This bit can only read as 1 when accessed by a remote debugger using the DAP. The bit clears to 0 when the processor enters Debug state.
20:23	DBG_KEY_P1	W	R	X	Debug key: Software must write 0xA05F to [31:16] to enable write accesses to bits [15:0], otherwise the processor ignores the write access.
24	S_RETIRE_ST	R	RW	X	When not in Debug state, indicates whether the processor has completed execution of at least one instruction since the last read of DHCSR. This is a sticky bit, that clears to 0 on a read of DHCSR. This bit is UNKNOWN: - after a Local reset, but is set to 1 as soon as the processor completes execution of an instruction - when S_LOCKUP is set to 1 - when S_HALT is set to 1. When the processor is not in Debug state, a debugger can check this bit to determine if the processor is stalled on a load, store or fetch access.
25	S_RESET_ST	R	RW	1	Indicates whether the processor has been reset since the last read of DHCSR. This is a sticky bit, that clears to 0 on a read of DHCSR
26:31	DBG_KEY_P2	W	R	X	See description for Bit 20

1.1.53 CM0P_DCRSR

Description: Debug Core Register Selector Register
Address: 0xE000EDF4
Offset: 0xEDF4
Retention: Retained
IsDeepSleep: No
Comment: With the DCRDR, see Debug Core Register Data Register, DCRDR on page C1-337, the DCRSR provides debug access to the ARM core registers and special-purpose registers. A write to DCRSR specifies the register to transfer, whether the transfer is a read or a write, and starts the transfer. This register is only accessible in Debug state. When the processor is in Debug state, the debugger must preserve the Exception number bits in the IPSR, otherwise behavior is UNPREDICTABLE
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:5]			REGSEL [4:0]				

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:17]							REGWNR [16:16]

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:4	REGSEL	RW	R	X	Specifies the ARM core register or special-purpose register to transfer.
	R0			0	CPU R0
	R1			1	CPU R1
	R2			2	CPU R2
	R3			3	CPU R3
	R4			4	CPU R4
	R5			5	CPU R5
	R6			6	CPU R6
	R7			7	CPU R7
	R8			8	CPU R8
	R9			9	CPU R9
	R10			10	CPU R10
	R11			11	CPU R11
	R12			12	CPU R12
	SP			13	Current Stack Pointer
	LR			14	CPU LR
	DBG_RA			15	DebugReturnAddress: the address of the first instruction to be executed on exit from Debug state.
	XPSR			16	xPSR
	MSP			17	Main stack pointer, MSP.
	PSP			18	Process stack pointer, PSP
	C_P			20	[31:24]: CONTROL [7:0]: PRIMASK.
16	REGWNR	RW	R	X	Specifies the type of access for the transfer.
	READ			0	Read transfer

Bits	Name	SW	HW	Default or Enum	Description
	WRITE			1	Write transfer

1.1.54 CM0P_DCRDR

Description: Debug Core Register Data Register
Address: 0xE000EDF8
Offset: 0xEDF8
Retention: Retained
IsDeepSleep: No
Comment: With the DCRSR, see Debug Core Register Selector Register, DCRSR on page C1-335, the DCRDR provides debug access to the ARM core registers and special-purpose registers. The DCRDR is the data register for these accesses.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	DBGTMP [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	DBGTMP [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	DBGTMP [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	DBGTMP [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	DBGTMP	RW	RW	X	Data temporary cache, for reading and writing CPU registers. This register is UNKNOWN: - on reset - when DHCSR.S_HALT = 0. - when DHCSR.S_REGRDY = 0 during execution of a DCRSR based transaction that updates the register

1.1.55 CM0P_DEMCR

Description: Debug Exception and Monitor Control Register
Address: 0xE000EDFC
Offset: 0xEDFC
Retention: Retained
IsDeepSleep: No
Comment: Manages vector catch behavior and enables the DWT.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:1]							VC_CORERESET [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:11]					VC_HARDERR [10:10]	None [9:8]	

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:25]							DWTENA [24:24]

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	VC_CORERESET	RW	R	0	Enable Reset Vector Catch. This causes a Local reset to halt a running system. If DHCSR.C_DEBUGEN is set to 0, the processor ignores the value of this bit.
10	VC_HARDERR	RW	R	0	Enable halting debug trap on a HardFault exception. If DHCSR.C_DEBUGEN is set to 0, the processor ignores the value of this bit.
24	DWTENA	RW	R	0	Global enable for all features configured and controlled by the DWT unit. When DWTENA is set to 0 DWT registers return UNKNOWN values on reads. In addition, it is IMPLEMENTATION DEFINED whether the processor ignores writes to the DWT while DWTENA is 0.

1.1.56 CM0P_SCS_PID4

Description: System Control Space ROM Table Peripheral ID #4
Address: 0xE000EFD0
Offset: 0xEFD0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x4

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	VALUE [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	VALUE	R		4	Peripheral ID #4

1.1.57 CM0P_SCS_PID0

Description: System Control Space ROM Table Peripheral ID #0
Address: 0xE000EFE0
Offset: 0xEFE0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x8

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	VALUE [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	VALUE	R		8	Peripheral ID #0

1.1.58 CM0P_SCS_PID1

Description: System Control Space ROM Table Peripheral ID #1
Address: 0xE000EFE4
Offset: 0xEFE4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xB0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	VALUE [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	VALUE	R		176	Peripheral ID #1

1.1.59 CM0P_SCS_PID2

Description: System Control Space ROM Table Peripheral ID #2
Address: 0xE000EFE8
Offset: 0xEFE8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xB

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	VALUE [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	VALUE	R		11	Peripheral ID #2

1.1.60 CM0P_SCS_PID3

Description: System Control Space ROM Table Peripheral ID #3
Address: 0xE000EFEC
Offset: 0xEFEC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	VALUE [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	VALUE	R		0	Peripheral ID #3

1.1.61 CM0P_SCS_CID0

Description: System Control Space ROM Table Component ID #0
Address: 0xE000EFF0
Offset: 0xEFF0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xD

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	VALUE [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	VALUE	R		13	Component ID #0

1.1.62 CM0P_SCS_CID1

Description: System Control Space ROM Table Component ID #1
Address: 0xE000EFF4
Offset: 0xEFF4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xE0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	VALUE [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	VALUE	R		224	Component ID #1

1.1.63 CM0P_SCS_CID2

Description: System Control Space ROM Table Component ID #2
Address: 0xE000EFF8
Offset: 0xEFF8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x5

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	VALUE [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	VALUE	R		5	Component ID #2

1.1.64 CM0P_SCS_CID3

Description: System Control Space ROM Table Component ID #3
Address: 0xE000EFFC
Offset: 0xEFFC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xB1

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	VALUE [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	VALUE	R		177	Component ID #3

1.1.65 CM0P_ROM_SCS

Description: CM0+ CoreSight ROM Table Peripheral #0
Address: 0xE00FF000
Offset: 0xFF000
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xFFF0F003

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	VALUE [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	VALUE	R		4293980163	Offset to SCS ROM Table

1.1.66 CM0P_ROM_DWT

Description: CM0+ CoreSight ROM Table Peripheral #1
Address: 0xE00FF004
Offset: 0xFF004
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xFFF02003

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	VALUE [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	VALUE	R		4293926915	Offset to DWT ROM Table

1.1.67 CM0P_ROM_BPU

Description: CM0+ CoreSight ROM Table Peripheral #2
Address: 0xE00FF008
Offset: 0xFF008
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xFFF03003

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	VALUE [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	VALUE	R		4293931011	Offset to BPU ROM Table

1.1.68 CM0P_ROM_END

Description: CM0+ CoreSight ROM Table End Marker
Address: 0xE00FF00C
Offset: 0xFF00C
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	VALUE [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	VALUE	R		0	End marker in peripheral list

1.1.69 CM0P_ROM_CSMT

Description: CM0+ CoreSight ROM Table Memory Type
Address: 0xE00FFFCC
Offset: 0xFFFCC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x1

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	VALUE [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	VALUE	R		1	Memory Type

1.1.70 CM0P_ROM_PID4

Description: CM0+ CoreSight ROM Table Peripheral ID #4
Address: 0xE00FFFD0
Offset: 0xFFFD0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x4

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	VALUE [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	VALUE	R		4	Peripheral ID #4

1.1.71 CM0P_ROM_PID0

Description: CM0+ CoreSight ROM Table Peripheral ID #0
Address: 0xE00FFFE0
Offset: 0xFFFE0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xC0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	VALUE [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	VALUE	R		192	Peripheral ID #0

1.1.72 CM0P_ROM_PID1

Description: CM0+ CoreSight ROM Table Peripheral ID #1
Address: 0xE00FFFE4
Offset: 0xFFFE4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xB4

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	VALUE [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	VALUE	R		180	Peripheral ID #1

1.1.73 CM0P_ROM_PID2

Description: CM0+ CoreSight ROM Table Peripheral ID #2
Address: 0xE00FFFE8
Offset: 0xFFFE8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xB

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	VALUE [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	VALUE	R		11	Peripheral ID #2

1.1.74 CM0P_ROM_PID3

Description: CM0+ CoreSight ROM Table Peripheral ID #3
Address: 0xE00FFFEC
Offset: 0xFFFEC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	VALUE [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	VALUE	R		0	Peripheral ID #3

1.1.75 CM0P_ROM_CID0

Description: CM0+ CoreSight ROM Table Component ID #0
Address: 0xE00FFFF0
Offset: 0xFFFF0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xD

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	VALUE [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	VALUE	R		13	Component ID #0

1.1.76 CM0P_ROM_CID1

Description: CM0+ CoreSight ROM Table Component ID #1
Address: 0xE00FFFF4
Offset: 0xFFFF4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x10

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	VALUE [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	VALUE	R		16	Component ID #1

1.1.77 CM0P_ROM_CID2

Description: CM0+ CoreSight ROM Table Component ID #2
Address: 0xE00FFFF8
Offset: 0xFFFF8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x5

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	VALUE [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	VALUE	R		5	Component ID #2

1.1.78 CM0P_ROM_CID3

Description: CM0+ CoreSight ROM Table Component ID #3
Address: 0xE00FFFFC
Offset: 0xFFFFC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xB1

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	VALUE [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	VALUE	R		177	Component ID #3

2 CPUSS

Description CPU Subsystem
Base Address 0x40100000
Size 0x1000
Slave Num CPUMEMSSV3_VER3

Register Name	Address	Permission	Description
CPUSS_SYSREQ	0x40100004	FULL	SYSCALL control register
CPUSS_SYSARG	0x40100008	FULL	SYSARG control register
CPUSS_FLASH_CTL	0x40100030	FULL	FLASH control register
CPUSS_ROM_CTL	0x40100034	FULL	ROM control register Note:ARB is not available for this register
CPUSS_RAM_CTL	0x40100038	FULL	RAM control register
CPUSS_DMAC_CTL	0x4010003C	FULL	DMA controller register
CPUSS_FAULT_CTL	0x401000AC	FULL	Fault Control Register
CPUSS_RAM_STATUS	0x401000D0	FULL	RAM Controller 0 Status
CPUSS_BOOT_RESULT_0	0x401000E0	FULL	Boot Result Register 0
CPUSS_BOOT_RESULT_1	0x401000E4	FULL	Boot Result Register 1
CPUSS_SL_CTL0	0x40100100	FULL	Slave control register
CPUSS_SL_CTL1	0x40100104	FULL	Slave control register
CPUSS_SL_CTL2	0x40100108	FULL	Slave control register
CPUSS_RAM_ECC_STATUS0	0x40100200	FULL	RAM ECC Status 0
CPUSS_RAM_ECC_STATUS1	0x40100204	FULL	RAM ECC Status 1
CPUSS_ECC_TEST	0x40100210	FULL	ECC Test
CPUSS_FLASHC_BERR_STATUS	0x40100500	FULL	Flash Bus Error Status
CPUSS_FLASHC_ECC_CTL	0x40100508	FULL	Flash ECC Control

2.1 Register Details

2.1.1 CPUSS_SYSREQ

Description: SYSCALL control register
Address: 0x40100004
Offset: 0x4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x30000000

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	SYSCALL_COMMAND [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	SYSCALL_COMMAND [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	SYSCALL_REQ [31:31]	HMASTER_0 [30:30]	ROM_ACCESS_EN [29:29]	PRIVILEGED [28:28]	DIS_RESET_VECT_REL [27:27]	EXTERNAL_SYS_REQ [26:26]	None [25:24]	

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:15	SYSCALL_COMMAND	RW		0	Opcode of the system call being requested.
26	EXTERNAL_SYS_REQ	RW1C	RW1S	0	External HW SYS REQ. This bit is set by HW to cause a SYSCALL to BOOTROM. This bit may only be cleared by SW. When this bit is set, the SYSCALL_COMMAND, PRIVILEDGED, HMASTER0, and SYSCALL_ARG content are invalid.
27	DIS_RESET_VECT_REL	RW	R	0	Disable Reset Vector fetch relocation: '0': CPU accesses to locations 0x0000:0000 - 0x0000:0007 are redirected to ROM. '1': CPU accesses to locations 0x0000:0000 - 0x0000:0007 are made to flash. Note that this field defaults to '0' on reset, ensuring actual reset vector fetches are always made to ROM. Note that this field does not affect DAP accesses. Flash DfT routines may set this bit to '1' to enable uninhibited read-back of programmed data in the first flash page.
28	PRIVILEGED	RW	A	1	Indicates whether the system is in privileged ('1') or user mode ('0'). Only CPU SW executing from ROM can set this field to '1' when ROM_ACCESS_EN is '1' (the CPU is executing a SystemCall NMI interrupt handler). Any other write to this field sets is to '0'. This field is used as the AHB-Lite hprot[1] signal to implement Cypress proprietary user/privileged modes. These modes are used to enable/disable access to specific MMIO registers and memory regions.

Bits	Name	SW	HW	Default or Enum	Description
29	ROM_ACCESS_EN	R	RW	1	Indicates that executing from Boot ROM is enabled. HW sets this field to '1', on reset or when the SystemCall NMI vector is fetched from Boot ROM. HW sets this field to '0', when the CPU is NOT executing from either Boot or System ROM. This bit is used for debug purposes only.
30	HMASTER_0	R	W	0	Indicates the source of the write access to the SYSREQ register. '0': CPU write access. '1': DAP write access. For a SW write to the SYSREQ register, the HW will update this field based on the value of SYSCALL_REQ. SYSCALL_REQ = 0 : the current source of write access is captured. SYSCALL_REQ = 1 : the previous value (captured when SYSCALL_REQ was 0), is retained/maintained until the next SW write to this register.
31	SYSCALL_REQ	RW	R	0	CPU/DAP writes a '1' to this field to request a SystemCall. The HMASTER_0 field indicates the source of the write access. Setting this field to '1' immediate results in a NMI. The SystemCall NMI interrupt handler sets this field to '0' after servicing the request.

2.1.2 CPUSS_SYSARG

Description: SYSARG control register
Address: 0x40100008
Offset: 0x8
Retention: Retained
IsDeepSleep: No
Comment: Used to make system requests to SROM code. System Requests transition from User Mode to Privileged Mode. See SAS for more details. Firmware/ATE should write CPUSS_SYSARG first and CPUSS_SYSREQ register next.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	SYSCALL_ARG [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	SYSCALL_ARG [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	SYSCALL_ARG [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	SYSCALL_ARG [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	SYSCALL_ARG	RW		0	Argument to System Call specified in SYSREQ. Semantics of argument depends on system call made. Typically a pointer to a parameter block.

2.1.3 CPUSS_FLASH_CTL

Description: FLASH control register
Address: 0x40100030
Offset: 0x30
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:5]			PREF_EN [4:4]	FLASH_WS [3:0]			

Bits	15	14	13	12	11	10	9	8
Name	None [15:9]							FLASH_INVALIDATE [8:8]

Bits	23	22	21	20	19	18	17	16
Name	None [23:22]		FLASH_ERR_SILENT [21:21]	FLASH_ECC_INJ_EN [20:20]	None [19:18]		ARB [17:16]	

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:3	FLASH_WS	RW	R	0	For Flash With ECC the number of wait states (WS): WS = 3 for SYSCLK <= FMAX WS = 2 for SYSCLK <= 3/4 * FMAX WS = 1 for SYSCLK <= 1/2 * FMAX WS = 0 for SYSCLK <= 1/4 * FMAX 4-15 : Future Use - To be used, if 3 Wait State is not sufficient.
4	PREF_EN	RW	R	0	Prefetch enable: '0': disabled. This is a desirable setting when FLASH_WS is 0 or when predictable execution time is required. '1': enabled.
8	FLASH_INVALIDATE	RW	RW1C	0	1': Invalidates the content of the flash controller's buffers.
16:17	ARB	RW	R	0	Arbitration policy: 0: CPU has priority 1: DW/DMA has priority 2: Roundrobin 3: Roundrobin - sticky
20	FLASH_ECC_INJ_EN	RW	R	0	Enable error injection for FLASH main interface. When'1', the parity (ECC_CTL.PARITY[7:0]) is used for a load from the ECC_CTL.WORD_ADDR[23:0] word address.

Bits	Name	SW	HW	Default or Enum	Description
21	FLASH_ERR_SILENT	RW	R	0	Specifies bus transfer behavior for a non-recoverable error on the FLASH macro main interface (either a non-correctable ECC error, a FLASH macro main interface internal error, a FLASH macro main interface memory hole access, a M0S8 protection violation error): 0: Bus transfer has a bus error. 1: Bus transfer does NOT have a bus error; i.e. the error is 'silent' In either case, a Zero value is returned. This field is ONLY used by CPU bus transfers. Non-CPU bus transfers always have a bus transfer with a bus error, in case of a non-recoverable error.

2.1.4 CPUSS_ROM_CTL

Description: ROM control register
Address: 0x40100034
Offset: 0x34
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:1]							ROM_WS [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	ROM_WS	RW	R	0	Amount of ROM wait states: '0': 0 wait states. Use this setting for newer, faster ROM design. Use this setting for older, slower ROM design and frequencies in the range [0, 24] MHz. '1': 1 wait state. Use this setting for older, slower ROM design and frequencies in the range <24, 48] MHz. Should always be set to 0.

2.1.5 CPUSS_RAM_CTL

Description: RAM control register
Address: 0x40100038
Offset: 0x38
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:7]	ECC_BIST_SWITCH [6:6]	None [5:5]	ECC_INJ_EN [4:4]	None [3:3]	ECC_AUTO_CORRECT [2:2]	None [1:1]	ECC_ENABLE [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:18]						ARB [17:16]	

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	ECC_ENABLE	RW	R	1	Enable ECC operation: '0': ECC Disabled - ECC is not generated/checked '1': ECC Enabled - ECC is generated/checked
2	ECC_AUTO_CORRECT	RW	R	1	HW ECC autocorrect functionality: '0': Disabled. '1': Enabled. HW automatically writes back SRAM with corrected data when a recoverable ECC error is detected.
4	ECC_INJ_EN	RW	R	0	Enable error injection. 0: Syndrome is source from ECC Syndrome hardware. 1: ECC_TEST.SYND_DATA is used when a full 32-bit write is done to the ECC_TEST.WORD_ADDR word address of SRAM0.
6	ECC_BIST_SWITCH	RW	R	0	ECC_BIST_SWITCH: Substitutes Syndrome bits for normal data path during BIST testing. Data bits 31:25 on the SRAM data path both to and from the SRAM are replaced with the SRAM Syndrome data bits 38:32 during BIST testing when this bit is set to 1. '0': Source normal datapath to BIST bus '1': Source Syndrome bits to BIST bus
16:17	ARB	RW	R	0	Arbitration Policy: '0': CPU has priority '1': DW/DMA has priority '2': Roundrobin '3': Roundrobin - sticky

2.1.6 CPUSS_DMAC_CTL

Description: DMA controller register
Address: 0x4010003C
Offset: 0x3C
Retention: Retained
IsDeepSleep: No
Comment: Arbitration control for the DMA controller AHB-Lite slave interface
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:18]						ARB [17:16]	

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
16:17	ARB	RW	R	0	Arbitration policy: 0: CPU has priority 1: DW/DMA has priority 2: Roundrobin 3: Roundrobin - sticky

2.1.7 CPUSS_FAULT_CTL

Description: Fault Control Register
Address: 0x401000AC
Offset: 0xAC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:18]						ARB [17:16]	

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
16:17	ARB	RW	R	0	Arbitration policy: 0: CPU has priority 1: DW/DMA has priority 2: Roundrobin 3: Roundrobin - sticky

2.1.8 CPUSS_RAM_STATUS

Description: RAM Controller 0 Status
Address: 0x401000D0
Offset: 0xD0
Retention: Retained
IsDeepSleep: No
Comment: This register is for the CPUSS system SRAM controller 0.
Default: 0x1

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:1]							WB _EMPTY [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	WB_EMPTY	R	W	1	Write buffer empty. This information is used when entering DeepSleep power mode: WB_EMPTY must be '1' before a transition to system DeepSleep power mode. '0': Write buffer NOT empty. '1': Write buffer empty. Note: the SRAM controller write buffer is only used when ECC checking is enabled. (RAMi_CTL.ECC_EN is '1').

2.1.9 CPUSS_BOOT_RESULT_0

Description: Boot Result Register 0
Address: 0x401000E0
Offset: 0xE0
Retention: Not Retained
IsDeepSleep: No
Comment: This register contains details of any results from the Boot Process
Default: 0x1

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	BOOT_RESULT [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	BOOT_RESULT [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	BOOT_RESULT [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	BOOT_RESULT [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	BOOT_RESULT	RW		1	Record details of Boot Process.

2.1.10 CPUSS_BOOT_RESULT_1

Description: Boot Result Register 1
Address: 0x401000E4
Offset: 0xE4
Retention: Not Retained
IsDeepSleep: No
Comment: This register contains details of any results from the Boot Process
Default: 0x1

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	BOOT_RESULT [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	BOOT_RESULT [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	BOOT_RESULT [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	BOOT_RESULT [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	BOOT_RESULT	RW		1	Record details of Boot Process.

2.1.11 CPUSS_SL_CTL

Description: Slave control register
Address: 0x40100100
Offset: 0x100
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:18]						ARB [17:16]	

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
16:17	ARB	RW	R	0	Arbitration policy: 0: CPU priority 1: DMA priority 2: Roundrobin 3: Roundrobin - sticky

2.1.12 CPUSS_RAM_ECC_STATUS0

Description: RAM ECC Status 0
Address: 0x40100200
Offset: 0x200
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	ECC_CAPTURE_ADDR_31_2 [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	ECC_CAPTURE_ADDR_31_2 [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	ECC_CAPTURE_ADDR_31_2 [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	ECC_CAPTURE_ADDR_SYNDROME_VALID [31:31]	None [30:30]	ECC_CAPTURE_ADDR_31_2 [29:24]					

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:29	ECC_CAPTURE_ADDR_31_2	R	RW	Undefined	Snapshot of CPUSS Address which caused the first correctable/un-correctable error interrupt. When first correctable/un-correctable error interrupt is generated, ECC_CAPTURE_ADDR_SYNDROME_VALID is transitioned from 0 to 1 , and this registered captures the first error address. The register only captures bits 31-2 of the address.
31	ECC_CAPTURE_ADDR_SYNDROME_VALID	RW1C	RW1S	0	ECC Capture address and Syndrome valid. 0: ECC_CAPTURE_ADDR_31_2 not valid 1: ECC_CAPTURE_ADDR_31_2 valid - SW writes a 1 to clear

2.1.13 CPUSS_RAM_ECC_STATUS1

Description: RAM ECC Status 1
Address: 0x40100204
Offset: 0x204
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:7]	ECC_CAPTURE_SYNDROME [6:0]						

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:6	ECC_CAPTURE_SYNDROME	R	RW	Undefined	Snapshot of CPUSS Syndrome which caused the first correctable/un-correctable error interrupt. When first correctable/un-correctable error interrupt is generated, ECC_CAPTURE_ADDR_SYNDROME_VALID is transitioned from 0 to 1 , and this registered captures the first Syndrome corresponding to the Error.

2.1.14 CPUSS_ECC_TEST

Description: ECC Test
Address: 0x40100210
Offset: 0x210
Retention: Retained
IsDeepSleep: No
Comment: Register defines the address and supplies the Syndrome for ECC Testing
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	WORD_ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	WORD_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	WORD_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	SYND_DATA [31:25]							WORD_ADDR [24:24]

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:24	WORD_ADDR	RW	R	0	Specifies the word address where an error will be injected. - For SRAMs, the word address WORD_ADDR[24:0] is the device address A[26:2]. On a write transfer to this SRAM address and when the corresponding RAM_CTL.ECC_INJ_EN or RAM1_CTL.ECC_INJ_EN bit is '1', the parity (SYND_DATA[6:0]) is injected into the corresponding SRAM location.
25:31	SYND_DATA	RW	R	0	ECC syndrome to use for error injection at address WORD_ADDR.

2.1.15 CPUSS_FLASHC_BERR_STATUS

Description: Flash Bus Error Status
Address: 0x40100500
Offset: 0x500
Retention: Retained
IsDeepSleep: No
Comment: Reports Bus Error Causes for Flash bus transactions
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:4]				FLASH_PROT_VIO [3:3]	FLASH_MEMORY_HOLE [2:2]	FLASH_UNCORRECTABLE [1:1]	INTERNAL_ERROR [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	INTERNAL_ERROR	RW1C	W1S	0	Specifies/registers the occurrence of a FLASH macro interface internal error (typically the result of a read access while a program erase operation is ongoing) as a result of a CM0+ access. SW clears this field to '0'. HW sets this field to '1' on a FLASH macro interface internal error. Typically, SW reads this field after a code section to detect the occurrence of an error. Note: this field is independent of FLASH_CTL.FLASH_ERR_SILENT.
1	FLASH_UNCORRECTABLE	RW1C	W1S	0	An Uncorrectable Read error occurred when accessing a Flash Macro. SW clears this field to '0'. HW sets this field to '1' on a FLASH macro uncorrectable error. Typically, SW reads this field after a code section to detect the occurrence of an error. Note: this field is independent of FLASH_CTL.FLASH_ERR_SILENT.
2	FLASH_MEMORY_HOLE	RW1C	W1S	0	An access to a non-existent Flash Address occurred. SW clears this field to '0'. HW sets this field to '1' on a FLASH macro access to a non-existent address. Typically, SW reads this field after a code section to detect the occurrence of an error. Note: this field is independent of FLASH_CTL.FLASH_ERR_SILENT.

Bits	Name	SW	HW	Default or Enum	Description
3	FLASH_PROT_VIO	RW1C	W1S	0	A protection violation occurred in Flash Controller. SW clears this field to '0'. HW sets this field to '1' on a protection violation occurred in Flash Controllers. Typically, SW reads this field after a code section to detect the occurrence of an error. Note: this field is independent of FLASH_CTL.FLASH_ERR_SILENT.

2.1.16 CPUSS_FLASHC_ECC_CTL

Description: Flash ECC Control
Address: 0x40100508
Offset: 0x508
Retention: Retained
IsDeepSleep: No
Comment: Note that for cache SRAM and FLASH work interface ECC, the word address is for a 32-bit word. For FLASH main interface ECC, the word address is for a 64-bit word.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	FLASH_WORD_ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	FLASH_WORD_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	FLASH_WORD_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	PARITY [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:23	FLASH_WORD_ADDR	RW	R	0	Specifies the word address where an error will be injected. - For FLASH interface ECC, the word address WORD_ADDR[23:0] is device address A[26:3]. On a FLASH main interface read and when FLASH_CTL.MAIN_ECC_INJ_EN bit is '1', the parity (PARITY[7:0]) replaces the FLASH macro parity (FLASH main interface read path is manipulated).
24:31	PARITY	RW	R	0	ECC parity to use for ECC error injection at address WORD_ADDR. - For FLASH interface ECC, the 8-bit parity PARITY[7:0] is for a 64-bit word.

3 CXPI

Description CXPI
Base Address 0x402E0000
Size 0x10000
Slave Num MMIO1

Register Name	Address	Permission	Description
CXPI0_ERROR_CTL	0x402E0000	FULL	Error control
CXPI0_TEST_CTL	0x402E0004	FULL	Test control

3.1 CH 0

Register Name	Address	Permission	Description
CXPI0_CH0_CTL0	0x402E8000	FULL	Control 0
CXPI0_CH0_CTL1	0x402E8004	FULL	Control 1
CXPI0_CH0_CTL2	0x402E8008	FULL	Control 2
CXPI0_CH0_STATUS	0x402E800C	FULL	Status
CXPI0_CH0_CMD	0x402E8010	FULL	Command
CXPI0_CH0_TX_RX_STATUS	0x402E8040	FULL	TX/RX status
CXPI0_CH0_TXPID_FI	0x402E8050	FULL	TXPID and Frame Information
CXPI0_CH0_RXPID_FI	0x402E8054	FULL	RXPID and Frame Information
CXPI0_CH0_CRC	0x402E8058	FULL	CRC
CXPI0_CH0_TX_FIFO_CTL	0x402E8080	FULL	TX FIFO control
CXPI0_CH0_TX_FIFO_STATUS	0x402E8084	FULL	TX FIFO status
CXPI0_CH0_TX_FIFO_WR	0x402E8088	FULL	TX FIFO write
CXPI0_CH0_RX_FIFO_CTL	0x402E80A0	FULL	RX FIFO control
CXPI0_CH0_RX_FIFO_STATUS	0x402E80A4	FULL	RX FIFO status
CXPI0_CH0_RX_FIFO_RD	0x402E80A8	FULL	RX FIFO read
CXPI0_CH0_RX_FIFO_RD_SILENT	0x402E80AC	FULL	RX FIFO silent read
CXPI0_CH0_INTR	0x402E80C0	FULL	Interrupt
CXPI0_CH0_INTR_SET	0x402E80C4	FULL	Interrupt set
CXPI0_CH0_INTR_MASK	0x402E80C8	FULL	Interrupt mask
CXPI0_CH0_INTR_MASKED	0x402E80CC	FULL	Interrupt masked

3.2 CH 1

Register Name	Address	Permission	Description
CXPI0_CH1_CTL0	0x402E8100	FULL	Control 0
CXPI0_CH1_CTL1	0x402E8104	FULL	Control 1
CXPI0_CH1_CTL2	0x402E8108	FULL	Control 2
CXPI0_CH1_STATUS	0x402E810C	FULL	Status
CXPI0_CH1_CMD	0x402E8110	FULL	Command
CXPI0_CH1_TX_RX_STATUS	0x402E8140	FULL	TX/RX status
CXPI0_CH1_TXPID_FI	0x402E8150	FULL	TXPID and Frame Information
CXPI0_CH1_RXPID_FI	0x402E8154	FULL	RXPID and Frame Information
CXPI0_CH1_CRC	0x402E8158	FULL	CRC
CXPI0_CH1_TX_FIFO_CTL	0x402E8180	FULL	TX FIFO control
CXPI0_CH1_TX_FIFO_STATUS	0x402E8184	FULL	TX FIFO status
CXPI0_CH1_TX_FIFO_WR	0x402E8188	FULL	TX FIFO write
CXPI0_CH1_RX_FIFO_CTL	0x402E81A0	FULL	RX FIFO control
CXPI0_CH1_RX_FIFO_STATUS	0x402E81A4	FULL	RX FIFO status
CXPI0_CH1_RX_FIFO_RD	0x402E81A8	FULL	RX FIFO read
CXPI0_CH1_RX_FIFO_RD_SILENT	0x402E81AC	FULL	RX FIFO silent read
CXPI0_CH1_INTR	0x402E81C0	FULL	Interrupt
CXPI0_CH1_INTR_SET	0x402E81C4	FULL	Interrupt set
CXPI0_CH1_INTR_MASK	0x402E81C8	FULL	Interrupt mask
CXPI0_CH1_INTR_MASKED	0x402E81CC	FULL	Interrupt masked

3.3 Register Details

3.3.1 CXPI_ERROR_CTL

Description: Error control
Address: 0x402E0000
Offset: 0x0
Retention: Retained
IsDeepSleep: No
Comment: This register supports error functionality: it enables HW injected channel transmitter errors. The receiver should detect these errors and report these errors through activation of corresponding interrupt causes.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:5]			CH_IDX [4:0]				

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:21]			TX_DATA_LENGTH_ERROR [20:20]	TX_PID_PARITY_ERROR [19:19]	TX_CRC_ERROR [18:18]	None [17:16]	

Bits	31	30	29	28	27	26	25	24
Name	ENABLED [31:31]	None [30:26]					TX_DATA_STOP_ERROR [25:25]	None [24:24]

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:4	CH_IDX	RW	R	0	Specifies the channel index of the channel to which HW injected channel transmitter errors applies.
18	TX_CRC_ERROR	RW	R	0	The crc field is inverted. At the receiver, this should result in INTR.RX_CRC_ERROR activation.
19	TX_PID_PARITY_ERROR	RW	R	0	In cxpi mode, the PID parity bit P[1] is inverted from !(ID[5] ^ ID[4] ^ ID[3] ^ ID[1]) to (ID[5] ^ ID[4] ^ ID[3] ^ ID[1]). At the receiver, this should result in INTR.RX_HEADER_PARITY_ERROR activation.
20	TX_DATA_LENGTH_ERROR	RW	R	0	The transmitter continues to send logical '0' (during IFS) after CRC field is transmitted. At the receiver, this should result in INTR.RX_DATA_LENGTH_ERROR activation. At the transmitter, this should result in INTR.TX_DATA_LENGTH_ERROR activation.
25	TX_DATA_STOP_ERROR	RW	R	0	The data field STOP bits are inverted to '0'. At the receiver, this should result in INTR.RX_FRAME_ERROR activation. At the transmitter, this should result in INTR.TX_FRAME_ERROR activation.

Bits	Name	SW	HW	Default or Enum	Description
31	ENABLED	RW	R	0	Error injection enable: '0': Disabled. '1': Enabled.

3.3.2 CXPI_TEST_CTL

Description: Test control
Address: 0x402E0004
Offset: 0x4
Retention: Retained
IsDeepSleep: No
Comment: This register support test functionality.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:5]			CH_IDX [4:0]				

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:17]							MODE [16:16]

Bits	31	30	29	28	27	26	25	24
Name	ENABLED [31:31]	None [30:24]						

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:4	CH_IDX	RW	R	0	Specifies the channel index of the channel to which test applies. The channel IO signals of channel indices CH_IDX and CH_NR-1 are connected as specified by MODE. CH_IDX should be in the range [0, CH_NR-2], as channel index CH_NR-1 is always involved in test and cannot be connected to itself. The test mode allows BOTH of the two connected channels to be tested. Note: this testing functionality simplifies SW development, but may also be used in the field to verify correct channel functionality.

Bits	Name	SW	HW	Default or Enum	Description
16	MODE	RW	R	0	Test mode: '0': Partial disconnect from IOSS. This mode's isolation allows for device test without relying on an external cxpi transceiver. The IOSS 'tx' IO cell can be used to observe messages outside of the device. - tx_in[CH_IDX] = IOSS cxpi_tx_in[CH_IDX]. - tx_in[CH_NR-1] = IOSS cxpi_tx_in[CH_IDX]. - rx_in[CH_IDX] = IOSS cxpi_tx_in[CH_IDX]. - rx_in[CH_NR-1] = IOSS cxpi_tx_in[CH_IDX]. - cxpi_tx_out[CH_IDX] = tx_out[CH_IDX] & tx_out[CH_NR-1]. - cxpi_tx_out[CH_NR-1] = tx_out[CH_IDX] & tx_out[CH_NR-1]. '1': Full disconnect from IOSS (the IOSS/HSIOM should disconnect 'tx_out' from the 'tx' IO cell). This mode's isolation allows for device test without effecting an operational cxpi cluster. - tx_in[CH_IDX] = cxpi_tx_out[CH_IDX]. - tx_in[CH_NR-1] = cxpi_tx_out[CH_IDX]. - rx_in[CH_IDX] = cxpi_tx_out[CH_IDX]. - rx_in[CH_NR-1] = cxpi_tx_out[CH_IDX]. - cxpi_tx_out[CH_IDX] = tx_out[CH_IDX] & tx_out[CH_NR-1]. - cxpi_tx_out[CH_NR-1] = tx_out[CH_IDX] & tx_out[CH_NR-1].
	PARTIAL_DISCONNECT			0	Partial disconnect
	FULL_DISCONNECT			1	Full disconnect
31	ENABLED	RW	R	0	Test enable: '0': Disabled. Functional mode. - tx_in[CH_IDX] = IOSS cxpi_tx_in[CH_IDX]. - tx_in[CH_NR-1] = IOSS cxpi_tx_in[CH_NR-1]. - rx_in[CH_IDX] = IOSS cxpi_rx_in[CH_IDX]. - rx_in[CH_NR-1] = IOSS cxpi_rx_in[CH_NR-1]. - cxpi_tx_out[CH_IDX] = tx_out[CH_IDX]. - cxpi_tx_out[CH_NR-1] = tx_out[CH_NR-1]. '1': Enabled. Test mode, specific test mode is specified by MODE.
	FUNCTIONAL_MODE			0	Functional mode
	TEST_MODE			1	Test mode

3.3.3 CH

3.3.3.1 CXPI_CH_CTL0

Description: Control 0
Address: 0x402E8000
Offset: 0x0
Retention: Retained
IsDeepSleep: No
Comment: This register contains controls for CXPI such as modes, offset, or master/slave. This register is programmed before the start of a transaction and not to be change inflight of any transaction. It can only be change during CXPI controller is quiescent.
Default: 0x10

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	RXPIDZERO_CHECK_EN [7:7]	None [6:5]		AUTO_EN [4:4]	None [3:1]			MODE [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:10]						PRESAMPLE_EN [9:9]	FILTER_EN [8:8]

Bits	23	22	21	20	19	18	17	16
Name				IFS [20:16]				

Bits	31	30	29	28	27	26	25	24
Name	ENABLED [31:31]	MASTER [30:30]	None [29:28]		BIT_ERROR_IGNORE [27:27]	None [26:25]		IBS [24:24]

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	MODE	RW	R	0	Mode of operation: '0': NRZ mode. '1': PWM mode.
	NRZ			0	NRZ mode
	PWM			1	PWM mode
4	AUTO_EN	RW	R	1	CXPI transceiver auto enable: '0': Disabled. '1': Enabled. The TX_RX_STATUS.EN_OUT field is controlled by HW.
7	RXPIDZERO_CHECK_EN	RW	R	0	Receive PID Zero Check Enable. 0 - No action if received PID[6:0] = 0 and PID[7]=1'b1. 1 - If received PID[6:0] = 0 and PID[7]=1'b1, HW (slave) does not clear CMD.RX_HEADER and will anticipate receiving header again (CMD.TX_HEADER=0). If CMD.TX_HEADER=1 in the same scenario, then HW (slave) clears CMD.RX_HEADER upon receiving the header follow by transmit PID. This mode is useful for case where polling method is used and CXPI controller is configured as slave. This would reduce dependency on SW to react to the header received within IBS=1.

Bits	Name	SW	HW	Default or Enum	Description
8	FILTER_EN	RW	R	0	RX filter enable (for 'cxpi_rx_in') '0': No filter '1': Median 3 (default value) operates on the last three 'cxpi_rx_in' values. The sequences '000', '001', '010', and '100' result in a filtered value '0'. The sequences '111', '110', '101', and '011' result in a filtered value '1'.
9	PRESAMPLE_EN	RW	R	0	Pre-sample enable for PWM mode. '0': Disbaled. '1': Enabled When sampling counter's value is greater than CTL1.T_LOW1, pre-sample FF will be set to '1' as long as detecting any '1' on 'cxpi_rx_in' and be cleared to '0' after sampling moment. At the sampling moment, if pre-sample FF or 'cxpi_rx_in' is '1', sample value will be '1', otherwise '0'.
16:20	IFS	RW	R	0	Inter Frame Space in bit periods: '0" Invalid. ... '10': 10 bit periods ... '31': 31 bit periods Values of <10 are not allowed. This field is used for transmission/reception for adding waiting inter frame space. Note that after a valid transaction (after CRC), HW waits for 10 bits as EOF. Hence, by setting CTL0.IFS=0xA means that HW will wait for 10bits before transmitting a new transaction (not including the EOF). Note: 0 is not allowed when IFS_WAIT=1. SW needs to ensure it has program valid values before it can set IFS_WAIT=1. If IFS_WAIT=1 after timeout occurs, the value of CTL0.IFS would need to consider the timeout count i.e. (IFS needed - CTL2.TIMEOUT_LENGTH-1) to get the total idle time. For example if TIMEOUT_LENGTH=9 and IFS needed is 20, then CTL0.IFS is set to 10.
21:24	IBS	RW	R	0	Inter Byte Space in bit periods: '0' No offset. '1' 1 IBS is inserted per every byte frame. ... '9' 9 IBS are inserted per every byte frame. Values >9 are invalid per spec. This field is used to control number of IBS after every byte frame when transmitting message frame. Note that this field is the minimum IBS inserted for every byte frame as the SW may require some time to prepare the response when it receives the PID. When receiving, this field is ignored with the exception of receiving header and transmitting response. For receiving header and transmitting response, SW can enable IBS insertion by setting TIMEOUT_SEL=1/2 prior to setting CMD.RX_HEADER=1 and CMD.RX_RESPONSE=1. If the received header corresponds to transmit response, SW clears CMD.RX_RESPONSE =0 and sets TX FIFO and CMD.TX_RESPONSE=1. HW waits for minimum IBS before transmit response (if timeout has not occurred yet). It is prohibit to program IBS>TIMEOUT_LENGTH. This field should not be changed during inflight transaction including EOF.

Bits	Name	SW	HW	Default or Enum	Description
27	BIT_ERROR_IGNORE	RW	R	0	Specifies behavior on a detected bit error during header or response transmission: '0': Message transfer is aborted. '1': Message transfer is NOT aborted. Note: This field does NOT effect the reporting of the bit error through INTR/STATUS.TX_BIT_ERROR; i.e. bit errors are always reported. Note: This field must not be set to '1' when it is NRZ mode. This is due to delay in transceiver will cause the transmitter behavior undefined when error occurs.
	ABORT_TX_MSG			0	Message transfer is aborted
	CONT_TX_MSG			1	Message transfer is NOT aborted
30	MASTER	RW	R	0	CXPI master mode. '0': Indicates CXPI as slave node. '1': Indicates CXPI as master node. This bit is only valid if ENABLED=1. SW needs to set only 1 node as master within the same CXPI cluster. SW needs to set this bit either at the same time as ENABLED or before ENABLED is set. If SW needs to change the controller to different mode, it needs to make sure that HW is quiescent before doing so.
	SLAVE_MODE			0	Slave mode
	MASTER_MODE			1	Master mode
31	ENABLED	RW	R	0	Channel enable: '0': Disabled. If a channel is disabled, CMD, STATUS, INTR MMIO registers will have their fields reset to their default value. '1': Enabled.
	DISABLED			0	Disabled
	ENABLED			1	Enabled

3.3.3.2 CXPI_CH_CTL1

Description: Control 1
Address: 0x402E8004
Offset: 0x4
Retention: Retained
IsDeepSleep: No
Comment: This register contains controls on configuring different timing controls at Data link layer. This register is programmed before the start of a transaction and not to be change inflight of any transaction. It can only be change during CXPI controller is quiescent.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	T_LOW1 [7:0]							

Bits	15	14	13	12	11	10	9	8
Name					None [11:9]			T_LOW1 [8:8]

Bits	23	22	21	20	19	18	17	16
Name			None [21:21]	T_LOW0 [20:16]				

Bits	31	30	29	28	27	26	25	24
Name	None [31:31]	T_OFFSET [30:24]						

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:8	T_LOW1	RW	R	0	Low count for logic 1. This is valid only for PWM mode. For master node, The count value here indicates the number of clocks per clk_cxpi_ch to drive a '0' at CXPI bus before releasing it to indicate a logical '1'. For slave node and pre-sample enabled, the count value indicates the number of clocks per clk_cxpi_ch to disable pre-sampling. 0: means 1 clock. 1: means 2 clocks .. 15: means 16 clocks. .. 399: means 400 clocks. Any value above 399 is invalid. Note that for NRZ mode, this field is ignored. Note that it must be set less than CTL1.T_OFFSET for slave node if pre-sample mode enabled. Note that it is also effective for pre-sample mode of master node.

Bits	Name	SW	HW	Default or Enum	Description
12:20	T_LOW0	RW	R	0	Low count for logic 0. This is valid only for PWM mode. The count value here indicates the number of clocks per clk_cxpi_ch to drive a '0' at CXPI bus before releasing it to indicate a logical '0'. 0: means 1 clock. 1: means 2 clocks .. 15: means 16 clocks .. 399: means 400 clocks Any value above 399 is invalid. Note that for NRZ mode, this field is ignored. Note that this field is used for TX.
22:30	T_OFFSET	RW	R	0	The value of offset that is used for sampling the 'rx'. The value of this counter is used in HW as below. - 0 : means 1 clock after detecting falling edge of 'rx' - 1 : means 2 clocks after detecting falling edge of 'rx' .. - 7 : means 8 clocks after detecting falling edge of 'rx' .. - 15 : means 16 clocks after detecting falling edge of 'rx' .. - 399 : means 400 clocks after detecting falling edge of 'rx' Any value above 399 is invalid.

3.3.3.3 CXPI_CH_CTL2

Description: Control 2
Address: 0x402E8008
Offset: 0x8
Retention: Retained
IsDeepSleep: No
Comment: This register contains fields for number of retries.
These registers are programmed before the start of a transaction and not to be change inflight of any transaction. It can only be change during CXPI controller is quiescent.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:2]						RETRY [1:0]	

Bits	15	14	13	12	11	10	9	8
Name	None [15:14]		T_WAKEUP_LENGTH [13:8]					

Bits	23	22	21	20	19	18	17	16
Name			None [21:20]		TIMEOUT_LENGTH [19:16]			

Bits	31	30	29	28	27	26	25	24
Name	TIMEOUT_SEL [31:30]		RXTX_DELAY [29:24]					

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:1	RETRY	RW	R	0	Number of retries after arbitration lost. '0': No retries. .. '3': 3 retries. HW will immediately retry after arbitration lost i.e. after the message frame that won the arbitration is complete and fulfilled IFS. If SW wants to manage the retransmission then SW can program RETRY =0. In this case, HW will not retry after arbitration lost and will set TX_HEADER_ARB_LOST bit. SW needs to trigger HW to resend by programming the CMD fields again.
8:13	T_WAKEUP_LENGTH	RW	R	0	Specifies the wake up pulse low period in Tbits that is transmitted during Standby mode. '0': 1 bit period '1': 2 bit period .. '49': 50 bit period Any value above 49 is invalid. This field is only valid if TX_WAKE_PULSE is set to 1.
16:19	TIMEOUT_LENGTH	RW	R	0	Timeout Length (in Tbits). Specifies the number of Tbits to exceed timeout between frame bytes within a message frame. CXPI spec states that the maximum allowed inter byte space (IBS) is 9Tbits. This field is valid only when TIMEOUT_SEL=1/2. '0' - 1Tbit '1' - 2Tbits .. '9' - 10Tbits Values >9 is invalid per CXPI spec. Note for NRZ mode, although there are propagation delay from transceiver to CXPI controller, the delay is cancelled out as the timeout is compared on the RX (for transmit case, HW waits for the feedback on RX).

Bits	Name	SW	HW	Default or Enum	Description
22:29	RXTX_DELAY	RW	R	0	Insert addtional delay from the falling edge of RX to the falling edge of TX for slave node transmitting '0'. This is valid only for PWM mode. The count value here indicates the number of clocks per clk_cxpi_ch. 0: None 1: means 1 clock. 2: means 2 clocks. ... 255: means 255 clocks. Note it must be set less than CTL1.T_LOW0. Note make sure that the falling edge of tx_out is ahead of the rising edge of master node clock when CTL0.PRESAMPLE_EN=1.
30:31	TIMEOUT_SEL	RW	R	0	Timeout Select. '0' - Timeout check is disabled. HW clears timeout counter. '1' - Timeout check is enabled and HW will refer to TIMEOUT_LENGTH as number of Tbits allowed between header and response. '2' - Timeout check is enabled to check header-header, header-response, and header-header-response within a message frame to be space within TIMEOUT_LENGTH bit time. '3' - invalid For '1', HW will restart/start timeout counter after transmitting/receiving header. HW will hold the counter if timeout until the next header is transmitted or received. Timeout will cause HW to stop transmission of the current message frame together with interrupt to SW. For receive, HW abort reception of the frame if timeout occurs while waiting for receiving response and notify SW with interrupt. For '2', HW will re-start/start timeout counter after receiving any frame bytes within a message frame. HW will hold the counter if timeout until the IFS. Timeout will cause HW to stop transmission of the current message frame and notify SW with interrupt. For receive, HW will abort reception of the message frame if timeout occurs while waiting for receiving response and notify SW with interrupt. For all cases, HW stops counting when it is out of a message frame such as IFS or CXPI bus IDLE. If the timeout counter > TIMEOUT_LENGTH, then it will set the INTR.TIMEOUT=1. Note that, TIMEOUT_SEL=1/2 also enables the count for IBS between receive header and transmit response on top of timeout check.
	TIMEOUT_DISABLED			0	Timeout check is disabled.
	TIMEOUT_CHECK_BTW_HDR_RSP			1	Timeout check is enabled and HW will refer to TIMEOUT_LENGHT as number of Tbits allowed between header and response.
	TIMEOUT_CHECK_BTW_HDR_HDR_RSP			2	Timeout check is enabled to check header-header, header-response, and header-header-response within a message frame to be space within TIMEOUT_LENGTH bit time.

3.3.3.4 CXPI_CH_STATUS

Description: Status
Address: 0x402E800C
Offset: 0xC
Retention: Not Retained
IsDeepSleep: No
Comment: The register fields are not retained. This is to ensure that they come up as '0' after coming out of DeepSleep system power mode.

This is a non-retained register; setting CTL0.ENABLED to '0' clears all status fields to '0'.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:5]			HEADER_RESPONSE [4:4]	None [3:2]		RETRIES_COUNT [1:0]	

Bits	15	14	13	12	11	10	9	8
Name	None [15:14]		RX_DONE [13:13]	TX_DONE [12:12]	None [11:10]		RX_BUSY [9:9]	TX_BUSY [8:8]

Bits	23	22	21	20	19	18	17	16
Name	RX_DATA_LENGTH_ERROR [23:23]	RX_HEADER_PARITY_ERROR [22:22]	RX_CRC_ERROR [21:21]	TX_BIT_ERROR [20:20]	TX_HEADER_ARB_LOST [19:19]	TIMEOUT [18:18]	None [17:16]	

Bits	31	30	29	28	27	26	25	24
Name	None [31:31]	TX_FRAME_ERROR [30:30]	RX_FRAME_ERROR [29:29]	TX_UNDERFLOW_ERROR [28:28]	RX_UNDERFLOW_ERROR [27:27]	TX_OVERFLOW_ERROR [26:26]	RX_OVERFLOW_ERROR [25:25]	TX_DATA_LENGTH_ERROR [24:24]

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:1	RETRIES_COUNT	R	W	0	Retries count. The value reflects the number of retries that HW tries to transmit a header/response. HW will reset counter (either case below): 1. after successfully transmit the retry attempt 2. SW clears the CMD.TX_HEADER='0' 3. HW clearing CMD.TX_HEADER=0 due to errors (TX_BIT_ERROR, TX_HEADER_ARB_LOST, TX_OVERFLOW_ERROR, TX_UNDERFLOW_ERROR, TX_DATA_LENGTH_ERROR, and TX_FRAME_ERROR)
4	HEADER_RESPONSE	R	W	0	Frame header/response identifier (only valid when TX_BUSY or RX_BUSY is '1') '0' - Frame header being transferred. '1' - Frame response being transferred.
8	TX_BUSY	R	W	0	Transmitter busy. - Set to '1' on the start of the following commands: TX_HEADER, TX_RESPONSE. - Set to '0' on successful completion of previous commands or when an error is detected.

Bits	Name	SW	HW	Default or Enum	Description
9	RX_BUSY	R	W	0	Receiver busy. - Set to '1' on the start of the following commands: RX_HEADER, RX_RESPONSE. - Set to '0' on successful completion of previous commands or when an error is detected.
12	TX_DONE	R	W	0	Transmitter done: - Set to '0' on the start of a new command. - Set to '1' on successful completion of the following command sequences: - TX_HEADER. - TX_HEADER, TX_RESPONSE. - RX_HEADER, TX_RESPONSE.
13	RX_DONE	R	W	0	Receiver done: - Set to '0' on the start of a new command. - Set to '1' on successful completion of the following commmand sequences: - RX_HEADER, RX_RESPONSE. - TX_HEADER, RX_RESPONSE.
18	TIMEOUT	R	W	0	Copy of INTR.TIMEOUT
19	TX_HEADER_ARB_LOST	R	W	0	Copy of INTR.TX_HEADER_ARB_LOST
20	TX_BIT_ERROR	R	W	0	Copy of INTR.TX_BIT_ERROR.
21	RX_CRC_ERROR	R	W	0	Copy of INTR.RX_CRC_ERROR.
22	RX_HEADER_PARITY _ERROR	R	W	0	Copy of INTR.RX_HEADER_PARITY_ERROR.
23	RX_DATA_LENGTH _ERROR	R	W	0	Copy of INTR.RX_DATA_LENGTH_ERROR.
24	TX_DATA_LENGTH _ERROR	R	W	0	Copy of INTR.TX_DATA_LENGTH_ERROR.
25	RX_OVERFLOW _ERROR	R	W	0	Copy of INTR.RX_OVERFLOW_ERROR.
26	TX_OVERFLOW_ERROR	R	W	0	Copy of INTR.TX_OVERFLOW_ERROR.
27	RX_UNDERFLOW _ERROR	R	W	0	Copy of INTR.RX_UNDERFLOW_ERROR.
28	TX_UNDERFLOW _ERROR	R	W	0	Copy of INTR.TX_UNDERFLOW_ERROR.
29	RX_FRAME_ERROR	R	W	0	Copy of INTR.RX_FRAME_ERROR.
30	TX_FRAME_ERROR	R	W	0	Copy of INTR.TX_FRAME_ERROR.

3.3.3.5 CXPI_CH_CMD

Description: Command
Address: 0x402E8010
Offset: 0x10
Retention: Retained
IsDeepSleep: No
Comment: The register fields are retained. When a CXPI channel is disabled (CTL0.ENABLED is set to '0'), HW sets all the register fields to '0'.

The following restrictions apply when programming the commands:
- If both TX_HEADER and RX_HEADER are set to 1'b1 together with both IFS_WAIT and RXPIDZERO_CHECK_EN set to 1'b0, TX_HEADER will have higher precedence.
- If TX_HEADER, RX_HEADER, and (IFS_WAIT or RXPIDZERO_CHECK_EN) are all set together, RX_HEADER will have higher priority.
- TX_RESPONSE and RX_RESPONSE are NOT mutually exclusive, but are evaluated in the following order (of decreasing priority): TX_RESPONSE, RX_RESPONSE.
- During normal mode the CMDs below are allowed
RX_HEADER, IFS_WAIT, TX_HEADER, TX_RESPONSE, RX_RESPONSE, SLEEP (Higher priority -> lower priority if all are set at the same time).
Note that after executing TX_HEADER, TX_RESPONSE would be higher priority compare to RX_RESPONSE.
Note that after executing RX_HEADER or after arbitration loss while attempting to execute TX_HEADER, RX_RESPONSE would be higher priority compare to TX_RESPONSE.
- During Standby mode the CMDs below are allowed
SLEEP, WAKE_TO_STANDBY, TX_WAKE_PULSE (Higher priority -> lower priority). Note that WAKE_TO_STANDBY and TX_WAKE_PULSE does not have conflict in priority.
- During Sleep mode the CMDs below are allowed
WAKE_TO_STANDBY.

The use case for the combination commands to transmit/receive message frames are as below:
TX_HEADER, RX_HEADER, RX_RESPONSE, WAIT_IFS: for master/slave in event trigger that is performing transmit PID and follow by receiving response. For master in polling that is performing transmit PTYPE and receive PID follow by receiving/transmitting response. For transmitting response, SW needs to clear RX_RESPONSE and set TX_RESPONSE after decoding PID. For master in polling that is performing transmit PID follow by receive response.
TX_HEADER, RX_HEADER, TX_RESPONSE, RX_RESPONSE, WAIT_IFS: for master/slave in event trigger that is performing transmit PID and follow by transmit response. For master in polling that is transmitting PID and transmit response.
RX_HEADER, RX_RESPONSE: For master/slave in event trigger that is receiving PID. This would be use for both transmit response and receive response since SW needs to decode the PID first before initating transmit response.
RX_HEADER, RX_RESPONSE, CTL0.RXPIDZERO_CHECK_EN: For slave in polling mode to receive PTYPE and PID. Both transmit and receive response will use this combination as SW needs to decode the PID first before initiating transmit response.
TX_HEADER, RX_HEADER, RX_RESPONSE, CTL0.RXPIDZERO_CHECK_EN: For slave in polling mode to receive PTYPE and transmit PID and receive response.
TX_HEADER, RX_HEADER, TX_RESPONSE, RX_RESPONSE, CTL0.RXPIDZERO_CHECK_EN: For slave in polling mode to receive PTYPE and transmit PID and transmit response.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:6]		IFS_WAIT [5:5]	TX_WAKE_PULSE [4:4]	WAKE_TO_STANDBY [3:3]	SLEEP [2:2]	TX_RESPONSE [1:1]	TX_HEADER [0:0]

Bits	15	14	13	12	11	10	9	8

Name	None [15:10]	RX_RESPONSE [9:9]	RX_HEADER [8:8]

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	TX_HEADER	RW	RW	0	SW sets this field to '1' to transmit a header. HW sets this field to '0' on successful completion of ANY of the following legal command sequences (also set to '0' when an error (such as bit error if bit_ignore=0, arbitration loss, tx data length error. For timeout please refer to SAS) is detected): - TX_HEADER - TX_HEADER, TX_RESPONSE. - TX_HEADER, RX_RESPONSE. The above is for transmission of PID without prior transmission of PTYPE. The header is transmitted when the PID field STOP bits are transmitted (INTR.TX_HEADER_DONE). HW sets this field to '1', when the 'tr_cmd_tx_header' input trigger is activated. This allows for time triggered CXPI message transfer. HW driven time triggered transfer eliminates the jitter that is typically associated with SW driven transfer. SW clears this field to '0', when it wants to cancel a pending request. Note that if SW clears this field to '0' while HW is already in the middle of the request, then the cancel will be ignored. The cancel request can happen when HW is pending a retry when it is still servicing the current transaction. Or the cancel request can occur when HW is checking IFS/bus idle-ness. Note that if PTYPE (TX_HEADER) is transmitted follow by receive response (RX_RESPONSE) or no response, HW clears TX_HEADER right after transmitting PTYPE.
1	TX_RESPONSE	RW	RW1C	0	SW sets this field to '1' to transmit a response. HW sets this field to '0' on successful completion of ANY of the legal command sequences (also set to '0' when an error is detected). - TX_HEADER, TX_RESPONSE. - RX_HEADER, TX_RESPONSE. SW can also clear this field to '0' if SW wants to cancel the TX_RESPONSE. The response is transmitted when the CRC are transmitted (INTR.TX_RESPONSE_DONE).

Bits	Name	SW	HW	Default or Enum	Description
2	SLEEP	RW1S	RW1C	0	SW sets this field to '1' to direct HW to sleep mode. HW transits from Normal to Sleep upon SLEEP=1 and both TX and RX is idle. HW sets this field to '0' when it is in Sleep mode. Note that, SW needs to manage the entry to sleep mode by checking the conditions are met before initiating sleep mode e.g. all slave nodes supports sleep and on transmitting sleep frames to indicate sleep to all slave nodes.SW shall not program SLEEP=1 when HW is executing TX_WAKEUP_PULSE command. If SW programs SLEEP=1 during HW executing TX_WAKEUP_PULSE command, it will cause HW to abruptly stop transmitting wakeup pulse as below: 1. HW not clearing TX_WAKEUP_PULSE 2. HW not setting TX_WAKEUP_DONE 3. HW outputting TX_OUT=0.
3	WAKE_TO_STANDBY	RW	RW1C	0	SW sets this field to '1' to direct HW to wake up from Sleep mode to Standby mode. SW clears this field to '0' from '1' when it wants to direct HW from Standby to Normal mode. HW clears this field to '0' when it is in Normal mode or back to Sleep mode from Standby mode. For the case of CXPI master mode, HW will move its power mode from Sleep->Standby when this field is set to '1'. When SW clears this field is from '1' to '0' in Standby mode, HW will move to Normal mode while HW starts transmitting clock. To transmit wake pulse, SW need to program TX_WAKE_PULSE accordingly in Standby mode before entering Normal. For the case of CXPI slave mode and PWM mode, HW will move power mode from Sleep->Standby when this field is set to '1'. HW will wait for detection of clock before moving from Standby->Normal. SW clearing this field to '0' will have no effect. For the case of CXPI slave mode and NRZ mode, HW will move power mode from Sleep->Standby when this field is set to '1'. HW needs to be directed by SW by clearing this field to '0' to move from Standby->Normal after SW has detected clock through another IP (e.g. MXTCPWM).
4	TX_WAKE_PULSE	RW	RW1C	0	SW sets this field to '1' to direct HW to send wake up pulse. HW will transmit wake up pulse in Standby state only. HW will ignore this field when it's not in Standby state. '1' - HW will drive CXPI bus to low for period dictated by T_WAKEUP_LENGTH. '0:'- No wake up pulse HW clears this field to '0' after it transmit the pulse per T_WAKEUP_LENGTH. For the case where more than 1 wake pulses are required, SW is expected to set this field to '1' again (after this field is cleared to '0') per the number of times the wake pulse is required.

Bits	Name	SW	HW	Default or Enum	Description
5	IFS_WAIT	RW	RW1C	0	SW sets this field to '1' to wait for IFS. HW clears this field to '0' after it detects logical '1' based on IFS. HW will keep this field to '1' if it detects logical '0' before fulfilling the number of logical '1' required. The intention of this bit is to provide capability for SW to direct HW to check bus idle-ness before transmitting. Without setting this bit before directing HW to send header, HW will not check bus idle before transmitting. Besides that, this bit will also provide SW an option to configure HW to wait for IFS before sending again PTYPE or PID to fulfill IFS if there is no response from other nodes. Note: SW needs to configure valid IFS values before setting IFS_WAIT=1.
8	RX_HEADER	RW	RW1C	0	SW sets this field to '1' to receive a header. HW sets this field to '0' on successful completion of the ANY of the legal command sequences. (Not set to '0' when an error is detected). -RX_HEADER -RX_HEADER, TX_RESPONSE -RX_HEADER, RX_RESPONSE The above applies for cases of receiving PID without prior receiving PTYPE. The header is received when the PID field STOP bits are received (INTR.RX_HEADER_PID_DONE and INTR.RX_HEADER_DONE). Typically, a slave node SW sets both RX_HEADER and RX_RESPONSE to '1', anticipating a transfer of a response from the master node to this slave node. After receipt of the header PID/PTYPE field (INTR.RX_HEADER_PID_DONE is activated), the slave node may decide to set TX_RESPONSE to '1' (which has lower priority than RX_RESPONSE hence RX_RESPONSE need to be clear to '0' by SW) to transmit a response. Note that, for cases with RXPIDZERO_CHECK_EN=1 for slave in polling mode, RX_HEADER is cleared upon receiving PTYPE if the next course of action is to transmit PID. If the next course of action is to receive PID, then the RX_HEADER is cleared upon completion of response.
9	RX_RESPONSE	RW	RW1C	0	SW sets this field to '1' to receive a response. HW sets this field to '0' on successful completion of ANY of the legal command sequences (NOT set to '0' when an error is detected). -TX_HEADER, RX_RESPONSE -RX_HEADER, RX_RESPONSE SW can set this field to '1' to be conservative on receiving response i.e. IBS=0 whenever it is receiving PID. If the PID corresponds to transmit response, the SW can then clear this field to '0' and set TX_RESPONSE=1 to direct HW to send response. The response is received after CRC are received (INTR.RX_RESPONSE_DONE).

3.3.3.6 CXPI_CH_TX_RX_STATUS

Description: TX/RX status
Address: 0x402E8040
Offset: 0x40
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: 0x5000000

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:18]						RX_IN [17:17]	TX_IN [16:16]

Bits	31	30	29	28	27	26	25	24
Name	None [31:27]					EN_OUT [26:26]	None [25:25]	TX_OUT [24:24]

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
16	TX_IN	R	W	Undefined	CXPI transmitter input ('tx_in', 'cxpi_tx_in' in functional mode). TX_IN and RX_IN can be used to determine a wakeup source. Note that wakeup source detection relies on the external transceiver functionality.
17	RX_IN	R	W	Undefined	CXPI receiver input ('rx_in', 'cxpi_rx_in' in functional mode).
24	TX_OUT	R	W	1	CXPI transmitter output ('tx_out', 'cxpi_tx_out').
26	EN_OUT	RW	RW	1	CXPI transceiver enable ('en_out', 'cxpi_en_out'). This field controls the enable (or low active sleep enable) of the external transceiver: '0': Disabled. '1': Enabled. If CTL0.AUTO_EN is '0', SW controls this field to enable the external transceiver. If CTL0.AUTO_EN is '1', HW controls this field to enable the external transceiver: - HW sets this field to '1' when it is out of Sleep state. If it moves to Sleep state, HW will clear this field to '0'.

3.3.3.7 CXPI_CH_TXPID_FI

Description: TXPID and Frame Information
Address: 0x402E8050
Offset: 0x50
Retention: Retained
IsDeepSleep: No
Comment: This registers holds information on TX's PID, FI and DLCEXT
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	PID [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	FI [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	DLCEXT [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:7	PID	RW	R	Undefined	Header protected identifier (PID). - Bits 6 downto 0: frame identifier ID[6:0]. - Bits 7: is odd parity bit. - PID[7] = ! (ID[6] ^ ID[5] ^ ID[4] ^ ID[3] ^ ID[2] ^ ID[1] ^ ID[0]) Software does not need to program the parity bit i.e. bit[7]. HW will calculate the odd parity bit and ignore the bit[7] if SW occupies this bit. Transmission: To be transmitted PID field. HW will ignore bit[7] and compute the parity bit based on bits[6:0] Note that, this field can be use by SW to send PType byte as the HW handles both PID and PType the same way. The frame type would occupy bit[6:0] and the odd parity will be calculated by the HW.
8:15	FI	RW	R	Undefined	Frame Information. This is the byte that will be transmitted as Frame Information. Per CXPI spec, FI[7:4] denotes the data length count (DLC). FI[3:2] denotes Network Management. Bit[3] - wakeup.ind Bit[2] - sleep.ind FI[1:0] denotes CT. Please program to 2'b11 if no support of counter.
16:23	DLCEXT	RW	R	Undefined	Data Length Count Extension. This field is intended for payload of more than 12B. This field is only valid if DLC=4'b1111 (FI[7:4]). The value specified in this field will be the new payload size. Valid values are 0-255.

3.3.3.8 CXPI_CH_RXPID_FI

Description: RXPID and Frame Information
Address: 0x402E8054
Offset: 0x54
Retention: Not Retained
IsDeepSleep: No
Comment: This register holds information on RX's PID, Frame Information, and DLCEXT.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	PID [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	FI [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	DLCEXT [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:7	PID	R	RW	Undefined	Header protected identifier (PID). - Bits 6 downto 0: frame identifier ID[6:0]. - Bits 7: is odd parity bit. - PID[7] = ! (ID[6] ^ ID[5] ^ ID[4] ^ ID[3] ^ ID[2] ^ ID[1] ^ ID[0]) Reception: Received PID field. SW uses the PID field to determine how to handle the response for a received frame header: TX_RESPONSE or RX_RESPONSE. Note that, this field can be use by SW to check PType byte as the HW handles both PID and PType the same way. The frame type would occupy bit[6:0] and bit[7] is the parity bit of the frame type. This parity bit is send by the transmitting node.
8:15	FI	R	RW	Undefined	Frame Information. This is the byte that is received as Frame Information. Per CXPI spec, FI[7:4] denotes the data length count (DLC). FI[3:2] denotes Network Management. Bit[3] - wakeup.ind Bit[2] - sleep.ind FI[1:0] denotes CT.
16:23	DLCEXT	R	RW	Undefined	Data Length Count Extension. This field is intended for payload of more than 12B. This field is only valid if DLC=4'b1111 (FI[15:12]). The value specified in this field will be the new payload size. Valid values are 0-255.

3.3.3.9 CXPI_CH_CRC

Description: CRC
Address: 0x402E8058
Offset: 0x58
Retention: Not Retained
IsDeepSleep: No
Comment: This register holds the CRC bytes for RX and TX.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	RXCRC1 [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	RXCRC2 [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	TXCRC1 [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	TXCRC2 [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:7	RXCRC1	R	RW	Undefined	CRC first byte for both CRC8 and CRC16. This is valid for both Normal frame and Long frame. HW will load this field with first byte of CRC upon receiving it.
8:15	RXCRC2	R	RW	Undefined	CRC second byte of CRC16. This is valid only for Long frames. HW will load this field with second byte of CRC upon receiving it.
16:23	TXCRC1	R	RW	Undefined	CRC first byte for both CRC8 and CRC16. This is valid for both Normal frame and Long frame. HW will load this field with first byte of CRC for transmit.
24:31	TXCRC2	R	RW	Undefined	CRC second byte of CRC16. This is valid only for Long frames. HW will load this field with second byte of CRC for transmit.

3.3.3.10 CXPI_CH_TX_FIFO_CTL

Description: TX FIFO control
Address: 0x402E8080
Offset: 0x80
Retention: Not Retained
IsDeepSleep: No
Comment: This is the transmit fifo control register
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:5]			TRIGGER_LEVEL [4:0]				

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:18]						FREEZE [17:17]	CLEAR [16:16]

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:4	TRIGGER_LEVEL	RW	R	0	Trigger level. When the TX FIFO has less entries than the number of this field, a transmitter trigger event is generated: -INTR.TX_FIFO_TRIGGER = (#FIFO entries < TRIGGER_LEVEL)
16	CLEAR	RW	R	0	This is a synchronous clear signal to the TX FIFO. When '1', the TX FIFO content are cleared. If a quick clear is required, the field should be set to '1' and followed by '0'. If a clear is required for an extended time, the field should be set to 1 during the complete time.
17	FREEZE	RW	R	0	Freeze functionality: '0': HW uses TX FIFO data and pops the data from the TX FIFO for every HW read. '1': HW read from TX FIFO does not pop the data from the TX FIFO. Note: Freeze functionality is for debug purpose only.

3.3.3.11 CXPI_CH_TX_FIFO_STATUS

Description: TX FIFO status
Address: 0x402E8084
Offset: 0x84
Retention: Not Retained
IsDeepSleep: No
Comment: This is the transmit fifo control register
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:5]			USED [4:0]				

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:21]			AVAIL [20:16]				

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:4	USED	R	W	0	Number of used/occupied entries in the TX FIFO. The field value is in the range [0, 16]. When '0', the TX FIFO is empty. When '16', the TX FIFO is full.
16:20	AVAIL	R	W	Undefined	TX FIFO Avail 0-No available slot in TX FIFO 1-1 available slot in TX FIFO. 2-2 available slot in TX FIFO. .. 16-16 available slot in TX FIFO. Note that the Fifo Width is 1Byte and each slot in this context is 1 depth of the Fifo. The number of bytes are determine through the number of data bytes in a message frame. (TXPID_FI.FI/TXPID_FI.DLCEXT)

3.3.3.12 CXPI_CH_TX_FIFO_WR

Description: TX FIFO write
Address: 0x402E8088
Offset: 0x88
Retention: Not Retained
IsDeepSleep: No
Comment: This register supports 32-bit access only
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:7	DATA	W	R	0	Transmit Data field. Transmission: To be transmitted data field. SW provides data field. HW shadows over the write data to TX FIFO after SW performs a write to this field. HW shadows the whole 8 bits to the TX FIFO and relies on the TXPID_FI.FI/TXPID_FI.DCLEXT to determine the number of bytes. SW needs to ensure that TX FIFO is not overwritten before the content is consumed by HW by checking TX_FIFO_STATUS.AVAIL. Otherwise, the previous content would be overwritten and resulting in TX FIFO's overflow error (INTR.TX_OVERFLOW_ERROR).

3.3.3.13 CXPI_CH_RX_FIFO_CTL

Description: RX FIFO control
Address: 0x402E80A0
Offset: 0xA0
Retention: Not Retained
IsDeepSleep: No
Comment: This register contains RX FIFO control
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:5]			TRIGGER_LEVEL [4:0]				

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:18]						FREEZE [17:17]	CLEAR [16:16]

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:4	TRIGGER_LEVEL	RW	R	0	Trigger level. When RX FIFO has more entries than the number of this field, a receiver trigger event is generated. - INTR_RX.FIFO_TRIGGER = (#FIFO entries > TRIGGER_LEVEL)
16	CLEAR	RW	R	0	When '1', the RX FIFO content are popped. If a quick clear is required, the field should be set to '1' and followed by '0'. If a clear is required for an extended time, the field should be set to 1 during the complete time.
17	FREEZE	RW	R	0	Freeze functionality: '0': HW writes to RX FIFO and push the data to RX FIFO. '1': HW write to RX FIFO does not push the data to the RX FIFO. Note: Freeze functionality is for debug purpose only.

3.3.3.14 CXPI_CH_RX_FIFO_STATUS

Description: RX FIFO status
Address: 0x402E80A4
Offset: 0xA4
Retention: Not Retained
IsDeepSleep: No
Comment: This register contains RX FIFO control
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:5]			USED [4:0]				

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:21]			AVAIL [20:16]				

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:4	USED	R	W	0	Number of used/occupied entries in the RX FIFO. The field value is in the range [0, 16]. When '0', the RX FIFO is empty. When '16', the RX FIFO is full.
16:20	AVAIL	R	W	Undefined	RX FIFO avail 0-No content in RX FIFO 1-1 available content in RX FIFO. 2-2 available content in RX FIFO. .. 16-16 available content in RX FIFO. Note that the Fifo Width is 1Byte and each content in this context means 1 fifo slot. The number of bytes in each slot are determine through the number of data bytes in a message frame. (RXPID_FI.FI/RXPID_FI.DLCEXT)

3.3.3.15 CXPI_CH_RX_FIFO_RD

Description: RX FIFO read
Address: 0x402E80A8
Offset: 0xA8
Retention: Not Retained
IsDeepSleep: No
Comment: This register supports a single 32-bit access to read data fields.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:7	DATA	R	W	Undefined	Received Data field. Software uses this data field. HW shadows the first content of the RX FIFO to this field. Software reading this field will remove the content from the RX FIFO and the next content of the RX FIFO will be shadowed over to this field. This field is 8bits and reflects the width of the RX FIFO. Software needs to rely on the RXPID_FI.FI/RXPID_FI.DLCEXT fields to determine number of bytes. Note that, during debug, a read from test controller would not remove/destory the content. Software needs to ensure it does not read from this field if there is no available content (from RX_FIFO_STATUS.USED). Otherwise, the content is undefined and it would result in RX FIFO underflow error. (INTR.RX_UNDERFLOW_ERROR).

3.3.3.16 CXPI_CH_RX_FIFO_RD_SILENT

Description: RX FIFO silent read
Address: 0x402E80AC
Offset: 0xAC
Retention: Not Retained
IsDeepSleep: No
Comment: This register supports a single 32-bit access to read data fields.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:7	DATA	R	W	Undefined	Data read from the RX FIFO. Reading data from this field would not pop the data from RX FIFO. This register is for debug purpose.

3.3.3.17 CXPI_CH_INTR

Description: Interrupt
Address: 0x402E80C0
Offset: 0xC0
Retention: Not Retained
IsDeepSleep: No
Comment: The register fields are not retained. This is to ensure that they come up as '0' after coming out of DeepSleep system power mode.

This is a non-retained register; setting CTL0.ENABLED to '0' clears all command fields to '0'.

An activated error interrupt cause aborts an ongoing frame transfer (except for bit errors when CTL0.BIT_ERROR_IGNORE is '1').

Note that, if there is noise sample after the sampling of the stop bit of CRC byte, the TX_HEADER_DONE, TX_RESPONSE_DONE, RX_HEADER_DONE, or RX_RESPONSE_DONE (which ever corresponding done to be set during the transaction) may assert before the full Tbit of the stop bit.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:5]			TX_FIFO_TRIGGER [4:4]	TX_WAKEUP_DONE [3:3]	None [2:2]	TX_RESPONSE_DONE [1:1]	TX_HEADER_DONE [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:14]		TXRX_COMPLETE [13:13]	RX_HEADER_PID_DONE [12:12]	RX_FIFO_TRIGGER [11:11]	RX_WAKEUP_DETECT [10:10]	RX_RESPONSE_DONE [9:9]	RX_HEADER_DONE [8:8]

Bits	23	22	21	20	19	18	17	16
Name	RX_DATA_LENGTH_ERROR [23:23]	RX_HEADER_PARITY_ERROR [22:22]	RX_CRC_ERROR [21:21]	TX_BIT_ERROR [20:20]	TX_HEADER_ARB_LOST [19:19]	TIMEOUT [18:18]	None [17:16]	

Bits	31	30	29	28	27	26	25	24
Name	None [31:31]	TX_FRAME_ERROR [30:30]	RX_FRAME_ERROR [29:29]	TX_UNDERFLOW_ERROR [28:28]	RX_UNDERFLOW_ERROR [27:27]	TX_OVERFLOW_ERROR [26:26]	RX_OVERFLOW_ERROR [25:25]	TX_DATA_LENGTH_ERROR [24:24]

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	TX_HEADER_DONE	RW1C	RW1S	0	HW sets this field to '1', when a frame header (PID field or PType field) is transmitted (the CMD.TX_HEADER is completed).
1	TX_RESPONSE_DONE	RW1C	RW1S	0	HW sets this field to '1', when a frame response (frame information fields, data fields, and crc field) is transmitted (the CMD.TX_RESPONSE is completed).

Bits	Name	SW	HW	Default or Enum	Description
3	TX_WAKEUP_DONE	RW1C	RW1S	0	HW sets this field to '1', when a wakeup signal is transmitted (per CTL2.T_WAKEUP_LENGTH). This interrupt cause is activated on a transition from dominant/'0' state to recessive/'1' state; i.e. at the end of the wakeup signal.
4	TX_FIFO_TRIGGER	RW1C	RW1S	0	HW sets this field to '1', when TX trigger is generated (#used TX FIFO < TRIGGER_LEVEL).
8	RX_HEADER_DONE	RW1C	RW1S	0	HW sets this field to '1', when a frame header (PID field or PType field) is received (the CMD.RX_HEADER is completed). Specifically: - When followed by CMD.TX_RESPONSE or CMD.RX_RESPONSE, this field is set to '1' after completion of the message frame transfer. - When not followed by a response command, this field is set to '1' after completion of the header transfer if RXPIDZERO_CHECK_EN=1 and header received is PID. If RXPIDZERO_CHECK_EN=0 and response commands are not set, HW will set this field to '1' after receiving PID or PTYPE.
9	RX_RESPONSE_DONE	RW1C	RW1S	0	HW sets this field to '1', when a frame response (frame information fields, data fields, and crc field) is received (the CMD.RX_RESPONSE is completed).
10	RX_WAKEUP_DETECT	RW1C	RW1S	0	HW sets this field to '1', when RX fall is detected in Sleep mode.
11	RX_FIFO_TRIGGER	RW1C	RW1S	0	HW sets this field to '1', when RX trigger is generated (#used RX FIFO > TRIGGER_LEVEL).
12	RX_HEADER_PID_DONE	RW1C	RW1S	0	HW sets this field to '1', when RX header (PID/PTYPE field) is received.
13	TXRX_COMPLETE	RW1C	RW1S	0	HW sets this field to '1', when message frame ends after EOF is completed and TX/RX_DATA_LENGTH_ERROR=0.
18	TIMEOUT	RW1C	RW1S	0	HW sets this field to '1', when the transmitted/received bytes space within a message frame is > TIMEOUT_LENGTH. SW needs to set TIMEOUT_SEL=0 before clearing TIMEOUT=0 to ensure HW does not immediately sets back the interrupt.
19	TX_HEADER_ARB_LOST	RW1C	RW1S	0	HW sets this field to '1', when it detects arbitration lost after the number of retries has exceed the maximum allowed retries. Note: The ongoing message transfer is aborted (INTR.TX_HEADER_DONE and INTR.TX_RESPONSE_DONE is NOT activated and the TX_HEADER and TX_RESPONSE command is cleared to 0).

Bits	Name	SW	HW	Default or Enum	Description
20	TX_BIT_ERROR	RW1C	RW1S	0	HW sets this field to '1', when a transmitted 'cxpi_tx_out' value does NOT match a received 'cxpi_rx_in' value. The match is performed for the PID fields or PType (for the START bit and STOP bit only) and for the rest of the response i.e. frame information fields, data fields and the crc field (for the START bit, DATA bits, and STOP bits). Note: When CTL0.BIT_ERROR_IGNORE is '0', the ongoing message transfer is aborted (INTR.TX_RESPONSE_DONE is NOT activated. INTR.TX_HEADER_DONE is NOT activated if bit error occurs during the transmission of header byte) and the TX_HEADER and TX_RESPONSE commands are set to '0'. When CTL0.BIT_ERROR_IGNORE is '1', the ongoing message transfer would be transferred.
21	RX_CRC_ERROR	RW1C	RW1S	0	HW sets this field to '1', when received CRC is not matching with the compute CRC from header and response. Note: The ongoing message transfer is aborted (INTR.RX_RESPONSE_DONE is NOT activated).
22	RX_HEADER_PARITY _ERROR	RW1C	RW1S	0	HW sets this field to '1', when the received PID field or PType field has a parity error. Note: The ongoing message transfer is aborted (INTR.RX_HEADER_PID_DONE is NOT activated).
23	RX_DATA_LENGTH _ERROR	RW1C	RW1S	0	HW sets this field to '1, when the received message frame's data fields are more than the value specified in DLC (for normal frame) or DLCEXT (for long frame) i.e. after receiving CRC byte(s), HW is receiving logical '0' during EOF. For the case of receiving data length less than DLC/DLCEXT, HW will also set this field to '1'. This is the case where IBS>9 before the number of data reaches data length, then HW will report as data length error. HW starts checking after frame information byte. Note: SW needs to handle the message transfer i.e. discard or flush out. HW will still set the RX_RESPONSE_DONE.
24	TX_DATA_LENGTH _ERROR	RW1C	RW1S	0	HW sets this field to '1, when the transmit message frame's data fields are more than the value specified in DLC (for normal frame) or DLCEXT (for long frame) i.e. after transmitting CRC(s) byte, HW is receiving logical '0' during EOF. Note: HW will still set TX_RESPONSE_DONE and the TX_HEADER and TX_RESPONSE commands are set to '0'.
25	RX_OVERFLOW _ERROR	RW1C	RW1S	0	HW sets this field to '1', when the RX data is overwritten by HW before the SW reads from it. In CXPI spec, this error is denoted as overrun error. Note: Upon this error, SW should discard the RX data in RX FIFO.

Bits	Name	SW	HW	Default or Enum	Description
26	TX_OVERFLOW_ERROR	RW1C	RW1S	0	HW sets this field to '1', when the TX data is overwritten by SW before the HW reads from it to transmit to CXPI bus. Note: The ongoing message transfer will continue when this error happens however, data transferred at CXPI bus will be bogus and HW will invert the CRC to invalidate the message at the receiving node. TX_HEADER and TX_RESPONSE commands are set to '0'.
27	RX_UNDERFLOW _ERROR	RW1C	RW1S	0	HW sets this field to '1', when RX FIFO is empty and SW reads from it. Note: Upon this error, SW should discard the RX data in RX FIFO.
28	TX_UNDERFLOW _ERROR	RW1C	RW1S	0	HW sets this field to '1', when TX FIFO is empty and HW reads from it. Note: The ongoing message transfer will continue when this error happens however, data transferred at CXPI will be bogus and HW will invert the CRC to invalidate the message at the receiving node. TX_HEADER and TX_RESPONSE commands are set to '0'.
29	RX_FRAME_ERROR	RW1C	RW1S	0	HW sets this field to '1', when the stop bit of a byte frame is incorrect. Note: The ongoing message transfer is aborted (INTR.RX_RESPONSE_DONE is NOT activated and the INTR.RX_HEADER_DONE is NOT activated if the frame error occurs during header byte or if frame error occurs during response byte (if the HEADER and RESPONSE commands are set together)).
30	TX_FRAME_ERROR	RW1C	RW1S	0	HW sets this field to '1', when the stop bit of a byte frame is incorrect. This error would be a subset of TX_BIT_ERROR and also subjected to BIT_ERROR_IGNORE field. Note: The ongoing message transfer is aborted (RX_HEADER_DONE and INTR.TX_RESPONSE_DONE are NOT activated. INTR.TX_HEADER_DONE is NOT activated if frame error occurs during the transmission of header byte) and the TX_HEADER and TX_RESPONSE commands are set to '0'. Note: When CTL0.BIT_ERROR_IGNORE is '0', the ongoing message transfer is aborted (INTR.TX_RESPONSE_DONE is NOT activated. INTR.TX_HEADER_DONE is NOT activated if frame error occurs during the transmission of header byte) and the TX_HEADER and TX_RESPONSE commands are set to '0'. When CTL0.BIT_ERROR_IGNORE is '1', the ongoing message transfer would be transferred.

3.3.3.18 CXPI_CH_INTR_SET

Description: Interrupt set
Address: 0x402E80C4
Offset: 0xC4
Retention: Not Retained
IsDeepSleep: No
Comment: When read, this register reflects the INTR register.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:5]			TX_FIFO_TRIGGER [4:4]	TX_WAKEUP_DONE [3:3]	None [2:2]	TX_RESPONSE_DONE [1:1]	TX_HEADER_DONE [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:14]		TXRX_COMPLETE [13:13]	RX_HEADER_PID_DONE [12:12]	RX_FIFO_TRIGGER [11:11]	RX_WAKEUP_DETECT [10:10]	RX_RESPONSE_DONE [9:9]	RX_HEADER_DONE [8:8]

Bits	23	22	21	20	19	18	17	16
Name	RX_DATA_LENGTH_ERROR [23:23]	RX_HEADER_PARITY_ERROR [22:22]	RX_CRC_ERROR [21:21]	TX_BIT_ERROR [20:20]	TX_HEADER_ARB_LOST [19:19]	TIMEOUT [18:18]	None [17:16]	

Bits	31	30	29	28	27	26	25	24
Name	None [31:31]	TX_FRAME_ERROR [30:30]	RX_FRAME_ERROR [29:29]	TX_UNDERFLOW_ERROR [28:28]	RX_UNDERFLOW_ERROR [27:27]	TX_OVERFLOW_ERROR [26:26]	RX_OVERFLOW_ERROR [25:25]	TX_DATA_LENGTH_ERROR [24:24]

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	TX_HEADER_DONE	RW1S	A	0	Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect).
1	TX_RESPONSE_DONE	RW1S	A	0	Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect).
3	TX_WAKEUP_DONE	RW1S	A	0	Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect).
4	TX_FIFO_TRIGGER	RW1S	A	0	Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect).
8	RX_HEADER_DONE	RW1S	A	0	Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect).
9	RX_RESPONSE_DONE	RW1S	A	0	Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect).
10	RX_WAKEUP_DETECT	RW1S	A	0	Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect).
11	RX_FIFO_TRIGGER	RW1S	A	0	Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect).
12	RX_HEADER_PID_DONE	RW1S	A	0	Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect).
13	TXRX_COMPLETE	RW1S	A	0	Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect).

Bits	Name	SW	HW	Default or Enum	Description
18	TIMEOUT	RW1S	A	0	Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect).
19	TX_HEADER_ARB_LOST	RW1S	A	0	Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect).
20	TX_BIT_ERROR	RW1S	A	0	Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect).
21	RX_CRC_ERROR	RW1S	A	0	Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect).
22	RX_HEADER_PARITY _ERROR	RW1S	A	0	Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect).
23	RX_DATA_LENGTH _ERROR	RW1S	A	0	Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect).
24	TX_DATA_LENGTH _ERROR	RW1S	A	0	Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect).
25	RX_OVERFLOW _ERROR	RW1S	A	0	Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect).
26	TX_OVERFLOW_ERROR	RW1S	A	0	Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect).
27	RX_UNDERFLOW _ERROR	RW1S	A	0	Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect).
28	TX_UNDERFLOW _ERROR	RW1S	A	0	Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect).
29	RX_FRAME_ERROR	RW1S	A	0	Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect).
30	TX_FRAME_ERROR	RW1S	A	0	Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect).

3.3.3.19 CXPI_CH_INTR_MASK

Description: Interrupt mask
Address: 0x402E80C8
Offset: 0xC8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:5]			TX_FIFO_TRIGGER [4:4]	TX_WAKEUP_DONE [3:3]	None [2:2]	TX_RESPONSE_DONE [1:1]	TX_HEADER_DONE [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:14]		TXRX_COMPLETE [13:13]	RX_HEADER_PID_DONE [12:12]	RX_FIFO_TRIGGER [11:11]	RX_WAKEUP_DETECT [10:10]	RX_RESPONSE_DONE [9:9]	RX_HEADER_DONE [8:8]

Bits	23	22	21	20	19	18	17	16
Name	RX_DATA_LENGTH_ERROR [23:23]	RX_HEADER_PARITY_ERROR [22:22]	RX_CRC_ERROR [21:21]	TX_BIT_ERROR [20:20]	TX_HEADER_ARB_LOST [19:19]	TIMEOUT [18:18]	None [17:16]	

Bits	31	30	29	28	27	26	25	24
Name	None [31:31]	TX_FRAME_ERROR [30:30]	RX_FRAME_ERROR [29:29]	TX_UNDERFLOW_ERROR [28:28]	RX_UNDERFLOW_ERROR [27:27]	TX_OVERFLOW_ERROR [26:26]	RX_OVERFLOW_ERROR [25:25]	TX_DATA_LENGTH_ERROR [24:24]

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	TX_HEADER_DONE	RW	R	0	Mask for corresponding field in INTR register.
1	TX_RESPONSE_DONE	RW	R	0	Mask for corresponding field in INTR register.
3	TX_WAKEUP_DONE	RW	R	0	Mask for corresponding field in INTR register.
4	TX_FIFO_TRIGGER	RW	R	0	Mask for corresponding field in INTR register.
8	RX_HEADER_DONE	RW	R	0	Mask for corresponding field in INTR register.
9	RX_RESPONSE_DONE	RW	R	0	Mask for corresponding field in INTR register.
10	RX_WAKEUP_DETECT	RW	R	0	Mask for corresponding field in INTR register.
11	RX_FIFO_TRIGGER	RW	R	0	Mask for corresponding field in INTR register.
12	RX_HEADER_PID_DONE	RW	R	0	Mask for corresponding field in INTR register.
13	TXRX_COMPLETE	RW	R	0	Mask for corresponding field in INTR register.
18	TIMEOUT	RW	R	0	Mask for corresponding field in INTR register.
19	TX_HEADER_ARB_LOST	RW	R	0	Mask for corresponding field in INTR register.
20	TX_BIT_ERROR	RW	R	0	Mask for corresponding field in INTR register.
21	RX_CRC_ERROR	RW	R	0	Mask for corresponding field in INTR register.
22	RX_HEADER_PARITY_ERROR	RW	R	0	Mask for corresponding field in INTR register.
23	RX_DATA_LENGTH_ERROR	RW	R	0	Mask for corresponding field in INTR register.

Bits	Name	SW	HW	Default or Enum	Description
24	TX_DATA_LENGTH _ERROR	RW	R	0	Mask for corresponding field in INTR register.
25	RX_OVERFLOW _ERROR	RW	R	0	Mask for corresponding field in INTR register.
26	TX_OVERFLOW_ERROR	RW	R	0	Mask for corresponding field in INTR register.
27	RX_UNDERFLOW _ERROR	RW	R	0	Mask for corresponding field in INTR register.
28	TX_UNDERFLOW _ERROR	RW	R	0	Mask for corresponding field in INTR register.
29	RX_FRAME_ERROR	RW	R	0	Mask for corresponding field in INTR register.
30	TX_FRAME_ERROR	RW	R	0	Mask for corresponding field in INTR register.

3.3.3.20 CXPI_CH_INTR_MASKED

Description: Interrupt masked
Address: 0x402E80CC
Offset: 0xCC
Retention: Not Retained
IsDeepSleep: No
Comment: When read, this register reflects a bitwise AND between the INTR and INTR_MASK registers. This register allows SW to read the status of all mask enabled interrupt causes with a single load operation, rather than two load operations: one for INTR and one for INTR_MASK. This simplifies Firmware development. The associated interrupt is active ('1'), when INTR_MASKED != 0.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:5]			TX_FIFO_TRIGGER [4:4]	TX_WAKEUP_DONE [3:3]	None [2:2]	TX_RESPONSE_DONE [1:1]	TX_HEADER_DONE [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:14]		TXRX_COMPLETE [13:13]	RX_HEADER_PID_DONE [12:12]	RX_FIFO_TRIGGER [11:11]	RX_WAKEUP_DETECT [10:10]	RX_RESPONSE_DONE [9:9]	RX_HEADER_DONE [8:8]

Bits	23	22	21	20	19	18	17	16
Name	RX_DATA_LENGTH_ERROR [23:23]	RX_HEADER_PARITY_ERROR [22:22]	RX_CRC_ERROR [21:21]	TX_BIT_ERROR [20:20]	TX_HEADER_ARB_LOST [19:19]	TIMEOUT [18:18]	None [17:16]	

Bits	31	30	29	28	27	26	25	24
Name	None [31:31]	TX_FRAME_ERROR [30:30]	RX_FRAME_ERROR [29:29]	TX_UNDERFLOW_ERROR [28:28]	RX_UNDERFLOW_ERROR [27:27]	TX_OVERFLOW_ERROR [26:26]	RX_OVERFLOW_ERROR [25:25]	TX_DATA_LENGTH_ERROR [24:24]

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	TX_HEADER_DONE	R	W	0	Logical AND of corresponding INTR and INTR_MASK fields.
1	TX_RESPONSE_DONE	R	W	0	Logical AND of corresponding INTR and INTR_MASK fields.
3	TX_WAKEUP_DONE	R	W	0	Logical AND of corresponding INTR and INTR_MASK fields.
4	TX_FIFO_TRIGGER	R	W	0	Logical AND of corresponding INTR and INTR_MASK fields.
8	RX_HEADER_DONE	R	W	0	Logical AND of corresponding INTR and INTR_MASK fields.
9	RX_RESPONSE_DONE	R	W	0	Logical AND of corresponding INTR and INTR_MASK fields.
10	RX_WAKEUP_DETECT	R	W	0	Logical AND of corresponding INTR and INTR_MASK fields.
11	RX_FIFO_TRIGGER	R	W	0	Logical AND of corresponding INTR and INTR_MASK fields.

Bits	Name	SW	HW	Default or Enum	Description
12	RX_HEADER_PID_DONE	R	W	0	Logical AND of corresponding INTR and INTR_MASK fields.
13	TXRX_COMPLETE	R	W	0	Logical AND of corresponding INTR and INTR_MASK fields.
18	TIMEOUT	R	W	0	Logical AND of corresponding INTR and INTR_MASK fields.
19	TX_HEADER_ARB_LOST	R	W	0	Logical AND of corresponding INTR and INTR_MASK fields.
20	TX_BIT_ERROR	R	W	0	Logical AND of corresponding INTR and INTR_MASK fields.
21	RX_CRC_ERROR	R	W	0	Logical AND of corresponding INTR and INTR_MASK fields.
22	RX_HEADER_PARITY _ERROR	R	W	0	Logical AND of corresponding INTR and INTR_MASK fields.
23	RX_DATA_LENGTH _ERROR	R	W	0	Logical AND of corresponding INTR and INTR_MASK fields.
24	TX_DATA_LENGTH _ERROR	R	W	0	Logical AND of corresponding INTR and INTR_MASK fields.
25	RX_OVERFLOW _ERROR	R	W	0	Logical AND of corresponding INTR and INTR_MASK fields.
26	TX_OVERFLOW_ERROR	R	W	0	Logical AND of corresponding INTR and INTR_MASK fields.
27	RX_UNDERFLOW _ERROR	R	W	0	Logical AND of corresponding INTR and INTR_MASK fields.
28	TX_UNDERFLOW _ERROR	R	W	0	Logical AND of corresponding INTR and INTR_MASK fields.
29	RX_FRAME_ERROR	R	W	0	Logical AND of corresponding INTR and INTR_MASK fields.
30	TX_FRAME_ERROR	R	W	0	Logical AND of corresponding INTR and INTR_MASK fields.

4 DMAC

Description DataWire/DMA Controller
Base Address 0x40101000
Size 0x1000
Slave Num CPUMEMSSV3_VER3

Register Name	Address	Permission	Description
DMAC_CTL	0x40101000	FULL	Control register
DMAC_STATUS	0x40101010	FULL	Status register
DMAC_STATUS_SRC_ADDR	0x40101014	FULL	Source address status register
DMAC_STATUS_DST_ADDR	0x40101018	FULL	Destination address register
DMAC_STATUS_CH_ACT	0x4010101C	FULL	Channel activation status register
DMAC_CH_CTL0	0x40101080	FULL	Channel control register
DMAC_CH_CTL1	0x40101084	FULL	Channel control register
DMAC_CH_CTL2	0x40101088	FULL	Channel control register
DMAC_CH_CTL3	0x4010108C	FULL	Channel control register
DMAC_CH_CTL4	0x40101090	FULL	Channel control register
DMAC_CH_CTL5	0x40101094	FULL	Channel control register
DMAC_CH_CTL6	0x40101098	FULL	Channel control register
DMAC_CH_CTL7	0x4010109C	FULL	Channel control register
DMAC_INTR	0x401017F0	FULL	Interrupt register
DMAC_INTR_SET	0x401017F4	FULL	Interrupt set register
DMAC_INTR_MASK	0x401017F8	FULL	Interrupt mask register
DMAC_INTR_MASKED	0x401017FC	FULL	Interrupt masked register

4.1 DESCR 0

Register Name	Address	Permission	Description
DMAC_DESCR0_PING_SRC	0x40101800	FULL	Ping source address
DMAC_DESCR0_PING_DST	0x40101804	FULL	Ping destination address
DMAC_DESCR0_PING_CTL	0x40101808	FULL	Ping control word
DMAC_DESCR0_PING_STATUS	0x4010180C	FULL	Ping status word
DMAC_DESCR0_PONG_SRC	0x40101810	FULL	Pong source address
DMAC_DESCR0_PONG_DST	0x40101814	FULL	Pong destination address
DMAC_DESCR0_PONG_CTL	0x40101818	FULL	Pong control word
DMAC_DESCR0_PONG_STATUS	0x4010181C	FULL	Pong status word

4.2 DESCR 1

Register Name	Address	Permission	Description
DMAC_DESCR1_PING_SRC	0x40101820	FULL	Ping source address
DMAC_DESCR1_PING_DST	0x40101824	FULL	Ping destination address
DMAC_DESCR1_PING_CTL	0x40101828	FULL	Ping control word
DMAC_DESCR1_PING_STATUS	0x4010182C	FULL	Ping status word
DMAC_DESCR1_PONG_SRC	0x40101830	FULL	Pong source address
DMAC_DESCR1_PONG_DST	0x40101834	FULL	Pong destination address
DMAC_DESCR1_PONG_CTL	0x40101838	FULL	Pong control word
DMAC_DESCR1_PONG_STATUS	0x4010183C	FULL	Pong status word

4.3 DESCR 2

Register Name	Address	Permission	Description
DMAC_DESCR2_PING_SRC	0x40101840	FULL	Ping source address
DMAC_DESCR2_PING_DST	0x40101844	FULL	Ping destination address
DMAC_DESCR2_PING_CTL	0x40101848	FULL	Ping control word
DMAC_DESCR2_PING_STATUS	0x4010184C	FULL	Ping status word
DMAC_DESCR2_PONG_SRC	0x40101850	FULL	Pong source address
DMAC_DESCR2_PONG_DST	0x40101854	FULL	Pong destination address
DMAC_DESCR2_PONG_CTL	0x40101858	FULL	Pong control word
DMAC_DESCR2_PONG_STATUS	0x4010185C	FULL	Pong status word

4.4 DESCR 3

Register Name	Address	Permission	Description
DMAC_DESCR3_PING_SRC	0x40101860	FULL	Ping source address
DMAC_DESCR3_PING_DST	0x40101864	FULL	Ping destination address
DMAC_DESCR3_PING_CTL	0x40101868	FULL	Ping control word
DMAC_DESCR3_PING_STATUS	0x4010186C	FULL	Ping status word
DMAC_DESCR3_PONG_SRC	0x40101870	FULL	Pong source address
DMAC_DESCR3_PONG_DST	0x40101874	FULL	Pong destination address
DMAC_DESCR3_PONG_CTL	0x40101878	FULL	Pong control word
DMAC_DESCR3_PONG_STATUS	0x4010187C	FULL	Pong status word

4.5 DESCR 4

Register Name	Address	Permission	Description
DMAC_DESCR4_PING_SRC	0x40101880	FULL	Ping source address
DMAC_DESCR4_PING_DST	0x40101884	FULL	Ping destination address
DMAC_DESCR4_PING_CTL	0x40101888	FULL	Ping control word
DMAC_DESCR4_PING_STATUS	0x4010188C	FULL	Ping status word
DMAC_DESCR4_PONG_SRC	0x40101890	FULL	Pong source address
DMAC_DESCR4_PONG_DST	0x40101894	FULL	Pong destination address
DMAC_DESCR4_PONG_CTL	0x40101898	FULL	Pong control word
DMAC_DESCR4_PONG_STATUS	0x4010189C	FULL	Pong status word

4.6 DESCR 5

Register Name	Address	Permission	Description
DMAC_DESCR5_PING_SRC	0x401018A0	FULL	Ping source address
DMAC_DESCR5_PING_DST	0x401018A4	FULL	Ping destination address
DMAC_DESCR5_PING_CTL	0x401018A8	FULL	Ping control word
DMAC_DESCR5_PING_STATUS	0x401018AC	FULL	Ping status word
DMAC_DESCR5_PONG_SRC	0x401018B0	FULL	Pong source address
DMAC_DESCR5_PONG_DST	0x401018B4	FULL	Pong destination address
DMAC_DESCR5_PONG_CTL	0x401018B8	FULL	Pong control word
DMAC_DESCR5_PONG_STATUS	0x401018BC	FULL	Pong status word

4.7 DESCR 6

Register Name	Address	Permission	Description
DMAC_DESCR6_PING_SRC	0x401018C0	FULL	Ping source address
DMAC_DESCR6_PING_DST	0x401018C4	FULL	Ping destination address
DMAC_DESCR6_PING_CTL	0x401018C8	FULL	Ping control word
DMAC_DESCR6_PING_STATUS	0x401018CC	FULL	Ping status word
DMAC_DESCR6_PONG_SRC	0x401018D0	FULL	Pong source address
DMAC_DESCR6_PONG_DST	0x401018D4	FULL	Pong destination address
DMAC_DESCR6_PONG_CTL	0x401018D8	FULL	Pong control word
DMAC_DESCR6_PONG_STATUS	0x401018DC	FULL	Pong status word

4.8 DESCR 7

Register Name	Address	Permission	Description
DMAC_DESCR7_PING_SRC	0x401018E0	FULL	Ping source address
DMAC_DESCR7_PING_DST	0x401018E4	FULL	Ping destination address
DMAC_DESCR7_PING_CTL	0x401018E8	FULL	Ping control word
DMAC_DESCR7_PING_STATUS	0x401018EC	FULL	Ping status word
DMAC_DESCR7_PONG_SRC	0x401018F0	FULL	Pong source address
DMAC_DESCR7_PONG_DST	0x401018F4	FULL	Pong destination address
DMAC_DESCR7_PONG_CTL	0x401018F8	FULL	Pong control word
DMAC_DESCR7_PONG_STATUS	0x401018FC	FULL	Pong status word

4.9 Register Details

4.9.1 DMAC_CTL

Description: Control register
Address: 0x40101000
Offset: 0x0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	ENABLED [31:31]	None [30:24]						

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
31	ENABLED	RW	R	0	0': IP is disabled. Non-retainable MMIO registers and logic functionality are reset (retainable MMIO registers are NOT reset): - INTR register is set to '0'. - DW/DMA functionality is aborted. - DW/DMA controller input/pending triggers are de-activated. - DW/DMA controller output triggers are de-activated. Disabling the IP has the same effect as an active 'rst_sys_act_n' reset in DeepSleep power mode. To prevent a loss of active (pending) DW/DMA triggers when disabling the IP or when transitioning from Active to DeepSleep power mode, the STATUS.ACTIVE and STATUS_CH_ACT.CH fields can be used. Note that most MMIO registers are retainable, and a transition from DeepSleep to Active/Sleep power modes makes the DW/DMA controller operational, and ready to react to DW/DMA input triggers that are activated after the transition. Triggers are Active/Sleep functionality. '1': IP is enabled.

4.9.2 DMAC_STATUS

Description: Status register
Address: 0x40101010
Offset: 0x10
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	DATA_NR [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	DATA_NR [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:19]					CH_ADDR [18:16]		

Bits	31	30	29	28	27	26	25	24
Name	ACTIVE [31:31]	PING_PONG [30:30]	PRIO [29:28]		None [27:27]	STATE [26:24]		

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:15	DATA_NR	R	W	Undefined	Specifies the index of the currently active data transfer. This value increases from '0' to CONTROL.DATA_NR.
16:18	CH_ADDR	R	W	Undefined	Specifies the channel number of the currently active channel. E.g. if we have 32 channels, the channel number address with CH_ADDR_WIDTH is LOG2 (32) = 5, and this field is a 5-bit field. If channel 7 is active, STATUS.ACTIVE is '1' and STATUS.CH_ADDR is '7'.
24:26	STATE	R	W	0	State of the data transfer engine. '0': DEFAULT state. '1': Loading descriptor (SRC, DST, CONTROL and STATUS words). '2': Loading data element from source location. '3': Storing data element to destination location. '4': Storing descriptor (STATUS word). '5': Wait for trigger de-activation. '6': Storing descriptor with error response (STATUS word).
28:29	PRIO	R	W	Undefined	Specifies the priority of the currently active channel.
30	PING_PONG	R	W	Undefined	Specifies the descriptor of the channel is currently in use. '0' - PING descriptor '1' - PONG descriptor
31	ACTIVE	R	W	0	Specifies if there is a currently active (pending) channel in the data transfer engine: '0': no currently active channel. '1': currently active channel.

4.9.3 DMAC_STATUS_SRC_ADDR

Description: Source address status register
Address: 0x40101014
Offset: 0x14
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	ADDR [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	ADDR	R	W	Undefined	Base address or current address of source location of currently active channel. The specific address information is cycle dependent. This field is provided for debug purposes. Functionally, no assumption should be made on whether the base or current address is provided. The specifics of the currently active channel are available through STATUS. Note while reading the STATUS, STATUS_SRC_ADDR and STATUS_DST_ADDR registers, the transfer engine may have moved from one active channel to another.

4.9.4 DMAC_STATUS_DST_ADDR

Description: Destination address register
Address: 0x40101018
Offset: 0x18
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	ADDR [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	ADDR	R	W	Undefined	Base address or current address of destination location of currently active channel. The specific address information is cycle dependent. This field is provided for debug purposes. Functionally, no assumption should be made on whether the base or current address is provided. The specifics of the currently active channel are available through STATUS. Note while reading the STATUS, STATUS_SRC_ADDR and STATUS_DST_ADDR registers, the transfer engine may have moved from one active channel to another.

4.9.5 DMAC_STATUS_CH_ACT

Description: Channel activation status register
Address: 0x4010101C
Offset: 0x1C
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	CH [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:7	CH	R	W	0	Channel activation status. Bit i is associated to channel i, with i = 0, ..., CH_NR-1. Software reads this field to get information on all actively pending channels (either in pending or in the data transfer engine).

4.9.6 DMAC_CH_CTL

Description: Channel control register
Address: 0x40101080
Offset: 0x80
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	ENABLED [31:31]	PING_PONG [30:30]	PRIO [29:28]		None [27:24]			

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
28:29	PRIO	RW	R	0	Channel priority, with '0' representing the highest priority and '3' representing the lowest priority. Priority decoding uses the channel priority to determine the highest priority activated channel. If multiple activated channels have the same highest priority, the channel with the lowest index i, is considered the highest priority activated channel.
30	PING_PONG	RW	RW	0	Each channel has two descriptor structures for double buffering purposes. As the controller operates on one structure, the main CPU can operate on the other structure. The descriptor structures are identified as PING ('0') and PONG ('1'). This field identifies the descriptor structure that is currently in use by the controller. Software sets this field to the desired descriptor structure. Hardware inverts the field value on the completion of a descriptor structure when CONTROL.FLIPPING of the current descriptor structure is set to '1'.
31	ENABLED	RW	RW1C	0	'0': channel disabled. The channel's trigger is ignored and the channel cannot be activated. If the activated channel is disabled, the data transfer(s) are aborted. '1': channel enabled. Software sets this field to '1' to enable a specific channel. Hardware sets this field to '0' on erroneous channel behavior (the specific error is specified by STATUS.RESP in the channel's descriptor structure).

4.9.7 DMAC_INTR

Description: Interrupt register
Address: 0x401017F0
Offset: 0x7F0
Retention: Not Retained
IsDeepSleep: No
Comment: The register fields are not retained. This is to ensure that they come up as '0' after coming out of DeepSleep system power mode.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	CH [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:7	CH	RW1C	RW1S	0	Set to '1', when event is detected. Write INTR field with '1', to clear bit. Write INTR_SET field with '1', to set bit.

4.9.8 DMAC_INTR_SET

Description: Interrupt set register
Address: 0x401017F4
Offset: 0x7F4
Retention: Not Retained
IsDeepSleep: No
Comment: When read, this register reflects the interrupt request register.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	CH [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:7	CH	RW1S	A	0	Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect).

4.9.9 DMAC_INTR_MASK

Description: Interrupt mask register
Address: 0x401017F8
Offset: 0x7F8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	CH [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:7	CH	RW	R	0	Mask for corresponding field in INTR register.

4.9.10 DMAC_INTR_MASKED

Description: Interrupt masked register
Address: 0x401017FC
Offset: 0x7FC
Retention: Not Retained
IsDeepSleep: No
Comment: When read, this register reflects a bitwise and between the interrupt request and mask registers. This register allows SW to read the status of all mask enabled interrupt causes with a single load operation, rather than two load operations: one for the interrupt causes and one for the masks. This simplifies Firmware development. The associated interrupt is active ('1'), when INTR_M_MASKED != 0.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	CH [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:7	CH	R	W	0	Logical BITWISE AND of corresponding request and mask fields.

4.9.11 DESCR

4.9.11.1 DMAC_DESCR_PING_SRC

Description: Ping source address
Address: 0x40101800
Offset: 0x0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	ADDR [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	ADDR	RW	RW	Undefined	Base address of source location. The effective source location is calculated by adding on offset (derived from PING.STATUS.CURR_DATA_NR) to this base address.

4.9.11.2 DMAC_DESCR_PING_DST

Description: Ping destination address
Address: 0x40101804
Offset: 0x4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	ADDR [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	ADDR	RW	RW	Undefined	Base address of destination location. The effective destination location is calculated by adding on offset (derived from PING.STATUS.CURR_DATA_NR) to this base address.

4.9.11.3 DMAC_DESCR_PING_CTL

Description: Ping control word
Address: 0x40101808
Offset: 0x8
Retention: Retained
IsDeepSleep: No
Comment: Bits 18 and 19 of this MMIO register are not used. A SW write operation should write '0' to the unused bits.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	DATA_NR [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	DATA_NR [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	SRC_ADDR_INCR [23:23]	SRC_TRANSFER_SIZE [22:22]	DST_ADDR_INCR [21:21]	DST_TRANSFER_SIZE [20:20]	None [19:18]		DATA_SIZE [17:16]	

Bits	31	30	29	28	27	26	25	24
Name	OPCODE [31:30]		FLIPPING [29:29]	PREEMPTABLE [28:28]	SET_CAUSE [27:27]	INV_DESCR [26:26]	WAIT_FOR_DEACT [25:24]	

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:15	DATA_NR	RW	RW	Undefined	Number of data elements that are transferred by a single descriptor. In DW mode (OPCODE is '0') each trigger initiates the transfer of a single data element. This field specifies the source and/or destination buffer size in data elements: buffer size = DATA_NR+1. The buffer is typically associated to a memory structure. In DMA mode (OPCODE is '1' or '2') each trigger initiates the transfer of DATA_NR+1 data elements.

Bits	Name	SW	HW	Default or Enum	Description
16:17	DATA_SIZE	RW	RW	Undefined	Specifies the data element size: '0': Byte (8 bits). '1': Halfword (16 bits). '2': Word (32 bits). DATA_SIZE, SRC_TRANSFER_SIZE and DST_TRANSFER_SIZE together determine how data elements are transferred. The following are the 9 legal settings: - DATA is 8 bit, SRC is 8 bit, DST is 8 bit - DATA is 8 bit, SRC is 32 bit (higher 24 bits are dropped), DST is 8 bit - DATA is 8 bit, SRC is 8 bit, DST is 32 bit (higher 24 bits are made '0') - DATA is 8 bit, SRC is 32 bit (higher 24 bits are dropped), DST is 32 bit (higher 24 bits are made '0') - DATA is 16 bit, SRC is 16 bit, DST is 16 bit - DATA is 16 bit, SRC is 32 bit (higher 16 bits are dropped), DST is 16 bit - DATA is 16 bit, SRC is 16 bit, DST is 32 bit (higher 16 bits are made '0') - DATA is 16 bit, SRC is 32 bit (higher 16 bits are dropped), DST is 32 bit (higher 16 bits are made '0') - DATA is 32 bit, SRC is 32 bit, DST is 32 bit
20	DST_TRANSFER_SIZE	RW	RW	Undefined	Specifies the bus transfer size to the destination location: '0': As specified by DATA_SIZE. '1': Word (32 bits). Distinguishing bus transfer size from data element size allows for destination components with data elements that are smaller than their 32-bit bus interface width. E.g., a DAC destination has a 32-bit bus transfer size, but only requires a 16-bit data element.
21	DST_ADDR_INCR	RW	RW	Undefined	Specifies whether the destination location address is incremented by the DST_TRANSFER_SIZE after each single data element transfer or not. '0' : No increment, typically used for transmit (TX) FIFO structures. '1': Increment, typically used for memory structures.
22	SRC_TRANSFER_SIZE	RW	RW	Undefined	Specifies the bus transfer size to the source location: '0': As specified by DATA_SIZE. '1': Word (32 bits). Distinguishing bus transfer size from data element size allows for source components with data elements that are smaller than their 32-bit bus interface width. E.g., an ADC source has a 32-bit bus transfer size, but only provides a 16-bit data element.
23	SRC_ADDR_INCR	RW	RW	Undefined	Specifies whether the source location address is incremented by the SRC_TRANSFER_SIZE after each single data element transfer or not. '0': No increment, typically used for receive (RX) FIFO structures. '1': Increment, typically used for memory structures.

Bits	Name	SW	HW	Default or Enum	Description
24:25	WAIT_FOR_DEACT	RW	RW	Undefined	Specifies whether the data transfer engine should wait for the channel to be deactivated; i.e. the selected system trigger is not active. This field is used to synchronize the controller's data transfer(s) with the agent that generated the trigger. This field is ONLY used at the completion of an opcode. E.g., a FIFO indicates that it is empty and it needs a new data sample. The agent removes the trigger ONLY when the data sample has been written by the transfer engine AND received by the agent. Furthermore, the agent's trigger may be delayed by a few cycles before it reaches the DW/DMA controller. This field is used for level sensitive trigger, which reflect state (pulse sensitive triggers should have this field set to '0'). The wait cycles incurred by this field reduce DW/DMA controller performance. '0': Do not wait for de-activation (for pulse sensitive triggers). '1': Wait for up to 4 cycles. '2': Wait for up to 8 cycles. '3': Wait indefinitely. This option may result in DW/DMA controller lockup if the system trigger is not de-activated by the source agent.
26	INV_DESCR	RW	RW	Undefined	'1': On completion of the current descriptor structure, the VALID bit of the descriptor's STATUS word is set to '0'.
27	SET_CAUSE	RW	RW	Undefined	'1': On completion of the current descriptor structure, the interrupt cause field of the channel is set to '1' (INTR.CH[i]).
28	PREEMPTABLE	RW	RW	Undefined	'1': Transfer is preemptable. In DMA mode (OPCODE is '1' or '2'), multi data element transfers are constructed out of multiple single data element load (from the source location) and store (to the destination location) sequences. This field allows higher priority activated channels to preempt the current transfer in between these atomic (load, store) sequences. Preemption will NOT deactivate the current channel. As a result, after completion of a higher priority activated channel, the current channel is rescheduled.
29	FLIPPING	RW	RW	Undefined	'1': On completion of the current descriptor structure, the current descriptor identifier CH_CTLi.PING_PONG is flipped/inverted. In DMA mode, descriptor list transfer, flipping of the current descriptor identifier can be used to construct a linked list of descriptor structures.

Bits	Name	SW	HW	Default or Enum	Description
30:31	OPCODE	RW	RW	Undefined	Specifies the specific data transfer (only when the VALID bit of the descriptor's STATUS word is '1'): '0': A single trigger initiates a single data element transfer (DW mode). This opcode specifies a transfer of a single data element. The current descriptor is completed when the amount of transferred single data elements equals the programmed buffer size (DATA_NR+1). '1': A single trigger initiates a single descriptor transfer (DMA mode). This opcode specifies a transfer of DATA_NR+1 data elements as specified by the current descriptor structure. The current descriptor is completed when its data transfer is completed. '2': A single trigger initiates a descriptor list transfer (DMA mode). This opcode specifies a transfer of DATA_NR+1 data elements as specified by the current descriptor structure and by successive valid descriptors. The current descriptor is completed when its data transfer is completed. This OPCODE relies on FLIPPING to be set to '1', such that the CH_CTLi.PING_PONG field is flipped/inverted and the successive descriptor is used. This continues for as long as the successive descriptor is valid. Note that as the HW is using the PING/PONG descriptor, the SW can prepare the alternate PONG/PING descriptor. The interrupt mechanism is used by HW to convey to the SW that the current descriptor is completed (and can be prepared for a successive transfer). After completion of the opcode (and waiting for de-activation, the channel's output trigger is activated).

4.9.11.4 DMAC_DESCR_PING_STATUS

Description: Ping status word
Address: 0x4010180C
Offset: 0xC
Retention: Retained
IsDeepSleep: No
Comment: Bits 30 down to 19 of this MMIO register are not used. A SW write operation should write '0' to the unused bits.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	CURR_DATA_NR [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	CURR_DATA_NR [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:19]					RESPONSE [18:16]		

Bits	31	30	29	28	27	26	25	24
Name	VALID [31:31]	None [30:24]						

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:15	CURR_DATA_NR	RW	RW	Undefined	Specifies the index of the current data transfer. This value increases from 0 to CONTROL.DATA_NR. HW sets this field: - When a descriptor is done (RESPONSE is DONE), the field is set to '0' when PING_CTL.INV_DESCR is '0' and the field is set to PING_CTL.DATA_NR when PING_CTL.INV_DESCR is '1'. - When a descriptor is not done (RESPONSE is NO_ERROR), the field reflects the progress of a data transfer. - In case of erroneous behavior (RESPONSE is neither DONE or NO_ERROR), the field is not updated, but keeps its value to ease debugging. HW only modifies this field for an active descriptor (STATUS.VALID to be '1'). At descriptor initialization, SW should set this field to '0'. This field allows software to read the progress of the data transfer. Note that SRC.ADDR and DST.ADDR represent base addresses and are not modified during data transfer. However, STATUS.CURR_DATA_NR is modified during data transfer and provides an offset wrt. the base addresses.

Bits	Name	SW	HW	Default or Enum	Description
16:18	RESPONSE	RW	RW	Undefined	Response code (the first two codes NO_ERROR and DONE are the result of normal behavior, the other codes are the result of erroneous behavior). '0'/NO_ERROR: No error. Setting this response does NOT set the interrupt cause bit to '1'. STATUS.VALID is NOT affected. CH_CTLi.ENABLED is NOT affected. CH_CTLi.PING_PONG is not updated. This response is used for an unused or not completed descriptor. Software should set the RESPONSE field to '0'/NO_ERROR during descriptor initialization. '1'/DONE: Descriptor is done (without errors). Setting this response sets the interrupt cause bit to '1' if CONTROL.SET_CAUSE is '1'. STATUS.VALID is set to '0' if CONTROL.INV_DESCR is '1'. CH_CTLi.ENABLED is NOT affected. CH_CTLi.PING_PONG is updated if CONTROL.FLIPPING is '1'. '2'/SRC_BUS_ERROR: Bus error while loading data from the source location. Setting this response sets the interrupt cause bit to '1'. STATUS.VALID is set '0'. CH_CTLi.ENABLED is set to '0'. CH_CTLi.PING_PONG is not updated (it identifies the descriptor that caused the error). '3'/DST_BUS_ERROR: Bus error while storing data to the destination location. Setting this response sets the interrupt cause bit to '1'. STATUS.VALID is set '0'. CH_CTLi.ENABLED is set to '0'. CH_CTLi.PING_PONG is not updated (it identifies the descriptor that caused the error). '4'/SRC_MISAL: Misalignment of source address. This occurs on a 16-bit bus transfer that is not 2-byte aligned or on a 32-bit bus transfer that is not 4-byte aligned. Setting this response sets the interrupt cause bit to '1'. STATUS.VALID is set '0'. CH_CTLi.ENABLED is set to '0'. CH_CTLi.PING_PONG is not updated (it identifies the descriptor that caused the error). '5'/DST_MISAL: Misalignment of destination address. This occurs on a 16-bit bus transfer that is not 2-byte aligned or on a 32-bit bus transfer that is not 4-byte aligned. Setting this response sets the interrupt cause bit to '1'. STATUS.VALID is set '0'. CH_CTLi.ENABLED is set to '0'. CH_CTLi.PING_PONG is not updated (it identifies the descriptor that caused the error). '6'/INVALID_DESCR: Invalid descriptor (STATUS.VALID is '0'). This occurs when an activated channel has an invalid descriptor. CH_CTLi.ENABLED is set to '0'. CH_CTLi.PING_PONG is not updated (it identifies the descriptor that caused the error).
31	VALID	RW	RW	Undefined	'0': Invalid, cannot be used for a data transfer. An attempt to use this descriptor for a data transfer will result in an INVALID_DESCR response code (and the interrupt cause bit is set to '1'). '1': Valid. Hardware set this field to '0' when a descriptor is done, but only if CONTROL.INV_DESCR is '1'. Software sets this field to '1' when a descriptor is initialized.

4.9.11.5 DMAC_DESCR_PONG_SRC

Description: Pong source address
Address: 0x40101810
Offset: 0x10
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	ADDR [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	ADDR	RW	RW	Undefined	See description of PING_SRC.

4.9.11.6 DMAC_DESCR_PONG_DST

Description: Pong destination address
Address: 0x40101814
Offset: 0x14
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	ADDR [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	ADDR	RW	RW	Undefined	See description of PING_DST.

4.9.11.7 DMAC_DESCR_PONG_CTL

Description: Pong control word
Address: 0x40101818
Offset: 0x18
Retention: Retained
IsDeepSleep: No
Comment: Bits 18 and 19 of this MMIO register are not used. A SW write operation should write '0' to the unused bits.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	DATA_NR [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	DATA_NR [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	SRC _ADDR_ INCR [23:23]	SRC _TRANS FER_SIZE [22:22]	DST_ADDR _INCR [21:21]	DST _TRANS FER_SIZE [20:20]	None [19:18]		DATA_SIZE [17:16]	

Bits	31	30	29	28	27	26	25	24
Name	OPCODE [31:30]		FLIPPING [29:29]	PREEMPTAB LE [28:28]	SET _CAUSE [27:27]	INV _DESCR [26:26]	WAIT_FOR_DEACT [25:24]	

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:15	DATA_NR	RW	RW	Undefined	See description of PING_CTL.
16:17	DATA_SIZE	RW	RW	Undefined	See description of PING_CTL.
20	DST_TRANSFER_SIZE	RW	RW	Undefined	See description of PING_CTL.
21	DST_ADDR_INCR	RW	RW	Undefined	See description of PING_CTL.
22	SRC_TRANSFER_SIZE	RW	RW	Undefined	See description of PING_CTL.
23	SRC_ADDR_INCR	RW	RW	Undefined	See description of PING_CTL.
24:25	WAIT_FOR_DEACT	RW	RW	Undefined	See description of PING_CTL.
26	INV_DESCR	RW	RW	Undefined	See description of PING_CTL.
27	SET_CAUSE	RW	RW	Undefined	See description of PING_CTL.
28	PREEMPTABLE	RW	RW	Undefined	See description of PING_CTL.
29	FLIPPING	RW	RW	Undefined	See description of PING_CTL.
30:31	OPCODE	RW	RW	Undefined	See description of PING_CTL.

4.9.11.8 DMAC_DESCR_PONG_STATUS

Description: Pong status word
Address: 0x4010181C
Offset: 0x1C
Retention: Retained
IsDeepSleep: No
Comment: Bits 30 down to 19 of this MMIO register are not used. A SW write operation should write '0' to the unused bits.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	CURR_DATA_NR [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	CURR_DATA_NR [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:19]					RESPONSE [18:16]		

Bits	31	30	29	28	27	26	25	24
Name	VALID [31:31]	None [30:24]						

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:15	CURR_DATA_NR	RW	RW	Undefined	See description of PING_STATUS.
16:18	RESPONSE	RW	RW	Undefined	See description of PING_STATUS.
31	VALID	RW	RW	Undefined	See description of PING_STATUS.

5 FAULT

Description Fault structures
Base Address 0x40130000
Size 0x10000
Slave Num FAULT

5.1 STRUCT 0

Register Name	Address	Permission	Description
FAULT_STRUCT0_CTL	0x40130000	FULL	Fault control
FAULT_STRUCT0_STATUS	0x4013000C	FULL	Fault status
FAULT_STRUCT0_DATA0	0x40130010	FULL	Fault data
FAULT_STRUCT0_DATA1	0x40130014	FULL	Fault data
FAULT_STRUCT0_PENDING0	0x40130040	FULL	Fault pending 0
FAULT_STRUCT0_MASK0	0x40130050	FULL	Fault mask 0
FAULT_STRUCT0_INTR	0x401300C0	FULL	Interrupt
FAULT_STRUCT0_INTR_SET	0x401300C4	FULL	Interrupt set
FAULT_STRUCT0_INTR_MASK	0x401300C8	FULL	Interrupt mask
FAULT_STRUCT0_INTR_MASKED	0x401300CC	FULL	Interrupt masked

5.2 STRUCT 1

Register Name	Address	Permission	Description
FAULT_STRUCT1_CTL	0x40130100	FULL	Fault control
FAULT_STRUCT1_STATUS	0x4013010C	FULL	Fault status
FAULT_STRUCT1_DATA0	0x40130110	FULL	Fault data
FAULT_STRUCT1_DATA1	0x40130114	FULL	Fault data
FAULT_STRUCT1_PENDING0	0x40130140	FULL	Fault pending 0
FAULT_STRUCT1_MASK0	0x40130150	FULL	Fault mask 0
FAULT_STRUCT1_INTR	0x401301C0	FULL	Interrupt
FAULT_STRUCT1_INTR_SET	0x401301C4	FULL	Interrupt set
FAULT_STRUCT1_INTR_MASK	0x401301C8	FULL	Interrupt mask
FAULT_STRUCT1_INTR_MASKED	0x401301CC	FULL	Interrupt masked

5.3 Register Details

5.3.1 STRUCT

5.3.1.1 FAULT_STRUCT_CTL

Description: Fault control
Address: 0x40130000
Offset: 0x0
Retention: Retained
IsDeepSleep: No
Comment: This register uses DeepSleep reset. Therefore, a DeepSleep reset (possibly as a result of CTL.RESET_EN) resets this register (including setting CTL.RESET_EN to '0').
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:3]					RESET_REQ_EN [2:2]	OUT_EN [1:1]	TR_EN [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	TR_EN	RW	R	0	Trigger output enable: '0': Disabled. The trigger output 'tr_fault' is '0'. '1': Enabled. The trigger output 'tr_fault' reflects STATUS.VALID. The trigger can be used to initiate a Datawire transfer of the FAULT data (FAULT_DATA0 through FAULT_DATA1).
1	OUT_EN	RW	R	0	IO output signal enable: '0': Disabled. The IO output signal 'fault_out' is '0'. The IO output enable signal 'fault_out_en' is '0'. '1': Enabled. The IO output signal 'fault_out' reflects STATUS.VALID. The IO output enable signal 'fault_out_en' is '1'.
2	RESET_REQ_EN	RW	R	0	Reset request enable: '0': Disabled. '1': Enabled. The output reset request signal 'fault_reset_req' reflects STATUS.VALID. This reset causes a warm/soft/core reset. This warm/soft/core reset does not affect the fault logic STATUS, DATA0, ..., DATA1 registers (allowing for post soft reset failure analysis). The 'fault_reset_req' signals of the individual fault report structures are combined (logically OR'd) into a single SRSS 'fault_reset_req' signal.

5.3.1.2 FAULT_STRUCT_STATUS

Description: Fault status
Address: 0x4013000C
Offset: 0xC
Retention: Retained
IsDeepSleep: No
Comment: This register uses cold reset (and is NOT affected by Active or DeepSleep reset). This allows for failure analysis after a warm reset (DeepSleep reset).
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:7]	IDX [6:0]						

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	VALID [31:31]	None [30:24]						

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:6	IDX	RW	W	Undefined	The fault source index for which fault information is captured in DATA0 through DATA1. The fault information is fault source specific and differs per product. The encoding will align with the definition in the Product Srpeadsheet. Note: this register field (and associated fault source data in DATA0 through DATA1) should only be considered valid, when VALID is '1'.

Bits	Name	SW	HW	Default or Enum	Description
31	VALID	RW	RW1S	0	Valid indication: '0': Invalid. '1': Valid. STATUS.IDX, DATA0, ..., DATA1 specify the fault. Note: Typically, HW sets this field to '1' (on an activated HW fault source that is 'enabled' by the MASK registers) and SW clears this field to '0' (typically by boot code SW (after a warm system reset, when the fault is handled). In this typical use case scenario, the HW source fault data is simultaneously captured into DATA0, ..., DATA1 when the VALID field is set to '1'. An exceptional SW use case scenario is identified as well. In this scenario, SW sets this field to '1' with a fault source index different to one of the defined HW fault sources. SW update is not restricted by the MASK registers). In both use case scenarios, the following holds: - STATUS.IDX, DATA0, ..., DATA1 can only be written when STATUS.VALID is '0'; the fault structure is not in use yet. Writing STATUS.VALID to '1' effectively locks the fault structure (until SW clears STATUS.VALID to '0'). This restriction requires a SW update to sequentially update the DATA registers followed by an update of the STATUS register. Note: For the exceptional SW use case, sequential updates to the DATA and STATUS registers may be 'interrupted' by a HW fault capture. In this case, the SW DATA register updates are overwritten by the HW update (and the STATUS.IDX field will reflect the HW capture)

5.3.1.3 FAULT_STRUCT_DATA

Description: Fault data
Address: 0x40130010
Offset: 0x10
Retention: Retained
IsDeepSleep: No
Comment: The DATA registers capture fault information.

These register use cold reset (and are NOT affected by Active or DeepSleep reset). This allows for failure analysis after a warm reset (DeepSleep reset).
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	DATA [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	DATA	RW	W	Undefined	Captured fault source data. Note: the DATA registers can only be written when STATUS.VALID is '0'. Note: the fault source index STATUS.IDX specifies the format of the DATA registers.

5.3.1.4 FAULT_STRUCT_PENDING0

Description: Fault pending 0
Address: 0x40130040
Offset: 0x40
Retention: Not Retained
IsDeepSleep: No
Comment: The PENDING0 register specifies pending (not captured) fault sources. The fault source for which data is captured in DATA0 through DATA1 and which is validated by STATUS.VALID and identified by STATUS.IDX is NOT included in this list of pending fault sources. When a fault source is captured, its corresponding bit field in PENDING0s set to '0'.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	SOURCE [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	SOURCE [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	SOURCE [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	SOURCE [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	SOURCE	R	W	Undefined	Bit mask of source causing the Fault. See the Product Spreadsheet Fault tab to determine the bit ordering.

5.3.1.5 FAULT_STRUCT_MASK0

Description: Fault mask 0
Address: 0x40130050
Offset: 0x50
Retention: Retained
IsDeepSleep: No
Comment: The MASK0 register specifies 'enables' for fault sources. Only 'enabled' fault sources will be captured by this fault structure (and result in STATUS.VALID and INTR.FAULT being set to '1'). When a fault source is captured, its corresponding bit field in PENDING0 is set to '0'.

When multiple fault structures are present and the mask fields of the fault structures overlap (the same source is 'enabled' for multiple fault structures), an overlapping enabled pending fault source is captured by a single fault structure that has not captured a fault (the fault structure with the lowest index has precedence).
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	SOURCE [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	SOURCE [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	SOURCE [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	SOURCE [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	SOURCE	RW	R	0	Fault source enables: Bits 31-0: Fault sources 31 to 0.

5.3.1.6 FAULT_STRUCT_INTR

Description: Interrupt
Address: 0x401300C0
Offset: 0xC0
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:1]							FAULT [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	FAULT	RW1C	RW1S	0	This interrupt cause field is activated (HW sets the field to '1') when an enabled (MASK0 pending fault source is captured: - STATUS.VALID is set to '1'. - STATUS.IDX specifies the fault source index. - DATA0 through DATA1 captures the fault source data. SW writes a '1' to this field to clear the interrupt cause to '0'. SW clear STATUS.VALID to '0' to enable capture of the next fault. Note that when there is an enabled pending fault source, the pending fault source is captured immediately and INTR.FAULT is immediately activated (set to '1').

5.3.1.7 FAULT_STRUCT_INTR_SET

Description: Interrupt set
Address: 0x401300C4
Offset: 0xC4
Retention: Not Retained
IsDeepSleep: No
Comment: When read, this register reflects the INTR register. For debug purposes, SW can write a '1' to activate a specific interrupt cause (this allows for debug of the SW ISR, without relying on HW to activate the interrupt cause).
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:1]							FAULT [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	FAULT	RW1S	A	0	SW writes a '1' to this field to set the corresponding field in the INTR register.

5.3.1.8 FAULT_STRUCT_INTR_MASK

Description: Interrupt mask
Address: 0x401300C8
Offset: 0xC8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:1]							FAULT [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	FAULT	RW	R	0	Mask bit for corresponding field in the INTR register.

5.3.1.9 FAULT_STRUCT_INTR_MASKED

Description: Interrupt masked
Address: 0x401300CC
Offset: 0xCC
Retention: Not Retained
IsDeepSleep: No
Comment: When read, this register reflects 'a bitwise AND' between the INTR and INTR_MASK registers.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:1]							FAULT [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	FAULT	R	W	0	Logical and of corresponding INTR and INTR_MASK fields.

6 GPIO

Description GPIO port control/configuration
Base Address 0x40040000
Size 0x4000
Slave Num MMIO0

Register Name	Address	Permission	Description
GPIO_INTR_CAUSE	0x40041000	FULL	Interrupt port cause register
GPIO_DFT_IO_TEST	0x40041010	FULL	IO SELF TEST control register for DfT purposes only

6.1 PRT 0

Register Name	Address	Permission	Description
GPIO_PRT0_DR	0x40040000	FULL	Port output data register
GPIO_PRT0_PS	0x40040004	FULL	Port IO pad state register
GPIO_PRT0_PC	0x40040008	FULL	Port configuration register Note:PORT_HYST_TRIM PORT_SLEW_CTL are not available for this register
GPIO_PRT0_INTR_CFG	0x4004000C	FULL	Port interrupt configuration register
GPIO_PRT0_INTR	0x40040010	FULL	Port interrupt status register
GPIO_PRT0_PC2	0x40040018	FULL	Port configuration register 2
GPIO_PRT0_DR_SET	0x40040040	FULL	Port output data set register
GPIO_PRT0_DR_CLR	0x40040044	FULL	Port output data clear register
GPIO_PRT0_DR_INV	0x40040048	FULL	Port output data invert register

6.2 PRT 1

Register Name	Address	Permission	Description
GPIO_PRT1_DR	0x40040100	FULL	Port output data register
GPIO_PRT1_PS	0x40040104	FULL	Port IO pad state register
GPIO_PRT1_PC	0x40040108	FULL	Port configuration register Note:PORT_HYST_TRIM PORT_SLEW_CTL are not available for this register
GPIO_PRT1_INTR_CFG	0x4004010C	FULL	Port interrupt configuration register
GPIO_PRT1_INTR	0x40040110	FULL	Port interrupt status register
GPIO_PRT1_PC2	0x40040118	FULL	Port configuration register 2
GPIO_PRT1_DR_SET	0x40040140	FULL	Port output data set register
GPIO_PRT1_DR_CLR	0x40040144	FULL	Port output data clear register
GPIO_PRT1_DR_INV	0x40040148	FULL	Port output data invert register

6.3 PRT 2

Register Name	Address	Permission	Description
GPIO_PRT2_DR	0x40040200	FULL	Port output data register Note:DATA3 DATA4 DATA5 DATA6 DATA7 are not available for this register
GPIO_PRT2_PS	0x40040204	FULL	Port IO pad state register Note:DATA3 DATA4 DATA5 DATA6 DATA7 are not available for this register
GPIO_PRT2_INTR_CFG	0x4004020C	FULL	Port interrupt configuration register Note:EDGE3_SEL EDGE4_SEL EDGE5_SEL EDGE6_SEL EDGE7_SEL are not available for this register
GPIO_PRT2_INTR	0x40040210	FULL	Port interrupt status register Note:DATA3 DATA4 DATA5 DATA6 DATA7 PS_DATA3 PS_DATA4 PS_DATA5 PS_DATA6 PS_DATA7 are not available for this register
GPIO_PRT2_DR_SET	0x40040240	FULL	Port output data set register
GPIO_PRT2_DR_CLR	0x40040244	FULL	Port output data clear register
GPIO_PRT2_DR_INV	0x40040248	FULL	Port output data invert register

6.4 PRT 3

Register Name	Address	Permission	Description
GPIO_PRT3_DR	0x40040300	FULL	Port output data register Note:DATA6 DATA7 are not available for this register
GPIO_PRT3_PS	0x40040304	FULL	Port IO pad state register Note:DATA6 DATA7 are not available for this register
GPIO_PRT3_PC	0x40040308	FULL	Port configuration register Note:DM6 DM7 PORT_HYST_TRIM PORT_SLEW_CTL are not available for this register
GPIO_PRT3_INTR_CFG	0x4004030C	FULL	Port interrupt configuration register Note:EDGE6_SEL EDGE7_SEL are not available for this register
GPIO_PRT3_INTR	0x40040310	FULL	Port interrupt status register Note:DATA6 DATA7 PS_DATA6 PS_DATA7 are not available for this register
GPIO_PRT3_PC2	0x40040318	FULL	Port configuration register 2 Note:INP_DIS6 INP_DIS7 are not available for this register
GPIO_PRT3_DR_SET	0x40040340	FULL	Port output data set register
GPIO_PRT3_DR_CLR	0x40040344	FULL	Port output data clear register
GPIO_PRT3_DR_INV	0x40040348	FULL	Port output data invert register

6.5 PRT 4

Register Name	Address	Permission	Description
GPIO_PRT4_DR	0x40040400	FULL	Port output data register
GPIO_PRT4_PS	0x40040404	FULL	Port IO pad state register
GPIO_PRT4_PC	0x40040408	FULL	Port configuration register Note:PORT_HYST_TRIM PORT_SLEW_CTL are not available for this register
GPIO_PRT4_INTR_CFG	0x4004040C	FULL	Port interrupt configuration register
GPIO_PRT4_INTR	0x40040410	FULL	Port interrupt status register
GPIO_PRT4_PC2	0x40040418	FULL	Port configuration register 2
GPIO_PRT4_DR_SET	0x40040440	FULL	Port output data set register
GPIO_PRT4_DR_CLR	0x40040444	FULL	Port output data clear register
GPIO_PRT4_DR_INV	0x40040448	FULL	Port output data invert register

6.6 PRT 5

Register Name	Address	Permission	Description
GPIO_PRT5_DR	0x40040500	FULL	Port output data register
GPIO_PRT5_PS	0x40040504	FULL	Port IO pad state register
GPIO_PRT5_PC	0x40040508	FULL	Port configuration register Note:PORT_HYST_TRIM PORT_SLEW_CTL are not available for this register
GPIO_PRT5_INTR_CFG	0x4004050C	FULL	Port interrupt configuration register
GPIO_PRT5_INTR	0x40040510	FULL	Port interrupt status register
GPIO_PRT5_PC2	0x40040518	FULL	Port configuration register 2
GPIO_PRT5_DR_SET	0x40040540	FULL	Port output data set register
GPIO_PRT5_DR_CLR	0x40040544	FULL	Port output data clear register
GPIO_PRT5_DR_INV	0x40040548	FULL	Port output data invert register

6.7 PRT 6

Register Name	Address	Permission	Description
GPIO_PRT6_DR	0x40040600	FULL	Port output data register Note:DATA1 DATA2 DATA3 DATA4 DATA5 DATA6 DATA7 are not available for this register
GPIO_PRT6_PS	0x40040604	FULL	Port IO pad state register Note:DATA1 DATA2 DATA3 DATA4 DATA5 DATA6 DATA7 are not available for this register
GPIO_PRT6_PC	0x40040608	FULL	Port configuration register Note:DM1 DM2 DM3 DM4 DM5 DM6 DM7 PORT_HYST_TRIM PORT_SLEW_CTL are not available for this register
GPIO_PRT6_INTR_CFG	0x4004060C	FULL	Port interrupt configuration register Note:EDGE1_SEL EDGE2_SEL EDGE3_SEL EDGE4_SEL EDGE5_SEL EDGE6_SEL EDGE7_SEL are not available for this register

Register Name	Address	Permission	Description
GPIO_PRT6_INTR	0x40040610	FULL	Port interrupt status register Note:DATA1 DATA2 DATA3 DATA4 DATA5 DATA6 DATA7 PS_DATA1 PS_DATA2 PS_DATA3 PS_DATA4 PS_DATA5 PS_DATA6 PS_DATA7 are not available for this register
GPIO_PRT6_PC2	0x40040618	FULL	Port configuration register 2 Note:INP_DIS1 INP_DIS2 INP_DIS3 INP_DIS4 INP_DIS5 INP_DIS6 INP_DIS7 are not available for this register
GPIO_PRT6_DR_SET	0x40040640	FULL	Port output data set register
GPIO_PRT6_DR_CLR	0x40040644	FULL	Port output data clear register
GPIO_PRT6_DR_INV	0x40040648	FULL	Port output data invert register

6.8 PRT 7

Register Name	Address	Permission	Description
GPIO_PRT7_DR	0x40040700	FULL	Port output data register Note:DATA2 DATA3 DATA4 DATA5 DATA6 DATA7 are not available for this register
GPIO_PRT7_PS	0x40040704	FULL	Port IO pad state register Note:DATA2 DATA3 DATA4 DATA5 DATA6 DATA7 are not available for this register
GPIO_PRT7_PC	0x40040708	FULL	Port configuration register Note:DM2 DM3 DM4 DM5 DM6 DM7 PORT_HYST_TRIM PORT_SLEW_CTL are not available for this register
GPIO_PRT7_INTR_CFG	0x4004070C	FULL	Port interrupt configuration register Note:EDGE2_SEL EDGE3_SEL EDGE4_SEL EDGE5_SEL EDGE6_SEL EDGE7_SEL are not available for this register
GPIO_PRT7_INTR	0x40040710	FULL	Port interrupt status register Note:DATA2 DATA3 DATA4 DATA5 DATA6 DATA7 PS_DATA2 PS_DATA3 PS_DATA4 PS_DATA5 PS_DATA6 PS_DATA7 are not available for this register
GPIO_PRT7_PC2	0x40040718	FULL	Port configuration register 2 Note:INP_DIS2 INP_DIS3 INP_DIS4 INP_DIS5 INP_DIS6 INP_DIS7 are not available for this register
GPIO_PRT7_DR_SET	0x40040740	FULL	Port output data set register
GPIO_PRT7_DR_CLR	0x40040744	FULL	Port output data clear register
GPIO_PRT7_DR_INV	0x40040748	FULL	Port output data invert register

6.9 Register Details

6.9.1 GPIO_INTR_CAUSE

Description: Interrupt port cause register
Address: 0x40041000
Offset: 0x1000
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	PORT_INT [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:7	PORT_INT	R	W	0	Each IO port has an associated bit field in this register. The bit field reflects the IO port's interrupt line (bit field i reflects 'interrupts_gpio[i]' for IO port i). The register is used when the system uses a shared/combined interrupt line 'interrupt_gpio'. The SW ISR reads the register to determine which IO port(s) is responsible for the shared/combined interrupt line 'interrupt_gpio'. Once, the IO port(s) is determined, the IO port's INTR register is read to determine the IO pad(s) in the IO port that caused the interrupt.

6.9.2 GPIO_DFT_IO_TEST

Description: IO SELF TEST control register for DfT purposes only
Address: 0x40041010
Offset: 0x1010
Retention: Retained
IsDeepSleep: No
Comment: This register is used to significantly reduce the test time for IO cells. It also avoids the need to develop a large amount of chip specific functional test vectors.
With ATPG it is not possible to get full stuck-at fault coverage for some IO cell inputs ('hld_ovr, oe_n, analog_en, analog_sel, analog_pol'). This register gives direct controllability on those inputs of all IO cells by bypassing the functional paths. That allows generic (not chip specific) ROOS code (also SWD IO cells are included) to get DfT fault-coverage for these signals. This register is used in conjunction with the GPIO.PC.dm[2:0], GPIO.DR.out and SRSS.CORE.PWR_STOP.FREEZE for control and results are observed through GPIO.PS.data.
Only one IO cell on the whole chip gets IO_TEST_0 and only one gets IO_TEST_1 and default values of IO_TEST_0 is '0' and IO_TEST_1 is '1'. Also only one IO cell on the whole chip gets assigned ADFT-0 and only one gets assigned ADFT-1. All four IO_TEST_0/1 and ADFT-0/1 pins are assigned in the product pin spreadsheet.
Default: 0x2020200

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:2]						DFT_IO_TEST_MODE [1:0]	

Bits	15	14	13	12	11	10	9	8
Name	None [15:13]			DFT_ANA_POL_0 [12:12]	DFT_ANA_SEL_0 [11:11]	DFT_ANALOG_EN_0 [10:10]	DFT_OE_N_0 [9:9]	DFT_HLD_OVR_0 [8:8]

Bits	23	22	21	20	19	18	17	16
Name	None [23:21]			DFT_ANA_POL_1 [20:20]	DFT_ANA_SEL_1 [19:19]	DFT_ANALOG_EN_1 [18:18]	DFT_OE_N_1 [17:17]	DFT_HLD_OVR_1 [16:16]

Bits	31	30	29	28	27	26	25	24
Name	None [31:29]			DFT_ANA_POL_2 [28:28]	DFT_ANA_SEL_2 [27:27]	DFT_ANALOG_EN_2 [26:26]	DFT_OE_N_2 [25:25]	DFT_HLD_OVR_2 [24:24]

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:1	DFT_IO_TEST_MODE	RW	R	0	DfT IO SELF TEST mode:
	OFF			0	Functional mode: disables the DfT IO SELF TEST; none of the 'DFT_*' control signals from this register control the IO cells.
	TEST_ADFT			1	select this mode during ADFT testing to control 'hld_ovr/oe_n/ analog_sel/ analog_pol/ analog_en' signals of IO cells as below: the ADFT-0 assigned IO cell connects to: DFT_*_0; the ADFT-1 assigned IO cell connects to: DFT_*_1; All other IO cells connect to: DFT_*_2;

Bits	Name	SW	HW	Default or Enum	Description
	TEST_ANA			2	select this mode for testing analog switches to control 'hld_ovr/oe_n/analog_en/analog_sel/analog_pol' signals of IO cells as below: the IO_TEST_0 assigned IO cell connects to: DFT_*_0; the IO_TEST_1 assigned IO cell connects to: DFT_*_1; All other IO cells connect to: DFT_*_2;
	TEST_GEN			3	select this mode for generic testing to control 'hld_ovr/oe_n/analog_en/analog_sel/analog_pol' signals of IO cells as below: All IO cells connect to: DFT_*_2;
8	DFT_HLD_OVR_0	RW	R	0	'hld_ovr' DfT control for IO cells depending on DFT_IO_TEST_MODE as given below. TEST_ADFT: Connects to 'hld_ovr' of the ADFT-0 assigned IO cell. TEST_ANA: Connects to 'hld_ovr' of the IO_TEST_0 assigned IO cell. TEST_GEN: not used.
9	DFT_OE_N_0	RW	R	1	'oe_n' DfT control for IO cells depending on DFT_IO_TEST_MODE as given below. TEST_ADFT: Connects to 'oe_n' of the ADFT-0 assigned IO cell. TEST_ANA: Connects to 'oe_n' of the IO_TEST_0 assigned IO cell. TEST_GEN: not used.
10	DFT_ANALOG_EN_0	RW	R	0	'analog_en' DfT control for IO cells depending on DFT_IO_TEST_MODE as given below. TEST_ADFT: Connects to 'analog_en' of the ADFT-0 assigned IO cell. TEST_ANA: Connects to 'analog_en' of the IO_TEST_0 assigned IO cell. TEST_GEN: not used.
11	DFT_ANA_SEL_0	RW	R	0	'analog_sel' DfT control for IO cells depending on DFT_IO_TEST_MODE as given below. TEST_ADFT: Connects to 'analog_sel' of the ADFT-0 assigned IO cell. TEST_ANA: Connects to 'analog_sel' of the IO_TEST_0 assigned IO cell. TEST_GEN: not used.
12	DFT_ANA_POL_0	RW	R	0	'analog_pol' DfT control for IO cells depending on DFT_IO_TEST_MODE as given below. TEST_ADFT: Connects to 'analog_pol' of the ADFT-0 assigned IO cell. TEST_ANA: Connects to 'analog_pol' of the IO_TEST_0 assigned IO cell. TEST_GEN: not used.
16	DFT_HLD_OVR_1	RW	R	0	'hld_ovr' DfT control for IO cells depending on DFT_IO_TEST_MODE as given below. TEST_ADFT: Connects to 'hld_ovr' of the ADFT-1 assigned IO cell. TEST_ANA: Connects to 'hld_ovr' of the IO_TEST_1 assigned IO cell. TEST_GEN: not used.
17	DFT_OE_N_1	RW	R	1	'oe_n' DfT control for IO cells depending on DFT_IO_TEST_MODE as given below. TEST_ADFT: Connects to 'oe_n' of the ADFT-1 assigned IO cell. TEST_ANA: Connects to 'oe_n' of the IO_TEST_1 assigned IO cell. TEST_GEN: not used.

Bits	Name	SW	HW	Default or Enum	Description
18	DFT_ANALOG_EN_1	RW	R	0	'analog_en' DfT control for IO cells depending on DFT_IO_TEST_MODE as given below. TEST_ADFT: Connects to 'analog_en' of the ADFT-1 assigned IO cell. TEST_ANA: Connects to 'analog_en' of the IO_TEST_1 assigned IO cell. TEST_GEN: not used.
19	DFT_ANA_SEL_1	RW	R	0	'analog_sel' DfT control for IO cells depending on DFT_IO_TEST_MODE as given below. TEST_ADFT: Connects to 'analog_sel' of the ADFT-1 assigned IO cell. TEST_ANA: Connects to 'analog_sel' of the IO_TEST_1 assigned IO cell. TEST_GEN: not used.
20	DFT_ANA_POL_1	RW	R	0	'analog_pol' DfT control for IO cells depending on DFT_IO_TEST_MODE as given below. TEST_ADFT: Connects to 'analog_pol' of the ADFT-1 assigned IO cell. TEST_ANA: Connects to 'analog_pol' of the IO_TEST_1 assigned IO cell. TEST_GEN: not used.
24	DFT_HLD_OVR_2	RW	R	0	'hld_ovr' DfT control for IO cells depending on DFT_IO_TEST_MODE as given below. TEST_ADFT: Connects to 'hld_ovr' of all IO cells other than ADFT-0/1 . TEST_ANA: Connects to 'hld_ovr' of all IO cells other than IO_TEST_0/1. TEST_GEN: Connects to 'hld_ovr' of all IO cells.
25	DFT_OE_N_2	RW	R	1	'oe_n' DfT control for IO cells depending on DFT_IO_TEST_MODE as given below. TEST_ADFT: Connects to 'oe_n' of all IO cells other than ADFT-0/1. TEST_ANA: Connects to 'oe_n' of all IO cells other than IO_TEST_0/1. TEST_GEN: Connects to 'oe_n' of all IO cells
26	DFT_ANALOG_EN_2	RW	R	0	'analog_en' DfT control for IO cells depending on DFT_IO_TEST_MODE as given below. TEST_ADFT: Connects to 'analog_en' of all IO cells other than ADFT-0/1. TEST_ANA: DFT_ANALOG_EN_2 && DM[0] connects to 'analog_en' of all IO cells other than IO_TEST_0/1. TEST_GEN: Connects to 'analog_en' of all IO cells
27	DFT_ANA_SEL_2	RW	R	0	'analog_sel' DfT control for IO cells depending on DFT_IO_TEST_MODE as given below. TEST_ADFT: Connects to 'analog_sel' of all IO cells other than ADFT-0/1. TEST_ANA: Connects to 'analog_sel' of all IO cells other than IO_TEST_0/1. TEST_GEN: Connects to 'analog_sel' of all IO cells.
28	DFT_ANA_POL_2	RW	R	0	'analog_pol' DfT control for IO cells depending on DFT_IO_TEST_MODE as given below. TEST_ADFT: Connects to 'analog_pol' of all IO cells other than ADFT-0/1. TEST_ANA: Connects to 'analog_pol' of all IO cells other than IO_TEST_0/1. TEST_GEN: Connects to 'analog_pol' of all IO cells.

6.9.3 PRT

6.9.3.1 GPIO_PRT_DR

Description: Port output data register
Address: 0x40040000
Offset: 0x0
Retention: Retained
IsDeepSleep: No
Comment: Used to read and write the output data for the IO pads in the port. A DR register write changes the output data to the written value. A DR register read reflects the output data (and not the current state of the input data for the IO pads). Using this DR register, Read-Modify-Write sequences are safely performed on a port with some IO pads configured as inputs.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	DATA7 [7:7]	DATA6 [6:6]	DATA5 [5:5]	DATA4 [4:4]	DATA3 [3:3]	DATA2 [2:2]	DATA1 [1:1]	DATA0 [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	DATA0	RW	RW	0	IO pad 0 output data.
1	DATA1	RW	RW	0	IO pad 1 output data.
2	DATA2	RW	RW	0	IO pad 2 output data.
3	DATA3	RW	RW	0	IO pad 3 output data.
4	DATA4	RW	RW	0	IO pad 4 output data.
5	DATA5	RW	RW	0	IO pad 5 output data.
6	DATA6	RW	RW	0	IO pad 6 output data.
7	DATA7	RW	RW	0	IO pad 7 output data.

6.9.3.2 GPIO_PRT_PS

Description: Port IO pad state register
Address: 0x40040004
Offset: 0x4
Retention: Not Retained
IsDeepSleep: No
Comment: Used to read. Writes to this register have no effect. If the drive mode for the pin is set to high Z Analog, the state will read 0 independent of the voltage on the pin.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	DATA7 [7:7]	DATA6 [6:6]	DATA5 [5:5]	DATA4 [4:4]	DATA3 [3:3]	DATA2 [2:2]	DATA1 [1:1]	DATA0 [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:9]							FLT_DATA [8:8]

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	DATA0	R	W	0	IO pad 0 state: 1: Logic high, if the pin voltage is above the input buffer threshold, logic high. 0: Logic low, if the pin voltage is below that threshold, logic low. If the drive mode for the pin is set to high Z Analog, the pin state will read 0 independent of the voltage on the pin.
1	DATA1	R	W	0	IO pad 1 state.
2	DATA2	R	W	0	IO pad 2 state.
3	DATA3	R	W	0	IO pad 3 state.
4	DATA4	R	W	0	IO pad 4 state.
5	DATA5	R	W	0	IO pad 5 state.
6	DATA6	R	W	0	IO pad 6 state.
7	DATA7	R	W	0	IO pad 7 state.
8	FLT_DATA	R	W	0	Reads of this register return the logical state of the filtered pin.

6.9.3.3 GPIO_PRT_PC

Description: Port configuration register
Address: 0x40040008
Offset: 0x8
Retention: Retained
IsDeepSleep: No
Comment: Configures the output drive and input buffer state for each pin, and the slew rate and input threshold selection for the whole port. One register is provided per port.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name			DM1 [5:3]			DM0 [2:0]		

Bits	15	14	13	12	11	10	9	8
Name		DM4 [14:12]			DM3 [11:9]			DM2 [8:8]

Bits	23	22	21	20	19	18	17	16
Name	DM7 [23:21]			DM6 [20:18]			DM5 [17:16]	

Bits	31	30	29	28	27	26	25	24
Name	PORT_IB_MODE_SEL [31:30]		None [29:26]				PORT _SLOW [25:25]	PORT _VTRIP _SEL [24:24]

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:2	DM0	RW	R	0	The GPIO drive mode for IO pad 0. Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the HSIOM is properly configured (HSIOM_PRT_SELx) before turning the IO on here to avoid producing glitches on the bus.
	OFF			0	Mode 0 (analog mode): Output buffer off (high Z). Input buffer off.
	INPUT			1	Mode 1: Output buffer off (high Z). Input buffer on.
	0_PU			2	Mode 2: Strong pull down ('0'), weak/resistive pull up (PU). Input buffer on. For GPIOV1P2_I2C, Strong pull down only.
	PD_1			3	Mode 3: Weak/resistive pull down (PD), strong pull up ('1'). Input buffer on. For GPIOV1P2_I2C: Weak pull down only.
	0_Z			4	Mode 4: Strong pull down ('0'), open drain (pull up off). Input buffer on. For GPIOV1P2_I2C, Strong pull down only.
	Z_1			5	Mode 5: Open drain (pull down off), strong pull up ('1'). Input buffer on. Illegal for GPIOV1P2_I2C
	0_1			6	Mode 6: Strong pull down ('0'), strong pull up ('1'). Input buffer on. For GPIOV1P2_I2C, Strong pull down only.
	PD_PU			7	Mode 7: Weak/resistive pull down (PD), weak/resistive pull up (PU). Input buffer on. For GPIOV1P2_I2C: Weak pull down only.
3:5	DM1	RW	R	0	The GPIO drive mode for IO pad 1.
6:8	DM2	RW	R	0	The GPIO drive mode for IO pad 2.
9:11	DM3	RW	R	0	The GPIO drive mode for IO pad 3.
12:14	DM4	RW	R	0	The GPIO drive mode for IO pad 4.

Bits	Name	SW	HW	Default or Enum	Description
15:17	DM5	RW	R	0	The GPIO drive mode for IO pad 5.
18:20	DM6	RW	R	0	The GPIO drive mode for IO pad 6.
21:23	DM7	RW	R	0	The GPIO drive mode for IO pad 7.
24	PORT_VTRIP_SEL	RW	R	0	The GPIO cells include a VTRIP_SEL signal to alter the input buffer voltage. Note: this bit is ignored for SIO ports, the VTRIP_SEL settings in the SIO register are used instead (a separate VTRIP_SEL is provided for each pin pair). 0: input buffer functions as a CMOS input buffer. 1: input buffer functions as a LVTTL input buffer. For GPIOV1P2 and GPIOV1P_I2C cells, PC.PORT_VTRIP_SEL is unused. Refer to DS register
25	PORT_SLOW	RW	R	0	This field controls the output edge rate of all pins on the port: '0': fast. '1': slow.
30:31	PORT_IB_MODE_SEL	RW	R	0	This field selects the input buffer reference. The size (1 or 2 bits) and functionality is dependent on the IO cell. For GPIOv2 IO cells, bit PORT_IB_MODE_SEL[1] is not used (GPIOv2 IO cell replaces GPIO IO cell): '0'/'2': CMOS input buffer (PORT_VTRIP_SEL is '0'), LVTTL input buffer (PORT_VTRIP_SEL is '1') '1'/'3': vcchib. For GPIO_OVTv2 and SIOv2 IO cells: '0': CMOS input buffer (PORT_VTRIP_SEL is '0'), LVTTL input buffer (PORT_VTRIP_SEL is '1') '1': vcchib. '2': OVT. '3': Reference (possibly from reference generator cell). For SIO IO cell, this field is present but not used as the SIO IO cell does not provide input buffer mode select functionality (SIOv2 IO cell will replace SIO IO cell, as soon as it is available). For GPIOV1P2 and GPIOV1P2_I2C cells, PC.PORT_IB_MODE_SEL unused. Refer to DS register.

6.9.3.4 GPIO_PRT_INTR_CFG

Description: Port interrupt configuration register
Address: 0x4004000C
Offset: 0xC
Retention: Retained
IsDeepSleep: No
Comment: This register configures the IRQ configuration for all pins in a port, with the IRQ type being individually pin-configurable.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	EDGE3_SEL [7:6]		EDGE2_SEL [5:4]		EDGE1_SEL [3:2]		EDGE0_SEL [1:0]	

Bits	15	14	13	12	11	10	9	8
Name	EDGE7_SEL [15:14]		EDGE6_SEL [13:12]		EDGE5_SEL [11:10]		EDGE4_SEL [9:8]	

Bits	23	22	21	20	19	18	17	16
Name	None [23:21]			FLT_SEL [20:18]			FLT_EDGE_SEL [17:16]	

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:1	EDGE0_SEL	RW	R	0	Sets which edge will trigger an IRQ for IO pad 0.
	DISABLE			0	Disabled
	RISING			1	Rising edge
	FALLING			2	Falling edge
	BOTH			3	Both rising and falling edges
2:3	EDGE1_SEL	RW	R	0	Sets which edge will trigger an IRQ for IO pad 1.
4:5	EDGE2_SEL	RW	R	0	Sets which edge will trigger an IRQ for IO pad 2.
6:7	EDGE3_SEL	RW	R	0	Sets which edge will trigger an IRQ for IO pad 3.
8:9	EDGE4_SEL	RW	R	0	Sets which edge will trigger an IRQ for IO pad 4.
10:11	EDGE5_SEL	RW	R	0	Sets which edge will trigger an IRQ for IO pad 5.
12:13	EDGE6_SEL	RW	R	0	Sets which edge will trigger an IRQ for IO pad 6.
14:15	EDGE7_SEL	RW	R	0	Sets which edge will trigger an IRQ for IO pad 7.
16:17	FLT_EDGE_SEL	RW	R	0	Same for the glitch filtered pin (selected by FLT_SEL).
	DISABLE			0	Disabled
	RISING			1	Rising edge
	FALLING			2	Falling edge
	BOTH			3	Both rising and falling edges
18:20	FLT_SEL	RW	R	0	Selects which pin is routed through the 50ns glitch filter to provide a glitch-safe interrupt.

6.9.3.5 GPIO_PRT_INTR

Description: Port interrupt status register
Address: 0x40040010
Offset: 0x10
Retention: Retained
IsDeepSleep: No
Comment: An interrupt cause is cleared (set to '0') by writing a '1' to the corresponding bit field. It is not recommended to write 0xff to clear all interrupt causes, as a new interrupt cause may have occurred between reading the register and clearing. Note that the interrupt cause fields and the associated interrupt provide Hibernate functionality (interrupt causes can be set to '1' and the interrupt can be activated in Hibernate power mode). The PS_DATA fields reflect the logical IO pad states of the port (also found in the PS register).
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	DATA7 [7:7]	DATA6 [6:6]	DATA5 [5:5]	DATA4 [4:4]	DATA3 [3:3]	DATA2 [2:2]	DATA1 [1:1]	DATA0 [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:9]							FLT_DATA [8:8]

Bits	23	22	21	20	19	18	17	16
Name	PS_DATA7 [23:23]	PS_DATA6 [22:22]	PS_DATA5 [21:21]	PS_DATA4 [20:20]	PS_DATA3 [19:19]	PS_DATA2 [18:18]	PS_DATA1 [17:17]	PS_DATA0 [16:16]

Bits	31	30	29	28	27	26	25	24
Name	None [31:25]							PS_FLT_DATA [24:24]

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	DATA0	RW1C	A	0	Interrupt pending on IO pad 0. Firmware writes 1 to clear the interrupt.
1	DATA1	RW1C	A	0	Interrupt pending on IO pad 1. Firmware writes 1 to clear the interrupt.
2	DATA2	RW1C	A	0	Interrupt pending on IO pad 2. Firmware writes 1 to clear the interrupt.
3	DATA3	RW1C	A	0	Interrupt pending on IO pad 3. Firmware writes 1 to clear the interrupt.
4	DATA4	RW1C	A	0	Interrupt pending on IO pad 4. Firmware writes 1 to clear the interrupt.
5	DATA5	RW1C	A	0	Interrupt pending on IO pad 5. Firmware writes 1 to clear the interrupt.
6	DATA6	RW1C	A	0	Interrupt pending on IO pad 6. Firmware writes 1 to clear the interrupt.
7	DATA7	RW1C	A	0	Interrupt pending on IO pad 7. Firmware writes 1 to clear the interrupt.
8	FLT_DATA	RW1C	A	0	Deglitched interrupt pending (selected by FLT_SEL).
16	PS_DATA0	R	W	0	`
17	PS_DATA1	R	W	0	N/A
18	PS_DATA2	R	W	0	N/A
19	PS_DATA3	R	W	0	N/A
20	PS_DATA4	R	W	0	N/A
21	PS_DATA5	R	W	0	N/A
22	PS_DATA6	R	W	0	N/A

Bits	Name	SW	HW	Default or Enum	Description
23	PS_DATA7	R	W	0	N/A
24	PS_FLT_DATA	R	W	0	This is a duplicate of the contents of the PS register, provided here to allow reading of both pin state and interrupt state of the port in a single read operation.

6.9.3.6 GPIO_PRT_PC2

Description: Port configuration register 2
Address: 0x40040018
Offset: 0x18
Retention: Retained
IsDeepSleep: No
Comment: Configures the input disable for each pin.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	INP_DIS7 [7:7]	INP_DIS6 [6:6]	INP_DIS5 [5:5]	INP_DIS4 [4:4]	INP_DIS3 [3:3]	INP_DIS2 [2:2]	INP_DIS1 [1:1]	INP_DIS0 [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	INP_DIS0	RW	R	0	Disables the input buffer for IO pad 0 independent of the port control drive mode (PC.DM). This bit should be set when analog signals are present on the pin and PC.DM != 0 is required to use the output driver.
1	INP_DIS1	RW	R	0	Disables the input buffer for IO pad 1.
2	INP_DIS2	RW	R	0	Disables the input buffer for IO pad 2.
3	INP_DIS3	RW	R	0	Disables the input buffer for IO pad 3.
4	INP_DIS4	RW	R	0	Disables the input buffer for IO pad 4.
5	INP_DIS5	RW	R	0	Disables the input buffer for IO pad 5.
6	INP_DIS6	RW	R	0	Disables the input buffer for IO pad 6.
7	INP_DIS7	RW	R	0	Disables the input buffer for IO pad 7.

6.9.3.7 GPIO_PRT_DR_SET

Description: Port output data set register
Address: 0x40040040
Offset: 0x40
Retention: Retained
IsDeepSleep: No
Comment: Used to set output data of specific IO pads in the corresponding port to '1', without affecting the output data of the other IO pads in the port. A DR_SET register read returns the same value as a DR register read.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:7	DATA	RW	A	0	IO pad i: '0': Output state DR.DATA[i] not affected. '1': Output state DR.DATA[i] set to '1'.

6.9.3.8 GPIO_PRT_DR_CLR

Description: Port output data clear register
Address: 0x40040044
Offset: 0x44
Retention: Retained
IsDeepSleep: No
Comment: Used to clear output data of specific IO pads in the corresponding port to '0', without affecting the output data of the other IO pads in the port. A DR_CLR register read returns the same value as a DR register read.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:7	DATA	RW	A	0	IO pad i: '0': Output state DR.DATA[i] not affected. '1': Output state DR.DATA[i] set to '0'.

6.9.3.9 GPIO_PRT_DR_INV

Description: Port output data invert register
Address: 0x40040048
Offset: 0x48
Retention: Retained
IsDeepSleep: No
Comment: Used to invert output data of specific IO pads in the corresponding port, without affecting the output data of the other IO pads in the port. A DR_INV register read returns the same value as a DR register read.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:7	DATA	RW	A	0	IO pad i: '0': Output state DR.DATA[i] not affected. '1': Output state DR.DATA[i] inverted ('0' => '1', '1' => '0').

7 HSIOM

Description High Speed IO Matrix (HSIOM)
Base Address 0x40020000
Size 0x4000
Slave Num MMIO0

Register Name	Address	Permission	Description
HSIOM_PUMP_CTL	0x40022000	FULL	Pump control
HSIOM_AMUX_SPLIT_CTL0	0x40022100	FULL	AMUX splitter cell control
HSIOM_AMUX_SPLIT_CTL1	0x40022104	FULL	AMUX splitter cell control

7.1 PRT 0

Register Name	Address	Permission	Description
HSIOM_PORT_SEL0	0x40020000	FULL	Port selection register

7.2 PRT 1

Register Name	Address	Permission	Description
HSIOM_PORT_SEL1	0x40020100	FULL	Port selection register

7.3 PRT 2

Register Name	Address	Permission	Description
HSIOM_PORT_SEL2	0x40020200	FULL	Port selection register Note:IO3_SEL IO4_SEL IO5_SEL IO6_SEL IO7_SEL are not available for this register

7.4 PRT 3

Register Name	Address	Permission	Description
HSIOM_PORT_SEL3	0x40020300	FULL	Port selection register Note:IO6_SEL IO7_SEL are not available for this register

7.5 PRT 4

Register Name	Address	Permission	Description
HSIOM_PORT_SEL4	0x40020400	FULL	Port selection register

7.6 PRT 5

Register Name	Address	Permission	Description
HSIOM_PORT_SEL5	0x40020500	FULL	Port selection register

7.7 PRT 6

Register Name	Address	Permission	Description
HSIOM_PORT_SEL6	0x40020600	FULL	Port selection register Note:IO1_SEL IO2_SEL IO3_SEL IO4_SEL IO5_SEL IO6_SEL IO7_SEL are not available for this register

7.8 PRT 7

Register Name	Address	Permission	Description
HSIOM_PORT_SEL7	0x40020700	FULL	Port selection register Note:IO2_SEL IO3_SEL IO4_SEL IO5_SEL IO6_SEL IO7_SEL are not available for this register

7.9 Register Details

7.9.1 HSIOM_PUMP_CTL

Description: Pump control
Address: 0x40022000
Offset: 0x2000
Retention: Retained
IsDeepSleep: No
Comment: This register ONLY exists when there is no PASS in a design. The PUMP is placed in the IOSS to bias the AMUX switches.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:1]							CLOCK _SEL [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	ENABLED [31:31]	None [30:24]						

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	CLOCK_SEL	RW	R	0	Clock select: '0': External clock. '1': Internal clock (deprecated).
31	ENABLED	RW	R	0	Pump enabled: '0': Disabled. '1': Enabled.

7.9.2 HSIOM_AMUX_SPLIT_CTL

Description: AMUX splitter cell control
Address: 0x40022100
Offset: 0x2100
Retention: Retained
IsDeepSleep: No
Comment: This register controls the breaking of AMUX buses A and B into multiple segments. It allows for grounding, disconnecting and feeding through. Feeding through is be done straight (from Left segment AMUXBUSA/AMUXBUSB to Right segment AMUXBUSA/AMUXBUSB).
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:7]	SWITCH_BB_S0 [6:6]	SWITCH_BB_SR [5:5]	SWITCH_BB_SL [4:4]	None [3:3]	SWITCH_AA_S0 [2:2]	SWITCH_AA_SR [1:1]	SWITCH_AA_SL [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	SWITCH_AA_SL	RW	R	0	T-switch control for Left AMUXBUSA switch: '0': switch open. '1': switch closed.
1	SWITCH_AA_SR	RW	R	0	T-switch control for Right AMUXBUSA switch: '0': switch open. '1': switch closed.
2	SWITCH_AA_S0	RW	R	0	T-switch control for AMUXBUSA vssa/ground switch: '0': switch open. '1': switch closed.
4	SWITCH_BB_SL	RW	R	0	T-switch control for Left AMUXBUSB switch.
5	SWITCH_BB_SR	RW	R	0	T-switch control for Right AMUXBUSB switch.
6	SWITCH_BB_S0	RW	R	0	T-switch control for AMUXBUSB vssa/ground switch.

7.9.3 PRT

7.9.3.1 HSIOM_PORT_SEL

Description: Port selection register
Address: 0x40020000
Offset: 0x0
Retention: Retained
IsDeepSleep: No
Comment: Note: these fields are HW:W purely for DfT observe functionality, not for functional reasons.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	IO1_SEL [7:4]				IO0_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
Name	IO3_SEL [15:12]				IO2_SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
Name	IO5_SEL [23:20]				IO4_SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
Name	IO7_SEL [31:28]				IO6_SEL [27:24]			

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:3	IO0_SEL	RW	RW	0	Selects connection for IO pad 0 route.
	GPIO			0	SW controlled GPIO.
	GPIO_DSI			1	SW controlled 'out', DSI controlled 'oe_n'.
	DSI_DSI			2	DSI controlled 'out' and 'oe_n'.
	DSI_GPIO			3	DSI controlled 'out', SW controlled 'oe_n'.
	CSD_SENSE			4	CapSense sense connection (analog mode)
	CSD_SHIELD			5	CapSense shield connection (analog mode)
	AMUXA			6	AMUXBUS A connection.
	AMUXB			7	AMUXBUS B connection.
	ACT_0			8	Chip specific Active source 0 connection.
	ACT_1			9	Chip specific Active source 1 connection.
	ACT_2			10	Chip specific Active source 2 connection.
	ACT_3			11	Chip specific Active source 3 connection.
	LCD_COM			12	LCD common connection. This mode provides DeepSleep functionality (provided that the LCD block exists, is enabled, and is properly configured).
	LCD_SEG			13	LCD segment connection. This mode provides DeepSleep functionality (provided that the LCD block is enabled and properly configured).
	DS_0			12	Chip specific DeepSleep source 0 connection.
	DS_1			13	Chip specific DeepSleep source 1 connection.
	DS_2			14	Chip specific DeepSleep source 2 connection.
	DS_3			15	Chip specific DeepSleep source 3 connection.
4:7	IO1_SEL	RW	RW	0	Selects connection for IO pad 1 route.
8:11	IO2_SEL	RW	RW	0	Selects connection for IO pad 2 route.
12:15	IO3_SEL	RW	RW	0	Selects connection for IO pad 3 route.
16:19	IO4_SEL	RW	RW	0	Selects connection for IO pad 4 route.
20:23	IO5_SEL	RW	RW	0	Selects connection for IO pad 5 route.
24:27	IO6_SEL	RW	RW	0	Selects connection for IO pad 6 route.
28:31	IO7_SEL	RW	RW	0	Selects connection for IO pad 7 route.

8 HVSS

Description High Voltage Subsystem
Base Address 0x40060000
Size 0x10000
Slave Num MMIO0

Register Name	Address	Permission	Description
HVSS_HVREG_STATUS	0x40060000	FULL	HVREG Status Note:PWR_GOOD_SLAVE is not available for this register
HVSS_HVREG_BIST	0x40060004	FULL	HVREG Bist Note:SLAVE_ADFT is not available for this register
HVSS_HVREG_CTRL	0x40060008	FULL	HVREG Control Note:EN_SLAVE is not available for this register
HVSS_LIN_CTL	0x40060020	FULL	LIN PHY Control
HVSS_LIN_TIMER	0x40060024	FULL	LIN Timer Control
HVSS_LIN_STATUS	0x40060028	FULL	LIN Status
HVSS_LIN_BIST	0x4006002C	FULL	LIN BIST Control
HVSS_LIN_INTR	0x40060030	FULL	HVSS Interrupt Request Register
HVSS_LIN_INTR_SET	0x40060034	FULL	HVSS Interrupt set register
HVSS_LIN_INTR_MASK	0x40060038	FULL	HVSS Interrupt mask register
HVSS_LIN_INTR_MASKED	0x4006003C	FULL	HVSS Interrupt masked register
HVSS_HVSS_DDFT	0x40060040	FULL	HVSS DDFT Control
HVSS_HVREG_TRIM	0x4006FF00	FULL	HVREG Master Trim (Output Voltage)
HVSS_LIN_TRIM	0x4006FF04	FULL	LIN Trim Settings
HVSS_HVREG_TRIM_VREF	0x4006FF10	FULL	HVREG Vref Trim
HVSS_HVREG_TRIM_VREF_TC	0x4006FF14	FULL	HVREG Vref Output Voltage temp-co Trim
HVSS_HVREG_TRIM_TSD	0x4006FF18	FULL	HVREG TSD detection temperatureTrim

8.1 Register Details

8.1.1 HVSS_HVREG_STATUS

Description: HVREG Status
Address: 0x40060000
Offset: 0x0
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:4]				THERMAL_SHUTDOWN [3:3]	None [2:2]	PWR_GOOD_MAST [1:1]	PWR_GOOD [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	PWR_GOOD	R	W	0	High if regulator is settled and operating within normal limits
1	PWR_GOOD_MAST	R	W	0	Master Power Good
3	THERMAL_SHUTDOWN	R	W	0	Thermal Shutdown Active

8.1.2 HVSS_HVREG_BIST

Description: HVREG Bist
Address: 0x40060004
Offset: 0x4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:5]			HVREG _DDFT [4:4]	HVREG_ADFT [3:0]			

Bits	15	14	13	12	11	10	9	8
Name	None [15:9]							EN_BURN _IN [8:8]

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:3	HVREG_ADFT	RW	R	0	Controls ADFT switches
	NORMAL			0	Normal operation, amuxbus_a=Z
	BIAS_CIRCUIT_CURRENT_MONITOR			1	Vbias monitor
	IREF1P4V			2	N/A
	IBIAS			3	N/A
	MAST_IDRIVE			4	N/A
	MAST_TSD_GATE			5	N/A
	MAST_TSD_DIODE			6	N/A
	MAST_ZENER_GATE			7	N/A
	MAST_ILIM			8	N/A
	MAST_ILIM2			9	N/A
	TSD_VTH_VOTAGE_DET			10	N/A
	TSD_VTH_VOTAGE_REL			11	N/A
	TSD_OUT_VCCD			12	N/A
	TSD_OUT_VCCD2			13	N/A
	RESERVED_14			14	N/A
	RESERVED_15			15	N/A
4	HVREG_DDFT	RW	R	0	Enable HVREG DDFT outputs to DDFT interface when '1' (PG on ddft0, '0' on ddft1)
8	EN_BURN_IN	RW	R	0	Enable burn-in test mode with Vccd(1.8V) domain

8.1.3 HVSS_HVREG_CTRL

Description: HVREG Control
Address: 0x40060008
Offset: 0x8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x3

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:6]		TSD_MODE [5:4]		None [3:2]		ZENER_CLAMP_MODE [1:0]	

Bits	15	14	13	12	11	10	9	8
Name	None [15:9]							EN_VDIV [8:8]

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:1	ZENER_CLAMP_MODE	RW	R	3	Controls zener clamp mode
	CLAMP_NOT_PRESENT_0			0	Zener disabled
	CLAMP_NOT_PRESENT_1			1	Zener disabled
	ZENER_CLAMP_PRESENT			2	Zener enabled
	ZENER_CLAMP_DIODE_PRESENT			3	Zener and diode enabled
4:5	TSD_MODE	RW	R	0	Controls thermal shutdown mode
	KEEP_REGULATORS_ON_FOR_TSD			0	Keep Vdd on for TSD event (LIN turns off)
	TURN_OFF_REGULATORS_ON_TSD			1	Turn off Vdd and LIN on TSD event
	RESERVED_2			2	N/A
	TURN_OFF_TSD			3	Turn off TSD circuit
8	EN_VDIV	RW	R	0	Enable Vbat Voltage divider

8.1.4 HVSS_LIN_CTL

Description: LIN PHY Control
Address: 0x40060020
Offset: 0x20
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:5]			RF _DETECT [4:4]	None [3:3]	LIN_MODE [2:0]		

Bits	15	14	13	12	11	10	9	8
Name	None [15:14]		SEL_CXPI_LIN [13:12]		None [11:9]			USE_ALT_I NTERFACE [8:8]

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	LIN_EN [31:31]	None [30:24]						

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:2	LIN_MODE	RW	R	0	Controls LIN mode
	DISABLED			0	OFF (TX off, Rx off, Bias Circuits Off), LIN pin recessive
	SLEEP			1	TX off, RX on, LIN pin recessive (typically used in deep-sleep)
	STANDBY			2	TX off, RX off, Bias circuits on (faster turn-on, not normally used)
	DIAGNOSIS			3	TX on, RX on, TX w/weak pull-down (broken wire detect diag)
	NORMAL_1_0			4	TX on, RX on, 1.0V/us TX edge rate, may not meet all parameters of LIN spec at some operating conditions
	NORMAL_1_5			5	TX on, RX on, 1.5V/us TX edge rate, meets all parameters of LIN spec
	NORMAL_2_0			6	TX on, RX on, 2.0V/us TX edge rate, may not meet all parameters of LIN spec at some operating conditions
	FAST			7	Fast mode (non-lin compliant, up to 100kb/s capable)
4	RF_DETECT	RW	R	0	Renamed from SL_ROUND. 0=off; 1=on, reduce impact on LIN driver from incoming EMI.
8	USE_ALT_INTERFACE	RW	R	0	Selects Primary or Alternate interface for PHY. The primary use is to enable compliance testing by directly manipulating the PHY interface through GPIOs. 0 = Primary interface (connected to internal LIN/CXPI controller through HSIOM) 1 = Alternate interface (connected to GPIOs through HSIOM)
12:13	SEL_CXPI_LIN	RW	R	0	Selects LIN or CXPI interface. Bit 1 selects between LIN and CXPI, Bit 0 selects between CXPI master and slave
	LIN_PHY_0			0	Operates as LIN interface

Bits	Name	SW	HW	Default or Enum	Description
	LIN_PHY_1			1	Operates as LIN interface
	CXPI_MASTER			2	Operates as CXPI master
	CXPI_SLAVE			3	Operates as CXPI slave
31	LIN_EN	RW	R	0	Master enable of the LIN/CXPI interface. 0=Interface is reset and LIN pin is in Hi-Z state 1=Enable the LIN interface

8.1.5 HVSS_LIN_TIMER

Description: LIN Timer Control
Address: 0x40060024
Offset: 0x24
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	WAKEUP_TIMER [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	None [15:12]				WAKEUP_TIMER [11:8]			

Bits	23	22	21	20	19	18	17	16
Name	FAULT_TIMER [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	FAULT_TIMER_EN [31:31]	WAKEUP_TIMER_EN [30:30]	None [29:28]		FAULT_TIMER [27:24]			

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:11	WAKEUP_TIMER	RW	R	0	Number of CLK_LF edges before wakeup interrupt is triggered
16:27	FAULT_TIMER	RW	R	0	Number of CLK_LF edges before fault interrupt is triggered
30	WAKEUP_TIMER_EN	RW	R	0	Wakeup timer is running, required for full LIN compatibility if using Deep-sleep power mode
31	FAULT_TIMER_EN	RW	R	0	Dominant state fault timer is running, required for full LIN compatibility

8.1.6 HVSS_LIN_STATUS

Description: LIN Status
Address: 0x40060028
Offset: 0x28
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:1]							LIN_RXD [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	LIN_RXD	R	W	0	Current state of LIN pin, except when LIN_CTL.LIN_MODE is 0 or 2, when RXD = 1.

8.1.7 HVSS_LIN_BIST

Description: LIN BIST Control
Address: 0x4006002C
Offset: 0x2C
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:6]		LIN_DFT_START [5:5]	LIN_DDFT [4:4]	None [3:3]	LIN_ADFT [2:0]		

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:2	LIN_ADFT	RW	R	0	Enables Test Modes
	NORMAL			0	Normal Operation (DFT disabled), amuxbus_a=Z, dft<1:0>=0
	CURRENT_MONITOR_LWAVE			1	amuxbus_a=Iwave (PMOS drain), dft<1:0>=0
	VOLTAGE_MONITOR_ERRBUFF			2	amuxbus_a=ErrBuff, dft<1:0>=0
	WEAK_OUTFET			3	OUTFET = 1/10, (amuxbus_a=Z, dft<1:0>=0)
	CURRENT_MONITOR_FOR_BIAS_CKT			4	amuxbus_a=Ibias monitor (PMOS drain), dft<1:0>=0
	SL_ROUND			5	0=Normal, 1=More moderate (rounded) edge for lower EMI
	DDFT_OSC			6	amuxbus_a = Z dft<1> = LIN_DFT_START, dft<0> = LIN_OSC
	DDFT_DELAY			7	amuxbus_a = Z dft<1> = LIN_DFT_START, dft<0> = LIN_DELAY
4	LIN_DDFT	RW	R	0	Enable LIN DDFT outputs to DDFT interface ddft1 = dft<1>, ddft0 = dft<0>
5	LIN_DFT_START	RW	R	0	Delay line input

8.1.8 HVSS_LIN_INTR

Description: HVSS Interrupt Request Register
Address: 0x40060030
Offset: 0x30
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:3]					HVREG _TSD [2:2]	FAULT [1:1]	WAKEUP [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	WAKEUP	RW1C	RW1S	0	Master asserted dominant state wakeup (wakeup timer timeout)
1	FAULT	RW1C	RW1S	0	Interface asserted state for too long (dominant state timeout)
2	HVREG_TSD	RW1C	RW1S	0	Thermal Shutdown Detected

8.1.9 HVSS_LIN_INTR_SET

Description: HVSS Interrupt set register
Address: 0x40060034
Offset: 0x34
Retention: Not Retained
IsDeepSleep: No
Comment: This register asserts an interrupt - used for s/w debugging. A read returns the content of the INTR register.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:3]					HVREG_TSD [2:2]	FAULT [1:1]	WAKEUP [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	WAKEUP	RW1S	A	0	Write with '1' to set corresponding bit in interrupt request register.
1	FAULT	RW1S	A	0	Write with '1' to set corresponding bit in interrupt request register.
2	HVREG_TSD	RW1S	A	0	Write with '1' to set corresponding bit in interrupt request register.

8.1.10 HVSS_LIN_INTR_MASK

Description: HVSS Interrupt mask register
Address: 0x40060038
Offset: 0x38
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:3]					HVREG _TSD [2:2]	FAULT [1:1]	WAKEUP [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	WAKEUP	RW	R	0	Mask bit for corresponding bit in interrupt request register.
1	FAULT	RW	R	0	Mask bit for corresponding bit in interrupt request register.
2	HVREG_TSD	RW	R	0	Mask bit for corresponding bit in interrupt request register.

8.1.11 HVSS_LIN_INTR_MASKED

Description: HVSS Interrupt masked register
Address: 0x4006003C
Offset: 0x3C
Retention: Not Retained
IsDeepSleep: No
Comment: If the value is not zero then the CSD interrupt signal to the NVIC is high. When read, this register reflects a bitwise AND between the interrupt request and mask registers.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:3]					HVREG_TSD [2:2]	FAULT [1:1]	WAKEUP [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	WAKEUP	R	W	0	Logical and of corresponding request and mask bits.
1	FAULT	R	W	0	Logical and of corresponding request and mask bits.
2	HVREG_TSD	R	W	0	Logical and of corresponding request and mask bits.

8.1.12 HVSS_HVSS_DDFT

Description: HVSS DDFT Control
Address: 0x40060040
Offset: 0x40
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:1]							LSOUT _DDFT [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	LSOUT_DDFT	RW	R	0	Enable LSOUT DDFT output to DDFT interface ddft1 = lsout_ddft, ddft0 = 0

8.1.13 HVSS_HVREG_TRIM

Description: HVREG Master Trim (Output Voltage)
Address: 0x4006FF00
Offset: 0xFF00
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:6]		TRIM [5:0]					

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:5	TRIM	RW	R	0	Trim for VDDD output.

8.1.14 HVSS_LIN_TRIM

Description: LIN Trim Settings
Address: 0x4006FF04
Offset: 0xFF04
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	SLEW_CTL [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:7	SLEW_CTL	RW	R	0	SLEW_CTL trim for LIN TX_DRV, (bits 3:0 used, 7:4 reserved)

8.1.15 HVSS_HVREG_TRIM_VREF

Description: HVREG Vref Trim
Address: 0x4006FF10
Offset: 0xFF10
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:6]		VREF_CTL [5:0]					

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:5	VREF_CTL	RW	R	0	Vref Trim

8.1.16 HVSS_HVREG_TRIM_VREF_TC

Description: HVREG Vref Output Voltage temp-co Trim
Address: 0x4006FF14
Offset: 0xFF14
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:6]		TC_CTL [5:0]					

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:5	TC_CTL	RW	R	0	Vref Temperature Trim

8.1.17 HVSS_HVREG_TRIM_TSD

Description: HVREG TSD detection temperatureTrim
Address: 0x4006FF18
Offset: 0xFF18
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:6]		TSD_CTL [5:0]					

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:5	TSD_CTL	RW	R	0	TSD Trim

9 LIN

Description LIN
Base Address 0x402D0000
Size 0x10000
Slave Num MMIO1

Register Name	Address	Permission	Description
LIN0_ERROR_CTL	0x402D0000	FULL	Error control
LIN0_TEST_CTL	0x402D0004	FULL	Test control

9.1 CH 0

Register Name	Address	Permission	Description
LIN0_CH0_CTL0	0x402D8000	FULL	Control 0
LIN0_CH0_CTL1	0x402D8004	FULL	Control 1
LIN0_CH0_STATUS	0x402D8008	FULL	Status
LIN0_CH0_CMD	0x402D8010	FULL	Command
LIN0_CH0_TX_RX_STATUS	0x402D8060	FULL	TX/RX status
LIN0_CH0_PID_CHECKSUM	0x402D8080	FULL	PID and checksum
LIN0_CH0_DATA0	0x402D8084	FULL	Response data 0
LIN0_CH0_DATA1	0x402D8088	FULL	Response data 1
LIN0_CH0_INTR	0x402D80C0	FULL	Interrupt
LIN0_CH0_INTR_SET	0x402D80C4	FULL	Interrupt set
LIN0_CH0_INTR_MASK	0x402D80C8	FULL	Interrupt mask
LIN0_CH0_INTR_MASKED	0x402D80CC	FULL	Interrupt masked

9.2 CH 1

Register Name	Address	Permission	Description
LIN0_CH1_CTL0	0x402D8100	FULL	Control 0
LIN0_CH1_CTL1	0x402D8104	FULL	Control 1
LIN0_CH1_STATUS	0x402D8108	FULL	Status
LIN0_CH1_CMD	0x402D8110	FULL	Command
LIN0_CH1_TX_RX_STATUS	0x402D8160	FULL	TX/RX status
LIN0_CH1_PID_CHECKSUM	0x402D8180	FULL	PID and checksum
LIN0_CH1_DATA0	0x402D8184	FULL	Response data 0
LIN0_CH1_DATA1	0x402D8188	FULL	Response data 1
LIN0_CH1_INTR	0x402D81C0	FULL	Interrupt
LIN0_CH1_INTR_SET	0x402D81C4	FULL	Interrupt set
LIN0_CH1_INTR_MASK	0x402D81C8	FULL	Interrupt mask
LIN0_CH1_INTR_MASKED	0x402D81CC	FULL	Interrupt masked

9.3 Register Details

9.3.1 LIN_ERROR_CTL

Description: Error control
Address: 0x402D0000
Offset: 0x0
Retention: Retained
IsDeepSleep: No
Comment: This register supports error functionality: it enables HW injected channel transmitter errors. The receiver should detect these errors and report these errors through activation of corresponding interrupt causes.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:5]			CH_IDX [4:0]				

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	TX_CHECKSUM_STOP_ERROR [23:23]	TX_CHECKSUM_ERROR [22:22]	TX_DATA_STOP_ERROR [21:21]	None [20:20]	TX_PID_STOP_ERROR [19:19]	TX_PARITY_ERROR [18:18]	TX_SYNC_STOP_ERROR [17:17]	TX_SYNC_ERROR [16:16]

Bits	31	30	29	28	27	26	25	24
Name	ENABLED [31:31]	None [30:24]						

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:4	CH_IDX	RW	R	0	Specifies the channel index of the channel to which HW injected channel transmitter errors applies.
16	TX_SYNC_ERROR	RW	R	0	The synchronization field is changed from 0x55 to 0x00. At the receiver, this should result in INTR.RX_HEADER_SYNC_ERROR activation.
17	TX_SYNC_STOP_ERROR	RW	R	0	The synchronization field STOP bits are inverted to '0'. At the receiver, this should result in INTR.RX_HEADER_SYNC_ERROR or INTR.RX_HEADER_FRAME_ERROR activation.
18	TX_PARITY_ERROR	RW	R	0	In LIN mode, the PID parity bit P[1] is inverted from !(ID[5] ^ ID[4] ^ ID[3] ^ ID[1]) to (ID[5] ^ ID[4] ^ ID[3] ^ ID[1]). At the receiver, this should result in INTR.RX_HEADER_PARITY_ERROR activation. In UART mode, a data field's parity bit is inverted.
19	TX_PID_STOP_ERROR	RW	R	0	The PID field STOP bits are inverted to '0'. At the receiver, this should result in INTR.RX_HEADER_FRAME_ERROR activation.

Bits	Name	SW	HW	Default or Enum	Description
21	TX_DATA_STOP _ERROR	RW	R	0	The data field STOP bits are inverted to '0'. At the receiver, this should result in INTR.RX_RESPONSE_FRAME_ERROR activation. Note: Used in UART mode.
22	TX_CHECKSUM_ERROR	RW	R	0	The checksum field is inverted. At the receiver, this should result in INTR.RX_RESPONSE_CHECKSUM_ERROR activation.
23	TX_CHECKSUM_STOP _ERROR	RW	R	0	The checksum field STOP bits are inverted to '0'. At the receiver, this should result in INTR.RX_RESPONSE_FRAME_ERROR activation.
31	ENABLED	RW	R	0	Error injection enable: '0': Disabled. '1': Enabled.

9.3.2 LIN_TEST_CTL

Description: Test control
Address: 0x402D0004
Offset: 0x4
Retention: Retained
IsDeepSleep: No
Comment: This register support test functionality.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:5]			CH_IDX [4:0]				

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:17]							MODE [16:16]

Bits	31	30	29	28	27	26	25	24
Name	ENABLED [31:31]	None [30:24]						

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:4	CH_IDX	RW	R	0	Specifies the channel index of the channel to which test applies. The channel IO signals of channel indices CH_IDX and CH_NR-1 are connected as specified by MODE. CH_IDX should be in the range [0, CH_NR-2], as channel index CH_NR-1 is always involved in test and cannot be connected to itself. The test mode allows BOTH of the two connected channels to be tested. Note: this testing functionality simplifies SW development, but may also be used in the field to verify correct channel functionality.

Bits	Name	SW	HW	Default or Enum	Description
16	MODE	RW	R	0	Test mode: '0': Partial disconnect from IOSS. This mode's isolation allows for device test without relying on an external LIN transceiver. The IOSS 'tx' IO cell can be used to observe messages outside of the device. - tx_in[CH_IDX] = IOSS lin_tx_in[CH_IDX]. - tx_in[CH_NR-1] = IOSS lin_tx_in[CH_IDX]. - rx_in[CH_IDX] = IOSS lin_tx_in[CH_IDX]. - rx_in[CH_NR-1] = IOSS lin_tx_in[CH_IDX]. - lin_tx_out[CH_IDX] = tx_out[CH_IDX] & tx_out[CH_NR-1]. - lin_tx_out[CH_NR-1] = tx_out[CH_IDX] & tx_out[CH_NR-1]. '1': Full disconnect from IOSS (the IOSS/HSIOM should disconnect 'tx_out' from the 'tx' IO cell). This mode's isolation allows for device test without effecting an operational LIN cluster. - tx_in[CH_IDX] = lin_tx_out[CH_IDX]. - tx_in[CH_NR-1] = lin_tx_out[CH_IDX]. - rx_in[CH_IDX] = lin_tx_out[CH_IDX]. - rx_in[CH_NR-1] = lin_tx_out[CH_IDX]. - lin_tx_out[CH_IDX] = tx_out[CH_IDX] & tx_out[CH_NR-1]. - lin_tx_out[CH_NR-1] = tx_out[CH_IDX] & tx_out[CH_NR-1].
31	ENABLED	RW	R	0	Test enable: '0': Disabled. Functional mode. - tx_in[CH_IDX] = IOSS lin_tx_in[CH_IDX]. - tx_in[CH_NR-1] = IOSS lin_tx_in[CH_NR-1]. - rx_in[CH_IDX] = IOSS lin_rx_in[CH_IDX]. - rx_in[CH_NR-1] = IOSS lin_rx_in[CH_NR-1]. - lin_tx_out[CH_IDX] = tx_out[CH_IDX]. - lin_tx_out[CH_NR-1] = tx_out[CH_NR-1]. '1': Enabled. Test mode, specific test mode is specified by MODE.

9.3.3 CH

9.3.3.1 LIN_CH_CTL0

Description: Control 0
Address: 0x402D8000
Offset: 0x0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x400C0101

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:5]			AUTO_EN [4:4]	None [3:2]		STOP_BITS [1:0]	

Bits	15	14	13	12	11	10	9	8
Name	None [15:10]						BREAK_DELIMITER_LENGTH [9:8]	

Bits	23	22	21	20	19	18	17	16
Name	None [23:21]			BREAK_WAKEUP_LENGTH [20:16]				

Bits	31	30	29	28	27	26	25	24
Name	ENABLED [31:31]	FILTER_EN [30:30]	PARITY_EN [29:29]	PARITY [28:28]	BIT_ERROR_IGNORE [27:27]	None [26:25]		MODE [24:24]

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:1	STOP_BITS	RW	R	1	STOP bit periods: '0': 1/2 bit period. '1': 1 bit period. '2': 1 1/2 bit period. '3': 2 bit periods. In LIN mode, this field should be set to '1' (the default value) . In UART mode, this field can be programmed as desired. Note: receiver STOP bit frame errors can only be detected if the number of STOP bit periods is 1 or more bit period.
4	AUTO_EN	RW	R	0	LIN transceiver auto enable: '0': Disabled. '1': Enabled. The TX_RX_STATUS.EN_OUT field is controlled by HW.

Bits	Name	SW	HW	Default or Enum	Description
8:9	BREAK_DELIMITER_LENGTH	RW	R	1	In LIN mode, this field specifies the break delimiter length: (used in header transmission, not used in header reception). '0': 1 bit period. '1': 2 bit periods (default value). '2': 3 bit periods. '3': 4 bit periods. In UART mode, this field specifies the data field size: '0': 5 bit data field. '1': 6 bit data field. '2': 7 bit data field. '3': 8 bit data field. When the data field size is less than 8 bits, the most significant (unused) bits of the DATAx.DATAy[7:0] fields should be set to '0' for the transmitter.
16:20	BREAK_WAKEUP_LENGTH	RW	R	12	Break/wakeup length (minus 1) in bit periods: '0': 1 bit period. ... '10': 11 bit periods (break length for slave nodes) ... '12': 13 bit periods (break length for master nodes) ... '30': 31 bit periods. '31': Illegal (should NOT be used!!!) This field is used for transmission/reception of BOTH break and wakeup signals. Note that these functions are mutually exclusive: - When CMD.TX_HEADER is '1', the field specifies the transmitted break field. - When CMD.TX_WAKEUP is '1', the field specifies the transmitted wakeup field. - When CMD.RX_HEADER is '1', the field specifies the to be received break field. - Otherwise, the field specifies the to be received wakeup field. Per the standard, the master wakeup duration is between 250 us and 5 ms. To support uncalibrated slaves, a slave has a detection threshold of 150 us (3 bit periods at 20 kbps). After transmission of a break or wakeup signal, the INTR.TX_BREAK_WAKEUP_DONE interrupt cause is activated. After reception of a wakeup signal, the INTR.RX_BREAK_WAKEUP_DONE interrupt cause is activated. To specify longer wakeup signals in terms of absolute time (us/ms rather than bit periods), the associated PERI clock divider value can be (temporarily) increased to make the LIN bit period longer. Note: entering bus sleep mode is achieved with the 'go-to-sleep' command.
24	MODE	RW	R	0	Mode of operation: '0': LIN mode. '1': UART mode.
	LIN			0	LIN mode.
	UART			1	UART mode.

Bits	Name	SW	HW	Default or Enum	Description
27	BIT_ERROR_IGNORE	RW	R	0	Specifies behavior on a detected bit error during header or response transmission: '0': Message transfer is aborted. '1': Message transfer is NOT aborted. Note: this field does NOT effect the reporting of the bit error through INTR/STATUS.TX_HEADER/RESPONSE_BIT_ERROR; i.e. bit errors are always reported.
28	PARITY	RW	R	0	Parity mode: '0': Even parity: even number of '1' bits (including parity). '1': Odd parity. Note: Used in UART mode only.
29	PARITY_EN	RW	R	0	Parity generation enable: '0': Disabled. No parity bit is transferred. '1': Enabled. The parity bit is transferred after the last (most significant) data field bit. Note: Used in UART mode only.
30	FILTER_EN	RW	R	1	RX filter (for 'lin_rx_in'): '0': No filter. '1': Median 3 (default value) operates on the last three 'lin_rx_in' values. The sequences '000', '001', '010' and '100' result in a filtered value '0'. The sequences '111', '110', '101' and '011' result in a filtered value '1'.
31	ENABLED	RW	R	0	Channel enable: '0': Disabled. If a channel is disabled, all non-retained MMIO registers (e.g. the TX_RX_STATUS, and INTR registers) have their fields reset to their default value. '1': Enabled.

9.3.3.2 LIN_CH_CTL1

Description: Control 1
Address: 0x402D8004
Offset: 0x4
Retention: Retained
IsDeepSleep: No
Comment: A master node is aware of a message's checksum mode and number of data fields. Therefore, a master node can set the CHECKSUM_ENHANCED and DATA_NR fields accordingly, BEFORE the message header transmission.

A slave node needs to derive a message's checksum mode and number of data fields from the received PID field, AFTER the message header reception. The INTR.RX_HEADER_DONE interrupt cause indicates that the message header is received and PID_CHECKSUM.PID contains the received PID field. Slave node SW can use this PID field information to set CHECKSUM_ENHANCED and DATA_NR fields accordingly. A minimum message response consists of at least 1 data field, and the CHECKSUM_ENHANCED and DATA_NR fields need to be set BEFORE the receipt of the STOP bit(s) of the first data field; i.e. SW effectively has a data field transfer duration to set the fields.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:3]					DATA_NR [2:0]		

Bits	15	14	13	12	11	10	9	8
Name	None [15:9]							CHECKSUM_ENHANCED [8:8]

Bits	23	22	21	20	19	18	17	16
Name	FRAME_TIMEOUT [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:26]						FRAME_TIMEOUT_SEL [25:24]	

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:2	DATA_NR	RW	R	Undefined	Number of data fields (minus 1) in the response (not including the checksum): '0': 1 data field. '1': 2 data fields. ... '7': 8 data fields. Note: master and slave nodes need to agree upon the number of data fields before message transfer. In RX_RESPONSE case, When PID (header) is received, firmware has the time of one response data byte, to modify CTL1.DATA_NR.

Bits	Name	SW	HW	Default or Enum	Description
8	CHECKSUM_ ENHANCED	RW	R	Undefined	Checksum mode: '0': Classic mode. PID field is NOT included in the checksum calculation. '1': Enhanced mode. PID field is included in the checksum calculation. This mode requires special attention when the master node transmits the header and a (different) slave node transmits the response: the slave node will use the calculated partial checksum over the received PID field as a starting point for the calculation over the to be transmitted data fields. Note: If the frame identifier ID[5:0] is 0x3c or 0x3d, the classic mode will ALWAYS be used for transmission and assumed for reception, independent of the CHECKSUM_ENHANCED value.
16:23	FRAME_TIMEOUT	RW	R	Undefined	Specifies the maximum allowed length (timeout value) for a frame, frame header or frame response in bit periods. The LIN specification prescribes to set the maximum length to 1.4x the nominal length (Theader_max = 1.4 x Theader_nom and Tresponse_max = 1.4 x Tresponse_nom). The nominal header length Theader_nom is 34 bit periods and the nominal response length Tresponse_nom is 10 * (data_nr + 1) bit periods (data_nr is the number of data fields) Note: the LIN specification specifies the following: 'Tools and tests shall check the Tframe_max (= Theader_max + Tresponse_max). Nodes shall not check this time. The receiving node of the frame shall accept the frame up to the next frame slot (i.e. next break field), even if it is longer then Tframe_max).'
24:25	FRAME_TIMEOUT_SEL	RW	R	0	Specifies the frame timeout mode: '0': No timeout functionality (default value). '1': Frame mode: detects timeout from the start of break field to checksum field STOP bits (inclusive). The minimum FRAME_TIMEOUT value is 34+20 bit periods (header and a response with 1 data field). '2': Frame header mode: detects timeout from the start of break field to PID field STOP bits (inclusive). The minimum FRAME_TIMEOUT value is 34 bit periods (header). '3': Frame response mode: detects timeout from the PID field STOP bits (exclusive) to checksum field STOP bits (the response space is included in the frame response). The minimum FRAME_TIMEOUT value is 20 bit periods (response with 1 data field).

9.3.3.3 LIN_CH_STATUS

Description: Status
Address: 0x402D8008
Offset: 0x8
Retention: Not Retained
IsDeepSleep: No
Comment: The register fields are not retained. This is to ensure that they come up as '0' after coming out of DeepSleep system power mode.

This is a non-retained register; setting CTL.ENABLED to '0' clears all status fields to '0'.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:6]		RX_DATA0_FRAME_ERROR [5:5]	HEADER_RESPONSE [4:4]	DATA_IDX [3:0]			

Bits	15	14	13	12	11	10	9	8
Name	None [15:14]		RX_DONE [13:13]	TX_DONE [12:12]	None [11:10]		RX_BUSY [9:9]	TX_BUSY [8:8]

Bits	23	22	21	20	19	18	17	16
Name	None [23:18]						TX_RESPONSE_BIT_ERROR [17:17]	TX_HEADER_BIT_ERROR [16:16]

Bits	31	30	29	28	27	26	25	24
Name	None [31:29]			RX_RESPONSE_CHECKSUM_ERROR [28:28]	RX_RESPONSE_FRAME_ERROR [27:27]	RX_HEADER_PARITY_ERROR [26:26]	RX_HEADER_SYNC_ERROR [25:25]	RX_HEADER_FRAME_ERROR [24:24]

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:3	DATA_IDX	R	W	0	Number of transferred data and checksum fields in the response (also acts as an index/address into response data field and checksum field registers (DATA0, DATA1, PID_CHECKSUM)) : '0': No data fields transferred. '1': Data field 1 transferred. ... '7': Data fields 1, 2, 3, ... and 7 transferred. '8': Data fields 1, 2, 3, ... and 8 transferred. '9': Data fields 1, 2, 3, ..., 8 and checksum field transferred. '10'-'15': Unused. Set to '0' on the start of a TX_HEADER or RX_HEADER command.
4	HEADER_RESPONSE	R	W	0	Frame header / response identifier (only valid when TX_BUSY or RX_BUSY is '1'): '0': Frame header being transferred. '1': Frame response being transferred.

Bits	Name	SW	HW	Default or Enum	Description
5	RX_DATA0_FRAME_ERROR	R	W	0	Frame response, first data field frame error. HW sets this field to '1' when the received STOP bits of the first response data field have an unexpected value (only after a RX_HEADER command), and this data byte is 0x00. HW clears this field to '0' at the falling edge of SYNC start bit (after INTR.RX_HEADER_BREAK_WAKEUP_DONE). This field is used together with INTR.RX_RESPONSE_FRAME_ERROR to distinguish 'no response', 'error response' and 'correct response' scenarios. Note: The ongoing message transfer is NOT aborted.
8	TX_BUSY	R	W	0	Transmitter busy. - Set to '1' on the start of the following commands: TX_HEADER, TX_RESPONSE, TX_WAKEUP. - Set to '0' on successful completion of previous commands or when an error is detected. In the successful completion case, TX_BUSY is updated one cycle after TX_DONE. In 'TX_HEADER, RX_RESPONSE' case, set to '0' at the start bit falling edge in the first response data byte, after header transmission
9	RX_BUSY	R	W	0	Receiver busy. - Set to '1' on the start of the following commands: RX_HEADER, RX_RESPONSE. in RX_HEADER case, set at Break filed rising edge. in RX_RESPONSE case, set at the start bit falling edge in the first response data byte. - Set to '0' on successful completion of previous commands or when an error is detected. In the successful completion case, RX_BUSY is updated one cycle after RX_DONE.
12	TX_DONE	R	W	0	Transmitter done: - Set to '0' on the start of a new command. - Set to '1' on successful completion of the following command sequences (if CTL.AUTO_EN is '1', this includes the 4-bit period external transceiver disable post-amble): - TX_HEADER. - TX_HEADER, TX_RESPONSE. - RX_HEADER, TX_RESPONSE. - TX_WAKEUP.
13	RX_DONE	R	W	0	Receiver done: - Set to '0' on the start of a new command. - Set to '1' on successful completion of the following command sequences (if CTL.AUTO_EN is '1', this includes the 4-bit period external transceiver disable post-amble): - RX_HEADER, RX_RESPONSE. - TX_HEADER, RX_RESPONSE.
16	TX_HEADER_BIT_ERROR	R	W	0	Copy of INTR.TX_HEADER_BIT_ERROR.
17	TX_RESPONSE_BIT_ERROR	R	W	0	Copy of INTR.TX_RESPONSE_BIT_ERROR.
24	RX_HEADER_FRAME_ERROR	R	W	0	Copy of INTR.RX_HEADER_FRAME_ERROR.
25	RX_HEADER_SYNC_ERROR	R	W	0	Copy of INTR.RX_HEADER_SYNC_ERROR.

Bits	Name	SW	HW	Default or Enum	Description
26	RX_HEADER_PARITY_ERROR	R	W	0	Copy of INTR.RX_HEADER_PARITY_ERROR.
27	RX_RESPONSE_FRAME_ERROR	R	W	0	Copy of INTR.RX_RESPONSE_FRAME_ERROR.
28	RX_RESPONSE_CHECKSUM_ERROR	R	W	0	Copy of INTR.RX_RESPONSE_CHECKSUM_ERROR.

9.3.3.4 LIN_CH_CMD

Description: Command
Address: 0x402D8010
Offset: 0x10
Retention: Retained
IsDeepSleep: No
Comment: The register fields are retained. When a LIN channel is disabled (CTL.ENABLED is set to '0'), HW sets all the register fields to '0'.

The following restrictions apply when programming the commands:
- TX_HEADER and RX_HEADER are mutually exclusive; i.e. cannot both be set to '1'.
- TX_WAKEUP is mutually exclusive with all other commands.
- TX_RESPONSE and RX_RESPONSE are NOT mutually exclusive, but are evaluated in the following order (of decreasing priority): TX_RESPONSE, RX_RESPONSE.

The CMD.TX_HEADER register field description provides all legal command sequences. The break or wakeup detection is always enabled, regardless of CMD register setting.

Note: LIN mode supports all commands, UART mode supports the TX_HEADER and RX_HEADER commands only.

Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:3]					TX_WAKEUP [2:2]	TX_RESPONSE [1:1]	TX_HEADER [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:10]						RX_RESPONSE [9:9]	RX_HEADER [8:8]

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	TX_HEADER	RW1S	RW	0	SW sets this field to '1' to transmit a header. HW sets this field to '0' on successful completion of ANY of the following legal command sequences (also set to '0' when an error is detected): - TX_HEADER - TX_HEADER, TX_RESPONSE. - TX_HEADER, RX_RESPONSE. - RX_HEADER, TX_RESPONSE. - RX_HEADER, RX_RESPONSE. - TX_WAKEUP. The header is transmitted when the PID field STOP bits are transmitted (INTR.TX_HEADER_DONE). HW sets this field to '1', when the 'tr_cmd_tx_header' input trigger is activated. This allows for time triggered LIN message transfer. HW driven time triggered transfer eliminates the jitter that is typically associated with SW driven transfer. In UART mode, a single data field (DATA0.DATA1) is transmitted.
1	TX_RESPONSE	RW1S	RW1C	0	SW sets this field to '1' to transmit a response. HW sets this field to '0' on successful completion of ANY of the legal command sequences (also set to '0' when an error is detected). The response is transmitted when the checksum field STOP bits are transmitted (INTR.TX_RESPONSE_DONE).
2	TX_WAKEUP	RW1S	RW1C	0	SW sets this field to '1' to transmit a wakeup signal. HW sets this field to '0' on successful completion of ANY of the legal command sequences (also set to '0' when an error is detected). The command generates CTL.BREAK_WAKEUP_LENGTH bit periods in the dominant state (low/'0') and transitions to the recessive state (high/'1') (INTR.TX_WAKEUP_DONE).

Bits	Name	SW	HW	Default or Enum	Description
8	RX_HEADER	RW1S	RW1C	0	SW sets this field to '1' to receive a header. HW sets this field to '0' on successful completion of the ANY of the legal command sequences (NOT set to '0' when an error is detected in LIN mode). The header is received when the PID field STOP bits are received (INTR.RX_HEADER_DONE). Typically, a slave node SW sets both RX_HEADER and RX_RESPONSE to '1', anticipating a transfer of a response from the master node to this slave node. After receipt of the header PID field (INTR.RX_HEADER_PID_DONE is activated), the slave node may decide to set TX_RESPONSE to '1' (which has a higher priority than RX_RESPONSE) to transmit a response. the Break detection is performed regardless of CMD.RX_HEADER. INTR.RX_BREAK_WAKEUP_DONE will trigger at LIN_RX rising edge, when the low pulse meet CTL0.BREAK_WAKEUP_LENGTH. when Break is detected, HW check CMD.RX_HEADER before entering SYNC byte processing state. when RX_HEADER is cleared, SW has at least 11 bit times to set RX_HEADER again, before next Break is detected (RX_BREAK_WAKEUP_DONE). in this case, there is no gap, Break will never be missed. In UART mode, a single data field in received (in DATA0.DATA1). HW set this field to '0' when the data field is received, or when an error is detected.
9	RX_RESPONSE	RW1S	RW1C	0	SW sets this field to '1' to receive a response. HW sets this field to '0' on successful completion of ANY of the legal command sequences (NOT set to '0' when an error is detected). The response is received when the checksum field STOP bits are received (INTR.RX_RESPONSE_DONE).

9.3.3.5 LIN_CH_TX_RX_STATUS

Description: TX/RX status
Address: 0x402D8060
Offset: 0x60
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: 0x5000000

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	SYNC_COUNTER [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:18]						RX_IN [17:17]	TX_IN [16:16]

Bits	31	30	29	28	27	26	25	24
Name	None [31:27]					EN_OUT [26:26]	None [25:25]	TX_OUT [24:24]

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:7	SYNC_COUNTER	R	W	Undefined	Synchronization counter in LIN channel clock periods. After the receipt of a synchronization field, this fields reflects the duration of the synchronization field. Ideally, SYNC_COUNTER = 8*16 = 128 (the synchronization fields consists of eight bit period of 16 LIN channel clock periods each). - If SYNC_COUNTER is less than 128, the LIN channel clock is too slow and the PERI/PCLK divider value should be decreased. - If SYNC_COUNTER is greater than 128, the LIN channel clock is too fast and the PERI/PCLK divider value should be increased. The biggest master-slave clock discrepancy occurs when the master is slow and the slave is fast or vice versa. At a 0.5 percent master inaccuracy and a 14 percent slave inaccuracy, this results in the extreme synchronization values of (.86 * 128) / 1.005 = 109.5 and (1.14 *128) / 0.995 = 146.6. We add a little margin for a valid range of [106, 152]. Note: Only slave nodes with imprecise clocks require clock resynchronization. Master and slave nodes with precise clocks do NOT require clock resynchronization.
16	TX_IN	R	W	Undefined	LIN transmitter input ('tx_in', 'lin_tx_in' in functional mode). TX_IN and RX_IN can be used to determine a wakeup source. Note that wakeup source detection relies on the external transceiver functionality.
17	RX_IN	R	W	Undefined	LIN receiver input ('rx_in', 'lin_rx_in' in functional mode).
24	TX_OUT	R	W	1	LIN transmitter output ('tx_out', 'lin_tx_out').

Bits	Name	SW	HW	Default or Enum	Description
26	EN_OUT	RW	RW	1	LIN transceiver enable ('en_out', 'lin_en_out'). This field controls the enable (or low active sleep enable) of the external transceiver: '0': Disabled. '1': Enabled. If CTL.AUTO_EN is '0', SW controls this field to enable the external transceiver. If CTL.AUTO_EN is '1', HW controls this field to enable the external transceiver: - Before a legal command sequence, HW sets this field to '1', if it is '0'. The start of the command sequence is effectively postponed by a 4-bit period preamble. - After a legal command sequence, HW clears this field to '0'. The end of the command sequence is effectively postponed by a 4-bit period postamble. Note: external transceivers require a 'power up' or 'power down' period of 1 or 2 bit periods, so a 4-bit period suffices for all known transceivers.

9.3.3.6 LIN_CH_PID_CHECKSUM

Description: PID and checksum
Address: 0x402D8080
Offset: 0x80
Retention: Retained
IsDeepSleep: No
Comment: This register supports 8-bit, 16-bit and 32-bit accesses.

A LIN header has a single PID field. This field is SW accessible through this register. The field is used in BOTH transmit and receive modes.

A LIN response has a single checksum field. This field is SW accessible through this register. The field is used in BOTH transmit and receive modes.

Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	PID [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	CHECKSUM [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:7	PID	RW	RW	Undefined	Header protected identifier (PID). - Bits 5 down to 0: frame identifier ID[5:0]. Frame identifier 0x3c is for a 'master request' frame, 0x3d is for a 'slave response' frame, 0x3e and 0x3f are for future LIN enhancements. Frame identifier ID[5:4] is optionally used for length control; i.e. specifies the number of response data fields. - Bits 1 down to 0: parity bits P[1] and P[0]. - P[1] = ! (ID[5] ^ ID[4] ^ ID[3] ^ ID[1]) - P[0] = (ID[4] ^ ID[2] ^ ID[1] ^ ID[0]) Transmission: To be transmitted PID field. SW needs to calculate the PID field parity bits P[1] and P[0]. Reception: Received PID field. Slave node SW uses the PID field to determine how to handle the response for a received frame header: TX_RESPONSE or RX_RESPONSE.
8:15	CHECKSUM	R	RW	Undefined	Checksum. Transmission: HW calculated checksum (SW does not need to calculate the checksum) over the transmitted PID field (optional per CTL.CHECKSUM_ENHANCED) and data fields. Reception: Received checksum. Note that in case of a RX_CHECKSUM_ERROR, SW can use the received PID field and the received data fields to calculate the correct checksum value.

9.3.3.7 LIN_CH_DATA0

Description: Response data 0
Address: 0x402D8084
Offset: 0x84
Retention: Retained
IsDeepSleep: No
Comment: This register supports 8-bit, 16-bit and 32-bit accesses. This allows for a single 32-bit access to write or read four data fields.

A LIN response has a maximum of eight data fields. These data fields are SW accessible through the DATA0 and DATA1 registers. These register are used in BOTH transmit and receive modes. If the LIN response is both transmitted and received, the to be transmitted data fields (provided by SW) in this register are overwritten by the received data fields (provided by HW).

Data field DATA1 is the first response data field (first to be transmitted/received). The number of transmitted/received data fields is specified by CTL.DATA_NR.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	DATA1 [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	DATA2 [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	DATA3 [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	DATA4 [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:7	DATA1	RW	RW	Undefined	Data field 1. Transmission: To be transmitted data field. SW provides data field. Reception: Received data field. SW uses the data field.
8:15	DATA2	RW	RW	Undefined	Data field 2.
16:23	DATA3	RW	RW	Undefined	Data field 3.
24:31	DATA4	RW	RW	Undefined	Data field 4.

9.3.3.8 LIN_CH_DATA1

Description: Response data 1
Address: 0x402D8088
Offset: 0x88
Retention: Retained
IsDeepSleep: No
Comment: This register supports 8-bit, 16-bit and 32-bit accesses. This allows for a single 32-bit access to write or read four data fields.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	DATA5 [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	DATA6 [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	DATA7 [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	DATA8 [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:7	DATA5	RW	RW	Undefined	Data field 5.
8:15	DATA6	RW	RW	Undefined	Data field 6.
16:23	DATA7	RW	RW	Undefined	Data field 7.
24:31	DATA8	RW	RW	Undefined	Data field 8.

9.3.3.9 LIN_CH_INTR

Description: Interrupt
Address: 0x402D80C0
Offset: 0xC0
Retention: Not Retained
IsDeepSleep: No
Comment: The register fields are not retained. This is to ensure that they come up as '0' after coming out of DeepSleep system power mode.

This is a non-retained register; setting CTL.ENABLED to '0' clears all command fields to '0'.

An activated error interrupt cause aborts an ongoing frame transfer (except for bit errors when CTL.BIT_ERROR_IGNORE is '1').

Note: LIN mode supports all interrupt causes. UART mode supports the RX_NOISE_DETECT, TX_HEADER_BIT_ERROR, RX_HEADER_FRAME_ERROR and RX_HEADER_PARITY_ERROR interrupt causes only.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:3]					TX_WAKEUP_DONE [2:2]	TX_RESPONSE_DONE [1:1]	TX_HEADER_DONE [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:15]	TIMEOUT [14:14]	RX_NOISE_DETECT [13:13]	None [12:12]	RX_HEADER_SYNC_DONE [11:11]	RX_BREAK_WAKEUP_DONE [10:10]	RX_RESPONSE_DONE [9:9]	RX_HEADER_DONE [8:8]

Bits	23	22	21	20	19	18	17	16
Name	None [23:18]						TX_RESPONSE_BIT_ERROR [17:17]	TX_HEADER_BIT_ERROR [16:16]

Bits	31	30	29	28	27	26	25	24
Name	None [31:29]			RX_RESPONSE_CHECKSUM_ERROR [28:28]	RX_RESPONSE_FRAME_ERROR [27:27]	RX_HEADER_PARITY_ERROR [26:26]	RX_HEADER_SYNC_ERROR [25:25]	RX_HEADER_FRAME_ERROR [24:24]

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	TX_HEADER_DONE	RW1C	RW1S	0	HW sets this field to '1', when a frame header (break field, synchronization field and PID field) is transmitted (the CMD.TX_HEADER is completed). Specifically: - When followed by CMD.TX_RESPONSE or CMD.RX_RESPONSE, this field is set to '1' after completion of the frame header transfer. - When not followed by a response command, this field is set to '1' after completion of the frame header transfer. If CTL.AUTO_EN is '1', this includes the 4-bit period external transceiver disable post-amble. Note: used in UART mode.
1	TX_RESPONSE_DONE	RW1C	RW1S	0	HW sets this field to '1', when a frame response (data fields and checksum field) is transmitted (the CMD.TX_RESPONSE is completed). If CTL.AUTO_EN is '1', this includes the 4-bit period external transceiver disable post-amble.
2	TX_WAKEUP_DONE	RW1C	RW1S	0	HW sets this field to '1', when a wakeup signal is transmitted (per CTL.BREAK_WAKEUP_LENGTH). This cause is activated on a transition from dominant/'0' state to recessive/'1' state; i.e. at the end of the wakeup signal.
8	RX_HEADER_DONE	RW1C	RW1S	0	HW sets this field to '1', when a frame header (break field, synchronization field and PID field) is received (the CMD.RX_HEADER is completed). Specifically: - When followed by CMD.TX_RESPONSE or CMD.RX_RESPONSE, this field is set to '1' after completion of the frame header transfer. - When not followed by a response command, this field is set to '1' after completion of the frame header transfer. If CTL.AUTO_EN is '1', this includes the 4-bit period external transceiver disable post-amble. Note: used in UART mode.
9	RX_RESPONSE_DONE	RW1C	RW1S	0	HW sets this field to '1', when a frame response (data fields and checksum field) is received (the CMD.RX_RESPONSE is completed). If CTL.AUTO_EN is '1', this includes the 4-bit period external transceiver disable post-amble. Note: activation implies that RX_RESPONSE_FRAME_ERROR and RX_RESPONSE_CHECKSUM_ERROR are not activated during response reception
10	RX_BREAK_WAKEUP_DONE	RW1C	RW1S	0	HW sets this field to '1', when a break or wakeup signal is received (per CTL.BREAK_WAKEUP_LENGTH). This cause is activated on a transition from dominant/'0' state to recessive/'1' state; i.e. at the end of the wakeup signal. The break or wakeup detection is always enabled, regardless of CMD register setting.
11	RX_HEADER_SYNC_DONE	RW1C	RW1S	0	HW sets this field to '1', when a synchronization field is received (including trailing STOP bits).

Bits	Name	SW	HW	Default or Enum	Description
13	RX_NOISE_DETECT	RW1C	RW1S	0	HW sets this field to '1', when isolated '0' or '1' 'in_rx_in' values are observed or when during sampling the last three 'lin_rx_in' values do NOT all have the same value. This mismatch is an indication of noise on the LIN line. Note: The ongoing frame transfer is NOT aborted. Note: Used in UART mode.
14	TIMEOUT	RW1C	RW1S	0	HW sets this field to '1', when a frame, frame header or frame response timeout is detected (per CTL.FRAME_TIMEOUT_SEL). Note: The ongoing frame transfer is NOT aborted.
16	TX_HEADER_BIT _ERROR	RW1C	RW1S	0	HW sets this field to '1', when a transmitted 'lin_tx_out' value does NOT match a received 'lin_rx_in' value (during header transmission). This specific test allows for delay through the external transceiver. This mismatch is an indication of bus collisions on the LIN line. The match is performed for the Wakeup, Break, SYNC and the PID fields (for the START bit, data Byte and STOP bit). Note: When CTL.BIT_ERROR_IGNORE is '0', the ongoing message transfer is aborted (INTR.TX_HEADER_DONE is NOT activated) and the TX_HEADER, TX_RESPONSE and TX_WAKEUP commands are set to '0'. Note: Used in UART mode.
17	TX_RESPONSE_BIT _ERROR	RW1C	RW1S	0	HW sets this field to '1', when a transmitted 'lin_tx_out' value does NOT match a received 'lin_rx_in' value (during response transmission). The match is performed for the data fields and the checksum field (for the START bit, data Byte and STOP bit). Note: When CTL.BIT_ERROR_IGNORE is '0', the ongoing message transfer is aborted (INTR.TX_RESPONSE_DONE is NOT activated) and the TX_HEADER, TX_RESPONSE and TX_WAKEUP commands are set to '0'.
24	RX_HEADER_FRAME _ERROR	RW1C	RW1S	0	HW sets this field to '1', when the received START or STOP bits have an unexpected value (during header reception). Note: The ongoing message transfer is aborted (INTR.RX_HEADER_DONE is NOT activated) and the TX_HEADER, TX_RESPONSE and TX_WAKEUP commands are set to '0'. Note: Used in UART mode.

Bits	Name	SW	HW	Default or Enum	Description
25	RX_HEADER_SYNC _ERROR	RW1C	RW1S	0	HW sets this field to '1', when the received synchronization field is not received within the synchronization counter range [106, 152] (see TX_RX_STATUS.SYNC_COUNTER). Note: The ongoing message transfer is aborted (INTR.RX_HEADER_SYNC_DONE is NOT activated) and the TX_HEADER, TX_RESPONSE and TX_WAKEUP commands are set to '0'.
26	RX_HEADER_PARITY _ERROR	RW1C	RW1S	0	HW sets this field to '1', when the received PID field has a parity error. Note: The ongoing message transfer is aborted (INTR.RX_PID_DONE is NOT activated) and the TX_HEADER, TX_RESPONSE and TX_WAKEUP commands are set to '0'. +G119 HW sets this field to '1', when the received data field has a parity error (when CTL0.PARITY_EN is '1').
27	RX_RESPONSE_FRAME _ERROR	RW1C	RW1S	0	HW sets this field to '1', when the received START or STOP bits have an unexpected value (during response reception). HW does NOT use this field for the STOP bits of the first data field after a RX_HEADER command, if the received data byte is 0x00. (STATUS.RX_DATA0_FRAME_ERROR is used instead). Note: The ongoing message transfer is aborted (INTR.RX_RESPONSE_DONE is NOT activated) and the TX_HEADER, TX_RESPONSE and TX_WAKEUP commands are set to '0'.
28	RX_RESPONSE _CHECKSUM_ERROR	RW1C	RW1S	0	HW sets this field to '1', when the calculated checksum over the received PID and data fields is not the same as the received checksum. Note: The ongoing message transfer is aborted (INTR.RX_RESPONSE_DONE is NOT activated) and the TX_HEADER, TX_RESPONSE and TX_WAKEUP commands are set to '0'.

9.3.3.10 LIN_CH_INTR_SET

Description: Interrupt set
Address: 0x402D80C4
Offset: 0xC4
Retention: Not Retained
IsDeepSleep: No
Comment: When read, this register reflects the INTR register.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:3]					TX_WAKEUP_DONE [2:2]	TX_RESPONSE_DONE [1:1]	TX_HEADER_DONE [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:15]	TIMEOUT [14:14]	RX_NOISE_DETECT [13:13]	None [12:12]	RX_HEADER_SYNC_DONE [11:11]	RX_BREAK_WAKEUP_DONE [10:10]	RX_RESPONSE_DONE [9:9]	RX_HEADER_DONE [8:8]

Bits	23	22	21	20	19	18	17	16
Name	None [23:18]						TX_RESPONSE_BIT_ERROR [17:17]	TX_HEADER_BIT_ERROR [16:16]

Bits	31	30	29	28	27	26	25	24
Name	None [31:29]			RX_RESPONSE_CHECKSUM_ERROR [28:28]	RX_RESPONSE_FRAME_ERROR [27:27]	RX_HEADER_PARITY_ERROR [26:26]	RX_HEADER_SYNC_ERROR [25:25]	RX_HEADER_FRAME_ERROR [24:24]

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	TX_HEADER_DONE	RW1S	A	0	Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect).
1	TX_RESPONSE_DONE	RW1S	A	0	Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect).
2	TX_WAKEUP_DONE	RW1S	A	0	Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect).
8	RX_HEADER_DONE	RW1S	A	0	Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect).
9	RX_RESPONSE_DONE	RW1S	A	0	Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect).
10	RX_BREAK_WAKEUP_DONE	RW1S	A	0	Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect).
11	RX_HEADER_SYNC_DONE	RW1S	A	0	Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect).
13	RX_NOISE_DETECT	RW1S	A	0	Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect).
14	TIMEOUT	RW1S	A	0	Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect).

Bits	Name	SW	HW	Default or Enum	Description
16	TX_HEADER_BIT _ERROR	RW1S	A	0	Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect).
17	TX_RESPONSE_BIT _ERROR	RW1S	A	0	Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect).
24	RX_HEADER_FRAME _ERROR	RW1S	A	0	Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect).
25	RX_HEADER_SYNC _ERROR	RW1S	A	0	Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect).
26	RX_HEADER_PARITY _ERROR	RW1S	A	0	Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect).
27	RX_RESPONSE_FRAME _ERROR	RW1S	A	0	Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect).
28	RX_RESPONSE _CHECKSUM_ERROR	RW1S	A	0	Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect).

9.3.3.11 LIN_CH_INTR_MASK

Description: Interrupt mask
Address: 0x402D80C8
Offset: 0xC8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:3]					TX_WAKEUP_DONE [2:2]	TX_RESPONSE_DONE [1:1]	TX_HEADER_DONE [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:15]	TIMEOUT [14:14]	RX_NOISE_DETECT [13:13]	None [12:12]	RX_HEADER_SYNC_DONE [11:11]	RX_BREAK_WAKEUP_DONE [10:10]	RX_RESPONSE_DONE [9:9]	RX_HEADER_DONE [8:8]

Bits	23	22	21	20	19	18	17	16
Name	None [23:18]						TX_RESPONSE_BIT_ERROR [17:17]	TX_HEADER_BIT_ERROR [16:16]

Bits	31	30	29	28	27	26	25	24
Name	None [31:29]			RX_RESPONSE_CHECKSUM_ERROR [28:28]	RX_RESPONSE_FRAME_ERROR [27:27]	RX_HEADER_PARITY_ERROR [26:26]	RX_HEADER_SYNC_ERROR [25:25]	RX_HEADER_FRAME_ERROR [24:24]

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	TX_HEADER_DONE	RW	R	0	Mask for corresponding field in INTR register.
1	TX_RESPONSE_DONE	RW	R	0	Mask for corresponding field in INTR register.
2	TX_WAKEUP_DONE	RW	R	0	Mask for corresponding field in INTR register.
8	RX_HEADER_DONE	RW	R	0	Mask for corresponding field in INTR register.
9	RX_RESPONSE_DONE	RW	R	0	Mask for corresponding field in INTR register.
10	RX_BREAK_WAKEUP_DONE	RW	R	0	Mask for corresponding field in INTR register.
11	RX_HEADER_SYNC_DONE	RW	R	0	Mask for corresponding field in INTR register.
13	RX_NOISE_DETECT	RW	R	0	Mask for corresponding field in INTR register.
14	TIMEOUT	RW	R	0	Mask for corresponding field in INTR register.
16	TX_HEADER_BIT_ERROR	RW	R	0	Mask for corresponding field in INTR register.
17	TX_RESPONSE_BIT_ERROR	RW	R	0	Mask for corresponding field in INTR register.
24	RX_HEADER_FRAME_ERROR	RW	R	0	Mask for corresponding field in INTR register.

Bits	Name	SW	HW	Default or Enum	Description
25	RX_HEADER_SYNC _ERROR	RW	R	0	Mask for corresponding field in INTR register.
26	RX_HEADER_PARITY _ERROR	RW	R	0	Mask for corresponding field in INTR register.
27	RX_RESPONSE_FRAME _ERROR	RW	R	0	Mask for corresponding field in INTR register.
28	RX_RESPONSE _CHECKSUM_ERROR	RW	R	0	Mask for corresponding field in INTR register.

9.3.3.12 LIN_CH_INTR_MASKED

Description: Interrupt masked
Address: 0x402D80CC
Offset: 0xCC
Retention: Not Retained
IsDeepSleep: No
Comment: When read, this register reflects a bitwise AND between the INTR and INTR_MASK registers. This register allows SW to read the status of all mask enabled interrupt causes with a single load operation, rather than two load operations: one for INTR and one for INTR_MASK. This simplifies Firmware development. The associated interrupt is active ('1'), when INTR_MASKED != 0.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:3]					TX_WAKEUP_DONE [2:2]	TX_RESPONSE_DONE [1:1]	TX_HEADER_DONE [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:15]	TIMEOUT [14:14]	RX_NOISE_DETECT [13:13]	None [12:12]	RX_HEADER_SYNC_DONE [11:11]	RX_BREAK_WAKEUP_DONE [10:10]	RX_RESPONSE_DONE [9:9]	RX_HEADER_DONE [8:8]

Bits	23	22	21	20	19	18	17	16
Name	None [23:18]						TX_RESPONSE_BIT_ERROR [17:17]	TX_HEADER_BIT_ERROR [16:16]

Bits	31	30	29	28	27	26	25	24
Name	None [31:29]			RX_RESPONSE_CHECKSUM_ERROR [28:28]	RX_RESPONSE_FRAME_ERROR [27:27]	RX_HEADER_PARITY_ERROR [26:26]	RX_HEADER_SYNC_ERROR [25:25]	RX_HEADER_FRAME_ERROR [24:24]

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	TX_HEADER_DONE	R	W	0	Logical AND of corresponding INTR and INTR_MASK fields.
1	TX_RESPONSE_DONE	R	W	0	Logical AND of corresponding INTR and INTR_MASK fields.
2	TX_WAKEUP_DONE	R	W	0	Logical AND of corresponding INTR and INTR_MASK fields.
8	RX_HEADER_DONE	R	W	0	Logical AND of corresponding INTR and INTR_MASK fields.
9	RX_RESPONSE_DONE	R	W	0	Logical AND of corresponding INTR and INTR_MASK fields.
10	RX_BREAK_WAKEUP_DONE	R	W	0	Logical AND of corresponding INTR and INTR_MASK fields.
11	RX_HEADER_SYNC_DONE	R	W	0	Logical AND of corresponding INTR and INTR_MASK fields.

Bits	Name	SW	HW	Default or Enum	Description
13	RX_NOISE_DETECT	R	W	0	Logical AND of corresponding INTR and INTR_MASK fields.
14	TIMEOUT	R	W	0	Logical AND of corresponding INTR and INTR_MASK fields.
16	TX_HEADER_BIT _ERROR	R	W	0	Logical AND of corresponding INTR and INTR_MASK fields.
17	TX_RESPONSE_BIT _ERROR	R	W	0	Logical AND of corresponding INTR and INTR_MASK fields.
24	RX_HEADER_FRAME _ERROR	R	W	0	Logical AND of corresponding INTR and INTR_MASK fields.
25	RX_HEADER_SYNC _ERROR	R	W	0	Logical AND of corresponding INTR and INTR_MASK fields.
26	RX_HEADER_PARITY _ERROR	R	W	0	Logical AND of corresponding INTR and INTR_MASK fields.
27	RX_RESPONSE_FRAME _ERROR	R	W	0	Logical AND of corresponding INTR and INTR_MASK fields.
28	RX_RESPONSE _CHECKSUM_ERROR	R	W	0	Logical AND of corresponding INTR and INTR_MASK fields.

10 LPCOMP

10.1 LPCOMP 0

Description Low Power Comparators
Base Address 0x402B0000
Size 0x10000
Slave Num MMIO1

Register Name	Address	Permission	Description
LPCOMP0_ID	0x402B0000	FULL	ID & Revision
LPCOMP0_CONFIG	0x402B0004	FULL	LPCOMP Configuration Register
LPCOMP0_INTR	0x402B0010	FULL	LPCOMP Interrupt request register
LPCOMP0_INTR_SET	0x402B0014	FULL	LPCOMP Interrupt set register
LPCOMP0_INTR_MASK	0x402B0018	FULL	LPCOMP Interrupt request mask
LPCOMP0_INTR_MASKED	0x402B001C	FULL	LPCOMP Interrupt request masked
LPCOMP0_TRIM1	0x402BFF00	FULL	LPCOMP Trim Register
LPCOMP0_TRIM2	0x402BFF04	FULL	LPCOMP Trim Register
LPCOMP0_TRIM3	0x402BFF08	FULL	LPCOMP Trim Register
LPCOMP0_TRIM4	0x402BFF0C	FULL	LPCOMP Trim Register

10.2 LPCOMP 1

Description Low Power Comparators
Base Address 0x402C0000
Size 0x10000
Slave Num MMIO1

Register Name	Address	Permission	Description
LPCOMP1_ID	0x402C0000	FULL	ID & Revision
LPCOMP1_CONFIG	0x402C0004	FULL	LPCOMP Configuration Register
LPCOMP1_INTR	0x402C0010	FULL	LPCOMP Interrupt request register
LPCOMP1_INTR_SET	0x402C0014	FULL	LPCOMP Interrupt set register
LPCOMP1_INTR_MASK	0x402C0018	FULL	LPCOMP Interrupt request mask
LPCOMP1_INTR_MASKED	0x402C001C	FULL	LPCOMP Interrupt request masked
LPCOMP1_TRIM1	0x402CFF00	FULL	LPCOMP Trim Register
LPCOMP1_TRIM2	0x402CFF04	FULL	LPCOMP Trim Register
LPCOMP1_TRIM3	0x402CFF08	FULL	LPCOMP Trim Register
LPCOMP1_TRIM4	0x402CFF0C	FULL	LPCOMP Trim Register

10.3 Register Details

10.3.1 LPCOMP_ID

Description: ID & Revision
Address: 0x402B0000
Offset: 0x0
Retention: Retained
IsDeepSleep: No
Comment: Includes the information of LPCOMP controller' ID and revision number
Default: 0x1E0E0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	ID [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	REVISION [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	REVISION [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:15	ID	R		57568	the ID of LPCOMP peripheral is 0xE0E0
16:31	REVISION	R		1	the version number is 0x0001

10.3.2 LPCOMP_CONFIG

Description: LPCOMP Configuration Register
Address: 0x402B0004
Offset: 0x4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	ENABLE1 [7:7]	OUT1 [6:6]	INTTYPE1 [5:4]		FILTER1 [3:3]	HYST1 [2:2]	MODE1 [1:0]	

Bits	15	14	13	12	11	10	9	8
Name	ENABLE2 [15:15]	OUT2 [14:14]	INTTYPE2 [13:12]		FILTER2 [11:11]	HYST2 [10:10]	MODE2 [9:8]	

Bits	23	22	21	20	19	18	17	16
Name	None [23:22]		DSI_LEVEL 2 [21:21]	DSI _BYPASS2 [20:20]	None [19:18]		DSI_LEVEL 1 [17:17]	DSI _BYPASS1 [16:16]

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:1	MODE1	RW	R	0	Operating mode for the comparator
	SLOW			0	Slow operating mode (uses less power, <50uA)
	FAST			1	Fast operating mode (uses more power, <400uA)
	ULP			2	Ultra low power operting mode (uses ~2-4uA)
2	HYST1	RW	R	0	Add 10mV hysteresis to the comparator - 0: Enable Hysteresis - 1: Disable Hysteresis
3	FILTER1	RW	R	0	Deprecated, Reserved, must be written 0
4:5	INTTYPE1	RW	R	0	Sets which edge will trigger an IRQ
	DISABLE			0	Disabled, no interrupts will be detected
	RISING			1	Rising edge
	FALLING			2	Falling edge
	BOTH			3	Both rising and falling edges
6	OUT1	R	RW	0	Current output value of the comparator.
7	ENABLE1	RW	R	0	Enable comparator #1
8:9	MODE2	RW	R	0	Operating mode for the comparator
	SLOW			0	Slow operating mode (uses less power, <50uA)
	FAST			1	Fast operating mode (uses more power, <400uA)
	ULP			2	Ultra low power operting mode (uses ~2-4uA)
10	HYST2	RW	R	0	Add 10mV hysteresis to the comparator - 0: Enable Hysteresis - 1: Disable Hysteresis
11	FILTER2	RW	R	0	Deprecated, Reserved, must be written 0
12:13	INTTYPE2	RW	R	0	Sets which edge will trigger an IRQ
	DISABLE			0	Disabled, no interrupts will be detected
	RISING			1	Rising edge
	FALLING			2	Falling edge
	BOTH			3	Both rising and falling edges

Bits	Name	SW	HW	Default or Enum	Description
14	OUT2	R	RW	0	Current output value of the comparator.
15	ENABLE2	RW	R	0	Enable comparator #2
16	DSI_BYPASS1	RW	R	0	Opamp1 bypass comparator output synchronization for DSI output: 0=synchronize (level or pulse), 1=bypass (output async) Note that in DeepSleep mode this bit needs to be set to observe the DSI output on the dedicated pin.
17	DSI_LEVEL1	RW	R	0	Opamp1 comparator DSI (trigger) out level : 0=pulse, 1=level
20	DSI_BYPASS2	RW	R	0	Opamp2 bypass comparator output synchronization for DSI output: 0=synchronize (level or pulse), 1=bypass (output async) Note that in DeepSleep mode this bit needs to be set to observe the DSI output on the dedicated pin.
21	DSI_LEVEL2	RW	R	0	Opamp2 comparator DSI (trigger) out level : 0=pulse, 1=level

10.3.3 LPCOMP_INTR

Description: LPCOMP Interrupt request register
Address: 0x402B0010
Offset: 0x10
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:2]						COMP2 [1:1]	COMP1 [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	COMP1	RW1C	RW1S	0	Comparator 1 Interrupt: hardware sets this interrupt when comparator 0 triggers. Write with '1' to clear bit.
1	COMP2	RW1C	RW1S	0	Comparator 2 Interrupt: hardware sets this interrupt when comparator 0 triggers. Write with '1' to clear bit.

10.3.4 LPCOMP_INTR_SET

Description: LPCOMP Interrupt set register
Address: 0x402B0014
Offset: 0x14
Retention: Retained
IsDeepSleep: No
Comment: This register asserts an interrupt - used for s/w debugging.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:2]						COMP2 [1:1]	COMP1 [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	COMP1	RW1S	A	0	Write with '1' to set corresponding bit in interrupt request register.
1	COMP2	RW1S	A	0	Write with '1' to set corresponding bit in interrupt request register.

10.3.5 LPCOMP_INTR_MASK

Description: LPCOMP Interrupt request mask
Address: 0x402B0018
Offset: 0x18
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:2]						COMP2_MASK [1:1]	COMP1_MASK [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	COMP1_MASK	RW	R	0	Mask bit for corresponding bit in interrupt request register.
1	COMP2_MASK	RW	R	0	Mask bit for corresponding bit in interrupt request register.

10.3.6 LPCOMP_INTR_MASKED

Description: LPCOMP Interrupt request masked
Address: 0x402B001C
Offset: 0x1C
Retention: Retained
IsDeepSleep: No
Comment: If the value is not zero then the LPCOMP interrupt signal to the NVIC is high. When read, this register reflects a bitwise AND between the interrupt request and mask registers.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:2]						COMP2_MASKED [1:1]	COMP1_MASKED [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	COMP1_MASKED	R	W	0	Logical and of corresponding request and mask bits.
1	COMP2_MASKED	R	W	0	Logical and of corresponding request and mask bits.

10.3.7 LPCOMP_TRIM1

Description: LPCOMP Trim Register
Address: 0x402BFF00
Offset: 0xFF00
Retention: Retained
IsDeepSleep: No
Comment: Trim fields for both comparators
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:5]			COMP1_TRIMA [4:0]				

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:4	COMP1_TRIMA	RW	R	0	Trim A for Comparator #1

10.3.8 LPCOMP_TRIM2

Description: LPCOMP Trim Register
Address: 0x402BFF04
Offset: 0xFF04
Retention: Retained
IsDeepSleep: No
Comment: Trim fields for both comparators
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:5]			COMP1_TRIMB [4:0]				

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:4	COMP1_TRIMB	RW	R	0	Trim B for Comparator #1

10.3.9 LPCOMP_TRIM3

Description: LPCOMP Trim Register
Address: 0x402BFF08
Offset: 0xFF08
Retention: Retained
IsDeepSleep: No
Comment: Trim fields for both comparators
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:5]			COMP2_TRIMA [4:0]				

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:4	COMP2_TRIMA	RW	R	0	Trim A for Comparator #2

10.3.10 LPCOMP_TRIM4

Description: LPCOMP Trim Register
Address: 0x402BFF0C
Offset: 0xFF0C
Retention: Retained
IsDeepSleep: No
Comment: Trim fields for both comparators
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:5]			COMP2_TRIMB [4:0]				

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:4	COMP2_TRIMB	RW	R	0	Trim B for Comparator #2

11 MSC

Description MultiSense Controller
Base Address 0x40290000
Size 0x10000
Slave Num MMIO1

Register Name	Address	Permission	Description
MSC_CTL	0x40290000	FULL	Configuration and Control
MSC_SPARE	0x40290004	FULL	Spare MMIO
MSC_SCAN_CTL1	0x40290008	FULL	Scan Control 1
MSC_SCAN_CTL2	0x4029000C	FULL	Scan Control 2
MSC_INIT_CTL1	0x40290010	FULL	Initialisation Control 1
MSC_INIT_CTL2	0x40290014	FULL	Initialisation Control 2
MSC_INIT_CTL3	0x40290018	FULL	Initialisation Control 3
MSC_INIT_CTL4	0x4029001C	FULL	Initialisation Control 4
MSC_SENSE_DUTY_CTL	0x40290020	FULL	Sense Clock Duty Cycle Control
MSC_SENSE_PERIOD_CTL	0x40290024	FULL	Sense Clock Period Control
MSC_FILTER_CTL	0x40290028	FULL	Filter Control
MSC_CCOMP_CDAC_CTL	0x40290030	FULL	Compensation CAPDAC Control
MSC_DITHER_CDAC_CTL	0x40290034	FULL	Flatspot/Dither CAPDAC Switch Control
MSC_CSW_CTL	0x40290040	FULL	Control Mux Switch Control
MSC_SW_SEL_GPIO	0x40290044	FULL	GPIO Switch Control
MSC_SW_SEL_CDAC_RE	0x40290048	FULL	Reference CAPDAC Switch Control
MSC_SW_SEL_CDAC_CO	0x4029004C	FULL	Compensation CAPDAC Switch Control
MSC_SW_SEL_CDAC_CF	0x40290050	FULL	Fine CAPDAC Switch Control
MSC_SW_SEL_CMOD1	0x40290054	FULL	CMOD Switch Control 1
MSC_SW_SEL_CMOD2	0x40290058	FULL	CMOD Switch Control 2
MSC_SW_SEL_CMOD3	0x4029005C	FULL	CMOD Switch Control 3
MSC_SW_SEL_CMOD4	0x40290060	FULL	CMOD Switch Control 4
MSC_OBS_CTL	0x40290070	FULL	Observability Control
MSC_STATUS1	0x40290100	FULL	General Status Register 1
MSC_STATUS2	0x40290104	FULL	General Status Register 2
MSC_STATUS3	0x40290108	FULL	General Status Register 3
MSC_RESULT_FIFO_STATUS	0x4029010C	FULL	Result FIFO Status
MSC_RESULT_FIFO_RD	0x40290110	FULL	Result FIFO Pointer
MSC_INTR	0x40290170	FULL	MSCv3 Interrupt Cause Register
MSC_INTR_SET	0x40290174	FULL	MSCv3 Interrupt Set Register
MSC_INTR_MASK	0x40290178	FULL	MSCv3 Interrupt Mask Register
MSC_INTR_MASKED	0x4029017C	FULL	MSCv3 Interrupt Masked Register
MSC_FRAME_CMD	0x40290190	FULL	Frame Command Register
MSC_SNS_STRUCT_CTL	0x40290200	FULL	Sensor Struct Control
MSC_SNS_SW_SEL_CSW_MASK2	0x4029020C	FULL	Control MUX Function Select Mask 2
MSC_SNS_SW_SEL_CSW_MASK1	0x40290210	FULL	Control MUX Function Select Mask 1
MSC_SNS_SW_SEL_CSW_MASK0	0x40290214	FULL	Control MUX Function Select Mask 0
MSC_SNS_SCAN_CTL	0x40290218	FULL	Sensor Scan Control
MSC_SNS_CDAC_CTL	0x4029021C	FULL	Sensor CAPDAC Control
MSC_SNS_CTL	0x40290220	FULL	Sense Control and Command Register
MSC_SW_SEL_CSW0	0x40290300	FULL	Control Switch MUX Switch Control
MSC_SW_SEL_CSW1	0x40290304	FULL	Control Switch MUX Switch Control
MSC_SW_SEL_CSW2	0x40290308	FULL	Control Switch MUX Switch Control
MSC_SW_SEL_CSW3	0x4029030C	FULL	Control Switch MUX Switch Control
MSC_SW_SEL_CSW4	0x40290310	FULL	Control Switch MUX Switch Control
MSC_SW_SEL_CSW5	0x40290314	FULL	Control Switch MUX Switch Control
MSC_SW_SEL_CSW6	0x40290318	FULL	Control Switch MUX Switch Control
MSC_SW_SEL_CSW7	0x4029031C	FULL	Control Switch MUX Switch Control
MSC_SW_SEL_CSW8	0x40290320	FULL	Control Switch MUX Switch Control
MSC_SW_SEL_CSW9	0x40290324	FULL	Control Switch MUX Switch Control
MSC_SW_SEL_CSW10	0x40290328	FULL	Control Switch MUX Switch Control
MSC_SW_SEL_CSW11	0x4029032C	FULL	Control Switch MUX Switch Control
MSC_SW_SEL_CSW12	0x40290330	FULL	Control Switch MUX Switch Control
MSC_SW_SEL_CSW13	0x40290334	FULL	Control Switch MUX Switch Control
MSC_SW_SEL_CSW14	0x40290338	FULL	Control Switch MUX Switch Control

Register Name	Address	Permission	Description
MSC_SW_SEL_CSW15	0x4029033C	FULL	Control Switch MUX Switch Control
MSC_SW_SEL_CSW_FUNC0	0x40290400	FULL	Control Switch MUX Switch Control Global Functions
MSC_SW_SEL_CSW_FUNC1	0x40290404	FULL	Control Switch MUX Switch Control Global Functions
MSC_SW_SEL_CSW_FUNC2	0x40290408	FULL	Control Switch MUX Switch Control Global Functions
MSC_SW_SEL_CSW_FUNC3	0x4029040C	FULL	Control Switch MUX Switch Control Global Functions
MSC_SW_SEL_CSW_FUNC4	0x40290410	FULL	Control Switch MUX Switch Control Global Functions
MSC_SW_SEL_CSW_FUNC5	0x40290414	FULL	Control Switch MUX Switch Control Global Functions
MSC_SW_SEL_CSW_FUNC6	0x40290418	FULL	Control Switch MUX Switch Control Global Functions
MSC_SW_SEL_CSW_FUNC7	0x4029041C	FULL	Control Switch MUX Switch Control Global Functions
MSC_SENSOR_DATA0	0x40291000	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1	0x40291004	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2	0x40291008	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3	0x4029100C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA4	0x40291010	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA5	0x40291014	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA6	0x40291018	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA7	0x4029101C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA8	0x40291020	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA9	0x40291024	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA10	0x40291028	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA11	0x4029102C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA12	0x40291030	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA13	0x40291034	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA14	0x40291038	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA15	0x4029103C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA16	0x40291040	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA17	0x40291044	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA18	0x40291048	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA19	0x4029104C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA20	0x40291050	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA21	0x40291054	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA22	0x40291058	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA23	0x4029105C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA24	0x40291060	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA25	0x40291064	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA26	0x40291068	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA27	0x4029106C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA28	0x40291070	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA29	0x40291074	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA30	0x40291078	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA31	0x4029107C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA32	0x40291080	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA33	0x40291084	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA34	0x40291088	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA35	0x4029108C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA36	0x40291090	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA37	0x40291094	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA38	0x40291098	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA39	0x4029109C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA40	0x402910A0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA41	0x402910A4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA42	0x402910A8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA43	0x402910AC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA44	0x402910B0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA45	0x402910B4	FULL	Sensor Configuration Storage

Register Name	Address	Permission	Description
MSC_SENSOR_DATA46	0x402910B8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA47	0x402910BC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA48	0x402910C0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA49	0x402910C4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA50	0x402910C8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA51	0x402910CC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA52	0x402910D0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA53	0x402910D4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA54	0x402910D8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA55	0x402910DC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA56	0x402910E0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA57	0x402910E4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA58	0x402910E8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA59	0x402910EC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA60	0x402910F0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA61	0x402910F4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA62	0x402910F8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA63	0x402910FC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA64	0x40291100	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA65	0x40291104	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA66	0x40291108	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA67	0x4029110C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA68	0x40291110	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA69	0x40291114	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA70	0x40291118	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA71	0x4029111C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA72	0x40291120	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA73	0x40291124	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA74	0x40291128	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA75	0x4029112C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA76	0x40291130	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA77	0x40291134	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA78	0x40291138	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA79	0x4029113C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA80	0x40291140	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA81	0x40291144	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA82	0x40291148	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA83	0x4029114C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA84	0x40291150	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA85	0x40291154	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA86	0x40291158	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA87	0x4029115C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA88	0x40291160	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA89	0x40291164	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA90	0x40291168	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA91	0x4029116C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA92	0x40291170	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA93	0x40291174	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA94	0x40291178	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA95	0x4029117C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA96	0x40291180	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA97	0x40291184	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA98	0x40291188	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA99	0x4029118C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA100	0x40291190	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA101	0x40291194	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA102	0x40291198	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA103	0x4029119C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA104	0x402911A0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA105	0x402911A4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA106	0x402911A8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA107	0x402911AC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA108	0x402911B0	FULL	Sensor Configuration Storage

Register Name	Address	Permission	Description
MSC_SENSOR_DATA109	0x402911B4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA110	0x402911B8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA111	0x402911BC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA112	0x402911C0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA113	0x402911C4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA114	0x402911C8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA115	0x402911CC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA116	0x402911D0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA117	0x402911D4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA118	0x402911D8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA119	0x402911DC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA120	0x402911E0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA121	0x402911E4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA122	0x402911E8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA123	0x402911EC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA124	0x402911F0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA125	0x402911F4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA126	0x402911F8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA127	0x402911FC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA128	0x40291200	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA129	0x40291204	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA130	0x40291208	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA131	0x4029120C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA132	0x40291210	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA133	0x40291214	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA134	0x40291218	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA135	0x4029121C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA136	0x40291220	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA137	0x40291224	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA138	0x40291228	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA139	0x4029122C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA140	0x40291230	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA141	0x40291234	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA142	0x40291238	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA143	0x4029123C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA144	0x40291240	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA145	0x40291244	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA146	0x40291248	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA147	0x4029124C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA148	0x40291250	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA149	0x40291254	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA150	0x40291258	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA151	0x4029125C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA152	0x40291260	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA153	0x40291264	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA154	0x40291268	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA155	0x4029126C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA156	0x40291270	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA157	0x40291274	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA158	0x40291278	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA159	0x4029127C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA160	0x40291280	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA161	0x40291284	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA162	0x40291288	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA163	0x4029128C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA164	0x40291290	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA165	0x40291294	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA166	0x40291298	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA167	0x4029129C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA168	0x402912A0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA169	0x402912A4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA170	0x402912A8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA171	0x402912AC	FULL	Sensor Configuration Storage

Register Name	Address	Permission	Description
MSC_SENSOR_DATA172	0x402912B0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA173	0x402912B4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA174	0x402912B8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA175	0x402912BC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA176	0x402912C0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA177	0x402912C4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA178	0x402912C8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA179	0x402912CC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA180	0x402912D0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA181	0x402912D4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA182	0x402912D8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA183	0x402912DC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA184	0x402912E0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA185	0x402912E4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA186	0x402912E8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA187	0x402912EC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA188	0x402912F0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA189	0x402912F4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA190	0x402912F8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA191	0x402912FC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA192	0x40291300	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA193	0x40291304	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA194	0x40291308	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA195	0x4029130C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA196	0x40291310	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA197	0x40291314	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA198	0x40291318	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA199	0x4029131C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA200	0x40291320	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA201	0x40291324	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA202	0x40291328	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA203	0x4029132C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA204	0x40291330	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA205	0x40291334	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA206	0x40291338	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA207	0x4029133C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA208	0x40291340	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA209	0x40291344	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA210	0x40291348	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA211	0x4029134C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA212	0x40291350	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA213	0x40291354	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA214	0x40291358	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA215	0x4029135C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA216	0x40291360	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA217	0x40291364	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA218	0x40291368	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA219	0x4029136C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA220	0x40291370	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA221	0x40291374	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA222	0x40291378	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA223	0x4029137C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA224	0x40291380	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA225	0x40291384	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA226	0x40291388	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA227	0x4029138C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA228	0x40291390	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA229	0x40291394	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA230	0x40291398	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA231	0x4029139C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA232	0x402913A0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA233	0x402913A4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA234	0x402913A8	FULL	Sensor Configuration Storage

Register Name	Address	Permission	Description
MSC_SENSOR_DATA235	0x402913AC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA236	0x402913B0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA237	0x402913B4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA238	0x402913B8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA239	0x402913BC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA240	0x402913C0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA241	0x402913C4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA242	0x402913C8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA243	0x402913CC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA244	0x402913D0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA245	0x402913D4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA246	0x402913D8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA247	0x402913DC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA248	0x402913E0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA249	0x402913E4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA250	0x402913E8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA251	0x402913EC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA252	0x402913F0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA253	0x402913F4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA254	0x402913F8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA255	0x402913FC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA256	0x40291400	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA257	0x40291404	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA258	0x40291408	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA259	0x4029140C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA260	0x40291410	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA261	0x40291414	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA262	0x40291418	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA263	0x4029141C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA264	0x40291420	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA265	0x40291424	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA266	0x40291428	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA267	0x4029142C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA268	0x40291430	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA269	0x40291434	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA270	0x40291438	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA271	0x4029143C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA272	0x40291440	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA273	0x40291444	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA274	0x40291448	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA275	0x4029144C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA276	0x40291450	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA277	0x40291454	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA278	0x40291458	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA279	0x4029145C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA280	0x40291460	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA281	0x40291464	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA282	0x40291468	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA283	0x4029146C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA284	0x40291470	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA285	0x40291474	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA286	0x40291478	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA287	0x4029147C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA288	0x40291480	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA289	0x40291484	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA290	0x40291488	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA291	0x4029148C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA292	0x40291490	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA293	0x40291494	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA294	0x40291498	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA295	0x4029149C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA296	0x402914A0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA297	0x402914A4	FULL	Sensor Configuration Storage

Register Name	Address	Permission	Description
MSC_SENSOR_DATA298	0x402914A8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA299	0x402914AC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA300	0x402914B0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA301	0x402914B4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA302	0x402914B8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA303	0x402914BC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA304	0x402914C0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA305	0x402914C4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA306	0x402914C8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA307	0x402914CC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA308	0x402914D0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA309	0x402914D4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA310	0x402914D8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA311	0x402914DC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA312	0x402914E0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA313	0x402914E4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA314	0x402914E8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA315	0x402914EC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA316	0x402914F0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA317	0x402914F4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA318	0x402914F8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA319	0x402914FC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA320	0x40291500	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA321	0x40291504	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA322	0x40291508	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA323	0x4029150C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA324	0x40291510	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA325	0x40291514	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA326	0x40291518	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA327	0x4029151C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA328	0x40291520	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA329	0x40291524	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA330	0x40291528	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA331	0x4029152C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA332	0x40291530	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA333	0x40291534	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA334	0x40291538	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA335	0x4029153C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA336	0x40291540	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA337	0x40291544	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA338	0x40291548	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA339	0x4029154C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA340	0x40291550	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA341	0x40291554	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA342	0x40291558	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA343	0x4029155C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA344	0x40291560	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA345	0x40291564	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA346	0x40291568	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA347	0x4029156C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA348	0x40291570	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA349	0x40291574	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA350	0x40291578	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA351	0x4029157C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA352	0x40291580	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA353	0x40291584	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA354	0x40291588	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA355	0x4029158C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA356	0x40291590	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA357	0x40291594	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA358	0x40291598	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA359	0x4029159C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA360	0x402915A0	FULL	Sensor Configuration Storage

Register Name	Address	Permission	Description
MSC_SENSOR_DATA361	0x402915A4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA362	0x402915A8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA363	0x402915AC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA364	0x402915B0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA365	0x402915B4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA366	0x402915B8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA367	0x402915BC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA368	0x402915C0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA369	0x402915C4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA370	0x402915C8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA371	0x402915CC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA372	0x402915D0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA373	0x402915D4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA374	0x402915D8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA375	0x402915DC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA376	0x402915E0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA377	0x402915E4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA378	0x402915E8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA379	0x402915EC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA380	0x402915F0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA381	0x402915F4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA382	0x402915F8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA383	0x402915FC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA384	0x40291600	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA385	0x40291604	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA386	0x40291608	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA387	0x4029160C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA388	0x40291610	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA389	0x40291614	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA390	0x40291618	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA391	0x4029161C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA392	0x40291620	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA393	0x40291624	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA394	0x40291628	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA395	0x4029162C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA396	0x40291630	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA397	0x40291634	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA398	0x40291638	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA399	0x4029163C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA400	0x40291640	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA401	0x40291644	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA402	0x40291648	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA403	0x4029164C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA404	0x40291650	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA405	0x40291654	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA406	0x40291658	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA407	0x4029165C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA408	0x40291660	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA409	0x40291664	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA410	0x40291668	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA411	0x4029166C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA412	0x40291670	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA413	0x40291674	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA414	0x40291678	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA415	0x4029167C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA416	0x40291680	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA417	0x40291684	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA418	0x40291688	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA419	0x4029168C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA420	0x40291690	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA421	0x40291694	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA422	0x40291698	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA423	0x4029169C	FULL	Sensor Configuration Storage

Register Name	Address	Permission	Description
MSC_SENSOR_DATA424	0x402916A0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA425	0x402916A4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA426	0x402916A8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA427	0x402916AC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA428	0x402916B0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA429	0x402916B4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA430	0x402916B8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA431	0x402916BC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA432	0x402916C0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA433	0x402916C4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA434	0x402916C8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA435	0x402916CC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA436	0x402916D0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA437	0x402916D4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA438	0x402916D8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA439	0x402916DC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA440	0x402916E0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA441	0x402916E4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA442	0x402916E8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA443	0x402916EC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA444	0x402916F0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA445	0x402916F4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA446	0x402916F8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA447	0x402916FC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA448	0x40291700	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA449	0x40291704	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA450	0x40291708	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA451	0x4029170C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA452	0x40291710	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA453	0x40291714	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA454	0x40291718	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA455	0x4029171C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA456	0x40291720	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA457	0x40291724	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA458	0x40291728	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA459	0x4029172C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA460	0x40291730	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA461	0x40291734	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA462	0x40291738	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA463	0x4029173C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA464	0x40291740	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA465	0x40291744	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA466	0x40291748	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA467	0x4029174C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA468	0x40291750	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA469	0x40291754	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA470	0x40291758	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA471	0x4029175C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA472	0x40291760	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA473	0x40291764	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA474	0x40291768	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA475	0x4029176C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA476	0x40291770	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA477	0x40291774	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA478	0x40291778	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA479	0x4029177C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA480	0x40291780	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA481	0x40291784	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA482	0x40291788	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA483	0x4029178C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA484	0x40291790	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA485	0x40291794	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA486	0x40291798	FULL	Sensor Configuration Storage

Register Name	Address	Permission	Description
MSC_SENSOR_DATA487	0x4029179C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA488	0x402917A0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA489	0x402917A4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA490	0x402917A8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA491	0x402917AC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA492	0x402917B0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA493	0x402917B4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA494	0x402917B8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA495	0x402917BC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA496	0x402917C0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA497	0x402917C4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA498	0x402917C8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA499	0x402917CC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA500	0x402917D0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA501	0x402917D4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA502	0x402917D8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA503	0x402917DC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA504	0x402917E0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA505	0x402917E4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA506	0x402917E8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA507	0x402917EC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA508	0x402917F0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA509	0x402917F4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA510	0x402917F8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA511	0x402917FC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA512	0x40291800	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA513	0x40291804	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA514	0x40291808	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA515	0x4029180C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA516	0x40291810	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA517	0x40291814	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA518	0x40291818	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA519	0x4029181C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA520	0x40291820	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA521	0x40291824	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA522	0x40291828	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA523	0x4029182C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA524	0x40291830	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA525	0x40291834	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA526	0x40291838	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA527	0x4029183C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA528	0x40291840	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA529	0x40291844	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA530	0x40291848	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA531	0x4029184C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA532	0x40291850	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA533	0x40291854	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA534	0x40291858	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA535	0x4029185C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA536	0x40291860	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA537	0x40291864	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA538	0x40291868	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA539	0x4029186C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA540	0x40291870	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA541	0x40291874	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA542	0x40291878	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA543	0x4029187C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA544	0x40291880	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA545	0x40291884	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA546	0x40291888	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA547	0x4029188C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA548	0x40291890	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA549	0x40291894	FULL	Sensor Configuration Storage

Register Name	Address	Permission	Description
MSC_SENSOR_DATA550	0x40291898	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA551	0x4029189C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA552	0x402918A0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA553	0x402918A4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA554	0x402918A8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA555	0x402918AC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA556	0x402918B0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA557	0x402918B4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA558	0x402918B8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA559	0x402918BC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA560	0x402918C0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA561	0x402918C4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA562	0x402918C8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA563	0x402918CC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA564	0x402918D0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA565	0x402918D4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA566	0x402918D8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA567	0x402918DC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA568	0x402918E0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA569	0x402918E4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA570	0x402918E8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA571	0x402918EC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA572	0x402918F0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA573	0x402918F4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA574	0x402918F8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA575	0x402918FC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA576	0x40291900	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA577	0x40291904	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA578	0x40291908	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA579	0x4029190C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA580	0x40291910	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA581	0x40291914	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA582	0x40291918	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA583	0x4029191C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA584	0x40291920	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA585	0x40291924	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA586	0x40291928	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA587	0x4029192C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA588	0x40291930	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA589	0x40291934	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA590	0x40291938	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA591	0x4029193C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA592	0x40291940	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA593	0x40291944	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA594	0x40291948	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA595	0x4029194C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA596	0x40291950	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA597	0x40291954	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA598	0x40291958	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA599	0x4029195C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA600	0x40291960	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA601	0x40291964	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA602	0x40291968	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA603	0x4029196C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA604	0x40291970	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA605	0x40291974	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA606	0x40291978	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA607	0x4029197C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA608	0x40291980	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA609	0x40291984	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA610	0x40291988	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA611	0x4029198C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA612	0x40291990	FULL	Sensor Configuration Storage

Register Name	Address	Permission	Description
MSC_SENSOR_DATA613	0x40291994	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA614	0x40291998	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA615	0x4029199C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA616	0x402919A0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA617	0x402919A4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA618	0x402919A8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA619	0x402919AC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA620	0x402919B0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA621	0x402919B4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA622	0x402919B8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA623	0x402919BC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA624	0x402919C0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA625	0x402919C4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA626	0x402919C8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA627	0x402919CC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA628	0x402919D0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA629	0x402919D4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA630	0x402919D8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA631	0x402919DC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA632	0x402919E0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA633	0x402919E4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA634	0x402919E8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA635	0x402919EC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA636	0x402919F0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA637	0x402919F4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA638	0x402919F8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA639	0x402919FC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA640	0x40291A00	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA641	0x40291A04	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA642	0x40291A08	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA643	0x40291A0C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA644	0x40291A10	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA645	0x40291A14	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA646	0x40291A18	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA647	0x40291A1C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA648	0x40291A20	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA649	0x40291A24	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA650	0x40291A28	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA651	0x40291A2C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA652	0x40291A30	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA653	0x40291A34	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA654	0x40291A38	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA655	0x40291A3C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA656	0x40291A40	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA657	0x40291A44	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA658	0x40291A48	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA659	0x40291A4C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA660	0x40291A50	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA661	0x40291A54	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA662	0x40291A58	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA663	0x40291A5C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA664	0x40291A60	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA665	0x40291A64	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA666	0x40291A68	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA667	0x40291A6C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA668	0x40291A70	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA669	0x40291A74	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA670	0x40291A78	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA671	0x40291A7C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA672	0x40291A80	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA673	0x40291A84	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA674	0x40291A88	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA675	0x40291A8C	FULL	Sensor Configuration Storage

Register Name	Address	Permission	Description
MSC_SENSOR_DATA676	0x40291A90	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA677	0x40291A94	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA678	0x40291A98	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA679	0x40291A9C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA680	0x40291AA0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA681	0x40291AA4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA682	0x40291AA8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA683	0x40291AAC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA684	0x40291AB0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA685	0x40291AB4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA686	0x40291AB8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA687	0x40291ABC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA688	0x40291AC0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA689	0x40291AC4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA690	0x40291AC8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA691	0x40291ACC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA692	0x40291AD0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA693	0x40291AD4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA694	0x40291AD8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA695	0x40291ADC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA696	0x40291AE0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA697	0x40291AE4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA698	0x40291AE8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA699	0x40291AEC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA700	0x40291AF0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA701	0x40291AF4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA702	0x40291AF8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA703	0x40291AFC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA704	0x40291B00	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA705	0x40291B04	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA706	0x40291B08	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA707	0x40291B0C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA708	0x40291B10	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA709	0x40291B14	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA710	0x40291B18	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA711	0x40291B1C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA712	0x40291B20	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA713	0x40291B24	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA714	0x40291B28	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA715	0x40291B2C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA716	0x40291B30	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA717	0x40291B34	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA718	0x40291B38	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA719	0x40291B3C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA720	0x40291B40	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA721	0x40291B44	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA722	0x40291B48	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA723	0x40291B4C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA724	0x40291B50	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA725	0x40291B54	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA726	0x40291B58	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA727	0x40291B5C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA728	0x40291B60	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA729	0x40291B64	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA730	0x40291B68	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA731	0x40291B6C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA732	0x40291B70	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA733	0x40291B74	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA734	0x40291B78	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA735	0x40291B7C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA736	0x40291B80	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA737	0x40291B84	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA738	0x40291B88	FULL	Sensor Configuration Storage

Register Name	Address	Permission	Description
MSC_SENSOR_DATA739	0x40291B8C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA740	0x40291B90	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA741	0x40291B94	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA742	0x40291B98	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA743	0x40291B9C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA744	0x40291BA0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA745	0x40291BA4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA746	0x40291BA8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA747	0x40291BAC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA748	0x40291BB0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA749	0x40291BB4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA750	0x40291BB8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA751	0x40291BBC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA752	0x40291BC0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA753	0x40291BC4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA754	0x40291BC8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA755	0x40291BCC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA756	0x40291BD0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA757	0x40291BD4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA758	0x40291BD8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA759	0x40291BDC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA760	0x40291BE0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA761	0x40291BE4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA762	0x40291BE8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA763	0x40291BEC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA764	0x40291BF0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA765	0x40291BF4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA766	0x40291BF8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA767	0x40291BFC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA768	0x40291C00	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA769	0x40291C04	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA770	0x40291C08	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA771	0x40291C0C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA772	0x40291C10	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA773	0x40291C14	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA774	0x40291C18	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA775	0x40291C1C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA776	0x40291C20	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA777	0x40291C24	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA778	0x40291C28	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA779	0x40291C2C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA780	0x40291C30	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA781	0x40291C34	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA782	0x40291C38	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA783	0x40291C3C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA784	0x40291C40	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA785	0x40291C44	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA786	0x40291C48	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA787	0x40291C4C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA788	0x40291C50	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA789	0x40291C54	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA790	0x40291C58	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA791	0x40291C5C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA792	0x40291C60	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA793	0x40291C64	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA794	0x40291C68	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA795	0x40291C6C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA796	0x40291C70	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA797	0x40291C74	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA798	0x40291C78	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA799	0x40291C7C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA800	0x40291C80	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA801	0x40291C84	FULL	Sensor Configuration Storage

Register Name	Address	Permission	Description
MSC_SENSOR_DATA802	0x40291C88	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA803	0x40291C8C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA804	0x40291C90	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA805	0x40291C94	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA806	0x40291C98	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA807	0x40291C9C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA808	0x40291CA0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA809	0x40291CA4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA810	0x40291CA8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA811	0x40291CAC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA812	0x40291CB0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA813	0x40291CB4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA814	0x40291CB8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA815	0x40291CBC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA816	0x40291CC0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA817	0x40291CC4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA818	0x40291CC8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA819	0x40291CCC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA820	0x40291CD0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA821	0x40291CD4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA822	0x40291CD8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA823	0x40291CDC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA824	0x40291CE0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA825	0x40291CE4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA826	0x40291CE8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA827	0x40291CEC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA828	0x40291CF0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA829	0x40291CF4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA830	0x40291CF8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA831	0x40291CFC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA832	0x40291D00	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA833	0x40291D04	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA834	0x40291D08	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA835	0x40291D0C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA836	0x40291D10	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA837	0x40291D14	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA838	0x40291D18	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA839	0x40291D1C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA840	0x40291D20	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA841	0x40291D24	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA842	0x40291D28	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA843	0x40291D2C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA844	0x40291D30	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA845	0x40291D34	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA846	0x40291D38	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA847	0x40291D3C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA848	0x40291D40	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA849	0x40291D44	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA850	0x40291D48	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA851	0x40291D4C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA852	0x40291D50	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA853	0x40291D54	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA854	0x40291D58	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA855	0x40291D5C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA856	0x40291D60	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA857	0x40291D64	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA858	0x40291D68	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA859	0x40291D6C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA860	0x40291D70	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA861	0x40291D74	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA862	0x40291D78	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA863	0x40291D7C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA864	0x40291D80	FULL	Sensor Configuration Storage

Register Name	Address	Permission	Description
MSC_SENSOR_DATA865	0x40291D84	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA866	0x40291D88	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA867	0x40291D8C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA868	0x40291D90	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA869	0x40291D94	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA870	0x40291D98	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA871	0x40291D9C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA872	0x40291DA0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA873	0x40291DA4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA874	0x40291DA8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA875	0x40291DAC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA876	0x40291DB0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA877	0x40291DB4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA878	0x40291DB8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA879	0x40291DBC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA880	0x40291DC0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA881	0x40291DC4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA882	0x40291DC8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA883	0x40291DCC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA884	0x40291DD0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA885	0x40291DD4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA886	0x40291DD8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA887	0x40291DDC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA888	0x40291DE0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA889	0x40291DE4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA890	0x40291DE8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA891	0x40291DEC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA892	0x40291DF0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA893	0x40291DF4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA894	0x40291DF8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA895	0x40291DFC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA896	0x40291E00	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA897	0x40291E04	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA898	0x40291E08	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA899	0x40291E0C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA900	0x40291E10	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA901	0x40291E14	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA902	0x40291E18	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA903	0x40291E1C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA904	0x40291E20	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA905	0x40291E24	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA906	0x40291E28	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA907	0x40291E2C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA908	0x40291E30	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA909	0x40291E34	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA910	0x40291E38	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA911	0x40291E3C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA912	0x40291E40	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA913	0x40291E44	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA914	0x40291E48	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA915	0x40291E4C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA916	0x40291E50	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA917	0x40291E54	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA918	0x40291E58	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA919	0x40291E5C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA920	0x40291E60	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA921	0x40291E64	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA922	0x40291E68	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA923	0x40291E6C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA924	0x40291E70	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA925	0x40291E74	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA926	0x40291E78	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA927	0x40291E7C	FULL	Sensor Configuration Storage

Register Name	Address	Permission	Description
MSC_SENSOR_DATA928	0x40291E80	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA929	0x40291E84	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA930	0x40291E88	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA931	0x40291E8C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA932	0x40291E90	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA933	0x40291E94	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA934	0x40291E98	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA935	0x40291E9C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA936	0x40291EA0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA937	0x40291EA4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA938	0x40291EA8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA939	0x40291EAC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA940	0x40291EB0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA941	0x40291EB4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA942	0x40291EB8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA943	0x40291EBC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA944	0x40291EC0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA945	0x40291EC4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA946	0x40291EC8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA947	0x40291ECC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA948	0x40291ED0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA949	0x40291ED4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA950	0x40291ED8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA951	0x40291EDC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA952	0x40291EE0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA953	0x40291EE4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA954	0x40291EE8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA955	0x40291EEC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA956	0x40291EF0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA957	0x40291EF4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA958	0x40291EF8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA959	0x40291EFC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA960	0x40291F00	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA961	0x40291F04	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA962	0x40291F08	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA963	0x40291F0C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA964	0x40291F10	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA965	0x40291F14	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA966	0x40291F18	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA967	0x40291F1C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA968	0x40291F20	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA969	0x40291F24	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA970	0x40291F28	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA971	0x40291F2C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA972	0x40291F30	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA973	0x40291F34	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA974	0x40291F38	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA975	0x40291F3C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA976	0x40291F40	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA977	0x40291F44	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA978	0x40291F48	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA979	0x40291F4C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA980	0x40291F50	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA981	0x40291F54	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA982	0x40291F58	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA983	0x40291F5C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA984	0x40291F60	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA985	0x40291F64	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA986	0x40291F68	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA987	0x40291F6C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA988	0x40291F70	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA989	0x40291F74	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA990	0x40291F78	FULL	Sensor Configuration Storage

Register Name	Address	Permission	Description
MSC_SENSOR_DATA991	0x40291F7C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA992	0x40291F80	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA993	0x40291F84	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA994	0x40291F88	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA995	0x40291F8C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA996	0x40291F90	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA997	0x40291F94	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA998	0x40291F98	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA999	0x40291F9C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1000	0x40291FA0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1001	0x40291FA4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1002	0x40291FA8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1003	0x40291FAC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1004	0x40291FB0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1005	0x40291FB4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1006	0x40291FB8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1007	0x40291FBC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1008	0x40291FC0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1009	0x40291FC4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1010	0x40291FC8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1011	0x40291FCC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1012	0x40291FD0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1013	0x40291FD4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1014	0x40291FD8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1015	0x40291FDC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1016	0x40291FE0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1017	0x40291FE4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1018	0x40291FE8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1019	0x40291FEC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1020	0x40291FF0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1021	0x40291FF4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1022	0x40291FF8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1023	0x40291FFC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1024	0x40292000	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1025	0x40292004	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1026	0x40292008	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1027	0x4029200C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1028	0x40292010	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1029	0x40292014	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1030	0x40292018	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1031	0x4029201C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1032	0x40292020	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1033	0x40292024	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1034	0x40292028	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1035	0x4029202C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1036	0x40292030	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1037	0x40292034	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1038	0x40292038	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1039	0x4029203C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1040	0x40292040	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1041	0x40292044	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1042	0x40292048	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1043	0x4029204C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1044	0x40292050	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1045	0x40292054	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1046	0x40292058	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1047	0x4029205C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1048	0x40292060	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1049	0x40292064	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1050	0x40292068	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1051	0x4029206C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1052	0x40292070	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1053	0x40292074	FULL	Sensor Configuration Storage

Register Name	Address	Permission	Description
MSC_SENSOR_DATA1054	0x40292078	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1055	0x4029207C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1056	0x40292080	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1057	0x40292084	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1058	0x40292088	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1059	0x4029208C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1060	0x40292090	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1061	0x40292094	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1062	0x40292098	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1063	0x4029209C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1064	0x402920A0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1065	0x402920A4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1066	0x402920A8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1067	0x402920AC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1068	0x402920B0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1069	0x402920B4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1070	0x402920B8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1071	0x402920BC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1072	0x402920C0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1073	0x402920C4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1074	0x402920C8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1075	0x402920CC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1076	0x402920D0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1077	0x402920D4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1078	0x402920D8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1079	0x402920DC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1080	0x402920E0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1081	0x402920E4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1082	0x402920E8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1083	0x402920EC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1084	0x402920F0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1085	0x402920F4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1086	0x402920F8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1087	0x402920FC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1088	0x40292100	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1089	0x40292104	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1090	0x40292108	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1091	0x4029210C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1092	0x40292110	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1093	0x40292114	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1094	0x40292118	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1095	0x4029211C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1096	0x40292120	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1097	0x40292124	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1098	0x40292128	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1099	0x4029212C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1100	0x40292130	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1101	0x40292134	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1102	0x40292138	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1103	0x4029213C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1104	0x40292140	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1105	0x40292144	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1106	0x40292148	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1107	0x4029214C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1108	0x40292150	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1109	0x40292154	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1110	0x40292158	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1111	0x4029215C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1112	0x40292160	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1113	0x40292164	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1114	0x40292168	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1115	0x4029216C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1116	0x40292170	FULL	Sensor Configuration Storage

Register Name	Address	Permission	Description
MSC_SENSOR_DATA1117	0x40292174	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1118	0x40292178	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1119	0x4029217C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1120	0x40292180	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1121	0x40292184	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1122	0x40292188	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1123	0x4029218C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1124	0x40292190	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1125	0x40292194	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1126	0x40292198	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1127	0x4029219C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1128	0x402921A0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1129	0x402921A4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1130	0x402921A8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1131	0x402921AC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1132	0x402921B0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1133	0x402921B4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1134	0x402921B8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1135	0x402921BC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1136	0x402921C0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1137	0x402921C4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1138	0x402921C8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1139	0x402921CC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1140	0x402921D0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1141	0x402921D4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1142	0x402921D8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1143	0x402921DC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1144	0x402921E0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1145	0x402921E4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1146	0x402921E8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1147	0x402921EC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1148	0x402921F0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1149	0x402921F4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1150	0x402921F8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1151	0x402921FC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1152	0x40292200	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1153	0x40292204	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1154	0x40292208	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1155	0x4029220C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1156	0x40292210	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1157	0x40292214	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1158	0x40292218	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1159	0x4029221C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1160	0x40292220	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1161	0x40292224	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1162	0x40292228	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1163	0x4029222C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1164	0x40292230	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1165	0x40292234	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1166	0x40292238	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1167	0x4029223C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1168	0x40292240	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1169	0x40292244	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1170	0x40292248	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1171	0x4029224C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1172	0x40292250	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1173	0x40292254	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1174	0x40292258	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1175	0x4029225C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1176	0x40292260	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1177	0x40292264	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1178	0x40292268	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1179	0x4029226C	FULL	Sensor Configuration Storage

Register Name	Address	Permission	Description
MSC_SENSOR_DATA1180	0x40292270	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1181	0x40292274	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1182	0x40292278	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1183	0x4029227C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1184	0x40292280	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1185	0x40292284	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1186	0x40292288	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1187	0x4029228C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1188	0x40292290	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1189	0x40292294	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1190	0x40292298	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1191	0x4029229C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1192	0x402922A0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1193	0x402922A4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1194	0x402922A8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1195	0x402922AC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1196	0x402922B0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1197	0x402922B4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1198	0x402922B8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1199	0x402922BC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1200	0x402922C0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1201	0x402922C4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1202	0x402922C8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1203	0x402922CC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1204	0x402922D0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1205	0x402922D4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1206	0x402922D8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1207	0x402922DC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1208	0x402922E0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1209	0x402922E4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1210	0x402922E8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1211	0x402922EC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1212	0x402922F0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1213	0x402922F4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1214	0x402922F8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1215	0x402922FC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1216	0x40292300	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1217	0x40292304	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1218	0x40292308	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1219	0x4029230C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1220	0x40292310	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1221	0x40292314	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1222	0x40292318	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1223	0x4029231C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1224	0x40292320	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1225	0x40292324	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1226	0x40292328	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1227	0x4029232C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1228	0x40292330	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1229	0x40292334	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1230	0x40292338	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1231	0x4029233C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1232	0x40292340	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1233	0x40292344	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1234	0x40292348	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1235	0x4029234C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1236	0x40292350	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1237	0x40292354	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1238	0x40292358	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1239	0x4029235C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1240	0x40292360	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1241	0x40292364	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1242	0x40292368	FULL	Sensor Configuration Storage

Register Name	Address	Permission	Description
MSC_SENSOR_DATA1243	0x4029236C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1244	0x40292370	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1245	0x40292374	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1246	0x40292378	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1247	0x4029237C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1248	0x40292380	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1249	0x40292384	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1250	0x40292388	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1251	0x4029238C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1252	0x40292390	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1253	0x40292394	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1254	0x40292398	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1255	0x4029239C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1256	0x402923A0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1257	0x402923A4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1258	0x402923A8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1259	0x402923AC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1260	0x402923B0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1261	0x402923B4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1262	0x402923B8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1263	0x402923BC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1264	0x402923C0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1265	0x402923C4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1266	0x402923C8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1267	0x402923CC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1268	0x402923D0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1269	0x402923D4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1270	0x402923D8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1271	0x402923DC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1272	0x402923E0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1273	0x402923E4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1274	0x402923E8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1275	0x402923EC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1276	0x402923F0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1277	0x402923F4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1278	0x402923F8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1279	0x402923FC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1280	0x40292400	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1281	0x40292404	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1282	0x40292408	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1283	0x4029240C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1284	0x40292410	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1285	0x40292414	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1286	0x40292418	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1287	0x4029241C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1288	0x40292420	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1289	0x40292424	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1290	0x40292428	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1291	0x4029242C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1292	0x40292430	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1293	0x40292434	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1294	0x40292438	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1295	0x4029243C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1296	0x40292440	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1297	0x40292444	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1298	0x40292448	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1299	0x4029244C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1300	0x40292450	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1301	0x40292454	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1302	0x40292458	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1303	0x4029245C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1304	0x40292460	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1305	0x40292464	FULL	Sensor Configuration Storage

Register Name	Address	Permission	Description
MSC_SENSOR_DATA1306	0x40292468	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1307	0x4029246C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1308	0x40292470	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1309	0x40292474	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1310	0x40292478	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1311	0x4029247C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1312	0x40292480	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1313	0x40292484	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1314	0x40292488	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1315	0x4029248C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1316	0x40292490	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1317	0x40292494	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1318	0x40292498	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1319	0x4029249C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1320	0x402924A0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1321	0x402924A4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1322	0x402924A8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1323	0x402924AC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1324	0x402924B0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1325	0x402924B4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1326	0x402924B8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1327	0x402924BC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1328	0x402924C0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1329	0x402924C4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1330	0x402924C8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1331	0x402924CC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1332	0x402924D0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1333	0x402924D4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1334	0x402924D8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1335	0x402924DC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1336	0x402924E0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1337	0x402924E4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1338	0x402924E8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1339	0x402924EC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1340	0x402924F0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1341	0x402924F4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1342	0x402924F8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1343	0x402924FC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1344	0x40292500	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1345	0x40292504	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1346	0x40292508	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1347	0x4029250C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1348	0x40292510	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1349	0x40292514	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1350	0x40292518	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1351	0x4029251C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1352	0x40292520	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1353	0x40292524	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1354	0x40292528	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1355	0x4029252C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1356	0x40292530	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1357	0x40292534	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1358	0x40292538	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1359	0x4029253C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1360	0x40292540	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1361	0x40292544	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1362	0x40292548	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1363	0x4029254C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1364	0x40292550	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1365	0x40292554	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1366	0x40292558	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1367	0x4029255C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1368	0x40292560	FULL	Sensor Configuration Storage

Register Name	Address	Permission	Description
MSC_SENSOR_DATA1369	0x40292564	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1370	0x40292568	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1371	0x4029256C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1372	0x40292570	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1373	0x40292574	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1374	0x40292578	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1375	0x4029257C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1376	0x40292580	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1377	0x40292584	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1378	0x40292588	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1379	0x4029258C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1380	0x40292590	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1381	0x40292594	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1382	0x40292598	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1383	0x4029259C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1384	0x402925A0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1385	0x402925A4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1386	0x402925A8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1387	0x402925AC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1388	0x402925B0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1389	0x402925B4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1390	0x402925B8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1391	0x402925BC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1392	0x402925C0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1393	0x402925C4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1394	0x402925C8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1395	0x402925CC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1396	0x402925D0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1397	0x402925D4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1398	0x402925D8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1399	0x402925DC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1400	0x402925E0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1401	0x402925E4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1402	0x402925E8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1403	0x402925EC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1404	0x402925F0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1405	0x402925F4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1406	0x402925F8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1407	0x402925FC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1408	0x40292600	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1409	0x40292604	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1410	0x40292608	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1411	0x4029260C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1412	0x40292610	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1413	0x40292614	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1414	0x40292618	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1415	0x4029261C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1416	0x40292620	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1417	0x40292624	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1418	0x40292628	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1419	0x4029262C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1420	0x40292630	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1421	0x40292634	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1422	0x40292638	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1423	0x4029263C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1424	0x40292640	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1425	0x40292644	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1426	0x40292648	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1427	0x4029264C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1428	0x40292650	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1429	0x40292654	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1430	0x40292658	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1431	0x4029265C	FULL	Sensor Configuration Storage

Register Name	Address	Permission	Description
MSC_SENSOR_DATA1432	0x40292660	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1433	0x40292664	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1434	0x40292668	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1435	0x4029266C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1436	0x40292670	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1437	0x40292674	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1438	0x40292678	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1439	0x4029267C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1440	0x40292680	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1441	0x40292684	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1442	0x40292688	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1443	0x4029268C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1444	0x40292690	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1445	0x40292694	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1446	0x40292698	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1447	0x4029269C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1448	0x402926A0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1449	0x402926A4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1450	0x402926A8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1451	0x402926AC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1452	0x402926B0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1453	0x402926B4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1454	0x402926B8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1455	0x402926BC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1456	0x402926C0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1457	0x402926C4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1458	0x402926C8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1459	0x402926CC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1460	0x402926D0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1461	0x402926D4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1462	0x402926D8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1463	0x402926DC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1464	0x402926E0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1465	0x402926E4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1466	0x402926E8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1467	0x402926EC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1468	0x402926F0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1469	0x402926F4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1470	0x402926F8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1471	0x402926FC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1472	0x40292700	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1473	0x40292704	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1474	0x40292708	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1475	0x4029270C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1476	0x40292710	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1477	0x40292714	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1478	0x40292718	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1479	0x4029271C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1480	0x40292720	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1481	0x40292724	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1482	0x40292728	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1483	0x4029272C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1484	0x40292730	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1485	0x40292734	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1486	0x40292738	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1487	0x4029273C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1488	0x40292740	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1489	0x40292744	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1490	0x40292748	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1491	0x4029274C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1492	0x40292750	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1493	0x40292754	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1494	0x40292758	FULL	Sensor Configuration Storage

Register Name	Address	Permission	Description
MSC_SENSOR_DATA1495	0x4029275C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1496	0x40292760	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1497	0x40292764	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1498	0x40292768	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1499	0x4029276C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1500	0x40292770	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1501	0x40292774	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1502	0x40292778	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1503	0x4029277C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1504	0x40292780	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1505	0x40292784	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1506	0x40292788	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1507	0x4029278C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1508	0x40292790	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1509	0x40292794	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1510	0x40292798	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1511	0x4029279C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1512	0x402927A0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1513	0x402927A4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1514	0x402927A8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1515	0x402927AC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1516	0x402927B0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1517	0x402927B4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1518	0x402927B8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1519	0x402927BC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1520	0x402927C0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1521	0x402927C4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1522	0x402927C8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1523	0x402927CC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1524	0x402927D0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1525	0x402927D4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1526	0x402927D8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1527	0x402927DC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1528	0x402927E0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1529	0x402927E4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1530	0x402927E8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1531	0x402927EC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1532	0x402927F0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1533	0x402927F4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1534	0x402927F8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1535	0x402927FC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1536	0x40292800	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1537	0x40292804	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1538	0x40292808	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1539	0x4029280C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1540	0x40292810	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1541	0x40292814	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1542	0x40292818	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1543	0x4029281C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1544	0x40292820	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1545	0x40292824	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1546	0x40292828	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1547	0x4029282C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1548	0x40292830	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1549	0x40292834	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1550	0x40292838	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1551	0x4029283C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1552	0x40292840	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1553	0x40292844	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1554	0x40292848	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1555	0x4029284C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1556	0x40292850	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1557	0x40292854	FULL	Sensor Configuration Storage

Register Name	Address	Permission	Description
MSC_SENSOR_DATA1558	0x40292858	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1559	0x4029285C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1560	0x40292860	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1561	0x40292864	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1562	0x40292868	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1563	0x4029286C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1564	0x40292870	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1565	0x40292874	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1566	0x40292878	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1567	0x4029287C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1568	0x40292880	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1569	0x40292884	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1570	0x40292888	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1571	0x4029288C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1572	0x40292890	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1573	0x40292894	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1574	0x40292898	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1575	0x4029289C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1576	0x402928A0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1577	0x402928A4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1578	0x402928A8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1579	0x402928AC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1580	0x402928B0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1581	0x402928B4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1582	0x402928B8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1583	0x402928BC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1584	0x402928C0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1585	0x402928C4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1586	0x402928C8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1587	0x402928CC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1588	0x402928D0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1589	0x402928D4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1590	0x402928D8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1591	0x402928DC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1592	0x402928E0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1593	0x402928E4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1594	0x402928E8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1595	0x402928EC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1596	0x402928F0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1597	0x402928F4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1598	0x402928F8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1599	0x402928FC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1600	0x40292900	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1601	0x40292904	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1602	0x40292908	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1603	0x4029290C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1604	0x40292910	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1605	0x40292914	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1606	0x40292918	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1607	0x4029291C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1608	0x40292920	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1609	0x40292924	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1610	0x40292928	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1611	0x4029292C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1612	0x40292930	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1613	0x40292934	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1614	0x40292938	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1615	0x4029293C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1616	0x40292940	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1617	0x40292944	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1618	0x40292948	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1619	0x4029294C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1620	0x40292950	FULL	Sensor Configuration Storage

Register Name	Address	Permission	Description
MSC_SENSOR_DATA1621	0x40292954	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1622	0x40292958	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1623	0x4029295C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1624	0x40292960	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1625	0x40292964	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1626	0x40292968	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1627	0x4029296C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1628	0x40292970	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1629	0x40292974	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1630	0x40292978	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1631	0x4029297C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1632	0x40292980	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1633	0x40292984	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1634	0x40292988	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1635	0x4029298C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1636	0x40292990	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1637	0x40292994	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1638	0x40292998	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1639	0x4029299C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1640	0x402929A0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1641	0x402929A4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1642	0x402929A8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1643	0x402929AC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1644	0x402929B0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1645	0x402929B4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1646	0x402929B8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1647	0x402929BC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1648	0x402929C0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1649	0x402929C4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1650	0x402929C8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1651	0x402929CC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1652	0x402929D0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1653	0x402929D4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1654	0x402929D8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1655	0x402929DC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1656	0x402929E0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1657	0x402929E4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1658	0x402929E8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1659	0x402929EC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1660	0x402929F0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1661	0x402929F4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1662	0x402929F8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1663	0x402929FC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1664	0x40292A00	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1665	0x40292A04	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1666	0x40292A08	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1667	0x40292A0C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1668	0x40292A10	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1669	0x40292A14	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1670	0x40292A18	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1671	0x40292A1C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1672	0x40292A20	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1673	0x40292A24	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1674	0x40292A28	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1675	0x40292A2C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1676	0x40292A30	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1677	0x40292A34	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1678	0x40292A38	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1679	0x40292A3C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1680	0x40292A40	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1681	0x40292A44	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1682	0x40292A48	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1683	0x40292A4C	FULL	Sensor Configuration Storage

Register Name	Address	Permission	Description
MSC_SENSOR_DATA1684	0x40292A50	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1685	0x40292A54	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1686	0x40292A58	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1687	0x40292A5C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1688	0x40292A60	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1689	0x40292A64	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1690	0x40292A68	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1691	0x40292A6C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1692	0x40292A70	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1693	0x40292A74	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1694	0x40292A78	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1695	0x40292A7C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1696	0x40292A80	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1697	0x40292A84	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1698	0x40292A88	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1699	0x40292A8C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1700	0x40292A90	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1701	0x40292A94	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1702	0x40292A98	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1703	0x40292A9C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1704	0x40292AA0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1705	0x40292AA4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1706	0x40292AA8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1707	0x40292AAC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1708	0x40292AB0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1709	0x40292AB4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1710	0x40292AB8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1711	0x40292ABC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1712	0x40292AC0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1713	0x40292AC4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1714	0x40292AC8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1715	0x40292ACC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1716	0x40292AD0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1717	0x40292AD4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1718	0x40292AD8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1719	0x40292ADC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1720	0x40292AE0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1721	0x40292AE4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1722	0x40292AE8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1723	0x40292AEC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1724	0x40292AF0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1725	0x40292AF4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1726	0x40292AF8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1727	0x40292AFC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1728	0x40292B00	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1729	0x40292B04	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1730	0x40292B08	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1731	0x40292B0C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1732	0x40292B10	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1733	0x40292B14	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1734	0x40292B18	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1735	0x40292B1C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1736	0x40292B20	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1737	0x40292B24	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1738	0x40292B28	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1739	0x40292B2C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1740	0x40292B30	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1741	0x40292B34	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1742	0x40292B38	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1743	0x40292B3C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1744	0x40292B40	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1745	0x40292B44	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1746	0x40292B48	FULL	Sensor Configuration Storage

Register Name	Address	Permission	Description
MSC_SENSOR_DATA1747	0x40292B4C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1748	0x40292B50	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1749	0x40292B54	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1750	0x40292B58	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1751	0x40292B5C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1752	0x40292B60	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1753	0x40292B64	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1754	0x40292B68	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1755	0x40292B6C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1756	0x40292B70	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1757	0x40292B74	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1758	0x40292B78	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1759	0x40292B7C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1760	0x40292B80	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1761	0x40292B84	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1762	0x40292B88	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1763	0x40292B8C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1764	0x40292B90	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1765	0x40292B94	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1766	0x40292B98	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1767	0x40292B9C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1768	0x40292BA0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1769	0x40292BA4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1770	0x40292BA8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1771	0x40292BAC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1772	0x40292BB0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1773	0x40292BB4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1774	0x40292BB8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1775	0x40292BBC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1776	0x40292BC0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1777	0x40292BC4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1778	0x40292BC8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1779	0x40292BCC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1780	0x40292BD0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1781	0x40292BD4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1782	0x40292BD8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1783	0x40292BDC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1784	0x40292BE0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1785	0x40292BE4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1786	0x40292BE8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1787	0x40292BEC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1788	0x40292BF0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1789	0x40292BF4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1790	0x40292BF8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1791	0x40292BFC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1792	0x40292C00	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1793	0x40292C04	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1794	0x40292C08	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1795	0x40292C0C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1796	0x40292C10	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1797	0x40292C14	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1798	0x40292C18	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1799	0x40292C1C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1800	0x40292C20	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1801	0x40292C24	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1802	0x40292C28	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1803	0x40292C2C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1804	0x40292C30	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1805	0x40292C34	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1806	0x40292C38	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1807	0x40292C3C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1808	0x40292C40	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1809	0x40292C44	FULL	Sensor Configuration Storage

Register Name	Address	Permission	Description
MSC_SENSOR_DATA1810	0x40292C48	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1811	0x40292C4C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1812	0x40292C50	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1813	0x40292C54	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1814	0x40292C58	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1815	0x40292C5C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1816	0x40292C60	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1817	0x40292C64	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1818	0x40292C68	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1819	0x40292C6C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1820	0x40292C70	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1821	0x40292C74	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1822	0x40292C78	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1823	0x40292C7C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1824	0x40292C80	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1825	0x40292C84	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1826	0x40292C88	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1827	0x40292C8C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1828	0x40292C90	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1829	0x40292C94	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1830	0x40292C98	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1831	0x40292C9C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1832	0x40292CA0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1833	0x40292CA4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1834	0x40292CA8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1835	0x40292CAC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1836	0x40292CB0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1837	0x40292CB4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1838	0x40292CB8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1839	0x40292CBC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1840	0x40292CC0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1841	0x40292CC4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1842	0x40292CC8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1843	0x40292CCC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1844	0x40292CD0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1845	0x40292CD4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1846	0x40292CD8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1847	0x40292CDC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1848	0x40292CE0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1849	0x40292CE4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1850	0x40292CE8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1851	0x40292CEC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1852	0x40292CF0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1853	0x40292CF4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1854	0x40292CF8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1855	0x40292CFC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1856	0x40292D00	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1857	0x40292D04	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1858	0x40292D08	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1859	0x40292D0C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1860	0x40292D10	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1861	0x40292D14	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1862	0x40292D18	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1863	0x40292D1C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1864	0x40292D20	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1865	0x40292D24	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1866	0x40292D28	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1867	0x40292D2C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1868	0x40292D30	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1869	0x40292D34	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1870	0x40292D38	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1871	0x40292D3C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1872	0x40292D40	FULL	Sensor Configuration Storage

Register Name	Address	Permission	Description
MSC_SENSOR_DATA1873	0x40292D44	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1874	0x40292D48	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1875	0x40292D4C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1876	0x40292D50	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1877	0x40292D54	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1878	0x40292D58	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1879	0x40292D5C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1880	0x40292D60	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1881	0x40292D64	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1882	0x40292D68	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1883	0x40292D6C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1884	0x40292D70	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1885	0x40292D74	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1886	0x40292D78	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1887	0x40292D7C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1888	0x40292D80	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1889	0x40292D84	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1890	0x40292D88	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1891	0x40292D8C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1892	0x40292D90	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1893	0x40292D94	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1894	0x40292D98	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1895	0x40292D9C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1896	0x40292DA0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1897	0x40292DA4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1898	0x40292DA8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1899	0x40292DAC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1900	0x40292DB0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1901	0x40292DB4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1902	0x40292DB8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1903	0x40292DBC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1904	0x40292DC0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1905	0x40292DC4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1906	0x40292DC8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1907	0x40292DCC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1908	0x40292DD0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1909	0x40292DD4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1910	0x40292DD8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1911	0x40292DDC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1912	0x40292DE0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1913	0x40292DE4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1914	0x40292DE8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1915	0x40292DEC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1916	0x40292DF0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1917	0x40292DF4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1918	0x40292DF8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1919	0x40292DFC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1920	0x40292E00	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1921	0x40292E04	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1922	0x40292E08	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1923	0x40292E0C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1924	0x40292E10	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1925	0x40292E14	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1926	0x40292E18	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1927	0x40292E1C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1928	0x40292E20	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1929	0x40292E24	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1930	0x40292E28	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1931	0x40292E2C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1932	0x40292E30	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1933	0x40292E34	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1934	0x40292E38	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1935	0x40292E3C	FULL	Sensor Configuration Storage

Register Name	Address	Permission	Description
MSC_SENSOR_DATA1936	0x40292E40	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1937	0x40292E44	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1938	0x40292E48	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1939	0x40292E4C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1940	0x40292E50	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1941	0x40292E54	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1942	0x40292E58	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1943	0x40292E5C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1944	0x40292E60	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1945	0x40292E64	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1946	0x40292E68	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1947	0x40292E6C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1948	0x40292E70	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1949	0x40292E74	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1950	0x40292E78	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1951	0x40292E7C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1952	0x40292E80	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1953	0x40292E84	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1954	0x40292E88	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1955	0x40292E8C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1956	0x40292E90	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1957	0x40292E94	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1958	0x40292E98	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1959	0x40292E9C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1960	0x40292EA0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1961	0x40292EA4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1962	0x40292EA8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1963	0x40292EAC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1964	0x40292EB0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1965	0x40292EB4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1966	0x40292EB8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1967	0x40292EBC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1968	0x40292EC0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1969	0x40292EC4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1970	0x40292EC8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1971	0x40292ECC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1972	0x40292ED0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1973	0x40292ED4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1974	0x40292ED8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1975	0x40292EDC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1976	0x40292EE0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1977	0x40292EE4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1978	0x40292EE8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1979	0x40292EEC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1980	0x40292EF0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1981	0x40292EF4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1982	0x40292EF8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1983	0x40292EFC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1984	0x40292F00	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1985	0x40292F04	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1986	0x40292F08	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1987	0x40292F0C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1988	0x40292F10	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1989	0x40292F14	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1990	0x40292F18	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1991	0x40292F1C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1992	0x40292F20	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1993	0x40292F24	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1994	0x40292F28	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1995	0x40292F2C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1996	0x40292F30	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1997	0x40292F34	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA1998	0x40292F38	FULL	Sensor Configuration Storage

Register Name	Address	Permission	Description
MSC_SENSOR_DATA1999	0x40292F3C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2000	0x40292F40	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2001	0x40292F44	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2002	0x40292F48	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2003	0x40292F4C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2004	0x40292F50	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2005	0x40292F54	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2006	0x40292F58	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2007	0x40292F5C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2008	0x40292F60	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2009	0x40292F64	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2010	0x40292F68	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2011	0x40292F6C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2012	0x40292F70	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2013	0x40292F74	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2014	0x40292F78	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2015	0x40292F7C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2016	0x40292F80	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2017	0x40292F84	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2018	0x40292F88	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2019	0x40292F8C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2020	0x40292F90	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2021	0x40292F94	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2022	0x40292F98	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2023	0x40292F9C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2024	0x40292FA0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2025	0x40292FA4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2026	0x40292FA8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2027	0x40292FAC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2028	0x40292FB0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2029	0x40292FB4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2030	0x40292FB8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2031	0x40292FBC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2032	0x40292FC0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2033	0x40292FC4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2034	0x40292FC8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2035	0x40292FCC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2036	0x40292FD0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2037	0x40292FD4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2038	0x40292FD8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2039	0x40292FDC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2040	0x40292FE0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2041	0x40292FE4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2042	0x40292FE8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2043	0x40292FEC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2044	0x40292FF0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2045	0x40292FF4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2046	0x40292FF8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2047	0x40292FFC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2048	0x40293000	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2049	0x40293004	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2050	0x40293008	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2051	0x4029300C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2052	0x40293010	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2053	0x40293014	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2054	0x40293018	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2055	0x4029301C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2056	0x40293020	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2057	0x40293024	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2058	0x40293028	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2059	0x4029302C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2060	0x40293030	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2061	0x40293034	FULL	Sensor Configuration Storage

Register Name	Address	Permission	Description
MSC_SENSOR_DATA2062	0x40293038	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2063	0x4029303C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2064	0x40293040	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2065	0x40293044	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2066	0x40293048	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2067	0x4029304C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2068	0x40293050	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2069	0x40293054	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2070	0x40293058	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2071	0x4029305C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2072	0x40293060	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2073	0x40293064	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2074	0x40293068	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2075	0x4029306C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2076	0x40293070	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2077	0x40293074	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2078	0x40293078	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2079	0x4029307C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2080	0x40293080	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2081	0x40293084	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2082	0x40293088	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2083	0x4029308C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2084	0x40293090	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2085	0x40293094	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2086	0x40293098	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2087	0x4029309C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2088	0x402930A0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2089	0x402930A4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2090	0x402930A8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2091	0x402930AC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2092	0x402930B0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2093	0x402930B4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2094	0x402930B8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2095	0x402930BC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2096	0x402930C0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2097	0x402930C4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2098	0x402930C8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2099	0x402930CC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2100	0x402930D0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2101	0x402930D4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2102	0x402930D8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2103	0x402930DC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2104	0x402930E0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2105	0x402930E4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2106	0x402930E8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2107	0x402930EC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2108	0x402930F0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2109	0x402930F4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2110	0x402930F8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2111	0x402930FC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2112	0x40293100	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2113	0x40293104	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2114	0x40293108	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2115	0x4029310C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2116	0x40293110	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2117	0x40293114	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2118	0x40293118	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2119	0x4029311C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2120	0x40293120	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2121	0x40293124	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2122	0x40293128	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2123	0x4029312C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2124	0x40293130	FULL	Sensor Configuration Storage

Register Name	Address	Permission	Description
MSC_SENSOR_DATA2125	0x40293134	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2126	0x40293138	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2127	0x4029313C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2128	0x40293140	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2129	0x40293144	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2130	0x40293148	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2131	0x4029314C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2132	0x40293150	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2133	0x40293154	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2134	0x40293158	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2135	0x4029315C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2136	0x40293160	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2137	0x40293164	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2138	0x40293168	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2139	0x4029316C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2140	0x40293170	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2141	0x40293174	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2142	0x40293178	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2143	0x4029317C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2144	0x40293180	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2145	0x40293184	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2146	0x40293188	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2147	0x4029318C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2148	0x40293190	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2149	0x40293194	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2150	0x40293198	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2151	0x4029319C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2152	0x402931A0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2153	0x402931A4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2154	0x402931A8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2155	0x402931AC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2156	0x402931B0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2157	0x402931B4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2158	0x402931B8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2159	0x402931BC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2160	0x402931C0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2161	0x402931C4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2162	0x402931C8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2163	0x402931CC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2164	0x402931D0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2165	0x402931D4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2166	0x402931D8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2167	0x402931DC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2168	0x402931E0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2169	0x402931E4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2170	0x402931E8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2171	0x402931EC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2172	0x402931F0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2173	0x402931F4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2174	0x402931F8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2175	0x402931FC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2176	0x40293200	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2177	0x40293204	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2178	0x40293208	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2179	0x4029320C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2180	0x40293210	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2181	0x40293214	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2182	0x40293218	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2183	0x4029321C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2184	0x40293220	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2185	0x40293224	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2186	0x40293228	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2187	0x4029322C	FULL	Sensor Configuration Storage

Register Name	Address	Permission	Description
MSC_SENSOR_DATA2188	0x40293230	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2189	0x40293234	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2190	0x40293238	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2191	0x4029323C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2192	0x40293240	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2193	0x40293244	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2194	0x40293248	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2195	0x4029324C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2196	0x40293250	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2197	0x40293254	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2198	0x40293258	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2199	0x4029325C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2200	0x40293260	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2201	0x40293264	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2202	0x40293268	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2203	0x4029326C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2204	0x40293270	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2205	0x40293274	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2206	0x40293278	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2207	0x4029327C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2208	0x40293280	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2209	0x40293284	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2210	0x40293288	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2211	0x4029328C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2212	0x40293290	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2213	0x40293294	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2214	0x40293298	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2215	0x4029329C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2216	0x402932A0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2217	0x402932A4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2218	0x402932A8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2219	0x402932AC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2220	0x402932B0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2221	0x402932B4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2222	0x402932B8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2223	0x402932BC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2224	0x402932C0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2225	0x402932C4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2226	0x402932C8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2227	0x402932CC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2228	0x402932D0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2229	0x402932D4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2230	0x402932D8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2231	0x402932DC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2232	0x402932E0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2233	0x402932E4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2234	0x402932E8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2235	0x402932EC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2236	0x402932F0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2237	0x402932F4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2238	0x402932F8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2239	0x402932FC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2240	0x40293300	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2241	0x40293304	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2242	0x40293308	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2243	0x4029330C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2244	0x40293310	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2245	0x40293314	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2246	0x40293318	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2247	0x4029331C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2248	0x40293320	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2249	0x40293324	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2250	0x40293328	FULL	Sensor Configuration Storage

Register Name	Address	Permission	Description
MSC_SENSOR_DATA2251	0x4029332C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2252	0x40293330	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2253	0x40293334	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2254	0x40293338	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2255	0x4029333C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2256	0x40293340	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2257	0x40293344	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2258	0x40293348	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2259	0x4029334C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2260	0x40293350	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2261	0x40293354	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2262	0x40293358	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2263	0x4029335C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2264	0x40293360	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2265	0x40293364	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2266	0x40293368	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2267	0x4029336C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2268	0x40293370	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2269	0x40293374	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2270	0x40293378	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2271	0x4029337C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2272	0x40293380	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2273	0x40293384	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2274	0x40293388	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2275	0x4029338C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2276	0x40293390	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2277	0x40293394	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2278	0x40293398	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2279	0x4029339C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2280	0x402933A0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2281	0x402933A4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2282	0x402933A8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2283	0x402933AC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2284	0x402933B0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2285	0x402933B4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2286	0x402933B8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2287	0x402933BC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2288	0x402933C0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2289	0x402933C4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2290	0x402933C8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2291	0x402933CC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2292	0x402933D0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2293	0x402933D4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2294	0x402933D8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2295	0x402933DC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2296	0x402933E0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2297	0x402933E4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2298	0x402933E8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2299	0x402933EC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2300	0x402933F0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2301	0x402933F4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2302	0x402933F8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2303	0x402933FC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2304	0x40293400	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2305	0x40293404	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2306	0x40293408	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2307	0x4029340C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2308	0x40293410	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2309	0x40293414	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2310	0x40293418	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2311	0x4029341C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2312	0x40293420	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2313	0x40293424	FULL	Sensor Configuration Storage

Register Name	Address	Permission	Description
MSC_SENSOR_DATA2314	0x40293428	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2315	0x4029342C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2316	0x40293430	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2317	0x40293434	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2318	0x40293438	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2319	0x4029343C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2320	0x40293440	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2321	0x40293444	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2322	0x40293448	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2323	0x4029344C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2324	0x40293450	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2325	0x40293454	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2326	0x40293458	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2327	0x4029345C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2328	0x40293460	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2329	0x40293464	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2330	0x40293468	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2331	0x4029346C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2332	0x40293470	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2333	0x40293474	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2334	0x40293478	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2335	0x4029347C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2336	0x40293480	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2337	0x40293484	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2338	0x40293488	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2339	0x4029348C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2340	0x40293490	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2341	0x40293494	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2342	0x40293498	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2343	0x4029349C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2344	0x402934A0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2345	0x402934A4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2346	0x402934A8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2347	0x402934AC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2348	0x402934B0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2349	0x402934B4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2350	0x402934B8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2351	0x402934BC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2352	0x402934C0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2353	0x402934C4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2354	0x402934C8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2355	0x402934CC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2356	0x402934D0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2357	0x402934D4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2358	0x402934D8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2359	0x402934DC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2360	0x402934E0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2361	0x402934E4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2362	0x402934E8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2363	0x402934EC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2364	0x402934F0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2365	0x402934F4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2366	0x402934F8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2367	0x402934FC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2368	0x40293500	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2369	0x40293504	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2370	0x40293508	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2371	0x4029350C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2372	0x40293510	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2373	0x40293514	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2374	0x40293518	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2375	0x4029351C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2376	0x40293520	FULL	Sensor Configuration Storage

Register Name	Address	Permission	Description
MSC_SENSOR_DATA2377	0x40293524	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2378	0x40293528	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2379	0x4029352C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2380	0x40293530	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2381	0x40293534	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2382	0x40293538	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2383	0x4029353C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2384	0x40293540	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2385	0x40293544	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2386	0x40293548	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2387	0x4029354C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2388	0x40293550	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2389	0x40293554	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2390	0x40293558	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2391	0x4029355C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2392	0x40293560	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2393	0x40293564	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2394	0x40293568	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2395	0x4029356C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2396	0x40293570	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2397	0x40293574	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2398	0x40293578	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2399	0x4029357C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2400	0x40293580	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2401	0x40293584	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2402	0x40293588	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2403	0x4029358C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2404	0x40293590	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2405	0x40293594	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2406	0x40293598	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2407	0x4029359C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2408	0x402935A0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2409	0x402935A4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2410	0x402935A8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2411	0x402935AC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2412	0x402935B0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2413	0x402935B4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2414	0x402935B8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2415	0x402935BC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2416	0x402935C0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2417	0x402935C4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2418	0x402935C8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2419	0x402935CC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2420	0x402935D0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2421	0x402935D4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2422	0x402935D8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2423	0x402935DC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2424	0x402935E0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2425	0x402935E4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2426	0x402935E8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2427	0x402935EC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2428	0x402935F0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2429	0x402935F4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2430	0x402935F8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2431	0x402935FC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2432	0x40293600	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2433	0x40293604	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2434	0x40293608	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2435	0x4029360C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2436	0x40293610	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2437	0x40293614	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2438	0x40293618	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2439	0x4029361C	FULL	Sensor Configuration Storage

Register Name	Address	Permission	Description
MSC_SENSOR_DATA2440	0x40293620	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2441	0x40293624	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2442	0x40293628	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2443	0x4029362C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2444	0x40293630	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2445	0x40293634	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2446	0x40293638	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2447	0x4029363C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2448	0x40293640	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2449	0x40293644	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2450	0x40293648	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2451	0x4029364C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2452	0x40293650	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2453	0x40293654	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2454	0x40293658	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2455	0x4029365C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2456	0x40293660	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2457	0x40293664	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2458	0x40293668	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2459	0x4029366C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2460	0x40293670	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2461	0x40293674	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2462	0x40293678	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2463	0x4029367C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2464	0x40293680	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2465	0x40293684	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2466	0x40293688	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2467	0x4029368C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2468	0x40293690	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2469	0x40293694	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2470	0x40293698	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2471	0x4029369C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2472	0x402936A0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2473	0x402936A4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2474	0x402936A8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2475	0x402936AC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2476	0x402936B0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2477	0x402936B4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2478	0x402936B8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2479	0x402936BC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2480	0x402936C0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2481	0x402936C4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2482	0x402936C8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2483	0x402936CC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2484	0x402936D0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2485	0x402936D4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2486	0x402936D8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2487	0x402936DC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2488	0x402936E0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2489	0x402936E4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2490	0x402936E8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2491	0x402936EC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2492	0x402936F0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2493	0x402936F4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2494	0x402936F8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2495	0x402936FC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2496	0x40293700	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2497	0x40293704	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2498	0x40293708	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2499	0x4029370C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2500	0x40293710	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2501	0x40293714	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2502	0x40293718	FULL	Sensor Configuration Storage

Register Name	Address	Permission	Description
MSC_SENSOR_DATA2503	0x4029371C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2504	0x40293720	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2505	0x40293724	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2506	0x40293728	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2507	0x4029372C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2508	0x40293730	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2509	0x40293734	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2510	0x40293738	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2511	0x4029373C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2512	0x40293740	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2513	0x40293744	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2514	0x40293748	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2515	0x4029374C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2516	0x40293750	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2517	0x40293754	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2518	0x40293758	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2519	0x4029375C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2520	0x40293760	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2521	0x40293764	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2522	0x40293768	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2523	0x4029376C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2524	0x40293770	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2525	0x40293774	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2526	0x40293778	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2527	0x4029377C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2528	0x40293780	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2529	0x40293784	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2530	0x40293788	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2531	0x4029378C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2532	0x40293790	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2533	0x40293794	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2534	0x40293798	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2535	0x4029379C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2536	0x402937A0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2537	0x402937A4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2538	0x402937A8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2539	0x402937AC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2540	0x402937B0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2541	0x402937B4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2542	0x402937B8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2543	0x402937BC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2544	0x402937C0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2545	0x402937C4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2546	0x402937C8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2547	0x402937CC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2548	0x402937D0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2549	0x402937D4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2550	0x402937D8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2551	0x402937DC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2552	0x402937E0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2553	0x402937E4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2554	0x402937E8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2555	0x402937EC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2556	0x402937F0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2557	0x402937F4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2558	0x402937F8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2559	0x402937FC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2560	0x40293800	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2561	0x40293804	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2562	0x40293808	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2563	0x4029380C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2564	0x40293810	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2565	0x40293814	FULL	Sensor Configuration Storage

Register Name	Address	Permission	Description
MSC_SENSOR_DATA2566	0x40293818	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2567	0x4029381C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2568	0x40293820	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2569	0x40293824	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2570	0x40293828	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2571	0x4029382C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2572	0x40293830	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2573	0x40293834	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2574	0x40293838	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2575	0x4029383C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2576	0x40293840	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2577	0x40293844	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2578	0x40293848	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2579	0x4029384C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2580	0x40293850	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2581	0x40293854	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2582	0x40293858	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2583	0x4029385C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2584	0x40293860	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2585	0x40293864	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2586	0x40293868	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2587	0x4029386C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2588	0x40293870	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2589	0x40293874	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2590	0x40293878	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2591	0x4029387C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2592	0x40293880	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2593	0x40293884	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2594	0x40293888	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2595	0x4029388C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2596	0x40293890	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2597	0x40293894	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2598	0x40293898	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2599	0x4029389C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2600	0x402938A0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2601	0x402938A4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2602	0x402938A8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2603	0x402938AC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2604	0x402938B0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2605	0x402938B4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2606	0x402938B8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2607	0x402938BC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2608	0x402938C0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2609	0x402938C4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2610	0x402938C8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2611	0x402938CC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2612	0x402938D0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2613	0x402938D4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2614	0x402938D8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2615	0x402938DC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2616	0x402938E0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2617	0x402938E4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2618	0x402938E8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2619	0x402938EC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2620	0x402938F0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2621	0x402938F4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2622	0x402938F8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2623	0x402938FC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2624	0x40293900	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2625	0x40293904	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2626	0x40293908	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2627	0x4029390C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2628	0x40293910	FULL	Sensor Configuration Storage

Register Name	Address	Permission	Description
MSC_SENSOR_DATA2629	0x40293914	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2630	0x40293918	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2631	0x4029391C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2632	0x40293920	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2633	0x40293924	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2634	0x40293928	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2635	0x4029392C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2636	0x40293930	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2637	0x40293934	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2638	0x40293938	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2639	0x4029393C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2640	0x40293940	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2641	0x40293944	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2642	0x40293948	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2643	0x4029394C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2644	0x40293950	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2645	0x40293954	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2646	0x40293958	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2647	0x4029395C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2648	0x40293960	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2649	0x40293964	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2650	0x40293968	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2651	0x4029396C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2652	0x40293970	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2653	0x40293974	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2654	0x40293978	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2655	0x4029397C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2656	0x40293980	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2657	0x40293984	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2658	0x40293988	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2659	0x4029398C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2660	0x40293990	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2661	0x40293994	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2662	0x40293998	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2663	0x4029399C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2664	0x402939A0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2665	0x402939A4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2666	0x402939A8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2667	0x402939AC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2668	0x402939B0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2669	0x402939B4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2670	0x402939B8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2671	0x402939BC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2672	0x402939C0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2673	0x402939C4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2674	0x402939C8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2675	0x402939CC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2676	0x402939D0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2677	0x402939D4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2678	0x402939D8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2679	0x402939DC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2680	0x402939E0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2681	0x402939E4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2682	0x402939E8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2683	0x402939EC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2684	0x402939F0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2685	0x402939F4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2686	0x402939F8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2687	0x402939FC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2688	0x40293A00	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2689	0x40293A04	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2690	0x40293A08	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2691	0x40293A0C	FULL	Sensor Configuration Storage

Register Name	Address	Permission	Description
MSC_SENSOR_DATA2692	0x40293A10	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2693	0x40293A14	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2694	0x40293A18	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2695	0x40293A1C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2696	0x40293A20	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2697	0x40293A24	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2698	0x40293A28	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2699	0x40293A2C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2700	0x40293A30	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2701	0x40293A34	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2702	0x40293A38	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2703	0x40293A3C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2704	0x40293A40	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2705	0x40293A44	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2706	0x40293A48	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2707	0x40293A4C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2708	0x40293A50	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2709	0x40293A54	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2710	0x40293A58	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2711	0x40293A5C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2712	0x40293A60	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2713	0x40293A64	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2714	0x40293A68	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2715	0x40293A6C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2716	0x40293A70	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2717	0x40293A74	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2718	0x40293A78	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2719	0x40293A7C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2720	0x40293A80	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2721	0x40293A84	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2722	0x40293A88	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2723	0x40293A8C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2724	0x40293A90	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2725	0x40293A94	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2726	0x40293A98	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2727	0x40293A9C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2728	0x40293AA0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2729	0x40293AA4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2730	0x40293AA8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2731	0x40293AAC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2732	0x40293AB0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2733	0x40293AB4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2734	0x40293AB8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2735	0x40293ABC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2736	0x40293AC0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2737	0x40293AC4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2738	0x40293AC8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2739	0x40293ACC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2740	0x40293AD0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2741	0x40293AD4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2742	0x40293AD8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2743	0x40293ADC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2744	0x40293AE0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2745	0x40293AE4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2746	0x40293AE8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2747	0x40293AEC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2748	0x40293AF0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2749	0x40293AF4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2750	0x40293AF8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2751	0x40293AFC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2752	0x40293B00	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2753	0x40293B04	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2754	0x40293B08	FULL	Sensor Configuration Storage

Register Name	Address	Permission	Description
MSC_SENSOR_DATA2755	0x40293B0C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2756	0x40293B10	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2757	0x40293B14	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2758	0x40293B18	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2759	0x40293B1C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2760	0x40293B20	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2761	0x40293B24	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2762	0x40293B28	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2763	0x40293B2C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2764	0x40293B30	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2765	0x40293B34	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2766	0x40293B38	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2767	0x40293B3C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2768	0x40293B40	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2769	0x40293B44	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2770	0x40293B48	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2771	0x40293B4C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2772	0x40293B50	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2773	0x40293B54	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2774	0x40293B58	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2775	0x40293B5C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2776	0x40293B60	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2777	0x40293B64	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2778	0x40293B68	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2779	0x40293B6C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2780	0x40293B70	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2781	0x40293B74	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2782	0x40293B78	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2783	0x40293B7C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2784	0x40293B80	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2785	0x40293B84	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2786	0x40293B88	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2787	0x40293B8C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2788	0x40293B90	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2789	0x40293B94	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2790	0x40293B98	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2791	0x40293B9C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2792	0x40293BA0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2793	0x40293BA4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2794	0x40293BA8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2795	0x40293BAC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2796	0x40293BB0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2797	0x40293BB4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2798	0x40293BB8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2799	0x40293BBC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2800	0x40293BC0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2801	0x40293BC4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2802	0x40293BC8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2803	0x40293BCC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2804	0x40293BD0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2805	0x40293BD4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2806	0x40293BD8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2807	0x40293BDC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2808	0x40293BE0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2809	0x40293BE4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2810	0x40293BE8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2811	0x40293BEC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2812	0x40293BF0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2813	0x40293BF4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2814	0x40293BF8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2815	0x40293BFC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2816	0x40293C00	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2817	0x40293C04	FULL	Sensor Configuration Storage

Register Name	Address	Permission	Description
MSC_SENSOR_DATA2818	0x40293C08	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2819	0x40293C0C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2820	0x40293C10	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2821	0x40293C14	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2822	0x40293C18	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2823	0x40293C1C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2824	0x40293C20	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2825	0x40293C24	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2826	0x40293C28	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2827	0x40293C2C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2828	0x40293C30	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2829	0x40293C34	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2830	0x40293C38	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2831	0x40293C3C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2832	0x40293C40	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2833	0x40293C44	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2834	0x40293C48	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2835	0x40293C4C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2836	0x40293C50	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2837	0x40293C54	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2838	0x40293C58	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2839	0x40293C5C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2840	0x40293C60	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2841	0x40293C64	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2842	0x40293C68	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2843	0x40293C6C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2844	0x40293C70	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2845	0x40293C74	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2846	0x40293C78	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2847	0x40293C7C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2848	0x40293C80	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2849	0x40293C84	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2850	0x40293C88	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2851	0x40293C8C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2852	0x40293C90	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2853	0x40293C94	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2854	0x40293C98	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2855	0x40293C9C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2856	0x40293CA0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2857	0x40293CA4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2858	0x40293CA8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2859	0x40293CAC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2860	0x40293CB0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2861	0x40293CB4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2862	0x40293CB8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2863	0x40293CBC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2864	0x40293CC0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2865	0x40293CC4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2866	0x40293CC8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2867	0x40293CCC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2868	0x40293CD0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2869	0x40293CD4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2870	0x40293CD8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2871	0x40293CDC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2872	0x40293CE0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2873	0x40293CE4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2874	0x40293CE8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2875	0x40293CEC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2876	0x40293CF0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2877	0x40293CF4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2878	0x40293CF8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2879	0x40293CFC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2880	0x40293D00	FULL	Sensor Configuration Storage

Register Name	Address	Permission	Description
MSC_SENSOR_DATA2881	0x40293D04	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2882	0x40293D08	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2883	0x40293D0C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2884	0x40293D10	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2885	0x40293D14	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2886	0x40293D18	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2887	0x40293D1C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2888	0x40293D20	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2889	0x40293D24	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2890	0x40293D28	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2891	0x40293D2C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2892	0x40293D30	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2893	0x40293D34	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2894	0x40293D38	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2895	0x40293D3C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2896	0x40293D40	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2897	0x40293D44	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2898	0x40293D48	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2899	0x40293D4C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2900	0x40293D50	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2901	0x40293D54	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2902	0x40293D58	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2903	0x40293D5C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2904	0x40293D60	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2905	0x40293D64	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2906	0x40293D68	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2907	0x40293D6C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2908	0x40293D70	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2909	0x40293D74	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2910	0x40293D78	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2911	0x40293D7C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2912	0x40293D80	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2913	0x40293D84	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2914	0x40293D88	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2915	0x40293D8C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2916	0x40293D90	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2917	0x40293D94	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2918	0x40293D98	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2919	0x40293D9C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2920	0x40293DA0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2921	0x40293DA4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2922	0x40293DA8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2923	0x40293DAC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2924	0x40293DB0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2925	0x40293DB4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2926	0x40293DB8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2927	0x40293DBC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2928	0x40293DC0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2929	0x40293DC4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2930	0x40293DC8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2931	0x40293DCC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2932	0x40293DD0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2933	0x40293DD4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2934	0x40293DD8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2935	0x40293DDC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2936	0x40293DE0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2937	0x40293DE4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2938	0x40293DE8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2939	0x40293DEC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2940	0x40293DF0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2941	0x40293DF4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2942	0x40293DF8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2943	0x40293DFC	FULL	Sensor Configuration Storage

Register Name	Address	Permission	Description
MSC_SENSOR_DATA2944	0x40293E00	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2945	0x40293E04	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2946	0x40293E08	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2947	0x40293E0C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2948	0x40293E10	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2949	0x40293E14	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2950	0x40293E18	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2951	0x40293E1C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2952	0x40293E20	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2953	0x40293E24	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2954	0x40293E28	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2955	0x40293E2C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2956	0x40293E30	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2957	0x40293E34	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2958	0x40293E38	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2959	0x40293E3C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2960	0x40293E40	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2961	0x40293E44	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2962	0x40293E48	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2963	0x40293E4C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2964	0x40293E50	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2965	0x40293E54	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2966	0x40293E58	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2967	0x40293E5C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2968	0x40293E60	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2969	0x40293E64	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2970	0x40293E68	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2971	0x40293E6C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2972	0x40293E70	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2973	0x40293E74	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2974	0x40293E78	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2975	0x40293E7C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2976	0x40293E80	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2977	0x40293E84	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2978	0x40293E88	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2979	0x40293E8C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2980	0x40293E90	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2981	0x40293E94	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2982	0x40293E98	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2983	0x40293E9C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2984	0x40293EA0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2985	0x40293EA4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2986	0x40293EA8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2987	0x40293EAC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2988	0x40293EB0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2989	0x40293EB4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2990	0x40293EB8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2991	0x40293EBC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2992	0x40293EC0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2993	0x40293EC4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2994	0x40293EC8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2995	0x40293ECC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2996	0x40293ED0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2997	0x40293ED4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2998	0x40293ED8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA2999	0x40293EDC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3000	0x40293EE0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3001	0x40293EE4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3002	0x40293EE8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3003	0x40293EEC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3004	0x40293EF0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3005	0x40293EF4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3006	0x40293EF8	FULL	Sensor Configuration Storage

Register Name	Address	Permission	Description
MSC_SENSOR_DATA3007	0x40293EFC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3008	0x40293F00	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3009	0x40293F04	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3010	0x40293F08	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3011	0x40293F0C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3012	0x40293F10	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3013	0x40293F14	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3014	0x40293F18	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3015	0x40293F1C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3016	0x40293F20	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3017	0x40293F24	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3018	0x40293F28	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3019	0x40293F2C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3020	0x40293F30	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3021	0x40293F34	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3022	0x40293F38	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3023	0x40293F3C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3024	0x40293F40	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3025	0x40293F44	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3026	0x40293F48	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3027	0x40293F4C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3028	0x40293F50	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3029	0x40293F54	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3030	0x40293F58	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3031	0x40293F5C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3032	0x40293F60	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3033	0x40293F64	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3034	0x40293F68	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3035	0x40293F6C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3036	0x40293F70	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3037	0x40293F74	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3038	0x40293F78	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3039	0x40293F7C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3040	0x40293F80	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3041	0x40293F84	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3042	0x40293F88	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3043	0x40293F8C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3044	0x40293F90	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3045	0x40293F94	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3046	0x40293F98	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3047	0x40293F9C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3048	0x40293FA0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3049	0x40293FA4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3050	0x40293FA8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3051	0x40293FAC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3052	0x40293FB0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3053	0x40293FB4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3054	0x40293FB8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3055	0x40293FBC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3056	0x40293FC0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3057	0x40293FC4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3058	0x40293FC8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3059	0x40293FCC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3060	0x40293FD0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3061	0x40293FD4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3062	0x40293FD8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3063	0x40293FDC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3064	0x40293FE0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3065	0x40293FE4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3066	0x40293FE8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3067	0x40293FEC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3068	0x40293FF0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3069	0x40293FF4	FULL	Sensor Configuration Storage

Register Name	Address	Permission	Description
MSC_SENSOR_DATA3070	0x40293FF8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3071	0x40293FFC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3072	0x40294000	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3073	0x40294004	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3074	0x40294008	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3075	0x4029400C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3076	0x40294010	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3077	0x40294014	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3078	0x40294018	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3079	0x4029401C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3080	0x40294020	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3081	0x40294024	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3082	0x40294028	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3083	0x4029402C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3084	0x40294030	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3085	0x40294034	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3086	0x40294038	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3087	0x4029403C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3088	0x40294040	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3089	0x40294044	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3090	0x40294048	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3091	0x4029404C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3092	0x40294050	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3093	0x40294054	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3094	0x40294058	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3095	0x4029405C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3096	0x40294060	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3097	0x40294064	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3098	0x40294068	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3099	0x4029406C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3100	0x40294070	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3101	0x40294074	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3102	0x40294078	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3103	0x4029407C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3104	0x40294080	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3105	0x40294084	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3106	0x40294088	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3107	0x4029408C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3108	0x40294090	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3109	0x40294094	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3110	0x40294098	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3111	0x4029409C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3112	0x402940A0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3113	0x402940A4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3114	0x402940A8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3115	0x402940AC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3116	0x402940B0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3117	0x402940B4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3118	0x402940B8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3119	0x402940BC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3120	0x402940C0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3121	0x402940C4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3122	0x402940C8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3123	0x402940CC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3124	0x402940D0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3125	0x402940D4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3126	0x402940D8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3127	0x402940DC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3128	0x402940E0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3129	0x402940E4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3130	0x402940E8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3131	0x402940EC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3132	0x402940F0	FULL	Sensor Configuration Storage

Register Name	Address	Permission	Description
MSC_SENSOR_DATA3133	0x402940F4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3134	0x402940F8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3135	0x402940FC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3136	0x40294100	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3137	0x40294104	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3138	0x40294108	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3139	0x4029410C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3140	0x40294110	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3141	0x40294114	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3142	0x40294118	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3143	0x4029411C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3144	0x40294120	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3145	0x40294124	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3146	0x40294128	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3147	0x4029412C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3148	0x40294130	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3149	0x40294134	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3150	0x40294138	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3151	0x4029413C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3152	0x40294140	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3153	0x40294144	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3154	0x40294148	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3155	0x4029414C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3156	0x40294150	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3157	0x40294154	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3158	0x40294158	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3159	0x4029415C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3160	0x40294160	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3161	0x40294164	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3162	0x40294168	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3163	0x4029416C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3164	0x40294170	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3165	0x40294174	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3166	0x40294178	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3167	0x4029417C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3168	0x40294180	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3169	0x40294184	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3170	0x40294188	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3171	0x4029418C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3172	0x40294190	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3173	0x40294194	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3174	0x40294198	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3175	0x4029419C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3176	0x402941A0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3177	0x402941A4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3178	0x402941A8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3179	0x402941AC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3180	0x402941B0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3181	0x402941B4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3182	0x402941B8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3183	0x402941BC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3184	0x402941C0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3185	0x402941C4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3186	0x402941C8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3187	0x402941CC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3188	0x402941D0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3189	0x402941D4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3190	0x402941D8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3191	0x402941DC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3192	0x402941E0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3193	0x402941E4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3194	0x402941E8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3195	0x402941EC	FULL	Sensor Configuration Storage

Register Name	Address	Permission	Description
MSC_SENSOR_DATA3196	0x402941F0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3197	0x402941F4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3198	0x402941F8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3199	0x402941FC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3200	0x40294200	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3201	0x40294204	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3202	0x40294208	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3203	0x4029420C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3204	0x40294210	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3205	0x40294214	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3206	0x40294218	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3207	0x4029421C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3208	0x40294220	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3209	0x40294224	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3210	0x40294228	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3211	0x4029422C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3212	0x40294230	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3213	0x40294234	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3214	0x40294238	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3215	0x4029423C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3216	0x40294240	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3217	0x40294244	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3218	0x40294248	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3219	0x4029424C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3220	0x40294250	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3221	0x40294254	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3222	0x40294258	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3223	0x4029425C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3224	0x40294260	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3225	0x40294264	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3226	0x40294268	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3227	0x4029426C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3228	0x40294270	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3229	0x40294274	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3230	0x40294278	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3231	0x4029427C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3232	0x40294280	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3233	0x40294284	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3234	0x40294288	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3235	0x4029428C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3236	0x40294290	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3237	0x40294294	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3238	0x40294298	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3239	0x4029429C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3240	0x402942A0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3241	0x402942A4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3242	0x402942A8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3243	0x402942AC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3244	0x402942B0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3245	0x402942B4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3246	0x402942B8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3247	0x402942BC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3248	0x402942C0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3249	0x402942C4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3250	0x402942C8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3251	0x402942CC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3252	0x402942D0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3253	0x402942D4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3254	0x402942D8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3255	0x402942DC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3256	0x402942E0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3257	0x402942E4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3258	0x402942E8	FULL	Sensor Configuration Storage

Register Name	Address	Permission	Description
MSC_SENSOR_DATA3259	0x402942EC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3260	0x402942F0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3261	0x402942F4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3262	0x402942F8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3263	0x402942FC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3264	0x40294300	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3265	0x40294304	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3266	0x40294308	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3267	0x4029430C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3268	0x40294310	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3269	0x40294314	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3270	0x40294318	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3271	0x4029431C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3272	0x40294320	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3273	0x40294324	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3274	0x40294328	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3275	0x4029432C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3276	0x40294330	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3277	0x40294334	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3278	0x40294338	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3279	0x4029433C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3280	0x40294340	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3281	0x40294344	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3282	0x40294348	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3283	0x4029434C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3284	0x40294350	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3285	0x40294354	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3286	0x40294358	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3287	0x4029435C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3288	0x40294360	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3289	0x40294364	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3290	0x40294368	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3291	0x4029436C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3292	0x40294370	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3293	0x40294374	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3294	0x40294378	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3295	0x4029437C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3296	0x40294380	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3297	0x40294384	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3298	0x40294388	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3299	0x4029438C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3300	0x40294390	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3301	0x40294394	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3302	0x40294398	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3303	0x4029439C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3304	0x402943A0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3305	0x402943A4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3306	0x402943A8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3307	0x402943AC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3308	0x402943B0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3309	0x402943B4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3310	0x402943B8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3311	0x402943BC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3312	0x402943C0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3313	0x402943C4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3314	0x402943C8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3315	0x402943CC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3316	0x402943D0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3317	0x402943D4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3318	0x402943D8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3319	0x402943DC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3320	0x402943E0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3321	0x402943E4	FULL	Sensor Configuration Storage

Register Name	Address	Permission	Description
MSC_SENSOR_DATA3322	0x402943E8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3323	0x402943EC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3324	0x402943F0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3325	0x402943F4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3326	0x402943F8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3327	0x402943FC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3328	0x40294400	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3329	0x40294404	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3330	0x40294408	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3331	0x4029440C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3332	0x40294410	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3333	0x40294414	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3334	0x40294418	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3335	0x4029441C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3336	0x40294420	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3337	0x40294424	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3338	0x40294428	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3339	0x4029442C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3340	0x40294430	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3341	0x40294434	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3342	0x40294438	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3343	0x4029443C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3344	0x40294440	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3345	0x40294444	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3346	0x40294448	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3347	0x4029444C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3348	0x40294450	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3349	0x40294454	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3350	0x40294458	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3351	0x4029445C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3352	0x40294460	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3353	0x40294464	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3354	0x40294468	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3355	0x4029446C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3356	0x40294470	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3357	0x40294474	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3358	0x40294478	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3359	0x4029447C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3360	0x40294480	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3361	0x40294484	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3362	0x40294488	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3363	0x4029448C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3364	0x40294490	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3365	0x40294494	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3366	0x40294498	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3367	0x4029449C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3368	0x402944A0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3369	0x402944A4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3370	0x402944A8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3371	0x402944AC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3372	0x402944B0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3373	0x402944B4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3374	0x402944B8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3375	0x402944BC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3376	0x402944C0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3377	0x402944C4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3378	0x402944C8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3379	0x402944CC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3380	0x402944D0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3381	0x402944D4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3382	0x402944D8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3383	0x402944DC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3384	0x402944E0	FULL	Sensor Configuration Storage

Register Name	Address	Permission	Description
MSC_SENSOR_DATA3385	0x402944E4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3386	0x402944E8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3387	0x402944EC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3388	0x402944F0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3389	0x402944F4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3390	0x402944F8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3391	0x402944FC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3392	0x40294500	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3393	0x40294504	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3394	0x40294508	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3395	0x4029450C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3396	0x40294510	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3397	0x40294514	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3398	0x40294518	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3399	0x4029451C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3400	0x40294520	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3401	0x40294524	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3402	0x40294528	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3403	0x4029452C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3404	0x40294530	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3405	0x40294534	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3406	0x40294538	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3407	0x4029453C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3408	0x40294540	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3409	0x40294544	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3410	0x40294548	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3411	0x4029454C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3412	0x40294550	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3413	0x40294554	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3414	0x40294558	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3415	0x4029455C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3416	0x40294560	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3417	0x40294564	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3418	0x40294568	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3419	0x4029456C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3420	0x40294570	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3421	0x40294574	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3422	0x40294578	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3423	0x4029457C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3424	0x40294580	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3425	0x40294584	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3426	0x40294588	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3427	0x4029458C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3428	0x40294590	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3429	0x40294594	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3430	0x40294598	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3431	0x4029459C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3432	0x402945A0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3433	0x402945A4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3434	0x402945A8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3435	0x402945AC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3436	0x402945B0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3437	0x402945B4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3438	0x402945B8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3439	0x402945BC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3440	0x402945C0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3441	0x402945C4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3442	0x402945C8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3443	0x402945CC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3444	0x402945D0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3445	0x402945D4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3446	0x402945D8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3447	0x402945DC	FULL	Sensor Configuration Storage

Register Name	Address	Permission	Description
MSC_SENSOR_DATA3448	0x402945E0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3449	0x402945E4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3450	0x402945E8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3451	0x402945EC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3452	0x402945F0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3453	0x402945F4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3454	0x402945F8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3455	0x402945FC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3456	0x40294600	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3457	0x40294604	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3458	0x40294608	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3459	0x4029460C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3460	0x40294610	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3461	0x40294614	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3462	0x40294618	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3463	0x4029461C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3464	0x40294620	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3465	0x40294624	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3466	0x40294628	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3467	0x4029462C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3468	0x40294630	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3469	0x40294634	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3470	0x40294638	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3471	0x4029463C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3472	0x40294640	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3473	0x40294644	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3474	0x40294648	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3475	0x4029464C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3476	0x40294650	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3477	0x40294654	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3478	0x40294658	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3479	0x4029465C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3480	0x40294660	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3481	0x40294664	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3482	0x40294668	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3483	0x4029466C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3484	0x40294670	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3485	0x40294674	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3486	0x40294678	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3487	0x4029467C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3488	0x40294680	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3489	0x40294684	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3490	0x40294688	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3491	0x4029468C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3492	0x40294690	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3493	0x40294694	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3494	0x40294698	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3495	0x4029469C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3496	0x402946A0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3497	0x402946A4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3498	0x402946A8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3499	0x402946AC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3500	0x402946B0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3501	0x402946B4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3502	0x402946B8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3503	0x402946BC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3504	0x402946C0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3505	0x402946C4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3506	0x402946C8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3507	0x402946CC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3508	0x402946D0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3509	0x402946D4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3510	0x402946D8	FULL	Sensor Configuration Storage

Register Name	Address	Permission	Description
MSC_SENSOR_DATA3511	0x402946DC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3512	0x402946E0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3513	0x402946E4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3514	0x402946E8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3515	0x402946EC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3516	0x402946F0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3517	0x402946F4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3518	0x402946F8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3519	0x402946FC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3520	0x40294700	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3521	0x40294704	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3522	0x40294708	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3523	0x4029470C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3524	0x40294710	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3525	0x40294714	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3526	0x40294718	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3527	0x4029471C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3528	0x40294720	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3529	0x40294724	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3530	0x40294728	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3531	0x4029472C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3532	0x40294730	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3533	0x40294734	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3534	0x40294738	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3535	0x4029473C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3536	0x40294740	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3537	0x40294744	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3538	0x40294748	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3539	0x4029474C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3540	0x40294750	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3541	0x40294754	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3542	0x40294758	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3543	0x4029475C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3544	0x40294760	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3545	0x40294764	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3546	0x40294768	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3547	0x4029476C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3548	0x40294770	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3549	0x40294774	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3550	0x40294778	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3551	0x4029477C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3552	0x40294780	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3553	0x40294784	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3554	0x40294788	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3555	0x4029478C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3556	0x40294790	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3557	0x40294794	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3558	0x40294798	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3559	0x4029479C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3560	0x402947A0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3561	0x402947A4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3562	0x402947A8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3563	0x402947AC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3564	0x402947B0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3565	0x402947B4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3566	0x402947B8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3567	0x402947BC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3568	0x402947C0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3569	0x402947C4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3570	0x402947C8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3571	0x402947CC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3572	0x402947D0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3573	0x402947D4	FULL	Sensor Configuration Storage

Register Name	Address	Permission	Description
MSC_SENSOR_DATA3574	0x402947D8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3575	0x402947DC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3576	0x402947E0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3577	0x402947E4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3578	0x402947E8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3579	0x402947EC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3580	0x402947F0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3581	0x402947F4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3582	0x402947F8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3583	0x402947FC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3584	0x40294800	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3585	0x40294804	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3586	0x40294808	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3587	0x4029480C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3588	0x40294810	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3589	0x40294814	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3590	0x40294818	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3591	0x4029481C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3592	0x40294820	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3593	0x40294824	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3594	0x40294828	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3595	0x4029482C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3596	0x40294830	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3597	0x40294834	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3598	0x40294838	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3599	0x4029483C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3600	0x40294840	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3601	0x40294844	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3602	0x40294848	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3603	0x4029484C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3604	0x40294850	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3605	0x40294854	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3606	0x40294858	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3607	0x4029485C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3608	0x40294860	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3609	0x40294864	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3610	0x40294868	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3611	0x4029486C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3612	0x40294870	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3613	0x40294874	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3614	0x40294878	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3615	0x4029487C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3616	0x40294880	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3617	0x40294884	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3618	0x40294888	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3619	0x4029488C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3620	0x40294890	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3621	0x40294894	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3622	0x40294898	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3623	0x4029489C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3624	0x402948A0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3625	0x402948A4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3626	0x402948A8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3627	0x402948AC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3628	0x402948B0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3629	0x402948B4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3630	0x402948B8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3631	0x402948BC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3632	0x402948C0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3633	0x402948C4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3634	0x402948C8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3635	0x402948CC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3636	0x402948D0	FULL	Sensor Configuration Storage

Register Name	Address	Permission	Description
MSC_SENSOR_DATA3637	0x402948D4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3638	0x402948D8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3639	0x402948DC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3640	0x402948E0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3641	0x402948E4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3642	0x402948E8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3643	0x402948EC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3644	0x402948F0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3645	0x402948F4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3646	0x402948F8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3647	0x402948FC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3648	0x40294900	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3649	0x40294904	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3650	0x40294908	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3651	0x4029490C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3652	0x40294910	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3653	0x40294914	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3654	0x40294918	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3655	0x4029491C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3656	0x40294920	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3657	0x40294924	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3658	0x40294928	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3659	0x4029492C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3660	0x40294930	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3661	0x40294934	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3662	0x40294938	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3663	0x4029493C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3664	0x40294940	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3665	0x40294944	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3666	0x40294948	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3667	0x4029494C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3668	0x40294950	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3669	0x40294954	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3670	0x40294958	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3671	0x4029495C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3672	0x40294960	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3673	0x40294964	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3674	0x40294968	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3675	0x4029496C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3676	0x40294970	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3677	0x40294974	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3678	0x40294978	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3679	0x4029497C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3680	0x40294980	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3681	0x40294984	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3682	0x40294988	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3683	0x4029498C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3684	0x40294990	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3685	0x40294994	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3686	0x40294998	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3687	0x4029499C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3688	0x402949A0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3689	0x402949A4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3690	0x402949A8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3691	0x402949AC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3692	0x402949B0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3693	0x402949B4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3694	0x402949B8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3695	0x402949BC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3696	0x402949C0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3697	0x402949C4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3698	0x402949C8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3699	0x402949CC	FULL	Sensor Configuration Storage

Register Name	Address	Permission	Description
MSC_SENSOR_DATA3700	0x402949D0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3701	0x402949D4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3702	0x402949D8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3703	0x402949DC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3704	0x402949E0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3705	0x402949E4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3706	0x402949E8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3707	0x402949EC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3708	0x402949F0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3709	0x402949F4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3710	0x402949F8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3711	0x402949FC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3712	0x40294A00	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3713	0x40294A04	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3714	0x40294A08	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3715	0x40294A0C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3716	0x40294A10	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3717	0x40294A14	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3718	0x40294A18	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3719	0x40294A1C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3720	0x40294A20	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3721	0x40294A24	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3722	0x40294A28	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3723	0x40294A2C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3724	0x40294A30	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3725	0x40294A34	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3726	0x40294A38	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3727	0x40294A3C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3728	0x40294A40	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3729	0x40294A44	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3730	0x40294A48	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3731	0x40294A4C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3732	0x40294A50	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3733	0x40294A54	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3734	0x40294A58	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3735	0x40294A5C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3736	0x40294A60	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3737	0x40294A64	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3738	0x40294A68	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3739	0x40294A6C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3740	0x40294A70	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3741	0x40294A74	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3742	0x40294A78	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3743	0x40294A7C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3744	0x40294A80	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3745	0x40294A84	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3746	0x40294A88	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3747	0x40294A8C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3748	0x40294A90	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3749	0x40294A94	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3750	0x40294A98	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3751	0x40294A9C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3752	0x40294AA0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3753	0x40294AA4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3754	0x40294AA8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3755	0x40294AAC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3756	0x40294AB0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3757	0x40294AB4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3758	0x40294AB8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3759	0x40294ABC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3760	0x40294AC0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3761	0x40294AC4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3762	0x40294AC8	FULL	Sensor Configuration Storage

Register Name	Address	Permission	Description
MSC_SENSOR_DATA3763	0x40294ACC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3764	0x40294AD0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3765	0x40294AD4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3766	0x40294AD8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3767	0x40294ADC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3768	0x40294AE0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3769	0x40294AE4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3770	0x40294AE8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3771	0x40294AEC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3772	0x40294AF0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3773	0x40294AF4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3774	0x40294AF8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3775	0x40294AFC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3776	0x40294B00	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3777	0x40294B04	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3778	0x40294B08	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3779	0x40294B0C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3780	0x40294B10	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3781	0x40294B14	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3782	0x40294B18	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3783	0x40294B1C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3784	0x40294B20	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3785	0x40294B24	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3786	0x40294B28	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3787	0x40294B2C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3788	0x40294B30	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3789	0x40294B34	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3790	0x40294B38	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3791	0x40294B3C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3792	0x40294B40	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3793	0x40294B44	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3794	0x40294B48	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3795	0x40294B4C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3796	0x40294B50	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3797	0x40294B54	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3798	0x40294B58	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3799	0x40294B5C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3800	0x40294B60	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3801	0x40294B64	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3802	0x40294B68	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3803	0x40294B6C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3804	0x40294B70	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3805	0x40294B74	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3806	0x40294B78	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3807	0x40294B7C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3808	0x40294B80	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3809	0x40294B84	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3810	0x40294B88	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3811	0x40294B8C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3812	0x40294B90	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3813	0x40294B94	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3814	0x40294B98	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3815	0x40294B9C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3816	0x40294BA0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3817	0x40294BA4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3818	0x40294BA8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3819	0x40294BAC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3820	0x40294BB0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3821	0x40294BB4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3822	0x40294BB8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3823	0x40294BBC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3824	0x40294BC0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3825	0x40294BC4	FULL	Sensor Configuration Storage

Register Name	Address	Permission	Description
MSC_SENSOR_DATA3826	0x40294BC8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3827	0x40294BCC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3828	0x40294BD0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3829	0x40294BD4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3830	0x40294BD8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3831	0x40294BDC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3832	0x40294BE0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3833	0x40294BE4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3834	0x40294BE8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3835	0x40294BEC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3836	0x40294BF0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3837	0x40294BF4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3838	0x40294BF8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3839	0x40294BFC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3840	0x40294C00	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3841	0x40294C04	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3842	0x40294C08	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3843	0x40294C0C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3844	0x40294C10	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3845	0x40294C14	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3846	0x40294C18	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3847	0x40294C1C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3848	0x40294C20	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3849	0x40294C24	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3850	0x40294C28	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3851	0x40294C2C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3852	0x40294C30	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3853	0x40294C34	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3854	0x40294C38	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3855	0x40294C3C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3856	0x40294C40	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3857	0x40294C44	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3858	0x40294C48	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3859	0x40294C4C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3860	0x40294C50	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3861	0x40294C54	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3862	0x40294C58	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3863	0x40294C5C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3864	0x40294C60	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3865	0x40294C64	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3866	0x40294C68	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3867	0x40294C6C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3868	0x40294C70	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3869	0x40294C74	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3870	0x40294C78	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3871	0x40294C7C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3872	0x40294C80	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3873	0x40294C84	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3874	0x40294C88	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3875	0x40294C8C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3876	0x40294C90	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3877	0x40294C94	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3878	0x40294C98	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3879	0x40294C9C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3880	0x40294CA0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3881	0x40294CA4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3882	0x40294CA8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3883	0x40294CAC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3884	0x40294CB0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3885	0x40294CB4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3886	0x40294CB8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3887	0x40294CBC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3888	0x40294CC0	FULL	Sensor Configuration Storage

Register Name	Address	Permission	Description
MSC_SENSOR_DATA3889	0x40294CC4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3890	0x40294CC8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3891	0x40294CCC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3892	0x40294CD0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3893	0x40294CD4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3894	0x40294CD8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3895	0x40294CDC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3896	0x40294CE0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3897	0x40294CE4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3898	0x40294CE8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3899	0x40294CEC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3900	0x40294CF0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3901	0x40294CF4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3902	0x40294CF8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3903	0x40294CFC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3904	0x40294D00	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3905	0x40294D04	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3906	0x40294D08	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3907	0x40294D0C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3908	0x40294D10	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3909	0x40294D14	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3910	0x40294D18	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3911	0x40294D1C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3912	0x40294D20	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3913	0x40294D24	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3914	0x40294D28	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3915	0x40294D2C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3916	0x40294D30	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3917	0x40294D34	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3918	0x40294D38	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3919	0x40294D3C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3920	0x40294D40	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3921	0x40294D44	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3922	0x40294D48	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3923	0x40294D4C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3924	0x40294D50	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3925	0x40294D54	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3926	0x40294D58	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3927	0x40294D5C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3928	0x40294D60	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3929	0x40294D64	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3930	0x40294D68	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3931	0x40294D6C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3932	0x40294D70	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3933	0x40294D74	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3934	0x40294D78	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3935	0x40294D7C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3936	0x40294D80	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3937	0x40294D84	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3938	0x40294D88	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3939	0x40294D8C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3940	0x40294D90	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3941	0x40294D94	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3942	0x40294D98	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3943	0x40294D9C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3944	0x40294DA0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3945	0x40294DA4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3946	0x40294DA8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3947	0x40294DAC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3948	0x40294DB0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3949	0x40294DB4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3950	0x40294DB8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3951	0x40294DBC	FULL	Sensor Configuration Storage

Register Name	Address	Permission	Description
MSC_SENSOR_DATA3952	0x40294DC0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3953	0x40294DC4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3954	0x40294DC8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3955	0x40294DCC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3956	0x40294DD0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3957	0x40294DD4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3958	0x40294DD8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3959	0x40294DDC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3960	0x40294DE0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3961	0x40294DE4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3962	0x40294DE8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3963	0x40294DEC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3964	0x40294DF0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3965	0x40294DF4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3966	0x40294DF8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3967	0x40294DFC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3968	0x40294E00	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3969	0x40294E04	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3970	0x40294E08	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3971	0x40294E0C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3972	0x40294E10	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3973	0x40294E14	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3974	0x40294E18	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3975	0x40294E1C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3976	0x40294E20	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3977	0x40294E24	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3978	0x40294E28	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3979	0x40294E2C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3980	0x40294E30	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3981	0x40294E34	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3982	0x40294E38	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3983	0x40294E3C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3984	0x40294E40	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3985	0x40294E44	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3986	0x40294E48	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3987	0x40294E4C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3988	0x40294E50	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3989	0x40294E54	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3990	0x40294E58	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3991	0x40294E5C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3992	0x40294E60	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3993	0x40294E64	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3994	0x40294E68	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3995	0x40294E6C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3996	0x40294E70	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3997	0x40294E74	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3998	0x40294E78	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA3999	0x40294E7C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA4000	0x40294E80	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA4001	0x40294E84	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA4002	0x40294E88	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA4003	0x40294E8C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA4004	0x40294E90	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA4005	0x40294E94	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA4006	0x40294E98	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA4007	0x40294E9C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA4008	0x40294EA0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA4009	0x40294EA4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA4010	0x40294EA8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA4011	0x40294EAC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA4012	0x40294EB0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA4013	0x40294EB4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA4014	0x40294EB8	FULL	Sensor Configuration Storage

Register Name	Address	Permission	Description
MSC_SENSOR_DATA4015	0x40294EBC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA4016	0x40294EC0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA4017	0x40294EC4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA4018	0x40294EC8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA4019	0x40294ECC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA4020	0x40294ED0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA4021	0x40294ED4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA4022	0x40294ED8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA4023	0x40294EDC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA4024	0x40294EE0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA4025	0x40294EE4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA4026	0x40294EE8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA4027	0x40294EEC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA4028	0x40294EF0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA4029	0x40294EF4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA4030	0x40294EF8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA4031	0x40294EFC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA4032	0x40294F00	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA4033	0x40294F04	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA4034	0x40294F08	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA4035	0x40294F0C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA4036	0x40294F10	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA4037	0x40294F14	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA4038	0x40294F18	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA4039	0x40294F1C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA4040	0x40294F20	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA4041	0x40294F24	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA4042	0x40294F28	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA4043	0x40294F2C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA4044	0x40294F30	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA4045	0x40294F34	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA4046	0x40294F38	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA4047	0x40294F3C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA4048	0x40294F40	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA4049	0x40294F44	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA4050	0x40294F48	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA4051	0x40294F4C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA4052	0x40294F50	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA4053	0x40294F54	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA4054	0x40294F58	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA4055	0x40294F5C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA4056	0x40294F60	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA4057	0x40294F64	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA4058	0x40294F68	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA4059	0x40294F6C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA4060	0x40294F70	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA4061	0x40294F74	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA4062	0x40294F78	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA4063	0x40294F7C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA4064	0x40294F80	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA4065	0x40294F84	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA4066	0x40294F88	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA4067	0x40294F8C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA4068	0x40294F90	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA4069	0x40294F94	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA4070	0x40294F98	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA4071	0x40294F9C	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA4072	0x40294FA0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA4073	0x40294FA4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA4074	0x40294FA8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA4075	0x40294FAC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA4076	0x40294FB0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA4077	0x40294FB4	FULL	Sensor Configuration Storage

Register Name	Address	Permission	Description
MSC_SENSOR_DATA4078	0x40294FB8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA4079	0x40294FBC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA4080	0x40294FC0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA4081	0x40294FC4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA4082	0x40294FC8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA4083	0x40294FCC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA4084	0x40294FD0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA4085	0x40294FD4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA4086	0x40294FD8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA4087	0x40294FDC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA4088	0x40294FE0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA4089	0x40294FE4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA4090	0x40294FE8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA4091	0x40294FEC	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA4092	0x40294FF0	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA4093	0x40294FF4	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA4094	0x40294FF8	FULL	Sensor Configuration Storage
MSC_SENSOR_DATA4095	0x40294FFC	FULL	Sensor Configuration Storage
MSC_TRIM_CTL	0x4029FF00	FULL	Trim Control

11.1 MODE 0

Register Name	Address	Permission	Description
MSC_MODE0_SENSE_DUTY_CTL	0x40290500	FULL	Sense Clock Duty Cycle Control
MSC_MODE0_SW_SEL_CDAC_FL	0x40290504	FULL	Flatspot/Dither CAPDAC Switch Control
MSC_MODE0_SW_SEL_TOP	0x40290508	FULL	Top Level Switch Control
MSC_MODE0_SW_SEL_COMP	0x4029050C	FULL	MSC Comparator Switch Control
MSC_MODE0_SW_SEL_SH	0x40290510	FULL	Shielding Switch Control

11.2 MODE 1

Register Name	Address	Permission	Description
MSC_MODE1_SENSE_DUTY_CTL	0x40290520	FULL	Sense Clock Duty Cycle Control
MSC_MODE1_SW_SEL_CDAC_FL	0x40290524	FULL	Flatspot/Dither CAPDAC Switch Control
MSC_MODE1_SW_SEL_TOP	0x40290528	FULL	Top Level Switch Control
MSC_MODE1_SW_SEL_COMP	0x4029052C	FULL	MSC Comparator Switch Control
MSC_MODE1_SW_SEL_SH	0x40290530	FULL	Shielding Switch Control

11.3 MODE 2

Register Name	Address	Permission	Description
MSC_MODE2_SENSE_DUTY_CTL	0x40290540	FULL	Sense Clock Duty Cycle Control
MSC_MODE2_SW_SEL_CDAC_FL	0x40290544	FULL	Flatspot/Dither CAPDAC Switch Control
MSC_MODE2_SW_SEL_TOP	0x40290548	FULL	Top Level Switch Control
MSC_MODE2_SW_SEL_COMP	0x4029054C	FULL	MSC Comparator Switch Control
MSC_MODE2_SW_SEL_SH	0x40290550	FULL	Shielding Switch Control

11.4 Register Details

11.4.1 MSC_CTL

Description: Configuration and Control
Address: 0x40290000
Offset: 0x0
Retention: Retained
IsDeepSleep: No
Comment: This register is used to configure and control the MSCv3 block.
Default: 0x100000

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:5]			MSCCMP_EN [4:4]	None [3:1]			SENSE_EN [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:13]			EXT_FRAME_START_EN [12:12]	None [11:9]			CLK_SYNC_EN [8:8]

Bits	23	22	21	20	19	18	17	16
Name	None [23:21]			BUF_MODE [20:20]	None [19:18]		OPERATING_MODE [17:16]	

Bits	31	30	29	28	27	26	25	24
Name	ENABLED [31:31]	None [30:25]						CLK_MSC_RATIO [24:24]

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	SENSE_EN	RW	R	0	Enables the sense modulator output. '0': All switches, static or dynamic, are open. '1': Switches can be closed/open as per MMIO setting and Sequencer FSM.
	DISABLED			0	N/A
	ENABLED			1	N/A
4	MSCCMP_EN	RW	R	0	MSC Comparator Enable.
	DISABLED			0	N/A
	ENABLED			1	N/A
8	CLK_SYNC_EN	RW	R	0	Control bit to create external channel sync clock. '0': msc_ext_sync_clk_out (and _out_en) tied 0. '1': Generate msc_ext_sync_clk_out using clock_sync_pos_en and set msc_ext_sync_clk_out_en = 1.
	DISABLED			0	N/A
	ENABLED			1	N/A
12	EXT_FRAME_START_EN	RW	R	0	Control bit to enable external frame start of Sequencer FSM via GPIO. '0': FSM is only sensitive to START_FRAME bit. '1': FSM sensitive to external frame start (and not sensitive to START_FRAME). This external start can be a new or pending external frame start event or an indication from the LP-AoC FSM.
	DISABLED			0	N/A
	ENABLED			1	N/A

Bits	Name	SW	HW	Default or Enum	Description
16:17	OPERATING_MODE	RW	R	0	Sequencer FSM Operating Mode '0': CPU Mode. '1': Chained-Scan DMA Mode. '2': Autonomous Scan Multi Sensor Mode. '3': Low Power Always-On-Capsense Mode.
	CPU			0	Frame scan configurations are stored in system RAM. Start of frame initiated by CPU via AHB. After each scan in frame, the end of scan interrupt is raised. The CPU extracts results and programs and starts the next scan. End of frame interrupt is produced so CPU can extract and process data.
	CS_DMA			1	Frame scan configurations are stored in system RAM. CPU writes into DMA registers to start a DMA transfer. i.e. CPU/firmware initiates a DMA transfer to write first scan configuration. The rest of the scans in the frame are chained via trigger to DMA. End of frame interrupt is produced so CPU can extract and process data.
	AS_MS			2	Frame scan configurations are stored in IP RAM. Start of frame initiated by CPU via AHB. The rest of the scans are chained autonomously by Sequencer FSM. End of frame interrupt is produced so CPU can extract and process data.
	LP_AOC			3	Frame scan configurations are stored in IP RAM. Start of frame initiated by LP-AOC timer expire. Rest of the scans are chained autonomously by Sequencer FSM. No end of frame interrupt, no data processing by CPU. Wake up interrupt fired upon valid signal detection (LP-AOC FSM).
20	BUF_MODE	RW	R	1	Shield buffer operating mode select. '0': High bandwidth mode. '1': Shield mode.
	HIGH_BW_MODE			0	N/A
	SHIELD_MODE			1	N/A
24	CLK_MSC_RATIO	RW	R	0	Control bit for logic that creates clk_msc from clk_hf. '0': Divided. clk_hf :: clk_msc is at least 2:1 divide ratio. Ratio controlled by clock_msc_pos_en and clock_msc_neg_en provided by PERI. '1': Pass-through. clk_hf :: clk_msc is 1:1.
	DIVIDED			0	N/A
	PASSTHROUGH			1	N/A
31	ENABLED	RW	R	0	Master enable of the MSCv3 IP. Must be set to '1' for any operation to function. When '0' all analog components are off and all switches are open.
	DISABLED			0	N/A
	ENABLED			1	N/A

11.4.2 MSC_SPARE

Description: Spare MMIO
Address: 0x40290004
Offset: 0x4
Retention: Retained
IsDeepSleep: No
Comment: For risk mitigation.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:6]		SPARE [5:0]					

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:5	SPARE	RW	RW	0	Spare MMIO (Hard IP).

11.4.3 MSC_SCAN_CTL1

Description: Scan Control 1
Address: 0x40290008
Offset: 0x8
Retention: Retained
IsDeepSleep: No
Comment: This register is used to configure the per-scan settings.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:6]		NUM_SAMPLES [5:4]		RESCAN_DEBUG_MODE [3:3]	NUM_AUTO_RESAMPLE [2:0]		

Bits	15	14	13	12	11	10	9	8
Name	None [15:15]	DEBUG_CONV_PH_SEL [14:12]			None [11:9]			RAW_COUNT_MODE [8:8]

Bits	23	22	21	20	19	18	17	16
Name	FRAME_START_PTR [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:2	NUM_AUTO_RESAMPLE	RW	R	0	If Sequencer detects a bad conversion and NUM_AUTO_RESAMPLE != 0, it will not store the bad result. Instead, it will automatically re-sample using current configuration without firmware intervention. This process repeats until a good conversion is produced or until the programmed maximum. If bad samples are produces for each programmed re-sample attempt, the final bad sample is stored.
3	RESCAN_DEBUG_MODE	RW	R	0	If this bit is set all results (good and bad) generated by NUM_AUTO_RESAMPLE are stored. Debug feature. Firmware Rule: Usable setting for NUM_AUTO_RESAMPLE is limited depending on the size of the result FIFO. Size of this FIFO determined by CONFIG_NR and SAMPLE_NR. If CONFIG_NR = 0, FIFO size is SAMPLE_NR. If CONFIG_NR > 0, FIFO size is SAMPLE_NR * CONFIG_NR. NUM_AUTO_RESAMPLE must be less than or equal to the FIFO size in debug mode.
	DISABLED			0	N/A
	ENABLED			1	N/A

Bits	Name	SW	HW	Default or Enum	Description
4:5	NUM_SAMPLES	RW	R	0	Number of samples (minus 1) to be scanned. NUM_SAMPLES > 1 results in autonomous scan same sensor (AS-SS) behaviour. Firmware Rule: Usable setting for NUM_SAMPLES is limited depending on the size of the result FIFO. Size of this FIFO determined by CONFIG_NR and SAMPLE_NR. If CONFIG_NR = 0, FIFO size is SAMPLE_NR. If CONFIG_NR > 0, FIFO size is SAMPLE_NR * CONFIG_NR. NUM_SAMPLES must be less than or equal to the FIFO size in debug mode.
8	RAW_COUNT_MODE	RW	R	0	Control bit to handle behaviour when RAW_COUNT exceeds 0xFFFF. '0': Saturate. In this scenario, RAW_COUNT is clamped at 0xFFFF and RESULT_FIFO_RD.OVERFLOW is set. '1': Overflow. In this scenario, RAW_COUNT rolls over and RESULT_FIFO_RD.OVERFLOW is set. This mode allows more sensitive tuning if measuring baseline capacitance is a don't care (e.g. SAR use case).
	SATURATE			0	N/A
	OVERFLOW			1	N/A
12:14	DEBUG_CONV_PH_SEL	RW	R	0	Debug counter conversion chop phase select for DEBUG_CONV_COUNT. Must be between 0 and NUM_CONV. The number of conversions (or chop phases) for a given scan is controlled by NUM_CONV. Although only discrete values are possible for NUM_CONV, any conversion index up to this number may be selected up to NUM_CONV. For example if NUM_CONV = 7 (number of conversions is 8), then DEBUG_CONG_PH_SEL can be any value between 0 and 7 to select the particular conversion that the count is required for.
16:23	FRAME_START_PTR	RW	R	0	Pointer to first sensor configuration of a frame. Hardware increments a local pointer from this start point. In LP-AoC mode, hardware returns to this pointer after the frame is complete prior to starting the next frame (after a timeout).

11.4.4 MSC_SCAN_CTL2

Description: Scan Control 2
Address: 0x4029000C
Offset: 0xC
Retention: Retained
IsDeepSleep: No
Comment: This register is used to configure global scan settings.
Default: 0x1

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	NUM_EPI_CYCLES [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	None [15:10]						NUM_EPI_CYCLES [9:8]	

Bits	23	22	21	20	19	18	17	16
Name	None [23:17]							CHOP_POL [16:16]

Bits	31	30	29	28	27	26	25	24
Name	None [31:25]							CHOP _EVEN _HOLD_EN [24:24]

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:9	NUM_EPI_CYCLES	RW	R	1	Number of clk_mod cycles to be run during EPILOGUE. Note that setting this register to 0 is an illegal configuration. This guarantees at least 1 clk_mod cycle during EPILOGUE (required to help timing closure in Sequencer FSM).
	MIN			1	N/A
16	CHOP_POL	RW	R	0	Polarity of first chop phase. Hardware updates chop control locally from this point (via inversion and following CHOP_EVEN_HOLD_EN programming also).
24	CHOP_EVEN_HOLD_EN	RW	R	0	Use this bit to hold the chop value at the end of every even chop phase of NUM_CONV.
	DISABLED			0	N/A
	ENABLED			1	N/A

11.4.5 MSC_INIT_CTL1

Description: Initialisation Control 1
Address: 0x40290010
Offset: 0x10
Retention: Retained
IsDeepSleep: No
Comment: This register is used to configure the scan coarse initialisation settings.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	NUM_INIT_CMOD_12_RAIL_CYCLES [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	None [15:12]				NUM_INIT_CMOD_12_RAIL_CYCLES [11:8]			

Bits	23	22	21	20	19	18	17	16
Name	NUM_INIT_CMOD_12_SHORT_CYCLES [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:29]			PER_SAMPLE [28:28]	NUM_INIT_CMOD_12_SHORT_CYCLES [27:24]			

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:11	NUM_INIT_CMOD_12_RAIL_CYCLES	RW	R	0	Duration of the coarse initialisation phase (e.g. connecting Cmod1 to vdda and Cmod2 to vssa in full-wave mode). Programmed in terms of clk_mod cycles.
16:27	NUM_INIT_CMOD_12_SHORT_CYCLES	RW	R	0	Duration of the coarse short phase (shorting Cmod1 and Cmod2 in full-wave mode). Programmed in terms of clk_mod cycles. Should be set to zero in the case of half-wave mode.
28	PER_SAMPLE	RW	R	0	Decides if coarse initialisation is done per sample when NUM_SAMPLES > 0 (i.e. more than one sample per scan). Applies to CMOD_SEL selected Cmod.
	DISABLED			0	N/A
	ENABLED			1	N/A

11.4.6 MSC_INIT_CTL2

Description: Initialisation Control 2
Address: 0x40290014
Offset: 0x14
Retention: Retained
IsDeepSleep: No
Comment: This register is used to configure the scan coarse initialisation settings.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	NUM_INIT_CMOD_34_RAIL_CYCLES [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	None [15:12]				NUM_INIT_CMOD_34_RAIL_CYCLES [11:8]			

Bits	23	22	21	20	19	18	17	16
Name	NUM_INIT_CMOD_34_SHORT_CYCLES [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:28]				NUM_INIT_CMOD_34_SHORT_CYCLES [27:24]			

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:11	NUM_INIT_CMOD_34 _RAIL_CYCLES	RW	R	0	Duration of the coarse initialisation phase (e.g. connecting Cmod3 to vdda and Cmod4 to vssa in full-wave mode). Programmed in terms of clk_mod cycles.
16:27	NUM_INIT_CMOD_34 _SHORT_CYCLES	RW	R	0	Duration of the coarse short phase (shorting Cmod3 and Cmod4 in full-wave mode). Programmed in terms of clk_mod cycles. Should be set to zero in the case of half-wave mode.

11.4.7 MSC_INIT_CTL3

Description: Initialisation Control 3
Address: 0x40290018
Offset: 0x18
Retention: Retained
IsDeepSleep: No
Comment: This register is used to configure the scan fine initialisation settings.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	NUM_PRO_OFFSET_CYCLES [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	INIT_MODE [15:15]	None [14:12]			CMOD_SEL [11:10]		NUM_PRO_OFFSET _TRIPS [9:8]	

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:7	NUM_PRO_OFFSET_CYCLES	RW	R	0	Maximum number of clk_mod cycles to be assigned for the PRO_OFFSET state. If NUM_PRO_OFFSET_TRIPS are observed before this timeout, exit at that point. Programming combinations: a) OFFSET_CYCLES == 0 && OFFSET_TRIPS == 0 -> Skip PRO_OFFSET b) OFFSET_CYCLES == 0 && OFFSET_TRIPS > 0 -> wait in PRO_OFFSET for OFFSET_TRIPS c) OFFSET_CYCLES > 0 && OFFSET_TRIPS == 0 -> wait in PRO_OFFSET for OFFSET_CYCLES d) OFFSET_CYCLES > 0 && OFFSET_TRIPS > 0 -> wait in PRO_OFFSET for the first of OFFSET_CYCLES and OFFSET_TRIPS. Note that if OFFSET_TRIPS > 0: i) SW_COTCA and SW_COCB autonomously adjust as per their description after each comparator trip apart from the last trip. Expect OFFSET_TRIPS-1 adjustments in PRO_OFFSET. ii) If FINE_MODE == COMPENSATION SW_CFTCA and SW_CFTCB autonomously swap settings after each comparator trip apart from the last trip. Expect OFFSET_TRIPS-1 adjustments in PRO_OFFSET. iii) For both sets of switches above, after the last trip the switches revert to their programmed MMIO setting when exiting PRO_OFFSET. If OFFSET_TRIPS == 0 and OFFSET_CYCLES > 0: Intention is that PRO_OFFSET be a fixed duration. The autonomous behaviour for this case is the same as the OFFSET_TRIPS > 0 case, except that the number of trips (and hence the number of adjustments for (i) and (ii) above) are unknown in advance. At the end of OFFSET_CYCLES, the switches revert to their programmed MMIO setting when exiting PRO_OFFSET.
8:9	NUM_PRO_OFFSET_TRIPS	RW	R	0	Number of comparator trips required to be observed in PRO_OFFSET before proceeding to dummy cycles. Note that a 'trip' is defined as a change of state of the comparator (either a 0 to 1 or a 1 to 0 transition). A trip at the very start of PRO_OFFSET is considered a trip with respect to this count.
10:11	CMOD_SEL	RW	R	0	Select which Cmod are used and the cycle thresholds to be used for coarse initialisation. Note this field affects which Cmod switches are autonomously initialised by hardware as well as influencing the cycle counters as per INIT_MODE. '0' || '2': Use NUM_INIT_CMOD_12_RAIL_CYCLES and NUM_INIT_CMOD_12_SHORT_CYCLES '1' || '3': Use NUM_INIT_CMOD_34_RAIL_CYCLES and NUM_INIT_CMOD_34_SHORT_CYCLES Firmware Rule: Firmware must program the appropriate SNS_SW_SEL_CMODx.ENABLED bits to match the Cmod selected with CMOD_SEL. Firmware must also set a valid INIT_MODE with CMOD_SEL.
	CMOD_12			0	Used for full-wave
	CMOD_34			1	Used for full-wave
	CMOD_1			2	Used for half-wave

Bits	Name	SW	HW	Default or Enum	Description
	CMOD_3			3	Used for half-wave
15	INIT_MODE	RW	R	0	Determines autonomous initialisation behaviour during INIT_CMOD. 0: Decode CMOD_SEL. CMOD_12: S1CV = 1, S2CG = 1 CMOD_34: S3CV = 1, S4CG = 1 CMOD_1: S1CV = 1 CMOD_3: S3CV = 1 1: Decode CMOD_SEL. Should be CMOD_1 or CMOD_3. Firmware Rule: Firmware should also close CBSO, FSP and one of BGRF/RMF/MBF to select type of reference. CMOD_1: C1CB = 1 CMOD_3: C3CB = 1
	REFERENCE_VDDA			0	Used for full and half wave when Vdda is reference.
	REFERENCE_VREF			1	Used for half-wave when Vref is reference.

11.4.8 MSC_INIT_CTL4

Description: Initialisation Control 4
Address: 0x4029001C
Offset: 0x1C
Retention: Retained
IsDeepSleep: No
Comment: This register is used to configure the scan fine initialisation settings.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	NUM_PRO_DUMMY_SUB_CONVS [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	NUM_PRO_WAIT_CYCLES [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:26]						NUM_PRO_WAIT _CYCLES [25:24]	

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:7	NUM_PRO_DUMMY _SUB_CONVS	RW	R	0	Number of sub-conversions (dummy cycles) to be run during PRO_DUMMY. Firmware Rule: If chopping is enabled (NUM_CONV > ONE), then NUM_PRO_DUMMY_SUB_CONVS must be >=1.
16:25	NUM_PRO_WAIT _CYCLES	RW	R	0	Number of clk_mod cycles to be run during PRO_WAIT. Firmware Rule: If chopping is enabled (NUM_CONV > ONE), then NUM_PRO_WAIT_CYCLES must be >=1.

11.4.9 MSC_SENSE_DUTY_CTL

Description: Sense Clock Duty Cycle Control
Address: 0x40290020
Offset: 0x20
Retention: Retained
IsDeepSleep: No
Comment: This register controls the duty cycle of the sensor clock.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	PHASE_WIDTH [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	None [15:12]				PHASE_WIDTH [11:8]			

Bits	23	22	21	20	19	18	17	16
Name	PHASE_SHIFT_CYCLES [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:28]				PHASE_WIDTH_SEL [27:27]	None [26:26]	PHASE_SHIFT_CYCLES [25:24]	

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:11	PHASE_WIDTH	RW	R	0	Control width (clk_mod cycles) of ph0 and ph2 OR ph1 and ph3. If set to zero, Fs is divided equally between all phases. This field is only applicable when LFSR_MODE = DIRECT_CLOCK.
16:25	PHASE_SHIFT_CYCLES	RW	R	0	Phase shift cycle control for ph0X and ph1X. Must be > 0 if PHASE_SHIFT_EN = 1.
27	PHASE_WIDTH_SEL	RW	R	0	Select which phases the PHASE_WIDTH applies to: '0': PHASE_WIDTH corresponds to width of ph0 and ph2. '1': PHASE_WIDTH corresponds to width of ph1 and ph3.
	PH0_AND_PH2			0	N/A
	PH1_AND_PH3			1	N/A

11.4.10 MSC_SENSE_PERIOD_CTL

Description: Sense Clock Period Control
Address: 0x40290024
Offset: 0x24
Retention: Retained
IsDeepSleep: No
Comment: This register controls the period of the sensor clock via spread spectrum / PRS.
Default: 0x84C

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	LFSR_POLY [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	None [15:12]				LFSR_POLY [11:8]			

Bits	23	22	21	20	19	18	17	16
Name	None [23:20]				LFSR_SCALE [19:16]			

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:11	LFSR_POLY	RW	R	2124	Programmable polynomial to be used for the sense LFSR. For example (default): G(x) = X^12 + X^7 + X^4 + X^3 + 1 LFSR_POLY = 0x84C (1000_0100_1100). Note that LFSR_POLY[i] = 1 if X^(i+1) is included in the polynomial. The +1 feedback term is implied and doesn't need a programmable bit.
16:19	LFSR_SCALE	RW	R	0	Shift the LFSR output left by LSFR_SCALE bits before adding to SENSE_DIV. This scaling is only applicable in spread spectrum mode. Note that the clock divider including the dithering term must fit in 12 bits, otherwise the result is undefined.

11.4.11 MSC_FILTER_CTL

Description: Filter Control
Address: 0x40290028
Offset: 0x28
Retention: Retained
IsDeepSleep: No
Comment: Global settings for sample filter.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:17]							BIT _FORMAT [16:16]

Bits	31	30	29	28	27	26	25	24
Name	None [31:25]							FILTER _MODE [24:24]

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
16	BIT_FORMAT	RW	R	0	Determines how the synchronised comparator output is interpreted by the filter pipeline. Firmware Rule: When FILTER_MODE = CIC1, BIT_FORMAT should be UNSIGNED.
	UNSIGNED			0	Input values [0,+1]
	SIGNED			1	Input values [-1,+1]. In this scenario a value of 0 is interpreted as -1.
24	FILTER_MODE	RW	R	0	N/A
	CIC1			0	Use the standard first order counter low pass filter (equivalent to CIC1). Scan Time = 2^M Number of CIC1 sub-samples = 1 Time for first valid CIC1 sub-sample = 2^M Number of valid CIC1 sub-samples = 1 CIC1 Scan Resolution = 2^M = N
	CIC2			1	Use CIC2 Filter. Advantage of CIC2 over CIC1 is a higher resolution result for an equivalent scan time. All valid sub-samples are averaged to achieve an overall sample result for the scan. Interrupt is fired for every valid sub-sample to facilitate debug of the individual sub-samples. Scan Time = 2^M Number of CIC2 sub-samples = (2^M)/N Time for first valid CIC2 sub-sample = 2N Number of valid CIC2 sub-samples = ((2^M)/N) - 1 CIC2 Scan Resolution = N^2

11.4.12 MSC_CCOMP_CDAC_CTL

Description: Compensation CAPDAC Control
Address: 0x40290030
Offset: 0x30
Retention: Retained
IsDeepSleep: No
Comment: Global settings for compensation CAPDAC.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	SEL_CO_PRO_OFFSET [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	EPILOGUE_EN [31:31]	None [30:24]						

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
8:15	SEL_CO_PRO_OFFSET	RW	R	0	Select value for Compensation CAPDAC size during PRO_OFFSET until the first comparator trip is observed. Otherwise SEL_CO applies.
31	EPILOGUE_EN	RW	R	0	Control on whether Ccomp is active during EPILOGUE for final balancing in a conversion. Note that for this bit to enable Ccomp during EPILOGUE, need SEL_CO > 0 or FINE_MODE = COMPENSATION.
	DISABLED			0	N/A
	ENABLED			1	N/A

11.4.13 MSC_DITHER_CDAC_CTL

Description: Flatspot/Dither CAPDAC Switch Control
Address: 0x40290034
Offset: 0x34
Retention: Retained
IsDeepSleep: No
Comment: Global settings for flatspot/dither CAPDAC.
Default: 0x8E0000

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	SEL_FL [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	LFSR_POLY_FL [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:7	SEL_FL	RW	R	0	Select value for Dither/Flatspot CAPDAC size. If dithering is enabled (FL_EN = 1), this is the seed value for the LFSR. If dithering is disabled, this value is presented directly to the hard IP as the CAPDAC code.
16:23	LFSR_POLY_FL	RW	RW	142	Dither/Flatspot CAPDAC LFSR polynomial. Uses same encoding as the spread spectrum polynomial LFSR_POLY. For example (default): G(x) = X^8 + X^4 + X^3 + X^2 + 1 LFSR_POLY_FL = 0x8E (1000_1110). Note that LFSR_POLY_FL[i] = 1 if X^(i+1) is included in the polynomial. The +1 feedback term is implied and doesn't need a programmable bit.

11.4.14 MSC_CSW_CTL

Description: Control Mux Switch Control
Address: 0x40290040
Offset: 0x40
Retention: Retained
IsDeepSleep: No
Comment: Each bit x in this register decides on the source of the switch control for control MUX x.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	CSW_FUNC_MODE [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	CSW_FUNC_MODE [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	CSW_FUNC_MODE [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	CSW_FUNC_MODE [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	CSW_FUNC_MODE	RW	R	0	Select between SW_SEL_CSW[x] and SW_SEL_CSW_FUNC. CSW_FUNC_MODE[x] = 0: Use SW_CSW_CTL for control MUX x. CSW_FUNC_MODE[x] = 1: Use SW_SEL_CSW_FUNC[y] for control MUX x as selected by y = {SW_SEL_CSW_MASK2[x],SW_SEL_CSW_MASK1[x],SW_SEL_CSW_MASK0[x]}.

11.4.15 MSC_SW_SEL_GPIO

Description: GPIO Switch Control
Address: 0x40290044
Offset: 0x44
Retention: Retained
IsDeepSleep: No
Comment: Details defined in MTMH#194. PHASE_GAP_*_EN has no influence on the signal options for this register since GPIO has in-built non overlap circuitry.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:7]	SW_CSD_SHIELD [6:4]			None [3:3]	SW_CSD_SENSE [2:0]		

Bits	15	14	13	12	11	10	9	8
Name	None [15:14]		SW_CSD_POLARITY [13:12]		None [11:9]			SW_CSD_MUTUAL [8:8]

Bits	23	22	21	20	19	18	17	16
Name	None [23:23]	SW_DSI_CMOD [22:20]			None [19:17]			SW_CSD_CHARGE [16:16]

Bits	31	30	29	28	27	26	25	24
Name	None [31:27]					SW_DSI_CSH_TANK [26:24]		

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:2	SW_CSD_SENSE	RW	R	0	MUX select for csd_sense waveform.
	LOGIC_0			0	N/A
	LOGIC_1			1	N/A
	PH0			2	N/A
	PH1			3	N/A
	PH0_OR_PH3			4	N/A
	PH0X			5	N/A
	PH1X			6	N/A
4:6	SW_CSD_SHIELD	RW	R	0	MUX select for csd_shield waveform.
	LOGIC_0			0	N/A
	LOGIC_1			1	N/A
	PH0			2	N/A
	PH1			3	N/A
	PH0_OR_PH3			4	N/A
	PH0_OR_FS2PH1_AND_PH1_OR_PH3			5	ph0 || [Fs2_ph1 && (ph1 || ph3)]
	PH1X			6	N/A
8	SW_CSD_MUTUAL	RW	R	0	MUX select for csd_mutual waveform.
	LOGIC_0			0	N/A
	LOGIC_1			1	N/A
12:13	SW_CSD_POLARITY	RW	R	0	MUX select for csd_polarity waveform.
	LOGIC_0			0	N/A
	LOGIC_1			1	N/A
	PH0_OR_PH1			2	N/A
16	SW_CSD_CHARGE	RW	R	0	MUX select for csd_charge waveform.
	LOGIC_0			0	N/A

Bits	Name	SW	HW	Default or Enum	Description
	LOGIC_1			1	N/A
20:22	SW_DSI_CMOD	RW	R	0	MUX select for dsi_cmod waveform. if CMOD_SEL = CMOD_12 | CMOD_1 dsi_cmod[0] = Decode SW_DSI_CMOD to select appropriate dsi_cmod waveform. dsi_cmod[1] = 0. if CMOD_SEL = CMOD_34 | CMOD_3 dsi_cmod[0] = 0. dsi_cmod[1] = Decode SW_DSI_CMOD to select appropriate dsi_cmod waveform. This is assuming that: dsi_cmod[0] is routed to cmod1 dsi_cmod[1] is routed to cmod3 Note that hardware overrides MMIO setting for dsi_cmod and sets it 1 during the INIT_SHORT state if using GPIO sensors (SW_DSI_CMOD != OPEN || SW_DSI_CSHTANK != OPEN).
	LOGIC_0			0	N/A
	LOGIC_1			1	N/A
	CHOP_PH1_PH0			2	chop == 1 ? ph1 : ph0
	CHOP_PH3_PH1			3	chop == 1 ? ph3 : ph1
	PH0			4	N/A
24:26	SW_DSI_CSH_TANK	RW	R	0	MUX select for dsi_csh_tank waveform. if CMOD_SEL = CMOD_12 | CMOD_1 dsi_csh_tank[0] = Decode SW_DSI_CSH_TANK to select appropriate dsi_csh_tank waveform. dsi_csh_tank[1] = 0. if CMOD_SEL = CMOD_34 | CMOD_3 dsi_csh_tank[0] = 0. dsi_csh_tank[1] = Decode SW_DSI_CSH_TANK to select appropriate dsi_csh_tank waveform. This is assuming that: dsi_csh_tank[0] is routed to cmod2 dsi_csh_tank[1] is routed to cmod4 Note that hardware overrides MMIO setting for dsi_csh_tank and sets it 1 during the INIT_SHORT state if using GPIO sensors (SW_DSI_CMOD != OPEN || SW_DSI_CSHTANK != OPEN).
	LOGIC_0			0	N/A
	LOGIC_1			1	N/A
	CHOP_PH0_PH1			2	chop == 1 ? ph0 : ph1
	CHOP_PH1_PH3			3	chop == 1 ? ph1 : ph3
	PH1			4	N/A

11.4.16 MSC_SW_SEL_CDAC_RE

Description: Reference CAPDAC Switch Control
Address: 0x40290048
Offset: 0x48
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:7]	SW_RECB [6:4]			None [3:3]	SW_RETCA [2:0]		

Bits	15	14	13	12	11	10	9	8
Name	None [15:15]	SW_RETG [14:12]			None [11:11]	SW_RETV [10:8]		

Bits	23	22	21	20	19	18	17	16
Name	None [23:22]		SW_REBG [21:20]		None [19:18]		SW_REBV [17:16]	

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:2	SW_RETCA	RW	R	0	Reference CAPDAC top plate to CSD Bus A Switch
	OPEN			0	sel = 00
	CLOSED			1	sel = 01
	CHOP_CLK_BAR			2	chop == 0 ? sel = 10 (clk_reffb) : sel = 11 (!clk_reffb)
	CHOP_CLK			3	chop == 1 ? sel = 10 (clk_reffb) : sel = 11 (!clk_reffb)
	PH1			4	DFT mode (ph1 ? sel = 01 : sel = 00)
	PH3			5	DFT mode (ph3 ? sel = 01 : sel = 00)
4:6	SW_RECB	RW	R	0	Reference CAPDAC to CSD Bus B Switch
	OPEN			0	sel = 00
	CLOSED			1	sel = 01
	CHOP_CLK_BAR			2	chop == 0 ? sel = 10 (clk_reffb) : sel = 11 (!clk_reffb)
	CHOP_CLK			3	chop == 1 ? sel = 10 (clk_reffb) : sel = 11 (!clk_reffb)
	PH1			4	DFT mode (ph1 ? sel = 01 : sel = 00)
	PH3			5	DFT mode (ph3 ? sel = 01 : sel = 00)
8:10	SW_RETV	RW	R	0	Reference CAPDAC top plate to vdda_q Switch. Firmware Rule: Do not program RETV and RETG such that they are closed simultaneously.
	OPEN			0	sel = 00
	CLOSED			1	sel = 01
	CLK			2	sel = 10 (clk_reffb)
	CLK_BAR			3	sel = 11 (!clk_reffb)
	PH0			4	DFT mode
	PH2			5	DFT mode
12:14	SW_RETG	RW	R	0	Reference CAPDAC top plate to vssa_q Switch. Firmware Rule: Do not program RETV and RETG such that they are closed simultaneously.
	OPEN			0	sel = 00
	CLOSED			1	sel = 01
	CLK			2	sel = 10 (clk_reffb)

Bits	Name	SW	HW	Default or Enum	Description
	CLK_BAR			3	sel = 11 (!clk_reffb)
	PH0			4	DFT mode
	PH2			5	DFT mode
16:17	SW_REBV	RW	R	0	Reference CAPDAC bottom plate to vdda_q Switch. Firmware Rule: Do not program REBV and REBG such that they are closed simultaneously.
	OPEN			0	sel = 00
	CLOSED			1	sel = 01
	CLK			2	sel = 10 (clk_reffb)
	CLK_BAR			3	sel = 11 (!clk_reffb)
20:21	SW_REBG	RW	R	0	Reference CAPDAC bottom plate to vssa_q Switch. Firmware Rule: Do not program REBV and REBG such that they are closed simultaneously.
	OPEN			0	sel = 00
	CLOSED			1	sel = 01
	CLK			2	sel = 10 (clk_reffb)
	CLK_BAR			3	sel = 11 (!clk_reffb)

11.4.17 MSC_SW_SEL_CDAC_CO

Description: Compensation CAPDAC Switch Control
Address: 0x4029004C
Offset: 0x4C
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:7]	SW_COCB [6:4]			None [3:3]	SW_COTCA [2:0]		

Bits	15	14	13	12	11	10	9	8
Name	None [15:15]	SW_COTG [14:12]			None [11:11]	SW_COTV [10:8]		

Bits	23	22	21	20	19	18	17	16
Name	None [23:22]		SW_COBG [21:20]		None [19:18]		SW_COBV [17:16]	

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:2	SW_COTCA	RW	R	0	Compensation CAPDAC top plate to CSD Bus A Switch. Note during the PRO_OFFSET state the following autonomous overriding occurs: (compout_sync ^ CHOP_POL) ? [sel = 11 (!clk_comp)] : [sel = 10 (clk_comp)]. Note that the CHOP_POL above is the hardware copy of the current chop polarity.
	OPEN			0	sel = 00
	CLOSED			1	sel = 01
	CHOP_CLK_BAR			2	chop == 0 ? sel = 10 (clk_comp) : sel = 11 (!clk_comp)
	CHOP_CLK			3	chop == 1 ? sel = 10 (clk_comp) : sel = 11 (!clk_comp)
	PH1			4	DFT mode (ph1 ? sel = 01 : sel = 00)
	PH3			5	DFT mode (ph3 ? sel = 01 : sel = 00)
4:6	SW_COCB	RW	R	0	Compensation CAPDAC to CSD Bus B Switch. Note during the PRO_OFFSET state the following autonomous overriding occurs: (compout_sync ^ CHOP_POL) ? [sel = 10 (clk_comp)] : [sel = 11 (!clk_comp)]. Note that the CHOP_POL above is the hardware copy of the current chop polarity.
	OPEN			0	sel = 00
	CLOSED			1	sel = 01
	CHOP_CLK_BAR			2	chop == 0 ? sel = 10 (clk_comp) : sel = 11 (!clk_comp)
	CHOP_CLK			3	chop == 1 ? sel = 10 (clk_comp) : sel = 11 (!clk_comp)
	PH1			4	DFT mode (ph1 ? sel = 01 : sel = 00)
	PH3			5	DFT mode (ph3 ? sel = 01 : sel = 00)
8:10	SW_COTV	RW	R	0	Compensation CAPDAC top plate to vdda_q Switch. Firmware Rule: Do not program COTV and COTG such that they are closed simultaneously.
	OPEN			0	sel = 00

Bits	Name	SW	HW	Default or Enum	Description
	CLOSED			1	sel = 01
	CLK			2	sel = 10 (clk_reffb)
	CLK_BAR			3	sel = 11 (!clk_reffb)
	PH0			4	DFT mode
	PH2			5	DFT mode
12:14	SW_COTG	RW	R	0	Compensation CAPDAC top plate to vssa_q Switch. Firmware Rule: Do not program COTV and COTG such that they are closed simultaneously.
	OPEN			0	sel = 00
	CLOSED			1	sel = 01
	CLK			2	sel = 10 (clk_reffb)
	CLK_BAR			3	sel = 11 (!clk_reffb)
	PH0			4	DFT mode
	PH2			5	DFT mode
16:17	SW_COBV	RW	R	0	Compensation CAPDAC bottom plate to vdda_q Switch. Firmware Rule: Do not program COBV and COBG such that they are closed simultaneously.
	OPEN			0	sel = 00
	CLOSED			1	sel = 01
	CLK			2	sel = 10 (clk_comp)
	CLK_BAR			3	sel = 11 (!clk_comp)
20:21	SW_COBG	RW	R	0	Compensation CAPDAC bottom plate to vssa_q Switch. Firmware Rule: Do not program COBV and COBG such that they are closed simultaneously.
	OPEN			0	sel = 00
	CLOSED			1	sel = 01
	CLK			2	sel = 10 (clk_comp)
	CLK_BAR			3	sel = 11 (!clk_comp)

11.4.18 MSC_SW_SEL_CDAC_CF

Description: Fine CAPDAC Switch Control
Address: 0x40290050
Offset: 0x50
Retention: Retained
IsDeepSleep: No
Comment: Note that FINE_MODE is connected to hard IP and MUX based on {FINE_MODE,sel} is done in the SoftIP.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:7]	SW_CFTCB [6:4]			None [3:3]	SW_CFTCA [2:0]		

Bits	15	14	13	12	11	10	9	8
Name	None [15:15]	SW_CFTG [14:12]			None [11:11]	SW_CFTV [10:8]		

Bits	23	22	21	20	19	18	17	16
Name	None [23:22]		SW_CFBG [21:20]		None [19:18]		SW_CFBV [17:16]	

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:2	SW_CFTCA	RW	R	0	Fine CAPDAC top plate to CSD Bus A Switch. Note during the PRO_OFFSET state the following autonomous overriding occurs if FINE_MODE = COMPENSATION: (compout_sync ^ CHOP_POL) ? [sel = 11 (!clk_comp)] : [sel = 10 (clk_comp)]. Note that the CHOP_POL above is the hardware copy of the current chop polarity.
	OPEN			0	sel = 00
	CLOSED			1	sel = 01
	CHOP_CLK_BAR			2	case({chop,FINE_MODE}) {1,REFERENCE} : sel = 11 (!clk_reffb) {1,COMPENSATION} : sel = 11 (!clk_comp) {0,REFERENCE} : sel = 10 (clk_reffb) {0,COMPENSATION} : sel = 10 (clk_comp)
	CHOP_CLK			3	case({chop,FINE_MODE}) {1,REFERENCE} : sel = 10 (clk_reffb) {1,COMPENSATION} : sel = 10 (clk_comp) {0,REFERENCE} : sel = 11 (!clk_reffb) {0,COMPENSATION} : sel = 11 (!clk_comp)
	PH1			4	DFT mode (ph1 ? sel = 01 : sel = 00)
	PH3			5	DFT mode (ph3 ? sel = 01 : sel = 00)
4:6	SW_CFTCB	RW	R	0	Fine CAPDAC top plate to CSD Bus B Switch. Note during the PRO_OFFSET state the following autonomous overriding occurs if FINE_MODE = COMPENSATION: (compout_sync ^ CHOP_POL) ? [sel = 10 (clk_comp)] : [sel = 11 (!clk_comp)]. Note that the CHOP_POL above is the hardware copy of the current chop polarity.
	OPEN			0	sel = 00
	CLOSED			1	sel = 01

Bits	Name	SW	HW	Default or Enum	Description
	CHOP_CLK_BAR			2	case({chop,FINE_MODE}) {1,REFERENCE} : sel = 11 (!clk_reffb) {1,COMPENSATION} : sel = 11 (!clk_comp) {0,REFERENCE} : sel = 10 (clk_reffb) {0,COMPENSATION} : sel = 10 (clk_comp)
	CHOP_CLK			3	case({chop,FINE_MODE}) {1,REFERENCE} : sel = 10 (clk_reffb) {1,COMPENSATION} : sel = 10 (clk_comp) {0,REFERENCE} : sel = 11 (!clk_reffb) {0,COMPENSATION} : sel = 11 (!clk_comp)
	PH1			4	DFT mode (ph1 ? sel = 01 : sel = 00)
	PH3			5	DFT mode (ph3 ? sel = 01 : sel = 00)
8:10	SW_CFTV	RW	R	0	Fine CAPDAC top plate to vdda_q Switch. Firmware Rule: Do not program CFTV and CFTG such that they are closed simultaneously.
	OPEN			0	sel = 00
	CLOSED			1	sel = 01
	CLK			2	sel = 10 [(FINE_MODE == REFERENCE) ? clk_reffb : clk_comp]
	CLK_BAR			3	sel = 11 [(FINE_MODE == REFERENCE) ? !clk_reffb : !clk_comp]
	PH0			4	DFT mode (ph0 ? sel = 01 : sel = 00)
	PH2			5	DFT mode (ph2 ? sel = 01 : sel = 00)
12:14	SW_CFTG	RW	R	0	Fine CAPDAC top plate to vssa_q Switch. Firmware Rule: Do not program CFTV and CFTG such that they are closed simultaneously.
	OPEN			0	sel = 00
	CLOSED			1	sel = 01
	CLK			2	sel = 10 [(FINE_MODE == REFERENCE) ? clk_reffb : clk_comp]
	CLK_BAR			3	sel = 11 [(FINE_MODE == REFERENCE) ? !clk_reffb : !clk_comp]
	PH0			4	DFT mode (ph0 ? sel = 01 : sel = 00)
	PH2			5	DFT mode (ph2 ? sel = 01 : sel = 00)
16:17	SW_CFBV	RW	R	0	Fine CAPDAC bottom plate to vdda_q Switch. Firmware Rule: Do not program CFBV and CFBG such that they are closed simultaneously.
	OPEN			0	sel = 00
	CLOSED			1	sel = 01
	CLK			2	FINE_MODE == REFERENCE ? sel = 10 (clk_reffb) : sel = 10 (clk_comp)
	CLK_BAR			3	FINE_MODE == REFERENCE ? sel = 11 (!clk_reffb) : sel = 11 (!clk_comp)
20:21	SW_CFBG	RW	R	0	Fine CAPDAC bottom plate to vssa_q Switch. Firmware Rule: Do not program CFBV and CFBG such that they are closed simultaneously.
	OPEN			0	sel = 00
	CLOSED			1	sel = 01
	CLK			2	FINE_MODE == REFERENCE ? sel = 10 (clk_reffb) : sel = 10 (clk_comp)
	CLK_BAR			3	FINE_MODE == REFERENCE ? sel = 11 (!clk_reffb) : sel = 11 (!clk_comp)

11.4.19 MSC_SW_SEL_CMOD1

Description: CMOD Switch Control 1
Address: 0x40290054
Offset: 0x54
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:4]				SW_C1CA [3:0]			

Bits	15	14	13	12	11	10	9	8
Name	None [15:14]		SW_C1CC [13:12]		SW_C1CB [11:8]			

Bits	23	22	21	20	19	18	17	16
Name	None [23:20]				SW_C1CV [19:16]			

Bits	31	30	29	28	27	26	25	24
Name	ENABLED [31:31]	REF _MODE [30:30]	None [29:28]		SW_C1CG [27:24]			

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:3	SW_C1CA	RW	R	0	CMOD1 to CSD Bus A Switch. During INIT_SHORT (used for full-wave scanning) if CMOD_SEL = CMOD_12, hardware sets C1CA = CLOSED. Firmware Rule: See rule for ENABLED.
	OPEN			0	N/A
	CLOSED			1	N/A
	CHOP_TWO_PHASE			2	chop == 0 ? ph0 : ph1
	CHOP_FOUR_PHASE			3	chop == 0 ? ph1 : ph3
	CHOP_MPSC_D			4	chop == 0 ? ph3 : ph1
	CHOP_MPRX			5	chop == 0 ? ph1 : ph0
	PH1			6	N/A
	PH3			7	N/A
	CHOP_CLK_BAR			8	chop == 0 ? clk_extfb : clk_extfb_bar
	CHOP_CLK			9	chop == 1 ? clk_extfb : clk_extfb_bar
8:11	SW_C1CB	RW	R	0	CMOD1 to CSD Bus B Switch. Firmware Rule: See rule for ENABLED.
	OPEN			0	N/A
	CLOSED			1	N/A
	CHOP_TWO_PHASE			2	chop == 0 ? ph1 : ph0
	CHOP_FOUR_PHASE			3	chop == 0 ? ph3 : ph1
	CHOP_MPSC_D			4	chop == 0 ? ph1 : ph3
	CHOP_MPRX			5	chop == 0 ? ph0 : ph1
	PH0			6	N/A
	PH2			7	N/A
	CHOP_CLK_BAR			8	chop == 0 ? clk_extfb : clk_extfb_bar
	CHOP_CLK			9	chop == 1 ? clk_extfb : clk_extfb_bar

Bits	Name	SW	HW	Default or Enum	Description
12:13	SW_C1CC	RW	R	0	CMOD1 to CSD Bus C Switch. Firmware Rule: See rule for ENABLED.
	OPEN			0	N/A
	CLOSED			1	N/A
	PH1_OR_PH3			2	N/A
16:19	SW_C1CV	RW	R	0	CMOD1 to vdda_q Switch. Firmware Rule: Do not program C1CV and C1CG such that they are closed simultaneously.
	OPEN			0	N/A
	CLOSED			1	N/A
	PH0			2	N/A
	PH1			3	N/A
	PH2			4	N/A
	PH0_OR_PH1			5	N/A
	PH0X			6	N/A
	PH1X			7	N/A
	PH0_OR_FS2PH0_AND_PH1_OR_PH3			8	ph0 || [Fs2_ph0 && (ph1 || ph3)]
	CLK			9	clk_extfb
24:27	SW_C1CG	RW	R	0	CMOD1 to vssa_q Switch. Firmware Rule: Do not program C1CV and C1CG such that they are closed simultaneously.
	OPEN			0	N/A
	CLOSED			1	N/A
	PH0			2	N/A
	PH1			3	N/A
	PH2			4	N/A
	PH1_OR_PH3			5	N/A
	PH2_OR_PH3			6	N/A
	PH0X			7	N/A
	PH1X			8	N/A
	PH2_OR_FS2PH1_AND_PH1_OR_PH3			9	ph2 || [Fs2_ph1 && (ph1 || ph3)]
	CLK_BAR			10	clk_extfb_bar
30	REF_MODE	RW	R	0	CMOD1 is used as a reference in scenario where CMOD can be re-purposed when not used as a CMOD.
	DISABLED			0	N/A
	ENABLED			1	N/A

Bits	Name	SW	HW	Default or Enum	Description
31	ENABLED	RW	R	0	CMOD1 enable. Firmware Rule: 1) If any of C1CA/C1CB/C1CC can be 1 (statically or dynamically), ENABLED must be 1. 2) If statically closing (using CLOSED setting) any of C1CA/C1CB/C2CC, ENABLE must be set to 1 in a previous bus access to ensure break-before-make. When re-opening from static CLOSED, C1CA/C1CB/C1CC must be opened in a previous bus access before clearing ENABLE to 0. This is not required for dynamic programming options since e.g. PH0 is not active when these registers are programmed. 3) In any use case where C1CA/C1CB/C1CC are required to be set CLOSED via autonomous scanning, rule (2) cannot be observed. Example use case below**. In this scenario to get the desired effect, the options are to either: a) Dedicate a specific CSW sensor for this purpose, follow rule (2) and do not change the settings autonomously for this sensor. b) Use unused Cmod switches (e.g. if Cmod1/2 are being used, use the switches for Cmod3/4). ** Any use case where a csdbusa/b/c is not used. For example FW CSX wherein csdbusc not used; then csdbusc is statically connected to vssa_sc (C1CG=CLOSED, ENABLED=1 and C1CC=CLOSED).
	DISABLED			0	N/A
	ENABLED			1	N/A

11.4.20 MSC_SW_SEL_CMOD2

Description: CMOD Switch Control 2
Address: 0x40290058
Offset: 0x58
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:4]				SW_C2CA [3:0]			

Bits	15	14	13	12	11	10	9	8
Name	None [15:14]		SW_C2CC [13:12]		SW_C2CB [11:8]			

Bits	23	22	21	20	19	18	17	16
Name	None [23:20]				SW_C2CV [19:16]			

Bits	31	30	29	28	27	26	25	24
Name	ENABLED [31:31]	REF _MODE [30:30]	None [29:28]		SW_C2CG [27:24]			

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:3	SW_C2CA	RW	R	0	CMOD2 to CSD Bus A Switch. During INIT_SHORT (used for full-wave scanning) if CMOD_SEL = CMOD_12, hardware sets C2CA = CLOSED. Firmware Rule: See rule for ENABLED.
	OPEN			0	N/A
	CLOSED			1	N/A
	CHOP_TWO_PHASE			2	chop == 0 ? ph0 : ph1
	CHOP_FOUR_PHASE			3	chop == 0 ? ph1 : ph3
	CHOP_MPSC_D			4	chop == 0 ? ph3 : ph1
	CHOP_MPRX			5	chop == 0 ? ph1 : ph0
	PH1			6	N/A
	PH3			7	N/A
	CHOP_CLK_BAR			8	chop == 0 ? clk_extfb : clk_extfb_bar
	CHOP_CLK			9	chop == 1 ? clk_extfb : clk_extfb_bar
8:11	SW_C2CB	RW	R	0	CMOD2 to CSD Bus B Switch. Firmware Rule: See rule for ENABLED.
	OPEN			0	N/A
	CLOSED			1	N/A
	CHOP_TWO_PHASE			2	chop == 0 ? ph1 : ph0
	CHOP_FOUR_PHASE			3	chop == 0 ? ph3 : ph1
	CHOP_MPSC_D			4	chop == 0 ? ph1 : ph3
	CHOP_MPRX			5	chop == 0 ? ph0 : ph1
	PH0			6	N/A
	PH2			7	N/A
	CHOP_CLK_BAR			8	chop == 0 ? clk_extfb : clk_extfb_bar
	CHOP_CLK			9	chop == 1 ? clk_extfb : clk_extfb_bar

Bits	Name	SW	HW	Default or Enum	Description
12:13	SW_C2CC	RW	R	0	CMOD2 to CSD Bus C Switch. Firmware Rule: See rule for ENABLED.
	OPEN			0	N/A
	CLOSED			1	N/A
	PH1_OR_PH3			2	N/A
16:19	SW_C2CV	RW	R	0	CMOD2 to vdda_q Switch. Firmware Rule: Do not program C2CV and C2CG such that they are closed simultaneously.
	OPEN			0	N/A
	CLOSED			1	N/A
	PH0			2	N/A
	PH1			3	N/A
	PH2			4	N/A
	PH0_OR_PH1			5	N/A
	PH0X			6	N/A
	PH1X			7	N/A
	PH0_OR_FS2PH0_AND_PH1_OR_PH3			8	ph0 || [Fs2_ph0 && (ph1 || ph3)]
	CLK			9	clk_extfb
24:27	SW_C2CG	RW	R	0	CMOD2 to vssa_q Switch. Firmware Rule: Do not program C2CV and C2CG such that they are closed simultaneously.
	OPEN			0	N/A
	CLOSED			1	N/A
	PH0			2	N/A
	PH1			3	N/A
	PH2			4	N/A
	PH1_OR_PH3			5	N/A
	PH2_OR_PH3			6	N/A
	PH0X			7	N/A
	PH1X			8	N/A
	PH2_OR_FS2PH1_AND_PH1_OR_PH3			9	ph2 || [Fs2_ph1 && (ph1 || ph3)]
	CLK_BAR			10	clk_extfb_bar
30	REF_MODE	RW	R	0	CMOD2 is used as a reference in scenario where CMOD can be re-purposed when not used as a CMOD.
	DISABLED			0	N/A
	ENABLED			1	N/A

Bits	Name	SW	HW	Default or Enum	Description
31	ENABLED	RW	R	0	CMOD2 enable. Firmware Rule: 1) If any of C2CA/C2CB/C2CC can be 1 (statically or dynamically), ENABLED must be 1. 2) If statically closing (using CLOSED setting) any of C2CA/C2CB/C2CC, ENABLE must be set to 1 in a previous bus access to ensure break-before-make. When re-opening from static CLOSED, C2CA/C2CB/C2CC must be opened in a previous bus access before clearing ENABLE to 0. This is not required for dynamic programming options since e.g. PH0 is not active when these registers are programmed. 3) In any use case where C2CA/C2CB/C2CC are required to be set CLOSED via autonomous scanning, rule (2) cannot be observed. Example use case below**. In this scenario to get the desired effect, the options are to either: a) Dedicate a specific CSW sensor for this purpose, follow rule (2) and do not change the settings autonomously for this sensor. b) Use unused Cmod switches (e.g. if Cmod1/2 are being used, use the switches for Cmod3/4). ** Any use case where a csdbusa/b/c is not used. For example FW CSX wherein csdbusc not used; then csdbusc is statically connected to vssa_sc (C2CG=CLOSED, ENABLED=1 and C2CC=CLOSED).
	DISABLED			0	N/A
	ENABLED			1	N/A

11.4.21 MSC_SW_SEL_CMOD3

Description: CMOD Switch Control 3
Address: 0x4029005C
Offset: 0x5C
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:4]				SW_C3CA [3:0]			

Bits	15	14	13	12	11	10	9	8
Name	None [15:14]		SW_C3CC [13:12]		SW_C3CB [11:8]			

Bits	23	22	21	20	19	18	17	16
Name	None [23:20]				SW_C3CV [19:16]			

Bits	31	30	29	28	27	26	25	24
Name	ENABLED [31:31]	REF _MODE [30:30]	None [29:28]		SW_C3CG [27:24]			

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:3	SW_C3CA	RW	R	0	CMOD3 to CSD Bus A Switch. Firmware Rule: See rule for ENABLED.
	OPEN			0	N/A
	CLOSED			1	N/A
	CHOP_TWO_PHASE			2	chop == 0 ? ph0 : ph1
	CHOP_FOUR_PHASE			3	chop == 0 ? ph1 : ph3
	CHOP_MPSC_D			4	chop == 0 ? ph3 : ph1
	CHOP_MPRX			5	chop == 0 ? ph1 : ph0
	PH1			6	N/A
	PH3			7	N/A
	CHOP_CLK_BAR			8	chop == 0 ? clk_extfb : clk_extfb_bar
	CHOP_CLK			9	chop == 1 ? clk_extfb : clk_extfb_bar
8:11	SW_C3CB	RW	R	0	CMOD3 to CSD Bus B Switch. During INIT_SHORT (used for full-wave scanning) if CMOD_SEL = CMOD_34, hardware sets C3CB = CLOSED. Firmware Rule: See rule for ENABLED.
	OPEN			0	N/A
	CLOSED			1	N/A
	CHOP_TWO_PHASE			2	chop == 0 ? ph1 : ph0
	CHOP_FOUR_PHASE			3	chop == 0 ? ph3 : ph1
	CHOP_MPSC_D			4	chop == 0 ? ph1 : ph3
	CHOP_MPRX			5	chop == 0 ? ph0 : ph1
	PH0			6	N/A
	PH2			7	N/A
	CHOP_CLK_BAR			8	chop == 0 ? clk_extfb : clk_extfb_bar
	CHOP_CLK			9	chop == 1 ? clk_extfb : clk_extfb_bar

Bits	Name	SW	HW	Default or Enum	Description
12:13	SW_C3CC	RW	R	0	CMOD3 to CSD Bus C Switch. Firmware Rule: See rule for ENABLED.
	OPEN			0	N/A
	CLOSED			1	N/A
	PH1_OR_PH3			2	N/A
16:19	SW_C3CV	RW	R	0	CMOD3 to vdda_q Switch. Firmware Rule: Do not program C3CV and C3CG such that they are closed simultaneously.
	OPEN			0	N/A
	CLOSED			1	N/A
	PH0			2	N/A
	PH1			3	N/A
	PH2			4	N/A
	PH0_OR_PH1			5	N/A
	PH0X			6	N/A
	PH1X			7	N/A
	PH0_OR_FS2PH0_AND_PH1_OR_PH3			8	ph0 || [Fs2_ph0 && (ph1 || ph3)]
	CLK			9	clk_extfb
24:27	SW_C3CG	RW	R	0	CMOD3 to vssa_q Switch. Firmware Rule: Do not program C3CV and C3CG such that they are closed simultaneously.
	OPEN			0	N/A
	CLOSED			1	N/A
	PH0			2	N/A
	PH1			3	N/A
	PH2			4	N/A
	PH1_OR_PH3			5	N/A
	PH2_OR_PH3			6	N/A
	PH0X			7	N/A
	PH1X			8	N/A
	PH2_OR_FS2PH1_AND_PH1_OR_PH3			9	ph2 || [Fs2_ph1 && (ph1 || ph3)]
	CLK_BAR			10	clk_extfb_bar
30	REF_MODE	RW	R	0	CMOD3 is used as a reference in scenario where CMOD can be re-purposed when not used as a CMOD.
	DISABLED			0	N/A
	ENABLED			1	N/A

Bits	Name	SW	HW	Default or Enum	Description
31	ENABLED	RW	R	0	CMOD3 enable. Firmware Rule: 1) If any of C3CA/C3CB/C3CC can be 1 (statically or dynamically), ENABLED must be 1. 2) If statically closing (using CLOSED setting) any of C3CA/C3CB/C3CC, ENABLE must be set to 1 in a previous bus access to ensure break-before-make. When re-opening from static CLOSED, C3CA/C3CB/C3CC must be opened in a previous bus access before clearing ENABLE to 0. This is not required for dynamic programming options since e.g. PH0 is not active when these registers are programmed. 3) In any use case where C3CA/C3CB/C3CC are required to be set CLOSED via autonomous scanning, rule (2) cannot be observed. Example use case below**. In this scenario to get the desired effect, the options are to either: a) Dedicate a specific CSW sensor for this purpose, follow rule (2) and do not change the settings autonomously for this sensor. b) Use unused Cmod switches (e.g. if Cmod1/2 are being used, use the switches for Cmod3/4). ** Any use case where a csdbusa/b/c is not used. For example FW CSX wherein csdbusc not used; then csdbusc is statically connected to vssa_sc (C3CG=CLOSED, ENABLED=1 and C3CC=CLOSED).
	DISABLED			0	N/A
	ENABLED			1	N/A

11.4.22 MSC_SW_SEL_CMOD4

Description: CMOD Switch Control 4
Address: 0x40290060
Offset: 0x60
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:4]				SW_C4CA [3:0]			

Bits	15	14	13	12	11	10	9	8
Name	None [15:14]		SW_C4CC [13:12]		SW_C4CB [11:8]			

Bits	23	22	21	20	19	18	17	16
Name	None [23:20]				SW_C4CV [19:16]			

Bits	31	30	29	28	27	26	25	24
Name	ENABLED [31:31]	REF _MODE [30:30]	None [29:28]		SW_C4CG [27:24]			

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:3	SW_C4CA	RW	R	0	CMOD4 to CSD Bus A Switch. Firmware Rule: See rule for ENABLED.
	OPEN			0	N/A
	CLOSED			1	N/A
	CHOP_TWO_PHASE			2	chop == 0 ? ph0 : ph1
	CHOP_FOUR_PHASE			3	chop == 0 ? ph1 : ph3
	CHOP_MPSC_D			4	chop == 0 ? ph3 : ph1
	CHOP_MPRX			5	chop == 0 ? ph1 : ph0
	PH1			6	N/A
	PH3			7	N/A
	CHOP_CLK_BAR			8	chop == 0 ? clk_extfb : clk_extfb_bar
	CHOP_CLK			9	chop == 1 ? clk_extfb : clk_extfb_bar
8:11	SW_C4CB	RW	R	0	CMOD4 to CSD Bus B Switch. During INIT_SHORT (used for full-wave scanning) if CMOD_SEL = CMOD_34, hardware sets C4CB = CLOSED. Firmware Rule: See rule for ENABLED.
	OPEN			0	N/A
	CLOSED			1	N/A
	CHOP_TWO_PHASE			2	chop == 0 ? ph1 : ph0
	CHOP_FOUR_PHASE			3	chop == 0 ? ph3 : ph1
	CHOP_MPSC_D			4	chop == 0 ? ph1 : ph3
	CHOP_MPRX			5	chop == 0 ? ph0 : ph1
	PH0			6	N/A
	PH2			7	N/A
	CHOP_CLK_BAR			8	chop == 0 ? clk_extfb : clk_extfb_bar
	CHOP_CLK			9	chop == 1 ? clk_extfb : clk_extfb_bar

Bits	Name	SW	HW	Default or Enum	Description
12:13	SW_C4CC	RW	R	0	CMOD4 to CSD Bus C Switch. Firmware Rule: See rule for ENABLED.
	OPEN			0	N/A
	CLOSED			1	N/A
	PH1_OR_PH3			2	N/A
16:19	SW_C4CV	RW	R	0	CMOD4 to vdda_q Switch. Firmware Rule: Do not program C4CV and C4CG such that they are closed simultaneously.
	OPEN			0	N/A
	CLOSED			1	N/A
	PH0			2	N/A
	PH1			3	N/A
	PH2			4	N/A
	PH0_OR_PH1			5	N/A
	PH0X			6	N/A
	PH1X			7	N/A
	PH0_OR_FS2PH0_AND_PH1_OR_PH3			8	ph0 || [Fs2_ph0 && (ph1 || ph3)]
	CLK			9	clk_extfb
24:27	SW_C4CG	RW	R	0	CMOD4 to vssa_q Switch. Firmware Rule: Do not program C4CV and C4CG such that they are closed simultaneously.
	OPEN			0	N/A
	CLOSED			1	N/A
	PH0			2	N/A
	PH1			3	N/A
	PH2			4	N/A
	PH1_OR_PH3			5	N/A
	PH2_OR_PH3			6	N/A
	PH0X			7	N/A
	PH1X			8	N/A
	PH2_OR_FS2PH1_AND_PH1_OR_PH3			9	ph2 || [Fs2_ph1 && (ph1 || ph3)]
	CLK_BAR			10	clk_extfb_bar
30	REF_MODE	RW	R	0	CMOD4 is used as a reference in scenario where CMOD can be re-purposed when not used as a CMOD.
	DISABLED			0	N/A
	ENABLED			1	N/A

Bits	Name	SW	HW	Default or Enum	Description
31	ENABLED	RW	R	0	CMOD4 enable. Firmware Rule: 1) If any of C4CA/C4CB/C4CC can be 1 (statically or dynamically), ENABLED must be 1. 2) If statically closing (using CLOSED setting) any of C4CA/C4CB/C4CC, ENABLE must be set to 1 in a previous bus access to ensure break-before-make. When re-opening from static CLOSED, C4CA/C4CB/C4CC must be opened in a previous bus access before clearing ENABLE to 0. This is not required for dynamic programming options since e.g. PH0 is not active when these registers are programmed. 3) In any use case where C4CA/C4CB/C4CC are required to be set CLOSED via autonomous scanning, rule (2) cannot be observed. Example use case below**. In this scenario to get the desired effect, the options are to either: a) Dedicate a specific CSW sensor for this purpose, follow rule (2) and do not change the settings autonomously for this sensor. b) Use unused Cmod switches (e.g. if Cmod1/2 are being used, use the switches for Cmod3/4). ** Any use case where a csdbusa/b/c is not used. For example FW CSX wherein csdbusc not used; then csdbusc is statically connected to vssa_sc (C4CG=CLOSED, ENABLED=1 and C4CC=CLOSED).
	DISABLED			0	N/A
	ENABLED			1	N/A

11.4.23 MSC_OBS_CTL

Description: Observability Control
Address: 0x40290070
Offset: 0x70
Retention: Retained
IsDeepSleep: No
Comment: Four observe signals are provided. These may be routed to DDFT, DSI, or HSIOM.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:4]				OBSERVE0 [3:0]			

Bits	15	14	13	12	11	10	9	8
Name	None [15:12]				OBSERVE1 [11:8]			

Bits	23	22	21	20	19	18	17	16
Name	None [23:20]				OBSERVE2 [19:16]			

Bits	31	30	29	28	27	26	25	24
Name	None [31:28]				OBSERVE3 [27:24]			

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:3	OBSERVE0	RW	R	0	Selects the source for observe output signal 0: 0: Fs 1: Comparator Output (direct from hard IP). 2: Comparator Output captured on clk_hf_adv. 3: Comparator Output captured on clk_mod. 4: Current raw counter LSB. 5: Scan Done (hardware set signal for INTR.SCAN) 6: ph0. 7: ph1. 8: ph2. 9: ph3. 10: ph0X 11: ph1X 12-14: Unused (0). 15: Sequencer FSM state bit 0.
	FS			0	N/A
	COMP_OUT			1	N/A
	COMP_OUT_ADV			2	N/A
	COMP_OUT_SYNC			3	N/A
	COUNTER_LSB			4	N/A
	SCAN_DONE			5	N/A
	PH0			6	N/A
	PH1			7	N/A
	PH2			8	N/A
	PH3			9	N/A
	PH0X			10	N/A
	PH1X			11	N/A
	UNUSED_1			12	N/A
	UNUSED_2			13	N/A
	UNUSED_3			14	N/A
	SM_STATE_0			15	N/A

Bits	Name	SW	HW	Default or Enum	Description
8:11	OBSERVE1	RW	R	0	Selects the source for observe output signal 1: 0-14: See OBSERVE0. 15: Sequencer FSM state bit 1.
	FS			0	N/A
	COMP_OUT			1	N/A
	COMP_OUT_ADV			2	N/A
	COMP_OUT_SYNC			3	N/A
	COUNTER_LSB			4	N/A
	SCAN_DONE			5	N/A
	PH0			6	N/A
	PH1			7	N/A
	PH2			8	N/A
	PH3			9	N/A
	PH0X			10	N/A
	PH1X			11	N/A
	UNUSED_1			12	N/A
	UNUSED_2			13	N/A
	UNUSED_3			14	N/A
	SM_STATE_1			15	N/A
16:19	OBSERVE2	RW	R	0	Selects the source for observe output signal 2: 0-14: See OBSERVE0. 15: Sequencer FSM state bit 2.
	FS			0	N/A
	COMP_OUT			1	N/A
	COMP_OUT_ADV			2	N/A
	COMP_OUT_SYNC			3	N/A
	COUNTER_LSB			4	N/A
	SCAN_DONE			5	N/A
	PH0			6	N/A
	PH1			7	N/A
	PH2			8	N/A
	PH3			9	N/A
	PH0X			10	N/A
	PH1X			11	N/A
	UNUSED_1			12	N/A
	UNUSED_2			13	N/A
	UNUSED_3			14	N/A
	SM_STATE_2			15	N/A
24:27	OBSERVE3	RW	R	0	Selects the source for observe output signal 3: 0-14: See OBSERVE0. 15: Sequencer FSM state bit 3.
	FS			0	N/A
	COMP_OUT			1	N/A
	COMP_OUT_ADV			2	N/A
	COMP_OUT_SYNC			3	N/A
	COUNTER_LSB			4	N/A
	SCAN_DONE			5	N/A
	PH0			6	N/A
	PH1			7	N/A
	PH2			8	N/A
	PH3			9	N/A
	PH0X			10	N/A
	PH1X			11	N/A

Bits	Name	SW	HW	Default or Enum	Description
	UNUSED_1			12	N/A
	UNUSED_2			13	N/A
	UNUSED_3			14	N/A
	SM_STATE_3			15	N/A

11.4.24 MSC_STATUS1

Description: General Status Register 1
Address: 0x40290100
Offset: 0x100
Retention: Not Retained
IsDeepSleep: No
Comment: Firmware observability of key nodes in MSCv3
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	RAW_COUNT [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	RAW_COUNT [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	RAW_COUNT_POS [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	RAW_COUNT_POS [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:15	RAW_COUNT	R	W	0	Live current raw counter. For debug/test purposes. In normal operation, Firmware/DMA will typically read results from RESULT_FIFO_RD. Note that in CIC2 mode, this value gets updated at the decimation rate. When the SUB_SAMPLE interrupt is asserted, firmware could read this value before the next SUB_SAMPLE interrupt fires to debug sub-samples if desired.
16:31	RAW_COUNT_POS	R	W	0	Useful for determining component counts for positive and negative charge by subtracting from RAW_COUNT. When PHASE_MODE_SEL = FOUR_PHASE RAW_COUNT_POS: Counts during ph1/ph2 of SUB_CONV. When PHASE_MODE_SEL = TWO_PHASE RAW_COUNT_POS: Counts during ph0 of SUB_CONV. This counter increments whenever the Cref CAPDAC is balancing during the corresponding phases above. Note that digital non-overlap is ignored for the purposes of this count since balancing occurs irrespective of these settings. Hence the 'raw' phases (pre application of any digital non-overlap) are considered as the measurement window for this counter. Applicable for CIC1 and CIC2 mode. In CIC2 mode the count is determined by the value of the input to the first integrator stage (equivalent to CIC1 behaviour).

11.4.25 MSC_STATUS2

Description: General Status Register 2
Address: 0x40290104
Offset: 0x104
Retention: Not Retained
IsDeepSleep: No
Comment: Firmware observability of key nodes in MSCv3
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	DEBUG_CONV_COUNT [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	DEBUG_CONV_COUNT [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:15	DEBUG_CONV_COUNT	R	W	0	Debug raw count for a particular conversion. Enabled only during a specified conversion of a sample (a specific chop phase). Only applicable for CIC1 mode. In CIC2 mode this counter remains zero.

11.4.26 MSC_STATUS3

Description: General Status Register 3
Address: 0x40290108
Offset: 0x108
Retention: Not Retained
IsDeepSleep: No
Comment: Firmware observability of key nodes in MSCv3
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	NUM_SUB_CONVS [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	NUM_SUB_CONVS [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:20]				SEQ_STATE [19:16]			

Bits	31	30	29	28	27	26	25	24
Name	None [31:29]			MSC_CMP_OUT [28:28]	None [27:25]			FS_CLOCK [24:24]

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:15	NUM_SUB_CONVS	R	W	0	Number of sub-conversions remaining while in PRO_DUMMY and SUB_CONV.
16:19	SEQ_STATE	R	W	0	MSC Sequencer FSM state.
	IDLE			0	N/A
	WAIT_DMA_WRITE			1	N/A
	LOAD_CONFIG			2	N/A
	WAIT_SCAN_START			3	N/A
	ASSERT_RDY			4	N/A
	WAIT_CONSENSUS			5	N/A
	INIT_CMOD			6	N/A
	INIT_SHORT			7	N/A
	PRO_OFFSET			8	N/A
	PRO_DUMMY			9	N/A
	PRO_WAIT			10	N/A
	SUB_CONV			11	N/A
	EPILOGUE			12	N/A
	WAIT_DMA_READ_NEW_SAMPLE			13	N/A
	WAIT_DMA_READ_EOF			14	N/A
	POST_SCAN			15	N/A
24	FS_CLOCK	R	W	0	Sense clock Fs control waveform. For debug/test purposes.
28	MSC_CMP_OUT	R	W	0	Output of main sensing comparator (synchronized). For debug/test purposes.

11.4.27 MSC_RESULT_FIFO_STATUS

Description: Result FIFO Status
Address: 0x4029010C
Offset: 0x10C
Retention: Retained
IsDeepSleep: No
Comment: Values are reset on frame start event.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	USED [7:0]							

Bits	15	14	13	12	11	10	9	8
Name							USED [9:8]	

Bits	23	22	21	20	19	18	17	16
Name					WR_PTR [19:16]			

Bits	31	30	29	28	27	26	25	24
Name	FIFO_OVERFLOW [31:31]	FIFO_UNDERFLOW [30:30]	RD_PTR [29:24]					

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:9	USED	R	W	0	Number of used/occupied entries in the result FIFO. When '0', the FIFO is empty.
10:19	WR_PTR	R	W	0	Result FIFO write pointer: FIFO location at which a new data is written by the hardware. Note: This functionality is intended for debugging purposes.
20:29	RD_PTR	R	W	0	Result FIFO read pointer: FIFO location from which data is read via AHB. Note: This functionality is intended for debugging purposes.
30	FIFO_UNDERFLOW	R	W	0	Hardware sets this field to '1', when reading from an empty FIFO (RESULT_FIFO_STATUS.USED is '0').
31	FIFO_OVERFLOW	R	W	0	Set if hardware attempts to write a RAW_COUNT (and associated metrics) to an already full result FIFO.

11.4.28 MSC_RESULT_FIFO_RD

Description: Result FIFO Pointer
Address: 0x40290110
Offset: 0x110
Retention: Not Retained
IsDeepSleep: No
Comment: When the IP is disabled (CTL.ENABLED is '0') or when the FIFO is empty, a read from this register returns '0' (no bus error is generated). This register is SW read-only; a SW write is ignored (no bus error is generated).
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	RAW_COUNT [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	RAW_COUNT [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:23]	RESAMPLE_COUNT [22:20]			None [19:17]			OVERFLOW [16:16]

Bits	31	30	29	28	27	26	25	24
Name	None [31:28]				BAD_CONV_COUNT [27:24]			

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:15	RAW_COUNT	R	W	0	FILTER_MODE = CIC1: Accumulated raw count for a sample. FILTER_MODE = CIC2: Average value of all valid sub-samples over all conversions in a sample. Note that the hardware averaging capabilities are limited. See INTR.CIC2_ERROR - if this interrupt asserts it *may* be possible to firmware back calculate the correct average. See SCAN_CTL1.RAW_COUNT_MODE for overflow behaviour of RAW_COUNT.
16	OVERFLOW	R	W	0	RAW_COUNT overflow.
20:22	RESAMPLE_COUNT	R	W	0	Counter indicating number of attempted re-samples (via NUM_AUTO_RESAMPLE) for this raw count. If RESAMPLE_COUNT = 0 and NUM_AUTO_RESAMPLE > 0, this raw count was obtained from the first sample attempt.

Bits	Name	SW	HW	Default or Enum	Description
24:27	BAD_CONV_COUNT	R	W	0	Counter to indicate whether conversion of a sample is bad at the end of each chop phase. This is true if the comparator has not tripped by the end of EPILOGUE in a chop phase. BAD_CONV_COUNT can have a maximum value of 8 (based on largest legal NUM_CONV). If RESAMPLE_COUNT > 0 and BAD_CONV_COUNT = 0, this indicates that RESAMPLE_COUNT bad samples were encountered before this good sample was obtained. If RESAMPLE_COUNT > 0 and BAD_CONV_COUNT > 0, this indicates that all NUM_AUTO_RESAMPLE attempts have been executed and the final attempt had BAD_CONV_COUNT bad conversions. In this situation RESAMPLE_COUNT should equal NUM_AUTO_RESAMPLE.

11.4.29 MSC_INTR

Description: MSCv3 Interrupt Cause Register
Address: 0x40290170
Offset: 0x170
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:5]			SAMPLE [4:4]	None [3:1]			SUB _SAMPLE [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:13]			INIT [12:12]	None [11:9]			SCAN [8:8]

Bits	23	22	21	20	19	18	17	16
Name	None [23:21]			CIC2 _ERROR [20:20]	None [19:17]			FRAME [16:16]

Bits	31	30	29	28	27	26	25	24
Name	FIFO _OVER FLOW [31:31]	FIFO _UNDE RFLOW [30:30]	None [29:25]					CONFIG _REQ [24:24]

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	SUB_SAMPLE	RW1C	RW1S	0	A valid CIC2 sub-sample is complete. To facilitate firmware averaging of sub-samples. For debug purposes.
4	SAMPLE	RW1C	RW1S	0	A single sample is complete. For debug purposes.
8	SCAN	RW1C	RW1S	0	A single scan is complete.
12	INIT	RW1C	RW1S	0	Coarse initialisation complete. For debug purposes.
16	FRAME	RW1C	RW1S	0	A single frame is complete.

Bits	Name	SW	HW	Default or Enum	Description
20	CIC2_ERROR	RW1C	RW1S	0	CIC2 error detected. This bit is set at the end of a sample if the number of valid CIC2 sub-samples is not one of [1,2,4,8,16]. At the end of a CIC2 sample, RESULT_FIFO_RD.RAW_COUNT contains the average of the valid sub-samples observed during that sample. The average is computed by a power of 2 shift as per below for the number of valid CIC2 samples observed: 0,1 -> no division (not a typical use case since an average of multiple sub-samples is desired) 2 -> divide by 2 3,4 -> divide by 4 5,6,7,8 -> divide by 8 9+ -> divide by 16 The RESULT_FIFO_RD.RAW_COUNT value is only the true average if the number of valid CIC2 sub-samples is [1,2,4,8,16]. However, in the cases of [3.4.5.6.9.10,11,12,13,14,15] firmware can back-calculate the real average from the computed average (RAW_COUNT) and the divisor used to compute that average (1,2,4,8,16 above) as follows assuming the number of valid sub-samples is known: Real_Average = Computed_Average*(Computed_Divider/NumSubSamples) If the number of sub-samples exceeds 16, this cannot be reliably computed due to internal hardware overflows.
24	CONFIG_REQ	RW1C	RW1S	0	Request for scan configuration and scan start. The Sequencer FSM is entering WAIT_SCAN_START when this interrupt is raised. This interrupt can be used in CPU mode in a multi-channel scenario with external frame start to indicate to firmware that it is required to configure the channel and start a scan.
30	FIFO_UNDERFLOW	RW1C	RW1S	0	Result FIFO underflow condition.
31	FIFO_OVERFLOW	RW1C	RW1S	0	Result FIFO overflow condition.

11.4.30 MSC_INTR_SET

Description: MSCv3 Interrupt Set Register
Address: 0x40290174
Offset: 0x174
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:5]			SAMPLE [4:4]	None [3:1]			SUB_SAMPLE [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:13]			INIT [12:12]	None [11:9]			SCAN [8:8]

Bits	23	22	21	20	19	18	17	16
Name	None [23:21]			CIC2_ERROR [20:20]	None [19:17]			FRAME [16:16]

Bits	31	30	29	28	27	26	25	24
Name	FIFO_OVERFLOW [31:31]	FIFO_UNDERFLOW [30:30]	None [29:25]					CONFIG_REQ [24:24]

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	SUB_SAMPLE	RW1S	A	0	Write with '1' to set corresponding bit in interrupt request register (a write of '0' has no effect).
4	SAMPLE	RW1S	A	0	Write with '1' to set corresponding bit in interrupt request register (a write of '0' has no effect).
8	SCAN	RW1S	A	0	Write with '1' to set corresponding bit in interrupt request register (a write of '0' has no effect).
12	INIT	RW1S	A	0	Write with '1' to set corresponding bit in interrupt request register (a write of '0' has no effect).
16	FRAME	RW1S	A	0	Write with '1' to set corresponding bit in interrupt request register (a write of '0' has no effect).
20	CIC2_ERROR	RW1S	A	0	Write with '1' to set corresponding bit in interrupt request register (a write of '0' has no effect).
24	CONFIG_REQ	RW1S	A	0	Write with '1' to set corresponding bit in interrupt request register (a write of '0' has no effect).
30	FIFO_UNDERFLOW	RW1S	A	0	Write with '1' to set corresponding bit in interrupt request register (a write of '0' has no effect).
31	FIFO_OVERFLOW	RW1S	A	0	Write with '1' to set corresponding bit in interrupt request register (a write of '0' has no effect).

11.4.31 MSC_INTR_MASK

Description: MSCv3 Interrupt Mask Register
Address: 0x40290178
Offset: 0x178
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:5]			SAMPLE [4:4]	None [3:1]			SUB_SAMPLE [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:13]			INIT [12:12]	None [11:9]			SCAN [8:8]

Bits	23	22	21	20	19	18	17	16
Name	None [23:21]			CIC2_ERROR [20:20]	None [19:17]			FRAME [16:16]

Bits	31	30	29	28	27	26	25	24
Name	FIFO_OVERFLOW [31:31]	FIFO_UNDERFLOW [30:30]	None [29:25]					CONFIG_REQ [24:24]

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	SUB_SAMPLE	RW	R	0	Mask bit for corresponding bit in interrupt cause register.
4	SAMPLE	RW	R	0	Mask bit for corresponding bit in interrupt cause register.
8	SCAN	RW	R	0	Mask bit for corresponding bit in interrupt cause register.
12	INIT	RW	R	0	Mask bit for corresponding bit in interrupt cause register.
16	FRAME	RW	R	0	Mask bit for corresponding bit in interrupt cause register.
20	CIC2_ERROR	RW	R	0	Mask bit for corresponding bit in interrupt cause register.
24	CONFIG_REQ	RW	R	0	Mask bit for corresponding bit in interrupt cause register.
30	FIFO_UNDERFLOW	RW	R	0	Mask bit for corresponding bit in interrupt cause register.
31	FIFO_OVERFLOW	RW	R	0	Mask bit for corresponding bit in interrupt cause register.

11.4.32 MSC_INTR_MASKED

Description: MSCv3 Interrupt Masked Register
Address: 0x4029017C
Offset: 0x17C
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:5]			SAMPLE [4:4]	None [3:1]			SUB_SAMPLE [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:13]			INIT [12:12]	None [11:9]			SCAN [8:8]

Bits	23	22	21	20	19	18	17	16
Name	None [23:21]			CIC2_ERROR [20:20]	None [19:17]			FRAME [16:16]

Bits	31	30	29	28	27	26	25	24
Name	FIFO_OVERFLOW [31:31]	FIFO_UNDERFLOW [30:30]	None [29:25]					CONFIG_REQ [24:24]

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	SUB_SAMPLE	R	W	0	Logical AND of corresponding INTR and INTR_MASK bits.
4	SAMPLE	R	W	0	Logical AND of corresponding INTR and INTR_MASK bits.
8	SCAN	R	W	0	Logical AND of corresponding INTR and INTR_MASK bits.
12	INIT	R	W	0	Logical AND of corresponding INTR and INTR_MASK bits.
16	FRAME	R	W	0	Logical AND of corresponding INTR and INTR_MASK bits.
20	CIC2_ERROR	R	W	0	Logical AND of corresponding INTR and INTR_MASK bits.
24	CONFIG_REQ	R	W	0	Logical AND of corresponding INTR and INTR_MASK bits.
30	FIFO_UNDERFLOW	R	W	0	Logical AND of corresponding INTR and INTR_MASK bits.
31	FIFO_OVERFLOW	R	W	0	Logical AND of corresponding INTR and INTR_MASK bits.

11.4.33 MSC_FRAME_CMD

Description: Frame Command Register
Address: 0x40290190
Offset: 0x190
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:1]							START_FRAME [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	START_FRAME	RW1S	RW1C	0	Start the MSCv3 sequencer frame process. Note that a rising edge on this bit also creates a 2x cycle clk_msc pulse on the msc_ext_frm_start_out signal. The corresponding msc_ext_frm_start_out_en is controlled by CTL.ENABLED. Sequencer FSM clears this bit on egress from IDLE. If START_FRAME is set by firmware when FSM is not in IDLE, the hardware must hold the bit set to allow for 'pending' frame behaviour. Firmware Rule: Note if FRAME_CMD is used in a multi-channel scenario care must be taken by firmware not to excessively delay FRAME_CMD to each individual channel. If not, a window exists where the first channel that sees FRAME_CMD can reach the WAIT_CONSENSUS state and mistakenly believe all channels are ready for lockstep scanning when the reality is the other channels are still in IDLE and indicating ready because they haven't been initiated yet.

11.4.34 MSC_SNS_STRUCT_CTL

Description: Sensor Struct Control
Address: 0x40290200
Offset: 0x200
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:4]				OFFSET [3:0]			

Bits	15	14	13	12	11	10	9	8
Name	None [15:12]				LENGTH [11:8]			

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:3	OFFSET	RW	RW	0	Starting offset into SNS_* registers of current sensor configuration in local IP storage. Used by LOAD_CONFIG state in Sequencer FSM. Applicable only when CONFIG_NR > 0.
8:11	LENGTH	RW	RW	0	Number of SNS_* registers from OFFSET for current sensor configuration in local IP storage. Used by LOAD_CONFIG state in Sequencer FSM. Applicable only when CONFIG_NR > 0.

11.4.35 MSC_SNS_SW_SEL_CSW_MASK2

Description: Control MUX Function Select Mask 2
Address: 0x4029020C
Offset: 0x20C
Retention: Retained
IsDeepSleep: No
Comment: Used only when > 4 functions needed in a frame.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	FUNC_MASK [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	FUNC_MASK [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	FUNC_MASK [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	FUNC_MASK [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	FUNC_MASK	RW	RW	0	{SNS_SW_SEL_CSW_MASK2.FUNC_MASK[x], SNS_SW_SEL_CSW_MASK1.FUNC_MASK[x], SNS_SW_SEL_CSW_MASK0.FUNC_MASK[x]} used to select appropriate SW_SEL_CSW_FUNC[x] when CSW_FUNC_MODE[x] = 1.

11.4.36 MSC_SNS_SW_SEL_CSW_MASK1

Description: Control MUX Function Select Mask 1
Address: 0x40290210
Offset: 0x210
Retention: Retained
IsDeepSleep: No
Comment: Used only when >2 functions needed in a frame.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	FUNC_MASK [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	FUNC_MASK [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	FUNC_MASK [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	FUNC_MASK [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	FUNC_MASK	RW	RW	0	{SNS_SW_SEL_CSW_MASK2.FUNC_MASK[x], SNS_SW_SEL_CSW_MASK1.FUNC_MASK[x], SNS_SW_SEL_CSW_MASK0.FUNC_MASK[x]} used to select appropriate SW_SEL_CSW_FUNC[x] when CSW_FUNC_MODE[x] = 1.

11.4.37 MSC_SNS_SW_SEL_CSW_MASK0

Description: Control MUX Function Select Mask 0
Address: 0x40290214
Offset: 0x214
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	FUNC_MASK [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	FUNC_MASK [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	FUNC_MASK [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	FUNC_MASK [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	FUNC_MASK	RW	RW	0	{SNS_SW_SEL_CSW_MASK2.FUNC_MASK[x], SNS_SW_SEL_CSW_MASK1.FUNC_MASK[x], SNS_SW_SEL_CSW_MASK0.FUNC_MASK[x]} used to select appropriate SW_SEL_CSW_FUNC[x] when CSW_FUNC_MODE[x] = 1.

11.4.38 MSC_SNS_SCAN_CTL

Description: Sensor Scan Control
Address: 0x40290218
Offset: 0x218
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	NUM_SUB_CONVS [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	NUM_SUB_CONVS [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	COMP_DIV [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	INIT_BYPASS [31:31]	NUM_CONV [30:28]			COMP_DIV [27:24]			

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:15	NUM_SUB_CONVS	RW	RW	0	Number of sub-conversions (minus 1) in a conversion.
16:27	COMP_DIV	RW	RW	0	The ratio (minus 1) of clk_comp::clk_mod. Notes for tuning: Fs = Fmod / Kref Fcomp = Kcomp * Fs MSCv3 MMIO provides: Kref = (SENSE_DIV+1) Fs = Fmod/(SENSE_DIV+1) Fcomp = Fmod / (COMP_DIV+1) Therefore: Kcomp = Fmod/[Fs*(COMP_DIV+1)] Kcomp = (SENSE_DIV+1)/(COMP_DIV+1) It is expected that Kcomp be programmed as an integer. Anything else is considered a mis-programming.
28:30	NUM_CONV	RW	RW	0	Number of conversions (minus 1) per scanned sample. This is required for chopping (chop polarity is updated per conversion). Firmware Rule: If chopping is enabled (NUM_CONV > ONE), then NUM_PRO_WAIT_CYCLES must be >=1 and NUM_PRO_DUMMY_SUB_CONVS must be >=1.
	ONE			0	N/A
	TWO			1	N/A
	FOUR			3	N/A
	EIGHT			7	N/A
31	INIT_BYPASS	RW	RW	0	Coarse initialisation bypass control. Applies to CMOD_SEL selected Cmod.

Bits	Name	SW	HW	Default or Enum	Description
	DISABLED			0	N/A
	ENABLED			1	N/A

11.4.39 MSC_SNS_CDAC_CTL

Description: Sensor CAPDAC Control
Address: 0x4029021C
Offset: 0x21C
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	SEL_RE [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	SEL_CO [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	FL_EN [23:23]	CLOCK _REF _RATE [22:22]	FINE _MODE [21:21]	SEL_CF [20:16]				

Bits	31	30	29	28	27	26	25	24
Name	None [31:29]			LFSR _SCALE _TYPE_FL [28:28]	None [27:27]	LFSR_SCALE_FL [26:24]		

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:7	SEL_RE	RW	RW	0	Select value for Reference CAPDAC size.
8:15	SEL_CO	RW	RW	0	Select value for Compensation CAPDAC size. Note if SEL_CO = 0 and FINE_MODE != COMPENSATION, then clk_comp is gated during PRO_DUMMY, SUB_CONV and EPILOGUE.
16:20	SEL_CF	RW	RW	0	Select value for Fine CAPDAC size.
21	FINE_MODE	RW	RW	0	Operational mode for Fine CAPDAC
	REFERENCE			0	N/A
	COMPENSATION			1	N/A
22	CLOCK_REF_RATE	RW	RW	0	Used to select clk_mod or clk_mod/2 to as clk_ref. This clock is gated depending on the synchronised comparator to generate the gated feedback clock (clk_reffb) to the Reference CAPDAC. '0': Use clk_mod. '1': Use clk_mod/2.
	CLK_MOD			0	N/A
	HALF_CLK_MOD			1	N/A
23	FL_EN	RW	RW	0	Dither/Flatspot LFSR enable control. '0': Dither/Flatspot LFSR is disabled. LFSR_SCALE_FL, LFSR_SCALE_TYPE_FL and ACTIVATION_MODE and MSB manipulation logic have no effect. The hard IP is presented with the code programmed into SEL_FL. '1': The Dither/Flatspot LFSR is enabled.
	DISABLED			0	N/A
	ENABLED			1	N/A

Bits	Name	SW	HW	Default or Enum	Description

24:26	LFSR_SCALE_FL	RW	RW	0	Shift the magnitude portion of the Flatspot/Dither CAPDAC LFSR output code left or right by LSFR_SCALE_FL bits. Direction of shift controlled by LFSR_SCALE_TYPE_FL.
					
					Note since the magnitude is 7-bits, the maximum shift is 6-bits. The sign bit does not form part of the shift.
					
					Example: 6-bit polynomial (x^6 + x^4 + x^3 + x^2 + 1).
					
					lfsr_fl_out[7] = lfsr_fl[5]; // Sign bit always connected in MSB to HardIP.
					if(LFSR_SCALE_TYPE_FL == LEFT)
					lfsr_out[6:0] = {2'b00,lfsr[4:0]} << LFSR_SCALE_FL; // Scaled 7-bit magnitude.
					else
					lfsr_out[6:0] = {2'b00,lfsr[4:0]} >> LFSR_SCALE_FL; // Scaled 7-bit magnitude.

	MAX			6	N/A
28	LFSR_SCALE_TYPE_FL	RW	RW	0	Flatspot/Dither CAPDAC shift direction.
	RIGHT			0	N/A
	LEFT			1	N/A

11.4.40 MSC_SNS_CTL

Description: Sense Control and Command Register
Address: 0x40290220
Offset: 0x220
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: 0xC000FE00

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	SENSE_MODE_SEL [7:6]		MULTI_CH_MODE [5:4]		None [3:3]	LAST [2:2]	VALID [1:1]	START_SCAN [0:0]

Bits	15	14	13	12	11	10	9	8
Name	DECIM_RATE [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	SENSE_DIV [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	LFSR_BITS [31:30]		LFSR_MODE [29:28]		SENSE_DIV [27:24]			

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	START_SCAN	RW1S	RW1C	0	Start the MSCv3 sequencer scan process. The sequencer will clear this bit when it is done. Depending on the mode the sequencer is done when all NUM_SAMPLES for this scan have been accumulated, or if the sequencer is reset.
1	VALID	RW	RW	0	Indicator of sensor configuration validity.
2	LAST	RW	RW	0	Indicator that current sensor configuration is the last sensor in the frame.
4:5	MULTI_CH_MODE	RW	RW	0	Multi channel mode configuration. Determines whether consensus mechanism is engaged to ensure channels scan in lockstep. '0': Single channel. '1': Wait for external sync (off-chip). '2': Wait for internal sync (on-chip).
	OFF			0	N/A
	EXTERNAL			1	N/A
	INTERNAL			2	N/A
6:7	SENSE_MODE_SEL	RW	RW	0	Sense mode register structure selection. This field allows quick change between registers that influence sense mode. This register selects which structure is currently 'live' and used by the IP. These registers are captured in MODE_STRUCT. The usable values in this register is determined by design time parameter SENSE_MODE_NR.
	SENSE_MODE_0			0	Use MODE_STRUCT[0].
	SENSE_MODE_1			1	Use MODE_STRUCT[1].
	SENSE_MODE_2			2	Use MODE_STRUCT[2].
	SENSE_MODE_3			3	Use MODE_STRUCT[3].

Bits	Name	SW	HW	Default or Enum	Description
8:15	DECIM_RATE	RW	RW	254	Sets the decimation rate for the sinc^2 filter (CIC2). Typically referred to as N. Note N = DECIM_RATE + 1. Only applies when FILTER_CTL.FILTER_MODE = CIC2, and irrelevant for CIC1 mode (no effect in this mode). Maximum value out of CIC2 is N^2 (unsigned input) and +/- N^2 (signed input). Since CIC2 uses a 16-bit pipeline, the maximum range is [0,2^16-1] (unsigned) and [-2^15,2^15-1] (signed). This implies a limitation on maximum usable DECIM_RATE depending on BIT_FORMAT signed/unsigned. BIT_FORMAT = UNSIGNED -> DECIM_RATE(max) = 254 (N = 255). BIT_FORMAT = SIGNED -> DECIM_RATE(max) = 180 (N = 181). The scan time for M-bit scan is 2^M clk_mod cycles. This value is determined by (SENSE_DIV+1)*(NUM_SUB_CONVS+1). Note that the CIC2 filter does not operate in the EPILOGUE state, so NUM_EPI_CYCLES does not feed into the above equation.
	MAX			254	N/A
16:27	SENSE_DIV	RW	RW	0	The length (minus 1) of the sense modulation 'clock' period in clk_mod cycles (frequency = Fs). SENSE_DIV + 1 = sense_ratio. Note this is the base divider, clock dithering may change the actual period length. Firmware Rule: Firmware is responsible for programming a value in this register to ensure correct operation. When LFSR_MODE = DIRECT_CLOCK, in 2-phase mode sense_ratio needs to be >=4 to allow for digital non-overlap. In 4-phase mode, sense_ratio needs to be >=8. If spread spectrum is enabled (LFSR_MODE = SPREAD_SPECTRUM), SENSE_DIV must be programmed large enough to ensure that negative dithering does not cause sense_ratio to become too small. It is possible for SENSE_DIV to be as low as zero though when LFSR_MODE = PRS (if digital non-overlap is disabled). This is because in PRS mode, SENSE_DIV defines the rate at which the LFSR is clocked and the MSB of the LFSR is used to create the phase signals.
28:29	LFSR_MODE	RW	RW	0	Mode for generating the sense clock. '0': Direct Clocking. '1': Spread Spectrum. '2': PRS.
	DIRECT_CLOCK			0	N/A
	SPREAD_SPECTRUM			1	N/A
	PRS			2	N/A

Bits	Name	SW	HW	Default or Enum	Description
30:31	LFSR_BITS	RW	RW	3	Selects the number of LSB bits to use from the LSFR to provide the clock dithering variation on the base period (spread spectrum mode). Caveat make sure that SENSE_DIV > the maximum absolute range (e.g. for 4B SENSE_DIV > 8), otherwise results are undefined.
	2B			0	Use 2 bits: range = [-2,1]
	3B			1	Use 3 bits: range = [-4,3]
	4B			2	Use 4 bits: range = [-8,7]
	5B			3	Use 5 bits: range = [-16,15] (default)

11.4.41 MSC_SW_SEL_CSW

Description: Control Switch MUX Switch Control
Address: 0x40290300
Offset: 0x300
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:4]				SW_SNCA [3:0]			

Bits	15	14	13	12	11	10	9	8
Name	None [15:14]		SW_SNCC [13:12]		SW_SNCB [11:8]			

Bits	23	22	21	20	19	18	17	16
Name	None [23:20]				SW_SNCV [19:16]			

Bits	31	30	29	28	27	26	25	24
Name	ENABLED [31:31]	REF _MODE [30:30]	None [29:28]		SW_SNCG [27:24]			

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:3	SW_SNCA	RW	R	0	Control MUX Sensor N to CSD Bus A Switch. Firmware Rule: See rule for ENABLED.
	OPEN			0	N/A
	CLOSED			1	N/A
	CHOP_TWO_PHASE			2	chop == 0 ? ph0 : ph1
	CHOP_FOUR_PHASE			3	chop == 0 ? ph1 : ph3
	CHOP_MPSC_D			4	chop == 0 ? ph3 : ph1
	CHOP_MPRX			5	chop == 0 ? ph1 : ph0
	PH1			6	N/A
	PH3			7	N/A
	CHOP_CLK_BAR			8	chop == 0 ? clk_extfb : clk_extfb_bar
	CHOP_CLK			9	chop == 1 ? clk_extfb : clk_extfb_bar
8:11	SW_SNCB	RW	R	0	Control MUX Sensor N to CSD Bus B Switch. Firmware Rule: See rule for ENABLED.
	OPEN			0	N/A
	CLOSED			1	N/A
	CHOP_TWO_PHASE			2	chop == 0 ? ph1 : ph0
	CHOP_FOUR_PHASE			3	chop == 0 ? ph3 : ph1
	CHOP_MPSC_D			4	chop == 0 ? ph1 : ph3
	CHOP_MPRX			5	chop == 0 ? ph0 : ph1
	PH0			6	N/A
	PH2			7	N/A
	CHOP_CLK_BAR			8	chop == 0 ? clk_extfb : clk_extfb_bar
	CHOP_CLK			9	chop == 1 ? clk_extfb : clk_extfb_bar
12:13	SW_SNCC	RW	R	0	Control MUX Sensor N to CSD Bus C Switch. Firmware Rule: See rule for ENABLED.
	OPEN			0	N/A

Bits	Name	SW	HW	Default or Enum	Description
	CLOSED			1	N/A
	PH1_OR_PH3			2	N/A
16:19	SW_SNCV	RW	R	0	Control MUX Sensor N to vdda_q Switch. Firmware Rule: Do not program SNCV and SNCG such that they are closed simultaneously.
	OPEN			0	N/A
	CLOSED			1	N/A
	PH0			2	N/A
	PH1			3	N/A
	PH2			4	N/A
	PH0_OR_PH1			5	N/A
	PH0X			6	N/A
	PH1X			7	N/A
	PH0_OR_FS2PH0_AND _PH1_OR_PH3			8	ph0 || [Fs2_ph0 && (ph1 || ph3)]
	CLK			9	clk_extfb
24:27	SW_SNCG	RW	R	0	Control MUX Sensor N to vssa_q Switch. Firmware Rule: Do not program SNCV and SNCG such that they are closed simultaneously.
	OPEN			0	N/A
	CLOSED			1	N/A
	PH0			2	N/A
	PH1			3	N/A
	PH2			4	N/A
	PH1_OR_PH3			5	N/A
	PH2_OR_PH3			6	N/A
	PH0X			7	N/A
	PH1X			8	N/A
	PH2_OR_FS2PH1_AND _PH1_OR_PH3			9	ph2 || [Fs2_ph1 && (ph1 || ph3)]
	CLK_BAR			10	clk_extfb_bar
30	REF_MODE	RW	R	0	Control MUX Sensor N is used as a reference.
	DISABLED			0	N/A
	ENABLED			1	N/A

Bits	Name	SW	HW	Default or Enum	Description
31	ENABLED	RW	R	0	Control MUX Sensor N enable. Firmware Rule: 1) If any of SNCA/SNCB/SNCC can be 1 (statically or dynamically), ENABLED must be 1. 2) If statically closing (using CLOSED setting) any of SNCA/SNCB/SNCC, ENABLE must be set to 1 in a previous bus access to ensure break-before-make. When re-opening from static CLOSED, SNCA/SNCB/SNCC must be opened in a previous bus access before clearing ENABLE to 0. This is not required for dynamic programming options since e.g. PH0 is not active when these registers are programmed. 3) In any use case where SNCA/SNCB/SNCC are required to be set CLOSED via autonomous scanning, rule (2) cannot be observed. Example use case below**. In this scenario to get the desired effect, the options are to either: a) Dedicate a specific CSW sensor for this purpose, follow rule (2) and do not change the settings autonomously for this sensor. b) Use unused Cmod switches (e.g. if Cmod1/2 are being used, use the switches for Cmod3/4). ** Any use case where a csdbusa/b/c is not used. For example FW CSX wherein csdbusc not used; then csdbusc is statically connected to vssa_sc (SNCG=CLOSED, ENABLED=1 and SNCC=CLOSED).
	DISABLED			0	N/A
	ENABLED			1	N/A

11.4.42 MSC_SW_SEL_CSW_FUNC

Description: Control Switch MUX Switch Control Global Functions
Address: 0x40290400
Offset: 0x400
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:4]				SW_SNCA [3:0]			

Bits	15	14	13	12	11	10	9	8
Name	None [15:14]		SW_SNCC [13:12]		SW_SNCB [11:8]			

Bits	23	22	21	20	19	18	17	16
Name	None [23:20]				SW_SNCV [19:16]			

Bits	31	30	29	28	27	26	25	24
Name	ENABLED [31:31]	REF _MODE [30:30]	None [29:28]		SW_SNCG [27:24]			

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:3	SW_SNCA	RW	R	0	Control MUX Sensor to CSD Bus A Switch. Firmware Rule: See corresponding rule in SW_SEL_CSW.
	OPEN			0	N/A
	CLOSED			1	N/A
	CHOP_TWO_PHASE			2	chop == 0 ? ph0 : ph1
	CHOP_FOUR_PHASE			3	chop == 0 ? ph1 : ph3
	CHOP_MPSC_D			4	chop == 0 ? ph3 : ph1
	CHOP_MPRX			5	chop == 0 ? ph1 : ph0
	PH1			6	N/A
	PH3			7	N/A
	CHOP_CLK_BAR			8	chop == 0 ? clk_extfb : clk_extfb_bar
	CHOP_CLK			9	chop == 1 ? clk_extfb : clk_extfb_bar
8:11	SW_SNCB	RW	R	0	Control MUX Sensor to CSD Bus B Switch. Firmware Rule: See corresponding rule in SW_SEL_CSW.
	OPEN			0	N/A
	CLOSED			1	N/A
	CHOP_TWO_PHASE			2	chop == 0 ? ph1 : ph0
	CHOP_FOUR_PHASE			3	chop == 0 ? ph3 : ph1
	CHOP_MPSC_D			4	chop == 0 ? ph1 : ph3
	CHOP_MPRX			5	chop == 0 ? ph0 : ph1
	PH0			6	N/A
	PH2			7	N/A
	CHOP_CLK_BAR			8	chop == 0 ? clk_extfb : clk_extfb_bar
	CHOP_CLK			9	chop == 1 ? clk_extfb : clk_extfb_bar

Bits	Name	SW	HW	Default or Enum	Description
12:13	SW_SNCC	RW	R	0	Control MUX Sensor to CSD Bus C Switch. Firmware Rule: See corresponding rule in SW_SEL_CSW.
	OPEN			0	N/A
	CLOSED			1	N/A
	PH1_OR_PH3			2	N/A
16:19	SW_SNCV	RW	R	0	Control MUX Sensor to vdda_q Switch. Firmware Rule: Do not program SNCV and SNCG such that they are closed simultaneously.
	OPEN			0	N/A
	CLOSED			1	N/A
	PH0			2	N/A
	PH1			3	N/A
	PH2			4	N/A
	PH0_OR_PH1			5	N/A
	PH0X			6	N/A
	PH1X			7	N/A
	PH0_OR_FS2PH0_AND_PH1_OR_PH3			8	ph0 || [Fs2_ph0 && (ph1 || ph3)]
	CLK			9	clk_extfb
24:27	SW_SNCG	RW	R	0	Control MUX Sensor to vssa_q Switch. Firmware Rule: Do not program SNCV and SNCG such that they are closed simultaneously.
	OPEN			0	N/A
	CLOSED			1	N/A
	PH0			2	N/A
	PH1			3	N/A
	PH2			4	N/A
	PH1_OR_PH3			5	N/A
	PH2_OR_PH3			6	N/A
	PH0X			7	N/A
	PH1X			8	N/A
	PH2_OR_FS2PH1_AND_PH1_OR_PH3			9	ph2 || [Fs2_ph1 && (ph1 || ph3)]
	CLK_BAR			10	clk_extfb_bar
30	REF_MODE	RW	R	0	Control MUX Sensor is used as a reference.
	DISABLED			0	N/A
	ENABLED			1	N/A
31	ENABLED	RW	R	0	Control MUX Sensor enable.
	DISABLED			0	N/A
	ENABLED			1	N/A

11.4.43 MSC_SENSOR_DATA

Description: Sensor Configuration Storage
Address: 0x40291000
Offset: 0x1000
Retention: Retained
IsDeepSleep: No
Comment: Not usable for MSCv3 (low power functionality only implemented for MSCv3LP)
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	DATA [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	DATA	RW	RW	0	Local IP storage to support per-sensor configuration for AS-MS mode. Storage requirement in bytes is CONFIG_NR * (number of per sensor registers) * 4. The per sensor registers all have the prefix SNS_*.

11.4.44 MSC_TRIM_CTL

Description: Trim Control
Address: 0x4029FF00
Offset: 0xFF00
Retention: Retained
IsDeepSleep: No
Comment: This register is used to configure the MSCv3 trim settings.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:6]		TRIM_POLARITY [5:5]	TRIM_EN [4:4]	TRIM_IN [3:0]			

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:3	TRIM_IN	RW	R	0	Controls magnitude of comparator offset trim.
4	TRIM_EN	RW	R	0	Enables comparator offset trim.
	DISABLED			0	N/A
	ENABLED			1	N/A
5	TRIM_POLARITY	RW	R	0	Controls polarity of comparator offset trim.

11.4.45 MODE

11.4.45.1 MSC_MODE_SENSE_DUTY_CTL

Description: Sense Clock Duty Cycle Control
Address: 0x40290500
Offset: 0x0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:7]	PH_GAP_2CYCLE_EN [6:6]	PHASE_GAP_FS2_PH1_EN [5:5]	PHASE_GAP_FS2_PH0_EN [4:4]	PHASE_GAP_PH3_EN [3:3]	PHASE_GAP_PH2_EN [2:2]	PHASE_GAP_PH1_EN [1:1]	PHASE_GAP_PH0_EN [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:11]					PHX_GAP_2CYCLE_EN [10:10]	PHASE_GAP_PH1X_EN [9:9]	PHASE_GAP_PH0X_EN [8:8]

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:29]			PHASE_MODE_SEL [28:28]	None [27:25]			PHASE_SHIFT_EN [24:24]

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	PHASE_GAP_PH0_EN	RW	R	0	Decide whether clk_mod cycle non-overlap gap is applied at the end of ph0. PHASE_GAP_PH0_EN = 0 -> No gap. PHASE_GAP_PH0_EN = 1 && PH_GAP_2CYCLE_EN = 0 -> 1x cycle gap. PHASE_GAP_PH0_EN = 1 && PH_GAP_2CYCLE_EN = 1 -> 2x cycle gap. Does not apply to signals controlled by SW_SEL_CSD and SW_SEL_DSI since GPIO has in-built non-overlap circuitry.
	DISABLED			0	N/A
	ENABLED			1	N/A
1	PHASE_GAP_PH1_EN	RW	R	0	Decide whether clk_mod cycle non-overlap gap is applied at the end of ph1. PHASE_GAP_PH1_EN = 0 -> No gap. PHASE_GAP_PH1_EN = 1 && PH_GAP_2CYCLE_EN = 0 -> 1x cycle gap. PHASE_GAP_PH1_EN = 1 && PH_GAP_2CYCLE_EN = 1 -> 2x cycle gap. Does not apply to signals controlled by SW_SEL_CSD and SW_SEL_DSI since GPIO has in-built non-overlap circuitry.

Bits	Name	SW	HW	Default or Enum	Description
	DISABLED			0	N/A
	ENABLED			1	N/A
2	PHASE_GAP_PH2_EN	RW	R	0	Decide whether clk_mod cycle non-overlap gap is applied at the end of ph2. PHASE_GAP_PH2_EN = 0 -> No gap. PHASE_GAP_PH2_EN = 1 && PH_GAP_2CYCLE_EN = 0 -> 1x cycle gap. PHASE_GAP_PH2_EN = 1 && PH_GAP_2CYCLE_EN = 1 -> 2x cycle gap. Does not apply to signals controlled by SW_SEL_CSD and SW_SEL_DSI since GPIO has in-built non-overlap circuitry.
	DISABLED			0	N/A
	ENABLED			1	N/A
3	PHASE_GAP_PH3_EN	RW	R	0	Decide whether clk_mod cycle non-overlap gap is applied at the end of ph3. PHASE_GAP_PH3_EN = 0 -> No gap. PHASE_GAP_PH3_EN = 1 && PH_GAP_2CYCLE_EN = 0 -> 1x cycle gap. PHASE_GAP_PH3_EN = 1 && PH_GAP_2CYCLE_EN = 1 -> 2x cycle gap. Does not apply to signals controlled by SW_SEL_CSD and SW_SEL_DSI since GPIO has in-built non-overlap circuitry.
	DISABLED			0	N/A
	ENABLED			1	N/A
4	PHASE_GAP_FS2_PH0_EN	RW	R	0	Decide whether clk_mod cycle non-overlap gap is applied at the end of Fs2_ph0. PHASE_GAP_FS2_PH0_EN = 0 -> No gap. PHASE_GAP_FS2_PH0_EN = 1 && PH_GAP_2CYCLE_EN = 0 -> 1x cycle gap. PHASE_GAP_FS2_PH0_EN = 1 && PH_GAP_2CYCLE_EN = 1 -> 2x cycle gap. Does not apply to signals controlled by SW_SEL_CSD and SW_SEL_DSI since GPIO has in-built non-overlap circuitry.
	DISABLED			0	N/A
	ENABLED			1	N/A
5	PHASE_GAP_FS2_PH1_EN	RW	R	0	Decide whether clk_mod cycle non-overlap gap is applied at the end of Fs2_ph0. PHASE_GAP_FS2_PH1_EN = 0 -> No gap. PHASE_GAP_FS2_PH1_EN = 1 && PH_GAP_2CYCLE_EN = 0 -> 1x cycle gap. PHASE_GAP_FS2_PH1_EN = 1 && PH_GAP_2CYCLE_EN = 1 -> 2x cycle gap. Does not apply to signals controlled by SW_SEL_CSD and SW_SEL_DSI since GPIO has in-built non-overlap circuitry.
	DISABLED			0	N/A
	ENABLED			1	N/A

Bits	Name	SW	HW	Default or Enum	Description
6	PH_GAP_2CYCLE_EN	RW	R	0	If set, applies a two cycle gap on ph0/ph1/ph2/ph3/Fs2_ph0/Fs2_ph1 if the corresponding PHASE_GAP_*_EN is set.
	ONE_CYCLE			0	N/A
	TWO_CYCLE			1	N/A
8	PHASE_GAP_PH0X_EN	RW	R	0	Decide whether clk_mod cycle non-overlap gap is applied at the end of ph0x. PHASE_GAP_PH0X_EN = 0 -> No gap. PHASE_GAP_PH0X_EN = 1 && PHX_GAP_2CYCLE_EN = 0 -> 1x cycle gap. PHASE_GAP_PH0X_EN = 1 && PHX_GAP_2CYCLE_EN = 1 -> 2x cycle gap. Does not apply to signals controlled by SW_SEL_CSD and SW_SEL_DSI since GPIO has in-built non-overlap circuitry.
	DISABLED			0	N/A
	ENABLED			1	N/A
9	PHASE_GAP_PH1X_EN	RW	R	0	Decide whether clk_mod cycle non-overlap gap is applied at the end of ph1x. PHASE_GAP_PH1X_EN = 0 -> No gap. PHASE_GAP_PH1X_EN = 1 && PHX_GAP_2CYCLE_EN = 0 -> 1x cycle gap. PHASE_GAP_PH1X_EN = 1 && PHX_GAP_2CYCLE_EN = 1 -> 2x cycle gap. Does not apply to signals controlled by SW_SEL_CSD and SW_SEL_DSI since GPIO has in-built non-overlap circuitry.
	DISABLED			0	N/A
	ENABLED			1	N/A
10	PHX_GAP_2CYCLE_EN	RW	R	0	If set, applies a two cycle gap on ph0X/ph1X if the corresponding PHASE_GAP_*_EN is set.
	ONE_CYCLE			0	N/A
	TWO_CYCLE			1	N/A
24	PHASE_SHIFT_EN	RW	R	0	Enable phase shift logic that generates the Ph0X and Ph1X waveforms. Used for inductive and impedance sensing. If enabled, PHASE_SHIFT_CYCLES must be > 0.
	DISABLED			0	N/A
	ENABLED			1	N/A
28	PHASE_MODE_SEL	RW	R	0	Select 4-phase or 2-phase mode. '0': Four phase. '1': Two phase.
	FOUR_PHASE			0	N/A
	TWO_PHASE			1	N/A

11.4.45.2 MSC_MODE_SW_SEL_CDAC_FL

Description: Flatspot/Dither CAPDAC Switch Control
Address: 0x40290504
Offset: 0x4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:7]	SW_FLCB [6:4]			None [3:3]	SW_FLTCA [2:0]		

Bits	15	14	13	12	11	10	9	8
Name	None [15:15]	SW_FLTG [14:12]			None [11:10]		SW_FLTV [9:8]	

Bits	23	22	21	20	19	18	17	16
Name	None [23:23]	SW_FLBG [22:20]			None [19:19]	SW_FLBV [18:16]		

Bits	31	30	29	28	27	26	25	24
Name	ACTIVATION_MODE [31:31]	None [30:24]						

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:2	SW_FLTCA	RW	R	0	Flatspot/Dither CAPDAC top plate to CSD Bus A Switch
	OPEN			0	N/A
	CLOSED			1	N/A
	CHOP_PH1_4PHASE			2	chop == 1 ? ph1 : ph3
	CHOP_PH3			3	chop == 1 ? ph3 : ph1
	CHOP_PH0			4	chop == 1 ? ph0 : ph1
	CHOP_PH1_2PHASE			5	chop == 1 ? ph1 : ph0
4:6	SW_FLCB	RW	R	0	Flatspot/Dither CAPDAC to CSD Bus B Switch
	OPEN			0	N/A
	CLOSED			1	N/A
	CHOP_PH1_4PHASE			2	chop == 1 ? ph1 : ph3
	CHOP_PH3			3	chop == 1 ? ph3 : ph1
	CHOP_PH0			4	chop == 1 ? ph0 : ph1
	CHOP_PH1_2PHASE			5	chop == 1 ? ph1 : ph0
8:9	SW_FLTV	RW	R	0	Flatspot/Dither CAPDAC top plate to vdda_q Switch. Firmware Rule: Do not program FLTV and FLTG such that they are closed simultaneously.
	OPEN			0	N/A
	CLOSED			1	N/A
	PH0			2	DFT mode
	PH2			3	DFT mode
12:14	SW_FLTG	RW	R	0	Flatspot/Dither CAPDAC top plate to vssa_q Switch. Firmware Rule: Do not program FLTV and FLTG such that they are closed simultaneously.
	OPEN			0	N/A

Bits	Name	SW	HW	Default or Enum	Description
	CLOSED			1	N/A
	PH1			2	N/A
	PH0_OR_PH2			3	N/A
	PH0			4	DFT mode
	PH2			5	DFT mode
16:18	SW_FLBV	RW	R	0	Flatspot/Dither CAPDAC bottom plate to vdda_q Switch. Firmware Rule: Do not program FLBV and FLBG such that they are closed simultaneously. Notes: 1) Equations below describe 'msb' term as raw LFSR output, and take into account overriding as defined by ACTIVATION_MODE. 2) Glitches on FLBV or FLBG during ph0 or ph2 are acceptable (if msb toggles at this time) as the FLTCA and FLCB switches are open during this phase so there is no connection into the comparator or the Cmod caps.
	OPEN			0	N/A
	CLOSED			1	N/A
	PH0X			2	N/A
	PH1X			3	N/A
	PRECHARGE_2_PH			4	[(msb^ph1)^(ph0||ph1)] & [ph0||ph1]
	PRECHARGE_2_PH_BAR			5	(![(msb^ph1)^(ph0||ph1)]) & [ph0||ph1]
	PRECHARGE_4_PH			6	[(msb^(ph2||ph3))^(ph0||ph2)] & [ph0||ph1||ph2||ph3]
	PRECHARGE_4_PH_BAR			7	(![(msb^(ph2||ph3))^(ph0||ph2)]) & [ph0||ph1||ph2||ph3]
20:22	SW_FLBG	RW	R	0	Flatspot/Dither CAPDAC bottom plate to vssa_q Switch. Firmware Rule: Do not program FLBV and FLBG such that they are closed simultaneously. Notes: 1) Equations below describe 'msb' term as raw LFSR output, and take into account overriding as defined by ACTIVATION_MODE. 2) Glitches on FLBV or FLBG during ph0 or ph2 are acceptable (if msb toggles at this time) as the FLTCA and FLCB switches are open during this phase so there is no connection into the comparator or the Cmod caps.
	OPEN			0	N/A
	CLOSED			1	N/A
	PH0X			2	N/A
	PH1X			3	N/A
	PRECHARGE_2_PH			4	[(msb^ph1)^(ph0||ph1)] & [ph0||ph1]
	PRECHARGE_2_PH_BAR			5	(![(msb^ph1)^(ph0||ph1)]) & [ph0||ph1]
	PRECHARGE_4_PH			6	[(msb^(ph2||ph3))^(ph0||ph2)] & [ph0||ph1||ph2||ph3]
	PRECHARGE_4_PH_BAR			7	(![(msb^(ph2||ph3))^(ph0||ph2)]) & [ph0||ph1||ph2||ph3]

Bits	Name	SW	HW	Default or Enum	Description
31	ACTIVATION_MODE	RW	R	0	Activation event for Dither/Flatspot LFSR. '0': Clock LFSR on ph0. '1': Clock LFSR on ph0 or ph2. Notes: PH0 activation can be used in both 2 and 4 phase mode (PHASE_MODE_SEL). PH0_OR_PH2 activation can be used in 4 phase mode only (PHASE_MODE_SEL). In PH0 activation mode, the LFSR clocks on ph0 only. However hardware autonomously intervenes by processing the LFSR MSB before routing to the HardIP as follows during any given sense period: PHASE_MODE_SEL = TWO_PHASE: Invert LFSR MSB on ph1 rising edge. PHASE_MODE_SEL = FOUR_PHASE: Invert LFSR MSB on ph2 rising edge.
	PH0			0	N/A
	PH0_OR_PH2			1	N/A

11.4.45.3 MSC_MODE_SW_SEL_TOP

Description: Top Level Switch Control
Address: 0x40290508
Offset: 0x8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:7]	MBCC [6:6]	None [5:5]	CBCC [4:4]	None [3:3]	CACC [2:2]	None [1:1]	CACB [0:0]

Bits	15	14	13	12	11	10	9	8
Name	AYB_EN [15:15]	AYB_CTL [14:12]			AYA_EN [11:11]	AYA_CTL [10:8]		

Bits	23	22	21	20	19	18	17	16
Name	SHV [23:20]				SOSH [19:18]		BYB [17:16]	

Bits	31	30	29	28	27	26	25	24
Name	MBF [31:31]	RMF [30:30]	BGRF [29:29]	None [28:28]	SHG [27:24]			

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	CACB	RW	R	0	CSD Bus A to CSD Bus B Switch. Note that hardware overrides MMIO setting for CACB and sets it CLOSED during the INIT_SHORT state if using GPIO sensors (SW_DSI_CMOD != OPEN || SW_DSI_CSHTANK != OPEN || AYA_EN == CLOSED || AYB_EN == CLOSED).
	OPEN			0	N/A
	CLOSED			1	N/A
2	CACC	RW	R	0	CSD Bus A to CSD Bus C Switch
	OPEN			0	N/A
	CLOSED			1	N/A
4	CBCC	RW	R	0	CSD Bus B to CSD Bus C Switch
	OPEN			0	N/A
	CLOSED			1	N/A
6	MBCC	RW	R	0	AMUXBUSB to CSD Bus C Switch
	OPEN			0	N/A
	CLOSED			1	N/A
8:10	AYA_CTL	RW	R	0	AMUXBUS A to CSD Bus A Switch. Controls second part of AYA switch (AYA_EN<1> on hardIP). Alternative to using dsi_cmod in GPIO mode. Note that hardware overrides MMIO setting for AYA and sets it CLOSED during the INIT_SHORT state if using GPIO sensors (SW_DSI_CMOD != OPEN || SW_DSI_CSHTANK != OPEN || AYA_EN == CLOSED || AYB_EN == CLOSED). This register is wired to the hard IP directly (no MUX required in soft IP).
	OPEN			0	Opens second part of AYA switch. Enables isolation on AYA if AYA_EN is also OPEN_ISOLATED.
	CLOSED			1	N/A

Bits	Name	SW	HW	Default or Enum	Description
	CHOP_TWO_PHASE			2	chop == 0 ? ph0 : ph1
	CHOP_FOUR_PHASE			3	chop == 0 ? ph1 : ph3
	CHOP_MPSC_D			4	chop == 0 ? ph3 : ph1
	CHOP_MPRX			5	chop == 0 ? ph1 : ph0
	PH0			6	N/A
	PH2			7	N/A
11	AYA_EN	RW	R	0	AMUXBUS A to CSD Bus A Switch. Controls the first part of AYA switch (AYA_EN<0> on the hardIP). This register is wired to the hard IP directly (no MUX required in soft IP).
	OPEN_ISOLATED			0	Opens first part of AYA switch. Enables isolation on AYA if AYA_CTL is also OPEN.
	CLOSED			1	Closes first part of AYA switch and disables isolation.
12:14	AYB_CTL	RW	R	0	AMUXBUS A to CSD Bus B Switch. Controls second part of AYB switch (AYB_EN<1> on hardIP). Alternative to using dsi_csh_tank in GPIO mode.
	OPEN			0	Opens second part of AYB switch. Enables isolation on AYB if AYB_EN is also OPEN_ISOLATED.
	CLOSED			1	N/A
	CHOP_TWO_PHASE			2	chop == 0 ? ph1 : ph0
	CHOP_FOUR_PHASE			3	chop == 0 ? ph3 : ph1
	CHOP_MPSC_D			4	chop == 0 ? ph1 : ph3
	CHOP_MPRX			5	chop == 0 ? ph0 : ph1
	PH0			6	N/A
	PH2			7	N/A
15	AYB_EN	RW	R	0	AMUXBUS A to CSD Bus B Switch. Controls first part of AYB switch (AYB_EN<0> on the hardIP). This register is wired to the hard IP directly (no MUX required in soft IP).
	OPEN_ISOLATED			0	Opens first part of AYB switch. Enables isolation on AYB if AYB_CTL is also OPEN.
	CLOSED			1	Closes first part of AYB switch and disables isolation.
16:17	BYB	RW	R	0	AMUXBUS B to CSD Bus B Switch. This register is wired to the hard IP directly (no MUX required in soft IP).
	OPEN_ISOLATED			0	sel = 00
	OPEN_NON_ISOLATED_CSDBUS			1	sel = 01
	OPEN_NON_ISOLATED_AMUXBUS			2	sel = 10
	CLOSED			3	sel = 11
18:19	SOSH	RW	R	0	COAX Shield to Shield Buffer Output Switch
	OPEN			0	N/A
	CLOSED			1	N/A
	PH1_OR_PH3			2	N/A
20:23	SHV	RW	R	0	COAX Shield to vdda_q Switch
	OPEN			0	N/A
	CLOSED			1	N/A
	PH0			2	N/A
	PH1			3	N/A
	PH2			4	N/A

Bits	Name	SW	HW	Default or Enum	Description
	PH3			5	N/A
	PH0X			6	N/A
	PH1X			7	N/A
	PH0_OR_FS2PH0_AND_PH1_OR_PH3			8	ph0 || [Fs2_ph0 && (ph1 || ph3)]
	PH2_OR_FS2PH1_AND_PH1_OR_PH3			9	ph2 || [Fs2_ph1 && (ph1 || ph3)]
24:27	SHG	RW	R	0	COAX Shield to vssa_q Switch
	OPEN			0	N/A
	CLOSED			1	N/A
	PH0			2	N/A
	PH1			3	N/A
	PH2			4	N/A
	PH3			5	N/A
	PH0X			6	N/A
	PH1X			7	N/A
	PH0_OR_FS2PH0_AND_PH1_OR_PH3			8	ph0 || [Fs2_ph0 && (ph1 || ph3)]
	PH2_OR_FS2PH1_AND_PH1_OR_PH3			9	ph2 || [Fs2_ph1 && (ph1 || ph3)]
29	BGRF	RW	R	0	Bandgap Reference to Filter Switch
	OPEN			0	N/A
	CLOSED			1	N/A
30	RMF	RW	R	0	Ratiometric Reference to Filter Switch
	OPEN			0	N/A
	CLOSED			1	N/A
31	MBF	RW	R	0	AMUXBUSB to Filter Switch
	OPEN			0	N/A
	CLOSED			1	N/A

11.4.45.4 MSC_MODE_SW_SEL_COMP

Description: MSC Comparator Switch Control
Address: 0x4029050C
Offset: 0xC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:7]	CPCA [6:6]	None [5:5]	CPMA [4:4]	None [3:3]	CPCS3 [2:2]	None [1:1]	CPCS1 [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:15]	CMCS2 [14:14]	None [13:13]	CPF [12:12]	None [11:11]	CMCB [10:10]	None [9:9]	CPCB [8:8]

Bits	23	22	21	20	19	18	17	16
Name	None [23:23]	CMF [22:22]	None [21:21]	CMG [20:20]	None [19:19]	CMV [18:18]	None [17:17]	CMCS4 [16:16]

Bits	31	30	29	28	27	26	25	24
Name	HALF_WAVE_EN [31:31]	None [30:24]						

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	CPCS1	RW	R	0	Comparator Plus Terminal to CMOD1 Sense Switch
	OPEN			0	N/A
	CLOSED			1	N/A
2	CPCS3	RW	R	0	Comparator Plus Terminal to CMOD3 Sense Switch
	OPEN			0	N/A
	CLOSED			1	N/A
4	CPMA	RW	R	0	Comparator Plus Terminal to AMUXBUSA Switch
	OPEN			0	N/A
	CLOSED			1	N/A
6	CPCA	RW	R	0	Comparator Plus Terminal to CSD Bus A Switch
	OPEN			0	N/A
	CLOSED			1	N/A
8	CPCB	RW	R	0	Comparator Plus Terminal to CSD Bus B Switch
	OPEN			0	N/A
	CLOSED			1	N/A
10	CMCB	RW	R	0	Comparator Minus Terminal to CSD Bus B Switch
	OPEN			0	N/A
	CLOSED			1	N/A
12	CPF	RW	R	0	Comparator Plus Terminal to Reference Filter Switch
	OPEN			0	N/A
	CLOSED			1	N/A
14	CMCS2	RW	R	0	Comparator Minus Terminal to CMOD2 Sense Switch
	OPEN			0	N/A
	CLOSED			1	N/A
16	CMCS4	RW	R	0	Comparator Minus Terminal to CMOD4 Sense Switch
	OPEN			0	N/A

Bits	Name	SW	HW	Default or Enum	Description
	CLOSED			1	N/A
18	CMV	RW	R	0	Comparator Minus Terminal to vdda_q Switch. Firmware Rule: Do not program CMV and CMG such that they are closed simultaneously.
	OPEN			0	N/A
	CLOSED			1	N/A
20	CMG	RW	R	0	Comparator Minus Terminal to vssa_q Switch. Firmware Rule: Do not program CMV and CMG such that they are closed simultaneously.
	OPEN			0	N/A
	CLOSED			1	N/A
22	CMF	RW	R	0	Comparator Minus Terminal to Reference Filter Switch
	OPEN			0	N/A
	CLOSED			1	N/A
31	HALF_WAVE_EN	RW	R	0	Enables halfwave mode in the comparator where reference is vdda_q. Firmware Rule: When HALF_WAVE_EN = ENABLED, CHOP_POL must be programmed to 1 in the case where INIT_MODE = REFERENCE_VDDA.
	DISABLED			0	N/A
	ENABLED			1	N/A

11.4.45.5 MSC_MODE_SW_SEL_SH

Description: Shielding Switch Control
Address: 0x40290510
Offset: 0x10
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x7000000

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:7]	C3SH [6:6]	None [5:5]	C3SHG [4:4]	None [3:3]	C1SH [2:2]	None [1:1]	C1SHG [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:15]	SPCS3 [14:14]	None [13:13]	SPCS1 [12:12]	None [11:11]	CBSO [10:10]	None [9:9]	SOMB [8:8]

Bits	23	22	21	20	19	18	17	16
Name	None [23:19]					CCSO [18:18]	None [17:17]	FSP [16:16]

Bits	31	30	29	28	27	26	25	24
Name	BUF_EN [31:31]	None [30:28]			BUF_SEL [27:24]			

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	C1SHG	RW	R	0	cmod1_2_sh to vssa Switch
	OPEN			0	N/A
	CLOSED			1	N/A
2	C1SH	RW	R	0	cmod1_2_sh to sh Switch (Drives cmod1_2_sh with shield signal)
	OPEN			0	N/A
	CLOSED			1	N/A
4	C3SHG	RW	R	0	cmod3_4_sh to vssa Switch
	OPEN			0	N/A
	CLOSED			1	N/A
6	C3SH	RW	R	0	cmod3_4_sh to sh Switch (Drives cmod3_4_sh with shield signal)
	OPEN			0	N/A
	CLOSED			1	N/A
8	SOMB	RW	R	0	Shield OpAmp to AMUXBUSB Switch
	OPEN			0	N/A
	CLOSED			1	N/A
10	CBSO	RW	R	0	CSD Bus B to Shield OpAmp Switch
	OPEN			0	N/A
	CLOSED			1	N/A
12	SPCS1	RW	R	0	Shield Positive Terminal to CMOD1 Sense Switch
	OPEN			0	N/A
	CLOSED			1	N/A
14	SPCS3	RW	R	0	Shield Positive Terminal to CMOD3 Sense Switch
	OPEN			0	N/A
	CLOSED			1	N/A
16	FSP	RW	R	0	Reference Filter to Shield Positive Terminal Switch

Bits	Name	SW	HW	Default or Enum	Description
	OPEN			0	N/A
	CLOSED			1	N/A
18	CCSO	RW	R	0	CSD Bus C to Shield OpAmp Switch
	OPEN			0	N/A
	CLOSED			1	N/A
24:27	BUF_SEL	RW	R	7	Selects value of compensation capacitance in shield buffer.
31	BUF_EN	RW	R	0	Enable the shield buffer. '0': Off '1': On
	DISABLED			0	N/A
	ENABLED			1	N/A

12 PASS

Description PASS top-level MMIO (DSABv2, INTR)
Base Address 0x403F0000
Size 0x10000
Slave Num MMIO2

Register Name	Address	Permission	Description
PASS_PASS_CTRL	0x403F0108	FULL	PASS Control

12.1 Register Details

12.1.1 PASS_PASS_CTRL

Description: PASS Control
Address: 0x403F0108
Offset: 0x108
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:2]						PMPCLK _SRC [1:1]	PMPCLK _BYP [0:0]

Bits	15	14	13	12	11	10	9	8
Name	RMB_BITS [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	PMPCLK_BYP	RW	R	0	- 0: Pump clk is clk_hf/2 - 1: Pump clk is selected from PMPCLK_SRC
1	PMPCLK_SRC	RW	R	0	- 0: Pump clk is clk_hf - 1: Pump clk is direct from SRSS
8:15	RMB_BITS	RW	R	0	Risk mitigation bits

13 PERI

Description Peripheral Interconnect
Base Address 0x40010000
Size 0x10000
Slave Num MMIO0

Register Name	Address	Permission	Description
PERI_DIV_CMD	0x40010000	FULL	Divider command register
PERI_PCLK_CTL0	0x40010100	FULL	Programmable clock control register
PERI_PCLK_CTL1	0x40010104	FULL	Programmable clock control register
PERI_PCLK_CTL2	0x40010108	FULL	Programmable clock control register
PERI_PCLK_CTL3	0x4001010C	FULL	Programmable clock control register
PERI_PCLK_CTL4	0x40010110	FULL	Programmable clock control register
PERI_PCLK_CTL5	0x40010114	FULL	Programmable clock control register
PERI_PCLK_CTL6	0x40010118	FULL	Programmable clock control register
PERI_PCLK_CTL7	0x4001011C	FULL	Programmable clock control register
PERI_PCLK_CTL8	0x40010120	FULL	Programmable clock control register
PERI_PCLK_CTL9	0x40010124	FULL	Programmable clock control register
PERI_PCLK_CTL10	0x40010128	FULL	Programmable clock control register
PERI_PCLK_CTL11	0x4001012C	FULL	Programmable clock control register
PERI_PCLK_CTL12	0x40010130	FULL	Programmable clock control register
PERI_PCLK_CTL13	0x40010134	FULL	Programmable clock control register
PERI_PCLK_CTL14	0x40010138	FULL	Programmable clock control register
PERI_PCLK_CTL15	0x4001013C	FULL	Programmable clock control register
PERI_DIV_16_CTL0	0x40010300	FULL	Divider control register (for 16.0 divider)
PERI_DIV_16_CTL1	0x40010304	FULL	Divider control register (for 16.0 divider)
PERI_DIV_16_CTL2	0x40010308	FULL	Divider control register (for 16.0 divider)
PERI_DIV_16_CTL3	0x4001030C	FULL	Divider control register (for 16.0 divider)
PERI_DIV_16_CTL4	0x40010310	FULL	Divider control register (for 16.0 divider)
PERI_DIV_16_CTL5	0x40010314	FULL	Divider control register (for 16.0 divider)
PERI_DIV_16_5_CTL0	0x40010400	FULL	Divider control register (for 16.5 divider)
PERI_DIV_16_5_CTL1	0x40010404	FULL	Divider control register (for 16.5 divider)
PERI_DIV_16_5_CTL2	0x40010408	FULL	Divider control register (for 16.5 divider)
PERI_DIV_16_5_CTL3	0x4001040C	FULL	Divider control register (for 16.5 divider)
PERI_DIV_16_5_CTL4	0x40010410	FULL	Divider control register (for 16.5 divider)
PERI_DIV_16_5_CTL5	0x40010414	FULL	Divider control register (for 16.5 divider)
PERI_TR_CTL	0x40010600	FULL	Trigger control register

13.1 TR_GROUP 0

Register Name	Address	Permission	Description
PERI_TR_GROUP0_TR_OUT_CTL0	0x40012000	FULL	Trigger control register
PERI_TR_GROUP0_TR_OUT_CTL1	0x40012004	FULL	Trigger control register
PERI_TR_GROUP0_TR_OUT_CTL2	0x40012008	FULL	Trigger control register
PERI_TR_GROUP0_TR_OUT_CTL3	0x4001200C	FULL	Trigger control register
PERI_TR_GROUP0_TR_OUT_CTL4	0x40012010	FULL	Trigger control register
PERI_TR_GROUP0_TR_OUT_CTL5	0x40012014	FULL	Trigger control register
PERI_TR_GROUP0_TR_OUT_CTL6	0x40012018	FULL	Trigger control register
PERI_TR_GROUP0_TR_OUT_CTL7	0x4001201C	FULL	Trigger control register

13.2 TR_GROUP 1

Register Name	Address	Permission	Description
PERI_TR_GROUP1_TR_OUT_CTL0	0x40012200	FULL	Trigger control register
PERI_TR_GROUP1_TR_OUT_CTL1	0x40012204	FULL	Trigger control register
PERI_TR_GROUP1_TR_OUT_CTL2	0x40012208	FULL	Trigger control register
PERI_TR_GROUP1_TR_OUT_CTL3	0x4001220C	FULL	Trigger control register
PERI_TR_GROUP1_TR_OUT_CTL4	0x40012210	FULL	Trigger control register
PERI_TR_GROUP1_TR_OUT_CTL5	0x40012214	FULL	Trigger control register
PERI_TR_GROUP1_TR_OUT_CTL6	0x40012218	FULL	Trigger control register
PERI_TR_GROUP1_TR_OUT_CTL7	0x4001221C	FULL	Trigger control register
PERI_TR_GROUP1_TR_OUT_CTL8	0x40012220	FULL	Trigger control register
PERI_TR_GROUP1_TR_OUT_CTL9	0x40012224	FULL	Trigger control register

13.3 TR_GROUP 2

Register Name	Address	Permission	Description
PERI_TR_GROUP2_TR_OUT_CTL	0x40012400	FULL	Trigger control register

13.4 TR_GROUP 3

Register Name	Address	Permission	Description
PERI_TR_GROUP3_TR_OUT_CTL0	0x40012600	FULL	Trigger control register
PERI_TR_GROUP3_TR_OUT_CTL1	0x40012604	FULL	Trigger control register

13.5 TR_GROUP 4

Register Name	Address	Permission	Description
PERI_TR_GROUP4_TR_OUT_CTL0	0x40012800	FULL	Trigger control register
PERI_TR_GROUP4_TR_OUT_CTL1	0x40012804	FULL	Trigger control register

13.6 TR_GROUP 5

Register Name	Address	Permission	Description
PERI_TR_GROUP5_TR_OUT_CTL0	0x40012A00	FULL	Trigger control register
PERI_TR_GROUP5_TR_OUT_CTL1	0x40012A04	FULL	Trigger control register

13.7 Register Details

13.7.1 PERI_DIV_CMD

Description: Divider command register
Address: 0x40010000
Offset: 0x0
Retention: Not Retained
IsDeepSleep: No
Comment: The (PA_SEL_TYPE, PA_SEL_DIV) field pair allows a divider to be phase aligned with another divider. E.g., consider a 48 MHz 'clk_hf', and a need for a 12 MHz divided clock A and a 8 MHz divided clock B. Clock A uses 8.0 integer divider 0 and is created by aligning it to 'clk_hf' ((PA_SEL_TYPE, PA_SEL_DIV) is (3, 63)) and DIV_8_CTL0.INT8_DIV is '4-1'. Clock B uses 8.0 integer divider 1 and is created by aligning it to clock A ((PA_SEL_TYPE, PA_SEL_DIV) is (0, 0)) and DIV_8_CTL1.INT8_DIV is '6-1'. This guarantees that clock B is phase aligned with clock B: as the smallest common multiple of the two clock periods is 12 'clk_hf' cycles, the clocks A and B will be aligned every 12 'clk_hf' cycles. Note: clock B is phase aligned to clock A, but still uses 'clk_hf' as a reference clock for its divider value.
Default: 0xFFFF

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	SEL_TYPE [7:6]		SEL_DIV [5:0]					

Bits	15	14	13	12	11	10	9	8
Name	PA_SEL_TYPE [15:14]		PA_SEL_DIV [13:8]					

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	ENABLE [31:31]	DISABLE [30:30]	None [29:24]					

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:5	SEL_DIV	RW	R	63	(SEL_TYPE, SEL_DIV) specifies the divider on which the command (DISABLE/ENABLE) is performed. If SEL_DIV is '63' and 'SEL_TYPE' is '3' (default/reset value), no divider is specified and no clock signal(s) are generated.
6:7	SEL_TYPE	RW	R	3	Specifies the divider type of the divider on which the command is performed: 0: 8.0 (integer) clock dividers. 1: 16.0 (integer) clock dividers. 2: 16.5 (fractional) clock dividers. 3: 24.5 (fractional) clock dividers.
8:13	PA_SEL_DIV	RW	R	63	(PA_SEL_TYPE, PA_SEL_DIV) specifies the divider to which phase alignment is performed for the clock enable command. Any enabled divider can be used as reference. This allows all dividers to be aligned with each other, even when they are enabled at different times. If PA_SEL_DIV is '63' and 'PA_SEL_TYPE' is '3', 'clk_hf' is used as reference.

Bits	Name	SW	HW	Default or Enum	Description
14:15	PA_SEL_TYPE	RW	R	3	Specifies the divider type of the divider to which phase alignment is performed for the clock enable command: 0: 8.0 (integer) clock dividers. 1: 16.0 (integer) clock dividers. 2: 16.5 (fractional) clock dividers. 3: 24.5 (fractional) clock dividers.
30	DISABLE	RW	RW1C	0	Clock divider disable command (mutually exclusive with ENABLE). SW sets this field to '1' and HW sets this field to '0'. The SEL_DIV and SEL_TYPE fields specify which divider is to be disabled. The HW sets the DISABLE field to '0' immediately and the HW sets the DIV_XXX_CTL.EN field of the divider to '0' immediately.
31	ENABLE	RW	RW1C	0	Clock divider enable command (mutually exclusive with DISABLE). Typically, SW sets this field to '1' to enable a divider and HW sets this field to '0' to indicate that divider enabling has completed. When a divider is enabled, its integer and fractional (if present) counters are initialized to '0'. If a divider is to be re-enabled using different integer and fractional divider values, the SW should follow these steps: 0: Disable the divider using the DIV_CMD.DISABLE field. 1: Configure the divider's DIV_XXX_CTL register. 2: Enable the divider using the DIV_CMD_ENABLE field. The SEL_DIV and SEL_TYPE fields specify which divider is to be enabled. The enabled divider may be phase aligned to either 'clk_hf' (typical usage) or to ANY enabled divider. The PA_SEL_DIV and P_SEL_TYPE fields specify the reference divider. The HW sets the ENABLE field to '0' when the enabling is performed and the HW sets the DIV_XXX_CTL.EN field of the divider to '1' when the enabling is performed. Note that enabling with phase alignment to a low frequency divider takes time. E.g. To align to a divider that generates a clock of 'clk_hf'/n (with n being the integer divider value INT_DIV+1), up to n cycles may be required to perform alignment. Phase alignment to 'clk_hf' takes affect immediately. SW can set this field to '0' during phase alignment to abort the enabling process.

13.7.2 PERI_PCLK_CTL

Description: Programmable clock control register
Address: 0x40010100
Offset: 0x100
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xFF

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	SEL_TYPE [7:6]		SEL_DIV [5:0]					

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:5	SEL_DIV	RW	R	63	Specifies one of the dividers of the divider type specified by SEL_TYPE. If SEL_DIV is '63' and 'SEL_TYPE' is '3' (default/reset value), no divider is specified and no clock control signal(s) are generated. When transitioning a clock between two out of phase dividers, spurious clock control signals may be generated for one 'clk_hf' cycle during this transition. These clock control signals may cause a single clock period that is smaller than any of the two divider periods. To prevent these spurious clock signals, the clock multiplexer can be disconnected (SEL_DIV is '63' and 'SEL_TYPE' is '3') for a transition time that is larger than the smaller of the two divider periods.
6:7	SEL_TYPE	RW	R	3	Specifies divider type: 0: 8.0 (integer) clock dividers. 1: 16.0 (integer) clock dividers. 2: 16.5 (fractional) clock dividers. 3: 24.5 (fractional) clock dividers.

13.7.3 PERI_DIV_16_CTL

Description: Divider control register (for 16.0 divider)
Address: 0x40010300
Offset: 0x300
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:1]							EN [0:0]

Bits	15	14	13	12	11	10	9	8
Name	INT16_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	INT16_DIV [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	EN	R	RW	0	Divider enabled. HW sets this field to '1' as a result of an ENABLE command. HW sets this field to '0' as a result on a DISABLE command. Note that this field is retained. As a result, the divider does NOT have to be re-enabled after transitioning from DeepSleep to Active power mode.
8:23	INT16_DIV	RW	R	0	Integer division by (1+INT16_DIV). Allows for integer divisions in the range [1, 65,536]. Note: this type of divider does NOT allow for a fractional division. For the generation of a divided clock, the integer division range is restricted to [2, 65,536]. For the generation of a 50/50 percent duty cycle digital divided clock, the integer division range is restricted to even numbers in the range [2, 65,536]. The generation of a 50/50 percent duty cycle analog divided clock has no restrictions. Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to '0' when transitioning from DeepSleep to Active power mode.

13.7.4 PERI_DIV_16_5_CTL

Description: Divider control register (for 16.5 divider)
Address: 0x40010400
Offset: 0x400
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	FRAC5_DIV [7:3]					None [2:1]		EN [0:0]

Bits	15	14	13	12	11	10	9	8
Name	INT16_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	INT16_DIV [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	EN	R	RW	0	Divider enabled. HW sets this field to '1' as a result of an ENABLE command. HW sets this field to '0' as a result on a DISABLE command. Note that this field is retained. As a result, the divider does NOT have to be re-enabled after transitioning from DeepSleep to Active power mode.
3:7	FRAC5_DIV	RW	R	0	Fractional division by (FRAC5_DIV/32). Allows for fractional divisions in the range [0, 31/32]. Note that fractional division results in clock jitter as some clock periods may be 1 'clk_hf' cycle longer than other clock periods. Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to '0' when transitioning from DeepSleep to Active power mode.
8:23	INT16_DIV	RW	R	0	Integer division by (1+INT16_DIV). Allows for integer divisions in the range [1, 65,536]. Note: combined with fractional division, this divider type allows for a division in the range [1, 65,536 31/32] in 1/32 increments. For the generation of a divided clock, the division range is restricted to [2, 65,536 31/32]. For the generation of a 50/50 percent duty cycle divided clock, the division range is restricted to [2, 65,536]. Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to '0' when transitioning from DeepSleep to Active power mode.

13.7.5 PERI_TR_CTL

Description: Trigger control register
Address: 0x40010600
Offset: 0x600
Retention: Not Retained
IsDeepSleep: No
Comment: This register provides SW control over trigger activation. This is useful for SW initiated triggers (e.g. DW/DMA transfers) or for debugging purposes. The control enables SW activation of one specific input trigger or output trigger of the trigger multiplexer structure.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:7]	TR_SEL [6:0]						

Bits	15	14	13	12	11	10	9	8
Name	None [15:12]				TR_GROUP [11:8]			

Bits	23	22	21	20	19	18	17	16
Name	TR_COUNT [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	TR_ACT [31:31]	TR_OUT [30:30]	None [29:24]					

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:6	TR_SEL	RW	R	0	Specifies the activated trigger when TR_ACT is '1'. TR_OUT specifies whether the activated trigger is an input trigger or output trigger to the trigger multiplexer. During activation (TR_ACT is '1'), SW should not modify this register field. If the specified trigger is not present, the trigger activation has no effect.
8:11	TR_GROUP	RW	R	0	Specifies the trigger group.
16:23	TR_COUNT	RW	RW	0	Amount of cycles a specific trigger is activated. During activation (TR_ACT is '1'), HW decrements this field to '0' using a cycle counter. During activation, SW should not modify this register field. A value of 255 is a special case: HW does NOT decrement this field to '0' and trigger activation is under direct control of TR_ACT: when TR_ACT is '1' the trigger is activated and when TR_ACT is '0' the trigger is deactivated.
30	TR_OUT	RW	R	0	Specifies whether trigger activation is for a specific input or output trigger of the trigger multiplexer. Activation of a specific input trigger, will result in activation of all output triggers that have the specific input trigger selected through their TR_OUT_CTL.SEL field. Activation of a specific output trigger, will result in activation of the specified TR_SEL output trigger only. '0': TR_SEL selection and trigger activation is for an input trigger to the trigger multiplexer. '1': TR_SEL selection and trigger activation is for an output trigger from the trigger multiplexer.

Bits	Name	SW	HW	Default or Enum	Description
31	TR_ACT	RW	RW1C	0	SW sets this field to '1' to activate (set to '1') a trigger as identified by TR_SEL and TR_OUT for TR_COUNT cycles. HW sets this field to '0' when the cycle counter is decremented to '0'. Note: a TR_COUNT value of 255 is a special case and trigger activation is under direct control of the TR_ACT field (the counter is not decremented). Note: when TR_ACT is '1', SW should not modify the other register fields. SW MUST NOT set TR_ACT bit to '1' while updating the other register bits simultaneously. At first the SW MUST update the other register bits as needed, and then set TR_ACT to '1' with a new register write.'

13.7.6 TR_GROUP

13.7.6.1 PERI_TR_GROUP_TR_OUT_CTL

Description: Trigger control register
Address: 0x40012000
Offset: 0x0
Retention: Retained
IsDeepSleep: No
Comment: This register specifies the input trigger for a specific output trigger in trigger group 0. Note that for SW initiated triggers, SW is responsible for activating the output trigger, rather than relying on a specific HW input trigger. For this reason, input trigger 0 is typically connected to a constant signal level of '0' at chip integration (design decision) and SW initiated output triggers are all connected to input trigger 0 (SW responsibility: TR_OUT_CTL.TR_SEL should be set to '0' to select the constant signal level '0' from chip level). As a result, SW initiated triggers can never be activated by a HW input trigger to the trigger multiplexer.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:5]			SEL [4:0]				

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:4	SEL	RW	R	0	Specifies input trigger. This field is typically set during the setup of a chip use case scenario. Changing this field while activated triggers are present on the input triggers may result in unpredictable behavior. Note that input trigger 0 (default value) is typically connected to a constant signal level of '0', and as a result will not cause HW activation of the output trigger.

14 PRGIO

Description Programmable IO configuration
Base Address 0x40050000
Size 0x1000
Slave Num MMIO0

14.1 PRT 0

Register Name	Address	Permission	Description
PRGIO_PRT0_CTL	0x40050000	FULL	Control register
PRGIO_PRT0_SYNC_CTL	0x40050010	FULL	Synchronization control register
PRGIO_PRT0_LUT_SEL0	0x40050020	FULL	LUT component input selection
PRGIO_PRT0_LUT_SEL1	0x40050024	FULL	LUT component input selection
PRGIO_PRT0_LUT_SEL2	0x40050028	FULL	LUT component input selection
PRGIO_PRT0_LUT_SEL3	0x4005002C	FULL	LUT component input selection
PRGIO_PRT0_LUT_SEL4	0x40050030	FULL	LUT component input selection
PRGIO_PRT0_LUT_SEL5	0x40050034	FULL	LUT component input selection
PRGIO_PRT0_LUT_SEL6	0x40050038	FULL	LUT component input selection
PRGIO_PRT0_LUT_SEL7	0x4005003C	FULL	LUT component input selection
PRGIO_PRT0_LUT_CTL0	0x40050040	FULL	LUT component control register
PRGIO_PRT0_LUT_CTL1	0x40050044	FULL	LUT component control register
PRGIO_PRT0_LUT_CTL2	0x40050048	FULL	LUT component control register
PRGIO_PRT0_LUT_CTL3	0x4005004C	FULL	LUT component control register
PRGIO_PRT0_LUT_CTL4	0x40050050	FULL	LUT component control register
PRGIO_PRT0_LUT_CTL5	0x40050054	FULL	LUT component control register
PRGIO_PRT0_LUT_CTL6	0x40050058	FULL	LUT component control register
PRGIO_PRT0_LUT_CTL7	0x4005005C	FULL	LUT component control register
PRGIO_PRT0_DU_SEL	0x400500C0	FULL	Data unit component input selection
PRGIO_PRT0_DU_CTL	0x400500C4	FULL	Data unit component control register
PRGIO_PRT0_DATA	0x400500F0	FULL	Data register

14.2 PRT 1

Register Name	Address	Permission	Description
PRGIO_PRT1_CTL	0x40050100	FULL	Control register
PRGIO_PRT1_SYNC_CTL	0x40050110	FULL	Synchronization control register
PRGIO_PRT1_LUT_SEL0	0x40050120	FULL	LUT component input selection
PRGIO_PRT1_LUT_SEL1	0x40050124	FULL	LUT component input selection
PRGIO_PRT1_LUT_SEL2	0x40050128	FULL	LUT component input selection
PRGIO_PRT1_LUT_SEL3	0x4005012C	FULL	LUT component input selection
PRGIO_PRT1_LUT_SEL4	0x40050130	FULL	LUT component input selection
PRGIO_PRT1_LUT_SEL5	0x40050134	FULL	LUT component input selection
PRGIO_PRT1_LUT_SEL6	0x40050138	FULL	LUT component input selection
PRGIO_PRT1_LUT_SEL7	0x4005013C	FULL	LUT component input selection
PRGIO_PRT1_LUT_CTL0	0x40050140	FULL	LUT component control register
PRGIO_PRT1_LUT_CTL1	0x40050144	FULL	LUT component control register
PRGIO_PRT1_LUT_CTL2	0x40050148	FULL	LUT component control register
PRGIO_PRT1_LUT_CTL3	0x4005014C	FULL	LUT component control register
PRGIO_PRT1_LUT_CTL4	0x40050150	FULL	LUT component control register
PRGIO_PRT1_LUT_CTL5	0x40050154	FULL	LUT component control register
PRGIO_PRT1_LUT_CTL6	0x40050158	FULL	LUT component control register
PRGIO_PRT1_LUT_CTL7	0x4005015C	FULL	LUT component control register
PRGIO_PRT1_DU_SEL	0x400501C0	FULL	Data unit component input selection
PRGIO_PRT1_DU_CTL	0x400501C4	FULL	Data unit component control register
PRGIO_PRT1_DATA	0x400501F0	FULL	Data register

14.3 Register Details

14.3.1 PRT

14.3.1.1 PRGIO_PRT_CTL

Description: Control register
Address: 0x40050000
Offset: 0x0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x2001400

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	BYPASS [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	None [15:13]			CLOCK_SRC [12:8]				

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	ENABLED [31:31]	None [30:26]					PIPELINE_EN [25:25]	HLD_OVR [24:24]

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:7	BYPASS	RW	R	Undefined	Bypass of the programmable IO, one bit for each IO pin: BYPASS[i] is for IO pin i. When ENABLED is '1', this field is used. When ENABLED is '0', this field is NOT used and PRGIO is always bypassed. '0': No bypass (programmable IO fabric is exposed). '1': Bypass (programmable IO fabric is hidden).

Bits	Name	SW	HW	Default or Enum	Description
8:12	CLOCK_SRC	RW	R	20	Clock ('clk_fabric') and reset ('rst_fabric_n') source selection: '0': io_data_in[0]/'1'. ... '7': io_data_in[7]/'1'. '8': chip_data[0]/'1'. ... '15': chip_data[7]/'1'. '16': clk_prgio/rst_sys_act_n. Used for both Active functionality synchronous logic on 'clk_prgio'. This selection is intended for synchronous operation on a PCLK specified clock frequency ('clock_prgio_en'). Note that the fabric's clocked elements are frequency aligned, but NOT phase aligned to 'clk_sys'. '17': clk_prgio/rst_sys_dpslp_n. Used for both DeepSleep functionality synchronous logic on 'clk_prgio' (note that 'clk_prgio' is NOT available in DeepSleep and Hibernate power modes). This selection is intended for synchronous operation on a PCLK specified clock frequency ('clock_prgio_en'). Note that the fabric's clocked elements are frequency aligned, but NOT phase aligned to 'clk_sys'. '18': clk_prgio/rst_sys_hib_n. Used for both Hibernate functionality synchronous logic on 'clk_prgio' (note that 'clk_prgio' is NOT available in DeepSleep and Hibernate power modes). This selection is intended for synchronous operation on a PCLK specified clock frequency ('clock_prgio_en'). Note that the fabric's clocked elements are frequency aligned, but NOT phase aligned to 'clk_sys'. '19': clk_lf/rst_lf_dpslp_n (note that 'clk_lf' is only available in DeepSleep power mode). This selection is intended for synchronous operation on'clk_lf'. Note that the fabric's clocked elements are frequency aligned, but NOT phase aligned to other 'clk_lf' clocked elements. '20'-'30': Clock source is constant '0'. Any of these clock sources should be selected when the IP is disabled to ensure low power consumption. '31': clk_sys/'1'. This selection is NOT intended for 'clk_sys' operation, but for asynchronous operation: three 'clk_sys' cycles after enabling the IP, the IP is fully functional (reset is de-activated). To be used for asynchronous (clockless) fabric functionality.

Bits	Name	SW	HW	Default or Enum	Description
24	HLD_OVR	RW	R	Undefined	IO cell hold override functionality. In DeepSleep and Hibernate power modes, the HSIOM holds the IO cell output and output enable signals if Active functionality is connected to the IO pads. This is undesirable if the PRGIO is supposed to deliver DeepSleep or Hibernate output functionality on these IO pads. This field is used to control the hold override functionality from the PRGIO: '0': The HSIOM controls the IO cell hold override functionality ('hsiom_hld_ovr'). '1': The PRGIO controls the IO cel hold override functionality: - In bypass mode (ENABLED is '0' or BYPASS[i] is '1'), the HSIOM control is used. - In NON bypass mode (ENABLED is '1' and BYPASS[i] is '0'), the PRGIO sets hold override to 'pwr_hld_ovr_hib' to enable PRGIO functionality in DeepSleep and Hibernate power modes (but disables it in Stop power mode). Note that in Hibernate power mode, the PRGIO should not rely on the state of Active or DeepSleep functionality signals from the HSIOM: these signals are clamped to '0' in Hibernate'
25	PIPELINE_EN	RW	R	1	Enable for pipeline register: '0': Disabled (register is bypassed). '1': Enabled.
31	ENABLED	RW	R	0	Enable for programmable IO. Should only be set to '1' when the programmable IO is completely configured: '0': Disabled (signals are bypassed; behavior as if BYPASS is 0xFF). When disabled, the fabric (data unit and LUTs) reset is activated. If the IP is disabled: - The PIPELINE_EN register field should be set to '1', to ensure low power consumption by preventing combinatorial loops. - The CLOCK_SRC register field should be set to '20'-'30' (clock is constant '0'), to ensure low power consumption. '1': Enabled. Once enabled, it takes 3 'clk_fabric' clock cycles till the fabric reset is de-activated and the fabric becomes fully functional. This ensures that the IO pins' input synchronizer states are flushed when the fabric is fully functional.

14.3.1.2 PRGIO_PRT_SYNC_CTL

Description: Synchronization control register
Address: 0x40050010
Offset: 0x10
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	IO_SYNC_EN [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	CHIP_SYNC_EN [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:7	IO_SYNC_EN	RW	R	Undefined	Synchronization of the IO pin input signals to 'clk_fabric', one bit for each IO pin: IO_SYNC_EN[i] is for IO pin i. '0': No synchronization. '1': Synchronization.
8:15	CHIP_SYNC_EN	RW	R	Undefined	Synchronization of the chip input signals to 'clk_fabric', one bit for each input: CHIP_SYNC_EN[i] is for input i. '0': No synchronization. '1': Synchronization.

14.3.1.3 PRGIO_PRT_LUT_SEL

Description: LUT component input selection
Address: 0x40050020
Offset: 0x20
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:4]				LUT_TR0_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
Name	None [15:12]				LUT_TR1_SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
Name	None [23:20]				LUT_TR2_SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:3	LUT_TR0_SEL	RW	R	Undefined	LUT input signal 'tr0_in' source selection: '0': Data unit output. '1': LUT 1 output. '2': LUT 2 output. '3': LUT 3 output. '4': LUT 4 output. '5': LUT 5 output. '6': LUT 6 output. '7': LUT 7 output. '8': chip_data[0] (for LUTs 0, 1, 2, 3); chip_data[4] (for LUTs 4, 5, 6, 7). '9': chip_data[1] (for LUTs 0, 1, 2, 3); chip_data[5] (for LUTs 4, 5, 6, 7). '10': chip_data[2] (for LUTs 0, 1, 2, 3); chip_data[6] (for LUTs 4, 5, 6, 7). '11': chip_data[3] (for LUTs 0, 1, 2, 3); chip_data[7] (for LUTs 4, 5, 6, 7). '12': io_data_in[0] (for LUTs 0, 1, 2, 3); io_data_in[4] (for LUTs 4, 5, 6, 7). '13': io_data_in[1] (for LUTs 0, 1, 2, 3); io_data_in[5] (for LUTs 4, 5, 6, 7). '14': io_data_in[2] (for LUTs 0, 1, 2, 3); io_data_in[6] (for LUTs 4, 5, 6, 7). '15': io_data_in[3] (for LUTs 0, 1, 2, 3); io_data_in[7] (for LUTs 4, 5, 6, 7).

Bits	Name	SW	HW	Default or Enum	Description
8:11	LUT_TR1_SEL	RW	R	Undefined	LUT input signal 'tr1_in' source selection: '0': LUT 0 output. '1': LUT 1 output. '2': LUT 2 output. '3': LUT 3 output. '4': LUT 4 output. '5': LUT 5 output. '6': LUT 6 output. '7': LUT 7 output. '8': chip_data[0] (for LUTs 0, 1, 2, 3); chip_data[4] (for LUTs 4, 5, 6, 7). '9': chip_data[1] (for LUTs 0, 1, 2, 3); chip_data[5] (for LUTs 4, 5, 6, 7). '10': chip_data[2] (for LUTs 0, 1, 2, 3); chip_data[6] (for LUTs 4, 5, 6, 7). '11': chip_data[3] (for LUTs 0, 1, 2, 3); chip_data[7] (for LUTs 4, 5, 6, 7). '12': io_data_in[0] (for LUTs 0, 1, 2, 3); io_data_in[4] (for LUTs 4, 5, 6, 7). '13': io_data_in[1] (for LUTs 0, 1, 2, 3); io_data_in[5] (for LUTs 4, 5, 6, 7). '14': io_data_in[2] (for LUTs 0, 1, 2, 3); io_data_in[6] (for LUTs 4, 5, 6, 7). '15': io_data_in[3] (for LUTs 0, 1, 2, 3); io_data_in[7] (for LUTs 4, 5, 6, 7).
16:19	LUT_TR2_SEL	RW	R	Undefined	LUT input signal 'tr2_in' source selection. Encoding is the same as for LUT_TR1_SEL.

14.3.1.4 PRGIO_PRT_LUT_CTL

Description: LUT component control register
Address: 0x40050040
Offset: 0x40
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	LUT [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	None [15:10]						LUT_OPC [9:8]	

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:7	LUT	RW	R	Undefined	LUT configuration. Depending on the LUT opcode LUT_OPC, the internal state lut_reg (captured in a flip-flop) and the LUT input signals tr0_in, tr1_in, tr2_in, the LUT configuration is used to determine the LUT output signal and the next sequential state (lut_reg).
8:9	LUT_OPC	RW	R	Undefined	LUT opcode specifies the LUT operation: '0': Combinatoral output, no feedback. tr_out = LUT[{tr2_in, tr1_in, tr0_in}]. '1': Combinatorial output, feedback. tr_out = LUT[{lut_reg, tr1_in, tr0_in}]. On clock: lut_reg <= tr_in2. '2': Sequential output, no feedback. temp = LUT[{tr2_in, tr1_in, tr0_in}]. tr_out = lut_reg. On clock: lut_reg <= temp. '3': Register with asynchronous set and reset. tr_out = lut_reg. enable = (tr2_in ^ LUT[4]) | LUT[5]. set = enable & (tr1_in ^ LUT[2]) & LUT[3]. clr = enable & (tr0_in ^ LUT[0]) & LUT[1]. Asynchronously (no clock required): lut_reg <= if (clr) '0' else if (set) '1'

14.3.1.5 PRGIO_PRT_DU_SEL

Description: Data unit component input selection
Address: 0x400500C0
Offset: 0xC0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:4]				DU_TR0_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
Name	None [15:12]				DU_TR1_SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
Name	None [23:20]				DU_TR2_SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
Name	None [31:30]		DU_DATA1_SEL [29:28]		None [27:26]		DU_DATA0_SEL [25:24]	

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:3	DU_TR0_SEL	RW	R	Undefined	Data unit input signal 'tr0_in' source selection: '0': Constant '0'. '1': Constant '1'. '2': Data unit output. '10-3': LUT 7 - 0 outputs. Otherwise: Undefined.
8:11	DU_TR1_SEL	RW	R	Undefined	Data unit input signal 'tr1_in' source selection. Encoding is the same as for DU_TR0_SEL.
16:19	DU_TR2_SEL	RW	R	Undefined	Data unit input signal 'tr2_in' source selection. Encoding is the same as for DU_TR0_SEL.
24:25	DU_DATA0_SEL	RW	R	Undefined	Data unit input data 'data0_in' source selection: '0': Constant '0'. '1': chip_data[7:0]. '2': io_data_in[7:0]. '3': DATA.DATA MMIO register field.
28:29	DU_DATA1_SEL	RW	R	Undefined	Data unit input data 'data1_in' source selection. Encoding is the same as for DU_DATA0_SEL.

14.3.1.6 PRGIO_PRT_DU_CTL

Description: Data unit component control register
Address: 0x400500C4
Offset: 0xC4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:3]					DU_SIZE [2:0]		

Bits	15	14	13	12	11	10	9	8
Name	None [15:12]				DU_OPC [11:8]			

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:2	DU_SIZE	RW	R	Undefined	Size/width of the data unit data operands (in bits) is DU_SIZE+1. E.g., if DU_SIZE is 7, the width is 8 bits.
8:11	DU_OPC	RW	R	Undefined	Data unit opcode specifies the data unit operation: '1': INCR '2': DECR '3': INCR_WRAP '4': DECR_WRAP '5': INCR_DECR '6': INCR_DECR_WRAP '7': ROR '8': SHR '9': AND_OR '10': SHR_MAJ3 '11': SHR_EQL. Otherwise: Undefined.

14.3.1.7 PRGIO_PRT_DATA

Description: Data register
Address: 0x400500F0
Offset: 0xF0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:7	DATA	RW	R	Undefined	Data unit input data source.

15 ROMTABLE

Description CoreSight ROM-Table with Cypress Vendor/Silicon ID
Base Address 0xF0000000
Size 0x1000
Slave Num MEMORYMAP

Register Name	Address	Permission	Description
ROMTABLE_ADDR	0xF0000000	FULL	Link to Cortex M0 ROM Table.
ROMTABLE_DID	0xF0000FCC	FULL	Device Type Identifier register.
ROMTABLE_PID4	0xF0000FD0	FULL	Peripheral Identification Register 4.
ROMTABLE_PID5	0xF0000FD4	FULL	Peripheral Identification Register 5.
ROMTABLE_PID6	0xF0000FD8	FULL	Peripheral Identification Register 6.
ROMTABLE_PID7	0xF0000FDC	FULL	Peripheral Identification Register 7.
ROMTABLE_PID0	0xF0000FE0	FULL	Peripheral Identification Register 0.
ROMTABLE_PID1	0xF0000FE4	FULL	Peripheral Identification Register 1.
ROMTABLE_PID2	0xF0000FE8	FULL	Peripheral Identification Register 2.
ROMTABLE_PID3	0xF0000FEC	FULL	Peripheral Identification Register 3.
ROMTABLE_CID0	0xF0000FF0	FULL	Component Identification Register 0.
ROMTABLE_CID1	0xF0000FF4	FULL	Component Identification Register 1.
ROMTABLE_CID2	0xF0000FF8	FULL	Component Identification Register 2.
ROMTABLE_CID3	0xF0000FFC	FULL	Component Identification Register 3.

15.1 Register Details

15.1.1 ROMTABLE_ADDR

Description: Link to Cortex M0 ROM Table.
Address: 0xF0000000
Offset: 0x0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xF00FF003

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:2]						FORMAT_32BIT [1:1]	PRESENT [0:0]

Bits	15	14	13	12	11	10	9	8
Name					None [11:8]			

Bits	23	22	21	20	19	18	17	16
Name	ADDR_OFFSET [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	ADDR_OFFSET [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	PRESENT	R	R	1	Entry present.
1	FORMAT_32BIT	R	R	1	ROM Table format: '0: 8-bit format. '1': 32-bit format.
12:31	ADDR_OFFSET	R	R	983295	Address offset of the Cortex-M0 ROM Table base address (0xe00f:f000) wrt. Cypress chip specific ROM Table base address (0xf000:0000). ADDR_OFFSET[19:0] = 0xe00f:f - 0xf000:0 = 0xf00f:f.

15.1.2 ROMTABLE_DID

Description: Device Type Identifier register.
Address: 0xF0000FCC
Offset: 0xFCC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x1

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	VALUE [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	VALUE	R	R	1	.

15.1.3 ROMTABLE_PID4

Description: Peripheral Identification Register 4.
Address: 0xF0000FD0
Offset: 0xFD0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	COUNT [7:4]				JEP_CONTINUATION [3:0]			

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:3	JEP_CONTINUATION	R	R	Undefined	JEP106 continuation code. This value is product specific and specified as part of the product definition in the CPUSS.JEPCONTINUATION parameter.
4:7	COUNT	R	R	0	Size of ROM Table is 2^COUNT * 4 KByte.

15.1.4 ROMTABLE_PID5

Description: Peripheral Identification Register 5.
Address: 0xF0000FD4
Offset: 0xFD4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	VALUE [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	VALUE	R	R	0	.

15.1.5 ROMTABLE_PID6

Description: Peripheral Identification Register 6.
Address: 0xF0000FD8
Offset: 0xFD8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	VALUE [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	VALUE	R	R	0	.

15.1.6 ROMTABLE_PID7

Description: Peripheral Identification Register 7.
Address: 0xF0000FDC
Offset: 0xFDC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	VALUE [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	VALUE	R	R	0	.

15.1.7 ROMTABLE_PID0

Description: Peripheral Identification Register 0.
Address: 0xF0000FE0
Offset: 0xFE0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	PN_MIN [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:7	PN_MIN	R	R	Undefined	JEP106 part number. 4 lsbs of CPUSS.PARTNUMBER parameter.

15.1.8 ROMTABLE_PID1

Description: Peripheral Identification Register 1.
Address: 0xF0000FE4
Offset: 0xFE4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	JEPID_MIN [7:4]				PN_MAJ [3:0]			

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:3	PN_MAJ	R	R	Undefined	JEP106 part number. 4 msbs of CPUSS.PARTNUMBER parameter.
4:7	JEPID_MIN	R	R	Undefined	JEP106 vendor id. 4 lsbs of CPUSS.JEPID parameter.

15.1.9 ROMTABLE_PID2

Description: Peripheral Identification Register 2.
Address: 0xF0000FE8
Offset: 0xFE8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	REV [7:4]				JEPID_MAJ [3:0]			

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:3	JEPID_MAJ	R	R	Undefined	JEP106 vendor id. 4 msbs of CPUSS.JEPID parameter.
4:7	REV	R	R	Undefined	Major REVision number (chip specific). Identifies the design iteration of the component. For first tape out: 0x1. This field is incremented on subsequent tape outs.

15.1.10 ROMTABLE_PID3

Description: Peripheral Identification Register 3.
Address: 0xF0000FEC
Offset: 0xFEC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	REV_AND [7:4]				CM [3:0]			

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:3	CM	R	R	0	Customer modified field. This field is used to track modifications to the original component design as a result of component IP reuse.
4:7	REV_AND	R	R	Undefined	Minor REVision number (chip specific). For first tape out: 0x1. This field is incremented on subsequent tape outs.

15.1.11 ROMTABLE_CID0

Description: Component Identification Register 0.
Address: 0xF0000FF0
Offset: 0xFF0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xD

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	VALUE [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	VALUE	R	R	13	Component identification byte 0 of 4-byte component identification 0xB105:100D.

15.1.12 ROMTABLE_CID1

Description: Component Identification Register 1.
Address: 0xF0000FF4
Offset: 0xFF4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x10

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	VALUE [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	VALUE	R	R	16	Component identification byte 1 of 4-byte component identification 0xB105:100D. Component class: 'ROM Table'.

15.1.13 ROMTABLE_CID2

Description: Component Identification Register 2.
Address: 0xF0000FF8
Offset: 0xFF8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x5

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	VALUE [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	VALUE	R	R	5	Component identification byte 2 of 4-byte component identification 0xB105:100D.

15.1.14 ROMTABLE_CID3

Description: Component Identification Register 3.
Address: 0xF0000FFC
Offset: 0xFFC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xB1

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	VALUE [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	VALUE	R	R	177	Component identification byte 3 of 4-byte component identification 0xB105:100D.

16 SAR

Description SAR ADC with Sequencer
Base Address 0x403A0000
Size 0x10000
Slave Num MMIO2

Register Name	Address	Permission	Description
SAR_CTRL	0x403A0000	FULL	Analog control register.
SAR_SAMPLE_CTRL	0x403A0004	FULL	Sample control register.
SAR_SAMPLE_TIME01	0x403A0010	FULL	Sample time specification ST0 and ST1
SAR_SAMPLE_TIME23	0x403A0014	FULL	Sample time specification ST2 and ST3
SAR_RANGE_THRES	0x403A0018	FULL	Global range detect threshold register.
SAR_RANGE_COND	0x403A001C	FULL	Global range detect mode register.
SAR_CHAN_EN	0x403A0020	FULL	Enable bits for the channels
SAR_START_CTRL	0x403A0024	FULL	Start control register (firmware trigger).
SAR_DFT_CTRL	0x403A0030	FULL	DFT control register.
SAR_CHAN_CONFIG0	0x403A0080	FULL	Channel configuration register.
SAR_CHAN_CONFIG1	0x403A0084	FULL	Channel configuration register.
SAR_CHAN_CONFIG2	0x403A0088	FULL	Channel configuration register.
SAR_CHAN_CONFIG3	0x403A008C	FULL	Channel configuration register.
SAR_CHAN_CONFIG4	0x403A0090	FULL	Channel configuration register.
SAR_CHAN_CONFIG5	0x403A0094	FULL	Channel configuration register.
SAR_CHAN_CONFIG6	0x403A0098	FULL	Channel configuration register.
SAR_CHAN_CONFIG7	0x403A009C	FULL	Channel configuration register.
SAR_CHAN_CONFIG8	0x403A00A0	FULL	Channel configuration register.
SAR_CHAN_CONFIG9	0x403A00A4	FULL	Channel configuration register.
SAR_CHAN_CONFIG10	0x403A00A8	FULL	Channel configuration register.
SAR_CHAN_CONFIG11	0x403A00AC	FULL	Channel configuration register.
SAR_CHAN_CONFIG12	0x403A00B0	FULL	Channel configuration register.
SAR_CHAN_CONFIG13	0x403A00B4	FULL	Channel configuration register.
SAR_CHAN_CONFIG14	0x403A00B8	FULL	Channel configuration register.
SAR_CHAN_CONFIG15	0x403A00BC	FULL	Channel configuration register.
SAR_CHAN_WORK0	0x403A0100	FULL	Channel working data register
SAR_CHAN_WORK1	0x403A0104	FULL	Channel working data register
SAR_CHAN_WORK2	0x403A0108	FULL	Channel working data register
SAR_CHAN_WORK3	0x403A010C	FULL	Channel working data register
SAR_CHAN_WORK4	0x403A0110	FULL	Channel working data register
SAR_CHAN_WORK5	0x403A0114	FULL	Channel working data register
SAR_CHAN_WORK6	0x403A0118	FULL	Channel working data register
SAR_CHAN_WORK7	0x403A011C	FULL	Channel working data register
SAR_CHAN_WORK8	0x403A0120	FULL	Channel working data register
SAR_CHAN_WORK9	0x403A0124	FULL	Channel working data register
SAR_CHAN_WORK10	0x403A0128	FULL	Channel working data register
SAR_CHAN_WORK11	0x403A012C	FULL	Channel working data register
SAR_CHAN_WORK12	0x403A0130	FULL	Channel working data register
SAR_CHAN_WORK13	0x403A0134	FULL	Channel working data register
SAR_CHAN_WORK14	0x403A0138	FULL	Channel working data register
SAR_CHAN_WORK15	0x403A013C	FULL	Channel working data register
SAR_CHAN_RESULT0	0x403A0180	FULL	Channel result data register
SAR_CHAN_RESULT1	0x403A0184	FULL	Channel result data register
SAR_CHAN_RESULT2	0x403A0188	FULL	Channel result data register
SAR_CHAN_RESULT3	0x403A018C	FULL	Channel result data register
SAR_CHAN_RESULT4	0x403A0190	FULL	Channel result data register
SAR_CHAN_RESULT5	0x403A0194	FULL	Channel result data register
SAR_CHAN_RESULT6	0x403A0198	FULL	Channel result data register
SAR_CHAN_RESULT7	0x403A019C	FULL	Channel result data register
SAR_CHAN_RESULT8	0x403A01A0	FULL	Channel result data register
SAR_CHAN_RESULT9	0x403A01A4	FULL	Channel result data register
SAR_CHAN_RESULT10	0x403A01A8	FULL	Channel result data register
SAR_CHAN_RESULT11	0x403A01AC	FULL	Channel result data register
SAR_CHAN_RESULT12	0x403A01B0	FULL	Channel result data register
SAR_CHAN_RESULT13	0x403A01B4	FULL	Channel result data register

Register Name	Address	Permission	Description
SAR_CHAN_RESULT14	0x403A01B8	FULL	Channel result data register
SAR_CHAN_RESULT15	0x403A01BC	FULL	Channel result data register
SAR_CHAN_WORK_UPDATED	0x403A0200	FULL	Channel working data register 'updated' bits
SAR_CHAN_RESULT_UPDATED	0x403A0204	FULL	Channel result data register 'updated' bits
SAR_INTR	0x403A0210	FULL	Interrupt request register.
SAR_INTR_SET	0x403A0214	FULL	Interrupt set request register
SAR_INTR_MASK	0x403A0218	FULL	Interrupt mask register.
SAR_INTR_MASKED	0x403A021C	FULL	Interrupt masked request register
SAR_SATURATE_INTR	0x403A0220	FULL	Saturate interrupt request register.
SAR_SATURATE_INTR_SET	0x403A0224	FULL	Saturate interrupt set request register
SAR_SATURATE_INTR_MASK	0x403A0228	FULL	Saturate interrupt mask register.
SAR_SATURATE_INTR_MASKED	0x403A022C	FULL	Saturate interrupt masked request register
SAR_RANGE_INTR	0x403A0230	FULL	Range detect interrupt request register.
SAR_RANGE_INTR_SET	0x403A0234	FULL	Range detect interrupt set request register
SAR_RANGE_INTR_MASK	0x403A0238	FULL	Range detect interrupt mask register.
SAR_RANGE_INTR_MASKED	0x403A023C	FULL	Range interrupt masked request register
SAR_INTR_CAUSE	0x403A0240	FULL	Interrupt cause register
SAR_INJ_CHAN_CONFIG	0x403A0280	FULL	Injection channel configuration register.
SAR_INJ_RESULT	0x403A0290	FULL	Injection channel result register
SAR_STATUS	0x403A02A0	FULL	Current status of internal SAR registers (mostly for debug)
SAR_AVG_STAT	0x403A02A4	FULL	Current averaging status (for debug)
SAR_MUX_SWITCH0	0x403A0300	FULL	SARMUX Firmware switch controls
SAR_MUX_SWITCH_CLEAR0	0x403A0304	FULL	SARMUX Firmware switch control clear
SAR_MUX_SWITCH1	0x403A0308	FULL	SARMUX Firmware switch controls
SAR_MUX_SWITCH_CLEAR1	0x403A030C	FULL	SARMUX Firmware switch control clear
SAR_MUX_SWITCH2	0x403A0310	FULL	EXPMUX and DIAGMUX Firmware switch controls Note:MUX_FW_EXP_P0_VPLUS MUX_FW_EXP_P1_VPLUS MUX_FW_EXP_P2_VPLUS MUX_FW_EXP_P3_VPLUS MUX_FW_EXP_P4_VPLUS MUX_FW_EXP_P5_VPLUS MUX_FW_EXP_P6_VPLUS MUX_FW_EXP_P7_VPLUS MUX_FW_EXP_P0_VMINUS MUX_FW_EXP_P1_VMINUS MUX_FW_EXP_P2_VMINUS MUX_FW_EXP_P3_VMINUS MUX_FW_EXP_P4_VMINUS MUX_FW_EXP_P5_VMINUS MUX_FW_EXP_P6_VMINUS MUX_FW_EXP_P7_VMINUS are not available for this register
SAR_MUX_SWITCH_CLEAR2	0x403A0314	FULL	EXPMUX and DIAGMUX Firmware switch control clear Note:MUX_FW_EXP_P0_VPLUS MUX_FW_EXP_P1_VPLUS MUX_FW_EXP_P2_VPLUS MUX_FW_EXP_P3_VPLUS MUX_FW_EXP_P4_VPLUS MUX_FW_EXP_P5_VPLUS MUX_FW_EXP_P6_VPLUS MUX_FW_EXP_P7_VPLUS MUX_FW_EXP_P0_VMINUS MUX_FW_EXP_P1_VMINUS MUX_FW_EXP_P2_VMINUS MUX_FW_EXP_P3_VMINUS MUX_FW_EXP_P4_VMINUS MUX_FW_EXP_P5_VMINUS MUX_FW_EXP_P6_VMINUS MUX_FW_EXP_P7_VMINUS are not available for this register
SAR_MUX_SWITCH_HW_CTRL	0x403A0340	FULL	SARMUX switch hardware control
SAR_MUX_SWITCH_HW_CTRL2	0x403A0344	FULL	EXPMUX and DIAGMUX switch hardware control Note:MUX_HW_CTRL_EXP_P0 MUX_HW_CTRL_EXP_P1 MUX_HW_CTRL_EXP_P2 MUX_HW_CTRL_EXP_P3 MUX_HW_CTRL_EXP_P4 MUX_HW_CTRL_EXP_P5 MUX_HW_CTRL_EXP_P6 MUX_HW_CTRL_EXP_P7 are not available for this register
SAR_MUX_SWITCH_STATUS	0x403A0350	FULL	SARMUX switch status

Register Name	Address	Permission	Description
SAR_MUX_SWITCH_STATUS2	0x403A0354	FULL	EXPMUX and DIAGMUX switch status Note:MUX_FW_EXP_P0_VPLUS MUX_FW_EXP_P1_VPLUS MUX_FW_EXP_P2_VPLUS MUX_FW_EXP_P3_VPLUS MUX_FW_EXP_P4_VPLUS MUX_FW_EXP_P5_VPLUS MUX_FW_EXP_P6_VPLUS MUX_FW_EXP_P7_VPLUS MUX_FW_EXP_P0_VMINUS MUX_FW_EXP_P1_VMINUS MUX_FW_EXP_P2_VMINUS MUX_FW_EXP_P3_VMINUS MUX_FW_EXP_P4_VMINUS MUX_FW_EXP_P5_VMINUS MUX_FW_EXP_P6_VMINUS MUX_FW_EXP_P7_VMINUS are not available for this register
SAR_PUMP_CTRL	0x403A0380	FULL	Switch pump control
SAR_ANA_TRIM	0x403AFF00	FULL	Analog trim register.
SAR_WOUNDING	0x403AFF04	FULL	SAR wounding register

16.1 Register Details

16.1.1 SAR_CTRL

Description: Analog control register.
Address: 0x403A0000
Offset: 0x0
Retention: Retained
IsDeepSleep: No
Comment: Based on pin out of the analog s8sar IP, not sure if this is sufficient or needed.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	VREF_BYP_CAP_EN [7:7]	VREF_SEL [6:4]			None [3:0]			

Bits	15	14	13	12	11	10	9	8
Name	PWR_CTRL_VREF [15:14]		SAR_HW_CTRL_NEGVREF [13:13]	None [12:12]	NEG_SEL [11:9]			None [8:8]

Bits	23	22	21	20	19	18	17	16
Name	None [23:22]		REFBUF_EN [21:21]	BOOSTPUMP_EN [20:20]	SPARE [19:16]			

Bits	31	30	29	28	27	26	25	24
Name	ENABLED [31:31]	SWITCH_DISABLE [30:30]	RESERVED_CTRL_29 [29:29]	RESERVED_CTRL_28 [28:28]	DEEPSLEEP_ON [27:27]	None [26:26]	ICONT_LV [25:24]	

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
4:6	VREF_SEL	RW	R	0	SARADC internal VREF selection.
	RESERVED_VREF_0			0	N/A
	RESERVED_VREF_1			1	N/A
	RESERVED_VREF_2			2	N/A
	VREF_ADFT			3	Test mode only
	VBGR			4	1.2V from SRSS BandGap (VREF buffer on)
	VREF_EXT			5	External precision Vref direct from a pin (low impedance path).
	VDDA_DIV_2			6	Vdda/2 (VREF buffer on)
	VDDA			7	Vdda.
7	VREF_BYP_CAP_EN	RW	R	0	VREF bypass cap enable for when VREF buffer is on
9:11	NEG_SEL	RW	R	0	SARADC internal NEG selection for Single ended conversion
	VSSA_KELVIN			0	NEG input of SARADC is connected to 'vssa_kelvin', gives more precision around zero. Note this opens both SARADC internal switches, therefore use this value to insert a break-before-make cycle on those switches when SWITCH_DISABLE is high.
	ART_VSSA			1	NEG input of SARADC is connected to VSSA in AROUTE close to the SARADC
	P1			2	NEG input of SARADC is connected to P1 pin of SARMUX
	P3			3	NEG input of SARADC is connected to P3 pin of SARMUX

Bits	Name	SW	HW	Default or Enum	Description
	P5			4	NEG input of SARADC is connected to P5 pin of SARMUX
	P7			5	NEG input of SARADC is connected to P7 pin of SARMUX
	ACORE			6	NEG input of SARADC is connected to an ACORE in AROUTE
	VREF			7	NEG input of SARADC is shorted with VREF input of SARADC.
13	SAR_HW_CTRL _NEGVREF	RW	R	0	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for VREF to NEG switch.
14:15	PWR_CTRL_VREF	RW	R	0	VREF buffer low power mode.
	NORMAL_PWR			0	normal power (default), bypass cap, max clk_sar is 18MHz.
	HALF_PWR			1	deprecated
	THIRD_PWR			2	Invalid for PSoC4A, otherwise 2X power, no bypass cap, max clk_sar is 1.8MHz
	QUARTER_PWR			3	deprecated
16:19	SPARE	RW	R	0	Spare controls, not yet designated, for late changes done with an ECO
20	BOOSTPUMP_EN	RW	R	0	SARADC internal pump: 0=disabled: pump output is VDDA, 1=enabled: pump output is boosted.
21	REFBUF_EN	RW	R	0	1 - Enable the SARREFBUF. This bit needs to be set when SAR is enabled and needs reference buffer.
24:25	ICONT_LV	RW	R	0	SARADC low power mode.
	NORMAL_PWR			0	normal power (default), max clk_sar is 18MHz.
	HALF_PWR			1	1/2 power mode, max clk_sar is 9MHz.
	MORE_PWR			2	1.333 power mode, max clk_sar is 18MHz.
	QUARTER_PWR			3	1/4 power mode, max clk_sar is 4.5MHz.
27	DEEPSLEEP_ON	RW	R	0	- 0: SARMUX IP disabled off during DeepSleep power mode - 1: SARMUX IP remains enabled during DeepSleep power mode (if ENABLED=1)
28	RESERVED_CTRL_28	RW	R	0	Reserved, must be left in default reset state (0)
29	RESERVED_CTRL_29	RW	R	0	Reserved, must be left in default reset state (0)
30	SWITCH_DISABLE	RW	R	0	Disable SAR sequencer from enabling routing switches (note DSI and firmware can always close switches independent of this control) - 0: Normal mode, SAR sequencer changes switches according to pin address in channel configurations - 1: Switches disabled, SAR sequencer does not enable any switches, it is the responsibility of the firmware or UDBs (through DSI) to set the switches to route the signal to be converted through the SARMUX
31	ENABLED	RW	R	0	- 0: SAR IP disabled (put analog in power down and stop clocks), also can clear FW_TRIGGER and INJ_START_EN (if not tailgaiting) on write. - 1: SAR IP enabled.

16.1.2 SAR_SAMPLE_CTRL

Description: Sample control register.
Address: 0x403A0004
Offset: 0x4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x80008

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	AVG_SHIFT [7:7]	AVG_CNT [6:4]			DIFFERENTIAL_SIGNED [3:3]	SINGLE_ENDED_SIGNED [2:2]	LEFT_ALIGN [1:1]	SUB_RESOLUTION [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:9]							AVG_MODE [8:8]

Bits	23	22	21	20	19	18	17	16
Name	None [23:20]				DSI_SYNC_TRIGGER [19:19]	DSI_TRIGGER_LEVEL [18:18]	DSI_TRIGGER_EN [17:17]	CONTINUOUS [16:16]

Bits	31	30	29	28	27	26	25	24
Name	EOS_DSI_OUT_EN [31:31]	None [30:24]						

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	SUB_RESOLUTION	RW	R	0	Conversion resolution for channels that have sub-resolution enabled (RESOLUTION=1) (otherwise resolution is 12-bit).
	8B			0	8-bit.
	10B			1	10-bit.
1	LEFT_ALIGN	RW	R	0	Left align data in data[15:0], default data is right aligned in data[11:0], with sign extension to 16 bits if the channel is differential.
2	SINGLE_ENDED_SIGNED	RW	R	0	Output data from a single ended conversion as a signed value If AVG_MODE = 1 (Interleaved averaging), then SINGLE_ENDED_SIGNED must be configured identically to DIFFERENTIAL_SIGNED.
	UNSIGNED			0	Default: result data is unsigned (zero extended if needed)
	SIGNED			1	result data is signed (sign extended if needed)
3	DIFFERENTIAL_SIGNED	RW	R	1	Output data from a differential conversion as a signed value when DIFFERENTIAL_EN or NEG_ADDR_EN is set to 1 If AVG_MODE = 1 (Interleaved averaging), then DIFFERENTIAL_SIGNED must be configured identically to SINGLE_ENDED_SIGNED.
	UNSIGNED			0	result data is unsigned (zero extended if needed)
	SIGNED			1	Default: result data is signed (sign extended if needed)

Bits	Name	SW	HW	Default or Enum	Description
4:6	AVG_CNT	RW	R	0	Averaging Count for channels that have averaging enabled (AVG_EN). A channel will be sampled (1<<(AVG_CNT+1)) = [2..256] times. - In ACCUNDUMP mode (1st order accumulate and dump filter) a channel will be sampled back to back, the average result is calculated and stored and then the next enabled channel is sampled. If shifting is not enabled (AVG_SHIFT=0) then the result is forced to shift right so that is fits in 16 bits, so right shift is done by max(0,AVG_CNT-3). - In INTERLEAVED mode one sample is taken per triggered scan, only in the scan where the final averaging count is reached a valid average is calculated and stored in the RESULT register (by definition the same scan for all the channels that have averaging enabled). In all other scans the RESULT register for averaged channels will have an invalid result and the intermediate accumulated value is stored in the 16-bit WORK register. In this mode make sure that the averaging count is low enough to ensure that the intermediate value does not exceed 16-bits otherwise the MSBs will be lost. So for a 12-bit resolution the averaging count should be set to 16 or less (AVG_CNT=<3).
7	AVG_SHIFT	RW	R	0	Averaging shifting: after averaging the result is shifted right to fit in the sample resolution. For averaging the sample resolution is the highest resolution allowed by wounding.
8	AVG_MODE	RW	R	0	Averaging mode, in DSI mode this bit is ignored and only AccuNDump mode is available.
	ACCUNDUMP			0	Accumulate and Dump (1st order accumulate and dump filter): a channel will be sampled back to back and averaged
	INTERLEAVED			1	Interleaved: On each scan (trigger) one sample is taken per channel and averaged over several scans. NOTE: If all channels in a scan are configured for interleaved averaging, then EOS is only asserted after the last scan of the average count. In addition, a new trigger which would cause a collision, will be ignored, except for the last scan of the average count. If the collision is detected in the the last scan, the trigger will be pended and will be executed after the last scan is completed.
16	CONTINUOUS	RW	R	0	- 0: Wait for next FW_TRIGGER (one shot) or hardware (DSI) trigger (e.g. from TPWM for periodic triggering) before scanning enabled channels. - 1: Continuously scan enabled channels, ignore triggers.
17	DSI_TRIGGER_EN	RW	R	0	- 0: firmware trigger only: disable hardware (DSI) trigger. - 1: enable hardware (DSI) trigger (e.g. from TCPWM, GPIO or UDB).
18	DSI_TRIGGER_LEVEL	RW	R	0	- 0: DSI trigger signal is a pulse input, a positive edge detected on the DSI trigger signal triggers a new scan. - 1: DSI trigger signal is a level input, as long as the DSI trigger signal remains high the SAR will do continuous scans.
19	DSI_SYNC_TRIGGER	RW	R	1	- 0: bypass clock domain synchronisation of the DSI trigger signal. - 1: synchronize the DSI trigger signal to the SAR clock domain, if needed an edge detect is done in the peripheral clock domain.

Bits	Name	SW	HW	Default or Enum	Description
31	EOS_DSI_OUT_EN	RW	R	0	Enable to output EOS_INTR to DSI. When enabled each time EOS_INTR is set by the hardware also a pulse is send on the dsi_eos signal.

16.1.3 SAR_SAMPLE_TIME01

Description: Sample time specification ST0 and ST1
Address: 0x403A0010
Offset: 0x10
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x40004

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	SAMPLE_TIME0 [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	None [15:10]						SAMPLE_TIME0 [9:8]	

Bits	23	22	21	20	19	18	17	16
Name	SAMPLE_TIME1 [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:26]						SAMPLE_TIME1 [25:24]	

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:9	SAMPLE_TIME0	RW	R	4	Sample time0 (aperture) in ADC clock cycles. Note that actual sample time is half a clock less than specified here. The minimum sample time is 194ns, which is 3.5 cycles (4 in this field) with an 18MHz clock. Minimum legal value in this register is 2.
16:25	SAMPLE_TIME1	RW	R	4	Sample time1

16.1.4 SAR_SAMPLE_TIME23

Description: Sample time specification ST2 and ST3
Address: 0x403A0014
Offset: 0x14
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x40004

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	SAMPLE_TIME2 [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	None [15:10]						SAMPLE_TIME2 [9:8]	

Bits	23	22	21	20	19	18	17	16
Name	SAMPLE_TIME3 [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:26]						SAMPLE_TIME3 [25:24]	

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:9	SAMPLE_TIME2	RW	R	4	Sample time2
16:25	SAMPLE_TIME3	RW	R	4	Sample time3

16.1.5 SAR_RANGE_THRES

Description: Global range detect threshold register.
Address: 0x403A0018
Offset: 0x18
Retention: Retained
IsDeepSleep: No
Comment: The values here are interpreted signed or unsigned according to the channel configuration. Note that Range detection is done on the value that is stored in the Result register, i.e. after averaging, shifting sign extension and left/right alignment.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	RANGE_LOW [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	RANGE_LOW [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	RANGE_HIGH [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	RANGE_HIGH [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:15	RANGE_LOW	RW	R	0	Low threshold for range detect.
16:31	RANGE_HIGH	RW	R	0	High threshold for range detect.

16.1.6 SAR_RANGE_COND

Description: Global range detect mode register.
Address: 0x403A001C
Offset: 0x1C
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	RANGE_COND [31:30]		None [29:24]					

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
30:31	RANGE_COND	RW	R	0	Range condition select.
	BELOW			0	result < RANGE_LOW
	INSIDE			1	RANGE_LOW <= result < RANGE_HIGH
	ABOVE			2	RANGE_HIGH <= result
	OUTSIDE			3	result < RANGE_LOW || RANGE_HIGH <= result

16.1.7 SAR_CHAN_EN

Description: Enable bits for the channels
Address: 0x403A0020
Offset: 0x20
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	CHAN_EN [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	CHAN_EN [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:15	CHAN_EN	RW	R	0	Channel enable. - 0: the corresponding channel is disabled. - 1: the corresponding channel is enabled, it will be included in the next scan.

16.1.8 SAR_START_CTRL

Description: Start control register (firmware trigger).
Address: 0x403A0024
Offset: 0x24
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:1]							FW_TRIGGER [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	FW_TRIGGER	RW1S	RW1C	0	When firmware writes a 1 here it will trigger the next scan of enabled channels, hardware clears this bit when the scan started with this trigger is completed. If scanning continuously the trigger is ignored and hardware clears this bit after the next scan is done. This bit is also cleared when the SAR is disabled.

16.1.9 SAR_DFT_CTRL

Description: DFT control register.
Address: 0x403A0030
Offset: 0x30
Retention: Not Retained
IsDeepSleep: No
Comment: Based on pin out of the analog s8sar IP.
Default: 0x2

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:2]						HIZ [1:1]	DLY_INC [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:23]	DFT_OUTC [22:20]			DFT_INC [19:16]			

Bits	31	30	29	28	27	26	25	24
Name	ADFT_OVERRIDE [31:31]	ADFT_OVERRIDE_EXPMUX [30:30]	DCEN [29:29]	EN_CSEL_DFT [28:28]	SEL_CSEL_DFT [27:24]			

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	DLY_INC	RW	R	0	DFT control: Control for delay circuits on sampling phase, =1 doubes the non-overlap delay
1	HIZ	RW	R	1	DFT control for getting higher input impedance, must be 1 (0 is deprecated)
16:19	DFT_INC	RW	R	0	DFT control for preamp inputs
20:22	DFT_OUTC	RW	R	0	DFT control for preamp outputs
24:27	SEL_CSEL_DFT	RW	R	0	Usage 1: DFT bits for DAC array Usage 2: For [0]=1 (when dcen=0): Delay timing for latch enable increased by 20 percent [1]=1: comparator preamp power level increased by 25 percent
28	EN_CSEL_DFT	RW	R	0	Mux select signal for DAC control
29	DCEN	RW	R	0	Delay Control Enable for latch. - 0: doubles the latch enable time. - 1: normal latch enable time.
30	ADFT_OVERRIDE_EXPMUX	RW	R	0	During deepsleep/ hibernate mode keep EXPMUX active, i.e. do not open all switches (disconnect), to be used for ADFT.
31	ADFT_OVERRIDE	RW	R	0	During deepsleep/ hibernate mode keep SARMUX active, i.e. do not open all switches (disconnect), to be used for ADFT

16.1.10 SAR_CHAN_CONFIG

Description: Channel configuration register.
Address: 0x403A0080
Offset: 0x80
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:7]	POS_PORT_ADDR [6:4]			None [3:3]	POS_PIN_ADDR [2:0]		

Bits	15	14	13	12	11	10	9	8
Name	None [15:14]		SAMPLE_TIME_SEL [13:12]		None [11:11]	AVG_EN [10:10]	RESOLUTION [9:9]	DIFFERENTIAL_EN [8:8]

Bits	23	22	21	20	19	18	17	16
Name	None [23:23]	NEG_PORT_ADDR [22:20]			None [19:19]	NEG_PIN_ADDR [18:16]		

Bits	31	30	29	28	27	26	25	24
Name	DSI_OUT_EN [31:31]	None [30:30]	DIAG_VMINUS_SINK [29:29]	DIAG_VMINUS_SOURCE [28:28]	DIAG_VPLUS_SINK [27:27]	DIAG_VPLUS_SOURCE [26:26]	None [25:25]	NEG_ADDR_EN [24:24]

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:2	POS_PIN_ADDR	RW	R	0	Address of the pin to be sampled by this channel (connected to Vplus)
4:6	POS_PORT_ADDR	RW	R	0	Address of the port that contains the pin to be sampled by this channel (connected to Vplus)
	SARMUX			0	SARMUX PORT pins. Select POS_PIN_ADDR 0-7 for GPIO 0-7 See DIFF_EN bit description for legacy differential mode
	CTB0			1	CTB0 Selet: POS_PIN_ADDR 2 for OA0 output (single ended) POS_PIN_ADDR 3 for OA1 outout (single ended) POS_PIN_ADDR 2 + DIFF_EN for OA0 on VP and OA1 on VN (differential)
	CSAMP_CH0			1	CSAMP Channel 0 Select POS_PIN ADDR 0 for CSAMP (SARBUS) input, always differential
	CTB1			2	CTB1 (see CTB0)
	CSAMP_CH1			2	CSAMP Channel 1 (See CSAMP Channel 0)
	CTB2			3	CTB2 (see CTB0)
	CSAMP_CH2			3	CSAMP Channel 2 (See CSAMP Channel 0)
	CTB3			4	CTB3 (see CTB0)
	CSAMP_CH3			4	CSAMP Channel 3 (See CSAMP Channel 0)
	EXPMUX			5	GPIO Expansion Mux (if present) See DIFF_EN bit description for legacy differential mode
	DIAGMUX			6	Diagnostic inputs

Bits	Name	SW	HW	Default or Enum	Description
	SARMUX_VIRT			7	SARMUX virtual port (VPORT0) Select POS_PIN_ADDR 0 for Temp Sensor Select POS_PIN_ADDR 2 for AMUXBUSA (single ended, test only) Select POS_PIN_ADDR 3 for AMUXBUSB (single ended, test only) Select POS_PIN_ADDR 2 + DIFF_EN for AMUXBUA on VP and AMUXBUS B on VN (differential, test only)
8	DIFFERENTIAL_EN	RW	R	0	Legacy differential mode, usage is described by port below: SARMUX: Legacy mode, use applications should use NEG_PORT/PIN_ADDR CTB0-3: Special purpose, see CTB0 description EXPMUX: Legacy mode, use applications should use NEG_PORT/PIN_ADDR DIAGMUX: Not applicable SARMUX_VIRT: Special purpose, see SARMUX_VIRT description LEGACY MODE DESCRIPTION: Differential enable for the selected port pin for this channel. If differential is enabled then POS_PIN_ADDR[0] is ignored and considered to be 0, i.e. POS_PIN_ADDR points to the even pin of a pin pair. For differential the even pin of the pair is connected to Vplus and the odd pin of the pair is connected to Vminus. POS_PORT_ADDR is used to identify the port that contains the pins. - 0: The voltage on the addressed pin is measured (Single-ended) and the resulting value is stored in the corresponding data register. - 1: The differential voltage on the addressed pin pair is measured and the resulting value is stored in the corresponding data register. (POS_PIN_ADDR[0] is ignored). NOTE: Set to 0 if using the NEG_PIN_ADDR and NEG_PORT_ADDR to select the negative source.
9	RESOLUTION	RW	R	0	Resolution for this channel. When AVG_EN is set this bit is ignored and always a 12-bit resolution (or highest resolution allowed by wounding) is used for this channel.
	MAXRES			0	The maximum resolution is used for this channel (maximum resolution depends on wounding).
	SUBRES			1	The resolution specified by SUB_RESOLUTION in the SAR_SAMPLE_CTRL register is used for this channel.
10	AVG_EN	RW	R	0	Averaging enable for this channel. If set the AVG_CNT and AVG_SHIFT settings are used for sampling the addressed pin(s)
12:13	SAMPLE_TIME_SEL	RW	R	0	Sample time select: select which of the 4 global sample times to use for this channel
16:18	NEG_PIN_ADDR	RW	R	0	Address of the neg pin to be sampled by this channel.
20:22	NEG_PORT_ADDR	RW	R	0	Address of the neg port that contains the pin to be sampled by this channel.
	SARMUX			0	SARMUX pins.
	EXPMUX			5	GPIO Expansion Mux (if present)
	DIAGMUX			6	Diagnostic inputs
	SARMUX_VIRT			7	SARMUX virtual port (VPORT0)

Bits	Name	SW	HW	Default or Enum	Description
24	NEG_ADDR_EN	RW	R	0	1 - The NEG_PIN_ADDR and NEG_PORT_ADDR determines what drives the Vminus pin. This is a variation of differential mode with no even-odd pair limitation 0 - The NEG_SEL determines what drives the Vminus pin.
26	DIAG_VPLUS_SOURCE	RW	R	0	Enable for 10uA current source on vplus signal, active during sampling of this channel
27	DIAG_VPLUS_SINK	RW	R	0	Enable for 10uA current sink on vplus signal, active during sampling of this channel
28	DIAG_VMINUS_SOURCE	RW	R	0	Enable for 10uA current source on vminus signal, active during sampling of this channel
29	DIAG_VMINUS_SINK	RW	R	0	Enable for 10uA current sink on vminus signal, active during sampling of this channel
31	DSI_OUT_EN	RW	R	0	DSI data output enable for this channel. - 0: the conversion result for this channel is only stored in the channel data register and the corresponding CHAN_DATA_VALID bit is set. - 1: the conversion result for this channel is stored in the channel data register and the corresponding CHAN_DATA_VALID bit is set. The same data (same formating), together with the channel number, is sent out on the DSI communication channel for processing in UDBs.

16.1.11 SAR_CHAN_WORK

Description: Channel working data register
Address: 0x403A0100
Offset: 0x100
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	WORK [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	WORK [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	CHAN_WORK_UPDATED_MIR [31:31]	None [30:24]						

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:15	WORK	R	RW	Undefined	SAR conversion working data of the channel. The data is written here right after sampling this channel.
31	CHAN_WORK_UPDATED_MIR	R	W	0	mirror bit of corresponding bit in SAR_CHAN_WORK_UPDATED register

16.1.12 SAR_CHAN_RESULT

Description: Channel result data register
Address: 0x403A0180
Offset: 0x180
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	RESULT [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	RESULT [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	CHAN_RESULT_UPDATED_MIR [31:31]	RANGE_INTR_MIR [30:30]	SATURATE_INTR_MIR [29:29]	None [28:24]				

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:15	RESULT	R	W	Undefined	SAR conversion result of the channel. The data is copied here from the WORK field after all enabled channels in this scan have been sampled.
29	SATURATE_INTR_MIR	R	W	0	mirror bit of corresponding bit in SAR_SATURATE_INTR register
30	RANGE_INTR_MIR	R	W	0	mirror bit of corresponding bit in SAR_RANGE_INTR register
31	CHAN_RESULT_UPDATED_MIR	R	W	0	mirror bit of corresponding bit in SAR_CHAN_RESULT_UPDATED register

16.1.13 SAR_CHAN_WORK_UPDATED

Description: Channel working data register 'updated' bits
Address: 0x403A0200
Offset: 0x200
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	CHAN_WORK_UPDATED [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	CHAN_WORK_UPDATED [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:15	CHAN_WORK_UPDATED	R	RW	0	If set the corresponding WORK register was updated, i.e. was already sampled during the current scan and, in case of Interleaved averaging, reached the averaging count. If this bit is low then either the channel is not enabled or the averaging count is not yet reached for Interleaved averaging.

16.1.14 SAR_CHAN_RESULT_UPDATED

Description: Channel result data register 'updated' bits
Address: 0x403A0204
Offset: 0x204
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	CHAN_RESULT_UPDATED [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	CHAN_RESULT_UPDATED [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:15	CHAN_RESULT _UPDATED	R	RW	0	If set the corresponding RESULT register was updated, i.e. was sampled during the previous scan and, in case of Interleaved averaging, reached the averaging count. If this bit is low then either the channel is not enabled or the averaging count is not yet reached for Interleaved averaging.

16.1.15 SAR_INTR

Description: Interrupt request register.
Address: 0x403A0210
Offset: 0x210
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	INJ_COLLISION_INTR [7:7]	INJ_RANGE_INTR [6:6]	INJ_SATURATE_INTR [5:5]	INJ_EOC_INTR [4:4]	DSI_COLLISION_INTR [3:3]	FW_COLLISION_INTR [2:2]	OVERFLOW_INTR [1:1]	EOS_INTR [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	EOS_INTR	RW1C	RW1S	0	End Of Scan Interrupt: hardware sets this interrupt after completing a scan of all the enabled channels. Write with '1' to clear bit.
1	OVERFLOW_INTR	RW1C	RW1S	0	Overflow Interrupt: hardware sets this interrupt when it sets a new EOS_INTR while that bit was not yet cleared by the firmware. Write with '1' to clear bit.
2	FW_COLLISION_INTR	RW1C	RW1S	0	Firmware Collision Interrupt: hardware sets this interrupt when FW_TRIGGER is asserted while the SAR is BUSY. Raising this interrupt is delayed to when the scan caused by the FW_TRIGGER has been completed, i.e. not when the preceeding scan with which this trigger collided is completed. When this interrupt is set it implies that the channels were sampled later than was intended (jitter). Write with '1' to clear bit.
3	DSI_COLLISION_INTR	RW1C	RW1S	0	DSI Collision Interrupt: hardware sets this interrupt when the DSI trigger signal is asserted while the SAR is BUSY. Raising this interrupt is delayed to when the scan caused by the DSI trigger has been completed, i.e. not when the preceeding scan with which this trigger collided is completed. When this interrupt is set it implies that the channels were sampled later than was intended (jitter). Write with '1' to clear bit.
4	INJ_EOC_INTR	RW1C	RW1S	0	Injection End of Conversion Interrupt: hardware sets this interrupt after completing the conversion for the injection channel (irrespective of if tailgating was used). Write with '1' to clear bit.
5	INJ_SATURATE_INTR	RW1C	RW1S	0	Injection Saturation Interrupt: hardware sets this interrupt if an injection conversion result (before averaging) is either 0x000 or 0xFFF (for 12-bit resolution), this is an indication that the ADC likely saturated. Write with '1' to clear bit.

Bits	Name	SW	HW	Default or Enum	Description
6	INJ_RANGE_INTR	RW1C	RW1S	0	Injection Range detect Interrupt: hardware sets this interrupt if the injection conversion result (after averaging) met the condition specified by the SAR_RANGE registers. Write with '1' to clear bit.
7	INJ_COLLISION_INTR	RW1C	RW1S	0	Injection Collision Interrupt: hardware sets this interrupt when the injection trigger signal is asserted (INJ_START_EN==1 && INJ_TAILGATING==0) while the SAR is BUSY. Raising this interrupt is delayed to when the sampling of the injection channel has been completed, i.e. not when the preceeding scan with which this trigger collided is completed. When this interrupt is set it implies that the injection channel was sampled later than was intended. Write with '1' to clear bit.

16.1.16 SAR_INTR_SET

Description: Interrupt set request register
Address: 0x403A0214
Offset: 0x214
Retention: Not Retained
IsDeepSleep: No
Comment: Not really a register, intended for verification/debug. When read, this register reflects the interrupt request register.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	INJ_COLLISION_SET [7:7]	INJ_RANGE_SET [6:6]	INJ_SATURATE_SET [5:5]	INJ_EOC_SET [4:4]	DSI_COLLISION_SET [3:3]	FW_COLLISION_SET [2:2]	OVERFLOW_SET [1:1]	EOS_SET [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	EOS_SET	RW1S	A	0	Write with '1' to set corresponding bit in interrupt request register.
1	OVERFLOW_SET	RW1S	A	0	Write with '1' to set corresponding bit in interrupt request register.
2	FW_COLLISION_SET	RW1S	A	0	Write with '1' to set corresponding bit in interrupt request register.
3	DSI_COLLISION_SET	RW1S	A	0	Write with '1' to set corresponding bit in interrupt request register.
4	INJ_EOC_SET	RW1S	A	0	Write with '1' to set corresponding bit in interrupt request register.
5	INJ_SATURATE_SET	RW1S	A	0	Write with '1' to set corresponding bit in interrupt request register.
6	INJ_RANGE_SET	RW1S	A	0	Write with '1' to set corresponding bit in interrupt request register.
7	INJ_COLLISION_SET	RW1S	A	0	Write with '1' to set corresponding bit in interrupt request register.

16.1.17 SAR_INTR_MASK

Description: Interrupt mask register.
Address: 0x403A0218
Offset: 0x218
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	INJ_COLLISION_MASK [7:7]	INJ_RANGE_MASK [6:6]	INJ_SATURATE_MASK [5:5]	INJ_EOC_MASK [4:4]	DSI_COLLISION_MASK [3:3]	FW_COLLISION_MASK [2:2]	OVERFLOW_MASK [1:1]	EOS_MASK [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	EOS_MASK	RW	R	0	Mask bit for corresponding bit in interrupt request register.
1	OVERFLOW_MASK	RW	R	0	Mask bit for corresponding bit in interrupt request register.
2	FW_COLLISION_MASK	RW	R	0	Mask bit for corresponding bit in interrupt request register.
3	DSI_COLLISION_MASK	RW	R	0	Mask bit for corresponding bit in interrupt request register.
4	INJ_EOC_MASK	RW	R	0	Mask bit for corresponding bit in interrupt request register.
5	INJ_SATURATE_MASK	RW	R	0	Mask bit for corresponding bit in interrupt request register.
6	INJ_RANGE_MASK	RW	R	0	Mask bit for corresponding bit in interrupt request register.
7	INJ_COLLISION_MASK	RW	R	0	Mask bit for corresponding bit in interrupt request register.

16.1.18 SAR_INTR_MASKED

Description: Interrupt masked request register
Address: 0x403A021C
Offset: 0x21C
Retention: Not Retained
IsDeepSleep: No
Comment: If the value is not zero then the SAR interrupt signal to the NVIC is high. When read, this register reflects a bitwise AND between the interrupt request and mask registers.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	INJ_COLLISION_MASKED [7:7]	INJ_RANGE_MASKED [6:6]	INJ_SATURATE_MASKED [5:5]	INJ_EOC_MASKED [4:4]	DSI_COLLISION_MASKED [3:3]	FW_COLLISION_MASKED [2:2]	OVERFLOW_MASKED [1:1]	EOS_MASKED [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	EOS_MASKED	R	W	0	Logical and of corresponding request and mask bits.
1	OVERFLOW_MASKED	R	W	0	Logical and of corresponding request and mask bits.
2	FW_COLLISION_MASKED	R	W	0	Logical and of corresponding request and mask bits.
3	DSI_COLLISION_MASKED	R	W	0	Logical and of corresponding request and mask bits.
4	INJ_EOC_MASKED	R	W	0	Logical and of corresponding request and mask bits.
5	INJ_SATURATE_MASKED	R	W	0	Logical and of corresponding request and mask bits.
6	INJ_RANGE_MASKED	R	W	0	Logical and of corresponding request and mask bits.
7	INJ_COLLISION_MASKED	R	W	0	Logical and of corresponding request and mask bits.

16.1.19 SAR_SATURATE_INTR

Description: Saturate interrupt request register.
Address: 0x403A0220
Offset: 0x220
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	SATURATE_INTR [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	SATURATE_INTR [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:15	SATURATE_INTR	RW1C	RW1S	0	Saturate Interrupt: hardware sets this interrupt for each channel if a conversion result (before averaging) of that channel is either 0x000 or 0xFFF (for 12-bit resolution), this is an indication that the ADC likely saturated. Write with '1' to clear bit.

16.1.20 SAR_SATURATE_INTR_SET

Description: Saturate interrupt set request register
Address: 0x403A0224
Offset: 0x224
Retention: Not Retained
IsDeepSleep: No
Comment: Not really a register, intended for verification/debug. When read, this register reflects the interrupt request register.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	SATURATE_SET [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	SATURATE_SET [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:15	SATURATE_SET	RW1S	A	0	Write with '1' to set corresponding bit in interrupt request register.

16.1.21 SAR_SATURATE_INTR_MASK

Description: Saturate interrupt mask register.
Address: 0x403A0228
Offset: 0x228
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	SATURATE_MASK [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	SATURATE_MASK [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:15	SATURATE_MASK	RW	R	0	Mask bit for corresponding bit in interrupt request register.

16.1.22 SAR_SATURATE_INTR_MASKED

Description: Saturate interrupt masked request register
Address: 0x403A022C
Offset: 0x22C
Retention: Not Retained
IsDeepSleep: No
Comment: Not really a register, just an entry in the read mux. If the value is not zero then the SAR interrupt signal to the NVIC is high. When read, this register reflects a bitwise AND between the interrupt request and mask registers.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	SATURATE_MASKED [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	SATURATE_MASKED [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:15	SATURATE_MASKED	R	W	0	Logical and of corresponding request and mask bits.

16.1.23 SAR_RANGE_INTR

Description: Range detect interrupt request register.
Address: 0x403A0230
Offset: 0x230
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	RANGE_INTR [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	RANGE_INTR [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:15	RANGE_INTR	RW1C	RW1S	0	Range detect Interrupt: hardware sets this interrupt for each channel if the conversion result (after averaging) of that channel met the condition specified by the SAR_RANGE registers. Write with '1' to clear bit.

16.1.24 SAR_RANGE_INTR_SET

Description: Range detect interrupt set request register
Address: 0x403A0234
Offset: 0x234
Retention: Not Retained
IsDeepSleep: No
Comment: Not really a register, intended for verification/debug. When read, this register reflects the interrupt request register.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	RANGE_SET [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	RANGE_SET [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:15	RANGE_SET	RW1S	A	0	Write with '1' to set corresponding bit in interrupt request register.

16.1.25 SAR_RANGE_INTR_MASK

Description: Range detect interrupt mask register.
Address: 0x403A0238
Offset: 0x238
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	RANGE_MASK [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	RANGE_MASK [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:15	RANGE_MASK	RW	R	0	Mask bit for corresponding bit in interrupt request register.

16.1.26 SAR_RANGE_INTR_MASKED

Description: Range interrupt masked request register
Address: 0x403A023C
Offset: 0x23C
Retention: Not Retained
IsDeepSleep: No
Comment: If the value is not zero then the SAR interrupt signal to the NVIC is high. When read, this register reflects a bitwise AND between the interrupt request and mask registers.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	RANGE_MASKED [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	RANGE_MASKED [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:15	RANGE_MASKED	R	W	0	Logical and of corresponding request and mask bits.

16.1.27 SAR_INTR_CAUSE

Description: Interrupt cause register
Address: 0x403A0240
Offset: 0x240
Retention: Not Retained
IsDeepSleep: No
Comment: copy of SAR_INTR_MASKED, plus reduction of SAR_RANGE_INTR_MASKED and SAR_SATURATION_INTR_MASKED
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	INJ_COLLISION_MASKED_MIR [7:7]	INJ_RANGE_MASKED_MIR [6:6]	INJ_SATURATE_MASKED_MIR [5:5]	INJ_EOC_MASKED_MIR [4:4]	DSI_COLLISION_MASKED_MIR [3:3]	FW_COLLISION_MASKED_MIR [2:2]	OVERFLOW_MASKED_MIR [1:1]	EOS_MASKED_MIR [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	RANGE_MASKED_RED [31:31]	SATURATE_MASKED_RED [30:30]	None [29:24]					

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	EOS_MASKED_MIR	R	W	0	Mirror copy of corresponding bit in SAR_INTR_MASKED
1	OVERFLOW_MASKED_MIR	R	W	0	Mirror copy of corresponding bit in SAR_INTR_MASKED
2	FW_COLLISION_MASKED_MIR	R	W	0	Mirror copy of corresponding bit in SAR_INTR_MASKED
3	DSI_COLLISION_MASKED_MIR	R	W	0	Mirror copy of corresponding bit in SAR_INTR_MASKED
4	INJ_EOC_MASKED_MIR	R	W	0	Mirror copy of corresponding bit in SAR_INTR_MASKED
5	INJ_SATURATE_MASKED_MIR	R	W	0	Mirror copy of corresponding bit in SAR_INTR_MASKED
6	INJ_RANGE_MASKED_MIR	R	W	0	Mirror copy of corresponding bit in SAR_INTR_MASKED
7	INJ_COLLISION_MASKED_MIR	R	W	0	Mirror copy of corresponding bit in SAR_INTR_MASKED
30	SATURATE_MASKED_RED	R	W	0	Reduction OR of all SAR_SATURATION_INTR_MASKED bits
31	RANGE_MASKED_RED	R	W	0	Reduction OR of all SAR_RANGE_INTR_MASKED bits

16.1.28 SAR_INJ_CHAN_CONFIG

Description: Injection channel configuration register.
Address: 0x403A0280
Offset: 0x280
Retention: Retained
IsDeepSleep: No
Comment: Intended use is firmware so no interaction with DSI.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:7]	INJ_PORT_ADDR [6:4]			None [3:3]	INJ_PIN_ADDR [2:0]		

Bits	15	14	13	12	11	10	9	8
Name	None [15:14]		INJ_SAMPLE_TIME_SEL [13:12]		None [11:11]	INJ_AVG_EN [10:10]	INJ_RESOLUTION [9:9]	INJ_DIFFERENTIAL_EN [8:8]

Bits	23	22	21	20	19	18	17	16
Name	None [23:23]	INJ_NEG_PORT_ADDR [22:20]			None [19:19]	INJ_NEG_PIN_ADDR [18:16]		

Bits	31	30	29	28	27	26	25	24
Name	INJ_START_EN [31:31]	INJ_TAILGATING [30:30]	INJ_DIAG_VMINUS_SINK [29:29]	INJ_DIAG_VMINUS_SOURCE [28:28]	INJ_DIAG_VPLUS_SINK [27:27]	INJ_DIAG_VPLUS_SOURCE [26:26]	None [25:25]	INJ_NEG_ADDR_EN [24:24]

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:2	INJ_PIN_ADDR	RW	R	0	Address of the pin to be sampled by this injection channel. If differential is enabled then INJ_PIN_ADDR[0] is ignored and considered to be 0, i.e. INJ_PIN_ADDR points to the even pin of a pin pair.
4:6	INJ_PORT_ADDR	RW	R	0	Address of the port that contains the pin to be sampled by this channel (connected to Vplus)
	SARMUX			0	SARMUX PORT pins. Select POS_PIN_ADDR 0-7 for GPIO 0-7 See DIFF_EN bit description for legacy differential mode
	CTB0			1	CTB0 Selet: POS_PIN_ADDR 2 for OA0 output (single ended) POS_PIN_ADDR 3 for OA1 outout (single ended) POS_PIN_ADDR 2 + DIFF_EN for OA0 on VP and OA1 on VN (differential)
	CSAMP_CH0			1	CSAMP Channel 0 Select POS_PIN ADDR 0 for CSAMP (SARBUS) input, always differential
	CTB1			2	CTB1 (see CTB0)
	CSAMP_CH1			2	CSAMP Channel 1 (See CSAMP Channel 0)
	CTB2			3	CTB2 (see CTB0)
	CSAMP_CH2			3	CSAMP Channel 2 (See CSAMP Channel 0)
	CTB3			4	CTB3 (see CTB0)
	CSAMP_CH3			4	CSAMP Channel 3 (See CSAMP Channel 0)
	EXPMUX			5	GPIO Expansion Mux (if present) See DIFF_EN bit description for legacy differential mode

Bits	Name	SW	HW	Default or Enum	Description
	DIAGMUX			6	Diagnostic inputs
	SARMUX_VIRT			7	SARMUX virtual port (VPORT0) Select POS_PIN_ADDR 0 for Temp Sensor Select POS_PIN_ADDR 2 for AMUXBUSA (single ended, test only) Select POS_PIN_ADDR 3 for AMUXBUSB (single ended, test only) Select POS_PIN_ADDR 2 + DIFF_EN for AMUXBUA on VP and AMUXBUS B on VN (differential, test only)
8	INJ_DIFFERENTIAL_EN	RW	R	0	Legacy differential mode, usage is described by port below: SARMUX: Legacy mode, use applications should use NEG_PORT/PIN_ADDR CTB0-3: Special purpose, see CTB0 description EXPMUX: Legacy mode, use applications should use NEG_PORT/PIN_ADDR DIAGMUX: Not applicable SARMUX_VIRT: Special purpose, see SARMUX_VIRT description LEGACY MODE DESCRIPTION: Differential enable for the selected port pin for this channel. If differential is enabled then POS_PIN_ADDR[0] is ignored and considered to be 0, i.e. POS_PIN_ADDR points to the even pin of a pin pair. For differential the even pin of the pair is connected to Vplus and the odd pin of the pair is connected to Vminus. POS_PORT_ADDR is used to identify the port that contains the pins. - 0: The voltage on the addressed pin is measured (Single-ended) and the resulting value is stored in the corresponding data register. - 1: The differential voltage on the addressed pin pair is measured and the resulting value is stored in the corresponding data register. (POS_PIN_ADDR[0] is ignored). NOTE: Set to 0 if using the NEG_PIN_ADDR and NEG_PORT_ADDR to select the negative source.
9	INJ_RESOLUTION	RW	R	0	Resolution for this channel.
	12B			0	12-bit resolution is used for this channel.
	SUBRES			1	The resolution specified by SUB_RESOLUTION in the SAR_SAMPLE_CTRL register is used for this channel.
10	INJ_AVG_EN	RW	R	0	Averaging enable for this channel. If set the AVG_CNT and AVG_SHIFT settings are used for sampling the addressed pin(s)
12:13	INJ_SAMPLE_TIME_SEL	RW	R	0	Injection sample time select: select which of the 4 global sample times to use for this channel
16:18	INJ_NEG_PIN_ADDR	RW	R	0	Address of the neg pin to be sampled by the injection channel.
20:22	INJ_NEG_PORT_ADDR	RW	R	0	Address of the neg port that contains the pin to be sampled by the injection channel.
	SARMUX			0	SARMUX pins.
	EXPMUX			5	GPIO Expansion Mux (if present)
	DIAGMUX			6	Diagnostic inputs
	SARMUX_VIRT			7	SARMUX virtual port (VPORT0)

Bits	Name	SW	HW	Default or Enum	Description
24	INJ_NEG_ADDR_EN	RW	R	0	1 - The NEG_PIN_ADDR and NEG_PORT_ADDR determines what drives the Vminus pin. This is a variation of differential mode with no even-odd pair limitation 0 - The NEG_SEL determines what drives the Vminus pin. DIFFERENTIAL_EN must be set to 0 for this feature to work correctly.
26	INJ_DIAG_VPLUS_SOURCE	RW	R	0	Enable for 10uA current source on vplus signal, active during sampling of this channel
27	INJ_DIAG_VPLUS_SINK	RW	R	0	Enable for 10uA current sink on vplus signal, active during sampling of this channel
28	INJ_DIAG_VMINUS_SOURCE	RW	R	0	Enable for 10uA current source on vminus signal, active during sampling of this channel
29	INJ_DIAG_VMINUS_SINK	RW	R	0	Enable for 10uA current sink on vminus signal, active during sampling of this channel
30	INJ_TAILGATING	RW	R	0	Injection channel tailgating. - 0: no tailgating for this channel, SAR is immediately triggered when the INJ_START_EN bit is set if the SAR is not busy. If the SAR is busy, the INJ channel addressed pin is sampled at the end of the current scan. - 1: injection channel tailgating. The addressed pin is sampled after the next trigger and after all enabled channels have been scanned.
31	INJ_START_EN	RW1S	RW1C	0	Set by firmware to enable the injection channel. If INJ_TAILGATING is not set this bit also functions as trigger for this channel. Cleared by hardware after this channel has been sampled (i.e. this channel is always one shot even if CONTINUOUS is set). Also cleared if the SAR is disabled. NOTE: If the intent is to trigger an injection channel with no tailgaiting (immediately if not busy), just prior to a firmware trigger, the following sequence must be followed to ensure that the injection channel starts first: - Trigger injection channel (set this bit to 1) - Poll for busy (wait for STATUS.SAR_BUSY == 1) - Trigger the scan (START_CTRL.FW_TRIGGER set to 1)

16.1.29 SAR_INJ_RESULT

Description: Injection channel result register
Address: 0x403A0290
Offset: 0x290
Retention: Not Retained
IsDeepSleep: No
Comment: Intended use is firmware only so double buffering is not considered needed here.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	INJ_RESULT [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	INJ_RESULT [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	INJ_EOC_INTR_MIR [31:31]	INJ_RANGE_INTR_MIR [30:30]	INJ_SATURATE_INTR_MIR [29:29]	INJ_COLLISION_INTR_MIR [28:28]	None [27:24]			

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:15	INJ_RESULT	R	W	Undefined	SAR conversion result of the channel.
28	INJ_COLLISION_INTR_MIR	R	W	0	mirror bit of corresponding bit in SAR_INTR register
29	INJ_SATURATE_INTR_MIR	R	W	0	mirror bit of corresponding bit in SAR_INTR register
30	INJ_RANGE_INTR_MIR	R	W	0	mirror bit of corresponding bit in SAR_INTR register
31	INJ_EOC_INTR_MIR	R	W	0	mirror bit of corresponding bit in SAR_INTR register

16.1.30 SAR_STATUS

Description: Current status of internal SAR registers (mostly for debug)
Address: 0x403A02A0
Offset: 0x2A0
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:6]		CUR_CHAN [5:0]					

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	BUSY [31:31]	SW_VREF_NEG [30:30]	None [29:24]					

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:5	CUR_CHAN	R	W	0	current channel being sampled (channel 16 indicates the injection channel), only valid if BUSY.
30	SW_VREF_NEG	R	W	0	the current switch status, including DSI and sequencer controls, of the switch in the SARADC that shorts NEG with VREF input (see NEG_SEL).
31	BUSY	R	W	0	If high then the SAR is busy with a conversion. This bit is always high when CONTINUOUS is set. Firmware should wait for this bit to be low before putting the SAR in power down.

16.1.31 SAR_AVG_STAT

Description: Current averaging status (for debug)
Address: 0x403A02A4
Offset: 0x2A4
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	CUR_AVG_ACCU [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	CUR_AVG_ACCU [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	INTRLV_BUSY [23:23]	None [22:20]			CUR_AVG_ACCU [19:16]			

Bits	31	30	29	28	27	26	25	24
Name	CUR_AVG_CNT [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:19	CUR_AVG_ACCU	R	W	0	the current value of the averaging accumulator
23	INTRLV_BUSY	R	W	0	If high then the SAR is in the middle of Interleaved averaging spanning several scans. While this bit is high the Firmware should not make any changes to the configuration registers otherwise some results may be incorrect. Note that the CUR_AVG_CNT status register below gives an indication how many more scans need to be done to complete the Interleaved averaging. This bit can be cleared by changing the averaging mode to ACCUNDUMP or by disabling the SAR.
24:31	CUR_AVG_CNT	R	W	0	the current value of the averaging counter. Note that the value shown is updated after the sampling time and therefore runs ahead of the accumulator update.

16.1.32 SAR_MUX_SWITCH0

Description: SARMUX Firmware switch controls
Address: 0x403A0300
Offset: 0x300
Retention: Retained
IsDeepSleep: No
Comment: Firmware control for SARMUX switches to connect analog signals to the SAR
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	MUX_FW_P7_VPLUS [7:7]	MUX_FW_P6_VPLUS [6:6]	MUX_FW_P5_VPLUS [5:5]	MUX_FW_P4_VPLUS [4:4]	MUX_FW_P3_VPLUS [3:3]	MUX_FW_P2_VPLUS [2:2]	MUX_FW_P1_VPLUS [1:1]	MUX_FW_P0_VPLUS [0:0]

Bits	15	14	13	12	11	10	9	8
Name	MUX_FW_P7_VMINUS [15:15]	MUX_FW_P6_VMINUS [14:14]	MUX_FW_P5_VMINUS [13:13]	MUX_FW_P4_VMINUS [12:12]	MUX_FW_P3_VMINUS [11:11]	MUX_FW_P2_VMINUS [10:10]	MUX_FW_P1_VMINUS [9:9]	MUX_FW_P0_VMINUS [8:8]

Bits	23	22	21	20	19	18	17	16
Name	MUX_FW_SARBUS1_VPLUS [23:23]	MUX_FW_SARBUS0_VPLUS [22:22]	MUX_FW_AMUXBUSB_VMINUS [21:21]	MUX_FW_AMUXBUSA_VMINUS [20:20]	MUX_FW_AMUXBUSB_VPLUS [19:19]	MUX_FW_AMUXBUSA_VPLUS [18:18]	MUX_FW_TEMP_VPLUS [17:17]	MUX_FW_VSSA_VMINUS [16:16]

Bits	31	30	29	28	27	26	25	24
Name	None [31:30]		MUX_FW_P7_COREIO3 [29:29]	MUX_FW_P6_COREIO2 [28:28]	MUX_FW_P5_COREIO1 [27:27]	MUX_FW_P4_COREIO0 [26:26]	MUX_FW_SARBUS1_VMINUS [25:25]	MUX_FW_SARBUS0_VMINUS [24:24]

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	MUX_FW_P0_VPLUS	RW1S	RW1C	0	Firmware control: 0=open, 1=close switch between pin P0 and vplus signal. Write with '1' to set bit.
1	MUX_FW_P1_VPLUS	RW1S	RW1C	0	Firmware control: 0=open, 1=close switch between pin P1 and vplus signal. Write with '1' to set bit.
2	MUX_FW_P2_VPLUS	RW1S	RW1C	0	Firmware control: 0=open, 1=close switch between pin P2 and vplus signal. Write with '1' to set bit.
3	MUX_FW_P3_VPLUS	RW1S	RW1C	0	Firmware control: 0=open, 1=close switch between pin P3 and vplus signal. Write with '1' to set bit.
4	MUX_FW_P4_VPLUS	RW1S	RW1C	0	Firmware control: 0=open, 1=close switch between pin P4 and vplus signal. Write with '1' to set bit.
5	MUX_FW_P5_VPLUS	RW1S	RW1C	0	Firmware control: 0=open, 1=close switch between pin P5 and vplus signal. Write with '1' to set bit.
6	MUX_FW_P6_VPLUS	RW1S	RW1C	0	Firmware control: 0=open, 1=close switch between pin P6 and vplus signal. Write with '1' to set bit.
7	MUX_FW_P7_VPLUS	RW1S	RW1C	0	Firmware control: 0=open, 1=close switch between pin P7 and vplus signal. Write with '1' to set bit.
8	MUX_FW_P0_VMINUS	RW1S	RW1C	0	Firmware control: 0=open, 1=close switch between pin P0 and vminus signal. Write with '1' to set bit.
9	MUX_FW_P1_VMINUS	RW1S	RW1C	0	Firmware control: 0=open, 1=close switch between pin P1 and vminus signal. Write with '1' to set bit.
10	MUX_FW_P2_VMINUS	RW1S	RW1C	0	Firmware control: 0=open, 1=close switch between pin P2 and vminus signal. Write with '1' to set bit.

Bits	Name	SW	HW	Default or Enum	Description
11	MUX_FW_P3_VMINUS	RW1S	RW1C	0	Firmware control: 0=open, 1=close switch between pin P3 and vminus signal. Write with '1' to set bit.
12	MUX_FW_P4_VMINUS	RW1S	RW1C	0	Firmware control: 0=open, 1=close switch between pin P4 and vminus signal. Write with '1' to set bit.
13	MUX_FW_P5_VMINUS	RW1S	RW1C	0	Firmware control: 0=open, 1=close switch between pin P5 and vminus signal. Write with '1' to set bit.
14	MUX_FW_P6_VMINUS	RW1S	RW1C	0	Firmware control: 0=open, 1=close switch between pin P6 and vminus signal. Write with '1' to set bit.
15	MUX_FW_P7_VMINUS	RW1S	RW1C	0	Firmware control: 0=open, 1=close switch between pin P7 and vminus signal. Write with '1' to set bit.
16	MUX_FW_VSSA _VMINUS	RW1S	RW1C	0	Firmware control: 0=open, 1=close switch between vssa_kelvin and vminus signal. Write with '1' to set bit.
17	MUX_FW_TEMP_VPLUS	RW1S	RW1C	0	Firmware control: 0=open, 1=close switch between temperature sensor and vplus signal, also powers on the temperature sensor. Write with '1' to set bit.
18	MUX_FW_AMUXBUSA _VPLUS	RW1S	RW1C	0	Firmware control: 0=open, 1=close switch between amuxbusa and vplus signal. Write with '1' to set bit.
19	MUX_FW_AMUXBUSB _VPLUS	RW1S	RW1C	0	Firmware control: 0=open, 1=close switch between amuxbusb and vplus signal. Write with '1' to set bit.
20	MUX_FW_AMUXBUSA _VMINUS	RW1S	RW1C	0	Firmware control: 0=open, 1=close switch between amuxbusa and vminus signal. Write with '1' to set bit.
21	MUX_FW_AMUXBUSB _VMINUS	RW1S	RW1C	0	Firmware control: 0=open, 1=close switch between amuxbusb and vminus signal. Write with '1' to set bit.
22	MUX_FW_SARBUS0 _VPLUS	RW1S	RW1C	0	Firmware control: 0=open, 1=close switch between sarbus0 and vplus signal. Write with '1' to set bit.
23	MUX_FW_SARBUS1 _VPLUS	RW1S	RW1C	0	Firmware control: 0=open, 1=close switch between sarbus1 and vplus signal. Write with '1' to set bit.
24	MUX_FW_SARBUS0 _VMINUS	RW1S	RW1C	0	Firmware control: 0=open, 1=close switch between sarbus0 and vminus signal. Write with '1' to set bit.
25	MUX_FW_SARBUS1 _VMINUS	RW1S	RW1C	0	Firmware control: 0=open, 1=close switch between sarbus1 and vminus signal. Write with '1' to set bit.
26	MUX_FW_P4_COREIO0	RW1S	RW1C	0	Firmware control: 0=open, 1=close switch between P4 and coreio0 signal. Write with '1' to set bit.
27	MUX_FW_P5_COREIO1	RW1S	RW1C	0	Firmware control: 0=open, 1=close switch between P5 and coreio1 signal. Write with '1' to set bit.
28	MUX_FW_P6_COREIO2	RW1S	RW1C	0	Firmware control: 0=open, 1=close switch between P6 and coreio2 signal. Write with '1' to set bit.
29	MUX_FW_P7_COREIO3	RW1S	RW1C	0	Firmware control: 0=open, 1=close switch between P7 and coreio3 signal. Write with '1' to set bit.

16.1.33 SAR_MUX_SWITCH_CLEAR0

Description: SARMUX Firmware switch control clear
Address: 0x403A0304
Offset: 0x304
Retention: Retained
IsDeepSleep: No
Comment: Not really a register, when read gives value from MUX_SWITCH0
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	MUX_FW_P7_VPLUS [7:7]	MUX_FW_P6_VPLUS [6:6]	MUX_FW_P5_VPLUS [5:5]	MUX_FW_P4_VPLUS [4:4]	MUX_FW_P3_VPLUS [3:3]	MUX_FW_P2_VPLUS [2:2]	MUX_FW_P1_VPLUS [1:1]	MUX_FW_P0_VPLUS [0:0]

Bits	15	14	13	12	11	10	9	8
Name	MUX_FW_P7_VMINUS [15:15]	MUX_FW_P6_VMINUS [14:14]	MUX_FW_P5_VMINUS [13:13]	MUX_FW_P4_VMINUS [12:12]	MUX_FW_P3_VMINUS [11:11]	MUX_FW_P2_VMINUS [10:10]	MUX_FW_P1_VMINUS [9:9]	MUX_FW_P0_VMINUS [8:8]

Bits	23	22	21	20	19	18	17	16
Name	MUX_FW_SARBUS1_VPLUS [23:23]	MUX_FW_SARBUS0_VPLUS [22:22]	MUX_FW_AMUXBUSB_VMINUS [21:21]	MUX_FW_AMUXBUSA_VMINUS [20:20]	MUX_FW_AMUXBUSB_VPLUS [19:19]	MUX_FW_AMUXBUSA_VPLUS [18:18]	MUX_FW_TEMP_VPLUS [17:17]	MUX_FW_VSSA_VMINUS [16:16]

Bits	31	30	29	28	27	26	25	24
Name	None [31:30]		MUX_FW_P7_COREIO3 [29:29]	MUX_FW_P6_COREIO2 [28:28]	MUX_FW_P5_COREIO1 [27:27]	MUX_FW_P4_COREIO0 [26:26]	MUX_FW_SARBUS1_VMINUS [25:25]	MUX_FW_SARBUS0_VMINUS [24:24]

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	MUX_FW_P0_VPLUS	RW1C	A	0	Write '1' to clear corresponding bit in MUX_SWITCH0
1	MUX_FW_P1_VPLUS	RW1C	A	0	Write '1' to clear corresponding bit in MUX_SWITCH0
2	MUX_FW_P2_VPLUS	RW1C	A	0	Write '1' to clear corresponding bit in MUX_SWITCH0
3	MUX_FW_P3_VPLUS	RW1C	A	0	Write '1' to clear corresponding bit in MUX_SWITCH0
4	MUX_FW_P4_VPLUS	RW1C	A	0	Write '1' to clear corresponding bit in MUX_SWITCH0
5	MUX_FW_P5_VPLUS	RW1C	A	0	Write '1' to clear corresponding bit in MUX_SWITCH0
6	MUX_FW_P6_VPLUS	RW1C	A	0	Write '1' to clear corresponding bit in MUX_SWITCH0
7	MUX_FW_P7_VPLUS	RW1C	A	0	Write '1' to clear corresponding bit in MUX_SWITCH0
8	MUX_FW_P0_VMINUS	RW1C	A	0	Write '1' to clear corresponding bit in MUX_SWITCH0
9	MUX_FW_P1_VMINUS	RW1C	A	0	Write '1' to clear corresponding bit in MUX_SWITCH0
10	MUX_FW_P2_VMINUS	RW1C	A	0	Write '1' to clear corresponding bit in MUX_SWITCH0
11	MUX_FW_P3_VMINUS	RW1C	A	0	Write '1' to clear corresponding bit in MUX_SWITCH0
12	MUX_FW_P4_VMINUS	RW1C	A	0	Write '1' to clear corresponding bit in MUX_SWITCH0
13	MUX_FW_P5_VMINUS	RW1C	A	0	Write '1' to clear corresponding bit in MUX_SWITCH0
14	MUX_FW_P6_VMINUS	RW1C	A	0	Write '1' to clear corresponding bit in MUX_SWITCH0
15	MUX_FW_P7_VMINUS	RW1C	A	0	Write '1' to clear corresponding bit in MUX_SWITCH0
16	MUX_FW_VSSA_VMINUS	RW1C	A	0	Write '1' to clear corresponding bit in MUX_SWITCH0
17	MUX_FW_TEMP_VPLUS	RW1C	A	0	Write '1' to clear corresponding bit in MUX_SWITCH0

Bits	Name	SW	HW	Default or Enum	Description
18	MUX_FW_AMUXBUSA_VPLUS	RW1C	A	0	Write '1' to clear corresponding bit in MUX_SWITCH0
19	MUX_FW_AMUXBUSB_VPLUS	RW1C	A	0	Write '1' to clear corresponding bit in MUX_SWITCH0
20	MUX_FW_AMUXBUSA_VMINUS	RW1C	A	0	Write '1' to clear corresponding bit in MUX_SWITCH0
21	MUX_FW_AMUXBUSB_VMINUS	RW1C	A	0	Write '1' to clear corresponding bit in MUX_SWITCH0
22	MUX_FW_SARBUS0_VPLUS	RW1C	A	0	Write '1' to clear corresponding bit in MUX_SWITCH0
23	MUX_FW_SARBUS1_VPLUS	RW1C	A	0	Write '1' to clear corresponding bit in MUX_SWITCH0
24	MUX_FW_SARBUS0_VMINUS	RW1C	A	0	Write '1' to clear corresponding bit in MUX_SWITCH0
25	MUX_FW_SARBUS1_VMINUS	RW1C	A	0	Write '1' to clear corresponding bit in MUX_SWITCH0
26	MUX_FW_P4_COREIO0	RW1C	A	0	Write '1' to clear corresponding bit in MUX_SWITCH0
27	MUX_FW_P5_COREIO1	RW1C	A	0	Write '1' to clear corresponding bit in MUX_SWITCH0
28	MUX_FW_P6_COREIO2	RW1C	A	0	Write '1' to clear corresponding bit in MUX_SWITCH0
29	MUX_FW_P7_COREIO3	RW1C	A	0	Write '1' to clear corresponding bit in MUX_SWITCH0

16.1.34 SAR_MUX_SWITCH1

Description: SARMUX Firmware switch controls
Address: 0x403A0308
Offset: 0x308
Retention: Retained
IsDeepSleep: No
Comment: Firmware control for SARMUX switches to connect analog signals to the SAR
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:4]				MUX_FW_ADFT1_SARBUS1 [3:3]	MUX_FW_ADFT0_SARBUS0 [2:2]	MUX_FW_P5_DFT_INM [1:1]	MUX_FW_P4_DFT_INP [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	MUX_FW_P4_DFT_INP	RW1S	RW1C	0	Firmware control: 0=open, 1=close switch between P4 pin and dft_inp signal. Write with '1' to set bit.
1	MUX_FW_P5_DFT_INM	RW1S	RW1C	0	Firmware control: 0=open, 1=close switch between P5 pin and dft_inm signal. Write with '1' to set bit.
2	MUX_FW_ADFT0_SARBUS0	RW1S	RW1C	0	Firmware control: 0=open, 1=close switch between adft0 signal and sarbus0 signal. Write with '1' to set bit.
3	MUX_FW_ADFT1_SARBUS1	RW1S	RW1C	0	Firmware control: 0=open, 1=close switch between adft1 signal and sarbus1 signal. Write with '1' to set bit.

16.1.35 SAR_MUX_SWITCH_CLEAR1

Description: SARMUX Firmware switch control clear
Address: 0x403A030C
Offset: 0x30C
Retention: Retained
IsDeepSleep: No
Comment: Not really a register, when read gives value from MUX_SWITCH1
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:4]				MUX_FW_ADFT1_SARBUS1 [3:3]	MUX_FW_ADFT0_SARBUS0 [2:2]	MUX_FW_P5_DFT_INM [1:1]	MUX_FW_P4_DFT_INP [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	MUX_FW_P4_DFT_INP	RW1C	A	0	Write '1' to clear corresponding bit in MUX_SWITCH1
1	MUX_FW_P5_DFT_INM	RW1C	A	0	Write '1' to clear corresponding bit in MUX_SWITCH1
2	MUX_FW_ADFT0_SARBUS0	RW1C	A	0	Write '1' to clear corresponding bit in MUX_SWITCH1
3	MUX_FW_ADFT1_SARBUS1	RW1C	A	0	Write '1' to clear corresponding bit in MUX_SWITCH1

16.1.36 SAR_MUX_SWITCH2

Description: EXPMUX and DIAGMUX Firmware switch controls
Address: 0x403A0310
Offset: 0x310
Retention: Retained
IsDeepSleep: No
Comment: Firmware control for EXPMUX and DIAGMUX switches to connect analog signals to the SAR
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	MUX_FW_VD7_VPLUS [23:23]	MUX_FW_VD6_VPLUS [22:22]	MUX_FW_VD5_VPLUS [21:21]	MUX_FW_VD4_VPLUS [20:20]	MUX_FW_VD3_VPLUS [19:19]	MUX_FW_VD2_VPLUS [18:18]	MUX_FW_VD1_VPLUS [17:17]	MUX_FW_VD0_VPLUS [16:16]

Bits	31	30	29	28	27	26	25	24
Name	MUX_FW_CSINK_VMINUS [31:31]	MUX_FW_CSRC_VMINUS [30:30]	MUX_FW_CSINK_VPLUS [29:29]	MUX_FW_CSRC_VPLUS [28:28]	MUX_FW_VG3_VMINUS [27:27]	MUX_FW_VG2_VMINUS [26:26]	MUX_FW_VG1_VMINUS [25:25]	MUX_FW_VG0_VMINUS [24:24]

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
16	MUX_FW_VD0_VPLUS	RW1S	RW1C	0	Firmware control: 0=open, 1=close switch between internal Vdiag.0 and vplus signal . Write with '1' to set bit.
17	MUX_FW_VD1_VPLUS	RW1S	RW1C	0	Firmware control: 0=open, 1=close switch between internal Vdiag.1 and vplus signal . Write with '1' to set bit.
18	MUX_FW_VD2_VPLUS	RW1S	RW1C	0	Firmware control: 0=open, 1=close switch between internal Vdiag.2 and vplus signal . Write with '1' to set bit.
19	MUX_FW_VD3_VPLUS	RW1S	RW1C	0	Firmware control: 0=open, 1=close switch between internal Vdiag.3 and vplus signal . Write with '1' to set bit.
20	MUX_FW_VD4_VPLUS	RW1S	RW1C	0	Firmware control: 0=open, 1=close switch between internal Vdiag.4 and vplus signal . Write with '1' to set bit.
21	MUX_FW_VD5_VPLUS	RW1S	RW1C	0	Firmware control: 0=open, 1=close switch between internal Vdiag.5 and vplus signal . Write with '1' to set bit.
22	MUX_FW_VD6_VPLUS	RW1S	RW1C	0	Firmware control: 0=open, 1=close switch between internal Vdiag.6 and vplus signal . Write with '1' to set bit.
23	MUX_FW_VD7_VPLUS	RW1S	RW1C	0	Firmware control: 0=open, 1=close switch between internal Vdiag.7 and vplus signal . Write with '1' to set bit.
24	MUX_FW_VG0_VMINUS	RW1S	RW1C	0	Firmware control: 0=open, 1=close switch between internal Vgnd.0 and vplus signal . Write with '1' to set bit.

Bits	Name	SW	HW	Default or Enum	Description
25	MUX_FW_VG1_VMINUS	RW1S	RW1C	0	Firmware control: 0=open, 1=close switch between internal Vgnd.1 and vplus signal . Write with '1' to set bit.
26	MUX_FW_VG2_VMINUS	RW1S	RW1C	0	Firmware control: 0=open, 1=close switch between internal Vgnd.2 and vplus signal . Write with '1' to set bit.
27	MUX_FW_VG3_VMINUS	RW1S	RW1C	0	Firmware control: 0=open, 1=close switch between internal Vgnd.3 and vplus signal . Write with '1' to set bit.
28	MUX_FW_CSRC_VPLUS	RW1S	RW1C	0	Firmware control: 0=open, 1=close switch between 10uA current source and the vplus signal Write with '1' to set bit.
29	MUX_FW_CSINK_VPLUS	RW1S	RW1C	0	Firmware control: 0=open, 1=close switch between 10uA current sink and the vplus signal Write with '1' to set bit.
30	MUX_FW_CSRC _VMINUS	RW1S	RW1C	0	Firmware control: 0=open, 1=close switch between 10uA current source and the vplus signal Write with '1' to set bit.
31	MUX_FW_CSINK _VMINUS	RW1S	RW1C	0	Firmware control: 0=open, 1=close switch between 10uA current sink and the vminus signal Write with '1' to set bit.

16.1.37 SAR_MUX_SWITCH_CLEAR2

Description: EXPMUX and DIAGMUX Firmware switch control clear
Address: 0x403A0314
Offset: 0x314
Retention: Retained
IsDeepSleep: No
Comment: Not really a register, when read gives value from MUX_SWITCH2
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	MUX_FW_VD7_VPLUS [23:23]	MUX_FW_VD6_VPLUS [22:22]	MUX_FW_VD5_VPLUS [21:21]	MUX_FW_VD4_VPLUS [20:20]	MUX_FW_VD3_VPLUS [19:19]	MUX_FW_VD2_VPLUS [18:18]	MUX_FW_VD1_VPLUS [17:17]	MUX_FW_VD0_VPLUS [16:16]

Bits	31	30	29	28	27	26	25	24
Name	MUX_FW_CSINK_VMINUS [31:31]	MUX_FW_CSRC_VMINUS [30:30]	MUX_FW_CSINK_VPLUS [29:29]	MUX_FW_CSRC_VPLUS [28:28]	MUX_FW_VG3_VMINUS [27:27]	MUX_FW_VG2_VMINUS [26:26]	MUX_FW_VG1_VMINUS [25:25]	MUX_FW_VG0_VMINUS [24:24]

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
16	MUX_FW_VD0_VPLUS	RW1C	A	0	Write '1' to clear corresponding bit in MUX_SWITCH2
17	MUX_FW_VD1_VPLUS	RW1C	A	0	Write '1' to clear corresponding bit in MUX_SWITCH2
18	MUX_FW_VD2_VPLUS	RW1C	A	0	Write '1' to clear corresponding bit in MUX_SWITCH2
19	MUX_FW_VD3_VPLUS	RW1C	A	0	Write '1' to clear corresponding bit in MUX_SWITCH2
20	MUX_FW_VD4_VPLUS	RW1C	A	0	Write '1' to clear corresponding bit in MUX_SWITCH2
21	MUX_FW_VD5_VPLUS	RW1C	A	0	Write '1' to clear corresponding bit in MUX_SWITCH2
22	MUX_FW_VD6_VPLUS	RW1C	A	0	Write '1' to clear corresponding bit in MUX_SWITCH2
23	MUX_FW_VD7_VPLUS	RW1C	A	0	Write '1' to clear corresponding bit in MUX_SWITCH2
24	MUX_FW_VG0_VMINUS	RW1C	A	0	Write '1' to clear corresponding bit in MUX_SWITCH2
25	MUX_FW_VG1_VMINUS	RW1C	A	0	Write '1' to clear corresponding bit in MUX_SWITCH2
26	MUX_FW_VG2_VMINUS	RW1C	A	0	Write '1' to clear corresponding bit in MUX_SWITCH2
27	MUX_FW_VG3_VMINUS	RW1C	A	0	Write '1' to clear corresponding bit in MUX_SWITCH2
28	MUX_FW_CSRC_VPLUS	RW1C	A	0	Write '1' to clear corresponding bit in MUX_SWITCH2
29	MUX_FW_CSINK_VPLUS	RW1C	A	0	Write '1' to clear corresponding bit in MUX_SWITCH2
30	MUX_FW_CSRC_VMINUS	RW1C	A	0	Write '1' to clear corresponding bit in MUX_SWITCH2
31	MUX_FW_CSINK_VMINUS	RW1C	A	0	Write '1' to clear corresponding bit in MUX_SWITCH2

16.1.38 SAR_MUX_SWITCH_HW_CTRL

Description: SARMUX switch hardware control
Address: 0x403A0340
Offset: 0x340
Retention: Retained
IsDeepSleep: No
Comment: Allow hardware control for SARMUX switches
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	MUX_HW_CTRL_P7 [7:7]	MUX_HW_CTRL_P6 [6:6]	MUX_HW_CTRL_P5 [5:5]	MUX_HW_CTRL_P4 [4:4]	MUX_HW_CTRL_P3 [3:3]	MUX_HW_CTRL_P2 [2:2]	MUX_HW_CTRL_P1 [1:1]	MUX_HW_CTRL_P0 [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	MUX_HW_CTRL_SARBUS1 [23:23]	MUX_HW_CTRL_SARBUS0 [22:22]	None [21:20]		MUX_HW_CTRL_AMUXBUSB [19:19]	MUX_HW_CTRL_AMUXBUSA [18:18]	MUX_HW_CTRL_TEMP [17:17]	MUX_HW_CTRL_VSSA [16:16]

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	MUX_HW_CTRL_P0	RW	R	0	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for pin P0 switches.
1	MUX_HW_CTRL_P1	RW	R	0	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for pin P1 switches.
2	MUX_HW_CTRL_P2	RW	R	0	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for pin P2 switches.
3	MUX_HW_CTRL_P3	RW	R	0	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for pin P3 switches.
4	MUX_HW_CTRL_P4	RW	R	0	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for pin P4 switches.
5	MUX_HW_CTRL_P5	RW	R	0	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for pin P5 switches.
6	MUX_HW_CTRL_P6	RW	R	0	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for pin P6 switches.
7	MUX_HW_CTRL_P7	RW	R	0	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for pin P7 switches.
16	MUX_HW_CTRL_VSSA	RW	R	0	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for vssa switch.
17	MUX_HW_CTRL_TEMP	RW	R	0	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for temp switch.

Bits	Name	SW	HW	Default or Enum	Description
18	MUX_HW_CTRL _AMUXBUSA	RW	R	0	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for amuxbusa switches.
19	MUX_HW_CTRL _AMUXBUSB	RW	R	0	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for amuxbusb switches.
22	MUX_HW_CTRL _SARBUS0	RW	R	0	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for sarbus0 switches.
23	MUX_HW_CTRL _SARBUS1	RW	R	0	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for sarbus1 switches.

16.1.39 SAR_MUX_SWITCH_HW_CTRL2

Description: EXPMUX and DIAGMUX switch hardware control
Address: 0x403A0344
Offset: 0x344
Retention: Retained
IsDeepSleep: No
Comment: Allow hardware control for EXPMUX and DIAGMUX switches
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	MUX_FW_VD7 [23:23]	MUX_FW_VD6 [22:22]	MUX_FW_VD5 [21:21]	MUX_FW_VD4 [20:20]	MUX_FW_VD3_VG3 [19:19]	MUX_FW_VD2_VG2 [18:18]	MUX_FW_VD1_VG1 [17:17]	MUX_FW_VD0_VG0 [16:16]

Bits	31	30	29	28	27	26	25	24
Name	MUX_FW_CSINK_VMINUS [31:31]	MUX_FW_CSRC_VMINUS [30:30]	MUX_FW_CSINK_VPLUS [29:29]	MUX_FW_CSRC_VPLUS [28:28]	None [27:24]			

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
16	MUX_FW_VD0_VG0	RW	R	0	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for Vdiag.0 and Vgnd.0 switches
17	MUX_FW_VD1_VG1	RW	R	0	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for Vdiag.1 and Vgnd.1 switches
18	MUX_FW_VD2_VG2	RW	R	0	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for Vdiag.2 and Vgnd.2 switches
19	MUX_FW_VD3_VG3	RW	R	0	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for Vdiag.3 and Vgnd.3 switches
20	MUX_FW_VD4	RW	R	0	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for Vdiag.4 switch.
21	MUX_FW_VD5	RW	R	0	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for Vdiag.5 switch.
22	MUX_FW_VD6	RW	R	0	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for Vdiag.6 switch.
23	MUX_FW_VD7	RW	R	0	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for Vdiag.7 switch.
28	MUX_FW_CSRC_VPLUS	RW	R	0	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting to close switch between 10uA current source and the vplus signal.

Bits	Name	SW	HW	Default or Enum	Description
29	MUX_FW_CSINK_VPLUS	RW	R	0	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for close switch between 10uA current sink and the vplus signal.
30	MUX_FW_CSRC _VMINUS	RW	R	0	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for close switch between 10uA current source and the vminus signal.
31	MUX_FW_CSINK _VMINUS	RW	R	0	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting to close switch between 10uA current sink and the vminus signal.

16.1.40 SAR_MUX_SWITCH_STATUS

Description: SARMUX switch status
Address: 0x403A0350
Offset: 0x350
Retention: Retained
IsDeepSleep: No
Comment: gives the current switch status including Firmware (MUX_SWITCH00 register), DSI and sequencer controls
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	MUX_FW_P7_VPLUS [7:7]	MUX_FW_P6_VPLUS [6:6]	MUX_FW_P5_VPLUS [5:5]	MUX_FW_P4_VPLUS [4:4]	MUX_FW_P3_VPLUS [3:3]	MUX_FW_P2_VPLUS [2:2]	MUX_FW_P1_VPLUS [1:1]	MUX_FW_P0_VPLUS [0:0]

Bits	15	14	13	12	11	10	9	8
Name	MUX_FW_P7_VMINUS [15:15]	MUX_FW_P6_VMINUS [14:14]	MUX_FW_P5_VMINUS [13:13]	MUX_FW_P4_VMINUS [12:12]	MUX_FW_P3_VMINUS [11:11]	MUX_FW_P2_VMINUS [10:10]	MUX_FW_P1_VMINUS [9:9]	MUX_FW_P0_VMINUS [8:8]

Bits	23	22	21	20	19	18	17	16
Name	MUX_FW_SARBUS1_VPLUS [23:23]	MUX_FW_SARBUS0_VPLUS [22:22]	MUX_FW_AMUXBUSB_VMINUS [21:21]	MUX_FW_AMUXBUSA_VMINUS [20:20]	MUX_FW_AMUXBUSB_VPLUS [19:19]	MUX_FW_AMUXBUSA_VPLUS [18:18]	MUX_FW_TEMP_VPLUS [17:17]	MUX_FW_VSSA_VMINUS [16:16]

Bits	31	30	29	28	27	26	25	24
Name	None [31:26]						MUX_FW_SARBUS1_VMINUS [25:25]	MUX_FW_SARBUS0_VMINUS [24:24]

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	MUX_FW_P0_VPLUS	R	W	0	switch status of corresponding bit in MUX_SWITCH0
1	MUX_FW_P1_VPLUS	R	W	0	switch status of corresponding bit in MUX_SWITCH0
2	MUX_FW_P2_VPLUS	R	W	0	switch status of corresponding bit in MUX_SWITCH0
3	MUX_FW_P3_VPLUS	R	W	0	switch status of corresponding bit in MUX_SWITCH0
4	MUX_FW_P4_VPLUS	R	W	0	switch status of corresponding bit in MUX_SWITCH0
5	MUX_FW_P5_VPLUS	R	W	0	switch status of corresponding bit in MUX_SWITCH0
6	MUX_FW_P6_VPLUS	R	W	0	switch status of corresponding bit in MUX_SWITCH0
7	MUX_FW_P7_VPLUS	R	W	0	switch status of corresponding bit in MUX_SWITCH0
8	MUX_FW_P0_VMINUS	R	W	0	switch status of corresponding bit in MUX_SWITCH0
9	MUX_FW_P1_VMINUS	R	W	0	switch status of corresponding bit in MUX_SWITCH0
10	MUX_FW_P2_VMINUS	R	W	0	switch status of corresponding bit in MUX_SWITCH0
11	MUX_FW_P3_VMINUS	R	W	0	switch status of corresponding bit in MUX_SWITCH0
12	MUX_FW_P4_VMINUS	R	W	0	switch status of corresponding bit in MUX_SWITCH0
13	MUX_FW_P5_VMINUS	R	W	0	switch status of corresponding bit in MUX_SWITCH0
14	MUX_FW_P6_VMINUS	R	W	0	switch status of corresponding bit in MUX_SWITCH0
15	MUX_FW_P7_VMINUS	R	W	0	switch status of corresponding bit in MUX_SWITCH0
16	MUX_FW_VSSA_VMINUS	R	W	0	switch status of corresponding bit in MUX_SWITCH0
17	MUX_FW_TEMP_VPLUS	R	W	0	switch status of corresponding bit in MUX_SWITCH0

Bits	Name	SW	HW	Default or Enum	Description
18	MUX_FW_AMUXBUSA_VPLUS	R	W	0	switch status of corresponding bit in MUX_SWITCH0
19	MUX_FW_AMUXBUSB_VPLUS	R	W	0	switch status of corresponding bit in MUX_SWITCH0
20	MUX_FW_AMUXBUSA_VMINUS	R	W	0	switch status of corresponding bit in MUX_SWITCH0
21	MUX_FW_AMUXBUSB_VMINUS	R	W	0	switch status of corresponding bit in MUX_SWITCH0
22	MUX_FW_SARBUS0_VPLUS	R	W	0	switch status of corresponding bit in MUX_SWITCH0
23	MUX_FW_SARBUS1_VPLUS	R	W	0	switch status of corresponding bit in MUX_SWITCH0
24	MUX_FW_SARBUS0_VMINUS	R	W	0	switch status of corresponding bit in MUX_SWITCH0
25	MUX_FW_SARBUS1_VMINUS	R	W	0	switch status of corresponding bit in MUX_SWITCH0

16.1.41 SAR_MUX_SWITCH_STATUS2

Description: EXPMUX and DIAGMUX switch status
Address: 0x403A0354
Offset: 0x354
Retention: Retained
IsDeepSleep: No
Comment: gives the current switch status including Firmware (MUX_SWITCH2 register), and sequencer controls
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	MUX_FW_VD7_VPLUS [23:23]	MUX_FW_VD6_VPLUS [22:22]	MUX_FW_VD5_VPLUS [21:21]	MUX_FW_VD4_VPLUS [20:20]	MUX_FW_VD3_VPLUS [19:19]	MUX_FW_VD2_VPLUS [18:18]	MUX_FW_VD1_VPLUS [17:17]	MUX_FW_VD0_VPLUS [16:16]

Bits	31	30	29	28	27	26	25	24
Name	MUX_FW_CSINK_VMINUS [31:31]	MUX_FW_CSRC_VMINUS [30:30]	MUX_FW_CSINK_VPLUS [29:29]	MUX_FW_CSRC_VPLUS [28:28]	MUX_FW_VG3_VMINUS [27:27]	MUX_FW_VG2_VMINUS [26:26]	MUX_FW_VG1_VMINUS [25:25]	MUX_FW_VG0_VMINUS [24:24]

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
16	MUX_FW_VD0_VPLUS	R	W	0	switch status of corresponding bit in MUX_SWITCH2
17	MUX_FW_VD1_VPLUS	R	W	0	switch status of corresponding bit in MUX_SWITCH2
18	MUX_FW_VD2_VPLUS	R	W	0	switch status of corresponding bit in MUX_SWITCH2
19	MUX_FW_VD3_VPLUS	R	W	0	switch status of corresponding bit in MUX_SWITCH2
20	MUX_FW_VD4_VPLUS	R	W	0	switch status of corresponding bit in MUX_SWITCH2
21	MUX_FW_VD5_VPLUS	R	W	0	switch status of corresponding bit in MUX_SWITCH2
22	MUX_FW_VD6_VPLUS	R	W	0	switch status of corresponding bit in MUX_SWITCH2
23	MUX_FW_VD7_VPLUS	R	W	0	switch status of corresponding bit in MUX_SWITCH2
24	MUX_FW_VG0_VMINUS	R	W	0	switch status of corresponding bit in MUX_SWITCH2
25	MUX_FW_VG1_VMINUS	R	W	0	switch status of corresponding bit in MUX_SWITCH2
26	MUX_FW_VG2_VMINUS	R	W	0	switch status of corresponding bit in MUX_SWITCH2
27	MUX_FW_VG3_VMINUS	R	W	0	switch status of corresponding bit in MUX_SWITCH2
28	MUX_FW_CSRC_VPLUS	R	W	0	switch status of corresponding bit in MUX_SWITCH2
29	MUX_FW_CSINK_VPLUS	R	W	0	switch status of corresponding bit in MUX_SWITCH2
30	MUX_FW_CSRC_VMINUS	R	W	0	switch status of corresponding bit in MUX_SWITCH2
31	MUX_FW_CSINK_VMINUS	R	W	0	switch status of corresponding bit in MUX_SWITCH2

16.1.42 SAR_PUMP_CTRL

Description: Switch pump control
Address: 0x403A0380
Offset: 0x380
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:1]							CLOCK _SEL [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	ENABLED [31:31]	None [30:24]						

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	CLOCK_SEL	RW	R	0	Clock select: 0=external clock, 1=internal clock (deprecated).
31	ENABLED	RW	R	0	0=disabled: pump output is VDDA_PUMP, 1=enabled: pump output is boosted.

16.1.43 SAR_ANA_TRIM

Description: Analog trim register.
Address: 0x403AFF00
Offset: 0xFF00
Retention: Retained
IsDeepSleep: No
Comment: Based on pin out of the analog s8sar IP, not sure if this is sufficient or needed, this contains trim values and user firmware is not supposed to change it.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:4]				TRIMUNIT [3:3]	CAP_TRIM [2:0]		

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:2	CAP_TRIM	RW	R	0	Attenuation cap trimming
3	TRIMUNIT	RW	R	0	Attenuation cap trimming

16.1.44 SAR_WOUNDING

Description: SAR wounding register
Address: 0x403AFF04
Offset: 0xFF04
Retention: Retained
IsDeepSleep: No
Comment: Indicates current wounding mode for SAR. The wounding bits are loaded from supervisory flash area during boot.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:2]						WOUND_RESOLUTION [1:0]	

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:1	WOUND_RESOLUTION	RW1S	R	0	Maximum SAR resolution allowed
	12BIT			0	unwounded: up to full 12-bit SAR resolution allowed
	10BIT			1	wounded: max resolution upto 10-bit SAR resolution allowed
	8BIT			2	wounded: only 8-bit SAR resolution allowed
	8BIT_TOO			3	wounded: only 8-bit SAR resolution allowed

17 SCB

17.1 SCB 0

Description Serial Communications Block (SPI/UART/I2C)
Base Address 0x40240000
Size 0x10000
Slave Num MMIO1

Register Name	Address	Permission	Description
SCB0_CTRL	0x40240000	FULL	Generic control register.
SCB0_STATUS	0x40240004	FULL	Generic status register.
SCB0_CMD_RESP_CTRL	0x40240008	FULL	Command/response control register.
SCB0_CMD_RESP_STATUS	0x4024000C	FULL	Command/response status register.
SCB0_SPI_CTRL	0x40240020	FULL	SPI control register.
SCB0_SPI_STATUS	0x40240024	FULL	SPI status register.
SCB0_UART_CTRL	0x40240040	FULL	UART control register.
SCB0_UART_TX_CTRL	0x40240044	FULL	UART transmitter control register.
SCB0_UART_RX_CTRL	0x40240048	FULL	UART receiver control register.
SCB0_UART_RX_STATUS	0x4024004C	FULL	UART receiver status register.
SCB0_UART_FLOW_CTRL	0x40240050	FULL	UART flow control register
SCB0_I2C_CTRL	0x40240060	FULL	I2C control register.
SCB0_I2C_STATUS	0x40240064	FULL	I2C status register.
SCB0_I2C_M_CMD	0x40240068	FULL	I2C master command register.
SCB0_I2C_S_CMD	0x4024006C	FULL	I2C slave command register.
SCB0_I2C_CFG	0x40240070	FULL	I2C configuration register.
SCB0_TX_CTRL	0x40240200	FULL	Transmitter control register.
SCB0_TX_FIFO_CTRL	0x40240204	FULL	Transmitter FIFO control register.
SCB0_TX_FIFO_STATUS	0x40240208	FULL	Transmitter FIFO status register.
SCB0_TX_FIFO_WR	0x40240240	FULL	Transmitter FIFO write register.
SCB0_RX_CTRL	0x40240300	FULL	Receiver control register.
SCB0_RX_FIFO_CTRL	0x40240304	FULL	Receiver FIFO control register.
SCB0_RX_FIFO_STATUS	0x40240308	FULL	Receiver FIFO status register.
SCB0_RX_MATCH	0x40240310	FULL	Slave address and mask register.
SCB0_RX_FIFO_RD	0x40240340	FULL	Receiver FIFO read register.
SCB0_RX_FIFO_RD_SILENT	0x40240344	FULL	Receiver FIFO read register.
SCB0_EZ_DATA0	0x40240400	FULL	Memory buffer registers.
SCB0_EZ_DATA1	0x40240404	FULL	Memory buffer registers.
SCB0_EZ_DATA2	0x40240408	FULL	Memory buffer registers.
SCB0_EZ_DATA3	0x4024040C	FULL	Memory buffer registers.
SCB0_EZ_DATA4	0x40240410	FULL	Memory buffer registers.
SCB0_EZ_DATA5	0x40240414	FULL	Memory buffer registers.
SCB0_EZ_DATA6	0x40240418	FULL	Memory buffer registers.
SCB0_EZ_DATA7	0x4024041C	FULL	Memory buffer registers.
SCB0_EZ_DATA8	0x40240420	FULL	Memory buffer registers.
SCB0_EZ_DATA9	0x40240424	FULL	Memory buffer registers.
SCB0_EZ_DATA10	0x40240428	FULL	Memory buffer registers.
SCB0_EZ_DATA11	0x4024042C	FULL	Memory buffer registers.
SCB0_EZ_DATA12	0x40240430	FULL	Memory buffer registers.
SCB0_EZ_DATA13	0x40240434	FULL	Memory buffer registers.
SCB0_EZ_DATA14	0x40240438	FULL	Memory buffer registers.
SCB0_EZ_DATA15	0x4024043C	FULL	Memory buffer registers.
SCB0_EZ_DATA16	0x40240440	FULL	Memory buffer registers.
SCB0_EZ_DATA17	0x40240444	FULL	Memory buffer registers.
SCB0_EZ_DATA18	0x40240448	FULL	Memory buffer registers.
SCB0_EZ_DATA19	0x4024044C	FULL	Memory buffer registers.
SCB0_EZ_DATA20	0x40240450	FULL	Memory buffer registers.
SCB0_EZ_DATA21	0x40240454	FULL	Memory buffer registers.
SCB0_EZ_DATA22	0x40240458	FULL	Memory buffer registers.
SCB0_EZ_DATA23	0x4024045C	FULL	Memory buffer registers.
SCB0_EZ_DATA24	0x40240460	FULL	Memory buffer registers.
SCB0_EZ_DATA25	0x40240464	FULL	Memory buffer registers.
SCB0_EZ_DATA26	0x40240468	FULL	Memory buffer registers.

Register Name	Address	Permission	Description
SCB0_EZ_DATA27	0x4024046C	FULL	Memory buffer registers.
SCB0_EZ_DATA28	0x40240470	FULL	Memory buffer registers.
SCB0_EZ_DATA29	0x40240474	FULL	Memory buffer registers.
SCB0_EZ_DATA30	0x40240478	FULL	Memory buffer registers.
SCB0_EZ_DATA31	0x4024047C	FULL	Memory buffer registers.
SCB0_INTR_CAUSE	0x40240E00	FULL	Active clocked interrupt signal register
SCB0_INTR_I2C_EC	0x40240E80	FULL	Externally clocked I2C interrupt request register
SCB0_INTR_I2C_EC_MASK	0x40240E88	FULL	Externally clocked I2C interrupt mask register
SCB0_INTR_I2C_EC_MASKED	0x40240E8C	FULL	Externally clocked I2C interrupt masked register
SCB0_INTR_SPI_EC	0x40240EC0	FULL	Externally clocked SPI interrupt request register
SCB0_INTR_SPI_EC_MASK	0x40240EC8	FULL	Externally clocked SPI interrupt mask register
SCB0_INTR_SPI_EC_MASKED	0x40240ECC	FULL	Externally clocked SPI interrupt masked register
SCB0_INTR_M	0x40240F00	FULL	Master interrupt request register.
SCB0_INTR_M_SET	0x40240F04	FULL	Master interrupt set request register
SCB0_INTR_M_MASK	0x40240F08	FULL	Master interrupt mask register.
SCB0_INTR_M_MASKED	0x40240F0C	FULL	Master interrupt masked request register
SCB0_INTR_S	0x40240F40	FULL	Slave interrupt request register.
SCB0_INTR_S_SET	0x40240F44	FULL	Slave interrupt set request register.
SCB0_INTR_S_MASK	0x40240F48	FULL	Slave interrupt mask register.
SCB0_INTR_S_MASKED	0x40240F4C	FULL	Slave interrupt masked request register
SCB0_INTR_TX	0x40240F80	FULL	Transmitter interrupt request register.
SCB0_INTR_TX_SET	0x40240F84	FULL	Transmitter interrupt set request register
SCB0_INTR_TX_MASK	0x40240F88	FULL	Transmitter interrupt mask register.
SCB0_INTR_TX_MASKED	0x40240F8C	FULL	Transmitter interrupt masked request register
SCB0_INTR_RX	0x40240FC0	FULL	Receiver interrupt request register.
SCB0_INTR_RX_SET	0x40240FC4	FULL	Receiver interrupt set request register.
SCB0_INTR_RX_MASK	0x40240FC8	FULL	Receiver interrupt mask register.
SCB0_INTR_RX_MASKED	0x40240FCC	FULL	Receiver interrupt masked request register

17.2 SCB 1

Description Serial Communications Block (SPI/UART/I2C)
Base Address 0x40250000
Size 0x10000
Slave Num MMIO1

Register Name	Address	Permission	Description
SCB1_CTRL	0x40250000	FULL	Generic control register.
SCB1_STATUS	0x40250004	FULL	Generic status register.
SCB1_CMD_RESP_CTRL	0x40250008	FULL	Command/response control register.
SCB1_CMD_RESP_STATUS	0x4025000C	FULL	Command/response status register.
SCB1_SPI_CTRL	0x40250020	FULL	SPI control register.
SCB1_SPI_STATUS	0x40250024	FULL	SPI status register.
SCB1_UART_CTRL	0x40250040	FULL	UART control register.
SCB1_UART_TX_CTRL	0x40250044	FULL	UART transmitter control register.
SCB1_UART_RX_CTRL	0x40250048	FULL	UART receiver control register.
SCB1_UART_RX_STATUS	0x4025004C	FULL	UART receiver status register.
SCB1_UART_FLOW_CTRL	0x40250050	FULL	UART flow control register
SCB1_I2C_CTRL	0x40250060	FULL	I2C control register.
SCB1_I2C_STATUS	0x40250064	FULL	I2C status register.
SCB1_I2C_M_CMD	0x40250068	FULL	I2C master command register.
SCB1_I2C_S_CMD	0x4025006C	FULL	I2C slave command register.
SCB1_I2C_CFG	0x40250070	FULL	I2C configuration register.
SCB1_TX_CTRL	0x40250200	FULL	Transmitter control register.
SCB1_TX_FIFO_CTRL	0x40250204	FULL	Transmitter FIFO control register.
SCB1_TX_FIFO_STATUS	0x40250208	FULL	Transmitter FIFO status register.
SCB1_TX_FIFO_WR	0x40250240	FULL	Transmitter FIFO write register.
SCB1_RX_CTRL	0x40250300	FULL	Receiver control register.
SCB1_RX_FIFO_CTRL	0x40250304	FULL	Receiver FIFO control register.
SCB1_RX_FIFO_STATUS	0x40250308	FULL	Receiver FIFO status register.
SCB1_RX_MATCH	0x40250310	FULL	Slave address and mask register.
SCB1_RX_FIFO_RD	0x40250340	FULL	Receiver FIFO read register.

Register Name	Address	Permission	Description
SCB1_RX_FIFO_RD_SILENT	0x40250344	FULL	Receiver FIFO read register.
SCB1_EZ_DATA0	0x40250400	FULL	Memory buffer registers.
SCB1_EZ_DATA1	0x40250404	FULL	Memory buffer registers.
SCB1_EZ_DATA2	0x40250408	FULL	Memory buffer registers.
SCB1_EZ_DATA3	0x4025040C	FULL	Memory buffer registers.
SCB1_EZ_DATA4	0x40250410	FULL	Memory buffer registers.
SCB1_EZ_DATA5	0x40250414	FULL	Memory buffer registers.
SCB1_EZ_DATA6	0x40250418	FULL	Memory buffer registers.
SCB1_EZ_DATA7	0x4025041C	FULL	Memory buffer registers.
SCB1_EZ_DATA8	0x40250420	FULL	Memory buffer registers.
SCB1_EZ_DATA9	0x40250424	FULL	Memory buffer registers.
SCB1_EZ_DATA10	0x40250428	FULL	Memory buffer registers.
SCB1_EZ_DATA11	0x4025042C	FULL	Memory buffer registers.
SCB1_EZ_DATA12	0x40250430	FULL	Memory buffer registers.
SCB1_EZ_DATA13	0x40250434	FULL	Memory buffer registers.
SCB1_EZ_DATA14	0x40250438	FULL	Memory buffer registers.
SCB1_EZ_DATA15	0x4025043C	FULL	Memory buffer registers.
SCB1_EZ_DATA16	0x40250440	FULL	Memory buffer registers.
SCB1_EZ_DATA17	0x40250444	FULL	Memory buffer registers.
SCB1_EZ_DATA18	0x40250448	FULL	Memory buffer registers.
SCB1_EZ_DATA19	0x4025044C	FULL	Memory buffer registers.
SCB1_EZ_DATA20	0x40250450	FULL	Memory buffer registers.
SCB1_EZ_DATA21	0x40250454	FULL	Memory buffer registers.
SCB1_EZ_DATA22	0x40250458	FULL	Memory buffer registers.
SCB1_EZ_DATA23	0x4025045C	FULL	Memory buffer registers.
SCB1_EZ_DATA24	0x40250460	FULL	Memory buffer registers.
SCB1_EZ_DATA25	0x40250464	FULL	Memory buffer registers.
SCB1_EZ_DATA26	0x40250468	FULL	Memory buffer registers.
SCB1_EZ_DATA27	0x4025046C	FULL	Memory buffer registers.
SCB1_EZ_DATA28	0x40250470	FULL	Memory buffer registers.
SCB1_EZ_DATA29	0x40250474	FULL	Memory buffer registers.
SCB1_EZ_DATA30	0x40250478	FULL	Memory buffer registers.
SCB1_EZ_DATA31	0x4025047C	FULL	Memory buffer registers.
SCB1_INTR_CAUSE	0x40250E00	FULL	Active clocked interrupt signal register
SCB1_INTR_I2C_EC	0x40250E80	FULL	Externally clocked I2C interrupt request register
SCB1_INTR_I2C_EC_MASK	0x40250E88	FULL	Externally clocked I2C interrupt mask register
SCB1_INTR_I2C_EC_MASKED	0x40250E8C	FULL	Externally clocked I2C interrupt masked register
SCB1_INTR_SPI_EC	0x40250EC0	FULL	Externally clocked SPI interrupt request register
SCB1_INTR_SPI_EC_MASK	0x40250EC8	FULL	Externally clocked SPI interrupt mask register
SCB1_INTR_SPI_EC_MASKED	0x40250ECC	FULL	Externally clocked SPI interrupt masked register
SCB1_INTR_M	0x40250F00	FULL	Master interrupt request register.
SCB1_INTR_M_SET	0x40250F04	FULL	Master interrupt set request register
SCB1_INTR_M_MASK	0x40250F08	FULL	Master interrupt mask register.
SCB1_INTR_M_MASKED	0x40250F0C	FULL	Master interrupt masked request register
SCB1_INTR_S	0x40250F40	FULL	Slave interrupt request register.
SCB1_INTR_S_SET	0x40250F44	FULL	Slave interrupt set request register.
SCB1_INTR_S_MASK	0x40250F48	FULL	Slave interrupt mask register.
SCB1_INTR_S_MASKED	0x40250F4C	FULL	Slave interrupt masked request register
SCB1_INTR_TX	0x40250F80	FULL	Transmitter interrupt request register.
SCB1_INTR_TX_SET	0x40250F84	FULL	Transmitter interrupt set request register
SCB1_INTR_TX_MASK	0x40250F88	FULL	Transmitter interrupt mask register.
SCB1_INTR_TX_MASKED	0x40250F8C	FULL	Transmitter interrupt masked request register
SCB1_INTR_RX	0x40250FC0	FULL	Receiver interrupt request register.
SCB1_INTR_RX_SET	0x40250FC4	FULL	Receiver interrupt set request register.
SCB1_INTR_RX_MASK	0x40250FC8	FULL	Receiver interrupt mask register.
SCB1_INTR_RX_MASKED	0x40250FCC	FULL	Receiver interrupt masked request register

17.3 Register Details

17.3.1 SCB_CTRL

Description: Generic control register.
Address: 0x40240000
Offset: 0x0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x300000F

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:4]				OVS [3:0]			

Bits	15	14	13	12	11	10	9	8
Name	None [15:13]			CMD_RESP_MODE [12:12]	BYTE_MODE [11:11]	EZ_MODE [10:10]	EC_OP_MODE [9:9]	EC_AM_MODE [8:8]

Bits	23	22	21	20	19	18	17	16
Name	None [23:18]						BLOCK [17:17]	ADDR_ACCEPT [16:16]

Bits	31	30	29	28	27	26	25	24
Name	ENABLED [31:31]	None [30:26]					MODE [25:24]	

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:3	OVS	RW	R	15	Serial interface bit period oversampling factor expressed in SCB clock cycles. Used for SPI and UART functionality. OVS + 1 SCB clock cycles constitute a single serial interface clock/bit cycle. This field is NOT used in externally clocked mode. If OVS is odd, the oversampling factor is even and the low and high phase of the interface clock period are the same. If OVS is even, the oversampling factor is odd and the low and high phase can differ by 1 SCB clock period. In SPI master mode, the valid range is [3, 15]. At an SCB frequency of 48 MHz, the maximum SPI bit rate is 12 Mbps, assuming ideal (0 ns) IO cell and routing (chip and board) delay. The calculated maximum bit rate decreases, when realistic chip and routing delays are taken into account. The effective system bit rate is dependent on the external SPI slave that we communicate with. If the SPI output clock to SPI MISO input round trip delay is significant (multiple SPI output clock cycles), it may be necessary to increase OVS and/or to set SPI_CTRL.LATE_MISO_SAMPLE to '1' to achieve the maximum possible system bit rate. In SPI slave mode, the OVS field is NOT used. However, there is a frequency requirement for the SCB clock wrt. the SPI input clock (IF) on the interface to guarantee functional correct behavior. This requirement is expressed as a ratio: SCB clock/IF clock. The ratio is dependent on the setting of RX_CTRL.MEDIAN and the external SPI master's capability to support 'late MISO sample' functionality (similar to our SPI master functionality represented by SPI_CTRL.LATE_MISO_SAMPLE): - MEDIAN is '0' and external SPI master has NO 'late MISO sample functionality': SCB clock/IF clock >= 6. At a SCB frequency of 48 MHz, the maximum bit rate is 8 Mbps. - MEDIAN is '0' and external SPI master has 'late MISO sample functionality': SCB clock/IF clock >= 3. At a SCB frequency of 48 MHz, the maximum bit rate is 16 Mbps. - MEDIAN is '1' and external SPI master has NO 'late MISO sample functionality': SCB clock/IF clock >= 8. At a SCB frequency of 48 MHz, the maximum bit rate is 6 Mbps. - MEDIAN is '1' and external SPI master has 'late MISO sample functionality': SCB clock/IF clock >= 4. At a SCB frequency of 48 MHz, the maximum bit rate is 12 Mbps. As discussed earlier, the calculated maximum bit rate decreases, when realistic chip and routing delays are taken into account. In UART standard submode (including LIN), the valid range is [7, 15]. In UART SmartCard submode, the valid range is [7, 15].

Bits	Name	SW	HW	Default or Enum	Description
					(Continuation) In UART TX IrDA submode this field indirectly specifies the oversampling. The oversampling determines the interface clock/bit cycle and the width of the pulse. Only normal transmission mode is supported, the pulse is roughly 3/16 of the bit period (for all bit rates). There is only one valid OVS value: - 0: 16 times oversampling. SCB clock frequency of 16*115.2 kHz for 115.2 kbps. SCB clock frequency of 16*57.6 kHz for 57.6 kbps. SCB clock frequency of 16*38.4 kHz for 38.4 kbps. SCB clock frequency of 16*19.2 kHz for 19.2 kbps. SCB clock frequency of 16*9.6 kHz for 9.6 kbps. SCB clock frequency of 16*2.4 kHz for 2.4 kbps. SCB clock frequency of 16*1.2 kHz for 1.2 kbps. - all other values are not used in normal mode. In UART RX IrDA submode (1.2, 2.4, 9.6, 19.2, 38.4, 57.6 and 115.2 kbps) this field indirectly specifies the oversampling. The oversampling determines the interface clock/bit cycle and the width of the pulse. In normal transmission mode, this pulse is roughly 3/16 of the bit period (for all bit rates). In low power transmission mode, this pulse is potentially smaller (down to 1.62 us typical and 1.41 us minimal) than 3/16 of the bit period (for < 115.2 kbps bitrates). Pulse widths greater or equal than two SCB clock cycles are guaranteed to be detected by the receiver. Pulse widths less than two SCB clock cycles and greater or equal than one SCB clock cycle may be detected by the receiver. Pulse widths less than one SCB clock cycle will not be detected by the receiver. RX_CTRL.MEDIAN should be set to '1' for IrDA receiver functionality. The SCB clock (as provided by the programmable clock block) and the oversampling together determine the IrDA bitrate. Normal mode, OVS field values (with the required SCB clock frequency): - 0: 16 times oversampling. SCB clock frequency of 16*115.2 kHz for 115.2 kbps. SCB clock frequency of 16*57.6 kHz for 57.6 kbps. SCB clock frequency of 16*38.4 kHz for 38.4 kbps. SCB clock frequency of 16*19.2 kHz for 19.2 kbps. SCB clock frequency of 16*9.6 kHz for 9.6 kbps. SCB clock frequency of 16*2.4 kHz for 2.4 kbps. SCB clock frequency of 16*1.2 kHz for 1.2 kbps. - all other values are not used in normal mode. Low power mode, OVS field values (with the required SCB clock frequency): - 0: 16 times oversampling. SCB clock frequency of 16*115.2 kHz for 115.2 kbps. - 1: 32 times oversampling. SCB clock frequency of 32*57.6 kHz for 57.6 kbps. - 2: 48 times oversampling. SCB clock frequency of 48*38.4 kHz for 38.4 kbps. - 3: 96 times oversampling. SCB clock frequency of 96*19.2 kHz for 19.2 kbps. - 4: 192 times oversampling.

Bits	Name	SW	HW	Default or Enum	Description
					(Continuation) SCB clock frequency of 192*9.6 kHz for 9.6 kbps. - 5: 768 times oversampling. SCB clock frequency of 768*2.4 kHz for 2.4 kbps. - 6: 1536 times oversampling. SCB clock frequency of 1536*1.2 kHz for 1.2 kbps. - all other values are not used in low power mode.
8	EC_AM_MODE	RW	R	0	This field specifies the clocking for the address matching (I2C) or slave selection detection logic (SPI) '0': Internally clocked mode '1': Externally clocked mode In internally clocked mode, the serial interface protocols run off the SCB clock. In externally clocked mode, the serial interface protocols run off the clock as provided by the serial interface. The clocking for the rest of the logic is determined by CTRL.EC_OP_MODE. Externally clocked mode is only used for synchronous serial interface protocols (SPI and I2C) in slave mode. In SPI mode, only Motorola submode (all Motorola modes: 0, 1, 2, 3) is supported. In UART mode this field should be '0'.
9	EC_OP_MODE	RW	R	0	This field specifies the clocking for the SCB block '0': Internally clocked mode '1': externally clocked mode In internally clocked mode, the serial interface protocols run off the SCB clock. In externally clocked mode, the serial interface protocols run off the clock as provided by the serial interface. Externally clocked operation mode is only used for synchronous serial interface protocols (SPI and I2C) in slave mode AND EZ mode. In SPI mode, only Motorola submode (all Motorola modes: 0, 1, 2, 3) is supported. The maximum SPI slave, EZ mode bitrate is 48 Mbps (transmission and IO delays outside the IP will degrade the effective bitrate). In UART mode this field should be '0'.
10	EZ_MODE	RW	R	0	Non EZ mode ('0') or EZ mode ('1'). In EZ mode, a meta protocol is applied to the serial interface protocol. This meta protocol adds meaning to the data frames transferred by the serial interface protocol: a data frame can represent a memory address, a write memory data element or a read memory data element. EZ mode is only used for synchronous serial interface protocols: SPI and I2C. In SPI mode, only Motorola submode (all Motorola modes: 0, 1, 2, 3) is supported and the transmitter should use continuous data frames; i.e. data frames not separated by slave deselection. This mode is only applicable to slave functionality. In EZ mode, the slave can read from and write to an addressable memory structure of 32 bytes. In EZ mode, data frames should 8-bit in size and should be transmitted and received with the Most Significant Bit (MSB) first. In UART mode this field should be '0'.

Bits	Name	SW	HW	Default or Enum	Description
11	BYTE_MODE	RW	R	0	Determines the number of bits per FIFO data element: '0': 16-bit FIFO data elements. '1': 8-bit FIFO data elements. This mode doubles the amount of FIFO entries, but TX_CTRL.DATA_WIDTH and RX_CTRL.DATA_WIDTH are restricted to [0, 7].
12	CMD_RESP_MODE	RW	R	0	Determines CMD_RESP mode of operation: '0': CMD_RESP mode disabled. '1': CMD_RESP mode enabled (also requires EC_AM_MODE and EC_OP_MODE to be set to '1').
16	ADDR_ACCEPT	RW	R	0	Determines whether a received matching address is accepted in the RX FIFO ('1') or not ('0'). In I2C mode, this field is used to allow the slave to put the received slave address or general call address in the RX FIFO. Note that a received matching address is put in the RX FIFO when this bit is '1' for both I2C read and write transfers. In multi-processor UART receiver mode, this field is used to allow the receiver to put the received address in the RX FIFO. Note: non-matching addresses are never put in the RX FIFO.
17	BLOCK	RW	R	0	Only used in externally clocked mode. If the externally clocked logic and the internal CPU accesses to EZ memory coincide/collide, this bit determines whether the CPU access should block and result in bus wait states ('BLOCK is 1') or not (BLOCK is '0'). IF BLOCK is '0' and the accesses collide, CPU read operations return 0xffff:ffff and CPU write operations are ignored. Colliding accesses are registered as interrupt causes: INTR_TX.BLOCKED and INTR_RX.BLOCKED.
24:25	MODE	RW	R	3	Mode of operation (3: Reserved)
	I2C			0	Inter-Integrated Circuits (I2C) mode.
	SPI			1	Serial Peripheral Interface (SPI) mode.
	UART			2	Universal Asynchronous Receiver/Transmitter (UART) mode.
31	ENABLED	RW	R	0	SCB block is enabled ('1') or not ('0'). The proper order in which to initialize SCB is as follows: - Program protocol specific information using SPI_CTRL, UART_CTRL (and UART_TX_CTRL and UART_RX_CTRL) or I2C_CTRL registers. This includes selection of a submode, master/slave functionality and transmitter/receiver functionality when applicable. - Program generic transmitter (TX_CTRL) and receiver (RX_CTRL) information. This includes enabling of the transmitter and receiver functionality. - Program transmitter FIFO (TX_FIFO_CTRL) and receiver FIFO (RX_FIFO_CTRL) information. - Program CTRL register to enable SCB, select the specific operation mode and oversampling factor. When this block is enabled, no control information should be changed. Changes should be made AFTER disabling this block, e.g. to modify the operation mode (from I2C to SPI) or to go from externally to internally clocked. The change takes effect after the block is re-enabled. Note that disabling the block will cause re-initialization of the design and associated state is lost (e.g. FIFO content).

17.3.2 SCB_STATUS

Description: Generic status register.
Address: 0x40240004
Offset: 0x4
Retention: Not Retained
IsDeepSleep: Yes
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:1]							EC_BUSY [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	EC_BUSY	R	W	Undefined	Indicates whether the externally clocked logic is potentially accessing the EZ memory (this is only possible in EZ mode). This bit can be used by SW to determine whether it is safe to issue a SW access to the EZ memory (without bus wait states (a blocked SW access) or bus errors being generated). Note that the INTR_TX.BLOCKED and INTR_RX.BLOCKED interrupt causes are used to indicate whether a SW access was actually blocked by externally clocked logic.

17.3.3 SCB_CMD_RESP_CTRL

Description: Command/response control register.
Address: 0x40240008
Offset: 0x8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:5]			BASE_RD_ADDR [4:0]				

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:21]			BASE_WR_ADDR [20:16]				

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:4	BASE_RD_ADDR	RW	R	0	I2C/SPI read base address for CMD_RESP mode. At the start of a read transfer this BASE_RD_ADDR is copied to CMD_RESP_STATUS.CURR_RD_ADDR. This field should not be modified during ongoing bus transfers.
16:20	BASE_WR_ADDR	RW	R	0	I2C/SPI write base address for CMD_RESP mode. At the start of a write transfer this BASE_WR_ADDR is copied to CMD_RESP_STATUS.CURR_WR_ADDR. This field should not be modified during ongoing bus transfers.

17.3.4 SCB_CMD_RESP_STATUS

Description: Command/response status register.
Address: 0x4024000C
Offset: 0xC
Retention: Not Retained
IsDeepSleep: Yes
Comment: The register fields reflect register states without a default/reset value (CURR_RD_ADDR and CURR_WR_ADDR) or reflect an external bus state. Therefore, these registers are undefined after the IP is enabled.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:5]			CURR_RD_ADDR [4:0]				

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:21]			CURR_WR_ADDR [20:16]				

Bits	31	30	29	28	27	26	25	24
Name	CMD_RESP_EC_BUSY [31:31]	CMD_RESP_EC_BUS_BUSY [30:30]	None [29:24]					

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:4	CURR_RD_ADDR	R	W	Undefined	I2C/SPI read current address for CMD_RESP mode. HW increments the field after a read access to the memory buffer. However, when the last memory buffer address is reached, the address is NOT incremented (but remains at the maximum memory buffer address). The field is used to determine how many bytes have been read (# bytes = CURR_RD_ADDR - CMD_RESP_CTRL.BASE_RD_ADDR). This field is reliable when there is no bus transfer. This field is potentially unreliable when there is a ongoing bus transfer, i.e. when CMD_RESP_EC_BUSY is '0', the field is reliable.
16:20	CURR_WR_ADDR	R	W	Undefined	I2C/SPI write current address for CMD_RESP mode. HW increments the field after a write access to the memory buffer. However, when the last memory buffer address is reached, the address is NOT incremented (but remains at the maximum memory buffer address). The field is used to determine how many bytes have been written (# bytes = CURR_WR_ADDR - CMD_RESP_CTRL.BASE_WR_ADDR). This field is reliable when there is no bus transfer. This field is potentially unreliable when there is a ongoing bus transfer, i.e. when CMD_RESP_EC_BUSY is '0', the field is reliable.

Bits	Name	SW	HW	Default or Enum	Description
30	CMD_RESP_EC_BUS_BUSY	R	W	Undefined	Indicates whether there is an ongoing bus transfer to the IP. '0': no ongoing bus transfer. '1': ongoing bus transfer. For SPI, the field is '1' when slave mode is selected. For I2C, the field is set to '1' at a I2C START/RESTART. In case of an address match, the field is set to '0' on a I2C STOP. In case of NO address match, the field is set to '0' after the failing address match.
31	CMD_RESP_EC_BUSY	R	W	Undefined	Indicates whether the CURR_RD_ADDR and CURR_WR_ADDR fields in this register are reliable (when CMD_RESP_EC_BUSY is '0') or not reliable (when CMD_RESP_EC_BUSY is '1'). Note: - When there is no ongoing bus transfer, CMD_RESP_EC_BUSY is '0' (reliable). - When there is a ongoing bus transfer, CMD_RESP_EC_BUSY is '0' (reliable), when the CURR_RD_ADDR and CURR_WR_ADDR are not being updated by the HW. - When there is a ongoing bus transfer, CMD_RESP_EC_BUSY is '1' (not reliable), when the CURR_RD_ADDR or CURR_WR_ADDR are being updated by the HW. Note that this update lasts one I2C clock cycle, or two SPI clock cycles.

17.3.5 SCB_SPI_CTRL

Description: SPI control register.
Address: 0x40240020
Offset: 0x20
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x3000000

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:6]		SCLK_CONTINUOUS [5:5]	LATE_MISO_SAMPLE [4:4]	CPOL [3:3]	CPHA [2:2]	SELECT_PRECEDE [1:1]	CONTINUOUS [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:12]				SSEL_POLARITY3 [11:11]	SSEL_POLARITY2 [10:10]	SSEL_POLARITY1 [9:9]	SSEL_POLARITY0 [8:8]

Bits	23	22	21	20	19	18	17	16
Name	None [23:17]							LOOPBACK [16:16]

Bits	31	30	29	28	27	26	25	24
Name	MASTER_MODE [31:31]	None [30:28]			SLAVE_SELECT [27:26]		MODE [25:24]	

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	CONTINUOUS	RW	R	0	Continuous SPI data transfers enabled ('1') or not ('0'). This field is used in master mode. In slave mode, both continuous and non-continuous SPI data transfers are supported independent of this field. When continuous transfers are enabled individual data frame transfers are not necessarily separated by slave deselection (as indicated by the level or pulse on the SELECT line): if the TX FIFO has multiple data frames, data frames are send out without slave deselection. When continuous transfers are not enabled individual data frame transfers are always separated by slave deselection: independent of the availability of TX FIFO data frames, data frames are sent out with slave deselection.
1	SELECT_PRECEDE	RW	R	0	Only used in SPI Texas Instruments' submode. When '1', the data frame start indication is a pulse on the Slave SELECT line that precedes the transfer of the first data frame bit. When '0', the data frame start indication is a pulse on the Slave SELECT line that coincides with the transfer of the first data frame bit.

Bits	Name	SW	HW	Default or Enum	Description
2	CPHA	RW	R	0	Only applicable in SPI Motorola submode. Indicates the clock phase. This field, together with the CPOL field, indicates when MOSI data is driven and MISO data is captured: - Motorola mode 0. CPOL is '0', CPHA is '0': MOSI is driven on a falling edge of SCLK. MISO is captured on a rising edge of SCLK. - Motorola mode 1. CPOL is '0', CPHA is '1': MOSI is driven on a rising edge of SCLK. MISO is captured on a falling edge of SCLK. - Motorola mode 2. CPOL is '1', CPHA is '0': MOSI is driven on a rising edge of SCLK. MISO is captured on a falling edge of SCLK. - Motorola mode 3. CPOL is '1', CPHA is '1': MOSI is driven on a falling edge of SCLK. MISO is captured on a rising edge of SCLK.
3	CPOL	RW	R	0	Indicates the clock polarity. Only used in SPI Motorola submode. This field, together with the CPHA field, indicates when MOSI data is driven and MISO data is captured: - CPOL is '0': SCLK is '0' when not transmitting data. - CPOL is '1': SCLK is '1' when not transmitting data.
4	LATE_MISO_SAMPLE	RW	R	0	Changes the SCLK edge on which MISO is captured. Only used in master mode. When '0', the default applies (for Motorola as determined by CPOL and CPHA, for Texas Instruments on the falling edge of SCLK and for National Semiconductors on the rising edge of SCLK). When '1', the alternate clock edge is used (which comes half a SPI SCLK period later). Late sampling addresses the round trip delay associated with transmitting SCLK from the master to the slave and transmitting MISO from the slave to the master.
5	SCLK_CONTINUOUS	RW	R	0	Only applicable in master mode. '0': SCLK is generated, when the SPI master is enabled and data is transmitted. '1': SCLK is generated, when the SPI master is enabled. This mode is useful for slave devices that use SCLK for functional operation other than just SPI functionality.
8	SSEL_POLARITY0	RW	R	0	Slave select polarity. SSEL_POLARITY0 applies to the outgoing SPI slave select signal 0 (master mode) and to the incoming SPI slave select signal (slave mode). only SPI_SELECT[0] is used in slave mode. For Motorola and National Semiconductors submodes: '0': slave select is low/'0' active. '1': slave select is high/'1' active. For Texas Instruments submode: '0': high/'1' active precede/coincide pulse. '1': low/'0' active precede/coincide pulse.
9	SSEL_POLARITY1	RW	R	0	Slave select polarity. SSEL_POLARITY1 applies to the outgoing SPI slave select signal 1 (master mode).
10	SSEL_POLARITY2	RW	R	0	Slave select polarity. SSEL_POLARITY2 applies to the outgoing SPI slave select signal 2 (master mode).
11	SSEL_POLARITY3	RW	R	0	Slave select polarity. SSEL_POLARITY3 applies to the outgoing SPI slave select signal 3 (master mode).

Bits	Name	SW	HW	Default or Enum	Description
16	LOOPBACK	RW	R	0	Local loopback control (does NOT affect the information on the pins). Only used in master mode. Not used in National Semiconductors submode. '0': No local loopback '1': the SPI master MISO line is connected to the SPI master MOSI line. In other words, in loopback mode the SPI master receives on MISO what it transmits on MOSI.
24:25	MODE	RW	R	3	Submode of SPI operation (3: Reserved).
	SPI_MOTOROLA			0	SPI Motorola submode. In master mode, when not transmitting data (Slave SELECT is inactive), SCLK is stable at CPOL. In slave mode, when not selected, SCLK is ignored; i.e. it can be either stable or clocking. In master mode, when there is no data to transmit (TX FIFO is empty), Slave SELECT is inactive.
	SPI_TI			1	SPI Texas Instruments submode. In master mode, when not transmitting data, SCLK is stable at '0'. In slave mode, when not selected, SCLK is ignored; i.e. it can be either stable or clocking. In master mode, when there is no data to transmit (TX FIFO is empty), Slave SELECT is inactive; i.e. no pulse is generated.
	SPI_NS			2	SPI National Semiconductors submode. In master mode, when not transmitting data, SCLK is stable at '0'. In slave mode, when not selected, SCLK is ignored; i.e. it can be either stable or clocking. In master mode, when there is no data to transmit (TX FIFO is empty), Slave SELECT is inactive.
26:27	SLAVE_SELECT	RW	R	0	Selects one of the four outgoing SPI slave select signals: - 0: Slave 0, SPI_SELECT[0]. - 1: Slave 1, SPI_SELECT[1]. - 2: Slave 2, SPI_SELECT[2]. - 3: Slave 3, SPI_SELECT[3]. Only used in master mode. SCB block should be disabled when changes are made to this field.
31	MASTER_MODE	RW	R	0	Master ('1') or slave ('0') mode. In master mode, transmission will commence on availability of data frames in the TX FIFO. In slave mode, when selected and there is no data frame in the TX FIFO, the slave will transmit all '1's. In both master and slave modes, received data frames will be lost if the RX FIFO is full.

17.3.6 SCB_SPI_STATUS

Description: SPI status register.
Address: 0x40240024
Offset: 0x24
Retention: Not Retained
IsDeepSleep: Yes
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:2]						SPI_EC _BUSY [1:1]	BUS_BUSY [0:0]

Bits	15	14	13	12	11	10	9	8
Name	CURR_EZ_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	BASE_EZ_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	BUS_BUSY	R	W	Undefined	SPI bus is busy. The bus is considered busy ('1') during an ongoing transaction. For Motorola and National submodes, the busy bit is '1', when the slave selection (low active) is activated. For TI submode, the busy bit is '1' from the time the preceding/coinciding slave select (high active) is activated for the first transmitted data frame, till the last MOSI/MISO bit of the last data frame is transmitted.
1	SPI_EC_BUSY	R	W	Undefined	Indicates whether the externally clocked logic is potentially accessing the EZ memory and/or updating BASE_ADDR or CURR_ADDR (this is only possible in EZ mode). This bit can be used by SW to determine whether BASE_ADDR and CURR_ADDR are reliable.
8:15	CURR_EZ_ADDR	R	W	Undefined	SPI current EZ address. Current address pointer. This field is only reliable in internally clocked mode. In externally clocked mode the field may be unreliable (during an ongoing transfer when SPI_EC_BUSY is '1'), as clock domain synchronization is not performed in the design.
16:23	BASE_EZ_ADDR	R	W	Undefined	SPI base EZ address. Address as provided by a SPI write transfer. This field is only reliable in internally clocked mode. In externally clocked mode the field may be unreliable, as clock domain synchronization is not performed in the design.

17.3.7 SCB_UART_CTRL

Description: UART control register.
Address: 0x40240040
Offset: 0x40
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x3000000

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:17]							LOOPBACK [16:16]

Bits	31	30	29	28	27	26	25	24
Name	None [31:26]						MODE [25:24]	

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
16	LOOPBACK	RW	R	0	Local loopback control (does NOT affect the information on the pins). 0: Loopback is not enabled 1: UART_TX is connected to UART_RX. UART_RTS is connected to UART_CTS. This allows a SCB UART transmitter to communicate with its receiver counterpart.
24:25	MODE	RW	R	3	Submode of UART operation (3: Reserved)
	UART_STD			0	Standard UART submode.
	UART_SMARTCARD			1	SmartCard (ISO7816) submode. Support for negative acknowledgement (NACK) on the receiver side and retransmission on the transmitter side.
	UART_IRDA			2	Infrared Data Association (IrDA) submode. Return to Zero modulation scheme. In this mode, the oversampling factor should be 16, that is OVS should be set to 15.

17.3.8 SCB_UART_TX_CTRL

Description: UART transmitter control register.
Address: 0x40240044
Offset: 0x44
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x2

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:6]		PARITY _ENABLED [5:5]	PARITY [4:4]	None [3:3]	STOP_BITS [2:0]		

Bits	15	14	13	12	11	10	9	8
Name	None [15:9]							RETRY_ON _NACK [8:8]

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:2	STOP_BITS	RW	R	2	Stop bits. STOP_BITS + 1 is the duration of the stop period in terms of halve bit periods. Valid range is [1, 7]; i.e. a stop period should last at least one bit period.
4	PARITY	RW	R	0	Parity bit. When '0', the transmitter generates an even parity. When '1', the transmitter generates an odd parity. Only applicable in standard UART and SmartCard submodes.
5	PARITY_ENABLED	RW	R	0	Parity generation enabled ('1') or not ('0'). Only applicable in standard UART submodes. In SmartCard submode, parity generation is always enabled through hardware. In IrDA submode, parity generation is always disabled through hardware
8	RETRY_ON_NACK	RW	R	0	When '1', a data frame is retransmitted when a negative acknowledgement is received. Only applicable to the SmartCard submode.

17.3.9 SCB_UART_RX_CTRL

Description: UART receiver control register.
Address: 0x40240048
Offset: 0x48
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xA0002

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:7]	POLARITY [6:6]	PARITY _ENABLED [5:5]	PARITY [4:4]	None [3:3]	STOP_BITS [2:0]		

Bits	15	14	13	12	11	10	9	8
Name	None [15:14]		SKIP _START [13:13]	LIN_MODE [12:12]	None [11:11]	MP_MODE [10:10]	DROP_ON _FRAME _ERROR [9:9]	DROP_ON _PARITY _ERROR [8:8]

Bits	23	22	21	20	19	18	17	16
Name	None [23:20]				BREAK_WIDTH [19:16]			

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:2	STOP_BITS	RW	R	2	Stop bits. STOP_BITS + 1 is the duration of the stop period in terms of halve bit periods. Valid range is [1, 7]; i.e. a stop period should last at least one bit period. If STOP_BITS is '1', stop bits error detection is NOT performed. If STOP_BITS is in [2, 7], stop bits error detection is performed and the associated interrupt cause INTR_RX.FRAME_ERROR is set to '1' if an error is detected. In other words, the receiver supports data frames with a 1 bit period stop bit sequence, but requires at least 1.5 bit period stop bit sequences to detect errors. This limitation is due to possible transmitter and receiver clock skew that prevents the design from doing reliable stop bit detection for short (1 bit period) stop bit sequences. Note that in case of a stop bits error, the successive data frames may get lost as the receiver needs to resynchronize its start bit detection. The amount of lost data frames depends on both the amount of stop bits, the idle ('1') time between data frames and the data frame value.
4	PARITY	RW	R	0	Parity bit. When '0', the receiver expects an even parity. When '1', the receiver expects an odd parity. Only applicable in standard UART and SmartCard submodes.
5	PARITY_ENABLED	RW	R	0	Parity checking enabled ('1') or not ('0'). Only applicable in standard UART submode. In SmartCard submode, parity checking is always enabled through hardware. In IrDA submode, parity checking is always disabled through hardware.
6	POLARITY	RW	R	0	Inverts incoming RX line signal. Inversion is after local loopback. This functionality is intended for IrDA receiver functionality.

Bits	Name	SW	HW	Default or Enum	Description
8	DROP_ON_PARITY_ERROR	RW	R	0	Behavior when a parity check fails. When '0', received data is sent to the RX FIFO. When '1', received data is dropped and lost. Only applicable in standard UART and SmartCard submodes (negatively acknowledged SmartCard data frames may be dropped with this field).
9	DROP_ON_FRAME_ERROR	RW	R	0	Behavior when an error is detected in a start or stop period. When '0', received data is sent to the RX FIFO. When '1', received data is dropped and lost.
10	MP_MODE	RW	R	0	Multi-processor mode. When '1', multi-processor mode is enabled. In this mode, RX_CTRL.DATA_WIDTH should indicate a 9-bit data frame. In multi-processor mode, the 9th received bit of a data frame separates addresses (bit is '1') from data (bit is '0'). A received address is matched with RX_MATCH.DATA and RX_MATCH.MASK. In the case of a match, subsequent received data are sent to the RX FIFO. In the case of NO match, subsequent received data are dropped.
12	LIN_MODE	RW	R	0	Only applicable in standard UART submode. When '1', the receiver performs break detection and baud rate detection on the incoming data. First, break detection counts the amount of bit periods that have a line value of '0'. BREAK_WIDTH specifies the minimum required amount of bit periods. Successful break detection sets the INTR_RX.BREAK_DETECT interrupt cause to '1'. Second, baud rate detection counts the amount of peripheral clock periods that are use to receive the synchronization byte (0x55; least significant bit first). The count is available through UART_RX_STATUS.BR_COUNTER. Successful baud rate detection sets the INTR_RX.BAUD_DETECT interrupt cause to '1' (BR_COUNTER is reliable). This functionality is used to synchronize/refine the receiver clock to the transmitter clock. The receiver software can use the BR_COUNTER value to set the right IP clock (from the programmable clock IP) to guarantee successful receipt of the first LIN data frame (Protected Identifier Field) after the synchronization byte.
13	SKIP_START	RW	R	0	Only applicable in standard UART submode. When '1', the receiver skips start bit detection for the first received data frame. Instead, it synchronizes on the first received data frame bit, which should be a '1'. This functionality is intended for wake up from DeepSleep when receiving a data frame. The transition from idle ('1') to START ('0') on the RX line is used to wake up the CPU. The transition detection (and the associated wake up functionality) is performed by the GPIO2 IP. The woken up CPU will enable the SCB's UART receiver functionality. Once enabled, it is assumed that the START bit is ongoing (the CPU wakeup and SCB enable time should be less than the START bit period). The SCB will synchronize to a '0' to '1' transition, which indicates the first data frame bit is received (first data frame bit should be '1'). After synchronization to the first data frame bit, the SCB will resume normal UART functionality: subsequent data frames will be synchronized on the receipt of a START bit.

Bits	Name	SW	HW	Default or Enum	Description
16:19	BREAK_WIDTH	RW	R	10	Break width. BREAK_WIDTH + 1 is the minimum width in bit periods of a break. During a break the transmitted/received line value is '0'. This feature is useful for standard UART submode and LIN submode ('break field' detection). Once, the break is detected, the INTR_RX.BREAK_DETECT bit is set to '1'. Note that break detection precedes baud rate detection, which is used to synchronize/refine the receiver clock to the transmitter clock. As a result, break detection operates with an unsynchronized/unrefined receiver clock. Therefore, the receiver's definition of a bit period is imprecise and the setting of this field should take this imprecision into account. The LIN standard also accounts for this imprecision: a LIN start bit followed by 8 data bits allows for up to 9 consecutive '0' bit periods during regular transmission, whereas the LIN break detection should be at least 13 consecutive '0' bit periods. This provides for a margin of 4 bit periods. Therefore, the default value of this field is set to 10, representing a minimal break field with of 10+1 = 11 bit periods; a value in between the 9 consecutive bit periods of a regular transmission and the 13 consecutive bit periods of a break field. This provides for slight imprecisions of the receiver clock wrt. the transmitter clock. There should not be a need to program this field to any value other than its default value.

17.3.10 SCB_UART_RX_STATUS

Description: UART receiver status register.
Address: 0x4024004C
Offset: 0x4C
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	BR_COUNTER [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	None [15:12]				BR_COUNTER [11:8]			

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:11	BR_COUNTER	R	W	Undefined	Amount of SCB clock periods that constitute the transmission of a 0x55 data frame (sent least significant bit first) as determined by the receiver. BR_COUNTER / 8 is the amount of SCB clock periods that constitute a bit period. This field has valid data when INTR_RX.BAUD_DETECT is set to '1'.

17.3.11 SCB_UART_FLOW_CTRL

Description: UART flow control register
Address: 0x40240050
Offset: 0x50
Retention: Retained
IsDeepSleep: No
Comment: UART flow control is a design time configuration parameter, which make the presence of this MMIO register conditional to the configuration. The 'uart_rts_out' and 'uart_cts_in' are always present on the IP interface. If flow control is configured out, 'uart_rts_out' is NOT connected, and 'uart_cts_in' should be connected to '0'.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:4]				TRIGGER_LEVEL [3:0]			

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:17]							RTS_POLARITY [16:16]

Bits	31	30	29	28	27	26	25	24
Name	None [31:26]						CTS_ENABLED [25:25]	CTS_POLARITY [24:24]

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:3	TRIGGER_LEVEL	RW	R	0	Trigger level. When the receiver FIFO has less entries than the amount of this field, a Ready To Send (RTS) output signal is activated. By setting this field to '0', flow control is effectively disabled (may be useful for debug purposes).
16	RTS_POLARITY	RW	R	0	Polarity of the RTS output signal: '0': RTS is active low; '1': RTS is active high; During SCB reset (Hibernate system power mode), RTS output signal is '1'. This represents an inactive state assuming an active low polarity.
24	CTS_POLARITY	RW	R	0	Polarity of the CTS input signal '0': CTS is active low ; '1': CTS is active high;

Bits	Name	SW	HW	Default or Enum	Description
25	CTS_ENABLED	RW	R	0	Enable use of CTS input signal by the UART transmitter: '0': Disabled. The UART transmitter ignores the CTS input signal and transmits when a data frame is available for transmission in the TX FIFO or the TX shift register. '1': Enabled. The UART transmitter uses CTS input signal to qualify the transmission of data. It transmits when CTS input signal is active and a data frame is available for transmission in the TX FIFO or the TX shift register. If UART_CTRL.LOOPBACK is '1', the CTS input signal is driven by the RTS output signal locally in SCB (both signals are subjected to signal polarity changes as indicated by RTS_POLARITY and CTS_POLARITY).

17.3.12 SCB_I2C_CTRL

Description: I2C control register.
Address: 0x40240060
Offset: 0x60
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xFB88

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	LOW_PHASE_OVS [7:4]				HIGH_PHASE_OVS [3:0]			

Bits	15	14	13	12	11	10	9	8
Name	S_NOT_READY_DATA_NACK [15:15]	S_NOT_READY_ADDR_NACK [14:14]	S_READY_DATA_ACK [13:13]	S_READY_ADDR_ACK [12:12]	S_GENERAL_IGNORE [11:11]	None [10:10]	M_NOT_READY_DATA_NACK [9:9]	M_READY_DATA_ACK [8:8]

Bits	23	22	21	20	19	18	17	16
Name	None [23:17]							LOOPBACK [16:16]

Bits	31	30	29	28	27	26	25	24
Name	MASTER_MODE [31:31]	SLAVE_MODE [30:30]	None [29:24]					

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:3	HIGH_PHASE_OVS	RW	R	8	Serial I2C interface high phase oversampling factor. HIGH_PHASE_OVS + 1 SCB clock periods constitute the high phase of a bit period. The valid range is [5, 15] with input signal median filtering and [4, 15] without input signal median filtering. The field is only used in master mode. In slave mode, the field is NOT used. However, there is a frequency requirement for the SCB clock wrt. the regular interface (IF) high time to guarantee functional correct behavior. With input signal median filtering, the IF high time should be >= 6 SCB clock cycles and <= 16 SCB clock cycles. Without input signal median filtering, the IF high time should be >= 5 SCB clock cycles and <= 16 SCB clock cycles.
4:7	LOW_PHASE_OVS	RW	R	8	Serial I2C interface low phase oversampling factor. LOW_PHASE_OVS + 1 SCB clock periods constitute the low phase of a bit period. The valid range is [7, 15] with input signal median filtering and [6, 15] without input signal median filtering. The field is only used in master mode. In slave mode, the field is NOT used. However, there is a frequency requirement for the SCB clock wrt. the regular (no stretching) interface (IF) low time to guarantee functionally correct behavior. With input signal median filtering, the IF low time should be >= 8 SCB clock cycles and <= 16 IP clock cycles. Without input signal median filtering, the IF low time should be >= 7 SCB clock cycles and <= 16 SCB clock cycles.

Bits	Name	SW	HW	Default or Enum	Description
8	M_READY_DATA_ACK	RW	R	1	When '1', a received data element by the master is immediately ACK'd when the receiver FIFO is not full.
9	M_NOT_READY_DATA_NACK	RW	R	1	When '1', a received data element byte the master is immediately NACK'd when the receiver FIFO is full. When '0', clock stretching is used instead (till the receiver FIFO is no longer full).
11	S_GENERAL_IGNORE	RW	R	1	When '1', a received general call slave address is immediately NACK'd (no ACK or clock stretching) and treated as a non matching slave address. This is useful for slaves that do not need any data supplied within the general call structure.
12	S_READY_ADDR_ACK	RW	R	1	When '1', a received (matching) slave address is immediately ACK'd when the receiver FIFO is not full. In EZ mode, this field should be set to '1'.
13	S_READY_DATA_ACK	RW	R	1	When '1', a received data element by the slave is immediately ACK'd when the receiver FIFO is not full. In EZ mode, this field should be set to '1'.
14	S_NOT_READY_ADDR_NACK	RW	R	1	This field is used during an address match or general call address in internally clocked mode Only used when: - EC_AM_MODE is '0', EC_OP_MODE is '0', S_GENERAL_IGNORE is '0] and non EZ mode. Functionality is as follows: - 1: a received (matching) slave address is immediately NACK'd when the receiver FIFO is full. - 0: clock stretching is performed (till the receiver FIFO is no longer full). For externally clocked logic (EC_AM is '1') on an address match or general call address (and S_GENERAL_IGNORE is '0'). Only used when (NOT used when EC_AM is '1' and EC_OP is '1' and address match and EZ mode): - EC_AM is '1' and EC_OP is '0'. - EC_AM is '1' and general call address match. - EC_AM is '1' and non EZ mode. Functionality is as follows: - 1: a received (matching or general) slave address is always immediately NACK'd. There are two possibilities: 1). the SCB clock is available (in Active system power mode) and it handles the rest of the current transfer. In this case the I2C master will not observe the NACK. 2).SCB clock is not present (in DeepSleep system power mode). In this case the I2C master will observe the NACK and may retry the transfer in the future (which gives the internally clocked logic the time to wake up from DeepSleep system power mode). - 0: clock stretching is performed (till the SCB clock is available). The logic will handle the ongoing transfer as soon as the clock is enabled.
15	S_NOT_READY_DATA_NACK	RW	R	1	Only used when: - non EZ mode Functionality is as follows: - 1: a received data element byte the slave is immediately NACK'd when the receiver FIFO is full. - 0: clock stretching is performed (till the receiver FIFO is no longer full).

Bits	Name	SW	HW	Default or Enum	Description
16	LOOPBACK	RW	R	0	Local loopback control (does NOT affect the information on the pins). Only applicable in master/slave mode. When '0', no loopback When '1', loopback is enabled internally in the peripheral, and as a result unaffected by other I2C devices. This allows a SCB I2C peripheral to address itself.
30	SLAVE_MODE	RW	R	0	Slave mode enabled ('1') or not ('0').
31	MASTER_MODE	RW	R	0	Master mode enabled ('1') or not ('0'). Note that both master and slave modes can be enabled at the same time. This allows the IP to address itself.

17.3.13 SCB_I2C_STATUS

Description: I2C status register.
Address: 0x40240064
Offset: 0x64
Retention: Not Retained
IsDeepSleep: Yes
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:6]		M_READ [5:5]	S_READ [4:4]	None [3:2]		I2C_EC_BUSY [1:1]	BUS_BUSY [0:0]

Bits	15	14	13	12	11	10	9	8
Name	CURR_EZ_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	BASE_EZ_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	BUS_BUSY	R	W	0	I2C bus is busy. The bus is considered busy ('1'), from the time a START is detected or from the time the SCL line is '0'. The bus is considered idle ('0'), from the time a STOP is detected. If SCB block is disabled, BUS_BUSY is '0'. After enabling the block, it takes time for the BUS_BUSY to detect a busy bus. This time is the maximum high time of the SCL line. For a 100 kHz interface frequency, this maximum high time may last roughly 5 us (half a bit period). For single master systems, BUS_BUSY does not have to be used to detect an idle bus before a master starts a transfer using I2C_M_CMD.M_START (no bus collisions). For multi-master systems, BUS_BUSY can be used to detect an idle bus before a master starts a transfer using I2C_M_CMD.M_START_ON_IDLE (to prevent bus collisions).
1	I2C_EC_BUSY	R	W	Undefined	Indicates whether the externally clocked logic is potentially accessing the EZ memory and/or updating BASE_EZ_ADDR or CURR_EZ_ADDR (this is only possible in EZ mode). This bit can be used by SW to determine whether BASE_EZ_ADDR and CURR_EZ_ADDR are reliable.
4	S_READ	R	W	0	I2C slave read transfer ('1') or I2C slave write transfer ('0'). When the I2C slave is inactive/idle or receiving START, REPEATED START, STOP or an address, this field is '0".
5	M_READ	R	W	0	I2C master read transfer ('1') or I2C master write transfer ('0'). When the I2C master is inactive/idle or transmitting START, REPEATED START, STOP or an address, this field is '0".

Bits	Name	SW	HW	Default or Enum	Description
8:15	CURR_EZ_ADDR	R	W	Undefined	I2C slave current EZ address. Current address pointer. This field is only reliable in internally clocked mode. In externally clocked mode the field may be unreliable (during an ongoing transfer when I2C_EC_BUSY is '1'), as clock domain synchronization is not performed in the design.
16:23	BASE_EZ_ADDR	R	W	Undefined	I2C slave base EZ address. Address as provided by an I2C write transfer. This field is only reliable in internally clocked mode. In externally clocked mode the field may be unreliable, as clock domain synchronization is not performed in the design.

17.3.14 SCB_I2C_M_CMD

Description: I2C master command register.
Address: 0x40240068
Offset: 0x68
Retention: Not Retained
IsDeepSleep: No
Comment: The register fields are not retained. This is to ensure that they come up as '0' after coming out of DeepSleep system power mode.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:5]			M_STOP [4:4]	M_NACK [3:3]	M_ACK [2:2]	M_START_ON_IDLE [1:1]	M_START [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	M_START	RW	RW1C	0	When '1', transmit a START or REPEATED START. Whether a START or REPEATED START is transmitted depends on the state of the master state machine. A START is only transmitted when the master state machine is in the default state. A REPEATED START is transmitted when the master state machine is not in the default state, but is working on an ongoing transaction. The REPEATED START can only be transmitted after a NACK or ACK has been received for a transmitted data element or after a NACK has been transmitted for a received data element. When this action is performed, the hardware sets this field to '0'.
1	M_START_ON_IDLE	RW	RW1C	0	When '1', transmit a START as soon as the bus is idle (I2C_STATUS.BUS_BUSY is '0', note that BUSY has a default value of '0'). For bus idle detection the hardware relies on STOP detection. As a result, bus idle detection is only functional after at least one I2C bus transfer has been detected on the bus (default/reset value of BUSY is '0') . A START is only transmitted when the master state machine is in the default state. When this action is performed, the hardware sets this field to '0'.
2	M_ACK	RW	RW1C	0	When '1', attempt to transmit an acknowledgement (ACK). When this action is performed, the hardware sets this field to '0'.
3	M_NACK	RW	RW1C	0	When '1', attempt to transmit a negative acknowledgement (NACK). When this action is performed, the hardware sets this field to '0'.

Bits	Name	SW	HW	Default or Enum	Description
4	M_STOP	RW	RW1C	0	When '1', attempt to transmit a STOP. When this action is performed, the hardware sets this field to '0'. I2C_M_CMD.M_START has a higher priority than this command: in situations where both a STOP and a REPEATED START could be transmitted, M_START takes precedence over M_STOP.

17.3.15 SCB_I2C_S_CMD

Description: I2C slave command register.
Address: 0x4024006C
Offset: 0x6C
Retention: Not Retained
IsDeepSleep: No
Comment: The register fields are not retained. This is to ensure that they come up as '0' after coming out of DeepSleep system power mode.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:2]						S_NACK [1:1]	S_ACK [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	S_ACK	RW	RW1C	0	When '1', attempt to transmit an acknowledgement (ACK). When this action is performed, the hardware sets this field to '0'. In EZ mode, this field should be set to '0' (it is only to be used in non EZ mode).
1	S_NACK	RW	RW1C	0	When '1', attempt to transmit a negative acknowledgement (NACK). When this action is performed, the hardware sets this field to '0'. In EZ mode, this field should be set to '0' (it is only to be used in non EZ mode). This command has a higher priority than I2C_S_CMD.S_ACK, I2C_CTRL.S_READY_ADDR_ACK or I2C_CTRL.S_READY_DATA_ACK.

17.3.16 SCB_I2C_CFG

Description: I2C configuration register.
Address: 0x40240070
Offset: 0x70
Retention: Retained
IsDeepSleep: No
Comment: The filters are used to remove glitches and to guarantee I2C compliant SCL and SDA setup and hold times. The filters are trimmable.
Default: 0x2A1013

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:5]			SDA_IN_FILT_SEL [4:4]	None [3:2]		SDA_IN_FILT_TRIM [1:0]	

Bits	15	14	13	12	11	10	9	8
Name	None [15:13]			SCL_IN_FILT_SEL [12:12]	None [11:10]		SCL_IN_FILT_TRIM [9:8]	

Bits	23	22	21	20	19	18	17	16
Name	None [23:22]		SDA_OUT_FILT2_TRIM [21:20]		SDA_OUT_FILT1_TRIM [19:18]		SDA_OUT_FILT0_TRIM [17:16]	

Bits	31	30	29	28	27	26	25	24
Name	None [31:30]		SDA_OUT_FILT_SEL [29:28]		None [27:24]			

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:1	SDA_IN_FILT_TRIM	RW	R	3	Trim settings for the 50ns glitch filter on the SDA input. Default setting meets the I2C glitch rejections specs. Programmability available if required
4	SDA_IN_FILT_SEL	RW	R	1	Enable for 50ns glitch filter on SDA input '0': 0 ns. '1: 50 ns (filter enabled).
8:9	SCL_IN_FILT_TRIM	RW	R	0	Trim settings for the 50ns glitch filter on the SCL input. Default setting meets the I2C glitch rejections specs. Programmability available if required
12	SCL_IN_FILT_SEL	RW	R	1	Enable for 50ns glitch filter on SCL input '0': 0 ns. '1: 50 ns (filter enabled).
16:17	SDA_OUT_FILT0_TRIM	RW	R	2	Trim settings for the 50ns delay filter on SDA output used to guarantee tHD_DAT I2C parameter. Default setting meets the I2C spec. Programmability available if required
18:19	SDA_OUT_FILT1_TRIM	RW	R	2	Trim settings for the 50ns delay filter on SDA output used to guarantee tHD_DAT I2C parameter. Default setting meets the I2C spec. Programmability available if required
20:21	SDA_OUT_FILT2_TRIM	RW	R	2	Trim settings for the 50ns delay filter on SDA output used to guarantee tHD_DAT I2C parameter. Default setting meets the I2C spec. Programmability available if required

Bits	Name	SW	HW	Default or Enum	Description
28:29	SDA_OUT_FILT_SEL	RW	R	0	Selection of cumulative filter delay on SDA output to meet tHD_DAT parameter '0': 0 ns. '1': 50 ns (filter 0 enabled). '2': 100 ns (filters 0 and 1 enabled). '3': 150 ns (filters 0, 1 and 2 enabled).

17.3.17 SCB_TX_CTRL

Description: Transmitter control register.
Address: 0x40240200
Offset: 0x200
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x107

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:4]				DATA_WIDTH [3:0]			

Bits	15	14	13	12	11	10	9	8
Name	None [15:9]							MSB _FIRST [8:8]

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:3	DATA_WIDTH	RW	R	7	Dataframe width. DATA_WIDTH + 1 is the amount of bits in a transmitted data frame. This number does not include start, parity and stop bits. For UART mode, the valid range is [3, 8]. For SPI, the valid range is [3, 15]. For I2C the only valid value is 7.
8	MSB_FIRST	RW	R	1	Least significant bit first ('0') or most significant bit first ('1'). For I2C, this field should be '1'.

17.3.18 SCB_TX_FIFO_CTRL

Description: Transmitter FIFO control register.
Address: 0x40240204
Offset: 0x204
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:4]				TRIGGER_LEVEL [3:0]			

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:18]						FREEZE [17:17]	CLEAR [16:16]

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:3	TRIGGER_LEVEL	RW	R	0	Trigger level. When the transmitter FIFO has less entries than the number of this field, a transmitter trigger event INTR_TX.TRIGGER is generated.
16	CLEAR	RW	R	0	When '1', the transmitter FIFO and transmitter shift register are cleared/invalidated. Invalidation will last for as long as this field is '1'. If a quick clear/invalidation is required, the field should be set to '1' and be followed by a set to '0'. If a clear/invalidation is required for an extended time period, the field should be set to '1' during the complete time period.
17	FREEZE	RW	R	0	When '1', hardware reads from the transmitter FIFO do not remove FIFO entries. Freeze will not advance the TX FIFO read pointer.

17.3.19 SCB_TX_FIFO_STATUS

Description: Transmitter FIFO status register.
Address: 0x40240208
Offset: 0x208
Retention: Not Retained
IsDeepSleep: No
Comment: This register is not used in EZ and CMD_RESP modes.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:5]			USED [4:0]				

Bits	15	14	13	12	11	10	9	8
Name	SR_VALID [15:15]	None [14:8]						

Bits	23	22	21	20	19	18	17	16
Name	None [23:20]				RD_PTR [19:16]			

Bits	31	30	29	28	27	26	25	24
Name	None [31:28]				WR_PTR [27:24]			

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:4	USED	R	W	0	Amount of entries in the transmitter FIFO. The value of this field ranges from 0 to FF_DATA_NR (EZ_DATA_NR/2).
15	SR_VALID	R	W	0	Indicates whether the TX shift registers holds a valid data frame ('1') or not ('0'). The shift register can be considered the top of the TX FIFO (the data frame is not included in the USED field of the TX FIFO). The shift register is a working register and holds the data frame that is currently transmitted (when the protocol state machine is transmitting a data frame) or the data frame that is transmitted next (when the protocol state machine is not transmitting a data frame).
16:19	RD_PTR	R	W	0	FIFO read pointer: FIFO location from which a data frame is read by the hardware.
24:27	WR_PTR	R	W	0	FIFO write pointer: FIFO location at which a new data frame is written.

17.3.20 SCB_TX_FIFO_WR

Description: Transmitter FIFO write register.
Address: 0x40240240
Offset: 0x240
Retention: Not Retained
IsDeepSleep: No
Comment: When the IP is disabled (CTRL.ENABLED is '0') or when the TX FIFO is full, a write to this register is dropped. This register should only be used in FIFO mode (and not in EZ or CMD_RESP modes). This register is 'write only'; a read from this register returns '0'.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:15	DATA	W	R	0	Data frame written into the transmitter FIFO. Behavior is similar to that of a PUSH operation. Note that when CTRL.BYTE_MODE is '1', only DATA[7:0] are used. A write to a full TX FIFO sets INTR_TX.OVERFLOW to '1'.

17.3.21 SCB_RX_CTRL

Description: Receiver control register.
Address: 0x40240300
Offset: 0x300
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x107

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:4]				DATA_WIDTH [3:0]			

Bits	15	14	13	12	11	10	9	8
Name	None [15:10]						MEDIAN [9:9]	MSB _FIRST [8:8]

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:3	DATA_WIDTH	RW	R	7	Dataframe width. DATA_WIDTH + 1 is the expected amount of bits in received data frame. This number does not include start, parity and stop bits. For UART mode, the valid range is [3, 8]. For SPI, the valid range is [3, 15]. For I2C the only valid value is 7. In EZ mode (for both SPI and I2C), the only valid value is 7.
8	MSB_FIRST	RW	R	1	Least significant bit first ('0') or most significant bit first ('1'). For I2C, this field should be '1'.
9	MEDIAN	RW	R	0	Median filter. When '1', a digital 3 taps median filter is performed on input interface lines. This filter should reduce the susceptibility to errors. However, its requires higher oversampling values. For UART IrDA submode, this field should always be '1'.

17.3.22 SCB_RX_FIFO_CTRL

Description: Receiver FIFO control register.
Address: 0x40240304
Offset: 0x304
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:4]				TRIGGER_LEVEL [3:0]			

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:18]						FREEZE [17:17]	CLEAR [16:16]

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:3	TRIGGER_LEVEL	RW	R	0	Trigger level. When the receiver FIFO has more entries than the number of this field, a receiver trigger event INTR_RX.TRIGGER is generated.
16	CLEAR	RW	R	0	When '1', the receiver FIFO and receiver shift register are cleared/invalidated. Invalidation will last for as long as this field is '1'. If a quick clear/invalidation is required, the field should be set to '1' and be followed by a set to '0'. If a clear/invalidation is required for an extended time period, the field should be set to '1' during the complete time period.
17	FREEZE	RW	R	0	When '1', hardware writes to the receiver FIFO have no effect. Freeze will not advance the RX FIFO write pointer.

17.3.23 SCB_RX_FIFO_STATUS

Description: Receiver FIFO status register.
Address: 0x40240308
Offset: 0x308
Retention: Not Retained
IsDeepSleep: No
Comment: This register is not used in EZ and CMD_RESP modes.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:5]			USED [4:0]				

Bits	15	14	13	12	11	10	9	8
Name	SR_VALID [15:15]	None [14:8]						

Bits	23	22	21	20	19	18	17	16
Name	None [23:20]				RD_PTR [19:16]			

Bits	31	30	29	28	27	26	25	24
Name	None [31:28]				WR_PTR [27:24]			

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:4	USED	R	W	0	Amount of entries in the receiver FIFO. The value of this field ranges from 0 to FF_DATA_NR (EZ_DATA_NR/2).
15	SR_VALID	R	W	0	Indicates whether the RX shift registers holds a (partial) valid data frame ('1') or not ('0'). The shift register can be considered the bottom of the RX FIFO (the data frame is not included in the USED field of the RX FIFO). The shift register is a working register and holds the data frame that is currently being received (when the protocol state machine is receiving a data frame).
16:19	RD_PTR	R	W	0	FIFO read pointer: FIFO location from which a data frame is read.
24:27	WR_PTR	R	W	0	FIFO write pointer: FIFO location at which a new data frame is written by the hardware.

17.3.24 SCB_RX_MATCH

Description: Slave address and mask register.
Address: 0x40240310
Offset: 0x310
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	MASK [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:7	ADDR	RW	R	0	Slave device address. In UART multi-processor mode, all 8 bits are used. In I2C slave mode, only bits 7 down to 1 are used. This reflects the organization of the first transmitted byte in a I2C transfer: the first 7 bits represent the address of the addressed slave, and the last 1 bit is a read/write indicator ('0': write, '1': read).
16:23	MASK	RW	R	0	Slave device address mask. This field is a mask that specifies which of the slave address bits take part in the matching. MATCH = ((ADDR & MASK) == ('slave address' & MASK)).

17.3.25 SCB_RX_FIFO_RD

Description: Receiver FIFO read register.
Address: 0x40240340
Offset: 0x340
Retention: Not Retained
IsDeepSleep: No
Comment: When the IP is disabled (CTRL.ENABLED is '0') or when the RX FIFO is empty, a read from this register returns 0xffff:ffff. This register should only be used in FIFO mode (and not in EZ or CMD_RESP modes). This register is 'read only'; a write to this register is ignored.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:15	DATA	R	W	Undefined	Data read from the receiver FIFO. Reading a data frame will remove the data frame from the FIFO; i.e. behavior is similar to that of a POP operation. Note that when CTRL.BYTE_MODE is '1', only DATA[7:0] are used. A read from an empty RX FIFO sets INTR_RX.UNDERFLOW to '1'. When this register is read through the debugger, the data frame will not be removed from the FIFO. Similar in operation to RX_FIFO_RD_SILENT

17.3.26 SCB_RX_FIFO_RD_SILENT

Description: Receiver FIFO read register.
Address: 0x40240344
Offset: 0x344
Retention: Not Retained
IsDeepSleep: No
Comment: When the IP is disabled (CTRL.ENABLED is '0') or when the RX FIFO is empty, a read from this register returns 0xffff:ffff. This register should only be used in FIFO mode (and not in EZ or CMD_RESP modes).
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:15	DATA	R	W	Undefined	Data read from the receiver FIFO. Reading a data frame will NOT remove the data frame from the FIFO; i.e. behavior is similar to that of a PEEK operation. Note that when CTRL.BYTE_MODE is '1', only DATA[7:0] are used. A read from an empty RX FIFO sets INTR_RX.UNDERFLOW to '1'.

17.3.27 SCB_EZ_DATA

Description: Memory buffer registers.
Address: 0x40240400
Offset: 0x400
Retention: Retained
IsDeepSleep: Yes
Comment: When the IP is disabled (CTRL.ENABLED is '0'), a read from these registers return 0xffff:ffff. It is under MMIO register control whether accesses to this register should introduce bus wait states or be discarded when the externally clocked logic is accessing the memory structure. These registers should only be used in EZ and CMD_RESP modes (and not in FIFO mode).
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:7	EZ_DATA	RW	RW	Undefined	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value.

17.3.28 SCB_INTR_CAUSE

Description: Active clocked interrupt signal register
Address: 0x40240E00
Offset: 0xE00
Retention: Retained
IsDeepSleep: Yes
Comment: Enables software to determine the source of the combined interrupt output signals 'interrupt_ic', 'interrupt_ec' and 'interrupt'.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:6]		SPI_EC [5:5]	I2C_EC [4:4]	RX [3:3]	TX [2:2]	S [1:1]	M [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	M	R	W	0	Master interrupt active ('interrupt_master'): INTR_M_MASKED != 0.
1	S	R	W	0	Slave interrupt active ('interrupt_slave'): INTR_S_MASKED != 0.
2	TX	R	W	0	Transmitter interrupt active ('interrupt_tx'): INTR_TX_MASKED != 0.
3	RX	R	W	0	Receiver interrupt active ('interrupt_rx'): INTR_RX_MASKED != 0.
4	I2C_EC	R	W	0	Externally clock I2C interrupt active ('interrupt_i2c_ec'): INTR_I2C_EC_MASKED != 0.
5	SPI_EC	R	W	0	Externally clocked SPI interrupt active ('interrupt_spi_ec'): INTR_SPI_EC_MASKED != 0.

17.3.29 SCB_INTR_I2C_EC

Description: Externally clocked I2C interrupt request register
Address: 0x40240E80
Offset: 0xE80
Retention: Retained
IsDeepSleep: Yes
Comment: The fields in this register are set by HW and are cleared by software by writing a '1'. These interrupt causes are generated by externally clocked logic. HW clears the interrupt causes to '0', when the IP is disabled.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:4]				EZ_READ_STOP [3:3]	EZ_WRITE_STOP [2:2]	EZ_STOP [1:1]	WAKE_UP [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	WAKE_UP	RW1C	A	0	Wake up request. Active on incoming slave request (with address match). Only used when CTRL.EC_AM_MODE is '1'.
1	EZ_STOP	RW1C	A	0	STOP detection. Activated on the end of a every transfer (I2C STOP). Only available for a slave request with an address match, in EZ and CMD_RESP modes, when CTRL.EC_OP_MODE is '1'.
2	EZ_WRITE_STOP	RW1C	A	0	STOP detection after a write transfer occurred. Activated on the end of a write transfer (I2C STOP). This event is an indication that a buffer memory location has been written to. For EZ mode: a transfer that only writes the base address does NOT activate this event. Only available for a slave request with an address match, in EZ and CMD_RESP modes, when CTRL.EC_OP_MODE is '1'.
3	EZ_READ_STOP	RW1C	A	0	STOP detection after a read transfer occurred. Activated on the end of a read transfer (I2C STOP). This event is an indication that a buffer memory location has been read from. Only available for a slave request with an address match, in EZ and CMD_RESP modes, when CTRL.EC_OP_MODE is '1'.

17.3.30 SCB_INTR_I2C_EC_MASK

Description: Externally clocked I2C interrupt mask register
Address: 0x40240E88
Offset: 0xE88
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:4]				EZ_READ_STOP [3:3]	EZ_WRITE_STOP [2:2]	EZ_STOP [1:1]	WAKE_UP [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	WAKE_UP	RW	R	0	Mask bit for corresponding bit in interrupt request register.
1	EZ_STOP	RW	R	0	Mask bit for corresponding bit in interrupt request register.
2	EZ_WRITE_STOP	RW	R	0	Mask bit for corresponding bit in interrupt request register.
3	EZ_READ_STOP	RW	R	0	Mask bit for corresponding bit in interrupt request register.

17.3.31 SCB_INTR_I2C_EC_MASKED

Description: Externally clocked I2C interrupt masked register
Address: 0x40240E8C
Offset: 0xE8C
Retention: Retained
IsDeepSleep: Yes
Comment: When read, this register reflects a bitwise and between the interrupt request and mask registers. This register allows SW to read the status of all mask enabled interrupt causes with a single load operation, rather than two load operations: one for the interrupt causes and one for the masks. This simplifies Firmware development. The associated interrupt is active ('1'), when INTR_I2C_EC_MASKED != 0.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:4]				EZ_READ_STOP [3:3]	EZ_WRITE_STOP [2:2]	EZ_STOP [1:1]	WAKE_UP [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	WAKE_UP	R	W	0	Logical and of corresponding request and mask bits.
1	EZ_STOP	R	W	0	Logical and of corresponding request and mask bits.
2	EZ_WRITE_STOP	R	W	0	Logical and of corresponding request and mask bits.
3	EZ_READ_STOP	R	W	0	Logical and of corresponding request and mask bits.

17.3.32 SCB_INTR_SPI_EC

Description: Externally clocked SPI interrupt request register
Address: 0x40240EC0
Offset: 0xEC0
Retention: Retained
IsDeepSleep: Yes
Comment: The fields in this register are set by HW and are cleared by software by writing a '1'. These interrupt causes are generated by externally clocked logic. HW clears the interrupt causes to '0', when the IP is disabled.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:4]				EZ_READ_STOP [3:3]	EZ_WRITE_STOP [2:2]	EZ_STOP [1:1]	WAKE_UP [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	WAKE_UP	RW1C	A	0	Wake up request. Active on incoming slave request when externally clocked selection is '1'. Only used when CTRL.EC_AM_MODE is '1'.
1	EZ_STOP	RW1C	A	0	STOP detection. Activated on the end of a every transfer (SPI deselection). Only available in EZ and CMD_RESP mode and when CTRL.EC_OP_MODE is '1'.
2	EZ_WRITE_STOP	RW1C	A	0	STOP detection after a write transfer occurred. Activated on the end of a write transfer (SPI deselection). This event is an indication that a buffer memory location has been written to. For EZ mode: a transfer that only writes the base address does NOT activate this event. Only used in EZ and CMD_RESP modes and when CTRL.EC_OP_MODE is '1'.
3	EZ_READ_STOP	RW1C	A	0	STOP detection after a read transfer occurred. Activated on the end of a read transfer (SPI deselection). This event is an indication that a buffer memory location has been read from. Only used in EZ and CMD_RESP modes and when CTRL.EC_OP_MODE is '1'.

17.3.33 SCB_INTR_SPI_EC_MASK

Description: Externally clocked SPI interrupt mask register
Address: 0x40240EC8
Offset: 0xEC8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:4]				EZ_READ_STOP [3:3]	EZ_WRITE_STOP [2:2]	EZ_STOP [1:1]	WAKE_UP [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	WAKE_UP	RW	R	0	Mask bit for corresponding bit in interrupt request register.
1	EZ_STOP	RW	R	0	Mask bit for corresponding bit in interrupt request register.
2	EZ_WRITE_STOP	RW	R	0	Mask bit for corresponding bit in interrupt request register.
3	EZ_READ_STOP	RW	R	0	Mask bit for corresponding bit in interrupt request register.

17.3.34 SCB_INTR_SPI_EC_MASKED

Description: Externally clocked SPI interrupt masked register
Address: 0x40240ECC
Offset: 0xECC
Retention: Retained
IsDeepSleep: Yes
Comment: When read, this register reflects a bitwise and between the interrupt request and mask registers. This register allows SW to read the status of all mask enabled interrupt causes with a single load operation, rather than two load operations: one for the interrupt causes and one for the masks. This simplifies Firmware development. The associated interrupt is active ('1'), when INTR_SPI_EC_MASKED != 0.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:4]				EZ_READ_STOP [3:3]	EZ_WRITE_STOP [2:2]	EZ_STOP [1:1]	WAKE_UP [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	WAKE_UP	R	W	0	Logical and of corresponding request and mask bits.
1	EZ_STOP	R	W	0	Logical and of corresponding request and mask bits.
2	EZ_WRITE_STOP	R	W	0	Logical and of corresponding request and mask bits.
3	EZ_READ_STOP	R	W	0	Logical and of corresponding request and mask bits.

17.3.35 SCB_INTR_M

Description: Master interrupt request register.
Address: 0x40240F00
Offset: 0xF00
Retention: Not Retained
IsDeepSleep: No
Comment: The register fields are not retained In DeepSleep power mode: HW clears the interrupt causes to '0', when coming out of DeepSleep power mode. In addition, HW clears the interrupt causes to '0', when the IP is disabled. As a result, the interrupt causes are only available in Active/Sleep power modes; they are generated by internally clocked logic (this logic operates on a clock that is only available in Active/Sleep power modes).

The interrupt causes should only be used for internally clocked operation; i.e. EC_OP is '0'.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:5]			I2C_STOP [4:4]	None [3:3]	I2C_ACK [2:2]	I2C_NACK [1:1]	I2C_ARB_LOST [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:10]						SPI_DONE [9:9]	I2C_BUS_ERROR [8:8]

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	I2C_ARB_LOST	RW1C	RW1S	0	I2C master lost arbitration: the value driven by the master on the SDA line is not the same as the value observed on the SDA line.
1	I2C_NACK	RW1C	RW1S	0	I2C master negative acknowledgement. Set to '1', when the master receives a NACK (typically after the master transmitted the slave address or TX data).
2	I2C_ACK	RW1C	RW1S	0	I2C master acknowledgement. Set to '1', when the master receives a ACK (typically after the master transmitted the slave address or TX data).
4	I2C_STOP	RW1C	RW1S	0	I2C master STOP. Set to '1', when the master has transmitted a STOP.
8	I2C_BUS_ERROR	RW1C	RW1S	0	I2C master bus error (unexpected detection of START or STOP condition).
9	SPI_DONE	RW1C	RW1S	0	SPI master transfer done event: all data frames in the transmit FIFO are sent and the transmit FIFO and shift register are empty.

17.3.36 SCB_INTR_M_SET

Description: Master interrupt set request register
Address: 0x40240F04
Offset: 0xF04
Retention: Not Retained
IsDeepSleep: No
Comment: When read, this register reflects the interrupt request register.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:5]			I2C_STOP [4:4]	None [3:3]	I2C_ACK [2:2]	I2C_NACK [1:1]	I2C_ARB_LOST [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:10]						SPI_DONE [9:9]	I2C_BUS_ERROR [8:8]

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	I2C_ARB_LOST	RW1S	A	0	Write with '1' to set corresponding bit in interrupt request register.
1	I2C_NACK	RW1S	A	0	Write with '1' to set corresponding bit in interrupt request register.
2	I2C_ACK	RW1S	A	0	Write with '1' to set corresponding bit in interrupt request register.
4	I2C_STOP	RW1S	A	0	Write with '1' to set corresponding bit in interrupt request register.
8	I2C_BUS_ERROR	RW1S	A	0	Write with '1' to set corresponding bit in interrupt request register.
9	SPI_DONE	RW1S	A	0	Write with '1' to set corresponding bit in interrupt request register.

17.3.37 SCB_INTR_M_MASK

Description: Master interrupt mask register.
Address: 0x40240F08
Offset: 0xF08
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:5]			I2C_STOP [4:4]	None [3:3]	I2C_ACK [2:2]	I2C_NACK [1:1]	I2C_ARB_LOST [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:10]						SPI_DONE [9:9]	I2C_BUS_ERROR [8:8]

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	I2C_ARB_LOST	RW	R	0	Mask bit for corresponding bit in interrupt request register.
1	I2C_NACK	RW	R	0	Mask bit for corresponding bit in interrupt request register.
2	I2C_ACK	RW	R	0	Mask bit for corresponding bit in interrupt request register.
4	I2C_STOP	RW	R	0	Mask bit for corresponding bit in interrupt request register.
8	I2C_BUS_ERROR	RW	R	0	Mask bit for corresponding bit in interrupt request register.
9	SPI_DONE	RW	R	0	Mask bit for corresponding bit in interrupt request register.

17.3.38 SCB_INTR_M_MASKED

Description: Master interrupt masked request register
Address: 0x40240F0C
Offset: 0xF0C
Retention: Not Retained
IsDeepSleep: No
Comment: When read, this register reflects a bitwise and between the interrupt request and mask registers. This register allows SW to read the status of all mask enabled interrupt causes with a single load operation, rather than two load operations: one for the interrupt causes and one for the masks. This simplifies Firmware development. The associated interrupt is active ('1'), when INTR_M_MASKED != 0.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:5]			I2C_STOP [4:4]	None [3:3]	I2C_ACK [2:2]	I2C_NACK [1:1]	I2C_ARB_LOST [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:10]						SPI_DONE [9:9]	I2C_BUS_ERROR [8:8]

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	I2C_ARB_LOST	R	W	0	Logical and of corresponding request and mask bits.
1	I2C_NACK	R	W	0	Logical and of corresponding request and mask bits.
2	I2C_ACK	R	W	0	Logical and of corresponding request and mask bits.
4	I2C_STOP	R	W	0	Logical and of corresponding request and mask bits.
8	I2C_BUS_ERROR	R	W	0	Logical and of corresponding request and mask bits.
9	SPI_DONE	R	W	0	Logical and of corresponding request and mask bits.

17.3.39 SCB_INTR_S

Description: Slave interrupt request register.
Address: 0x40240F40
Offset: 0xF40
Retention: Not Retained
IsDeepSleep: No
Comment: The register fields are not retained In DeepSleep power mode: HW clears the interrupt causes to '0', when coming out of DeepSleep power mode. In addition, HW clears the interrupt causes to '0', when the IP is disabled. As a result, the interrupt causes are only available in Active/Sleep power modes; they are generated by internally clocked logic (this logic operates on a clock that is only available in Active/Sleep power modes).

The interrupt causes should only be used for internally clocked operation; i.e. EC_OP is '0'.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	I2C_GENERAL [7:7]	I2C_ADDR_MATCH [6:6]	I2C_START [5:5]	I2C_STOP [4:4]	I2C_WRITE_STOP [3:3]	I2C_ACK [2:2]	I2C_NACK [1:1]	I2C_ARB_LOST [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:12]				SPI_BUS_ERROR [11:11]	SPI_EZ_STOP [10:10]	SPI_EZ_WRITE_STOP [9:9]	I2C_BUS_ERROR [8:8]

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	I2C_ARB_LOST	RW1C	RW1S	0	I2C slave lost arbitration: the value driven on the SDA line is not the same as the value observed on the SDA line (while the SCL line is '1'). This should not occur, it represents erroneous I2C bus behavior. In case of lost arbitration, the I2C slave state machine aborts the ongoing transfer. The Firmware may decide to clear the TX and RX FIFOs in case of this error.
1	I2C_NACK	RW1C	RW1S	0	I2C slave negative acknowledgement received. Set to '1', when the slave receives a NACK (typically after the slave transmitted TX data).
2	I2C_ACK	RW1C	RW1S	0	I2C slave acknowledgement received. Set to '1', when the slave receives a ACK (typically after the slave transmitted TX data).

Bits	Name	SW	HW	Default or Enum	Description
3	I2C_WRITE_STOP	RW1C	RW1S	0	I2C STOP event for I2C write transfer intended for this slave (address matching is performed). Set to '1', when STOP or REPEATED START event is detected. The REPEATED START event is included in this interrupt cause such that the I2C transfers separated by a REPEATED START can be distinguished and potentially treated separately by the Firmware. Note that the second I2C transfer (after a REPEATED START) may be to a different slave address. In non EZ mode, the event is detected on any I2C write transfer intended for this slave. Note that a I2C write address intended for the slave (address is matching and a it is a write transfer) will result in a I2C_WRITE_STOP event independent of whether the I2C address is ACK'd or NACK'd. In EZ mode, the event is detected only on I2C write transfers that have EZ data written to the memory structure (an I2C write transfer that only communicates an I2C address and EZ address, will not result in this event being detected).
4	I2C_STOP	RW1C	RW1S	0	I2C STOP event for I2C (read or write) transfer intended for this slave (address matching is performed). Set to '1', when STOP or REPEATED START event is detected. The REPEATED START event is included in this interrupt cause such that the I2C transfers separated by a REPEATED START can be distinguished and potentially treated separately by the Firmware. Note that the second I2C transfer (after a REPEATED START) may be to a different slave address. The event is detected on any I2C transfer intended for this slave. Note that a I2C address intended for the slave (address is matching) will result in a I2C_STOP event independent of whether the I2C address is ACK'd or NACK'd.
5	I2C_START	RW1C	RW1S	0	I2C slave START received. Set to '1', when START or REPEATED START event is detected. In the case of externally clocked address matching (CTRL.EC_AM_MODE is '1') AND clock stretching is performed (I2C_CTRL.S_NOT_READY_ADDR_NACK is '0'), this field is NOT set. The Firmware should use INTR_S_EC.WAKE_UP, INTR_S.I2C_ADDR_MATCH and INTR_S.I2C_GENERAL.
6	I2C_ADDR_MATCH	RW1C	RW1S	0	I2C slave matching address received. If CTRL.ADDR_ACCEPT, the received address (including the R/W bit) is available in the RX FIFO. In the case of externally clocked address matching (CTRL.EC_AM_MODE is '1') and internally clocked operation (CTRL.EC_OP_MODE is '0'), this field is set when the event is detected.
7	I2C_GENERAL	RW1C	RW1S	0	I2C slave general call address received. If CTRL.ADDR_ACCEPT, the received address 0x00 (including the R/W bit) is available in the RX FIFO. In the case of externally clocked address matching (CTRL.EC_AM_MODE is '1') and internally clocked operation (CTRL.EC_OP_MODE is '0'), this field is set when the event is detected.

Bits	Name	SW	HW	Default or Enum	Description
8	I2C_BUS_ERROR	RW1C	RW1S	0	I2C slave bus error (unexpected detection of START or STOP condition). This should not occur, it represents erroneous I2C bus behavior. In case of a bus error, the I2C slave state machine abort the ongoing transfer. The Firmware may decide to clear the TX and RX FIFOs in case of this error.
9	SPI_EZ_WRITE_STOP	RW1C	RW1S	0	SPI slave deselected after a write EZ SPI transfer occurred.
10	SPI_EZ_STOP	RW1C	RW1S	0	SPI slave deselected after any EZ SPI transfer occurred.
11	SPI_BUS_ERROR	RW1C	RW1S	0	SPI slave deselected at an unexpected time in the SPI transfer. The Firmware may decide to clear the TX and RX FIFOs in case of this error.

17.3.40 SCB_INTR_S_SET

Description: Slave interrupt set request register.
Address: 0x40240F44
Offset: 0xF44
Retention: Not Retained
IsDeepSleep: No
Comment: When read, this register reflects the interrupt request register.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	I2C_GENERAL [7:7]	I2C_ADDR_MATCH [6:6]	I2C_START [5:5]	I2C_STOP [4:4]	I2C_WRITE_STOP [3:3]	I2C_ACK [2:2]	I2C_NACK [1:1]	I2C_ARB_LOST [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:12]				SPI_BUS_ERROR [11:11]	SPI_EZ_STOP [10:10]	SPI_EZ_WRITE_STOP [9:9]	I2C_BUS_ERROR [8:8]

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	I2C_ARB_LOST	RW1S	A	0	Write with '1' to set corresponding bit in interrupt request register.
1	I2C_NACK	RW1S	A	0	Write with '1' to set corresponding bit in interrupt request register.
2	I2C_ACK	RW1S	A	0	Write with '1' to set corresponding bit in interrupt request register.
3	I2C_WRITE_STOP	RW1S	A	0	Write with '1' to set corresponding bit in interrupt request register.
4	I2C_STOP	RW1S	A	0	Write with '1' to set corresponding bit in interrupt request register.
5	I2C_START	RW1S	A	0	Write with '1' to set corresponding bit in interrupt request register.
6	I2C_ADDR_MATCH	RW1S	A	0	Write with '1' to set corresponding bit in interrupt request register.
7	I2C_GENERAL	RW1S	A	0	Write with '1' to set corresponding bit in interrupt request register.
8	I2C_BUS_ERROR	RW1S	A	0	Write with '1' to set corresponding bit in interrupt request register.
9	SPI_EZ_WRITE_STOP	RW1S	A	0	Write with '1' to set corresponding bit in interrupt request register.
10	SPI_EZ_STOP	RW1S	A	0	Write with '1' to set corresponding bit in interrupt request register.
11	SPI_BUS_ERROR	RW1S	A	0	Write with '1' to set corresponding bit in interrupt request register.

17.3.41 SCB_INTR_S_MASK

Description: Slave interrupt mask register.
Address: 0x40240F48
Offset: 0xF48
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	I2C_GENERAL [7:7]	I2C_ADDR_MATCH [6:6]	I2C_START [5:5]	I2C_STOP [4:4]	I2C_WRITE_STOP [3:3]	I2C_ACK [2:2]	I2C_NACK [1:1]	I2C_ARB_LOST [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:12]				SPI_BUS_ERROR [11:11]	SPI_EZ_STOP [10:10]	SPI_EZ_WRITE_STOP [9:9]	I2C_BUS_ERROR [8:8]

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	I2C_ARB_LOST	RW	R	0	Mask bit for corresponding bit in interrupt request register.
1	I2C_NACK	RW	R	0	Mask bit for corresponding bit in interrupt request register.
2	I2C_ACK	RW	R	0	Mask bit for corresponding bit in interrupt request register.
3	I2C_WRITE_STOP	RW	R	0	Mask bit for corresponding bit in interrupt request register.
4	I2C_STOP	RW	R	0	Mask bit for corresponding bit in interrupt request register.
5	I2C_START	RW	R	0	Mask bit for corresponding bit in interrupt request register.
6	I2C_ADDR_MATCH	RW	R	0	Mask bit for corresponding bit in interrupt request register.
7	I2C_GENERAL	RW	R	0	Mask bit for corresponding bit in interrupt request register.
8	I2C_BUS_ERROR	RW	R	0	Mask bit for corresponding bit in interrupt request register.
9	SPI_EZ_WRITE_STOP	RW	R	0	Mask bit for corresponding bit in interrupt request register.
10	SPI_EZ_STOP	RW	R	0	Mask bit for corresponding bit in interrupt request register.
11	SPI_BUS_ERROR	RW	R	0	Mask bit for corresponding bit in interrupt request register.

17.3.42 SCB_INTR_S_MASKED

Description: Slave interrupt masked request register
Address: 0x40240F4C
Offset: 0xF4C
Retention: Not Retained
IsDeepSleep: No
Comment: When read, this register reflects a bitwise and between the interrupt request and mask registers. This register allows SW to read the status of all mask enabled interrupt causes with a single load operation, rather than two load operations: one for the interrupt causes and one for the masks. This simplifies Firmware development. The associated interrupt is active ('1'), when INTR_S_MASKED != 0.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	I2C_GENERAL [7:7]	I2C_ADDR_MATCH [6:6]	I2C_START [5:5]	I2C_STOP [4:4]	I2C_WRITE_STOP [3:3]	I2C_ACK [2:2]	I2C_NACK [1:1]	I2C_ARB_LOST [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:12]				SPI_BUS_ERROR [11:11]	SPI_EZ_STOP [10:10]	SPI_EZ_WRITE_STOP [9:9]	I2C_BUS_ERROR [8:8]

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	I2C_ARB_LOST	R	W	0	Logical and of corresponding request and mask bits.
1	I2C_NACK	R	W	0	Logical and of corresponding request and mask bits.
2	I2C_ACK	R	W	0	Logical and of corresponding request and mask bits.
3	I2C_WRITE_STOP	R	W	0	Logical and of corresponding request and mask bits.
4	I2C_STOP	R	W	0	Logical and of corresponding request and mask bits.
5	I2C_START	R	W	0	Logical and of corresponding request and mask bits.
6	I2C_ADDR_MATCH	R	W	0	Logical and of corresponding request and mask bits.
7	I2C_GENERAL	R	W	0	Logical and of corresponding request and mask bits.
8	I2C_BUS_ERROR	R	W	0	Logical and of corresponding request and mask bits.
9	SPI_EZ_WRITE_STOP	R	W	0	Logical and of corresponding request and mask bits.
10	SPI_EZ_STOP	R	W	0	Logical and of corresponding request and mask bits.
11	SPI_BUS_ERROR	R	W	0	Logical and of corresponding request and mask bits.

17.3.43 SCB_INTR_TX

Description: Transmitter interrupt request register.
Address: 0x40240F80
Offset: 0xF80
Retention: Not Retained
IsDeepSleep: No
Comment: The register fields are not retained In DeepSleep power mode: HW clears the interrupt causes to '0', when coming out of DeepSleep power mode. In addition, HW clears the interrupt causes to '0', when the IP is disabled. As a result, the interrupt causes are only available in Active/Sleep power modes; they are generated by internally clocked logic (this logic operates on a clock that is only available in Active/Sleep power modes).
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	BLOCKED [7:7]	UNDERFLOW [6:6]	OVERFLOW [5:5]	EMPTY [4:4]	None [3:2]		NOT_FULL [1:1]	TRIGGER [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:11]					UART_ARB_LOST [10:10]	UART_DONE [9:9]	UART_NACK [8:8]

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	TRIGGER	RW1C	RW1S	0	Less entries in the TX FIFO than the value specified by TX_FIFO_CTRL. Only used in FIFO mode.
1	NOT_FULL	RW1C	RW1S	0	TX FIFO is not full. Dependent on CTRL.BYTE_MODE: (FF_DATA_NR = EZ_DATA_NR/2) BYTE_MODE is '0': # entries != FF_DATA_NR/2. BYTE_MODE is '1': # entries != FF_DATA_NR. Only used in FIFO mode.
4	EMPTY	RW1C	RW1S	0	TX FIFO is empty; i.e. it has 0 entries. Only used in FIFO mode.
5	OVERFLOW	RW1C	RW1S	0	Attempt to write to a full TX FIFO. Only used in FIFO mode.
6	UNDERFLOW	RW1C	RW1S	0	Attempt to read from an empty TX FIFO. This happens when SCB is ready to transfer data and EMPTY is '1'. Only used in FIFO mode.
7	BLOCKED	RW1C	RW1S	0	SW cannot get access to the EZ memory (EZ data access), due to an externally clocked EZ access. This may happen when STATUS.EC_BUSY is '1'.
8	UART_NACK	RW1C	RW1S	0	UART transmitter received a negative acknowledgement in SmartCard mode. Set to '1', when event is detected. Write with '1' to clear bit.

Bits	Name	SW	HW	Default or Enum	Description
9	UART_DONE	RW1C	RW1S	0	UART transmitter done event. This happens when the IP is done transferring all data in the TX FIFO; i.e. EMPTY is '1'. Set to '1', when event is detected. Write with '1' to clear bit.
10	UART_ARB_LOST	RW1C	RW1S	0	UART lost arbitration: the value driven on the TX line is not the same as the value observed on the RX line. This condition event is useful when transmitter and receiver share a TX/RX line. This is the case in LIN or SmartCard modes. Set to '1', when event is detected. Write with '1' to clear bit.

17.3.44 SCB_INTR_TX_SET

Description: Transmitter interrupt set request register
Address: 0x40240F84
Offset: 0xF84
Retention: Not Retained
IsDeepSleep: No
Comment: When read, this register reflects the interrupt request register.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	BLOCKED [7:7]	UNDERFLOW [6:6]	OVERFLOW [5:5]	EMPTY [4:4]	None [3:2]		NOT_FULL [1:1]	TRIGGER [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:11]					UART_ARB_LOST [10:10]	UART_DONE [9:9]	UART_NACK [8:8]

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	TRIGGER	RW1S	A	0	Write with '1' to set corresponding bit in interrupt request register.
1	NOT_FULL	RW1S	A	0	Write with '1' to set corresponding bit in interrupt request register.
4	EMPTY	RW1S	A	0	Write with '1' to set corresponding bit in interrupt request register.
5	OVERFLOW	RW1S	A	0	Write with '1' to set corresponding bit in interrupt request register.
6	UNDERFLOW	RW1S	A	0	Write with '1' to set corresponding bit in interrupt request register.
7	BLOCKED	RW1S	A	0	Write with '1' to set corresponding bit in interrupt request register.
8	UART_NACK	RW1S	A	0	Write with '1' to set corresponding bit in interrupt request register.
9	UART_DONE	RW1S	A	0	Write with '1' to set corresponding bit in interrupt request register.
10	UART_ARB_LOST	RW1S	A	0	Write with '1' to set corresponding bit in interrupt request register.

17.3.45 SCB_INTR_TX_MASK

Description: Transmitter interrupt mask register.
Address: 0x40240F88
Offset: 0xF88
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	BLOCKED [7:7]	UNDERFLOW [6:6]	OVERFLOW [5:5]	EMPTY [4:4]	None [3:2]		NOT_FULL [1:1]	TRIGGER [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:11]					UART_ARB_LOST [10:10]	UART_DONE [9:9]	UART_NACK [8:8]

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	TRIGGER	RW	R	0	Mask bit for corresponding bit in interrupt request register.
1	NOT_FULL	RW	R	0	Mask bit for corresponding bit in interrupt request register.
4	EMPTY	RW	R	0	Mask bit for corresponding bit in interrupt request register.
5	OVERFLOW	RW	R	0	Mask bit for corresponding bit in interrupt request register.
6	UNDERFLOW	RW	R	0	Mask bit for corresponding bit in interrupt request register.
7	BLOCKED	RW	R	0	Mask bit for corresponding bit in interrupt request register.
8	UART_NACK	RW	R	0	Mask bit for corresponding bit in interrupt request register.
9	UART_DONE	RW	R	0	Mask bit for corresponding bit in interrupt request register.
10	UART_ARB_LOST	RW	R	0	Mask bit for corresponding bit in interrupt request register.

17.3.46 SCB_INTR_TX_MASKED

Description: Transmitter interrupt masked request register
Address: 0x40240F8C
Offset: 0xF8C
Retention: Not Retained
IsDeepSleep: No
Comment: When read, this register reflects a bitwise and between the interrupt request and mask registers. This register allows SW to read the status of all mask enabled interrupt causes with a single load operation, rather than two load operations: one for the interrupt causes and one for the masks. This simplifies Firmware development. The associated interrupt is active ('1'), when INTR_TX_MASKED != 0.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	BLOCKED [7:7]	UNDERFLOW [6:6]	OVERFLOW [5:5]	EMPTY [4:4]	None [3:2]		NOT_FULL [1:1]	TRIGGER [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:11]					UART_ARB_LOST [10:10]	UART_DONE [9:9]	UART_NACK [8:8]

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	TRIGGER	R	W	0	Logical and of corresponding request and mask bits.
1	NOT_FULL	R	W	0	Logical and of corresponding request and mask bits.
4	EMPTY	R	W	0	Logical and of corresponding request and mask bits.
5	OVERFLOW	R	W	0	Logical and of corresponding request and mask bits.
6	UNDERFLOW	R	W	0	Logical and of corresponding request and mask bits.
7	BLOCKED	R	W	0	Logical and of corresponding request and mask bits.
8	UART_NACK	R	W	0	Logical and of corresponding request and mask bits.
9	UART_DONE	R	W	0	Logical and of corresponding request and mask bits.
10	UART_ARB_LOST	R	W	0	Logical and of corresponding request and mask bits.

17.3.47 SCB_INTR_RX

Description: Receiver interrupt request register.
Address: 0x40240FC0
Offset: 0xFC0
Retention: Not Retained
IsDeepSleep: No
Comment: The register fields are not retained In DeepSleep power mode: HW clears the interrupt causes to '0', when coming out of DeepSleep power mode. In addition, HW clears the interrupt causes to '0', when the IP is disabled. As a result, the interrupt causes are only available in Active/Sleep power modes; they are generated by internally clocked logic (this logic operates on a clock that is only available in Active/Sleep power modes).
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	BLOCKED [7:7]	UNDERFLOW [6:6]	OVERFLOW [5:5]	None [4:4]	FULL [3:3]	NOT _EMPTY [2:2]	None [1:1]	TRIGGER [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:12]				BREAK _DETECT [11:11]	BAUD _DETECT [10:10]	PARITY _ERROR [9:9]	FRAME _ERROR [8:8]

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	TRIGGER	RW1C	RW1S	0	More entries in the RX FIFO than the value specified by TRIGGER_LEVEL in SCB_RX_FIFO_CTL. Only used in FIFO mode.
2	NOT_EMPTY	RW1C	RW1S	0	RX FIFO is not empty. Only used in FIFO mode.
3	FULL	RW1C	RW1S	0	RX FIFO is full. Note that received data frames are lost when the RX FIFO is full. Dependent on CTRL.BYTE_MODE: (FF_DATA_NR = EZ_DATA_NR/2) BYTE_MODE is '0': # entries == FF_DATA_NR/2. BYTE_MODE is '1': # entries == FF_DATA_NR. Only used in FIFO mode.
5	OVERFLOW	RW1C	RW1S	0	Attempt to write to a full RX FIFO. Note: in I2C mode, the OVERFLOW is set when a data frame is received and the RX FIFO is full, independent of whether it is ACK'd or NACK'd. Only used in FIFO mode.
6	UNDERFLOW	RW1C	RW1S	0	Attempt to read from an empty RX FIFO. Only used in FIFO mode.
7	BLOCKED	RW1C	RW1S	0	SW cannot get access to the EZ memory (EZ_DATA accesses), due to an externally clocked EZ access. This may happen when STATUS.EC_BUSY is '1'.

Bits	Name	SW	HW	Default or Enum	Description
8	FRAME_ERROR	RW1C	RW1S	0	Frame error in received data frame. Set to '1', when event is detected. Write with '1' to clear bit. This can be either a start or stop bit(s) error: Start bit error: after the detection of the beginning of a start bit period (RX line changes from '1' to '0'), the middle of the start bit period is sampled erroneously (RX line is '1'). Note: a start bit error is detected BEFORE a data frame is received. Stop bit error: the RX line is sampled as '0', but a '1' was expected. Note: a stop bit error may result in failure to receive successive data frame(s). Note: a stop bit error is detected AFTER a data frame is received. A stop bit error is detected after a data frame is received, and the UART_RX_CTL.DROP_ON_FRAME_ERROR field specifies whether the received frame is dropped or send to the RX FIFO. If UART_RX_CTL.DROP_ON_FRAME_ERROR is '1', the received data frame is dropped. If UART_RX_CTL.DROP_ON_FRAME_ERROR is '0', the received data frame is send to the RX FIFO. Note that Firmware can only identify the erroneous data frame in the RX FIFO if it is fast enough to read the data frame before the hardware writes a next data frame into the RX FIFO; i.e. the RX FIFO does not have error flags to tag erroneous data frames.
9	PARITY_ERROR	RW1C	RW1S	0	Parity error in received data frame. Set to '1', when event is detected. Write with '1' to clear bit. If UART_RX_CTL.DROP_ON_PARITY_ERROR is '1', the received frame is dropped. If UART_RX_CTL.DROP_ON_PARITY_ERROR is '0', the received frame is send to the RX FIFO. In SmartCard submode, negatively acknowledged data frames generate a parity error. Note that Firmware can only identify the erroneous data frame in the RX FIFO if it is fast enough to read the data frame before the hardware writes a next data frame into the RX FIFO.
10	BAUD_DETECT	RW1C	RW1S	0	LIN baudrate detection is completed. The receiver software uses the UART_RX_STATUS.BR_COUNTER value to set the right IP clock (from the programmable clock IP) to guarantee successful receipt of the first LIN data frame (Protected Identifier Field) after the synchronization byte. Set to '1', when event is detected. Write with '1' to clear bit.
11	BREAK_DETECT	RW1C	RW1S	0	Break detection is successful: the line is '0' for UART_RX_CTRL.BREAK_WIDTH + 1 bit period. Can occur at any time to address unanticipated break fields; i.e. 'break-in-data' is supported. This feature is supported for the UART standard and LIN submodes. For the UART standard submodes, ongoing receipt of data frames is NOT affected; i.e. Firmware is expected to take the proper action. For the LIN submode, possible ongoing receipt of a data frame is stopped and the (partially) received data frame is dropped and baud rate detection is started. Set to '1', when event is detected. Write with '1' to clear bit.

17.3.48 SCB_INTR_RX_SET

Description: Receiver interrupt set request register.
Address: 0x40240FC4
Offset: 0xFC4
Retention: Not Retained
IsDeepSleep: No
Comment: When read, this register reflects the interrupt request register.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	BLOCKED [7:7]	UNDERFLOW [6:6]	OVERFLOW [5:5]	None [4:4]	FULL [3:3]	NOT _EMPTY [2:2]	None [1:1]	TRIGGER [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:12]				BREAK _DETECT [11:11]	BAUD _DETECT [10:10]	PARITY _ERROR [9:9]	FRAME _ERROR [8:8]

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	TRIGGER	RW1S	A	0	Write with '1' to set corresponding bit in interrupt request register.
2	NOT_EMPTY	RW1S	A	0	Write with '1' to set corresponding bit in interrupt status register.
3	FULL	RW1S	A	0	Write with '1' to set corresponding bit in interrupt status register.
5	OVERFLOW	RW1S	A	0	Write with '1' to set corresponding bit in interrupt status register.
6	UNDERFLOW	RW1S	A	0	Write with '1' to set corresponding bit in interrupt status register.
7	BLOCKED	RW1S	A	0	Write with '1' to set corresponding bit in interrupt status register.
8	FRAME_ERROR	RW1S	A	0	Write with '1' to set corresponding bit in interrupt status register.
9	PARITY_ERROR	RW1S	A	0	Write with '1' to set corresponding bit in interrupt status register.
10	BAUD_DETECT	RW1S	A	0	Write with '1' to set corresponding bit in interrupt status register.
11	BREAK_DETECT	RW1S	A	0	Write with '1' to set corresponding bit in interrupt status register.

17.3.49 SCB_INTR_RX_MASK

Description: Receiver interrupt mask register.
Address: 0x40240FC8
Offset: 0xFC8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	BLOCKED [7:7]	UNDERFLOW [6:6]	OVERFLOW [5:5]	None [4:4]	FULL [3:3]	NOT _EMPTY [2:2]	None [1:1]	TRIGGER [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:12]				BREAK _DETECT [11:11]	BAUD _DETECT [10:10]	PARITY _ERROR [9:9]	FRAME _ERROR [8:8]

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	TRIGGER	RW	R	0	Mask bit for corresponding bit in interrupt request register.
2	NOT_EMPTY	RW	R	0	Mask bit for corresponding bit in interrupt request register.
3	FULL	RW	R	0	Mask bit for corresponding bit in interrupt request register.
5	OVERFLOW	RW	R	0	Mask bit for corresponding bit in interrupt request register.
6	UNDERFLOW	RW	R	0	Mask bit for corresponding bit in interrupt request register.
7	BLOCKED	RW	R	0	Mask bit for corresponding bit in interrupt request register.
8	FRAME_ERROR	RW	R	0	Mask bit for corresponding bit in interrupt request register.
9	PARITY_ERROR	RW	R	0	Mask bit for corresponding bit in interrupt request register.
10	BAUD_DETECT	RW	R	0	Mask bit for corresponding bit in interrupt request register.
11	BREAK_DETECT	RW	R	0	Mask bit for corresponding bit in interrupt request register.

17.3.50 SCB_INTR_RX_MASKED

Description: Receiver interrupt masked request register
Address: 0x40240FCC
Offset: 0xFCC
Retention: Not Retained
IsDeepSleep: No
Comment: When read, this register reflects a bitwise and between the interrupt request and mask registers. This register allows SW to read the status of all mask enabled interrupt causes with a single load operation, rather than two load operations: one for the interrupt causes and one for the masks. This simplifies Firmware development. The associated interrupt is active ('1'), when INTR_RX_MASKED != 0.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	BLOCKED [7:7]	UNDERFLOW [6:6]	OVERFLOW [5:5]	None [4:4]	FULL [3:3]	NOT _EMPTY [2:2]	None [1:1]	TRIGGER [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:12]				BREAK _DETECT [11:11]	BAUD _DETECT [10:10]	PARITY _ERROR [9:9]	FRAME _ERROR [8:8]

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	TRIGGER	R	W	0	Logical and of corresponding request and mask bits.
2	NOT_EMPTY	R	W	0	Logical and of corresponding request and mask bits.
3	FULL	R	W	0	Logical and of corresponding request and mask bits.
5	OVERFLOW	R	W	0	Logical and of corresponding request and mask bits.
6	UNDERFLOW	R	W	0	Logical and of corresponding request and mask bits.
7	BLOCKED	R	W	0	Logical and of corresponding request and mask bits.
8	FRAME_ERROR	R	W	0	Logical and of corresponding request and mask bits.
9	PARITY_ERROR	R	W	0	Logical and of corresponding request and mask bits.
10	BAUD_DETECT	R	W	0	Logical and of corresponding request and mask bits.
11	BREAK_DETECT	R	W	0	Logical and of corresponding request and mask bits.

18 SFLASH

Description Supervisory Flash Area (Cypress Trim & Wounding Info)
Base Address 0xFFFE000
Size 0x400
Slave Num MEMORYMAP

Register Name	Address	Permission	Description
SFLASH_SILICON_ID	0xFFFE000	FULL	Silicon ID
SFLASH_SWD_CONFIG	0xFFFE002	FULL	SWD pinout selector
SFLASH_DPSLP_KEY_DELAY	0xFFFE012	FULL	DeepSleep wakeup value for PWR_KEY_DELAY
SFLASH_SWD_LISTEN	0xFFFE014	FULL	Listen Window Length
SFLASH_FLASH_START	0xFFFE018	FULL	Flash Image Start Address
SFLASH_USER_SFLASH_AREA0	0xFFFE040	FULL	Pointer to between 0 and 2 customer usable SFLASH regions
SFLASH_USER_SFLASH_AREA1	0xFFFE044	FULL	Pointer to between 0 and 2 customer usable SFLASH regions
SFLASH_DIE_UNIQUE_ID0	0xFFFE050	FULL	Uses manufacturing identity to create a unique die ID
SFLASH_DIE_UNIQUE_ID1	0xFFFE054	FULL	Uses manufacturing identity to create a unique die ID
SFLASH_DIE_UNIQUE_ID2	0xFFFE058	FULL	Uses manufacturing identity to create a unique die ID
SFLASH_DIE_UNIQUE_ID3	0xFFFE05C	FULL	Uses manufacturing identity to create a unique die ID
SFLASH_DIE_UNIQUE_ID4	0xFFFE060	FULL	Uses manufacturing identity to create a unique die ID
SFLASH_DIE_UNIQUE_ID5	0xFFFE064	FULL	Uses manufacturing identity to create a unique die ID
SFLASH_IMO_TRIM_LT0	0xFFFE200	FULL	IMO Frequency Trim Register (SRSS-Lite) - From 24 to 48 MHz in steps of 4 MHz
SFLASH_IMO_TRIM_LT1	0xFFFE201	FULL	IMO Frequency Trim Register (SRSS-Lite) - From 24 to 48 MHz in steps of 4 MHz
SFLASH_IMO_TRIM_LT2	0xFFFE202	FULL	IMO Frequency Trim Register (SRSS-Lite) - From 24 to 48 MHz in steps of 4 MHz
SFLASH_IMO_TRIM_LT3	0xFFFE203	FULL	IMO Frequency Trim Register (SRSS-Lite) - From 24 to 48 MHz in steps of 4 MHz
SFLASH_IMO_TRIM_LT4	0xFFFE204	FULL	IMO Frequency Trim Register (SRSS-Lite) - From 24 to 48 MHz in steps of 4 MHz
SFLASH_IMO_TRIM_LT5	0xFFFE205	FULL	IMO Frequency Trim Register (SRSS-Lite) - From 24 to 48 MHz in steps of 4 MHz
SFLASH_IMO_TRIM_LT6	0xFFFE206	FULL	IMO Frequency Trim Register (SRSS-Lite) - From 24 to 48 MHz in steps of 4 MHz
SFLASH_IMO_TRIM_LT7	0xFFFE207	FULL	IMO Frequency Trim Register (SRSS-Lite) - From 24 to 48 MHz in steps of 4 MHz
SFLASH_IMO_TCTRIM_LT0	0xFFFE208	FULL	IMO Temperature Compensation Trim - From 24 to 48 MHz in steps of 4 MHz
SFLASH_IMO_TCTRIM_LT1	0xFFFE209	FULL	IMO Temperature Compensation Trim - From 24 to 48 MHz in steps of 4 MHz
SFLASH_IMO_TCTRIM_LT2	0xFFFE20A	FULL	IMO Temperature Compensation Trim - From 24 to 48 MHz in steps of 4 MHz
SFLASH_IMO_TCTRIM_LT3	0xFFFE20B	FULL	IMO Temperature Compensation Trim - From 24 to 48 MHz in steps of 4 MHz
SFLASH_IMO_TCTRIM_LT4	0xFFFE20C	FULL	IMO Temperature Compensation Trim - From 24 to 48 MHz in steps of 4 MHz
SFLASH_IMO_TCTRIM_LT5	0xFFFE20D	FULL	IMO Temperature Compensation Trim - From 24 to 48 MHz in steps of 4 MHz
SFLASH_IMO_TCTRIM_LT6	0xFFFE20E	FULL	IMO Temperature Compensation Trim - From 24 to 48 MHz in steps of 4 MHz
SFLASH_IMO_TCTRIM_LT7	0xFFFE20F	FULL	IMO Temperature Compensation Trim - From 24 to 48 MHz in steps of 4 MHz
SFLASH_IMO_STEPSIZE_LT0	0xFFFE210	FULL	IMO Stepsize Trim - From 24 to 48 MHz in steps of 4 MHz

Register Name	Address	Permission	Description
SFLASH_IMO_STEPSIZE_LT1	0xFFFE211	FULL	IMO Stepsize Trim - From 24 to 48 MHz in steps of 4 MHz
SFLASH_IMO_STEPSIZE_LT2	0xFFFE212	FULL	IMO Stepsize Trim - From 24 to 48 MHz in steps of 4 MHz
SFLASH_IMO_STEPSIZE_LT3	0xFFFE213	FULL	IMO Stepsize Trim - From 24 to 48 MHz in steps of 4 MHz
SFLASH_IMO_STEPSIZE_LT4	0xFFFE214	FULL	IMO Stepsize Trim - From 24 to 48 MHz in steps of 4 MHz
SFLASH_IMO_STEPSIZE_LT5	0xFFFE215	FULL	IMO Stepsize Trim - From 24 to 48 MHz in steps of 4 MHz
SFLASH_IMO_STEPSIZE_LT6	0xFFFE216	FULL	IMO Stepsize Trim - From 24 to 48 MHz in steps of 4 MHz
SFLASH_IMO_STEPSIZE_LT7	0xFFFE217	FULL	IMO Stepsize Trim - From 24 to 48 MHz in steps of 4 MHz
SFLASH_IMO_4PCT_LIM	0xFFFE218	FULL	IMO trim 4 percent deviation from nominal
SFLASH_IMO_3PCT_LIM	0xFFFE219	FULL	IMO trim 3 percent deviation from nominal
SFLASH_PILO_6PCT_LIM	0xFFFE21A	FULL	PILO trim 6 percent deviation from nominal
SFLASH_SAR_TEMP_MULTIPLIER	0xFFFE37C	FULL	SAR Temperature Sensor Multiplication Factor
SFLASH_SAR_TEMP_OFFSET	0xFFFE37E	FULL	SAR Temperature Sensor Offset

18.1 Register Details

18.1.1 SFLASH_SILICON_ID

Description: Silicon ID
Address: 0xFFFE000
Offset: 0x0
Retention: Retained
IsDeepSleep: No
Comment: Copied during Boot to CPUSS.SILICON_ID
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	SI_ID [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	SI_ID [15:8]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:15	SI_ID	RW	R	X	Silicon ID

18.1.2 SFLASH_SWD_CONFIG

Description: SWD pinout selector
Address: 0xFFFE002
Offset: 0x2
Retention: Retained
IsDeepSleep: No
Comment: Used in BootROM to determine primary or alternate SWD location.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:1]							SWD _SELECT [0:0]

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	SWD_SELECT	RW	R	X	0: Use Primary SWD location 1: Use Alternate SWD location (if defined)

18.1.3 SFLASH_DPSLP_KEY_DELAY

Description: DeepSleep wakeup value for PWR_KEY_DELAY
Address: 0xFFFE012
Offset: 0x12
Retention: Retained
IsDeepSleep: No
Comment: Used by firmware during exit from DeepSleep
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	WAKEUP_HOLDOFF [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	None [15:10]						WAKEUP_HOLDOFF [9:8]	

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:9	WAKEUP_HOLDOFF	RW	R	X	Delay (in 12MHz IMO clock cycles) to wait for references to settle on wakeup from DeepSleep. PBOD is ignored and system does not resume until this delay expires.

18.1.4 SFLASH_SWD_LISTEN

Description: Listen Window Length
Address: 0xFFFE014
Offset: 0x14
Retention: Retained
IsDeepSleep: No
Comment: Number of clock cycles to wait for SWD acquire to occur during boot.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	CYCLES [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	CYCLES [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	CYCLES [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	CYCLES [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	CYCLES	RW		X	Number of clock cycles

18.1.5 SFLASH_FLASH_START

Description: Flash Image Start Address
Address: 0xFFFE018
Offset: 0x18
Retention: Retained
IsDeepSleep: No
Comment: Flash Image start address. If this field is FFFF_FFFF (recommended) the firmware start address is loaded from vector table locations 0,1 (0000_0000 - 0000_0007). If this field is not FFFF_FFFF it is assumed to be a valid firmware start address.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	ADDRESS [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	ADDRESS [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	ADDRESS [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	ADDRESS [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	ADDRESS	RW		X	Start Address

18.1.6 SFLASH_USER_SFLASH_AREA

Description: Pointer to between 0 and 2 customer usable SFLASH regions
Address: 0xFFFE040
Offset: 0x40
Retention: Retained
IsDeepSleep: No
Comment: The SIZE field indicates whether each area is available
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	LOCATION [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	LOCATION [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	SIZE [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	SIZE [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:15	LOCATION	RW		X	Specifies the lower 16 bits of the absolute address pointer to the start of a user available SFLASH. The upper bits of the pointer are hardcoded as '0x0FFF'.
16:31	SIZE	RW		X	Specifies the size in bytes of the user area. A size of zero indicates that this area is not valid.

18.1.7 SFLASH_DIE_UNIQUE_ID

Description: Uses manufacturing identity to create a unique die ID
Address: 0xFFFE050
Offset: 0x50
Retention: Retained
IsDeepSleep: No
Comment: Manufacturing Data used to form Unique DieID.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	ID [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	ID [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	ID	RW		X	ID Data composed of manufacturing data. Includes manufacturing date (day, month, and year), die identity (fabrication lot, wafer number, x & y coordinates), minor revision number, and test details. The first 64 bits cannot repeat more than once per 10 years The first 96 bits are guaranteed never to repeat Up to 192 bits can be used

18.1.8 SFLASH_IMO_TRIM_LT

Description: IMO Frequency Trim Register (SRSS-Lite) - From 24 to 48 MHz in steps of 4 MHz
Address: 0xFFFE200
Offset: 0x200
Retention: Retained
IsDeepSleep: No
Comment: CLK_IMO_TRIM1 for each frequency 24..48MHz step 4MHz, plus one special frequency
IMO_TRIM_LT[0]: 24 MHz
IMO_TRIM_LT[1]: 28 MHz
IMO_TRIM_LT[2]: 32 MHz
IMO_TRIM_LT[3]: 36 MHz
IMO_TRIM_LT[4]: 40 MHz
IMO_TRIM_LT[5]: 44 MHz
IMO_TRIM_LT[6]: 48 MHz
IMO_TRIM_LT[7]: Special frequency if defined in the architecture TRM
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	OFFSET [7:0]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:7	OFFSET	RW		X	Frequency trim bits. These bits are determined at manufacturing time for each frequency setting.

18.1.9 SFLASH_IMO_TCTRIM_LT

Description: IMO Temperature Compensation Trim - From 24 to 48 MHz in steps of 4 MHz
Address: 0xFFFE208
Offset: 0x208
Retention: Retained
IsDeepSleep: No
Comment: CLK_IMO_TRIM2 for each frequency 24..48MHz step 4MHz, plus one special frequency
IMO_TCTRIM_LT[0]: 24 MHz
IMO_TCTRIM_LT[1]: 28 MHz
IMO_TCTRIM_LT[2]: 32 MHz
IMO_TCTRIM_LT[3]: 36 MHz
IMO_TCTRIM_LT[4]: 40 MHz
IMO_TCTRIM_LT[5]: 44 MHz
IMO_TCTRIM_LT[6]: 48 MHz
IMO_TCTRIM_LT[7]: Special frequency if defined in the architecture TRM
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	TCTRIM [7:4]				None [3:3]	FSOFFSET [2:0]		

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:2	FSOFFSET	RW		X	Frequency trim bits. These bits are determined at manufacturing time for each frequency setting.
4:7	TCTRIM	RW		X	IMO temperature compensation trim. These bits are determined at manufacturing time for each frequency setting.

18.1.10 SFLASH_IMO_STEPSIZE_LT

Description: IMO Stepsize Trim - From 24 to 48 MHz in steps of 4 MHz
Address: 0xFFFE210
Offset: 0x210
Retention: Retained
IsDeepSleep: No
Comment: CLK_IMO_TRIM3 for each frequency 24..48MHz step 4MHz, plus one special frequency
IMO_STEPSIZE_LT[0]: 24 MHz
IMO_STEPSIZE_LT[1]: 28 MHz
IMO_STEPSIZE_LT[2]: 32 MHz
IMO_STEPSIZE_LT[3]: 36 MHz
IMO_STEPSIZE_LT[4]: 40 MHz
IMO_STEPSIZE_LT[5]: 44 MHz
IMO_STEPSIZE_LT[6]: 48 MHz
IMO_STEPSIZE_LT[7]: Special frequency if defined in the architecture TRM
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:5]			STEPSIZE [4:0]				

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:4	STEPSIZE	RW		X	IMO trim stepsize bits. These bits are determined at manufacturing time for each frequency setting.

18.1.11 SFLASH_IMO_4PCT_LIM

Description: IMO trim 4 percent deviation from nominal
Address: 0xFFFE218
Offset: 0x218
Retention: Retained
IsDeepSleep: No
Comment: For parts with HPOSC, and applications which use HPOSC to provide run-time calibration of the IMO frequency.

This register provides a limit for the deviation (either positive or negative) from the nominal IMO trim expressed as an 11 bit value (OFFSET|FSOFFSET). Trims beyond this limit indicate that the IMO has been shifted more than 4 percent from nominal frequency. The 4 percent limit should be applied when conditions support a 3 percent IMO accuracy. 1 percent HPOSC accuracy + 3 percent IMO accuracy means that a > 4 percent deviation is likely caused by a hardware failure in HPOSC, IMO, and/or calibration counters.

This limit only applies when SRSS_CLK_IMO_SELECT.FREQ is set to 48_MHZ.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	TRIM_LIMIT [7:0]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:7	TRIM_LIMIT	RW		X	TRIM_LIMIT expressed as a positive integer. This value should be added to and subtracted from the nominal IMO trim to create upper/lower limits.

18.1.12 SFLASH_IMO_3PCT_LIM

Description: IMO trim 3 percent deviation from nominal
Address: 0xFFFE219
Offset: 0x219
Retention: Retained
IsDeepSleep: No
Comment: For parts with HPOSC, and applications which use HPOSC to provide run-time calibration of the IMO frequency.

This register provides a limit for the deviation (either positive or negative) from the nominal IMO trim expressed as an 11 bit value (OFFSET|FSOFFSET). Trims beyond this limit indicate that the IMO has been shifted more than 3 percent from nominal frequency. The 3 percent limit should be applied when conditions support a 2 percent IMO accuracy. 1 percent HPOSC accuracy + 2 percent IMO accuracy means that a > 3 percent deviation is likely caused by a hardware failure in HPOSC, IMO, and/or calibration counters.

This limit only applies when SRSS_CLK_IMO_SELECT.FREQ is set to 48_MHZ.

Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	TRIM_LIMIT [7:0]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:7	TRIM_LIMIT	RW		X	TRIM_LIMIT expressed as a positive integer. This value should be added to and subtracted from the nominal IMO trim

18.1.13 SFLASH_PILO_6PCT_LIM

Description: PILO trim 6 percent deviation from nominal
Address: 0xFFFE21A
Offset: 0x21A
Retention: Retained
IsDeepSleep: No
Comment: For parts with HPOSC, and applications which use HPOSC to provide run-time calibration of the PILO frequency.

This register provides a limit for the deviation (either positive or negative) from the nominal PILO trim expressed as an 8 bit value (TR_CAP). Trims beyond this limit indicate that the PILO has been shifted more than 6 percent from nominal frequency. As 1 percent HPOSC accuracy + 5 percent PILO accuracy means that a > 6 percent deviation is likely caused by a hardware failure in HPOSC, PILO, and/or calibration counters.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	TRIM_LIMIT [7:0]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:7	TRIM_LIMIT	RW		X	TRIM_LIMIT expressed as a positive integer. This value should be added to and subtracted from the nominal PILO trim

18.1.14 SFLASH_SAR_TEMP_MULTIPLIER

Description: SAR Temperature Sensor Multiplication Factor
Address: 0xFFFE37C
Offset: 0x37C
Retention: Retained
IsDeepSleep: No
Comment: This field intended for use in firmware and is not used by the BootROM boot process.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	TEMP_MULTIPLIER [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	TEMP_MULTIPLIER [15:8]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:15	TEMP_MULTIPLIER	RW		X	Multiplier value for SAR temperature sensor in fixed point 0.16 format. Note: this field exists in products that contain SAR (m0s8sar) only.

18.1.15 SFLASH_SAR_TEMP_OFFSET

Description: SAR Temperature Sensor Offset
Address: 0xFFFE37E
Offset: 0x37E
Retention: Retained
IsDeepSleep: No
Comment: This field intended for use in firmware and is not used by the BootROM boot process.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	TEMP_OFFSET [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	TEMP_OFFSET [15:8]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:15	TEMP_OFFSET	RW		X	Offset value for SAR temperature sensor in fixed point 10.6 format. Note: this field exists in products that contain SAR (m0s8sar) only.

19 SPCIF

Description Flash Control Interface
Base Address 0x40110000
Size 0x10000
Slave Num CPUMEMSSV3_VER3

Register Name	Address	Permission	Description
SPCIF_GEOMETRY	0x40110000	FULL	Flash/NVL geometry information Note:NVL is not available for this register
SPCIF_FLASH_LOCK	0x40110060	FULL	Flash Lock Register
SPCIF_FLASH_MACRO_WE	0x40110064	FULL	Flash Macro Write Enable
SPCIF_INTR	0x401107F0	FULL	SPCIF interrupt request register
SPCIF_INTR_SET	0x401107F4	FULL	SPCIF interrupt set request register
SPCIF_INTR_MASK	0x401107F8	FULL	SPCIF interrupt mask register
SPCIF_INTR_MASKED	0x401107FC	FULL	SPCIF interrupt masked request register

19.1 Register Details

19.1.1 SPCIF_GEOMETRY

Description: Flash/NVL geometry information
Address: 0x40110000
Offset: 0x0
Retention: Retained
IsDeepSleep: No
Comment: This register indicates the flash/NVLatch geometry parameters for the current device. This does not take wounding into account, which may restrict access to flash memory. Note that the default values of the read-only fields are determined by the CPUSS design time configuration.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	FLASH [7:0]							

Bits	15	14	13	12	11	10	9	8
Name			FLASH [13:8]					

Bits	23	22	21	20	19	18	17	16
Name	FLASH_ROW [23:22]		NUM_FLASH [21:20]		SFLASH [19:16]			

Bits	31	30	29	28	27	26	25	24
Name	DE_CPD _LP [31:31]	None [30:24]						

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:13	FLASH	R	W	Undefined	Regular flash capacity in 256 Byte multiples (chip dependent). If multiple flash macros are present, this field provides the flash capacity of all flash macros together: '0': 256 Bytes. '1': 2*256 Bytes. ... '16383': 16384*256 Bytes.
14:19	SFLASH	R	W	Undefined	Supervisory flash capacity in 256 Byte multiples (chip dependent). If multiple flash macros are present, this field provides the supervisory flash capacity of all flash macros together: '0': 256 Bytes. '1': 2*256 Bytes. ... '63': 64*256 Bytes.
20:21	NUM_FLASH	R	W	Undefined	Number of flash macros (chip dependent): '0': 1 flash macro '1': 2 flash macros '2': 3 flash macros '3': 4 flash macros

Bits	Name	SW	HW	Default or Enum	Description
22:23	FLASH_ROW	R	W	Undefined	Page size in 64 Byte multiples (chip dependent): '0': 64 byte '1': 128 byte '2': 192 byte '3': 256 byte The page size is used to determine the number of Bytes in a page for Flash page based operations (e.g. PGM_PAGE). Note: the field name FLASH_ROW is misleading, as this field specifies the number of Bytes in a page, rather than the number of Bytes in a row. In a single plane flash macro architecture, a page consists of a single row. However, in a multi plane flash macro architecture, a page consists of multiple rows from different planes.
31	DE_CPD_LP	RW		0	0': SRAM busy wait loop has not been copied. '1': Busy wait loop has been written into SRAM.

19.1.2 SPCIF_FLASH_LOCK

Description: Flash Lock Register
Address: 0x40110060
Offset: 0x60
Retention: Retained
IsDeepSleep: No
Comment: Locks Macro Write enables when key is written to register.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	KEY [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	KEY [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	KEY [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	KEY [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	KEY	W	R	0	Write Only register that locks/unlocks access to the FLASH MACRO_WE register by writing a key value to the register. The Key is the 32 bit value '0xF56B3A81'. When this specific bit pattern is written to the register, write access to FLASH_MACRO_WE is toggled between locked and unlocked. The bit FLASH_MACRO_WE.LOCKED toggles upon receipt of the required key value.

19.1.3 SPCIF_FLASH_MACRO_WE

Description: Flash Macro Write Enable
Address: 0x40110064
Offset: 0x64
Retention: Retained
IsDeepSleep: No
Comment: Locks Macro Write enables when key is written to register.
Default: 0xF

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:1]							MAC_WRITE_EN [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	LOCKED [31:31]	None [30:24]						

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	MAC_WRITE_EN	RW	A	1	Access control to Flash Macros Write Access. This is a bit mask where each bit controls Program/Erase Access to the corresponding Macro. When the bit is set to '1' then the Macro may be programmed/erased, when the bit is set to '0', the Macro content is locked. The content of this register may only be changed when FLASH_MACRO_WE.LOCKED is '0'.
31	LOCKED	R	W	0	When set indicates that write access to FLASH_MACRO_WE.MAC_WRITE_EN is blocked. The value of this bit toggles when the key value is written into FLASH_LOCK.KEY.

19.1.4 SPCIF_INTR

Description: SPCIF interrupt request register
Address: 0x401107F0
Offset: 0x7F0
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:1]							TIMER [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	TIMER	RW1C	RW1S	0	Timer counter value reaches '0'. Set to '1', when event is detected. Write INTR field with '1', to clear bit. Write INTR_SET field with '1', to set bit.

19.1.5 SPCIF_INTR_SET

Description: SPCIF interrupt set request register
Address: 0x401107F4
Offset: 0x7F4
Retention: Not Retained
IsDeepSleep: No
Comment: When read, this register reflects the interrupt request register.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:1]							TIMER [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	TIMER	RW1S	A	0	Write INTR_SET field with '1' to set corresponding INTR field.

19.1.6 SPCIF_INTR_MASK

Description: SPCIF interrupt mask register
Address: 0x401107F8
Offset: 0x7F8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:1]							TIMER [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	TIMER	RW	R	0	Mask for corresponding field in INTR register.

19.1.7 SPCIF_INTR_MASKED

Description: SPCIF interrupt masked request register
Address: 0x401107FC
Offset: 0x7FC
Retention: Not Retained
IsDeepSleep: No
Comment: When read, this register reflects a bitwise and between the interrupt request and mask registers.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:1]							TIMER [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	TIMER	R	W	0	Logical and of corresponding request and mask fields.

20 SRSSHV

Description System Resources High Voltage Subsystem
Base Address 0x40030000
Size 0x10000
Slave Num MMIO0

Register Name	Address	Permission	Description
PWR_CONTROL	0x40030000	FULL	Power Mode Control (Lock Protected)
PWR_KEY_DELAY	0x40030004	FULL	Power System Key&Delay Register (Lock Protected)
TST_MODE	0x40030014	FULL	Test Mode Control Register
CLK_CAL_CNT1	0x4003001C	FULL	Clock Calibration Counter 1
CLK_CAL_CNT2	0x40030020	FULL	Clock Calibration Counter 2
CLK_SELECT	0x40030028	FULL	Clock Select Register (Lock Protected)
CLK_ILO_CONFIG	0x4003002C	FULL	ILO Configuration (Lock Protected)
CLK_IMO_CONFIG	0x40030030	FULL	IMO Configuration (Lock Protected)
CLK_DFT_SELECT	0x40030034	FULL	Clock DFT Mode Selection Register
SRSS_MASKED	0x40030040	FULL	SRSS Interrupt Masked Register
SRSS_INTR	0x40030044	FULL	SRSS Interrupt Register
SRSS_INTR_SET	0x40030048	FULL	SRSS Interrupt Set Register
SRSS_INTR_MASK	0x4003004C	FULL	SRSS Interrupt Mask Register
RES_CAUSE	0x40030054	FULL	Reset Cause Observation Register
REG_PROT	0x40030080	FULL	Register Protection
CRWDT_CTL	0x40030090	FULL	Challenge Response WatchDog Control (Lock Protected)
CRWDT_CHALLENGE	0x40030094	FULL	Challenge Response WatchDog Challenge Value
CRWDT_RESPONSE	0x40030098	FULL	Challenge Response WatchDog Response Value
CRWDT_UPCNT	0x4003009C	FULL	Challenge Response WatchDog Up Counter
CRWDT_EARLY	0x400300A0	FULL	Challenge Response WatchDog Early Limit (Lock Protected)
CRWDT_WARN	0x400300A4	FULL	Challenge Response WatchDog Warning Limit (Lock Protected)
CRWDT_LATE	0x400300A8	FULL	Challenge Response WatchDog Late Limit (Lock Protected)
CRWDT_CONFIG	0x400300AC	FULL	Challenge Response WatchDog Configuration
LIFETIME_CTL	0x400300B0	FULL	Liftetime Counter Control (Lock Protected)
LIFETIME_WAKEUP	0x400300B4	FULL	Lifetime Wakeup Value
LIFETIME_COUNTER	0x400300B8	FULL	Lifetime Counter Current Value
PWR_SSV_CTL	0x400300E0	FULL	Supply Supervisory Control Register (Lock Protected)
PWR_SSV_STATUS	0x400300E4	FULL	Supply Supervision Status Register
HPOSC_CTL	0x40030300	FULL	High Precision Oscillator Control (Lock Protected)
PILO_CTL	0x40030400	FULL	Precision Low Power Oscillator Control (Lock Protected)
PWR_BG_TRIM1	0x4003FF00	FULL	Bandgap Trim Register (Lock Protected)
PWR_BG_TRIM2	0x4003FF04	FULL	Bandgap Trim Register (Lock Protected)
CLK_IMO_SELECT	0x4003FF08	FULL	IMO Frequency Select Register (Lock Protected)
CLK_IMO_TRIM1	0x4003FF0C	FULL	IMO Trim Register (Lock Protected)
CLK_IMO_TRIM2	0x4003FF10	FULL	IMO Trim Register (Lock Protected)
CLK_IMO_TRIM3	0x4003FF14	FULL	IMO Trim Register (Lock Protected)
PWR_PWRSYS_TRIM1	0x4003FF18	FULL	Power System Trim Register (Lock Protected)
TRIM_BODVCCD	0x4003FF1C	FULL	Brown Out Detect Trim (VCCD) (Lock Protected)
TRIM_OVDVCCD	0x4003FF20	FULL	Over Voltage Detect Trim (VCCD) (Lock Protected)
TRIM_HPOSC0_CTL	0x4003FF24	FULL	High Precision Oscillator Trim Control 0 (Lock Protected)
TRIM_HPOSC1_CTL	0x4003FF28	FULL	High Precision Oscillator Trim Control 1 (Lock Protected)
TRIM_HPOSC2_CTL	0x4003FF2C	FULL	High Precision Oscillator Trim Control 2 (Lock Protected)
TRIM_HPOSC3_CTL	0x4003FF30	FULL	High Precision Oscillator Trim Control 3 (Lock Protected)

Register Name	Address	Permission	Description
TRIM_HPOSC4_CTL	0x4003FF34	FULL	High Precision Oscillator Trim Control 4 (Lock Protected)
TRIM_PILO0_CTL	0x4003FF38	FULL	Low Frequency Oscillator Trim Control 0 (Lock Protected)
TRIM_PILO1_CTL	0x4003FF3C	FULL	Low Frequency Oscillator Trim Control 1 (Lock Protected)
TRIM_PILO2_CTL	0x4003FF40	FULL	Low Frequency Oscillator Trim Control 2 (Lock Protected)
TRIM_PILO3_CTL	0x4003FF44	FULL	Low Frequency Oscillator Trim Control 3 (Lock Protected)
TRIM_PILO4_CTL	0x4003FF48	FULL	Low Frequency Oscillator Trim Control 4 (Lock Protected)
TRIM_PILO5_CTL	0x4003FF4C	FULL	Low Frequency Oscillator Trim Control 5 (Lock Protected)
TRIM_BODVDDD	0x4003FF50	FULL	Brown Out Detect Trim (VDDD) (Lock Protected)
TRIM_OVDVDDD	0x4003FF54	FULL	Over Voltage Detect Trim (VDDD) (Lock Protected)

20.1 WDT

Register Name	Address	Permission	Description
WDT_CTL	0x40030100	FULL	WDT Control Register
WDT_LOWER_LIMIT	0x40030104	FULL	WDT Lower Limit Register
WDT_UPPER_LIMIT	0x40030108	FULL	WDT Upper Limit Register
WDT_WARN_LIMIT	0x4003010C	FULL	WDT Warn Limit Register
WDT_CONFIG	0x40030110	FULL	WDT Configuration Register
WDT_CNT	0x40030114	FULL	WDT Count Register
WDT_LOCK	0x40030140	FULL	WDT Lock register
WDT_SERVICE	0x40030144	FULL	WDT Service register
WDT_INTR	0x40030150	FULL	WDT Interrupt Register
WDT_INTR_SET	0x40030154	FULL	WDT Interrupt Set Register
WDT_INTR_MASK	0x40030158	FULL	WDT Interrupt Mask Register
WDT_INTR_MASKED	0x4003015C	FULL	WDT Interrupt Masked Register

20.2 Register Details

20.2.1 PWR_CONTROL

Description: Power Mode Control (Lock Protected)
Address: 0x40030000
Offset: 0x0
Retention: Retained
IsDeepSleep: No
Comment: Controls the device power mode options and allows observation of current state.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:6]		LPM _READY [5:5]	DEBUG _SESSION [4:4]	POWER_MODE [3:0]			

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	EXT_VCCD [23:23]	None [22:20]			SPARE [19:18]		OVER _TEMP _THRESH [17:17]	OVER _TEMP_EN [16:16]

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:3	POWER_MODE	R	RW	0	Current power mode of the device. Note that this field cannot be read in all power modes on actual silicon.
	RESET			0	RESET state
	ACTIVE			1	ACTIVE state
	SLEEP			2	SLEEP state
	DEEP_SLEEP			3	DEEP_SLEEP state
4	DEBUG_SESSION	R	RW	0	Indicates whether a debug session is active (CDBGPWRUPREQ signal is 1)
	NO_SESSION			0	No debug session active
	SESSION_ACTIVE			1	Debug session is active
5	LPM_READY	R	RW	0	Indicates whether the low power mode regulator is ready to enter DeepSleep mode. 0: If DeepSleep mode is requested, device will enter SLEEP mode. When low power regulators are ready, device will automatically enter the originally requested mode. 1: Normal operation. DeepSleep works as described.
16	OVER_TEMP_EN	RW	R	0	Enables the die over temperature sensor. Must be enabled when using the TEMP_HIGH interrupt.
17	OVER_TEMP_THRESH	RW	R	0	Over-temperature threshold. 0: TEMP_HIGH condition occurs between 120C and 125C. 1: TEMP_HIGH condition occurs between 60C and 75C (used for testing).
18:19	SPARE	R	RW	0	Spare AHB readback bits that are hooked to PWR_PWRSYS_TRIM1.SPARE_TRIM[1:0] through spare logic equivalent to bitwise inversion. Engineering only, should always be set to default.

Bits	Name	SW	HW	Default or Enum	Description
23	EXT_VCCD	RW	A	0	Always write 0 except as noted below. PSoC4-S0 and Streetfighter CapSense products may set this bit if Vccd is provided externally (on Vccd pin). Setting this bit turns off the active regulator and will lead to system reset (BOD) unless both Vddd and Vccd pins are supplied externally. This register field reset with hard reset (power related, XRES, WDT).

20.2.2 PWR_KEY_DELAY

Description: Power System Key&Delay Register (Lock Protected)
Address: 0x40030004
Offset: 0x4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xF8

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	WAKEUP_HOLDOFF [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	None [15:10]						WAKEUP_HOLDOFF [9:8]	

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:9	WAKEUP_HOLDOFF	RW	R	248	Delay to wait for references to settle on wakeup from DeepSleep. BOD is ignored and system does not resume until this delay expires. Note that the same delay on POR is hard-coded. The default assumes the output of the predivider is 48MHz + 3 percent. Firmware may scale this setting according to the fastest actual clock frequency that can occur when waking from DeepSleep.

20.2.3 TST_MODE

Description: Test Mode Control Register
Address: 0x40030014
Offset: 0x14
Retention: Retained
IsDeepSleep: Yes
Comment: Controls primary test mode. This is a single bit that can be written directly from the ATE/Programmer in any protection mode. It's main function is to signal to the Boot ROM that normal firmware execution is not to commence after boot is complete. Instead the Boot ROM will enter a wait loop for system commands.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:3]					SWD_CONNECTED [2:2]	None [1:0]	

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	TEST_MODE [31:31]	TEST_KEY_DFT_EN [30:30]	None [29:29]	BLOCK_ALT_XRES [28:28]	None [27:24]			

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
2	SWD_CONNECTED	R	RW	0	0: SWD not active 1: SWD activated (Line Reset & Connect sequence passed) (Note: this bit replaces TST_CTRL.SWD_CONNECTED and is present in all M0S8 products except TSG4)
28	BLOCK_ALT_XRES	RW	A	0	Relevant only for parts that have the alternate XRES mechanism of overloading a GPIO pin temporarily as alternate XRES during test. When set, this bit blocks the alternate XRES function, such that the pin can be used for normal I/O or for ddft/adft observation. This register field resets with hard reset (power related, XRES, WDT)
30	TEST_KEY_DFT_EN	R	RW	0	This bit is set when a XRES test mode key is shifted in. It is the value of the test_key_dft_en signal. When this bit is set, the BootROM will not yield execution to the FLASH image (same function as setting TEST_MODE bit below).
31	TEST_MODE	RW	R	0	0: Normal operation mode 1: Test mode (any test mode) Setting this bit will prevent BootROM from yielding execution to Flash image.

20.2.4 CLK_CAL_CNT1

Description: Clock Calibration Counter 1
Address: 0x4003001C
Offset: 0x1C
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: 0x80000000

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	CAL_COUNTER1 [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	CAL_COUNTER1 [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	CAL_COUNTER_DONE [31:31]	None [30:24]						

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:15	CAL_COUNTER1	RW	A	0	Down-counter clocked on DFT output #0 (see CLK_DFT_SELECT). This register always reads as zero. Counting starts internally when this register is written with a nonzero value. CAL_COUNTER_DONE goes immediately low to indicate that the counter has started and will be asserted when the counters are done. Do not write this field unless CAL_COUNTER_DONE==1. Both clocks must be running or the measurement will not complete. A stalled counter can be recovered by selecting valid clocks, waiting until the measurement completes, and discarding the first result. CAL_COUNTER1 should always be > 1. Due to internal clock synchronization CAL_COUNTER1 should be at least 5 times the 1/F_cnt2.
31	CAL_COUNTER_DONE	R	W	1	Status bit indicating that the internal counter #1 is finished counting and CLK_CAL_CNT2.COUNTER stopped counting up

20.2.5 CLK_CAL_CNT2

Description: Clock Calibration Counter 2
Address: 0x40030020
Offset: 0x20
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	CAL_COUNTER2 [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	CAL_COUNTER2 [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:15	CAL_COUNTER2	R	RW	0	Up-counter clocked on DFT output #1 (see CLK_DFT_SELECT). When CLK_CAL_CNT1.CAL_COUNTER_DONE==1, the counter is stopped and can be read by SW. Do not read this value unless CAL_COUNTER_DONE==1. The expected final value is related to the ratio of clock frequencies used for the two counters and the value loaded into counter 1: CLK_CAL_CNT2.CAL_COUNTER2=(F_cnt2/F_cnt1)*(CLK_CAL_CNT1.CAL_COUNTER1)

20.2.6 CLK_SELECT

Description: Clock Select Register (Lock Protected)
Address: 0x40030028
Offset: 0x28
Retention: Retained
IsDeepSleep: No
Comment: Configures direction of all clock multiplexers and selectors. See clock startup times for clock sources for wait periods before switching to them. Selecting a clock source that is not supported/not enabled will result in undefined behavior. It takes about 3 cycles of the new selected clock to switch away from the old clock to the new clock. Do not disable the original clock during this time.
Default: 0x8

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	SYSCLK_DIV [7:6]		PUMP_SEL [5:4]		HFCLK_DIV [3:2]		HFCLK_SEL [1:0]	

Bits	15	14	13	12	11	10	9	8
Name	None [15:9]							LFCLK _SEL [8:8]

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:1	HFCLK_SEL	RW	R	0	Selects a source for clk_hf and dsi_in[0]. Note that not all products support all clock sources. Selecting a clock source that is not supported or enabled will result in undefined behavior. It takes about 3 cycles of the new selected clock to switch away from the old clock to the new clock. Do not disable the original clock during this time.
	IMO			0	IMO - Internal R/C Oscillator
	EXTCLK			1	EXTCLK - External Clock Pin
	ECO			2	ECO - External-Crystal Oscillator or PLL subsystem output
	HPOSC			3	HPOSC - High Precision Oscillator. Only if HPOSC_PRESENT=1
2:3	HFCLK_DIV	RW	R	2	Selects clk_hf predivider value. It will take 3-4 clock cycles to switch to the new predivder value
	NO_DIV			0	Transparent mode, feed through selected clock source w/o dividing.
	DIV_BY_2			1	Divide selected clock source by 2
	DIV_BY_4			2	Divide selected clock source by 4
	DIV_BY_8			3	Divide selected clock source by 8
4:5	PUMP_SEL	RW	R	0	Selects clock source for charge pump clock. This clock is not guaranteed to be glitch free when changing any of its sources or settings.
	GND			0	No clock, connect to gnd
	IMO			1	Use main IMO output
	HFCLK			2	Use clk_hf (using selected source after predivider but before prescaler)
6:7	SYSCLK_DIV	RW	R	0	Select clk_sys prescaler value.

Bits	Name	SW	HW	Default or Enum	Description
	NO_DIV			0	clk_sys= clk_hf/1
	DIV_BY_2			1	clk_sys= clk_hf/2
	DIV_BY_4			2	clk_sys= clk_hf/4
	DIV_BY_8			3	clk_sys= clk_hf/8
8	LFCLK_SEL	RW	A	0	Low Frequency Clock Select. Selecting a clock source that is not enabled will result in undefined behavior. If a clock source is disabled while selected, then the clock merely stops to all sources that receive it. In such a scenario, the disabled clock must be re-enabled, prior to switching FROM this clock source. Writes to this field are ignored unless the WDT is unlocked using WDT_LOCK register. It takes about 3 cycles of the new selected clock to switch away from the old clock to the new clock. Do not disable the original clock during this time. This register field resets with hard reset (power related, XRES, WDT).
	ILO			0	ILO - Internal Low Frequency Oscillator
	PILO			1	PILO - Precision Internal Low Frequency Oscillator. Only if PILO_PRESENT=1

20.2.7 CLK_ILO_CONFIG

Description: ILO Configuration (Lock Protected)
Address: 0x4003002C
Offset: 0x2C
Retention: Retained
IsDeepSleep: No
Comment: Internal slow speed R/C oscillator (32kHz) configuration register.
Default: 0x80000000

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	ENABLE [31:31]	None [30:24]						

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
31	ENABLE	RW	A	1	Master enable for ILO oscillator. Clearing this bit will disable the ILO. Do not disable this clock if the CLK_LF uses it clock the source. Writes to this field are ignored when LFCLK_SEL is using this clock as the source and WDT is locked using WDT_LOCK register. This register resets when there is power related reset POR/XRES/BOD/OVD/WDT

20.2.8 CLK_IMO_CONFIG

Description: IMO Configuration (Lock Protected)
Address: 0x40030030
Offset: 0x30
Retention: Retained
IsDeepSleep: No
Comment: Internal high speed R/C oscillator configuration register. Note that this oscillator comes up active on power up. The oscillator provides the primary system clock (HFCLK) on power up until firmware configures differently. This oscillator is also used before system start to count out power up delays. This is done in fast IMO (FIMO) mode that does not require any external references and runs at a fixed 12MHz.
Default: 0x80000000

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	ENABLE [31:31]	None [30:24]						

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
31	ENABLE	RW	R	1	Master enable for IMO oscillator. Clearing this bit will disable the IMO. Don't do this if the system is running off it.

20.2.9 CLK_DFT_SELECT

Description: Clock DFT Mode Selection Register
Address: 0x40030034
Offset: 0x34
Retention: Retained
IsDeepSleep: No
Comment: Selects which clock sources to route to the Calibration Counters.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:7]	DFT_EDGE0 [6:6]	DFT_DIV0 [5:4]		DFT_SEL0 [3:0]			

Bits	15	14	13	12	11	10	9	8
Name	None [15:15]	DFT_EDGE1 [14:14]	DFT_DIV1 [13:12]		DFT_SEL1 [11:8]			

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:3	DFT_SEL0	RW	R	0	Select clock for Calibration Counter #1
	NC			0	Disabled - output is 0
	ILO			1	ILO output
	IMO			2	IMO output
	ECO			3	ECO output (if available)
	EXTCLK			4	External clock input
	HFCLK			5	Not appropriate for use with calibration counters
	LFCLK			6	Not appropriate for use with calibration counters
	SYSCLK			7	Not appropriate for use with calibration counters
	PUMPCLK			8	Not appropriate for use with calibration counters
	SLPCTRLCLK			9	Not appropriate for use with calibration counters
	HPOSC			10	HPOSC output. Applicable only if HPOSC_PRESENT=1
	PILO			11	PILO output. Applicable only if PILO_PRESENT=1
	ILO_EN			12	Not appropriate for use with calibration counters
	IMO_EN			13	Not appropriate for use with calibration counters
	HPOSC_EN			14	Not appropriate for use with calibration counters
	PILO_EN			15	Not appropriate for use with calibration counters
4:5	DFT_DIV0	RW	R	0	Calibration Counter #1 pre-divider
	NO_DIV			0	Direct Output
	DIV_BY_2			1	Divide by 2
	DIV_BY_4			2	Divide by 4
	DIV_BY_8			3	Divide by 8
6	DFT_EDGE0	RW	R	0	Edge sensitivity for pre-divider (only relevant when DIV0>0).
	POSEDGE			0	Use posedge for divider
	NEGEDGE			1	Use negedge for divider

Bits	Name	SW	HW	Default or Enum	Description
8:11	DFT_SEL1	RW	R	0	Select clock for Calibration Counter #2
	NC			0	Disabled - output is 0
	ILO			1	ILO output
	IMO			2	IMO output
	ECO			3	ECO output (if available)
	EXTCLK			4	External clock input
	HFCLK			5	Not appropriate for use with calibration counters
	LFCLK			6	Not appropriate for use with calibration counters
	SYSCLK			7	Not appropriate for use with calibration counters
	PUMPCLK			8	Not appropriate for use with calibration counters
	SLPCTRLCLK			9	Not appropriate for use with calibration counters
	HPOSC			10	HPOSC output. Applicable only if HPOSC_PRESENT=1
	PILO			11	PILO output. Applicable only if PILO_PRESENT=1
	ILO_EN			12	Not appropriate for use with calibration counters
	IMO_EN			13	Not appropriate for use with calibration counters
	HPOSC_EN			14	Not appropriate for use with calibration counters
	PILO_EN			15	Not appropriate for use with calibration counters
12:13	DFT_DIV1	RW	R	0	Calibration Counter #2 pre-divider
	NO_DIV			0	Direct Output
	DIV_BY_2			1	Divide by 2
	DIV_BY_4			2	Divide by 4
	DIV_BY_8			3	Divide by 8
14	DFT_EDGE1	RW	R	0	Edge sensitivity for pre-divider (only relevant when DIV0>0).
	POSEDGE			0	Use posedge for divider
	NEGEDGE			1	Use negedge for divider

20.2.10 SRSS_MASKED

Description: SRSS Interrupt Masked Register
Address: 0x40030040
Offset: 0x40
Retention: Retained
IsDeepSleep: No
Comment: Bitwise 'AND' between the interrupt request and mask registers so firmware can read the status of all mask enabled interrupt causes with a single load operation
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:5]			CRWDT [4:4]	CLK_CAL [3:3]	LIFETIME_ WAKEUP [2:2]	TEMP _HIGH [1:1]	None [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
1	TEMP_HIGH	R	RW	0	Logical and of corresponding request and mask bits.
2	LIFETIME_WAKEUP	R	RW	0	Logical and of corresponding request and mask bits.
3	CLK_CAL	R	RW	0	Logical and of corresponding request and mask bits.
4	CRWDT	R	RW	0	Logical and of corresponding request and mask bits.

20.2.11 SRSS_INTR

Description: SRSS Interrupt Register
Address: 0x40030044
Offset: 0x44
Retention: Retained
IsDeepSleep: No
Comment: Interrupt signals from SRSS
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:5]			CRWDT [4:4]	CLK_CAL [3:3]	LIFETIME_ WAKEUP [2:2]	TEMP _HIGH [1:1]	None [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
1	TEMP_HIGH	RW1C	A	0	Regulator over-temp interrupt. This interrupt can occur when a short circuit exists on the vccd pin or when extreme loads are applied on IO-cells causing the die to overheat. Firmware is encourage to shutdown all IO cells and then go to DeepSleep mode when this interrupt occurs if protection against such conditions is desired.
2	LIFETIME_WAKEUP	RW1C	A	0	Wakeup Interrupt from LIFETIME Counter. This bit is set when LIFETIME_COUNTER ==LIFETIME_WAKEUP. This is a DeepSleep Interrupt. The interrupt source will reset only with hard reset (power related, XRES, WDT).
3	CLK_CAL	RW1C	A	0	Clock calibration counter is done. This field is reset during DeepSleep mode.
4	CRWDT	RW1C	A	0	Interrupt from CRWDT. This bit is set by the CRWDT when enabled by CRWDT_CONFIG.

20.2.12 SRSS_INTR_SET

Description: SRSS Interrupt Set Register
Address: 0x40030048
Offset: 0x48
Retention: Retained
IsDeepSleep: No
Comment: Can be used to set interrupts for firmware testing.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:5]			CRWDT [4:4]	CLK_CAL [3:3]	LIFETIME_ WAKEUP [2:2]	TEMP _HIGH [1:1]	None [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
1	TEMP_HIGH	RW1S	A	0	Writing 1 to this bit internally sets the overtemp interrupt. This can be observed by reading SRSS_INTR.TEMP_HIGH. This bit always reads back as zero.
2	LIFETIME_WAKEUP	RW1S	A	0	Writing 1 to this bit internally sets the LIFETIME_WAKEUP interrupt. Reads back same as SRSS_INTR.LIFETIME_WAKEUP. The interrupt source will reset only with hard reset (power related, XRES, WDT).
3	CLK_CAL	RW1S	A	0	Set interrupt for clock calibration counter done. This field is reset during DeepSleep mode. Reads back same as SRSS_INTR.CLK_CAL.
4	CRWDT	RW1S	A	0	Set interrupt for Challenge/Response Interrupt. Reads back same as SRSS_INTR.CRWDT.

20.2.13 SRSS_INTR_MASK

Description: SRSS Interrupt Mask Register
Address: 0x4003004C
Offset: 0x4C
Retention: Retained
IsDeepSleep: No
Comment: Controls whether interrupt is forwarded to CPU.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:5]			CRWDT [4:4]	CLK_CAL [3:3]	LIFETIME_ WAKEUP [2:2]	TEMP _HIGH [1:1]	None [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
1	TEMP_HIGH	RW	R	0	Masks REG_OVERTEMP interrupt
2	LIFETIME_WAKEUP	RW	R	0	Mask for lifetime counter
3	CLK_CAL	RW	R	0	Mask for clock calibration done
4	CRWDT	RW	R	0	Mask for CRWDT interrupt

20.2.14 RES_CAUSE

Description: Reset Cause Observation Register
Address: 0x40030054
Offset: 0x54
Retention: Retained
IsDeepSleep: No
Comment: Indicates the cause for the latest reset(s) that occurred in the system. All bits in this register assert when the corresponding reset cause occurs and must be cleared by firmware. Low-voltage cause bits are reset whenever the low-voltage supply is initialized, including XRES, POR, brown-out, WDT.

High-voltage cause bit: caused by condition that could involve or imply loss of system state
- BOD/OVD because we are operating outside of the timing closure window
- WDT because the lack of servicing could imply a fundamental problem causing loss of state

Low-voltage cause bit: typically caused by soft errors
- CRWDT because processor might have lost state
- Fault, likely due to multiple bit ECC error
- Soft reset requested by the processor

Default: 0x40000000

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:5]			RESET_SOFT [4:4]	RESET_PROT_FAULT [3:3]	None [2:2]	RESET_ACT_FAULT [1:1]	RESET_WDT [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:10]						RESET_CRWDT [9:9]	None [8:8]

Bits	23	22	21	20	19	18	17	16
Name	None [23:23]	RESET_OVD VCCD [22:22]	None [21:21]	RESET_OVD VDDD [20:20]	RESET_BOD VCCD [19:19]	None [18:18]	RESET_BOD VDDD [17:17]	RESET_XRES [16:16]

Bits	31	30	29	28	27	26	25	24
Name	None [31:31]	RESET_POR VDDD [30:30]	None [29:25]					RESET_BODHVSS [24:24]

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	RESET_WDT	RW1C	A	0	A WatchDog Timer reset has occurred since last power cycle. This is a high-voltage cause detection, this bit blocks recording of other high-voltage cause bits, except RESET_PORVDDD and XRES. Hardware clears this bit during POR. This bit is not blocked by other HV cause bits.
1	RESET_ACT_FAULT	RW1C	A	0	Reset caused by the Fault Infrastructure. This is a low-voltage cause bit that hardware clears when the low-voltage supply is initialized (see comments above).

Bits	Name	SW	HW	Default or Enum	Description
3	RESET_PROT_FAULT	RW1C	A	0	A protection violation occurred that requires a RESET. This includes, but is not limited to, hitting a debug breakpoint while in Privileged Mode.
4	RESET_SOFT	RW1C	A	0	Cortex-M0 requested a system reset through it's SYSRESETREQ. This can be done via a debugger probe or in firmware.
9	RESET_CRWDT	RW1C	A	0	Challenge/Response Watchdog reset. This is a low-voltage cause bit that hardware clears when the low-voltage supply is initialized (see comments above).
16	RESET_XRES	RW1C	A	0	External XRES pin was asserted. This is a high-voltage cause bit that blocks recording of other high-voltage cause bits, except RESET_PORVDDD. Hardware clears this bit during POR. This bit is not blocked by other HV cause bits.
17	RESET_BODVDDD	RW1C	A	0	Internal VDDD supply crossed brown-out limit. Note that this cause will only be observable as long as the VDDD supply does not go below the POR (power on reset) detection limit. Below this limit it is not possible to reliably retain information in the device. This is a high-voltage cause bit that blocks recording of other high-voltage cause bits, except RESET_PORVDDD and RESET_XRES. Hardware clears this bit during POR.
19	RESET_BODVCCD	RW1C	A	0	Internal VCCD core supply crossed the brown-out limit. Note that this detector will detect gross issues with the internal core supply, but may not catch all brown-out conditions. Functional and timing supervision (CSV, WDT) is provided to create fully failsafe internal crash detection. This is a high-voltage cause bit that blocks recording of other high-voltage cause bits, except RESET_PORVDDD and RESET_XRES. Hardware clears this bit during POR.
20	RESET_OVDVDDD	RW1C	A	0	Overvoltage detection on the external VDDD supply. This is a high-voltage cause bit that blocks recording of other high-voltage cause bits, except RESET_PORVDDD and RESET_XRES. Hardware clears this bit during POR.
22	RESET_OVDVCCD	RW1C	A	0	Overvoltage detection on the internal core VCCD supply. This is a high-voltage cause bit that blocks recording of other high-voltage cause bits, except RESET_PORVDDD and RESET_XRES. Hardware clears this bit during POR.
24	RESET_BODHVSS	RW1C	A	0	Internal VDDD supply crossed brown-out limit. Note that this cause will only be observable as long as the VDDD supply does not go below the POR (power on reset) detection limit. Below this limit it is not possible to reliably retain information in the device. This is a high-voltage cause bit that blocks recording of other high-voltage cause bits, except RESET_PORVDDD and RESET_XRES. Hardware clears this bit during POR. This detector is a backup detector in the high voltage sub-system that is on even in deep sleep. This detector is used for engineering debug purposes only.
30	RESET_PORVDDD	RW1C	A	1	Indicator that a POR occurred. This is a high-voltage cause bit, and hardware clears the other bits when this one is set. It does not block further recording of other high-voltage causes.

20.2.15 REG_PROT

Description: Register Protection
Address: 0x40030080
Offset: 0x80
Retention: Retained
IsDeepSleep: No
Comment: Unlocks access to Lock Protected Registers when the Magic Number is written into the register.
Default: 0xF08169E7

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	MAGIC [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	MAGIC [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	MAGIC [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	MAGIC [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	MAGIC	RW	R	4035013095	Setting this register to the value 0xf08169e7 unlocks access to Lock Protected Registers. These registers can not be written to unless this value has been written into this register. Writing a value OTHER than the magic key will disable access to the registers. The register POR value is set to 'unlock' the register access. The registers locked are PWR_CONTROL, PWR_KEY_DELAY, CLK_SELECT, CLK_ILO_CONFIG, CLK_IMO_CONFIG, CRWDT_CTL, CRWDT_EARLY, PWR_SSV_CTL, CRWDT_WARN, CRWDT_LATE, LIFETIME_CTL,HPOSC_CTL(if HPOSC_PRESENT=1), PILO_CTL(if PILO_PRESENT=1), and all trim registers

20.2.16 CRWDT_CTL

Description: Challenge Response WatchDog Control (Lock Protected)
Address: 0x40030090
Offset: 0x90
Retention: Retained
IsDeepSleep: No
Comment: Window WatchDog Control Register - locked when REG_PROT.MAGIC != Magic Number
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	ENABLED [31:31]	STATUS _ENABLED [30:30]	None [29:24]					

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
30	STATUS_ENABLED	R	RW	0	Indicates actual state of CRWDT enable. May lag ENABLED by up to one clk_lf cycles.
31	ENABLED	RW	R	0	When set to '1' enables Challenge/Response WatchDog Timer to Count. Will require 2 clk_lf cycles to take effect.

20.2.17 CRWDT_CHALLENGE

Description: Challenge Response WatchDog Challenge Value
Address: 0x40030094
Offset: 0x94
Retention: Retained
IsDeepSleep: No
Comment: Challenge register for Windowed WatchDog.
Default: 0xFF

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	CHALLENGE [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:7	CHALLENGE	R	RW	255	Challenge/Response WatchDog Challenge value. Implements the LFSR CCRC8-AutoSar using the polynomial x^8+x^5+x^3+x^2+x+1. The next value in the LFSR sequence is used to compare against the value subsequently written to the CRWDT_RESPONSE register. Incremented by write to CRWDT_RESPONSE to LFSR value next in the LFSR sequence after the value written to CRWDT_RESPONSE. Also incremented each time this register before a response is written to CRWDT_RESPONSE.

20.2.18 CRWDT_RESPONSE

Description: Challenge Response WatchDog Response Value
Address: 0x40030098
Offset: 0x98
Retention: Retained
IsDeepSleep: No
Comment: Response register for Windowed WatchDog
Default: 0xFF

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	RESPONSE [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:7	RESPONSE	RW	R	255	Challenge/Response WatchDog Response value. Value is compared against the expected next value in the LFSR sequence following the value obtained from CRWDT_CHALLENGE. If the values match, the CRWDT_UPCNT resets. If the values miscompare, the action selected by CRWDT_CONFIG.CHALLENGE_FAIL_ACTION occurs.

20.2.19 CRWDT_UPCNT

Description: Challenge Response WatchDog Up Counter
Address: 0x4003009C
Offset: 0x9C
Retention: Retained
IsDeepSleep: No
Comment: Response register for Windowed WatchDog
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	UPCNT [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	UPCNT [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	UPCNT [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:23	UPCNT	R	RW	0	Challenge/Response WatchDog Up Counter. The counter upcounts upon every clk_lf occurrence when enabled. If a match occurs between CRWDT_CHALLENGE and CRWDT_RESPONSE, the counter resets. If there is a mismatch, the action is taken selected by CRWDT_CONFIG.CHALLENGE_FAIL_ACTION. The counter will also reset when CRWDT_UPCNT=CRWDT_LATE. CRWDT_CTL.ENABLED=0 - Counter reset CRWDT_CTL.ENABLED=1 - Counter Increments

20.2.20 CRWDT_EARLY

Description: Challenge Response WatchDog Early Limit (Lock Protected)
Address: 0x400300A0
Offset: 0xA0
Retention: Retained
IsDeepSleep: No
Comment: Windowed WatchDog Early Count value
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	EARLY [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	EARLY [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	EARLY [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:23	EARLY	RW	R	0	Challenge/Response Early Value will cause the action selected by CRWDT_CONFIG.EARLY_ACTION if CRWDT_UPCNT < CRWDT_EARLY and there is a CRWDT_CHALLENGE/CRWDT_RESPONSE match. Writes to this register are ignored when CRWDT_CTL.ENABLED<>0.

20.2.21 CRWDT_WARN

Description: Challenge Response WatchDog Warning Limit (Lock Protected)
Address: 0x400300A4
Offset: 0xA4
Retention: Retained
IsDeepSleep: No
Comment: Windowed WatchDog Warning Value
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	WARNING [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	WARNING [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	WARNING [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:23	WARNING	RW	R	0	Challenge/Response Warning Value will cause the action selected by CRWDT_CONFIGWARN_ACTION if CRWDT_UPCNT>CRWDT_WARN and there is a CRWDT_CHALLENGE/CRWDT_RESPONSE match. Writes to this register are ignored when CRWDT_CTL.ENABLED<>0.

20.2.22 CRWDT_LATE

Description: Challenge Response WatchDog Late Limit (Lock Protected)
Address: 0x400300A8
Offset: 0xA8
Retention: Retained
IsDeepSleep: No
Comment: Windowed WatchDog Late Value
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	LATE [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	LATE [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	LATE [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:23	LATE	RW	R	0	Challenge/Response Late Value will cause action selected by CRWDT_CONFIG.LATE_ACTION if CRWDT_UPCNT = CRWDT_LATE. Writes to this register are ignored when CRWDT_CTL.ENABLED<>0.

20.2.23 CRWDT_CONFIG

Description: Challenge Response WatchDog Configuration
Address: 0x400300AC
Offset: 0xAC
Retention: Retained
IsDeepSleep: No
Comment: Configuration for watchdog.
Default: 0x810

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:5]			LATE_ACTION [4:4]	None [3:1]			EARLY_ACTION [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:12]				CHALLENGE_FAIL_ACTION [11:11]	None [10:9]		WARN_ACTION [8:8]

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	DEBUG_RUN [31:31]	None [30:24]						

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	EARLY_ACTION	RW	A	0	Action taken if this watchdog when the proper response is written to CRWDT_RESPONSE before CRWDT_UPCNT reaches CRWDT_EARLY. EARLY_ACTION is ignored (i.e. treated as NOTHING) when a debugger is connected. For CRWDT_EARLY > CRWDT_UPCNT: The action is triggered on same edge as when it meets this condition. For CRWDT_EARLY <= CRWDT_UPCNT: No action is triggered. Writes to this register are ignored when CRWDT_CTL.ENABLED<>0.
	NOTHING			0	Do nothing
	FAULT_AND_INT			1	Trigger a Fault and interrupt
4	LATE_ACTION	RW	A	1	Action taken if this watchdog is not serviced before CRWDT_LATE s reached. The counter resets CRWDT_UPCNT when CRWDT_LATE is reached, regardless of CRWDT_CONFIG.LATE_ACTION setting. LATE_ACTION is ignored (i.e. treated as NOTHING) when a debugger is connected. For CRWDT_LATE == CRWDT_UPCNT: The action is triggered on same edge as when it meets this condition. For CRWDT_LATE > CRWDT_UPCNT: No action is taken Writes to this register are ignored when CRWDT_CTL.ENABLED<>0.

Bits	Name	SW	HW	Default or Enum	Description
	NOTHING			0	Do nothing
	FAULT_RESET			1	Trigger a fault. Further, trigger a system-wide reset if the CRWDT is not disabled within 6 clk_lf cycles.
8	WARN_ACTION	RW	A	0	Action taken if this watchdog when the proper response is written to CRWDT_RESPONSE and CRWDT_UPCNT reaches CRWDT_WARN and CRWDT_UPCNT<CRWDT_LATE. WARN_ACTION is ignored (i.e. treated as NOTHING) when a debugger is connected. For CRWDT_WARN == CRWDT_UPCNT && CRWDT_LATE > CRWDT_UPCNT: The action is triggered on same edge as when it meets this condition. For CRWDT_WARN <CRWDT_UPCNT: No action is triggered. Writes to this register are ignored when CRWDT_CTL.ENABLED<>0.
	NOTHING			0	Do nothing
	FAULT_AND_INT			1	Trigger a Fault and interrupt
11	CHALLENGE_FAIL_ACTION	RW	A	1	Action taken when a failed response occurs, i.e. the expected LFSR value is different than the expected value. Writes to this register are ignored when CRWDT_CTL.ENABLED<>0.
	NOTHING			0	Do nothing
	RESET			1	Trigger a reset
31	DEBUG_RUN	RW	A	0	Pauses/runs this counter while a debugger is connected. Other behaviors are unchanged during debugging, including service, configuration updates and enable/disable. Note it may take up to two clk_lf cycles for the counter to pause and another two cycles to unpause, due to internal synchronization. If the debugger is connected for at least two clk_lf cycles, the EARLY_ACTION is ignored until after the first service after the debugger is disconnected. This prevents an unintentional trigger of the EARLY_ACTION before the firmware realigns the servicing period. After the first service, EARLY_ACTION behaves as configured. If the debugger is disconnected before two clk_lf cycles, the EARLY_ACTION may or may not be ignored. 0: When debugger connected, counter pauses incrementing. 1: When debugger connected, counter increments normally, but reset generation is blocked. Writes to this register are ignored when CRWDT_CTL.ENABLED<>0.

20.2.24 LIFETIME_CTL

Description: Liftetime Counter Control (Lock Protected)
Address: 0x400300B0
Offset: 0xB0
Retention: Retained
IsDeepSleep: No
Comment: This register resets with hard reset (power related, XRES, WDT).
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:3]					PRESEL [2:0]		

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	ENABLED [31:31]	STATUS _ENABLED [30:30]	None [29:24]					

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:2	PRESEL	RW	A	0	Select Divide ratio for Preselector. Legal values are 0-4. Values 5, 6, and 7 yield the same result as PERSEL_DIV32. Do not change this setting when lifetime counter is enabled (LIFETIME_CTL.ENABLED=1). Due to internal synchronization, it takes about 1 LFCLK cycles to update the counters after a write to this register. This register bit only resets for XRES, POR, or a detected BOD.
	PRESEL_DIV2			0	Divide CLK_LF by 2
	PRESEL_DIV4			1	Divide CLK_LF by 4
	PRESEL_DIV8			2	Divide CLK_LF by 8
	PRESEL_DIV16			3	Divide CLK_LF by 16
	PRESEL_DIV32			4	Divide CLK_LF by 32
30	STATUS_ENABLED	R	RW	0	Indicates actual state of lifetime counter enable. May lag ENABLED by up to one clk_lf cycles.
31	ENABLED	RW	A	0	When set to '1' enables LIFETIME_COUNTER to increment. Due to internal synchronization, may take up to one clk_lf cycles to take effect. The synchronization can be checked by waiting until ENABLED==STATUS_ENABLED whenever ENABLED is changed. When ENABLE changes from 1->0, the counter can be loaded with new COUNT value. Refer to LIFETIME_COUNTER.COUNT for details. User can enter DeepSleep without waiting for synchronization to complete (ENABLED==STATUS_ENABLED). This register bit only resets for XRES, POR, or a detected BOD.

20.2.25 LIFETIME_WAKEUP

Description: Lifetime Wakeup Value
Address: 0x400300B4
Offset: 0xB4
Retention: Retained
IsDeepSleep: No
Comment: This register resets with hard reset (power related, XRES, WDT).
Default: 0xFFFFFFFF

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	WAKEUP [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	WAKEUP [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	WAKEUP [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	WAKEUP [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	WAKEUP	RW	A	4294967295	Compare the WAKEUP value against LIFETIME_COUNTER. If they are equal interrupt_wakeup to set. Due to internal synchronization, it may take up to 1 LFCLK cycles to update the counters after a write to this register. This register bit only resets for XRES, POR, or a detected BOD.

20.2.26 LIFETIME_COUNTER

Description: Lifetime Counter Current Value
Address: 0x400300B8
Offset: 0xB8
Retention: Retained
IsDeepSleep: No
Comment: This register resets with hard reset (power related, XRES, WDT).
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	COUNT [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	COUNT [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	COUNT [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	COUNT [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	COUNT	RW	A	0	Lifetime Counter which clocks on the output of the CLK_LF PreScalar output controlled by LIFETIME_CTL.PRESEL. The counter doesn't increment unless LIFETIME_CTL.STATUS_ENABLED =1. FW is responsible for initializing this value after reset and maintaining the running value. SW writes will be ignored when LIFETIME_CTL.ENABLED=1. The counter needs to be disabled one LFCLK cycle (or LIFETIME_CTL.STATUS_ENABLED=0) for the internal synchronization of this field to take place. This register bit only resets for XRES, POR, or a detected BOD.

20.2.27 PWR_SSV_CTL

Description: Supply Supervisory Control Register (Lock Protected)
Address: 0x400300E0
Offset: 0xE0
Retention: Retained
IsDeepSleep: No
Comment: Controls for brownout and over-voltage detectors. This register resets with hard reset (power related, XRES, WDT).
Default: 0x808

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:4]				BODVDDD_ENABLE [3:3]	None [2:0]		

Bits	15	14	13	12	11	10	9	8
Name	None [15:12]				BODVCCD_ENABLE [11:11]	None [10:8]		

Bits	23	22	21	20	19	18	17	16
Name	None [23:20]				OVDVDDD_ENABLE [19:19]	None [18:16]		

Bits	31	30	29	28	27	26	25	24
Name	BODHVSS_ENABLE [31:31]	None [30:28]			OVDVCCD_ENABLE [27:27]	None [26:24]		

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
3	BODVDDD_ENABLE	RW	A	1	Enable for BOD on vddd. This cannot be disabled during normal operation.
11	BODVCCD_ENABLE	RW	A	1	Enable for BOD on vccd. This cannot be disabled during normal operation.
19	OVDVDDD_ENABLE	RW	A	0	Enable for OVD on vddd. FW should enable this after the OVD trims are set during boot-up and keep it enabled.
27	OVDVCCD_ENABLE	RW	A	0	Enable for OVD on vccd. FW should enable this after the OVD trims are set during boot-up and keep it enabled.
31	BODHVSS_ENABLE	RW	A	0	Enable for BOD on vddd from HVSS. This gives BOD robustness during DeepSleep. FW should enable during boot-up and keep it enabled.

20.2.28 PWR_SSV_STATUS

Description: Supply Supervision Status Register
Address: 0x400300E4
Offset: 0xE4
Retention: Retained
IsDeepSleep: No
Comment: Status for brownout and over-voltage detectors.
Default: 0x1005

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:3]					BODVCCD_OK [2:2]	None [1:1]	BODVDDD_OK [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:13]			BODHVSS_OK [12:12]	None [11:11]	OVDVCCD_OK [10:10]	None [9:9]	OVDVDDD_OK [8:8]

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	BODVDDD_OK	R	RW	1	BOD indicates vddd is ok. This will always read 1, because a detected brownout will reset the chip.
2	BODVCCD_OK	R	RW	1	BOD indicates vccd is ok. This will always read 1, because a detected brownout will reset the chip.
8	OVDVDDD_OK	R	RW	0	OVD indicates vddd is ok. After OVDVDDD is enabled it will always read 1, because a detected over-voltage condition will reset the chip.
10	OVDVCCD_OK	R	RW	0	OVD indicates vccd is ok. After OVDVCCD is enabled it will always read 1, because a detected over-over-voltage condition will reset the chip.
12	BODHVSS_OK	R	RW	1	BODHVSS indicates vddd is ok. This will always read 1, because a detected brownout will reset the chip.

20.2.29 HPOSC_CTL

Description: High Precision Oscillator Control (Lock Protected)
Address: 0x40030300
Offset: 0x300
Retention: Retained
IsDeepSleep: No
Comment: High Precision Osc Control
Default: 0x1

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:5]			CTAT_SWB [4:4]	None [3:2]		CTAT_SEL [1:1]	LEAKC _DIS [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	IMO_EN [31:31]	None [30:24]						

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	LEAKC_DIS	RW	R	1	RESERVED
1	CTAT_SEL	RW	R	0	CTAT generator selection, only valid when CTAT_SW = 1. 0 - Low noise type CTAT generator 1 - Fast start-up type CTAT generator
4	CTAT_SWB	RW	R	0	Selection control for internal CTAT generator. 0 - Auto Select (Fast start followed by low noise generator) 1 - Generator selected by CTAT_SEL
31	IMO_EN	RW	R	0	HPOSC enable. Setting this bit will enable the HPOSC and clearing this bit will disable the HPOSC. Don't disable this clock if the system is using this clock as the source.

20.2.30 PILO_CTL

Description: Precision Low Power Oscillator Control (Lock Protected)
Address: 0x40030400
Offset: 0x400
Retention: Retained
IsDeepSleep: No
Comment: Precision Low Power Oscillator Control.
Default: 0xC001

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:5]			CTAT_SWB [4:4]	None [3:2]		CTAT_SEL [1:1]	LEAKC _DIS [0:0]

Bits	15	14	13	12	11	10	9	8
Name	TR_CAP [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	ILO_EN [31:31]	None [30:24]						

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	LEAKC_DIS	RW	R	1	RESERVED
1	CTAT_SEL	RW	R	0	CTAT generator selection, only valid when CTAT_SW = 1. 0 - Low noise type CTAT generator 1 - Fast start-up type CTAT generator
4	CTAT_SWB	RW	R	0	Selection control for internal CTAT generator. 0 - Auto Select (Fast start followed by low noise generator) 1 - Generator selected by CTAT_SEL
8:15	TR_CAP	RW	A	192	PILO user temperature fine trim. This register field resets with hard reset (power related, XRES, WDT)..
31	ILO_EN	RW	A	0	PILO enable. Setting this bit will enable the PILO and clearing this bit will disable it. Do not disable this clock prior to changing CLK_LF to use the PILO as a source. CLK_LF must be configured to use PILO as a source while the PILO clock is enabled prior to making such a change. Writes to this field are ignored when LFCLK_SEL is using this clock as the source and WDT is locked using WDT_LOCK register. Consequently, if CLK_LF is sourced by the PILO and the PILO is to be disabled, clear WDT_LOCK beforehand. This register field resets with hard reset (power related, XRES, WDT).

20.2.31 PWR_BG_TRIM1

Description: Bandgap Trim Register (Lock Protected)
Address: 0x4003FF00
Offset: 0xFF00
Retention: Retained
IsDeepSleep: No
Comment: Trim bits for Reference System
Default: 0xD

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:6]		REF_VTRIM [5:0]					

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:5	REF_VTRIM	RW	R	13	Trims the bandgap reference voltage output. Used to trim the VBG to the voltage where its temperature curvature is minimal. Bit [5] is unused within the bandgap block.

20.2.32 PWR_BG_TRIM2

Description: Bandgap Trim Register (Lock Protected)
Address: 0x4003FF04
Offset: 0xFF04
Retention: Retained
IsDeepSleep: No
Comment: Trim bits for Reference System
Default: 0x23

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:6]		REF_ITRIM [5:0]					

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:5	REF_ITRIM	RW	R	35	Trims the bandgap reference current output. Used to trim the IBG to the voltage where its temperature curvature is minimal.

20.2.33 CLK_IMO_SELECT

Description: IMO Frequency Select Register (Lock Protected)
Address: 0x4003FF08
Offset: 0xFF08
Retention: Retained
IsDeepSleep: No
Comment: Selects the operating frequency of the IMO
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:3]					FREQ [2:0]		

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:2	FREQ	RW	R	0	Select operating frequency
	24_MHZ			0	IMO runs at 24 MHz
	28_MHZ			1	IMO runs at 28 MHz
	32_MHZ			2	IMO runs at 32 MHz
	36_MHZ			3	IMO runs at 36 MHz
	40_MHZ			4	IMO runs at 40 MHz
	44_MHZ			5	IMO runs at 44 MHz
	48_MHZ			6	IMO runs at 48 MHz

20.2.34 CLK_IMO_TRIM1

Description: IMO Trim Register (Lock Protected)
Address: 0x4003FF0C
Offset: 0xFF0C
Retention: Retained
IsDeepSleep: No
Comment: Trims IMO frequency to within datasheet accuracy, or allows for trimming IMO to frequency lock to a more accurate frequency source.
Default: 0x6C

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	OFFSET [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:7	OFFSET	RW	RW	108	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. This field is hardware updated during USB osclock mode. This field is mapped to the most significant bits of the IMO trim imo_clk_trim[10:3]. The step size of 1 LSB on this field is nominally 160 kHz.

20.2.35 CLK_IMO_TRIM2

Description: IMO Trim Register (Lock Protected)
Address: 0x4003FF10
Offset: 0xFF10
Retention: Retained
IsDeepSleep: No
Comment: IMO Trim Bits
Default: 0xA0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	TCTRIM [7:4]				None [3:3]	FSOFFSET [2:0]		

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:2	FSOFFSET	RW	RW	0	Frequency trim bits. These bits are not trimmed during manufacturing and kept at 0 under normal operation. This field is hardware updated during USB osclock mode. This field is mapped to the least significant bits of the IMO trim imo_clk_trim[2:0]. The step size of 1 LSB on this field is nominally 20 kHz.
4:7	TCTRIM	RW	R	10	IMO temperature compensation trim. These bits are determined at manufacturing time to adjust for temperature dependence. This bits are dependent on frequency and need to be changed using the Cypress provided frequency change algorithm.

20.2.36 CLK_IMO_TRIM3

Description: IMO Trim Register (Lock Protected)
Address: 0x4003FF14
Offset: 0xFF14
Retention: Retained
IsDeepSleep: No
Comment: IMO Trim Bits
Default: 0xF

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:5]			STEPSIZE [4:0]				

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:4	STEPSIZE	RW	R	15	IMO trim stepsize bits. These bits are determined at manufacturing time to adjust for process variation. They are used to tune the stepsize of the FSOFFSET and OFFSET trims.

20.2.37 PWR_PWRSYS_TRIM1

Description: Power System Trim Register (Lock Protected)
Address: 0x4003FF18
Offset: 0xFF18
Retention: Retained
IsDeepSleep: No
Comment: Power System Trim Bits
Default: 0x10

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	SPARE_TRIM [7:4]				DPSLP_REF_TRIM [3:0]			

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:3	DPSLP_REF_TRIM	RW	R	0	Trims the DeepSleep reference that is used by the DeepSleep regulator and DeepSleep power comparator.
4:7	SPARE_TRIM	RW	R	1	Active-Reference temperature compensation trim (repurposed from spare bits). Bits [7:6] - trim the Active-Reference IREF temperature coefficient (TC). 00: TC = 0 (unchanged) 01: TC = +80ppm/C 10: TC = -80ppm/C 11: TC = -150ppm/C Bits [5:4] - trim the Active-Reference VREF temperature coefficient (TC). 00: TC = 0 (unchanged) 01: TC = -50ppm/C 10: TC = -80ppm/C 11: TC = +150ppm/C

20.2.38 TRIM_BODVCCD

Description: Brown Out Detect Trim (VCCD) (Lock Protected)
Address: 0x4003FF1C
Offset: 0xFF1C
Retention: Retained
IsDeepSleep: No
Comment: Power System Trim Bits. This register resets with hard reset (power related, XRES, WDT).
Default: 0x8

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:5]			BOD_RANGE_SELECT_VCCD [4:4]	BOD_TRIPSEL_VCCD [3:0]			

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:3	BOD_TRIPSEL_VCCD	RW	A	8	BOD VCCD trim (production)
4	BOD_RANGE_SELECT_VCCD	RW	A	0	Range select between 1.6V Vs 1.69V nominal.

20.2.39 TRIM_OVDVCCD

Description: Over Voltage Detect Trim (VCCD) (Lock Protected)
Address: 0x4003FF20
Offset: 0xFF20
Retention: Retained
IsDeepSleep: No
Comment: Power System Trim Bits. This register resets with hard reset (power related, XRES, WDT).
Default: 0x7

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:4]				OVD_TRIPSEL_VCCD [3:0]			

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:3	OVD_TRIPSEL_VCCD	RW	A	7	OVD VCCD trim (options)

20.2.40 TRIM_HPOSC0_CTL

Description: High Precision Oscillator Trim Control 0 (Lock Protected)
Address: 0x4003FF24
Offset: 0xFF24
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xF

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	PTATEC [7:6]		CTATEC [5:4]		PTATEF [3:2]		CTATEF [1:0]	

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:1	CTATEF	RW	R	3	HPOSC frequency CTAT extra-fine trim
2:3	PTATEF	RW	R	3	Fine trim for HPOSC PTAT current
4:5	CTATEC	RW	R	0	Coarse trim for HPOSC CTAT current
6:7	PTATEC	RW	R	0	Coarse trim for HPOSC PTAT current

20.2.41 TRIM_HPOSC1_CTL

Description: High Precision Oscillator Trim Control 1 (Lock Protected)
Address: 0x4003FF28
Offset: 0xFF28
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xD

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:5]			TCF [4:0]				

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:4	TCF	RW	R	13	HPOSC temp-co fine trim

20.2.42 TRIM_HPOSC2_CTL

Description: High Precision Oscillator Trim Control 2 (Lock Protected)
Address: 0x4003FF2C
Offset: 0xFF2C
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xA4

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	PTAT [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:7	PTAT	RW	R	164	HPOSC PTAT trim

20.2.43 TRIM_HPOSC3_CTL

Description: High Precision Oscillator Trim Control 3 (Lock Protected)
Address: 0x4003FF30
Offset: 0xFF30
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xB1

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	CTAT [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:7	CTAT	RW	R	177	HPOSC CTAT trim

20.2.44 TRIM_HPOSC4_CTL

Description: High Precision Oscillator Trim Control 4 (Lock Protected)
Address: 0x4003FF34
Offset: 0xFF34
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x3

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	HPOSC_LEAK [7:3]					TOC [2:0]		

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:2	TOC	RW	R	3	HPOSC temp-co coarse trim
3:7	HPOSC_LEAK	RW	R	0	HPOSC leakage cancellation trim

20.2.45 TRIM_PILO0_CTL

Description: Low Frequency Oscillator Trim Control 0 (Lock Protected)
Address: 0x4003FF38
Offset: 0xFF38
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	PTATEC [7:6]		CTATEC [5:4]		PTATEF [3:2]		CTATEF [1:0]	

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:1	CTATEF	RW	A	0	PILO frequency CTAT extra-fine trim
2:3	PTATEF	RW	A	0	PILO frequency PTATextra-fine trim
4:5	CTATEC	RW	A	0	PILO temperature CTAT extra-coarse trim
6:7	PTATEC	RW	A	0	PILO temperature PTATextra-coarse trim

20.2.46 TRIM_PILO1_CTL

Description: Low Frequency Oscillator Trim Control 1 (Lock Protected)
Address: 0x4003FF3C
Offset: 0xFF3C
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:5]			TCF [4:0]				

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:4	TCF	RW	A	0	PILO temp-co fine trim (MSB, bit 4, is not used)

20.2.47 TRIM_PILO2_CTL

Description: Low Frequency Oscillator Trim Control 2 (Lock Protected)
Address: 0x4003FF40
Offset: 0xFF40
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	PTAT [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:7	PTAT	RW	A	0	PILO frequency PTAT coarse trim

20.2.48 TRIM_PILO3_CTL

Description: Low Frequency Oscillator Trim Control 3 (Lock Protected)
Address: 0x4003FF44
Offset: 0xFF44
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	CTAT [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:7	CTAT	RW	A	0	PILO frequency CTAT coarse trim

20.2.49 TRIM_PILO4_CTL

Description: Low Frequency Oscillator Trim Control 4 (Lock Protected)
Address: 0x4003FF48
Offset: 0xFF48
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:4]				TCC [3:0]			

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:3	TCC	RW	A	0	PILO temperature coarse trim

20.2.50 TRIM_PILO5_CTL

Description: Low Frequency Oscillator Trim Control 5 (Lock Protected)
Address: 0x4003FF4C
Offset: 0xFF4C
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:5]			PILO_TR_LEAK [4:0]				

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:4	PILO_TR_LEAK	RW	A	0	PILO leakage cancellation trim

20.2.51 TRIM_BODVDDD

Description: Brown Out Detect Trim (VDDD) (Lock Protected)
Address: 0x4003FF50
Offset: 0xFF50
Retention: Retained
IsDeepSleep: No
Comment: Power System Trim Bits. This register resets with hard reset (power related, XRES, WDT).
Default: 0x8

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:4]				BOD_TRIPSEL_VDDD [3:0]			

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:3	BOD_TRIPSEL_VDDD	RW	A	8	BOD VDDD trim (options)

20.2.52 TRIM_OVDVDDD

Description: Over Voltage Detect Trim (VDDD) (Lock Protected)
Address: 0x4003FF54
Offset: 0xFF54
Retention: Retained
IsDeepSleep: No
Comment: Power System Trim Bits. This register resets with hard reset (power related, XRES, WDT).
Default: 0x7

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:5]			OVD_RANGE_SELECT_VDDD [4:4]	OVD_TRIPSEL_VDDD [3:0]			

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:3	OVD_TRIPSEL_VDDD	RW	A	7	OVD VDDD trim (options)
4	OVD_RANGE_SELECT_VDDD	RW	A	0	Range select between 3.8V Vs 5.77V nominal.

20.2.53 WDT

20.2.53.1 WDT_CTL

Description: WDT Control Register
Address: 0x40030100
Offset: 0x0
Retention: Retained
IsDeepSleep: No
Comment: Control register for watchdog. Writes are ignored when locked (i.e. Corresponding LOCK.WDT_LOCK<>0).
Default: 0x80000001

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:1]							ENABLED [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	ENABLE [31:31]	None [30:24]						

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	ENABLED	R	RW	1	Indicates actual state of watchdog. May lag ENABLE by up to three clk_lf cycles.
31	ENABLE	RW	A	1	Enable watchdog. May take up to three clk_lf cycles to take effect. When ENABLE changes from 1->0, the counter is cleared. Do not enter DeepSleep if ENABLE<>ENABLED. This can be done by waiting until ENABLE==ENABLED whenever ENABLE is changed. 0: Counter is disabled (not clocked). 1: Counter is enabled (counting up)

20.2.53.2 WDT_LOWER_LIMIT

Description: WDT Lower Limit Register
Address: 0x40030104
Offset: 0x4
Retention: Retained
IsDeepSleep: No
Comment: Lower limit for watchdog. Writes are ignored when locked (i.e. Corresponding LOCK.WDT_LOCK<>0) or when enabled (i.e. ENABLE==1 and ENABLED==1).
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	LOWER_LIMIT [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	LOWER_LIMIT [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	LOWER_LIMIT [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	LOWER_LIMIT [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	LOWER_LIMIT	RW	A	0	Lower limit for watchdog. See LOWER_ACTION.

20.2.53.3 WDT_UPPER_LIMIT

Description: WDT Upper Limit Register
Address: 0x40030108
Offset: 0x8
Retention: Retained
IsDeepSleep: No
Comment: Upper limit for watchdog. Writes are ignored when locked (i.e. Corresponding LOCK.WDT_LOCK<>0) or when enabled (i.e. ENABLE==1 and ENABLED==1).
Default: 0x8000

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	UPPER_LIMIT [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	UPPER_LIMIT [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	UPPER_LIMIT [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	UPPER_LIMIT [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	UPPER_LIMIT	RW	A	32768	Upper limit for watchdog. See UPPER_ACTION.

20.2.53.4 WDT_WARN_LIMIT

Description: WDT Warn Limit Register
Address: 0x4003010C
Offset: 0xC
Retention: Retained
IsDeepSleep: No
Comment: Warn limit for watchdog. Writes are ignored when locked (i.e. Corresponding LOCK.WDT_LOCK<>0) or when enabled (i.e. ENABLE==1 and ENABLED==1).
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	WARN_LIMIT [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	WARN_LIMIT [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	WARN_LIMIT [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	WARN_LIMIT [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	WARN_LIMIT	RW	A	0	Warn limit for watchdog. See WARN_ACTION.

20.2.53.5 WDT_CONFIG

Description: WDT Configuration Register
Address: 0x40030110
Offset: 0x10
Retention: Retained
IsDeepSleep: No
Comment: Configuration for watchdog. Writes are ignored when locked (i.e. Corresponding LOCK.WDT_LOCK<>0) or when enabled (i.e. ENABLE==1 and ENABLED==1).
Default: 0x10

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:5]			UPPER_ACTION [4:4]	None [3:1]			LOWER_ACTION [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:13]			AUTO_SERVICE [12:12]	None [11:9]			WARN_ACTION [8:8]

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	DEBUG_RUN [31:31]	None [30:30]	DPSLP_PAUSE [29:29]	DEBUG_TRIGGER_EN [28:28]	None [27:24]			

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	LOWER_ACTION	RW	A	0	Action taken if this watchdog is serviced before LOWER_LIMIT is reached. LOWER_ACTION is ignored (i.e. treated as NOTHING) when a debugger is connected and/or when the chip is in DeepSleep modes. For LOWER_LIMIT >= 1: The action is triggered on same edge when it meets this condition. For LOWER_LIMIT == 0: No action is triggered.
	NOTHING			0	Do nothing
	RESET			1	Trigger a reset.
4	UPPER_ACTION	RW	A	1	Action taken if this watchdog is not serviced before UPPER_LIMIT is reached. The counter stops counting when UPPER_LIMIT is reached, regardless of UPPER_ACTION setting. UPPER_ACTION is ignored (i.e. treated as NOTHING) when a debugger is connected. For UPPER_LIMIT >= 2: The action is triggered on same edge when it meets this condition. For UPPER_LIMIT < 2: The action may take up to one extra clk_lf cycle to trigger.
	NOTHING			0	Do nothing
	RESET			1	Trigger a reset.

Bits	Name	SW	HW	Default or Enum	Description
8	WARN_ACTION	RW	A	0	Action taken when the count value reaches WARN_LIMIT. The minimum setting to achieve a periodic interrupt is WARN_LIMIT==1. A setting of zero will trigger once but not periodically. For WARN_LIMIT >= 2: The action is triggered on same edge when it meets this condition. For WARN_LIMIT < 2 : The action may take up to one extra clk_lf cycle to trigger.
	NOTHING			0	Do nothing
	INT			1	Trigger an interrupt.
12	AUTO_SERVICE	RW	A	0	Automatically service when the count value reaches WARN_LIMIT. This allows creation of a periodic interrupt if this counter is not needed as a watchdog. This field is ignored when LOWER_ACTION<>NOTHING or when UPPER_ACTION<>NOTHING.
28	DEBUG_TRIGGER_EN	RW	A	0	Enables the trigger input for WDT to pause the counter during debug mode. To pause at a breakpoint while debugging, configure the trigger matrix to connect the related CPU halted signal to the trigger input for this WDT, and then set this bit. It takes up to two clk_lf cycles for the trigger signal to be processed. Triggers that are less than two clk_lf cycles may be missed. Synchronization error can accumulate each time it is halted. 0: Pauses the counter whenever a debug probe is connected. 1: Pauses the counter whenever a debug probe is connected and the trigger input is high.
29	DPSLP_PAUSE	RW	A	0	Pauses/runs this counter when the system is in DeepSleep. Note it may take up to two clk_lf cycles for the counter to pause, due to internal synchronization. During DeepSleep wakeup, the pause request is removed when clk_hf starts clocking, and then it may take up to two clk_lf cycles for the counter to start. After wakeup, the LOWER_ACTION is ignored until after the first service. This prevents an unintentional trigger of the LOWER_ACTION before the firmware realigns the servicing period. After the first service, LOWER_ACTION behaves as configured. 0: Counter behaves normally during DeepSleep. 1: Counter pauses during DeepSleep.
31	DEBUG_RUN	RW	A	0	Pauses/runs this counter while a debugger is connected. Other behaviors are unchanged during debugging, including service, configuration updates and enable/disable. Note it may take up to two clk_lf cycles for the counter to pause and another two cycles to unpause, due to internal synchronization. If the debugger is connected for at least two clk_lf cycles, the LOWER_ACTION is ignored until after the first service after the debugger is disconnected. This prevents an unintentional trigger of the LOWER_ACTION before the firmware realigns the servicing period. After the first service, LOWER_ACTION behaves as configured. If the debugger is disconnected before two clk_lf cycles, the LOWER_ACTION may or may not be ignored. 0: When debugger connected, counter pauses incrementing as configured in DEBUG_TRIGGER_EN. 1: When debugger connected, counter increments normally, but reset generation is blocked.

20.2.53.6 WDT_CNT

Description: WDT Count Register
Address: 0x40030114
Offset: 0x14
Retention: Retained
IsDeepSleep: No
Comment: Count value for watchdog. Writes are ignored when locked (i.e. Corresponding LOCK.WDT_LOCK<>0) or when enabled (i.e. ENABLE==1 and ENABLED==1).
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	CNT [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	CNT [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	CNT [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	CNT [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	CNT	RW	A	0	Current value of subcounter for this WDT. This field may lag the actual count value by up to one clk_lf cycle, due to internal synchronization. When this subcounter is disabled and unlocked, the count value can be written for verification and debugging purposes. Software writes are always ignored when the subcounter is enabled.

20.2.53.7 WDT_LOCK

Description: WDT Lock register
Address: 0x40030140
Offset: 0x40
Retention: Retained
IsDeepSleep: No
Comment: Lock or unlock the registers in this WDT
Default: 0x3

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:2]						WDT_LOCK [1:0]	

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:1	WDT_LOCK	RW	A	3	Prohibits writing control and configuration registers related to this WDT when not equal 0 (as specified in the other register descriptions). Requires at least two different writes to unlock. Note that this field is 2 bits to force multiple writes only. This register also locks the clk_lf settings.
	NO_CHG			0	No effect
	CLR0			1	Clears bit 0
	CLR1			2	Clears bit 1
	SET01			3	Sets both bits 0 and 1

20.2.53.8 WDT_SERVICE

Description: WDT Service register
Address: 0x40030144
Offset: 0x44
Retention: Retained
IsDeepSleep: No
Comment: Control the behavior of the Watchdog counters. Writes to this register are ignored when LOCK.WDT_LOCK<>0. All fields in this register can be used while counter is in operation.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:1]							SERVICE [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	SERVICE	RW1S	RW1C	0	Services the watchdog. This resets the count value to zero. This may take up to three clk_lf cycle to take effect. Hardware clears this bit, after necessary synchronization. To ensure a pending SERVICE write is reflected, firmware should wait until this bit reads low before attempting to write SERVICE=1. If WDT is disabled, SERVICE will not trigger a LOWER_ACTION and will not clear a preloaded count value.

20.2.53.9 WDT_INTR

Description: WDT Interrupt Register
Address: 0x40030150
Offset: 0x50
Retention: Retained
IsDeepSleep: No
Comment: Interrupt signal from WDT. Reset with power resets, xres and WDT
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:1]							WDT [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	WDT	RW1C	A	0	WDT Interrupt Request. This bit is set as configured by WDT action and limits. Due to internal synchronization, it takes up to 8 SYSCLK cycles to update after a W1C or reading this register and during this time AHB bus is stalled.

20.2.53.10 WDT_INTR_SET

Description: WDT Interrupt Set Register
Address: 0x40030154
Offset: 0x54
Retention: Retained
IsDeepSleep: No
Comment: Can be used to set interrupts for firmware testing.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:1]							WDT [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	WDT	RW1S	A	0	Set interrupt. Due to internal synchronization, it takes up to 8 SYSCLK cycles to update after a W1S or reading from this register and during this time AHB bus is stalled. Reads back same as WDT_B.INTR.WDT

20.2.53.11 WDT_INTR_MASK

Description: WDT Interrupt Mask Register
Address: 0x40030158
Offset: 0x58
Retention: Retained
IsDeepSleep: No
Comment: Controls whether interrupt is forwarded to CPU. All masks block the interrupt when 0 and forward the interrupt when 1
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:1]							WDT [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	WDT	RW	R	0	Mask for watchdog timer. Clearing this bit will not forward the interrupt to the CPU.

20.2.53.12 WDT_INTR_MASKED

Description: WDT Interrupt Masked Register
Address: 0x4003015C
Offset: 0x5C
Retention: Retained
IsDeepSleep: No
Comment: Bitwise AND between the interrupt request and mask registers so firmware can read the status of all mask enabled interrupt causes with a single load operation
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:1]							WDT [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	WDT	R	RW	0	Logical and of corresponding request and mask bits. Due to internal synchronization, it takes up to 8 SYSCLK cycles to read from this register. During this time AHB bus is stalled.

21 TCPWM

Description Timer/Counter/PWM
Base Address 0x40200000
Size 0x10000
Slave Num MMIO1

Register Name	Address	Permission	Description
TCPWM_CTRL	0x40200000	FULL	TCPWM control register 0.
TCPWM_CMD	0x40200008	FULL	TCPWM command register.
TCPWM_INTR_CAUSE	0x4020000C	FULL	TCPWM Counter interrupt cause register.

21.1 CNT 0

Register Name	Address	Permission	Description
TCPWM_CNT0_CTRL	0x40200100	FULL	Counter control register
TCPWM_CNT0_STATUS	0x40200104	FULL	Counter status register
TCPWM_CNT0_COUNTER	0x40200108	FULL	Counter count register
TCPWM_CNT0_CC	0x4020010C	FULL	Counter compare/capture register
TCPWM_CNT0_CC_BUFF	0x40200110	FULL	Counter buffered compare/capture register
TCPWM_CNT0_PERIOD	0x40200114	FULL	Counter period register
TCPWM_CNT0_PERIOD_BUFF	0x40200118	FULL	Counter buffered period register
TCPWM_CNT0_TR_CTRL0	0x40200120	FULL	Counter trigger control register 0
TCPWM_CNT0_TR_CTRL1	0x40200124	FULL	Counter trigger control register 1
TCPWM_CNT0_TR_CTRL2	0x40200128	FULL	Counter trigger control register 2
TCPWM_CNT0_INTR	0x40200130	FULL	Interrupt request register.
TCPWM_CNT0_INTR_SET	0x40200134	FULL	Interrupt set request register.
TCPWM_CNT0_INTR_MASK	0x40200138	FULL	Interrupt mask register.
TCPWM_CNT0_INTR_MASKED	0x4020013C	FULL	Interrupt masked request register

21.2 CNT 1

Register Name	Address	Permission	Description
TCPWM_CNT1_CTRL	0x40200140	FULL	Counter control register
TCPWM_CNT1_STATUS	0x40200144	FULL	Counter status register
TCPWM_CNT1_COUNTER	0x40200148	FULL	Counter count register
TCPWM_CNT1_CC	0x4020014C	FULL	Counter compare/capture register
TCPWM_CNT1_CC_BUFF	0x40200150	FULL	Counter buffered compare/capture register
TCPWM_CNT1_PERIOD	0x40200154	FULL	Counter period register
TCPWM_CNT1_PERIOD_BUFF	0x40200158	FULL	Counter buffered period register
TCPWM_CNT1_TR_CTRL0	0x40200160	FULL	Counter trigger control register 0
TCPWM_CNT1_TR_CTRL1	0x40200164	FULL	Counter trigger control register 1
TCPWM_CNT1_TR_CTRL2	0x40200168	FULL	Counter trigger control register 2
TCPWM_CNT1_INTR	0x40200170	FULL	Interrupt request register.
TCPWM_CNT1_INTR_SET	0x40200174	FULL	Interrupt set request register.
TCPWM_CNT1_INTR_MASK	0x40200178	FULL	Interrupt mask register.
TCPWM_CNT1_INTR_MASKED	0x4020017C	FULL	Interrupt masked request register

21.3 CNT 2

Register Name	Address	Permission	Description
TCPWM_CNT2_CTRL	0x40200180	FULL	Counter control register
TCPWM_CNT2_STATUS	0x40200184	FULL	Counter status register
TCPWM_CNT2_COUNTER	0x40200188	FULL	Counter count register
TCPWM_CNT2_CC	0x4020018C	FULL	Counter compare/capture register
TCPWM_CNT2_CC_BUFF	0x40200190	FULL	Counter buffered compare/capture register
TCPWM_CNT2_PERIOD	0x40200194	FULL	Counter period register
TCPWM_CNT2_PERIOD_BUFF	0x40200198	FULL	Counter buffered period register
TCPWM_CNT2_TR_CTRL0	0x402001A0	FULL	Counter trigger control register 0
TCPWM_CNT2_TR_CTRL1	0x402001A4	FULL	Counter trigger control register 1
TCPWM_CNT2_TR_CTRL2	0x402001A8	FULL	Counter trigger control register 2
TCPWM_CNT2_INTR	0x402001B0	FULL	Interrupt request register.
TCPWM_CNT2_INTR_SET	0x402001B4	FULL	Interrupt set request register.
TCPWM_CNT2_INTR_MASK	0x402001B8	FULL	Interrupt mask register.
TCPWM_CNT2_INTR_MASKED	0x402001BC	FULL	Interrupt masked request register

21.4 CNT 3

Register Name	Address	Permission	Description
TCPWM_CNT3_CTRL	0x402001C0	FULL	Counter control register
TCPWM_CNT3_STATUS	0x402001C4	FULL	Counter status register
TCPWM_CNT3_COUNTER	0x402001C8	FULL	Counter count register
TCPWM_CNT3_CC	0x402001CC	FULL	Counter compare/capture register
TCPWM_CNT3_CC_BUFF	0x402001D0	FULL	Counter buffered compare/capture register
TCPWM_CNT3_PERIOD	0x402001D4	FULL	Counter period register
TCPWM_CNT3_PERIOD_BUFF	0x402001D8	FULL	Counter buffered period register
TCPWM_CNT3_TR_CTRL0	0x402001E0	FULL	Counter trigger control register 0
TCPWM_CNT3_TR_CTRL1	0x402001E4	FULL	Counter trigger control register 1
TCPWM_CNT3_TR_CTRL2	0x402001E8	FULL	Counter trigger control register 2
TCPWM_CNT3_INTR	0x402001F0	FULL	Interrupt request register.
TCPWM_CNT3_INTR_SET	0x402001F4	FULL	Interrupt set request register.
TCPWM_CNT3_INTR_MASK	0x402001F8	FULL	Interrupt mask register.
TCPWM_CNT3_INTR_MASKED	0x402001FC	FULL	Interrupt masked request register

21.5 CNT 4

Register Name	Address	Permission	Description
TCPWM_CNT4_CTRL	0x40200200	FULL	Counter control register
TCPWM_CNT4_STATUS	0x40200204	FULL	Counter status register
TCPWM_CNT4_COUNTER	0x40200208	FULL	Counter count register
TCPWM_CNT4_CC	0x4020020C	FULL	Counter compare/capture register
TCPWM_CNT4_CC_BUFF	0x40200210	FULL	Counter buffered compare/capture register
TCPWM_CNT4_PERIOD	0x40200214	FULL	Counter period register
TCPWM_CNT4_PERIOD_BUFF	0x40200218	FULL	Counter buffered period register
TCPWM_CNT4_TR_CTRL0	0x40200220	FULL	Counter trigger control register 0
TCPWM_CNT4_TR_CTRL1	0x40200224	FULL	Counter trigger control register 1
TCPWM_CNT4_TR_CTRL2	0x40200228	FULL	Counter trigger control register 2
TCPWM_CNT4_INTR	0x40200230	FULL	Interrupt request register.
TCPWM_CNT4_INTR_SET	0x40200234	FULL	Interrupt set request register.
TCPWM_CNT4_INTR_MASK	0x40200238	FULL	Interrupt mask register.
TCPWM_CNT4_INTR_MASKED	0x4020023C	FULL	Interrupt masked request register

21.6 Register Details

21.6.1 TCPWM_CTRL

Description: TCPWM control register 0.
Address: 0x40200000
Offset: 0x0
Retention: Not Retained
IsDeepSleep: No
Comment: Used to disable/enable the counters.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:5]			COUNTER_ENABLED [4:0]				

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:4	COUNTER_ENABLED	RW	R	0	Counter enables for counters 0 up to CNT_NR-1. '0': counter disabled. '1': counter enabled. Counter static configuration information (e.g. CTRL.MODE, all TR_CTRL0, TR_CTRL1, and TR_CTRL2 register fields) should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ('tr_overflow', 'tr_underflow' and 'tr_compare_match'). - the counter's line outputs ('line_out' and 'line_compl_out').

21.6.2 TCPWM_CMD

Description: TCPWM command register.
Address: 0x40200008
Offset: 0x8
Retention: Not Retained
IsDeepSleep: No
Comment: Enables software controlled counter operation.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:5]			COUNTER_CAPTURE [4:0]				

Bits	15	14	13	12	11	10	9	8
Name	None [15:13]			COUNTER_RELOAD [12:8]				

Bits	23	22	21	20	19	18	17	16
Name	None [23:21]			COUNTER_STOP [20:16]				

Bits	31	30	29	28	27	26	25	24
Name	None [31:29]			COUNTER_START [28:24]				

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:4	COUNTER_CAPTURE	RW1S	RW1C	0	Counters SW capture trigger. When written with '1', a capture trigger is generated and the HW sets the field to '0' when the SW trigger has taken effect. It should be noted that the HW operates on the counter frequency. If the counter is disabled through CTRL.COUNTER_ENABLED, the field is immediately set to '0'.
8:12	COUNTER_RELOAD	RW1S	RW1C	0	Counters SW reload trigger. For HW behavior, see COUNTER_CAPTURE field.
16:20	COUNTER_STOP	RW1S	RW1C	0	Counters SW stop trigger. For HW behavior, see COUNTER_CAPTURE field.
24:28	COUNTER_START	RW1S	RW1C	0	Counters SW start trigger. For HW behavior, see COUNTER_CAPTURE field.

21.6.3 TCPWM_INTR_CAUSE

Description: TCPWM Counter interrupt cause register.
Address: 0x4020000C
Offset: 0xC
Retention: Not Retained
IsDeepSleep: No
Comment: Enables software to determine the source of the combined interrupt output signal 'interrupt'. The register fields are not retained. This is to ensure that they come up as '0' after coming out of DeepSleep system power mode.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:5]			COUNTER_INT [4:0]				

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:4	COUNTER_INT	R	W	0	Counters interrupt signal active. If the counter is disabled through CTRL.COUNTER_ENABLED, the associated interrupt field is immediately set to '0'.

21.6.4 CNT

21.6.4.1 TCPWM_CNT_CTRL

Description: Counter control register
Address: 0x40200100
Offset: 0x0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:4]				PWM _STOP_ON _KILL [3:3]	PWM _SYNC_ KILL [2:2]	AUTO _RELOAD _PERIOD [1:1]	AUTO _RELOAD _CC [0:0]

Bits	15	14	13	12	11	10	9	8
Name	GENERIC [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:22]		QUADRATURE_MODE [21:20]		None [19:19]	ONE _SHOT [18:18]	UP_DOWN_MODE [17:16]	

Bits	31	30	29	28	27	26	25	24
Name	None [31:27]					MODE [26:24]		

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	AUTO_RELOAD_CC	RW	R	0	Specifies switching of the CC and buffered CC values. This field has a function in TIMER, PWM, PWM_DT and PWM_PR modes. Timer mode: '0': never switch. '1': switch on a compare match event. PWM, PWM_DT, PWM_PR modes: '0: never switch. '1': switch on a terminal count event with an actively pending switch event.
1	AUTO_RELOAD _PERIOD	RW	R	0	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM, PWM_DT and PWM_PR modes. '0': never switch. '1': switch on a terminal count event with an actively pending switch event.
2	PWM_SYNC_KILL	RW	R	0	Specifies asynchronous/synchronous kill behavior: '1': synchronous kill mode: the kill event disables the 'dt_line_out' and 'dt_line_compl_out' signals till the next terminal count event (synchronous kill). In synchronous kill mode, STOP_EDGE should be RISING_EDGE. '0': asynchronous kill mode: the kill event only disables the 'dt_line_out' and 'dt_line_compl_out' signals when present. In asynchronous kill mode, STOP_EDGE should be NO_EDGE_DET. This field has a function in PWM and PWM_DT modes only. This field is only used when PWM_STOP_ON_KILL is '0'.

Bits	Name	SW	HW	Default or Enum	Description
3	PWM_STOP_ON_KILL	RW	R	0	Specifies whether the counter stops on a kill events: '0': kill event does NOT stop counter. '1': kill event stops counter. This field has a function in PWM, PWM_DT and PWM_PR modes only.
8:15	GENERIC	RW	R	0	Generic 8-bit control field. In PWM_DT mode, this field is used to determine the dead time: amount of dead time cycles in the counter clock domain. In all other modes, the lower 3 bits of this field determine pre-scaling of the selected counter clock.
	DIVBY1			0	Divide by 1 (other-than-PWM_DT mode)
	DIVBY2			1	Divide by 2 (other-than-PWM_DT mode)
	DIVBY4			2	Divide by 4 (other-than-PWM_DT mode)
	DIVBY8			3	Divide by 8 (other-than-PWM_DT mode)
	DIVBY16			4	Divide by 16 (other-than-PWM_DT mode)
	DIVBY32			5	Divide by 32 (other-than-PWM_DT mode)
	DIVBY64			6	Divide by 64 (other-than-PWM_DT mode)
	DIVBY128			7	Divide by 128 (other-than-PWM_DT mode)
16:17	UP_DOWN_MODE	RW	R	0	Determines counter direction.
	COUNT_UP			0	Count up (to PERIOD). An overflow event is generated when the counter reaches PERIOD, and is changed to a different value. A terminal count event is generated when the counter reaches PERIOD, and is changed to a different value.
	COUNT_DOWN			1	Count down (to '0'). An underflow event is generated when the counter reaches '0', and is changed to a different value. A terminal count event is generated when the counter reaches '0', and is changed to a different value.
	COUNT_UPDN1			2	Count up (to PERIOD), then count down (to '0'). An overflow event is generated when the counter reaches PERIOD, and is changed to a different value. An underflow event is generated when the counter reaches '0', and is changed to a different value. A terminal count event is generated when the counter reaches '0', and is changed to a different value.
	COUNT_UPDN2			3	Count up (to PERIOD), then count down (to '0'). An overflow event is generated when the counter reaches PERIOD, and is changed to a different value. An underflow event is generated when the counter reaches '0', and is changed to a different value. A terminal count event is generated when the counter reaches '0', and is changed to a different value AND when the counter reaches PERIOD, and is changed to a different value. (this counter direction can be used for PWM functionality with asymmetrical updates).
18	ONE_SHOT	RW	R	0	When '0', counter runs continuous. When '1', counter is turned off by hardware when a terminal count event is generated.
20:21	QUADRATURE_MODE	RW	R	0	In QUAD mode selects quadrature encoding mode (X1/X2/X4). In PWM, PWM_DT and PWM_PR modes, these two bits can be used to invert 'dt_line_out' and 'dt_line_compl_out'. Inversion is the last step in generation of 'dt_line_out' and 'dt_line_compl_out'; i.e. a disabled output line 'dt_line_out' has the value QUADRATURE_MODE[0] and a disabled output line 'dt_line_compl_out' has the value QUADRATURE_MODE[1].

Bits	Name	SW	HW	Default or Enum	Description
	X1			0	X1 encoding (QUAD mode)
	X2			1	X2 encoding (QUAD mode)
	X4			2	X4 encoding (QUAD mode)
	INV_OUT			1	When bit 0 is '1', QUADRATURE_MODE[0] inverts 'dt_line_out' (PWM/PWM_DT modes)
	INV_COMPL_OUT			2	When bit 1 is '1', QUADRATURE_MODE[1] inverts 'dt_line_compl_out' (PWM/PWM_DT modes)
24:26	MODE	RW	R	0	Counter mode.
	TIMER			0	Timer mode
	CAPTURE			2	Capture mode
	QUAD			3	Quadrature encoding mode
	PWM			4	Pulse width modulation (PWM) mode
	PWM_DT			5	PWM with deadtime insertion mode
	PWM_PR			6	Pseudo random pulse width modulation

21.6.4.2 TCPWM_CNT_STATUS

Description: Counter status register
Address: 0x40200104
Offset: 0x4
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:1]							DOWN [0:0]

Bits	15	14	13	12	11	10	9	8
Name	GENERIC [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	RUNNING [31:31]	None [30:24]						

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	DOWN	R	RW	0	When '0', counter is counting up. When '1', counter is counting down. In QUAD mode, this field indicates the direction of the latest counter change: '0' when last incremented and '1' when last decremented.
8:15	GENERIC	R	RW	0	Generic 8-bit counter field. In PWM_DT mode, this counter is used for dead time insertion. In all other modes, this counter is used for pre-scaling the selected counter clock. PWM_DT mode can NOT use prescaled clock functionality.
31	RUNNING	R	RW	0	When '0', the counter is NOT running. When '1', the counter is running.

21.6.4.3 TCPWM_CNT_COUNTER

Description: Counter count register
Address: 0x40200108
Offset: 0x8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	COUNTER [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	COUNTER [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:15	COUNTER	RW	RW	0	16-bit counter value. It is advised to not write to this field when the counter is running.

21.6.4.4 TCPWM_CNT_CC

Description: Counter compare/capture register
Address: 0x4020010C
Offset: 0xC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xFFFF

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	CC [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	CC [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:15	CC	RW	RW	65535	In CAPTURE mode, captures the counter value. In other modes, compared to counter value.

21.6.4.5 TCPWM_CNT_CC_BUFF

Description: Counter buffered compare/capture register
Address: 0x40200110
Offset: 0x10
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xFFFF

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	CC [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	CC [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:15	CC	RW	RW	65535	Additional buffer for counter CC register.

21.6.4.6 TCPWM_CNT_PERIOD

Description: Counter period register
Address: 0x40200114
Offset: 0x14
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xFFFF

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:15	PERIOD	RW	RW	65535	Period value: upper value of the counter. When the counter should count for n cycles, this field should be set to n-1.

21.6.4.7 TCPWM_CNT_PERIOD_BUFF

Description: Counter buffered period register
Address: 0x40200118
Offset: 0x18
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xFFFF

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:15	PERIOD	RW	RW	65535	Additional buffer for counter PERIOD register.

21.6.4.8 TCPWM_CNT_TR_CTRL0

Description: Counter trigger control register 0
Address: 0x40200120
Offset: 0x20
Retention: Retained
IsDeepSleep: No
Comment: Used to select triggers for specific counter events.
Default: 0x10

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	COUNT_SEL [7:4]				CAPTURE_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
Name	STOP_SEL [15:12]				RELOAD_SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
Name	None [23:20]				START_SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:3	CAPTURE_SEL	RW	R	0	Selects one of the 16 input triggers as a capture trigger. Input trigger 0 is always '0' and input trigger 1 is always '1'. Input trigger 2 is the first external trigger line (tcpwm.tr_in[0]). In the PWM, PWM_DT and PWM_PR modes this trigger is used to switch the values if the compare and period registers with their buffer counterparts.
4:7	COUNT_SEL	RW	R	1	Selects one of the 16 input triggers as a count trigger. In QUAD mode, this is the first phase (phi A). Default setting selects input trigger 1, which is always '1'.
8:11	RELOAD_SEL	RW	R	0	Selects one of the 16 input triggers as a reload trigger. In QUAD mode, this is the index or revolution pulse. In this mode, it will update the counter with the value in the TCPWM_CNTn_PERIOD register.
12:15	STOP_SEL	RW	R	0	Selects one of the 16 input triggers as a stop trigger. In PWM, PWM_DT and PWM_PR modes, this is the kill trigger. In these modes, the kill trigger is used to either temporarily block the PWM outputs (PWM_STOP_ON_KILL is '0') or stop the functionality (PWM_STOP_ON_KILL is '1'). For the PWM and PWM_DT modes, the blocking of the output signals can be asynchronous (STOP_EDGE should be NO_EDGE_DET) in which case the blocking is as long as the trigger is '1' or synchronous (STOP_EDGE should be RISING_EDGE) in which case it extends till the next terminal count event.
16:19	START_SEL	RW	R	0	Selects one of the 16 input triggers as a start trigger. In QUAD mode, this is the second phase (phi B).

21.6.4.9 TCPWM_CNT_TR_CTRL1

Description: Counter trigger control register 1
Address: 0x40200124
Offset: 0x24
Retention: Retained
IsDeepSleep: No
Comment: Used to determine edge detection for specific counter triggers. Events will only take effect on enabled counters.
Default: 0x3FF

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	STOP_EDGE [7:6]		RELOAD_EDGE [5:4]		COUNT_EDGE [3:2]		CAPTURE_EDGE [1:0]	

Bits	15	14	13	12	11	10	9	8
Name	None [15:10]						START_EDGE [9:8]	

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:1	CAPTURE_EDGE	RW	R	3	A capture event will copy the counter value into the CC register.
	RISING_EDGE			0	Rising edge. Any rising edge generates an event.
	FALLING_EDGE			1	Falling edge. Any falling edge generates an event.
	BOTH_EDGES			2	Rising AND falling edge. Any odd amount of edges generates an event.
	NO_EDGE_DET			3	No edge detection, use trigger as is.
2:3	COUNT_EDGE	RW	R	3	A counter event will increase or decrease the counter by '1'.
	RISING_EDGE			0	Rising edge. Any rising edge generates an event.
	FALLING_EDGE			1	Falling edge. Any falling edge generates an event.
	BOTH_EDGES			2	Rising AND falling edge. Any odd amount of edges generates an event.
	NO_EDGE_DET			3	No edge detection, use trigger as is.
4:5	RELOAD_EDGE	RW	R	3	A reload event will initialize the counter. When counting up, the counter is initialized to '0'. When counting down, the counter is initialized with PERIOD.
	RISING_EDGE			0	Rising edge. Any rising edge generates an event.
	FALLING_EDGE			1	Falling edge. Any falling edge generates an event.
	BOTH_EDGES			2	Rising AND falling edge. Any odd amount of edges generates an event.
	NO_EDGE_DET			3	No edge detection, use trigger as is.
6:7	STOP_EDGE	RW	R	3	A stop event, will stop the counter; i.e. it will no longer be running. Stopping will NOT disable the counter.
	RISING_EDGE			0	Rising edge. Any rising edge generates an event.
	FALLING_EDGE			1	Falling edge. Any falling edge generates an event.
	BOTH_EDGES			2	Rising AND falling edge. Any odd amount of edges generates an event.
	NO_EDGE_DET			3	No edge detection, use trigger as is.

Bits	Name	SW	HW	Default or Enum	Description
8:9	START_EDGE	RW	R	3	A start event will start the counter; i.e. the counter will become running. Starting does NOT enable the counter. A start event will not initialize the counter whereas the reload event does.
	RISING_EDGE			0	Rising edge. Any rising edge generates an event.
	FALLING_EDGE			1	Falling edge. Any falling edge generates an event.
	BOTH_EDGES			2	Rising AND falling edge. Any odd amount of edges generates an event.
	NO_EDGE_DET			3	No edge detection, use trigger as is.

21.6.4.10 TCPWM_CNT_TR_CTRL2

Description: Counter trigger control register 2
Address: 0x40200128
Offset: 0x28
Retention: Retained
IsDeepSleep: No
Comment: Used to control counter 'line_out', 'dt_line_out' and 'dt_line_compl_out' output signals.
Default: 0x3F

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:6]		UNDERFLOW_MODE [5:4]		OVERFLOW_MODE [3:2]		CC_MATCH_MODE [1:0]	

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:1	CC_MATCH_MODE	RW	R	3	Determines the effect of a compare match event (COUNTER equals CC register) on the 'line_out' output signals. Note that INVERT is especially useful for center aligned pulse width modulation. To generate a duty cycle of 0 percent, the counter CC register should be set to '0'. For a 100 percent duty cycle, the counter CC register should be set to larger than the counter PERIOD register.
	SET			0	Set to '1'
	CLEAR			1	Set to '0'
	INVERT			2	Invert
	NO_CHANGE			3	No Change
2:3	OVERFLOW_MODE	RW	R	3	Determines the effect of a counter overflow event (COUNTER reaches PERIOD) on the 'line_out' output signals.
	SET			0	Set to '1'
	CLEAR			1	Set to '0'
	INVERT			2	Invert
	NO_CHANGE			3	No Change
4:5	UNDERFLOW_MODE	RW	R	3	Determines the effect of a counter underflow event (COUNTER reaches '0') on the 'line_out' output signals.
	SET			0	Set to '1'
	CLEAR			1	Set to '0'
	INVERT			2	Invert
	NO_CHANGE			3	No Change

21.6.4.11 TCPWM_CNT_INTR

Description: Interrupt request register.
Address: 0x40200130
Offset: 0x30
Retention: Not Retained
IsDeepSleep: No
Comment: The register fields are not retained. This is to ensure that they come up as '0' after coming out of DeepSleep system power mode. HW clears the interrupt causes to '0', when the counter is disabled.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:2]						CC _MATCH [1:1]	TC [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	TC	RW1C	RW1S	0	Terminal count event. Set to '1', when event is detected. Write with '1' to clear bit.
1	CC_MATCH	RW1C	RW1S	0	Counter matches CC register event. Set to '1', when event is detected. Write with '1' to clear bit.

21.6.4.12 TCPWM_CNT_INTR_SET

Description: Interrupt set request register.
Address: 0x40200134
Offset: 0x34
Retention: Not Retained
IsDeepSleep: No
Comment: When read, this register reflects the interrupt request register.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:2]						CC _MATCH [1:1]	TC [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	TC	RW1S	A	0	Write with '1' to set corresponding bit in interrupt request register.
1	CC_MATCH	RW1S	A	0	Write with '1' to set corresponding bit in interrupt request register.

21.6.4.13 TCPWM_CNT_INTR_MASK

Description: Interrupt mask register.
Address: 0x40200138
Offset: 0x38
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:2]						CC _MATCH [1:1]	TC [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	TC	RW	R	0	Mask bit for corresponding bit in interrupt request register.
1	CC_MATCH	RW	R	0	Mask bit for corresponding bit in interrupt request register.

21.6.4.14 TCPWM_CNT_INTR_MASKED

Description: Interrupt masked request register
Address: 0x4020013C
Offset: 0x3C
Retention: Not Retained
IsDeepSleep: No
Comment: When read, this register reflects a bitwise AND between the interrupt request and mask registers.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:2]						CC _MATCH [1:1]	TC [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	TC	R	W	0	Logical and of corresponding request and mask bits.
1	CC_MATCH	R	W	0	Logical and of corresponding request and mask bits.

References

[1] 002-34138: PSOC™ high voltage (HV) mixed signal (MS) MCU architecture reference manual

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Document revision	Date	Description of changes
**	2021-12-03	Initial release
*A	2025-02-28	• New registers have been added. • Fields of registers changed wherever applicable. • Other errata fixes, updates and corrections.
*B	2025-03-31	Updated the title as “PSOC™ 4 high voltage (HV) mixed signal (MS) MCU: PSOC™ 4 HVMS-64K registers”.

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