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Spec No: 001-12946

Spec Title: MOBL(R) CLOCK M300/M600, THREE-PLL PROGRAMMABLE CLOCK GENERATOR FOR PORTABLE APPLICATIONS

Replaced by: None

MoBL® Clock
M300/M600

Three-PLL Programmable Clock Generator for Portable Applications

OBSOLETE

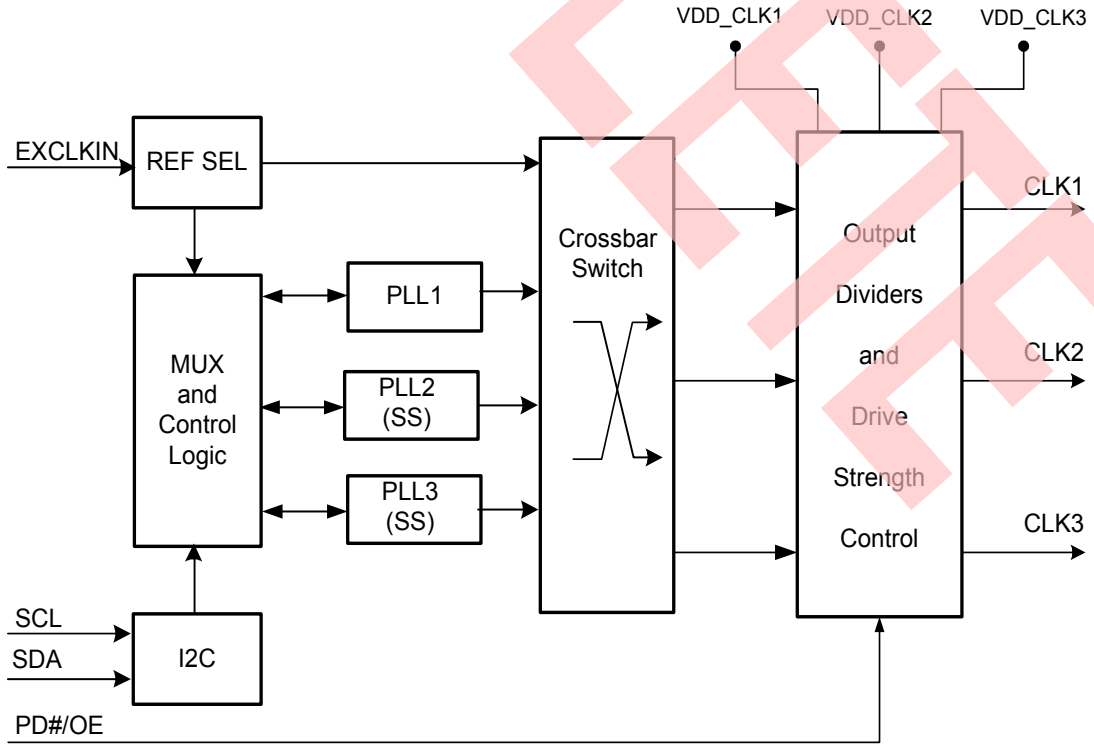
Features

- Device Operating Voltage Options:
  - MoBL Clock M300 Family: 1.8 V
  - MoBL Clock M600 Family: 2.5 V, 3.0 V, or 3.3 V
- Selectable clock output voltages for both MoBL Clock M300 and M600:
  - 1.5 V, 1.8 V, 2.5 V, 3.0 V, or 3.3 V
- Fully integrated ultra low power phase-locked loops (PLLs)
- Input reference clock frequency range: 1–48 MHz
- Output clock frequency range: 3–50 MHz
- Three I²C™ programmable output clocks
- Programmable output drive strengths
- 150 ps typical cycle-to-cycle jitter
- Optional Spread Spectrum for EMI reduction
- 16-pin (3 × 3 × 0.6 mm) QFN Package
- Industrial temperature range

Benefits

- Suitable for cell phone, portable, and consumer electronics applications
- Multiple high-performance PLLs allow synthesis of unrelated frequencies
- Application compatibility in multiple output voltage levels
- Optional Spread Spectrum capable PLLs with Lexmark or Linear profile for maximum EMI reduction
- PLLs can be programmed for system frequency margin tests
- Meets critical timing requirements in complex system designs
- Individually enable or disable each output using I²C
- Ease of output clock selection using programmable crossbar switches

Logic Block Diagram



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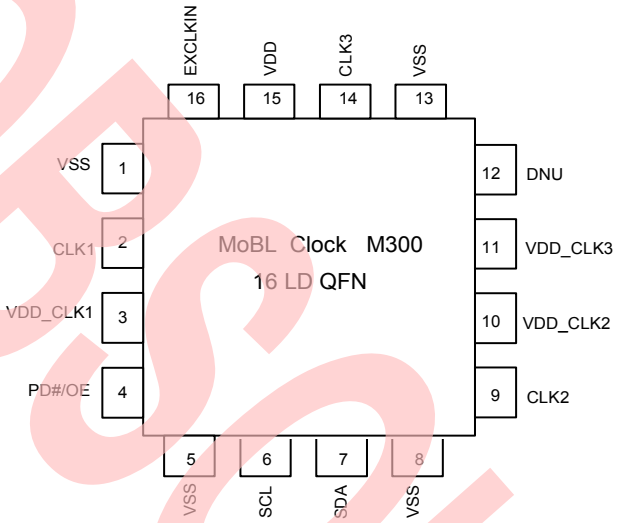
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Pinouts

Figure 1. 16-pin QFN pinout

MoBL Clock M300



Pin Definitions

MoBL Clock M300 Family (V_{DD} = 1.8 V Supply)

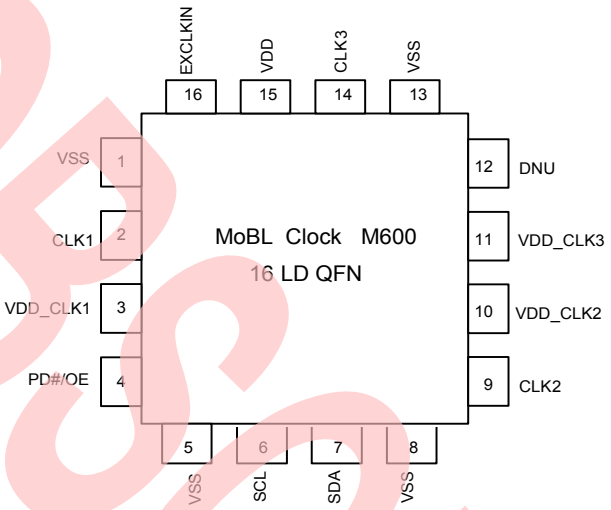
Pin Number	Name	I/O	Description
1	VSS	Power	GND
2	CLK1	Output	Programmable Clock Output. Output voltage depends on VDD_CLK1 voltage
3	VDD_CLK1	Power	Power Supply for output CLK1: 1.5 V/1.8 V/2.5 V/3.0 V/3.3 V
4	PD#/OE	Input	Multifunction Programmable pin: Output Enable or Power Down Modes
5	VSS	Power	GND
6	SCL	Input	I^2C-Bus Clock Line
7	SDA	Input/Output	I^2C-Bus Data Line
8	VSS	Power	GND
9	CLK2	Output	Programmable Clock Output. Output voltage depends on VDD_CLK2 voltage
10	VDD_CLK2	Power	Power Supply for output CLK2: 1.5 V/1.8 V/2.5 V/3.0 V/3.3 V
11	VDD_CLK3	Power	Power Supply for output CLK3: 1.5 V/1.8 V/2.5 V/3.0 V/3.3 V
12	DNU	DNU	Do Not Use this pin
13	VSS	Power	GND
14	CLK3	Output	Programmable Clock Output. Output voltage depends on VDD_CLK3 voltage
15	VDD	Power	Power Supply: 1.8 V
16	EXCLKIN	Input	1.8 V External Reference Clock

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Pinouts

Figure 2. 16-pin QFN pinout

MoBL Clock M600



Pin Definitions

MoBL Clock M600 Family (V_{DD} = 2.5 V, 3.0 V or 3.3 V Supply)

Pin Number	Name	I/O	Description
1	VSS	Power	GND
2	CLK1	Output	Programmable Clock Output. Output voltage depends on VDD_CLK1 voltage
3	VDD_CLK1	Power	Power Supply for output CLK1: 1.5 V/1.8 V/2.5 V/3.0 V/3.3 V
4	PD#/OE	Input	Multifunction Programmable pin: Output Enable or Power Down Modes
5	VSS	Power	GND
6	SCL	Input	I^2C-Bus Clock Line
7	SDA	Input/Output	I^2C-Bus Data Line
8	VSS	Power	GND
9	CLK2	Output	Programmable Clock Output. Output voltage depends on VDD_CLK2 voltage
10	VDD_CLK2	Power	Power Supply for output CLK2: 1.5 V/1.8 V/2.5 V/3.0 V/3.3 V
11	VDD_CLK3	Power	Power Supply for output CLK3: 1.5 V/1.8 V/2.5 V/3.0 V/3.3 V
12	DNU	DNU	Do Not Use this pin
13	VSS	Power	GND
14	CLK3	Output	Programmable Clock Output. Output voltage depends on VDD_CLK3 voltage
15	VDD	Power	Power Supply: 2.5 V/3.0 V/3.3 V
16	EXCLKIN	Input	2.5 V/3.0 V/3.3 V External Reference Clock

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General Description

Three Configurable PLLs

The MoBL® Clock M300/M600 Family of products are three-PLL Clock Generator ICs designed for cell phone, portable, or consumer electronics applications. It can be used to generate three independent output frequencies ranging from 3 to 50 MHz from a single input reference clock.

I²C Programming

The MoBL® Clock M300 and M600 have a serial I²C interface that programs the configuration memory array to synthesize output frequencies by programmable output divider, spread characteristics, and drive strength. I²C can also be used for in-system control of these programmable features.

Input Reference Clocks

The input to the M300 and M600 is designed to use an external reference clock with a frequency range of 1 MHz to 48 MHz at the EXCLKIN pin. The voltage level for the input reference clock used must follow VDD voltage used for the device as shown in the DC and AC specifications.

Output Power Supply Options

There are three clock outputs CLK1, CLK2, and CLK3 driven by three separate output power supplies: VDD_CLK1, VDD_CLK2, and VDD_CLK3 respectively. Different voltage level for each of these power supplies can be used and they can be any of 1.5 V, 1.8 V, 2.5 V, 3.0 V, or 3.3 V giving user multiple choice of output clock voltage levels.

Output Source Selection

These devices have three clock outputs, CLK1, CLK2 and CLK3. There are four available clock sources for these outputs. These clock sources are: PLL1, PLL2, PLL3, or EXCLKIN. Output clock source selection is done using three out of four crossbar switch. Thus, any one of these four available clock sources can be arbitrarily selected for the clock outputs. This gives user a flexibility to have up to three independent clocks and a Reference clock output.

Spread Spectrum Control

Two of the three PLLs (PLL2 and PLL3) have spread spectrum capability for EMI reduction in the system. The device uses a Cypress proprietary PLL and Spread Spectrum Clock (SSC) technology to synthesize and modulate the frequency of the PLL. The spread spectrum feature can be turned on or off by I²C device programming. It can be factory programmed to either center spread range from ±0.125% to ±2.50%, or down spread range from –0.25% to –5.0%, with Lexmark or Linear modulation profile.

PD#/OE Mode

PD#/OE input (Pin 4) can be programmed to operate as either power down (PD#) or output enable (OE) mode. Note that power down shuts off the entire chip, resulting in minimum power consumption for the device. Setting this signal high brings the device in the operational mode with default register settings. The PD# turn-on time is limited by the turn-on time of the PLLs. Disabled outputs are first driven to a low state before turning off. When off, they are held low by internal weak resistors (~160k ohms)

When this pin is programmed as Output Enable (OE), clock outputs can be enabled or disabled using OE (pin 4). Individual clock outputs can be programmed to be sensitive to this OE pin.

Keep Alive Mode

By activating the device in the Keep Alive Mode, power down mode is changed to power saving mode, which disables all PLLs and outputs, but preserves the contents of the volatile registers. Thus, any configuration changes made via the I²C interface are preserved. By deactivating the Keep Alive Mode, I²C memory is not preserved during power down, but power consumption is reduced relative to the Keep Alive Mode.

Output Drive Strength

The DC drive strength of the individual clock output can be programmed for different values. Table 1 shows the typical rise and fall times for different drive strength settings.

Table 1. Output Drive Strength

Output Drive Strength	Rise/Fall Time (ns) (Typical Value)
Low	6.8
Mid Low	3.4
Mid High	2.0
High	1.0

Factory Specific Configuration and Custom Programming

The device is available with Factory Specific programmed frequencies as shown in the Ordering Information page. This factory specific programmed part can be used for the device evaluation purposes. The MoBL® Clock can be custom programmed to any desired frequencies and listed features. For customer specific programming and I²C programmable memory bitmap definitions, please contact local Cypress Field Application Engineer (FAE) or sales representative.

PROFILE

Functional Overview

I²C Serial Interface

To enhance the flexibility and function of the clock synthesizer, a two-signal I²C serial interface is provided. This interface is used to write (and optionally read) control registers that control various device functions such as enabling individual clock output buffers. The registers initialize to their default setting upon power up and therefore, use of this interface is optional. Clock device registers are normally changed upon system initialization. Any data written via I²C is volatile and is not retained when the device is powered down.

The I²C interface uses two signals, SDA and SCL, that operates up to 400 kbits/s in Read or Write mode. The SDA and SCL timing and data transfer sequence is shown in Figure 3 on page 7. The basic Write serial format is as follows:

Start Bit; 7-bit Device Address (DA); R/$\overline{W}$ Bit; Slave Clock Acknowledge (ACK); 8-bit Memory Address (MA); ACK; 8-bit Data; ACK; 8-bit Data in MA+1 if desired; ACK; 8-bit Data in MA+2; ACK; etc. until STOP Bit. The basic serial format is illustrated in Figure 4 on page 7.

Device Address

The device serial interface address is 69H. The device address is combined with a read/write bit as the LSB and is sent after each start bit.

Data Valid

Data is valid when the clock is HIGH, and can only be transitioned when the clock is LOW, as illustrated in Figure 5 on page 7.

Data Frame

Every new data frame is indicated by a start and stop sequence, as illustrated in Figure 6 on page 8.

Start Sequence – SDA going LOW when SCL is HIGH indicates a Start Frame. Every time a start signal is supplied, the next 8-bit data must be the device address (seven bits) and a R/$\overline{W}$ bit, followed by register address (eight bits) and register data (eight bits).

Stop Sequence – SDA going HIGH when SCL is HIGH indicates a Stop Frame. A Stop Frame frees the bus to write to another part on the same bus or to write to another random register address.

Acknowledge Pulse

During Write Mode, the MoBL Clock M300/M600 responds with an Acknowledge pulse after every eight bits. This is done by pulling the SDA line LOW during the N*9th clock cycle, as illustrated in Figure 7 on page 8 (N = the number of bytes transmitted). During Read Mode, the master generates the acknowledge pulse after reading the data packet.

Write Operations

Writing Individual Bytes

A valid write operation must have a full 8-bit register address after the device address word from the master, which is followed by an acknowledge bit from the slave (ack = 0/LOW). The next eight bits must contain the data word intended for storage. After the receiving the data word, the slave responds with another acknowledge bit (ack = 0/LOW), and the master must end the write sequence with a STOP condition.

Writing Multiple Bytes

To write multiple bytes at a time, the master must not end the write sequence with a STOP condition, but instead sends multiple contiguous bytes of data to be stored. After each byte, the slave responds with an acknowledge bit, the same as after the first byte, and accepts data until the acknowledge bit is responded to by the STOP condition. When receiving multiple bytes, the MoBL Clock M300/M600 internally increments the register address.

Read Operations

Read operations are initiated the same way as Write operations except that the R/W bit of the slave address is set to ‘1’ (HIGH). There are three basic read operations: current address read, random read, and sequential read.

Current Address Read

The MoBL Clock M300/M600 have an onboard address counter that retains ‘1’ more than the address of the last word accessed. If the last word written or read was word ‘n’, then a current address read operation returns the value stored in location ‘n+1’. When the MoBL Clock M300/M600 receives the slave address with the R/W bit set to a ‘1’, it issues an acknowledge and transmits the 8-bit word. The master device does not acknowledge the transfer, but generates a STOP condition, which causes the MoBL Clock M300/M600 to stop transmission.

Random Read

Through random read operations, the master may access any memory location. To perform this type of read operation, first set the word address. To do this, send the address to the MoBL Clock M300/M600 as part of a write operation. After the word address is sent, the master generates a START condition following the acknowledge. This terminates the write operation before any data is stored in the address, but not before the internal address pointer is set. Next, the master reissues the control byte with the R/W byte set to ‘1’. The MoBL Clock M300/M600 then issues an acknowledge and transmits the 8-bit word. The master device does not acknowledge the transfer, but generates a STOP condition, which causes the MoBL Clock M300/M600 to stop transmission.

Sequential Read

Sequential read operations follow the same process as random reads except that the master issues an acknowledge instead of a STOP condition after transmission of the first 8-bit data word. This action increments the internal address pointer, and subsequently outputs the next 8-bit data word. By continuing to issue acknowledges instead of STOP conditions, the master serially reads the entire contents of the slave device memory. When the internal address pointer points to the FFH register, after the next increment, the pointer points to the 00H register.

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Figure 3. Data Transfer Sequence on the Serial Bus

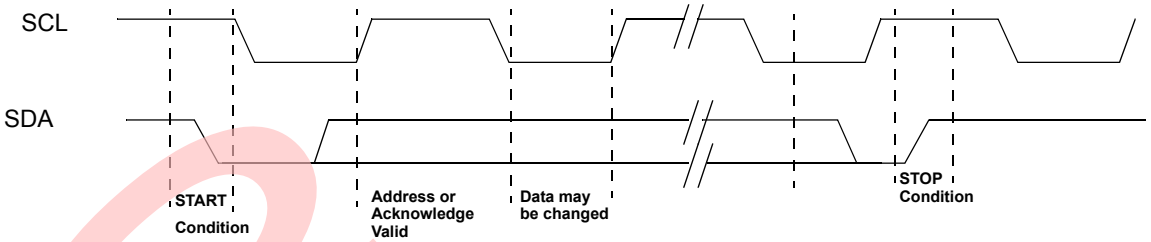


Figure 4. Data Frame Architecture

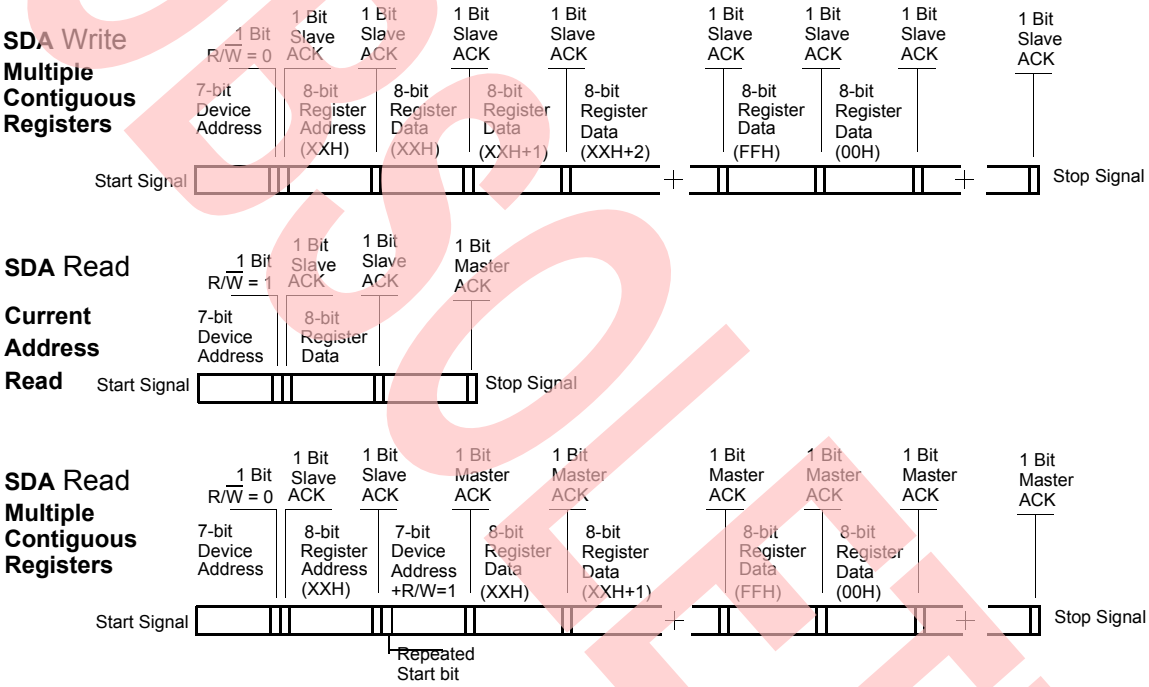
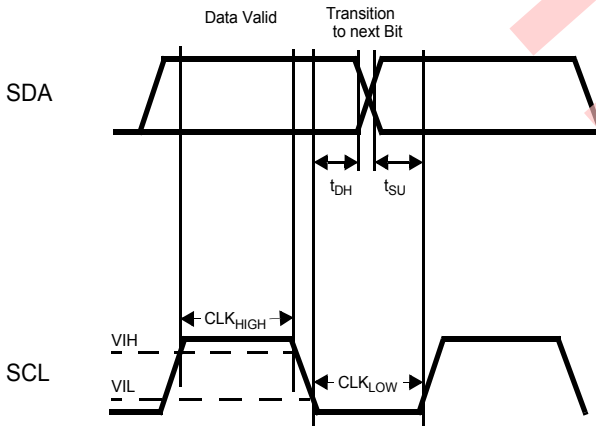


Figure 5. Data Valid and Data Transition Periods



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Serial Programming Interface Timing

Figure 6. Start and Stop Frame

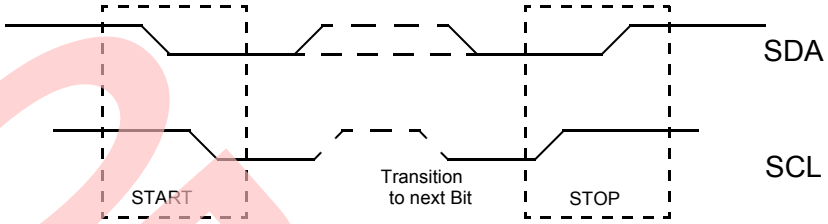
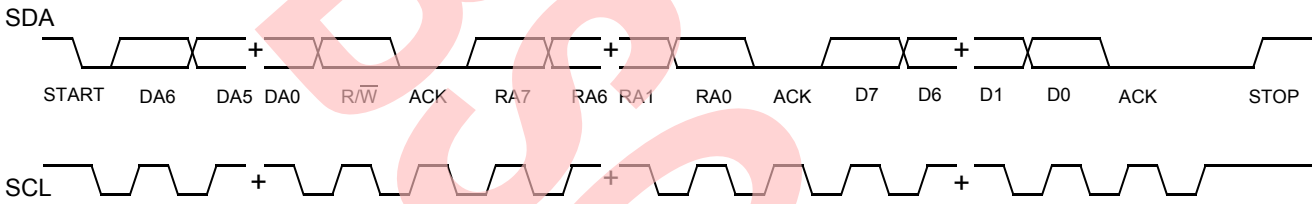


Figure 7. Frame Format (Device Address, R/$\overline{W}$, Register Address, Register Data)



Serial I²C Programming Interface Timing Specifications

Parameter	Description	Min	Max	Unit
f_{SCL}	Frequency of SCL	–	400	kHz
	Start Mode Time from SDA LOW to SCL LOW	0.6	–	µs
CLK_{LOW}	SCL LOW Period	1.3	–	µs
CLK_{HIGH}	SCL HIGH Period	0.6	–	µs
t_{SU}	Data Transition to SCL HIGH	250	–	ns
t_{DH}	Data Hold (SCL LOW to data transition)	0	–	ns
	Rise Time of SCL and SDA	–	300	ns
	Fall Time of SCL and SDA	–	300	ns
	Stop Mode Time from SCL HIGH to SDA HIGH	0.6	–	µs
	Stop Mode to Start Mode	1.3	–	µs

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Absolute Maximum Conditions

Parameter	Description	Condition	Min	Max	Unit
V_{DD}	Supply Voltage for MoBL Clock M6xx		–0.5	4.4	V
V_{DD}	Supply Voltage for MoBL Clock M3xx		–0.5	2.8	V
V_{DD_CLKX}	Supply Voltage for MoBL Clock M3xx/M6xx		–0.5	4.4	V
V_{IN}	Input Voltage for MoBL Clock M6xx	Relative to V_{SS}	–0.5	V_{DD}+0.5	V
V_{IN}	Input Voltage for MoBL Clock M3xx	Relative to V_{SS}	–0.5	2.2	V
T_S	Temperature, Storage	Non Functional	–65	+150	°C
ESD_{HBM}	ESD Protection (Human Body Model)	JEDEC EIA/JESD22-A114-E	2000	–	V
UL-94	Flammability Rating	V-0 @1/8 in.	–	10	ppm
MSL	Moisture Sensitivity Level		3		

Recommended Operating Conditions

The Recommended Operating Conditions table for MoBL Clock M3xx/M6xx family.

Parameter	Description	Min	Typ	Max	Unit
V_{DD}	VDD Operating voltage for MoBL Clock M6xx	2.25	–	3.60	V
V_{DD}	VDD Operating voltage for MoBL Clock M3xx	1.65	1.80	1.95	V
V_{DD_CLKX}	Output Driver Voltage for MoBL Clock M3xx/M6xx	1.43	–	3.60	V
T_{AI}	Industrial Ambient Temperature	–40	–	85	°C
C_{LOAD}	Maximum Load Capacitance	–	–	15	pF
t_{PU}	Power up time for all V_{DD} to reach minimum specified voltage (power ramps must be monotonic)	0.05	–	500	ms

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DC Electrical Specifications

The DC Electrical Spec. table for MoBL Clock M3xx/M6xx family (V_{DD_CLKX} = 1.5 V/1.8 V/2.5 V/3.0 V/3.3 V)

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{OL}	Output Low Voltage, CLK pins	I_{OL} = 2 mA, drive strength = [00]	–	–	0.4	V
		I_{OL} = 3 mA, drive strength = [01]				
		I_{OL} = 7 mA, drive strength = [10]				
		I_{OL} = 12 mA, drive strength = [11]				
V_{OH}	Output High Voltage, CLK pins	I_{OH} = –2 mA, drive strength = [00]	V_{DD_CLKX} – 0.4	–	–	V
		I_{OH} = –3 mA, drive strength = [01]				
		I_{OH} = –7 mA, drive strength = [10]				
		I_{OH} = –12 mA, drive strength = [11]				
V_{OLSD}	Output Low Voltage, SDA	I_{OL} = 4 mA	–	–	0.4	V
V_{IL1}	Input Low Voltage of PD#/OE, SDA and SCL pins		–	–	0.2 × V_{DD}	V
V_{IL2}	Input Low Voltage of EXCLKIN pin		–	–	0.1 × V_{DD}	V
V_{IH1}	Input High Voltage of PD#/OE, SDA and SCL pins		0.8 × V_{DD}	–	–	V
V_{IH2}	Input High Voltage of EXCLKIN for MoBL Clock M6xx		0.9 × V_{DD}	–	–	V
V_{IH3}	Input High Voltage of EXCLKIN pin MoBL Clock M3xx		0.9 × V_{DD}	–	2.2	V
I_{IH}	Input High Current, PD#/OE	V_{IH} = V_{DD}	–	–	10	µA
I_{IL}	Input Low Current, PD#/OE	V_{IL} = 0V	–	–	10	µA
R_{DN}	Pull Down Resistor of clocks (CLK1-CLK3) in off-state	Clock outputs in off-state by setting PD# = Low	100	160	250	kΩ
I_{DD} [1, 2]	Supply Current	All outputs running, C_{LOAD} = 0	–	15	–	mA
I_{DDS} [1]	Standby Current	PD# = Low, and I^2C circuit not in Keep Alive Mode	–	3	–	µA
C_{IN} [2]	Input Capacitance	SCL, SDA, and PD#/OE inputs	–	–	7	pF

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Notes
1. This parameter is configuration dependent. The specified value is for the drive level setting of [1,1].
2. Parameters are guaranteed by design and characterization. Not 100% tested in production. All parameters specified with fully loaded outputs.

AC Electrical Specifications

The AC Electrical Specifications table for M3xx/M6xx (V_{DD_CLKX} = 1.5 V/1.8 V/2.5 V/3.0 V/3.3 V) family.

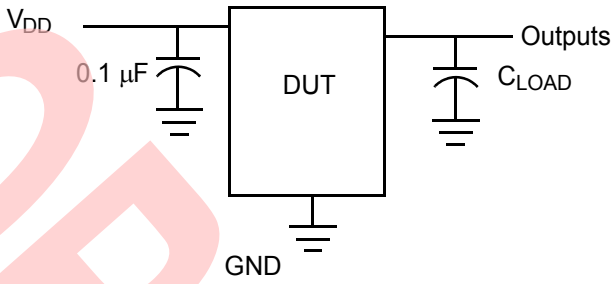
Parameter	Description	Conditions	Min	Typ	Max	Unit
F_{CLK}	Clock Output Frequency	All clock outputs	3	–	50	MHz
F_{REF}	Driven Reference Clock Frequency	EXCLKIN Clock	1	–	48	MHz
DC	Output Clock Duty Cycle	Duty Cycle as defined in Figure 9, t_1/t_2 measured at 50% of V_{DD_CLKX}	45	50	55	%
T_{RF1}[3]	Output Clock Rise/Fall Time	Measured from 20% to 80% of V_{DD_CLKX}, as shown in Figure 10, C_{LOAD} = 15 pF, drive strength = [00]	–	6.8	10.0	ns
T_{RF2}[3]	Output Clock Rise/Fall Time	Measured from 20% to 80% of V_{DD_CLKX}, as shown in Figure 10, C_{LOAD} = 15 pF, drive strength = [01]	–	3.4	5.0	ns
T_{RF3}[3]	Output Clock Rise/Fall Time	Measured from 20% to 80% of V_{DD_CLKX}, as shown in Figure 10, C_{LOAD} = 15 pF, drive strength = [10]	–	2.0	3.0	ns
T_{RF4}[3]	Output Clock Rise/Fall Time	Measured from 20% to 80% of V_{DD_CLKX}, as shown in Figure 10, C_{LOAD} = 15 pF, drive strength = [11]	–	1.0	1.5	ns
T_{CCJ}[3, 4]	Cycle-to-cycle Jitter	EXCLKIN = CLKx = 48 MHz, C_{LOAD} = 15 pF, 3 PLLs and 1 output for each PLL enabled, drive strength = [11]	–	150	–	ps
T_{LOCK}[3]	PLL Lock Time		–	1	3	ms

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Notes
3. Parameters are guaranteed by design and characterization. Not 100% tested in production. All parameters specified with fully loaded outputs.
4. This parameter is configuration dependent. The specified value is for the drive level setting of [1,1].

Test and Measurement Setup

Figure 8. Test and Measurement Setup



Voltage and Timing Definitions

Figure 9. Duty Cycle Definition

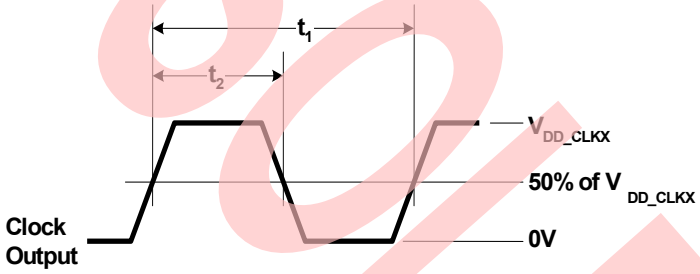
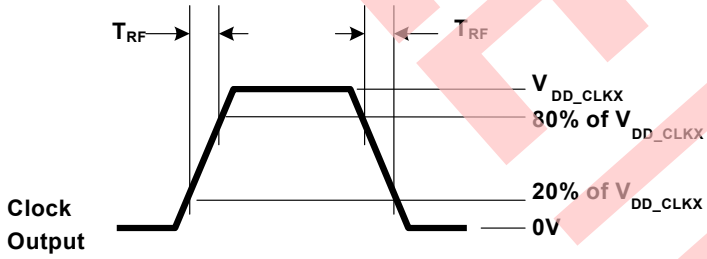


Figure 10. Rise Time = T_{RF}, Fall Time = T_{RF}



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Ordering Information

Part Number [5]	Frequency Configuration	Other Programmable Features	Package	Production Flow
Pb-free				
M300LFXI	Factory Specific Configuration With EXCLKIN = 19.2 MHz CLK1 = 48.0 MHz, CLK2 = 27.0 MHz, CLK3 = 16.9344 MHz	VDD = 1.8 V VDD_CLKx = 1.5/1.8/2.5/3.0/3.3 V Power Down = Enabled Keep Alive = Disabled Spread Spectrum = Disabled Output Drive Strength = [11]	16-pin QFN	Industrial, –40 °C to 85 °C
M300LFXIT	Factory Specific Configuration With EXCLKIN = 19.2 MHz CLK1 = 48.0 MHz, CLK2 = 27.0 MHz, CLK3 = 16.9344 MHz	VDD = 1.8V VDD_CLKx = 1.5/1.8/2.5/3.0/3.3 V Power Down = Enabled Keep Alive = Disabled Spread Spectrum = Disabled Output Drive Strength = [11]	16-pin QFN – Tape & Reel	Industrial, –40 °C to 85 °C
M600LFXI	Factory Specific Configuration With EXCLKIN = 19.2 MHz CLK1 = 48.0 MHz, CLK2 = 27.0 MHz, CLK3 = 16.9344 MHz	VDD = 2.5/3.0/3.3 V VDD_CLKx = 1.5/1.8/2.5/3.0/3.3 V Power Down = Enabled Keep Alive = Disabled Spread Spectrum = Disabled Output Drive Strength = [11]	16-pin QFN	Industrial, –40 °C to 85 °C
M600LFXIT	Factory Specific Configuration With EXCLKIN = 19.2 MHz CLK1 = 48.0 MHz, CLK2 = 27.0 MHz, CLK3 = 16.9344 MHz	VDD = 2.5/3.0/3.3 V VDD_CLKx = 1.5/1.8/2.5/3.0/3.3 V Power Down = Enabled Keep Alive = Disabled Spread Spectrum = Disabled Output Drive Strength = [11]	16-pin QFN – Tape & Reel	Industrial, –40 °C to 85 °C

Some product offerings are factory programmed customer specific devices with customized part numbers. The Possible Configurations table shows the available device types, but not complete part numbers. Contact your local Cypress FAE or Sales Representative for more information.

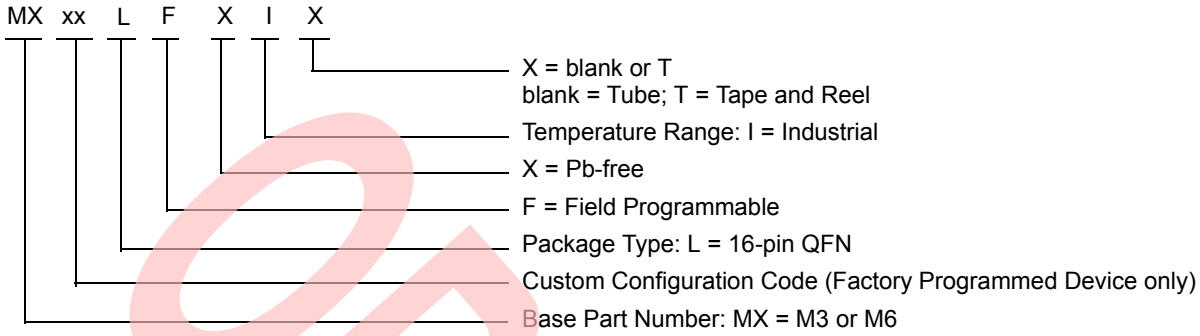
Possible Configurations

Part Number [5]	Frequency Configuration	Other Programmable Features	Package	Production Flow
M3xxLFXI	Customer Specific Configuration	VDD = 1.8 V VDD_CLKx = 1.5/1.8/2.5/3.0/3.3 V	16-pin QFN	Industrial, –40 °C to 85 °C
M3xxLFXIT	Customer Specific Configuration	VDD = 1.8 V VDD_CLKx = 1.5/1.8/2.5/3.0/3.3 V	16-pin QFN-Tape & Reel	Industrial, –40 °C to 85 °C
M6xxLFXI	Customer Specific Configuration	VDD = 2.5/3.0/3.3 V VDD_CLKx = 1.5/1.8/2.5/3.0/3.3 V	16-pin QFN	Industrial, –40 °C to 85 °C
M6xxLFXIT	Customer Specific Configuration	VDD = 2.5/3.0/3.3 V VDD_CLKx = 1.5/1.8/2.5/3.0/3.3 V	16-pin QFN-Tape & Reel	Industrial, –40 °C to 85 °C

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Note
5. xx indicates factory programmed parts based on customer specific configuration. For more details, contact your local Cypress FAE or Sales Representative

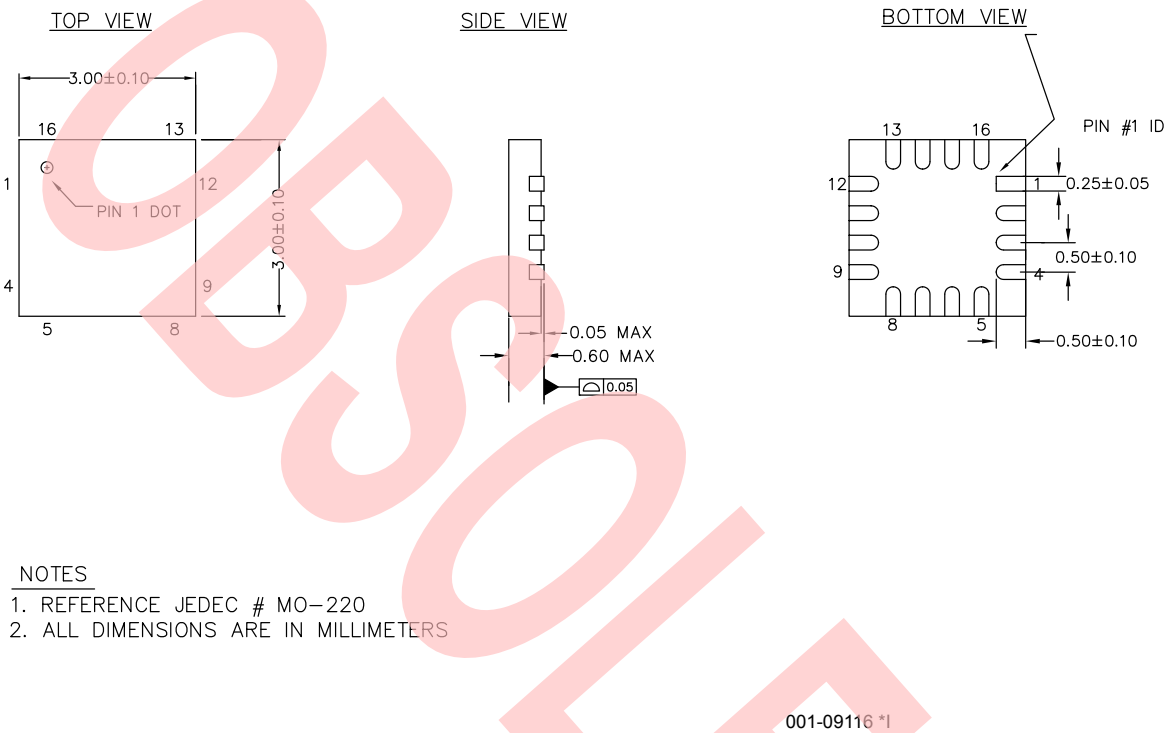
Ordering Code Definitions



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Package Drawing and Dimensions

Figure 11. 16-pin Chip On Lead (3 × 3 × 0.6 mm) LG16A/LD16A (Sawn) Package Outline, 001-09116



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Acronyms

Acronym	Description
EMI	Electromagnetic Interference
ESD	Electrostatic Discharge
EPROM	Erasable Programmable Read Only Memory
FAE	Field Application Engineer
OE	Output Enable
PLL	Phase Locked Loop
QFN	Quad Flat No-lead
SSC	Spread Spectrum Clock

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
kΩ	kilohm
kHz	kilohertz
MHz	megahertz
µA	microampere
µs	microsecond
mA	milliampere
ms	millisecond
ns	nanosecond
Ω	ohm
ppm	parts per million
%	percent
pF	picofarad
ps	picosecond
V	volt

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Document History Page

Document Title: MoBL® Clock M300/M600, Three-PLL Programmable Clock Generator for Portable Applications Document Number: 001-12946				
Rev.	**ECN No.**	**Submission Date**	**Orig. of Change**	**Description of Change**
**	1471544	See ECN	RGL / AESA	New data sheet.
*A	2750166	08/10/2009	TSAI	Post to external web.
*B	2897317	03/22/10	KVM	Updated Ordering Information. No change in part numbers. Added Possible Configurations. Moved 'xx' parts from Ordering Information to Possible Configurations. Updated Package Drawing and Dimensions.
*C	3104150	12/07/2010	BASH	Added Ordering Code Definitions. Added Acronyms and Units of Measure. Minor edits and updated in new template.
*D	4207164	12/02/2013	CINM	Updated Package Drawing and Dimensions: spec 001-09116 – Changed revision from *E to *I. Updated to new template. Completing Sunset Review.
*E	5260248	05/05/2016	PSR	Obsolete document.

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