FM23MLD16

8-Mbit F-RAM Memory

Features

8Mbit Ferroelectric Nonvolatile RAM

- Organized as 512Kx16
- Configurable as 1Mx8 Using /UB, /LB
- High Endurance 100 Trillion (10^{14}) Read/Writes
- NoDelay™ Writes
- Page Mode Operation to 33MHz
- Advanced High-Reliability Ferroelectric Process

SRAM Compatible

- JEDEC 512Kx16 SRAM Pinout
- 60 ns Access Time, 115 ns Cycle Time

Advanced Features

- Low V_{DD} Monitor Protects Memory against Inadvertent Writes

Superior to Battery-backed SRAM Modules

- No Battery Concerns
- Monolithic Reliability
- True Surface Mount Solution, No Rework Steps
- Superior for Moisture, Shock, and Vibration

Low Power Operation

- 2.7V – 3.6V Power Supply
- 14 mA Active Current

Industry Standard Configuration

- Industrial Temperature -40° C to +85° C
- 48-pin “Green”/RoHS FBGA package

Description

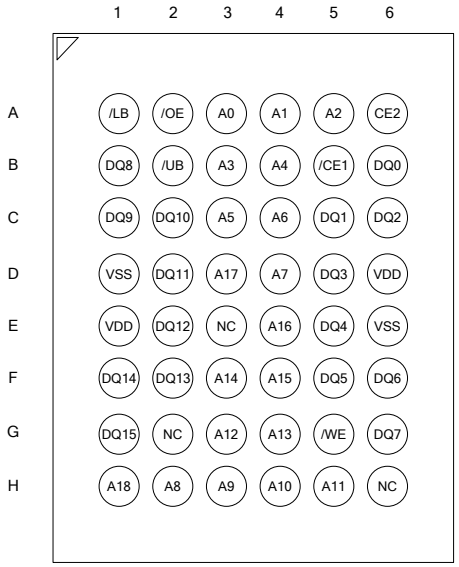
The FM23MLD16 is a 512Kx16 nonvolatile memory that reads and writes like a standard SRAM. A ferroelectric random access memory or F-RAM is nonvolatile, which means that data is retained after power is removed. It provides data retention for over 10 years while eliminating the reliability concerns, functional disadvantages, and system design complexities of battery-backed SRAM (BBSRAM). Fast write timing and very high write endurance make F-RAM superior to other types of memory.

In-system operation of the FM23MLD16 is very similar to other RAM devices and can be used as a drop-in replacement for standard SRAM. Read and write cycles may be triggered by a chip enable or simply by changing the address. The F-RAM memory is nonvolatile due to its unique ferroelectric memory process. These features make the FM23MLD16 ideal for nonvolatile memory applications requiring frequent or rapid writes in the form of an SRAM.

The FM23MLD16 includes a low voltage monitor that blocks access to the memory array when V_{DD} drops below a critical threshold. The memory is protected against an inadvertent access and data corruption under this condition.

The FM23MLD16 F-RAM is available in a 48-ball FBGA surface mount package. Device specifications are guaranteed over the industrial temperature range of –40°C to +85°C.

48-Ball FBGA Top View (Ball Down)



Ordering Information	
FM23MLD16-60-BG	60 ns access, 48-pin “Green”/RoHS FBGA

Not recommended for new designs

This product conforms to specifications per the terms of the Ramtron standard warranty. The product has completed Ramtron’s internal qualification testing and has reached production status.

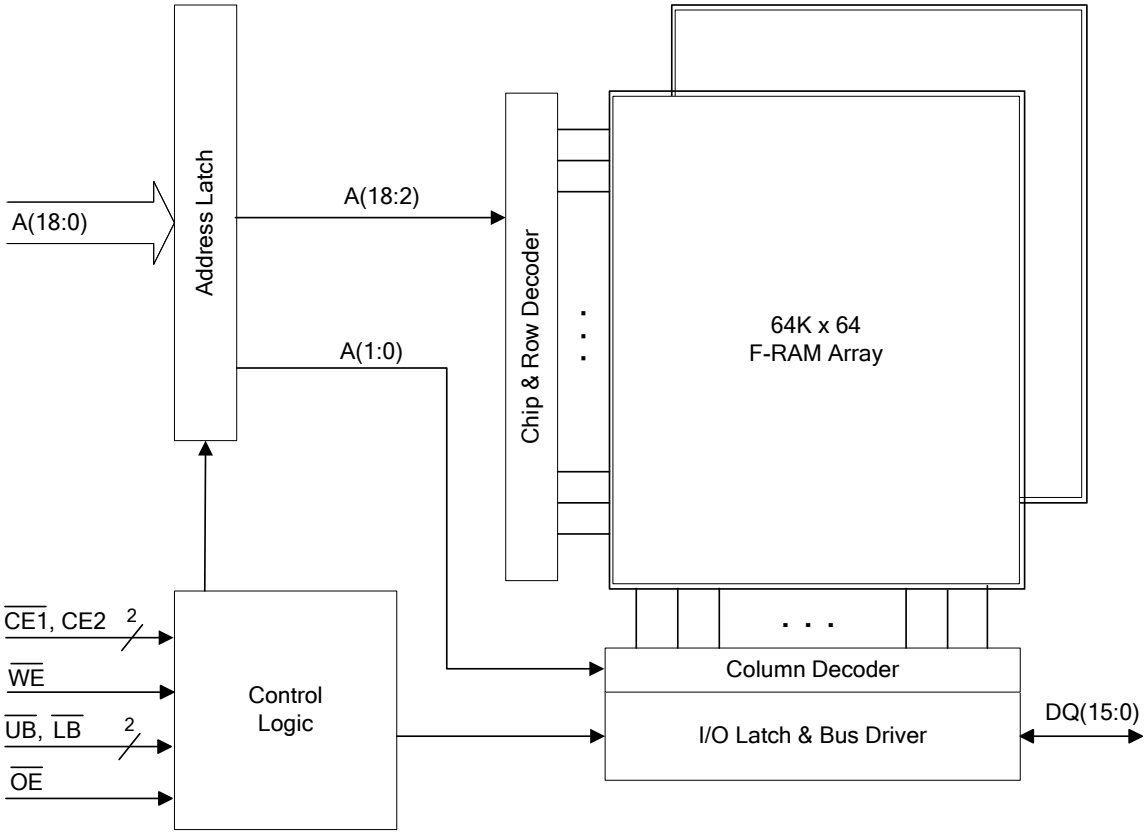


Figure 1. Block Diagram

Pin Description

Pin Name	Type	Pin Description
A(18:0)	Input	Address inputs: The A(17:0) address lines select one of 262,144 words in each of the F-RAM die. A18 selects one of the two die. The lowest two address lines A(1:0) may be used for page mode read and write operations.
/CE1, CE2	Input	Chip Enable inputs: The device is selected and a new memory access begins on the falling edge of /CE1 (while CE2 high) or the rising edge of CE2 (while /CE1 low). The entire address is latched internally at this point.
/WE	Input	Write Enable: A write cycle begins when /WE is asserted. The rising edge causes the FM23MLD16 to write the data on the DQ bus to the F-RAM array. The falling edge of /WE latches a new column address for page mode write cycles.
/OE	Input	Output Enable: When /OE is low, the FM23MLD16 drives the data bus when valid read data is available. Deasserting /OE high tri-states the DQ pins.
DQ(15:0)	I/O	Data: 16-bit bi-directional data bus for accessing the F-RAM array.
/UB	Input	Upper Byte Select: Enables DQ(15:8) pins during reads and writes. These pins are hi-Z if /UB is high.
/LB	Input	Lower Byte Select: Enables DQ(7:0) pins during reads and writes. These pins are hi-Z if /LB is high.
VDD	Supply	Supply Voltage: 3.3V
VSS	Supply	Ground

Not recommended for new designs

Functional Truth Table [1]

/CE1	CE2	/WE	A(18:2)	A(1:0)	Operation
H X	X L	X X	X X	X X	Standby/Idle
↓ L	H ↑	H H	V V	V V	Read
L	H	H	No Change	Change	Page Mode Read
L	H	H	Change	V	Random Read
↓ L	H ↑	L L	V V	V V	/CE-Controlled Write [2]
L	H	↓	V	V	/WE-Controlled Write [2, 3]
L	H	↓	No Change	V	Page Mode Write [4]
↑ L	H ↓	X X	X X	X X	Starts Precharge

Notes:

1) H=Logic High, L=Logic Low, V=Valid Data, X=Don't Care.
2) For write cycles, data-in is latched on the rising edge of /CE1 or /WE of the falling edge of CE2, whichever comes first.
3) /WE-controlled write cycle begins as a Read cycle and A(18:3) is latched then.
4) Addresses A(2:0) must remain stable for at least 15 ns during page mode operation.

Byte Select Truth Table

/OE	/LB	/UB	Operation
H	X	X	Read; Outputs Disabled
X	H	H	
L	H	L	Read; DQ(7:0) Hi-Z
	L	H	Read; DQ(15:8) Hi-Z
	L	L	Read
X	H	L	Write; Mask DQ(7:0)
	L	H	Write; Mask DQ(15:8)
	L	L	Write

Not recommended for new designs

Overview

The FM23MLD16 is a wordwide F-RAM memory logically organized as 524,288 x 16 and accessed using an industry standard parallel interface. All data written to the part is immediately nonvolatile with no delay. The device offers page mode operation which provides higher speed access to addresses within a page (row). An access to a different page is triggered by toggling a chip enable pin or simply by changing the upper address A(18:2).

Memory Operation

Users access 524,288 memory locations, each with 16 data bits through a parallel interface. The F-RAM memory is organized as 2 die each having 64K rows. Each row has 4 column locations, which allows fast access in page mode operation. Once an initial address has been latched by the falling edge of /CE1 (while CE2 high) or the rising edge of CE2 (while /CE1 low), subsequent column locations may be accessed without the need to toggle a chip enable. When either chip enable pin is deasserted, a precharge operation begins. Writes occur immediately at the end of the access with no delay. The /WE pin must be toggled for each write operation. The write data is stored in the nonvolatile memory array immediately, which is a feature unique to F-RAM called NoDelay™ writes.

Read Operation

A read operation begins on the falling edge of /CE1 (while CE2 high) or the rising edge of CE2 (while /CE1 low). The /CE-initiated access causes the address to be latched and starts a memory read cycle if /WE is high. Data becomes available on the bus after the access time has been satisfied. Once the address has been latched and the access completed, a new access to a random location (different row) may begin while both chip enables are still active. The minimum cycle time for random addresses is t_{RC}. Note that unlike SRAMs, the FM23MLD16's /CE-initiated access time is faster than the address cycle time.

The FM23MLD16 will drive the data bus when /OE and at least one of the byte enables (/UB, /LB) is asserted low. The upper data byte is driven when /UB is low, and the lower data byte is driven when /LB is low. If /OE is asserted after the memory access time has been satisfied, the data bus will be driven with valid data. If /OE is asserted prior to completion of the memory access, the data bus will not be driven until valid data is available. This feature minimizes supply current in the system by eliminating transients caused by invalid data being driven onto the bus. When /OE is deasserted high, the data bus will remain in a high-Z state.

Write Operation

Writes occur in the FM23MLD16 in the same time interval as reads. The FM23MLD16 supports both /CE- and /WE-controlled write cycles. In both cases, the address A(18:2) is latched on the falling edge of /CE1 (while CE2 high) or the rising edge of CE2 (while /CE1 low).

In a /CE-controlled write, the /WE signal is asserted prior to beginning the memory cycle. That is, /WE is low when the device is activated with a chip enable. In this case, the device begins the memory cycle as a write. The FM23MLD16 will not drive the data bus regardless of the state of /OE as long as /WE is low. Input data must be valid when the device is deselected with a chip enable. In a /WE-controlled write, the memory cycle begins when the device is activated with a chip enable. The /WE signal falls some time later. Therefore, the memory cycle begins as a read. The data bus will be driven if /OE is low, however it will hi-Z once /WE is asserted low. The /CE- and /WE-controlled write timing cases are shown in the Electrical Specifications section. In the *Write Cycle Timing 2* diagram, the data bus is shown as a hi-Z condition while the chip is write-enabled and before the required setup time. Although this is drawn to look like a mid-level voltage, it is recommended that all DQ pins comply with the minimum V_{IH}/V_{IL} operating levels.

Write access to the array begins on the falling edge of /WE after the memory cycle is initiated. The write access terminates on the deassertion of /WE, /CE1, or CE2, whichever comes first. A valid write operation requires the user to meet the access time specification prior to deasserting /WE, /CE1, or CE2. Data setup time indicates the interval during which data cannot change prior to the end of the write access (rising edge of /WE or the chip is deselected with /CE1 or CE2).

Unlike other truly nonvolatile memory technologies, there is no write delay with F-RAM. Since the read and write access times of the underlying memory are the same, the user experiences no delay through the bus. The entire memory operation occurs in a single bus cycle. Data polling, a technique used with EEPROMs to determine if a write is complete, is unnecessary.

Page Mode Operation

The FM23MLD16 provides the user fast access to any data within a row element. Each row has 4 column address locations. Address inputs A(1:0) define the column address to be accessed. An access can start on any column address, and other column

Not recommended for new designs

locations may be accessed without the need to toggle the CE pins. For fast access reads, once the first data byte is driven onto the bus, the column address inputs A(1:0) may be changed to a new value. A new data byte is then driven to the DQ pins no later than t_{AAP}, which is less than half the initial read access time. For fast access writes, the first write pulse defines the first write access. While the device is selected (both chip enables asserted), a subsequent write pulse along with a new column address provides a page mode write access.

Precharge Operation

The precharge operation is an internal condition in which the state of the memory is being prepared for a new access. Precharge is user-initiated by driving at least one of the chip enable signals to an inactive state. It must remain high for at least the minimum precharge time t_{PC}.

SRAM Drop-In Replacement

The FM23MLD16 has been designed to be a drop-in replacement for standard asynchronous SRAMs. The device does not require the CE pins to toggle for each new address. Both CE pins may remain active indefinitely. When both CE pins are active, the device automatically detects address changes and a new access is begun. This functionality allows the chip enable pins to be tied active (/CE1 grounded, CE2 tied to V_{DD}) as you might with an SRAM. It also allows page mode operation at speeds up to 33MHz.

A typical application is shown in Figure 2. It shows a pullup resistor on /CE1 which will keep the pin high during power cycles assuming the MCU/MPU pin tri-states during the reset condition. The pullup resistor value should be chosen to ensure the /CE1 pin tracks V_{DD} yet a high enough value that the current drawn when /CE1 is low is not an issue. Although not required, it is recommended that CE2 be tied to V_{DD} if the controller provides an active-low chip enable.

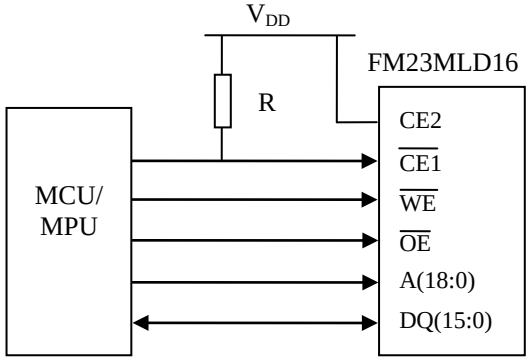


Figure 2. Typical Application using Pullup Resistor on /CE1

For applications that require the lowest power consumption, the /CE1 signal should be active only during memory accesses. The FM23MLD16 draws supply current while /CE1 is low, even if addresses and control signals are static. While /CE1 is high, the device draws no more than the maximum standby current I_{SB}.

Note that if /CE1 is grounded and CE2 tied to V_{DD}, the user must be sure /WE is not low at powerup or powerdown events. If the chip is enabled and /WE is low during power cycles, data corruption will occur. Figure 3 shows a pullup resistor on /WE which will keep the pin high during power cycles assuming the MCU/MPU pin tri-states during the reset condition. The pullup resistor value should be chosen to ensure the /WE pin tracks V_{DD} yet a high enough value that the current drawn when /WE is low is not an issue. A 10Kohm resistor draws 330uA when /WE is low and V_{DD}=3.3V.

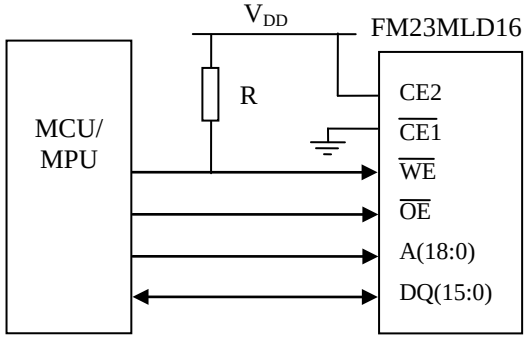


Figure 3. Use of Pullup Resistor on /WE

The /UB and /LB byte select pins are active for both read and write cycles. They may be used to allow the device to be wired as a 1Mx8 memory. The upper and lower data bytes can be tied together and controlled with the byte selects. Individual byte enables or the next higher address line A(19) may be available from the system processor.

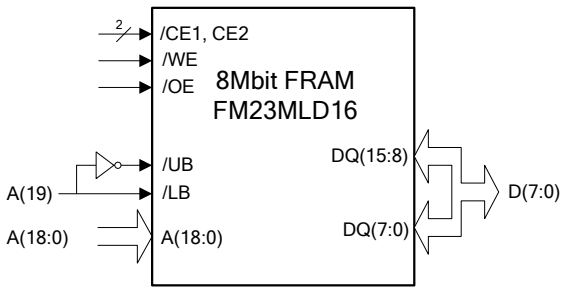


Figure 4. FM23MLD16 Wired as 1Mx8

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PCB Layout Recommendations

A 0.1uF decoupling capacitor should be placed close to each power/ground pair (solder balls 1D/1E and 6D/6E). The ground side of the capacitor should be connected to either a ground plane or low impedance path back to the V_{SS} pins. It is best to use a chip capacitor that has low ESR and has good high frequency characteristics.

If the controller drives the address and chip enable from the same timing edge, it is best to keep the address routes short and of equal length. A simple RC circuit may be inserted in the chip enable path to provide some delay and timing margin for the FM23MLD16's address setup time t_{AS}.

As a general rule, the layout designer may need to add series termination resistors to controller outputs that have fast transitions or routes that are > 15cm in length. This is only necessary if the edge rate is less than or equal to the round trip trace delay. Signal overshoot and ringback may be large enough to cause erratic device behavior. It is best to add a 50 ohm resistor (30 – 60 ohms) near the output driver (controller) to reduce such transmission line effects.

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Electrical Specifications

Absolute Maximum Ratings

Symbol	Description	Ratings
V_{DD}	Power Supply Voltage with respect to V_{SS}	-1.0V to +4.5V
V_{IN}	Voltage on any signal pin with respect to V_{SS}	-1.0V to +4.5V and $V_{IN} < V_{DD}+1V$
T_{STG}	Storage Temperature	-55°C to +125°C
T_{LEAD}	Lead Temperature (Soldering, 10 seconds)	300° C
V_{ESD}	Electrostatic Discharge Voltage - Human Body Model (JEDEC Std JESD22-A114-D) - Charged Device Model (JEDEC Std JESD22-C101-C) - Machine Model (JEDEC Std JESD22-A115-A)	 1.5kV 1.2kV 170V
	Package Moisture Sensitivity Level	MSL-3

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only, and the functional operation of the device at these or any other conditions above those listed in the operational section of this specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

DC Operating Conditions (T_A = -40° C to + 85° C, V_{DD} = 2.7V to 3.6V unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{DD}	Power Supply	2.7	3.3	3.6	V	
I_{DD}	Power Supply Current		9	14	mA	1
I_{SB}	Standby Current @ T_A = 25°C @ T_A = 85°C		 180 -	 300 540	 µA µA	2
V_{TP}	V_{DD} Trip Point to Block Accesses	2.2	-	2.6	V	3
I_{LI}	Input Leakage Current			±1	µA	
I_{LO}	Output Leakage Current			±1	µA	
V_{IH}	Input High Voltage	2.2		V_{DD} + 0.3	V	
V_{IL}	Input Low Voltage	-0.3		0.6	V	
V_{OH1}	Output High Voltage (I_{OH} = -1.0 mA)	2.4			V	
V_{OH2}	Output High Voltage (I_{OH} = -100 µA)	V_{DD}-0.2			V	
V_{OL1}	Output Low Voltage (I_{OL} = 2.1 mA)			0.4	V	
V_{OL2}	Output Low Voltage (I_{OL} = 100 µA)			0.2	V	

Notes

1. V_{DD} = 3.6V, CE pin(s) cycling at min. cycle time. All inputs toggling at CMOS levels (0.2V or V_{DD}-0.2V), all DQ pins unloaded.
2. V_{DD} = 3.6V, /CE1 at V_{DD} or CE2 at V_{SS}, all other pins are static and at CMOS levels (0.2V or V_{DD}-0.2V).
3. If $V_{DD} < V_{TP}$, all memory accesses are blocked regardless of input pin conditions.

Not recommended for new designs

Read Cycle AC Parameters (T_A = -40° C to + 85° C, V_{DD} = 2.7V to 3.6V unless otherwise specified)

Symbol	Parameter	Min	Max	Units	Notes
t_{RC}	Read Cycle Time	115	-	ns	
t_{CE}	Chip Enable Access Time	-	60	ns	
t_{AA}	Address Access Time	-	115	ns	
t_{OH}	Output Hold Time	25	-	ns	
t_{AAP}	Page Mode Address Access Time	-	28	ns	
t_{OHP}	Page Mode Output Hold Time	5	-	ns	
t_{CA}	Chip Enable Active Time	60	-	ns	
t_{PC}	Precharge Time	55	-	ns	
t_{BA}	/UB, /LB Access Time	-	20	ns	
t_{AS}	Address Setup Time (to /CE1, CE2 active)	5	-	ns	
t_{AH}	Address Hold Time (CE-controlled)	60	-	ns	
t_{OE}	Output Enable Access Time	-	15	ns	
t_{HZ}	Chip Enable to Output High-Z	-	10	ns	1
t_{OHZ}	Output Enable High to Output High-Z	-	10	ns	1
t_{BHZ}	/UB, /LB High to Output High-Z	-	10	ns	1

Write Cycle AC Parameters (T_A = -40° C to + 85° C, V_{DD} = 2.7V to 3.6V unless otherwise specified)

Symbol	Parameter	Min	Max	Units	Notes
t_{WC}	Write Cycle Time	115	-	ns	
t_{CA}	Chip Enable Active Time	60	-	ns	
t_{CW}	Chip Enable to Write Enable High	60	-	ns	
t_{PC}	Precharge Time	55	-	ns	
t_{BHZ}	/UB, /LB High to Output High-Z	5		ns	
t_{PWC}	Page Mode Write Enable Cycle Time	25	-	ns	
t_{WP}	Write Enable Pulse Width	16	-	ns	
t_{AS}	Address Setup Time (to /CE1, CE2 active)	5	-	ns	
t_{ASP}	Page Mode Address Setup Time (to /WE low)	8	-	ns	
t_{AHP}	Page Mode Address Hold Time (to /WE low)	15	-	ns	
t_{WLC}	Write Enable Low to Chip Disabled	25	-	ns	
t_{WLA}	Write Enable Low to A(18:2) Change	25	-	ns	
t_{AWH}	A(18:2) Change to Write Enable High	115	-	ns	
t_{DS}	Data Input Setup Time	14	-	ns	
t_{DH}	Data Input Hold Time	5	-	ns	
t_{WZ}	Write Enable Low to Output High Z	-	10	ns	1
t_{WX}	Write Enable High to Output Driven	10	-	ns	1
t_{WS}	Write Enable to /CE Low Setup Time	0	-	ns	2
t_{WH}	Write Enable to /CE High Hold Time	0	-	ns	2

Notes

1 This parameter is guaranteed by design.

2 The relationship between /CE and /WE determines if a /CE- or /WE-controlled write occurs. The parameters t_{WS} and t_{WH} are not tested.

Capacitance (T_A = 25° C , f=1 MHz, V_{DD} = 3.3V)

Symbol	Parameter	Min	Max	Units	Notes
$C_{I/O}$	Input/Output Capacitance (all DQ)	-	16	pF	
C_{IN1}	Input Capacitance (/CE1, CE2, A18)	-	6	pF	
C_{IN2}	Input Capacitance (A17-A0, /WE, /OE, /LB, /UB)	-	12	pF	

Not recommended for new designs

Power Cycle Timing (T_A = -40° C to + 85° C, V_{DD} = 2.7V to 3.6V unless otherwise specified)

Symbol	Parameter	Min	Max	Units	Notes
t_{PU}	Power-Up to First Access Time (after V_{DD} min)	450	-	µs	
t_{PD}	Last Write (/WE high) to Power Down Time (prior to V_{TP})	0	-	µs	
t_{VR}	V_{DD} Rise Time	50	-	µs/V	1,2
t_{VF}	V_{DD} Fall Time	100	-	µs/V	1,2

Notes

1 Slope measured at any point on V_{DD} waveform.

2 Ramtron cannot test or characterize all V_{DD} power ramp profiles. The behavior of the internal circuits is difficult to predict when V_{DD} is below the level of a transistor threshold voltage. Ramtron strongly recommends that V_{DD} power up faster than 100ms through the range of 0.4V to 1.0V.

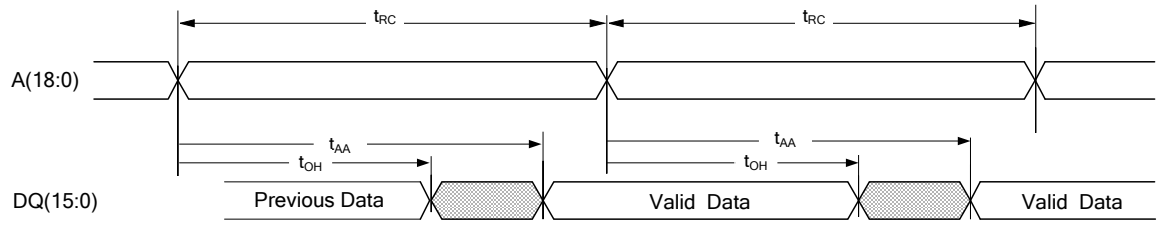
Data Retention (V_{DD} = 2.7V to 3.6V)

Parameter	Min	Units	Notes
Data Retention			
@ +85C	5	Years	
@ +80C	10	Years	
@ +75C	20	Years	

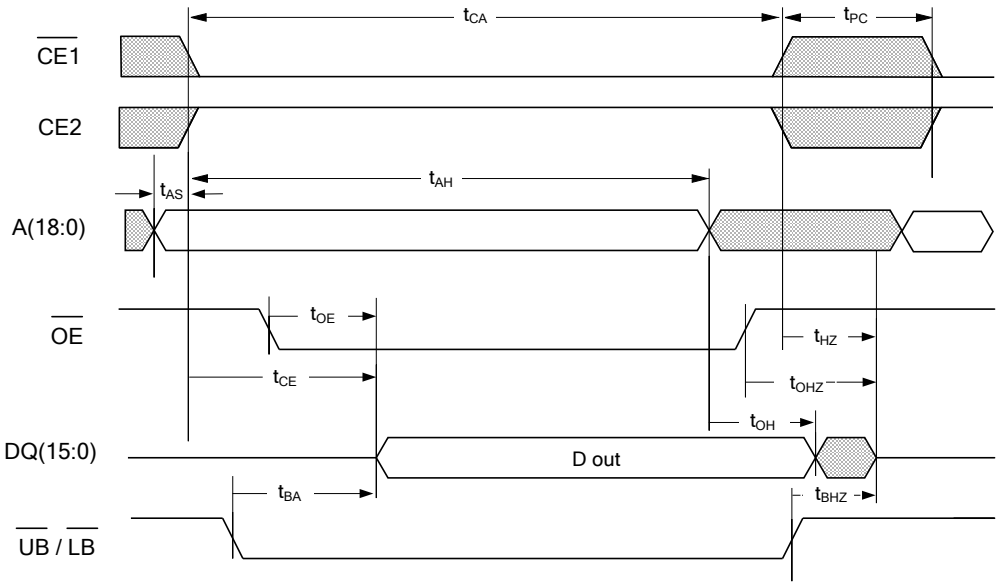
AC Test Conditions

Input Pulse Levels	0 to 3V	Input and Output Timing Levels	1.5V
Input Rise and Fall Times	3 ns	Output Load Capacitance	30pF

Read Cycle Timing 1 (/CE1 low, CE2 high, /OE low)

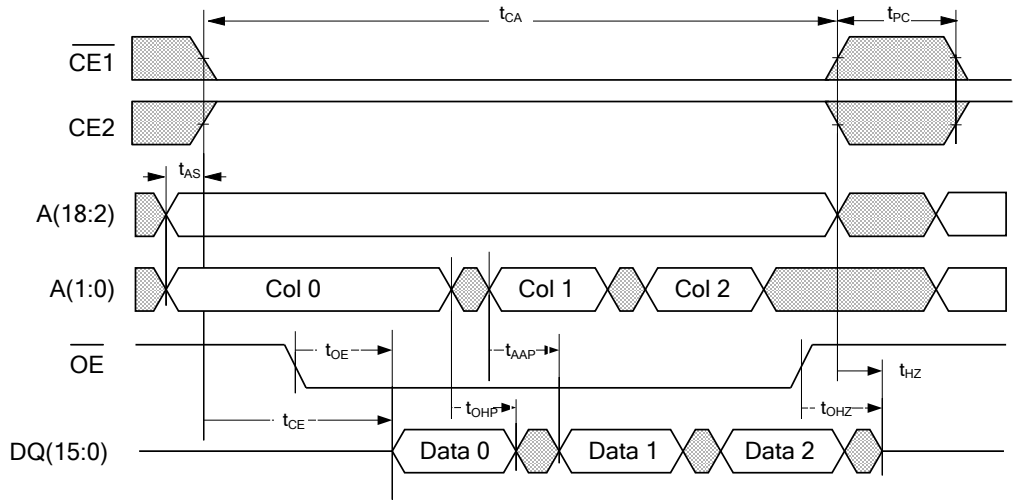


Read Cycle Timing 2 (/CE-controlled)



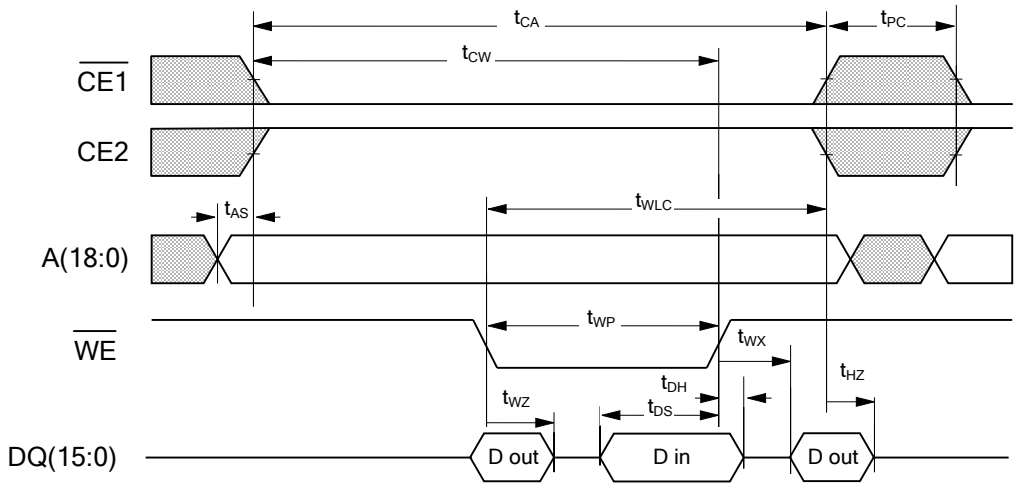
Not recommended for new designs

Page Mode Read Cycle Timing

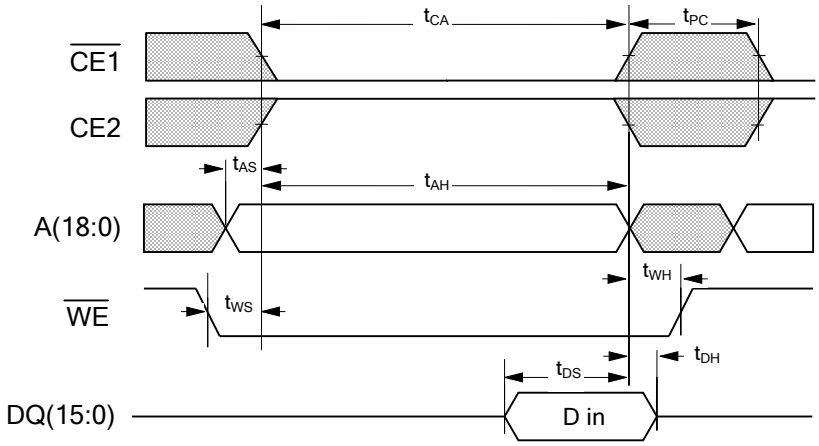


1. Although sequential column addressing is shown, it is not required.

Write Cycle Timing 1 (/WE-Controlled, /OE low)

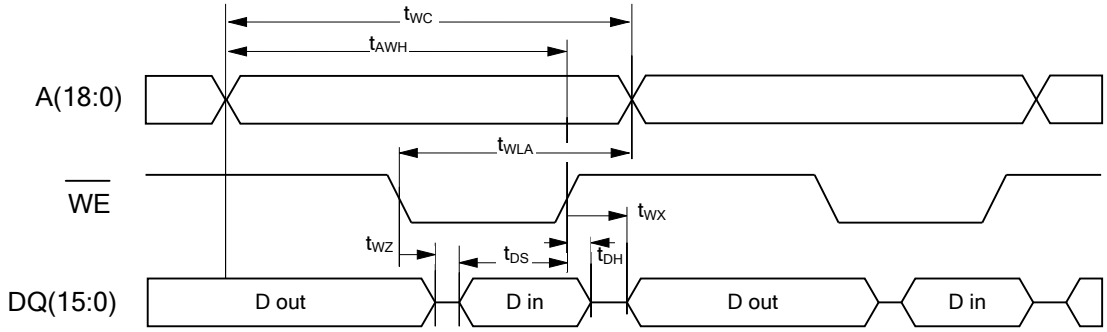


Write Cycle Timing 2 (/CE-Controlled)

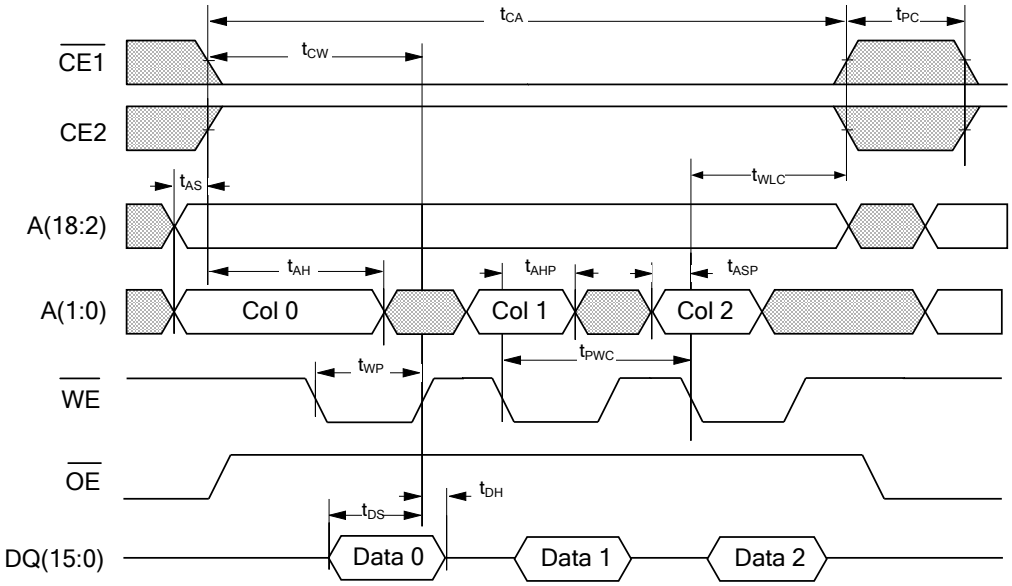


Not recommended for new designs

Write Cycle Timing 3 (/CE1 low, CE2 high)



Page Mode Write Cycle Timing

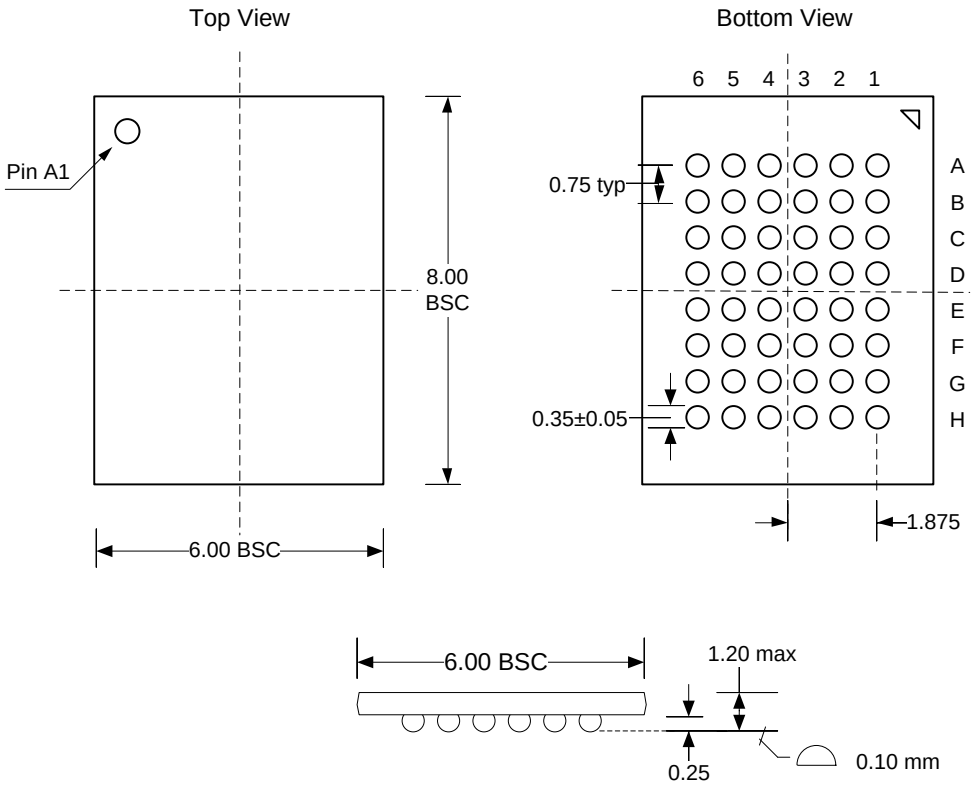


1. Although sequential column addressing is shown, it is not required.

Not recommended for new designs

Mechanical Drawing

48-ball FBGA (0.75mm ball pitch)



Note: All dimensions in millimeters.

48 FBGA Package Marking Scheme

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RAMTRON
XXXXXX-S-P
LLLLLL
YYWW
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Legend:
XXXXXX= part number, S=speed, P=package
LLLLLL= lot code, YY=year, WW=work week

Examples: FM23MLD16, “Green”/RoHS FBGA package,
Lot C8556953BG1, Year 2008, Work Week 44

RAMTRON
FM23MLD16-60-BG
C8556953BG1
0844

Not recommended for new designs

Revision History

Revision	Date	Summary
1.0	12/12/2008	Initial release.
1.1	1/4/2012	Added ESD ratings.
1.2	2/10/2012	Changed timing parameters t_{AS}, t_{AAP}, and t_{DH}. Changed data retention table.
1.3	3/30/2012	Changed package solder ball diameter.
2.0	6/27/2012	Changed to Production status.

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Errata

All errata for this product are fixed effective date code 0920 (YY=09, WW=20). For more information refer to datasheet 001-86212 Rev. *A or contact Cypress Technical Support at http://www.cypress.com/support.

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Document History

Document Title: FM23MLD16, 8-Mbit (512Kx16) F-RAM Memory
Document Number: 001-86212

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	3912932	GVCH	02/25/2013	New Spec
*A	4000965	GVCH	05/15/2013	Added Appendix A - Errata for FM23MLD16
*B	4045491	GVCH	06/30/2013	All errata items are fixed and the errata have been removed.
*C	4191946	GVCH	11/14/2013	Added watermark as “Not recommended for new designs.”

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