SIEMENS

Microcomputer Components

8-Bit CMOS Microcontroller

C509-L

Data Sheet 09.96

SIEMENS

8-Bit CMOS Microcontroller C509-L

Advance Information

- Full upward compatibility with SAB 80C517/80C517A and 8051/C501 microcontrollers
- 256 byte on-chip RAM
- 3K byte of on-chip XRAM
- 256 directly addressable bits
- 375 ns instruction cycle at 16-MHz oscillator frequency
- On-chip emulation support logic (Enhanced Hooks Technology ™)
- External program and data memory expandable up to 64 Kbyte each
- 8-bit A/D converter with 15 multiplexed inputs and built-in self calibration
- Two 16-bit timers/counters (8051 compatible)
- Three 16-bit timers/counters (can be used in combination with the compare/capture unit)
- Powerful compare/capture unit (CCU) with up to 29 high-speed or PWM output channels or 13 capture inputs
- Arithmetic unit for division, multiplication, shift and normalize operations
- Eight datapointers instead of one for indirect addressing of program and external data memory

(further features are on next page)

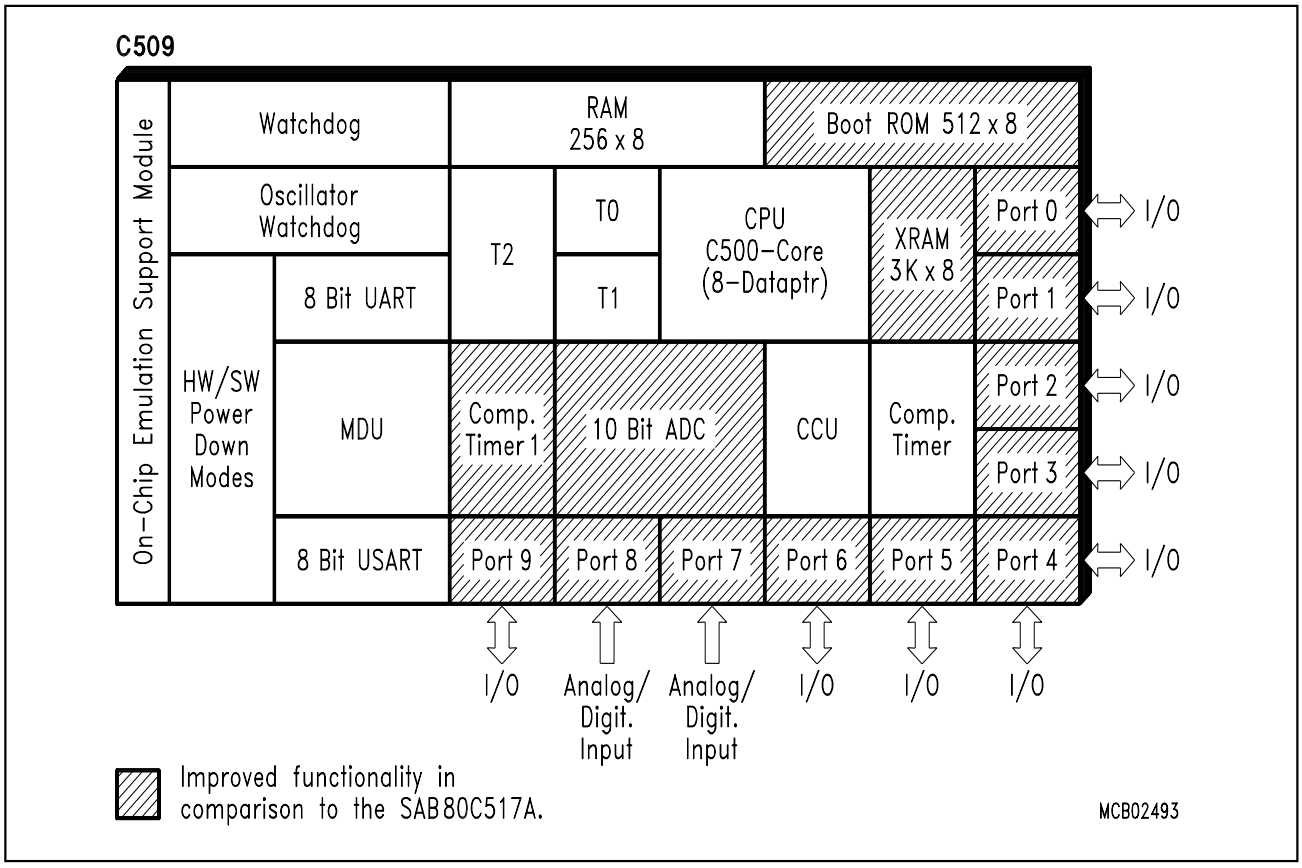


Figure 1
C509-L Functional Units

Features (continued) :

- Extended watchdog facilities
  - 15-bit programmable watchdog timer
  - Oscillator watchdog
- Ten I/O ports
  - Eight bidirectional 8-bit I/O ports with selectable port structure
    quasi-bidirectional port structure (8051 compatible)
    bidirectional port structure with CMOS voltage levels
  - One 8-bit and one 7-bit input port for analog and digital input signals
- Two full-duplex serial interfaces with own baud rate generators
- Four priority level interrupt systems, 19 interrupt vectors
- Three power saving modes
  - Slow-down mode
  - Idle mode
  - Power-down mode
- Siemens high-performance ACMOS technology
- M-QFP-100-2 rectangular quad flat package
- Temperature Ranges : SAB-C509-L T_A = 0 to 70 °C
  SAF-C509-L T_A = -40 to 85 °C

The C509-L is a high-end microcontroller in the Siemens C500 8-bit microcontroller family. It is based on the well-known industry standard 8051 architecture; a great number of enhancements and new peripheral features extend its capabilities to meet the extensive requirements of new applications. Further, the C509-L is a superset of the Siemens SAB 80C517/80C517A 8-bit microcontroller thus offering an easy upgrade path for SAB 80C517/80C517A users.

The high performance of the C509-L microcontroller is achieved by the C500-Core with a maximum operating frequency of 16 MHz internal (and external) CPU clock. While maintaining all the features of the SAB 80C517A, the C509-L is expanded by one I/O port, in its compare/capture capabilities, by A/D converter functions, by additional 1 KByte of on-chip RAM (now 3 KByte XRAM) and by an additional user-selectable CMOS port structure. The C509-L is mounted in a P-MQFP-100-2 package.

Ordering Information

Type	Ordering Code	Package	Description (8-Bit CMOS microcontroller)
SAB-C509-LM	Q67120-C1045	P-MQFP-100-2	for external memory (16 MHz)
SAF-C509-LM	Q67120-C0983	P-MQFP-100-2	for external memory (16 MHz) ext. temp. – 40 ˚C to 85 ˚C

Note: Versions for extended temperature ranges – 40 ˚C to 110 ˚C (SAH-C509-L) and – 40 ˚C to 125 ˚C (SAK-C509-L) are available on request.

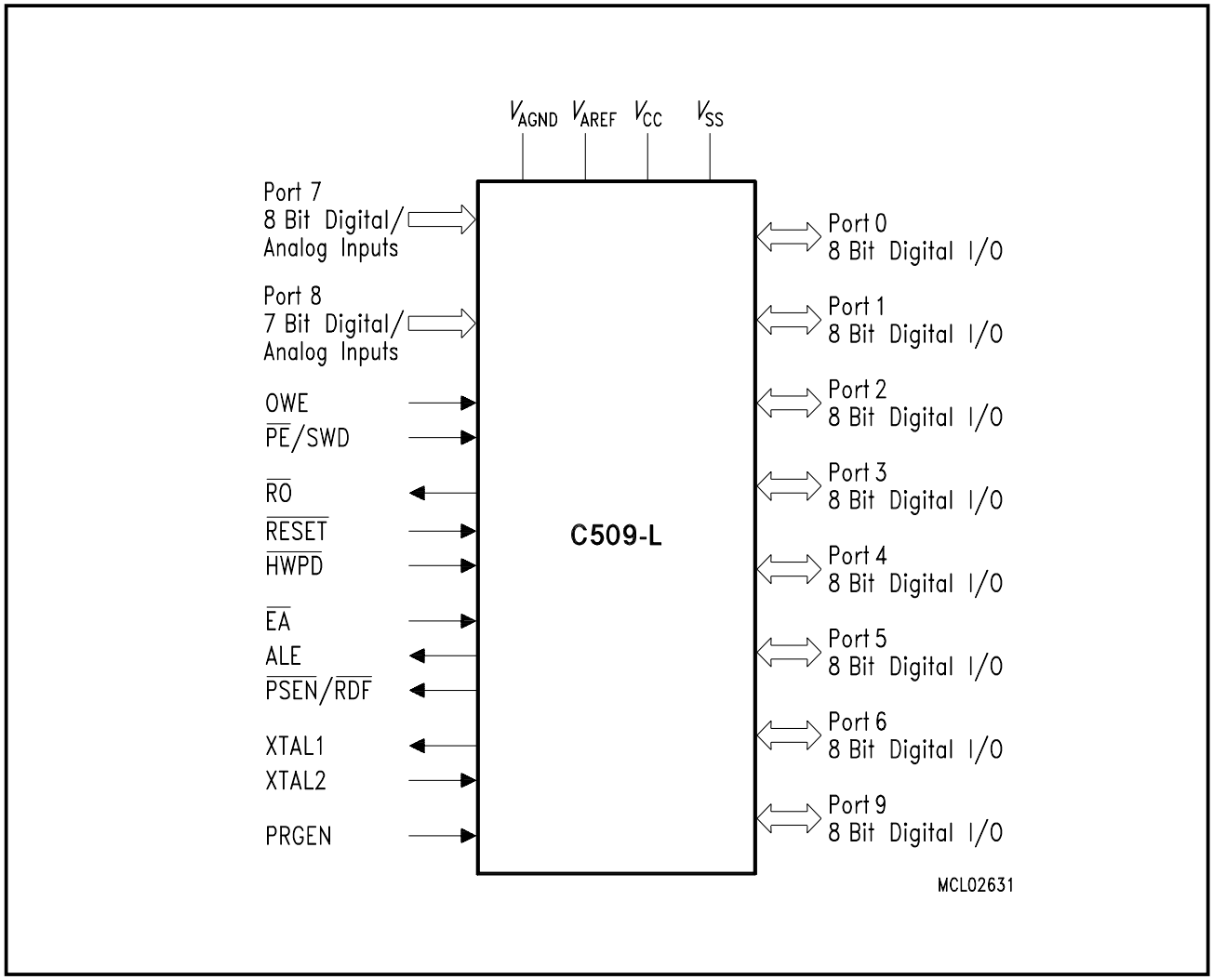


Figure 2
Logic Symbol

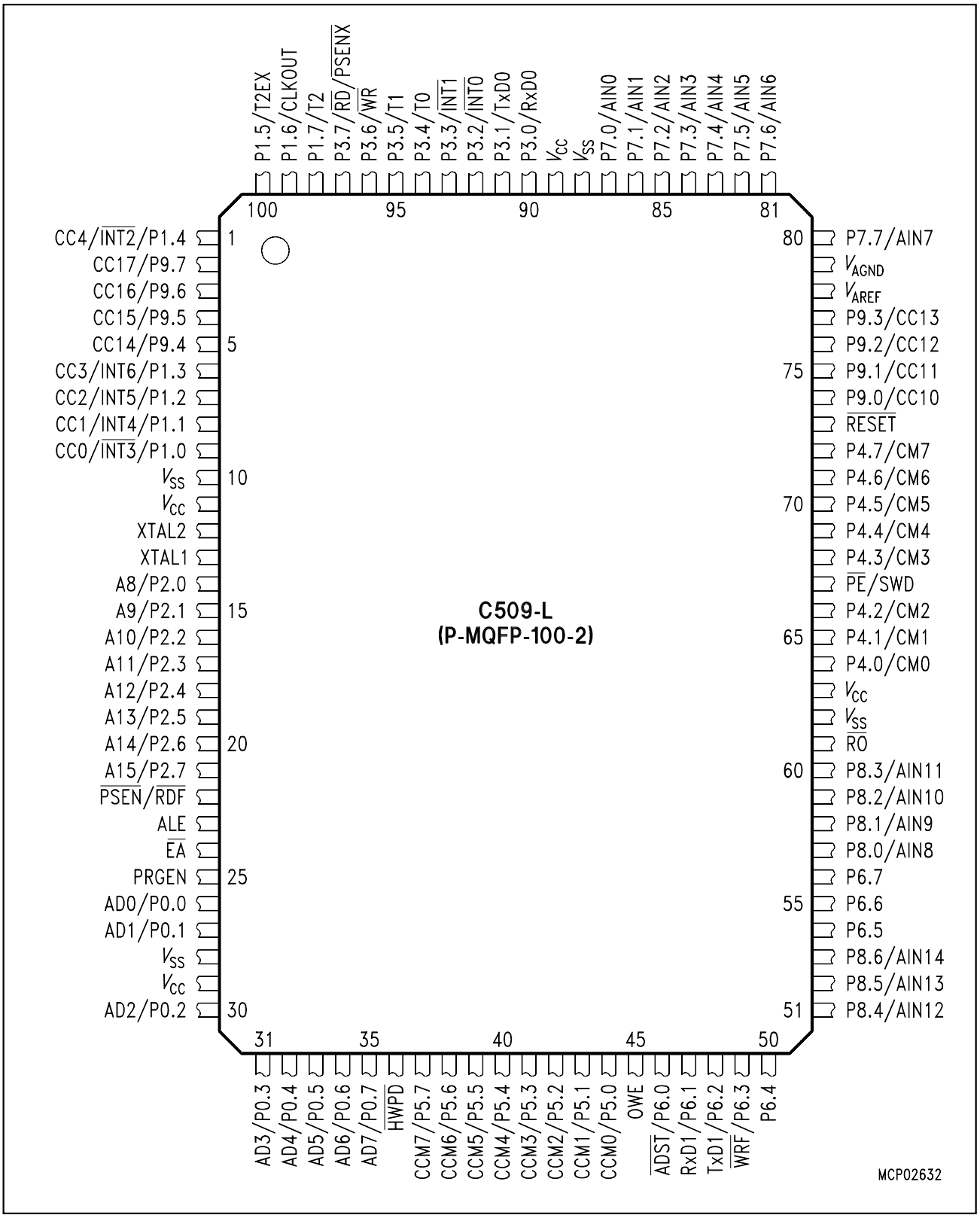


Figure 3
C509-L Pin Configuration (P-MQFP-100-2, Top View)

Table 1
Pin Definitions and Functions

Symbol	Pin Number	I/O*)	Function
P1.0 - P1.7	9-6, 1, 100-98	I/O	**Port 1** is an 8-bit quasi-bidirectional I/O port with internal pullup resistors. Port 1 pins that have 1's written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, port 1 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pullup resistors. Port 1 can also be switched into a bidirectional mode, in which CMOS levels are provided. In this bidirectional mode, each port 1 pin can be programmed individually as input or output. Port 1 also contains the interrupt, timer, clock, capture and compare pins that are used by various options. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate (except when used for the compare functions). The secondary functions are assigned to the pins of port 1 as follows :
	9		P1.0 $\overline{INT3}$ CC0 $\overline{Interrupt\ 3\ input}$ / compare 0 output / capture 0 input
	8		P1.1 INT4 CC1 Interrupt 4 input / compare 1 output / capture 1 input
	7		P1.2 INT5 CC2 Interrupt 5 input / compare 2 output / capture 2 input
	6		P1.3 INT6 CC3 Interrupt 6 input / compare 3 output / capture 3 input
	1		P1.4 $\overline{INT2}$ CC4 $\overline{Interrupt\ 2}$ input / compare 4 output / capture 4 input
	100		P1.5 T2EX Timer 2 external reload trigger input
	99		P1.6 CLKOUT System clock output
	98		P1.7 T2 Counter 2 input

*) I = Input
O = Output

Table 1
Pin Definitions and Functions (cont'd)

Symbol	Pin Number	I/O*)	Function
P9.0 - P9.7	74-77, 5-2	I/O	**Port 9** is an 8-bit quasi-bidirectional I/O port with internal pullup resistors. Port 9 pins that have 1's written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, port 9 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pullup resistors. Port 9 can also be switched into a bidirectional mode, in which CMOS levels are provided. In this bidirectional mode, each port 1 pin can be programmed individually as input or output. Port 9 also serves alternate compare functions. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. The secondary functions are assigned to the pins of port 9 as follows : P9.0-P9.7 CC10-CC17 Compare/capture channel 0-7 output/input
XTAL2	12	–	**XTAL2** is the input to the inverting oscillator amplifier and input to the internal clock generator circuits. When supplying the C509-L with an external clock source, XTAL2 should be driven, while XTAL1 is left unconnected. A duty cycle of 0.4 to 0.6 of the clock signal is required. Minimum and maximum high and low times as well as rise/fall times specified in the AC characteristics must be observed.
XTAL1	13	–	**XTAL1** Output of the inverting oscillator amplifier. This pin is used for the oscillator operation with crystal or ceramic resonartor

*) I = Input
O = Output

Table 1
Pin Definitions and Functions (cont'd)

Symbol	Pin Number	I/O*)	Function
P2.0 – P2.7	14-21	I/O	**Port 2** is a 8-bit I/O port. Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @DPTR). In this application it uses strong internal pullup resistors when issuing 1s. During accesses to external data memory that use 8-bit addresses (MOVX @Ri), port 2 issues the contents of the P2 special function register. P2.0 - P2.7 A8 - A15 Address lines 8 - 15
$\overline{\text{PSEN}}$ / $\overline{\text{RDF}}$	22	O	**$\overline{\text{Program Store Enable}}$ / $\overline{\text{Read FLASH}}$** The $\overline{\text{PSEN}}$ output is a control signal that enables the external program memory to the bus during external code fetch operations. It is activated every third oscillator period. $\overline{\text{PSEN}}$ is not activated during external data memory accesses caused by MOVX instructions. $\overline{\text{PSEN}}$ is not activated when instructions are executed from the internal Boot ROM or from the XRAM. In external programming mode $\overline{\text{RDF}}$ becomes active when executing external data memory read (MOVX) instructions.
ALE	23	O	**Address Latch Enable** This output is used for latching the low byte of the address into external memory during normal operation. It is activated every third oscillator period except during an external data memory access caused by MOVX instructions.
$\overline{\text{EA}}$	24	I	**$\overline{\text{External Access Enable}}$** The status of this pin is latched at the end of a reset. When held at low level, the C509-L fetches all instructions from the external program memory. For the C509-L this pin must be tied low.
PRGEN	25	I	**External Flash-EPROM Program Enable** A low level at this pin disables the programming of an external Flash-EPROM. To enable the programming of an external Flash-EPROM, the pin PRGEN must be held at high level and bit PRGEN1 in SFR SYSCON1 has to be set. There is no internal pullup resistor connected to this pin.

*) I = Input
O = Output

Table 1
Pin Definitions and Functions (cont'd)

Symbol	Pin Number	I/O*)	Function
P0.0 – P0.7	26, 27, 30-35	I/O	**Port 0** is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1s written to them float, and in that state can be used as high-impendance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program or data memory. In this operating mode it uses strong internal pullup resistors when issuing 1 s. P0.0 - P0.7 AD0-AD7 Address/data lines 0 - 7
$\overline{\text{HWPD}}$	36	I	**$\overline{\text{Hardware Power Down}}$** A low level on this pin for the duration of one machine cycle while the oscillator is running resets the C509-L. A low level for a longer period will force the part to power down mode with the pins floating. There is no internal pullup resistor connected to this pin.
P5.0 - P5.7	44-37	I/O	**Port 5** is an 8-bit quasi-bidirectional I/O port with internal pullup resistors. Port 5 pins that have 1's written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, port 5 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pullup resistors. Port 5 can also be switched into a bidirectional mode, in which CMOS levels are provided. In this bidirectional mode, each port 5 pin can be programmed individually as input or output. Port 5 also serves as alternate function for "Concurrent Compare" and "Set/Reset compare" functions. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. The secondary functions are assigned to the pins of port 5 as follows : P5.0 - P5.7 CCM0-CCM7 Concurrent Compare or Set/Reset lines 0 - 7

*) I = Input
O = Output

Table 1
Pin Definitions and Functions (cont'd)

Symbol	Pin Number	I/O*)	Function
OWE	45	I	**Oscillator Watchdog Enable** A high level on this pin enables the oscillator watchdog. When left unconnected, this pin is pulled high by a weak internal pullup resistor. The logic level at OWE should not be changed during normal operation. When held at low level the oscillator watchdog function is turned off. During hardware power down the pullup resistor is switched off.
P6.0 - P6.7	46-50, 54-56	I/O	**Port 6** is an 8-bit quasi-bidirectional I/O port with internal pullup resistors. Port 6 pins that have 1's written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, port 6 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pullup resistors. Port 6 can also be switched into a bidirectional mode, in which CMOS levels are provided. In this bidirectional mode, each port 6 pin can be programmed individually as input or output. Port 6 also contains the external A/D converter control pin, the receive and transmission lines for the serial port 1, and the write-FLASH control signal. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. The secondary functions are assigned to the pins of port 6 as follows : P6.0 $\overline{\text{ADST}}$ External A/D converter start pin P6.1 R×D1 Receiver data input of serial interface 1 P6.2 T×D1 Transmitter data output of serial interface 1 P6.3 $\overline{\text{WRF}}$ The $\overline{\text{WRF}}$ (write Flash) signal is active when the programming mode is selected. In this mode $\overline{\text{WRF}}$ becomes active when executing external data memory write (MOVX) instructions.
	46		
	47		
	48		
	49		

*) I = Input
O = Output

Table 1
Pin Definitions and Functions (cont'd)

Symbol	Pin Number	I/O*)	Function
P8.0 - P8.6	57-60, 51-53	I	**Port 8** is a 7-bit unidirectional input port. Port pins can be used for digital input if voltage levels meet the specified input high/low voltages, and for the higher 7-bit of the multiplexed analog inputs of the A/D converter simultaneously. P8.0 - P8.6 AIN8 - AIN14 Analog input 8 - 14
$\overline{RO}$	61	O	**$\overline{\text{Reset Output}}$** This pin outputs the internally synchronized reset request signal. This signal may be generated by an external hardware reset, a watchdog timer reset or an oscillator watchdog reset. The $\overline{RO}$ output is active low.
P4.0 – P4.7	64-66, 68-72	I/O	**Port 4** is an 8-bit quasi-bidirectional I/O port with internal pull-up resistors. Port 4 pins that have 1's written to them are pulled high by the internal pull-up resistors, and in that state can be used as inputs. As inputs, port 4 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pull-up resistors. Port 4 also erves as alternate compare functions. The output latch corresponding to a secondary functionmust be programmed to a one (1) for that function to operate. The secondary functions are assigned to the pins of port 4 as follows : P4.0 - P4.7 CM0 - CM7 Compare channel 0 - 7
$\overline{PE}$ / SWD	67	I	**$\overline{\text{Power Saving Modes Enable}}$ / Start Watchdog Timer** A low level on this pin allows the software to enter the power down mode, idle and slow down mode. If the low level is also seen during reset, the watchdog timer function is off on default. Usage of the software controlled power saving modes is blocked, when this pin is held on high level. A high level during reset performs an automatic start of the watchdog timer immediately after reset. When left unconnected this pin is pulled high by a weak internal pullup resistor. During hardware power down the pullup resistor is switched off.

*) I = Input
O = Output

Table 1
Pin Definitions and Functions (cont'd)

Symbol	Pin Number	I/O*)	Function
$\overline{\text{RESET}}$	73	I	**$\overline{\text{RESET}}$** A low level on this pin for the duration of one machine cycle while the oscillator is running resets the C509-L. A small internal pullup resistor permits power-on reset using only a capacitor connected to V_{SS}.
V_{AREF}	78	–	**Reference voltage** for the A/D converter
V_{AGND}	79	–	**Reference ground** for the A/D converter
P7.0 - P7.7	87-80	I	**Port 7** Port 7 is an 8-bit unidirectional input port. Port pins can be used for digital input if voltage levels meet the specified input high/low voltages, and for the lower 8-bit of the multiplexed analog inputs of the A/D converter simultaneously. P7.0 - P7.7 AIN0 - AIN7 Analog input 0 - 7

*) I = Input
O = Output

Table 1
Pin Definitions and Functions (cont'd)

Symbol	Pin Number	I/O*)	Function
P3.0 – P3.7	90-97	I/O	**Port 3** is an 8-bit quasi-bidirectional I/O port with internal pullup resistors. Port 3 pins that have 1's written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, port 3 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pullup resistors. Port 3 also contains two external interrupt inputs, the timer 0/1 inputs, the serial port 0 receive/transmit line and the external memory strobe pins. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. The secondary functions are assigned to the port pins of port 3 as follows
	90		P3.0 RxD0 Receiver data input (asynchronous) or data input/output (synchronous) of serial interface 0
	91		P3.1 TxD0 Transmitter data output (asynchronous) or clock output (synchronous) of the serial interface 0
	92		P3.2 $\overline{INT0}$ $\overline{Interrupt\ 0\ input}$ / timer 0 gate control
	93		P3.3 $\overline{INT1}$ $\overline{Interrupt\ 1\ input}$ / timer 1 gate control
	94		P3.4 T0 Counter 0 input
	95		P3.5 T1 Counter 1 input
	96		P3.6 $\overline{WR}$ The write control signal latches the data byte from port 0 into the external data memory
	97		P3.7 $\overline{RD}$ / The read control signal enables the external data memory to port 0
			$\overline{PSENX}$ $\overline{PSENX}$ (external program store enable) enables the external code memory when the external / internal XRAM mode or external / internal programming mode is selected.
V_{SS}	10, 28, 62, 88	–	**Circuit ground potential**
V_{CC}	11, 29, 63, 89	–	**Supply terminal** for all operating modes

*) I = Input
O = Output

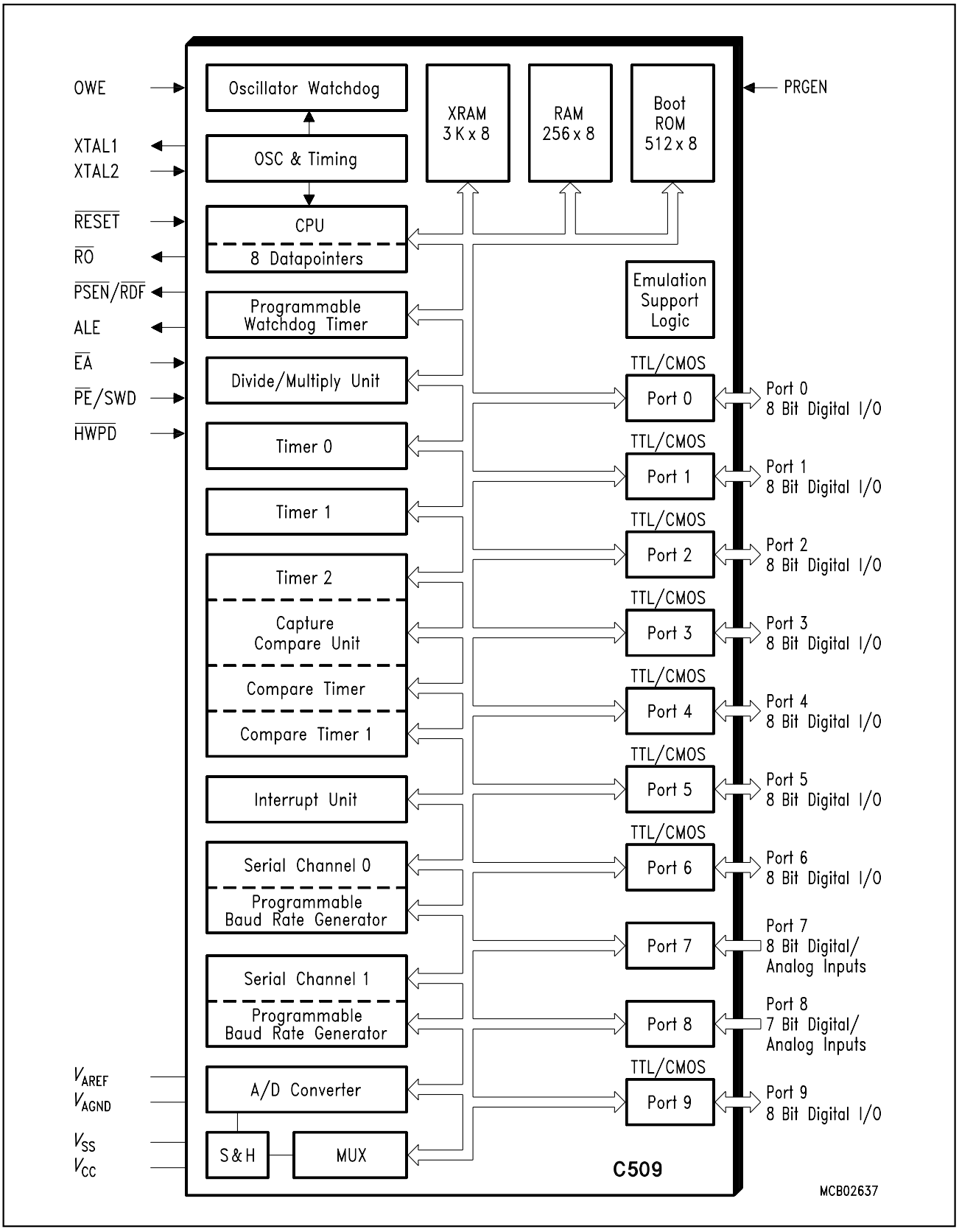


Figure 4
Block Diagram of the C509-L

CPU

The C509-L is efficient both as a controller and as an arithmetic processor. It has extensive facilities for binary and BCD arithmetic and excels in its bit-handling capabilities. Efficient use of program memory results from an instruction set consisting of 44 % one-byte, 41 % two-byte, and 15% three-byte instructions. With a 6 MHz crystal, 58% of the instructions are executed in 1.0µs (12 MHz: 500 ns, 16 MHz : 375 ns).

Special Function Register PSW (Address $D0_H$) **Reset Value : 00_H**

Bit No.	MSB							LSB	
	$D7_H$	$D6_H$	$D5_H$	$D4_H$	$D3_H$	$D2_H$	$D1_H$	$D0_H$	
$D0_H$	CY	AC	F0	RS1	RS0	OV	F1	P	PSW

Bit	Function
CY	Carry Flag Used by arithmetic instruction.
AC	Auxiliary Carry Flag Used by instructions which execute BCD operations.
F0	General Purpose Flag
RS1 RS0	Register Bank select control bits These bits are used to select one of the four register banks.

RS1	RS0	Function
0	0	Bank 0 selected, data address 00_H-07_H
0	1	Bank 1 selected, data address 08_H-$0F_H$
1	0	Bank 2 selected, data address 10_H-17_H
1	1	Bank 3 selected, data address 18_H-$1F_H$

OV	Overflow Flag Used by arithmetic instruction.
F1	General Purpose Flag
P	Parity Flag Set/cleared by hardware after each instruction to indicate an odd/even number of "one" bits in the accumulator, i.e. even parity.

Memory Organization

The C509-L CPU manipulates data and operands in the following five address spaces:

- up to 64 Kbyte of external program memory
- up to 64 Kbyte of external data memory
- 512 byte of internal Boot ROM (program memory)
- 256 bytes of internal data memory
- 3 Kbyte of external XRAM data memory
- a 128 byte special function register area

Figure 5 illustrates the memory address spaces of the C509-L.

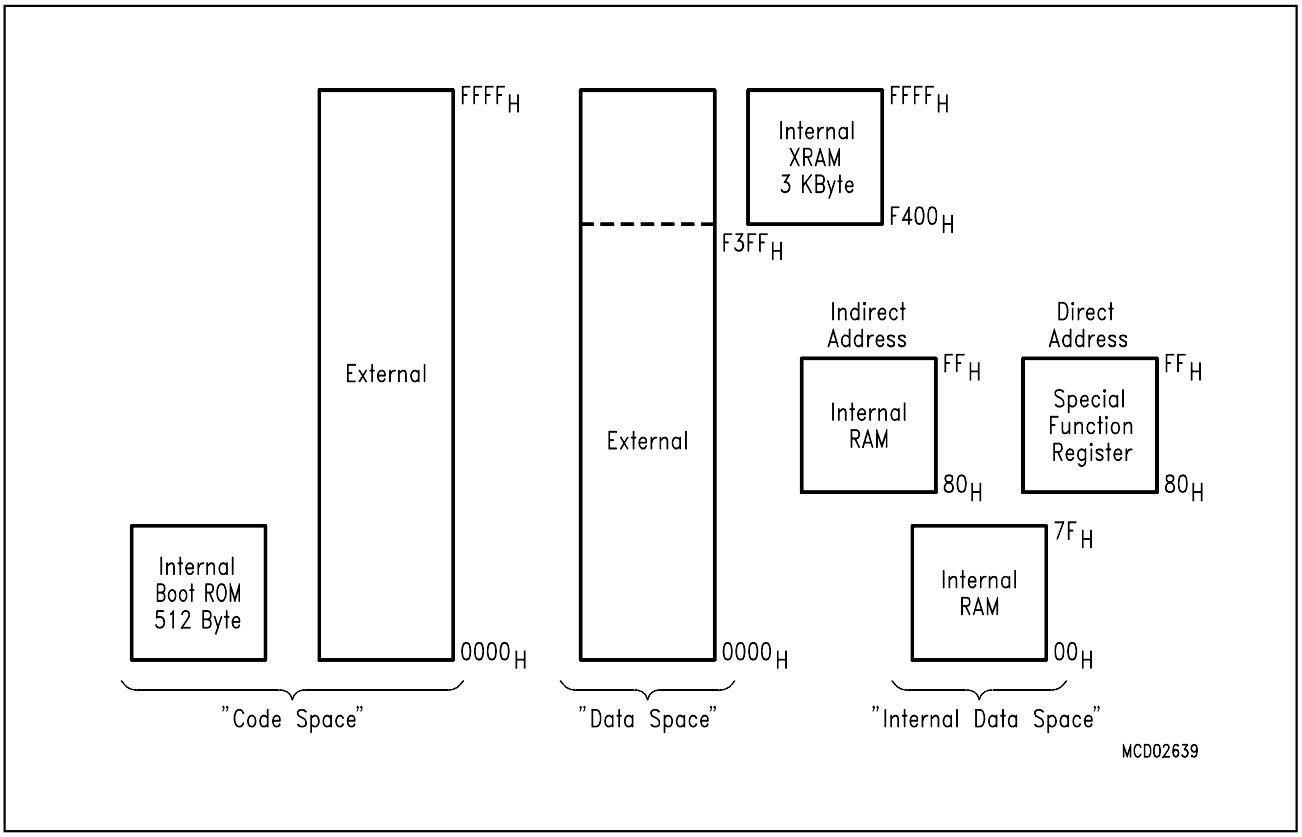


Figure 5
C509-L Memory Map

The C509-L can operate in four different operating modes (chipmodes) with different program and data memory organizations :

- Normal Mode
- XRAM Mode
- Bootstrap Mode
- Programming Mode

Table 2 describes the program and data memory areas which are available in the different chipmodes of the C509-L. It also shows the control bits of SFR SYSCON1, which are used for the software selection of the chipmodes. **Figures 6** to **9** shows the four chipmode configurations with the code and data memory partitioning.

Table 2
Overview of Program and Data Memory Organization

Operating Mode (Chipmode)	Program Memory		Data Memory		SYSCON1 Bits	
	Ext.	Int.	Ext.	Int.	PRGEN 1	SWAP
Normal Mode	0000_H - $FFFF_H$	–	0000_H - $F3FF_H$	$F400_H$ - $FFFF_H$ (XRAM)	0	0
XRAM Mode	0200_H - $F3FF_H$	0000_H - $01FF_H$ = Boot ROM; $F400_H$ - $FFFF_H$ = (XRAM)	0000_H - $FFFF_H$ (read only)	–	0	1
Bootstrap Mode	0200_H - $F3FF_H$	0000_H - $01FF_H$ = Boot ROM	0000_H - $F3FF_H$	$F400_H$ – $FFFF_H$ (XRAM)	1	0
Programming Mode	0200_H - $FFFF_H$	0000_H - $01FF_H$ = Boot ROM; $F400_H$ - $FFFF_H$ = XRAM	0000_H - $FFFF_H$ (read and write)	–	1	1

Normal Mode Configuration

The Normal Mode is the standard 8051 compatible operating mode of the C509-L. In this mode 64K byte external code memory and 61K byte external SRAM as well as 3K byte internal data memory (XRAM) are provided. If the is disabled (default after reset), totally 64K byte external data memory are available. The Boot ROM is disabled. The external program memory is controlled by the $\overline{PSEN}$/$\overline{RDF}$ signal. Read and write accesses to the external data memory are controlled by the $\overline{RD}$ and $\overline{WR}$ pins of port 3.

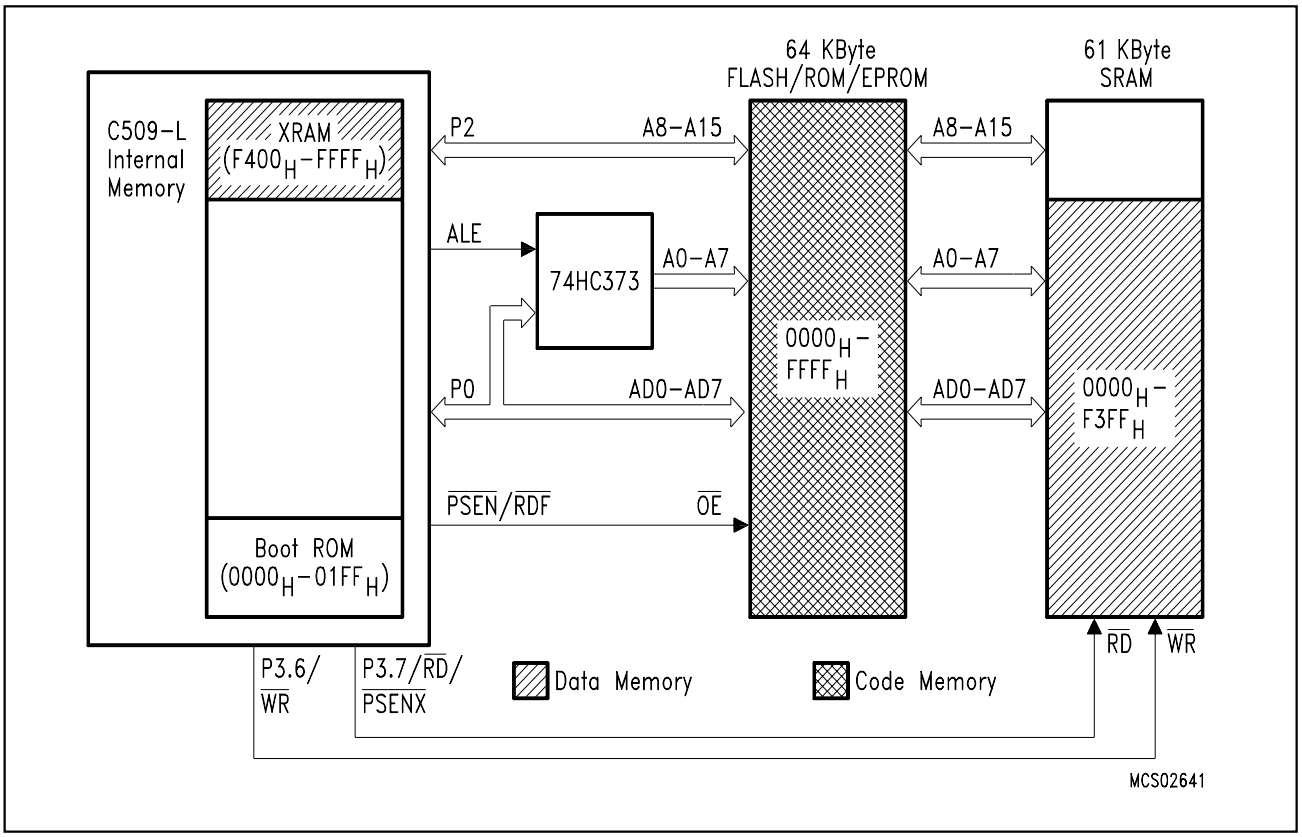


Figure 6
Locations of Code- and Data Memory in Normal Mode

XRAM Mode Configuration

The XRAM Mode is implemented in the C509-L for executing e.g. up to 3K byte diagnostic software which has been loaded into the XRAM in the Bootstrap Mode via the serial interface. In this operating mode the Boot ROM, the XRAM, and the external data memory are mapped into the code memory area, while the external ROM/EPROM is mapped into the external data memory area. External program memory fetches from the SRAM are controlled by the P3.7/$\overline{RD}$/$\overline{PSENX}$ pin. External data memory read accesses from the ROM/EPROM are controlled by the $\overline{PSEN}$/$\overline{RDF}$ pin. In XRAM mode, the external data memory can only be read but not written.

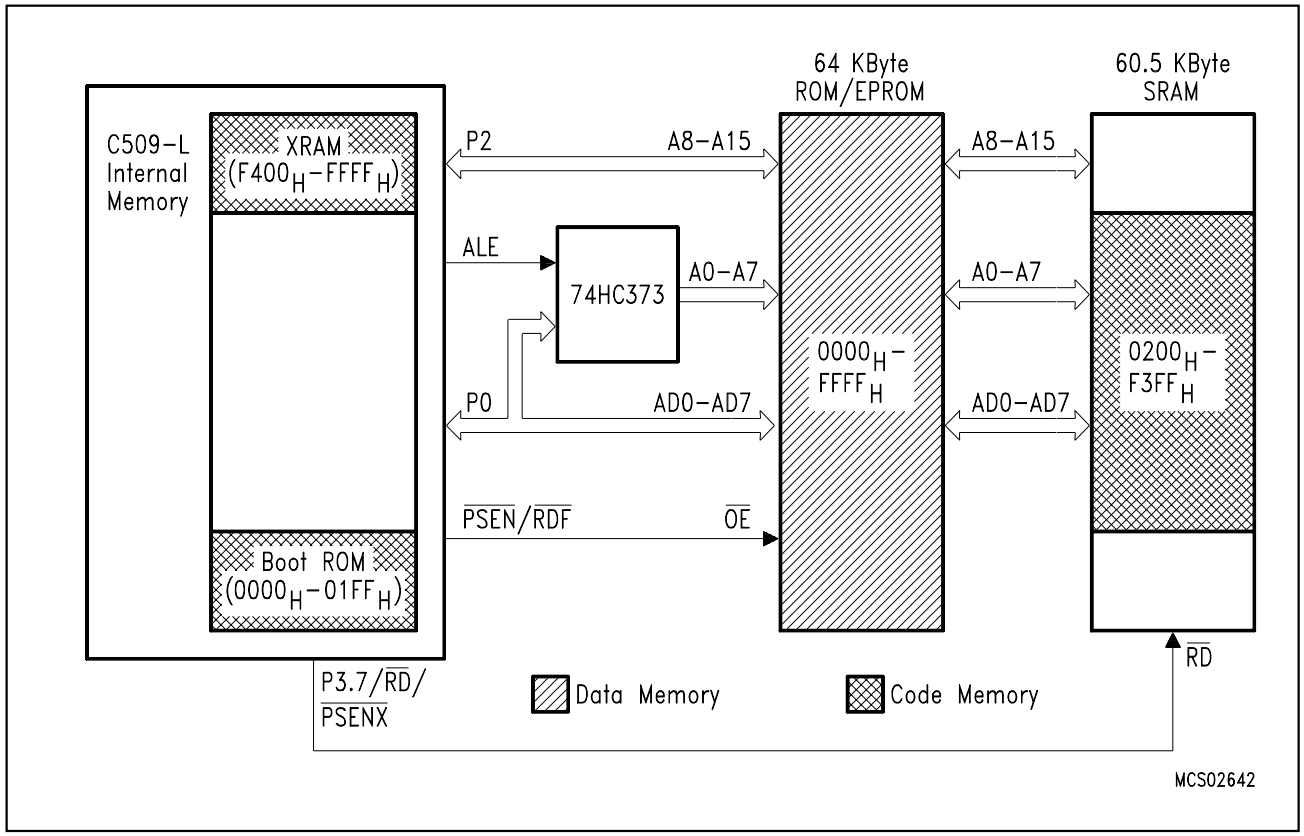


Figure 7
Locations of Code- and Data Memory in XRAM Mode

Bootstrap Mode Configuration

In the Bootstrap Mode the Boot ROM and the external FLASH/ROM/EPROM are mapped into the code memory area. 61K byte external SRAM as well as 3K byte internal data memory (XRAM) are provided in the external data memory area. The external program memory is controlled by the $\overline{PSEN}/\overline{RDF}$ signal. Read and write accesses to the external data memory are controlled by the $\overline{RD}$ and $\overline{WR}$ pins of port 3.

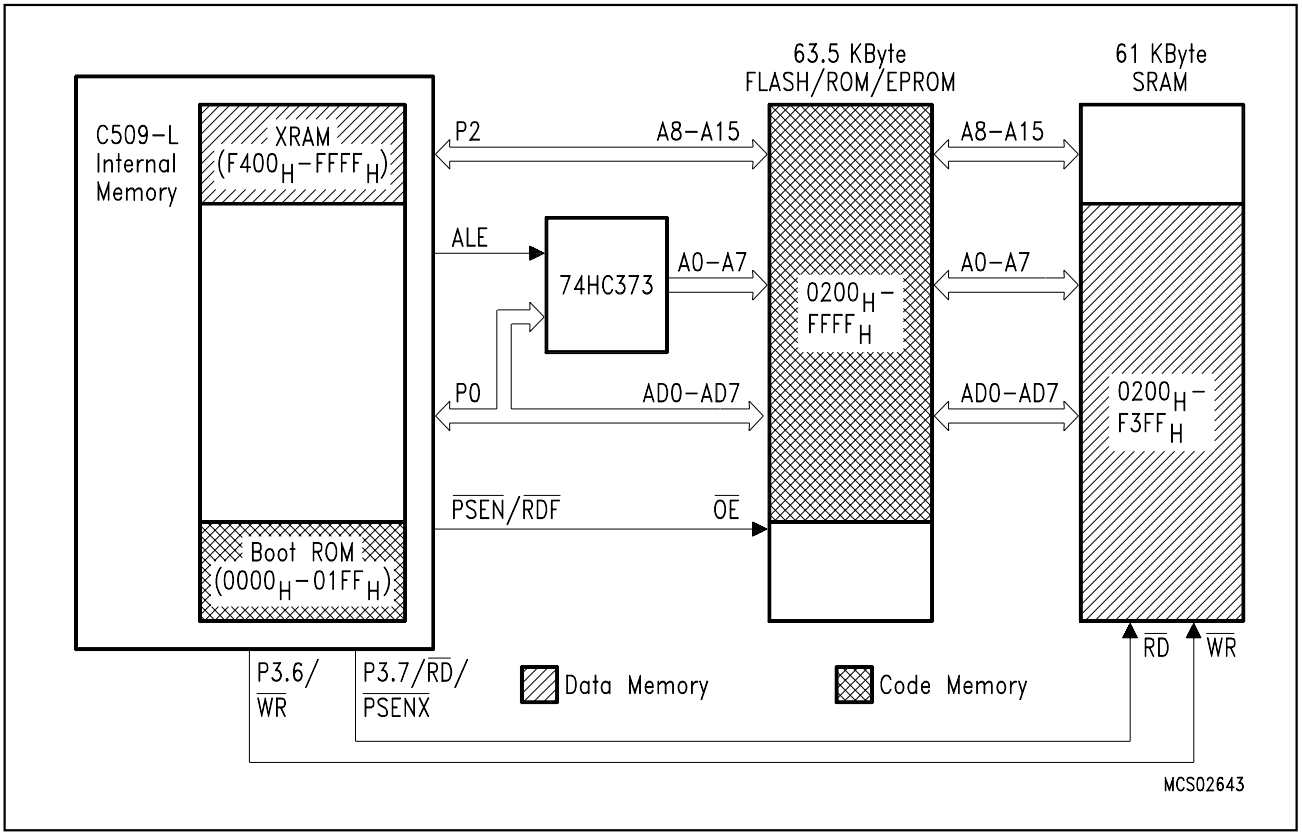


Figure 8
Locations of Code- and Data Memory in Bootstrap Mode

Programming Mode Configuration

The External Programming Mode is implemented for the in-circuit programming of external 5V-only FLASH EPROMs. Similar as in the XRAM mode, the Boot ROM, the XRAM, and the external data memory (SRAM) are mapped into the code memory area, while the external FLASH memory is mapped into the external data memory area. Additionally to the XRAM mode, the FLASH memory can also be written through external data memory accesses (MOVX instructions). External program memory fetches from the SRAM are controlled by the P3.7/$\overline{RD}$/$\overline{PSENX}$ pin. External data memory read/write accesses from/to the ROM/EPROM are controlled by the $\overline{PSEN}$/$\overline{RDF}$ and P6.3/$\overline{WRF}$ pin.

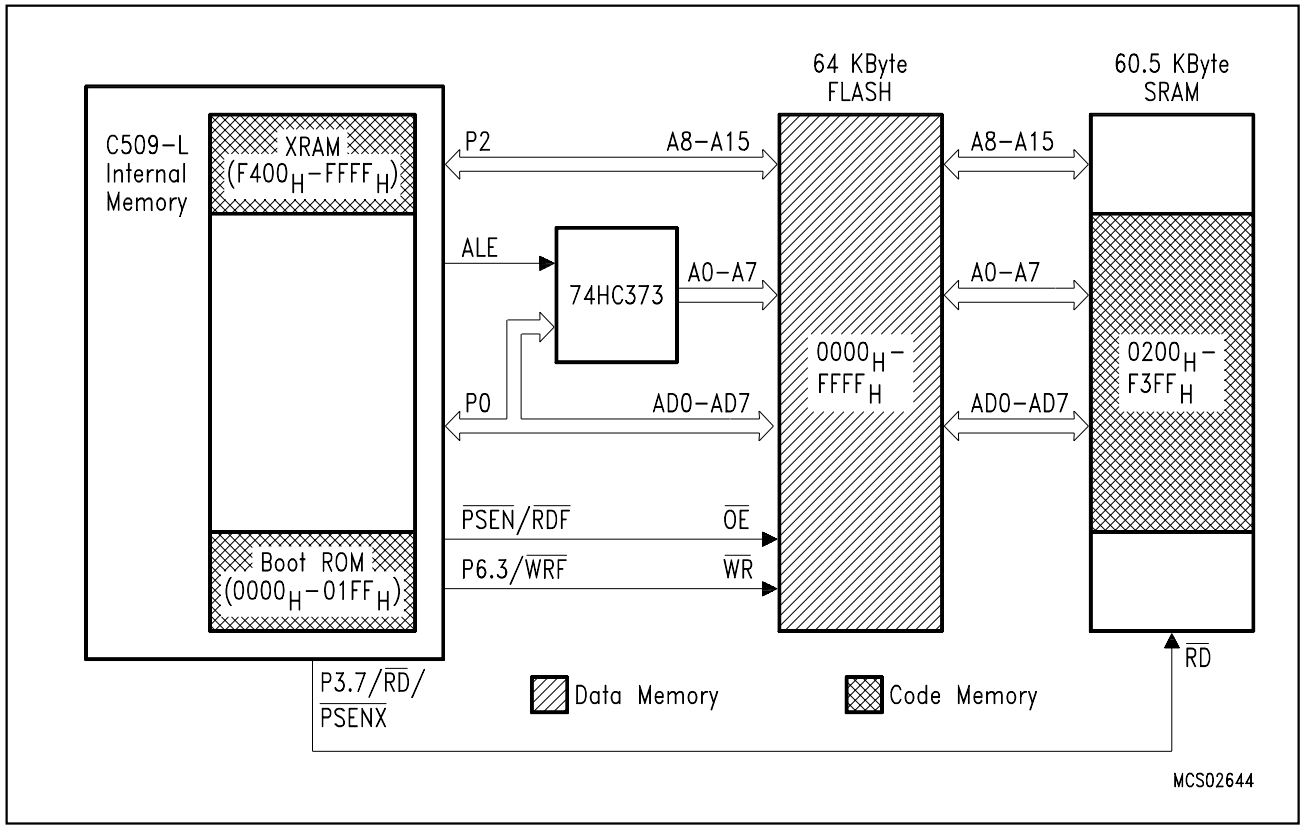


Figure 9
Locations of Code- and Data Memory in Programming Mode

The Bootstrap Loader

The C509-L includes a bootstrap mode, which is activated by setting the PRGEN pin at logic high level at the rising edge of the $\overline{\text{RESET}}$ or the $\overline{\text{HWPD}}$ signal (bit PRGEN1=1). In this mode software routines of the bootstrap loader, located at the addresses 0000_H to $01FF_H$ in the boot ROM will be executed. Its purpose is to allow the easy and quick programming of the internal XRAM ($F400_H$ to $FFFF_H$) via serial interface while the MCU is in-circuit. This allows to transfer custom routines to the XRAM, which will program an external 64 KByte FLASH memory. The serial routines of the bootstrap loader may be replaced by own custom software or even can be blocked to prevent unauthorized persons from reading out or writing to the external FLASH memory. Therefore the bootstrap loader checks an external FLASH memory for existing custom software and executes it.

The bootstrap loader consists of three functional parts which represent the three phases as described below.

Phase I : Check for existing custom software in the external FLASH memory and execute it.

Phase II : Establish a serial connection and automatically synchronize to the transfer speed (baud rate) of the serial communication partner (host).

Phase III : Perform the serial communication to the host. The host controls the bootstrap loader by sending header informations, which select one of four operating modes. These modes are :

- Mode 0 : Transfer a custom program from the host to the XRAM ($F400_H$ - $FFFF_H$). This mode returns to the beginning of phase III.
- Mode 1 : Execute a custom program in the XRAM at any start address from $F400_H$ to $FFFF_H$.
- Mode 2 : Check the contents of any area of the external FLASH memory by calculating a checksum. This mode returns to the beginning of phase III.
- Mode 3 : Execute a custom program in the FLASH memory at any start address beyond 0200_H (at addresses 0000_H to $01FF_H$ the boot-ROM is active).

The three phases of the bootstrap loader program and their connections are illustrated in **figure 10**.

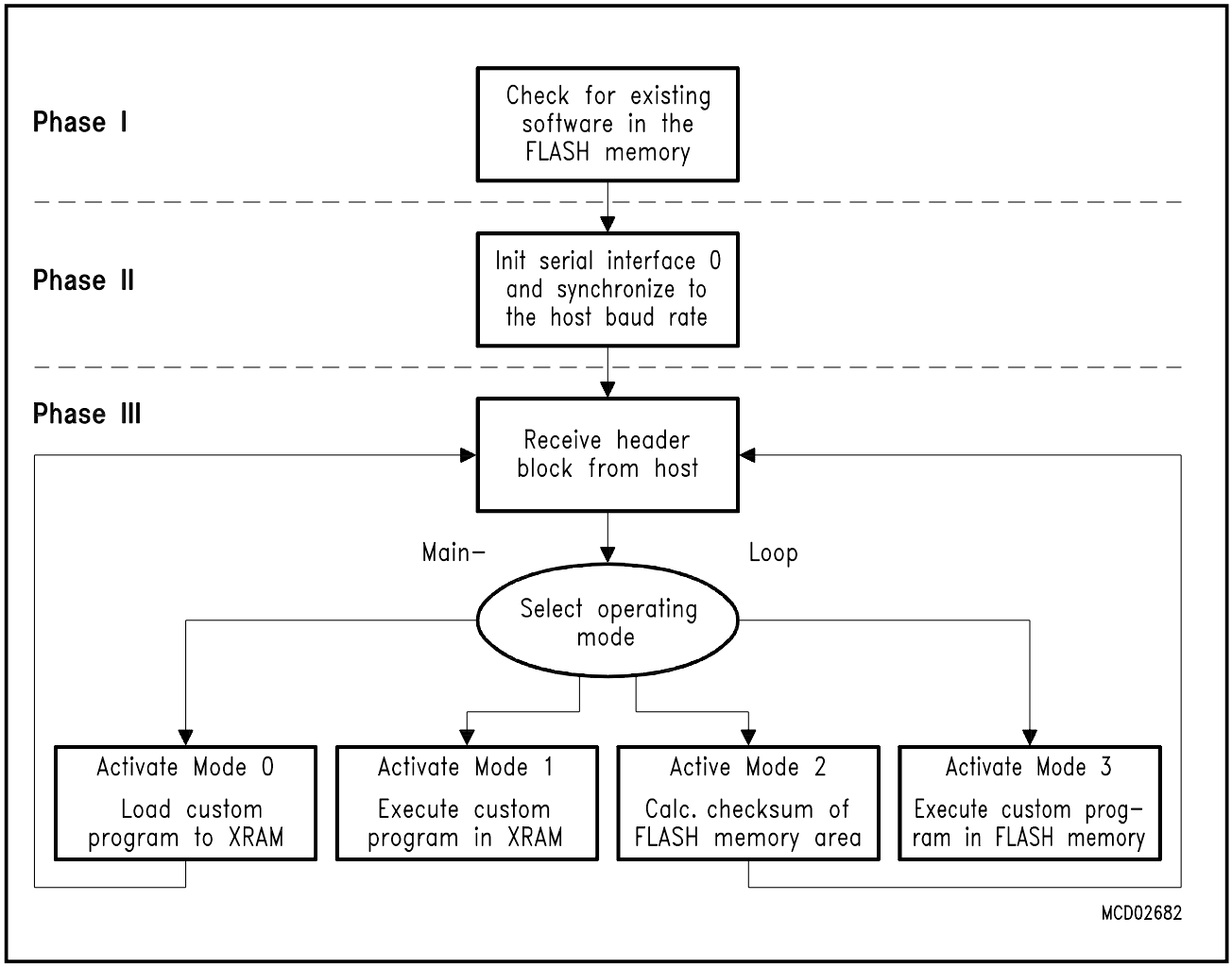


Figure 10
The Three Phases of the Bootstrap Loader

The serial communication, which is activated in phase II is performed with the integrated serial interface 0 of the C509-L. Using a full- or half-duplex serial cable (RS232) the MCU must be connected to the serial port of the host computer as shown in **figure** .

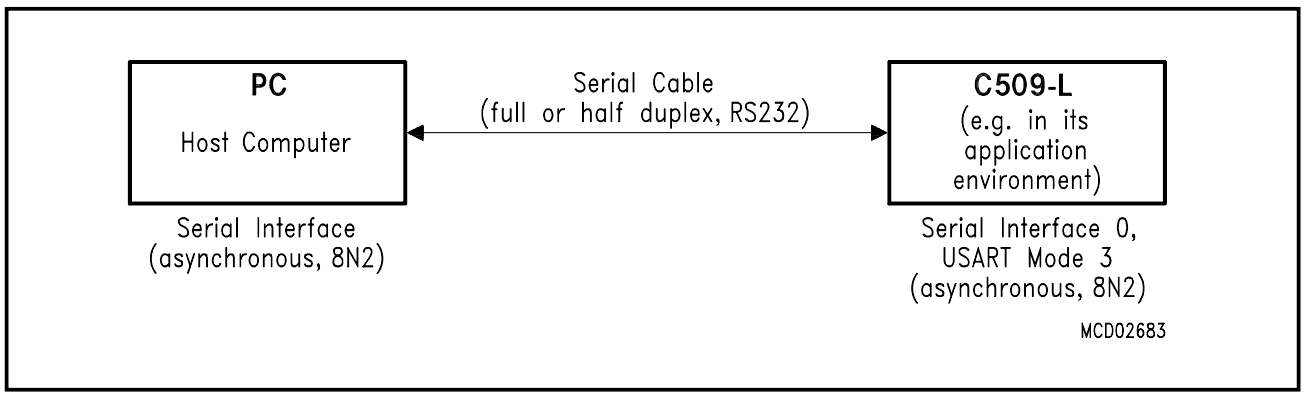


Figure 11
Bootstrap Loader Interface to the PC

Control of XRAM Access

The XRAM in the C509-L is a memory area that is logically located at the upper end of the external memory space, but is integrated on the chip. Because the XRAM is used in the same way as external data memory the same instruction types (MOVX) must be used for accessing the XRAM. Two bits in SFR SYSCON, XMAP0 and XMAP1, control the accesses to the XRAM.

Special Function Register SYSCON (Address $B1_H$) **Reset Value : $1010XX01_B$**

Bit No.	MSB 7	6	5	4	3	2	1	LSB 0	
$B1_H$	CLKP	PMOD	1	RMAP	–	–	XMAP1	XMAP0	SYSCON

The functions of the shaded bits are not used for XRAM control.

Bit	Function
XMAP1	XRAM visible access control Control bit for $\overline{RD}$/$\overline{WR}$ signals during XRAMaccesses. If addresses are outside the XRAM address range or if XRAM is disabled, this bit has no effect. XMAP1 = 0 : The signals $\overline{RD}$ and $\overline{WR}$ are not activated during accesses to the XRAM XMAP1 = 1 : Ports 0, 2 and the signals $\overline{RD}$ and $\overline{WR}$ are activated during accesses to XRAM. In this mode, address and data information during XRAM/CAN Controller accesses are visible externally.
XMAP0	Global XRAM access enable/disable control XMAP0 = 0 : The access to XRAM is enabled. XMAP0 = 1 : The access to XRAM is disabled (default after reset!). All MOVX accesses are performed via the external bus. Further, this bit is hardware protected.

Bit XMAP0 is hardware protected. If it is reset once (XRAM access enabled) it cannot be set by software. Only a reset operation will set the XMAP0 bit again.

The XRAM can be accessed by read/write instructions (MOVX A,DPTR, MOVX @DPTR,A), which use the 16-bit DPTR for indirect addressing. For accessing the XRAM, the effective address stored in DPTR must be in the range of $F700_H$ to $FFFF_H$.38

The XRAM can be also accessed by read/write instructions (MOVX A,@Ri, MOVX @Ri,A), which use only an 8-bit address (indirect addressing with registers R0 or R1). Therefore, a special page register XPAGE which provides the upper address information (A8-A15) during 8-bit XRAM accesses.

The behaviour of Port 0 and P2 during a MOVX access depends on the control bits XMAP0 and XMAP1 in register SYSCON and on the state of pin $\overline{EA}$. **Table 3** lists the various operating conditions.

		$\overline{EA}$ = 0			$\overline{EA}$ = 1		
		XMAP1, XMAP0			XMAP1, XMAP0		
		00	**10**	**X1**	**00**	**10**	**X1**
MOVX @DPTR	DPTR < XRAM address range	a)P0/P2→Bus b)$\overline{RD}$/$\overline{WR}$ active c)ext.memory is used	a)P0/P2→Bus b)$\overline{RD}$/$\overline{WR}$ active c)ext.memory is used	a)P0/P2→Bus b)$\overline{RD}$/$\overline{WR}$ active c)ext.memory is used	a)P0/P2→Bus b)$\overline{RD}$/$\overline{WR}$ active c)ext.memory is used	a)P0/P2→Bus b)$\overline{RD}$/$\overline{WR}$ active c)ext.memory is used	a)P0/P2→Bus b)$\overline{RD}$/$\overline{WR}$ active c)ext.memory is used
	DPTR ≥ XRAM address range	a)P0/P2→Bus ($\overline{WR}$ / $\overline{RD}$ Data) b)$\overline{RD}$/$\overline{WR}$ inactive c)XRAM is used	a)P0/P2→Bus ($\overline{WR}$ / $\overline{RD}$ Data) b)$\overline{RD}$/$\overline{WR}$ active c)XRAM is used	a)P0/P2→Bus b)$\overline{RD}$/$\overline{WR}$ active c) ext.memory is used	a)P0/P2→I/0 b)$\overline{RD}$/$\overline{WR}$ inactive c)XRAM is used	a)P0/P2→Bus ($\overline{WR}$ / $\overline{RD}$ Data) b)$\overline{RD}$/$\overline{WR}$ active c)XRAM is used	a)P0/P2→Bus b)$\overline{RD}$/$\overline{WR}$ active c) ext.memory is used
MOVX @ Ri	XPAGE < XRAM addr.page range	a)P0→Bus P2→I/O b)$\overline{RD}$/$\overline{WR}$ active c)ext.memory is used	a)P0→Bus P2→I/O b)$\overline{RD}$/$\overline{WR}$ active c)ext.memory is used	a)P0→Bus P2→I/O b)$\overline{RD}$/$\overline{WR}$ active c)ext.memory is used	a)P0→Bus P2→I/O b)$\overline{RD}$/$\overline{WR}$ active c)ext.memory is used	a)P0→Bus P2→I/O b)$\overline{RD}$/$\overline{WR}$ active c)ext.memory is used	a)P0→Bus P2→I/O b)$\overline{RD}$/$\overline{WR}$ active c)ext.memory is used
	XPAGE ≥ XRAM addr.page range	a)P0→Bus ($\overline{WR}$ / $\overline{RD}$ Data) P2→I/O b)$\overline{RD}$/$\overline{WR}$ inactive c)XRAM is used	a)P0→Bus ($\overline{WR}$ / $\overline{RD}$ Data) P2→I/O b)$\overline{RD}$/$\overline{WR}$ active c)XRAM is used	a)P0→Bus P2→I/O b)$\overline{RD}$/$\overline{WR}$ active c)ext.memory is used	a)P2→I/O P0/P2→I/O b)$\overline{RD}$/$\overline{WR}$ inactive c)XRAM is used	a)P0→Bus ($\overline{WR}$ / $\overline{RD}$ Data) P2→I/O b)$\overline{RD}$/$\overline{WR}$ active c)XRAM is used	a)P0→Bus P2→I/O b)$\overline{RD}$/$\overline{WR}$ active c)ext.memory is used

modes compatible to 8051/C501 family

Table 3
Behaviour of P0/P2 and $\overline{RD}$/$\overline{WR}$ During MOVX Accesses

Reset and System Clock

The reset input is an active low input at pin $\overline{\text{RESET}}$. Since the reset is synchronized internally, the $\overline{\text{RESET}}$ pin must be held low for at least two machine cycles (12 oscillator periods) while the oscillator is running. A pullup resistor is internally connected to V_{CC} to allow a power-up reset with an external capacitor only. An automatic reset can be obtained when V_{CC} is applied by connecting the reset pin to V_{SS} via a capacitor. **Figure 12** shows the possible reset circuitries.

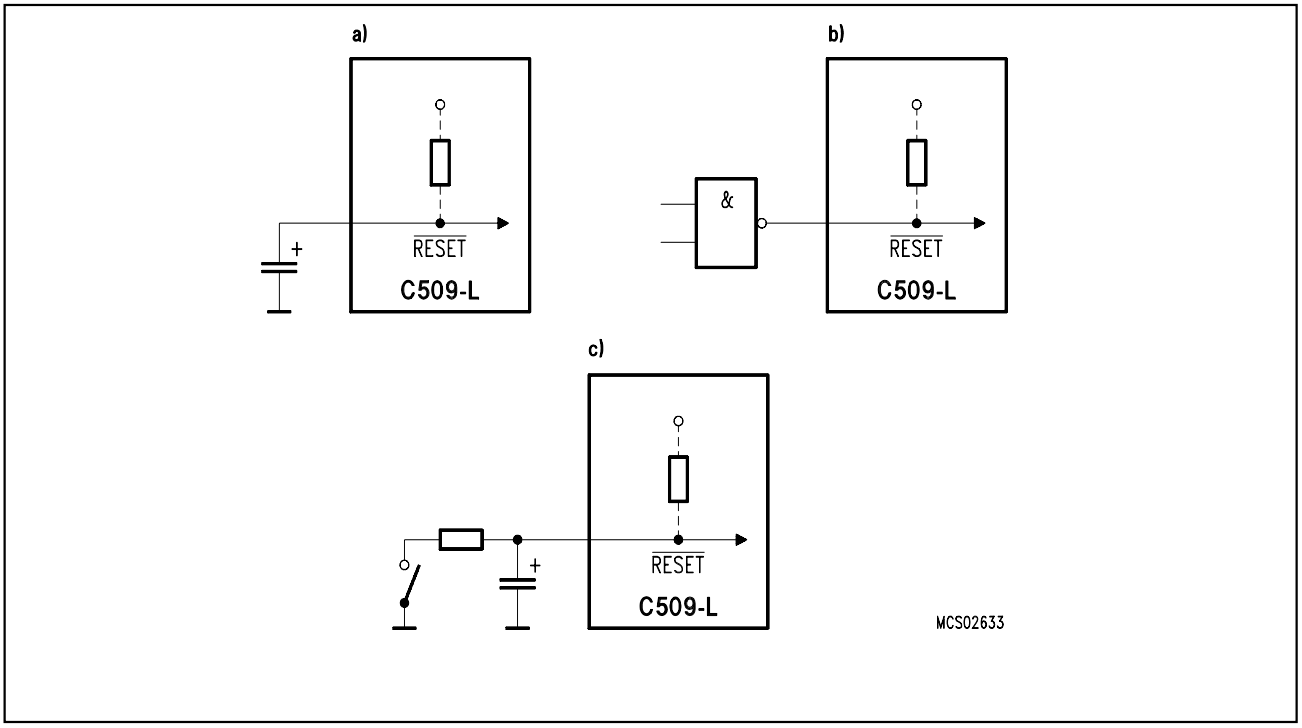


Figure 12
Reset Circuitries

Figure 13 shows the recommended oscillator circiutries for crystal and external clock operation.

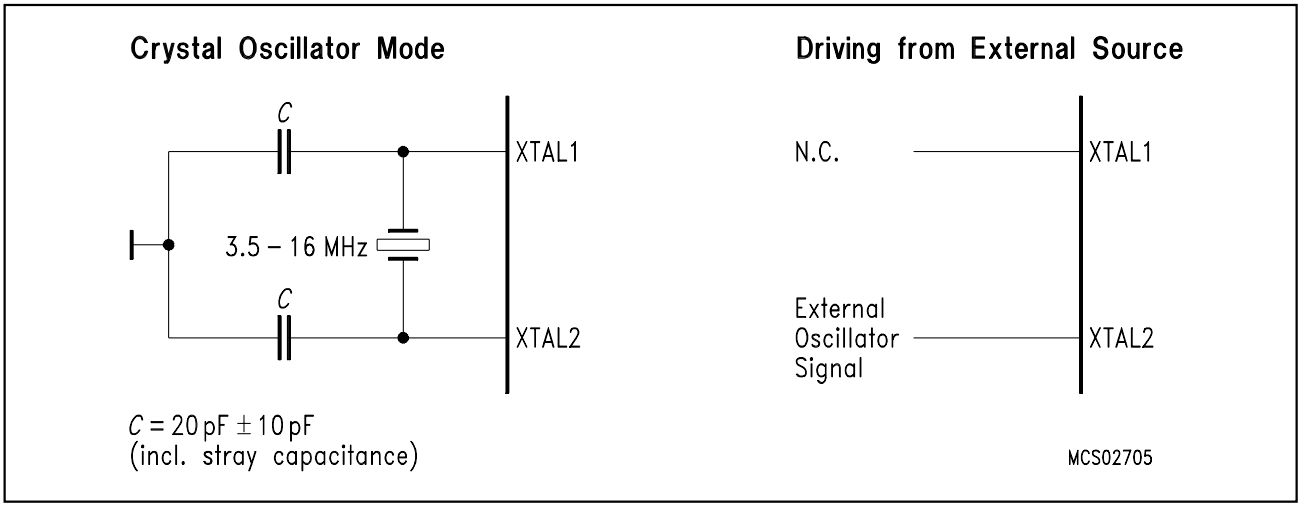


Figure 13
Recommended Oscillator Circuitries

Multiple Datapointers

As a functional enhancement to the standard 8051 architecture, the C509-L contains eight 16-bit datapointers instead of only one datapointer. The instruction set uses just one of these datapointers at a time. The selection of the actual datapointer is done in the special function regsiter DPSEL. **Figure 14** illustrates the datapointer addressing mechanism.

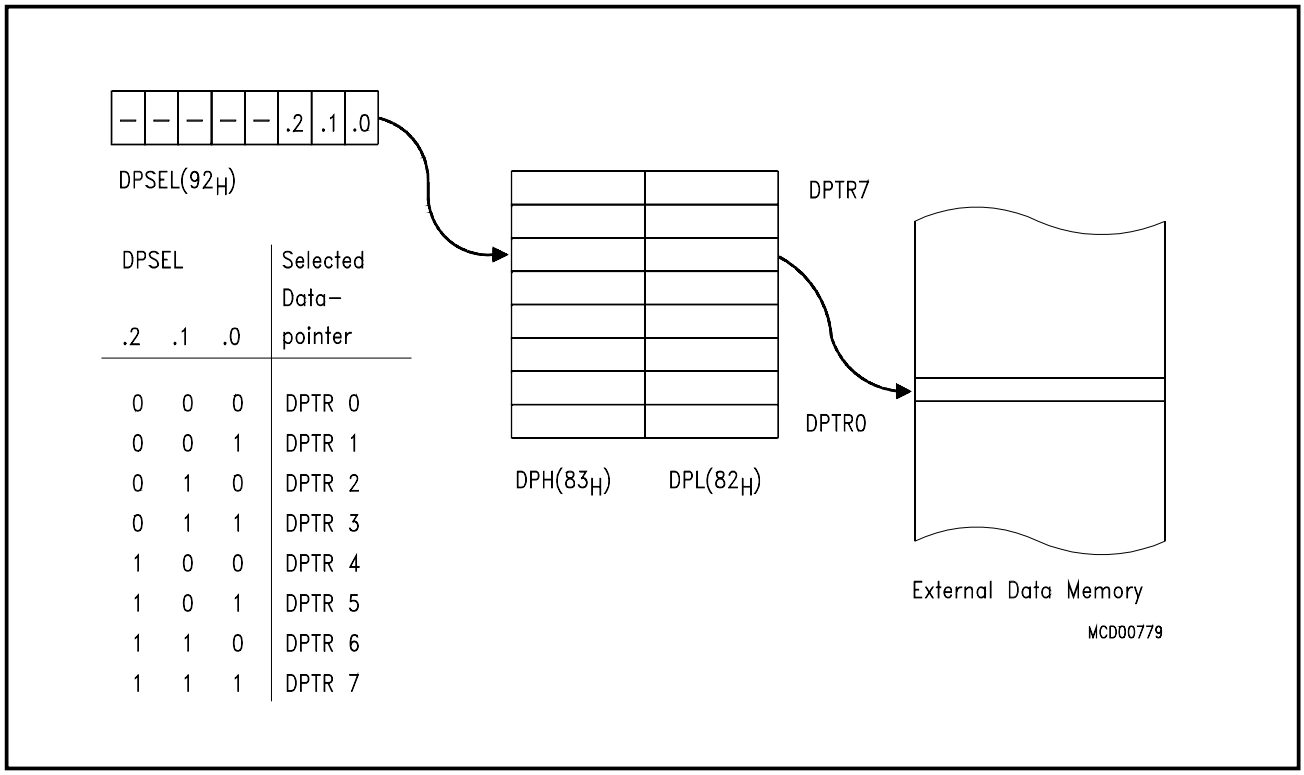


Figure 14
External Data Memory Addressing using Multiple Datapointers

Enhanced Hooks Emulation Concept

The Enhanced Hooks Emulation Concept of the C500 microcontroller family is a new, innovative way to control the execution of C500 MCUs and to gain extensive information on the internal operation of the controllers. Emulation of on-chip ROM based programs is possible, too (not true for the C509-L, because it lacks internal program memory).
Each production chip has built-in logic for the supprt of the Enhanced Hooks Emulation Concept. Therefore, no costly bond-out chips are necessary for emulation. This also ensure that emulation and production chips are identical.

The Enhanced Hooks Technology™, which requires embedded logic in the C500 allows the C500 together with an EH-IC to function similar to a bond-out chip. This simplifies the design and reduces costs of an ICE-system. ICE-systems using an EH-IC and a compatible C500 are able to emulate all operating modes of the different versions of the C500 microcontrollers. This includes emulation of ROM, ROM with code rollover and ROMless modes of operation. It is also able to operate in single step mode and to read the SFRs after a break.

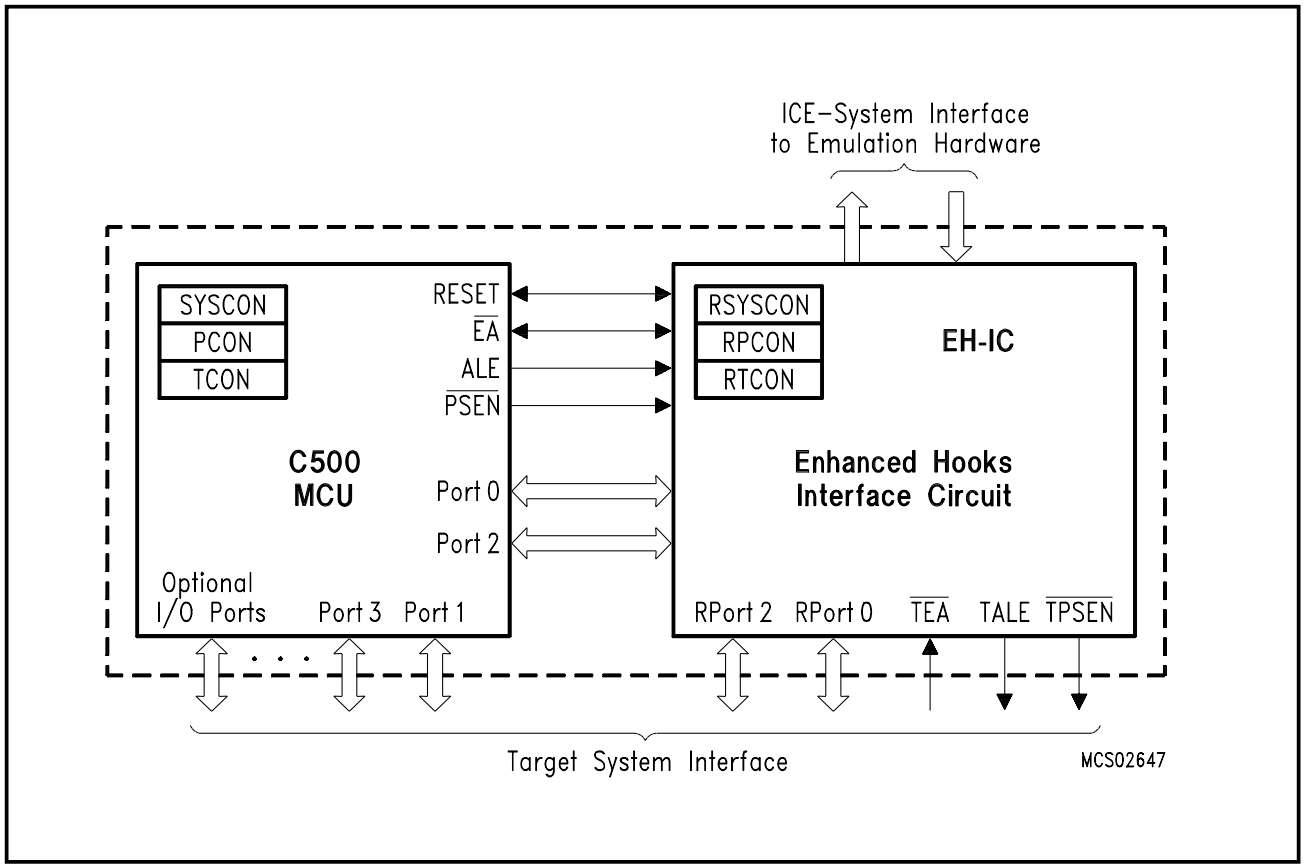


Figure 15
Basic C500 MCU Enhanced Hooks Concept Configuration

Port 0, port 2 and some of the control lines of the C500 based MCU are used by Enhanced Hooks Emulation Concept to control the operation of the device during emulation and to transfer informations about the programm execution and data transfer between the external emulation hardware (ICE-system) and the C500 MCU.

Special Function Registers

All registers, except the program counter and the four general purpose register banks, reside in the special function register area. Several special function registers of the C509-L (CC10-17, CT1REL, CC1EN, CAFR) are located in the mapped special function register area. For accessing the mapped special function register area, bit RMAP in special function register SYSCON must be set. All other special function registers are located in the standard special function register area. As long as bit RMAP is set, mapped special function registers can be accessed. This bit is not cleared by hardware automatically.

Special Function Register SYSCON (Address $B1_H$) **Reset Value : $1010XX01_B$**

Bit No.	MSB 7	6	5	4	3	2	1	LSB 0	
$B1_H$	CLKP	PMOD	1	RMAP	–	–	XMAP1	XMAP0	SYSCON

Bit	Function
RMAP	Special function register map bit RMAP = 0 : The access to the non-mapped (standard) special function register area is enabled (reset value). RMAP = 1 : The access to the mapped special function register area is enabled.

The 103 special function register (SFR) include pointers and registers that provide an interface between the CPU and the other on-chip peripherals. The SFRs of the C509-L are listed in **table 4** and **table 5**. In **table 4** they are organized in groups which refer to the functional blocks of the C509-L. **Table 5** illustrates the contents of the SFRs in numeric order of their addresses. The most right column of **table 5** indicates if an SFR is accessed with a mapped procedure controlled by either RMAP or PDIR.

Table 4
Special Function Registers - Functional Blocks

Block	Symbol	Name	Address	Contents after Reset
CPU	ACC	Accumulator	**$E0_H$** [1]	**00_H**
	B	B-Register	**$F0_H$** [1]	**00_H**
	DPH	Data Pointer, High Byte	83_H	00_H
	DPL	Data Pointer, Low Byte	82_H	00_H
	DPSEL	Data Pointer Select Register	92_H	$XXXXX000_B$ [3]
	PSW	Program Status Word	**$D0_H$** [1]	**00_H**
	SP	Stack Pointer	81_H	07_H
	SYSCON1	System Control Register 1	$B2_H$	$00XXXEE0_B$ [3][6]
SFR Mapping	SYSCON [2]	System Control Register	$B1_H$	$1010XX01_B$ [3]
Interrupt System	IEN0	Interrupt Enable Register 0	**$A8_H$** [1]	**00_H**
	CTCON [2]	Compare Timer Control Register	$E1_H$	01000000_B [3]
	CT1CON [2]	Compare Timer 1 Control Register	BC_H	$X1XX0000_B$ [3]
	IEN1 [2]	Interrupt Enable Register 1	**$B8_H$** [1]	**00_H**
	IEN2 [2]	Interrupt Enable Register 2	$9A_H$	$XX0000X0_B$ [3]
	IEN3	Interrupt Enable Register 3	BE_H	$XXXX00XX_B$ [3]
	IP0 [2]	Interrupt Priority Register 0	$A9_H$	00_H
	IP1 [2]	Interrupt Priority Register 1	$B9_H$	$0X000000_B$ [3]
	IRCON0	Interrupt Request Control Register 0	**$C0_H$** [1]	**00_H**
	IRCON1	Interrupt Request Control Register 1	$D1_H$	00_H
	IRCON2 [4]	Interrupt Request Control Register 2	BF_H	00_H
	EICC1 [4]	Interrupt Request Enable Register for CT1	BF_H	FF_H
	TCON [2]	Timer Control Register	**88_H** [1]	**00_H**
	T2CON [2]	Timer 2 Control Register	**$C8_H$** [1]	**00_H**
XRAM	XPAGE	Page Address Register for XRAM	91_H	00_H
	SYSCON [2]	System Control Register	$B1_H$	$1010XX01_B$ [3]
A/D Converter	ADCON0	A/D Converter Control Register 0	**$D8_H$** [1]	**00_H**
	ADCON1	A/D Converter Control Register 1	DC_H	01000000_B [3]
	ADDATH	A/D Converter Data Register, High Byte	$D9_H$	00_H
	ADDATL	A/D Converter Data Register, Low Byte	DA_H	00_H

1) Bit-addressable special function registers
2) This special function register is listed repeatedly since some bits of it also belong to other functional blocks.
3) X means that the value is indeterminate or the location is reserved
4) Register is mapped by bit PDIR.
5) Register is mapped by bit RMAP.
6) "E" means that the value of the bit is defined by the logic level at pin PRGEN at the rising edge of the $\overline{\text{RESET}}$ or $\overline{\text{HWPD}}$ signals.

Table 4
Special Function Registers - Functional Blocks (cont'd)

Block	Symbol	Name	Address	Contents after Reset
Compare / Capture Unit (CCU) Timer 2	CCEN	Compare/Capture Enable Register	$C1_H$	00_H
	CC4EN	Compare/Capture 4 Enable Register	$C9_H$	00_H
	CCH1	Compare/Capture Register 1, High Byte	$C3_H$	00_H
	CCH2	Compare/Capture Register 2, High Byte	$C5_H$	00_H
	CCH3	Compare/Capture Register 3, High Byte	$C7_H$	00_H
	CCH4	Compare/Capture Register 4, High Byte	CF_H	00_H
	CCL1	Compare/Capture Register 1, Low Byte	$C2_H$	00_H
	CCL2	Compare/Capture Register 2, Low Byte	$C4_H$	00_H
	CCL3	Compare/Capture Register 3, Low Byte	$C6_H$	00_H
	CCL4	Compare/Capture Register 4, Low Byte	CE_H	00_H
	CMEN [5)]	Compare Enable Register	$F6_H$	00_H
	CMH0 [5)]	Compare Register 0, High Byte	$D3_H$	00_H
	CMH1 [5)]	Compare Register 1, High Byte	$D5_H$	00_H
	CMH2 [5)]	Compare Register 2, High Byte	$D7_H$	00_H
	CMH3 [5)]	Compare Register 3, High Byte	$E3_H$	00_H
	CMH4 [5)]	Compare Register 4, High Byte	$E5_H$	00_H
	CMH5 [5)]	Compare Register 5, High Byte	$E7_H$	00_H
	CMH6 [5)]	Compare Register 6, High Byte	$F3_H$	00_H
	CMH7 [5)]	Compare Register 7, High Byte	$F5_H$	00_H
	CML0 [5)]	Compare Register 0, Low Byte	$D2_H$	00_H
	CML1 [5)]	Compare Register 1, Low Byte	$D4_H$	00_H
	CML2 [5)]	Compare Register 2, Low Byte	$D6_H$	00_H
	CML3 [5)]	Compare Register 3, Low Byte	$E2_H$	00_H
	CML4 [5)]	Compare Register 4, Low Byte	$E4_H$	00_H
	CML5 [5)]	Compare Register 5, Low Byte	$E6_H$	00_H
	CML6 [5)]	Compare Register 6, Low Byte	$F2_H$	00_H
	CML7 [5)]	Compare Register 7, Low Byte	$F4_H$	00_H
	CC1EN [5)]	Compare/Capture Enable Register	$F6_H$	00_H
	CC1H0 [5)]	Compare/Capture 1 Register 0, High Byte	$D3_H$	00_H
	CC1H1 [5)]	Compare/Capture 1 Register 1, High Byte	$D5_H$	00_H
	CC1H2 [5)]	Compare/Capture 1 Register 2, High Byte	$D7_H$	00_H
	CC1H3 [5)]	Compare/Capture 1 Register 3, High Byte	$E3_H$	00_H
	CC1H4 [5)]	Compare/Capture 1 Register 4, High Byte	$E5_H$	00_H
	CC1H5 [5)]	Compare/Capture 1 Register 5, High Byte	$E7_H$	00_H
	CC1H6 [5)]	Compare/Capture 1 Register 6, High Byte	$F3_H$	00_H
	CC1H7 [5)]	Compare/Capture 1 Register 7, High Byte	$F5_H$	00_H
	CC1L0 [5)]	Compare/Capture 1 Register 0, Low Byte	$D2_H$	00_H
	CC1L1 [5)]	Compare/Capture 1 Register 1, Low Byte	$D4_H$	00_H
	CC1L2 [5)]	Compare/Capture 1 Register 2, Low Byte	$D6_H$	00_H
	CC1L3 [5)]	Compare/Capture 1 Register 3, Low Byte	$E2_H$	00_H
	CC1L4 [5)]	Compare/Capture 1 Register 4, Low Byte	$E4_H$	00_H
	CC1L5 [5)]	Compare/Capture 1 Register 5, Low Byte	$E6_H$	00_H
	CC1L6 [5)]	Compare/Capture 1 Register 6, Low Byte	$F2_H$	00_H
	CC1L7 [5]	Compare/Capture 1 Register 7, Low Byte	$F4_H$	00_H
	CMSEL [5)]	Compare Input Select	$F7_H$	00_H

[5)] Register is mapped by bit RMAP.

Table 4
Special Function Registers - Functional Blocks (cont'd)

Block	Symbol	Name	Address	Contents after Reset
Compare / Capture Unit (CCU) Timer 2 cont'd	CAFR [5]	Capture 1, Falling/Rising Edge Register	$F7_H$	00_H
	CRCH	Comp./Rel./Capt. Reg. High Byte	CB_H	00_H
	CRCL	Comp./Rel./Capt. Reg. Low Byte	CA_H	00_H
	COMSETL	Compare Set Register, Low Byte	$A1_H$	00_H
	COMSETH	Compare Set Register, High Byte	$A2_H$	00_H
	COMCLRL	Compare Clear Register, Low Byte	$A3_H$	00_H
	COMCLRH	Compare Clear Register, High Byte	$A4_H$	00_H
	SETMSK	Compare Set Mask Register	$A5_H$	00_H
	CLRMSK	Compare Clear Mask Register	$A6_H$	00_H
	CTCON [2]	Compare Timer Control Register	$E1_H$	01000000_B [3]
	CTRELH [5]	Compare Timer Rel. Reg., High Byte	DF_H	00_H
	CTRELL [5]	Compare Timer Rel. Reg., Low Byte	DE_H	00_H
	CT1RELH [5]	Compare Timer 1 Rel. Reg., High Byte	DF_H	00_H
	CT1RELL [5]	Compare Timer 1 Rel. Reg., Low Byte	DE_H	00_H
	TH2	Timer 2, High Byte	CD_H	00_H
	TL2	Timer 2, Low Byte	CC_H	00_H
	T2CON [2]	Timer 2 Control Register	**$C8_H$** [1]	**00_H**
	CT1CON [2]	Compare Timer 1 Control Register	BC_H	$X1XX0000_B$ [3]
	PRSC [2]	Prescaler Control Register	$B4_H$	11010101_B [3]
Serial Channels	ADCON0 [2]	A/D Converter Control Register	**$D8_H$** [1]	**00_H**
	PCON [2]	Power Control Register	87_H	00_H
	S0BUF	Serial Channel 0 Buffer Register	99_H	XX_H [3]
	S0CON	Serial Channel 0 Control Register	**98_H** [1]	**00_H**
	S0RELL	Serial Channel 0 Reload Reg., Low Byte	AA_H	$D9_H$
	S0RELH	Serial Channel 0 Reload Reg., High Byte	BA_H	$XXXXXX11_B$ [3]
	S1BUF	Serial Channel 1 Buffer Register	$9C_H$	XX_H [3]
	S1CON	Serial Channel 1 Control Register	$9B_H$	01000000_B [3]
	S1RELL	Serial Channel 1 Reload Reg., Low Byte	$9D_H$	00_H
	S1RELH	Serial Channel 1 Reload Reg., High Byte	BB_H	$XXXXXX11_B$ [3]
Watchdog	IEN0 [2]	Interrupt Enable Register 0	**$A8_H$** [1]	**00_H**
	IEN1 [2]	Interrupt Enable Register 1	**$B8_H$** [1]	**00_H**
	IP0 [2]	Interrupt Priority Register 0	$A9_H$	00_H
	IP1 [2]	Interrupt Priority Register 1	$B9_H$	$0X000000_B$ [3]
	WDTREL	Watchdog Timer Reload Register	86_H	00_H
	WDTL [6]	Watchdog Timer Register, Low Byte	84_H	00_H
	WDTH [6]	Watchdog Timer Register, High Byte	85_H	00_H

1) Bit-addressable special function registers
2) This special function register is listed repeatedly since some bits of it also belong to other functional blocks.
3) X means that the value is indeterminate or the location is reserved
4) Register is mapped by bit PDIR.
5) Register is mapped by bit RMAP.
6) Registers are only readable and cannot be written.

Table 4
Special Function Registers - Functional Blocks (cont'd)

Block	Symbol	Name	Address	Contents after Reset
MUL/DIV Unit	ARCON	Arithmetic Control Register	EF_H	$0XXXXXXX_B$ [3]
	MD0	Multiplication/Division Register 0	$E9_H$	XX_H [3]
	MD1	Multiplication/Division Register 1	EA_H	XX_H [3]
	MD2	Multiplication/Division Register 2	EB_H	XX_H [3]
	MD3	Multiplication/Division Register 3	EC_H	XX_H [3]
	MD4	Multiplication/Division Register 4	ED_H	XX_H [3]
	MD5	Multiplication/Division Register 5	EE_H	XX_H [3]
Timer 0 / Timer 1	TCON	Timer Control Register	**88_H** [1]	**00_H**
	TH0	Timer 0, High Byte	$8C_H$	00_H
	TH1	Timer 1, High Byte	$8D_H$	00_H
	TL0	Timer 0, Low Byte	$8A_H$	00_H
	TL1	Timer 1, Low Byte	$8B_H$	00_H
	TMOD	Timer Mode Register	89_H	00_H
	PRSC [2]	Prescaler Control Register	$B4_H$	11010101_B [3]
Ports	P0 [4]	Port 0	**80_H** [1]	**FF_H**
	DIR0 [4]	Direction Register Port 0	**80_H** [1]	**FF_H**
	P1 [4]	Port 1	**90_H** [1]	**FF_H**
	DIR1 [4]	Direction Register Port 1	**90_H** [1]	**FF_H**
	P2 [4]	Port 2	**$A0_H$** [1]	**FF_H**
	DIR2 [4]	Direction Register Port 2	**$A0_H$** [1]	**FF_H**
	P3 [4]	Port 3	**$B0_H$** [1]	**FF_H**
	DIR3 [4]	Direction Register Port 3	**$B0_H$** [1]	**FF_H**
	P4 [4]	Port 4	**$E8_H$** [1]	**FF_H**
	DIR4 [4]	Direction Register Port 4	**$E8_H$** [1]	**FF_H**
	P5 [4]	Port 5	**$F8_H$** [1]	**FF_H**
	DIR5 [4]	Direction Register Port 5	**$F8_H$** [1]	**FF_H**
	P6 [4]	Port 6	FA_H	FF_H
	DIR6 [4]	Direction Register Port 6	FA_H	FF_H
	P7	Port 7, Analog/Digital Input	DB_H	--
	P8	Port 8, Analog/Digital Input	DD_H	--
	P9 [4]	Port 9	$F9_H$	FF_H
	DIR9 [4]	Direction Register Port 9	$F9_H$	FF_H
Power Saving Modes	PCON	Power Control Register	87_H	00_H

[1] Bit-addressable special function registers
[2] This special function register is listed repeatedly since some bits of it also belong to other functional blocks.
[3] X means that the value is indeterminate and the location is reserved
[4] Register is mapped by bit PDIR.
[5] Register is mapped by bit RMAP.

Table 5
Contents of the SFRs, SFRs in numeric order of their addresses

Addr	Register	Content after Reset [1]	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Mapped by [2]
80_H	P0	FF_H	.7	.6	.5	.4	.3	.2	.1	.0	PDIR=0
80_H	DIR0	FF_H	.7	.6	.5	.4	.3	.2	.1	.0	PDIR=1
81_H	SP	07_H	.7	.6	.5	.4	.3	.2	.1	.0	–
82_H	DPL	00_H	.7	.6	.5	.4	.3	.2	.1	.0	–
83_H	DPH	00_H	.7	.6	.5	.4	.3	.2	.1	.0	–
84_H	WDTL	00_H	.7	.6	.5	.4	.3	.2	.1	.0	–
85_H	WDTH	00_H	.7	.6	.5	.4	.3	.2	.1	.0	–
86_H	WDTREL	00_H	WPSEL	.6	.5	.4	.3	.2	.1	.0	–
87_H	PCON	00_H	SMOD	PDS	IDLS	SD	GF1	GF0	PDE	IDLE	–
88_H	TCON	00_H	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	–
89_H	TMOD	00_H	GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0	–
$8A_H$	TL0	00_H	.7	.6	.5	.4	.3	.2	.1	.0	–
$8B_H$	TL1	00_H	.7	.6	.5	.4	.3	.2	.1	.0	–
$8C_H$	TH0	00_H	.7	.6	.5	.4	.3	.2	.1	.0	–
$8D_H$	TH1	00_H	.7	.6	.5	.4	.3	.2	.1	.0	–
90_H	P1	FF_H	T2	CLK-OUT	T2EX	$\overline{INT2}$	INT6	INT5	INT4	$\overline{INT3}$	PDIR=0
90_H	DIR1	FF_H	.7	.6	.5	.4	.3	.2	.1	.0	PDIR=1
91_H	XPAGE	00_H	.7	.6	.5	.4	.3	.2	.1	.0	–
92_H	DPSEL	XXXX. $X000_B$	–	–	–	–	–	.2	.1	.0	–
98_H	S0CON	00_H	SM0	SM1	SM20	REN0	TB80	RB80	TI0	RI0	–
99_H	S0BUF	XX_H	.7	.6	.5	.4	.3	.2	.1	.0	–
$9A_H$	IEN2	XX00. $00X0_B$	–	–	ECR	ECS	ECT	ECMP	–	ES1	–
$9B_H$	S1CON	0100. 0000_B	SM	S1P	SM21	REN1	TB81	RB81	TI1	RI1	–
$9C_H$	S1BUF	XX_H	.7	.6	.5	.4	.3	.2	.1	.0	–
$9D_H$	S1RELL	00_H	.7	.6	.5	.4	.3	.2	.1	.0	–
$A0_H$	P2	FF_H	.7	.6	.5	.4	.3	.2	.1	.0	PDIR=0
$A0_H$	DIR2	FF_H	.7	.6	.5	.4	.3	.2	.1	.0	PDIR=1
$A1_H$	COMSETL	00_H	.7	.6	.5	.4	.3	.2	.1	.0	–

1) X means that the value is indeterminate or the location is reserved.
2) SFRs with a comment in this column are mapped registers.
Shaded registers are bit-addressable special function registers.

Table 5
Contents of the SFRs, SFRs in numeric order of their addresses (cont'd)

Addr	Register	Content after Reset [1]	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Mapped by [2]
$A2_H$	COMSETH	00_H	.7	.6	.5	.4	.3	.2	.1	.0	–
$A3_H$	COMCLRL	00_H	.7	.6	.5	.4	.3	.2	.1	.0	–
$A4_H$	COMCLRH	00_H	.7	.6	.5	.4	.3	.2	.1	.0	–
$A5_H$	SETMSK	00_H	.7	.6	.5	.4	.3	.2	.1	.0	–
$A6_H$	CLRMSK	00_H	.7	.6	.5	.4	.3	.2	.1	.0	–
$A8_H$	IEN0	00_H	EAL	WDT	ET2	ES0	ET1	EX1	ET0	EX0	–
$A9_H$	IP0	00_H	OWDS	WDTS	.5	.4	.3	.2	.1	.0	–
AA_H	S0RELL	$D9_H$	.7	.6	.5	.4	.3	.2	.1	.0	–
$B0_H$	P3	FF_H	$\overline{RD}$	WR	T1	T0	$\overline{INT1}$	$\overline{INT0}$	TxD0	RxD0	PDIR=0
$B0_H$	DIR3	FF_H	.7	.6	.5	.4	.3	.2	.1	.0	PDIR=1
$B1_H$	SYSCON	1010. $XX01_B$	CLKP	PMOD	1	RMAP	–	–	XMAP1	XMAP0	–
$B2_H$	SYSCON1 [3]	00XX. $XEE0_B$	ESWC	SWC	–	EA1	EA0	PRGEN1	PRGEN0	SWAP	–
$B4_H$	PRSC	1101. 0101_B	WDTP	S0P	T2P1	T2P0	T1P1	T1P0	T0P1	T0P0	–
$B8_H$	IEN1	00_H	EXEN2	SWDT	EX6	EX5	EX4	EX3	EX2	EADC	–
$B9_H$	IP1	0X00. 0000_B	PDIR	–	.5	.4	.3	.2	.1	.0	–
BA_H	S0RELH	XXXX. $XX11_B$	–	–	–	–	–	–	.1	.0	–
BB_H	S1RELH	XXXX. $XX11_B$	–	–	–	–	–	–	.1	.0	–
BC_H	CT1CON	X1XX. 0000_B	–	CT1P	–	–	CT1F	CLK12	CLK11	CLK10	–
BE_H	IEN3	XXXX. $00XX_B$	–	–	–	–	ECT1	ECC1	–	–	–
BF_H	IRCON2	00_H	ICC17	ICC16	ICC15	ICC14	ICC13	ICC12	ICC11	ICC10	PDIR=0
BF_H	EICC1	FF_H	EICC17	EICC16	EICC15	EICC14	EICC13	EICC12	EICC11	EICC10	PDIR=1
$C0_H$	IRCON0	00_H	EXF2	TF2	IEX6	IEX5	IEX4	IEX3	IEX2	IADC	–
$C1_H$	CCEN	00_H	COCAH3	COCAL3	COCAH2	COCAL2	COCAH1	COCAL1	COCAH0	COCAL0	–

1) X means that the value is indeterminate or the location is reserved.
2) SFRs with a comment in this column are mapped registers.
3) "E" means that the value of the bit is defined by the logic level at pin PRGEN at the rising edge of the $\overline{RESET}$ or $\overline{HWPD}$ signals.
Shaded registers are bit-addressable special function registers.

Table 5
Contents of the SFRs, SFRs in numeric order of their addresses (cont'd)

Addr	Register	Content after Reset [1]	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Mapped by [2]
$C2_H$	CCL1	00_H	.7	.6	.5	.4	.3	.2	.1	.0	–
$C3_H$	CCH1	00_H	.7	.6	.5	.4	.3	.2	.1	.0	–
$C4_H$	CCL2	00_H	.7	.6	.5	.4	.3	.2	.1	.0	–
$C5_H$	CCH2	00_H	.7	.6	.5	.4	.3	.2	.1	.0	–
$C6_H$	CCL3	00_H	.7	.6	.5	.4	.3	.2	.1	.0	–
$C7_H$	CCH3	00_H	.7	.6	.5	.4	.3	.2	.1	.0	–
$C8_H$	T2CON	00_H	T2PS	I3FR	I2FR	T2R1	T2R0	T2CM	T2I1	T2I0	–
$C9_H$	CC4EN	00_H	COCO EN1	COCO N2	COCO N1	COCO N0	COCO EN0	COCAH 4	COCAL 4	COM0	–
CA_H	CRCL	00_H	.7	.6	.5	.4	.3	.2	.1	.0	–
CB_H	CRCH	00_H	.7	.6	.5	.4	.3	.2	.1	.0	–
CC_H	TL2	00_H	.7	.6	.5	.4	.3	.2	.1	.0	–
CD_H	TH2	00_H	.7	.6	.5	.4	.3	.2	.1	.0	–
CE_H	CCL4	00_H	.7	.6	.5	.4	.3	.2	.1	.0	–
CF_H	CCH4	00_H	.7	.6	.5	.4	.3	.2	.1	.0	–
$D0_H$	PSW	00_H	CY	AC	F0	RS1	RS0	OV	F1	P	–
$D1_H$	IRCON1	00_H	ICMP7	ICMP6	ICMP5	ICMP4	ICMP3	ICMP2	ICMP1	ICMP0	–
$D2_H$	CML0	00_H	.7	.6	.5	.4	.3	.2	.1	.0	RMAP=0
$D2_H$	CC1L0	00_H	.7	.6	.5	.4	.3	.2	.1	.0	RMAP=1
$D3_H$	CMH0	00_H	.7	.6	.5	.4	.3	.2	.1	.0	RMAP=0
$D3_H$	CC1H0	00_H	.7	.6	.5	.4	.3	.2	.1	.0	RMAP=1
$D4_H$	CML1	00_H	.7	.6	.5	.4	.3	.2	.1	.0	RMAP=0
$D4_H$	CC1L1	00_H	.7	.6	.5	.4	.3	.2	.1	.0	RMAP=1
$D5_H$	CMH1	00_H	.7	.6	.5	.4	.3	.2	.1	.0	RMAP=0
$D5_H$	CC1H1	00_H	.7	.6	.5	.4	.3	.2	.1	.0	RMAP=1
$D6_H$	CML2	00_H	.7	.6	.5	.4	.3	.2	.1	.0	RMAP=0
$D6_H$	CC1L2	00_H	.7	.6	.5	.4	.3	.2	.1	.0	RMAP=1
$D7_H$	CMH2	00_H	.7	.6	.5	.4	.3	.2	.1	.0	RMAP=0
$D7_H$	CC1H2	00_H	.7	.6	.5	.4	.3	.2	.1	.0	RMAP=1
$D8_H$	ADCON0	00_H	BD	CLK	ADEX	BSY	ADM	MX2	MX1	MX0	–
$D9_H$	ADDATH	00_H	.7 (MSB)	.6	.5	.4	.3	.2	.1	.0	–

1) X means that the value is indeterminate or the location is reserved.
2) SFRs with a comment in this column are mapped registers.
Shaded registers are bit-addressable special function registers.

Table 5
Contents of the SFRs, SFRs in numeric order of their addresses (cont'd)

Addr	Register	Content after Reset [1]	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Mapped by [2]
DA_H	ADDATL	00_H	.7	.6 (LSB)	–	–	–	–	–	–	–
DB_H	P7	–	.7	.6	.5	.4	.3	.2	.1	.0	–
DC_H	ADCON1	0100.0000_B	ADCL1	ADCL0	ADST1	ADST0	MX3	MX2	MX1	MX0	–
DD_H	P8	–	–	.6	.5	.4	.3	.2	.1	.0	–
DE_H	CTRELL	00_H	.7	.6	.5	.4	.3	.2	.1	.0	RMAP=0
DE_H	CT1RELL	00_H	.7	.6	.5	.4	.3	.2	.1	.0	RMAP=1
DF_H	CTRELH	00_H	.7	.6	.5	.4	.3	.2	.1	.0	RMAP=0
DF_H	CT1RELH	00_H	.7	.6	.5	.4	.3	.2	.1	.0	RMAP=1
$E0_H$	ACC	00_H	.7	.6	.5	.4	.3	.2	.1	.0	–
$E1_H$	CTCON	0100.0000_B	T2PS1	CTP	ICR	ICS	CTF	CLK2	CLK1	CLK0	–
$E2_H$	CML3	00_H	.7	.6	.5	.4	.3	.2	.1	.0	RMAP=0
$E2_H$	CC1L3	00_H	.7	.6	.5	.4	.3	.2	.1	.0	RMAP=1
$E3_H$	CMH3	00_H	.7	.6	.5	.4	.3	.2	.1	.0	RMAP=0
$E3_H$	CC1H3	00_H	.7	.6	.5	.4	.3	.2	.1	.0	RMAP=1
$E4_H$	CML4	00_H	.7	.6	.5	.4	.3	.2	.1	.0	RMAP=0
$E4_H$	CC1L4	00_H	.7	.6	.5	.4	.3	.2	.1	.0	RMAP=1
$E5_H$	CMH4	00_H	.7	.6	.5	.4	.3	.2	.1	.0	RMAP=0
$E5_H$	CC1H4	00_H	.7	.6	.5	.4	.3	.2	.1	.0	RMAP=1
$E6_H$	CML5	00_H	.7	.6	.5	.4	.3	.2	.1	.0	RMAP=0
$E6_H$	CC1L5	00_H	.7	.6	.5	.4	.3	.2	.1	.0	RMAP=1
$E7_H$	CMH5	00_H	.7	.6	.5	.4	.3	.2	.1	.0	RMAP=0
$E7_H$	CC1H5	00_H	.7	.6	.5	.4	.3	.2	.1	.0	RMAP=1
$E8_H$	P4	FF_H	CM7	CM6	CM5	CM4	CM3	CM2	CM1	CM0	PDIR=0
$E8_H$	DIR4	FF_H	.7	.6	.5	.4	.3	.2	.1	.0	PDIR=1
$E9_H$	MD0	XX_H	.7	.6	.5	.4	.3	.2	.1	.0	–
EA_H	MD1	XX_H	.7	.6	.5	.4	.3	.2	.1	.0	–
EB_H	MD2	XX_H	.7	.6	.5	.4	.3	.2	.1	.0	–
EC_H	MD3	XX_H	.7	.6	.5	.4	.3	.2	.1	.0	–
ED_H	MD4	XX_H	.7	.6	.5	.4	.3	.2	.1	.0	–

1) X means that the value is indeterminate or the location is reserved.
2) SFRs with a comment in this column are mapped registers.
Shaded registers are bit-addressable special function registers.

Table 5
Contents of the SFRs, SFRs in numeric order of their addresses (cont'd)

Addr	Register	Content after Reset [1]	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Mapped by [2]
EE_H	MD5	XX_H	.7	.6	.5	.4	.3	.2	.1	.0	–
EF_H	ARCON	0XXX. XXXX_B	MDEF	MDOV	SLR	SC.4	SC.3	SC.2	SC.1	SC.0	–
$F0_H$	B	00_H	.7	.6	.5	.4	.3	.2	.1	.0	–
$F2_H$	CML6	00_H	.7	.6	.5	.4	.3	.2	.1	.0	RMAP=0
$F2_H$	CC1L6	00_H	.7	.6	.5	.4	.3	.2	.1	.0	RMAP=1
$F3_H$	CMH6	00_H	.7	.6	.5	.4	.3	.2	.1	.0	RMAP=0
$F3_H$	CC1H6	00_H	.7	.6	.5	.4	.3	.2	.1	.0	RMAP=1
$F4_H$	CML7	00_H	.7	.6	.5	.4	.3	.2	.1	.0	RMAP=0
$F4_H$	CC1L7	00_H	.7	.6	.5	.4	.3	.2	.1	.0	RMAP=1
$F5_H$	CMH7	00_H	.7	.6	.5	.4	.3	.2	.1	.0	RMAP=0
$F5_H$	CC1H7	00_H	.7	.6	.5	.4	.3	.2	.1	.0	RMAP=1
$F6_H$	CMEN	00_H	.7	.6	.5	.4	.3	.2	.1	.0	RMAP=0
$F6_H$	CC1EN	00_H	.7	.6	.5	.4	.3	.2	.1	.0	RMAP=1
$F7_H$	CMSEL	00_H	.7	.6	.5	.4	.3	.2	.1	.0	RMAP=0
$F7_H$	CAFR	00_H	.7	.6	.5	.4	.3	.2	.1	.0	RMAP=1
$F8_H$	P5	FF_H	CCM7	CCM6	CCM5	CCM4	CCM3	CCM2	CCM1	CCM0	PDIR=0
$F8_H$	DIR5	FF_H	.7	.6	.5	.4	.3	.2	.1	.0	PDIR=1
$F9_H$	P9	FF_H	CC17	CC16	CC15	CC14	CC13	CC12	CC11	CC10	PDIR=0
$F9_H$	DIR9	FF_H	.7	.6	.5	.4	.3	.2	.1	.0	PDIR=1
FA_H	P6	FF_H	.7	.6.	.5	.4	.3	TxD1	RxD1	$\overline{ADST}$	PDIR=0
FA_H	DIR6	FF_H	.7	.6	.5	.4	.3	.2	.1	.0	PDIR=1

1) X means that the value is indeterminate or the location is reserved.
2) SFRs with a comment in this column are mapped registers.
Shaded registers are bit-addressable special function registers.

Digital I/O Ports

The C509-L allows for digital I/O on 64 lines grouped into 8 bidirectional 8-bit ports. Each port bit consists of a latch, an output driver and an input buffer. Read and write accesses to the I/O ports P0 through P6 and P9 are performed via their corresponding special function registers P0 to P6 and P9. The port structure of the C509-L is designed to operate either as a quasi-bidirectional port structure, compatible to the standard 8051-Family, or as a genuine bidirectional port structure. This port operating mode can be selected by software (setting or clearing the bit PMOD in the SFR SYSCON).

The output drivers of port 0 and 2 and the input buffers of port 0 are also used for accessing external memory. In this application, port 0 outputs the low byte of the external memory address, time-multiplexed with the byte being written or read. Port 2 outputs the high byte of the external memory address when the address is 16 bits wide. Otherwise, the port 2 pins continue emitting the P2 SFR contents.

Analog Input Ports

Ports 7 and 8 are available as input ports only and provide for two functions. When used as digital inputs, the corresponding SFR's P7 and P8 contain the digital value applied to port 7 and port 8 lines. When used for analog inputs the desired analog channel is selected by a three-bit field in SFR ADCON0 or a four-bit field in SFR ADCON1. Of course, it makes no sense to output a value to these input-only ports by writing to the SFR's P7 or P8; this will have no effect.

lf a digital value is to be read, the voltage levels are to be held within the input voltage specifications (V_{IL}/V_{IH}). Since P7 and P8 are not bit-addressable registers, all input lines of P7 or P8 are read at the same time by byte instructions.

Nevertheless, it is possible to use ports 7 and 8 simultaneously for analog and digital input. However, care must be taken that all bits of P7 or P8 that have an undetermined value caused by their analog function are masked.

Port Structure Selection

After a reset operation of the C509-L, the quasi-bidirectional 8051-compatible port structure is selected. For selection of the bidirectional port structure (CMOS) the bit PMOD of SFR SYSCON must be set. Because each port pin can be programmed as an input or an output, additionally, after the selection of the bidirectional mode the direction register of the ports must be written (except the analog/digital input ports 7,8). This direction registers are mapped to the port registers. This means, the port register address is equal to its direction register address. **Figure 16** illustrates the port- and direction register configuration.

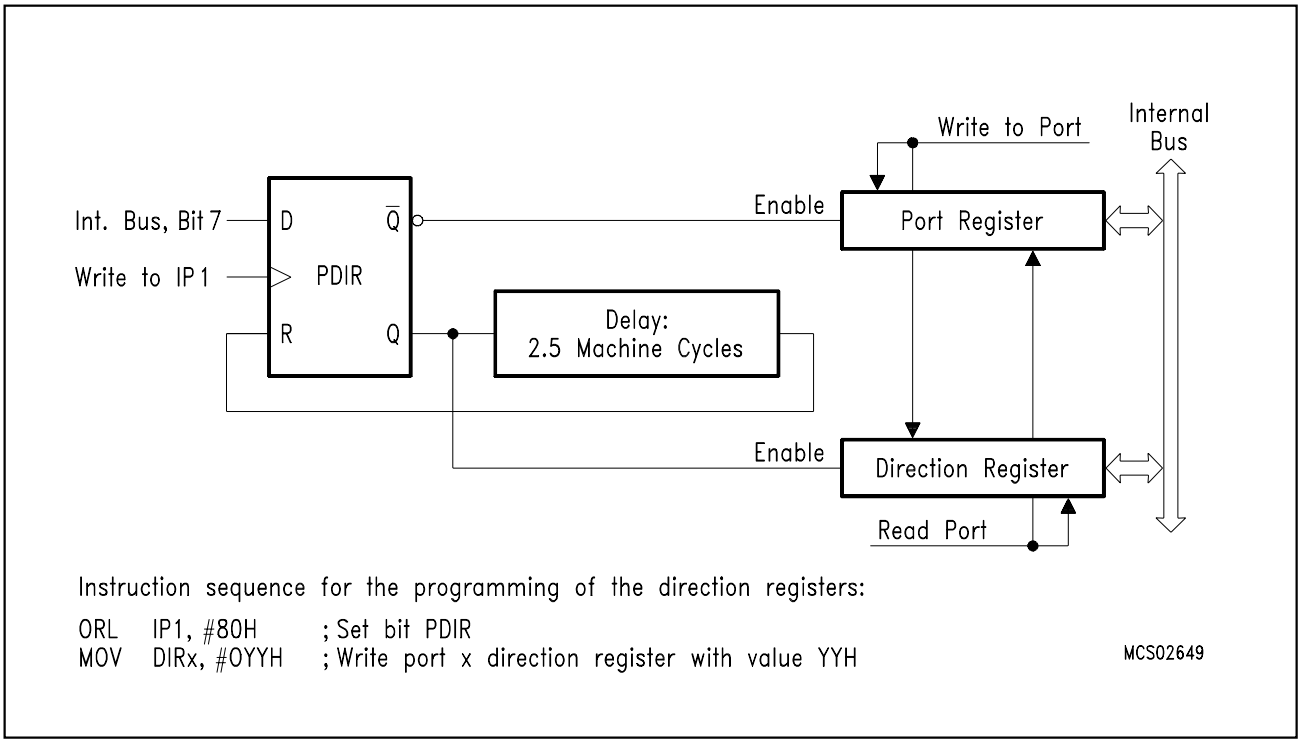


Figure 16
Port Register, Direction Register

For the access the direction registers a double instruction sequence must be executed. The first instruction has to set bit PDIR in SFR IP1. Thereafter, a second instruction can read or write the direction registers. PDIR will automatically be cleared after the second machine cycle (S2P2) after having been set. For this time, the access to the direction register is enabled and the register can be read or written. Further, the double instruction sequence as shown in **figure 16**, cannot be interrupted by an interrupt,

When the bidirectional port structure is activated (bit PMOD in SFR SYSCON =1) after a reset, the ports are defined as inputs (direction registers default values after reset are set to FF_H).

With PMOD = 0 (quasi-bidirectional port structure selected), any access to the direction registers has no effect on the port driver circuitries.

Timer / Counter 0 and 1

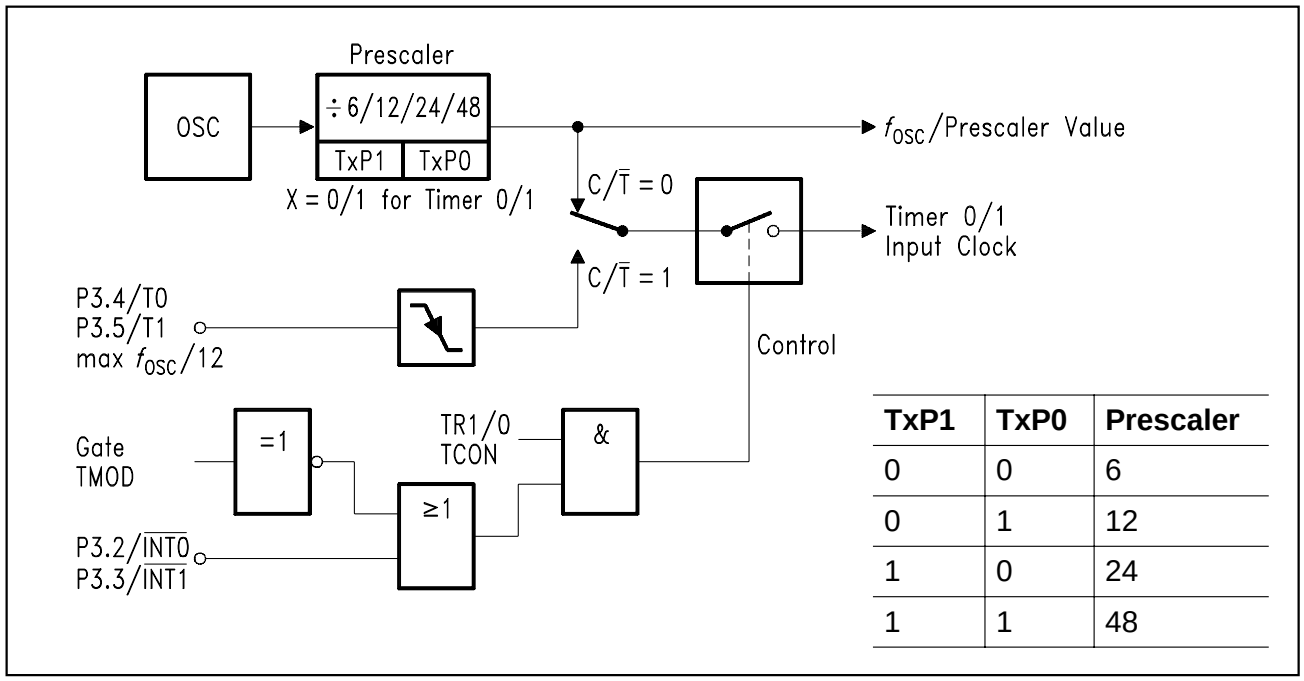
Timer/Counter 0 and 1 can be used in four operating modes as listed in **table 6** :

Table 6
Timer/Counter 0 and 1 Operating Modes

Mode	Description	TMOD		Input Clock	
		M1	M0	internal	external (max)
0	8-bit timer/counter with a divide-by-32 prescaler	0	0	f_{osc}/6x32 up to f_{osc}/48x32	f_{osc}/12x32
1	16-bit timer/counter	0	1	f_{osc}/6 up to f_{osc}/48	f_{osc}/12
2	8-bit timer/counter with 8-bit autoreload	1	0		
3	Timer/counter 0 used as one 8-bit timer/counter and one 8-bit timer Timer 1 stops	1	1		

In the “timer” function (C/$\overline{T}$ = ‘0’) the register is incremented by a count rate of f_{osc}/6 up to f_{osc}/32.

In the “counter” function the register is incremented in response to a 1-to-0 transition at its corresponding external input pin (P3.4/T0, P3.5/T1). Since it takes two machine cycles to detect a falling edge the max. count rate is f_{osc}/12. External inputs $\overline{INT0}$ and $\overline{INT1}$ (P3.2, P3.3) can be programmed to function as a gate to facilitate pulse width measurements. **Figure 17** illustrates the input clock logic of timer 0/1.



TxP1	TxP0	Prescaler
0	0	6
0	1	12
1	0	24
1	1	48

Figure 17
Timer/Counter 0 and 1 Input Clock Logic

Compare / Capture Unit (CCU)

The compare/capture unit can be used in all kinds of digital signal generation and event capturing like pulse generation, pulse width modulation, pulse width measuring etc. The CCU consists of three 16-bit timer/counters and an array of several compare or compare/capture registers. A set of control registers is used for flexible adapting of the CCU to a wide variety of applications.

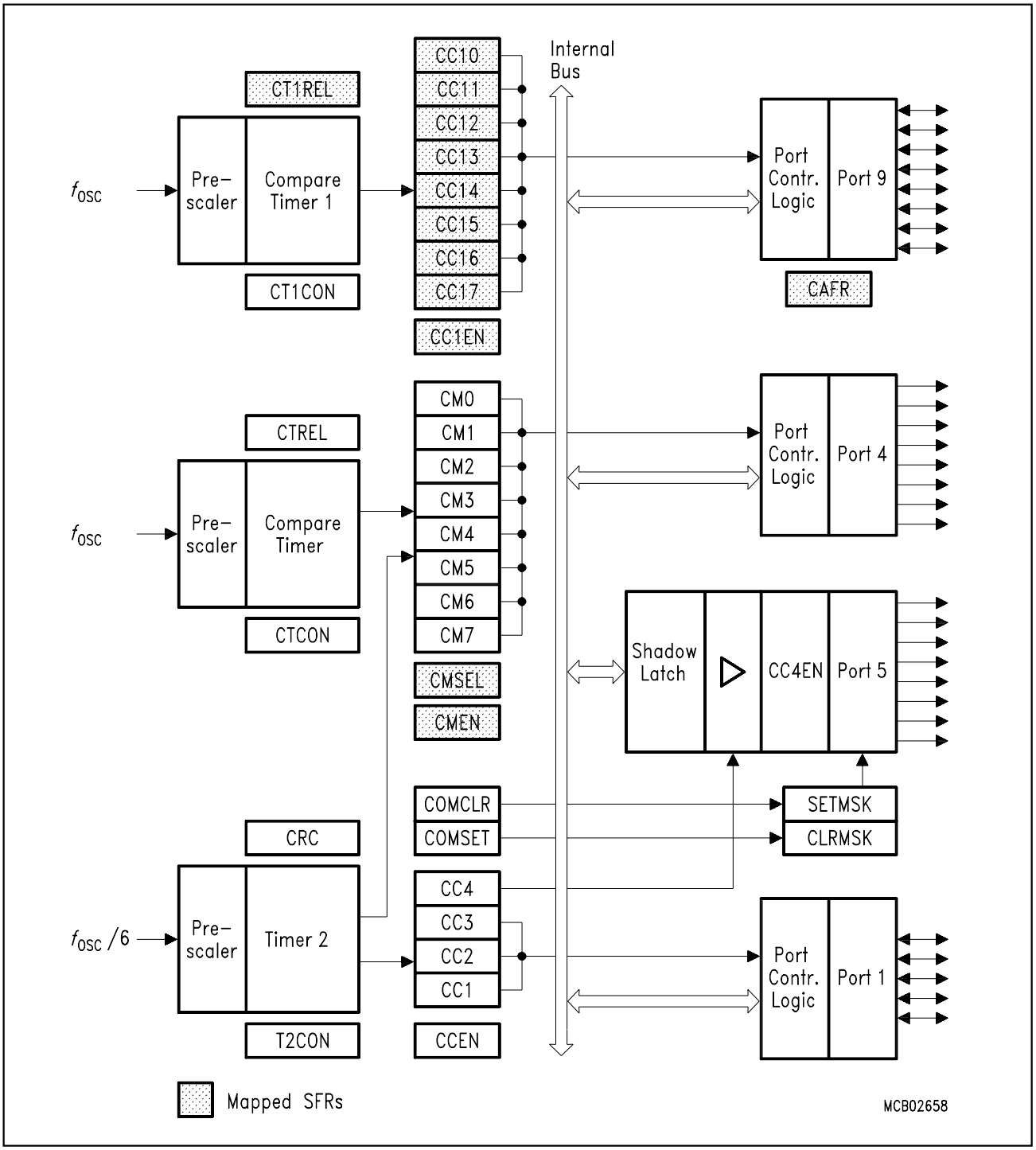


Figure 18
Block Diagram of the CCU

The block diagram in **figure 18** shows the general configuration of the CCU. All CC1 to CC4 registers and the CRC register are exclusively assigned to timer 2. Each of the eight compare registers CM0 through CM7 can either be assigned to timer 2 or to the faster compare timer, e.g. to provide up to 8 PWM output channels. The assignment of the CMx registers - which can be done individually for every single register - is combined with an automatic selection of one of the two possible compare modes. The compare/capture registers CC10 to CC17 and the reload register CT1REL are assigned to compare timer 1 and are mapped to the corresponding registers of the compare timer.

The compare function and the reaction of the corresponding outputs depend on the timer/compare register combination. **Table 7** shows the possible configurations of the CCU and the corresponding compare modes which can be selected. The following sections describe the function of these configurations.

Table 7
CCU Configurations

Assigned Timer	Compare Register	Compare Output at	Possible Modes
Timer 2	CRCH/CRCL CCH1/CCL1 CCH2/CCL2 CCH3/CCL3 CCH4/CCL4	P1.0/$\overline{\text{INT3}}$/CC0 P1.1/INT4/CC1 P1.2/INT5/CC2 P1.3/INT6/CC3 P1.4/$\overline{\text{INT2}}$/CC4	Compare mode 0, 1 + Reload Compare mode 0, 1 / capture Compare mode 0, 1 / capture Compare mode 0, 1 / capture Compare mode 0, 1 / capture)
	CCH4/CCL4	P1.4/$\overline{\text{INT2}}$/CC4 P5.0/CCM0 to P5.7/CCM7	Compare mode 1 “Concurrent compare“
	CMH0/CML0 to CMH7/CML7	P4.0/CM0 to P4.7/CM7	Compare mode 0
	COMSET COMCLR	P5.0/CCM0 to P5.7/CCM7	Compare mode 2
Compare Timer	CMH0/CML0 to CMH7/CML7	P4.0/CM0 to P4.7/CM7	Compare mode 1
Compare Timer 1	CC1H0/CC1L0 to CC1H7/CC1L7	P5.0/CCM0 to P5.7/CCM7	Compare mode 0 / capture

Timer 2 Operation

Gated Timer Mode : In gated timer function, the external input pin P1.7/T2 operates as a gate to the input of timer 2. If T2 is high, the internal clock input is gated to the timer. T2 = 0 stops the counting procedure.The external gate signal is sampled once every machine cycle.

Event Counter Mode : In the event counter function, the timer 2 is incremented in response to a 1-to-0 transition at its corresponding external input pin P1.7/T2. In this function, the external input is sampled every machine cycle. The maximum count rate is 1/12 of the oscillator frequency.

Reload of Timer 2 : Two reload modes are selectable:
In mode 0, when timer 2 rolls over from all 1's to all 0's, it not only sets TF2 but also causes the timer 2 registers to be loaded with the 16-bit value in the CRC register, which is preset by software.
In mode 1, a 16-bit reload from the CRC register is caused by a negative transition at the corresponding input pin P1.5/T2EX.

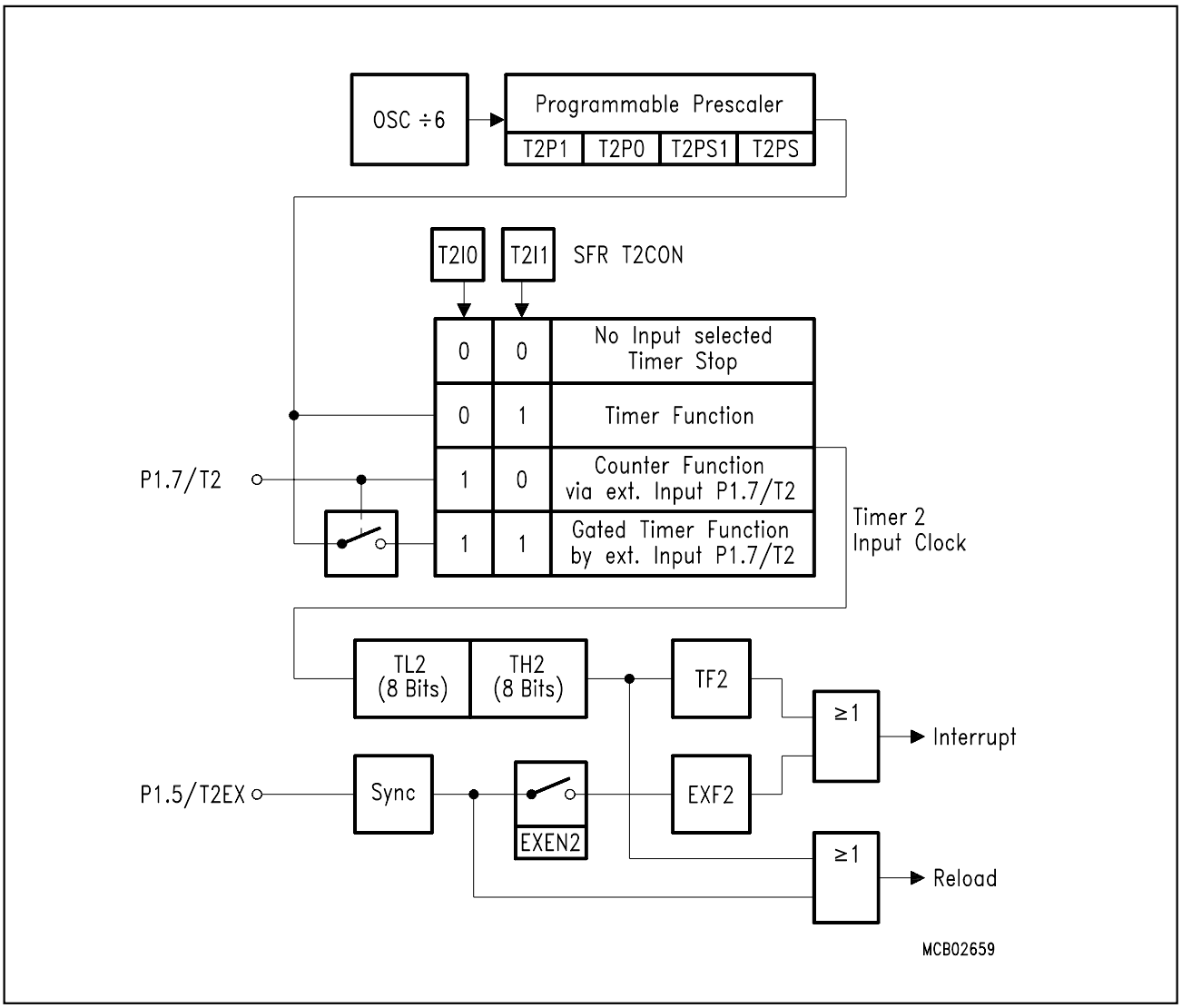


Figure 19
Block Diagram of Timer 2

Compare Timer Operation

The compare timers receive its input clock from a programmable prescaler which provides input frequencies, ranging from f_{OSC} up to $f_{OSC}/256$. The compare timers are, once started, free-running 16-bit timers, which on overflow are automatically reloaded by the contents of the 16-bit reload registers. The compare timers have - as any other timer in the C509-L - their own interrupt request flags CTF and CT1F. These flags are set when the timer count rolls over from all ones to the reload value. **Figure 20** shows the block diagram of compare timer and compare timer 1.

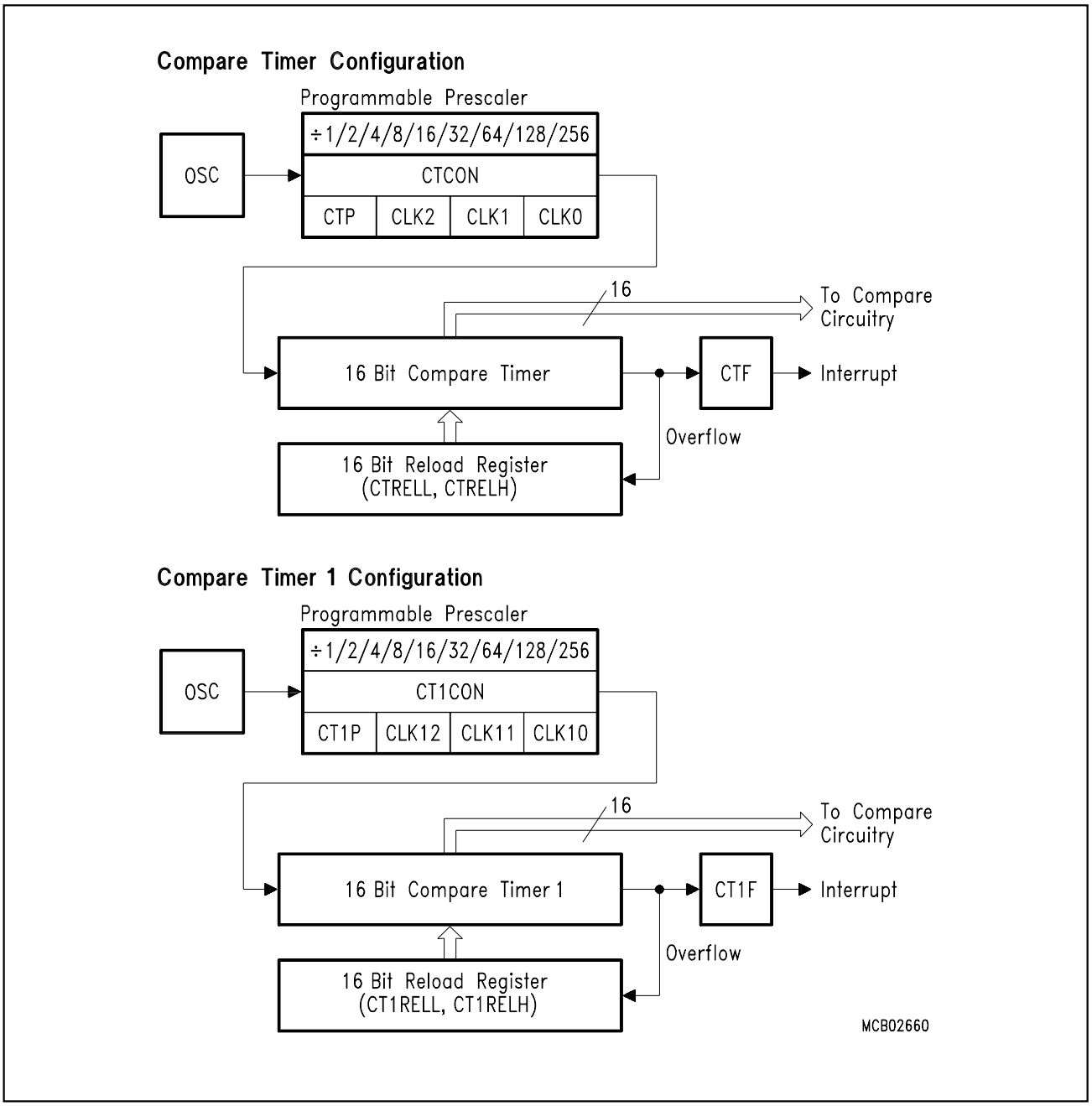


Figure 20
Compare Timer and Compare Timer 1 Block Diagram

Compare Modes

The compare function of a timer/register combination operates as follows. the 16-bit value stored in a compare or compare/capture register is compared with the contents of the timer register. If the count value in the timer register matches the stored value, an appropriate output signal is generated at a corresponding port pin. Several timer/compare register combinations are selectable (see **table 7**). In these configurations three cdifferent ompare modes are selectable.

Compare Mode 0

In compare mode 0, upon matching the timer and compare register contents, the output signal changes from low to high. lt goes back to a low level on timer overflow. As long as compare mode 0 is enabled, the appropriate output pin is controlled by the timer circuit only and writing to the port will have no effect. **Figure 21** shows a functional diagram of a port circuit when used in compare mode 0. The port latch is directly controlled by the timer overflow and compare match signals. The input line from the internal bus and the write-to-latch line of the port latch are disconnected when compare mode 0 is enabled.

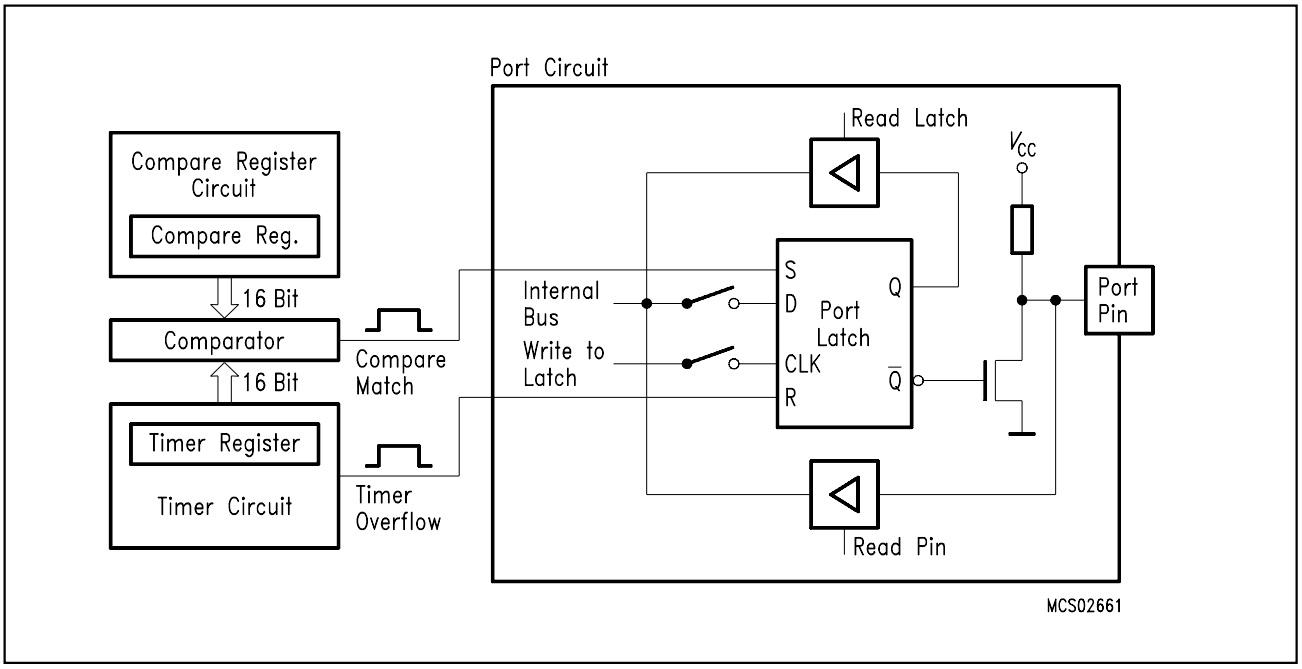


Figure 21
Port Latch in Compare Mode 0

Compare Mode 1

Ilf compare mode 1 is enabled (can only be selected for compare registers assigned to timer 2) and the software writes to the appropriate output latch at the port, the new value will not appear at the output pin until the next compare match occurs. Thus, it can be choosen whether the output signal has to make a new transition (1-to-0 or 0-to-1, depending on the actual pin-level) or should keep its old value at the time when the timer value matches the stored compare value.

In compare mode 1 (see **figure 22**) the port circuit consists of two separate latches. One latch (which acts as a "shadow latch") can be written under software control, but its value will only be transferred to the port latch (and thus to the port pin) when a compare match occurs.

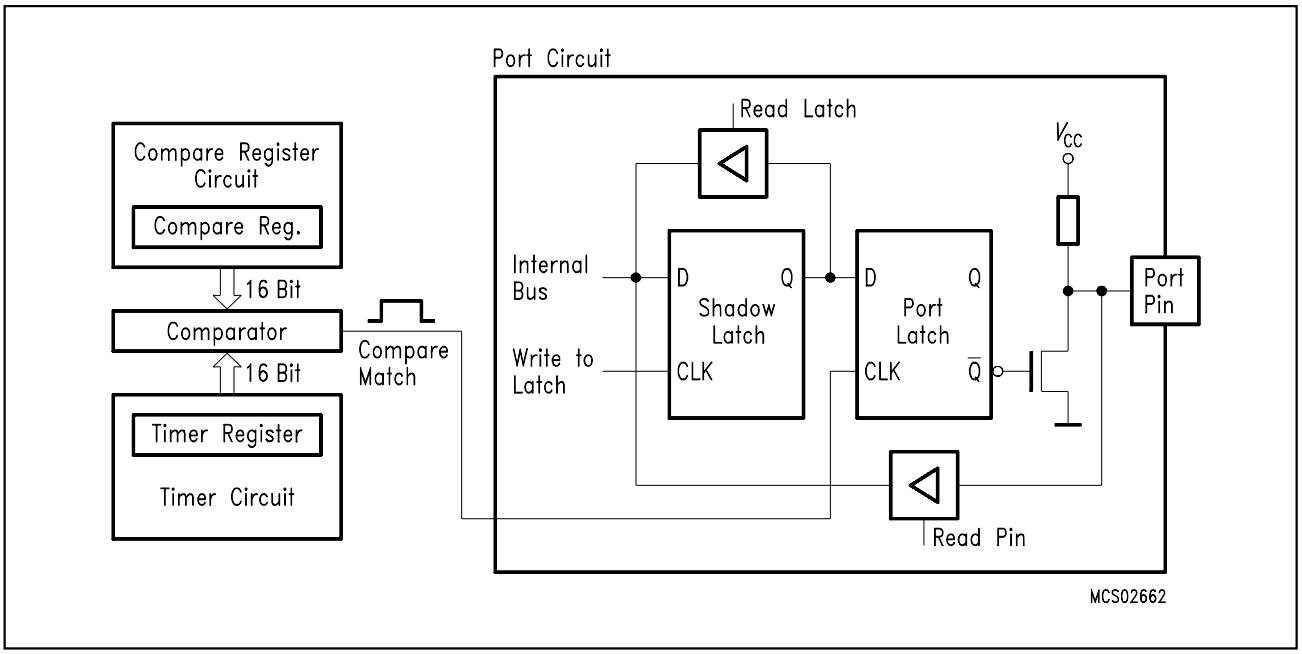


Figure 22
Compare Function in Compare Mode 1

Compare Mode 2

In the compare mode 2 the port 5 pins are under control of compare/capture register CC4, but under control of the compare registers COMSET and COMCLR. When a compare match occurs with register COMSET, a high level appears at the pins of port 5 when the corresponding bits in the mask register SETMSK are set. When a compare match occurs with register COMCLR, a low level appears at the pins of port 5 when the corresponding bits in the mask register CLRMSK are set.

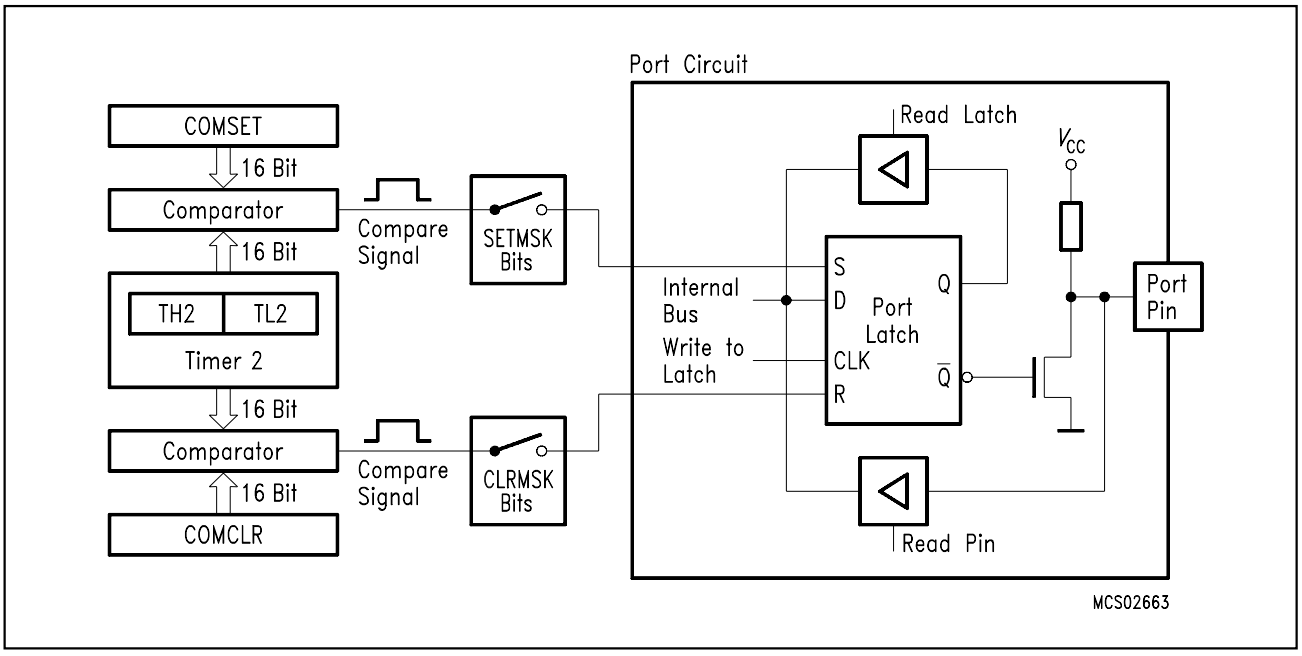


Figure 23
Compare Function of Compare Mode 2

Multiplication / Division Unit (MDU)

This on-chip arithmetic unit of the C509-L provides fast 32-bit division, 16-bit multiplication as well as shift and normalize features. All operations are unsigned integer operations. **Table 8** describes the five general operations the MDU is able to perform.

Table 8
MDU Operation Characteristics

Operation	Result	Remainder	Execution Time
32bit/16bit	32bit	16bit	6 t_{CY} 1)
16bit/16bit	16bit	16bit	4 t_{CY} 1)
16bit x 16bit	32bit	–	4 t_{CY} 1)
32-bit normalize	–	–	6 t_{CY} 2)
32-bit shift L/R	–	–	6 t_{CY} 2)

1) 1 t_{CY} = 6 • CLP = 1 machine cycle = 375 ns at 16-MHz oscillator frequency
2) The maximal shift speed is 6 shifts per machine cycle

The MDU consists of seven special function registers (MD0-MD5, ARCON) which are used as operand, result, and control registers. The three operation phases are shown in **figure 24**.

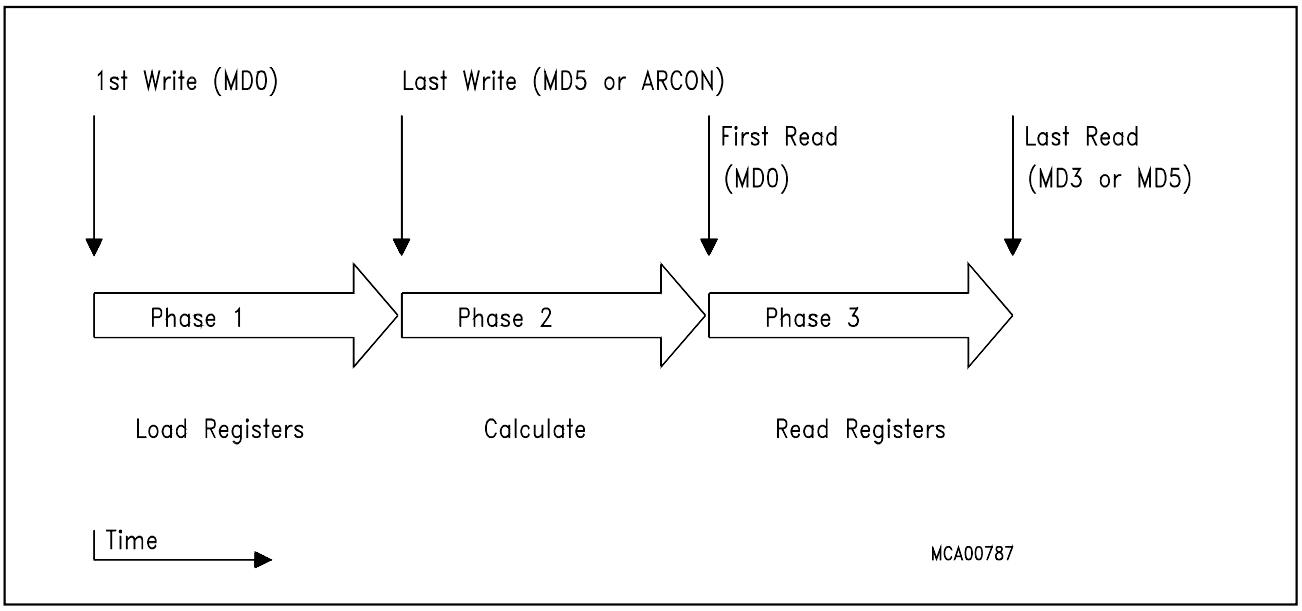


Figure 24
Operating Phases of the MDU

For starting an operation, registers MD0 to MD5 and ARCON must be written to in a certain sequence according table 8 and 9. The order the registers are accessed determines the type of the operation. A shift operation is started by a final write operation to SFR ARCON.

Table 9
Programming the MDU for Multiplication and Division

Operation	32Bit/16Bit		16Bit/16Bit		16Bit x 16Bit	
First Write	MD0	D'endL	MD0	D'endL	MD0	M'andL
	MD1	D'end	MD1	D'endH	MD4	M'orL
	MD2	D'end				
	MD3	D'endH	MD4	D'orL	MD1	M'andH
	MD4	D'orL				
Last Write	MD5	D'orH	MD5	D'orH	MD5	M'orH
First Read	MD0	QuoL	MD0	QuoL	MD0	PrL
	MD1	Quo	MD1	QuoH	MD1	
	MD2	Quo				
	MD3	QuoH	MD4	RemL	MD2	
	MD4	RemL				
Last Read	MD5	RemH	MD5	RemH	MD3	PrH

Abbrevations :

D'end : Dividend, 1st operand of division
D'or : Divisor, 2nd operand of division
M'and : Multiplicand, 1st operand of multiplication
M'or : Multiplicator, 2nd operand of multiplication
Pr : Product, result of multiplication
Rem : Remainder
Quo : Quotient, result of division
...L : means, that this byte is the least significant of the 16-bit or 32-bit operand
...H : means, that this byte is the most significant of the 16-bit or 32-bit operand

Table 10
Programming athe MDU for a Shift or Normalize Operation

Operation	Normalize, Shift Left, Shift Right	
First write	MD0	least significant byte
	MD1	.
	MD2	.
	MD3	most significant byte
Last write	ARCON	start of conversion
First read	MD0	least significant byte
	MD1	.
	MD2	.
Last read	MD3	most significant byte

Serial Interfaces 0 and 1

The C509-L has two serial interfaces which are functionally nearly identical concerning the asynchronous modes of operation. The two channels are full-duplex, meaning they can transmit and receive simultaneously. The serial channel 0 is completely compatible with the serial channel of the C501 (one synchronous mode, three asynchronous modes). Serial channel 1 has the same functionality in its asynchronous modes, but the synchronous mode and the fixed baud rate UART mode is missing.

The operating modes of the serial interfaces is illustrated in **table 11**. The possible baudrates can be calculated using the formulas given in **table 12**.

Table 11
Operating Modes of Serial Interface 0 and 1

Serial Interface	Mode	S0CON		S1CON	Description
		SM0	SM1	SM	
0	0	0	0	–	Shift register mode Serial data enters and exits through R×D0; T×D0 outputs the shift clock; 8-bit are transmitted/received (LSB first); fixed baud rate
	1	0	1	–	8-bit UART, variable baud rate 10 bits are transmitted (through T×D0) or received (at R×D0)
	2	1	0	–	9-bit UART, fixed baud rate 11 bits are transmitted (through T×D0) or received (at R×D0)
	3	1	1	–	9-bit UART, variable baud rate Like mode 2
1	A	–	–	0	9-bit UART; variable baud rate 11 bits are transmitted (through T×D1) or received (at R×D1)
	B	–	–	1	8-bit UART; variable baud rate 10 bits are transmitted (through T×D1) or received (at R×D1)

For clarification some terms regarding the difference between "baud rate clock" and "baud rate" should be mentioned. In the asynchronous modes the serial interfaces require a clock rate which is 16 times the baud rate for internal synchronization. Therefore, the baud rate generators/timers have to provide a "baud rate clock" (output signal in **figure 25** and **figure 26**) to the serial interface which - there divided by 16 - results in the actual "baud rate". Further, the abrevation f_{OSC} refers to the oscillator frequency (crystal or external clock operation).

The variable baud rates for modes 1 and 3 of the serial interface 0 can be derived from either timer 1 or a decdicated baud rate generator (see **figure 25**). The variable baud rates for modes A and B of the serial interface 1 are derived from a decdicated baud rate generator as shown in **figure 26**.

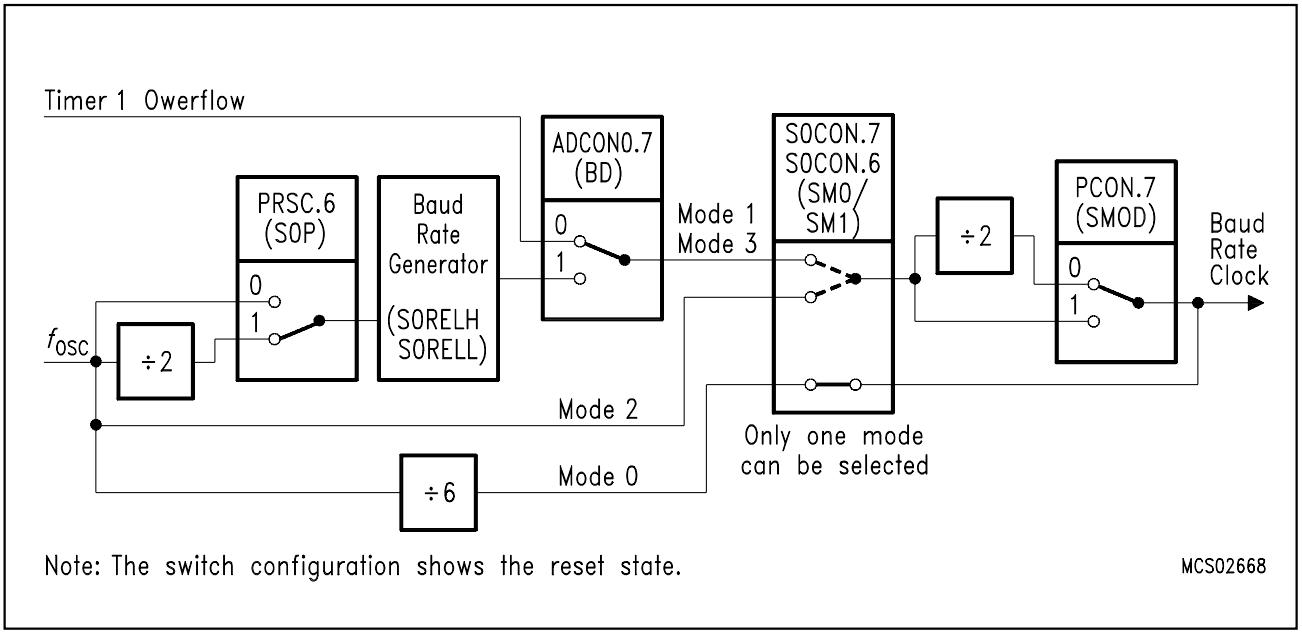


Figure 25
Serial Interface 0 : Baud Rate Generation Configuration

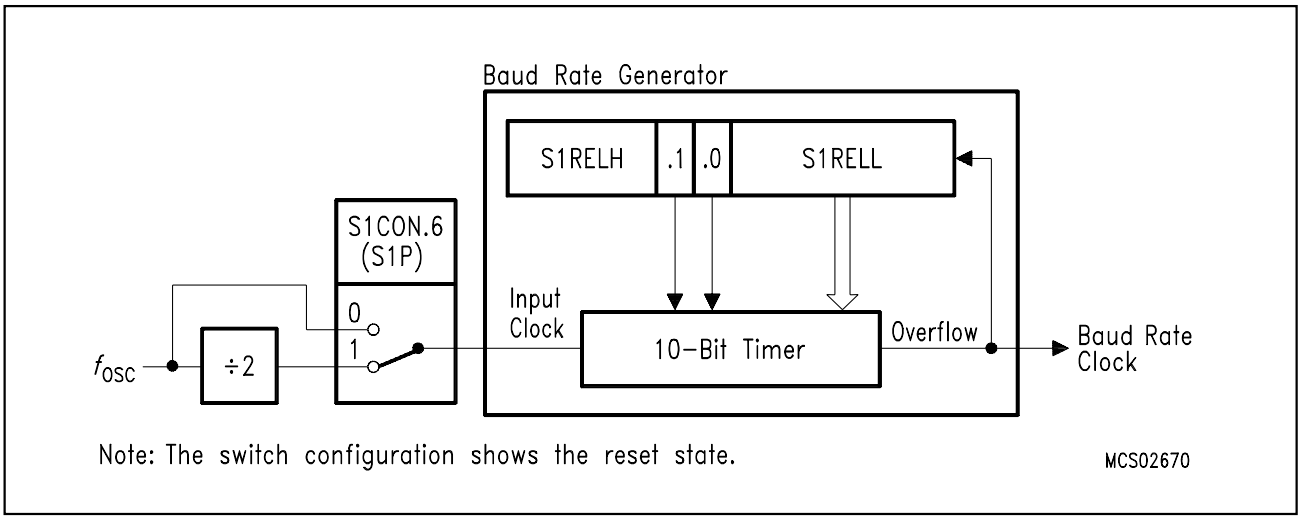


Figure 26
Serial Interface 1 : Baud Rate Generator Configuration

Table 12 below lists the values/formulas for the baud rate calculation of serial interface 0 and 1 with its dependencies of the control bits BD, SMOD, S0P, and S1P.

Table 12
Serial Interface 0 - Baud Rate Dependencies

Serial Interface 0 Operating Modes	Active Control Bits				Baud Rate Calculation
	BD	S0P	SMOD	S1P	
Mode 0 (Shift Register)	–	–	–	–	f_{OSC} / 6
Mode 1 (8-bit UART) Mode 3 (9-bit UART)	0	–	0 or 1	–	Controlled by timer 1 overflow : (2^{SMOD} × timer 1 overflow rate) / 32
	1	0 or 1	0 or 1	–	Controlled by baud rate generator : ($2^{S0P} \times 2^{SMOD} \times f_{OSC}$) / (64 × baud rate generator overflow rate)
Mode 2 (9-bit UART)	–	–	0 1	–	f_{OSC} / 32 f_{OSC} / 16
Mode A (9-bit UART) Mode B (8-bit UART)	–	–	–	0 or 1	($2^{S1P} \times f_{OSC}$) / (32 × baud rate generator overflow rate)

10-Bit A/D Converter

The C509-L has a high perfomance 10-bit A/D converter (**figure 27**) with 15 inputs included which uses successive approximation technique for the conversion and uses self calibration mechanisms for reduction and compensation of offset and linearity errors

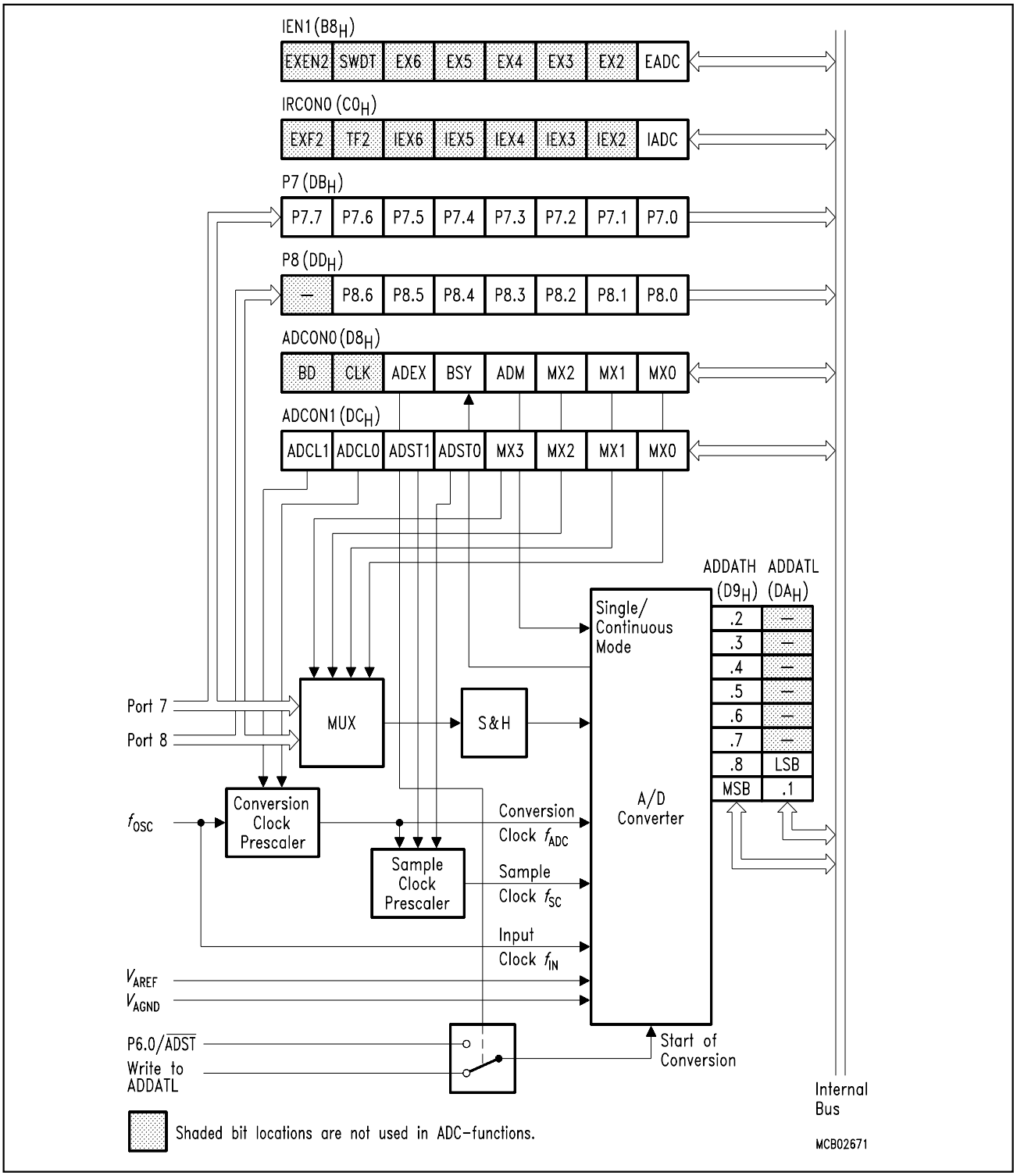
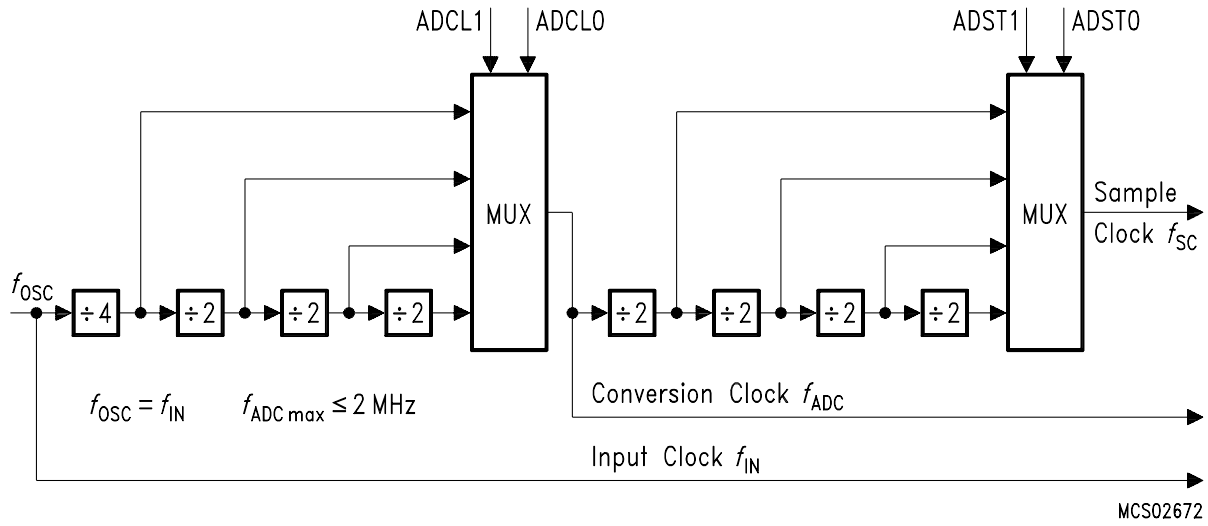


Figure 27
A/D Converter Block Diagram

The A/D converter provides the following features:

- 15 multiplexed input channels, which can also be used as digital inputs (port 7, port 8)
- 10-bit resolution
- Single or continuous conversion mode
- Internal or external start-of-conversion trigger capability
- Programmable conversion and sample clock
- Interrupt request generation after each conversion
- Using successive approximation conversion technique via a capacitor array
- Built-in hidden calibration of offset and linearity errors

The A/D converter uses basically three clock signals for operation : the input clock f_{IN} (=1/t_{IN}), the conversion clock f_{ADC} (=1/t_{ADC}) and the sample clock f_{SC} (=1/t_{SC}). All clock signals are derived from the C509-L system clock f_{OSC} which is applied at the XTAL pins. The input clock f_{IN} is equal to f_{OSC} while the conversion clock and the sample clock must be adapted. The conversion clock is limited to a maximum frequency of 2 MHz. The table in **figure 28** defines the divider ratio for the conversion and sample clock of each combination of the prescaler bits.



Conversion Clock f_{ADC}			Sample Clock f_{SC}					
ADCL1	ADCL0	f_{ADC}	ADST1 0	ADST0 0	ADST1 0	ADST0 1	ADST1 1	ADST0 0	ADST1 1	ADST0 1
0	0	f_{IN} / 4	f_{IN} / 8		f_{IN} / 16		f_{IN} / 32		f_{IN} / 64	
0	1	f_{IN} / 8	f_{IN} / 16		f_{IN} / 32		f_{IN} / 64		f_{IN} / 128	
1	0	f_{IN} / 16	f_{IN} / 32		f_{IN} / 64		f_{IN} / 128		f_{IN} / 256	
1	1	f_{IN} / 32	f_{IN} / 64		f_{IN} / 128		f_{IN} / 256		f_{IN} / 512	

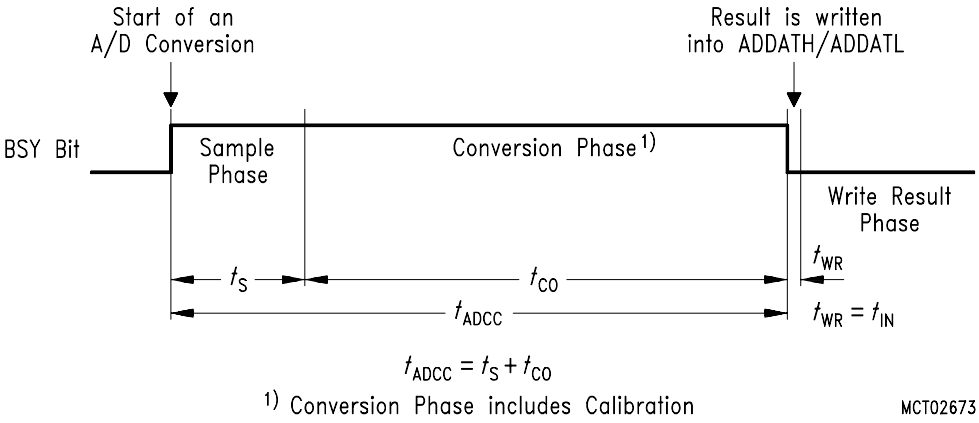
Figure 28
A/D Converter Clock Selection

A/D Conversion Timing

An A/D conversion is internally started by writing into the SFR ADDATL with dummy data. A write to SFR ADDATL will start a new conversion even if a conversion is currently in progress. Basically, the A/D conversion procedure is divided into three parts :

- Sample phase (t_S), used for sampling the analog input voltage.
- Conversion phase (t_{CO}), used for the real A/D conversion.(includes calibration)
- Write result phase (t_{WR}), used for writing the conversion result into the ADDAT registers.

The total A/D conversion time is defined by t_{ADCC} which is the sum of the two phase times t_S and t_{CO}. The duration of the two phases of an A/D conversion is specified by its specific timing parameter as shown in **figure 29**.



Conversion Clock Prescaler		Sample Clock Prescaler		Sample Time	Conversion Time	ConversionTime	
ADCL1	ADCL0	ADST1	ADST0	t_S	t_{CO}	t_{ADCC}	Number of CPU Cycles
0	0	0	0	8 x t_{IN}	40 x t_{IN}	48 x t_{IN}	8
		0	1	16 x t_{IN}		56 x t_{IN}	9
		1	0	32 x t_{IN}		72 x t_{IN}	12
		1	1	64 x t_{IN}		104 x t_{IN}	17
0	1	0	0	16 x t_{IN}	80 x t_{IN}	96 x t_{IN}	16
		0	1	32 x t_{IN}		112 x t_{IN}	18
		1	0	64 x t_{IN}		144 x t_{IN}	24
		1	1	128 x t_{IN}		208 x t_{IN}	34
1	0	0	0	32 x t_{IN}	160 x t_{IN}	192 x t_{IN}	32
		0	1	64 x t_{IN}		224 x t_{IN}	37
		1	0	128 x t_{IN}		288 x t_{IN}	48
		1	1	256 x t_{IN}		416 x t_{IN}	69
1	1	0	0	64 x t_{IN}	320 x t_{IN}	384 x t_{IN}	64
		0	1	128 x t_{IN}		448 x t_{IN}	74
		1	0	256 x t_{IN}		576 x t_{IN}	96
		1	1	512 x t_{IN}		832 x t_{IN}	138

Figure 29
A/D Conversion Timing

Interrupt System

The C509-L provides 19 interrupt sources with four priority levels. 12 interrupts can be generated by the on-chip peripherals and 7 interrupts may be triggered externally. In the C509-L the 19 interrupt sources are combined to six groups of three or four interrupt sources. Each interrupt group can be programmed to one of the four interrupt priority levels. **Figure 30** to **33** give a general overview of the interrupt sources and illustrate the interrupt request and control flags.

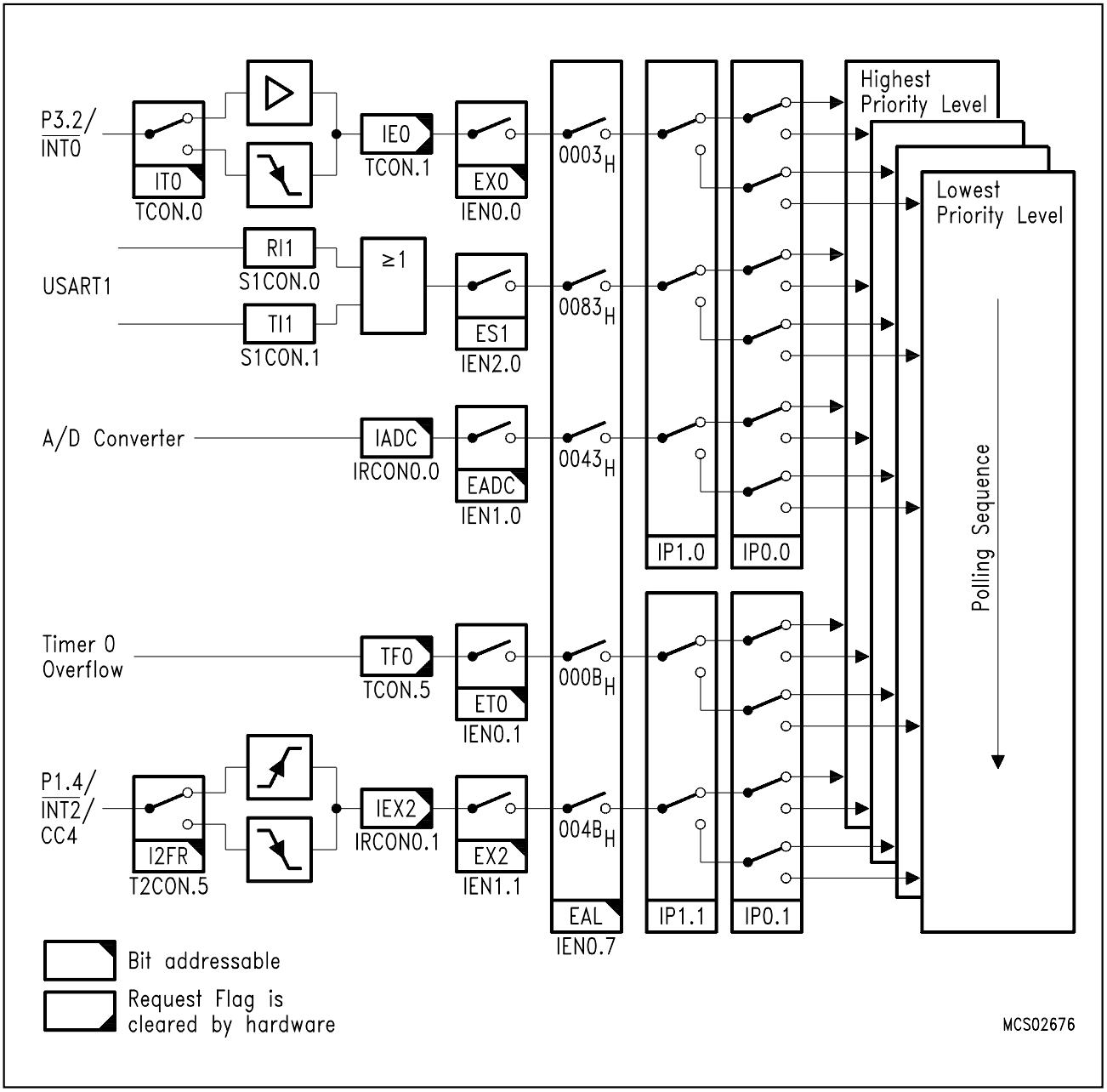


Figure 30
Interrupt Request Sources (Part 1)

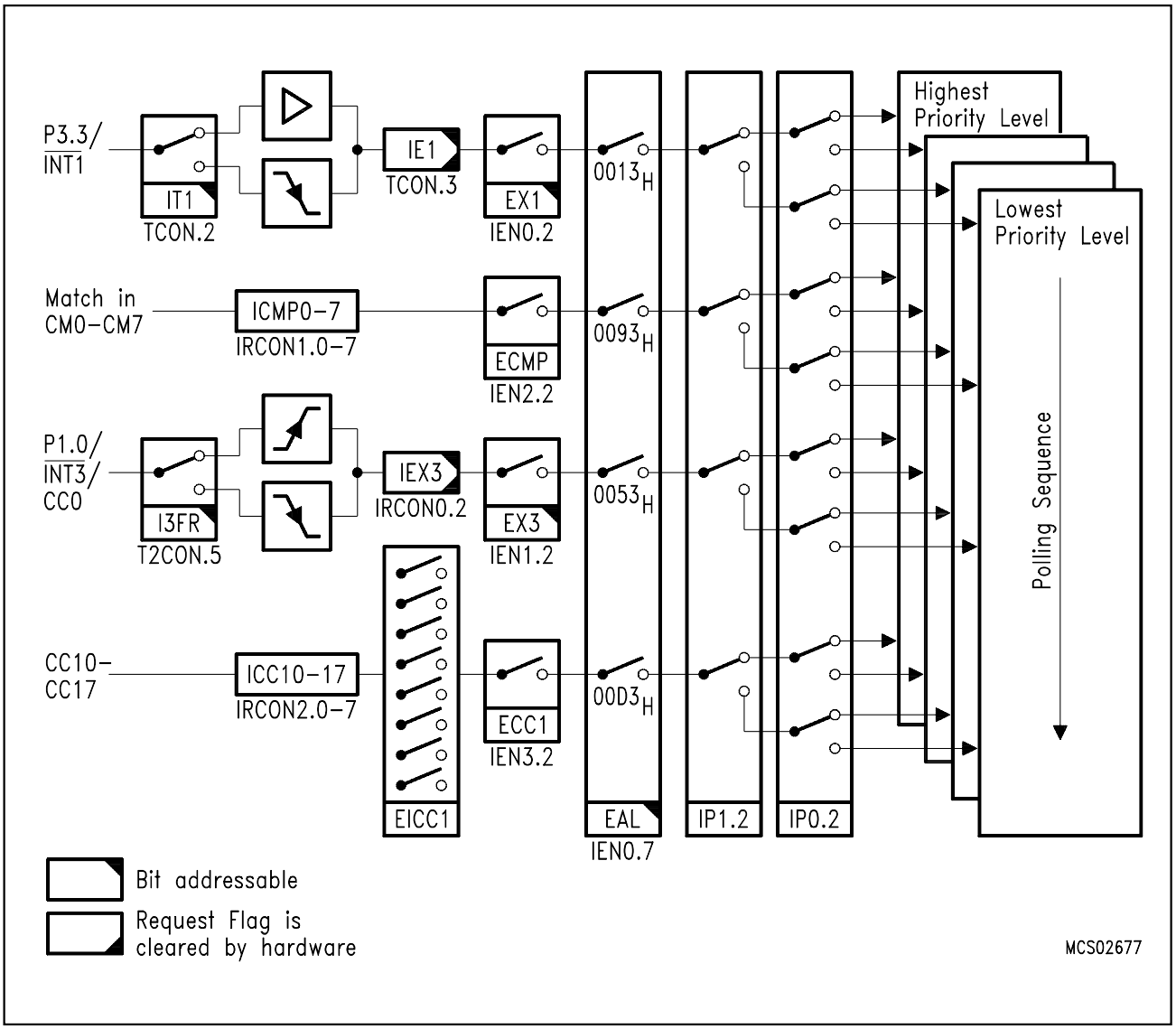


Figure 31
Interrupt Request Sources (Part 2)

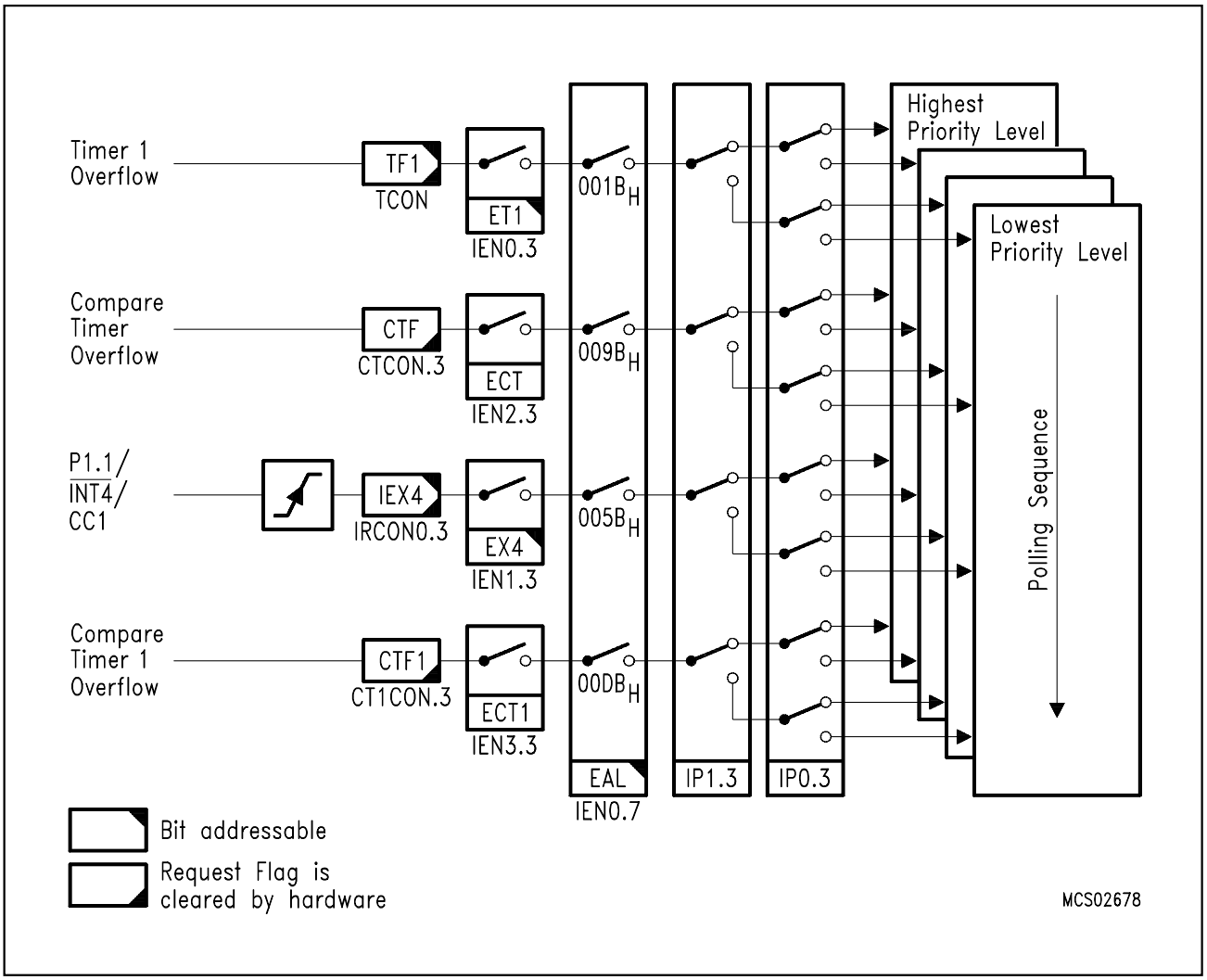


Figure 32
Interrupt Request Sources (Part 3)

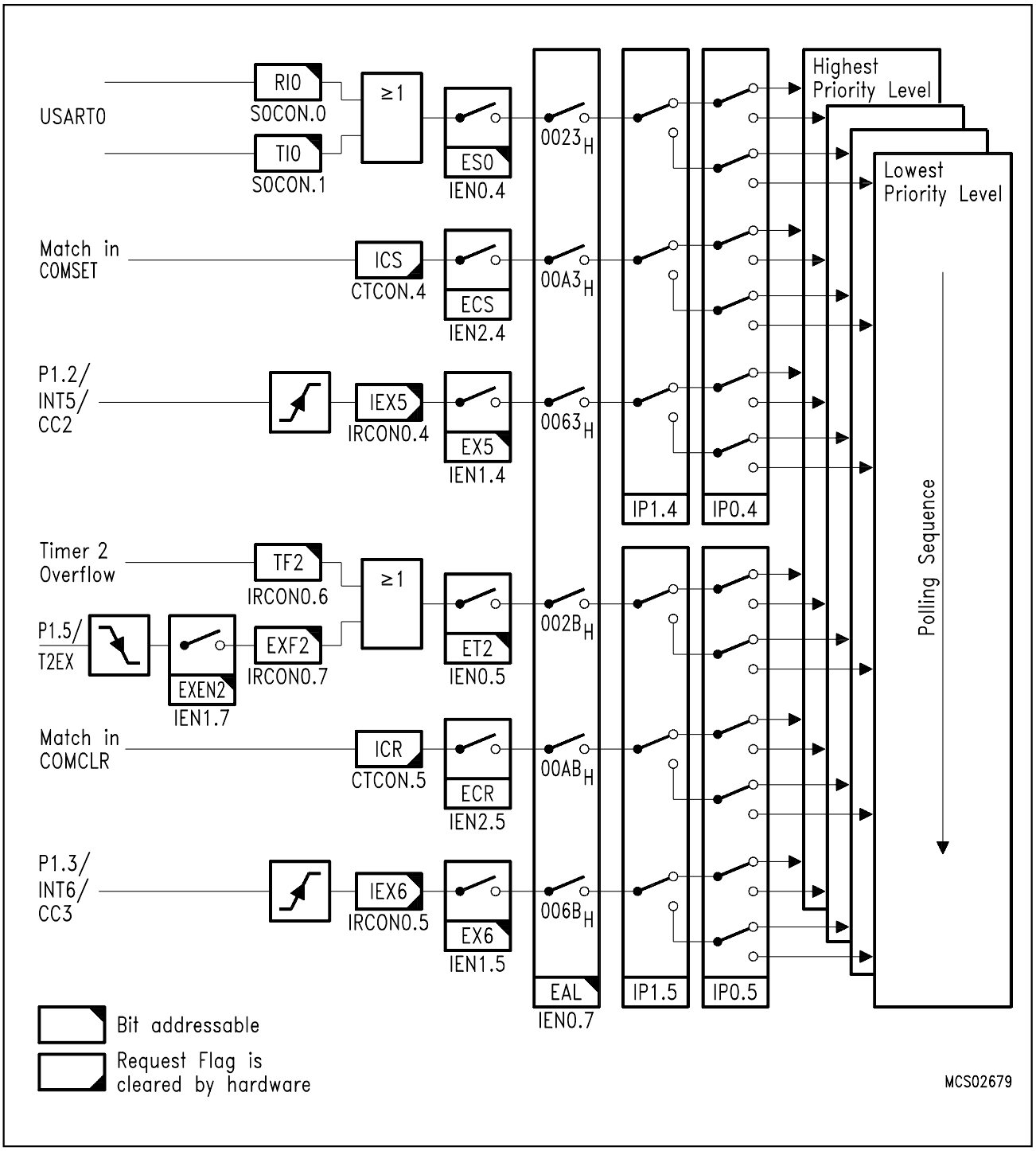


Figure 33
Interrupt Request Sources (Part 4)

Table 13
Interrupt Sources and their Corresponding Interrupt Vectors

Interrupt Source	Interrupt Vector Address	Interrupt Request Flags
External Interrupt 0	0003_H	IE0
Timer 0 Overflow	$000B_H$	TF0
External Interrupt 1	0013_H	IE1
Timer 1 Overflow	$001B_H$	TF1
Serial Channel 0	0023_H	RI0 / TI0
Timer 2 Overflow / Ext. Reload	$002B_H$	TF2 / EXF2
A/D Converter	0043_H	IADC
External Interrupt 2	$004B_H$	IEX2
External Interrupt 3	0053_H	IEX3
External Interrupt 4	$005B_H$	IEX4
External Interrupt 5	0063_H	IEX5
External Interrupt 6	$006B_H$	IEX6
Serial Channel 1	0083_H	RI1 / TI1
Compare Match Interupt of Compare Registers CM0-CM7 assigned to Timer 2	0093_H	ICMP0 - ICMP7
Compare Timer Overflow	$009B_H$	CTF
Compare Match Interupt of Compare Register COMSET	$00A3_H$	ICS
Compare Match Interupt of Compare Register COMCLR	$00AB_H$	ICR
Compare / Capture Event interrupt	$00D3_H$	ICC10 - ICC17
Compare Timer 1 Overflow	$00DB_H$	CT1F

Fail Save Mechanisms

The C509-L offers two on-chip peripherals which monitor the program flow and ensure an automatic "fail-safe" reaction for cases where the controller's hardware fails or the software hangs up:

- A programmable watchdog timer (WDT) with variable time-out period from 189 microseconds up to approx. 0.79 seconds at 16 MHz.
- An oscillator watchdog (OWD) which monitors the on-chip oscillator and forces the microcontroller into the reset state if the on-chip oscillator fails.

Programmable Watchdog Timer

The watchdog timer in the C509-L is a 15-bit timer, which is incremented by a count rate of $f_{OSC}/12$ up to $f_{OSC}/384$. For programming of the watchdog timer overflow rate, the upper 7 bit of the watchdog timer can be written. **Figure 34** shows the block diagram of the watchdog timer unit.

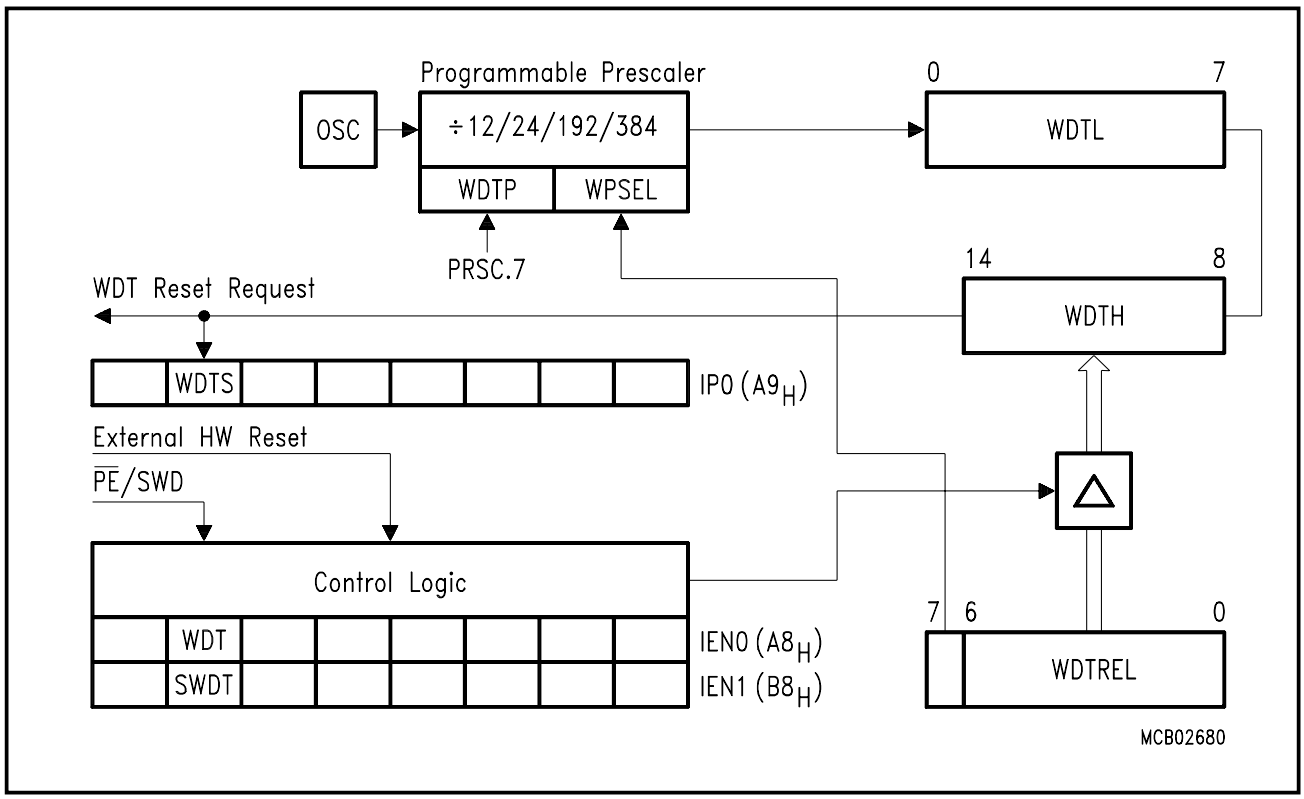


Figure 34
Block Diagram of the Programmable Watchdog Timer

The watchdog timer can be started by software (bit SWDT) or by hardware through pin $\overline{PE}$/SWD, but it cannot be stopped during active mode of the C509-L. If the software fails to refresh the running watchdog timer an internal reset will be initiated on watchdog timer overflow. For refreshing of the watchdog timer the content of the SFR WDTREL is transferred to the upper 7-bit of the watchdog timer. The refresh sequence consists of two consecutive instructions which set the bits WDT and SWDT each. The reset cause (external reset or reset caused by the watchdog) can be examined by software (flag WDTS). It must be noted, however, that the watchdog timer is halted during the idle mode and power down mode of the processor.

Oscillator Watchdog

The oscillator watchdog of the C509-L serves for three functions :

- **Monitoring of the on-chip oscillator's function.**
  The watchdog supervises the on-chip oscillator's frequency; if it is lower than the frequency of the auxiliary RC oscillator in the watchdog unit, the internal clock is supplied by the RC oscillator and the device is brought into reset; if the failure condition disappears (i.e. the on-chip oscillator has a higher frequency than the RC oscillator), the part executes a final reset phase of appr. 0.5 ms in order to allow the oscillatior to stabilize; then the oscillator watchdog reset is released and the part starts program execution again.
- **Restart from the hardware power down mode.**
  If the hardware power down mode is terminated the oscillator watchdog has to control the correct start-up of the on-chip oscillator and to restart the program. The oscillator watchdog function is only part of the complete hardware power down sequence; however, the watchdog works identically to the monitoring function.
- **Fast internal reset after power-on.**
  In this function the oscillator watchdog unit provides a clock supply for the reset before the on-chip oscillator has started. In this case the oscillator watchdog unit also works identically to the monitoring function.

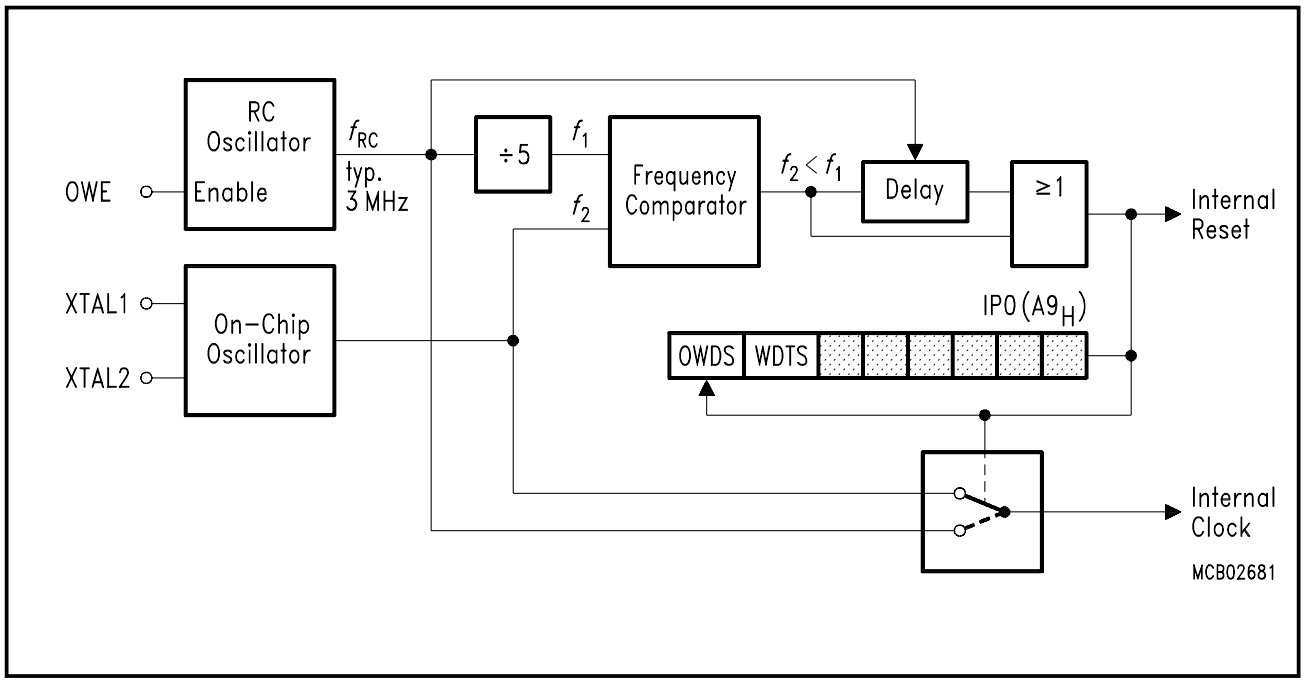


Figure 35
Block Diagram of the Oscillator Watchdog

Power Saving Modes

The C509-L provides three power saving modes in which power consumption can be significantly reduced.

- **Idle mode**
  The CPU is gated off from the oscillator. All peripherals are still provided with the clock and are able to work.
- **Power down mode**
  The operation of the C509-L is completely stopped and the oscillator is turned off. This mode is used to save the contents of the internal RAM with a very low standby current. Power down mode can be entered by software or by hardware (pin $\overline{\text{HWPD}}$).
- **Slow-down mode**
  The controller keeps up the full operating functionality, but its normal clock frequency is internally divided by eight. This slows down all parts of the controller, the CPU and all peripherals, to 1/8 th of their normal operating frequency. Slowing down the frequency greatly reduces power consumption.

Table 14 gives a general overview of the entry and exit procedures of the power saving modes.

Table 14
Power Saving Modes Overview

Mode	Entering 2-Instruction Example	Leaving by	Remarks
Idle mode	ORL PCON, #01H ORL PCON, #20H	Ocurrence of an interrupt from a peripheral unit	CPU clock is stopped; CPU maintains their data; peripheral units are active (if enabled) and provided with clock
		Hardware Reset	
Software Power-Down Mode	ORL PCON, #02H ORL PCON, #40H	Hardware Reset	Oscillator is stopped; contents of on-chip RAM and SFR's are maintained;
Hardware Power-Down Mode	Low level at pin $\overline{\text{HWPD}}$	High level at pin $\overline{\text{HWPD}}$	
Slow Down Mode	ORL PCON,#10H	ANL PCON,#0EFH or Hardware Reset	Oscillator frequency is reduced to 1/8 of its nominal frequency

In the power down mode of operation, V_{CC} can be reduced to minimize power consumption. It must be ensured, however, that V_{CC} is not reduced before the power down mode is invoked, and that V_{CC} is restored to its normal operating level, before the power down mode is terminated.

If e.g. the idle mode is left through an interrupt, the microcontroller state (CPU, ports, peripherals) remains preserved. If a power saving mode is left by a hardware reset, the microcontroller state is disturbed and replaced by the reset state of the C509-L.

Absolute Maximum Ratings

Ambient temperature under bias (T_A) ..... – 40 to 110 °C
Storage temperature (T_{stg}) ..... – 65 °C to 150 °C
Voltage on V_{CC} pins with respect to ground (V_{SS}) ..... – 0.5 V to 6.5 V
Voltage on any pin with respect to ground (V_{SS}) ..... – 0.5 V to V_{CC} +0.5 V
Input current on any pin during overload condition ..... – 10 mA to 10 mA
Absolute sum of all input currents during overload condition ..... I 100 mA I
Power dissipation ..... 1 W

Note:

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for longer periods may affect device reliability. During overload conditions ($V_{IN} > V_{CC}$ or $V_{IN} < V_{SS}$) the Voltage on V_{CC} pins with respect to ground (V_{SS}) must not exceed the values defined by the absolute maximum ratings.

DC Characteristics

V_{CC} = 5 V + 10%, – 15%; V_{SS} = 0 V T_A = 0 to 70 °C for the SAB-C509
T_A = – 40 to 85 °C for the SAF-C509

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input low voltage (except $\overline{EA}$, $\overline{RESET}$, $\overline{HWPD}$)	V_{IL}	– 0.5	0.2 V_{CC} – 0.1	V	–
Input low voltage ($\overline{EA}$)	V_{IL1}	– 0.5	0.2 V_{CC} – 0.3	V	–
Input low voltage ($\overline{HWPD}$, $\overline{RESET}$)	V_{IL2}	– 0.5	0.2 V_{CC} + 0.1	V	–
Input low voltage (CMOS) (ports 0 - 9)	V_{ILC}	– 0.5	0.3 V_{CC}	V	–
Input high voltage (except $\overline{RESET}$, XTAL2 and $\overline{HWPD}$	V_{IH}	0.2 V_{CC} + 0.9	V_{CC} + 0.5	V	–
Input high voltage to XTAL2	V_{IH1}	0.7 V_{CC}	V_{CC} + 0.5	V	–
Input high voltage to $\overline{RESET}$ and $\overline{HWPD}$	V_{IH2}	0.6 V_{CC}	V_{CC} + 0.5	V	–
Input high voltage (CMOS) (ports 0 - 9)	V_{IHC}	0.7 V_{CC}	V_{CC} + 0.5	V	–
CMOS input hysteresis (ports 1, 3 to 9)	V_{IHYS}	0.1	–	V	–

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Output low voltage (ports 1, 2, 3, 4, 5, 6, 9)	V_{OL}	–	0.45	V	I_{OL} = 1.6 mA [1]
Output low voltage (port 0, ALE, $\overline{PSEN}$/$\overline{RDF}$, $\overline{RO}$)	V_{OL1}	–	0.45	V	I_{OL} = 3.2mA [1]
Output high voltage (ports 1, 2, 3, 4, 5, 6, 9)	V_{OH}	2.4 0.9 V_{CC}	– –	V V	I_{OH} = –80 µA I_{OH} = –10 µA
Output high voltage (port 0 in external bus mode, ALE, $\overline{PSEN}$/$\overline{RDF}$, $\overline{RO}$)	V_{OH1}	2.4 0.9 V_{CC}	– –	V V	I_{OH} = –800 µA [2] I_{OH} = –80 µA [2]
Output high voltage (CMOS) (ports 1, 2, 3, 4, 5, 6, 9)	V_{OHC}	0.9 V_{CC}	–	V	I_{OH} = –800 µA
Logic input low current (ports 1, 2, 3, 4, 5, 6, 9)	I_{IL}	– 10	– 70	µA	V_{IN} = 0.45 V
Logical 1-to-0 transition current (ports 1, 2, 3, 4, 5, 6, 9)	I_{TL}	– 65	– 650	µA	V_{IN} = 2 V
Input leakage current [7] (port 0, 7, 8, $\overline{HWPD}$)	I_{LI}	–	± 100	nA	0.45 < V_{IN} < V_{CC}
(port 0 in CMOS)			± 150	nA	0.45 < V_{IN} < V_{CC} T_A > 100 °C
Input leakage current ($\overline{EA}$, PRGEN) (ports 1, 2, 3, 4, 5, 6, 9 in CMOS)	I_{LIC}	–	± 1	µA	0.45 < V_{IN} < V_{CC}
Input low current to $\overline{RESET}$ for reset	I_{LI2}	– 10	–100	µA	V_{IN} = 0.45 V
Input low current (XTAL2)	I_{LI3}	–	– 15	µA	V_{IN} = 0.45 V
Input low current ($\overline{PE}$/SWD, OWE)	I_{LI4}	–	– 20	µA	V_{IN} = 0.45 V
Pin capacitance	C_{IO}	–	10	pF	f_C = 1 MHz T_A = 25 °C
Overload current	I_{OV}	–	± 5	mA	[10] [11]

Parameter	Symbol	Limit Values		Unit	Test Condition
		typ. [12]	max.		
Power supply current:					
C509-L, Active mode, 12 MHz [8]	I_{CC}	[9]	TBD	mA	V_{CC} = 5 V, [4]
C509-L, Active mode, 16 MHz [8]	I_{CC}	[9]	TBD	mA	V_{CC} = 5 V, [4]
C509-L, Idle mode, 12 MHz [8]	I_{CC}	–	TBD	mA	V_{CC} = 5 V, [5]
C509-L, Idle mode, 16 MHz [8]	I_{CC}	[9]	TBD	mA	V_{CC} = 5 V, [5]
C509-L, Slow down mode, 12 MHz	I_{CC}	–	TBD	mA	V_{CC} = 5 V, [6]
C509-L, Slow down mode, 16 MHz	I_{CC}	–	TBD	mA	V_{CC} = 5 V, [6]
C509-L, Power Down Mode	I_{PD}	5	50	µA	V_{CC} = 2...5.5

Notes :

1) Capacitive loading on ports 0 and 2 may cause spurious noise pulses to be superimposed on the V_{OL} of ALE and port 1, 3, 4, 5, 6, and 9. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operation. In the worst case (capacitive loading > 100 pF), the noise pulse on ALE line may exceed 0.8 V. In such cases it may be desirable to qualify ALE with a schmitt-trigger, or use an address latch with a schmitt-trigger strobe input.

2) Capacitive loading on ports 0 and 2 may cause the V_{OH} on ALE and PSEN/$\overline{RDF}$ to momentarily fall below the 0.9 V_{CC} specification when the address lines are stabilizing.

3) I_{PD} (power down mode) is measured under following conditions:
EA = $\overline{RESET}$ = V_{CC}; Port0 = Port7 = Port8 = V_{CC}; XTAL1 = N.C.; XTAL2 = V_{SS}; $\overline{PE}$/SWD = OWE = V_{SS}; $\overline{HWDP}$ = V_{CC}; V_{AREF} = V_{CC}; V_{AGND} = V_{SS}; all other pins are disconnected.
Hardware power down mode current (I_{PD}) is measured with OWE =V_{CC} or V_{SS}.

4) I_{CC} (active mode) is measured with:
XTAL2 driven with t_R/t_F = 5 ns , V_{IL} = V_{SS} + 0.5 V, V_{IH} = V_{CC} – 0.5 V; XTAL1 = N.C.; EA = $\overline{PE}$/SWD= V_{CC} ; Port0 = Port7 = Port8 = V_{CC} ; $\overline{HWPD}$ = V_{CC} ; $\overline{RESET}$ = V_{SS}; all other pins are disconnected. I_{CC} would be slightly higher if a crystal oscillator is used.

5) I_{CC} (idle mode) is measured with all output pins disconnected and with all peripherals disabled;
XTAL2 driven with t_R/t_F = 5 ns, V_{IL} = V_{SS} + 0.5 V, V_{IH} = V_{CC} – 0.5 V; XTAL1 = N.C.; $\overline{RESET}$ = V_{CC};
$\overline{HWPD}$ = V_{CC} ; Port0 = Port7 = Port8 = V_{CC} ; $\overline{EA}$ = $\overline{PE}$/SWD = V_{SS}; all other pins are disconnected;

6) I_{CC} (slow down mode) is measured with all output pins disconnected and with all peripherals disabled;
XTAL2 driven with t_R/t_F = 5 ns, V_{IL} = V_{SS} + 0.5 V, V_{IH} = V_{CC} – 0.5 V; XTAL1 = N.C.; $\overline{RESET}$ = V_{CC};
$\overline{HWPD}$ = V_{CC} ; Port7 = Port8 = V_{CC} ; $\overline{EA}$ = $\overline{PE}$/SWD = V_{SS}; all other pins are disconnected;

7) Input leakage current for port 0 is measured with $\overline{RESET}$ = V_{CC}.

8) $I_{CC\ max}$ at other frequencies is given by:
active mode:TBD
idle mode:TBD
where f_{osc} is the oscillator frequency in MHz. I_{CC} values are given in mA and measured at V_{CC} = 5 V.

9) Typical power supply current ($I_{CC\ typ}$) with test conditiones as defined in note 4 and 5 is given by:
active mode, 12 MHz :45 mA
active mode, 16 MHz :72 mA
idle mode, 16 MHz :29 mA

10) Overload conditions occur if the standard operating conditions are exeeded, ie. the voltage on any pin exceeds the specified range (i.e. V_{OV} > V_{CC} + 0.5 V or V_{OV} < V_{SS} - 0.5 V). The supply voltage V_{CC} and V_{SS} must remain within the specified limits. The absolute sum of input currents on all port pins may not exceed 50 mA.

11) Not 100% tested, guaranteed by design characterization.

12) The typical I_{CC} values are periodically measured at T_A = +25 °C but not 100% tested.

A/D Converter Characteristics

T_A = 0 to 70 °C for the SAB-C509
T_A = – 40 to 85 °C for the SAF-C509
V_{CC} = 5 V + 10%, – 15%; V_{SS} = 0 V
4 V ≤ V_{AREF} ≤ V_{CC}+0.1 V ; V_{SS}-0.1 V ≤ V_{AGND} ≤ V_{SS}+0.2 V

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Analog input voltage	V_{AIN}	V_{AGND}	V_{AREF}	V	1)
Sample time	t_S	8 t_{IN}	512 t_{IN}		2) see table below
Conversion time	t_{ADCC}	48 t_{IN}	832 t_{IN}		3) see table below
Total unadjusted error	TUE	–	± 2	LSB	4)
Internal resistance of reference voltage source	R_{AREF}	–	t_{ADC} / 250 - 0.25	kΩ	t_{ADC} in [ns] 5) 6)
Internal resistance of analog source	R_{ASRC}	–	t_S / 500 - 0.25	kΩ	t_S in [ns] 3) 6)
ADC input capacitance	C_{AIN}	–	50	pF	6)

Notes see next page.

Clock calculation table

Conversion Clock Selection			Sample Clock Selection			Sample Time t_S	Conversion Time t_{ADCC}
ADCL1	ADCL0	Prescaler CCP	ADST1	ADST0	Prescaler SCP		
0	0	4	0 0 1 1	0 1 0 1	2	8 x t_{IN} 16 x t_{IN} 32 x t_{IN} 64 x t_{IN}	48 x t_{IN} 56 x t_{IN} 72 x t_{IN} 104 x t_{IN}
0	1	8	0 0 1 1	0 1 0 1	4	16 x t_{IN} 32 x t_{IN} 64 x t_{IN} 128 x t_{IN}	96 x t_{IN} 112 x t_{IN} 144 x t_{IN} 208 x t_{IN}
1	0	16	0 0 1 1	0 1 0 1	8	32 x t_{IN} 64 x t_{IN} 128 x t_{IN} 256 x t_{IN}	192 x t_{IN} 224 x t_{IN} 288 x t_{IN} 416 x t_{IN}
1	1	32	0 0 1 1	0 1 0 1	16	64 x t_{IN} 128 x t_{IN} 256 x t_{IN} 512 x t_{IN}	384 x t_{IN} 448 x t_{IN} 576 x t_{IN} 832 x t_{IN}

Further timing conditions : t_{ADC} min = 500 ns = CCP x CLP
t_{IN} = 1 / f_{OSC} = CLP
t_{SC} = t_{ADC} x SCP

Notes:

1) V_{AIN} may exeed V_{AGND} or V_{AREF} up to the absolute maximum ratings. However, the conversion result in these cases will be $X000_H$ or $X3FF_H$, respectively.

2) During the sample time the input capacitance C_{AIN} can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach their final voltage level within t_S. After the end of the sample time t_S, changes of the analog input voltage have no effect on the conversion result.

3) This parameter includes the sample time t_S, the time for determining the digital result and the time for the calibration. Values for the conversion clock f_{ADC} depend on programming and can be taken from the table below.

4) T_{UE} is tested at V_{AREF} = 5.0 V, V_{AGND} = 0 V, V_{CC} = 4.9 V. It is guaranteed by design characterization for all other voltages within the defined voltage range.
If an overload condition occurs on maximum 2 not selected analog input pins and the absolute sum of input overload currents on all analog input pins does not exceed 10 mA, an additional conversion error of 1/2 LSB is permissible.

5) During the conversion the ADC's capacitance must be repeatedly charged or discharged. The internal resistance of the reference source must allow the capacitance to reach their final voltage level within the indicated time. The maximum internal resistance results from the programmed conversion timing.

6) Not 100% tested, but guaranteed by design characterization.

AC Characteristics

V_{CC} = 5 V + 10%, – 15%; V_{SS} = 0 V T_A = 0 to 70 °C for the SAB-C509
T_A = – 40 to 85 °C for the SAF-C509

(C_L for port 0, ALE and $\overline{PSEN}$ outputs = 100 pF; C_L for all other outputs = 80 pF)

Program Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		16-MHz clock Duty Cycle 0.4 to 0.6		Variable Clock 1/CLP = 3.5 MHz to 16 MHz		
		min.	max.	min.	max.	
ALE pulse width	t_{LHLL}	48	–	CLP-15	–	ns
Address setup to ALE	t_{AVLL}	10	–	TCL_{Hmin}-15	–	ns
Address hold after ALE	t_{LLAX}	10	–	TCL_{Hmin}-15	–	ns
Address to valid instruction in	t_{LLIV}	–	75	–	2 CLP-50	ns
ALE to $\overline{PSEN}$/$\overline{RDF}$	t_{LLPL}	10	–	TCL_{Lmin}-15	–	ns
$\overline{PSEN}$/$\overline{RDF}$ pulse width	t_{PLPH}	73	–	CLP+ TCL_{Hmin}-15	–	ns
$\overline{PSEN}$/$\overline{RDF}$ to valid instruction in	t_{PLIV}	–	38	–	CLP+ TCL_{Hmin}-50	ns
Input instruction hold after $\overline{PSEN}$/ $\overline{RDF}$	t_{PXIX}	0	–	0	–	ns
Input instruction float after $\overline{PSEN}$/ $\overline{RDF}$	t_{PXIZ} *)	–	15	–	TCL_{Lmin}-10	ns
Address valid after $\overline{PSEN}$/$\overline{RDF}$	t_{PXAV} *)	20	–	TCL_{Lmin}-5	–	ns
Address to valid instruction in	t_{AVIV}	–	95	–	2 CLP+ TCL_{Hmin}-55	ns
Address float to $\overline{PSEN}$/$\overline{RDF}$	t_{AZPL}	- 5		- 5	–	ns

*) Interfacing the C509-L to devices with float times up to 20 ns is permissible. This limited bus contention will not cause any damage to port 0 drivers.

External Data Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		16-MHz clock Duty Cycle 0.4 to 0.6		Variable Clock 1/CLP= 3.5 MHz to 16 MHz		
		min.	max.	min.	max.	
$\overline{RD}$ pulse width	t_{RLRH}	158	–	3 CLP-30	–	ns
$\overline{WR}$ pulse width	t_{WLWH}	158	–	3 CLP-30	–	ns
Address hold after ALE	t_{LLAX2}	48	–	CLP -15	–	ns
$\overline{RD}$ to valid data in	t_{RLDV}	–	100	–	2 CLP+ TCL_{Hmin}-50	ns
Data hold after $\overline{RD}$	t_{RHDX}	0		0	–	ns
Data float after $\overline{RD}$	t_{RHDZ}	–	51	–	CLP-12	ns
ALE to valid data in	t_{LLDV}	–	200	–	4 CLP-50	ns
Address to valid data in	t_{AVDV}	–	200	–	4 CLP+ TCL_{Hmin}-75	ns
ALE to $\overline{WR}$ or $\overline{RD}$	t_{LLWL}	73	103	CLP+ TCL_{Lmin}-15	CLP+ TCL_{Lmin}+15	ns
Address valid to $\overline{WR}$	t_{AVWL}	95	–	2 CLP-30	–	ns
$\overline{WR}$ or $\overline{RD}$ high to ALE high	t_{WHLH}	10	40	TCL_{Hmin}-15	TCL_{Hmin}+15	ns
Data valid to $\overline{WR}$ transition	t_{QVWX}	5	–	TCL_{Lmin}-20	–	ns
Data setup before $\overline{WR}$	t_{QVWH}	163	–	3 CLP+ TCL_{Lmin}-50	–	ns
Data hold after $\overline{WR}$	t_{WHQX}	5	–	TCL_{Hmin}-20	–	ns
Address float after $\overline{RD}$	t_{RLAZ}	–	0	–	0	ns

External Clock Drive XTAL2

Parameter	Symbol	CPU Clock = 16 MHz Duty cycle 0.4 to 0.6		Variable CPU Clock 1/CLP = 3.5 to 16 MHz		Unit
		min.	max.	min.	max.	
Oscillator period	CLP	62.5	62.5	62.5	285	ns
High time	TCL_H	25	–	25	$CLP-TCL_L$	ns
Low time	TCL_L	25	–	25	$CLP-TCL_H$	ns
Rise time	t_R	–	10	–	10	ns
Fall time	t_F	–	10	–	10	ns
Oscillator duty cycle	DC	0.4	0.6	25 / CLP	1 - 25 / CLP	–
Clock cycle	TCL	25	37.5	$CLP * DC_{min}$	$CLP * DC_{max}$	ns

Note: The 16 MHz values in the tables are given as an example for a typical duty cycle variation of the oscillator clock from 0.4 to 0.6.

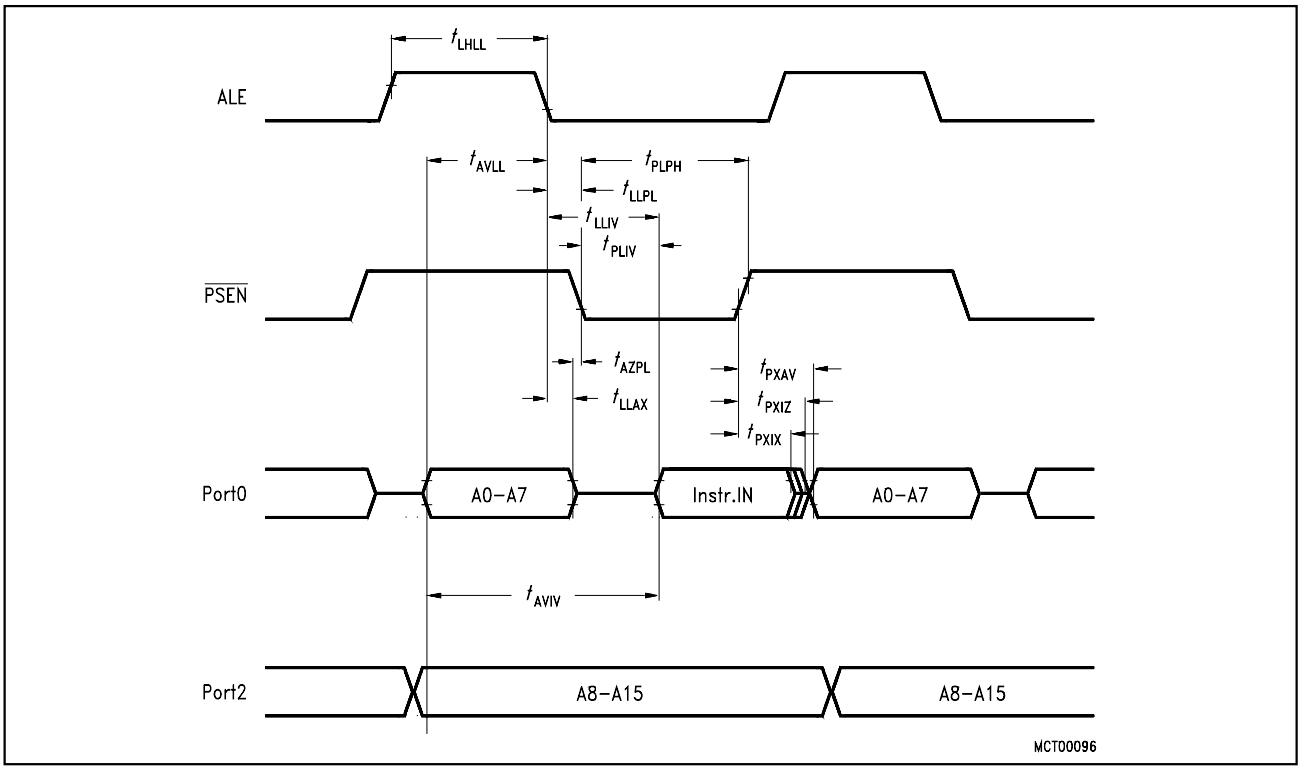


Figure 36
Program Memory Read Cycle

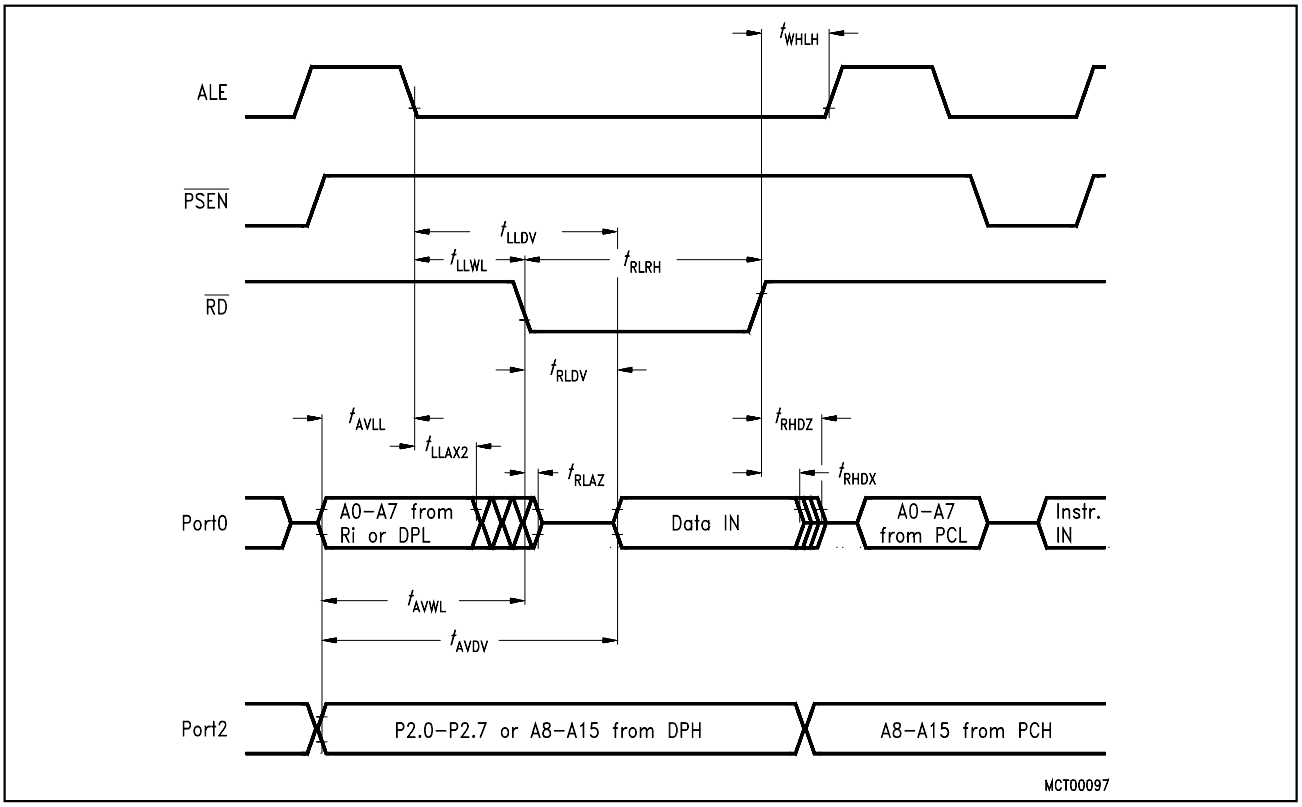


Figure 37
Data Memory Read Cycle

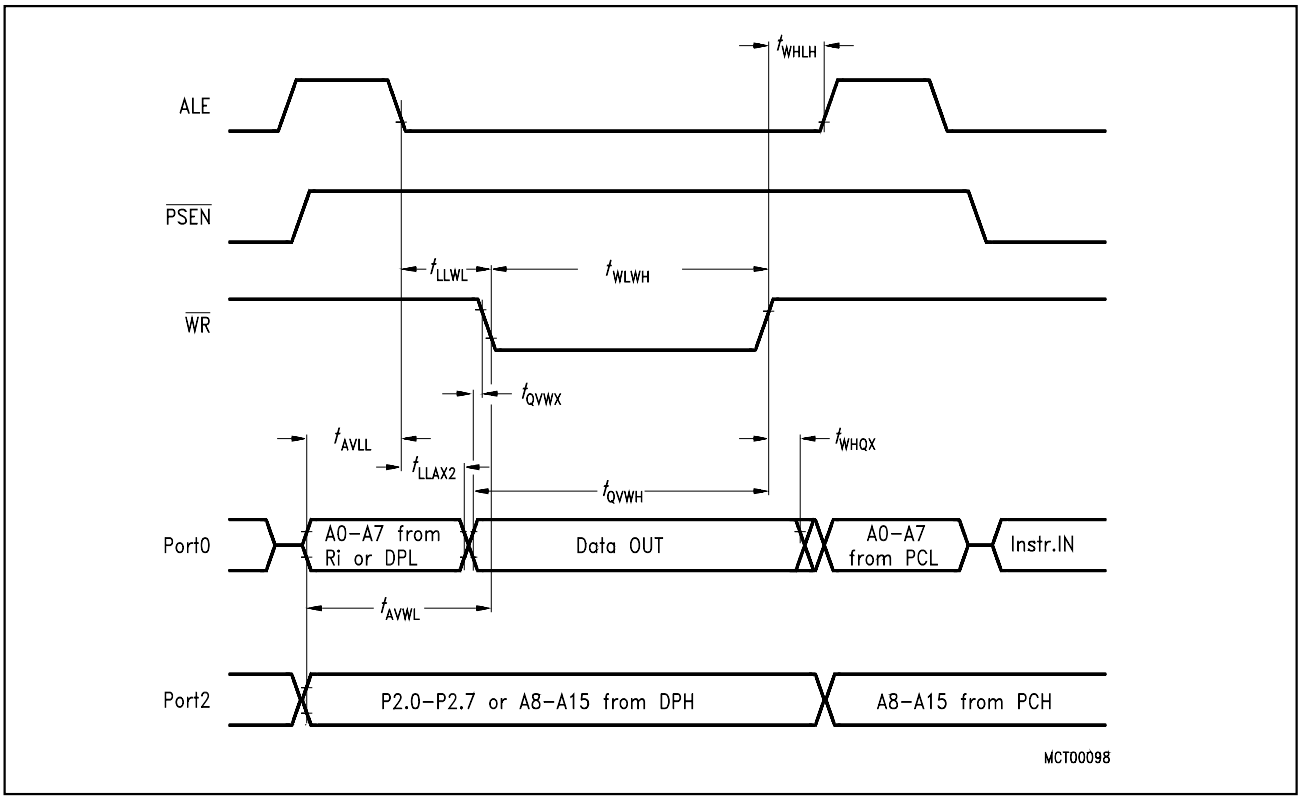


Figure 38
Data Memory Write Cycle

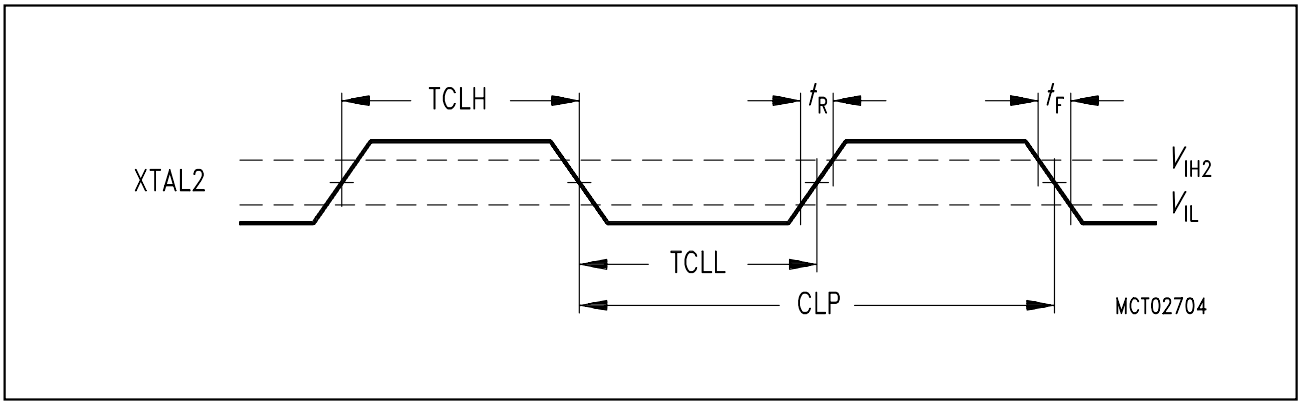
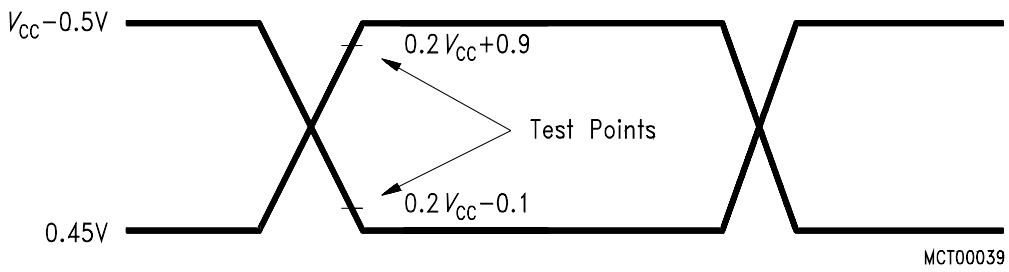
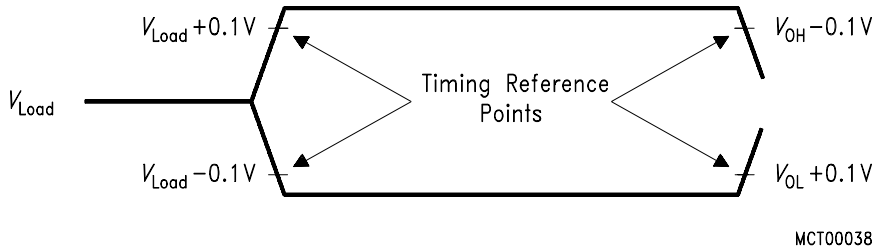


Figure 39
External Clock Drive Drive XTAL2



AC Inputs during testing are driven at V_{CC} - 0.5 V for a logic '1' and 0.45 V for a logic '0'. Timing measurements are made at V_{IHmin} for a logic '1' and V_{ILmax} for a logic '0'.

Figure 40
AC Testing: Input, Output Waveforms



For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs. $I_{OL}/I_{OH} \geq \pm$ 20 mA

Figure 41
AC Testing: Float Waveforms

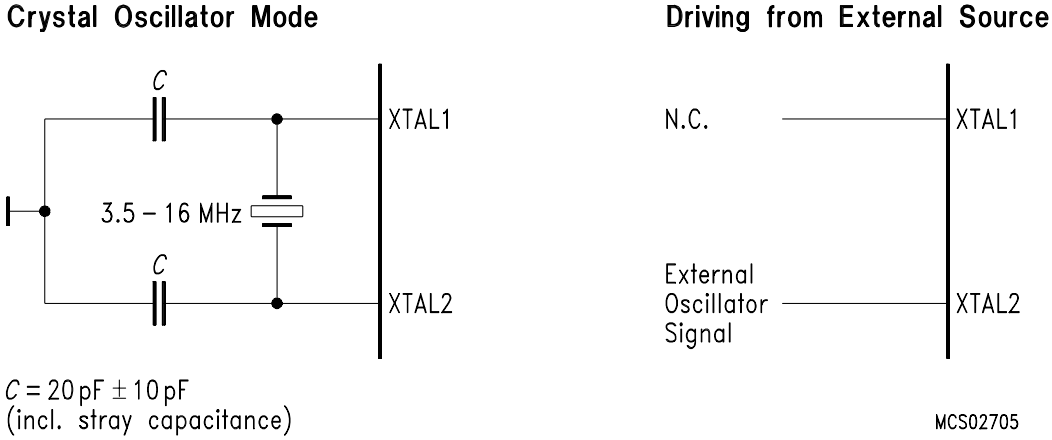


Figure 42
Recommended Oscillator Circuits for Crystal Oscillators up to 16 MHz