CYF0018V
CYF0036V
CYF0072V

18/36/72-Mbit Programmable FIFOs

Features

- Memory organization
  - Industry's largest first in first out (FIFO) memory densities: 18-Mbit, 36-Mbit, and 72-Mbit
  - Selectable memory organization: × 9, × 12, × 16, × 18, × 20, × 24, × 32, × 36
- Up to 133-MHz clock operation
- Unidirectional operation
- Independent read and write ports
  - Supports simultaneous read and write operations
  - Reads and writes operate on independent clocks, upto a maximum ratio of two, enabling data buffering across clock domains.
  - Supports multiple I/O voltage standard: low voltage complementary metal oxide semiconductor (LVCMOS) 3.3 V and 1.8 V voltage standards.
- Input and output enable control for write mask and read skip operations
- Mark and retransmit: resets read pointer to user marked position
- Empty, full, half-full, and programmable almost-empty and almost-full status flags with configured offsets
- Flow-through mailbox register to send data from input to output port, bypassing the FIFO sequence
- Configure programmable flags and registers through serial or parallel modes
- Separate serial clock (SCLK) input for serial programming
- Master reset to clear entire FIFO
- Partial reset to clear data but retain programmable settings
- Joint test action group (JTAG) port provided for boundary scan function
- Industrial temperature range: –40 °C to +85 °C

Functional Description

The Cypress programmable FIFO family offers the industry's highest-density programmable FIFO memory device. It has independent read and write ports, which can be clocked up to 133 MHz. User can configure input and output bus sizes. The maximum bus size of 36 bits enables a maximum data throughput of 4.8 Gbps. The user-programmable registers enable user to configure the device operation as desired. The device also offers a simple and easy-to-use interface to reduce implementation and debugging efforts, improve time-to-market, and reduce engineering costs. This makes it an ideal memory choice for a wide range of applications including multiprocessor interfaces, video and image processing, networking and telecommunications, high-speed data acquisition, or any system that needs buffering at high speeds across different clock domains.

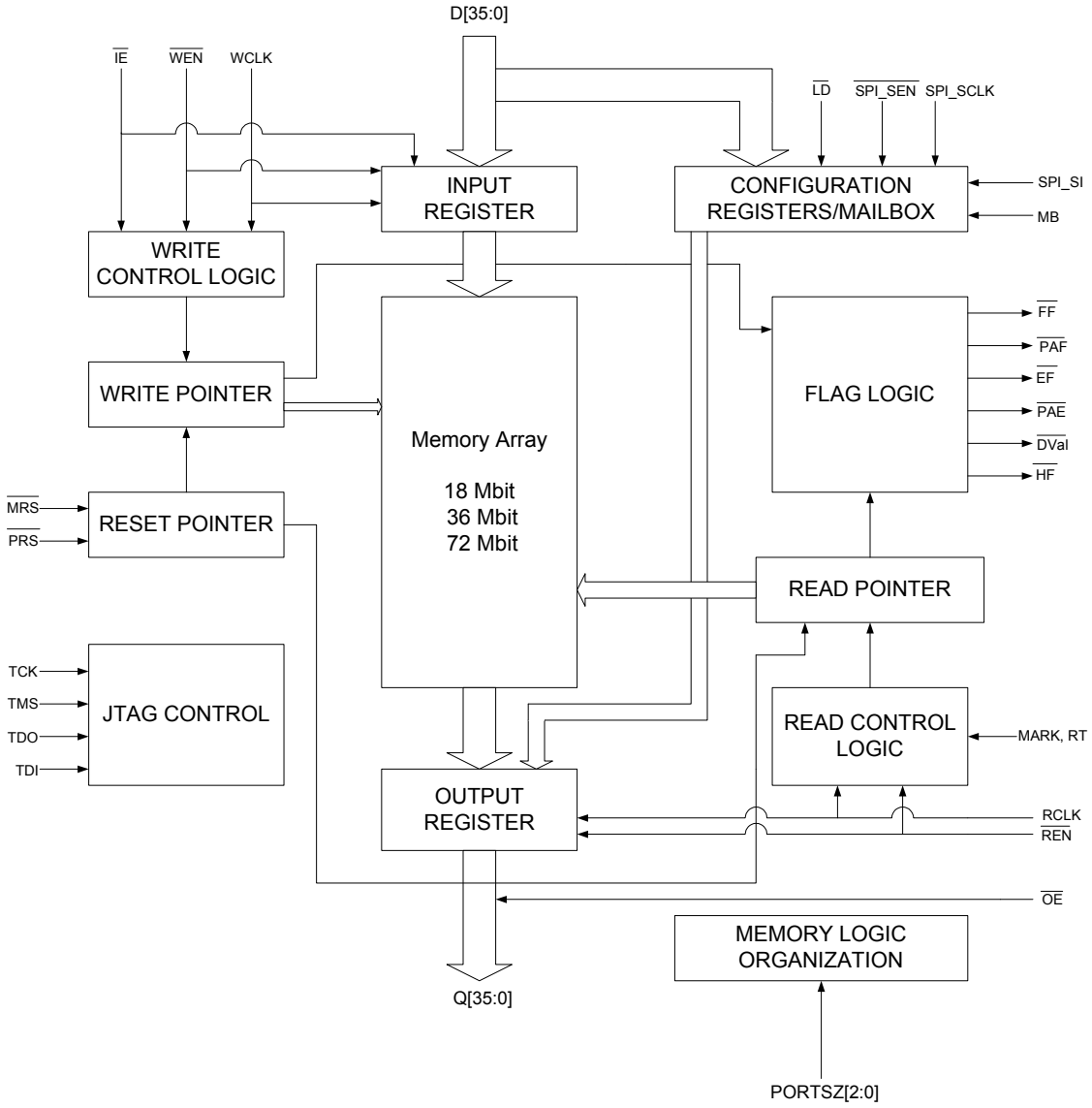
As implied by the name, the functionality of the FIFO is such that the data is read out of the read port in the same sequence in which it was written into the write port. If writes and inputs are enabled ($\overline{WEN}$ & $\overline{IE}$), data on the write port gets written into the device at the rising edge of write clock. Enabling reads and outputs ($\overline{REN}$ & $\overline{OE}$) fetches data on the read port at every rising edge of read clock. Both reads and writes can occur simultaneously at different speeds provided the ratio between read and write clock is in the range of 0.5 to 2. Appropriate flags are set whenever the FIFO is empty, almost-empty, half-full, almost-full or full.

The device also supports mark and retransmit of data, and a flow-through mailbox register.

All product features and specs are common to all densities (CYF0072V, CYF0036V, and CYF0018V). All descriptions are given assuming the 72Mbit (CYF0072V) device is operated in × 36 mode. They are valid for other densities (CYF0036V, and CYF0018V) and all port sizes × 9, × 12, × 16, × 18, × 20, × 24 and × 32 unless otherwise specified. The only difference will be in the input and output bus width. Table 1 on page 7 shows the part of bus with valid data from D[35:0] and Q[35:0] in × 9, × 12, × 16, × 18, × 20, × 24, × 32 and × 36 modes.

For a complete list of related documentation, click here.

Logic Block Diagram



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Pin Diagram for CYF0XXXVXXL [1]

Figure 1. 209-ball FBGA pinout (Top View)

	1	2	3	4	5	6	7	8	9	10	11
A	$\overline{FF}$	D0	D1	DNU	PORTSZ0	PORTSZ1	DNU	DNU	RT	Q0	Q1
B	$\overline{EF}$	D2	D3	DNU	DNU	PORTSZ2	DNU	DNU	$\overline{REN}$	Q2	Q3
C	D4	D5	$\overline{WEN}$	DNU	V_{CC1}	DNU	V_{CC1}	DNU	RCLK	Q4	Q5
D	D6	D7	V_{SS}	V_{CC1}	DNU	$\overline{LD}$	DNU	V_{CC1}	Vss	Q6	Q7
E	D8	D9	V_{CC2}	V_{CC2}	V_{CCIO}	V_{CCIO}	V_{CCIO}	V_{CC2}	V_{CC2}	Q8	Q9
F	D10	D11	V_{SS}	V_{SS}	V_{SS}	DNU	V_{SS}	V_{SS}	V_{SS}	Q10	Q11
G	D12	D13	V_{CC2}	V_{CC2}	V_{CCIO}	V_{CC1}	V_{CCIO}	V_{CC2}	V_{CC2}	Q12	Q13
H	D14	D15	V_{SS}	V_{SS}	V_{SS}	V_{CC1}	V_{SS}	V_{SS}	V_{SS}	Q14	Q15
J	D16	D17	V_{CC2}	V_{CC2}	V_{CCIO}	V_{CC1}	V_{CCIO}	V_{CC2}	V_{CC2}	Q16	Q17
K	DNU	DNU	WCLK	DNU	V_{SS}	$\overline{IE}$	V_{SS}	DNU	V_{CCIO}	V_{CCIO}	V_{CCIO}
L	D18	D19	V_{CC2}	V_{CC2}	V_{CCIO}	V_{CC1}	V_{CCIO}	V_{CC2}	V_{CC2}	Q18	Q19
M	D20	D21	V_{SS}	V_{SS}	V_{SS}	V_{CC1}	V_{SS}	V_{SS}	V_{SS}	Q20	Q21
N	D22	D23	V_{CC2}	V_{CC2}	V_{CCIO}	V_{CC1}	V_{CCIO}	V_{CC2}	V_{CC2}	Q22	Q23
P	D24	D25	V_{SS}	V_{SS}	V_{SS}	$\overline{SPI_SEN}$	V_{SS}	V_{SS}	V_{SS}	Q24	Q25
R	D26	D27	V_{CC2}	V_{CC2}	V_{CCIO}	V_{CCIO}	V_{CCIO}	V_{CC2}	V_{CC2}	Q26	Q27
T	D28	D29	V_{SS}	V_{CC1}	V_{CC1}	SPI_SI	V_{CC1}	V_{CC1}	V_{SS}	Q28	Q29
U	$\overline{DVal}$	DNU	D30	D31	$\overline{PRS}$	DNU [2]	SPI_SCLK	V_{REF}	$\overline{OE}$	Q30	Q31
V	$\overline{PAF}$	$\overline{PAE}$	D32	D33	DNU	$\overline{MRS}$	MB	DNU	MARK	Q32	Q33
W	TDO	$\overline{HF}$	D34	D35	TDI	DNU	TMS	TCK	DNU	Q34	Q35

Notes
1. Pin Diagram for 18-Mbit, 36-Mbit & 72-Mbit; 1.8V & 3.3V IO voltage options.
2. This pin should be tied to V_{SS} preferably or can be left floating to ensure normal operation.

Pin Definitions

Pin Name	I/O	Pin Description
$\overline{\text{MRS}}$	Input	Master reset: $\overline{\text{MRS}}$ initializes the internal read and write pointers to zero, resets all flags and sets the output register to all zeroes. During Master Reset, the configuration registers are set to default values.
$\overline{\text{PRS}}$	Input	Partial reset: $\overline{\text{PRS}}$ initializes the internal read and write pointers to zero, resets all flags and sets the output register to all zeroes. During Partial Reset, the configuration register settings are retained.
PORTSZ [2:0]	Input	Port word size select: Port word width select pins (common for read and write ports).
WCLK	Input	Write clock: The rising edge clocks data into the FIFO when writes are enabled ($\overline{\text{WEN}}$ asserted). Data is written into the FIFO memory when $\overline{\text{LD}}$ is high and into configuration registers when $\overline{\text{LD}}$ is low.
$\overline{\text{LD}}$	Input	Load: When $\overline{\text{LD}}$ is LOW, D[7:0] (Q[7:0]) are written (read) into (from) the configuration registers. When $\overline{\text{LD}}$ is HIGH, D[35:0] (Q[35:0]) are written (read) into (from) the FIFO memory.
$\overline{\text{WEN}}$	Input	Write enable: Control signal to enable writes to the device. When $\overline{\text{WEN}}$ is low data present on the inputs is written to the FIFO memory or configuration registers on every rising edge of WCLK.
$\overline{\text{IE}}$	Input	Input enable: $\overline{\text{IE}}$ is the data input enable signal that controls the enabling and disabling of the 36-bit data input pins. If it is enabled, data on the D[35:0] pins is written into the FIFO. The internal write address pointer is always incremented at rising edge of WCLK if $\overline{\text{WEN}}$ is enabled, regardless of the $\overline{\text{IE}}$ level. This is used for 'write masking' or incrementing the write pointer without writing into a location.
D[35:0]	Input	Data inputs: Data inputs for a 36-bit bus.
RCLK	Input	Read clock: The rising edge initiates a read from the FIFO when reads are enabled ($\overline{\text{REN}}$ asserted). Data is read from the FIFO memory when $\overline{\text{LD}}$ is high & from the configuration registers if $\overline{\text{LD}}$ is low.
$\overline{\text{REN}}$	Input	Read enable: Control signal to enable reads from the device. When $\overline{\text{REN}}$ is low data is read from the FIFO memory or configuration registers on every rising edge of RCLK.
$\overline{\text{OE}}$	Input	Output enable: When $\overline{\text{OE}}$ is LOW, FIFO data outputs are enabled; when $\overline{\text{OE}}$ is HIGH, the FIFO's outputs are in High Z (high impedance) state.
Q[35:0]	Output	Data outputs: Data outputs for a 36-bit bus.
$\overline{\text{DVal}}$	Output	Data valid: Active low data valid signal to indicate valid data on Q[35:0].
MARK	Input	Mark for retransmit: When this pin is asserted the memory location corresponding to the data present on the output bus is marked. Any subsequent retransmit operation resets the read pointer to this location.
RT	Input	Retransmit: A HIGH pulse on RT resets the internal read pointer to a physical location of the FIFO which is marked by the user (using MARK pin). With every valid read cycle after retransmit, previously accessed data is read until the FIFO is empty.
MB	Input	Mailbox: When asserted the reads and writes happen to flow-through mailbox register.
$\overline{\text{EF}}$	Output	Empty flag: When $\overline{\text{EF}}$ is LOW, the FIFO is empty. $\overline{\text{EF}}$ is synchronized to RCLK.
$\overline{\text{PAE}}$	Output	Programmable almost-empty: When $\overline{\text{PAE}}$ is LOW, the FIFO is almost empty based on the almost-empty offset value programmed into the FIFO. It is synchronized to RCLK.
$\overline{\text{HF}}$	Output	Half-full flag: When $\overline{\text{HF}}$ is LOW, half of the FIFO is full. $\overline{\text{HF}}$ is synchronized to WCLK.
$\overline{\text{PAF}}$	Output	Programmable almost-full: When $\overline{\text{PAF}}$ is LOW, the FIFO is almost full based on the almost-full offset value programmed into the FIFO. It is synchronized to WCLK.
$\overline{\text{FF}}$	Output	Full flag: When $\overline{\text{FF}}$ is LOW, the FIFO is full. $\overline{\text{FF}}$ is synchronized to WCLK.
SPI_SCLK	Input	Serial clock: A rising edge on SPI_SCLK clocks the serial data present on the SPI_SI input into the offset registers if SPI_SEN is enabled.
SPI_SI	Input	Serial input: Serial input data in SPI mode.
$\overline{\text{SPI_SEN}}$	Input	Serial enable: Enables serial loading of programmable flag offsets and configuration registers.
TCK	Input	Test clock (TCK) pin for JTAG.
TMS	Input	Test mode select (TMS) pin for JTAG.

Pin Definitions (continued)

Pin Name	I/O	Pin Description
TDI	Input	Test data in (TDI) pin for JTAG.
TDO	Output	Test data out (TDO) pin for JTAG.
V_{REF}	Input Reference	Reference voltage: Reference voltage (regardless of I/O standard used)
V_{CC1}	Power Supply	Core voltage supply 1: 1.8 V supply voltage
V_{CC2}	Power Supply	Core voltage supply 2: 1.5 V supply voltage
V_{CCIO}	Power Supply	Supply for I/Os
V_{SS}	Ground	Ground
DNU	–	Do not use: These pins need to be left floating.

Architecture

The CYF0072V, CYF0036V, and CYF0018V are memory arrays of 72-Mbit, 36-Mbit, and 18-Mbit respectively. The memory organization is user configurable and word sizes can be selected as × 9, × 12, × 16, × 18, × 20, × 24, × 32, or × 36. The logic blocks to implement the FIFO functionality and the associated features are built around these memory arrays.

The input and output data buses have a maximum width of 36 bits. The input data bus goes to an input register and the data flow from the input register to the memory is controlled by the write control logic. The inputs to the write logic block are WCLK, WEN and IE. When the writes are enabled through WEN and if the inputs are enabled by IE, then the data on the input bus is written into the memory array at the rising edge of WCLK. This also increments the write pointer. Enabling writes but disabling the data input pins through IE only increments the write pointer without doing any writes or altering the contents of the memory location.

Similarly, the output register is connected to the data output bus. Transfer of contents from the memory to the output register is controlled by the read control logic. The inputs to the read control logic include RCLK, REN, OE, RT and MARK. When reads are enabled by REN and outputs are enabled using OE, the data from the memory pointed by the read pointer is transferred to the output data bus at the rising edge of RCLK along with active low DVal. If the outputs are disabled but the reads enabled, the outputs are in high impedance state, but internally the read pointer is incremented.

During write operation, the number of writes performed is always an even number (i.e., minimum write burst length is two and number of writes always a multiple of two). Whereas during read operation, the number of reads performed can be even or odd (i.e., minimum read burst length is one).

The MARK signal is used to ‘mark’ the location from which data is retransmitted when requested and RT is asserted to retransmit the data from the marked location.

Reset Logic

The FIFO can be reset in two ways: Master Reset ($\overline{MRS}$) and Partial Reset ($\overline{PRS}$). The $\overline{MRS}$ initializes the read and write pointers to zero and sets the output register to all zeroes. It also resets all flags & the configuration registers to their default values. The word size is configured through pins; values of the three PORTSZ pins are latched during $\overline{MRS}$. A Master Reset is required after power-up before accessing the FIFO.

$\overline{PRS}$ resets the read pointer, write pointer and mark location to the first physical location in the memory array. It also resets all flags to their default values. $\overline{PRS}$ does not affect the programmed configuration register values. Any changes to configuration registers during device operation mandates a $\overline{PRS}$ cycle to guarantee accurate flag operation.

Selecting Word Sizes

The word sizes are configured based on the logic levels on the PORTSZ pins during the master reset ($\overline{MRS}$) cycle only (latched on low to high edge). The port size cannot be changed during normal mode of operation and these pins are ignored. Table 1. explains the pins of D[35:0] and Q[35:0] that will have valid data in modes where the word size is less than × 36. If word size is less than × 36, the unused output pins are tri-stated by the device and unused input pins will be ignored by the internal logic. The pins with valid data input D[N:0] and output Q[N:0] is given in Table 1.

Memory Organization for Different Port Sizes

The 72-Mbit memory has different organization for different port sizes. Table 1 shows the depth of the FIFO for all port sizes.

Note that for all port sizes, four to eight locations are not available for writing the data and are used to safeguard against false synchronization of empty and full flags.

Table 1. Word Size Selection

PORTSZ[2:0]	Word Size	FIFO Depth [3]	Memory Size [3]	Active Input Data Pins D[N:0]	Active Output Data Pins Q[N:0]
000	× 9	8 Meg	72-Mbit	D[8:0]	Q[8:0]
001	× 12	4 Meg	48-Mbit	D[11:0]	Q[11:0]
010	× 16	4 Meg	64-Mbit	D[15:0]	Q[15:0]
011	× 18	4 Meg	72-Mbit	D[17:0]	Q[17:0]
100	× 20	2 Meg	40-Mbit	D[19:0]	Q[19:0]
101	× 24	2 Meg	48-Mbit	D[23:0]	Q[23:0]
110	× 32	2 Meg	64-Mbit	D[31:0]	Q[31:0]
111	× 36	2 Meg	72-Mbit	D[35:0]	Q[35:0]

Note
3. For all port sizes, four to eight locations are not available for writing the data.

Data Valid Signal (DVal)

Data valid (DVal) is an active low signal, synchronized to RCLK and is provided to check for valid data on the output bus. When a read operation is performed, the DVal signal goes low along with output data. This helps user to capture the data without keeping track of REN to data output latency. This signal also helps when write and read operations are performed continuously at different frequencies by indicating when valid data is available at the output port Q[35:0].

Write Mask and Read Skip Operation

As mentioned in Architecture on page 7, enabling writes but disabling the inputs (IE HIGH) increments the write pointer without doing any write operations or altering the contents of the location.

This feature is called Write Mask and allows user to move the write pointer without actually writing to the locations. This “write masking” ability is useful in some video applications such as Picture In Picture (PIP).

Similarly, during a read operation, if the outputs are disabled by keeping the OE high, the read data does not appear on the output bus; however, the read pointer is incremented. This feature is referred to as a Read Skip Operation.

Flow-through Mailbox Register

This feature transfers data from input to output directly bypassing the FIFO sequence. When MB signal is asserted the data present in D[35:0] will be available at Q[35:0] after two WCLK cycles. Normal read and write operations are not allowed during flow-through mailbox operation. Before starting Flow-through mailbox operation FIFO read should be completed to make data valid DVal high in order to avoid data loss from FIFO. The width of flow-through mailbox register always corresponds to port size.

Flag Operation

This device provides five flag pins to indicate the condition of the FIFO.

Full Flag

The Full Flag (FF) operates on double word (burst length of two) boundaries and goes LOW when the device is full. Write operations are inhibited whenever FF is LOW regardless of the state of WEN. FF is synchronized to WCLK, that is, it is exclusively updated by each rising edge of WCLK. The worst case assertion latency for Full Flag is four. As the user cannot know that the FIFO is full for four clock cycles, it is possible that user continues writing data during this time. In this case, the four data words written will be stored to prevent data loss and these words have to be read back in order for full flag to get de-asserted. The minimum number of reads required to de-assert full-flag is two and the maximum number of reads required to de-assert full flag is six. The assertion and de-assertion of Full flag with associated latencies is explained in Latency Table on page 14.

Half-Full Flag

The Half-Full (HF) flag goes LOW when half of the memory array is written. HF is synchronized to WCLK. The assertion and de-assertion of Half-Full flag with associated latencies is explained in Latency Table on page 17.

Empty Flag

The Empty Flag (EF) deassertion depends on burst writes and goes LOW when the device is empty. Read operations are inhibited whenever EF is LOW, regardless of the state of REN. EF is synchronized to RCLK, that is, it is exclusively updated by each rising edge of RCLK. The assertion and de-assertion of Empty flag with associated latencies is explained in Latency Table on page 17.

Programmable Almost-Empty and Almost-Full Flags

The CYF0072V includes programmable Almost-Empty and Almost-Full flags. Each flag operates on word boundaries and is programmed (see Programming Flag Offsets and Configuration Registers on page 9) a specific distance from the corresponding boundary flags (Empty or Full). (offset can range from 16 to 1023) When the FIFO contains the number of words for which the flags are programmed, the PAF or PAE is asserted, signifying that the FIFO is either almost-full or almost-empty. The default flag offset for both PAE and PAF is 127 words. These programmable flag boundaries have thresholds associated with them. Table 2 gives the assertion and de-assertion conditions for PAE & PAF flags based on these thresholds assuming default offset values.

The PAF flag signal transition is caused by the rising edge of WCLK and the PAE flag transition is caused by the rising edge of RCLK. The assertion and de-assertion of these flags with associated latencies is explained in Latency Table on page 17.

Table 2. Programmable Flag Assertion/De-assertion Thresholds

Operation	PAE offset	Number of FIFO words - PAE	PAF offset	Number of FIFO words - PAF
Assertion	127	# FIFO words <= (PAE offset + 2) i.e. # FIFO words <= 129	127	# FIFO words >= FIFO depth - (offset + 1) i.e. # FIFO words >= 2M - 128
Deassertion	127	# FIFO words > (offset) i.e. # FIFO words > 127	127	# FIFO words < FIFO depth - (offset) i.e. # FIFO words < 2M - 127

Retransmit from Mark Operation

The retransmit feature is useful for transferring packets of data repeatedly. It enables the receipt of data to be acknowledged by the receiver and retransmitted if necessary. Initiation of a retransmit operation (using RT pin) resets the internal read pointer to a physical location of the FIFO that is marked by the user (using the MARK pin). With every valid read cycle after retransmit, data is read out starting from the marked location and the read pointer is incremented until the FIFO is empty. Data written to FIFO after initiation of a retransmit operation are also transmitted. The full depth of the FIFO can be repeatedly retransmitted.

Flags are governed by the relative locations of the read and write pointers and are updated during a retransmit cycle. Refer to the latency table for the associated flag update latencies after initiation of a retransmit cycle.

Asserting RT initiates a retransmit operation. The retransmit feature can be used when two or more data words have been written to the FIFO. When the MARK pin is asserted, the memory location corresponding to the data present on the output bus is marked. A mark operation is mandated prior to initiating a Retransmit operation.

A retransmit operation should not be initiated when reads or writes are in progress. User should wait for four RCLK cycles after disabling reads before RT is asserted to ensure that the reads are completed.

On initiation of RT the ‘marked’ location becomes the new Full Boundary. If user continues to write the data after initiation of a retransmit operation, FF will be asserted when this boundary is reached i.e. FF is asserted once the write pointer reaches the marked location.This prevents overwriting and data-loss. During RT reads the full boundary remains frozen to the marked location and is released when the FIFO becomes empty. i.e. FF remains LOW until the entire FIFO is read. Full flag is released $L_{FF_RELEASE}$ clocks after the EF is asserted. Full boundary is also released on a reset operation (MRS or PRS).

Refer to Latency Table on page 17 for more details.

Programming Flag Offsets and Configuration Registers

The CYF0072V has ten 8-bit user configurable registers. These registers contain the almost-full (M) and almost-empty (N) offset values which decide when the PAF and PAE flags are asserted.

These registers can be programmed in one of two ways: serial loading or parallel loading method. The loading method is selected using the SPI_SEN (Serial Enable) pin. A low on the SPI_SEN selects the serial method for writing into the registers. For serial programming, there is a separate SCLK and a Serial Input (SI). In parallel mode, a LOW on the load (LD) pin causes the write and read operation to these registers. The write and read operation happens from the first location (0x1) to the last location (0xA) in a sequence. If LD is HIGH, the writes occur to the FIFO.

Register values can be read through the parallel output port regardless of the programming mode selected (serial or parallel). Register values cannot be read serially. The registers may be programmed (and reprogrammed) any time after master reset, regardless of whether serial or parallel programming is selected. Any changes to configuration registers during device operation mandates a PRS cycle to guarantee accurate flag operation.

See Table 4 on page 11 and Table 5 on page 12 for access to configuration registers in serial and parallel modes.

In parallel mode, the read and write operations loop back when the maximum address location of the configuration registers is reached. Simultaneous read and write operations should be avoided on the configuration registers. Any change in configuration registers will take effect after eight write clock cycles (WCLK) cycles.

Table 3. Configuration Registers

ADDR	Configuration Register	Default	Bit [7]	Bit [6]	Bit [5]	Bit [4]	Bit [3]	Bit [2]	Bit [1]	Bit [0]
0x1	Reserved	0x00	X	X	X	X	X	X	X	X
0x2	Reserved	0x00	X	X	X	X	X	X	X	X
0x3	Reserved	0x00	X	X	X	X	X	X	X	X
0x4	Almost-Empty Flag generation address - (LSB) (N)	0x7F	D7	D6	D5	D4	D3	D2	D1	D0
0x5	Almost-Empty Flag generation address - (MSB) (N)	0x00	X	X	X	X	X	X	D9	D8
0x6	Reserved	0x00	X	X	X	X	X	X	X	X
0x7	Almost-Full Flag generation address - (LSB) (M)	0x7F	D7	D6	D5	D4	D3	D2	D1	D0
0x8	Almost-Full Flag generation address - (MSB) (M)	0x00	X	X	X	X	X	X	D9	D8
0x9	Reserved	0x00	X	X	X	X	X	X	X	X
0xA	Fast CLK Bit Register	1XXXXXXXb	Fast CLK bit	X	X	X	X	X	X	X

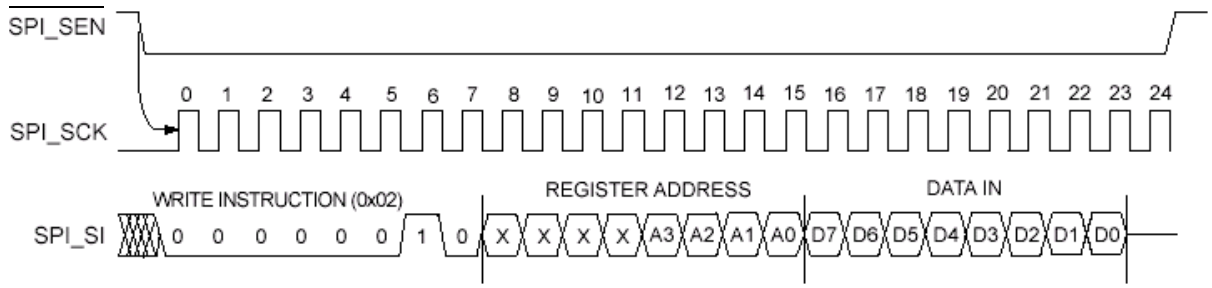
Table 4. Writing and Reading Configuration Registers in Parallel Mode

$\overline{\text{SPI_SEN}}$	$\overline{\text{LD}}$	$\overline{\text{WEN}}$	$\overline{\text{REN}}$	WCLK	RCLK	SPI_SCLK	Operation
1	0	0	1	↑ First rising edge because both LD and WEN are low	X	X	Parallel write to first register
1	0	0	1	↑ Second rising edge	X	X	Parallel write to second register
1	0	0	1	↑ Third rising edge	X	X	Parallel write to third register
1	0	0	1	↑ Fourth rising edge	X	X	Parallel write to fourth register
1	0	0	1	•	X	X	•
1	0	0	1	•	X	X	•
1	0	0	1	•	X	X	•
1	0	0	1	↑ Tenth rising edge	X	X	Parallel write to tenth register
1	0	0	1	↑ Eleventh rising edge	X	X	Parallel write to first register (roll back)
1	0	1	0	X	↑ First rising edge since both LD and REN are low	X	Parallel read from first register
1	0	1	0	X	↑ Second rising edge	X	Parallel read from second register
1	0	1	0	X	↑ Third rising edge	X	Parallel read from third register
1	0	1	0	X	↑ Fourth rising edge	X	Parallel read from fourth register
1	0	1	0	X	•	X	•
1	0	1	0	X	•	X	•
1	0	1	0	X	•	X	•
1	0	1	0	X	↑ Tenth rising edge	X	Parallel read from tenth register
1	0	1	0	X	↑ Eleventh rising edge	X	Parallel read from first register (roll back)
1	X	1	1	X	X	X	No operation
X	1	0	X	↑ Rising edge	X	X	Write to FIFO memory
X	1	X	0	X	↑ Rising edge	X	Read from FIFO memory
0	0	X	1	X	X	X	Illegal operation

Table 5. Writing into Configuration Registers in Serial Mode

$\overline{\text{SPI_SEN}}$	$\overline{\text{LD}}$	$\overline{\text{WEN}}$	$\overline{\text{REN}}$	WCLK	RCLK	SCLK	Operation
0	1	X	X	X	X	↑ Rising edge	Each rising of the SCLK clocks in one bit from the SI (Serial In). Any of the 10 registers can be addressed and written to, following the SPI protocol.
X	1	0	X	↑ Rising edge	X	X	Parallel write to FIFO memory.
X	1	X	0	X	↑ Rising edge	X	Parallel read from FIFO memory.
1	0	1	1	X	X	X	This corresponds to parallel mode (refer to Table 4 on page 11).

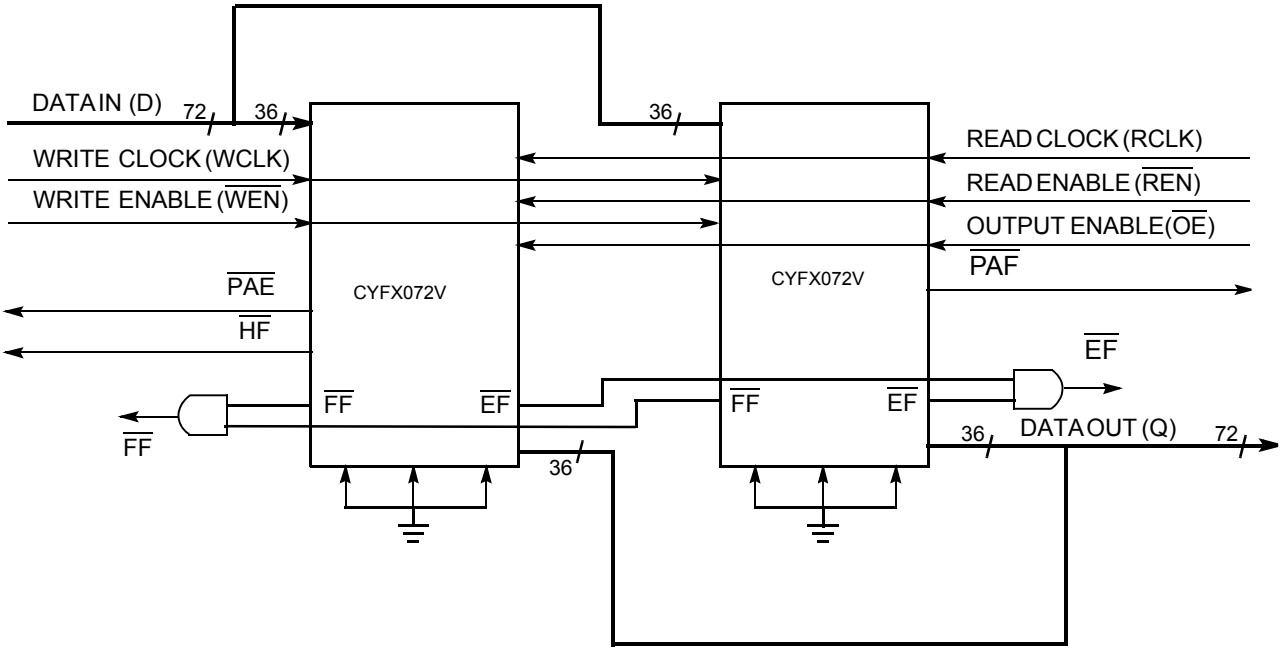
Figure 2. Serial WRITE to Configuration Register



Width Expansion Configuration

The width of CYFX072V can be expanded to provide word widths greater than 36 bits. During width expansion mode, all control line inputs are common and all flags are available. Empty (Full) flags are created by ANDing the Empty (Full) flags of every FIFO; the PAE and PAF flags can be detected from any one device. This technique avoids reading data from or writing data to the FIFO that is “staggered” by one clock cycle due to the variations in skew between RCLK and WCLK. Figure 3 demonstrates an example of 72 bit-word width by using two 36-bit word CYFX072Vs.

Figure 3. Using Two CYFX072V for Width Expansion



Power Up

The device becomes functional after V_{CC1}, V_{CC2}, V_{CCIO}, and V_{REF} attain minimum stable voltage required as given in Recommended DC Operating Conditions on page 16. The device can be accessed t_{PU} time after these supplies attain the minimum required level (see Switching Characteristics on page 19). There is no specific power sequencing required for the device.

Read/Write Clock Requirements

The read and write clocks must satisfy the following requirements:

- Both read (RCLK) and write (WCLK) clocks should be free-running.
- The clock frequency for both clocks should be between the minimum and maximum range given in Electrical Characteristics on page 16.
- The WCLK to RCLK ratio should be in the range of 0.5 to 2.

For proper FIFO operation, the device must determine which of the input clocks – RCLK or WCLK – is faster. This is evaluated using counters after the MRS cycle. The device uses two 9-bit counters (one running on RCLK and other on WCLK), which count 256 cycles of read and write clocks after MRS. The clock of the counter which reaches its terminal count first is used as master clock inside the FIFO.

When there is change in the relative frequency of RCLK and WCLK during normal operation of FIFO, user can specify it by using “Fast CLK bit” in the configuration register (0xA).

“1” - indicates f_{req} (WCLK) > f_{req} (RCLK)

“0” - indicates f_{req} (WCLK) < f_{req} (RCLK)

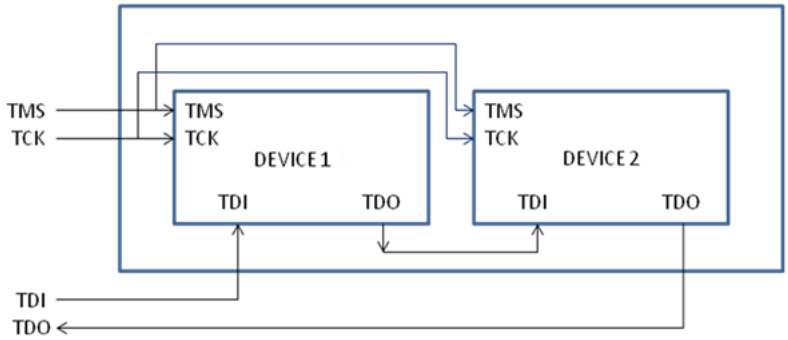
The result of counter evaluated frequency is available in this register bit. User can override the counter evaluated frequency for faster clock by changing this bit.

Whenever there is a change in this bit value, user must wait t_{PLL} time before issuing the next read or write to FIFO.

JTAG Operation

The Programmable FIFO has two devices connected internally in a JTAG chain as shown in figure Figure 4.

Figure 4. Device Connection in a JTAG Chain



Test Access Port

Test Clock (TCK)

The test clock is used only with the TAP controller. All inputs are captured on the rising edge of TCK. All outputs are driven on the falling edge of TCK.

Test Mode Select (TMS)

The TMS input is used to give commands to the TAP controller and is sampled on the rising edge of TCK. This pin may be left unconnected if the TAP is not used. The pin is pulled up internally, resulting in a logic HIGH level.

Test Data-In (TDI)

The TDI pin is used to serially input information into the registers and can be connected to the input of any of the registers. The register between TDI and TDO is chosen by the instruction that is loaded into the TAP instruction register. For information on loading the instruction register, see the TAP Controller State Diagram. TDI is internally pulled up and can be left unconnected if the TAP is unused in an application. TDI is connected to the most significant bit (MSB) on any of the TAP registers.

Test Data-Out (TDO)

The TDO output pin is used to serially clock data out from the registers. The output is active, depending upon the current state of the TAP state machine. The output changes on the falling edge of TCK. TDO is connected to the least significant bit (LSB) of any of the TAP registers.

Note: Reset is performed by forcing TMS HIGH (V_{DD}) for five rising edges of TCK.

Tap Registers

Registers are connected between the TDI and TDO pins to scan the data in and out of the test circuitry. Only one register can be selected at a time through the instruction registers. Data is serially loaded into the TDI pin on the rising edge of TCK. Data is output on the TDO pin on the falling edge of TCK.

Instruction Register

Three-bit instructions can be serially loaded into the instruction register. This register is loaded when it is placed between the TDI and TDO pins, as shown in Figure 5. Upon power-up, the instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a Reset state.

Bypass Register

To save time when serially shifting data through registers, it is sometimes advantageous to skip certain chips. The bypass register is a single-bit register that can be placed between TDI and TDO pins. This enables shifting of data through the device with minimal delay.

Boundary Scan Register

The boundary scan register is connected to all of the input and output pins on the device. Several No Connect (NC) pins are also included in the scan register to reserve pins for higher density devices.

The boundary scan register is loaded with the contents of the device input and output ring when the TAP controller is in the Capture-DR state and is then placed between the TDI and TDO pins when the controller is moved to the Shift-DR state. The EXTEST, SAMPLE/PRELOAD instructions can be used to capture the contents of the input and output ring. The MSB of the register is connected to TDI and the LSB is connected to TDO.

Identification (ID) Register

The ID register is loaded with a vendor-specific, 32-bit code during the Capture-DR state when the IDCODE command is loaded in the instruction register. The IDCODE is hardwired into the device and can be shifted out when the TAP controller is in the Shift-DR state. The ID register has a vendor code and other information described in Table 6.

JTAG ID Codes

Table 6. JTAG IDCODES

	IR Register Length	Device ID (HEX)	Bypass Register Length
Device-1	3	"Ignore"	1
Device-2	8	1E3261CF	1

OPCODES Supported

Table 7. OPCODES Supported

Device-1	Opcode (Binary)		Device-2	Opcode (Binary)
BYPASS	111		BYPASS	11111111
			EXTEST	00000000
			HIGHZ	00000111
			SAMPLE/PRELOAD	00000001
			IDCODE	00001111

JTAG Instructions

IDCODE

The IDCODE instruction loads a vendor-specific, 32-bit code into the instruction register. It also places the instruction register between the TDI and TDO pins and shifts the IDCODE out of the device when the TAP controller enters the Shift-DR state. The IDCODE instruction is loaded into the instruction register at power-up or whenever the TAP controller is supplied a Test-Logic-RST state.

SAMPLE/PRELOAD

SAMPLE/PRELOAD is an IEEE 1149.1 mandatory instruction. When the SAMPLE/PRELOAD instructions are loaded into the instruction register and the TAP controller is in the Capture-DR state, a snapshot of data on the input and output pins is captured in the boundary scan register.

PRELOAD places an initial data pattern at the latched parallel outputs of the boundary scan register cells before the selection of another boundary scan test operation.

The shifting of data for the SAMPLE and PRELOAD phases can occur concurrently when required; that is, while the data captured is shifted out, the preloaded data can be shifted in.

BYPASS

When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a Shift-DR state, the bypass register is placed between the TDI and TDO pins. The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board.

HIGHZ

The HIGHZ instruction mode is used to set all the user I/O pins to an inactive drive state. These pins are tri-stated until a new JATG instruction is executed. When this instruction is selected, the bypass register is connected between the TDI and TDO ports.

EXTEST

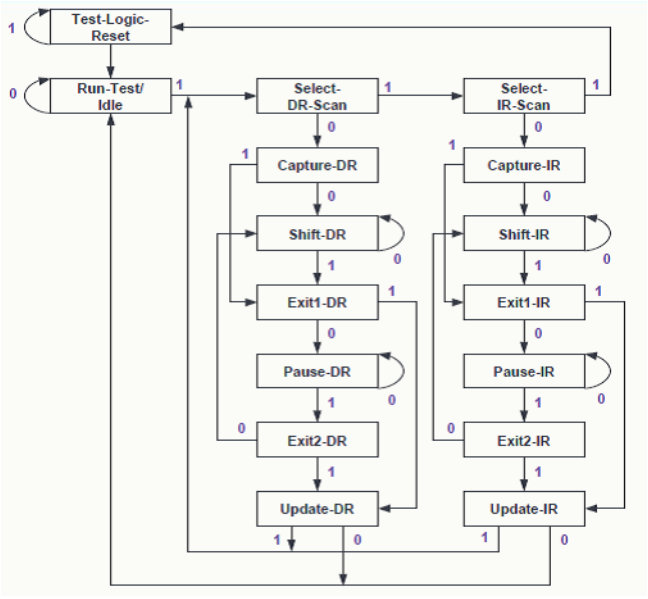
The EXTEST instruction drives the preloaded data out through the system output pins. This instruction also connects the boundary scan register for serial access between the TDI and TDO in the Shift-DR controller state.

Instruction Update and Bypass

1. Every time an instruction is loaded through JTAG port, BYPASS command needs to be loaded on device 1.
   For example, to push PRELOAD command, BYPASS to device-1 "111" + PRELOAD to device-2 "00000001" needs to be sent.
2. When both devices are put on BYPASS, any pattern sent in should be observed on TDO after two TCK delay.

TAP Controller State Diagram

Figure 5. TAP Controller State Diagram



TAP controller is a Finite State Machine with 16 states as shown in Figure 5. State change is determined by the state of TMS on rising edge of TCK. Figure 5 shows the value of TMS for each state transition.

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. These user guidelines are not tested.

Storage temperature (without bias) ..... –65 °C to +150 °C

Ambient temperature with power applied ..... –55 °C to +125 °C

Core supply voltage 1 (V_{CC1}) to ground potential .....–0.3 V to 2.5 V

Core supply voltage 2 (V_{CC2}) to ground potential .....–0.3 V to 1.65 V

Latch up current ..... >100 mA

I/O port supply voltage (V_{CCIO}) .....–0.3 V to 3.7 V

Voltage applied to I/O pins .....–0.3 V to 3.75 V

Output current into outputs (LOW) ..... 24 mA

Static discharge voltage (per MIL–STD–883, Method 3015) ..... > 2001 V

Operating Range

Range	Ambient Temperature
Industrial	–40 °C to +85 °C

Recommended DC Operating Conditions

Parameter [4]	Description		Min	Typ	Max	Unit
V_{CC1}	Core supply voltage 1		1.70	1.80	1.90	V
V_{CC2}	Core supply voltage 2		1.425	1.5	1.575	V
V_{REF}	Reference voltage (irrespective of I/O standard used)		0.7	0.75	0.8	V
V_{CCIO}	I/O supply voltage, read and write banks.	LVCMOS33	3.00	3.30	3.60	V
		LVCMOS18	1.70	1.8	1.90	V

Electrical Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
I_{CC}	Active current	$V_{CC1} = V_{CC1MAX}$	–	–	300	mA
		$V_{CC2} = V_{CC2MAX}$ (All I/O switching, 133 MHz)	–	–	600	mA
		$V_{CCIO} = V_{CCIOMAX}$ (All outputs disabled)	–	–	100	mA
I_I	Input pin leakage current	$V_{IN} = V_{CCIOmax}$ to 0 V	–15	–	15	µA
I_{OZ}	I/O pin leakage current	$V_O = V_{CCIOmax}$ to 0 V	–15	–	15	µA
C_P	Capacitance for TMS and TCK	–	–	–	16	pF
C_{PIO}	Capacitance for all other pins except TMS and TCK	–	–	–	8	pF

Note
4. Device operation guaranteed for a supply rate > 1 V / µs.

I/O Characteristics

(Over the operating range)

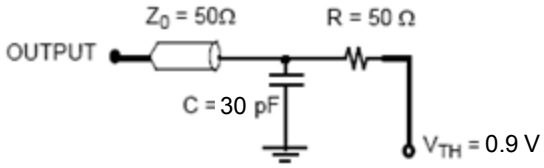
I/O Standard	Nominal I/O Supply Voltage	Input Voltage (V)		Output Voltage (V)		Output Current (mA)	
		V_{IL}(max)	V_{IH}(min)	V_{OL}(max)	V_{OH}(min)	I_{OL}(max)	I_{OH}(max)
LVCMOS33	3.3 V	0.80	2.20	0.45	2.40	24	24
LVCMOS18	1.8 V	30% V_{CCIO}	65% V_{CCIO}	0.45	V_{CCIO} – 0.45	16	16

Latency Table

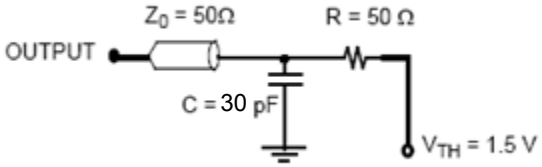
Latency Parameter	Number of Cycles	Detail
$L_{\overline{FF}_ASSERT}$	Max = 4	Last data write to $\overline{FF}$ going low.
$L_{\overline{EF}_ASSERT}$	0	Last data read to $\overline{EF}$ going low.
$L_{\overline{PRS}_TO_ACTIVE}$	32 [5]	$\overline{PRS}$ deassert to normal operation.
$L_{MAILBOX}$	2	Latency from write port to read port when MB = 1 (wrt WCLK).
$L_{\overline{REN}_TO_DATA}$	4	Latency when $\overline{REN}$ is asserted low to first data output from FIFO.
$L_{\overline{REN}_TO_CONFIG}$	4	Latency when $\overline{REN}$ is asserted along with $\overline{LD}$ to first data read from configuration registers.
$L_{\overline{WEN}_TO_\overline{PAE}_HI}$	5 [5]	Write to $\overline{PAE}$ going high.
$L_{\overline{WEN}_TO_\overline{PAF}_LO}$	5 [5]	Write to $\overline{PAF}$ going low.
$L_{\overline{REN}_TO_\overline{PAE}_LO}$	7 [5]	Read to $\overline{PAE}$ going low.
$L_{\overline{REN}_TO_\overline{PAF}_HI}$	7 [5]	Read to $\overline{PAF}$ going high.
$L_{\overline{FF}_DEASSERT}$	8 [5]	Read to $\overline{FF}$ going high.
$L_{RT_TO_\overline{REN}}$	17	First RCLK posedge after RT goes low to initiation of reads by pulling $\overline{REN}$ low. Flags update within this period after initiation of a retransmit operation.
$L_{RT_TO_DATA}$	Max = 21 [5]	First RCLK posedge after RT goes LOW to valid data on Q[35:0].
L_{IN}	Max = 26 [5]	Initial latency for data read after FIFO goes empty during simultaneous read/write.
$L_{\overline{EF}_DEASSERT}$	Max = 24 [5]	Write to $\overline{EF}$ going high.
$L_{\overline{FF}_RELEASE}$	Max = 6	$\overline{EF}$ going low to $\overline{FF}$ deassert during retransmit reads.

Note
5. These latency values are valid for a clock ratio of 1.

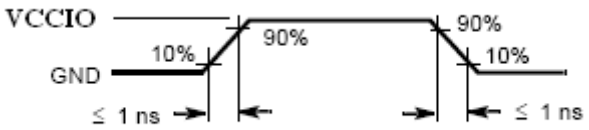
Figure 6. AC Test Load Conditions



(a) V_{CCIO} = 1.8 Volt



(b) V_{CCIO} = 3.3 Volt



(c) All Input Pulses

Switching Characteristics

Parameter	Description		-133		Unit
			Min	Max	
t_{PU}	Power-up time after all supplies reach minimum value		–	2	ms
t_S	Clock cycle frequency	3.3 V LVCMOS	24	133	MHz
t_S	Clock cycle frequency	1.8 V LVCMOS	24	133	MHz
t_A	Data access time		–	10	ns
t_{CLK}	Clock cycle time		7.5	41.67	ns
t_{CLKH}	Clock high time		3.375	–	ns
t_{CLKL}	Clock low time		3.375	–	ns
t_{DS}	Data setup time		3	–	ns
t_{DH}	Data hold time		3	–	ns
t_{ENS}	Enable setup time		3	–	ns
t_{ENH}	Enable hold time		3	–	ns
t_{ENS_SI}	Setup time for SPI_SI and $\overline{\text{SPI_SEN}}$ pins		5	–	ns
t_{ENH_SI}	Hold time for SPI_SI and $\overline{\text{SPI_SEN}}$ pins		5	–	ns
t_{RATE_SPI}	Frequency of SCLK		–	25	MHz
t_{RS}	Reset pulse width		100	–	ns
t_{PZS}	Port size select to $\overline{\text{MRS}}$ seup time		25	–	ns
t_{PZH}	$\overline{\text{MRS}}$ to port size select hold time		25	–	ns
t_{RSF}	Reset to flag output time		–	50	ns
t_{PRT}	Retransmit pulse width		5	–	RCLK cycles
t_{OLZ}	Output enable to output in Low Z		4	15	ns
t_{OE}	Output enable to output valid		–	15	ns
t_{OHZ}	Output enable to output in High Z		–	15	ns
t_{WFF}	Write clock to $\overline{\text{FF}}$		–	8.5	ns
t_{REF}	Read clock to $\overline{\text{EF}}$		–	8.5	ns
t_{PAF}	Clock to $\overline{\text{PAF}}$ flag		–	17	ns
t_{PAE}	Clock to $\overline{\text{PAE}}$ flag		–	17	ns
t_{HF}	Clock to $\overline{\text{HF}}$ flag		–	17	ns
t_{PLL}	Time required to synchronize PLL		–	1024	cycles
t_{RATE_JTAG}	JTAG TCK cycle time		100	–	ns
t_{S_JTAG}	Setup time for JTAG TMS,TDI		8	–	ns
t_{H_JTAG}	Hold time for JTAG TMS,TDI		8	–	ns
t_{CO_JTAG}	JTAG TCK low to TDO valid		–	20	ns

Switching Waveforms

Figure 7. Write Cycle Timing

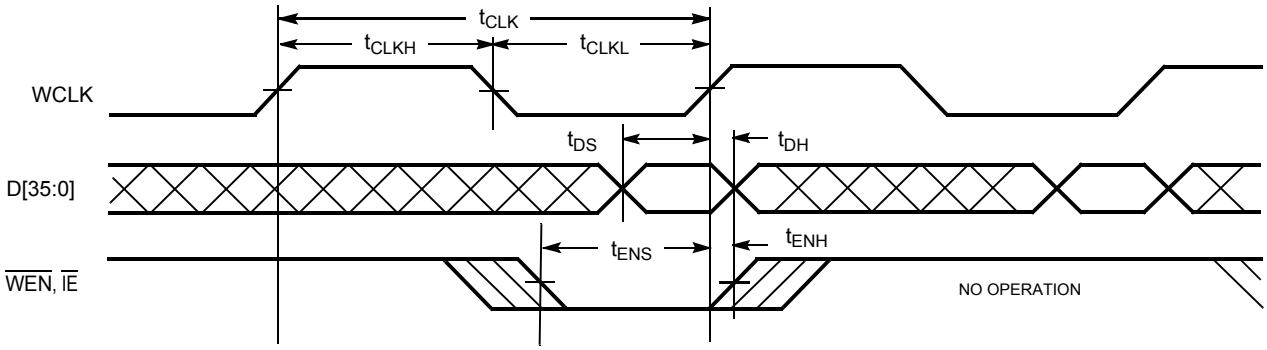
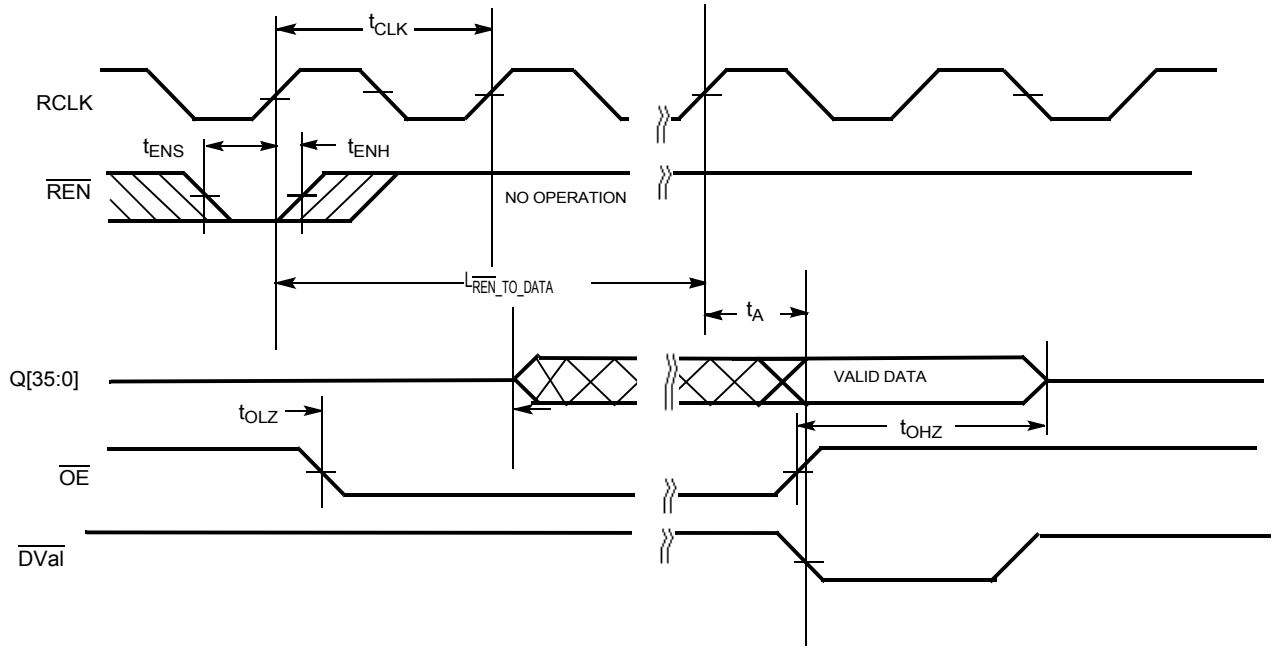


Figure 8. Read Cycle Timing



Switching Waveforms (continued)

Figure 9. Reset Timing

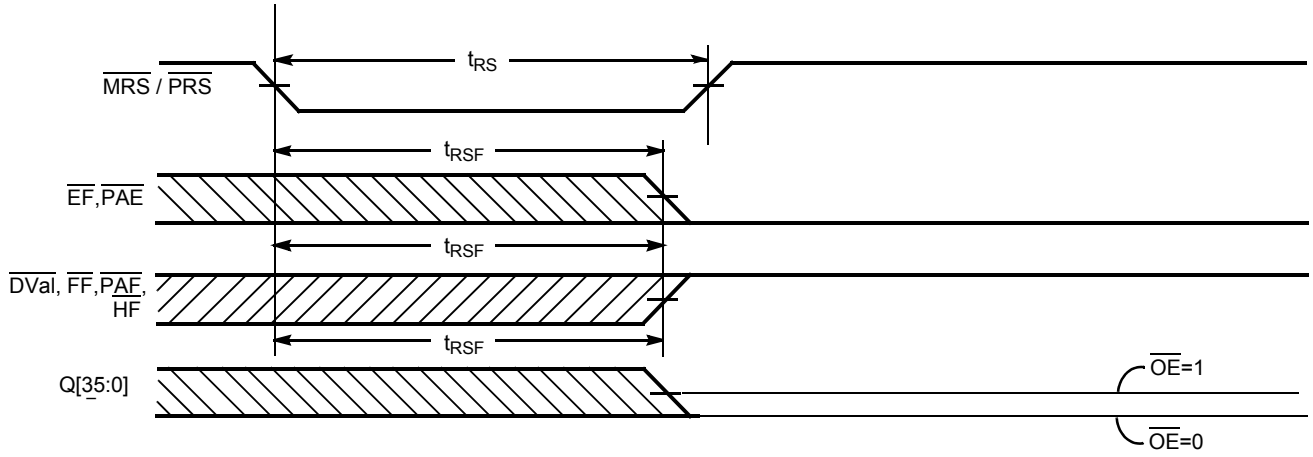
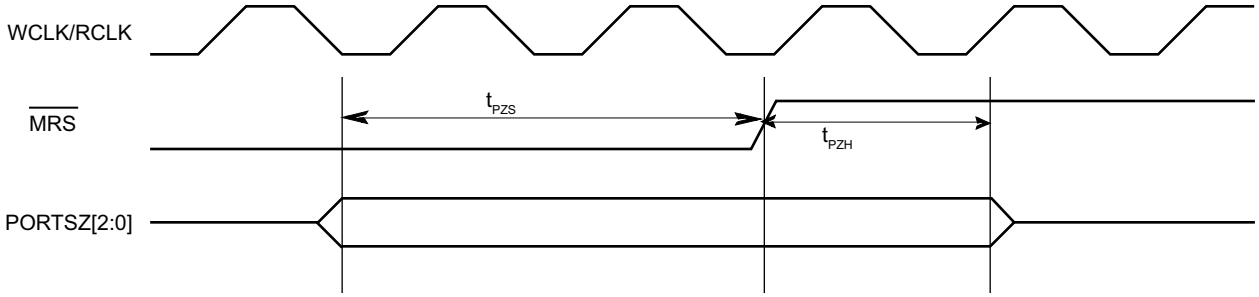


Figure 10. MRS to PORTSZ[2:0]



Switching Waveforms (continued)

Figure 11. Empty Flag Timing

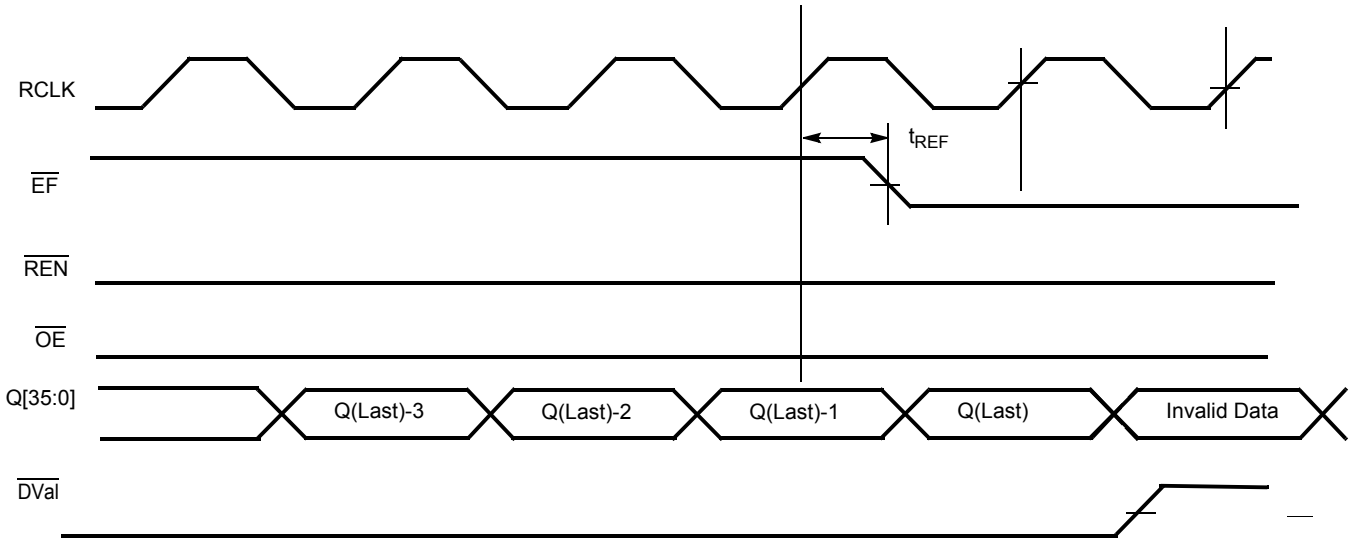
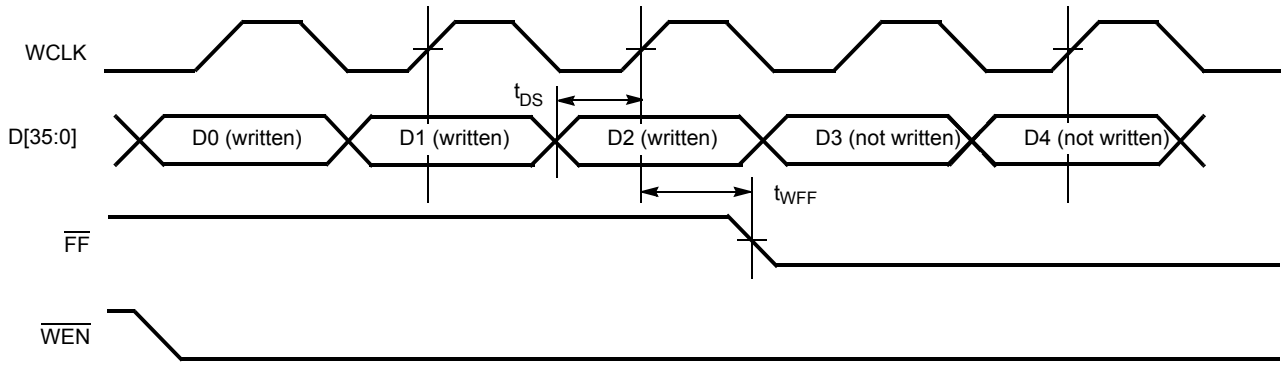


Figure 12. Full Flag Timing



Switching Waveforms (continued)

Figure 13. Initial Data Latency

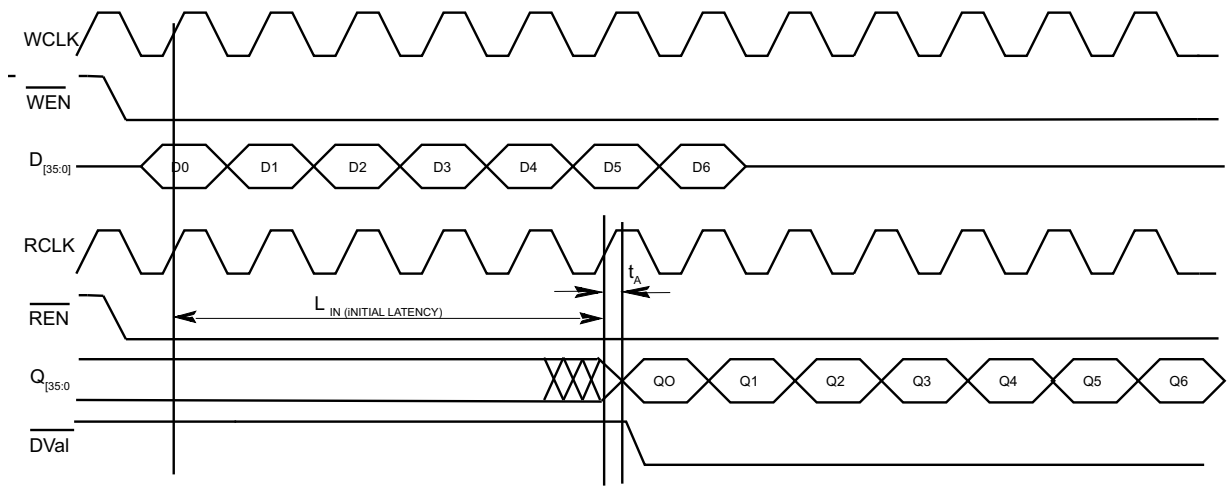
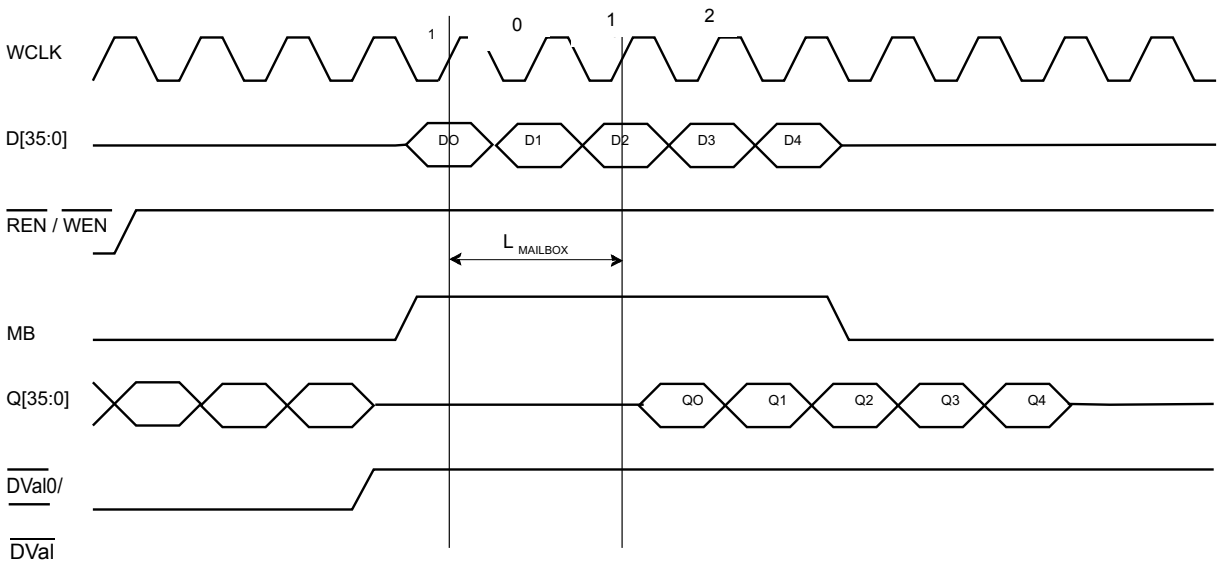


Figure 14. Flow-through Mailbox Operation



Switching Waveforms (continued)

Figure 15. Configuration Register Write

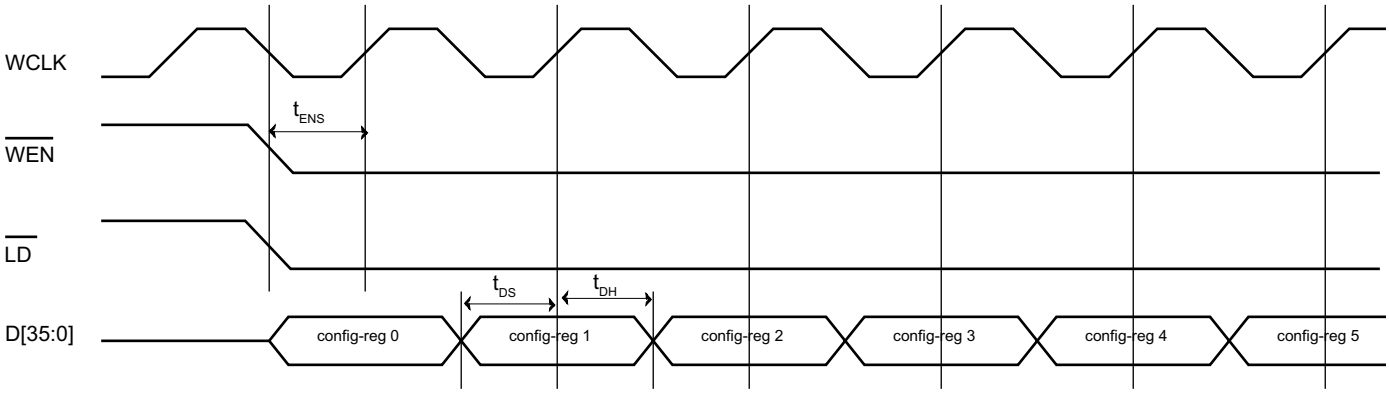


Figure 16. Configuration Register Read

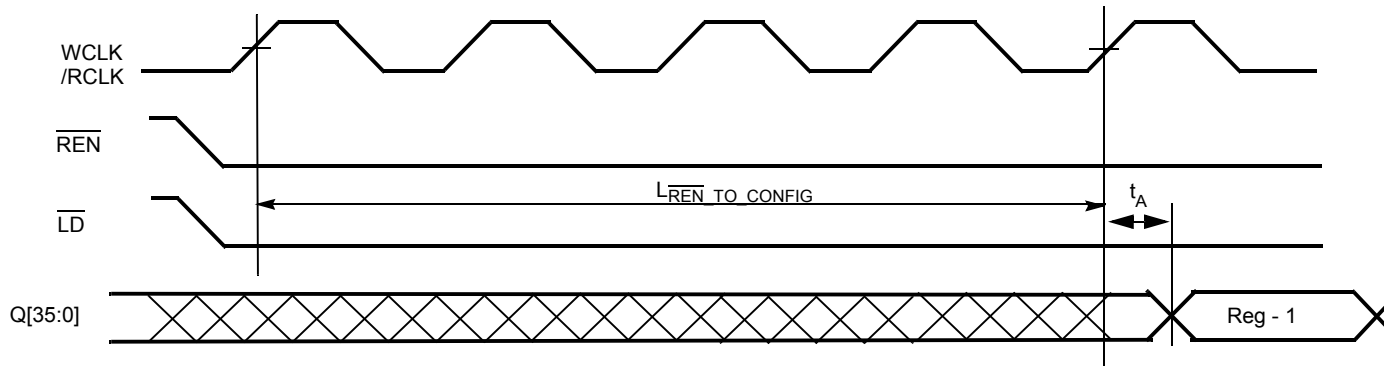
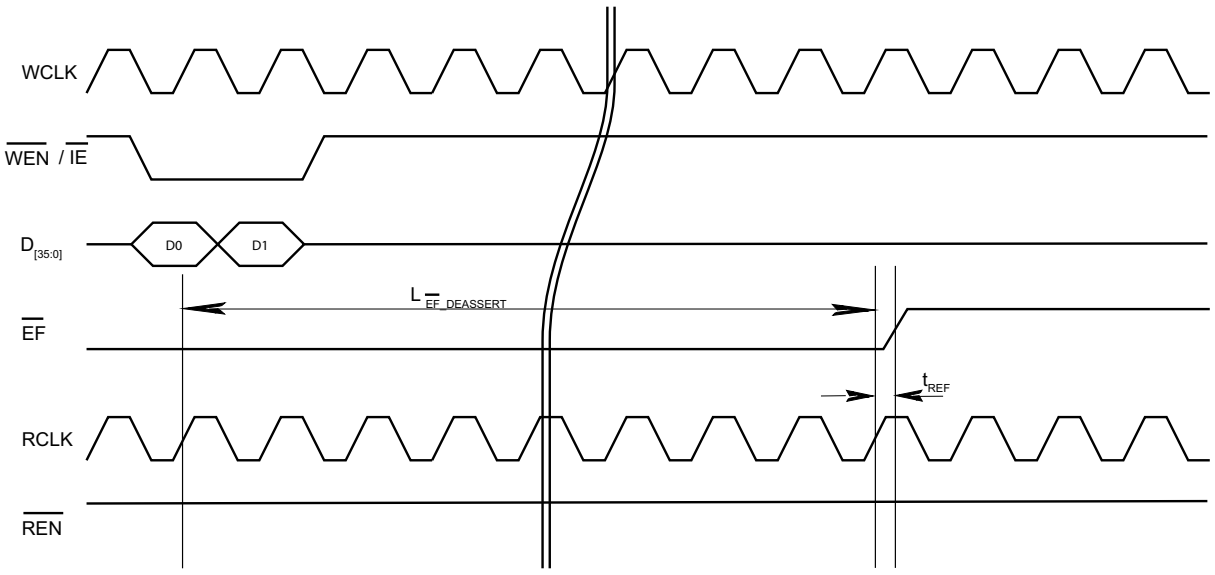


Figure 17. Empty Flag Deassertion



Switching Waveforms (continued)

Figure 18. Empty Flag Assertion

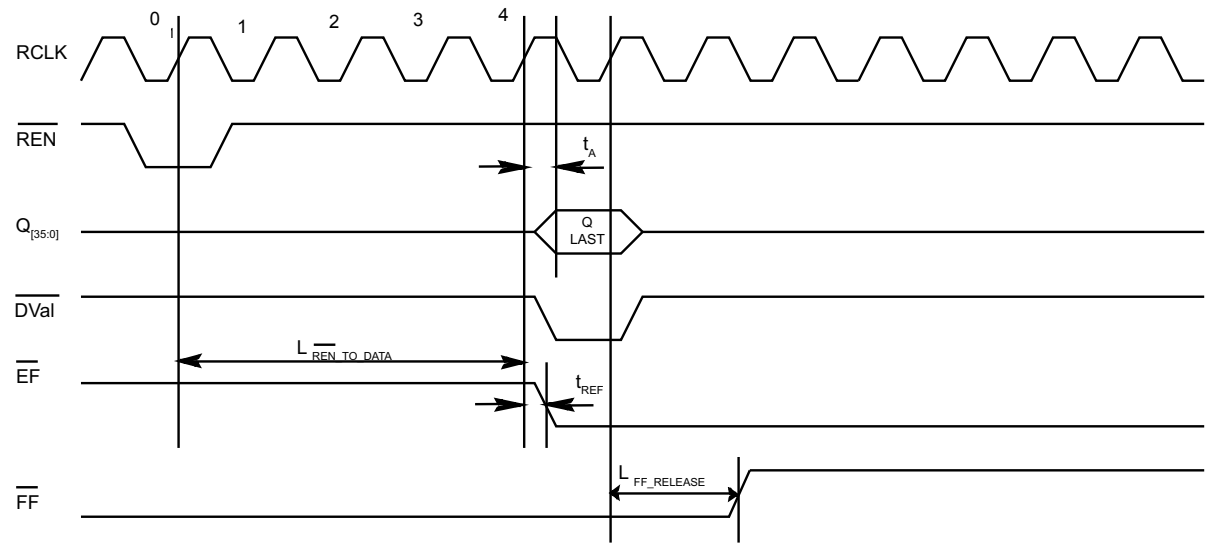
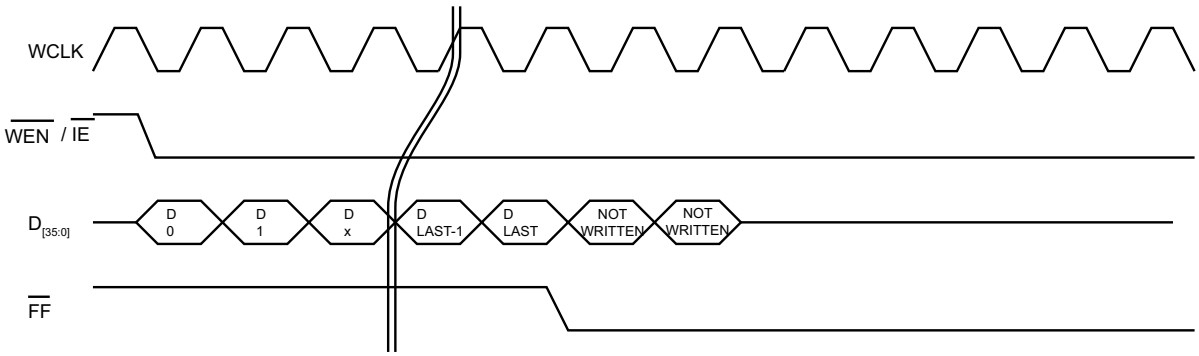


Figure 19. Full Flag Assertion



Switching Waveforms (continued)

Figure 20. Full Flag Deassertion

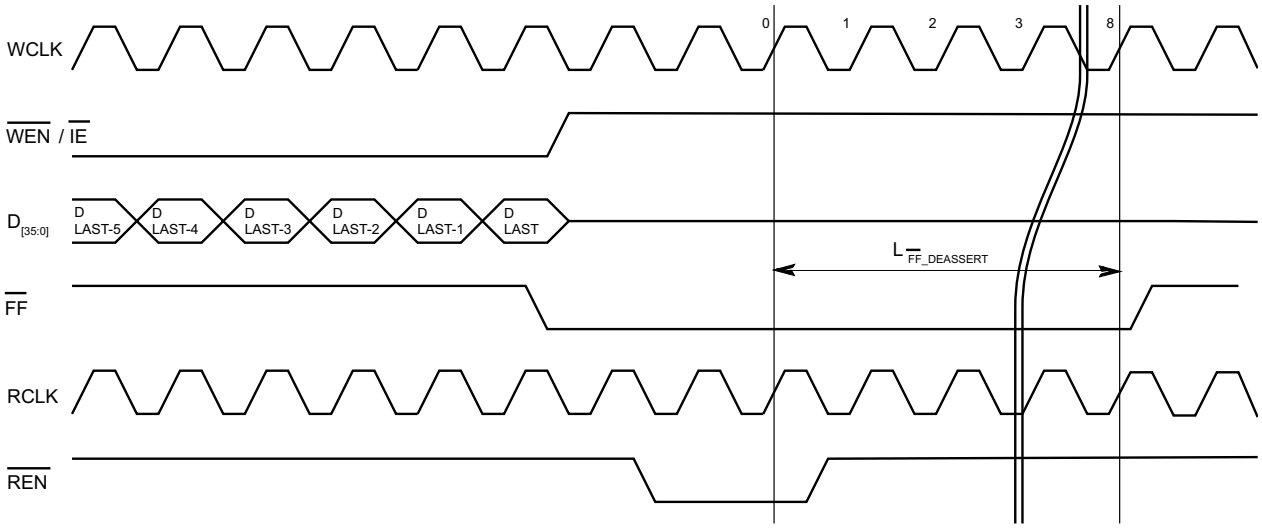
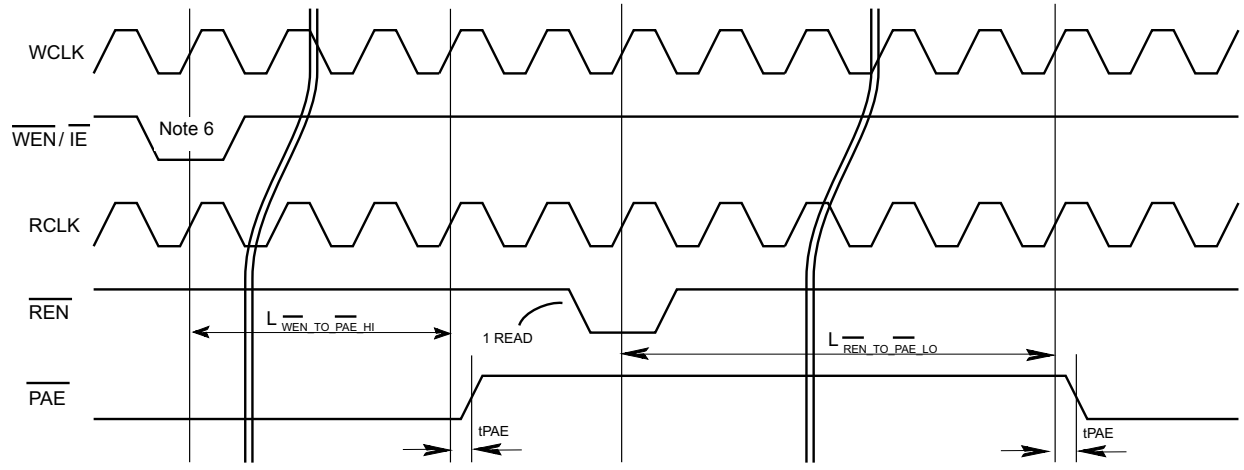


Figure 21. PAE Assertion and Deassertion



Note
6. Refer to Table 2 on page 8 and Latency Table on page 17 for the Programmable Flag boundaries.

Switching Waveforms (continued)

Figure 22. $\overline{PAF}$ Assertion and Deassertion

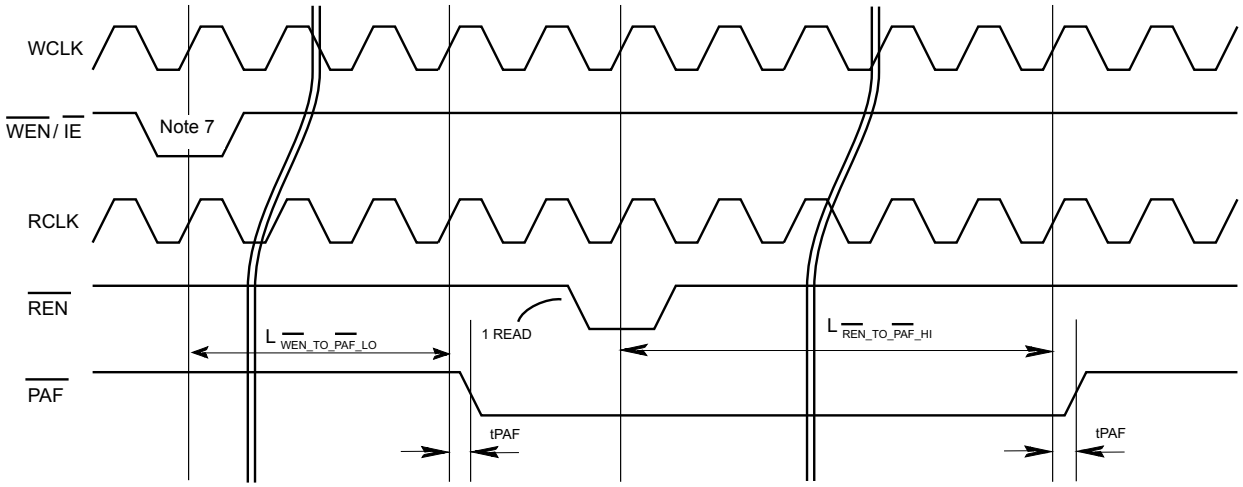
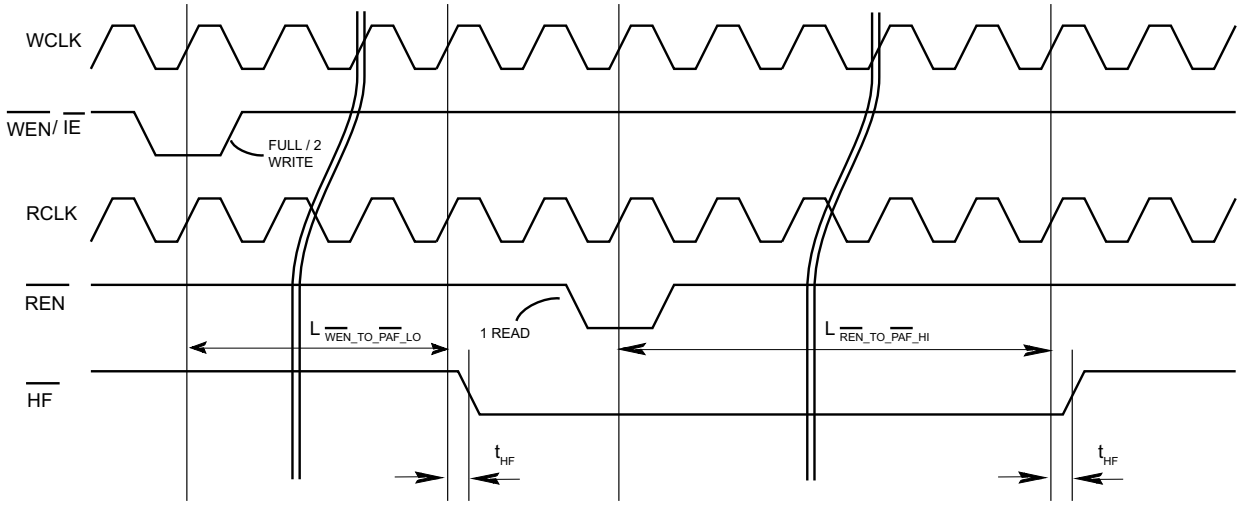


Figure 23. $\overline{HF}$ Assertion and Deassertion



Note
7. Refer to Table 2 on page 8 and Latency Table on page 17 for the Programmable Flag boundaries.

Switching Waveforms (continued)

Figure 24. Mark

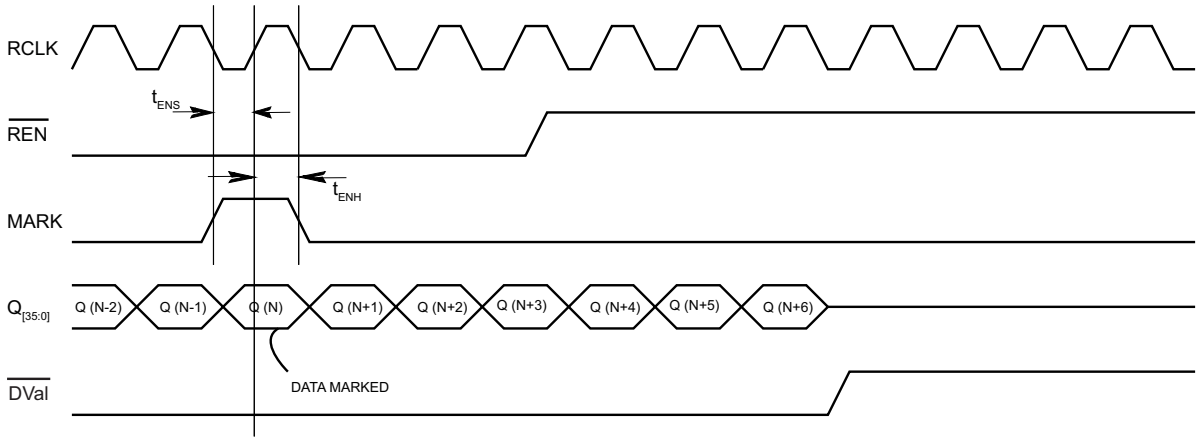
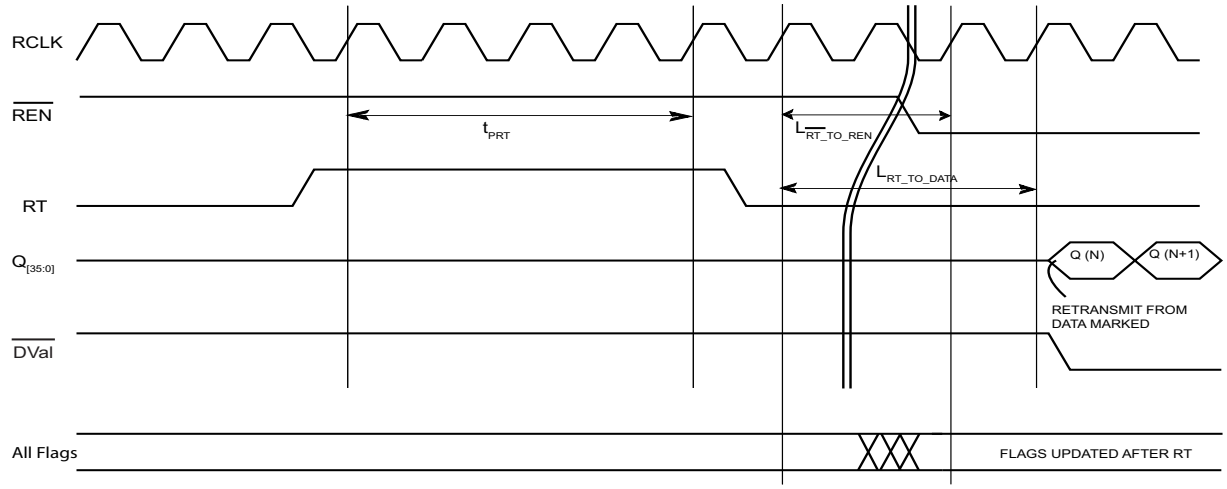


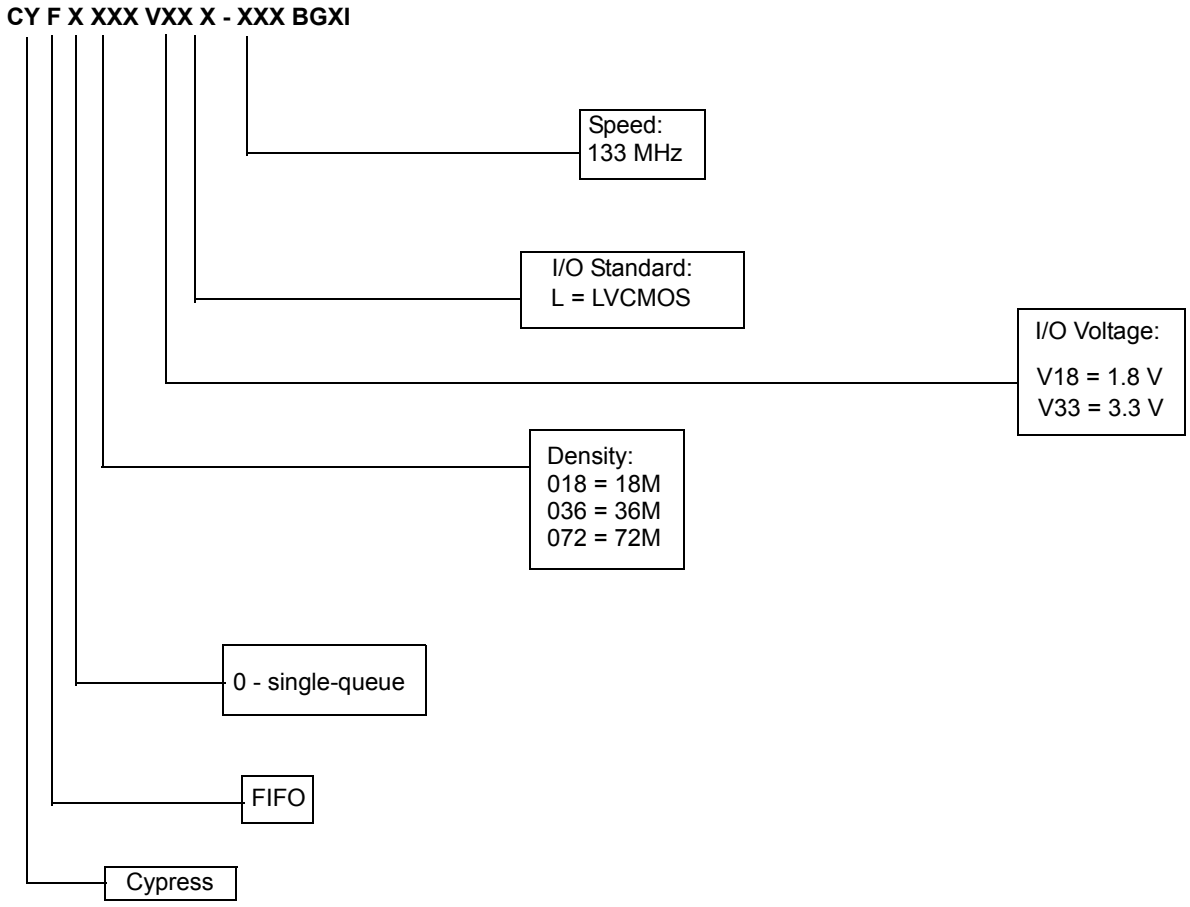
Figure 25. Retransmit



Ordering Information

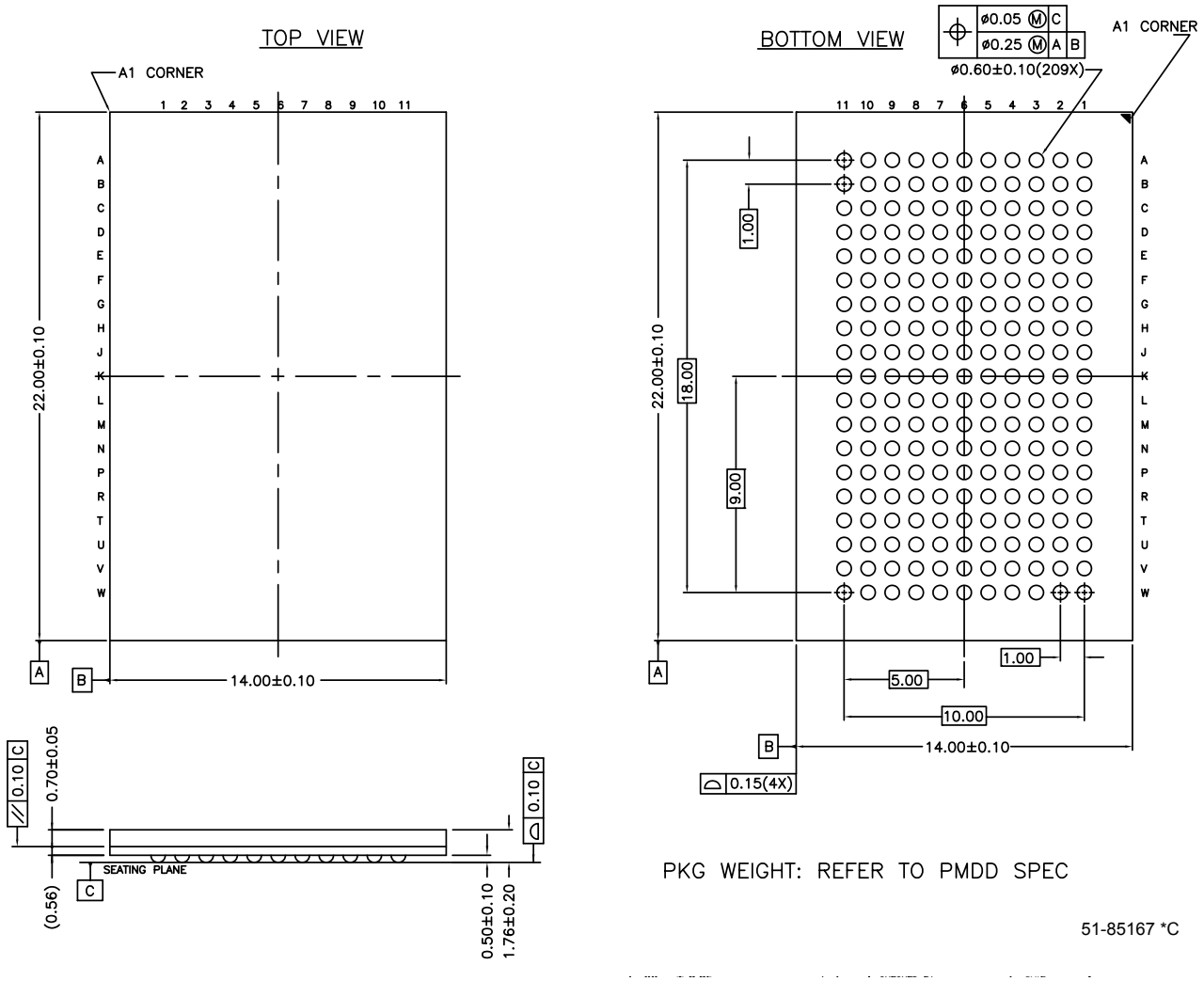
Speed (MHz)	Ordering Code	Package Diagram	Package Type	Operating Range
133	CYF0018V33L-133BGXI	51-85167	209-ball FBGA (14 × 22 × 1.76 mm)	Industrial
	CYF0036V33L-133BGXI			
	CYF0072V33L-133BGXI			
	CYF0018V18L-133BGXI			
	CYF0072V18L-133BGXI			

Ordering Code Definitions



Package Diagram

Figure 26. 209-ball FBGA (14 × 22 × 1.76 mm) BB209A Package Outline, 51-85167



Acronyms

Acronym	Description
$\overline{FF}$	Full Flag
FIFO	First In First Out
$\overline{HF}$	Half Full
$\overline{IE}$	Input Enable
I/O	Input/Output
FBGA	Fine-Pitch Ball Grid Array
JTAG	Joint Test Action Group
LSB	Least Significant Bit
LVCMOS	Low Voltage Complementary Metal Oxide Semiconductor
MB	Mailbox
$\overline{MRS}$	Master Reset
MSB	Most Significant Bit
$\overline{OE}$	Output Enable
$\overline{PAF}$	Programmable Almost-Full
$\overline{PAE}$	Programmable Almost-Empty
$\overline{PRS}$	Partial Reset
RCLK	Read Clock
$\overline{REN}$	Read Enable
RCLK	Read Clock
SCLK	Serial Clock
TCK	Test Clock
TDI	Test Data In
TDO	Test Data Out
TMS	Test Mode Select
WCLK	Write Clock
$\overline{WEN}$	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
mA	milliampere
mm	millimeter
ms	millisecond
ns	nanosecond
Ω	ohm
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CYF0018V/CYF0036V/CYF0072V, 18/36/72-Mbit Programmable FIFOs Document Number: 001-53687				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	2711566	VKN / PYRS	05/27/09	New data sheet.
*A	2725088	NXR	06/26/2009	Included pinout, AC and DC specs, timing diagrams and package diagram
*B	2839536	NXR	01/28/2010	Changed Balls B5, D5, F6, K1, K2, K4, K8 and U2 from NC to DNU, Balls C5, C7, G6, H6, J6, L6, M6, N6, T5, T7 from NC to VCC1, Balls K9, K10, K11 from NC to VCCIOR, Ball W9 from NC to Vref in pin configuration table Swapped Voltage range of V_{SS1} and V_{SS2} Updated I_{CC} spec Removed T_{SKEW} parameter Added Ordering Information table Added Part Numbering Nomenclature. Changed title to CYF0018V/CYF0036V/CYF0072V/CYFX144VXXX, 18/36/72-Mbit Programmable FIFOs.
*C	2884377	HKV	02/25/2010	Post to external web.
*D	2963225	AJU / HPV	06/28/2010	Changed frequency of operation from 250 MHz to 150 MHz Removed Depth Expansion feature and changed associated pin functionality Removed Independent Port size selectability feature Added Data Valid (DVal) signal feature Updated Logic Block Diagram to reflect above changes. Pinout changes: Balls V5, V8, A7, B7, D7, and C6 renamed DNU Ball U1 changed from RXO to DVal Ball V2 changed from WXO/HF to HF Ball A5, A6, B6 changed from WPORTSZ to PORTSZ Ball A9 changed from RT/FL to RT Renamed pwr as POWER, gnd as GND Added Table 4 Table 6 – LD changed to '1' for serial writes Updated Electrical Characteristics and I/O Characteristics Switching Characteristics Table: Renamed tPC as tPU Min frequency changed from 110MH to 24MHz Changed t_{CLKH} and t_{CLKL} to 3.15 ns Changed All setup and hold times to 3 ns Changed t_{RSF} to 50 ns Removed t_{RSR} Changed All clock-to-flag timing to min = 8 ns and max = 14 ns T_{PLL} changed to 6 ms Changed all OE-related parameters to 15 ns Scaled I_{CC} for reduced frequency Updated all waveforms Added the following table: "Word Size Selection". Added the sections JTAG Operation, and Latency Table Added Acronyms.
*E	2994379	AJU	07/26/2010	Updated Ordering Information
*F	3101023	SIVS	12/03/2010	Added supply-wise current consumption data in Electrical Characteristics. Changed initial latency L_{IN} from 34 to 26 and added initial latency L_{IN} for 110 MHz part in Latency Table. Added 110 MHz part information in JTAG Operation Added details for the 110 MHz part in Switching Characteristics. Added details for the 110 MHz part in Ordering Information.
*G	3129722	HKV	01/06/2011	Post to external web.

Document History Page (continued)

Document Title: CYF0018V/CYF0036V/CYF0072V, 18/36/72-Mbit Programmable FIFOs
Document Number: 001-53687

Revision	ECN	Orig. of Change	Submission Date	Description of Change
*H	3197271	SIVS	03/31/2011	Removed 144 Mbit parts from the data sheet Removed multi-queue information from data sheet Removed 2.5 V and 1.5 V options Removed HSTL I/II I/O standard Added clock ratio requirement between RCLK and WCLK Removed redundant Xs from part number to improve readability Removed tie to GND option on DNU pins in pin description Added information on Flag operations to add clarity Added explanation for flow-through mailbox operation Added details on active pins in various port sizes in Table 1. Added Configuration register write to normal operation latency details. Changed configuration register definitions and default values Changed number of unusable locations to four to eight Added JTAG related operation Added latch-up current parameter in maximum operating conditions. Removed 2.5 V and 1.5 V options from DC operating condition table 6. Removed 110 MHz part details and added Cpio parameter in table 7. Removed 2.5 V and 1.5 V options from Table 8. Added latency parameters in Table 9. changed V_{OL}(max) value of LVCMOS33 in table11 Removed 110 MHz part detail from switching characteristics Added timing waveform to improve clarity. Modified ordering information and definition.
*I	3388143	AJU	09/29/2011	Updated Pin Diagram for CYF0XXXVXXL [1] (Added Note 2 and referred the same note in DNU in ball U6). Updated Programming Flag Offsets and Configuration Registers (Updated Table 4 (WCLK column in first row)). Updated Recommended DC Operating Conditions (Added Note 4 and referred the same note in Parameter column). Updated Latency Table (Changed Details for the parameters $L_{\overline{WEN}_TO_\overline{PAE}_HI}$ and $L_{\overline{REN}_TO_\overline{PAE}_LO}$). Updated Switching Waveforms (Removed the clock cycle numbers in Figure 13, Figure 14, Figure 18, and Figure 20). Updated Package Diagram. Updated in new template.
*J	3652368	ADMU	08/16/2012	Updated Pin Diagram for CYF0XXXVXXL [1] (Updated Figure 1 on page 4 (W9 ball marked as DNU)). Added Figure 6 (Test Load Conditions). Updated Switching Characteristics (Changed minimum values of t_{S_JTAG}, t_{H_JTAG} parameters from 5 ns to 8 ns, changed maximum value of t_{CO_JTAG} parameter from 10 ns to 20 ns).
*K	3735896	ADMU	09/07/2012	Updated package diagram 51-85167 to *C Updated “Output current into outputs (LOW)” parameter under Maximum Ratings section from 20 mA to 24 mA.

Document History Page (continued)

Document Title: CYF0018V/CYF0036V/CYF0072V, 18/36/72-Mbit Programmable FIFOs
Document Number: 001-53687

Revision	ECN	Orig. of Change	Submission Date	Description of Change
*L	3940217	ADMU	03/22/2013	Updated Features. Updated Functional Description. Updated Logic Block Diagram. Updated Pin Diagram for CYF0XXXVXXL [1]: Added Note 1 and referred the same note in Figure 1. Updated Pin Definitions. Updated Architecture: Updated Reset Logic, Data Valid Signal (DVal), Flag Operation, Retransmit from Mark Operation, Programming Flag Offsets and Configuration Registers, Read/Write Clock Requirements. Added Table 2. Updated Latency Table. Updated Switching Waveforms: Updated Figure 13, Figure 14, Figure 18, Figure 20, Figure 21, Figure 22, Figure 23, Figure 25. Added Note 6 and referred the same note in $\overline{WEN}$ / $\overline{IE}$ in Figure 21. Added Note 7 and referred the same note in $\overline{WEN}$ / $\overline{IE}$ in Figure 22. Updated Ordering Information (Updated part numbers).
*M	3997615	ADMU	05/11/2013	Added Errata.
*N	4078255	ADMU	07/26/2013	Added Errata footnotes (Note 4, 7, 8, 11). Updated Architecture: Updated Retransmit from Mark Operation: Added Note 4 and referred the same note in 2nd paragraph and last paragraph. Updated Latency Table: Added Note 7 and referred the same note in "$L_{\overline{FF}_RELEASE}$" parameter. Updated Switching Waveforms: Added Note 8 and referred the same note in "$L_{\overline{FF}_RELEASE}$" in Figure 18. Added Note 11 and referred the same note in "All Flags" and "FLAGS UPDATED AFTER RT" in Figure 25. Updated in new template.
*O	4202562	SMCH	11/27/2013	Updated Errata.
*P	4580426	SMCH	11/25/2014	Added related documentation hyperlink in page 1.
*Q	5326858	SMCH	06/28/2016	Updated Logic Block Diagram. Updated Pin Diagram for CYF0XXXVXXL [1]. Updated Pin Definitions. Updated JTAG Operation. Removed Errata section. Updated CY Logo and Sales Disclaimer.
*R	5379263	DEVM	07/29/2016	Updated Pin Diagram for CYF0XXXVXXL [1]: Replaced TRST\ with DNU.
*S	5963236	AESATMP8	11/10/2017	Updated logo and Copyright.

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