8-Mbit (1M words × 8 bit) static RAM with error-correcting code (ECC)

Features

- High speed
  - t_{AA} = 10 ns
- Embedded error-correcting code (ECC) for single-bit error correction
- Low active and standby currents
  - I_{CC} = 90 mA typical at 100 MHz
  - I_{SB2} = 20 mA typical
- Operating voltage range: 2.2 V to 3.6 V
- 1.0-V data retention
- Transistor-transistor logic (TTL) compatible inputs and outputs
- ERR pin to indicate 1-bit error detection and correction
- Available in Pb-free 44-pin TSOP II package

Functional description

The CY7C1059H and CY7C1059HE are dual chip enable high-performance CMOS fast static RAM devices with embedded ECC. The CY7C1059H device is available in standard pin configurations. The CY7C1059HE device includes a single bit error indication pin (ERR) that signals the host processor in the case of an ECC error-detection and correction event.

To write to the device, take chip enables ($\overline{CE}_1$ LOW and CE_2 HIGH) and write enable ($\overline{WE}$) input LOW. Data on the eight I/O pins (I/O_0 through I/O_7) is then written into the location specified on the address pins (A_0 through A_{20}).

To read from the device, take chip enables ($\overline{CE}_1$ LOW and CE_2 HIGH) and output enable ($\overline{OE}$) LOW while forcing the write enable ($\overline{WE}$) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins. See **Truth table – CY7C1059H/CY7C1059HE on page 18** for a complete description of read and write modes. The input and output pins (I/O_0 through I/O_7) are placed in a high impedance state when the device is deselected ($\overline{CE}_1$ HIGH or CE_2 LOW), the outputs are disabled ($\overline{OE}$ HIGH), or during a write operation ($\overline{CE}_1$ LOW, CE_2 HIGH, and $\overline{WE}$ LOW).

On CY7C1059HE devices, the detection and correction of a single-bit error in the accessed location is indicated by the assertion of the ERR output (ERR = High) [1].

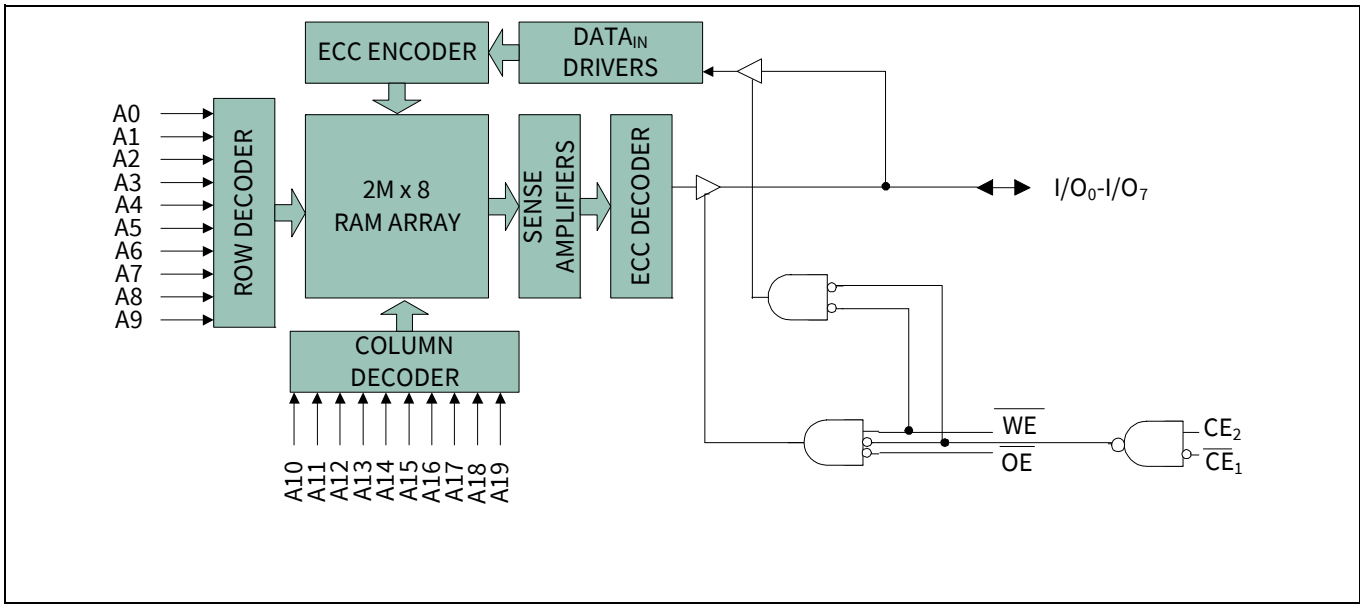
All I/Os (I/O_0 through I/O_7) are placed in a high impedance state when the device is deselected ($\overline{CE}_1$ HIGH or CE_2 LOW), and control signals are de-asserted ($\overline{CE}_1$ / CE_2, $\overline{OE}$, $\overline{WE}$). CY7C1059H and CY7C1059HE devices are available in a 44-pin TSOP II package with center power and ground (revolutionary) pinout package.

Note

1. Automatic write back on error detection feature is not supported in this device.

Logic block diagram – CY7C1059H

Logic block diagram – CY7C1059H



Logic block diagram – CY7C1059HE

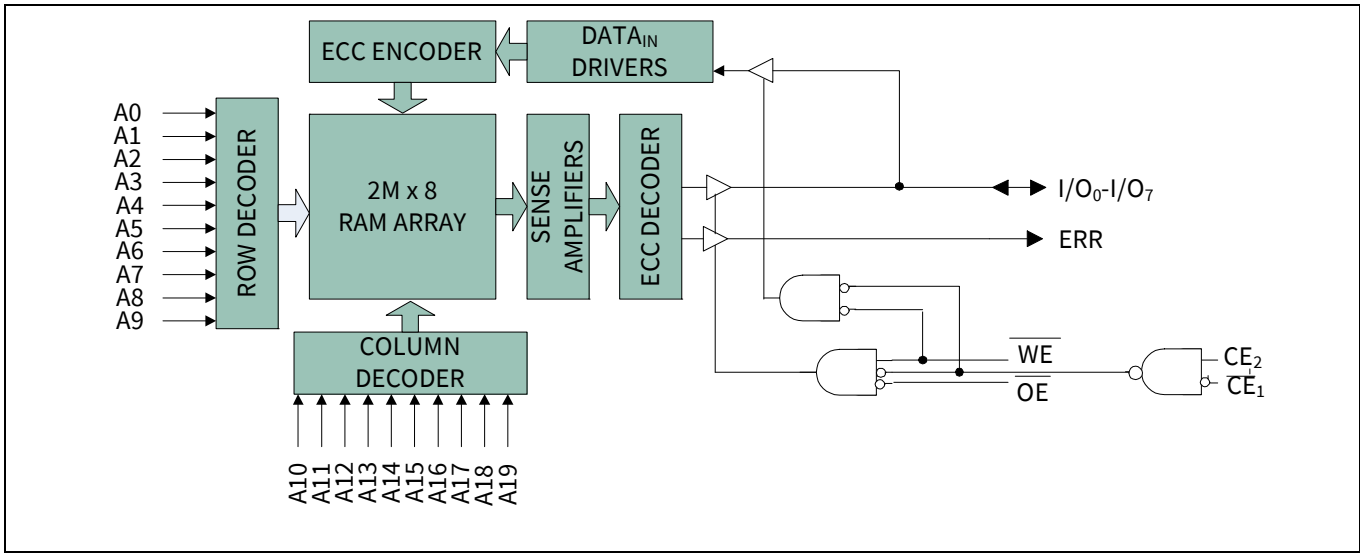


Table of contents

1 Pin configurations

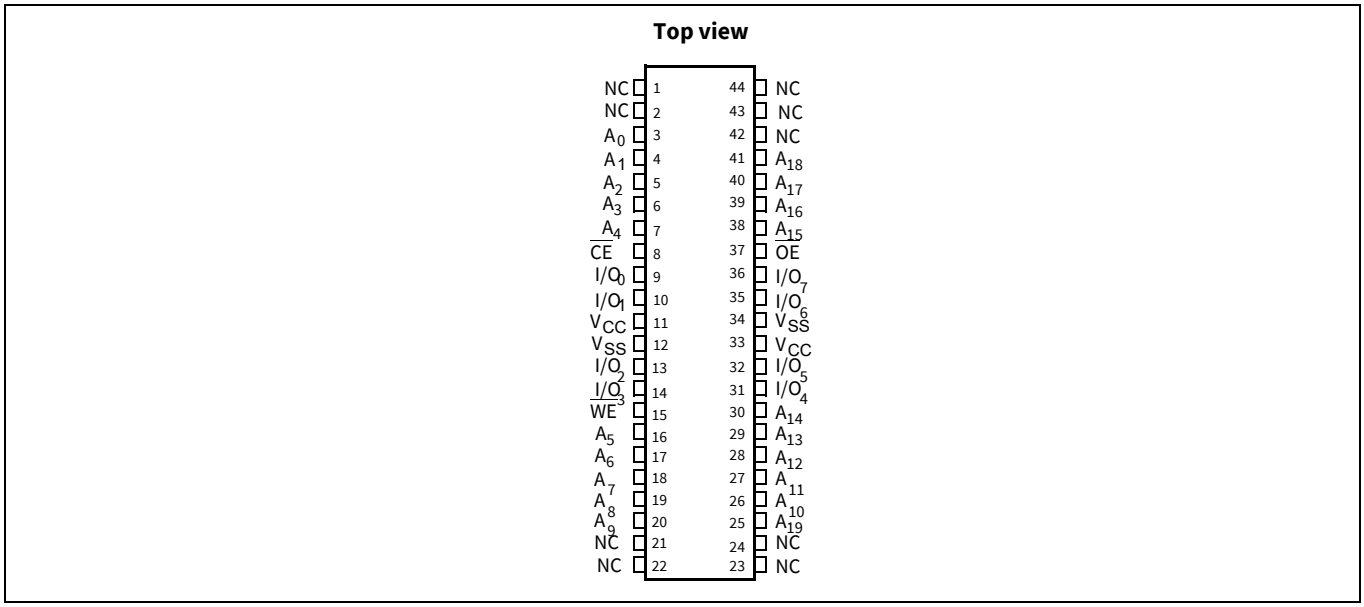


Figure 1 44-pin TSOP II[2]

Note
2. NC pins are not connected on the die.

2 Product portfolio

Table 1 Product portfolio

Product	Features and options (see the "Pin configurations" on page 4 section)	Range	V_{CC} range (V)	Speed (ns)	Power dissipation			
					Operating I_{CC}, (mA) f = f_{max}		Standby, I_{SB2} (mA)	
					Typ [3]	Max	Typ [3]	Max
CY7C1059H30	Dual-chip enable	Industrial	2.2 V–3.6 V	10	90	110	20	30
CY7C1059HE30	Dual-chip enable and ERR output		2.2 V–3.6 V	10	90	110	20	30

Note

3. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = 1.8 V (for V_{CC} range of 1.65 V–2.2 V), V_{CC} = 3 V (for V_{CC} range of 2.2 V–3.6 V), and V_{CC} = 5 V (for V_{CC} range of 4.5 V–5.5 V), T_A = 25°C.

3 Maximum ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature ..... –65°C to +150°C

Ambient temperature with power applied ..... –55°C to +125°C

Supply voltage on V_{CC} relative to GND ..... –0.5 V to +6.0 V

DC voltage applied to outputs in high Z state [4] ..... –0.5 V to V_{CC} + 0.5 V

DC input voltage [4] ..... –0.5 V to V_{CC} + 0.5 V

Current into outputs (LOW) ..... 20 mA

Static discharge voltage (MIL-STD-883, method 3015) ..... >2001 V

Latch up current ..... > 140 mA

Note

4. $V_{IL(min)}$ = –2.0 V and $V_{IH(max)}$ = V_{CC} + 2 V for pulse durations of less than 20 ns.

4 Operating range

Table 2 Operating range

Grade	Ambient temperature	V_{CC}
Industrial	–40°C to +85°C	2.2 V to 3.6 V

5 DC electrical characteristics

Table 3 DC electrical characteristics

Over the operating range of –40°C to 85°C

Parameter	Description		Test conditions		10 ns			Unit
					Min	Typ [6]	Max	
V_{OH}	Output HIGH voltage	2.2 V to 2.7 V	V_{CC} = Min, I_{OH} = –1.0 mA		2.0	–	–	V
		2.7 V to 3.0 V	V_{CC} = Min, I_{OH} = –4.0 mA		2.2	–	–	
		3.0 V to 3.6 V	V_{CC} = Min, I_{OH} = –4.0 mA		2.4	–	–	
V_{OL}	Output LOW voltage	2.2 V to 2.7 V	V_{CC} = Min, I_{OL} = 2 mA		–	–	0.4	
		2.7 V to 3.6 V	V_{CC} = Min, I_{OL} = 8 mA		–	–	0.4	
V_{IH}	Input HIGH voltage	2.2 V to 2.7 V	–		2.0	–	V_{CC} + 0.3	
		2.7 V to 3.6 V	–		2.0	–	V_{CC} + 0.3	
V_{IL}	Input LOW voltage [5]	2.2 V to 2.7 V	–		–0.3	–	0.6	
		2.7 V to 3.6 V	–		–0.3	–	0.8	
I_{IX}	Input leakage current		GND ≤ V_{IN} ≤ V_{CC}		–1.0	–	+1.0	µA
I_{OZ}	Output leakage current		GND ≤ V_{OUT} ≤ V_{CC}, output disabled		–1.0	–	+1.0	
I_{CC}	Operating supply current		V_{CC} = Max, I_{OUT} = 0 mA, CMOS levels	f = 100 MHz	–	90.0	110.0	mA
				f = 66.7 MHz	–	70.0	80.0	
I_{SB1}	Automatic CE power down current – TTL inputs		Max V_{CC}, $\overline{CE}$ ≥ V_{IH} [7], V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}		–	–	40.0	
I_{SB2}	Automatic CE power down current – CMOS inputs		Max V_{CC}, $\overline{CE}$ ≥ V_{CC} – 0.2 V [7], V_{IN} ≥ V_{CC} – 0.2 V or V_{IN} ≤ 0.2 V, f = 0		–	20.0 [6]	30.0	

Notes

5. $V_{IL(min)}$ = –2.0 V and $V_{IH(max)}$ = V_{CC} + 2 V for pulse durations of less than 20 ns.
6. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = 3 V (for V_{CC} range of 2.2 V–3.6 V) T_A = 25°C.
7. For all dual chip enable devices, $\overline{CE}$ is the logical combination of $\overline{CE}_1$ and CE_2. When $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW; when $\overline{CE}_1$ is HIGH or CE_2 is LOW, $\overline{CE}$ is HIGH.

6 Capacitance

Table 4 Capacitance

Parameter [8]	Description	Test conditions	44-pin TSOP II	Unit
C_{IN}	Input capacitance	$T_A = 25°C, f = 1\ MHz, V_{CC} = V_{CC(typ)}$	10	pF
C_{OUT}	I/O capacitance		10	

Note

8. Tested initially and after any design or process changes that may affect these parameters.

7 Thermal resistance

Table 5 Thermal resistance

Parameter [9]	Description	Test conditions	44-pin TSOP II	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	66.93	°C/W
Θ_{JC}	Thermal resistance (junction to case)		13.09	

Note

9. Tested initially and after any design or process changes that may affect these parameters.

8 AC test loads and waveforms

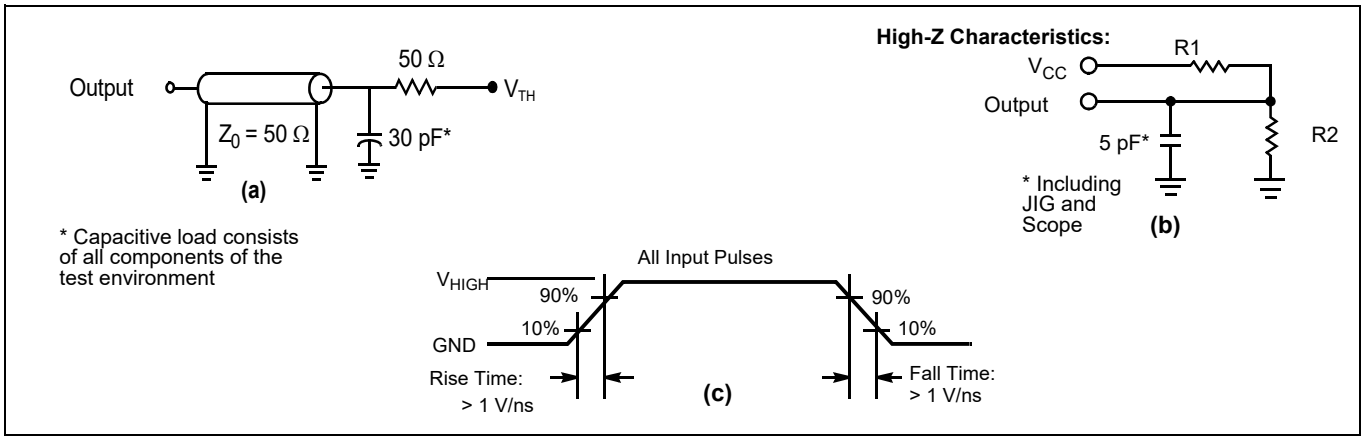


Figure 2 AC test loads and waveforms[10]

Table 6 AC test loads and waveforms

Parameters	1.8 V	3.0 V	5.0 V	Unit
R1	1667	317	317	Ω
R2	1538	351	351	Ω
V_{TH}	0.9	1.5	1.5	V
V_{HIGH}	1.8	3	3	V

Note

10. Full device AC operation assumes a 100-µs ramp time from 0 to V_{CC}(min) and 100-µs wait time after V_{CC} stabilization.

9 Data retention

9.1 Data retention characteristics

Table 7 Data retention characteristics

Over the operating range of –40°C to 85°C

Parameter	Description	Conditions	Min	Max	Unit
V_{DR}	V_{CC} for data retention	–	1.0	–	V
I_{CCDR}	Data retention current	$V_{CC}=V_{DR}$, $\overline{CE} \geq V_{CC} - 0.2$ V [11], $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V	–	30.0	mA
t_{CDR} [12]	Chip deselect to data retention time	–	0	–	ns
t_R [12, 13]	Operation recovery time	$V_{CC} \geq 2.2$ V	10.0	–	
		$V_{CC} < 2.2$ V	15.0	–	

9.2 Data retention waveform

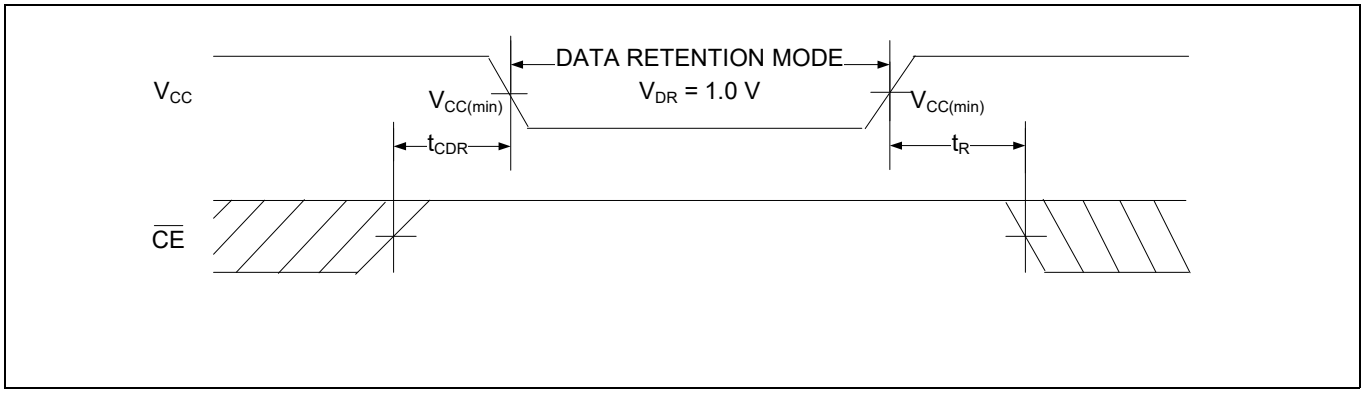


Figure 3 Data retention waveform[11]

Notes

11. For all dual chip enable devices, $\overline{CE}$ is the logical combination of $\overline{CE}_1$ and CE_2. When $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW; when $\overline{CE}_1$ is HIGH or CE_2 is LOW, $\overline{CE}$ is HIGH.
12. This parameter is guaranteed by design and is not tested.
13. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min.)} \geq 100$ µs or stable at $V_{CC(min.)} \geq 100$ µs.

10 AC switching characteristics

Table 8 AC switching characteristics

Over the operating range of –40°C to 85°C

Parameter [14]	Description	10 ns		Unit
		Min	Max	
Read cycle				
t_{POWER}	V_{CC} stable to first access [15, 16]	100.0	–	µs
t_{RC}	Read cycle time	10.0	–	ns
t_{AA}	Address to data / ERR valid	–	10.0	
t_{OHA}	Data / ERR hold from address change	3.0	–	
t_{ACE}	$\overline{CE}$ LOW to data / ERR valid [17]	–	10.0	
t_{DOE}	$\overline{OE}$ LOW to data / ERR valid	–	5.0	
t_{LZOE}	$\overline{OE}$ LOW to low Z [18, 19, 20]	0	–	
t_{HZOE}	$\overline{OE}$ HIGH to high Z [18, 19, 20]	–	5.0	
t_{LZCE}	$\overline{CE}$ LOW to low Z [17, 18, 19, 20]	3.0	–	
t_{HZCE}	$\overline{CE}$ HIGH to high Z [17, 18, 19, 20]	–	5.0	
t_{PU}	$\overline{CE}$ LOW to power-up [16, 17]	0	–	
t_{PD}	$\overline{CE}$ HIGH to power-down [16, 17]	–	10.0	
Write cycle [21, 22]				

Notes

14. Test conditions assume signal transition time (rise/fall) of 3 ns or less, timing reference levels of 1.5 V (for $V_{CC} \geq 3$ V) and $V_{CC}/2$ (for $V_{CC} < 3$ V), and input pulse levels of 0 to 3 V (for $V_{CC} \geq 3$ V) and 0 to V_{CC} (for $V_{CC} < 3$ V). Test conditions for the read cycle use output loading shown in part (a) of **Figure 2 on page 11**, unless specified otherwise.
15. t_{POWER} gives minimum amount of time that the power supply is at stable V_{CC} until first memory access is performed.
16. These parameters are guaranteed by design and are not tested.
17. For all dual chip enable devices, $\overline{CE}$ is the logical combination of $\overline{CE}_1$ and CE_2. When $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW; when $\overline{CE}_1$ is HIGH or CE_2 is LOW, $\overline{CE}$ is HIGH.
18. t_{HZOE}, t_{HZCE}, t_{HZWE}, t_{LZOE}, t_{LZCE}, and t_{LZWE} are specified with a load capacitance of 5 pF as in (b) of **Figure 2 on page 11**. Transition is measured ±200 mV from steady state voltage.
19. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZBE} is less than t_{LZBE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any device.
20. Tested initially and after any design or process changes that may affect these parameters.
21. The internal write time of the memory is defined by the overlap of $\overline{WE} = V_{IL}$, $\overline{CE} = V_{IL}$. These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
22. The minimum write pulse width for write cycle No.2 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) should be sum of t_{HZWE} and t_{SD}.

Table 8 AC switching characteristics *(continued)*

Over the operating range of –40°C to 85°C

Parameter [14]	Description	10 ns		Unit
		Min	Max	
t_{WC}	Write cycle time	10.0	–	ns
t_{SCE}	$\overline{CE}$ LOW to write end [17]	7.0	–	
t_{AW}	Address setup to write end	7.0	–	
t_{HA}	Address hold from write end	0	–	
t_{SA}	Address setup to write start	0	–	
t_{PWE}	$\overline{WE}$ pulse width	7.0	–	
t_{SD}	Data setup to write end	5.0	–	
t_{HD}	Data hold from write end	0	–	
t_{LZWE}	$\overline{WE}$ HIGH to low Z [18, 19, 20]	3.0	–	
t_{HZWE}	$\overline{WE}$ LOW to high Z [18, 19, 20]	–	5.0	

Notes

14. Test conditions assume signal transition time (rise/fall) of 3 ns or less, timing reference levels of 1.5 V (for $V_{CC} \geq 3$ V) and $V_{CC}/2$ (for $V_{CC} < 3$ V), and input pulse levels of 0 to 3 V (for $V_{CC} \geq 3$ V) and 0 to V_{CC} (for $V_{CC} < 3$ V). Test conditions for the read cycle use output loading shown in part (a) of **Figure 2 on page 11**, unless specified otherwise.
15. t_{POWER} gives minimum amount of time that the power supply is at stable V_{CC} until first memory access is performed.
16. These parameters are guaranteed by design and are not tested.
17. For all dual chip enable devices, $\overline{CE}$ is the logical combination of $\overline{CE_1}$ and CE_2. When $\overline{CE_1}$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW; when $\overline{CE_1}$ is HIGH or CE_2 is LOW, $\overline{CE}$ is HIGH.
18. t_{HZOE}, t_{HZCE}, t_{HZWE}, t_{LZOE}, t_{LZCE}, and t_{LZWE} are specified with a load capacitance of 5 pF as in (b) of **Figure 2 on page 11**. Transition is measured ±200 mV from steady state voltage.
19. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZBE} is less than t_{LZBE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any device.
20. Tested initially and after any design or process changes that may affect these parameters.
21. The internal write time of the memory is defined by the overlap of $\overline{WE} = V_{IL}$, $\overline{CE} = V_{IL}$. These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
22. The minimum write pulse width for write cycle No.2 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) should be sum of t_{HZWE} and t_{SD}.

11 Switching waveforms

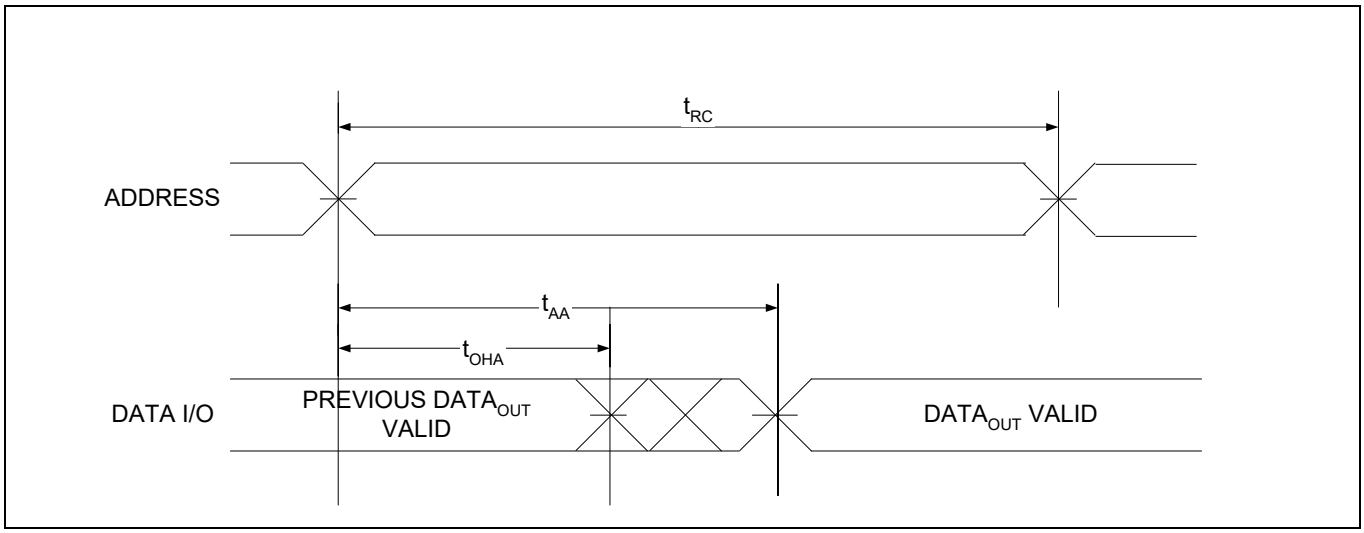


Figure 4 Read cycle No. 1 of CY7C1059H (address transition controlled)[23, 24]

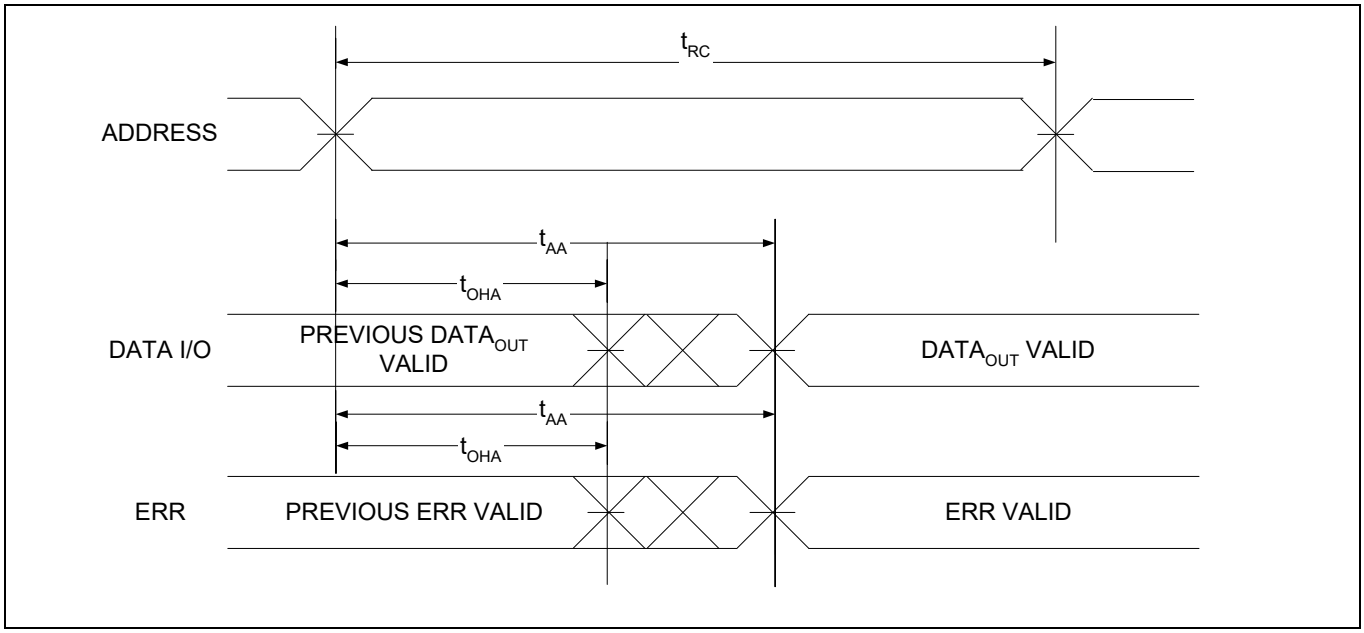


Figure 5 Read cycle No. 2 of CY7C1059HE (address transition controlled)[23, 24]

Notes
23. The device is continuously selected, $\overline{OE} = V_{IL}$, $\overline{CE} = V_{IL}$.
24. $\overline{WE}$ is HIGH for read cycle.

Switching waveforms

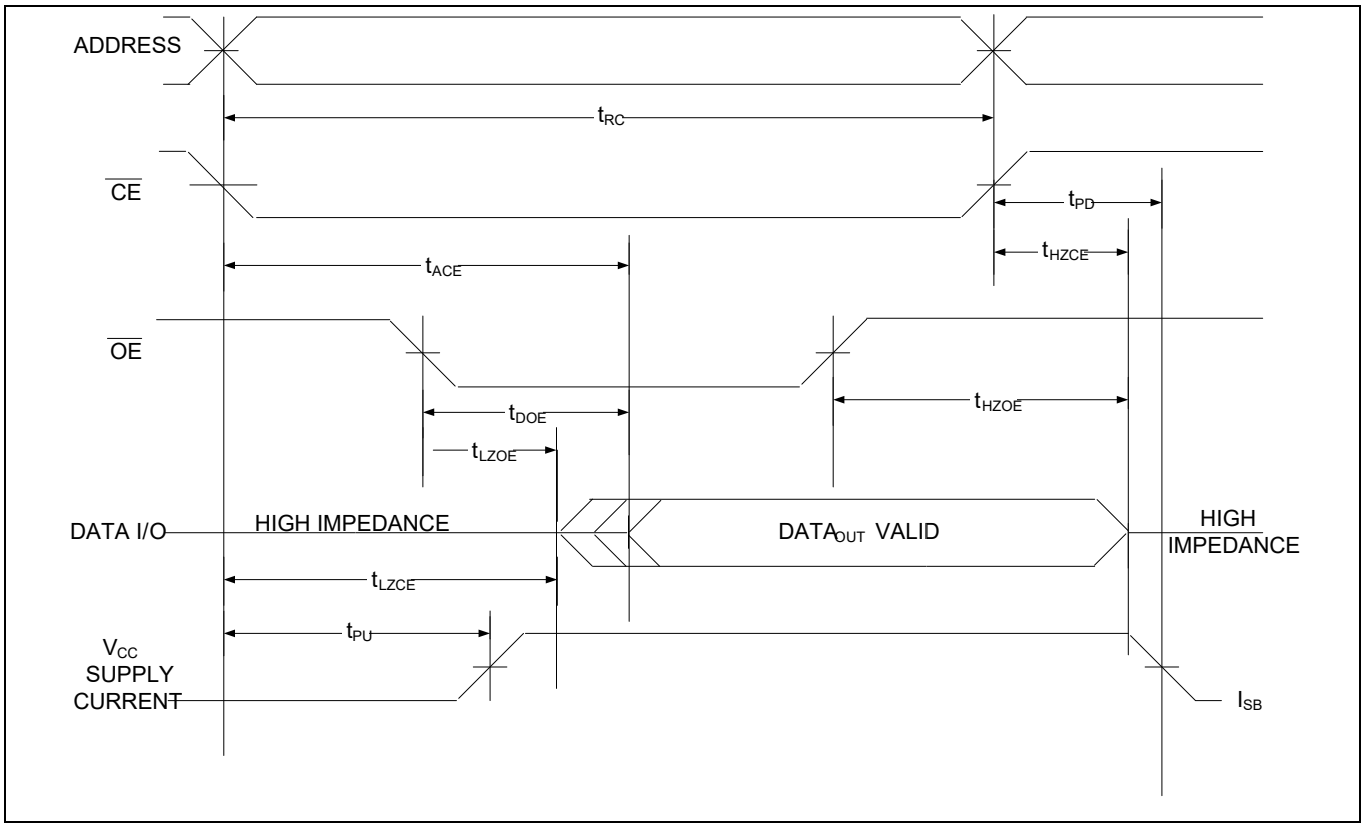


Figure 6 Read cycle No. 3 ($\overline{OE}$ controlled, $\overline{WE}$ HIGH) [25, 26, 27]

Notes

25. For all dual chip enable devices, $\overline{CE}$ is the logical combination of $\overline{CE}_1$ and CE_2. When $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW; when $\overline{CE}_1$ is HIGH or CE_2 is LOW, $\overline{CE}$ is HIGH.
26. $\overline{WE}$ is HIGH for read cycle.
27. Address valid prior to or coincident with $\overline{CE}$ LOW transition.

Switching waveforms

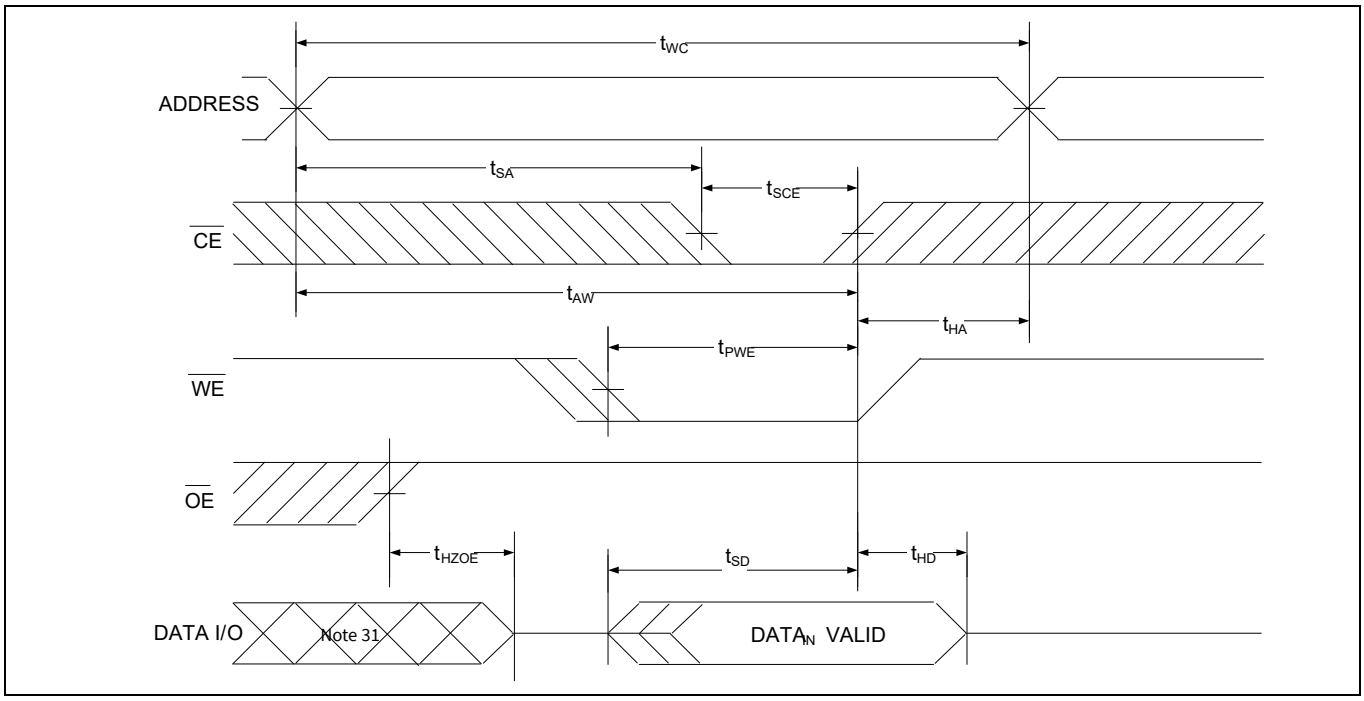


Figure 7 Write cycle No. 1 ($\overline{CE}$ Controlled) [28, 29, 30]

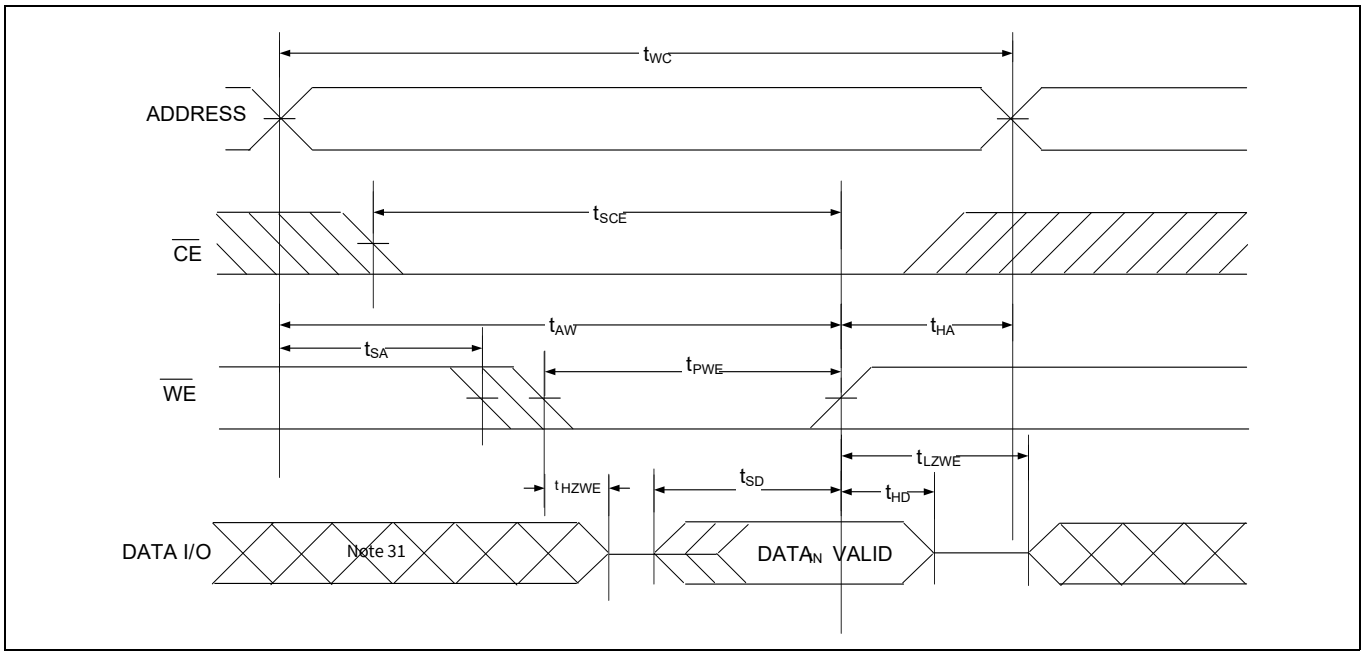


Figure 8 Write Cycle No. 2 ($\overline{WE}$ Controlled, $\overline{OE}$ Low) [28, 29, 30, 32]

Notes

28. For all dual chip enable devices, $\overline{CE}$ is the logical combination of $\overline{CE}_1$ and CE_2. When $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW; when $\overline{CE}_1$ is HIGH or CE_2 is LOW, $\overline{CE}$ is HIGH.
29. The internal write time of the memory is defined by the overlap of $\overline{WE} = V_{IL}$, $\overline{CE} = V_{IL}$. These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
30. Data I/O is in high impedance state if $\overline{CE} = V_{IH}$, or $\overline{OE} = V_{IH}$.
31. During this time I/O are in output put state. Do not apply input signals.
32. The minimum write cycle width should be sum of t_{HZWE} and t_{SD}.

12 Truth table – CY7C1059H/CY7C1059HE

Table 9 Truth table – CY7C1059H/CY7C1059HE

$\overline{CE_1}$	CE_2	$\overline{OE}$	$\overline{WE}$	I/O_0–I/O_7	Mode	Power
H	X [33]	X [33]	X [33]	High Z	Power-down	Standby (I_{SB})
X [33]	L	X [33]	X [33]	High Z	Power-down	Standby (I_{SB})
L	H	L	H	Data out	Read all bits	Active (I_{CC})
L	H	X [33]	L	Data in	Write all bits	Active (I_{CC})
L	H	H	H	High Z	Selected, outputs disabled	Active (I_{CC})

Note
33.The input voltage levels on these pins should be either at V_{IH} or V_{IL}.

13 ERR output- CY7C1059HE

Table 10 ERR output – CY7C1059HE

Output [34]	Mode
0	Read operation, no single bit error in the stored data.
1	Read operation, single bit error detected and corrected.
High Z	Device deselected or outputs disabled or write operation

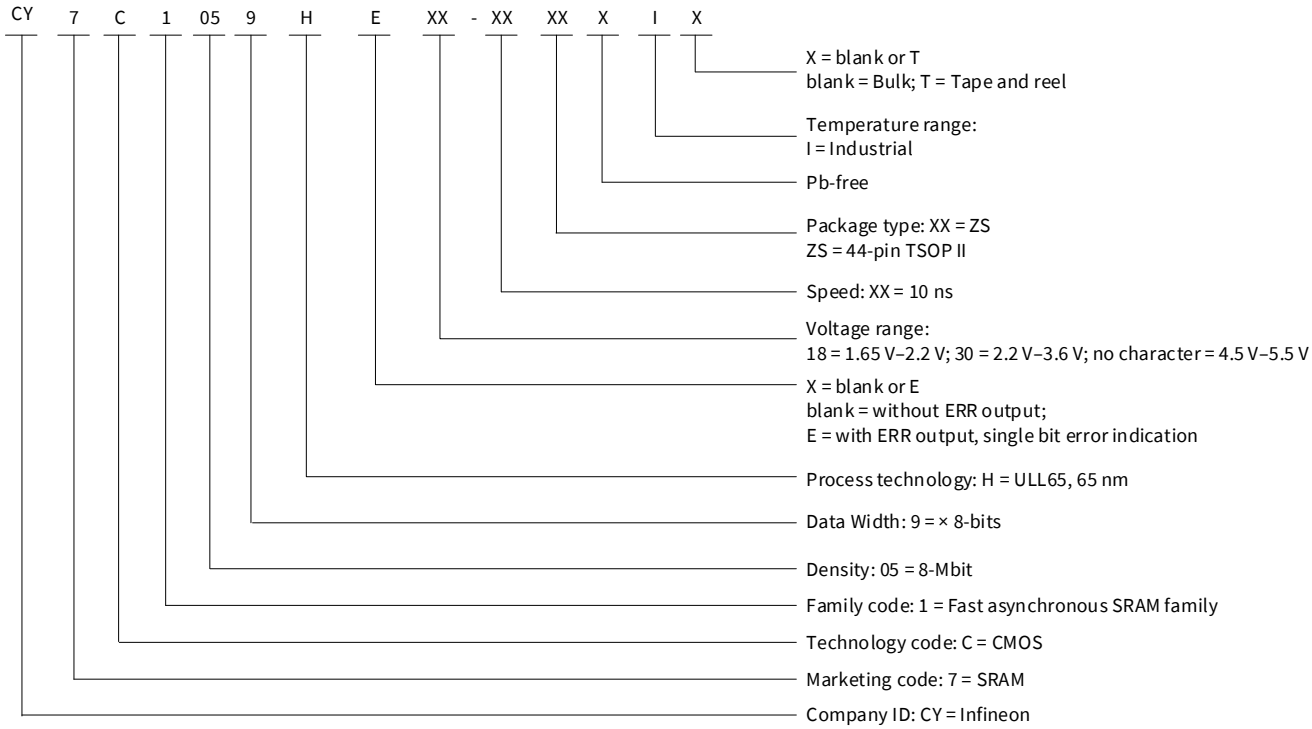
Note
34.ERR is an Output pin.If not used, this pin should be left floating.

14 Ordering information

Table 11 Ordering information

Speed (ns)	Voltage range	Ordering code	Package diagram	Package type (All Pb-free)	ERR pin / ball	Operating range
10	2.2 V–3.6 V	CY7C1059H30-10ZSXI	51-85087	44-pin TSOP II	No	Industrial

14.1 Ordering code definitions



15 Package diagram

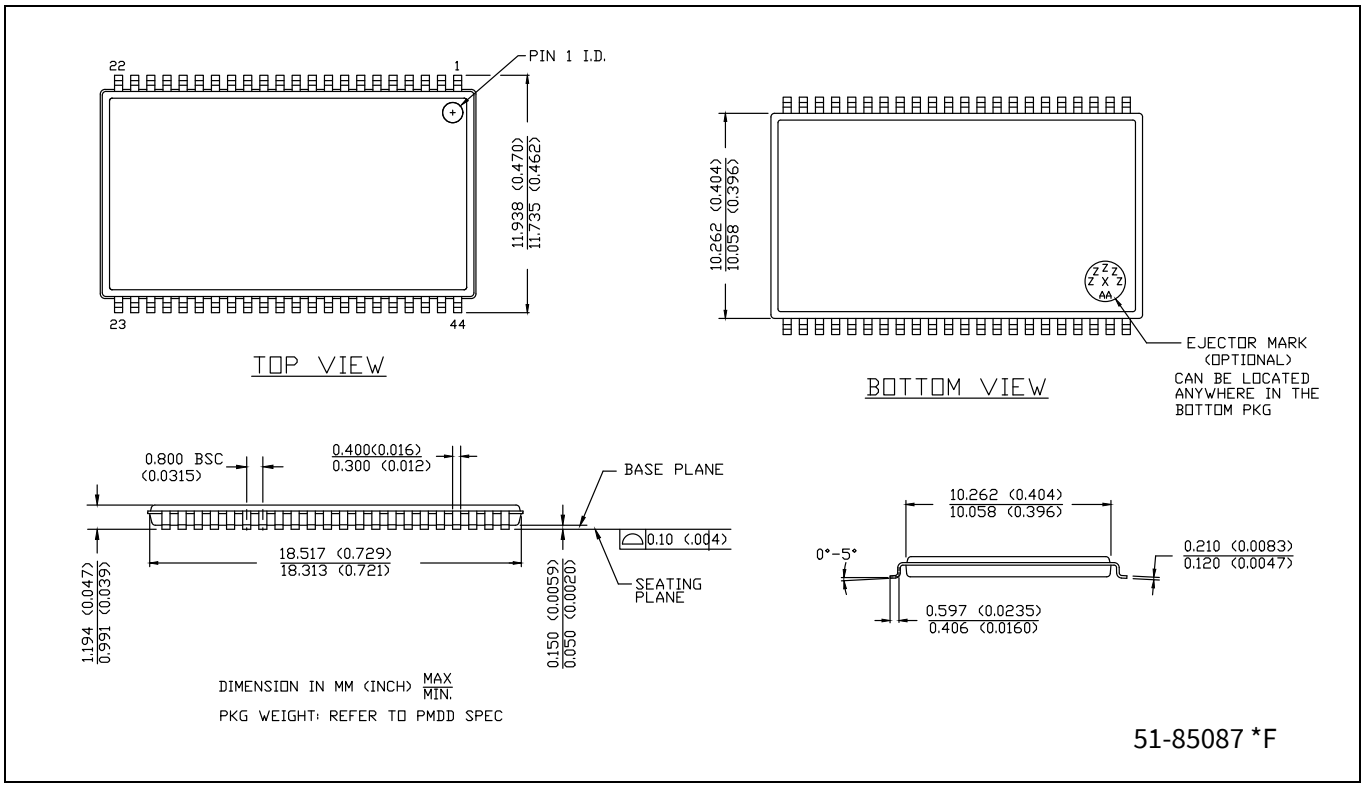


Figure 9 44-pin TSOP II (18.4 × 10.2 × 1.194 mm) Z54-II package outline, 51-85087

16 Acronyms

Table 12 Acronyms

Acronym	Description
$\overline{CE}$	chip enable
CMOS	complementary metal oxide semiconductor
I/O	input/output
$\overline{OE}$	output enable
SRAM	static random access memory
TSOP	thin small outline package
TTL	transistor-transistor logic
VFBGA	very fine-pitch ball grid array
$\overline{WE}$	write enable

17 Document conventions

17.1 Units of measure

Table 13 Unit of measure

Symbol	Unit of measure
°C	degree celsius
MHz	megahertz
µA	microampere
µs	microsecond
mA	milliampere
mm	millimeter
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Revision history

Document version	Date of release	Description of changes
**	2021-11-02	Initial release

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