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CY2XF33LXC533T

High-Performance LVDS Oscillator with Frequency Margining - Pin Control

Features

- Low jitter crystal oscillator (XO)
- Less than 1 ps typical RMS phase jitter
- Differential LVDS output
- Output frequency from 50 MHz to 690 MHz
- Two frequency margining control pins (FS0, FS1)
- Factory configured or field programmable
- Integrated phase-locked loop (PLL)
- Supply voltage: 3.3 V or 2.5 V
- Pb-free package: 5.0 × 3.2 mm LCC
- Commercial and industrial temperature ranges

Functional Description

The CY2XF33LXC533T is a high-performance and high-frequency crystal oscillator (XO). It uses a Cypress proprietary low-noise PLL to synthesize the frequency from an integrated crystal. The output frequency can be changed through two select pins, allowing easy frequency margin testing in applications.

The CY2XF33LXC533T is available as a factory configured device or as a field programmable device.

The FS0 and FS1 pins select between four different output frequencies, as shown in Table 2 on page 4. Frequency margining is a common application for this feature. One frequency is used for the standard operating mode of the device, while the other frequencies are available for margin testing, either during product development or in system manufacturing test.

Table 1. Frequency Select

FS1	FS0	Output Frequency
0	0	Frequency 0
0	1	Frequency 1
1	0	Frequency 2
1	1	Frequency 3

When changing the output frequency, the frequency transition is not guaranteed to be smooth. There can be frequency excursions beyond the start frequency and the new frequency. Glitches and runt pulses are possible, and time must be allowed for the PLL to relock.

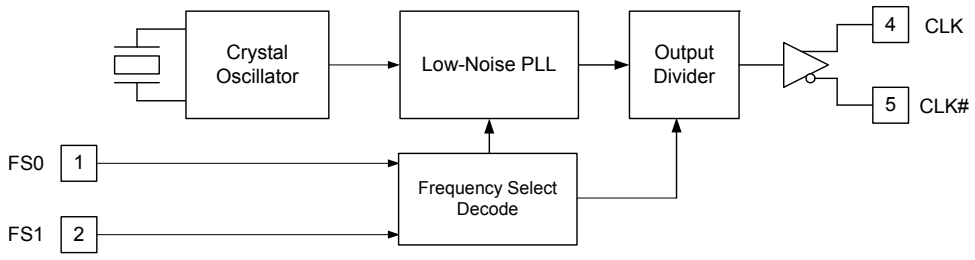
Programming Description

The CY2XF33LXC533T is a programmable device. Before being used in an application, it must be programmed with the output frequencies and other variables described in a later section. Two different device types are available, each with its own programming flow. They are described in the following sections.

Factory Configured CY2XF33LXC533T

For customers wanting ready-to-use devices, the CY2XF33LXC533T is available with no field programming required. All requests are submitted to the local Cypress Field Application Engineer (FAE) or sales representative. After the request is processed, the user receives a new part number, samples, and data sheet with the programmed values. This part number is used for additional sample requests and production orders.

Logic Block Diagram



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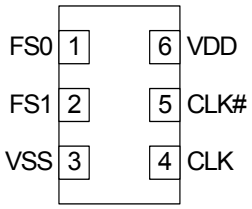
Pin Configuration

Figure 1. 6-pin Ceramic LCC pinout - CY2XF33LXC533T



Pin Definitions

Pin	Name	I/O Type	Description
1, 2	FS0, FS1	CMOS input	Frequency select
4, 5	CLK, CLK#	LVDS output	Differential output clock
6	VDD	Power	Supply voltage: 2.5 V or 3.3 V
3	VSS	Power	Ground

Application-Specific Factory Configurations

Part Number	VDD	FS1	FS0	Output Frequency	RMS Phase Jitter (Random)	
					Offset Range	Jitter (Typical)
CY2XF33LXC533T	3.3 V	0	0	350.00 MHz	12 kHz to 20 MHz	0.51 ps
		0	1	400.00 MHz		0.49 ps
		1	0	533.00 MHz		1.00 ps
		1	1	200.00 MHz		0.55 ps

Programming Variables

Output Frequencies

The CY2XF33LXC533T is programmed with up to four independent output frequencies, which are then selected using the FS0 and FS1 pins. The device can synthesize frequencies to a resolution of 1 part per million (ppm), but the actual accuracy of the output frequency is limited by the accuracy of the integrated reference crystal.

The CY2XF33LXC533T has an output frequency range of 50 MHz to 690 MHz, but the range is not continuous. The CY2XF33LXC533T cannot generate frequencies in the ranges of 521 MHz to 529 MHz and 596 MHz to 617 MHz.

Industrial versus Commercial Device Performance

Industrial and Commercial devices have different internal crystals. This has a potentially significant impact on performance levels for applications requiring the lowest possible phase noise. CyberClocks Online Software displays expected performance for both options.

Phase Noise versus Jitter Performance

In most cases, the device configuration for optimal phase noise performance is different from the device configuration for optimal cycle to cycle or period jitter. CyberClocks Online Software includes algorithms to optimize performance for either parameter.

Table 2. Device Programming Variables

Variable
Output frequency 0 (Power on default)
Output frequency 1
Output frequency 2
Output frequency 3
Optimization (phase noise or jitter)
Temperature range (Commercial or industrial)

Absolute Maximum Conditions

Parameter	Description	Condition	Min	Max	Unit
V_{DD}	Supply voltage	–	–0.5	4.4	V
V_{IN}[1]	Input voltage, DC	Relative to V_{SS}	–0.5	V_{DD} + 0.5	V
T_S	Temperature, storage	Non operating	–55	135	°C
T_J	Temperature, junction	–	–40	135	°C
ESD_{HBM}	ESD protection (human body model)	JEDEC STD 22-A114-B	2000	–	V
Θ_{JA}[2]	Thermal resistance, junction to ambient	0 m/s airflow	64		°C/W

Operating Conditions

Parameter	Description	Min	Typ	Max	Unit
V_{DD}	3.3 V supply voltage range	3.135	3.3	3.465	V
	2.5 V supply voltage range	2.375	2.5	2.625	V
T_{PU}	Power up time for V_{DD} to reach minimum specified voltage (power ramp is monotonic)	0.05	–	500	ms
T_A	Ambient temperature (commercial)	0	–	70	°C
	Ambient temperature (industrial)	–40	–	85	°C

Notes
1. The voltage on any input or I/O pin cannot exceed the power pin during power up.
2. Simulated. The board is derived from the JEDEC multilayer standard. It measures 76 × 114 × 1.6 mm and has 4-layers of copper (2/1/1/2 oz.). The internal layers are 100% copper planes, while the top and bottom layers have 50% metalization. No vias are included in the model.

DC Electrical Characteristics

Parameter	Description	Condition	Min	Typ	Max	Unit
I_{DD}[3]	Operating supply current	V_{DD} = 3.465 V, CLK = 150 MHz, output terminated	–	–	120	mA
		V_{DD} = 2.625 V, CLK = 150 MHz, output terminated	–	–	115	mA
V_{OD}	LVDS differential output voltage	V_{DD} = 3.3 V or 2.5 V, defined in Figure 3 on page 8 as terminated in Figure 2 on page 7	247	–	454	mV
ΔV_{OD}	Change in V_{OD} between complementary output states	V_{DD} = 3.3 V or 2.5 V, defined in Figure 3 on page 8 as terminated in Figure 2 on page 7	–	–	50	mV
V_{OS}	LVDS offset output voltage	V_{DD} = 3.3 V or 2.5 V, defined in Figure 4 on page 8 as terminated in Figure 2 on page 7	1.125	–	1.375	V
ΔV_{OS}	Change in V_{OS} between complementary output states	V_{DD} = 3.3 V or 2.5 V, R_{TERM} = 100 Ω between CLK and CLK#	–	–	50	mV
V_{IH}	Input high voltage	–	0.7 × V_{DD}	–	–	V
V_{IL}	Input Low voltage	–	–	–	0.3 × V_{DD}	V
I_{IH0}	Input high current, FS0 pin	Input = V_{DD}	–	–	115	µA
I_{IH1}	Input high current, FS1 pin	Input = V_{DD}	–	–	10	µA
I_{IL0}	Input low current, FS0 pin	Input = V_{SS}	–50	–	–	µA
I_{IL1}	Input low current, FS1 pin	Input = V_{SS}	–20	–	–	µA
C_{IN0}[4]	Input capacitance, FS0 pin	–	–	15	–	pF
C_{IN1}[4]	Input capacitance, FS1 pin	–	–	4	–	pF

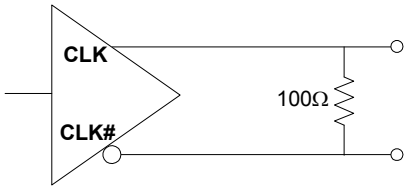
Notes
3. I_{DD} includes ~4 mA of current that is dissipated externally in the output termination resistors.
4. Not 100% tested, guaranteed by design and characterization.

AC Electrical Characteristics

Parameter [5]	Description	Condition	Min	Typ	Max	Unit
F_{OUT}	Output frequency [6]	–	50	–	690	MHz
FSC	Frequency stability, commercial devices [7]	T_A = 0 °C to 70 °C	–	–	±35	ppm
FSI	Frequency stability, industrial devices [7]	T_A = –40 °C to 85 °C	–	–	±55	ppm
AG	Aging, 10 years	–	–	–	±15	ppm
T_{DC}	Output duty cycle	F ≤ 450 MHz, measured at zero crossing	45	50	55	%
		F > 450 MHz, measured at zero crossing	40	50	60	%
T_R, T_F	Output rise and fall time	20% and 80% of full output swing	–	0.35	1.0	ns
T_{LOCK}	Startup time	Time for CLK to reach valid frequency measured from the time $V_{DD} = V_{DD(min)}$	–	–	5	ms
T_{LFS}	Re-lock time	Time for CLK to reach valid frequency from FS0 or FS1 pin change	–	–	1	ms
$T_{Jitter(\phi)}$	RMS phase jitter (random)	f_{OUT} = 106.25 MHz (12 kHz–20 MHz)	–	1	–	ps

Termination Circuits

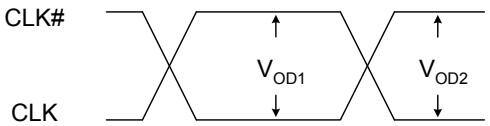
Figure 2. LVDS Termination



Notes
5. Not 100% tested, guaranteed by design and characterization.
6. This parameter is specified in CyberClocks Online software.
7. Frequency stability is the maximum variation in frequency from F_0. It includes initial accuracy, plus variation from temperature and supply voltage.

Switching Waveforms

Figure 3. Output Voltage Swing



$$\Delta V_{OD} = V_{OD1} - V_{OD2}$$

Figure 4. Output Offset Voltage

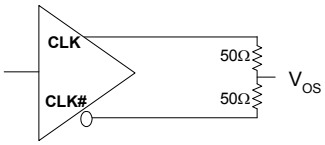
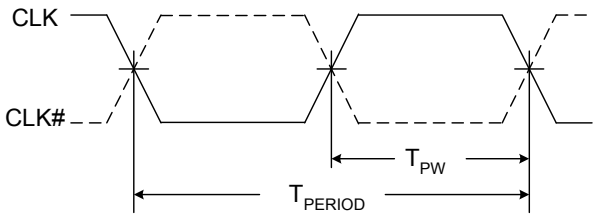


Figure 5. Output Duty Cycle Timing



$$T_{DC} = \frac{T_{PW}}{T_{PERIOD}}$$

Figure 6. Output Rise and Fall Time

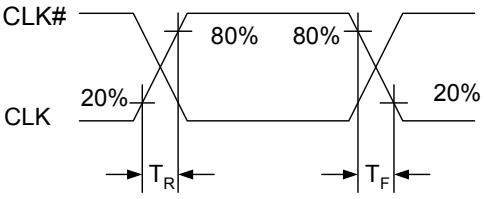
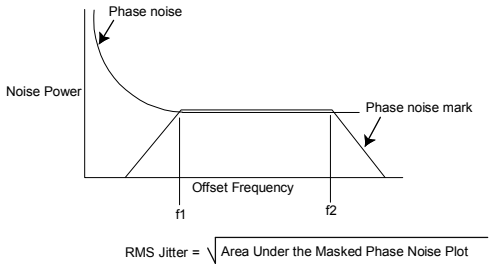


Figure 7. RMS Phase Jitter



Ordering Information

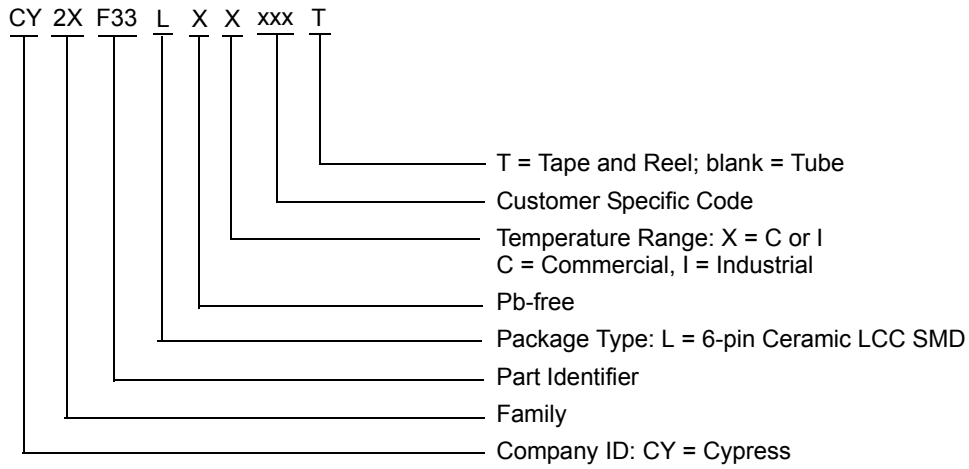
Part Number	Configuration	Package Description	Product Flow
Pb-free			
CY2XF33LXC533T [8]	Factory-configured	6-pin Ceramic LCC SMD - Tape and Reel	Commercial, 0 °C to 70 °C

Possible Configuration

Some product offerings are factory programmed customer specific devices with customized part numbers.The Possible Configurations table shows the available device types, but not complete part numbers. Contact your local Cypress FAE of Sales Representative for more information.

Part Number [9]	Configuration	Package Description	Product Flow
Pb-free			
CY2XF33LXCxxxT	Factory Configured	6-pin Ceramic LCC SMD - Tape and Reel	Commercial, 0 °c to 70 °C
CY2XF33LXIxxxT	Factory Configured	6-pin Ceramic LCC SMD - Tape and Reel	Industrial, –40 °C to 85 °C

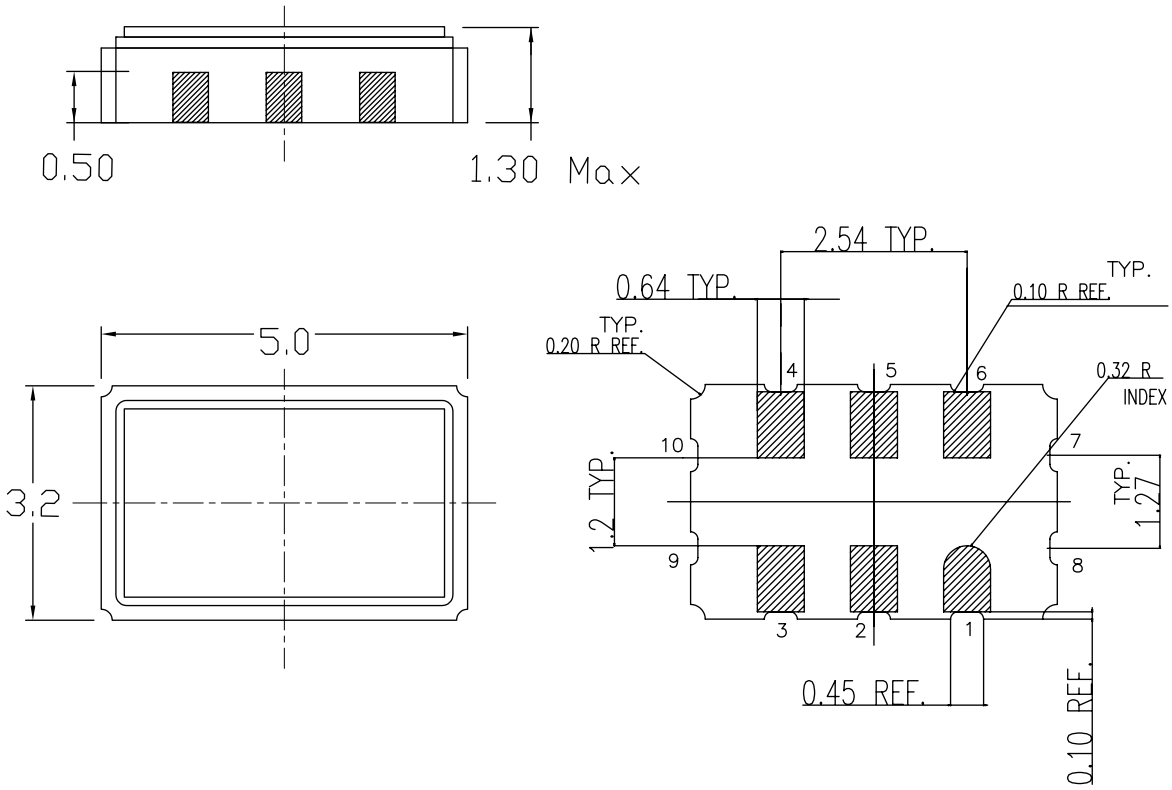
Ordering Code Definitions



Notes
8. Device configuration details are described in the Application-Specific Factory Configurations on page 4.
9. “xxx” is a factory assigned code that identifies the programming option.For more details, contact your local Cypress FAE or Sales Representative.

Package Drawings and Dimensions

Figure 8. 6-pin Ceramic LCC (5.0 × 3.2 × 1.3 mm) LZ06A Package Outline, 001-10044



Dimensions in mm
Kyocera dwg ref KD−VA6432−A
Package Weight ~ 0.12 grams

001-10044 *C

Acronyms

Acronym	Description
CMOS	complementary metal oxide semiconductor
ESD	electrostatic discharge
FAE	field application engineer
I/O	input/output
JEDEC	joint electron devices engineering council
LCC	leadless ceramic carrier
LVDS	low voltage differential signaling
PLL	phase locked loop
SMD	surface mount package

Document Conventions

Units of Measures

Symbol	Unit of Measure
°C	degree Celsius
kHz	kilohertz
MHz	megahertz
µA	microamperes
mA	milliamperes
mm	millimeter
ms	milliseconds
mV	millivolts
ns	nanoseconds
Ω	ohms
%	percent
pF	picofarads
ppm	parts per million
ps	picoseconds
V	volts
W	watts

Document History Page

Document Title: CY2XF33LXC533T, High-Performance LVDS Oscillator with Frequency Margining - Pin Control Document Number: 001-72034				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	3341593	BASH	08/30/2011	New data sheet. Reviewed by RAJA from Tech Support.
*A	4504048	XHT	09/19/2014	Updated Package Drawings and Dimensions: spec 001-10044 – Changed revision from *B to *C. Completing Sunset Review.
*B	5475564	XHT	10/14/2016	Updated to new template. Completing Sunset Review.
*C	5974188	AESATMP9	11/22/2017	Updated logo and copyright.

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