CY24242

Laser Printer System Frequency Synthesizer

Features

- Maximized EMI suppression using Cypress's Spread Spectrum technology
- Reduces measured EMI by as much as 10 dB
- Four skew-controlled copies of CPU output
- Four skew-controlled copies of SDRAM output
- One copy of 14.31818-MHz Reference output
- One copy of 48-MHz USB clock (not spread)
- Selectable SSFTG modulation width
- Available in 28-pin SSOP (209 mil)

Key Specifications

Supply Voltage:
VDDCORE: .....3.3 V ± 10%
VDDC: .....3.3 V ± 10% or 2.5 V ± 5%
VDDS: .....3.3 V ± 10% or 2.5 V ± 5%
VDDU: .....3.3 V ± 10% or 2.5 V ± 5%
CPU Clock Cycle to Cycle Jitter: .....250 ps
USBCLK Long term Jitter: ..... ± 500 ps
CPU0:3 Clock Skew: .....250 ps
CPU, SDRAM Output on Resistance: .....15 Ω
Logic inputs have 250 KΩ pull-up resistors

Pin Selectable Frequency [1]

FS1	FS0	CPU(0:3), SDRAM(0:3)	USBCLK
0	0	133.3 MHz	48 MHz
0	1	100 MHz	48 MHz
1	0	66.6 MHz	48 MHz
1	1	50 MHz	48 MHz

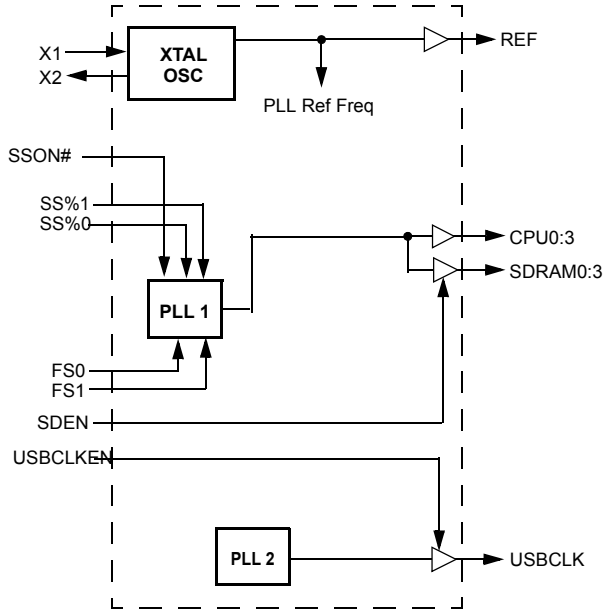
Spread Characteristics

SSON#	SS%1	SS%0	CPU(0:3), SDRAM(0:3)
0	0	0	–0.5%
0	0	1	–1.0%
0	1	0	–2.5%
0	1	1	–3.75%
1	0	0	0 (off)\
1	0	1	0 (off)
1	1	0	0 (off)
1	1	1	0 (off)

For a complete list of related documentation, click here.

Note
1. All clock output loaded with maximum lump capacitance test load specified in AC Electrical Characteristics section.

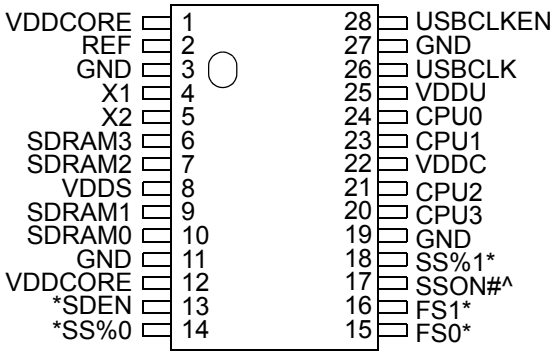
Block Diagram



Contents

Pin Configuration [2, 3] **4**
Pin Definitions **5**
Spread Spectrum Generator **6**
Absolute Maximum Ratings[4] **7**
DC Electrical Characteristics **7**
AC Electrical Characteristics **8**
CPU Clock Outputs, CPU0:3 8
SDRAM Clock Outputs, SDRAM0:3 9
REF Clock Outputs 10
USBCLK Clock Output 10
Ordering Information **11**
Ordering Code Definitions 11
Package Diagrams **12**
Acronyms **13**
Document Conventions **13**
Units of Measure 13
Document History Page **14**
Sales, Solutions, and Legal Information **15**
Worldwide Sales and Design Support 15
Products 15
PSoC® Solutions 15
Cypress Developer Community 15
Technical Support 15

Pin Configuration [2, 3]



Notes
2. Signals marked with [*] have internal pull-up resistors.
3. Signal marked with [^] has internal pull-down resistors.

Pin Definitions

Pin Name	Pin No.	Pin Type	Pin Description
CPU0:3	24, 23, 21, 20	O	CPU Clock Outputs: These four outputs run at a frequency set by FS0:1. The width of the Spread Spectrum Modulation is enabled by pin SSON#, and selected by pins SS%0:1.
SDRAM0:3	10, 9, 7, 6	O	SDRAM Outputs: These four SDRAM clock outputs run synchronously to the CPU clock. Modulation and frequency follow the CPU outputs.
FS0:1	15, 16	I	Frequency Selection Inputs: Selects CPU clock frequency as shown in Pin Selectable Frequency [1] on page 1.
SS%0:1	14, 18	I	Modulation Width Selection Inputs: These inputs select the width of the Spread Spectrum feature when it is enabled by SSON#.
USBCLK	26	O	USB Output: Timing signal running at 48.0080 MHz when a 14.31818-MHz frequency is provided as the reference. (167 ppm accuracy to 48 MHz, the output is equal to the reference times 57/17.)
SSON#	17	I	CPU Spread Spectrum Enable Input: When this pin is pulled LOW, outputs CPU0:3 and SDRAM0:3 will have the Spread Spectrum Feature enabled.
USBCLKEN	28	I	USB Disable Input: When this pin is pulled LOW, output USBCLK will be disabled to a LOW state.
REF	2	O	Reference Output: This output will be equal in frequency to the reference signal provided at X1/X2.
SDEN	13	I	SDRAM Bank Disable Input: When this pin is pulled LOW, outputs SDRAM0:3 will be disabled to a LOW state.
X1	4	I	Crystal Connection or External Reference Frequency Input: Connect to either a 14.318-MHz crystal or other reference signal.
X2	5	I	Crystal Connection: An input connection for an external 14.318-MHz crystal. If using an external reference, this pin must be left unconnected.
VDDCORE	1, 12	P	Power Connection: Core Power supply. Connect to 3.3 V supply.
VDDU	25	P	Power Connection: Power supply for the USB output. Connect to 3.3 V or 2.5 V supply.
VDDC	22	P	Power Connection: Power supply for the CPU outputs. Connect to 3.3 V or 2.5 V supply.
VDDS	8	P	Power Connection: Power supply for the SDRAM outputs. Connect to 3.3 V or 2.5 V supply.
GND	3, 11, 19, 27	G	Ground Connections: Connect all ground pins to the common system ground plane.

Spread Spectrum Generator

The device generates a clock that is frequency modulated in order to increase the bandwidth that it occupies. By increasing the bandwidth of the fundamental and its harmonics, the amplitudes of the radiated electromagnetic emissions are reduced. This effect is depicted in Figure 1.

As shown in Figure 1, a harmonic of a modulated clock has a much lower amplitude than that of an unmodulated signal. The reduction in amplitude is dependent on the harmonic number and the frequency deviation or spread. The equation for the reduction is

$$dB = 6.5 + 9*\log_{10}(P) + 9*\log_{10}(F)$$

Where *P* is the percentage of deviation and *F* is the frequency in MHz where the reduction is measured.

The output clock is modulated with a waveform depicted in Figure 2. This waveform, as discussed in “Spread Spectrum Clock Generation for the Reduction of Radiated Emissions” by Bush, Fessler, and Hardin, produces the maximum reduction in the amplitude of radiated electromagnetic emissions. The deviation selected for this chip is ±0.5% of the center frequency. Figure 2 details the Cypress spreading pattern. Cypress does offer options with more spread and greater EMI reduction. Contact your local Sales representative for details on these devices.

Spread Spectrum clocking is activated or deactivated by selecting the appropriate values for bits 1–0 in data byte 0 of the SMBus data stream.

Figure 1. Clock Harmonic with and without SSCG Modulation Frequency Domain Representation

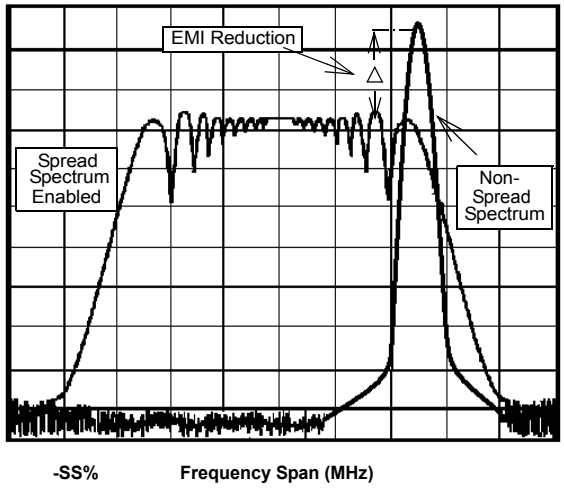
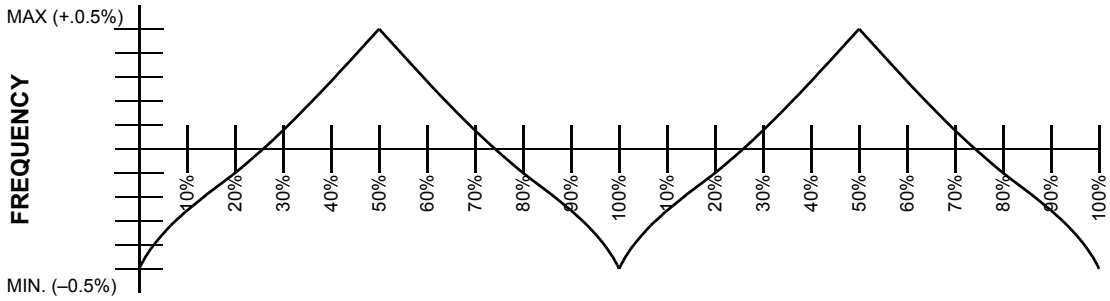


Figure 2. Typical Modulation Profile



Absolute Maximum Ratings[4]

Stresses greater than those listed in this table may cause permanent damage to the device. These represent a stress rating only. Operation of the device at these or any other conditions above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability.

Parameter	Description	Rating	Unit
V_{DD}, V_{IN}	Voltage on any pin with respect to GND	–0.5 to +7.0	V
T_{STG}	Storage Temperature	–65 to +150	°C
T_A	Operating Temperature	–55 to +125	°C
T_B	Ambient Temperature under Bias	0 to +70	°C
ESD_{PROT}	Input ESD Protection	2 (min.)	kV

DC Electrical Characteristics

T_A = 0°C to +70°C, V_{DDQ3} = 3.3 V ± 10%

Parameter	Description	Test Condition	Min	Typ	Max	Unit
Supply Current						
I_{DDQ3}	Supply Current (3.3 V)	CPUCLK = 100 MHz Outputs Loaded[4]	–	–	400	mA
I_{DDQ2}	Supply Current (2.5 V)	CPUCLK = 100 MHz Outputs Loaded[4]	–	–	400	mA
Logic Inputs[5]						
V_{IL}	Input Low Voltage	–	GND – 3	–	0.8	V
V_{IH}	Input High Voltage	–	2.0	–	V_{DD} +.3	V
I_{IL}	Input Low Current[6]	–	–	–	–25	µA
I_{IH}	Input High Current[6]	–	–	–	10	µA
Crystal Oscillator						
V_{TH}	X1 Input Threshold Voltage[7]	–	–	1.5	–	V
C_{LOAD}	Load Capacitance, Imposed on External Crystal[8]	–	–	14	–	pF
$C_{IN,X1}$	X1 Input Capacitance[9]	Pin X2 unconnected	–	28	–	pF
Pin Capacitance/Inductance						
C_{IN}	Input Pin Capacitance	Except X1 and X2	–	–	5	pF
C_{OUT}	Output Pin Capacitance	–	–	–	6	pF
L_{IN}	Input Pin Inductance	–	–	–	7	nH

Notes
4. Multiple Supplies: The voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.
5. CY24242 logic inputs have internal pull-up resistors.
6. X1 input threshold voltage (typical) is $V_{DDQ}/2$.
7. All clock output loaded with maximum lump capacitance test load specified in AC Electrical Characteristics section.
8. The CY24242 contains an internal crystal load capacitor between pin X1 and ground and another between pin X2 and ground. Total load placed on crystal is 14 pF; this includes typical stray capacitance of short PCB traces to crystal.
9. X1 input capacitance is applicable when driving X1 with an external clock source (X2 is left unconnected).

AC Electrical Characteristics

T_A = 0 °C to +70 °C, V_{DD} = V_{DDQ3} = 3.3 V ± 10%, f_{XTL} = 14.31818 MHz

AC clock parameters are tested and guaranteed over stated operating conditions using the stated lump capacitive load at the clock output.

CPU Clock Outputs, CPU0:3

(Lump Capacitance Test Load = 20 pF, V_{DDC} = 3.3 V)

Parameter	Description	Test Condition/Comments	CPU = 66 MHz			CPU = 100 MHz			Unit
			Min	Typ	Max	Min	Typ	Max	
t_P	Period	Measured on rising edge at 1.5 V	15	–	15.5	10	–	10.5	ns
t_H	High Time	Duration of clock cycle above 2.4 V	5.2	–	–	3.0	–	–	ns
t_L	Low Time	Duration of clock cycle below 0.4 V	5	–	–	2.8	–	–	ns
t_R	Output Rise Edge Rate	Measured from 0.4 V to 2.4 V	0.4	–	3.2	0.4	–	3.2	V/ns
t_F	Output Fall Edge Rate	Measured from 2.4 V to 0.4 V	0.4	–	3.2	0.4	–	3.2	V/ns
t_D	Duty Cycle	Measured on rising and falling edge at 1.5 V	45	–	55	45	–	55	%
t_{JC}	Jitter, Cycle-to-Cycle	Measured on rising edge at 1.5 V. Maximum difference of cycle time between two adjacent cycles.	–	–	250	–	–	250	ps
t_{SK}	Output Skew	Measured on rising edge at 1.5 V	–	–	250	–	–	250	ps
f_{ST}	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.	–	–	3	–	–	3	ms
Z_o	AC Output Impedance	Average value during switching transition. Used for determining series termination value.	–	20	–	–	20	–	Ω

SDRAM Clock Outputs, SDRAM0:3

(Lump Capacitance Test Load = 30 pF, V_{DDC} = 3.3 V)

Parameter	Description	Test Condition/Comments	CPU = 66 MHz			CPU = 100 MHz			Unit
			Min	Typ	Max	Min	Typ	Max	
t_P	Period	Measured on rising edge at 1.5 V	15	–	15.5	10	–	10.5	ns
t_H	High Time	Duration of clock cycle above 2.4 V	5.2	–	–	3.0	–	–	ns
t_L	Low Time	Duration of clock cycle below 0.4 V	5	–	–	2.8	–	–	ns
t_R	Output Rise Edge Rate	Measured from 0.4 V to 2.4 V	0.4	–	3.2	0.4	–	3.2	V/ns
t_F	Output Fall Edge Rate	Measured from 2.4 V to 0.4 V	0.4	–	3.2	0.4	–	3.2	V/ns
t_D	Duty Cycle	Measured on rising and falling edge at 1.5 V	45	–	55	45	–	55	%
t_{JC}	Jitter, Cycle-to-Cycle	Measured on rising edge at 1.5 V. Maximum difference of cycle time between two adjacent cycles.	–	–	250	–	–	250	ps
t_{SK}	Output Skew	Measured on rising edge at 1.5 V		100	300		100	350	ps
t_{SK}	CPU to SDRAM Clock Skew	Covers all CPU/SDRAM outputs. Measured on rising edge at 1.5 V.	–	–	350	–	–	350	ps
f_{ST}	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.	–	–	3	–	–	3	ms
Z_o	AC Output Impedance	Average value during switching transition. Used for determining series termination value.	–	20	–	–	20	–	Ω

REF Clock Outputs

(Lump Capacitance Test Load = 20 pF)

Parameter	Description	Test Condition/Comments	CPU = 66/100MHz			Unit
			Min	Typ	Max	
f	Frequency, Actual	Frequency equal to the reference provided at pins X1, X2		14.318		MHz
t_R	Output Rise Edge Rate		0.5	–	2	V/ns
t_F	Output Fall Edge Rate		0.5	–	2	V/ns
t_D	Duty Cycle	Measured on rising and falling edge at 1.5 V	45	–	55	%
f_{ST}	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.	–	–	3	ms
Z_o	AC Output Impedance	Average value during switching transition. Used for determining series termination value.	–	40	–	Ω

USBCLK Clock Output

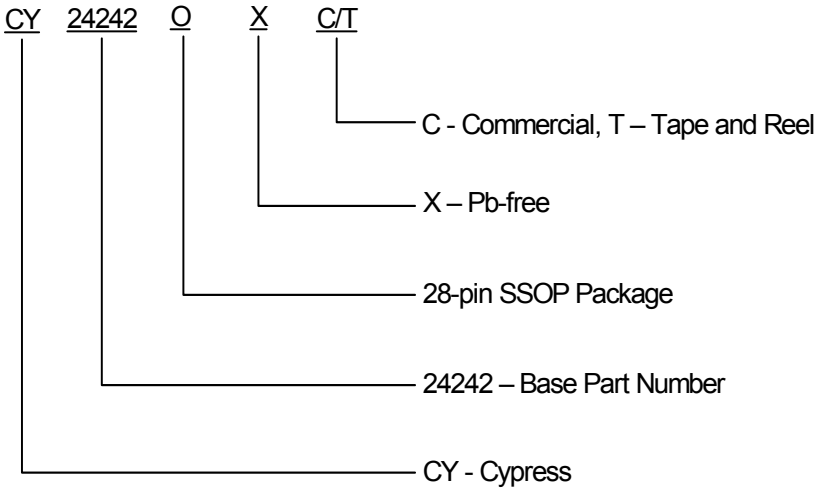
(Lump Capacitance Test Load = 20 pF, V_{DDC} = 3.3 V)

Parameter	Description	Test Condition/Comments	CPU = 66/100 MHz			Unit
			Min	Typ	Max	
t_R	Output Rise Edge Rate	–	0.5	–	2	V/ns
t_F	Output Fall Edge Rate	–	0.5	–	2	V/ns
t_D	Duty Cycle	Measured on rising and falling edge at 1.5 V	45	–	55	%
t_{JL}	Jitter, Long term	Measured on rising edge at 1.5 V. Maximum difference of cycle time between two adjacent cycles.	–	–	500	
t_{JC}	Jitter, Cycle-to-Cycle	Measured on rising edge at 1.5 V. Maximum difference of cycle time between two adjacent cycles.	–	–	400	
f_{ST}	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.	–	–	3	ms
Z_o	AC Output Impedance	Average value during switching transition. Used for determining series termination value.	–	40	–	Ω

Ordering Information

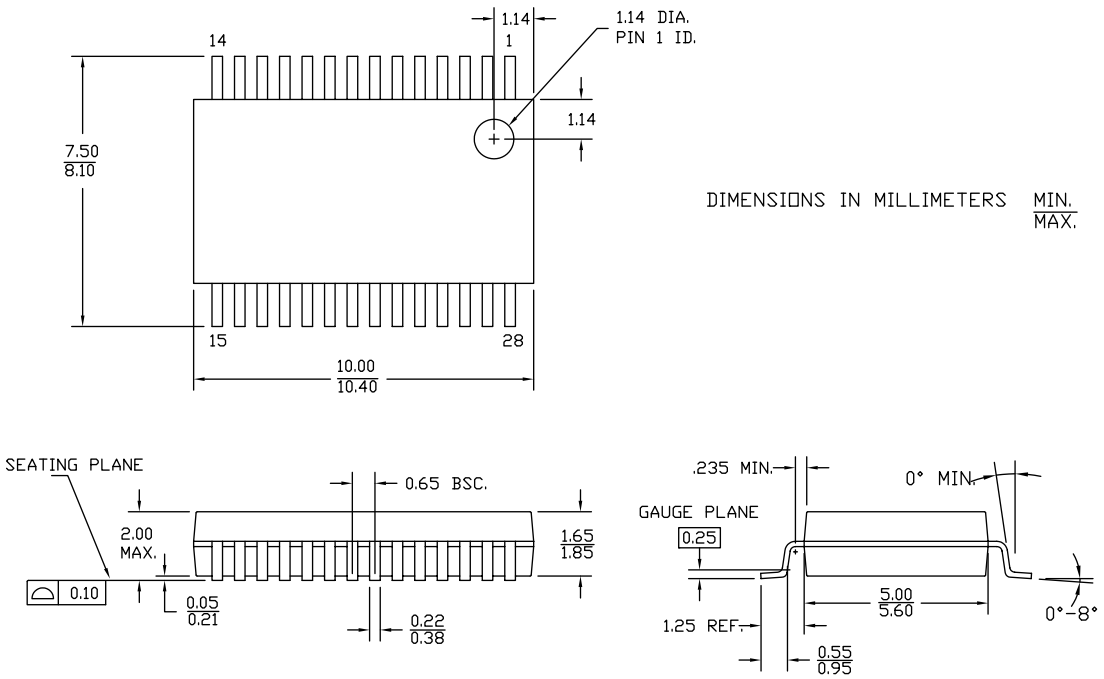
Ordering Code	Package Type	Temperature Grade
Standard		
Pb-free		
CY24242OXC	28-pin SSOP (300 Mils)	C (Commercial 0 °C–70 °C)
CY24242OXCT	28-pin SSOP (300 Mils) – Tape and Reel	C (Commercial 0 °C–70 °C)

Ordering Code Definitions



Package Diagrams

Figure 3. 28-pin SSOP (210 Mils) Package Outline, 51-85079



51-85079 *E

Acronyms

Acronym	Description
CCJ	Cycle to Cycle Jitter
DNU	Do Not Use
DUT	Device Under Test
EMI	Electromagnetic Interference
ESD	Electrostatic Discharge
FAE	Field Application Engineer
FS	Frequency Select
LTJ	Long Term Jitter
PJ	Period Jitter
PLL	Phase Locked Loop

Document Conventions

Units of Measure

Symbol	Unit of Measure
A	ampere
°C	degrees Celsius
dB	decibel
fF	femtofarad
Kbit	1024 bits
KB	1024 bytes
KHz	kilohertz
KΩ	kilohm
MHz	megahertz
MΩ	megaohm
mA	milliampere
ms	millisecond
mV	millivolt
nA	nanoampere
ns	nanosecond
nV	nanovolt
Ω	ohm
ppm	parts per million
pA	picoampere
pF	picofarad
ps	picosecond
V	volt
W	watt

Document History Page

Document Title: CY24242, Laser Printer System Frequency Synthesizer Document Number: 38-07268				
Rev.	**ECN No.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	110533	10/08/01	SZV	Change from Spec number: 38-01133 to 38-07268
*A	122866	12/20/02	RBI	Added power-up requirements to maximum ratings information.
*B	310556	See ECN	RGL	Added Pb-free devices
*C	2896383	03/19/10	CXQ	Updated ordering information. Removed part numbers CY24242PVC and CY24242PVCT Updated package diagram Updated copyright section
*D	2915602	04/16/10	SHEA	Minor ECN to correct title in the document history page
*E	3188105	03/04/2011	CXQ	Added Ordering Code Definitions. Added Acronyms and Units of Measure.
*F	4321602	03/26/2014	CINM	Updated Package Diagrams: spec 51-85079 – Changed revision from *D to *E. Updated in new template. Completing Sunset Review.
*G	4581659	11/28/2014	AJU	Added related documentation hyperlink in page 1.

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

Products

Automotive	cypress.com/go/automotive
Clocks & Buffers	cypress.com/go/clocks
Interface	cypress.com/go/interface
Lighting & Power Control	cypress.com/go/powerpsoc cypress.com/go/plc
Memory	cypress.com/go/memory
PSoC	cypress.com/go/psoc
Touch Sensing	cypress.com/go/touch
USB Controllers	cypress.com/go/USB
Wireless/RF	cypress.com/go/wireless

PSoC® Solutions

psoc.cypress.com/solutions

PSoC 1 | PSoC 3 | PSoC 4 | PSoC 5LP

Cypress Developer Community

Community | Forums | Blogs | Video | Training

Technical Support

cypress.com/go/support

© Cypress Semiconductor Corporation, 2001-2014. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress product. Nor does it convey or imply any license under patent or other rights. Cypress products are not warranted nor intended to be used for medical, life support, life saving, critical control or safety applications, unless pursuant to an express written agreement with Cypress. Furthermore, Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Any Source Code (software and/or firmware) is owned by Cypress Semiconductor Corporation (Cypress) and is protected by and subject to worldwide patent protection (United States and foreign), United States copyright laws and international treaty provisions. Cypress hereby grants to licensee a personal, non-exclusive, non-transferable license to copy, use, modify, create derivative works of, and compile the Cypress Source Code and derivative works for the sole purpose of creating custom software and or firmware in support of licensee product to be used only in conjunction with a Cypress integrated circuit as specified in the applicable agreement. Any reproduction, modification, translation, compilation, or representation of this Source Code except as specified above is prohibited without the express written permission of Cypress.

Disclaimer: CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Cypress reserves the right to make changes without further notice to the materials described herein. Cypress does not assume any liability arising out of the application or use of any product or circuit described herein. Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress' product in a life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Use may be limited by and subject to the applicable Cypress software license agreement.

All products and company names mentioned in this document may be the trademarks of their respective holders.