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CY241V08A-01,04
CY241V8A-01

MPEG Clock Generator with VCXO

Features

- Integrated Phase-Locked Loop (PLL)
- Low Jitter, High Accuracy Outputs
- VCXO with Analog Adjust
- 3.3 V Operation
- Compatible with MK3727 (–1, –4)
- Application compatibility for a wide variety of Designs
- Enables Design compatibility
- Lower Drive Strength settings (CY241V08A–04)

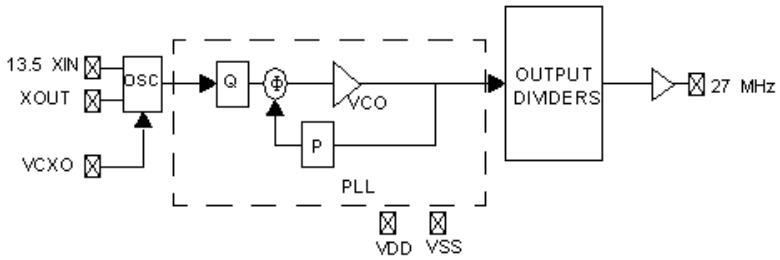
Benefits

- Digital VCXO control
- Second source for existing designs
- Highest performance PLL tailored for multimedia applications
- Meets critical timing requirements in complex system designs

Functional Description

For a complete list of related documentation, click here.

CY241V08A-01, -04 Logic Block Diagram



Selector Guide

Part Number	Outputs	Input Frequency Range	Output Frequencies	VCXO Control Curve	Other Features
CY241V08A-01	1	13.5 MHz pullable crystal input according to Cypress specification	1 copy of 27 MHz	linear	Compatible with MK3727
CY241V08A-04	1	13.5 MHz pullable crystal input according to Cypress specification	1 copy of 27 MHz	linear	Same as CY241V08A-01 except lower drive strength settings

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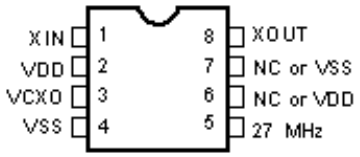
Pin Configurations

Figure 1. 8-pin SOIC pinout

CY241V08A-01, -04



Pin Descriptions

Name	Pin Number	Description
XIN	1	Reference crystal input
VDD	2	Voltage supply
VCXO	3	Input analog control for VCXO
VSS	4	Ground
27 MHz	5	27 MHz clock output
NC/VDD	6	No connect or voltage supply
NC/VSS	7	No connect or ground
XOUT	8	Reference crystal output

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Absolute Maximum Conditions

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Supply Voltage (V_{DD}) ..... –0.5 to +7.0 V

DC Input Voltage ..... –0.5 V to V_{DD} + 0.5 V

Storage Temperature (Non-condensing) ..... –55 °C to +125 °C

Junction Temperature ..... –40 °C to +125 °C

Data Retention at Tj = 125 °C ..... > 10 years

Package Power Dissipation ..... 350 mW

ESD (Human Body Model) MIL-STD-883 ..... > 2000 V

Pullable Crystal Specifications

Parameter [1]	Description	Comments	Min	Typ	Max	Unit
F_{NOM}	Nominal crystal frequency	Parallel resonance, fundamental mode, AT cut	–	13.5	–	MHz
C_{LNOM}	Nominal load capacitance		–	14	–	pF
R_1	Equivalent series resistance (ESR)	Fundamental mode	–	–	25	Ω
R_3/R_1	Ratio of third overtone mode ESR to fundamental mode ESR	Ratio used because typical R_1 values are much less than the maximum spec	3	–	–	–
DL	Crystal drive level	No external series resistor assumed	150	–	–	µW
F_{3SEPHI}	Third overtone separation from 3 × F_{NOM}	High side	300	–	–	ppm
F_{3SEPLO}	Third overtone separation from 3 × F_{NOM}	Low side	–	–	–150	ppm
C_0	Crystal shunt capacitance		–	–	7	pF
C_0/C_1	Ratio of shunt to motional capacitance		180	–	250	–
C_1	Crystal motional capacitance		14.4	18	21.6	fF

Recommended Operating Conditions

Parameter	Description	Min	Typ	Max	Unit
V_{DD}	Operating Voltage	3.135	3.3	3.465	V
T_A	Ambient Temperature	0	–	70	°C
C_{LOAD}	Maximum Load Capacitance	–	–	15	pF
t_{PU}	Power up time for all VDD pins to reach minimum specified voltage (power ramps must be monotonic)	0.05	–	500	ms

Note

1. Crystals that meet this specification include: Ecliptek ECX-5788-13.500M, Siward XTL001050A-13.5-14-400, Raltron A-13.500-14-CL, PDI HA13500XFSA14XC.

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DC Electrical Specifications

Parameter	Name	Description	Min	Typ	Max	Unit
I_{OH}	Output HIGH Current	$V_{OH} = V_{DD} – 0.5$ V, $V_{DD} = 3.3$ V	12	24	–	mA
I_{OL}	Output LOW Current	$V_{OL} = 0.5$ V, $V_{DD} = 3.3$ V	12	24	–	mA
C_{IN}	Input Capacitance	Except XIN, XOUT pins	–	–	7	pF
V_{VCXO}	VCXO Input Range		0	–	V_{DD}	V
$f_{\Delta XO}$[2]	VCXO Pullability Range	Low Side	–	–	–115	ppm
		High Side	115	–	–	ppm
I_{VDD}	Supply Current		–	30	35	mA

Thermal Resistance

Parameter [3]	Description	Test Conditions	8-pin SOIC	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, according to EIA/JESD51.	135	°C/W
Θ_{JC}	Thermal resistance (junction to case)		53	°C/W

AC Electrical Specifications

($V_{DD} = 3.3$ V)

Parameter [4]	Name	Description	Min	Typ	Max	Unit
DC	Output Duty Cycle	Duty Cycle is defined in Figure 3, 50% of V_{DD}	45	50	55	%
ER_{OR}	Rising Edge Rate -01	Output Clock Edge Rate, Measured from 20% to 80% of V_{DD}, C_{LOAD} = 15 pF See Figure 4.	0.8	1.4	–	V/ns
ER_{OF}	Falling Edge Rate -01	Output Clock Edge Rate, Measured from 80% to 20% of V_{DD}, C_{LOAD} = 15 pF, See Figure 4.	0.8	1.4	–	V/ns
ER_{OR}	Rising Edge Rate -04	Output Clock Edge Rate, Measured from 20% to 80% of V_{DD}, C_{LOAD} = 15 pF, See Figure 4.	0.7	1.1	–	V/ns
ER_{OF}	Falling Edge Rate -04	Output Clock Edge Rate, Measured from 80% to 20% of V_{DD}, C_{LOAD} = 15 pF, See Figure 4.	0.7	1.1	–	V/ns
t_9	Clock Jitter	Peak-to-peak period jitter	–	–	100	ps
t_{10}	PLL Lock Time		–	–	3	ms

Notes
2. –115/+115 ppm assumes 2.5 pF of additional board level load capacitance. This range will be shifted down with more board capacitance or shifted up with less board capacitance.
3. Tested initially and after any design or process change that may affect these parameters.
4. Not 100% tested.

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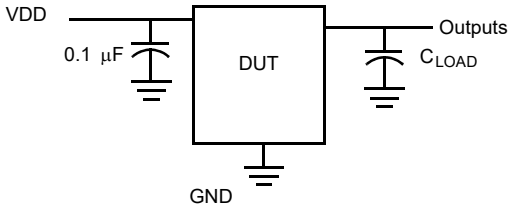
Test and Measurement Setup

Figure 2. Test and Measurement Setup



Voltage and Timing Definitions

Figure 3. Duty Cycle Definition

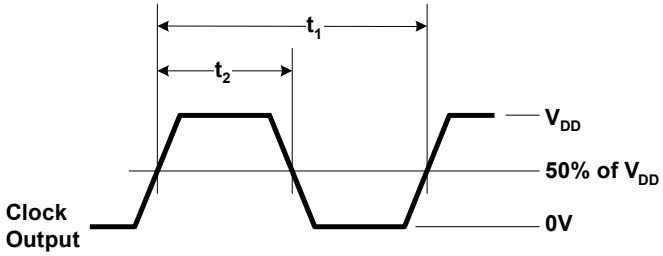
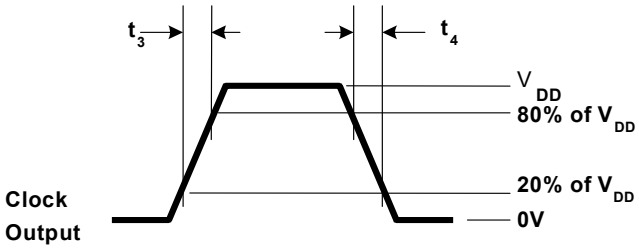


Figure 4. ER = (0.6 x V_{DD})/t_3, EF = (0.6 x V_{DD})/t_4



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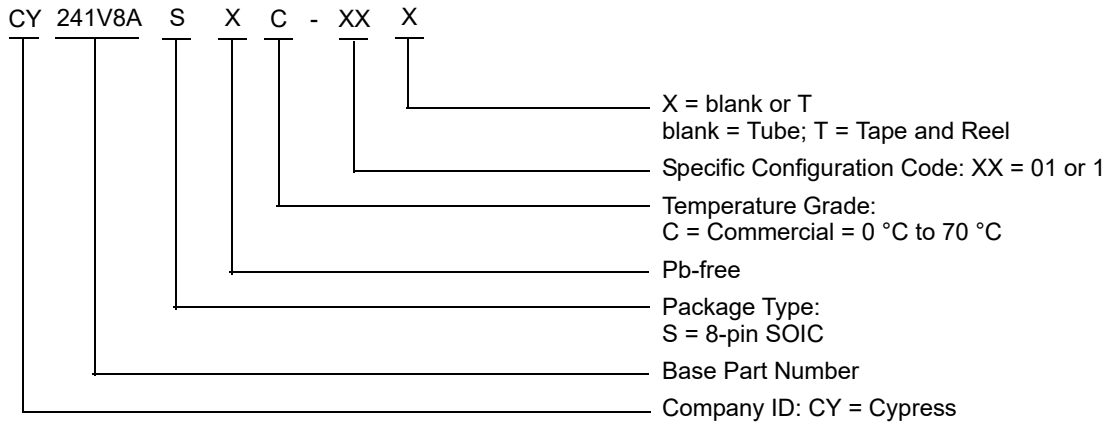
Ordering Information

Ordering Code	Package Type	Operating Range	Operating Voltage	Features
Pure Sn				
CY241V8ASXC-1S	8-pin SOIC	Commercial	3.3 V	Linear VCXO control curve

Ordering Code Definitions



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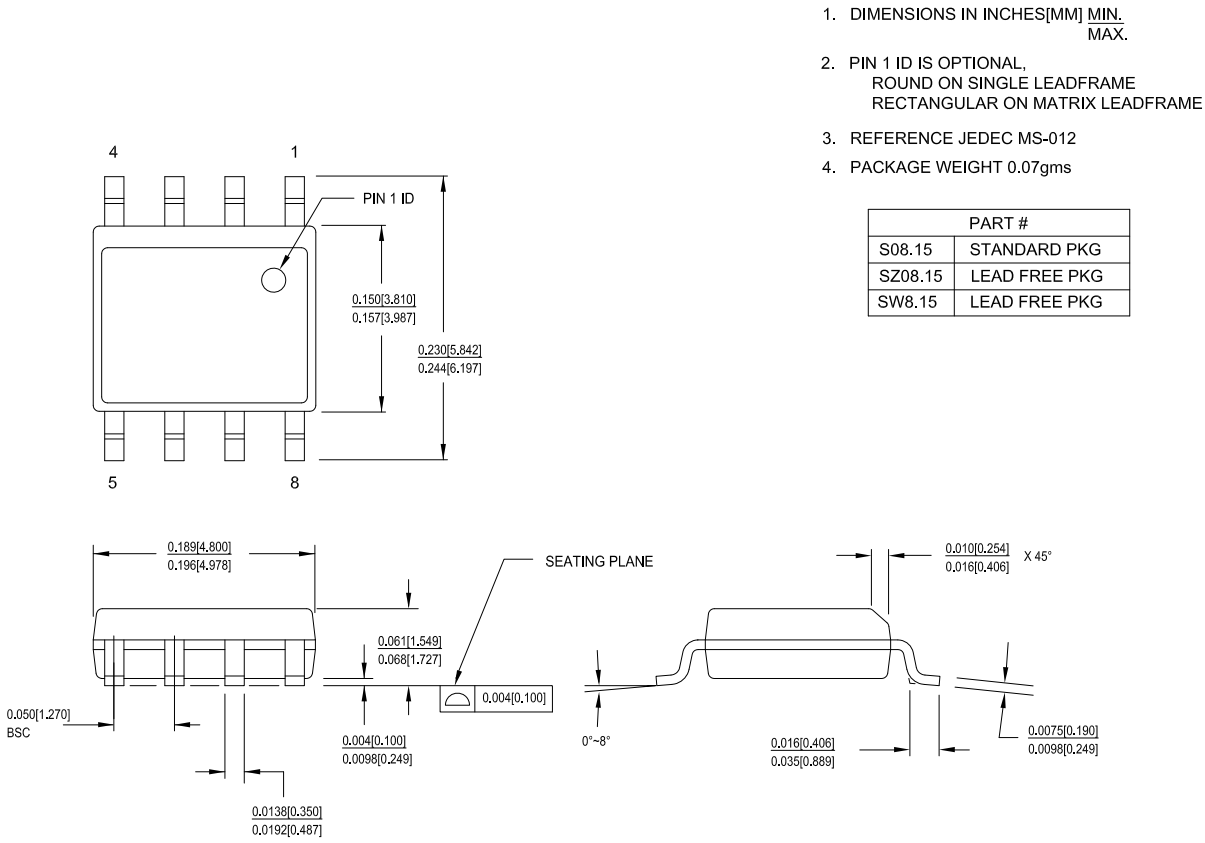
Package Diagrams

Figure 5. 8-pin SOIC (150 Mils) S0815/SZ815/SW815 Package Outline, 51-85066



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Acronyms

Acronym	Description
ESD	Electrostatic Discharge
ESR	Equivalent Series Resistance
PLL	Phase Locked Loop
SOIC	Small Outline Integrated Circuit
VCXO	Voltage Controlled Crystal Oscillator

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
fF	femtofarad
MHz	megahertz
µF	microfarad
µW	microwatt
mA	milliampere
ms	millisecond
mW	milliwatt
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
ppm	parts per million
ps	picosecond
V	volt

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Document History Page

Document Title: CY241V08A-01,04/CY241V8A-01, MPEG Clock Generator with VCXO Document Number: 38-07656			
Rev.	**ECN No.**	**Submission Date**	**Description of Change**
**	214069	03/26/2004	New data sheet.
*A	220404	04/22/2004	Minor Change: Post to external web.
*B	393122	08/22/2005	Updated Document Title to read as “CY241V08A-01,04/CY241V8A-01, MPEG Clock Generator with VCXO”. Updated Ordering Information: Updated part numbers.
*C	414184	12/14/2005	Minor Change: Updated Benefits: Deleted unnecessary text.
*D	455059	04/21/2006	Updated Ordering Information: Updated part numbers. Updated to new template. Post to internal spec system.
*E	2759384	09/02/2009	Updated to new template. Post to external web.
*F	2897423	03/22/2010	Updated Ordering Information: Updated part numbers. Updated Package Diagrams: spec 51-85066 – Changed revision from *C to *D. Updated to new template. Completing Sunset Review.
*G	4009177	05/23/2013	Updated Ordering Information: No change in part numbers. Added Ordering Code Definitions. Updated Package Diagrams: spec 51-85066 – Changed revision from *D to *F. Added Acronyms and Units of Measure. Updated to new template. Completing Sunset Review.
*H	4580603	11/26/2014	Updated Functional Description: Added “For a complete list of related documentation, click here.” at the end. Updated Ordering Information: Updated part numbers.
*I	5267358	05/11/2016	Added Thermal Resistance. Updated Package Diagrams: spec 51-85066 – Changed revision from *F to *H. Updated to new template. Completing Sunset Review.
*J	6073305	02/16/2018	Updated Package Diagrams: spec 51-85066 – Changed revision from *H to *I. Updated to new template.
*K	6903402	06/22/2020	Added watermark “Not Recommended for New Designs” across the document. Updated to new template. Completing Sunset Review.

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